

# Compal Confidential

## PAWF5/F6 M/B Schematics Document

### Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-02-03

REV: 0.1

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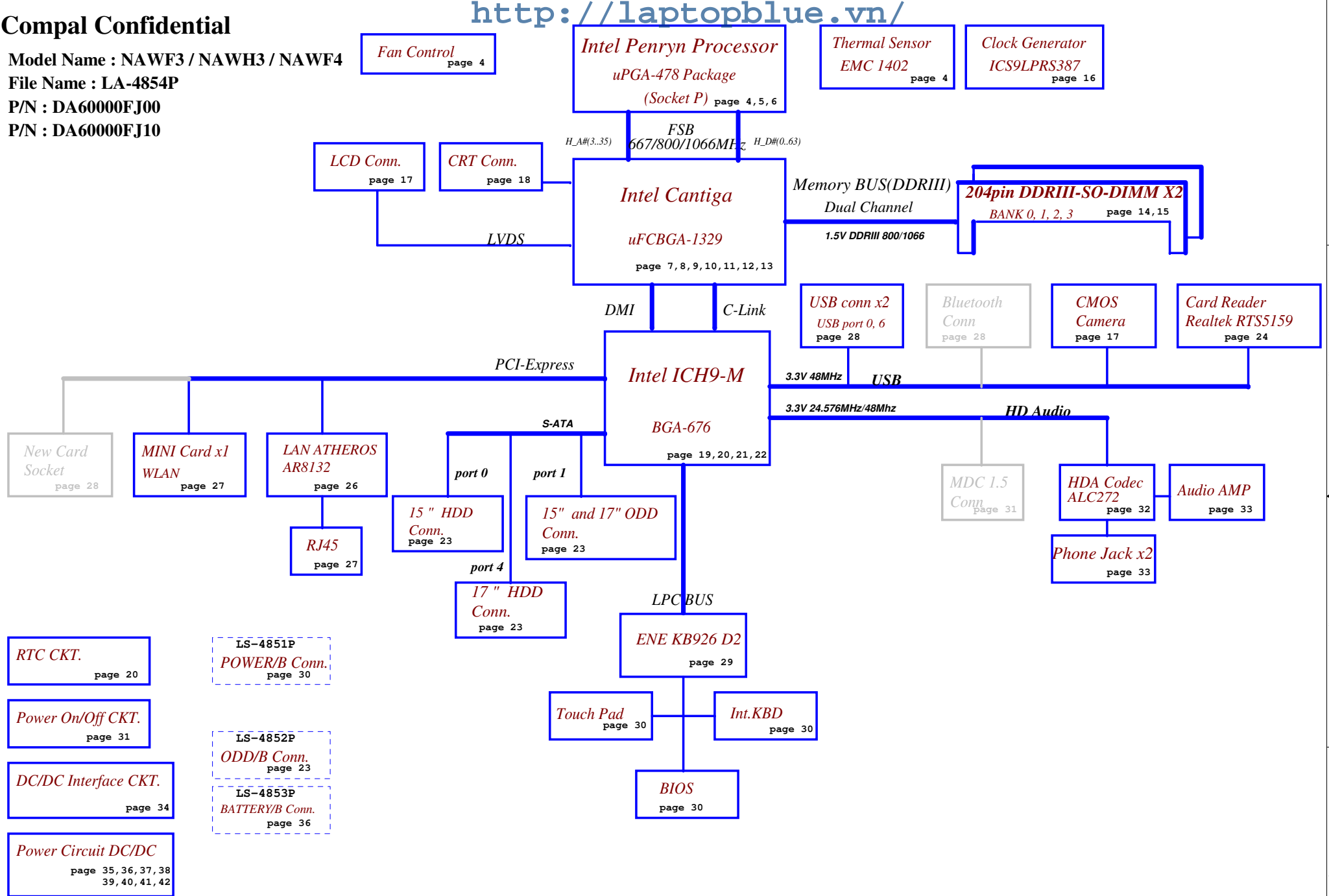
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Model Name : NAWF3 / NAWH3 / NAWF4

File Name : LA-4854P

P/N : DA60000FJ00

P/N : DA60000FJ10



## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

## EC SM Bus2 address

## ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	0.1 (PVT)
6	
7	

## BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
PAWF5	F5@
PAWF7	F7@
8114	8114@
8132	8132@

## PCIE table

PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

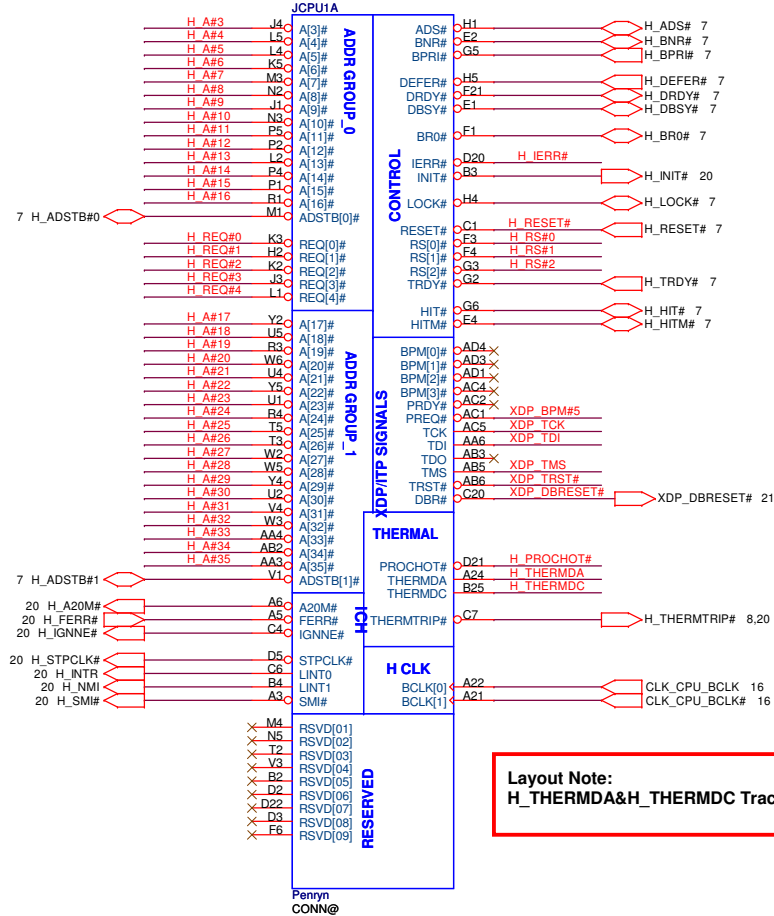
## SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	

## USB table

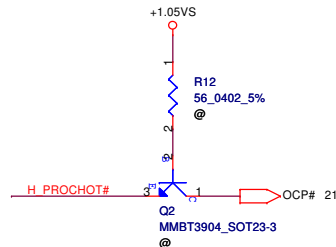
	UHCI1	Port0	MB USB Conn.
EHCI1	UHCI2	Port1	
		Port2	
		Port3	CMOS Camera
		Port4	Card Reader
EHCI2	UHCI3	Port5	New Card(Reserved)
		Port6	MB USB Conn.
		Port7	
		Port8	Blue Tooth
		Port9	
		Port10	Wireless Card
		Port11	

7 H\_A#[3..35] H\_A#[3..35]  
 7 H\_REQ#[0..4] H\_REQ#[0..4]  
 7 H\_RS#[0..2] H\_RS#[0..2]

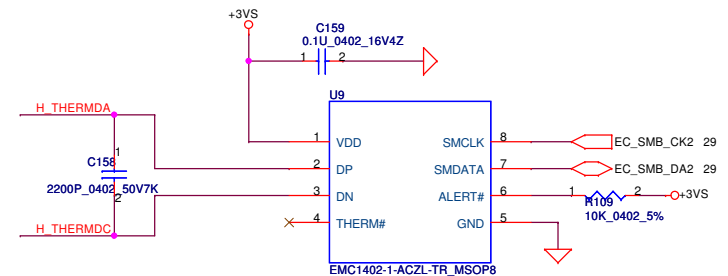
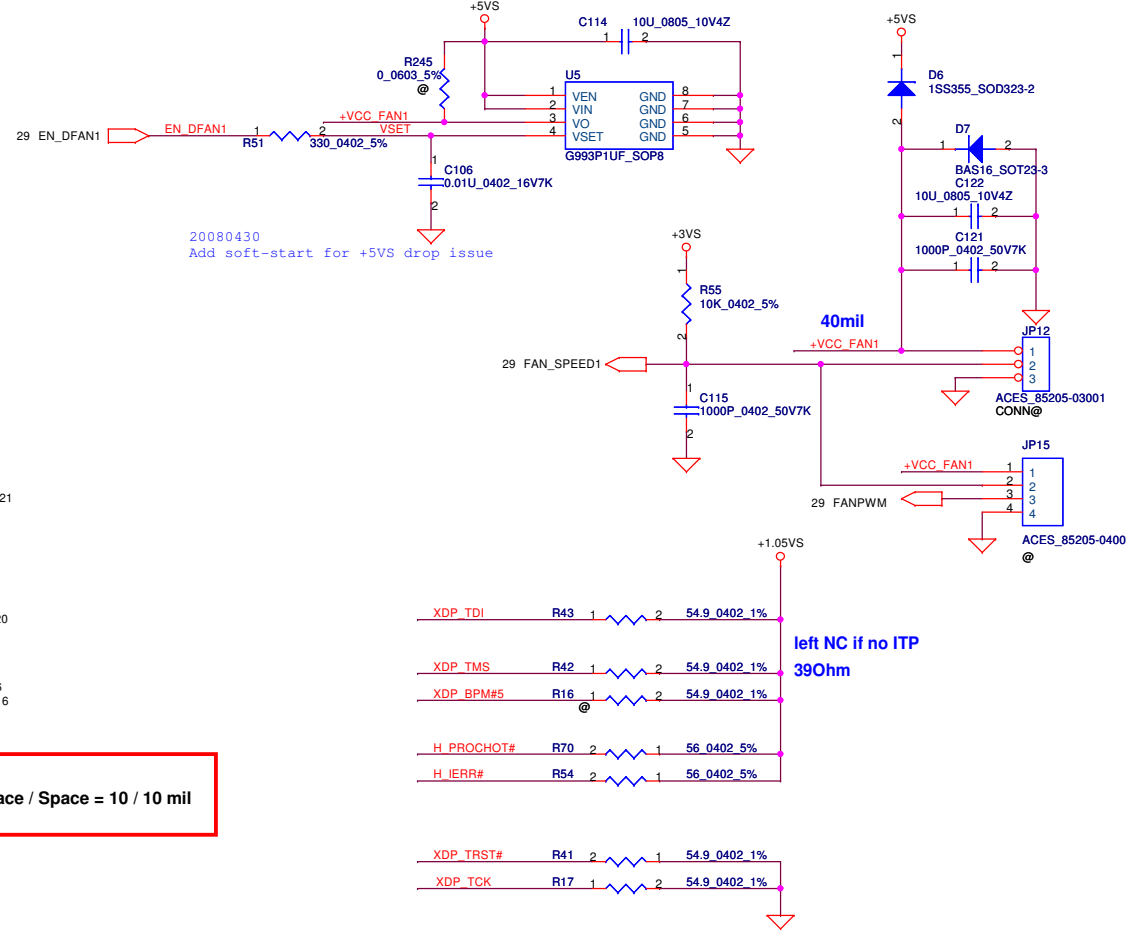


Layout Note:  
 H\_THERMDA&H\_THERMDC Trace / Space = 10 / 10 mil

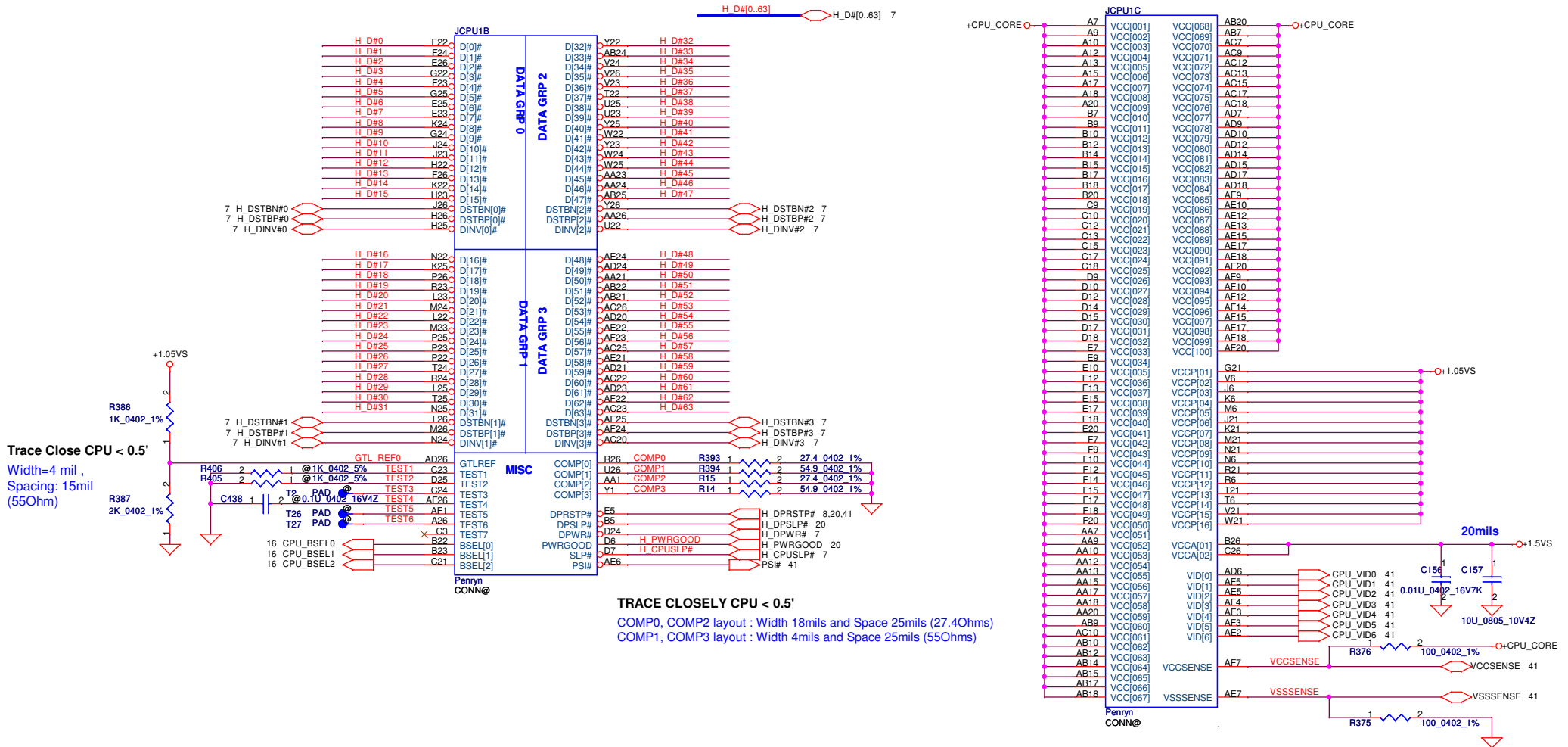
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



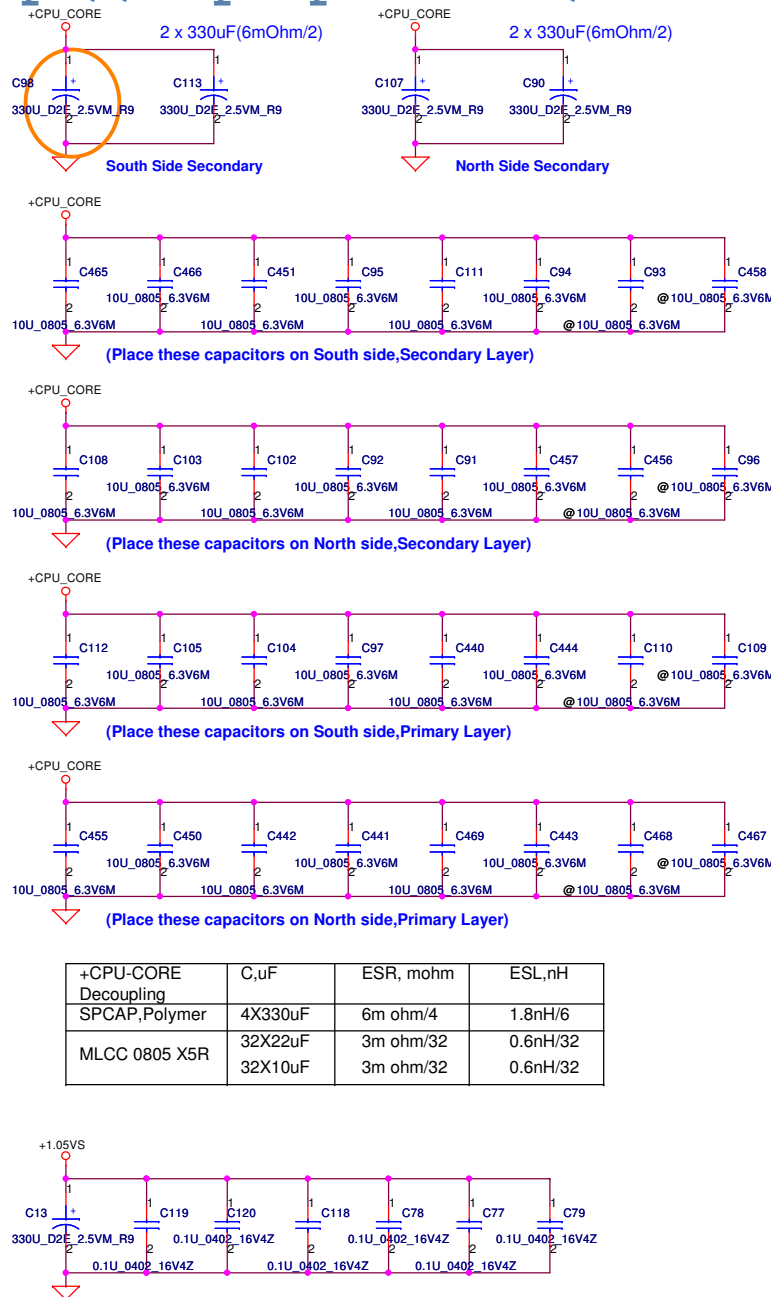
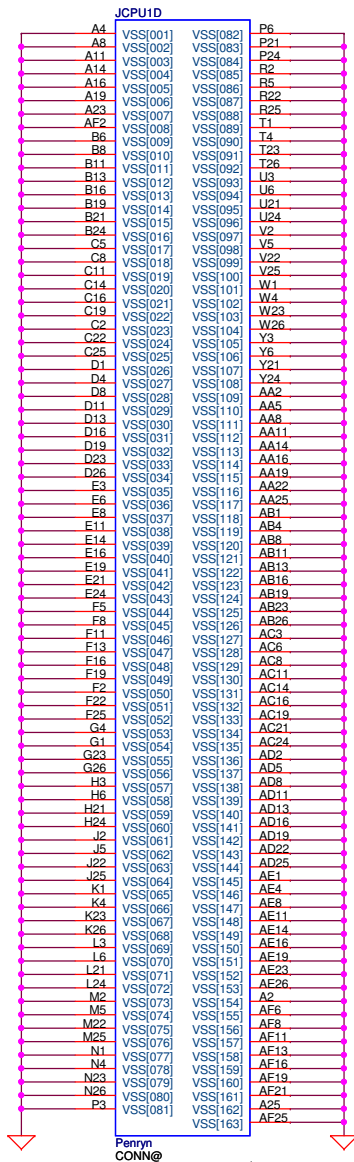
## FAN1 Conn

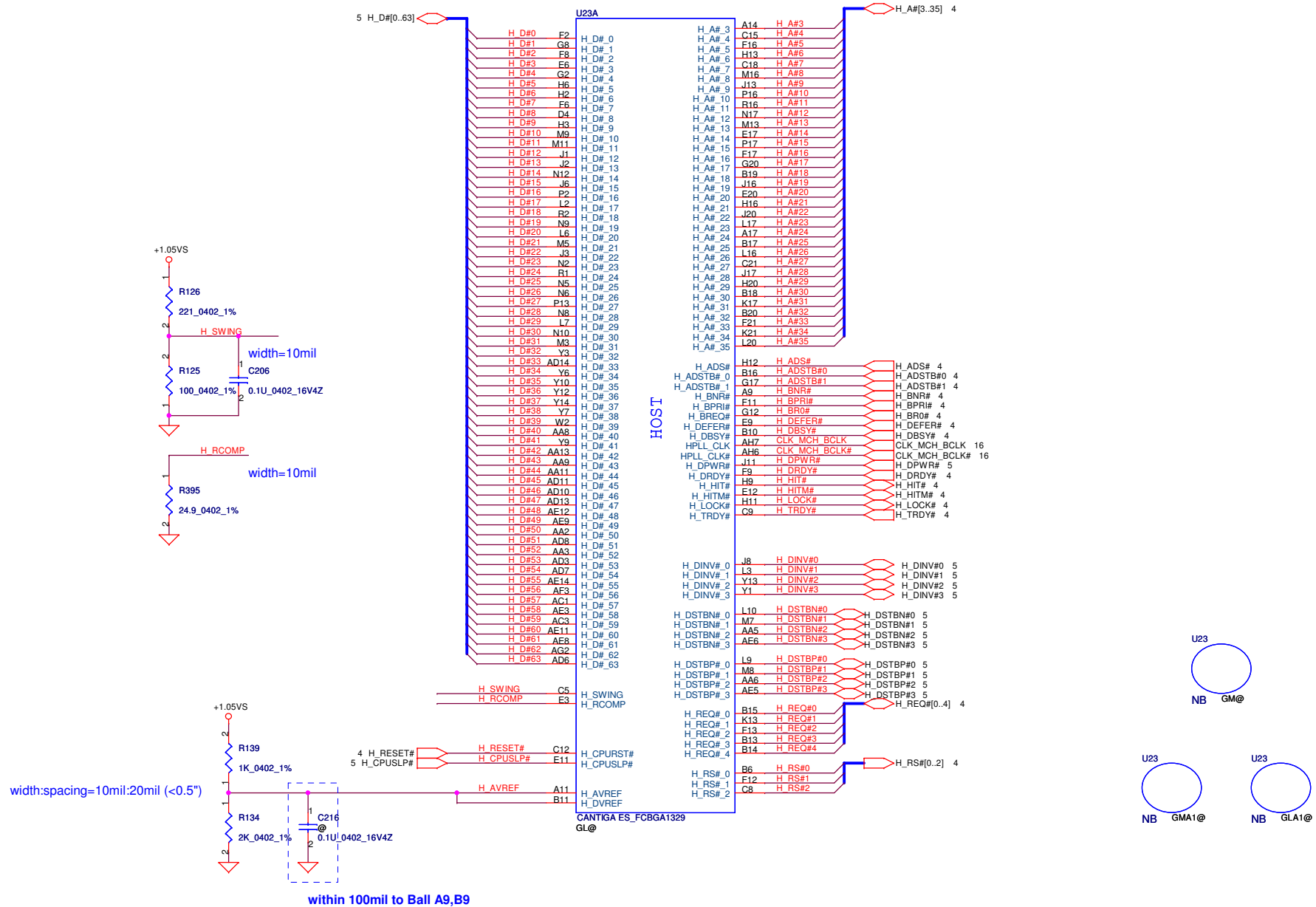


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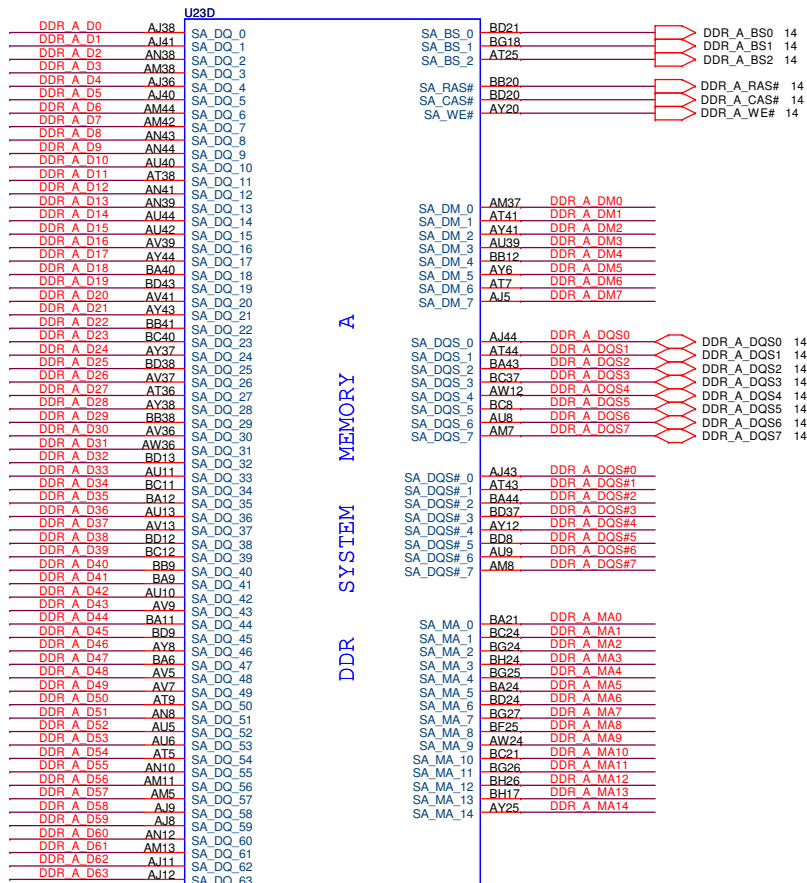


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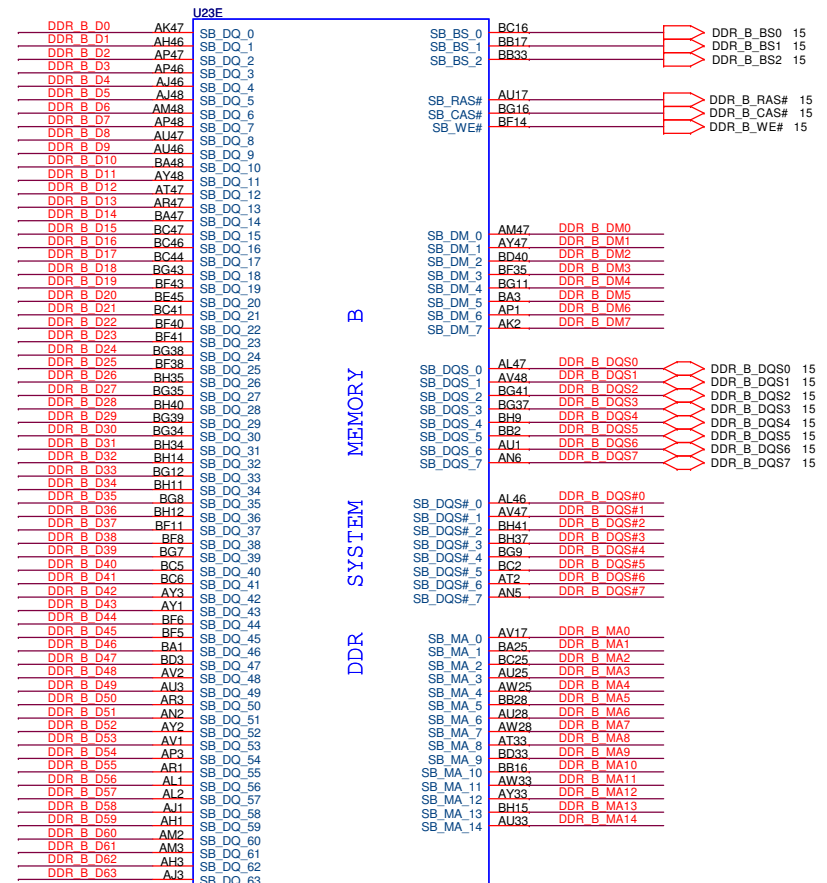




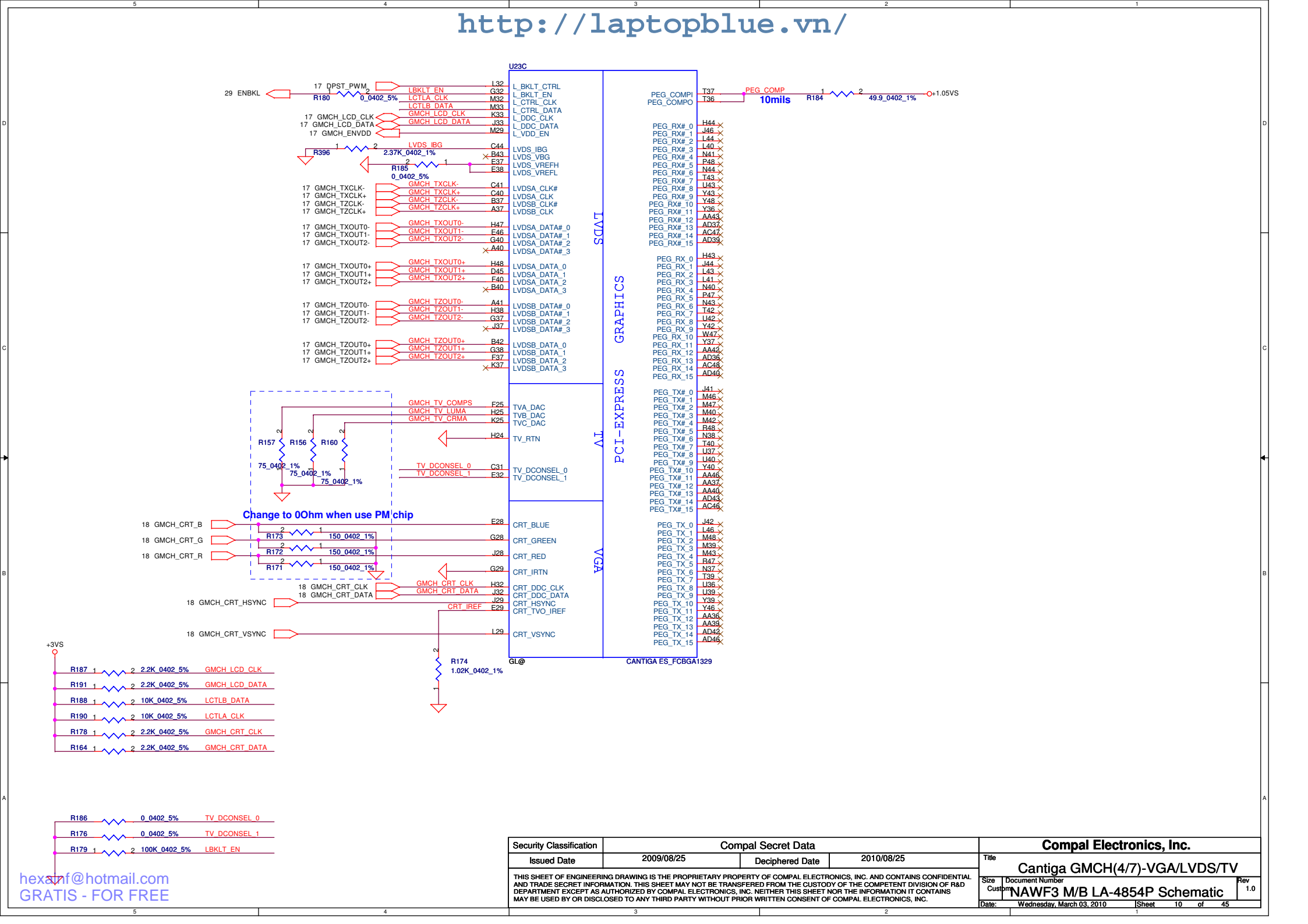




GM@ CANTIGA ES\_FCBGA1329



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<http://laptopblue.vn/>

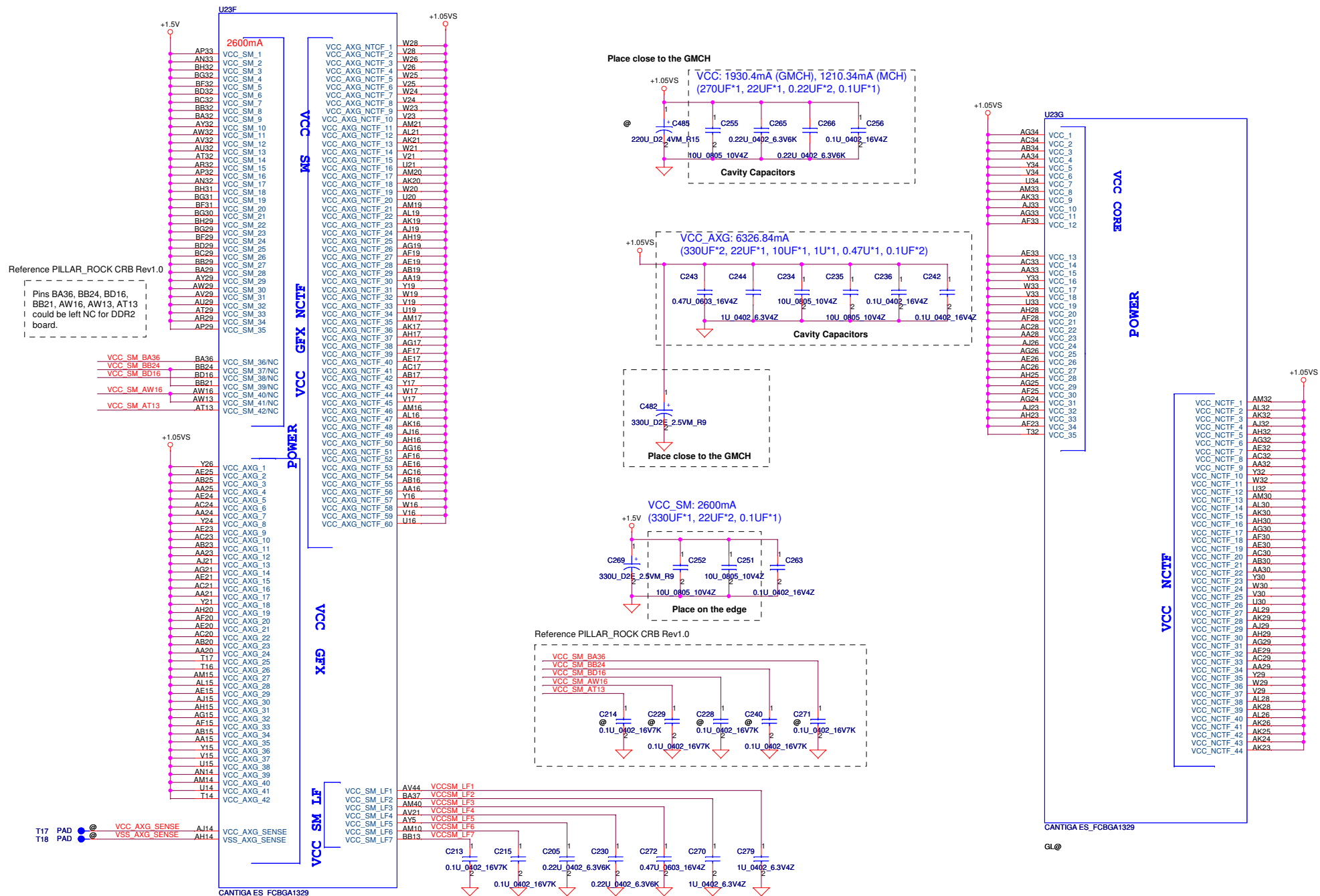
hexaf@hotmai.com

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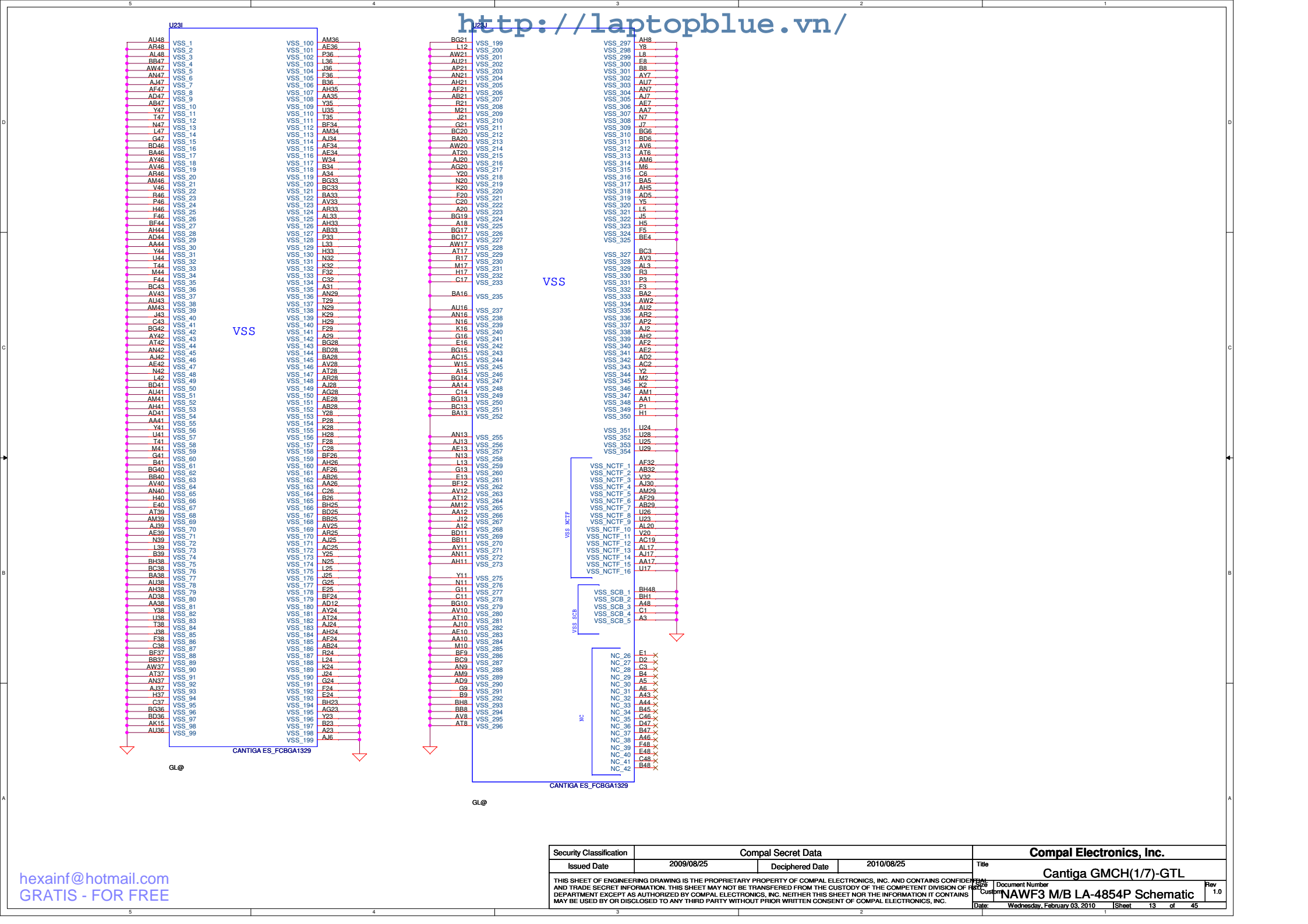
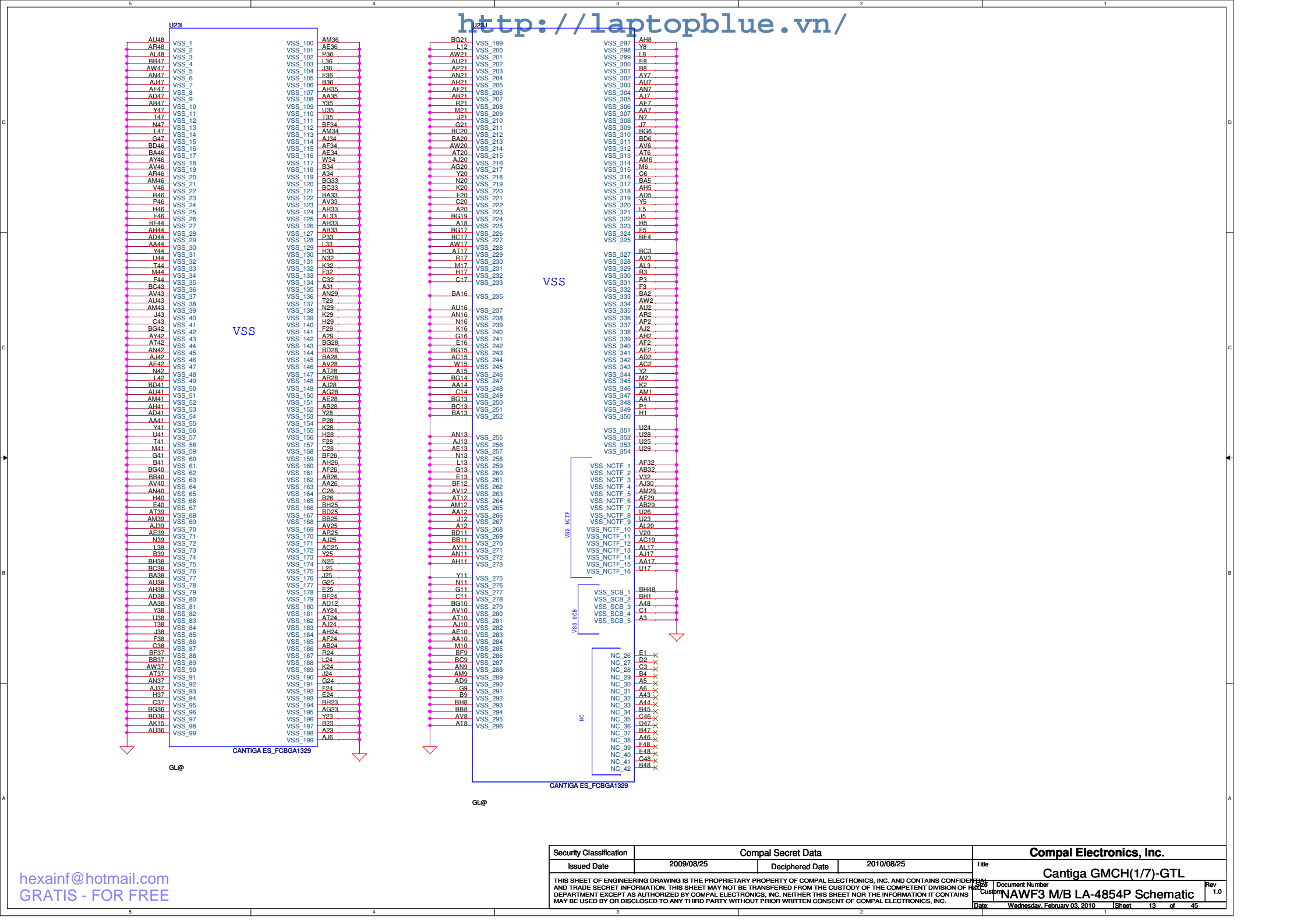
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Cantiga GMCH(4/7)-VGA/LVDS/TV			
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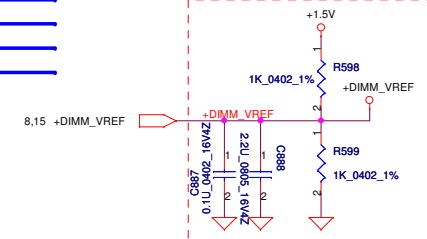
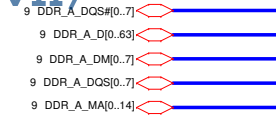
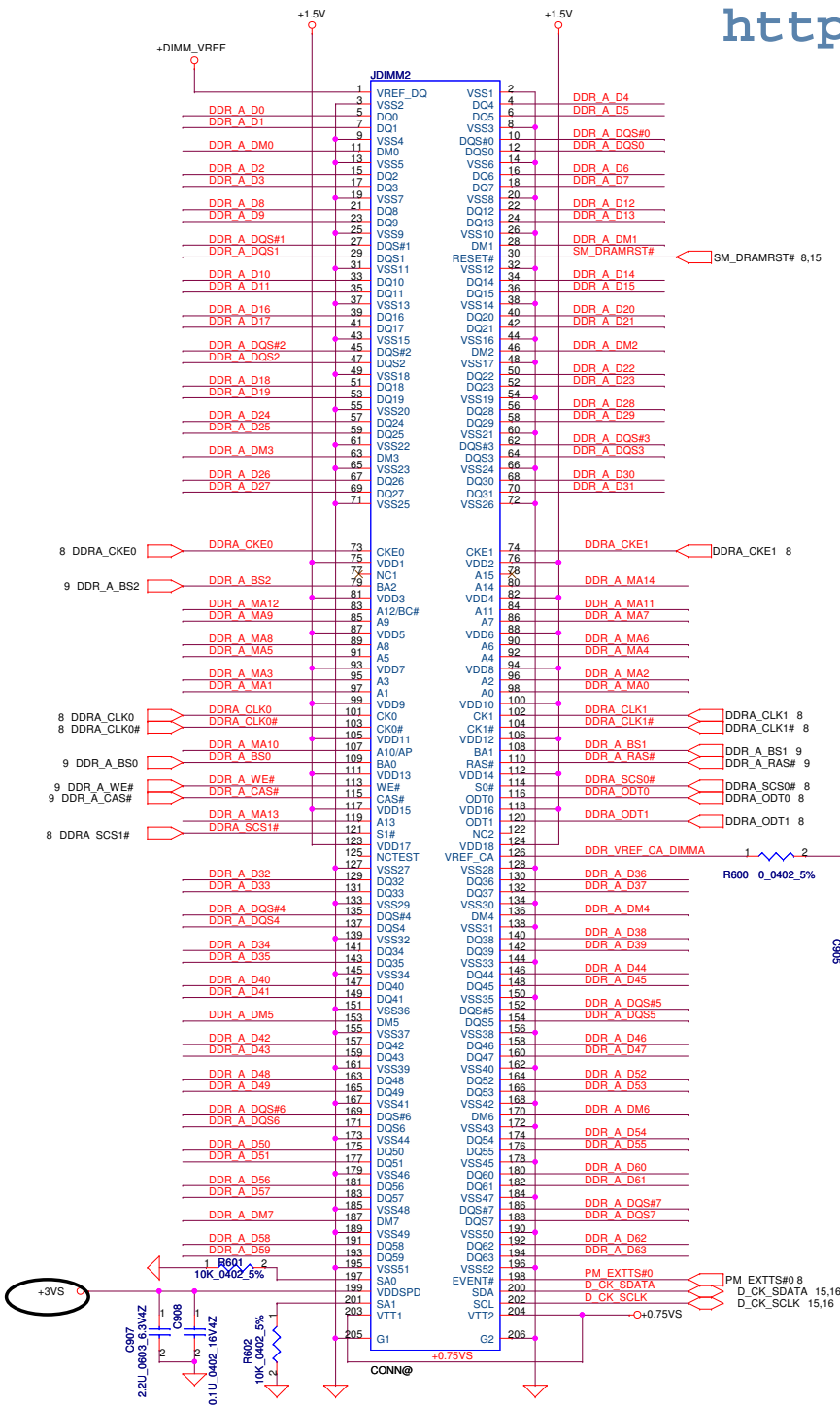


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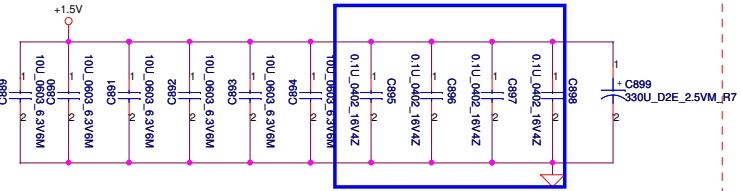
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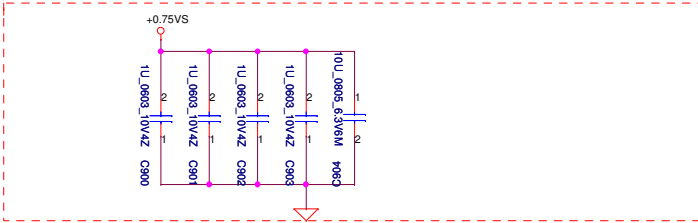
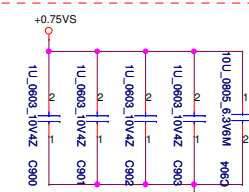


Layout Note:  
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMM0



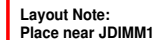
Layout Note:  
Place near JDIMM2.203 & JDIMM2.204



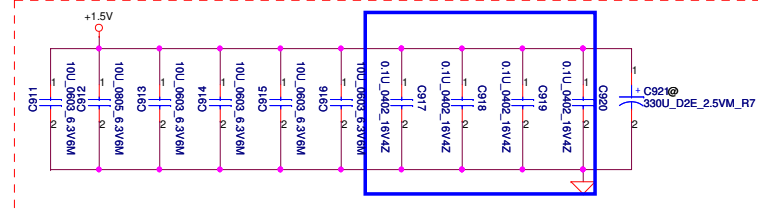
hexainf@hotmail.com  
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DIMM0 REV H:5.2mm (BOT)

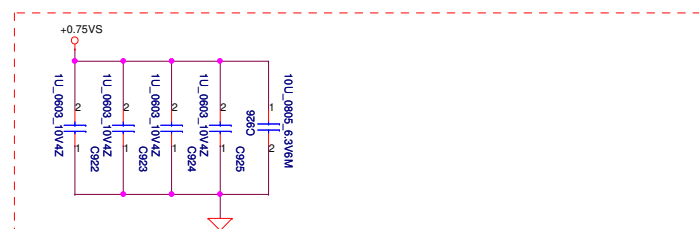
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Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



**Layout Note:**  
Place near JDIMM1.203 & JDIMM1.204



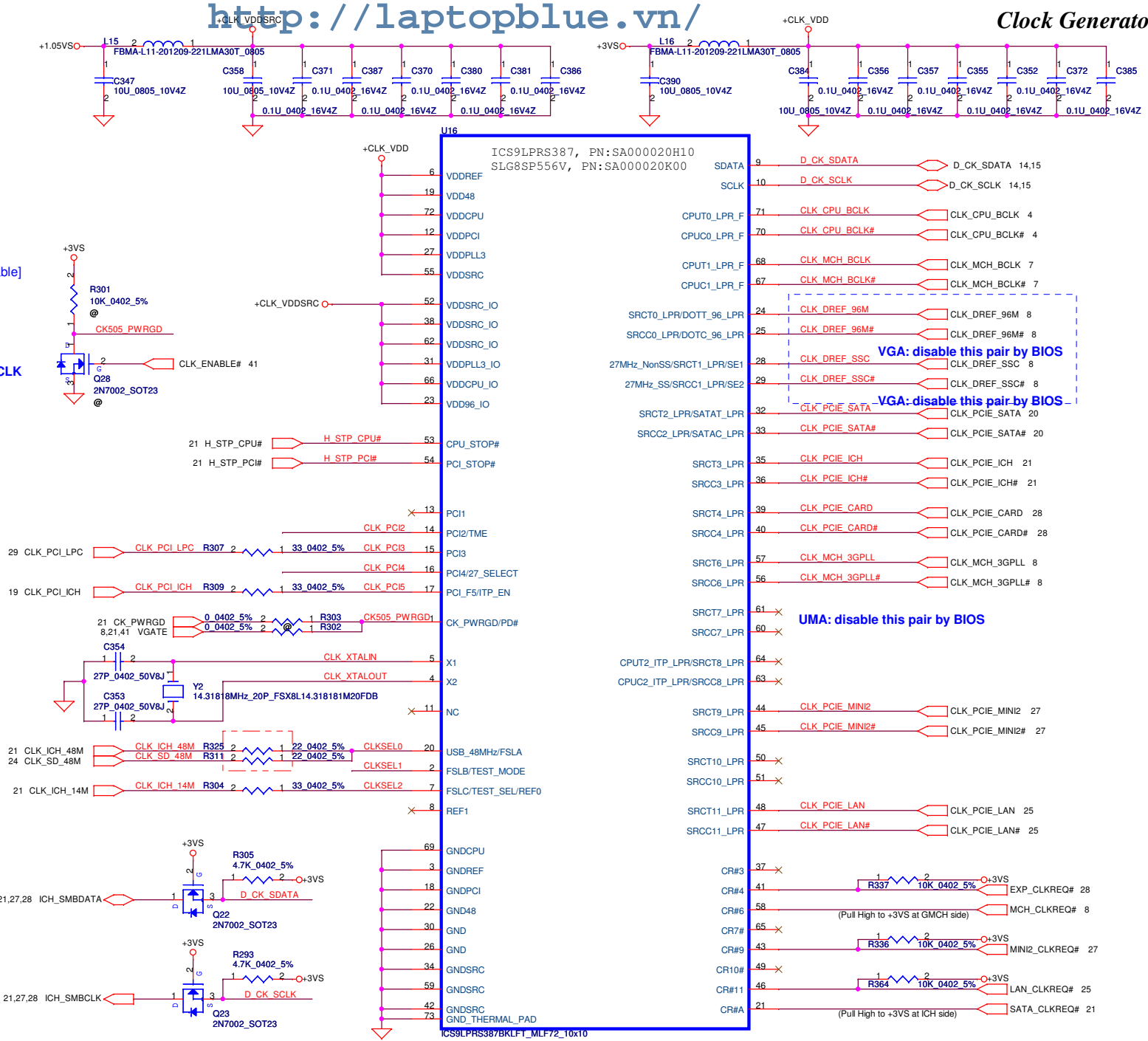
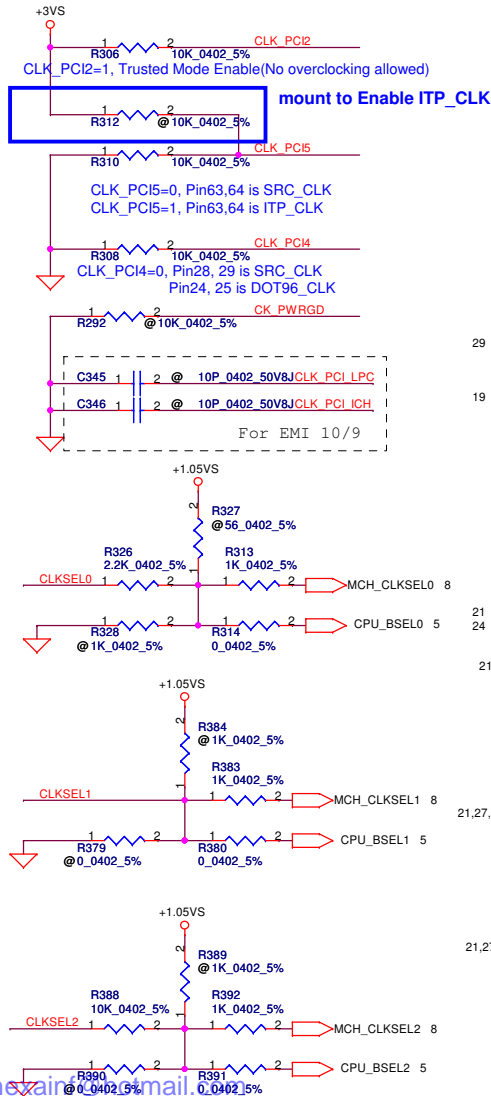


FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
CLKSEL2	CLKSEL1	CLKSEL0			
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

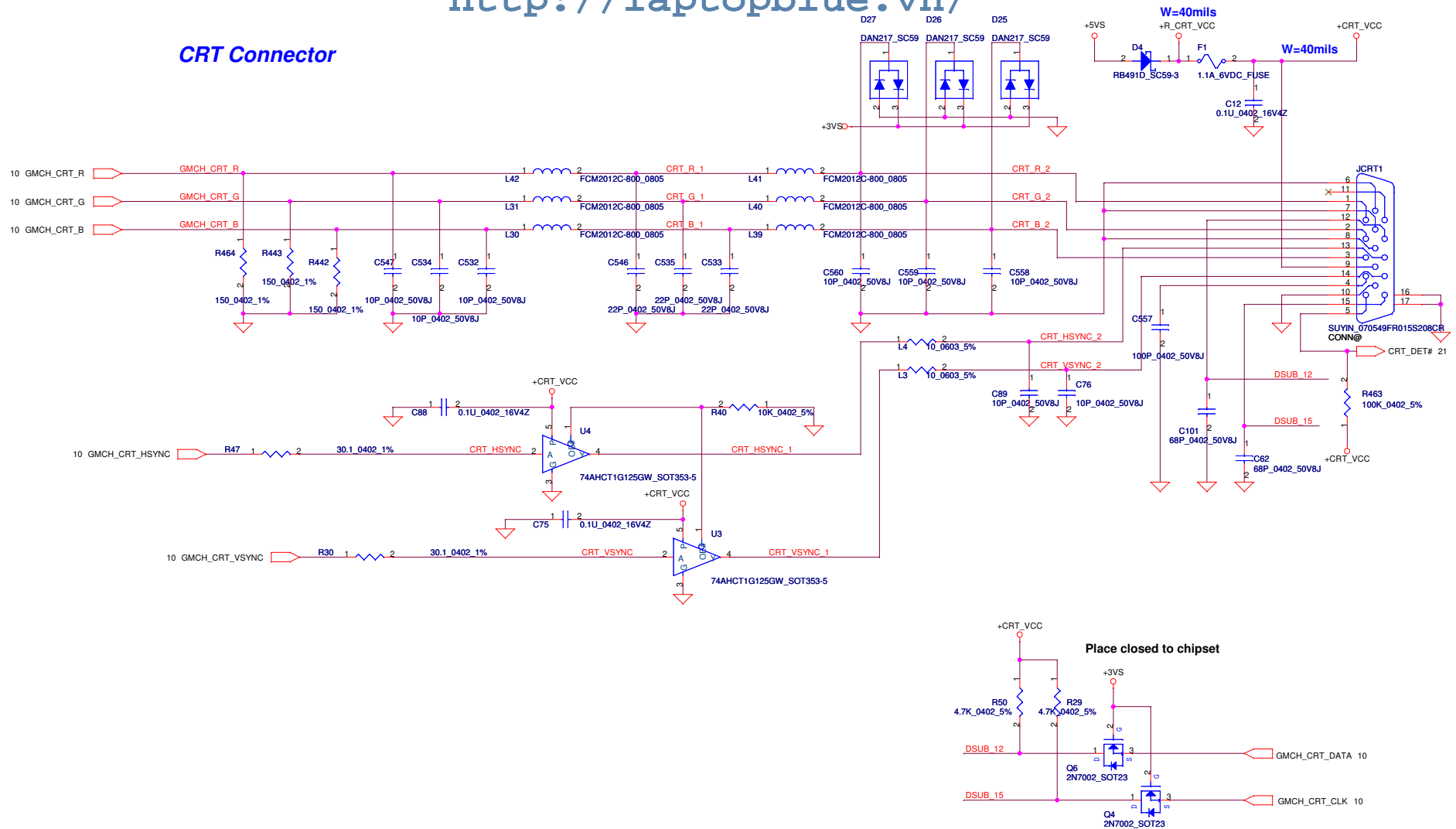
SRC7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]

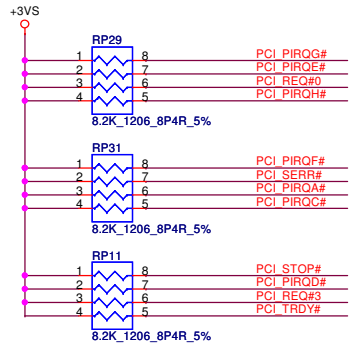
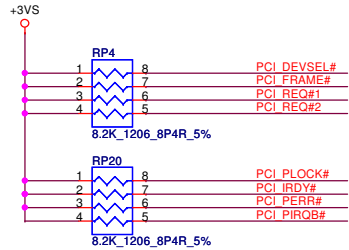


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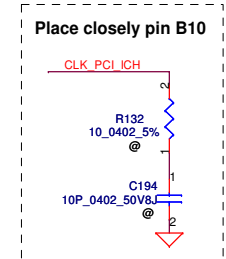
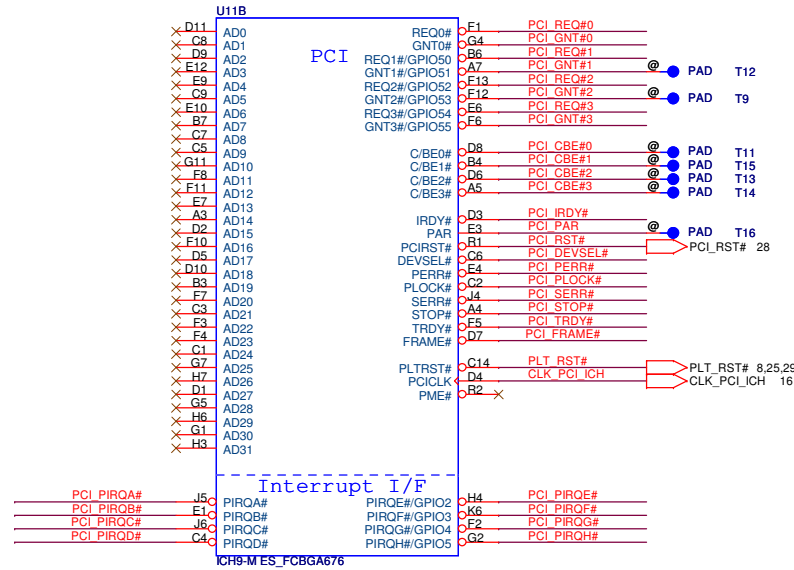


# CRT Connector

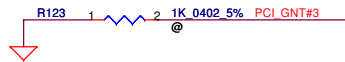




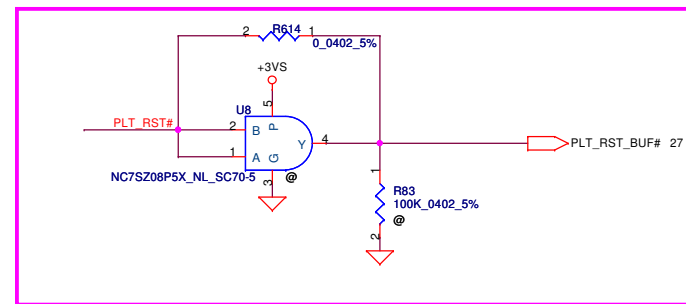
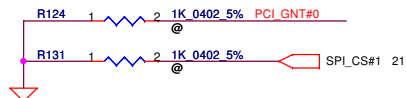
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

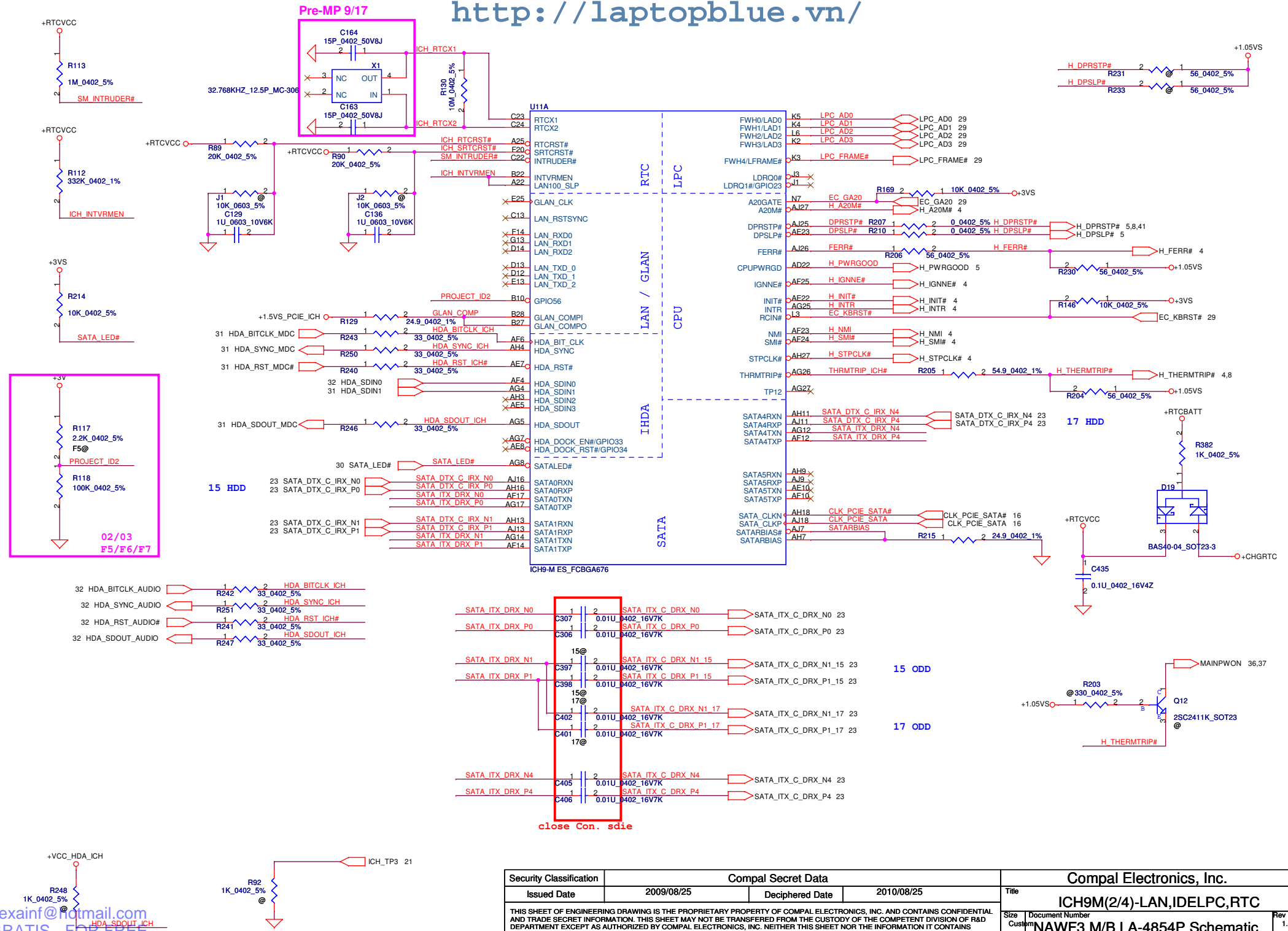


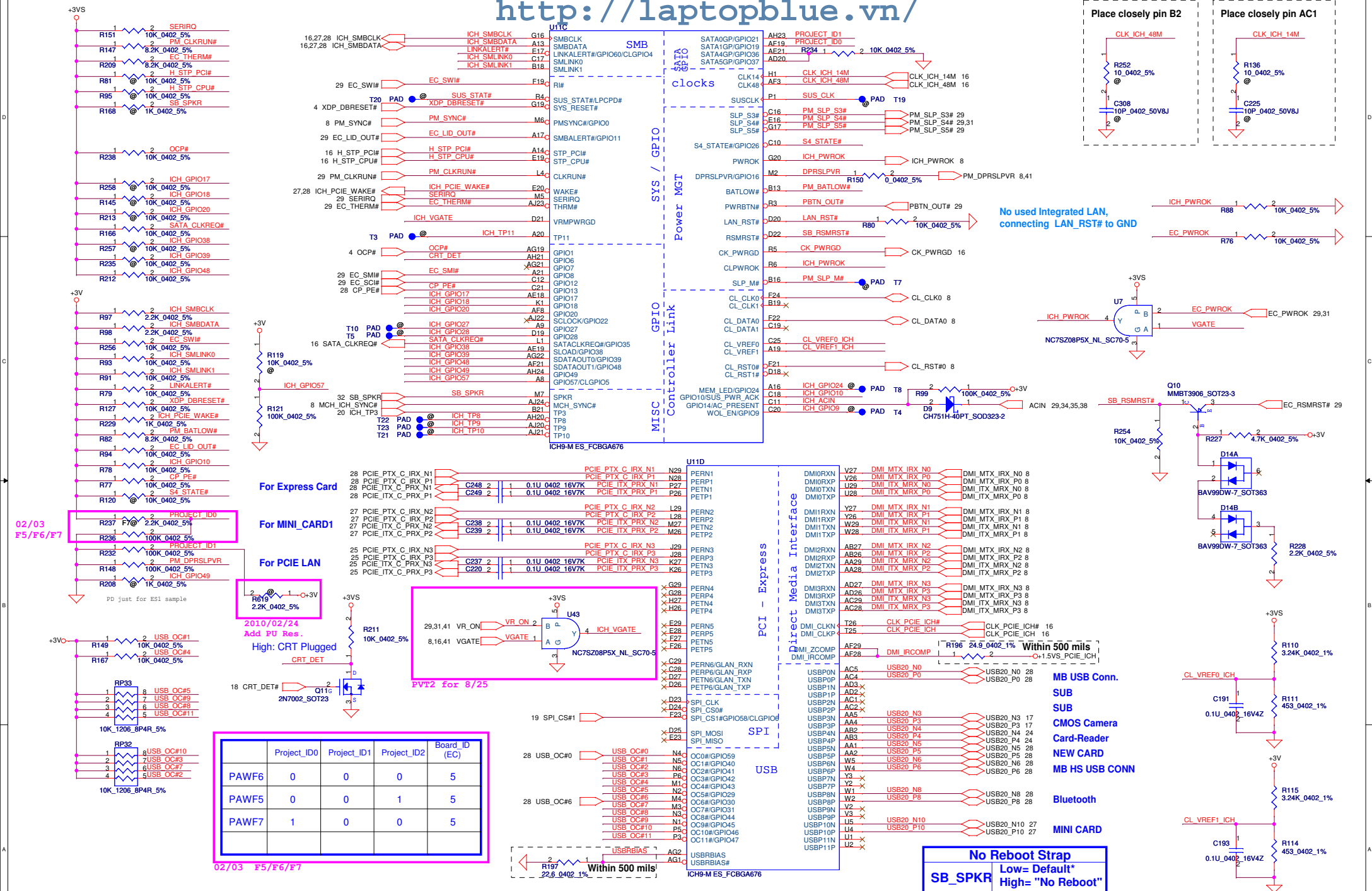
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



PVT2 8/24

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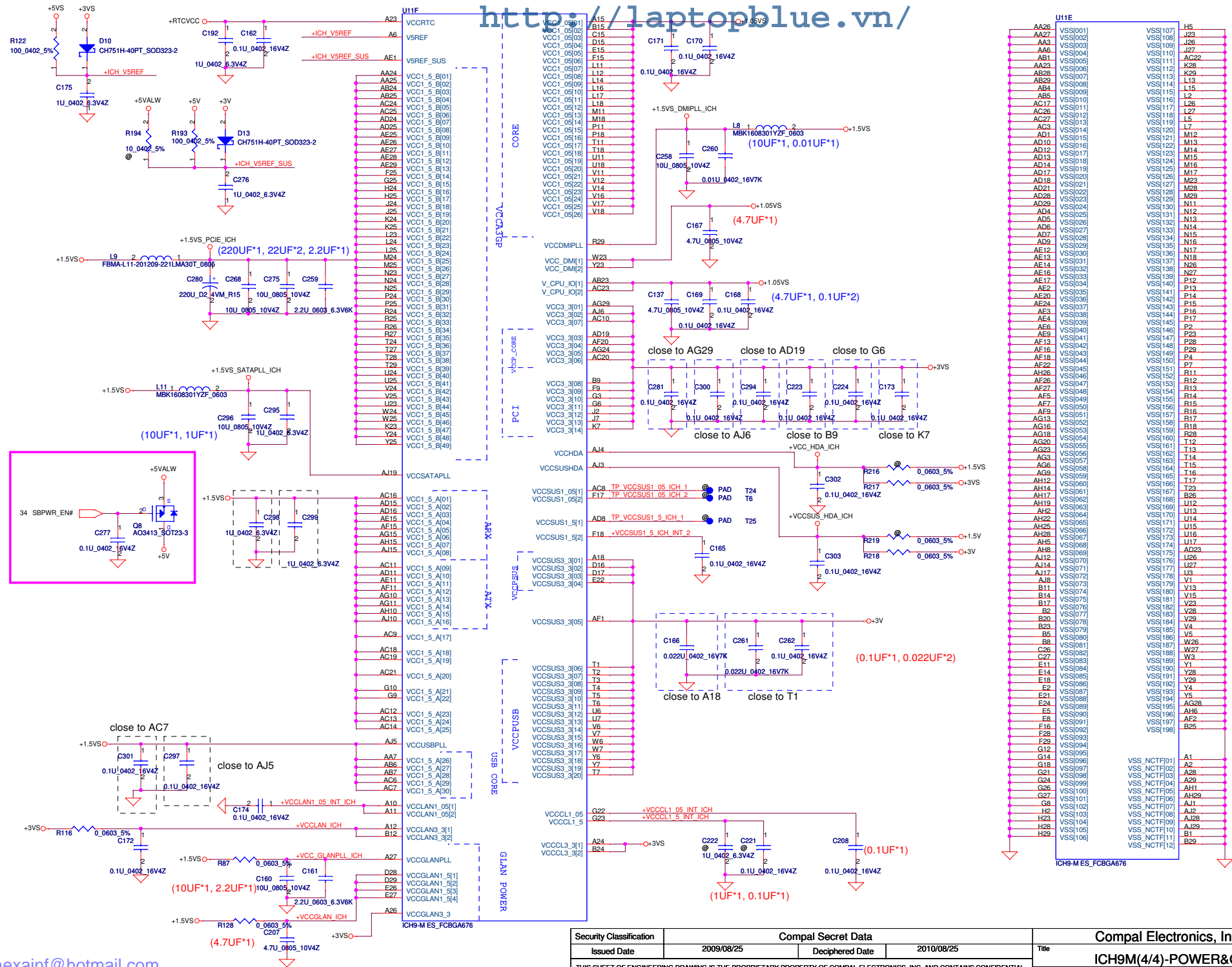


	Project_ID0	Project_ID1	Project_ID2	Board_ID (EC)
PAWF6	0	0	0	5
PAWF5	0	0	1	5
PAWF7	1	0	0	5

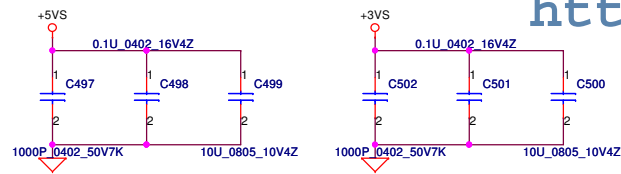
Internal TPM Strap		DMI Termination Voltage	
SPI_MOSI	Low= Disable* High=TPM enable by MCH strap	GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

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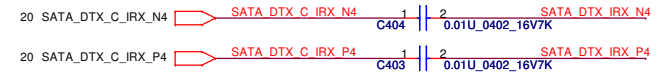
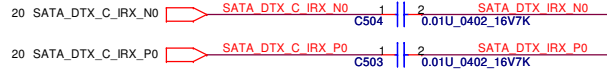
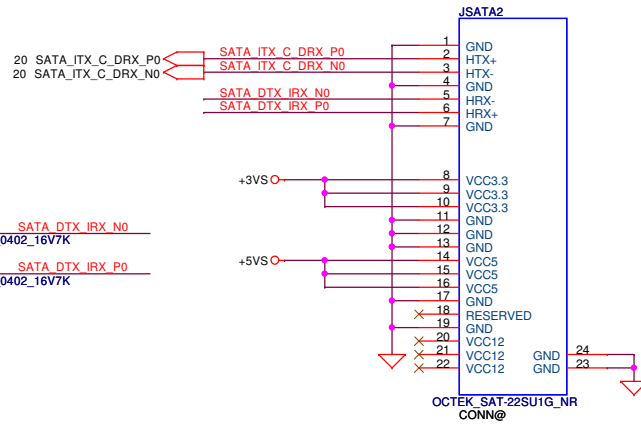




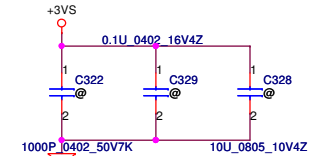
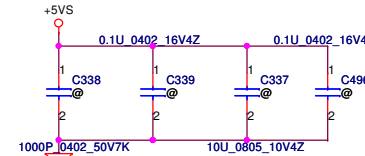
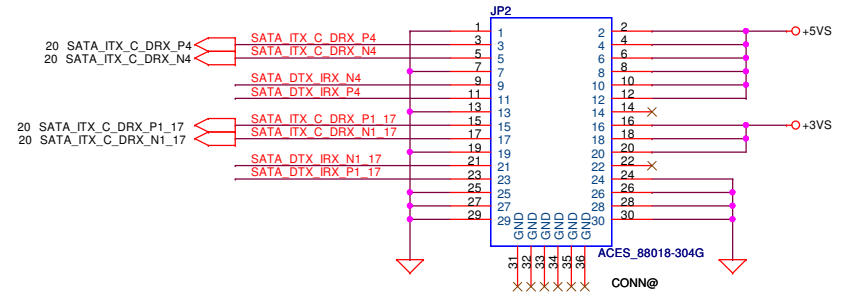
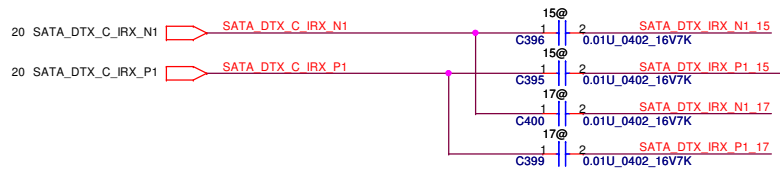
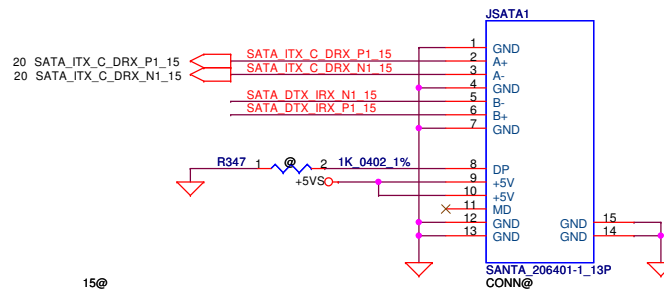
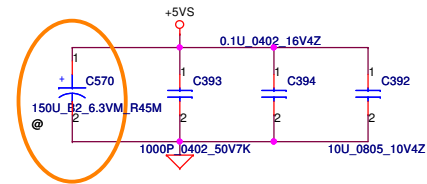




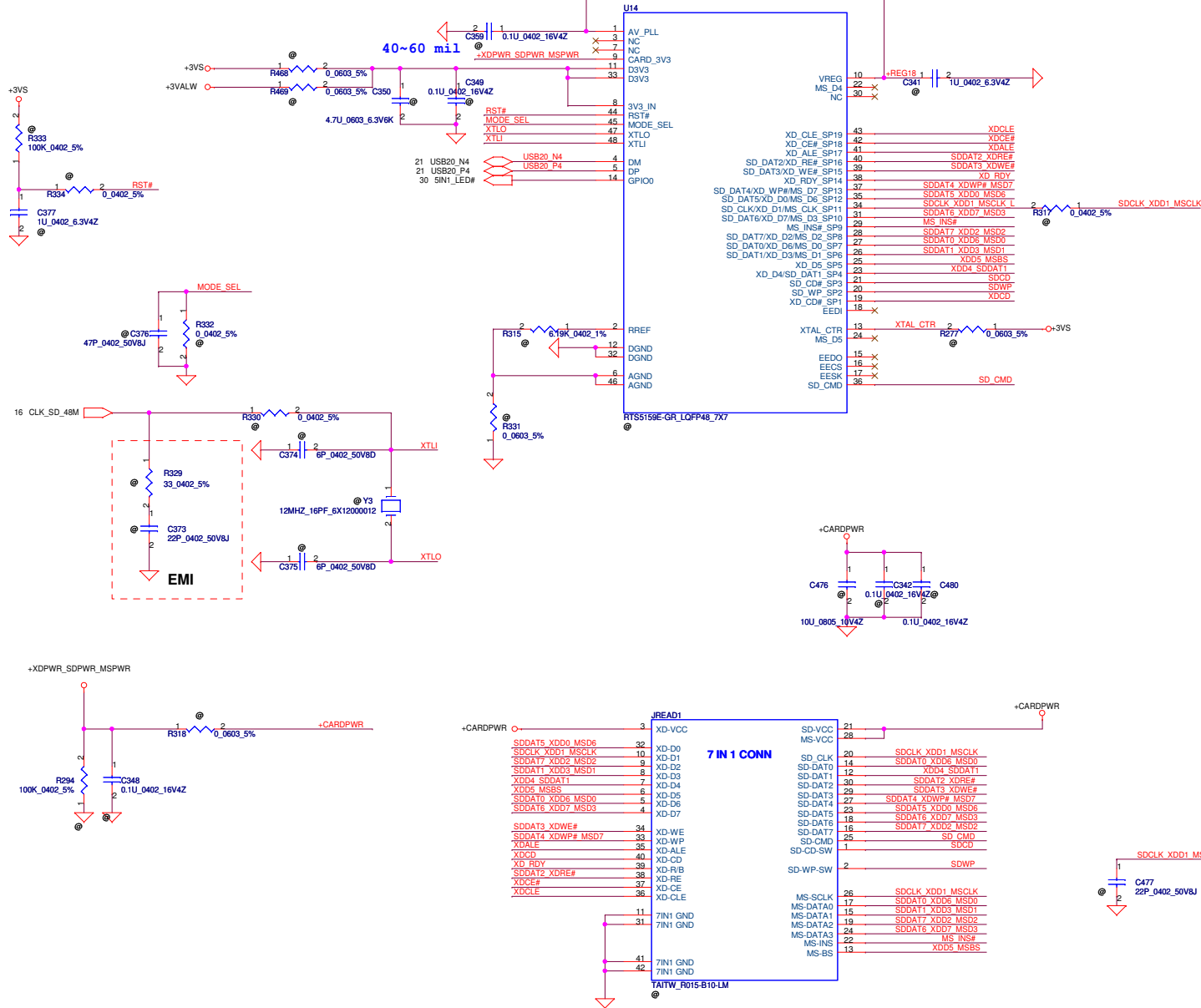
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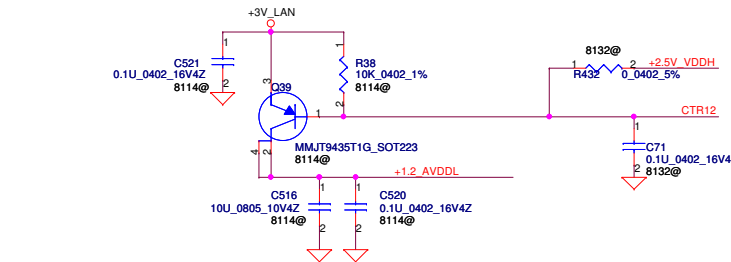
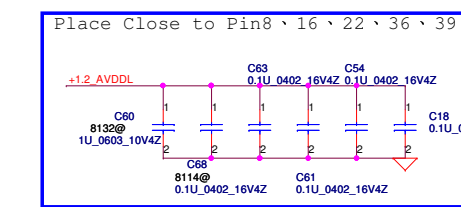
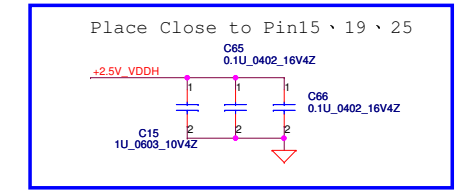
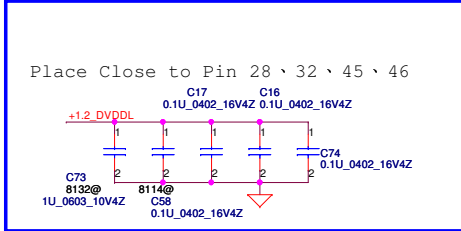
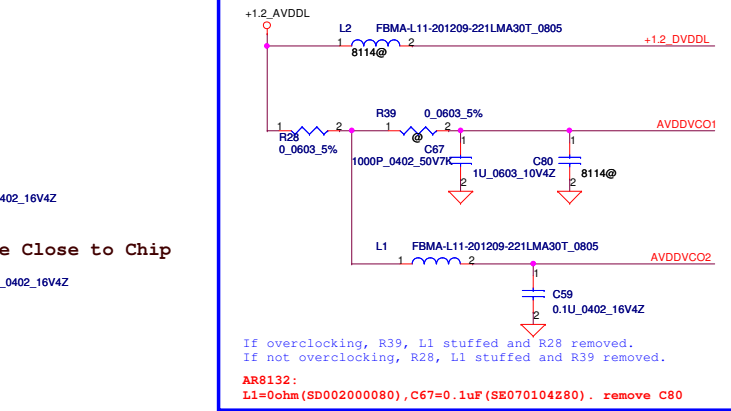
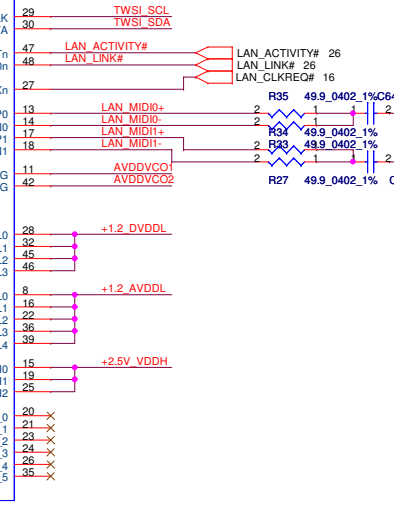
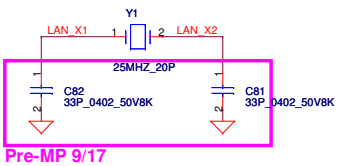
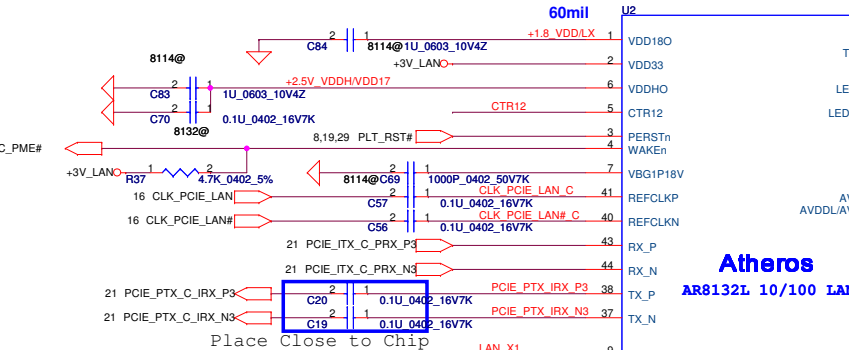
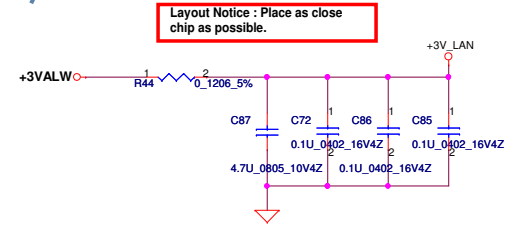
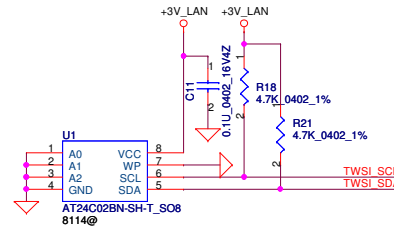
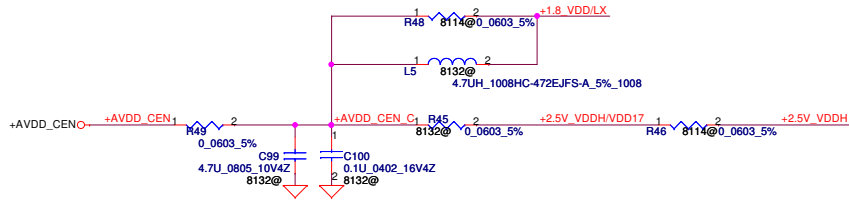
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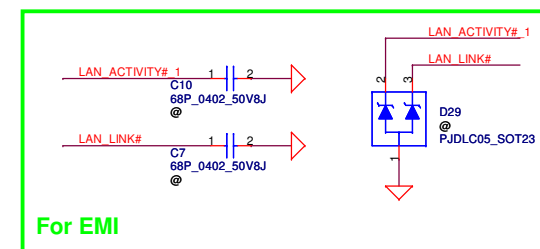
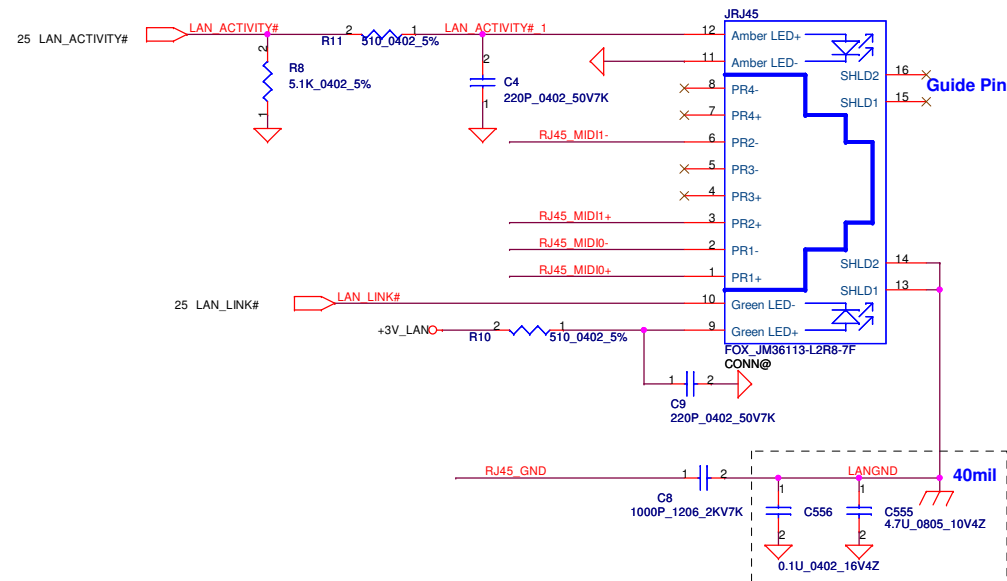
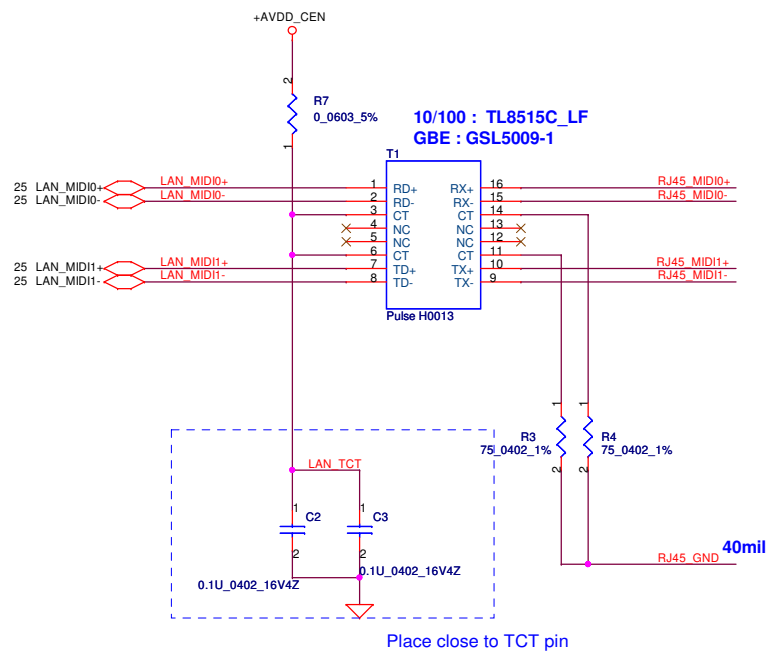
Vender suggestion



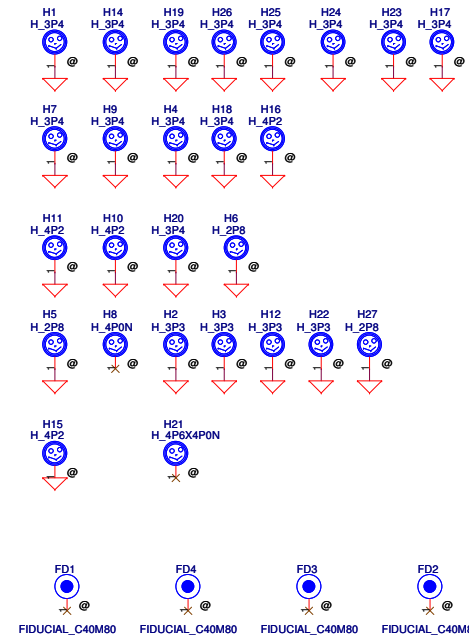
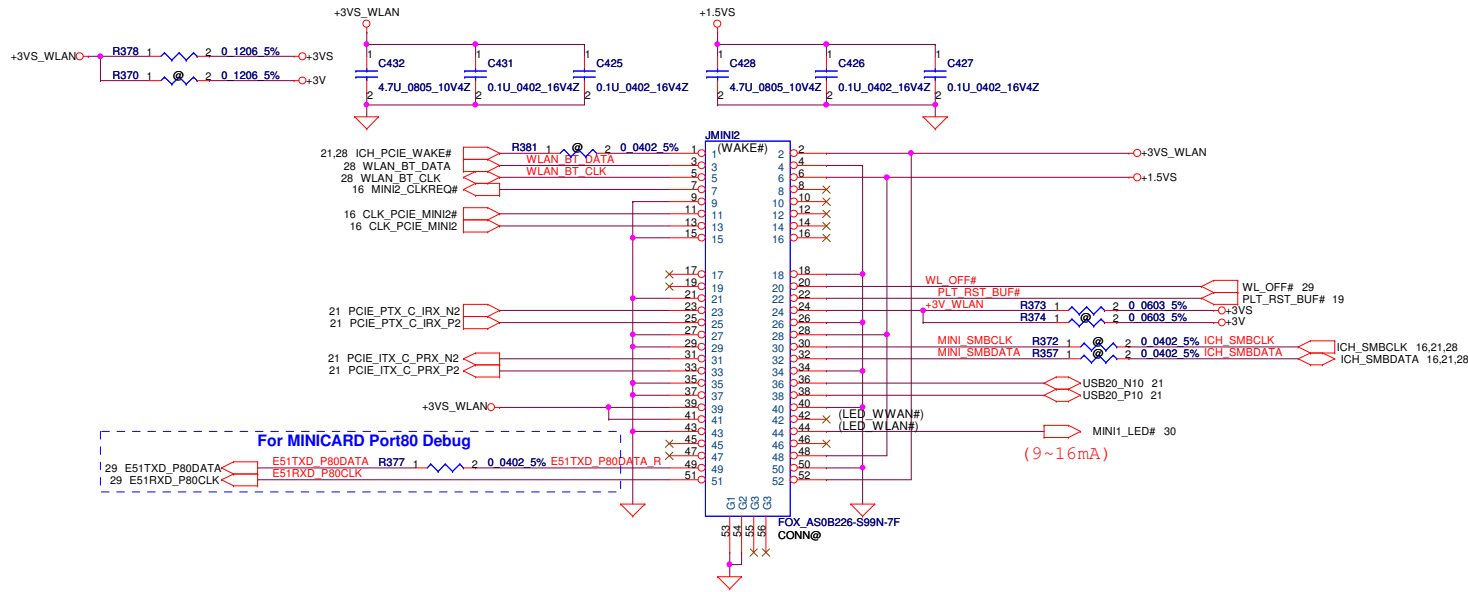
02/03 F5/F6/F7  
remove Card reader



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				NAWF3 M/B LA-4854P Schematic	
				Date: Wednesday, March 03, 2010	
				Sheet 25 of 45	

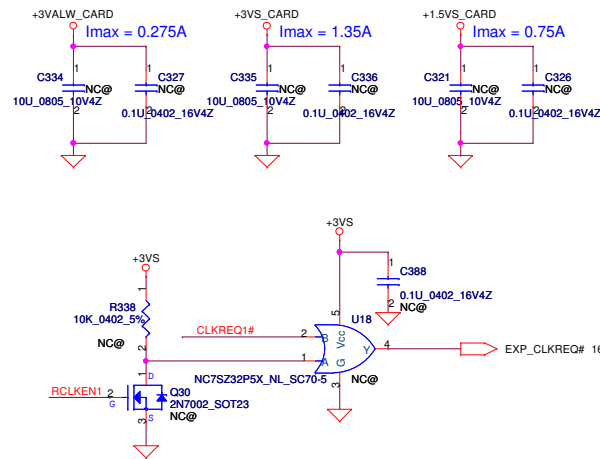
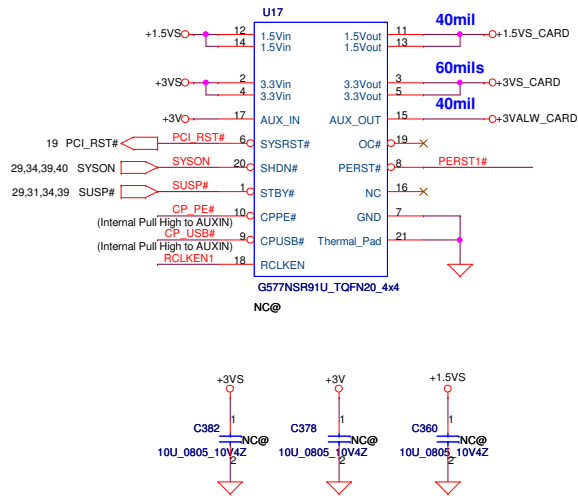


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

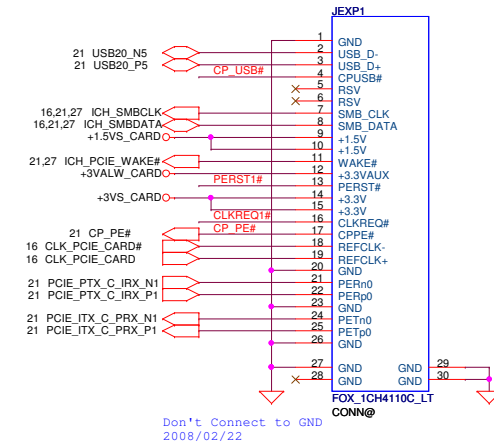


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Issued Date		2009/08/25		Deciphered Date		2010/08/25		Title			
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								Document Number		Rev	
								NAWF3 M/B LA-4854P Schematic		1.0	
Date				Wednesday, March 03, 2010		Sheet		27 of 45			

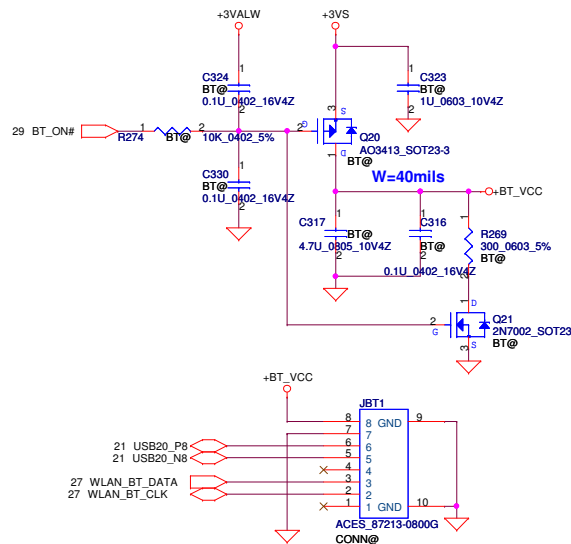
## New Card Power Switch



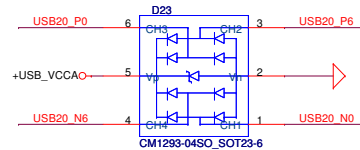
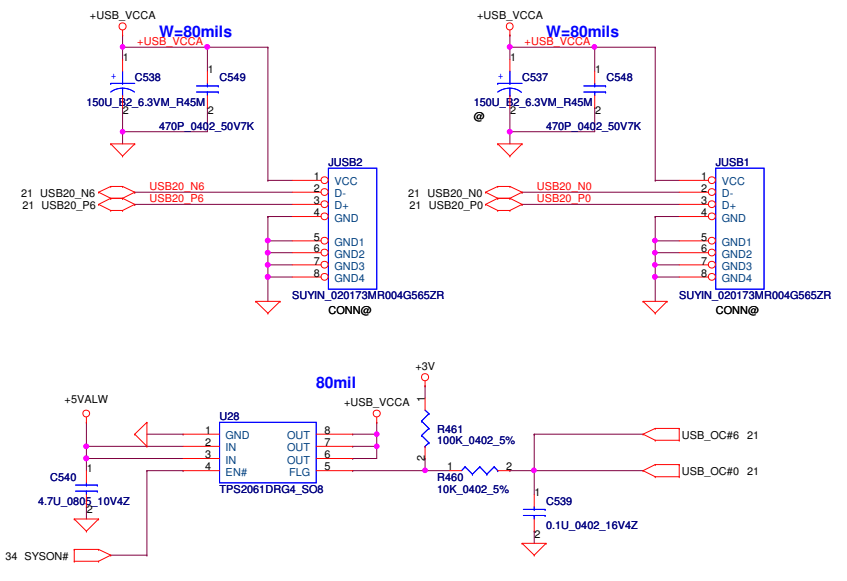
## New Card Socket (Left/TOP)



## Bluetooth Conn.

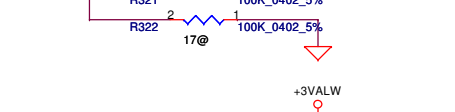
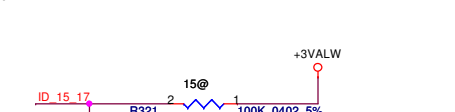
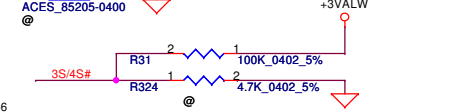
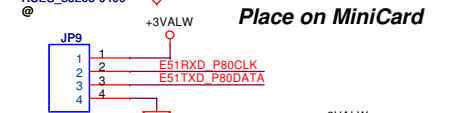
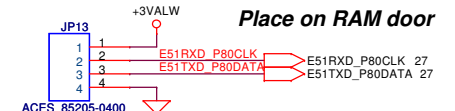


## USB CONN.

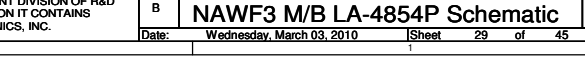
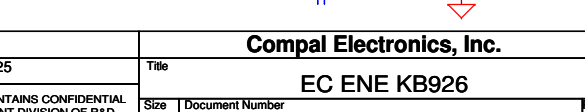
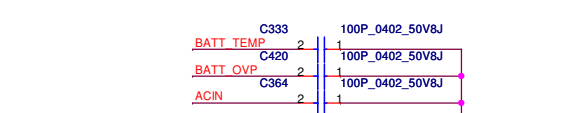
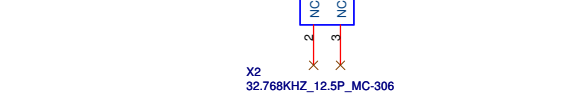
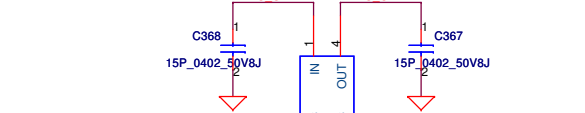
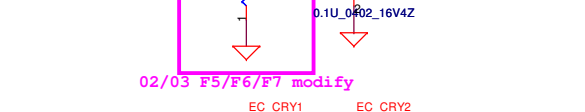
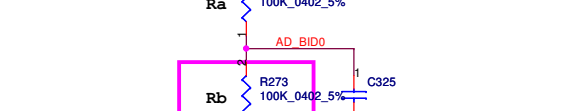
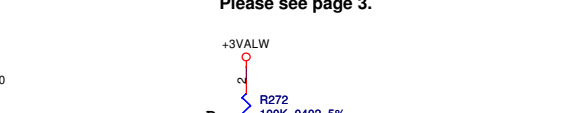
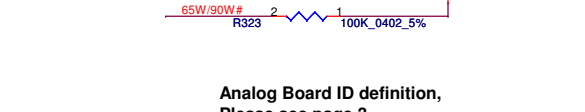
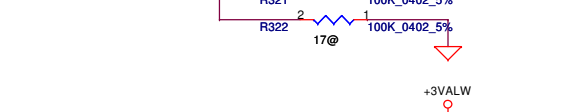
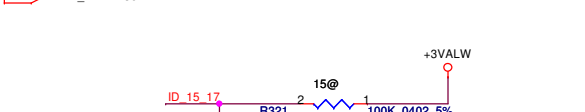
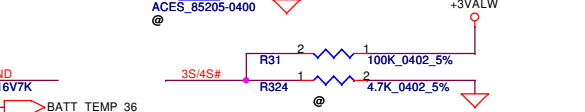
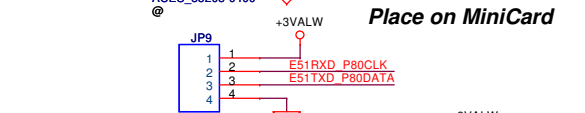
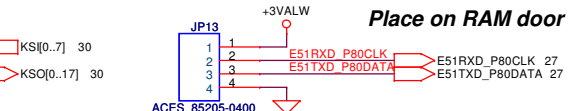
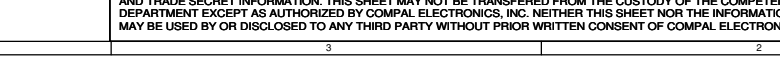
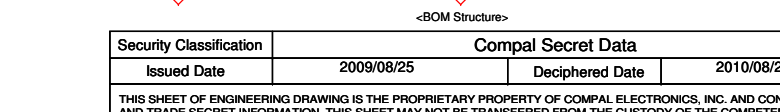
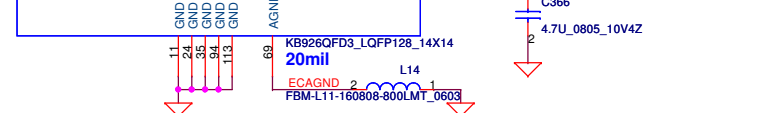
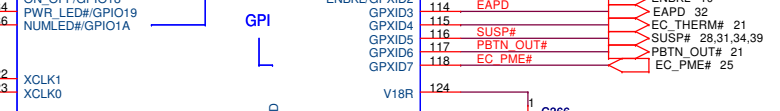
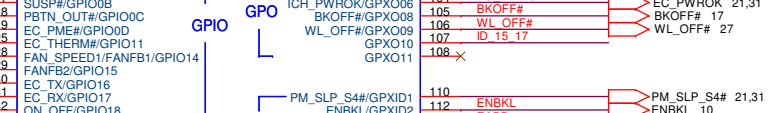
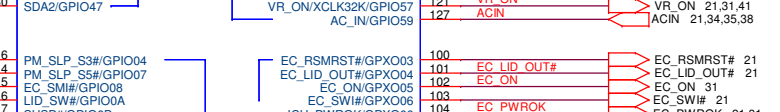
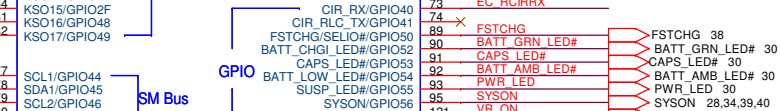
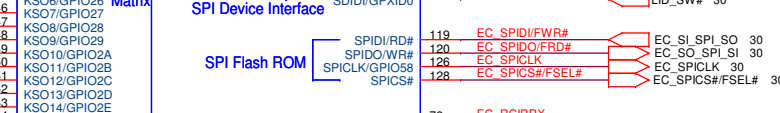
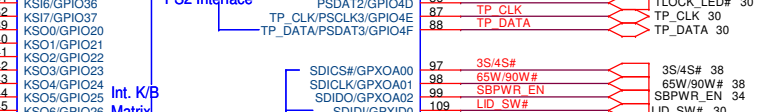
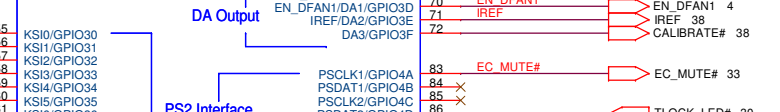
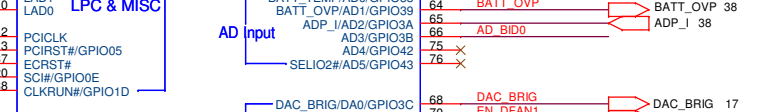
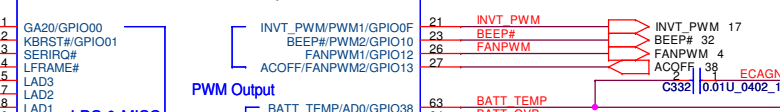
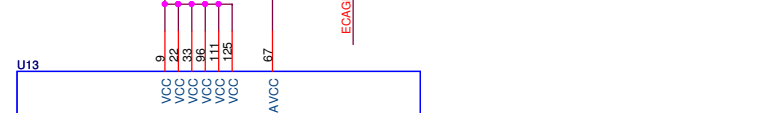
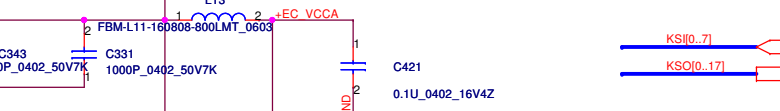
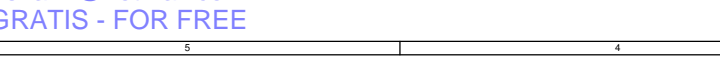
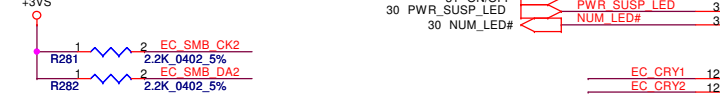
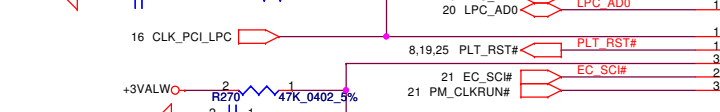
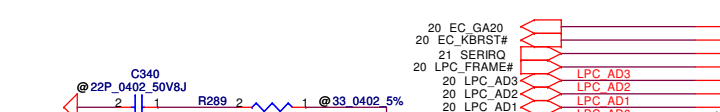
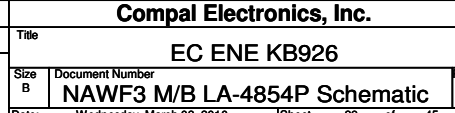
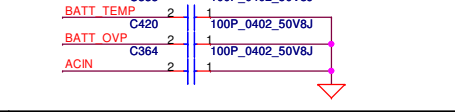
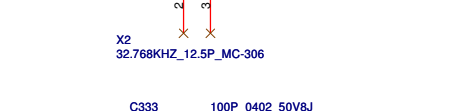
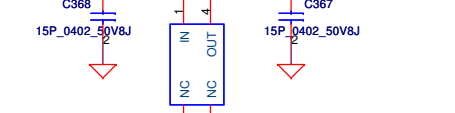
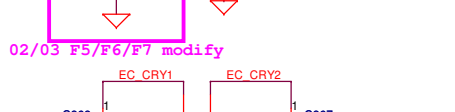
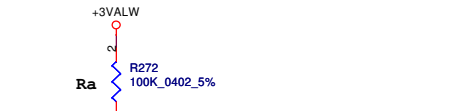


Place on RAM door

Place on MiniCard

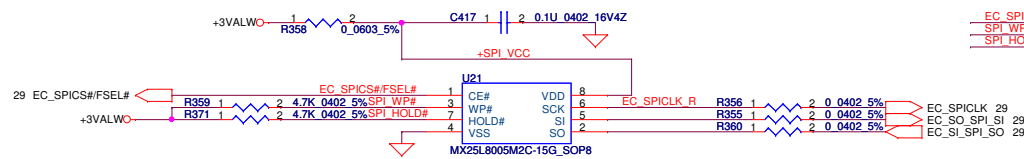


Analog Board ID definition, Please see page 3.



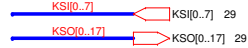
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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Size	Document Number	NAWF3 M/B LA-4854P Schematic		Rev	1.0
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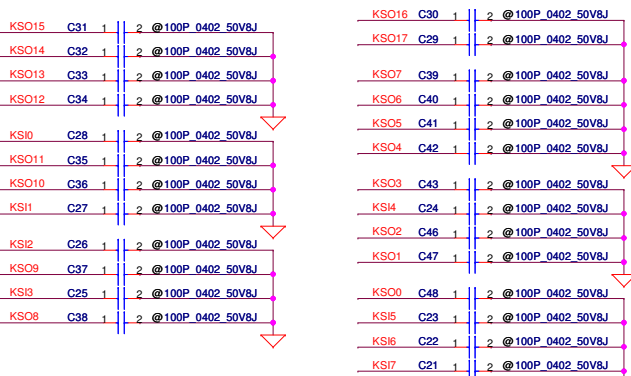
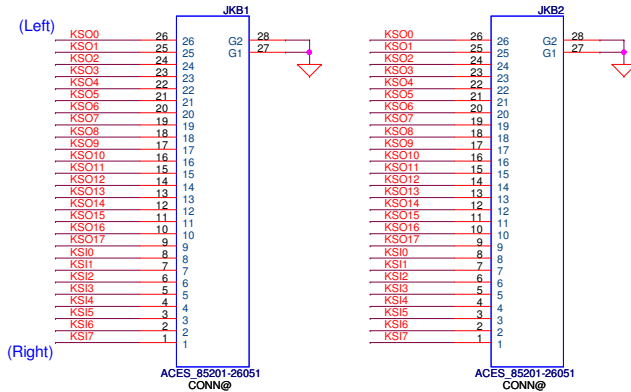
ENE suggestion SPI Frequency over 66MHz  
SST: 50MHz  
MXIC: 70MHz  
ST: 40MHz

## INT\_KBD Conn.

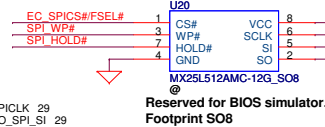
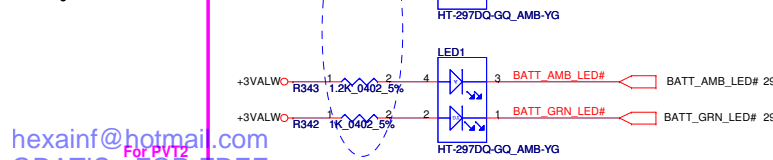
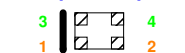


15"

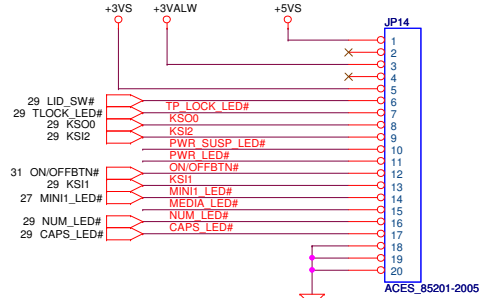
17"



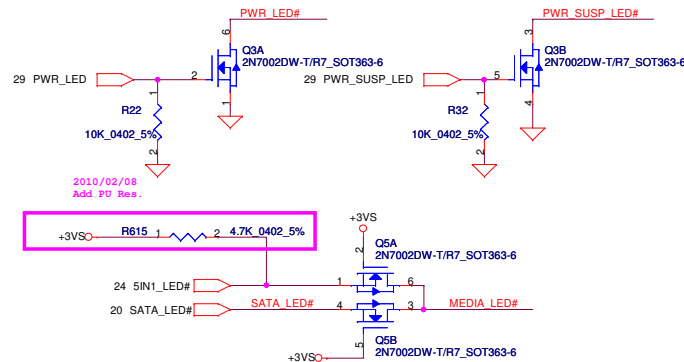
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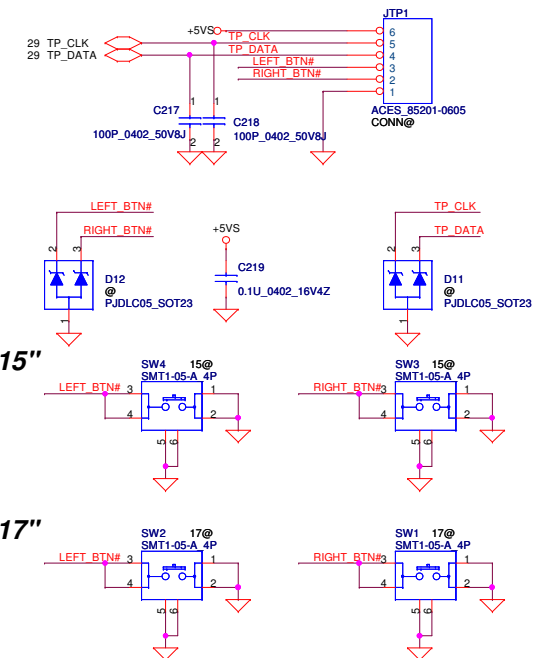
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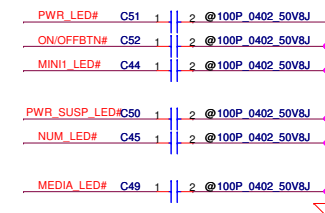
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KSI1	WL_BTN#
KSI2	TLOCK_BTN#
KSI3	
KSI4	
KSI5	



## To TP/B Conn.



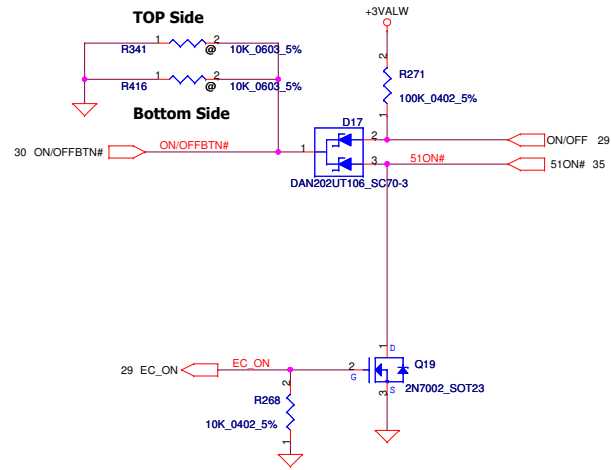
## FOR EMI



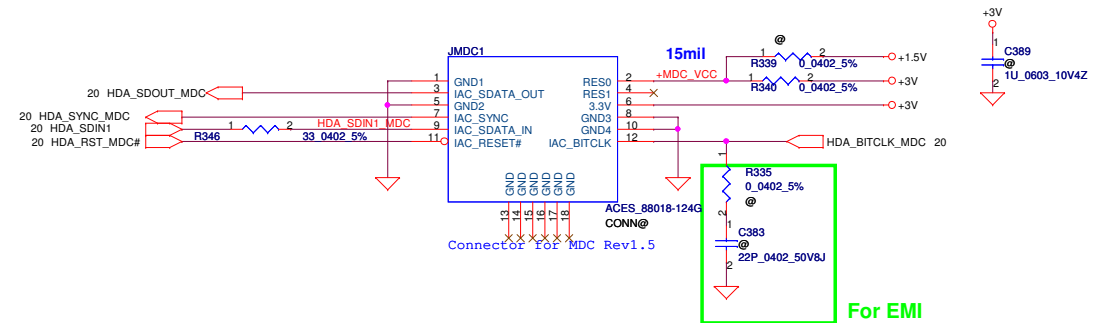
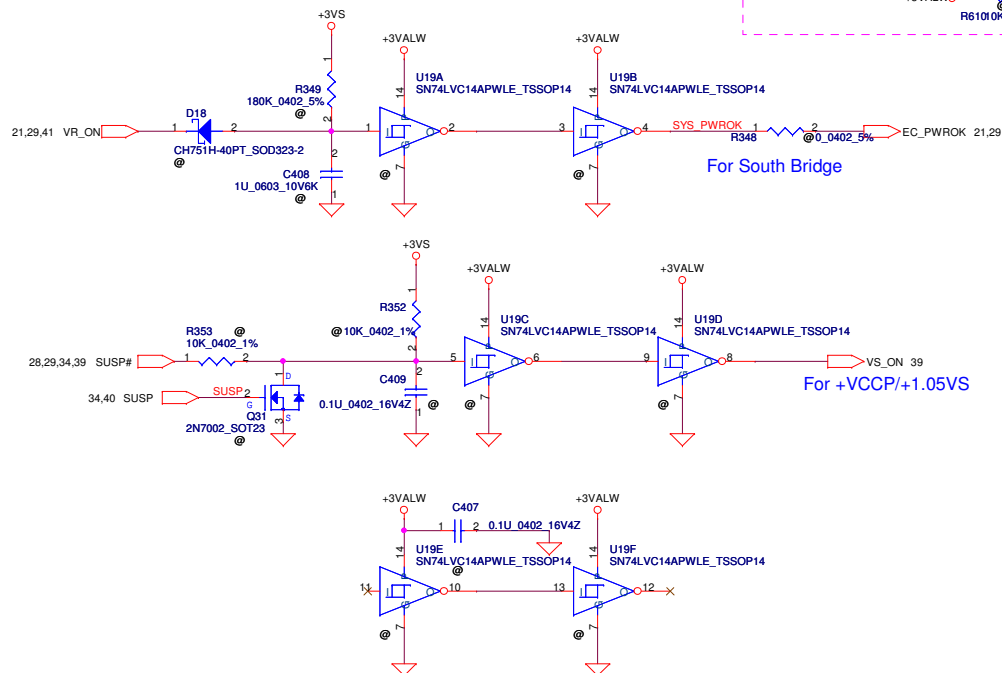
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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				Date	Wednesday, March 03, 2010
				Sheet	30 of 45
				Rev	1.0

## Power Button

ON/OFF switch

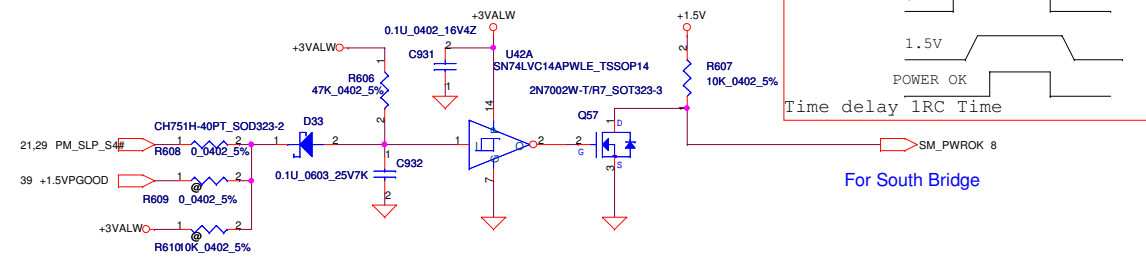
***HDA MDC Conn.***

### ***Power ON Circuit***



**For EMI**

## DDR3



For South Bridge

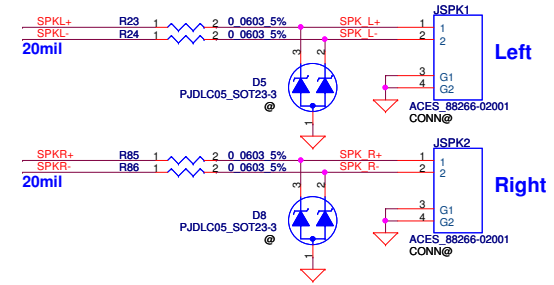
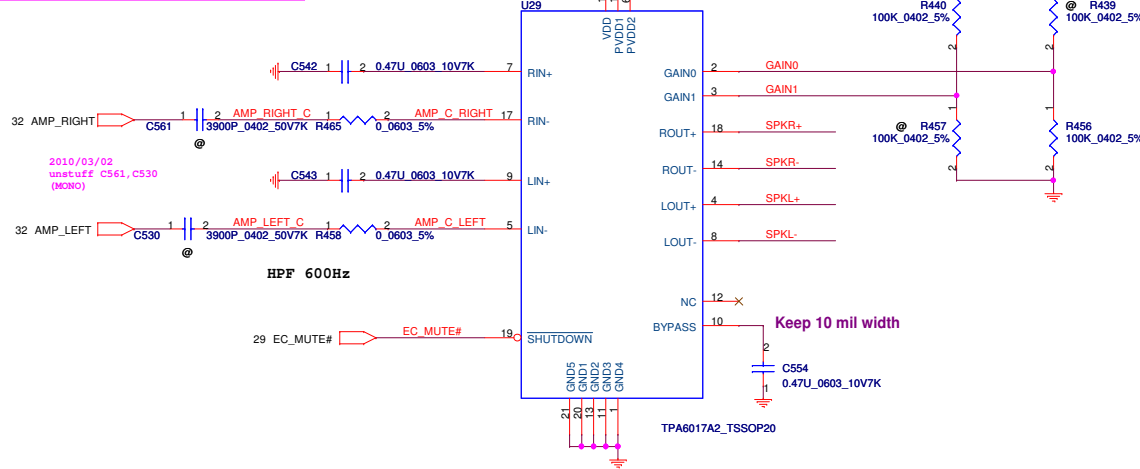
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	Power OK, Reset , MDC
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				NAWF3 M/B LA-4854P Schematic	
				Date	Wednesday, March 03, 2010

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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	HD Audio Codec ALC272
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				NAWF3 M/B LA-4854P Schematic	1.0
Date	Wednesday, March 03, 2010	Sheet	32	of	45

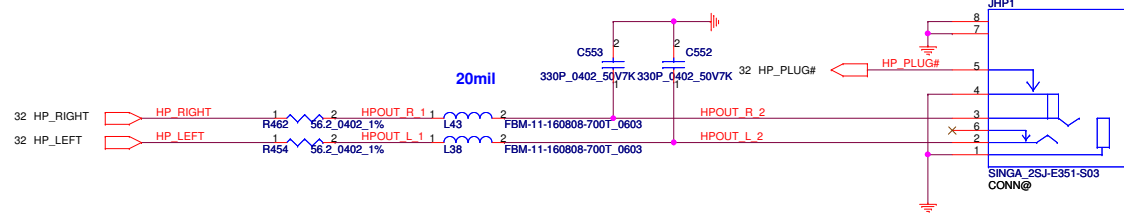
# Int. Speaker Conn.

2010/02/08  
Add Net name

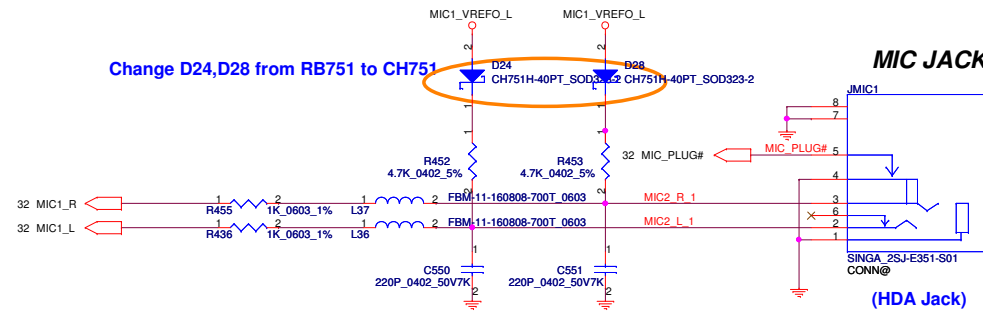
32 AMP\_RIGHT\_C AMP\_RIGHT\_C  
32 AMP\_LEFT\_C AMP\_LEFT\_C



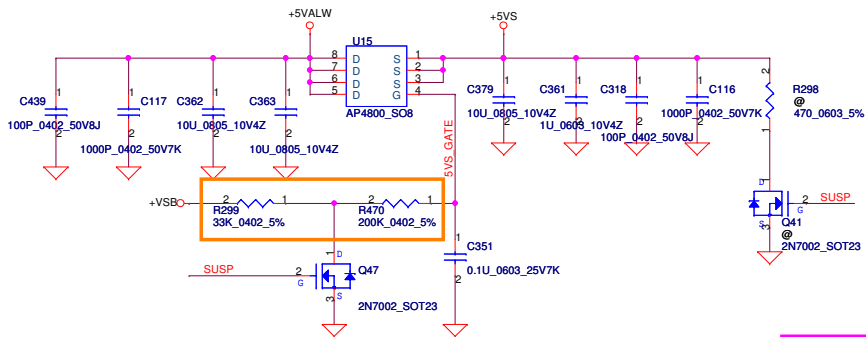
## LINE Out/Headphone Out



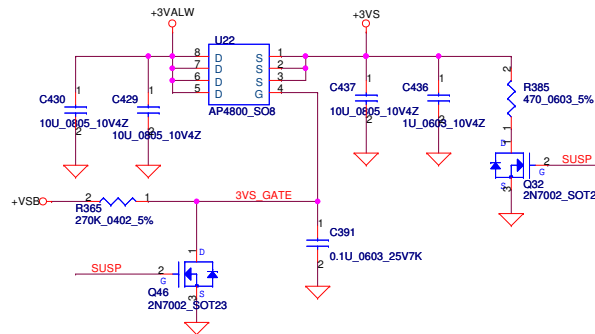
Change D24,D28 from RB751 to CH751



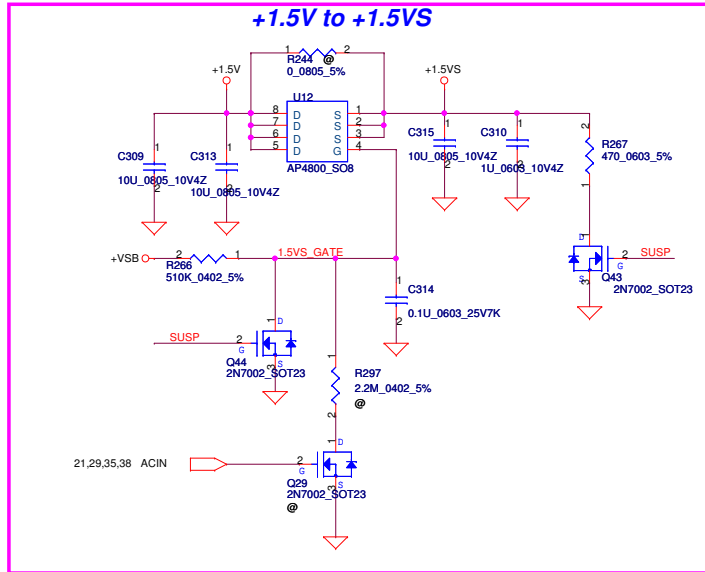
### +5VALW TO +5VS



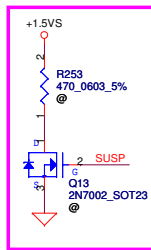
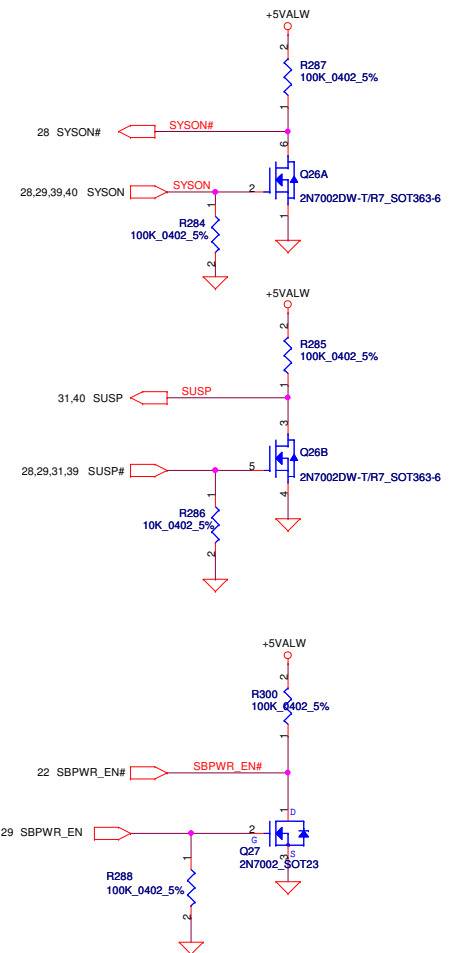
### +3VALW TO +3VS



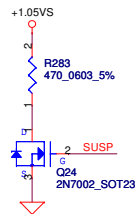
### +1.5V to +1.5VS



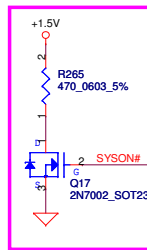
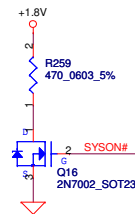
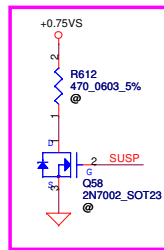
PVT2 for 8/24



PVT2 for 8/24

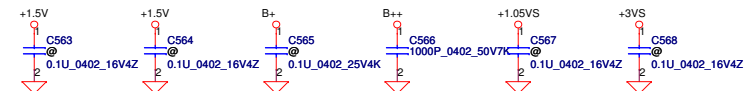


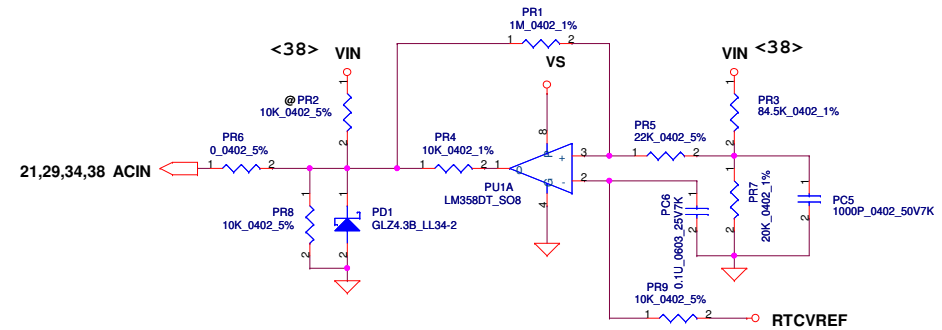
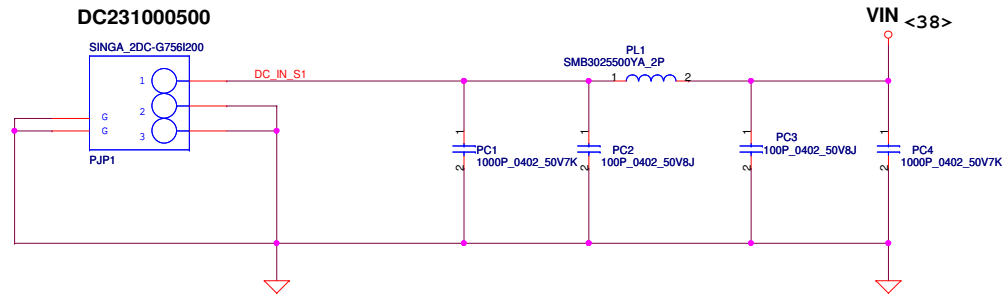
PVT2 for 8/24



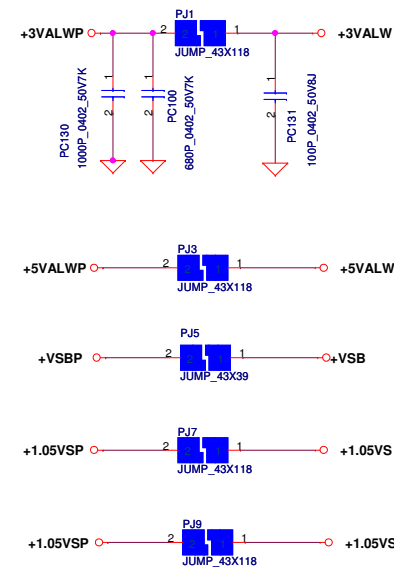
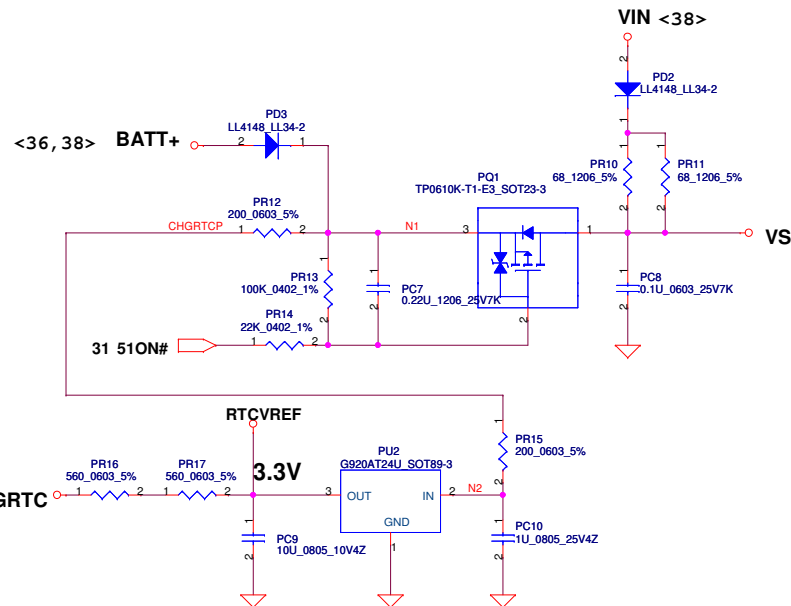
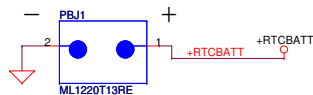
PVT2 for 8/24

### Reserve for EMI request

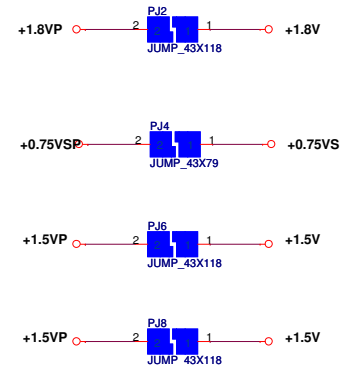


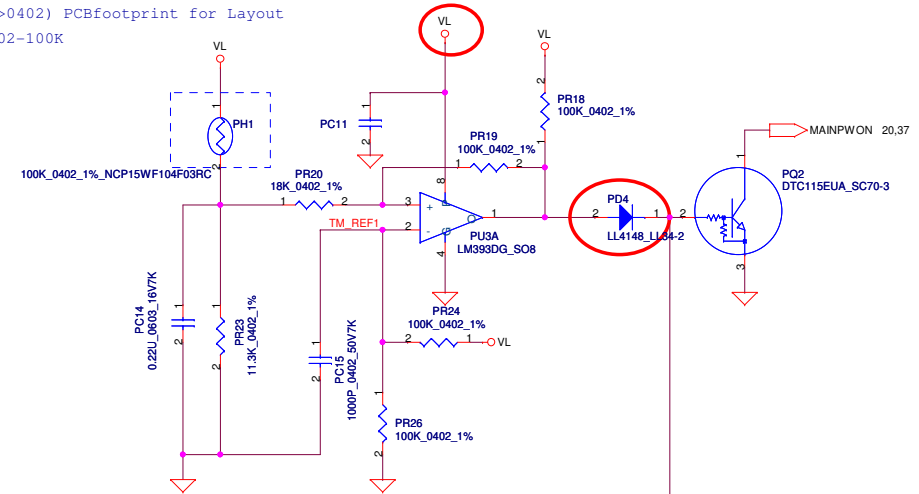
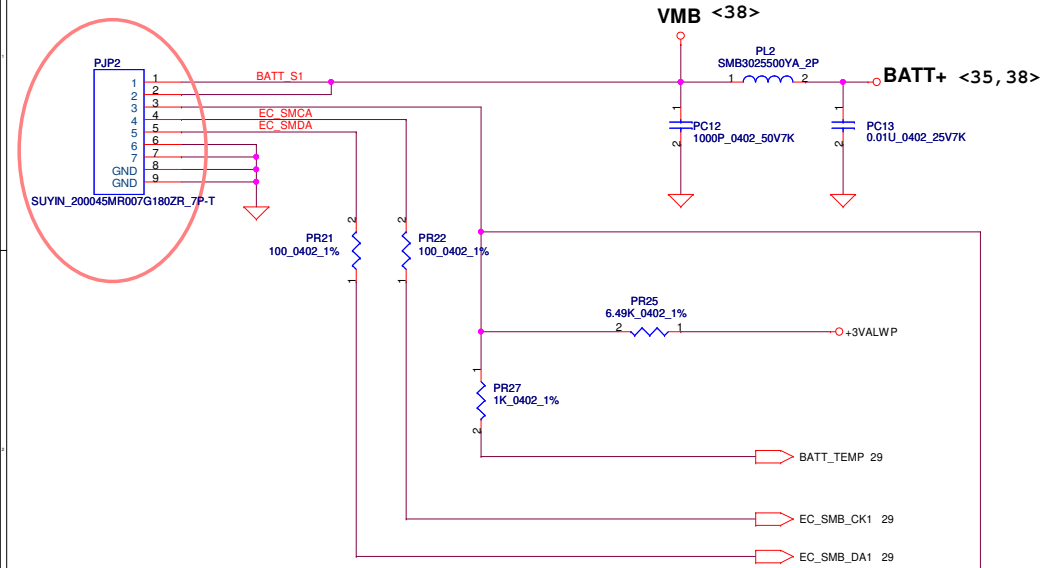


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



Delete (PJ16/PJ17/PJ18)  
1.1VLD0 + VGA\_CORE JUMPER





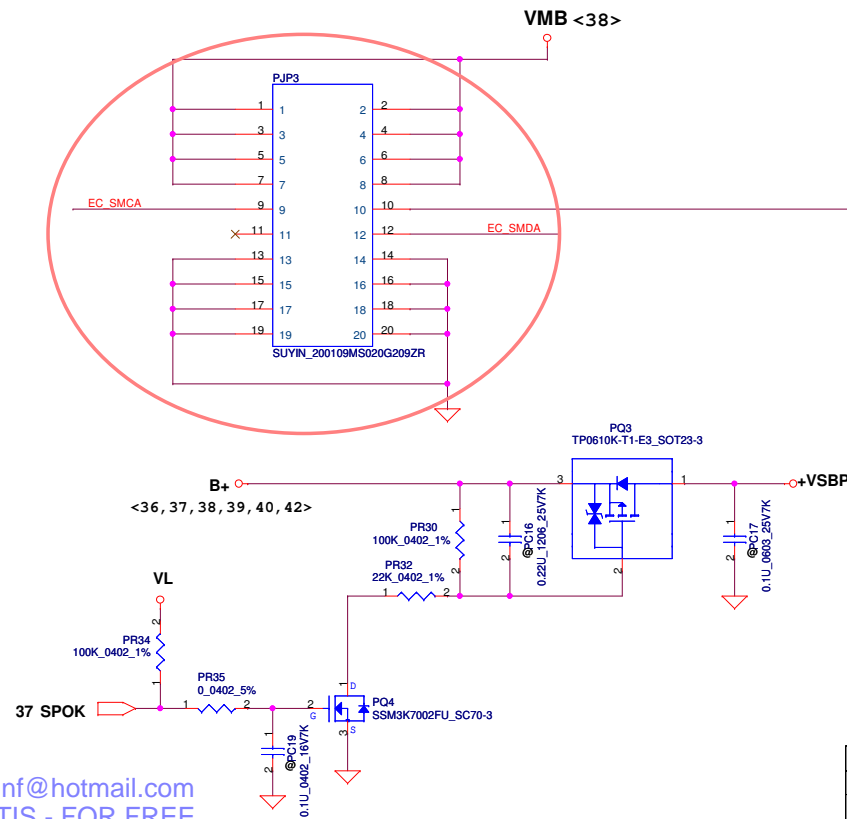
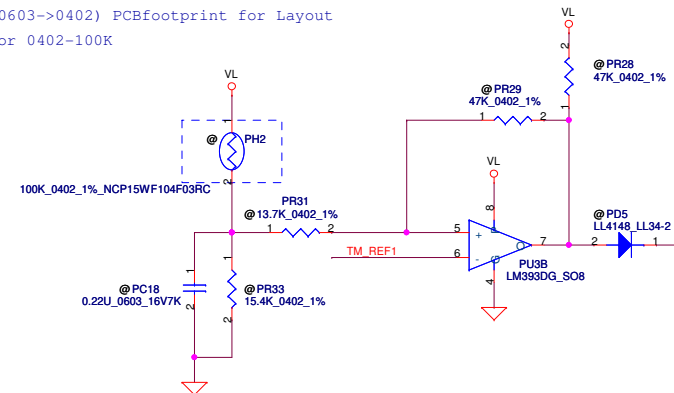
**PH2 near main Battery CONN :**

BAT. thermal protection at 90 degree C

Recovery at 70 degree C

2009\_08\_06 (0603->0402) PCBfootprint for Layout

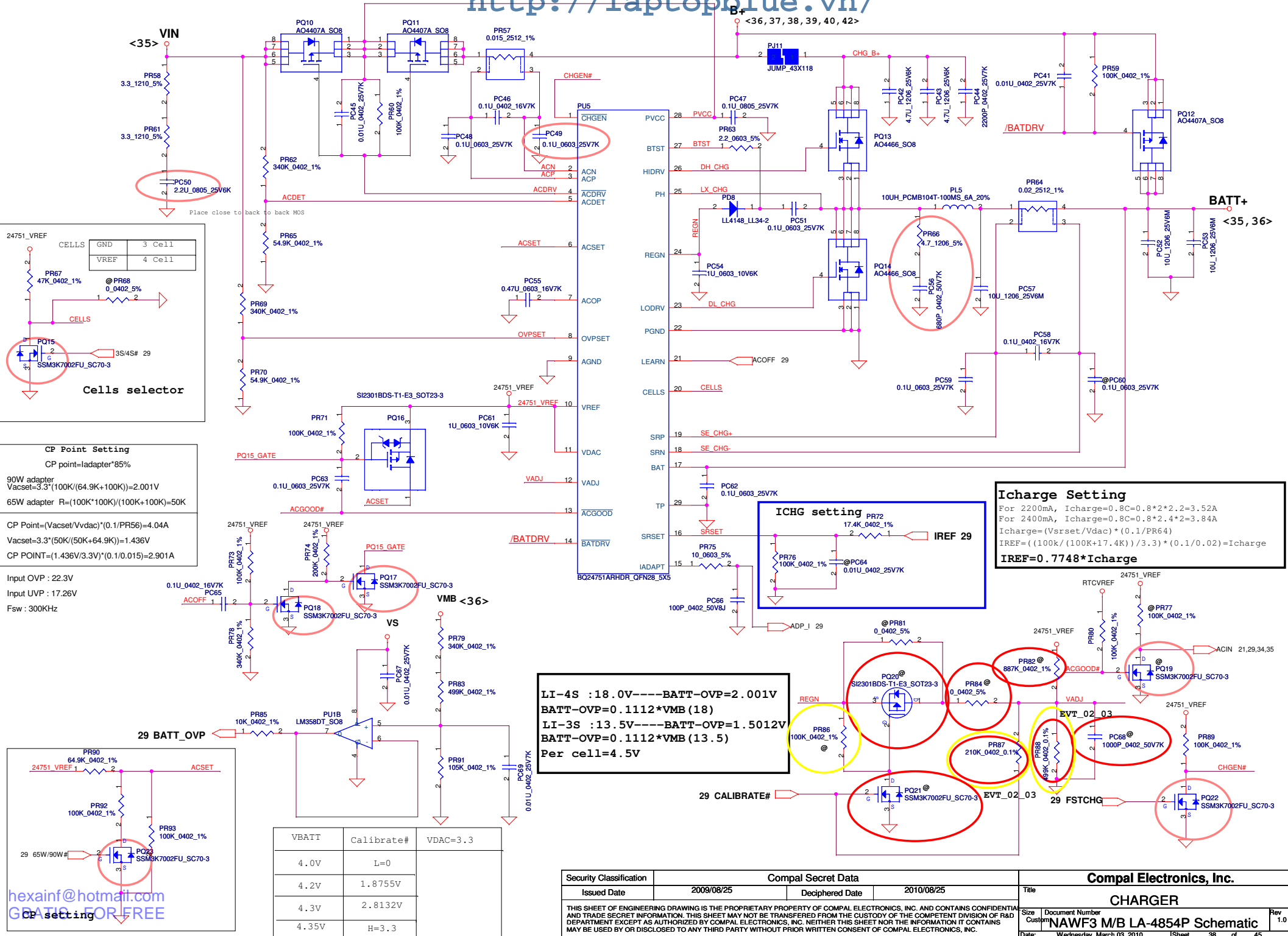
Change P/N for 0402-100K

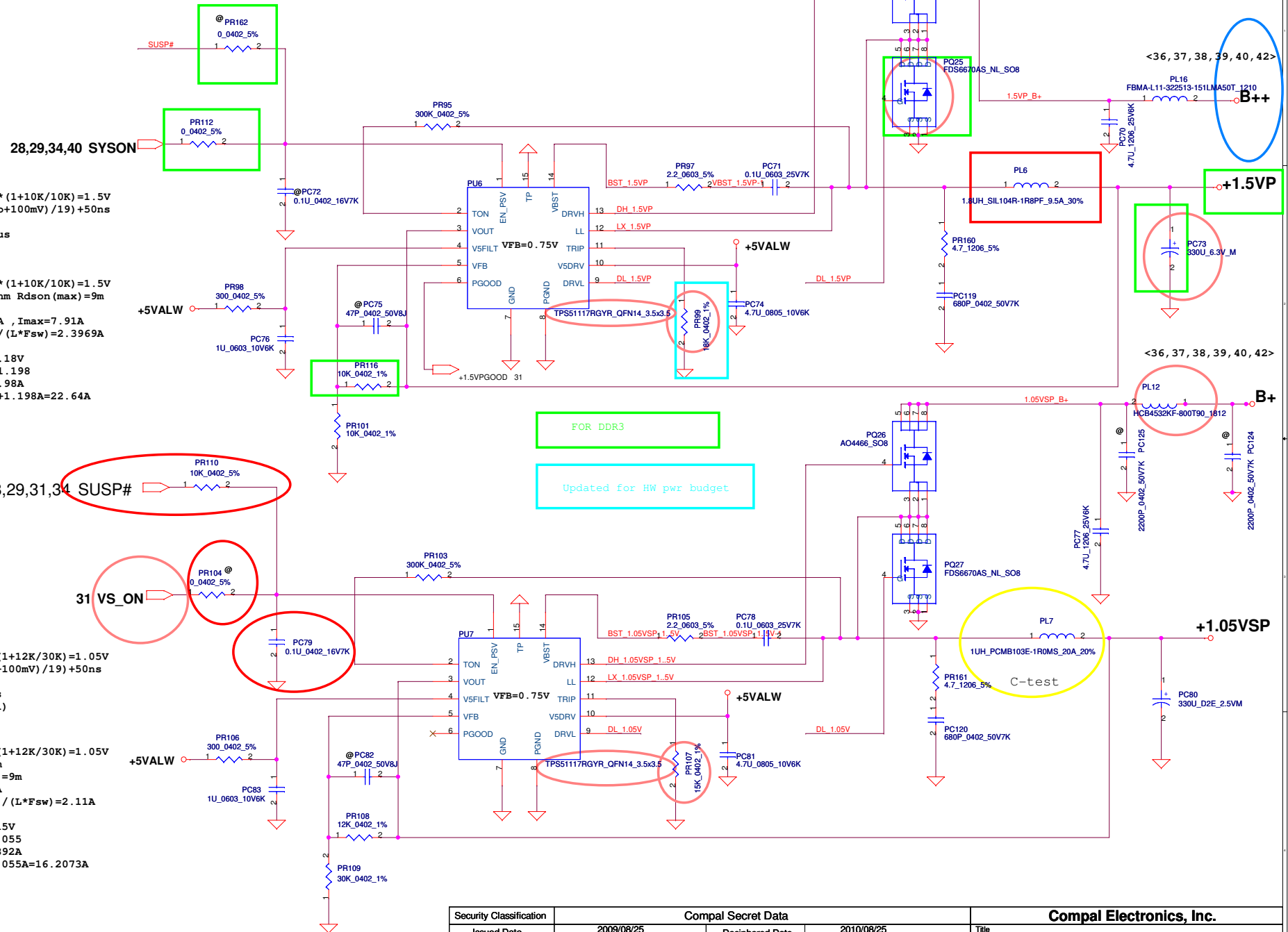


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						Size Custom		Document Number		Rev	
						Date		Wednesday, March 03, 2010		Sheet 36 of 45	
						NAWF3 M/B LA-4854P Schematic					
						1.0					

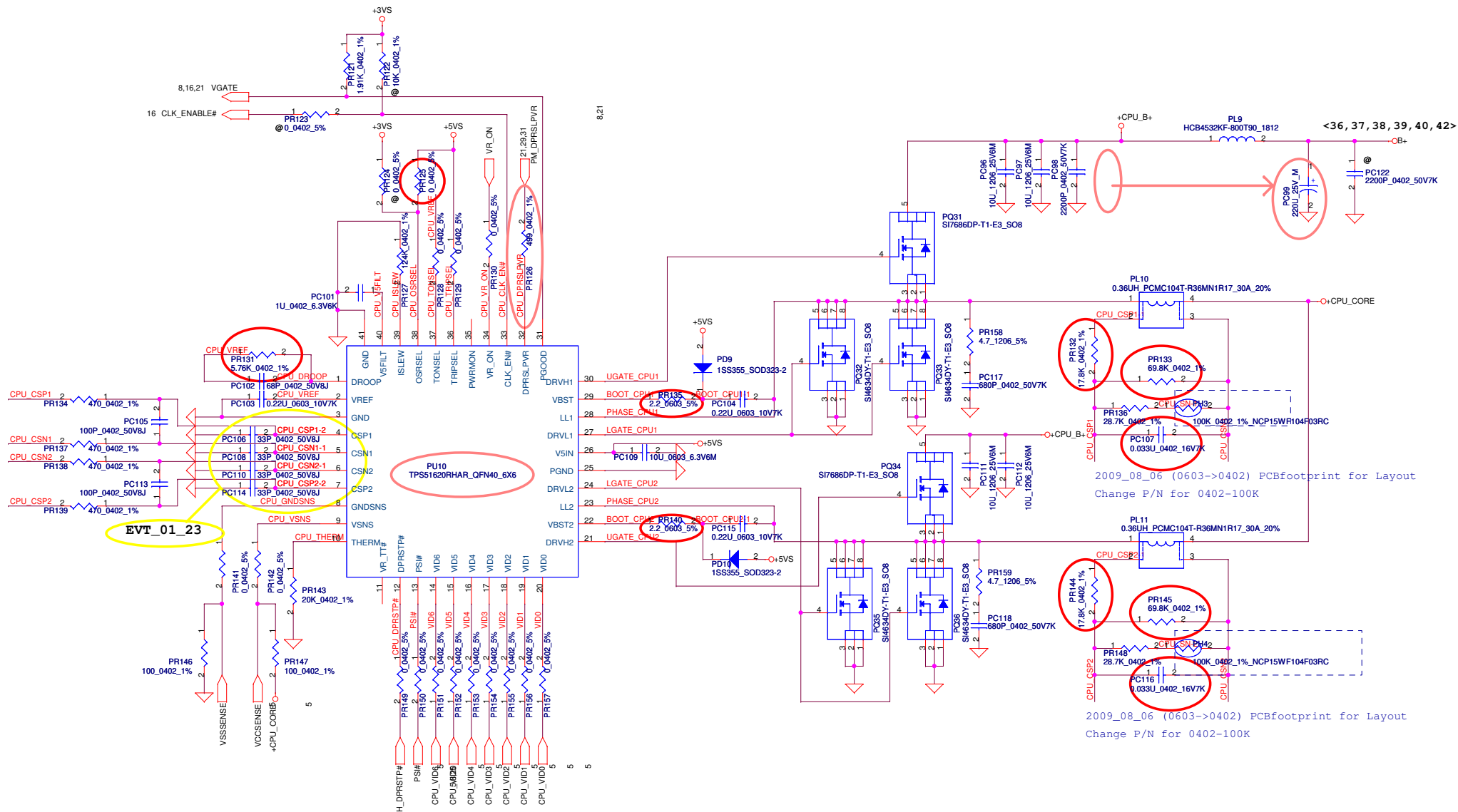












Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Size		Document Number		Rev	
Custom		NAWF3 M/B LA-4854P Schematic		1.0	
Date:		Wednesday, February 03, 2010		Sheet 42 of 45	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP  RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

COMPAL ELECTRONICS			
Title			
PIR POWER2			
Size	Document Number		Rev
	KAWF0 M/B LA-4431P Schematic		0.2
Date:	Wednesday, February 03, 2010		Sheet 43 of 45



Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 ( HCB4532KF-800T90_1812) Add PL 14 ( FBMA-L11-322513-151LMA50T_1210) Add PL 15 ( FBMA-L11-322513-151LMA50T_1210) Add PC126 ( 100P_0402_50V8J) Add PC128 ( 100P_0402_50V8J) Add PC129 ( 1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 ( 100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT
<div><div>COMPAL ELECTRONICS</div><div>Title<div>&lt;Title&gt;PIR POWER3</div></div><div><div>Size A</div><div>Document Number KAWF0 M/B LA-4431P Schematic</div><div>Rev 0.2</div></div><div>Date:Wednesday, February 03, 2010Sheet44of45</div></div>							

09/01 Change DDR2 as DDR3 PIR

- 1. P.8 Remove R181 ; Stuff R220, R222 ; Unstuff R221
- 2. P.14 Remove RP28, RP27, RP19, RP18, RP10, RP9, RP3, RP25, RP26, RP17, RP16, RP8, RP7, R138, R200, R195, R350, R351  
Remove C148, C186, C185, C134, C202, C415, C412, C413, C414, C187, C149, C146,C183, C188, C147, C203, C150, C135  
Remove C201, C204, C184, C200, C285, C411, C410  
Change JDIMM2 P/N  
Add R598~R602 ; C887~C908
- 3. P.15 Remove RP30, RP24, RP23, RP15, RP14, RP6, RP2, RP22, RP21, RP13, RP12, RP5, RP1, R137, R52, R53  
Remove C283, C284, C197, C181, C143, C198, C144, C182, C210, C180, C142, C131, C212, C133, C179  
Remove C211, C196, C199, C132, C209, C141, C140, C178, C145  
Change JDIMM1 P/N  
Add R603~R605 ; C909~C930
- 4. P.31 Add R608, R607, R606, C931, C932, D33, U42, Q57
- 5. P.34 Unstuff R244, R253, Q13 ; Stuff C309, C313, C310, C314, R266, R267, Q43, Q44, U12, R265, Q17

09/01 Other PIR

- 1. P.17 Unstuff D20, R411 ; Add R611 for DISPOFF#
- 2. P.19 Unstuff U8, R83 ; Add R614 for PLT\_RST#
- 3. P.21 Add U43 ; Remove R75 for ICH\_VGATE
- 4. P.23 Unstuff C570
- 5. P.30 Change LED1, LED2 P/N
- 6. P.32 Add D34, R613 for Audio BEEP#

09/17

- 1. P.25 Change C81, C82 27pF as 33pF for Xtal 25MHz(TXC suggest value)
- 2. P.20 Change C163, C164 18pF as 15pF for Xtal 32.768kHz (TXC suggest value)
- 3. P.29 Change R273 8.2k ohm as 18k ohm for Board ID

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Size	Customer	Document Number	NAWF3 M/B LA-4854P Schematic		Rev
Date	Wednesday, February 03, 2010	Sheet	45	of	45
				1.0	