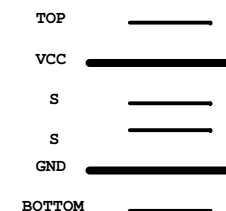


<http://laptopblue.vn/>

REVISION : PCB STACKUP

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number

JV42-DN

Date: Wednesday, November 18, 2009

Sheet 1 of 63

Rev	S
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http://mycomp.su/xl

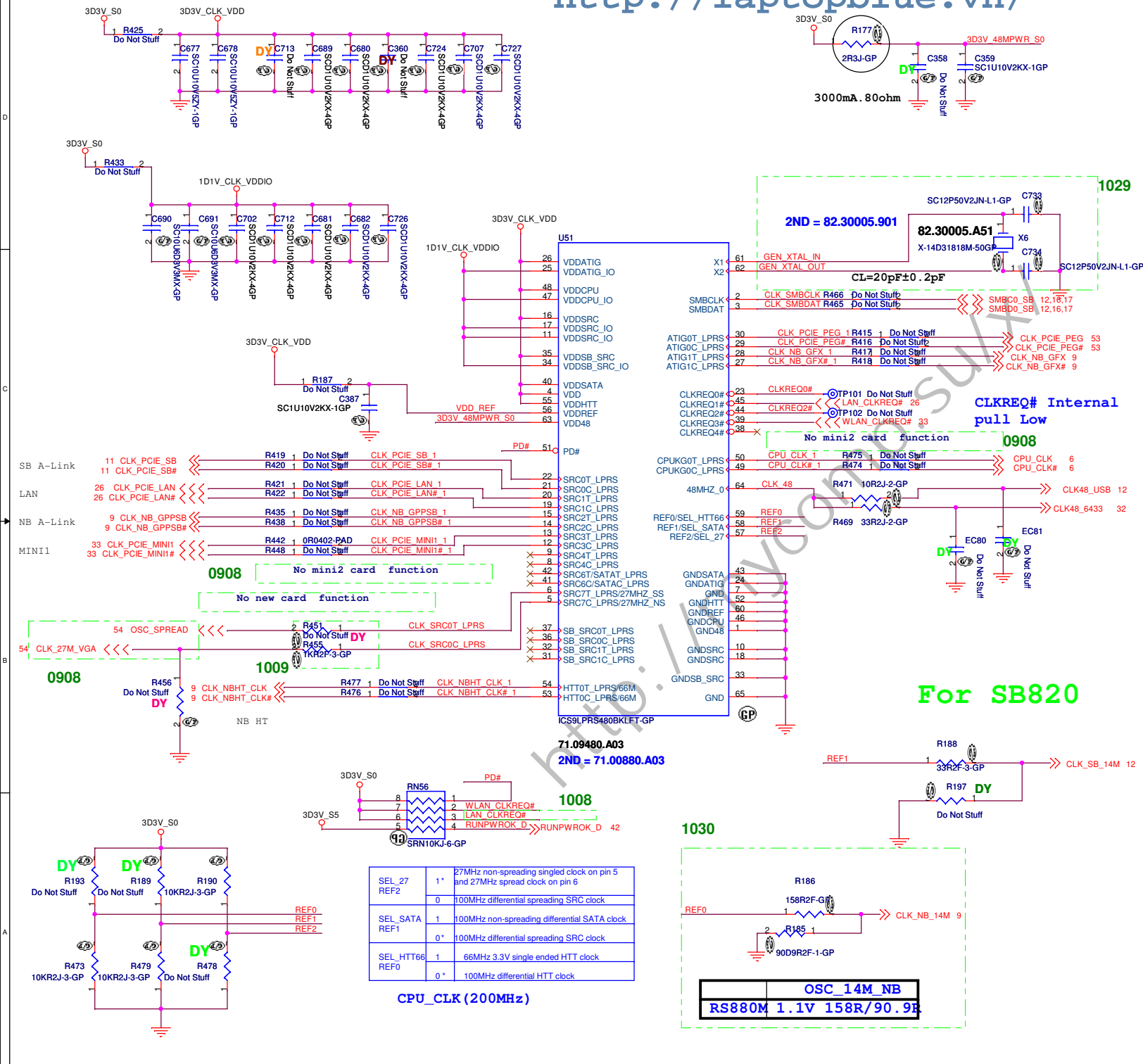
UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
History			
Size	Document Number		Rev
A3	JV42-DN		SA
Date: Thursday, November 05, 2009		Sheet	2 of 63

1

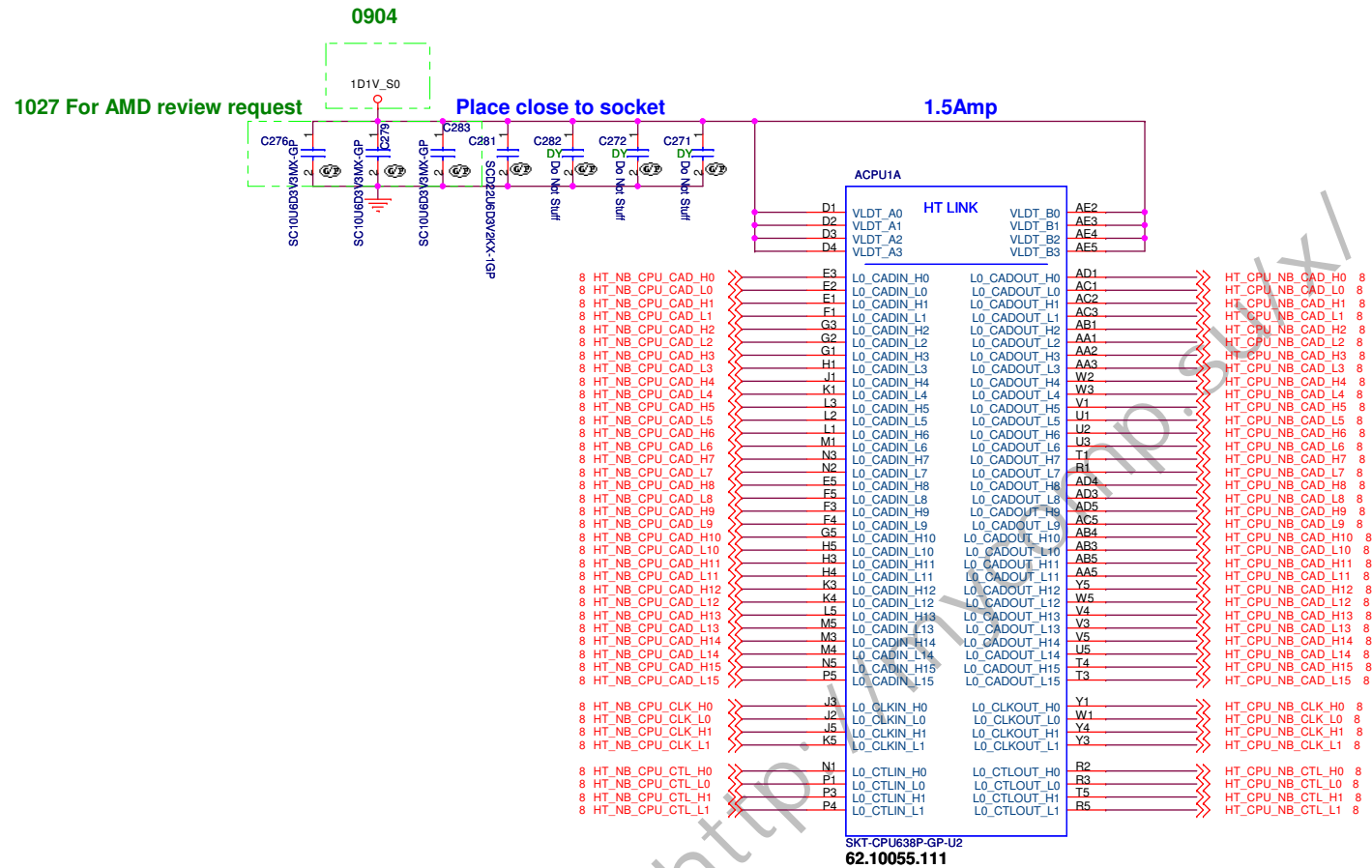
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

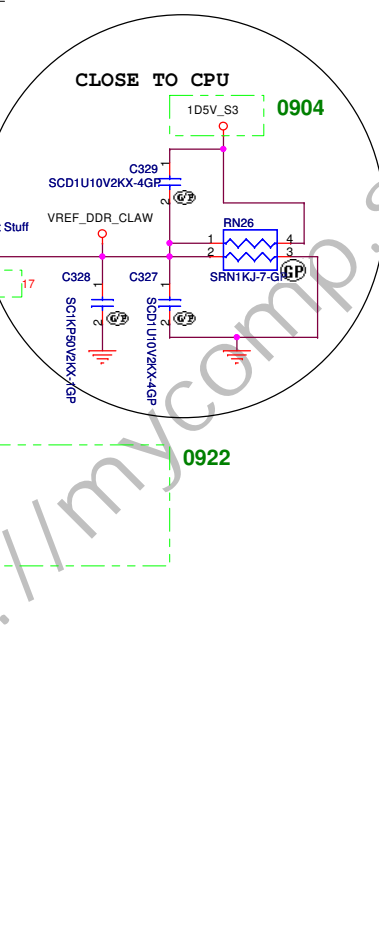
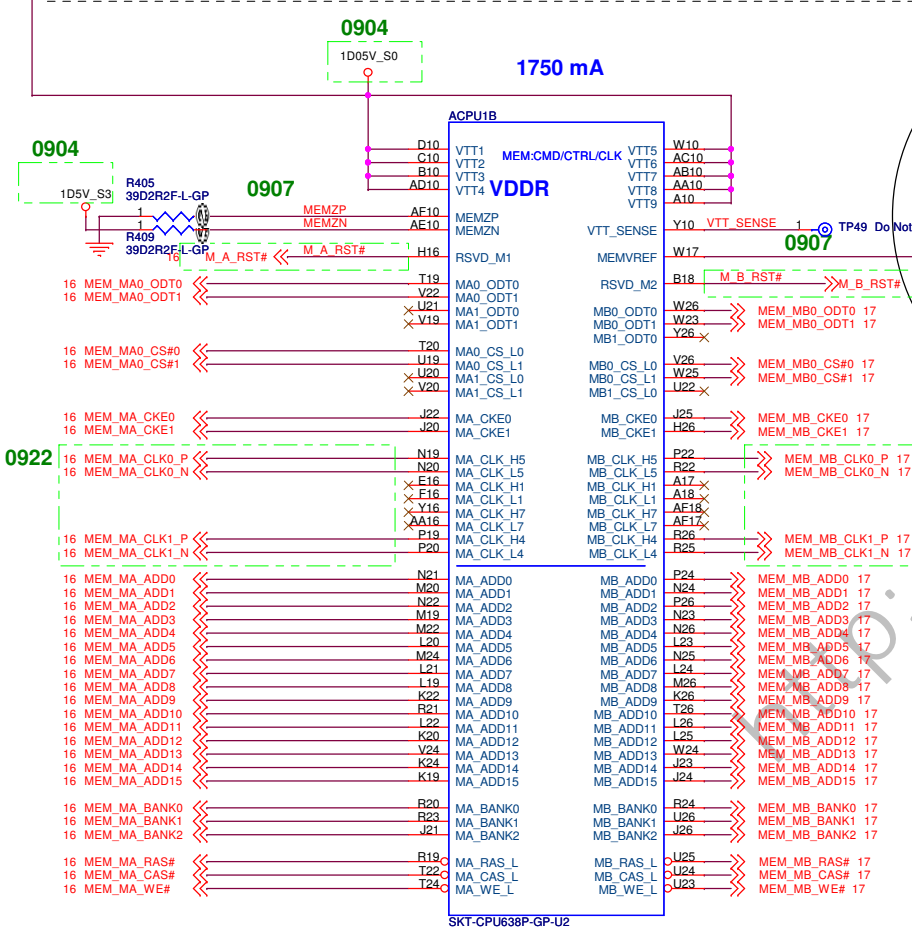
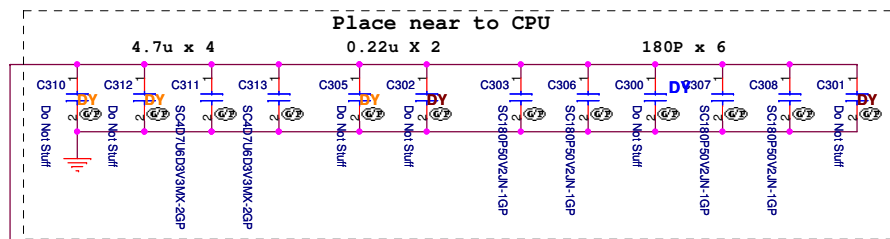


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Taipei Hsien 221, Taiwan, R.O.C.

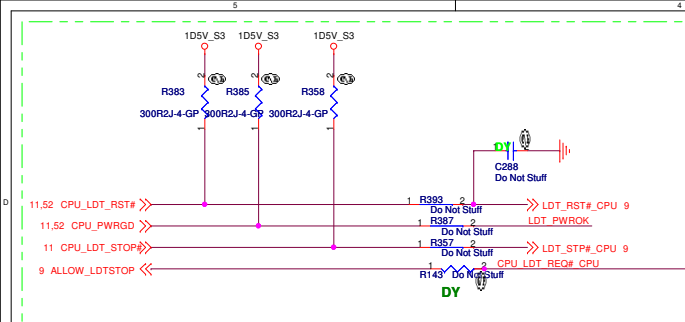


SKT-BGA638H176



		ACPUIC		MEM-DATA	
16	MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11
16	MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11
16	MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14
16	MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14
16	MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11
16	MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11
16	MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12
16	MEM_MA_DATA7	E13	MA_DATA7	MB_DATA7	A13
16	MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15
16	MEM_MA_DATA9	E15	MA_DATA9	MB_DATA9	A16
16	MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19
16	MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20
16	MEM_MA_DATA12	F14	MA_DATA12	MB_DATA12	C14
16	MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14
16	MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18
16	MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18
16	MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20
16	MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21
16	MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24
16	MEM_MA_DATA19	F20	MA_DATA19	MB_DATA19	C25
16	MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20
16	MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20
16	MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24
16	MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24
16	MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	F23
16	MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E22
16	MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25
16	MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26
16	MEM_MA_DATA28	E21	MA_DATA28	MB_DATA28	C26
16	MEM_MA_DATA29	E22	MA_DATA29	MB_DATA29	D26
16	MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23
16	MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	D24
16	MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	A24
16	MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23
16	MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24
16	MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AE24
16	MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	A26
16	MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25
16	MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AE25
16	MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AC22
16	MEM_MA_DATA40	AA20	MA_DATA40	MB_DATA40	AD22
16	MEM_MA_DATA41	AA18	MA_DATA41	MB_DATA41	AE20
16	MEM_MA_DATA42	AB18	MA_DATA42	MB_DATA42	AF20
16	MEM_MA_DATA43	AB21	MA_DATA43	MB_DATA43	AE24
16	MEM_MA_DATA44	AD21	MA_DATA44	MB_DATA44	AE23
16	MEM_MA_DATA45	AD19	MA_DATA45	MB_DATA45	AC20
16	MEM_MA_DATA46	Y18	MA_DATA46	MB_DATA46	AD20
16	MEM_MA_DATA47	AD17	MA_DATA47	MB_DATA47	AD18
16	MEM_MA_DATA48	W16	MA_DATA48	MB_DATA48	AE18
16	MEM_MA_DATA49	W14	MA_DATA49	MB_DATA49	AC14
16	MEM_MA_DATA50	Y14	MA_DATA50	MB_DATA50	AE14
16	MEM_MA_DATA51	Y17	MA_DATA51	MB_DATA51	AE19
16	MEM_MA_DATA52	AB17	MA_DATA52	MB_DATA52	AC18
16	MEM_MA_DATA53	AB15	MA_DATA53	MB_DATA53	AF16
16	MEM_MA_DATA54	AD15	MA_DATA54	MB_DATA54	AF15
16	MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AF15
16	MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AF13
16	MEM_MA_DATA57	Y12	MA_DATA57	MB_DATA57	AG12
16	MEM_MA_DATA58	W11	MA_DATA58	MB_DATA58	AB11
16	MEM_MA_DATA59	AB14	MA_DATA59	MB_DATA59	Y11
16	MEM_MA_DATA60	AA14	MA_DATA60	MB_DATA60	AF14
16	MEM_MA_DATA61	AB12	MA_DATA61	MB_DATA61	AF11
16	MEM_MA_DATA62	AA12	MA_DATA62	MB_DATA62	AD11
16	MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11
16	MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12
16	MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16
16	MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22
16	MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25
16	MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26
16	MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22
16	MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16
16	MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12
16	MEM_MA_DQ0_S_P	G13	MA_DQ0_S_H0	MB_DQ0_S_H0	C12
16	MEM_MA_DQ0_S_N	H13	MA_DQ0_S_L0	MB_DQ0_S_L0	D12
16	MEM_MA_DQ0_S_P	G16	MA_DQ0_S_H1	MB_DQ0_S_H1	B16
16	MEM_MA_DQ0_S_N	G15	MA_DQ0_S_L1	MB_DQ0_S_L1	C16
16	MEM_MA_DQ0_S2_P	C22	MA_DQ0_S_H2	MB_DQ0_S_H2	A24
16	MEM_MA_DQ0_S2_N	G22	MA_DQ0_S_L2	MB_DQ0_S_L2	E26
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16	MEM_MA_DQ0_S3_N	MA_DQ0_S_L3	MB_DQ0_S_L3		AC25
16	MEM_MA_DQ0_S4_P	AD23	MA_DQ0_S_H4	MB_DQ0_S_H4	AC26
16	MEM_MA_DQ0_S4_N	AC23	MA_DQ0_S_L4	MB_DQ0_S_L4	AF21
16	MEM_MA_DQ0_S5_P	AB19	MA_DQ0_S_H5	MB_DQ0_S_H5	AF22
16	MEM_MA_DQ0_S5_N	AB20	MA_DQ0_S_L5	MB_DQ0_S_L5	AE16
16	MEM_MA_DQ0_S6_P	Y15	MA_DQ0_S_H6	MB_DQ0_S_H6	AD16
16	MEM_MA_DQ0_S6_N	W15	MA_DQ0_S_L6	MB_DQ0_S_L6	AF12
16	MEM_MA_DQ0_S7_P	W12	MA_DQ0_S_H7	MB_DQ0_S_H7	AE12
16	MEM_MA_DQ0_S7_N	W13	MA_DQ0_S_L7	MB_DQ0_S_L7	AE12

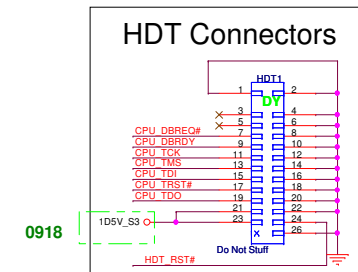
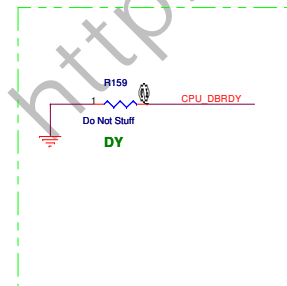
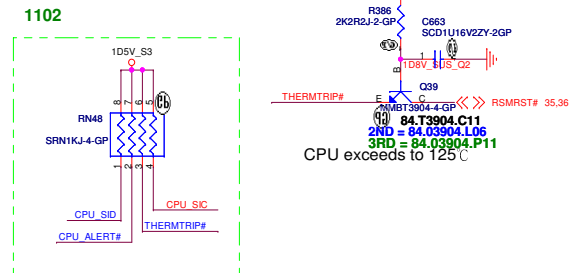
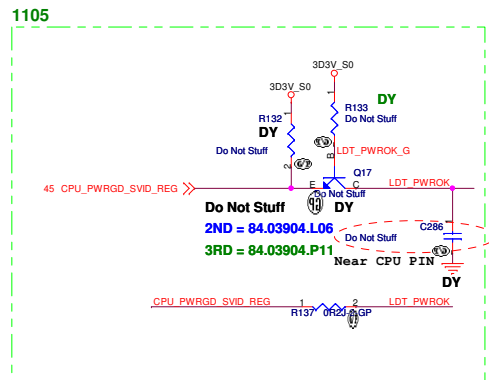
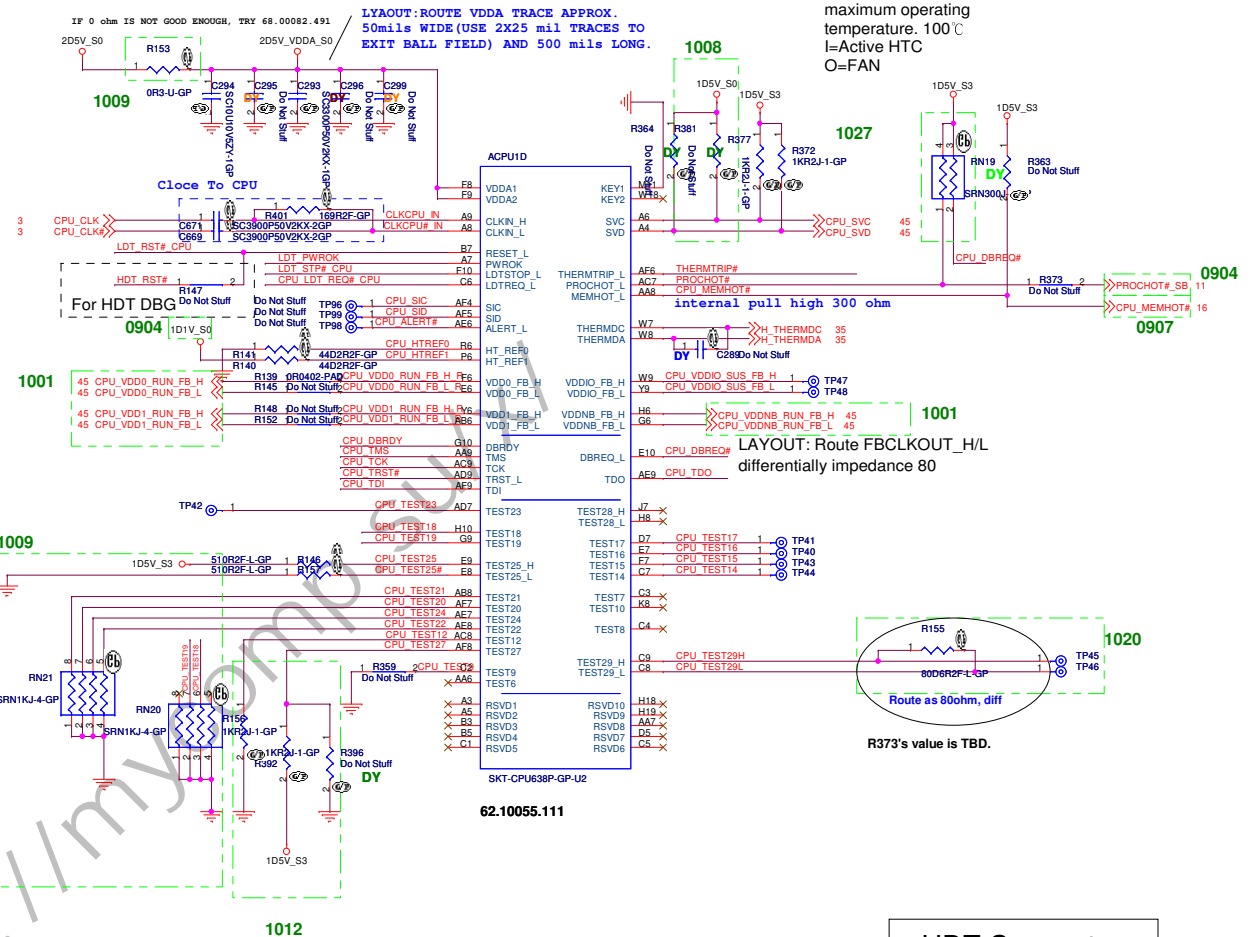
SKT-CPUG38P-GP-U2



0929

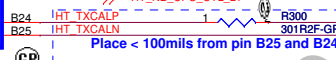
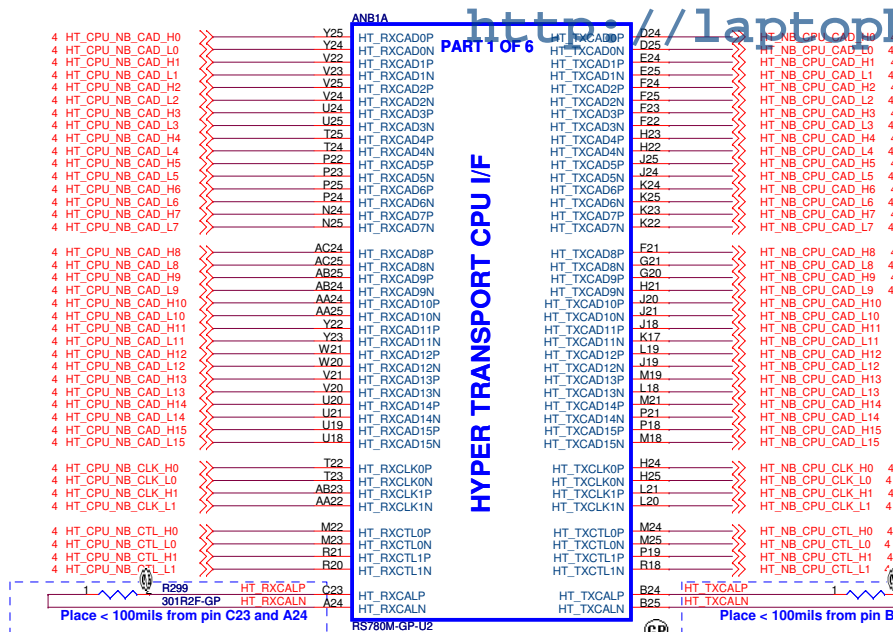
<http://laptopblue.vn/>

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

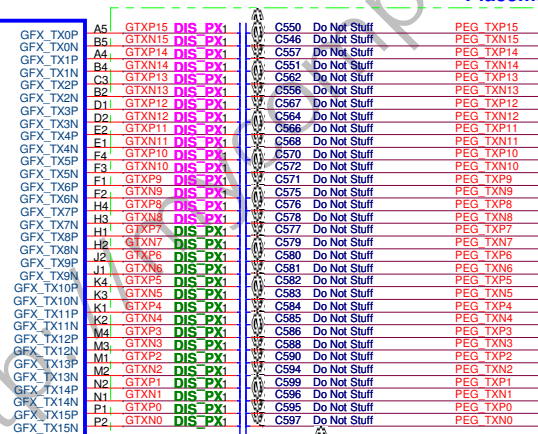
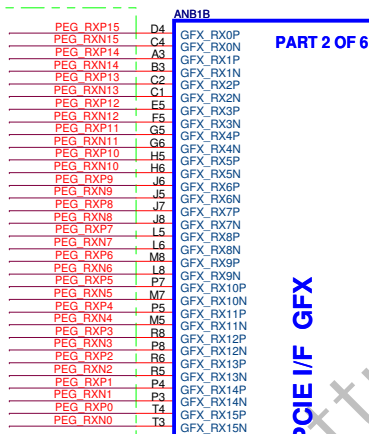




HYPER TRANSPORT CPU I/F



0915
Exchange



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PEG_TXN[15..0] 53

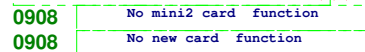
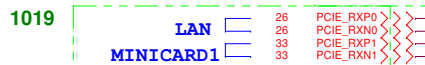
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1030 for HDMI function

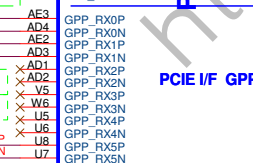
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GTNX15	UMA	C549	1	SCD1U16V2KX-3GP	HDMI_DATA2-	21
GTXP14	UMA	C561	1	SCD1U16V2KX-3GP	HDMI_DATA1+	21
GTNX14	UMA	C555	1	SCD1U16V2KX-3GP	HDMI_DATA1-	21
GTXP13	UMA	C563	1	SCD1U16V2KX-3GP	HDMI_DATA0+	21
GTNX13	UMA	C560	1	SCD1U16V2KX-3GP	HDMI_DATA0-	21
GTXP12	UMA	C569	1	SCD1U16V2KX-3GP	HDMI_CLK+	21
GTNX12	UMA	C565	1	SCD1U16V2KX-3GP	HDMI_CLK-	21

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

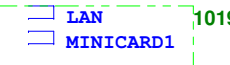
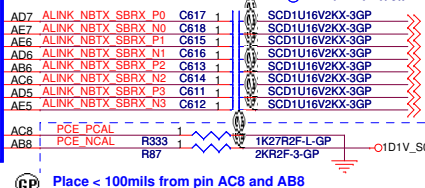
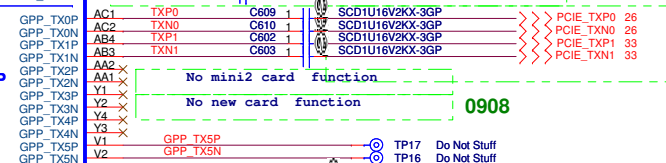


A-LINK



PCIE I/F GPR

PCIE I/F SB

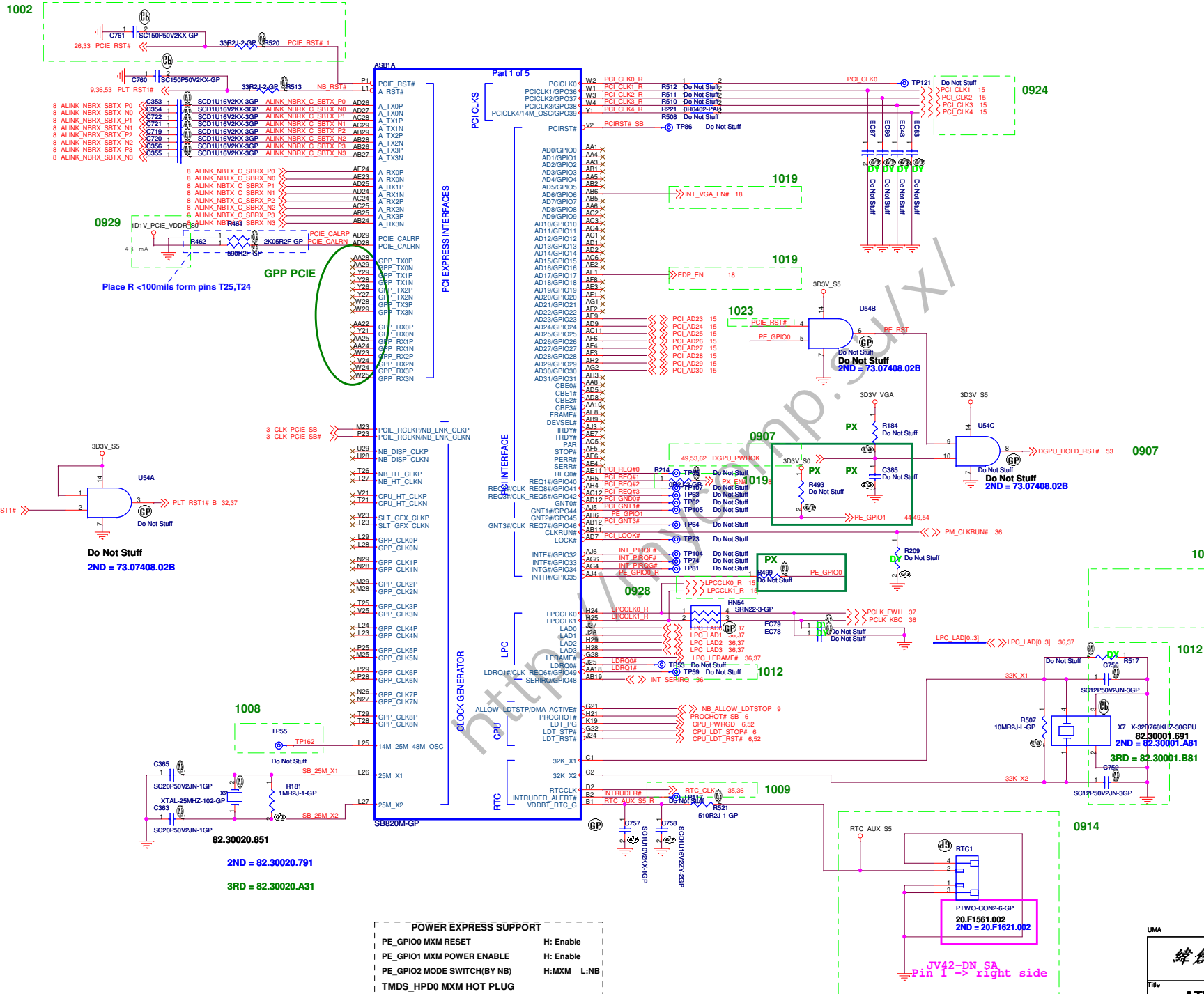


0915
Exchange

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				ATi-RS880M_HT LINK&PCle(1/3)			
Size		Document Number				Rev	
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Date: Thursday, November 05, 2009				Sheet 8 of		63	



USB	
Pair	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CAR
0	USB1

UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ATi-SB820 USB&GPIO (2/5)

Size	
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Document Number

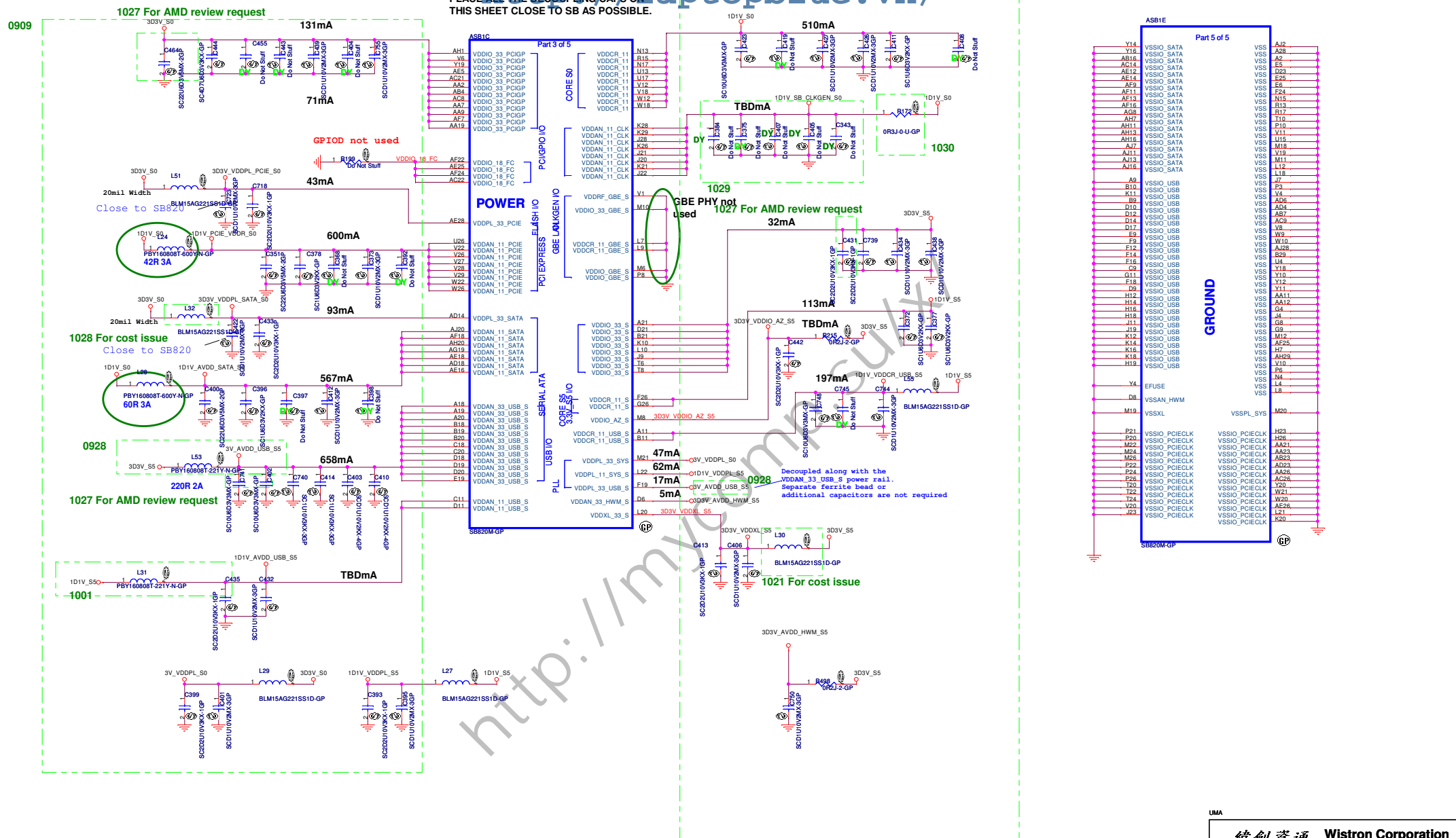
JV42-DN

Rev

Date: Th

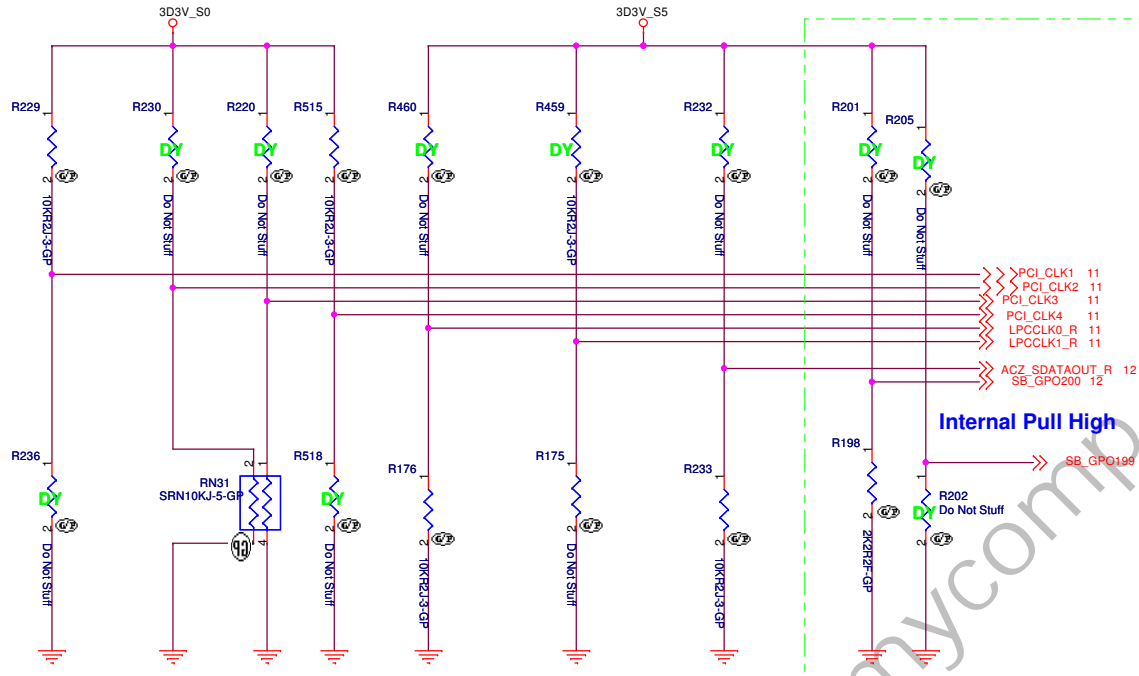
Thursday, November 01





REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1002

DEBUG STRAPS

Do Not Stuff	TP67	PCI_AD23	11
Do Not Stuff	TP70	PCI_AD24	11
Do Not Stuff	TP66	PCI_AD25	11
Do Not Stuff	TP77	PCI_AD26	11
Do Not Stuff	TP80	PCI_AD27	11
Do Not Stuff	TP110	PCI_AD28	11
Do Not Stuff	TP108	PCI_AD29	11
Do Not Stuff	TP111	PCI_AD30	11

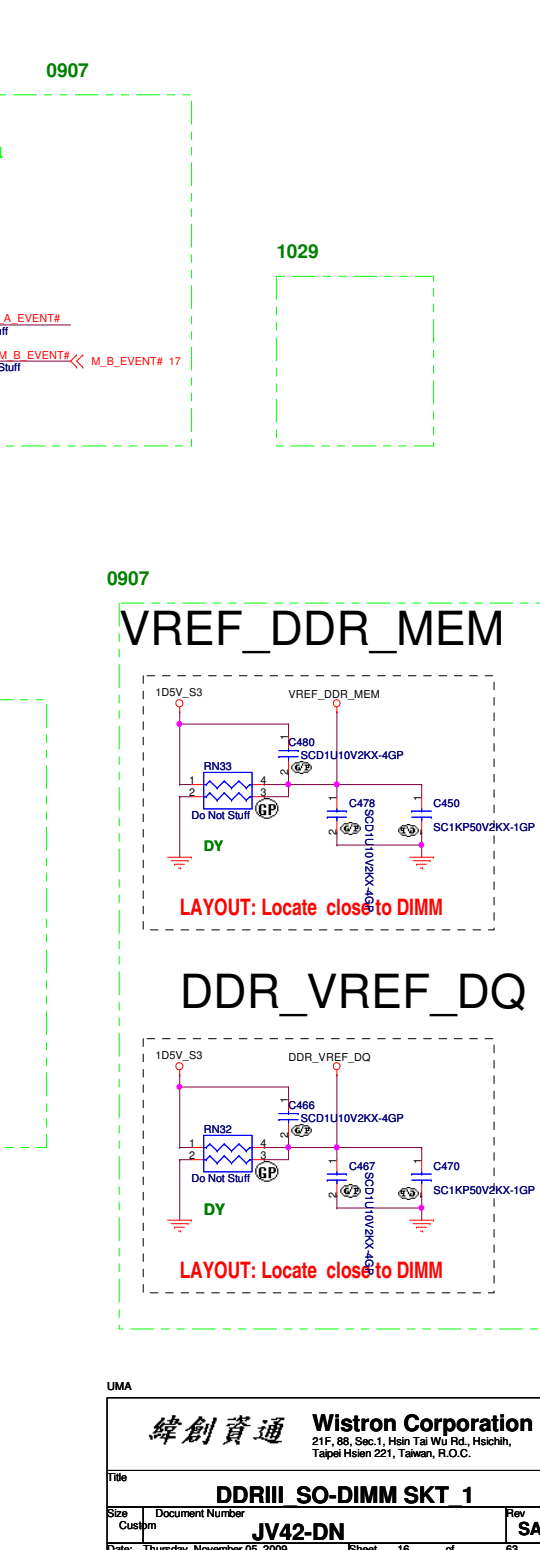
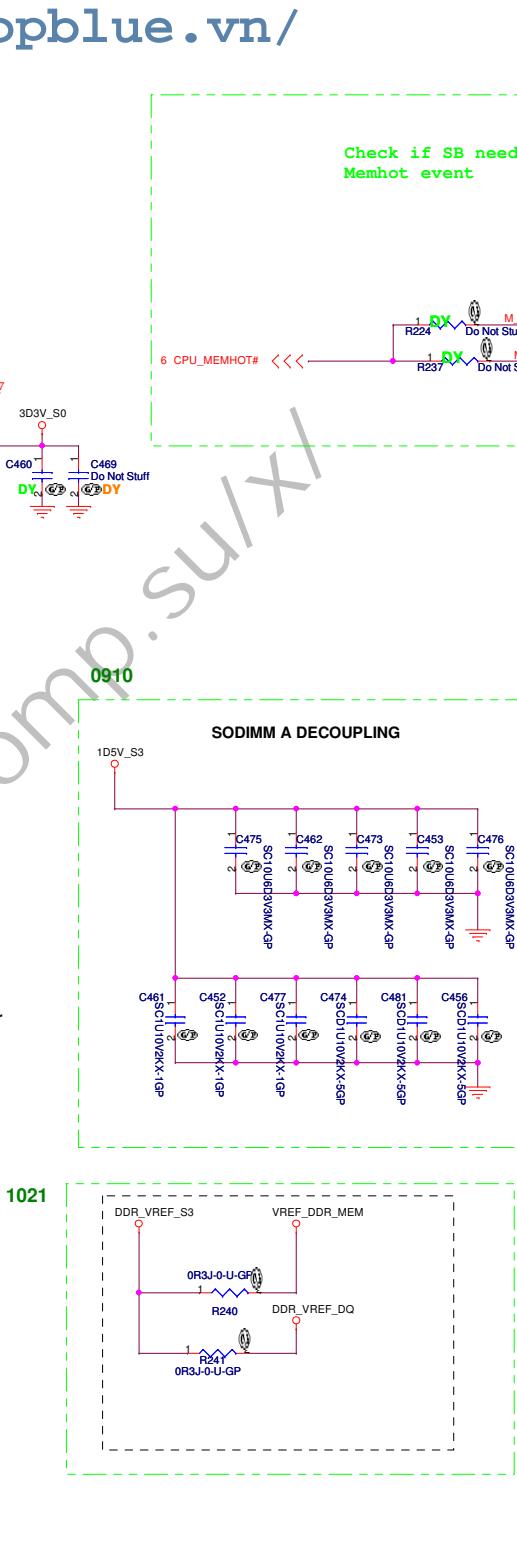
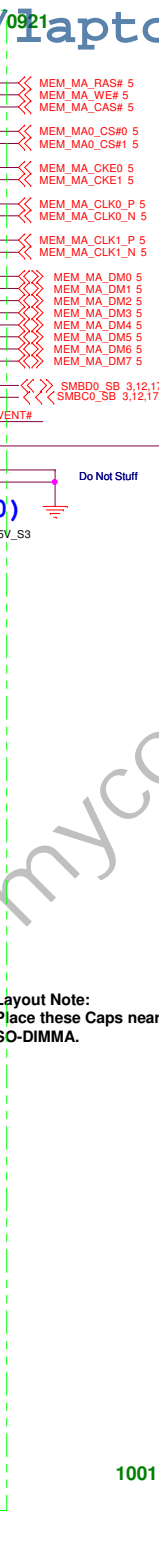
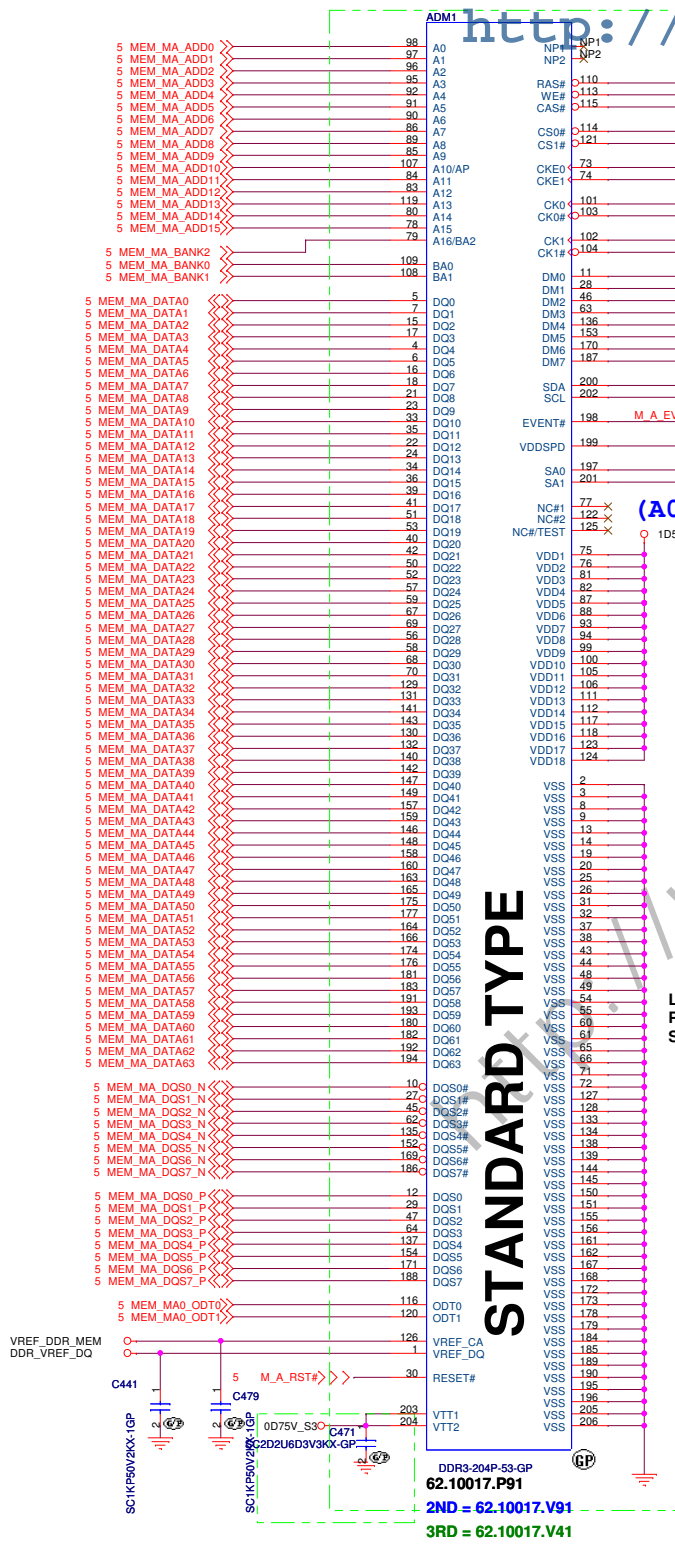
	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCI Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCI Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

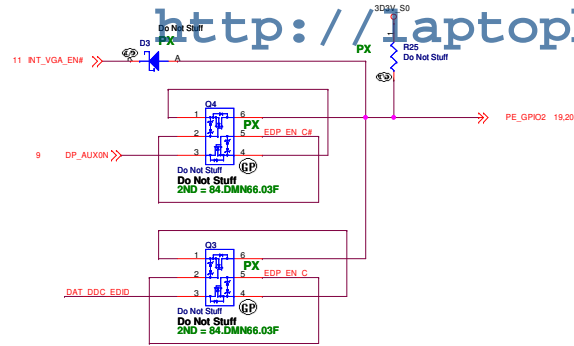
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ATI-SB820 STRAPPING (5/5)		
Size	Document Number				Rev
A3	JV42-DN				SA
Date:	Wednesday, November 18, 2009		Sheet	15	of 63





Function	SEL
A_N to NB_1	L
A_N to NB_2	H

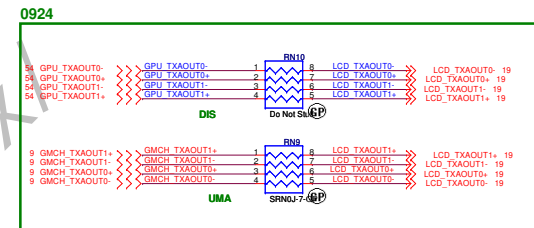
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

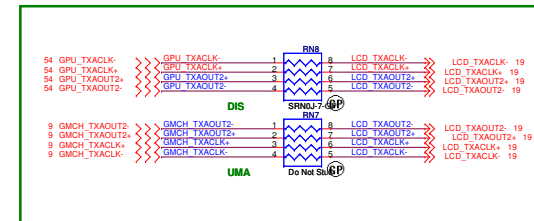
H = HIGH Logic Level L = LOW Logic Level

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

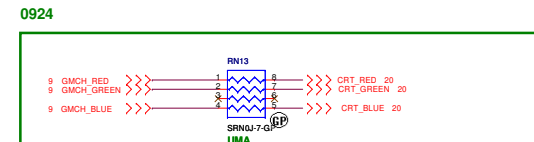
H = HIGH Logic Level L = LOW Logic Level



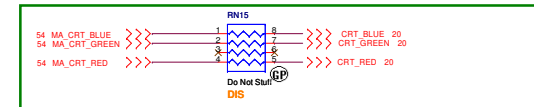
None PX



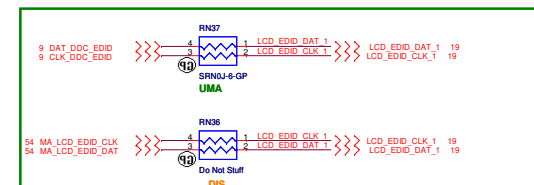
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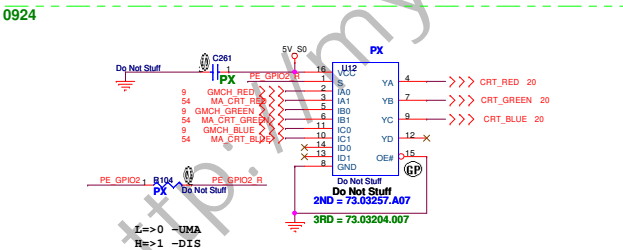
SRN0J-7-GP



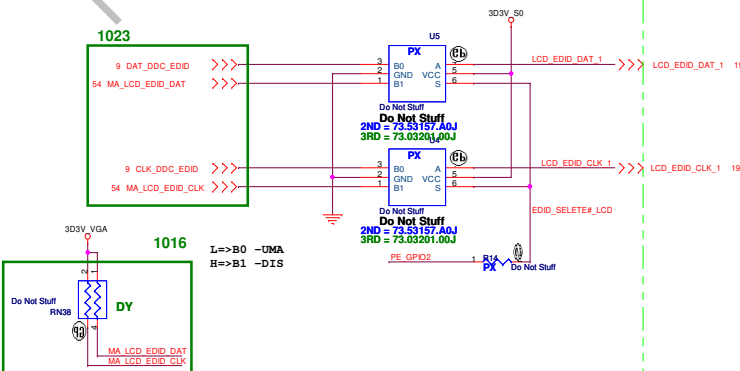
None PX



None PX

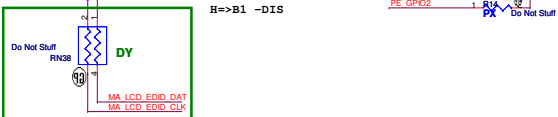


L=>0 -UMA
H=>1 -DIS



L=>B0 -UMA

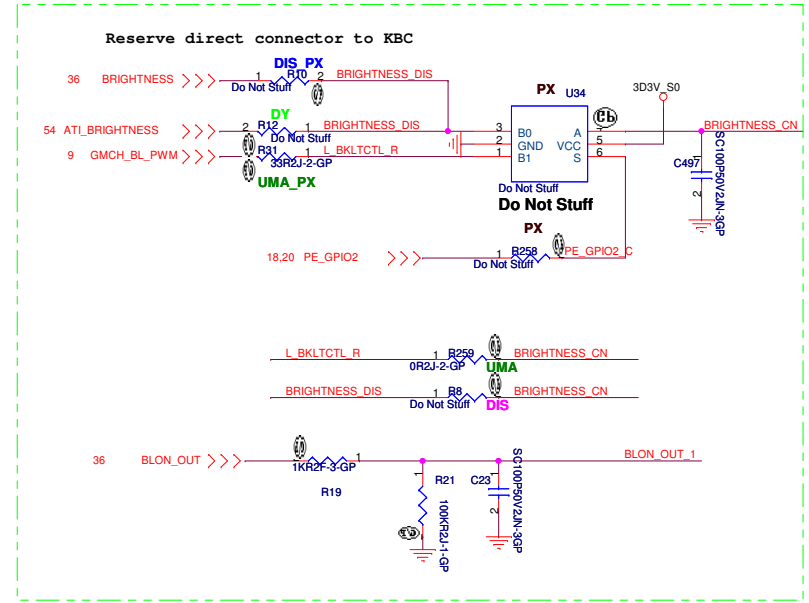
PE GPIO2 1 R14 PX Do Not Stuff



Change PX

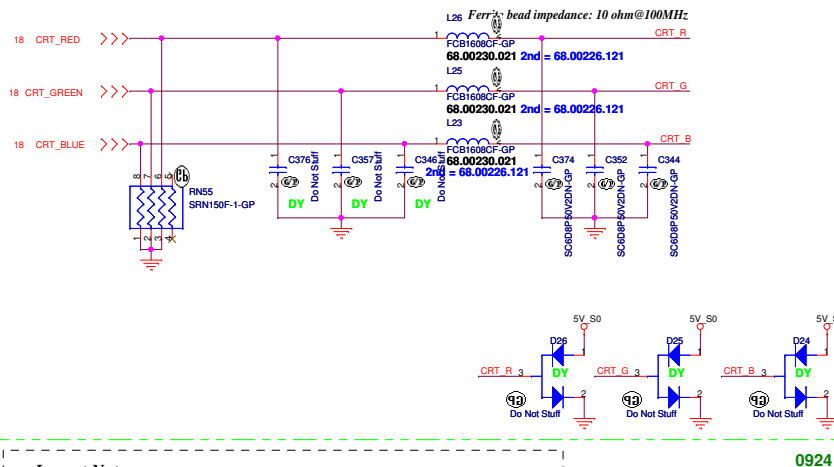


CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



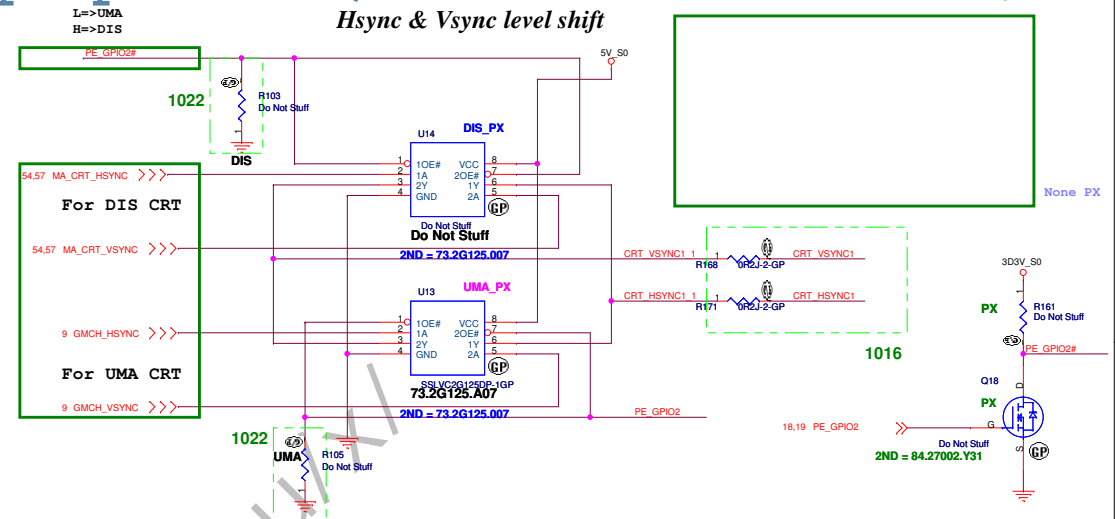
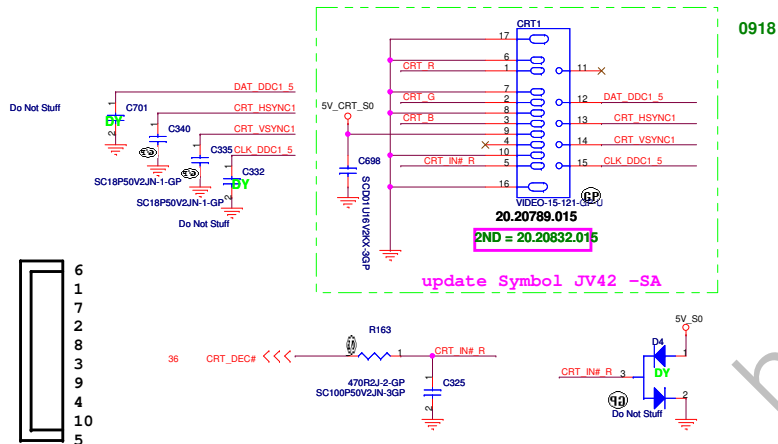
UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD CONN			
Size	Document Number		Rev
Custom	JV42-DN		SA
Date:	Thursday, November 05, 2009	Sheet 19 of	63

Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

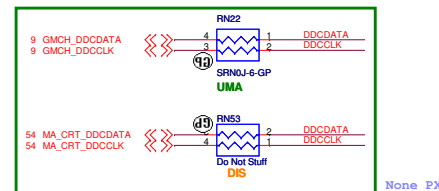
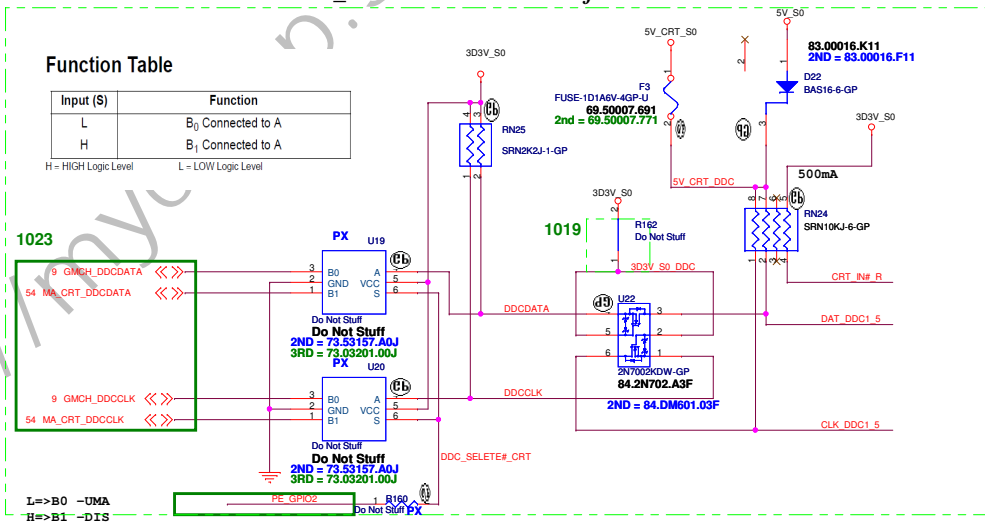


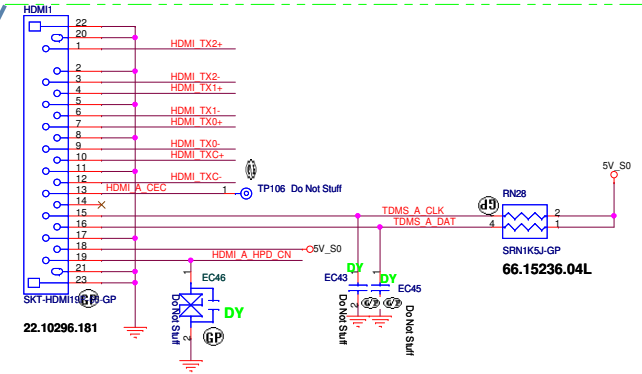
DDC_CLK & DATA level shift

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

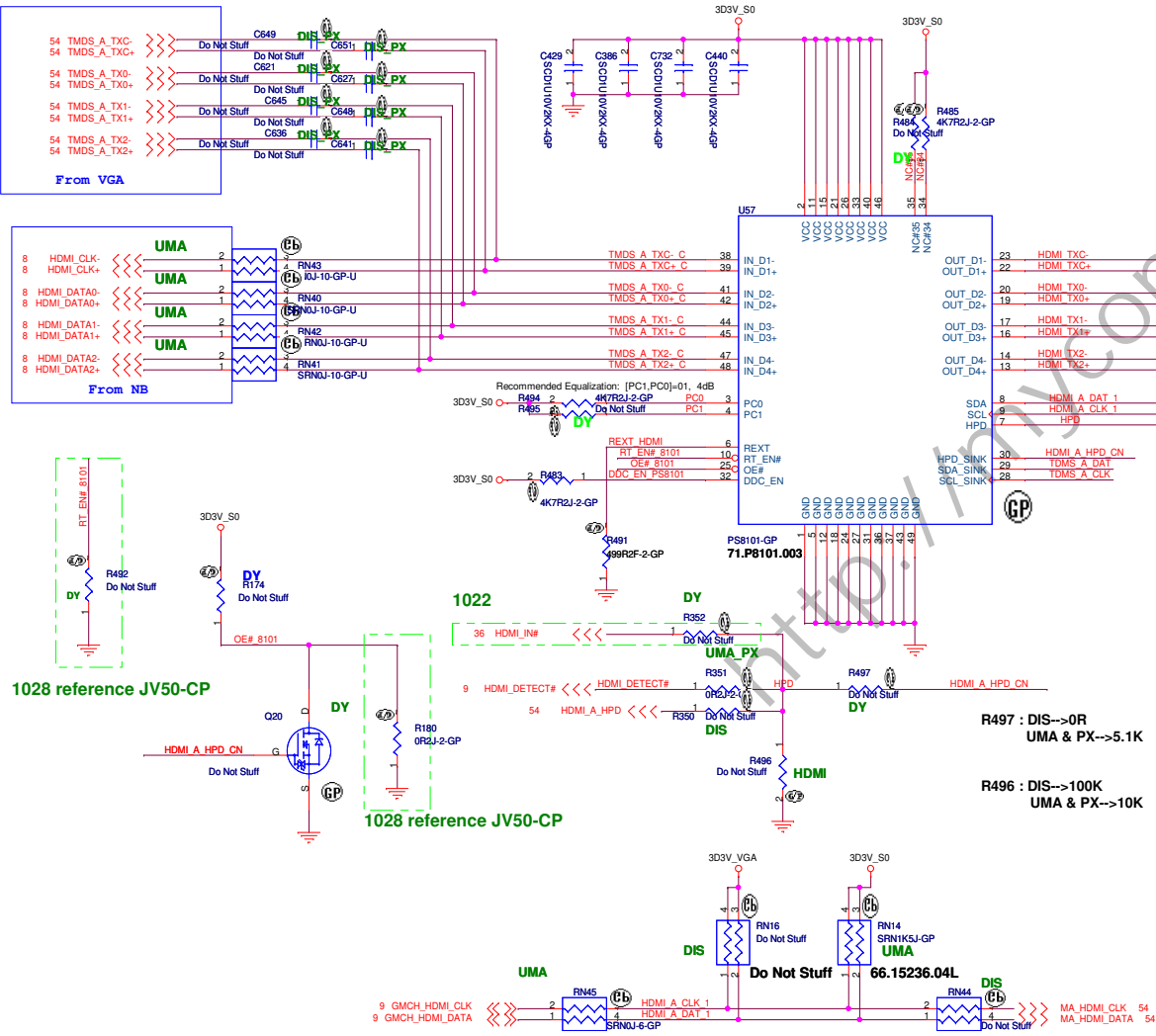
H = HIGH Logic Level L = LOW Logic Level





1026 for Layout request

1026 for Layout request



1028 reference JV50-CP

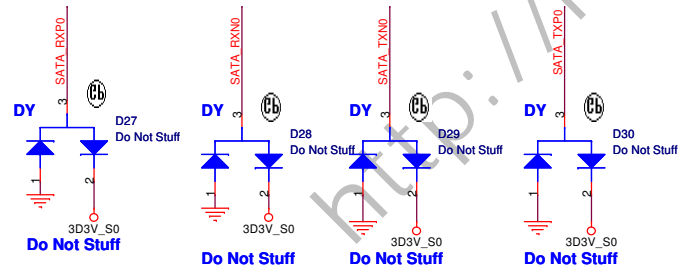
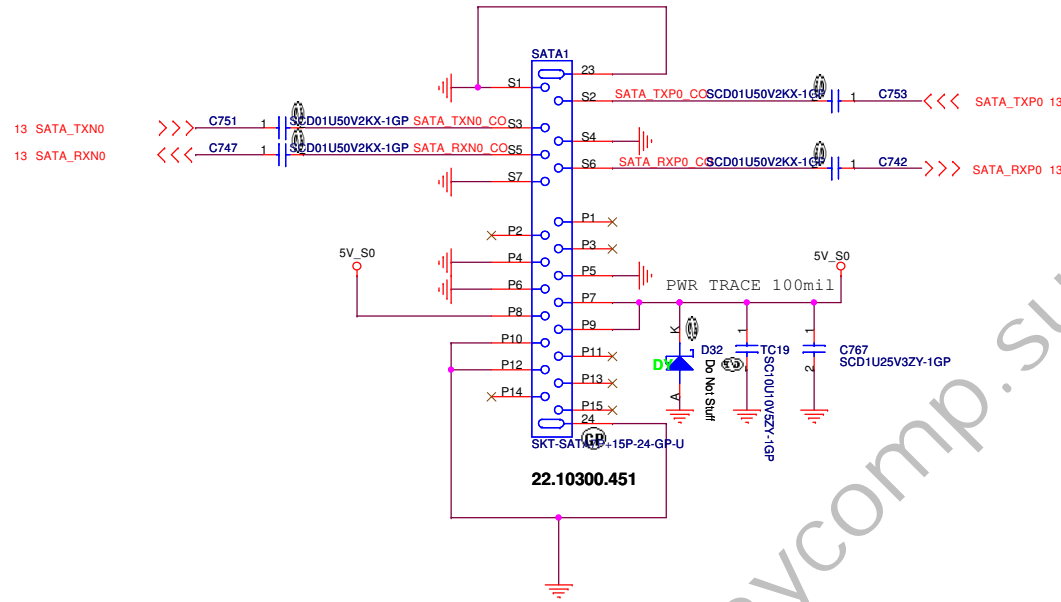
1028 reference JV50-CP

R497 : DIS-->0R
UMA & PX-->5.1K

R496 : DIS-->100K
UMA & PX-->10K

SATA Connector

0923



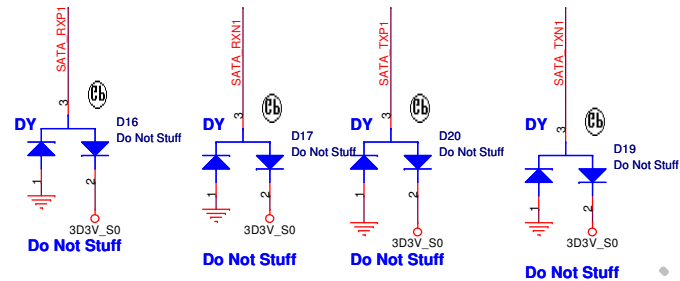
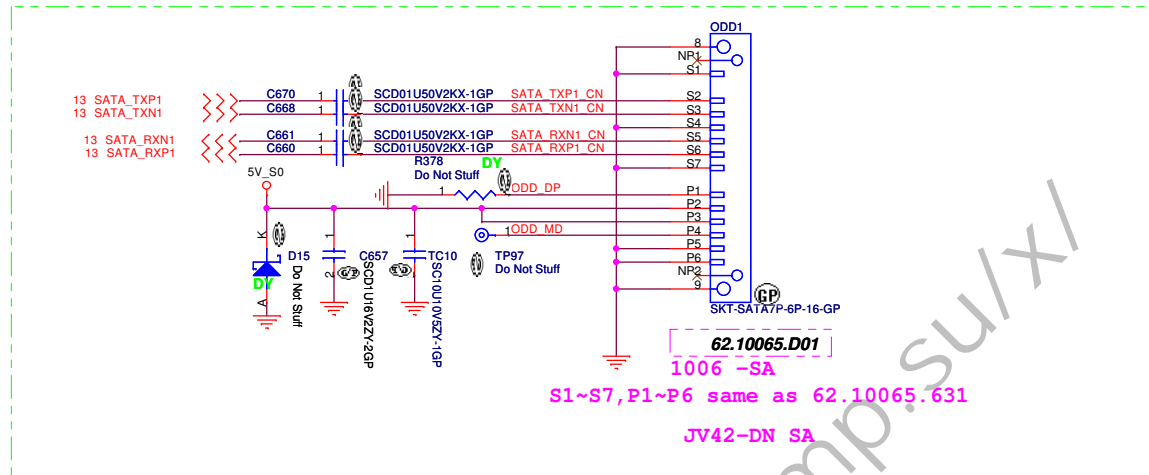
UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		HDD	
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ODD Connector

1009



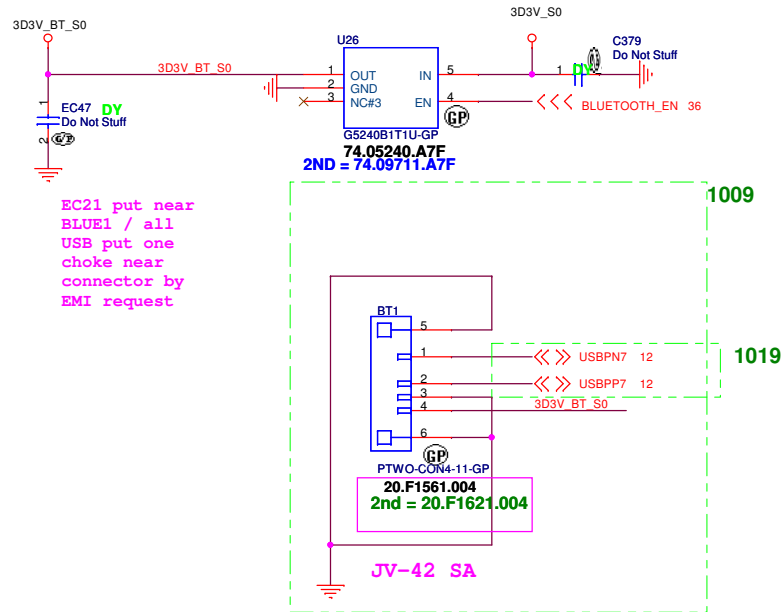
UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title			ODD
Size	Document Number	Rev	
	JV42-DN	SA	
Date:	Thursday, November 05, 2009	Sheet	23 of 63

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



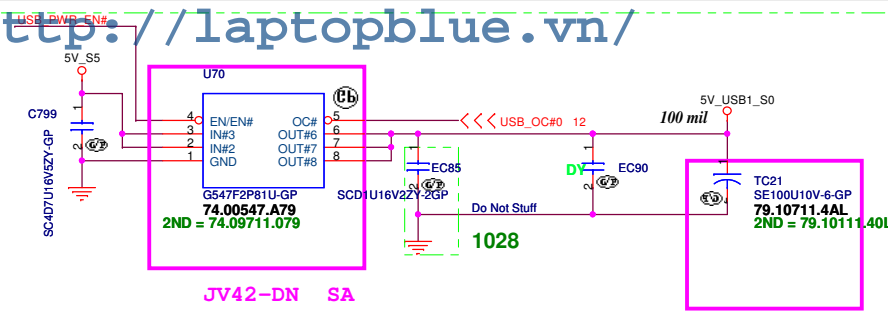
Pin 1 ->right side
20.D0197.104 Pin1 -> left side
change net sequence
can us JV50-CP Cable

UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BLUETOOTH			
Size	Document Number	Rev	SA
	JV42-DN		
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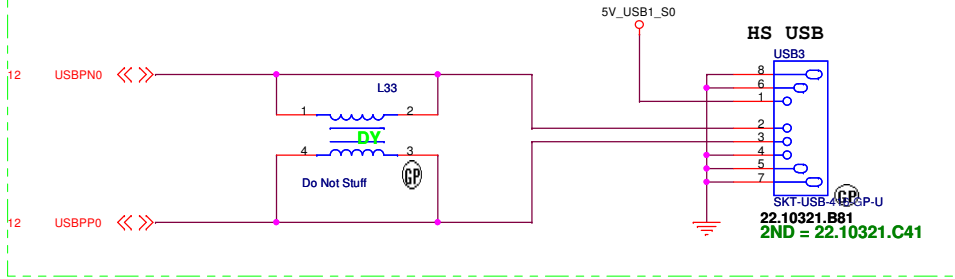


0910

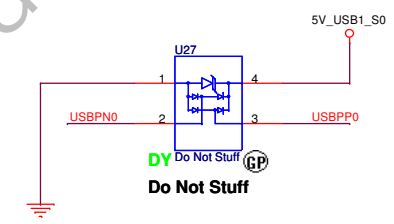


JV42-DN SA

1028 for EMC request



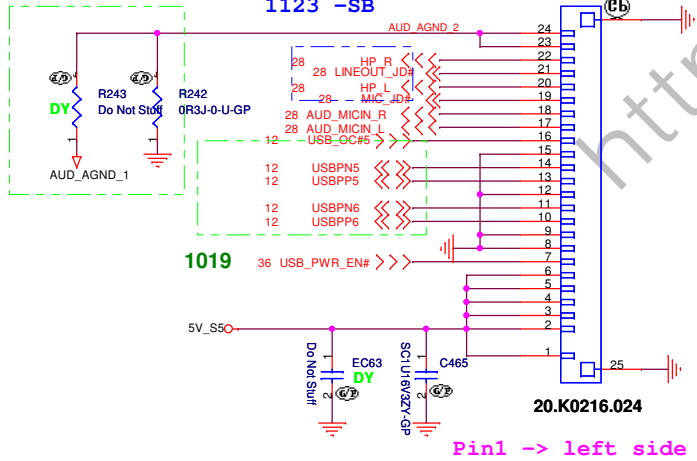
Pin1 -> right side
22.10218.T51 Pin1 -> left side (JV42-DN)
change Net sequence



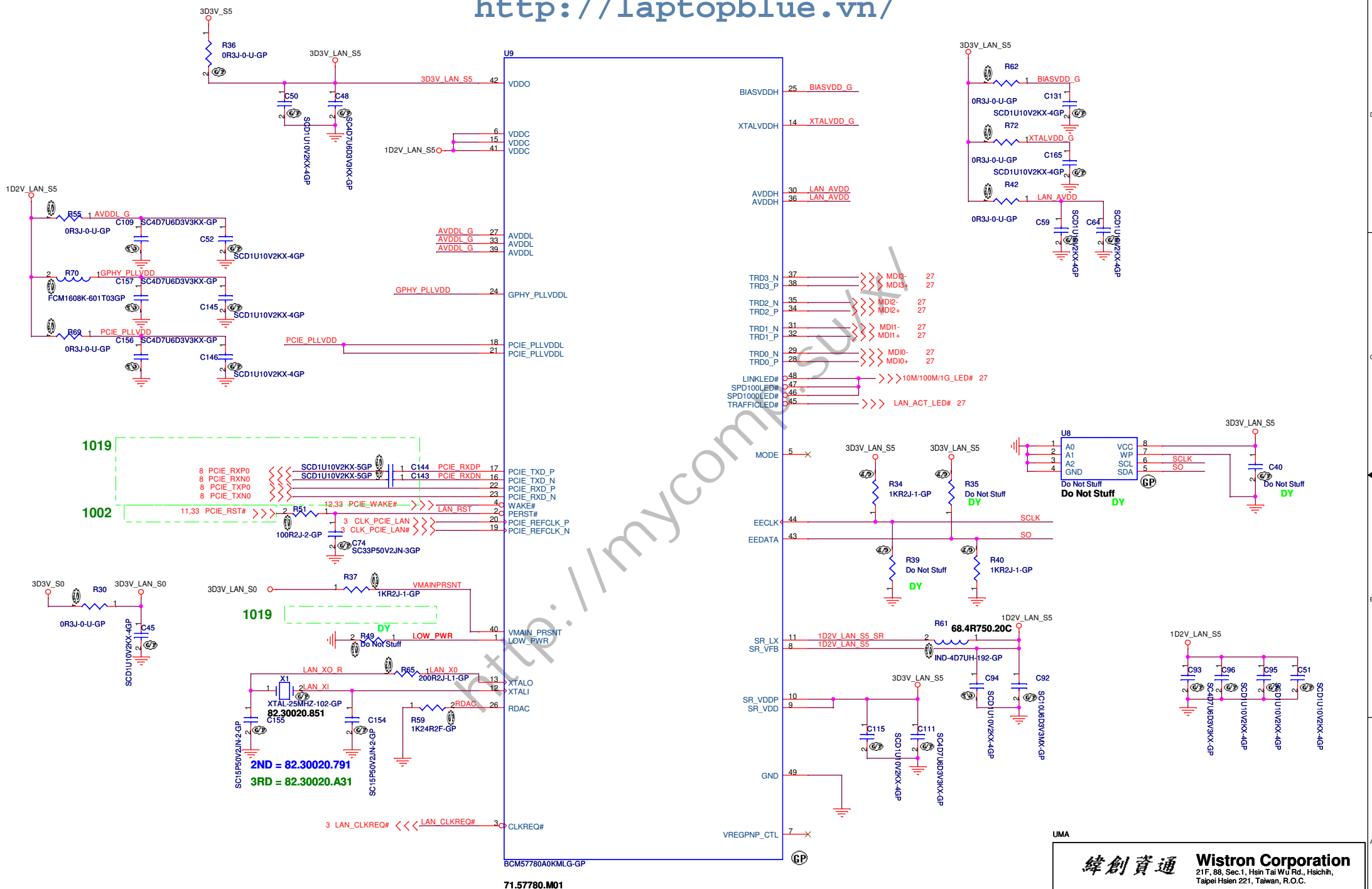
0910



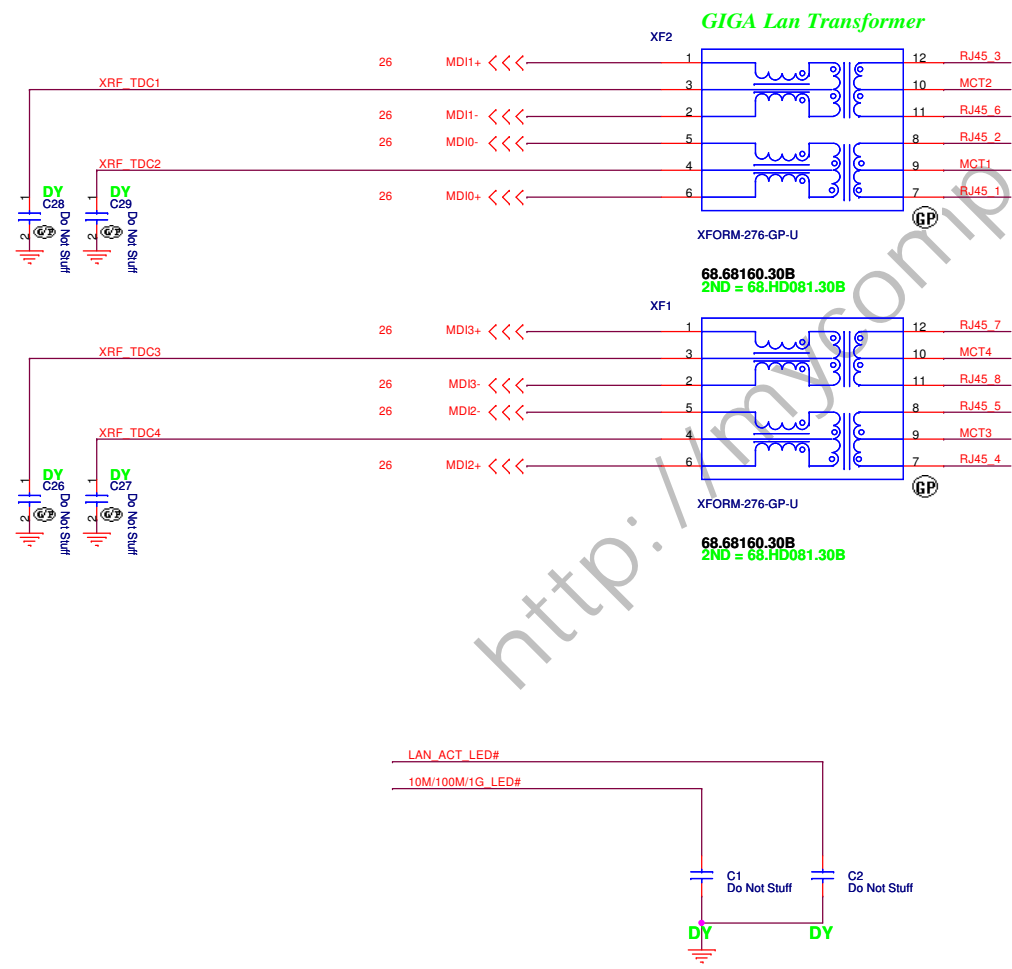
1021



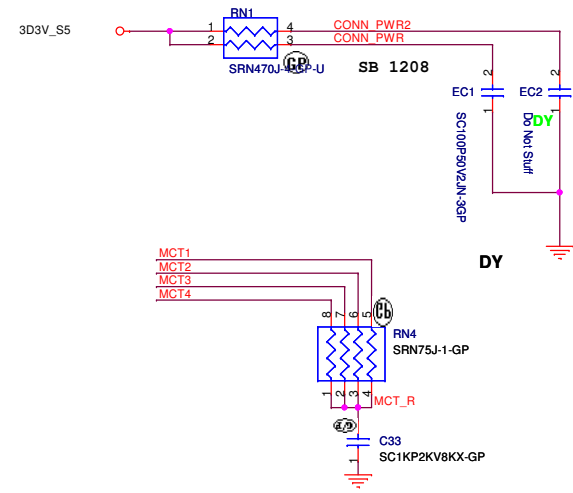
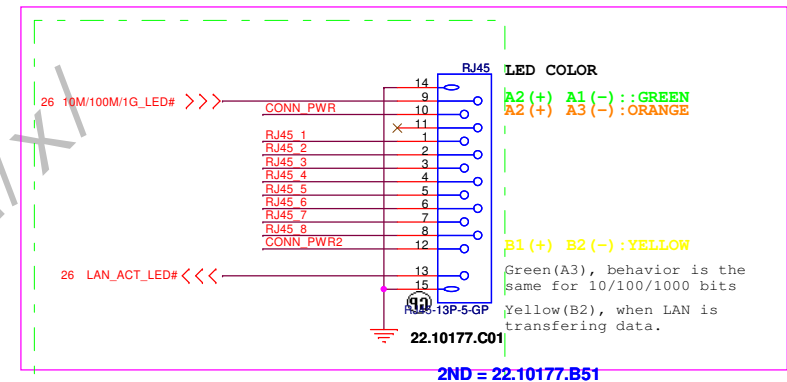
Pin1 -> left side

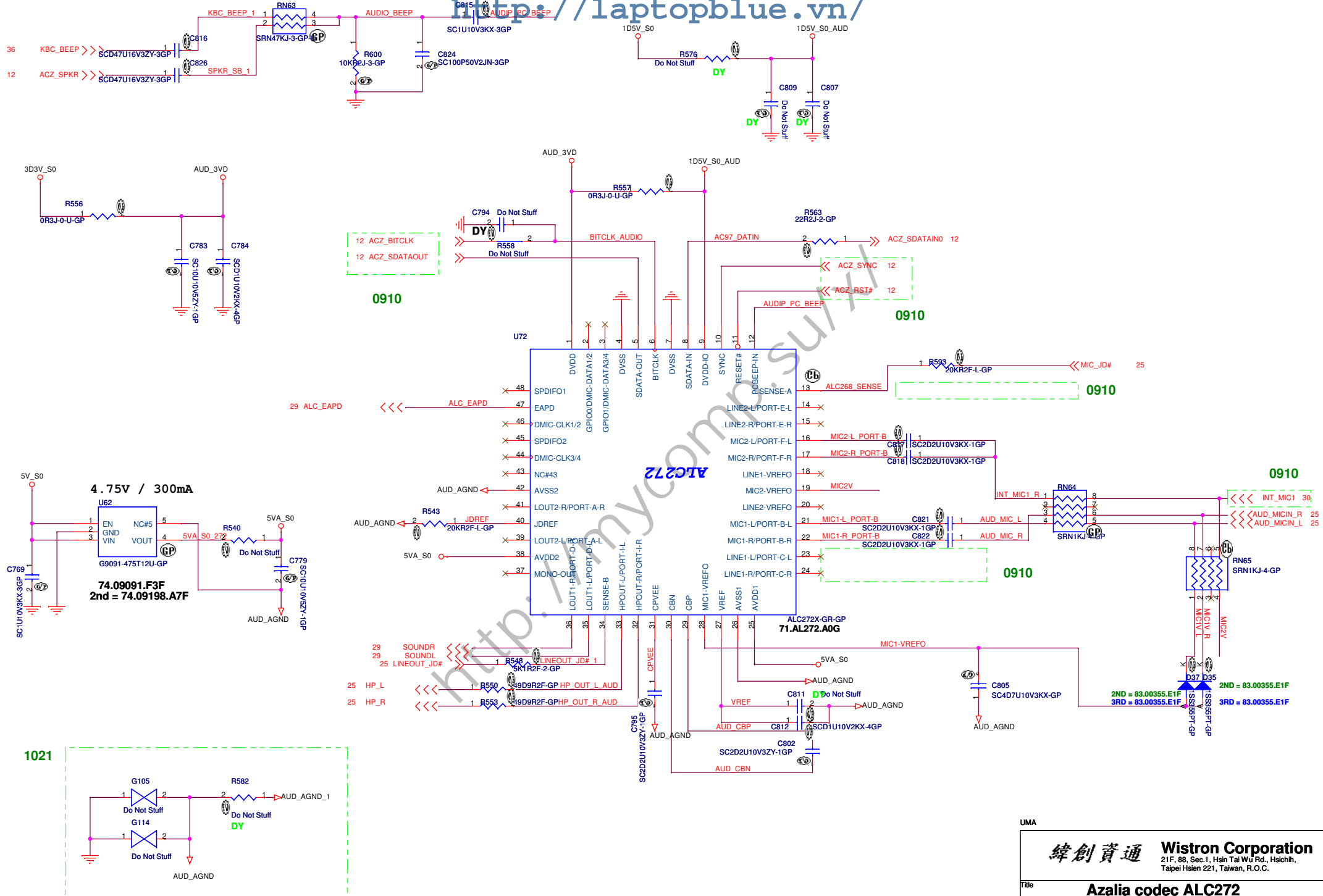


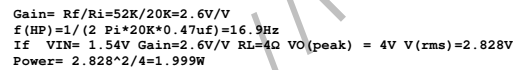
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



0923

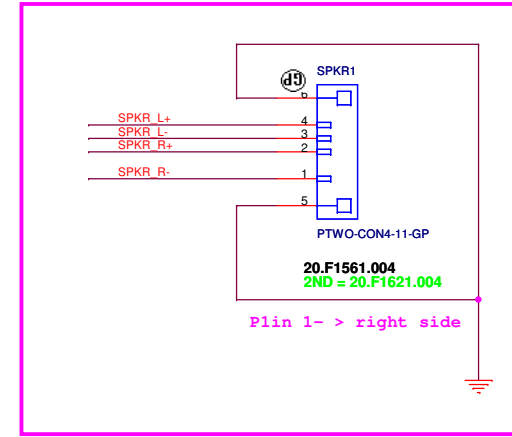
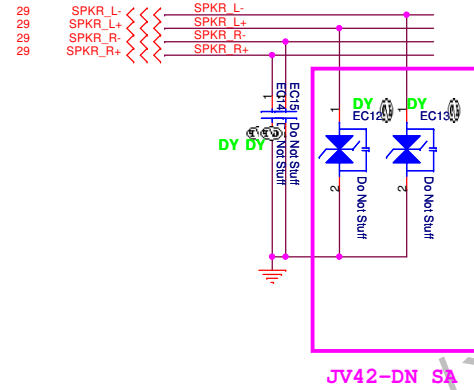






0914

0910



JV42-DN SA

JV42-DN SA

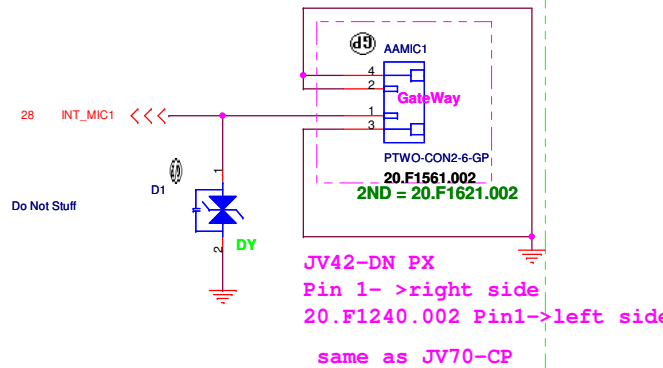
0910

LINE OUT

0911

1016

Internal Mic



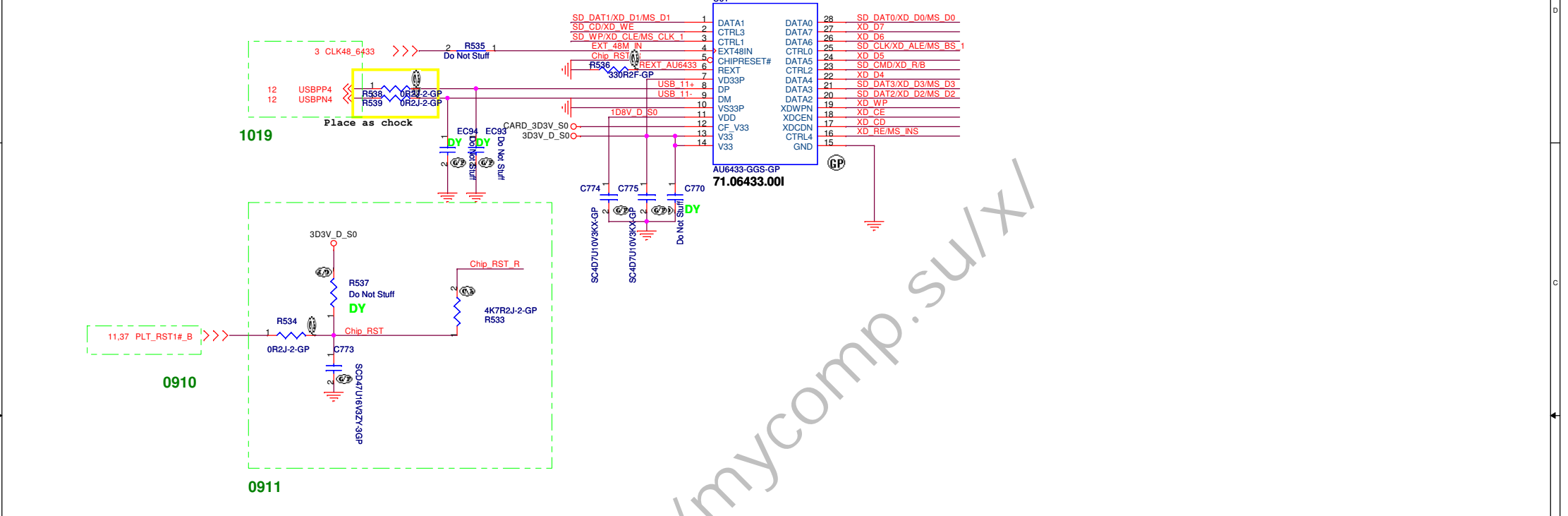
UMA

No Modem Function

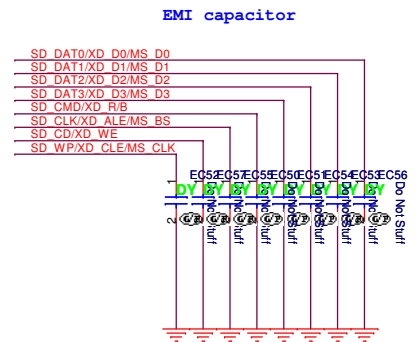
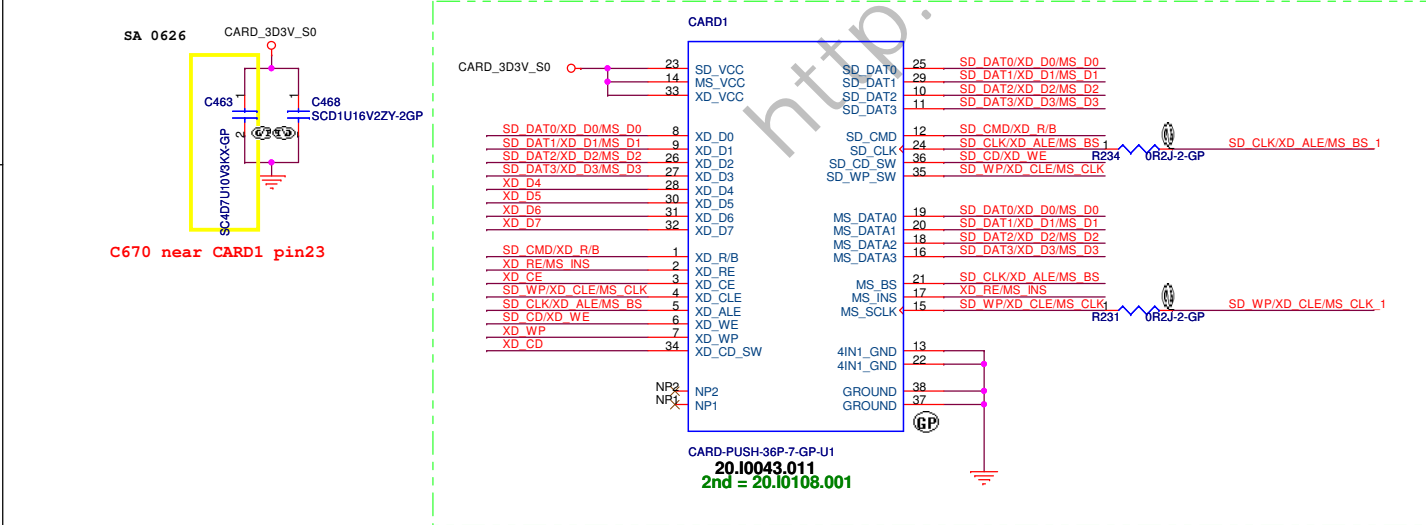
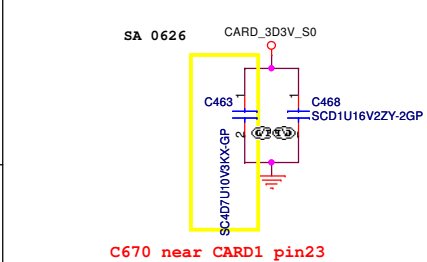
http://mycomp.su/xl

UMA

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Title			
MDC			
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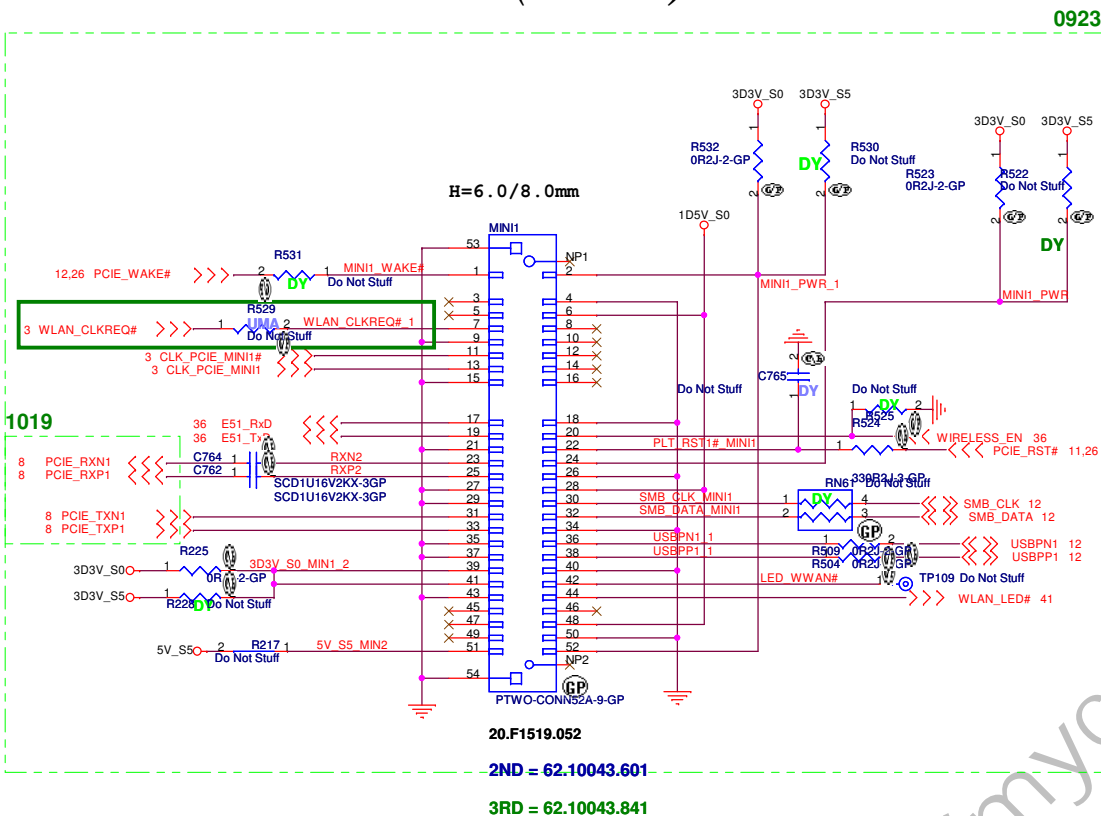
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



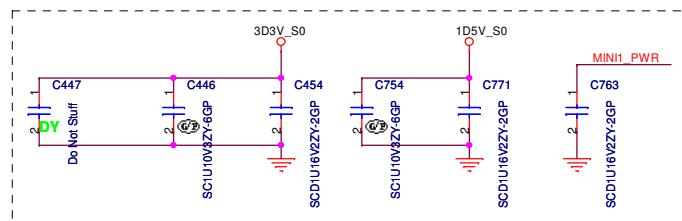
Mini Card Connector(WLAN)

<http://laptopblue.vn/>

No Mini Card Function (Robson2 and 3G)



Place near MINI1



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
MINI CARD			
Size	Document Number		Rev
	JV42-DN		S
Date:	Wednesday, November 18, 2009	Sheet 33 of	63

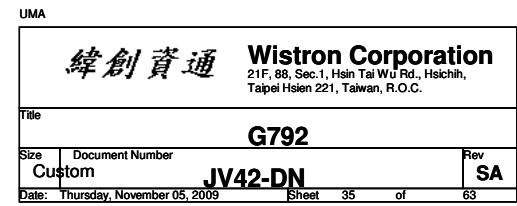
No NEWCARD Function

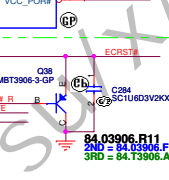
<http://laptopblue.vn/>

<http://mycomp.su/xl>

UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
NEW CARD			
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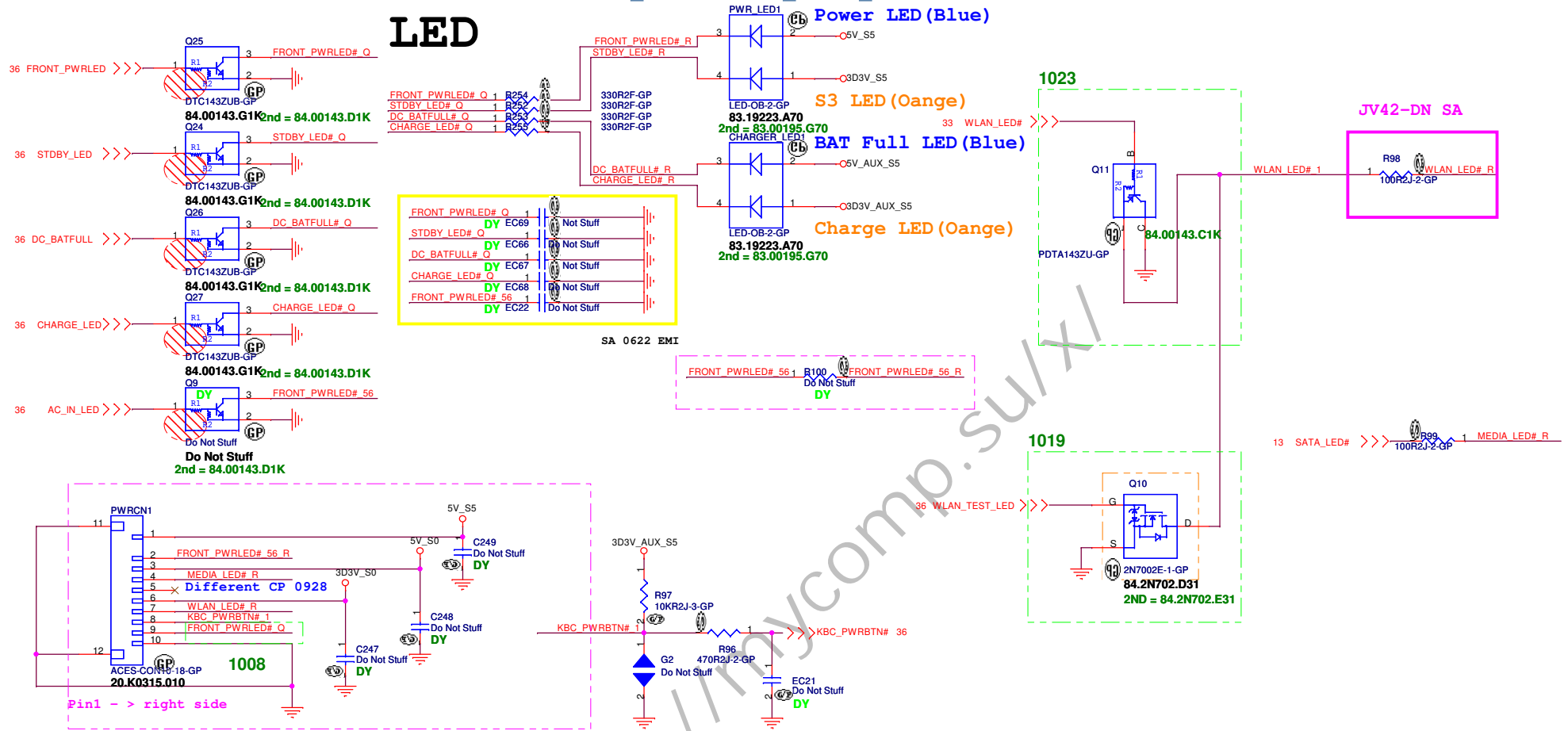
NONE BOARD

http://mycomp.su/xl

http://laptopblue.vn/

http://mycomp.su/xl

LED



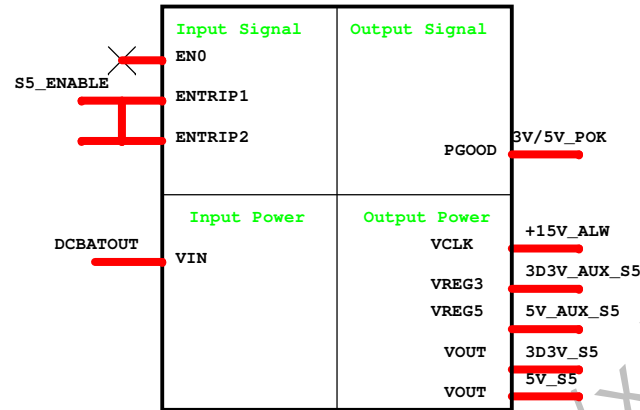
JV42-DN SA 0928

Pin 1	5V_S5	
Pin 2	(DY) FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	NC	
Pin 10	GND	

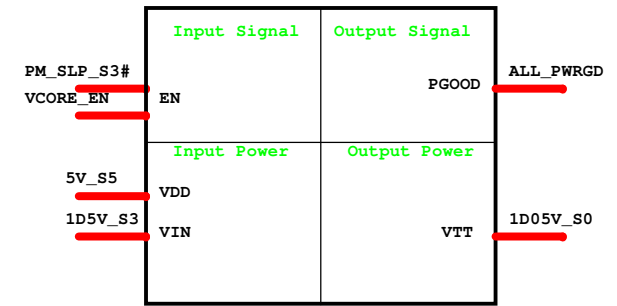
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			LED
Size	Document Number	Rev	
A3	JV42-DN	SA	
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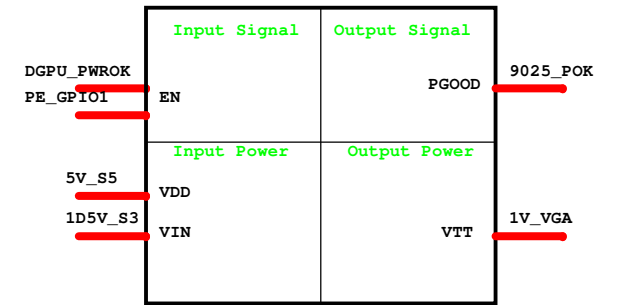
DCDC 5V/3D3V(RT8223)



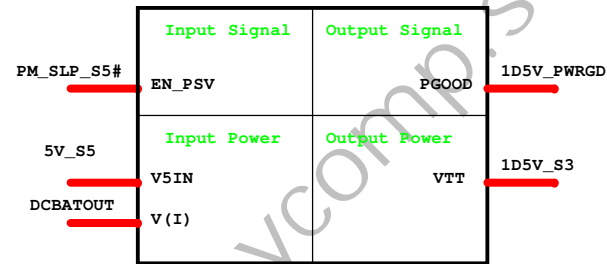
DCDC 1D05V_S0(RT9025)



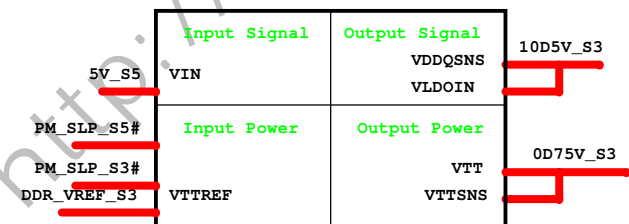
DCDC 1V_VGA(RT9025)



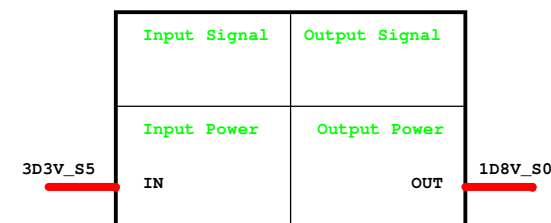
DCDC 1D5V(RT8209E)



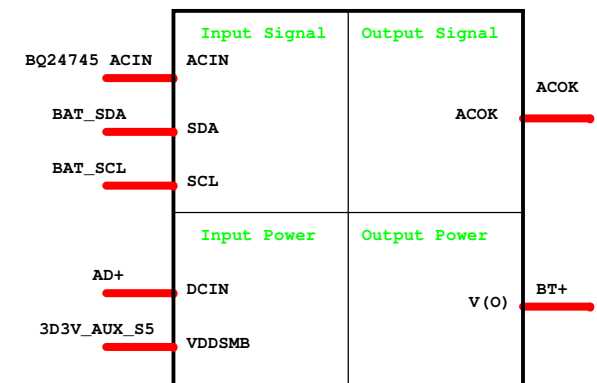
0D75V LDO RT9026



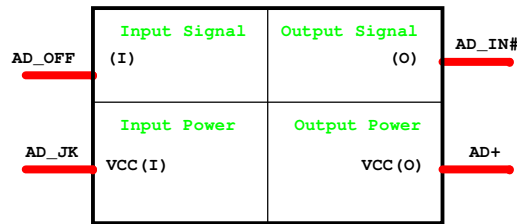
1D8V LDO RT8015A



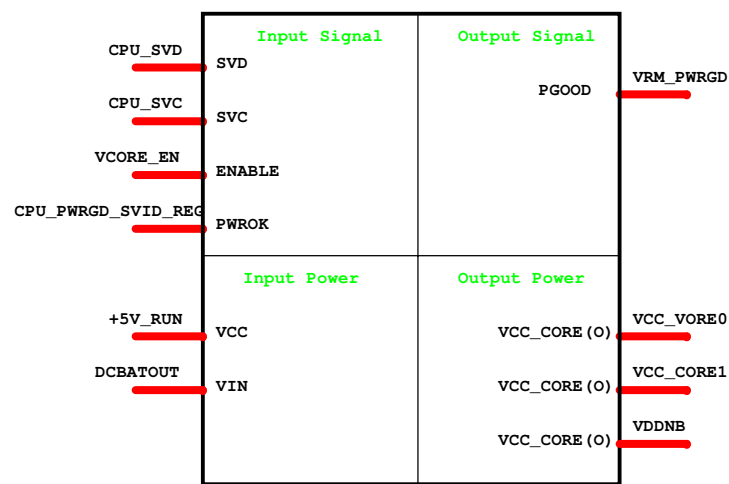
CHARGER BQ24745



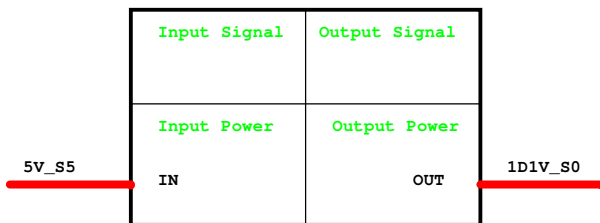
Adapter



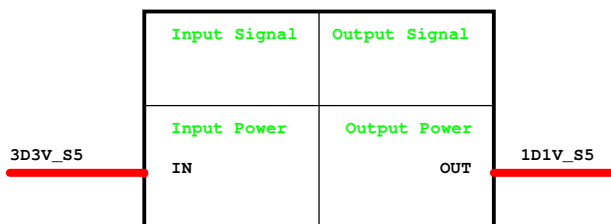
CPU_CORE
ISL6265HRTZ



1D1V LDO RT8209E



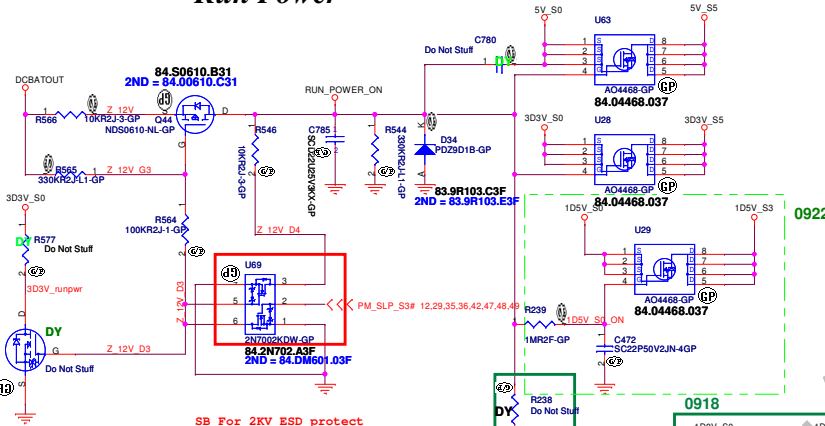
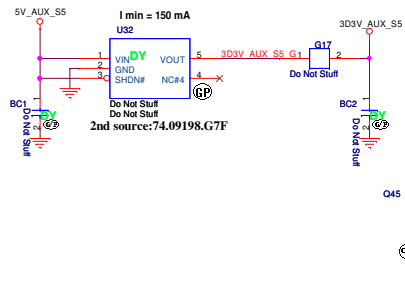
1D1V LDO RT9025



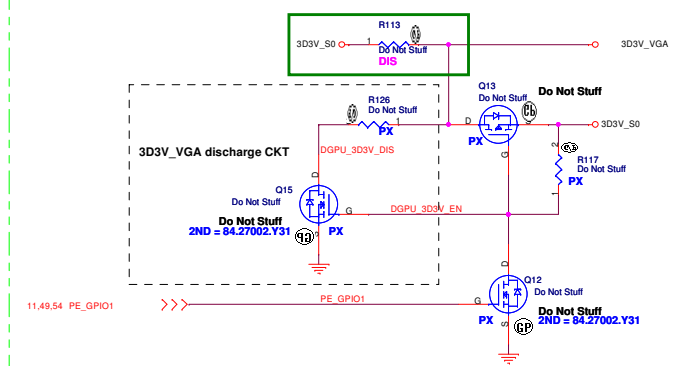
UMA

Run Power

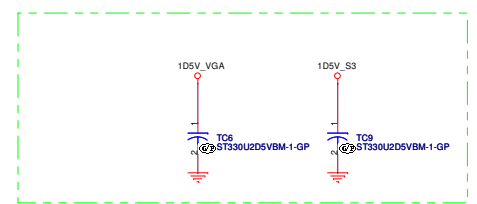
Aux Power 3D3V_AUX_S5



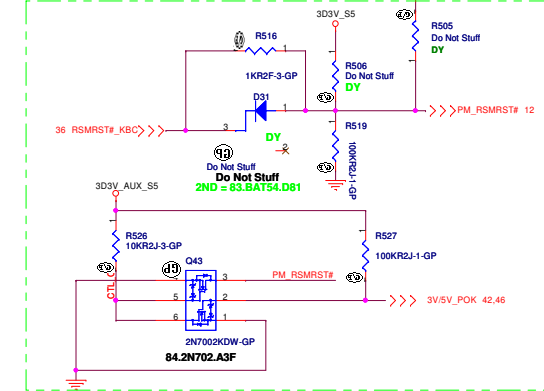
+3VS to 3.3V_DELAY Transfer



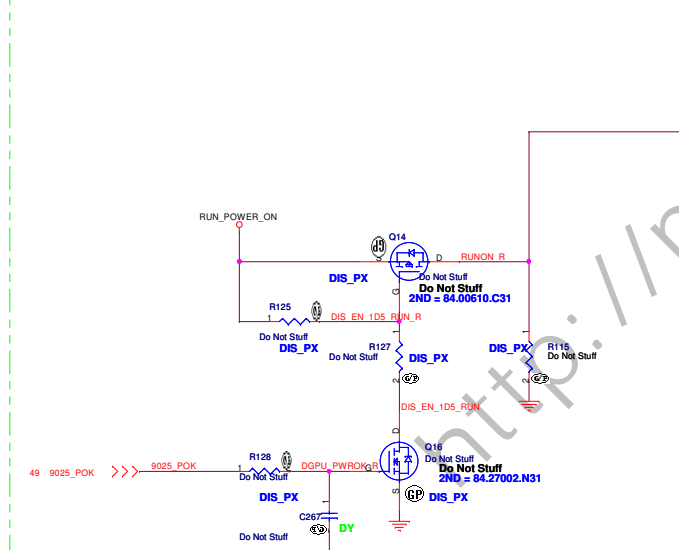
Please closed U77 for Park issue



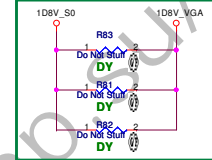
1022



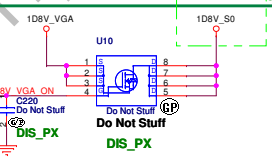
1008



0922



0918



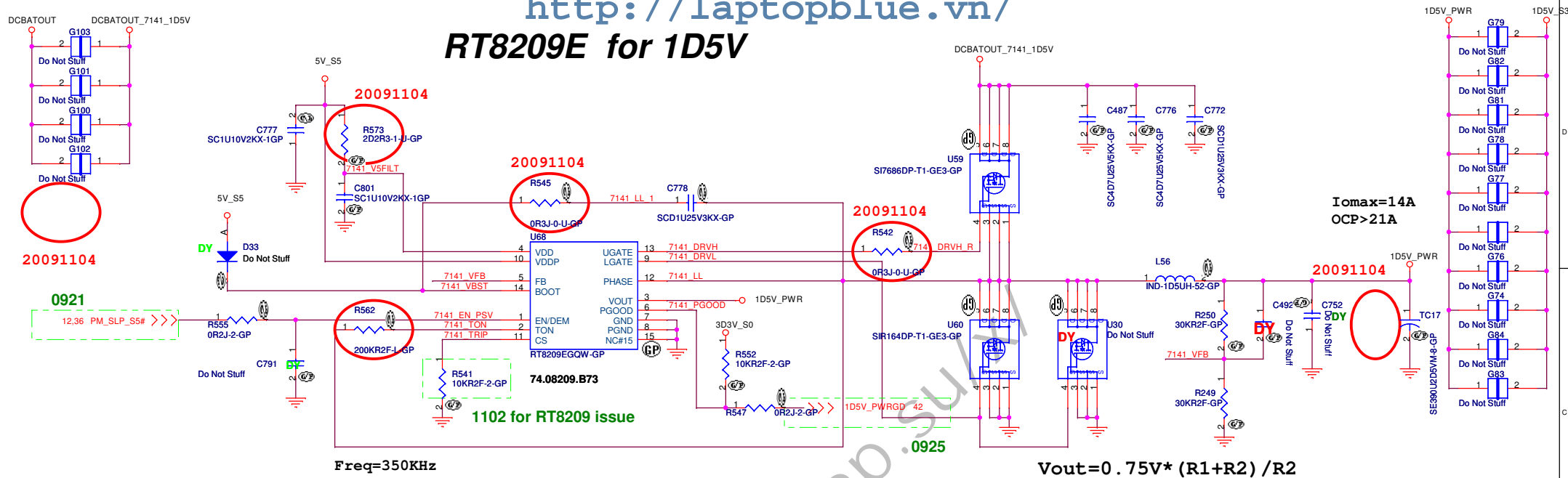


http://laptopblue.vn/

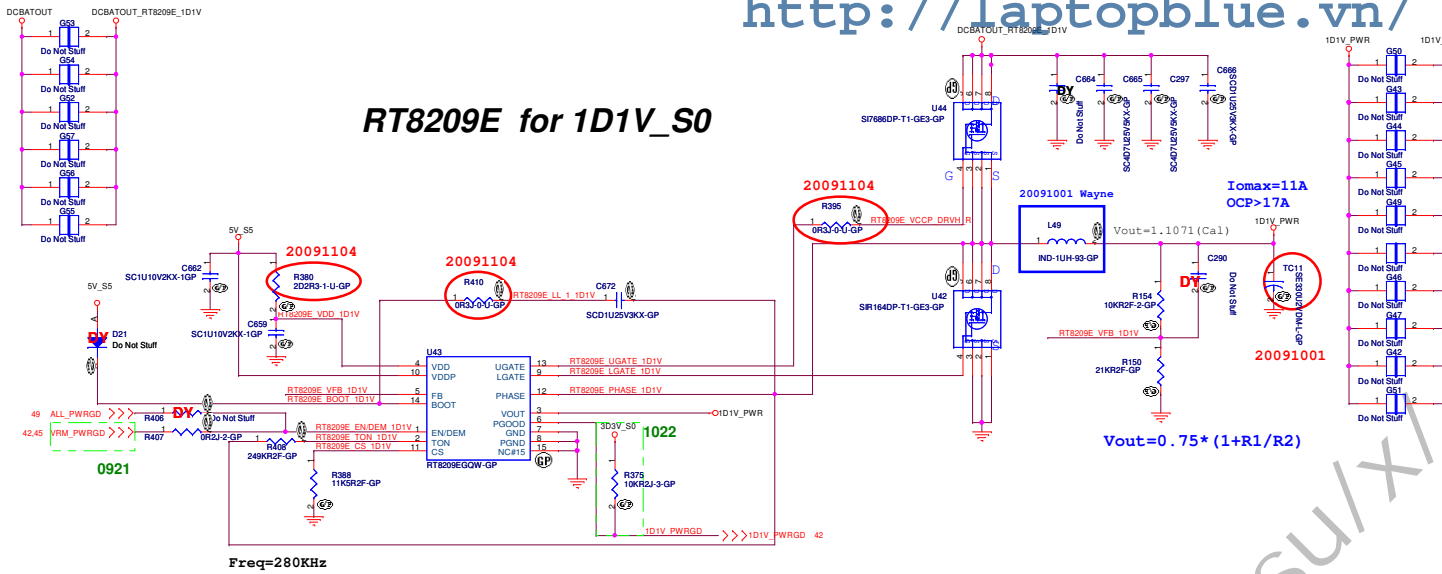
http://laptopblue.vn/

http://laptopblue.vn/

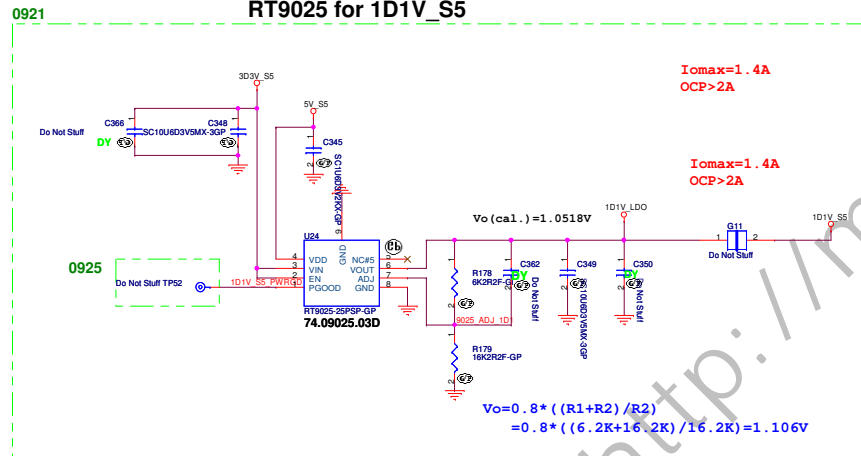
<http://laptopblue.vn/>
RT8209E for 1D5V



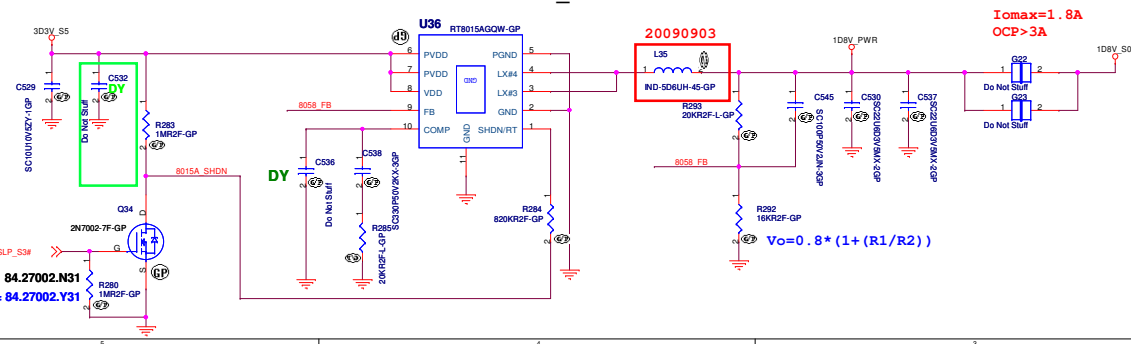
RT209E for 1D1V_S0



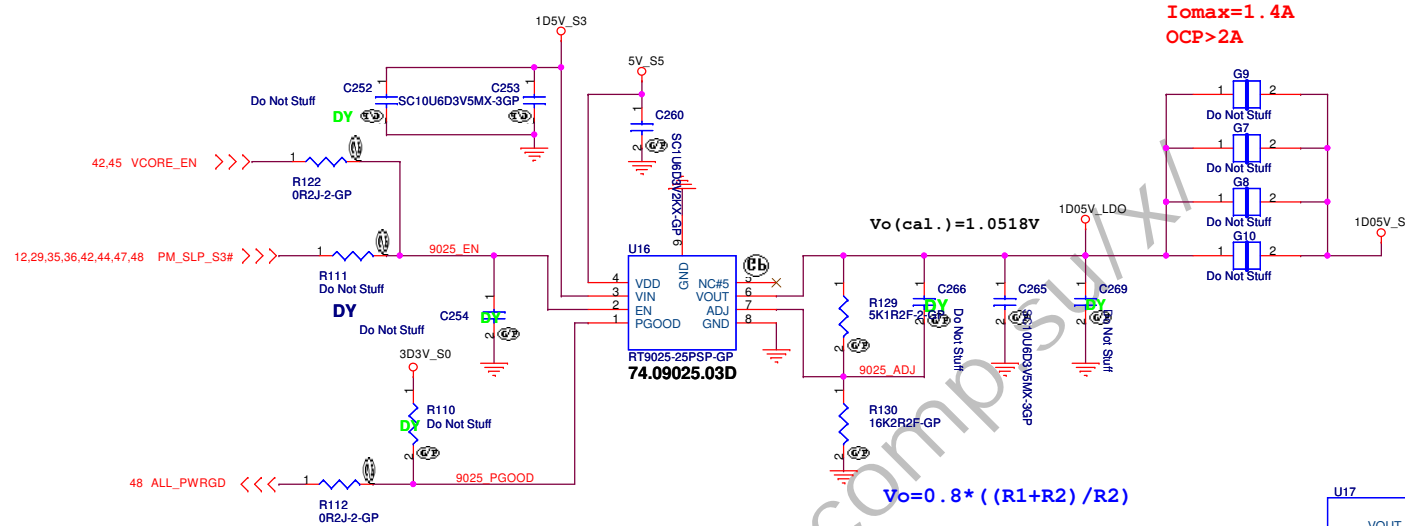
RT9025 for 1D1V_S5



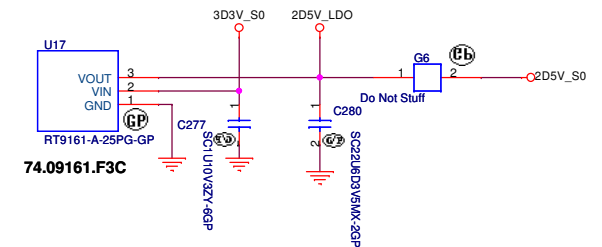
RT8015A for 1D8V_S0



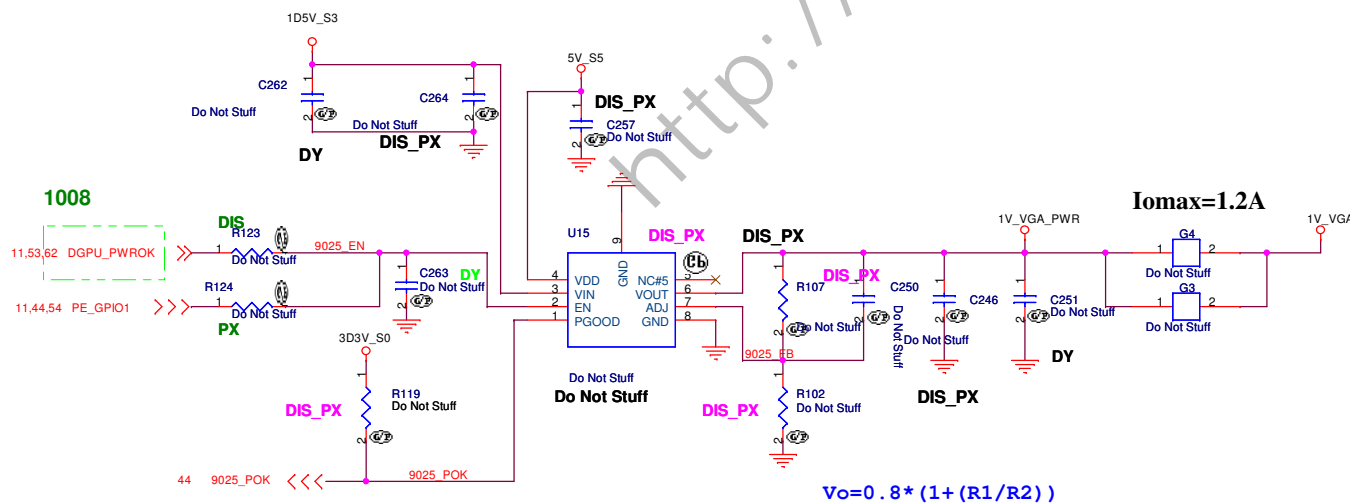
RT9025 for 1D05V_S0



2D5V Iomax=0.2A



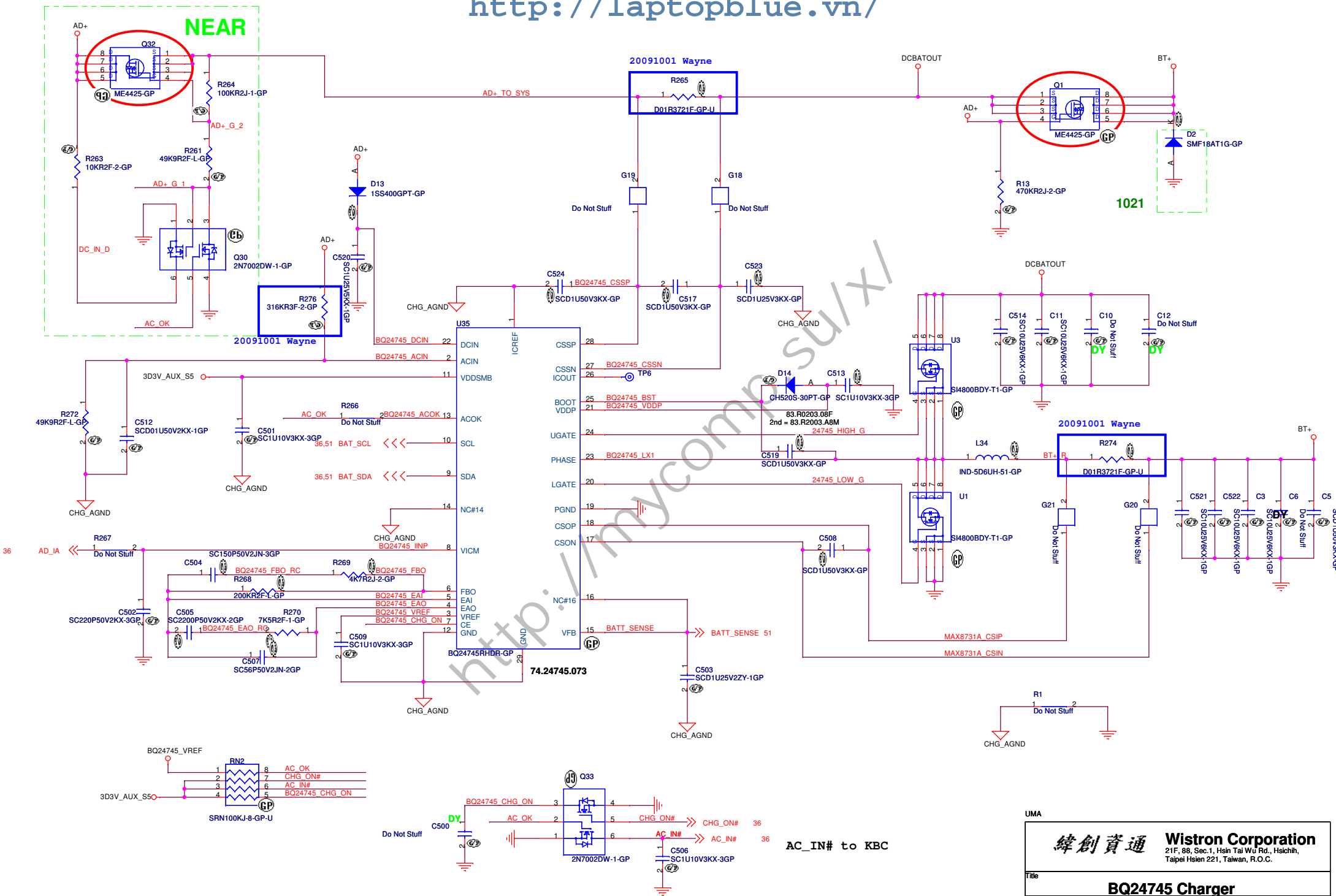
Place near to CPU



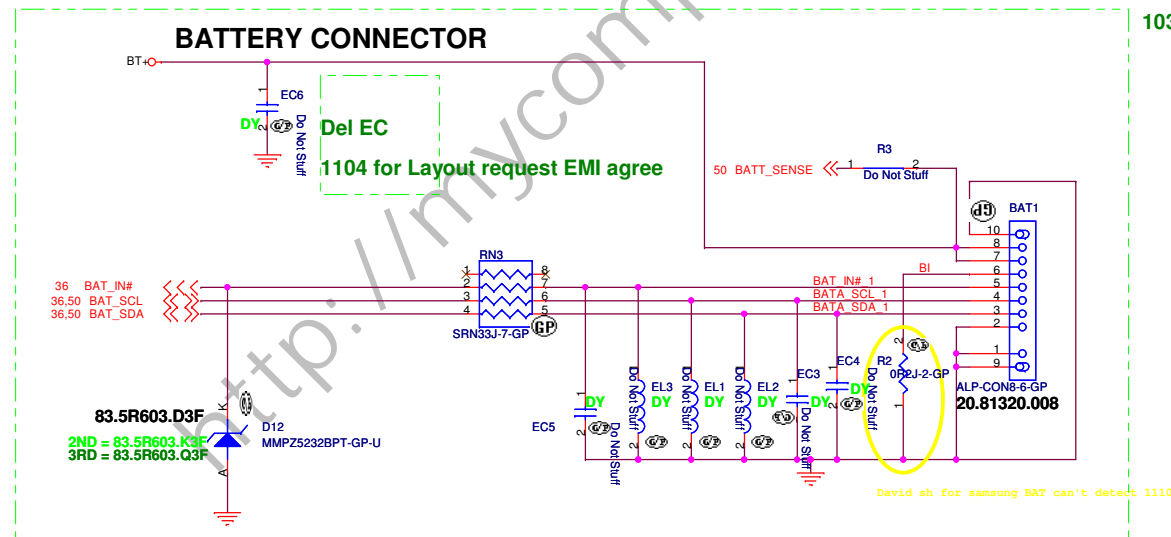
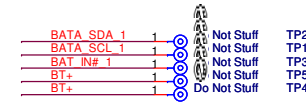
UMA

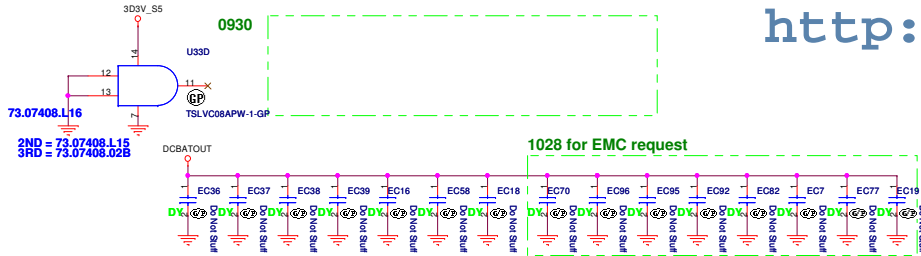
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LDO 1D05V/2D5V/1V		
Size	Document Number	Rev
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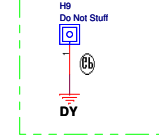


1030

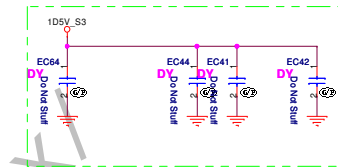




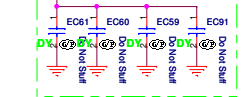
1104 for Layout request



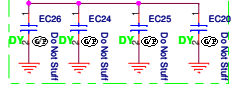
1028 for EMC request



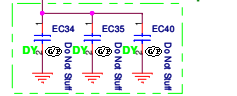
3D3V_S5 1028 for EMC request



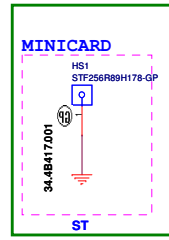
1D1V_S0 1028 for EMC request



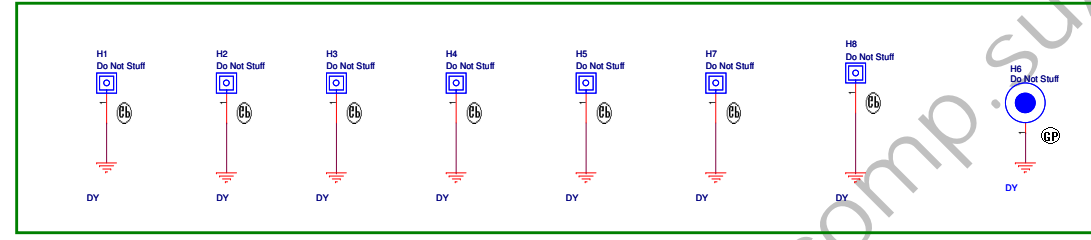
VCC_CORE_S0 1028 for EMC request



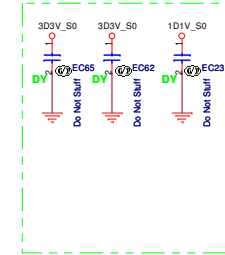
SA



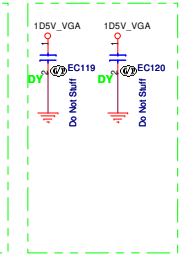
SA



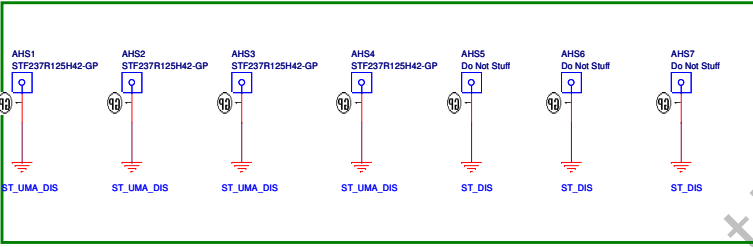
1102 for RF request



1103 for RF request



SA



SA

SB

-1

Check test point

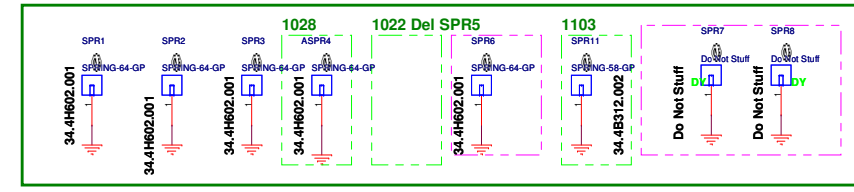
3D3V_S0	TP129	Do Not Stuff
3D3V_AUX_S5	TP125	Do Not Stuff
3D3V_S5	TP123	Do Not Stuff
5V_S5	TP122	Do Not Stuff
12,36 PM_PWRBTN#	TP124	Do Not Stuff
6,11 CPU_PWRGD	TP127	Do Not Stuff
35,36,46 SS_ENABLE	TP126	Do Not Stuff
6,11 CPU_LDT_RST#	TP128	Do Not Stuff

Test Point放在Dimm Door打開可量測處

SA

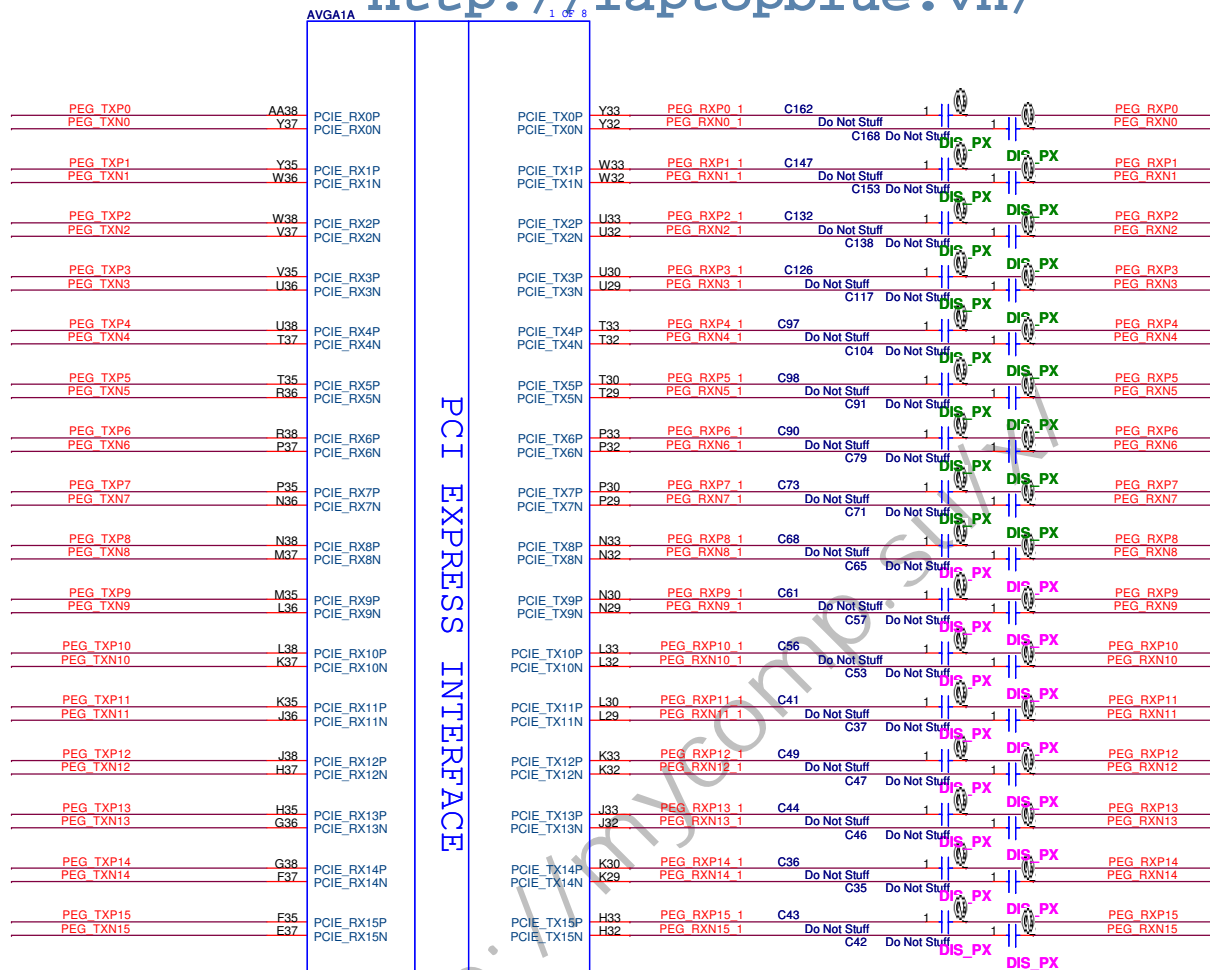
RF Spring

EMI

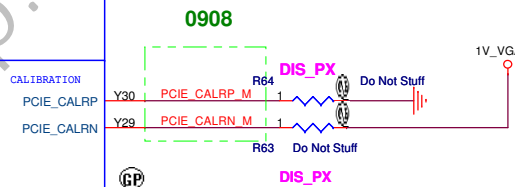
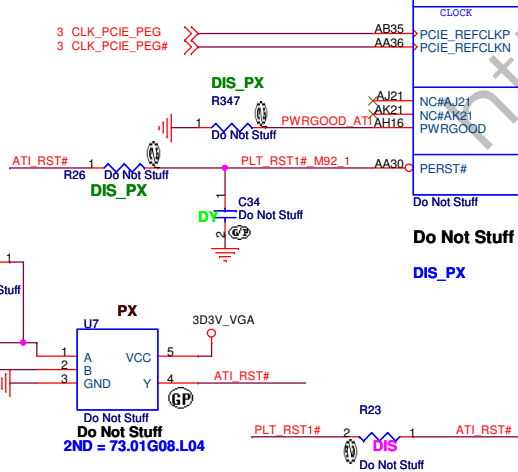


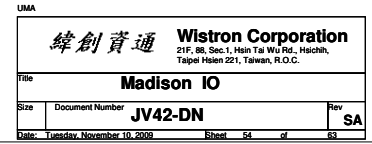
8 PEG_TXP[15..0] << PEG_TXP[15..0]
8 PEG_TXN[15..0] << PEG_TXN[15..0]

8 PEG_RXP[15..0] << PEG_RXP[15..0]
8 PEG_RXN[15..0] << PEG_RXN[15..0]

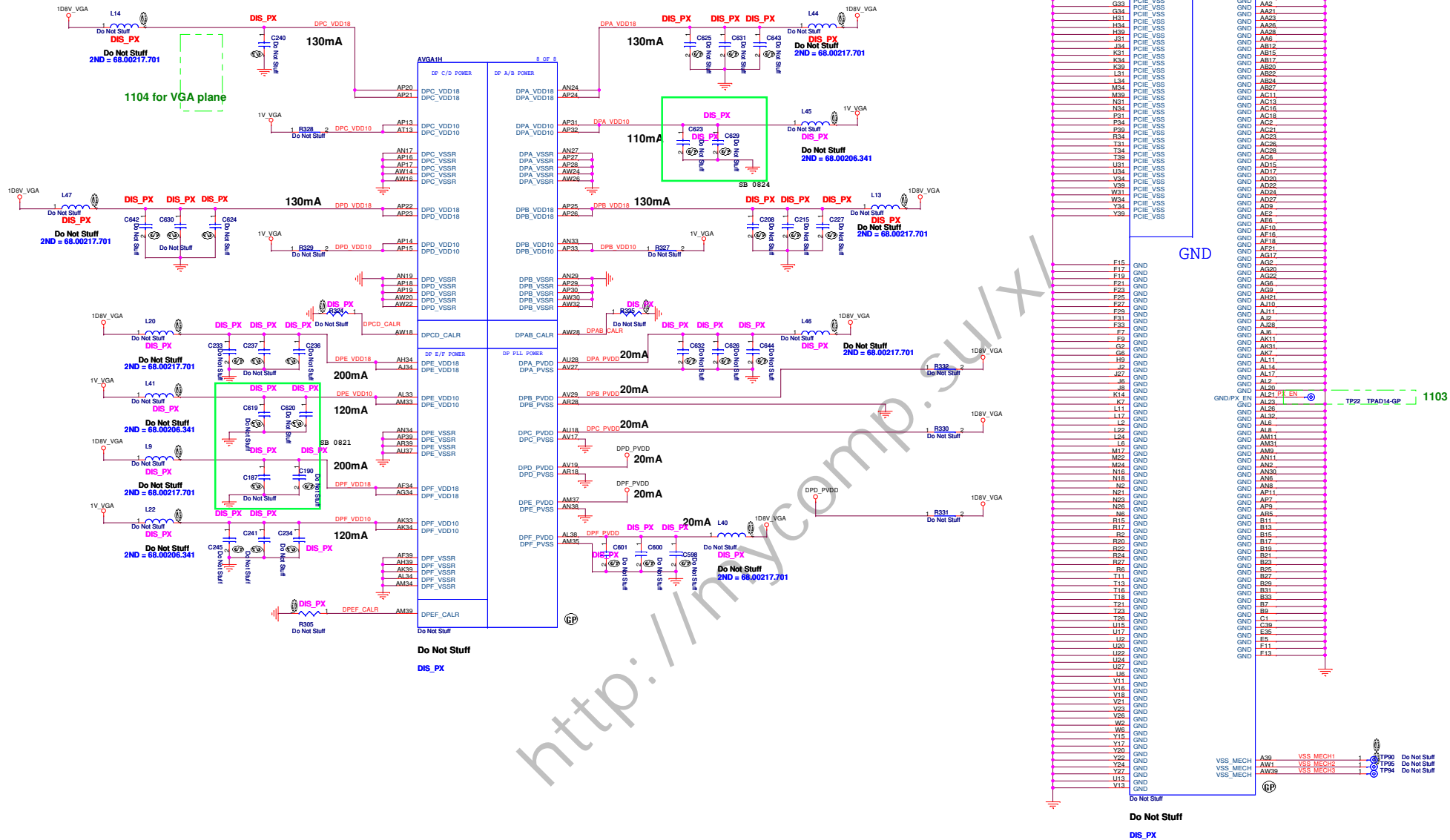


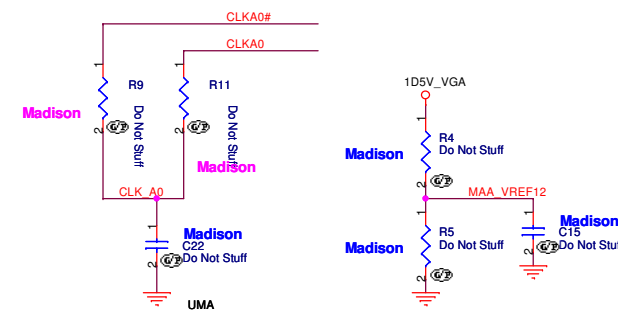
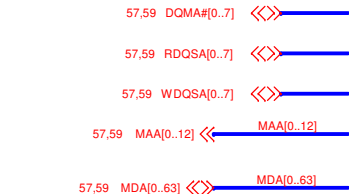
PCI EXPRESS INTERFACE

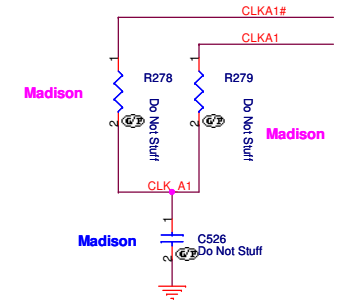
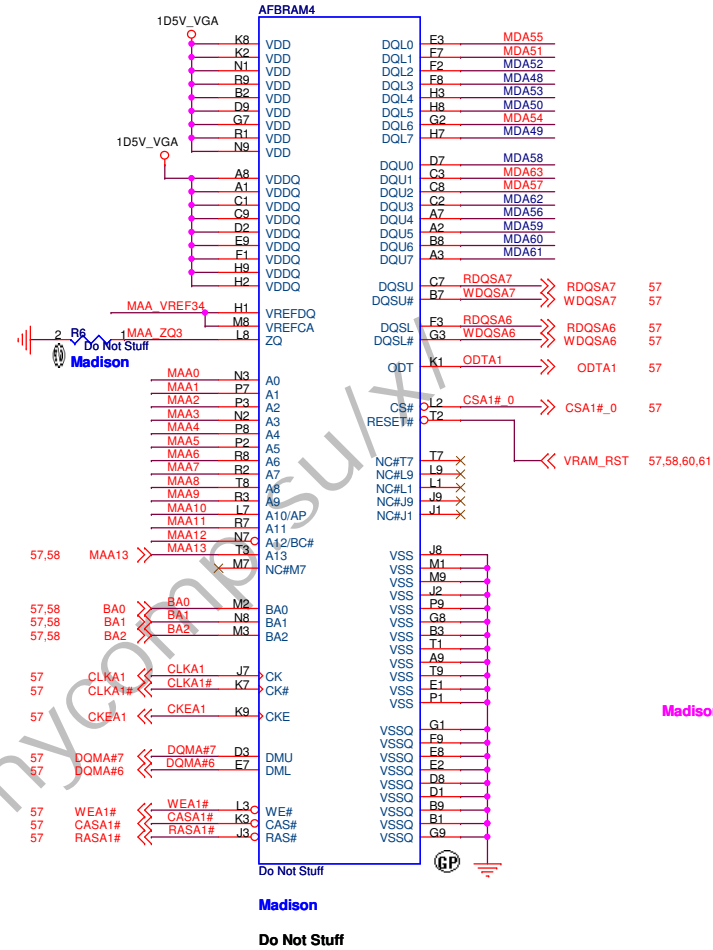
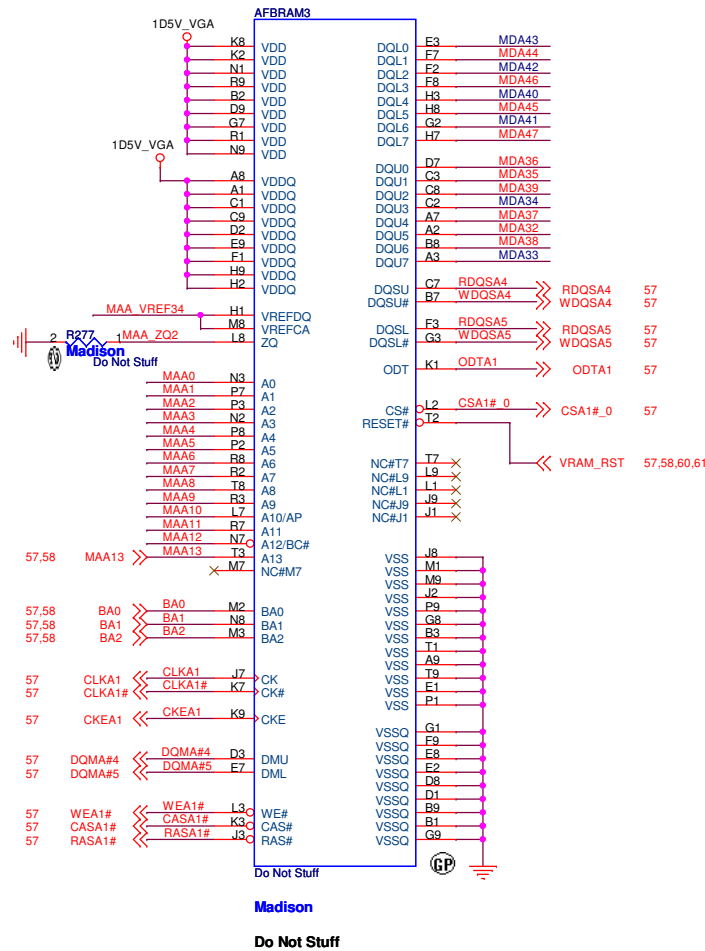












SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

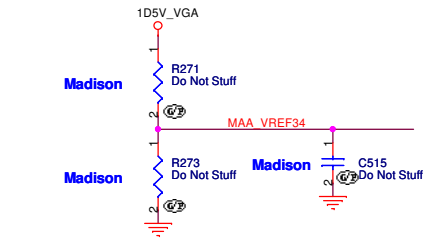
57,58 DQMA#[0..7] <<>>

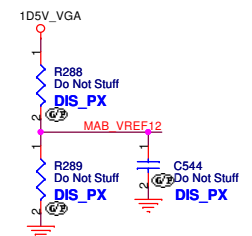
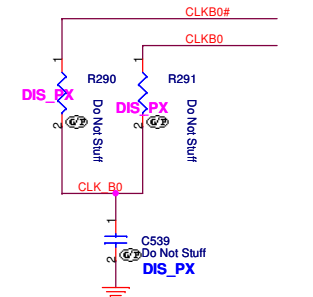
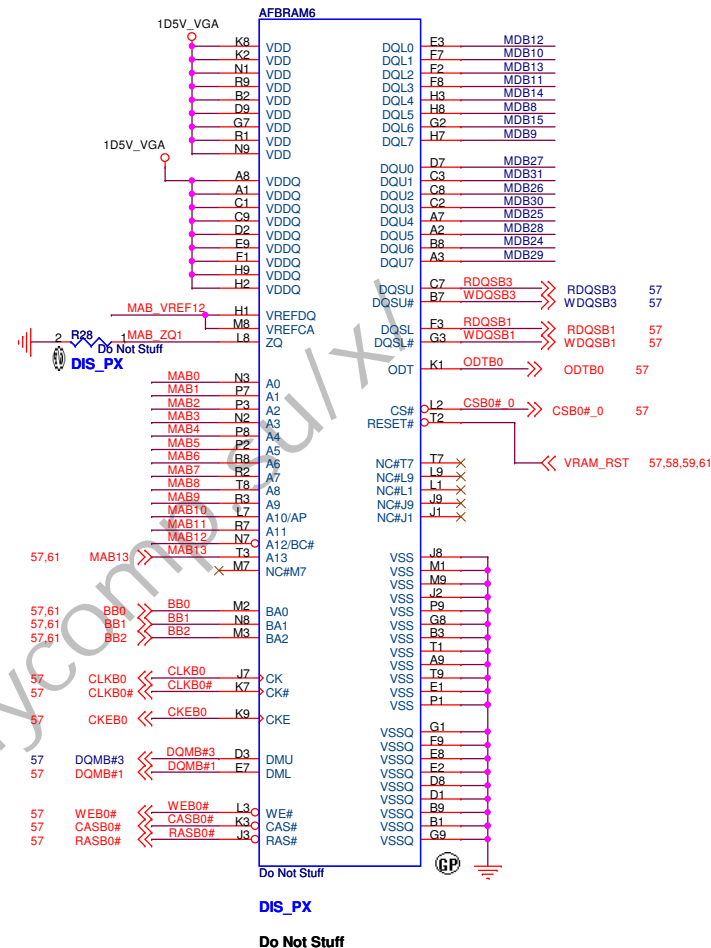
57,58 RDQSA#[0..7] <<>>

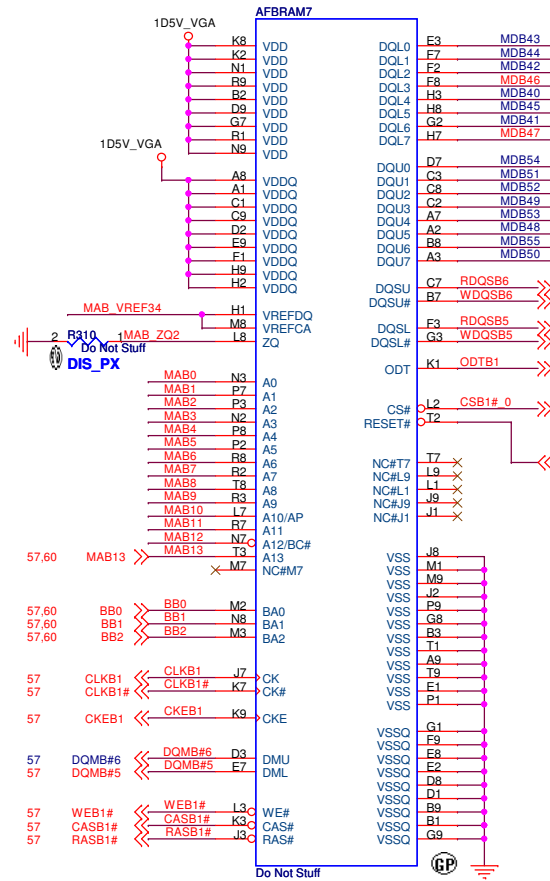
57,58 WDQSA#[0..7] <<>>

57,58 MAA#[0..12] <<>>

57,58 MDA#[0..63] <<>>



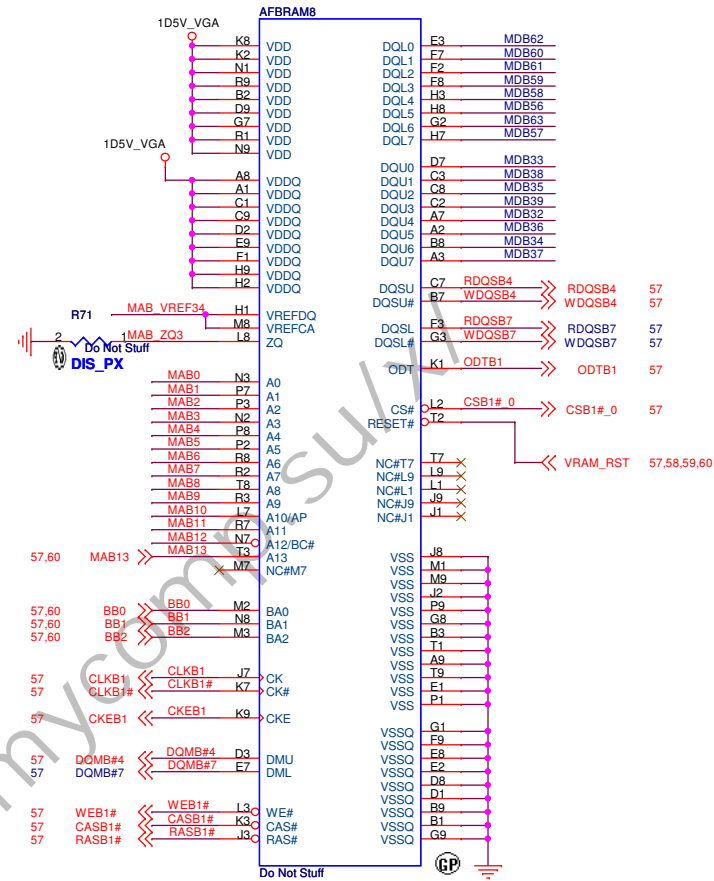




DIS_PX

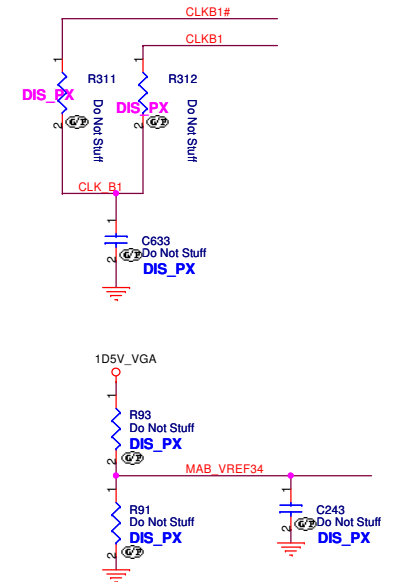
Do Not Stuff

SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



DIS_PX

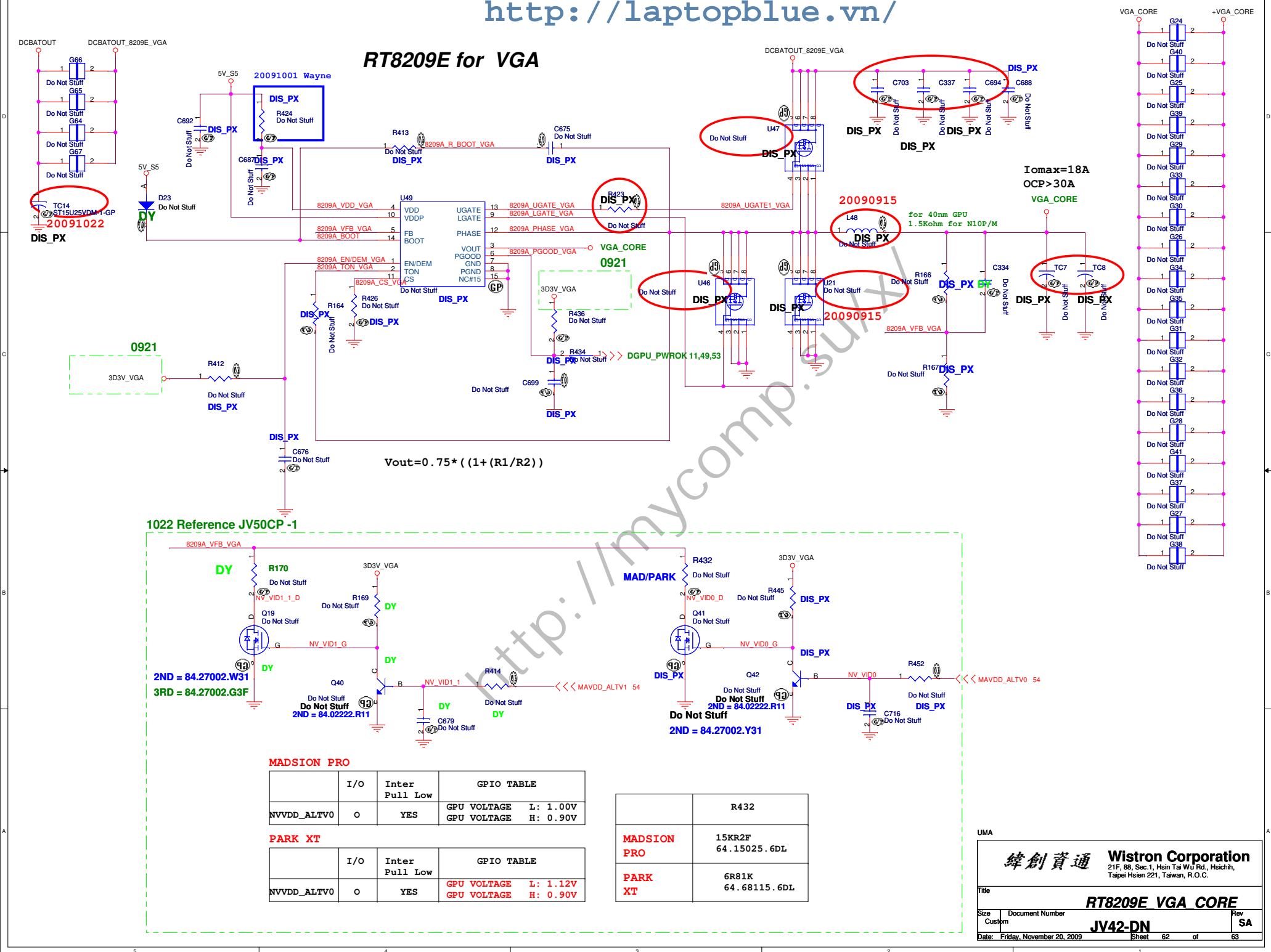
Do Not Stuff



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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NB

RS780-->RS880M
71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP
71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80 歐姆 1% resistor to GND
A12: TBD 歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931 歐姆 1% resistor to VDDAN_11_SATA
A12: TBD 歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01
Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

CRT

UMA-->L1-->2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)
C62-->DY

HDMI

R497 : DIS-->0R
UMA & PX-->5.1K (R497 63.51234.1DL R402H16 5K1R2J-4-GP)
R496 : DIS-->100K
UMA & PX-->10K(R496 63.10334.1DL R402H16 10KR2J-3-GP)

R432(MAD/PARK)

Madison-->V15KR2F 64.15025.6DL
Park-->R432 64.68115.6DL

BOM

1st -> Diserete Madison Hynix(S02G)
2nd -> UMA (S01G)
1st +3rd -> Diserete Park Hynix(S03G)
1st +3rd -> Diserete Park Samsung(S04G)
1st -> Diserete Madison Samsung (S05G)

PX=PARK+Hynix(1st +3rd)

UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
NOTE			
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