

Compal Confidential

NDWGO Schematics Document

AMD S1g3/ RS880M/ SB710

2009 / 09 / 22

LA-5991P

Rev:0.1

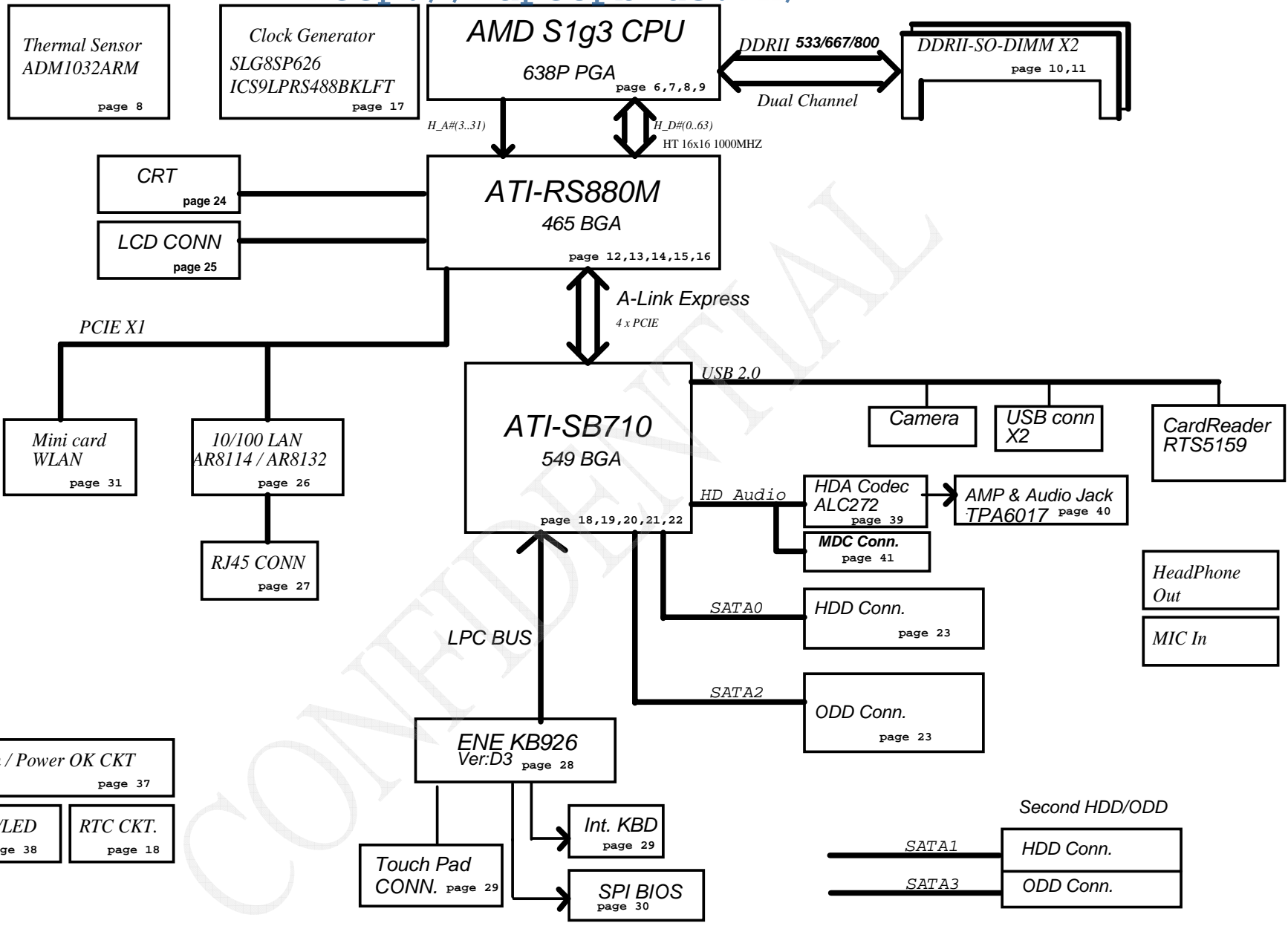
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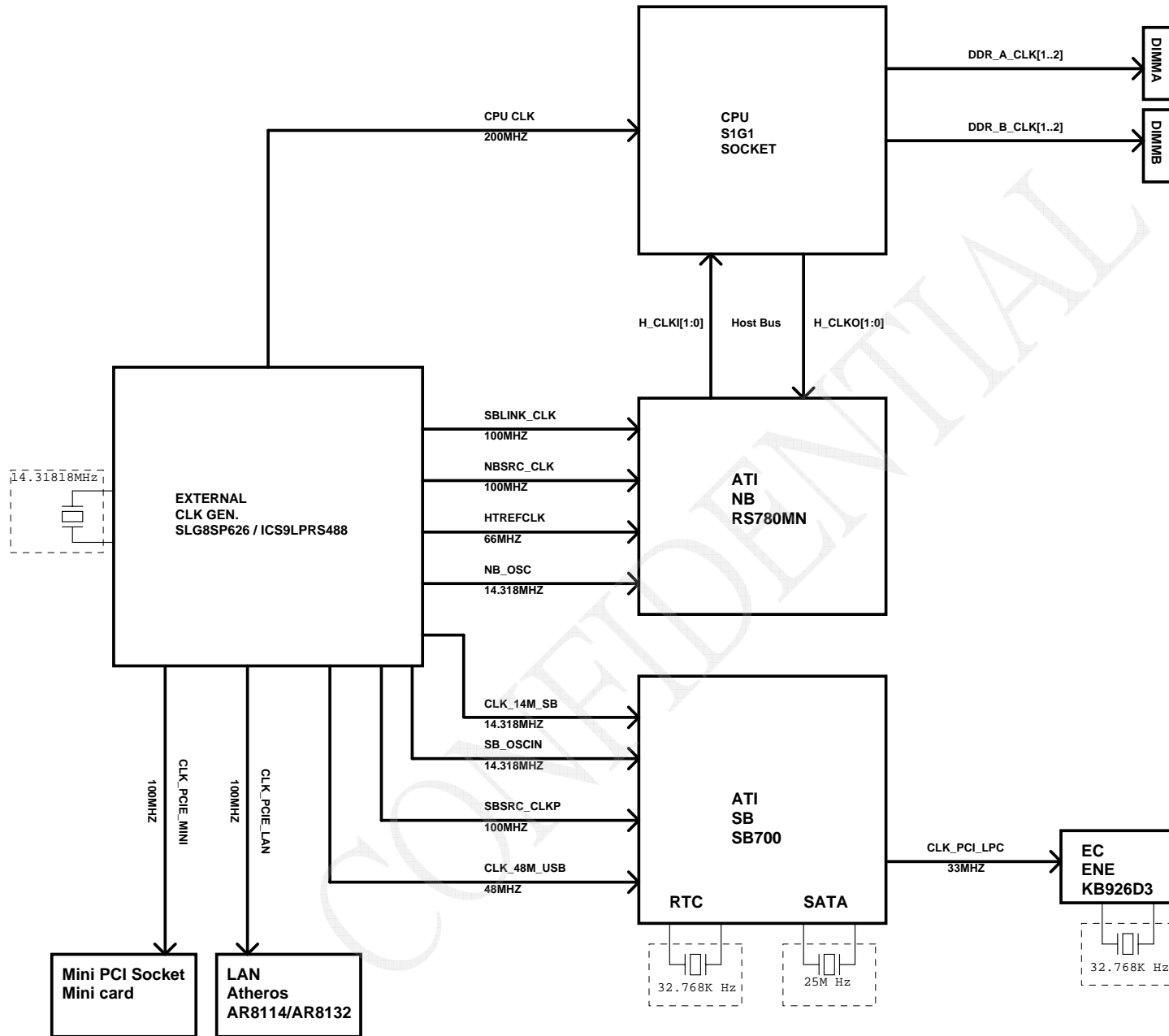
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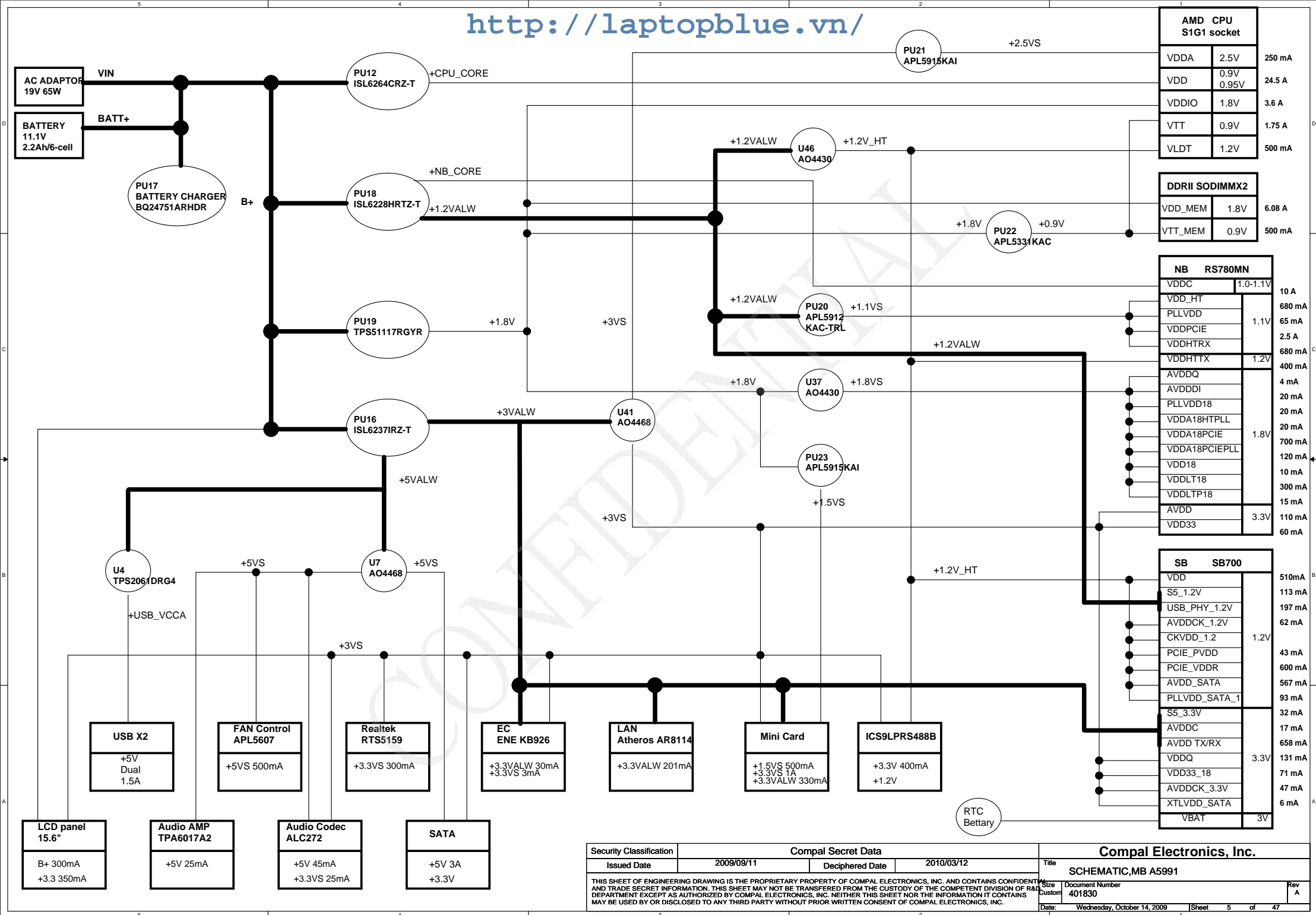
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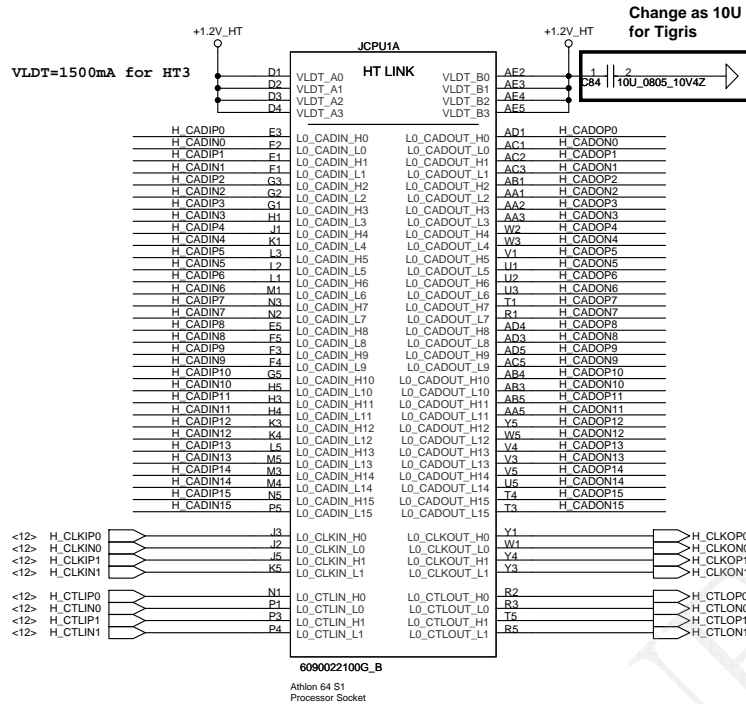


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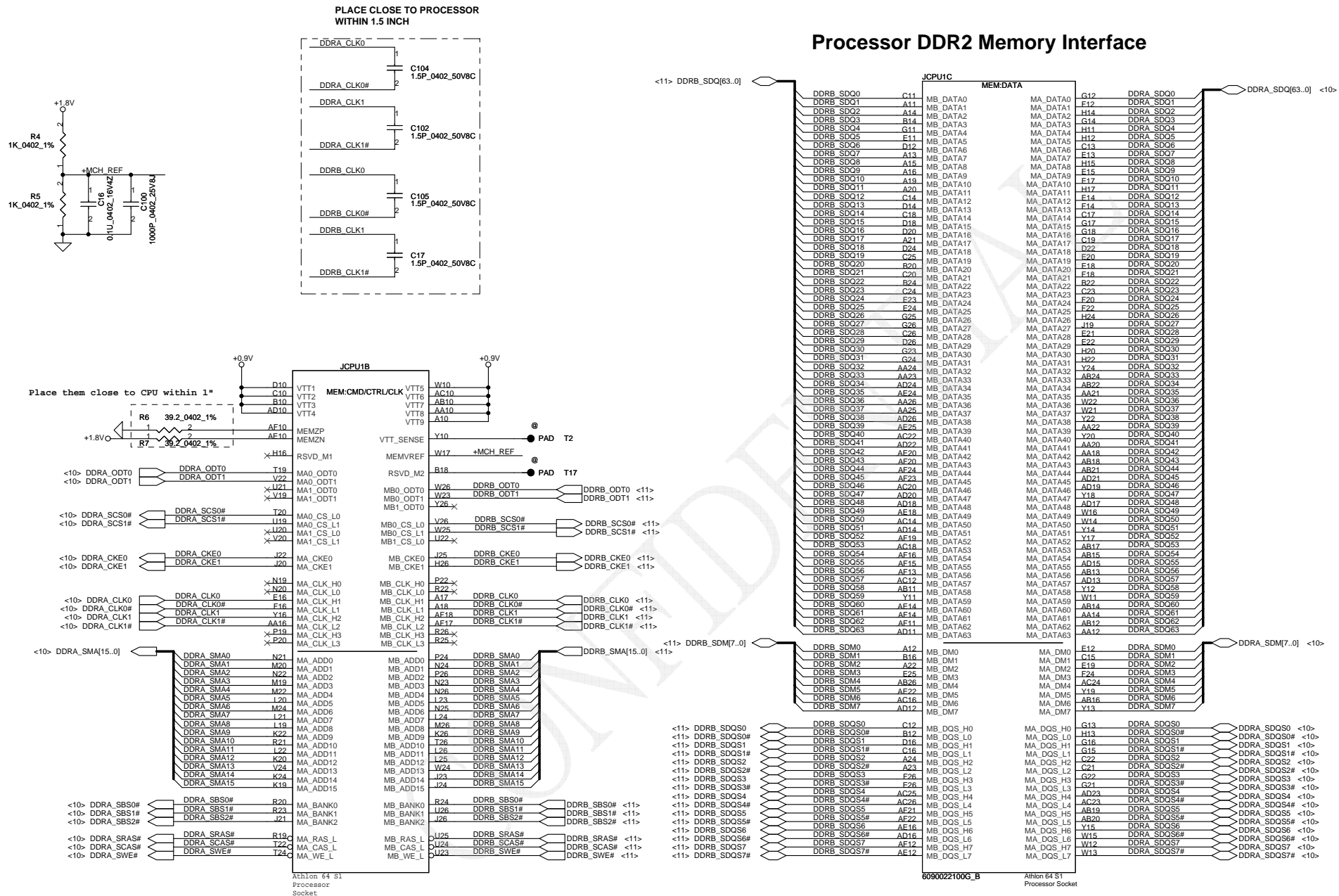


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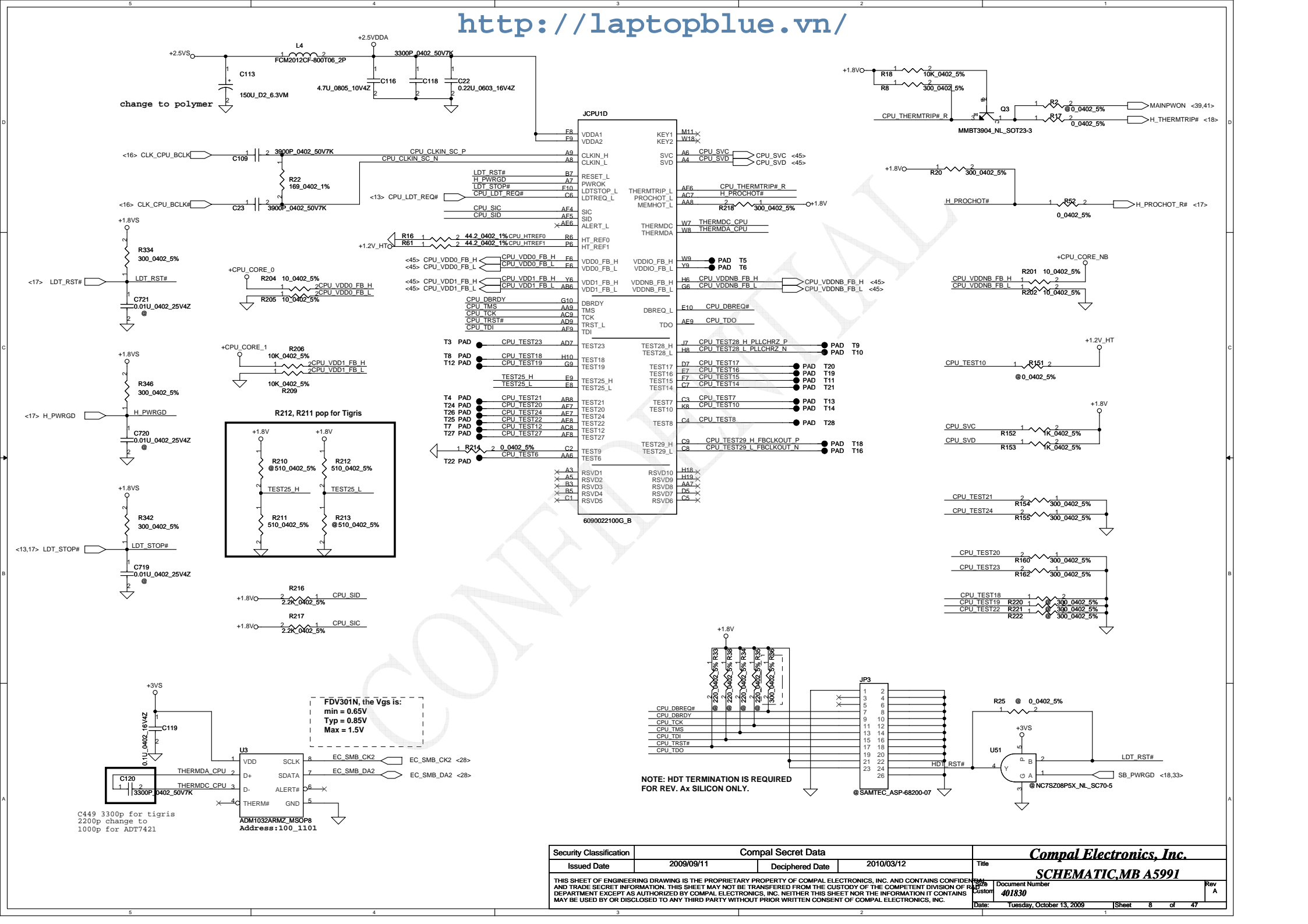




Processor DDR2 Memory Interface



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change to polymer

FDV301N, the Vgs is:
 min = 0.65V
 Typ = 0.85V
 Max = 1.5V

NOTE: HDT TERMINATION IS REQUIRED FOR REV. A.x SILICON ONLY.

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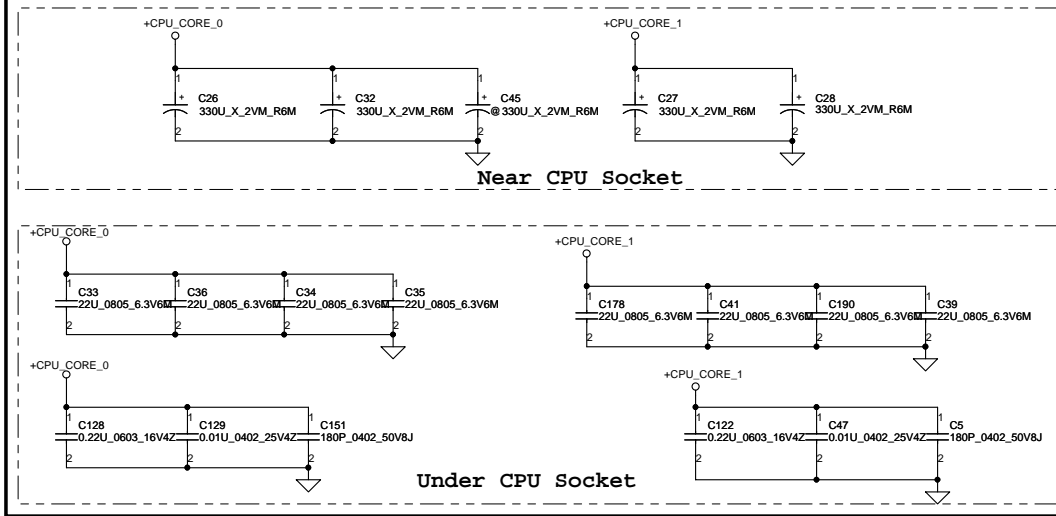
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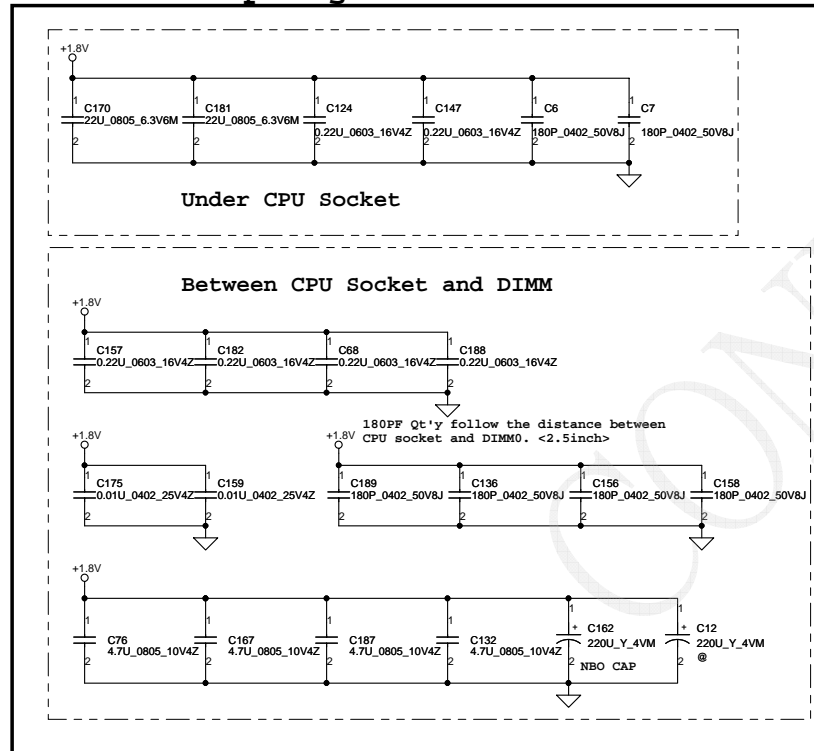
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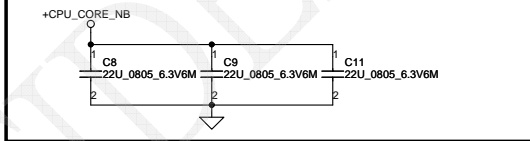
VDD(+CPU_CORE) decoupling.



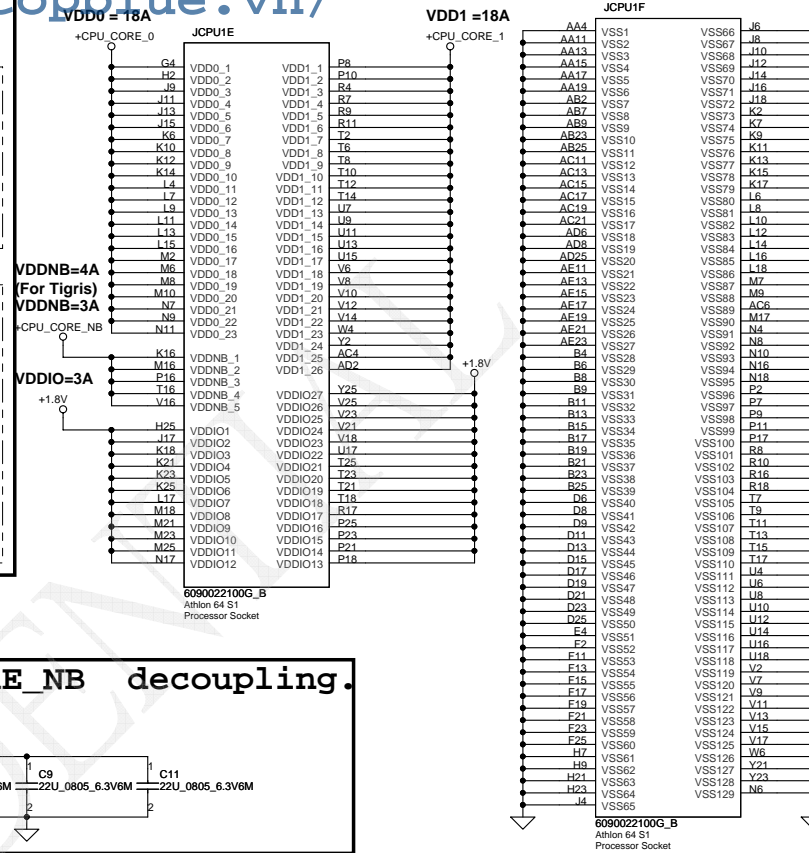
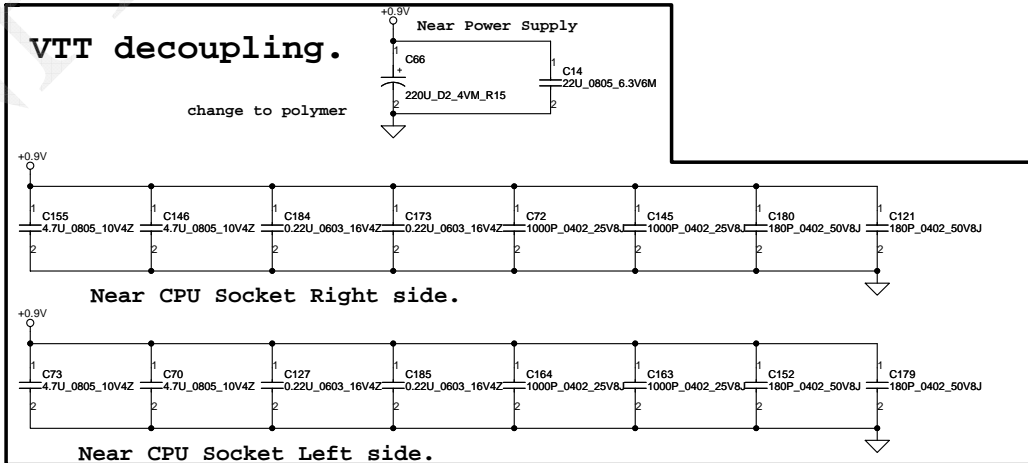
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.

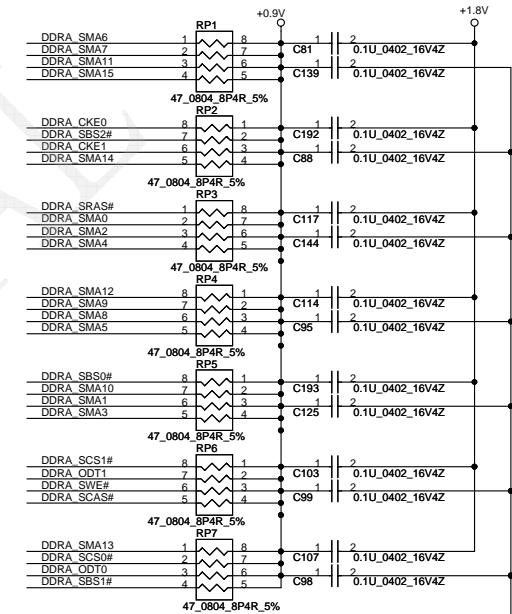
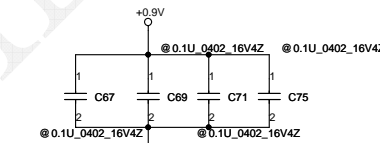
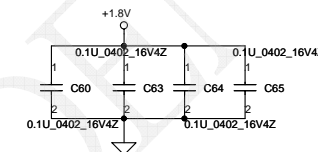
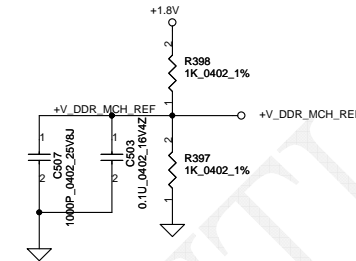


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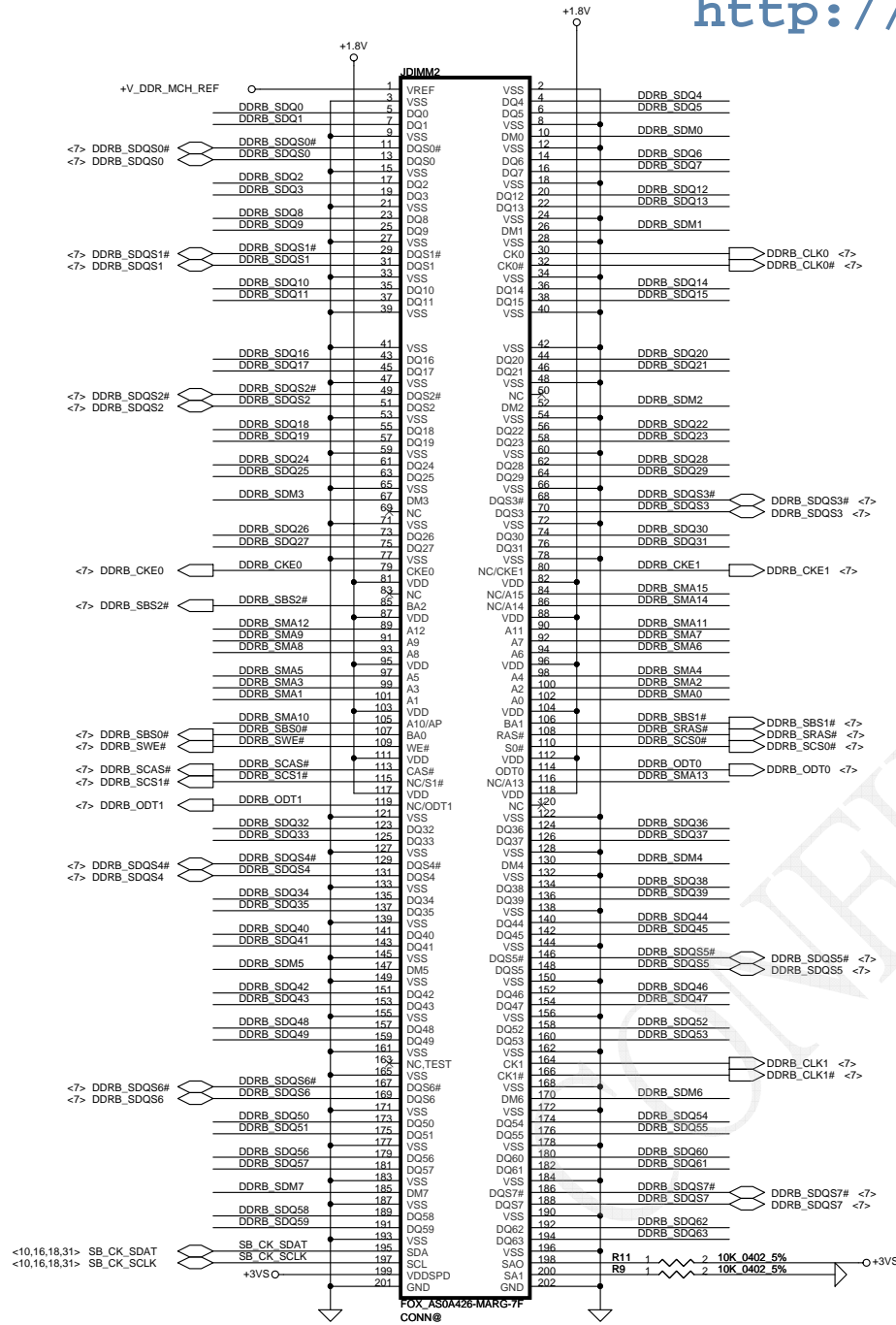
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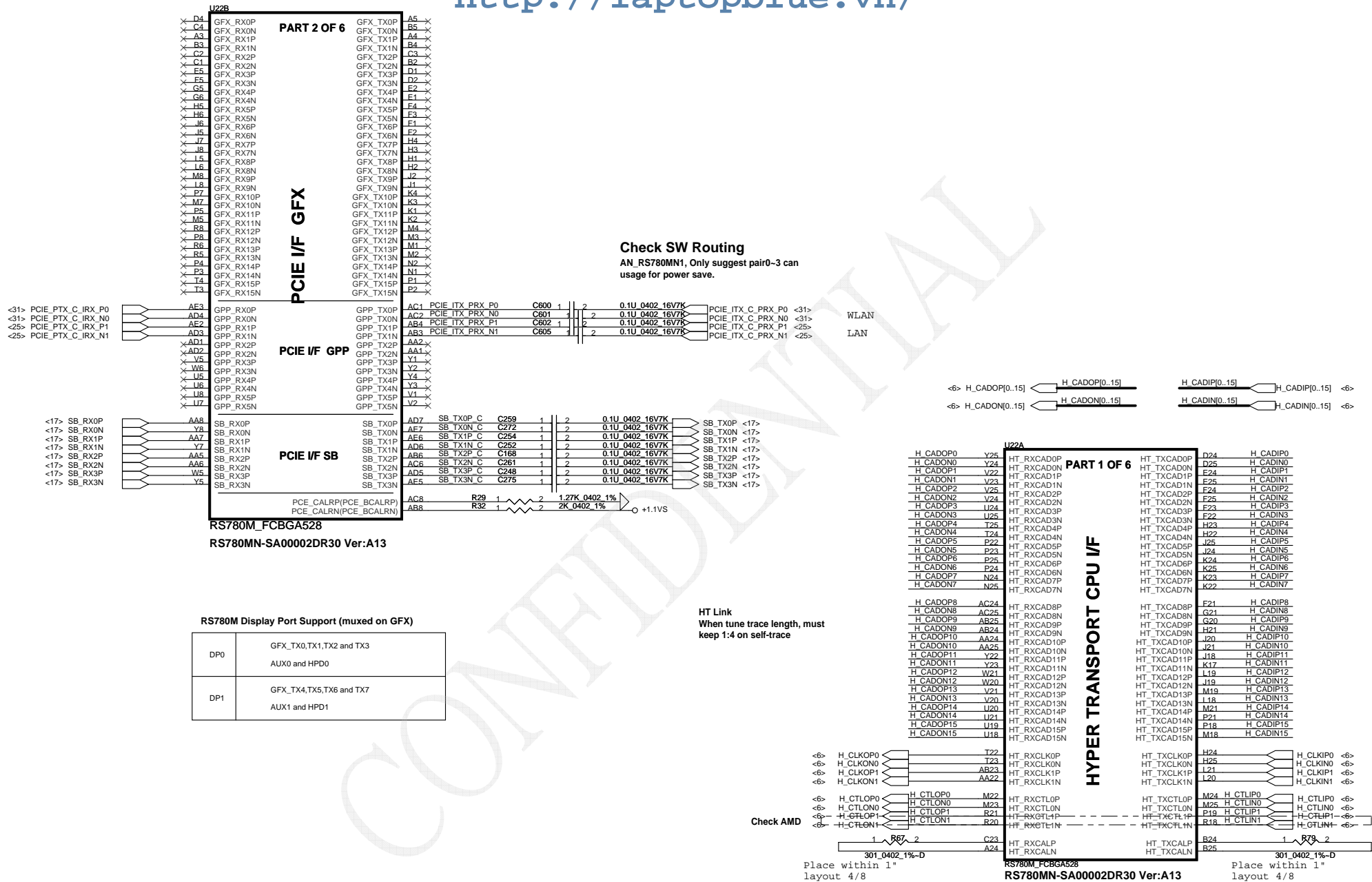


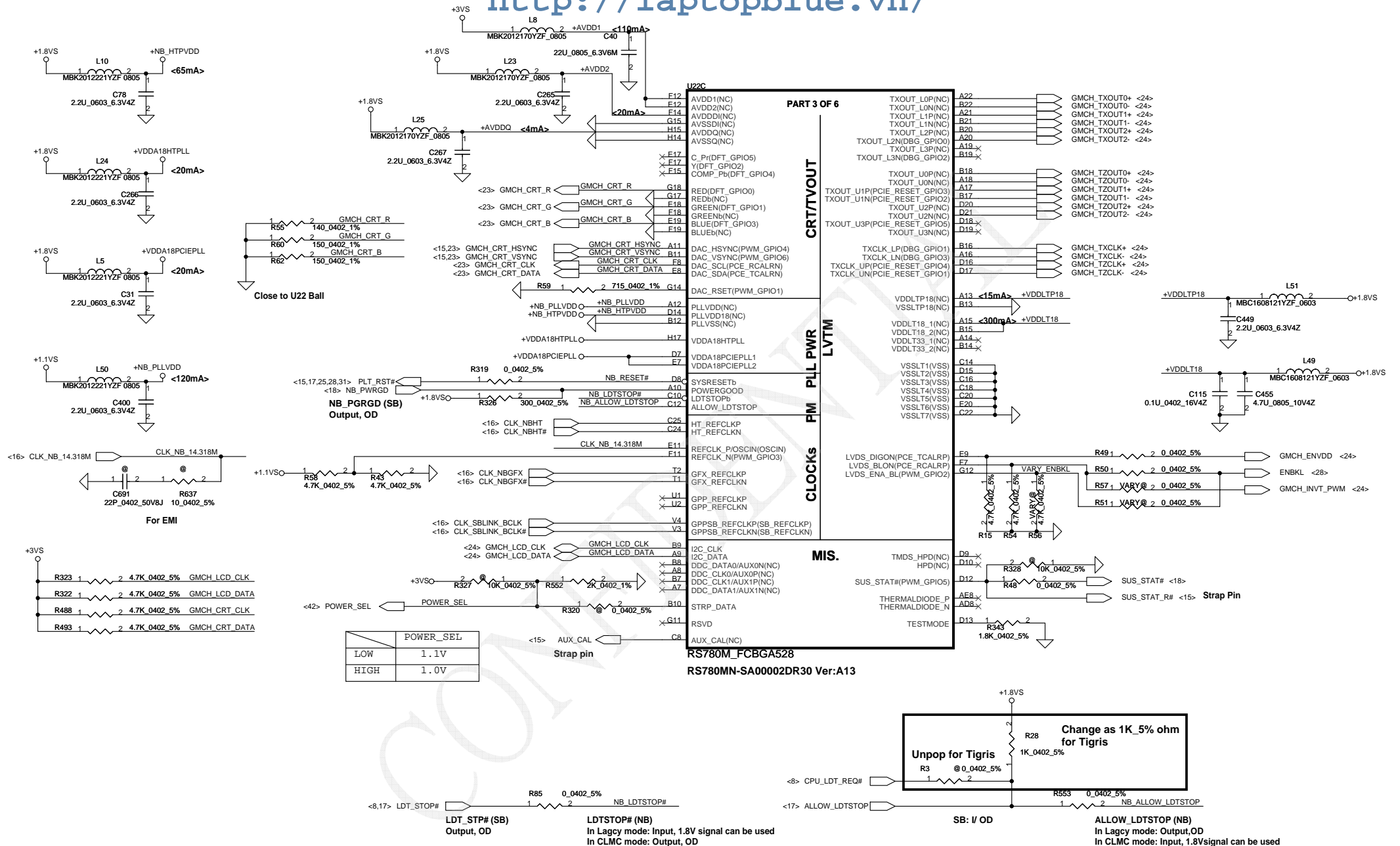
DIMM1 REV H:9.2mm (BOT)

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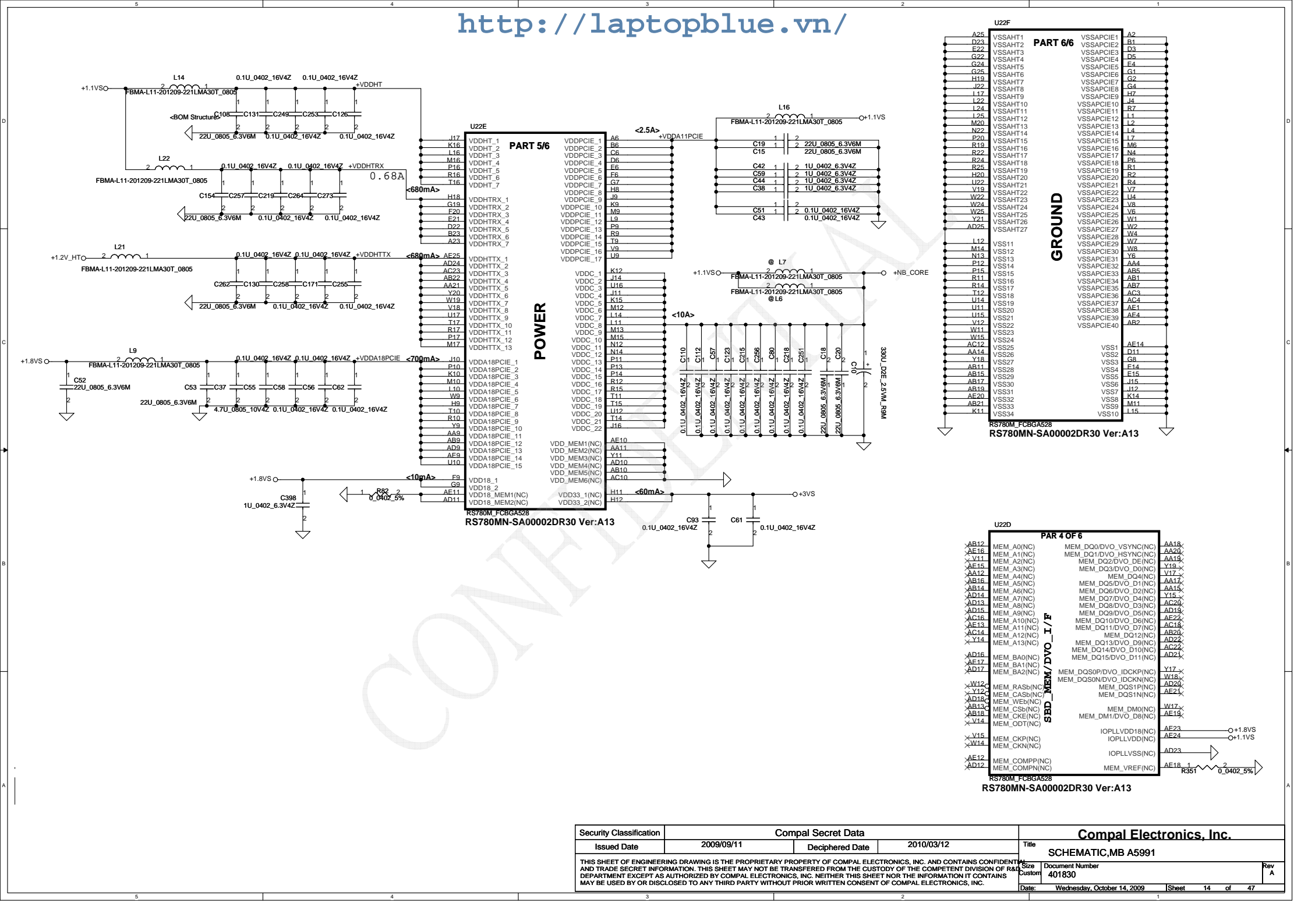
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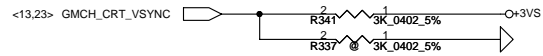
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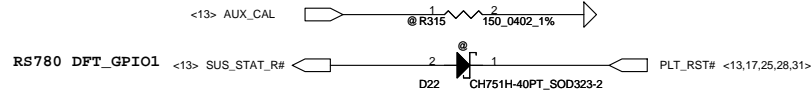
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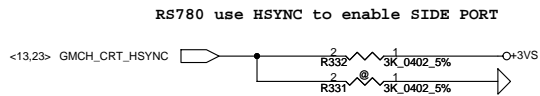
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

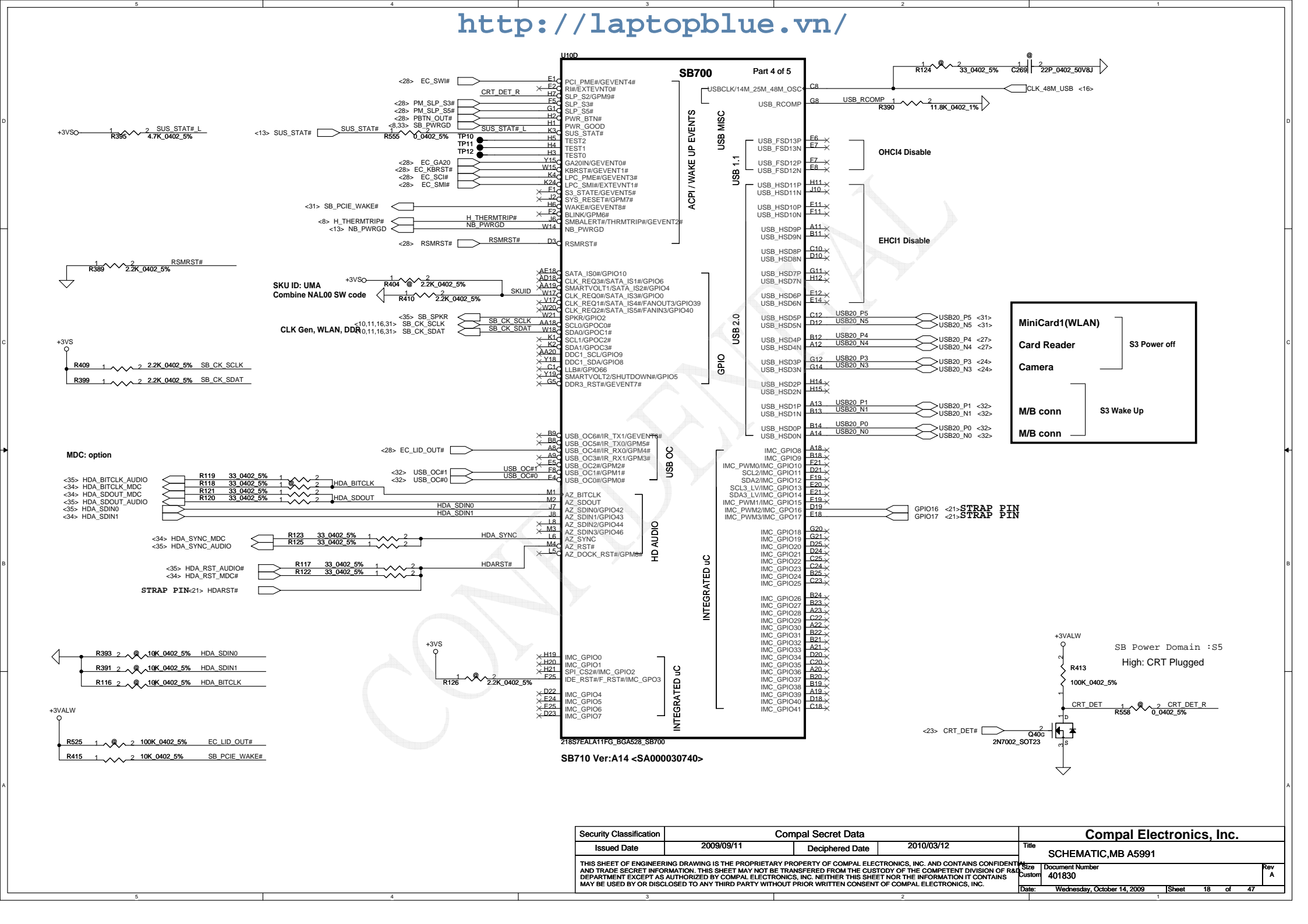


RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

Main
HDD

2nd
HDD

Main
ODD

2nd
ODD

<22> SATA_STX_DRX_P0
<22> SATA_STX_DRX_N0
<22> SATA_DTX_C_SRX_N0
<22> SATA_DTX_C_SRX_P0
<22> SATA_STX_DRX_P1
<22> SATA_STX_DRX_N1
<22> SATA_DTX_C_SRX_N1
<22> SATA_DTX_C_SRX_P1
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<22> SATA_DTX_C_SRX_N2
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<22> SATA_STX_DRX_P3
<22> SATA_STX_DRX_N3
<22> SATA_DTX_C_SRX_N3
<22> SATA_DTX_C_SRX_P3

SB700
Part 2 of 5

IDE_IORDY# AA24
IDE_IRQ# AA25
IDE_A0 Y22
IDE_A1 Y23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AC24
IDE_IOR# AC24
IDE_IOW# Y25
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE22
IDE_D3/GPIO18 AC22
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AD20
IDE_D10/GPIO25 AE21
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23
SPI_DI/GPIO12 G6
SPI_DO/GPIO11 D2
SPI_CLK/GPIO47 D1
SPI_HOLD#/GPIO31 F4
SPI_CS1#/GPIO32 F3
LAN_RST#/GPIO13 J15
ROM_RST#/GPIO14 J1
FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 P8
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 D4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7
AVDD F6
AVSS G7

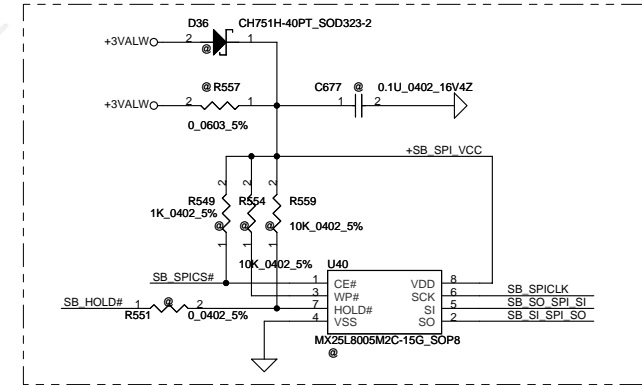
SERIAL ATA

SPI ROM

HW MONITOR

SATA PWR

218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12



Reserve For Debug

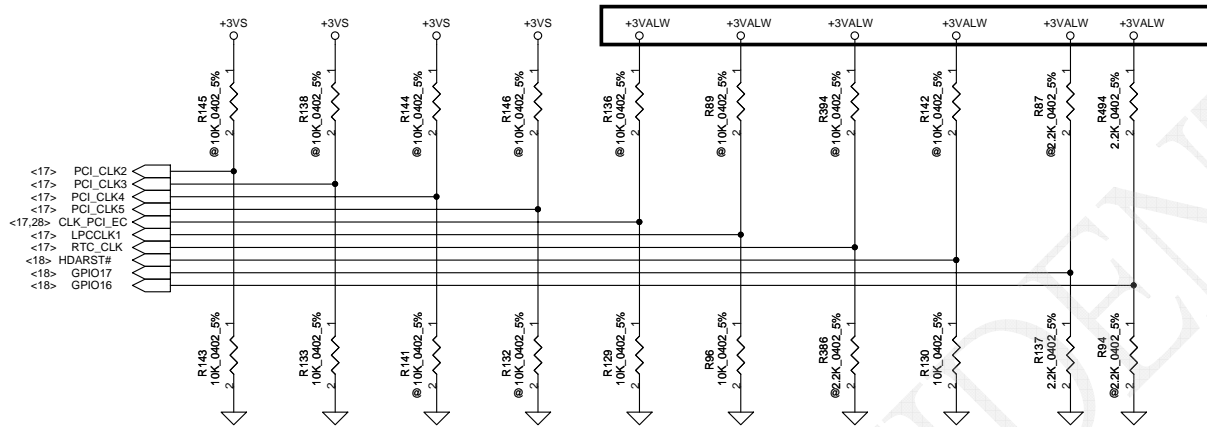
for ACIN level issue

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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

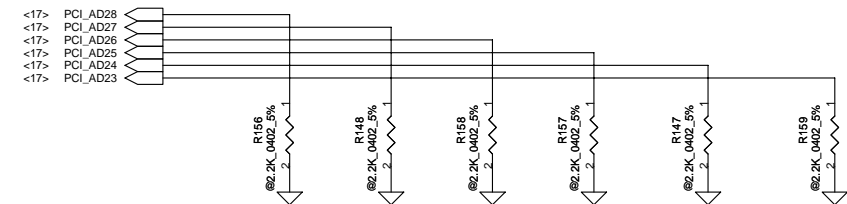


DEBUG STRAPS

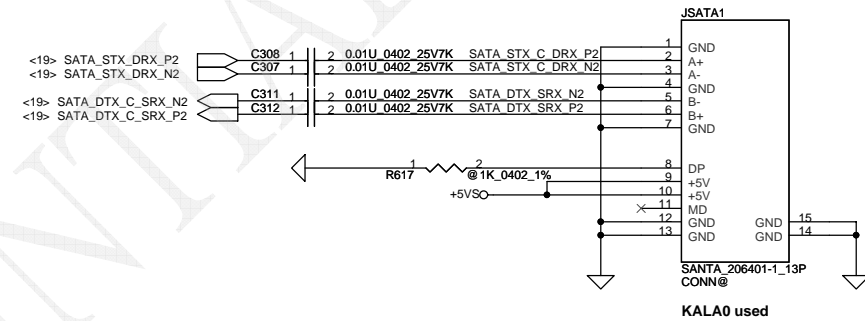
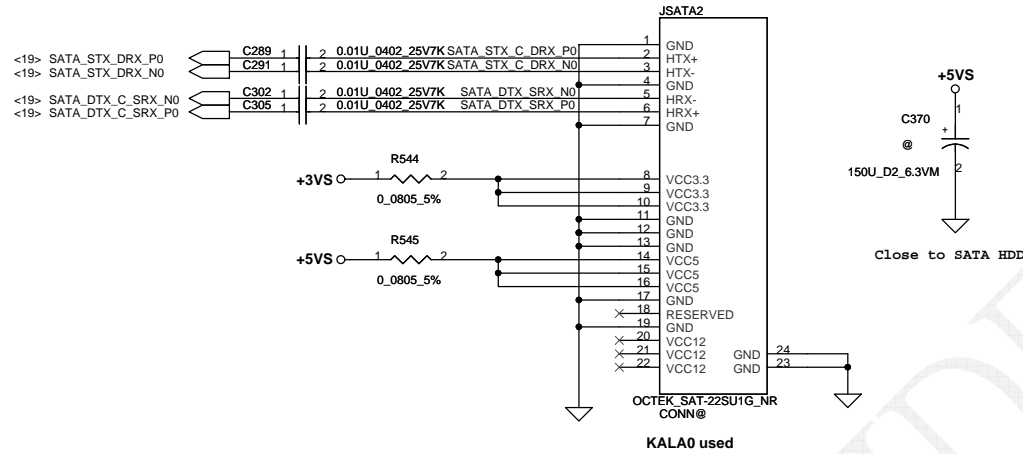
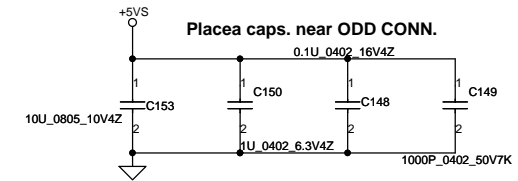
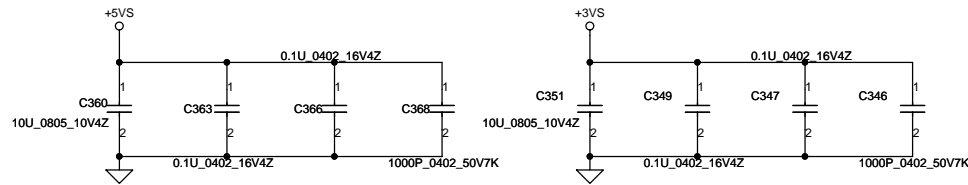
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

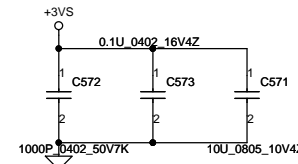
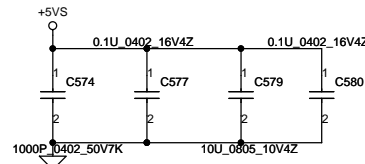
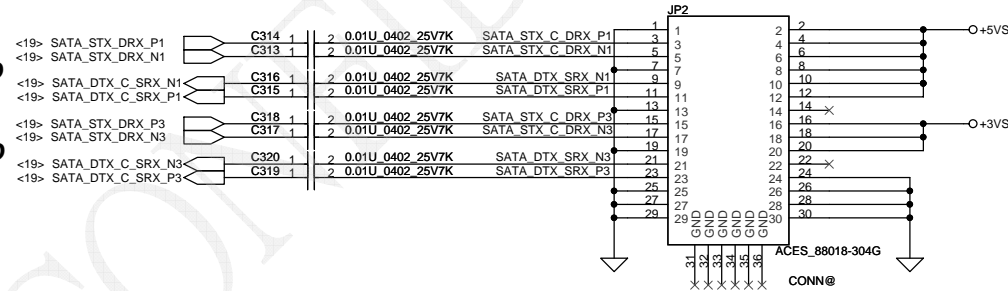


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Second HDD

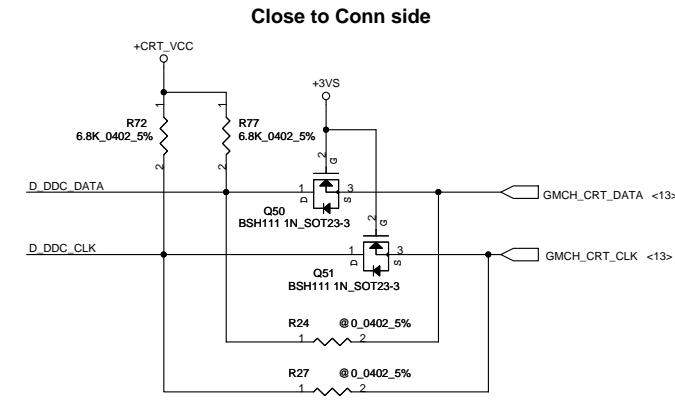
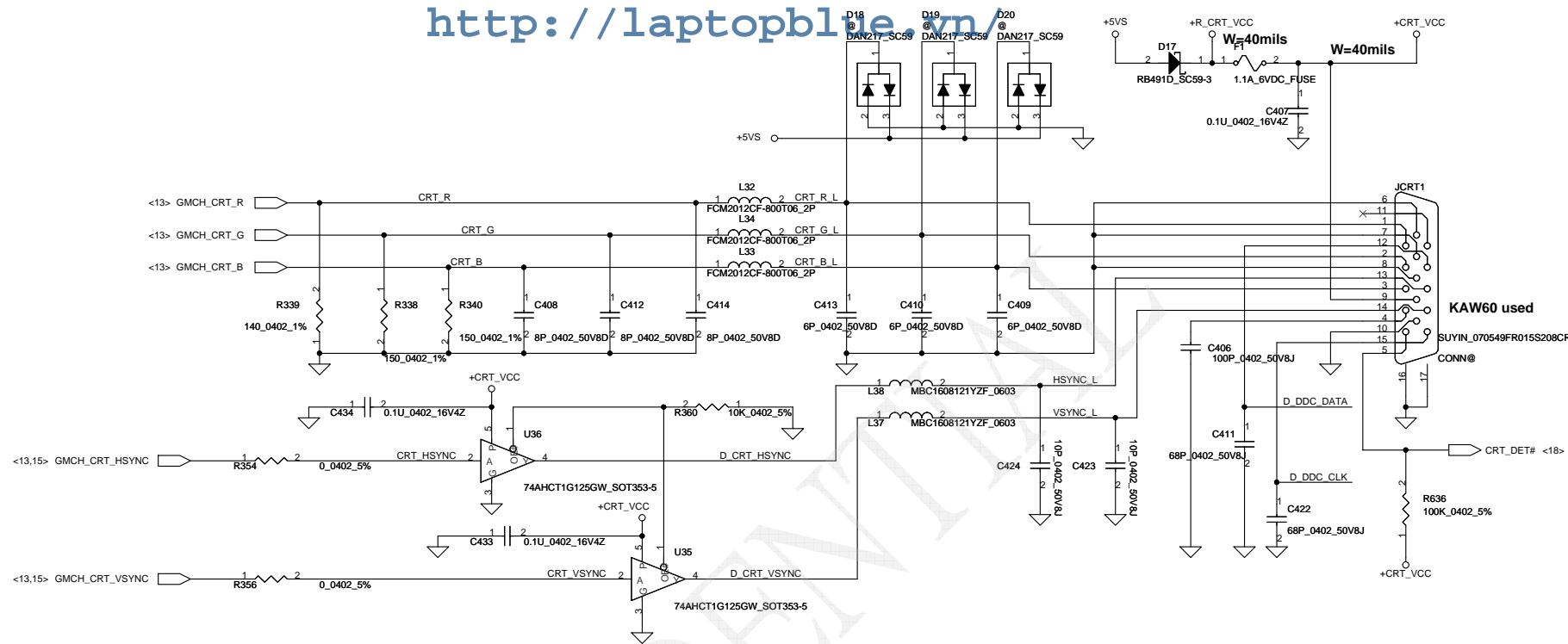
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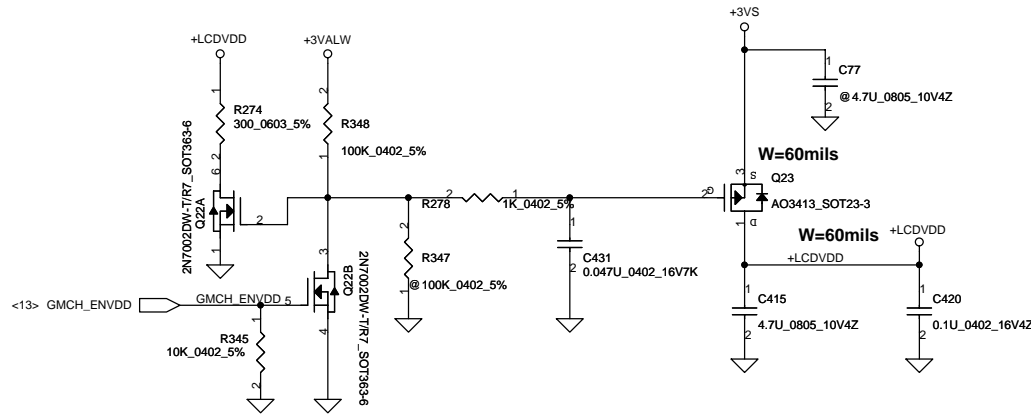
CRT Connector

http://laptopbluie.vn/

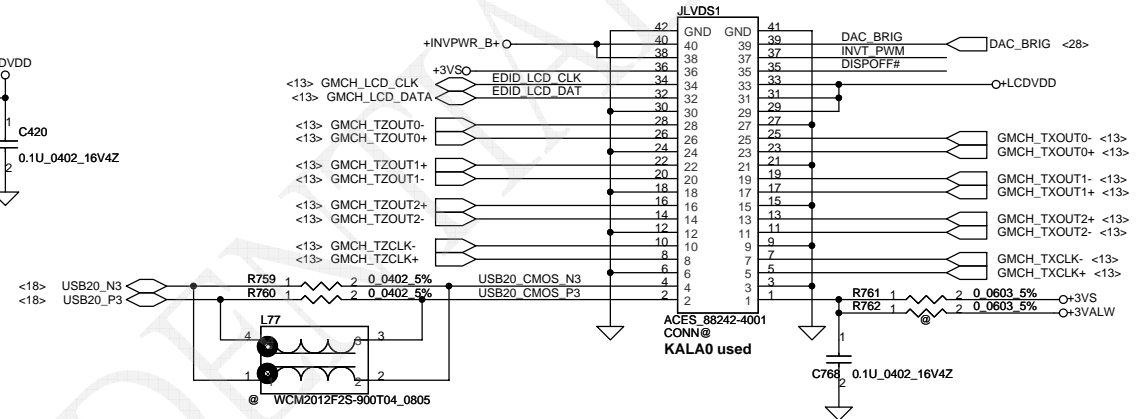


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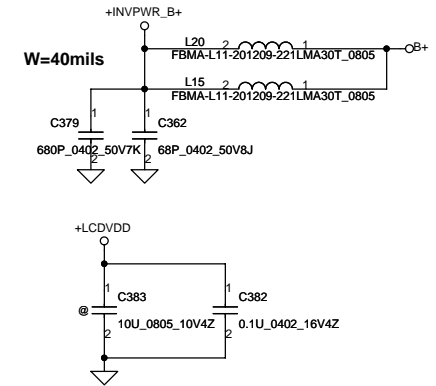
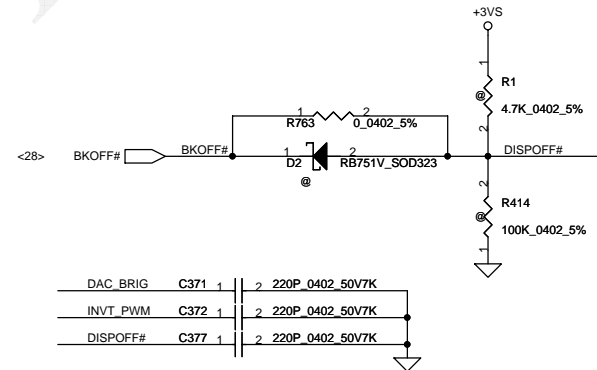
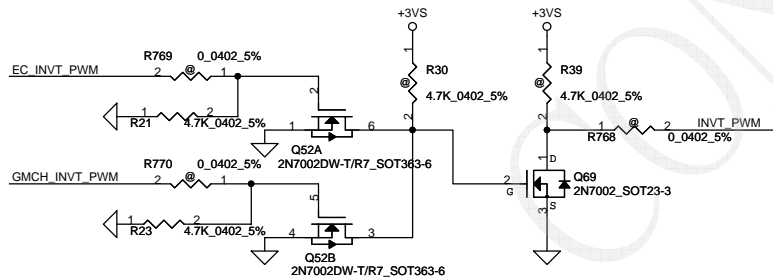
LCD POWER CIRCUIT



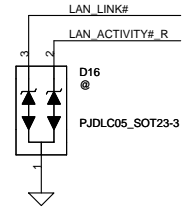
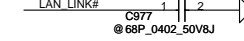
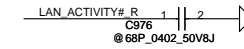
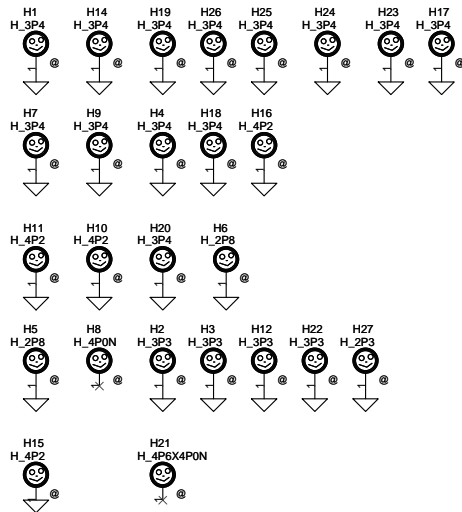
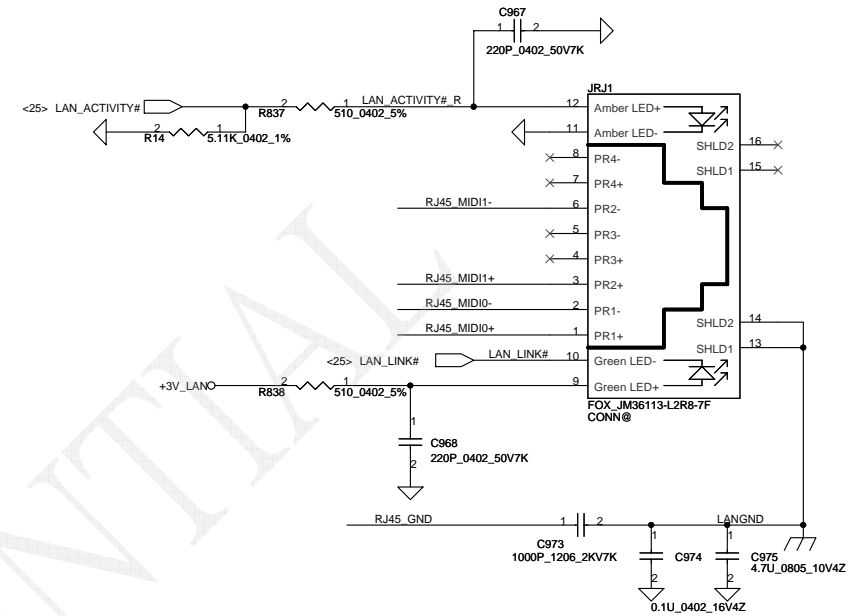
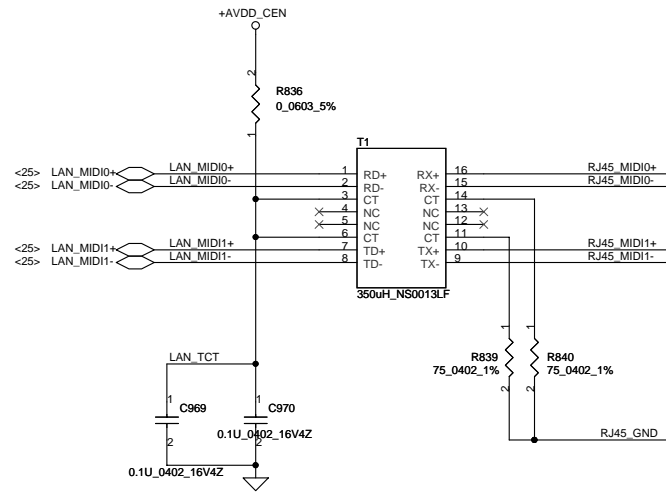
LCD/PANEL CONN.



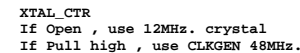
VARYBRIGHT FUNCTION



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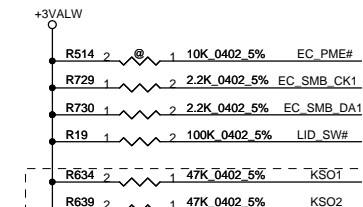
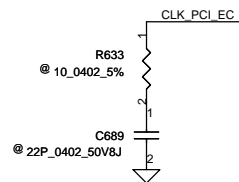


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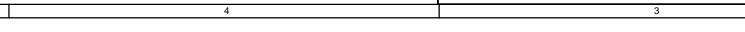
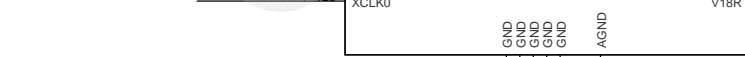
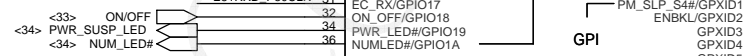
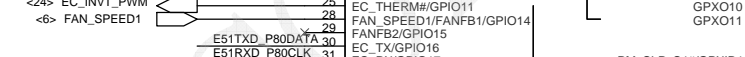
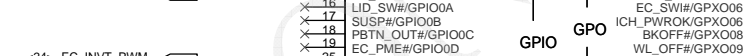
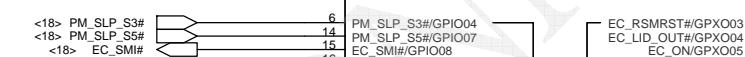
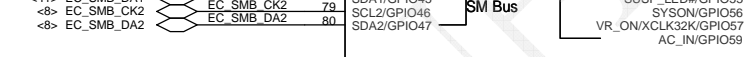
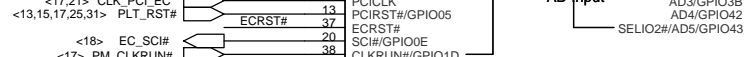
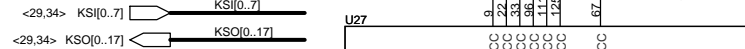
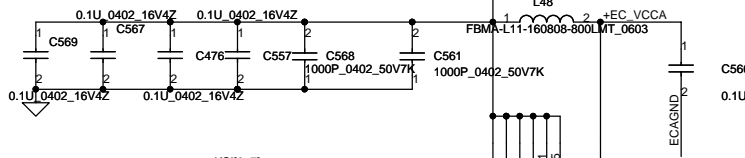
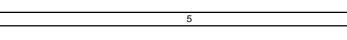
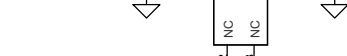
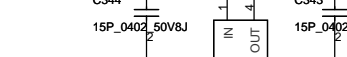
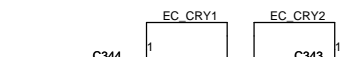
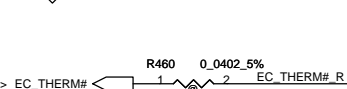
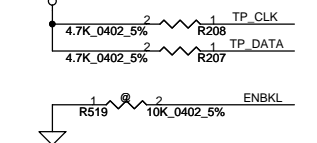
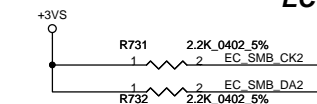


EMI

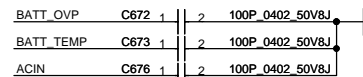
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EC test-mode issue

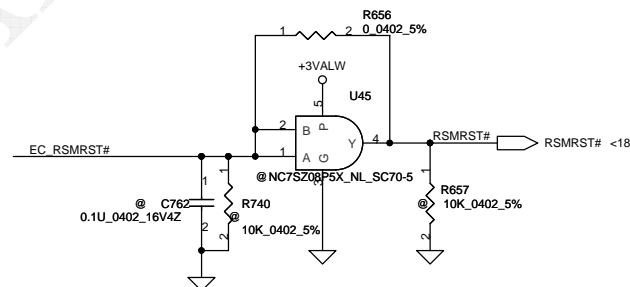
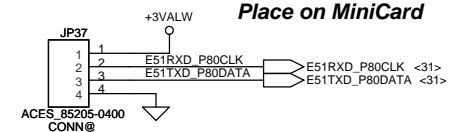


Please close to EC pin

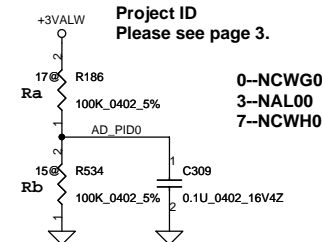


For EC Tools

Place on MiniCard

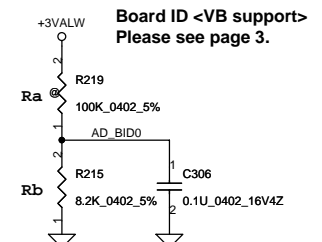


Project ID
Please see page 3.



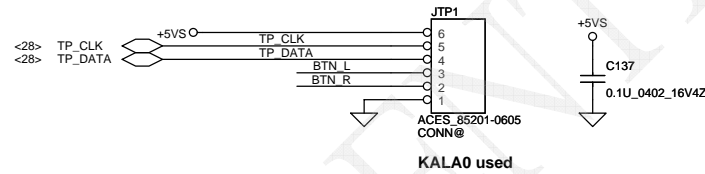
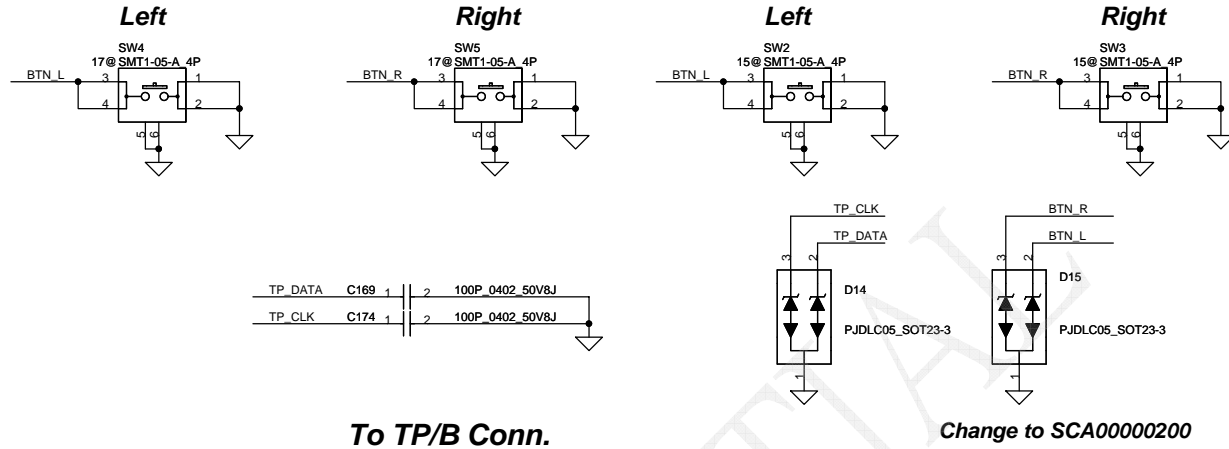
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3--NAL00
7--NCWH0

Board ID <VB support>
Please see page 3.



Chagne to D3 version

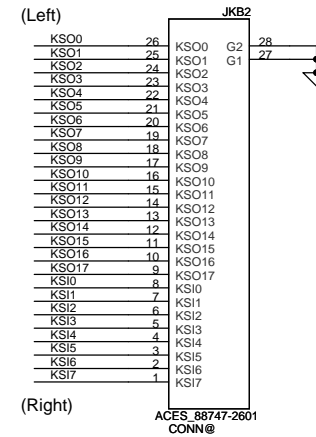
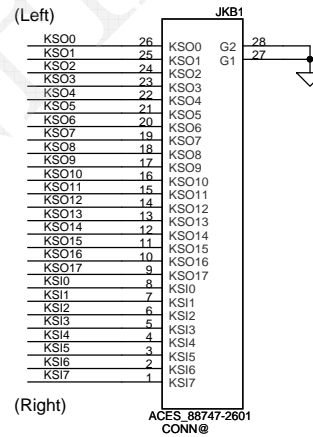
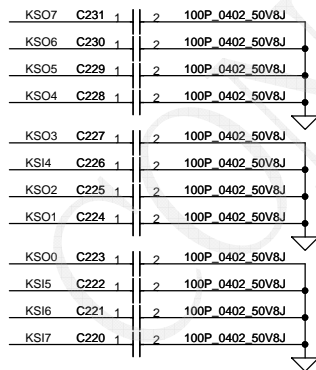
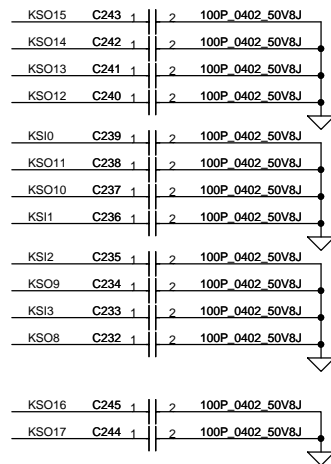
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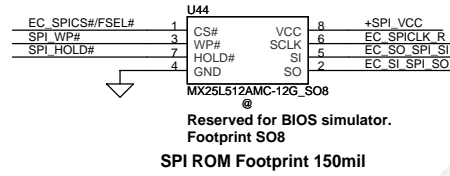
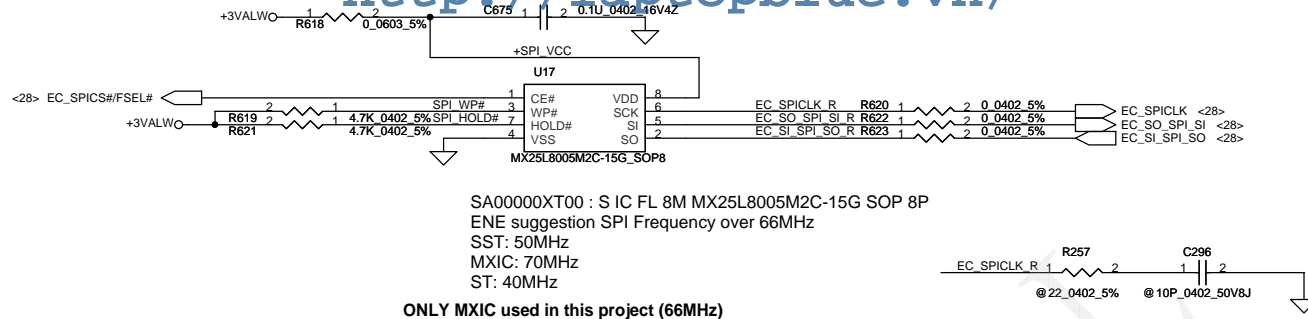
INT_KBD Conn.



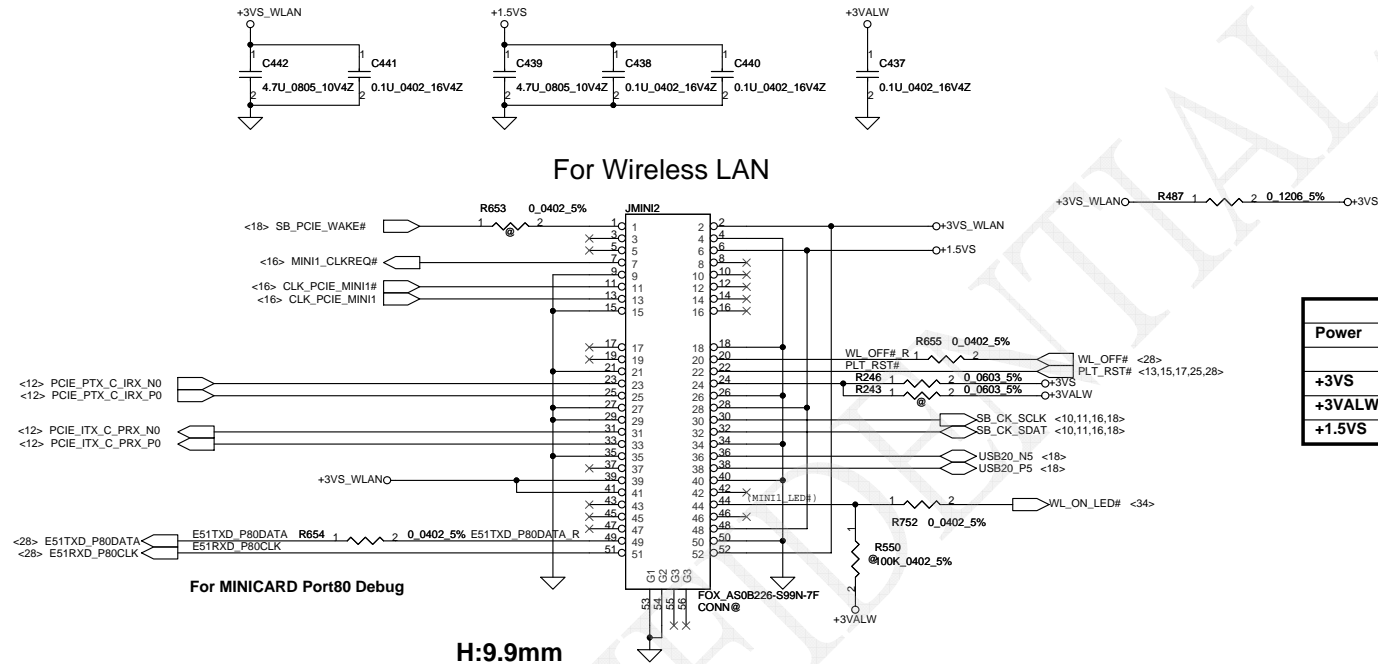
KB1 for 15" KB2 for 17"



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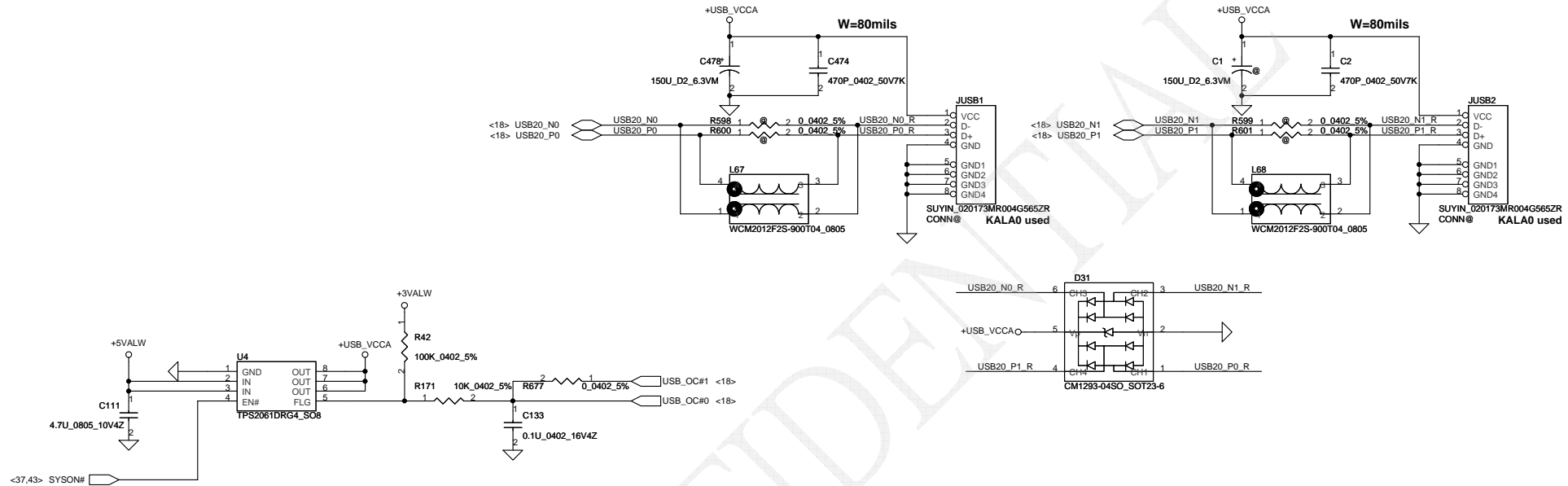


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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

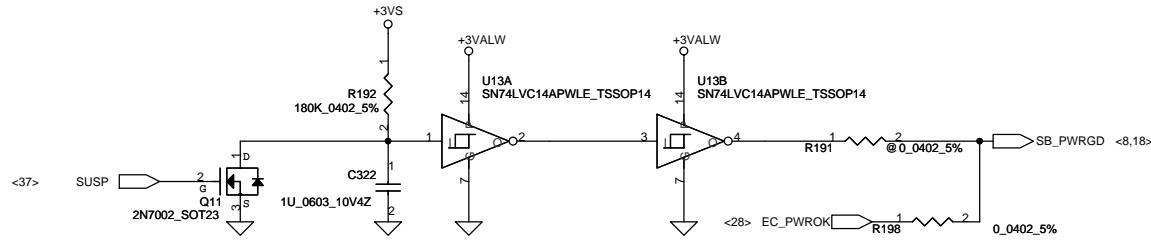
USB CONN. 1 & 2



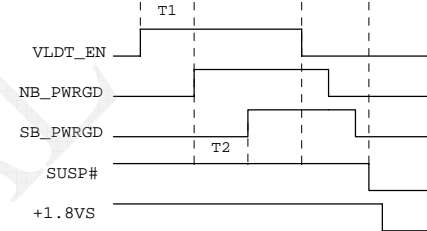
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Power ON Circuit

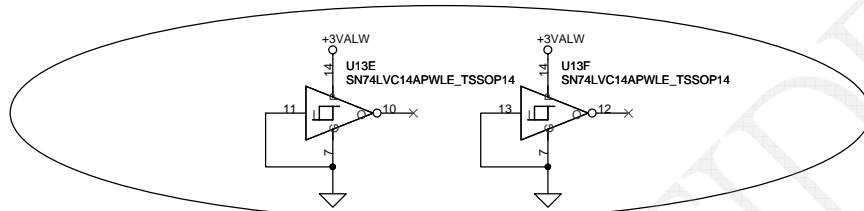
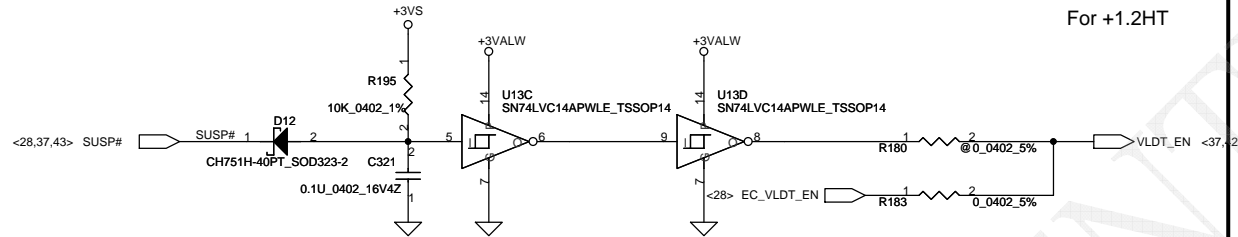
For South Bridge



note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



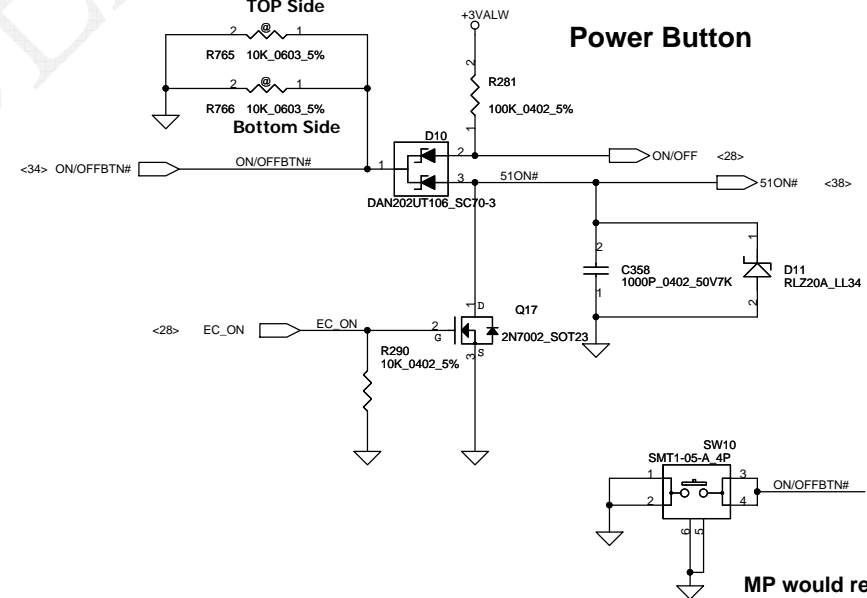
For +1.2HT



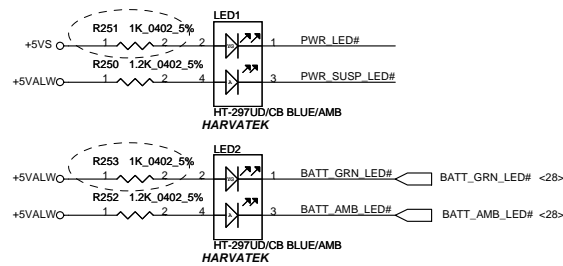
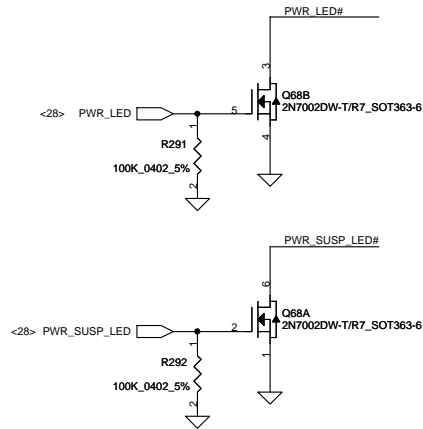
TOP Side

Bottom Side

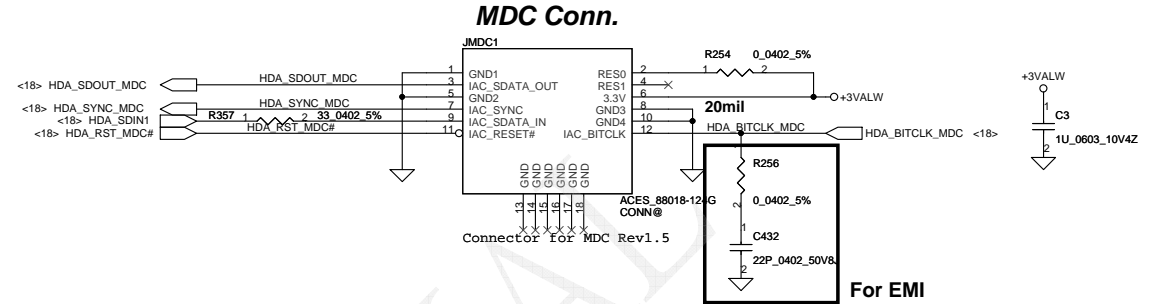
Power Button



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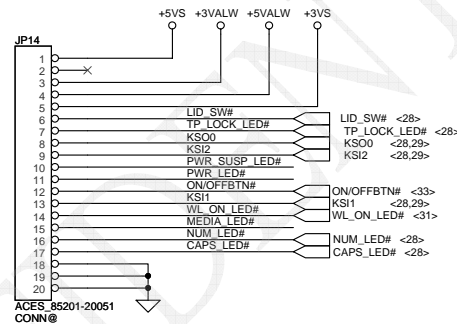


BLUE/AMB LED

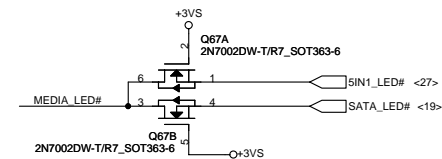
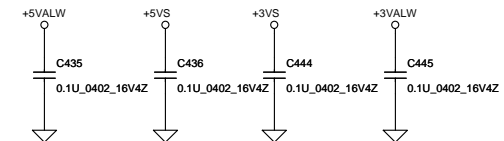


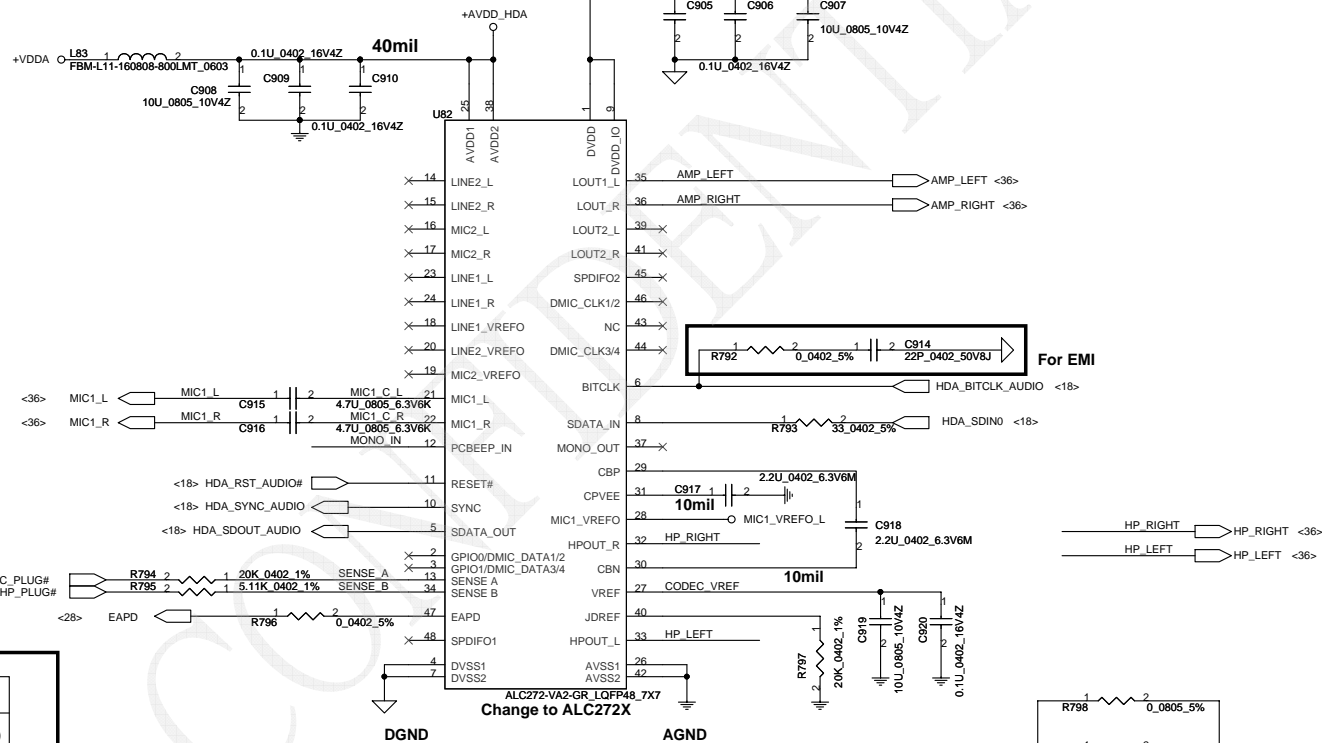
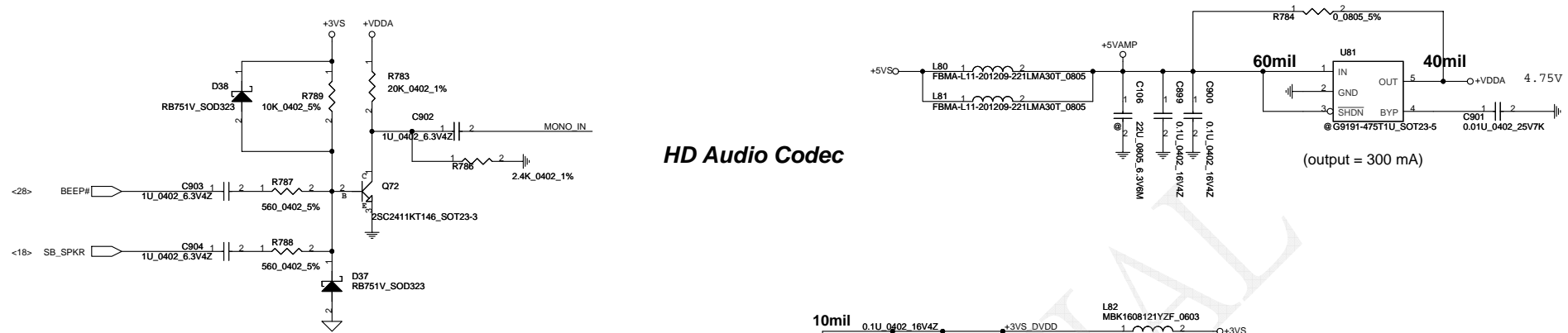
For EMI

To PWR LED/B



	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	

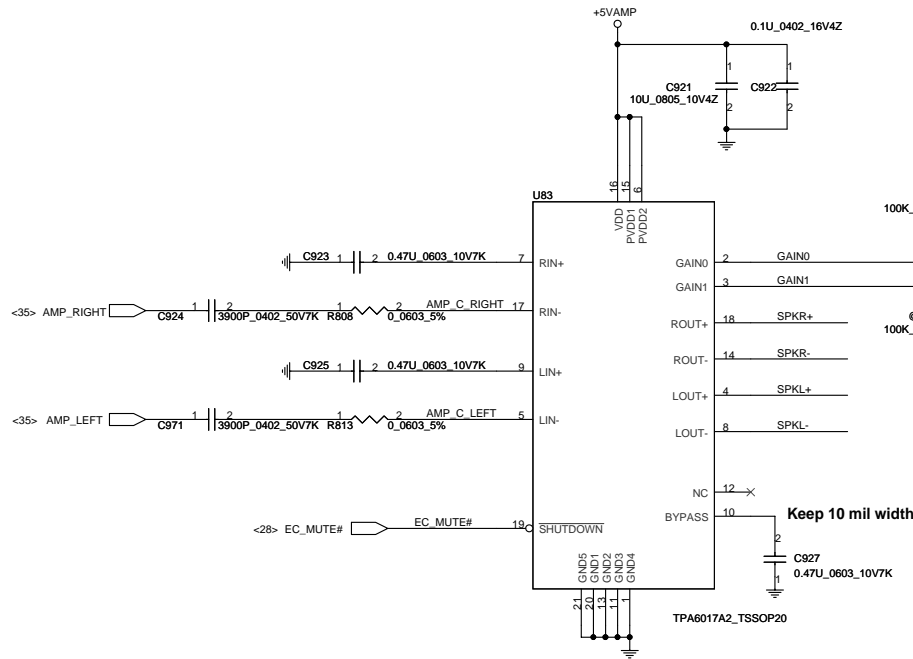




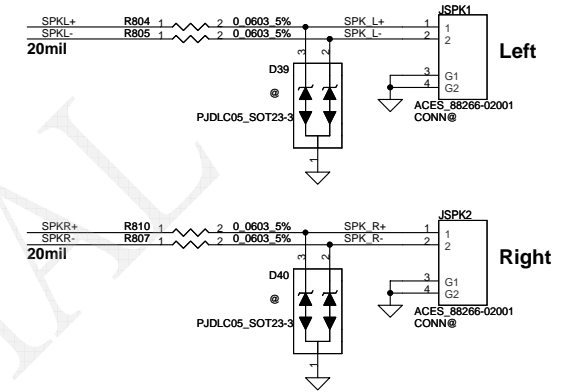
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

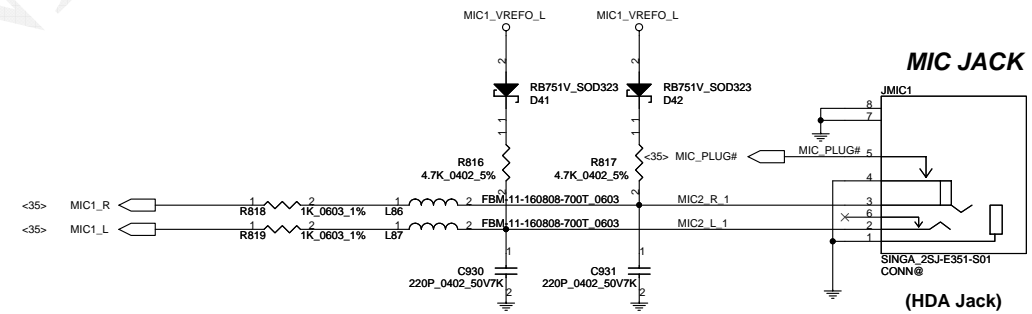
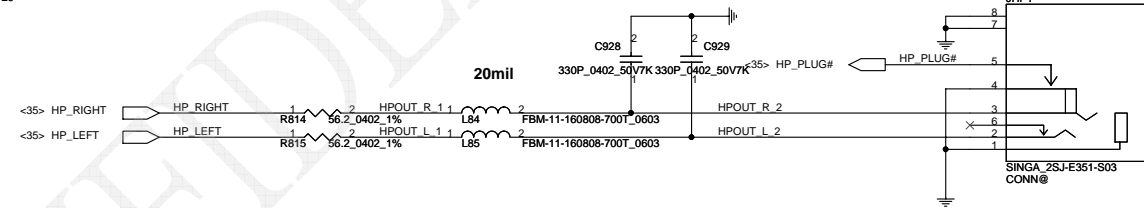
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Int. Speaker Conn.

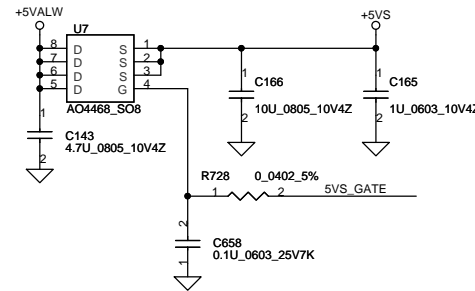


LINE Out/Headphone Out

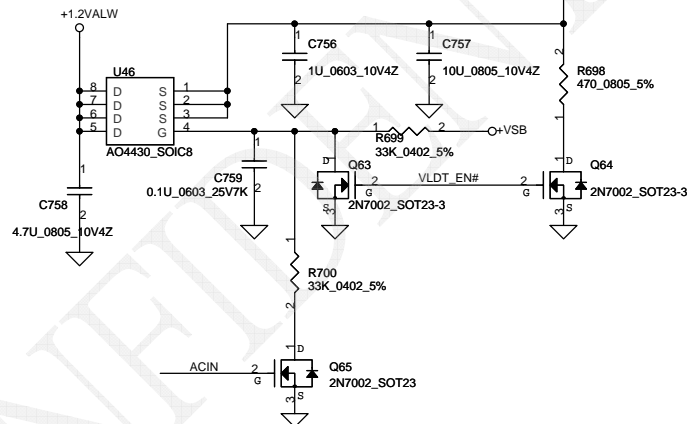


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+5VALW TO +5VS

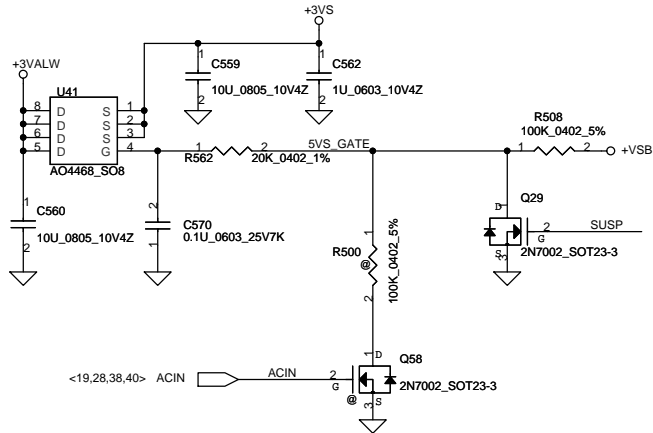


+1.2VALW TO +1.2V_HT

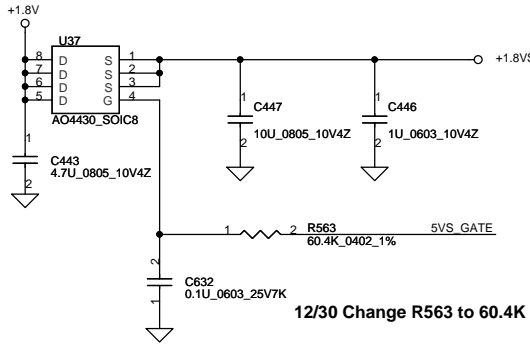


For PWR request

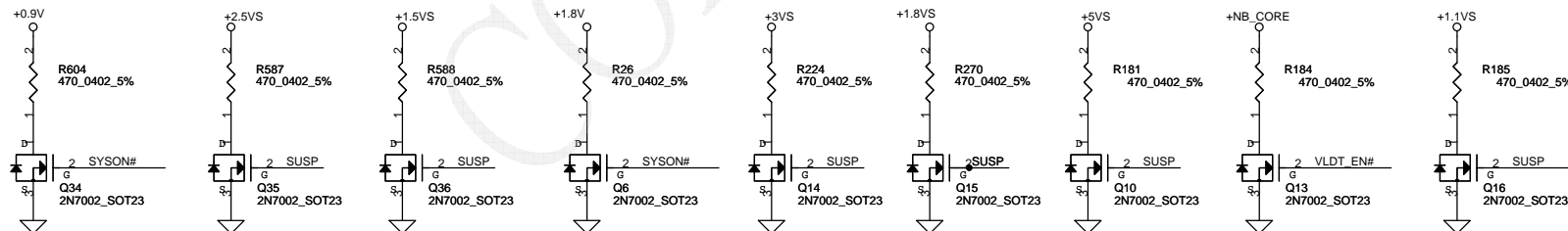
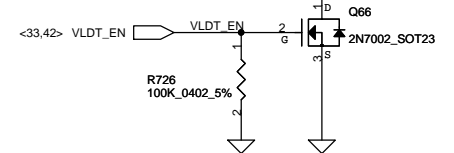
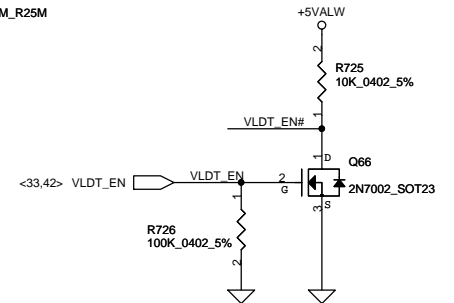
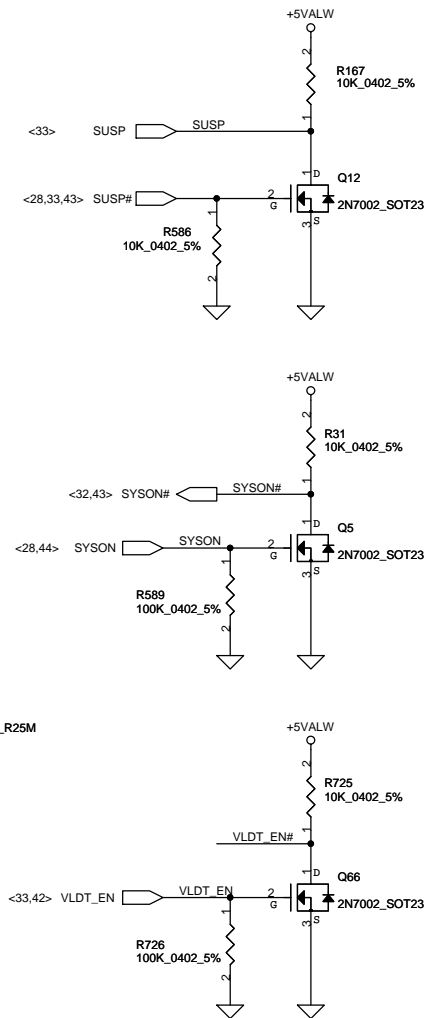
+3VALW TO +3VS



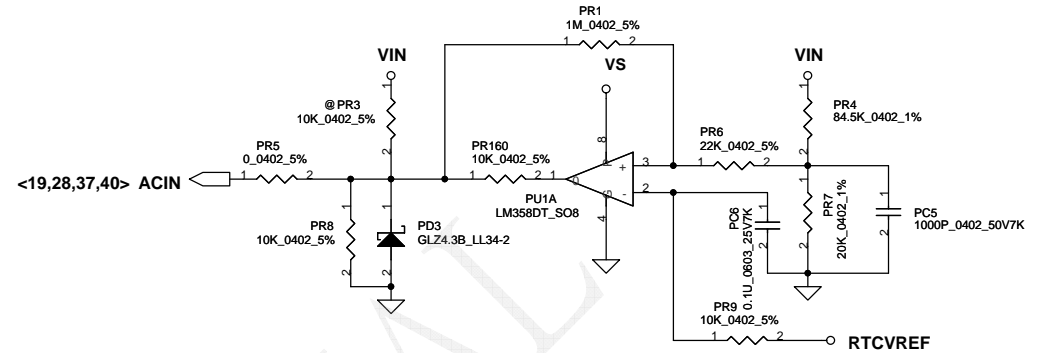
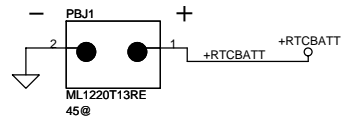
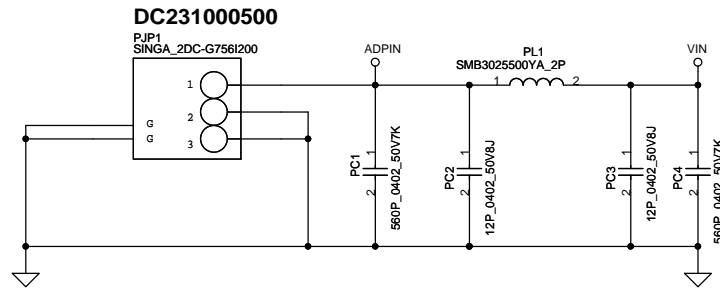
+1.8V TO +1.8VS



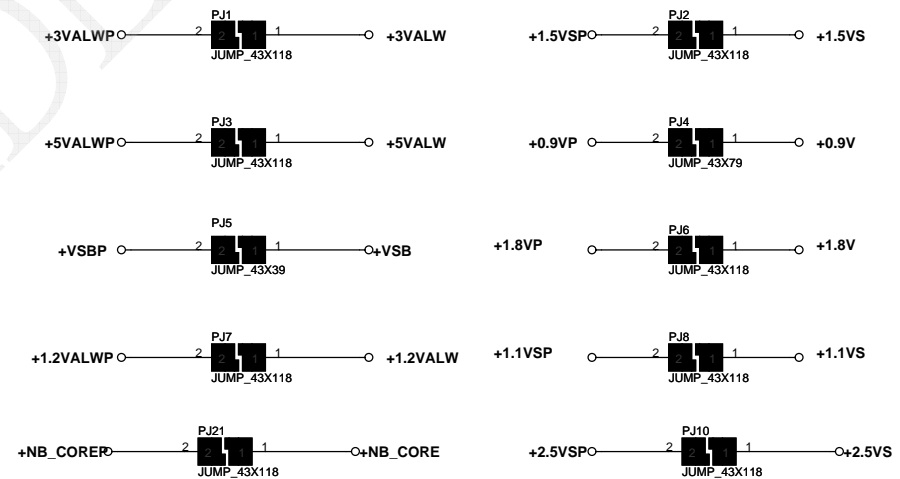
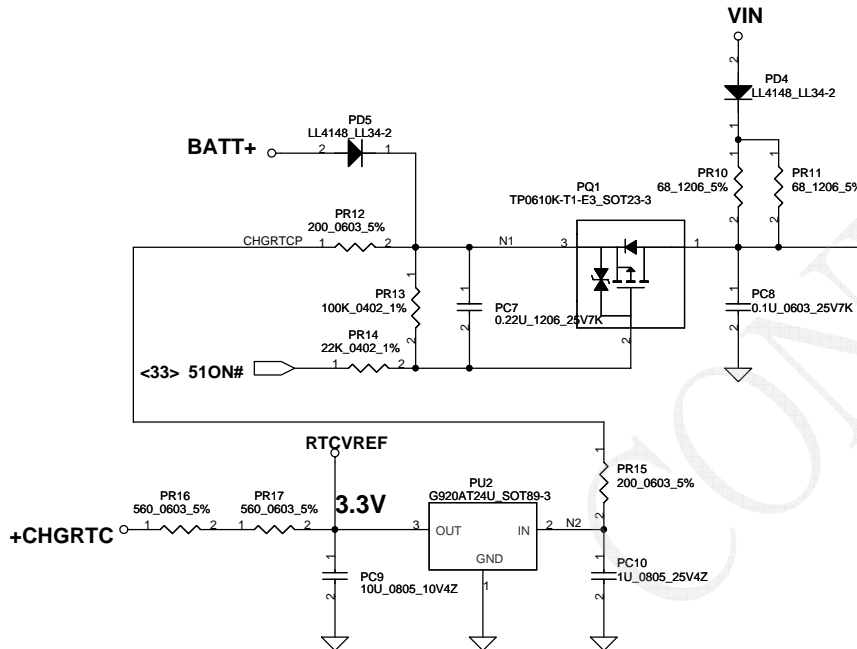
12/30 Change R563 to 60.4K

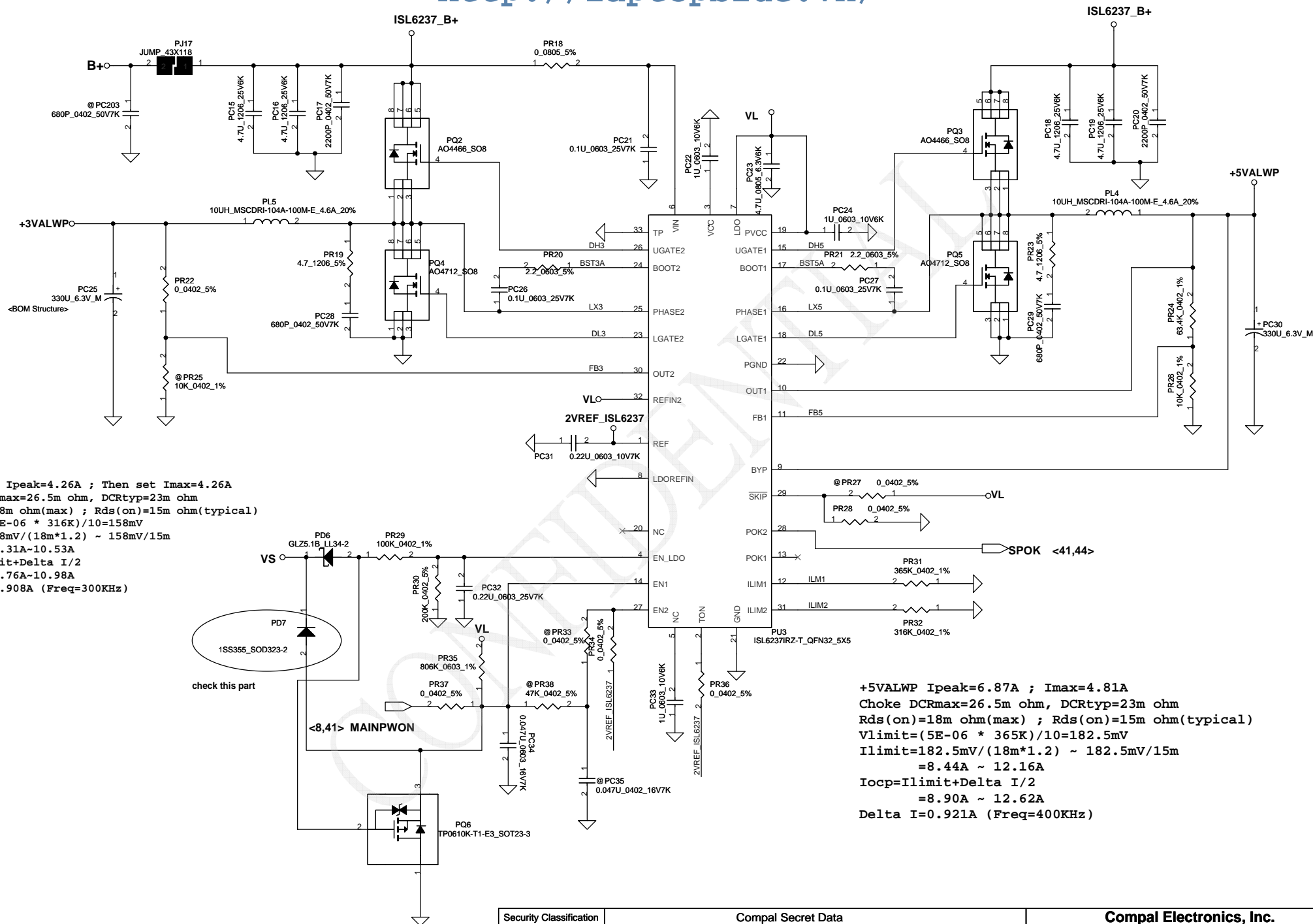


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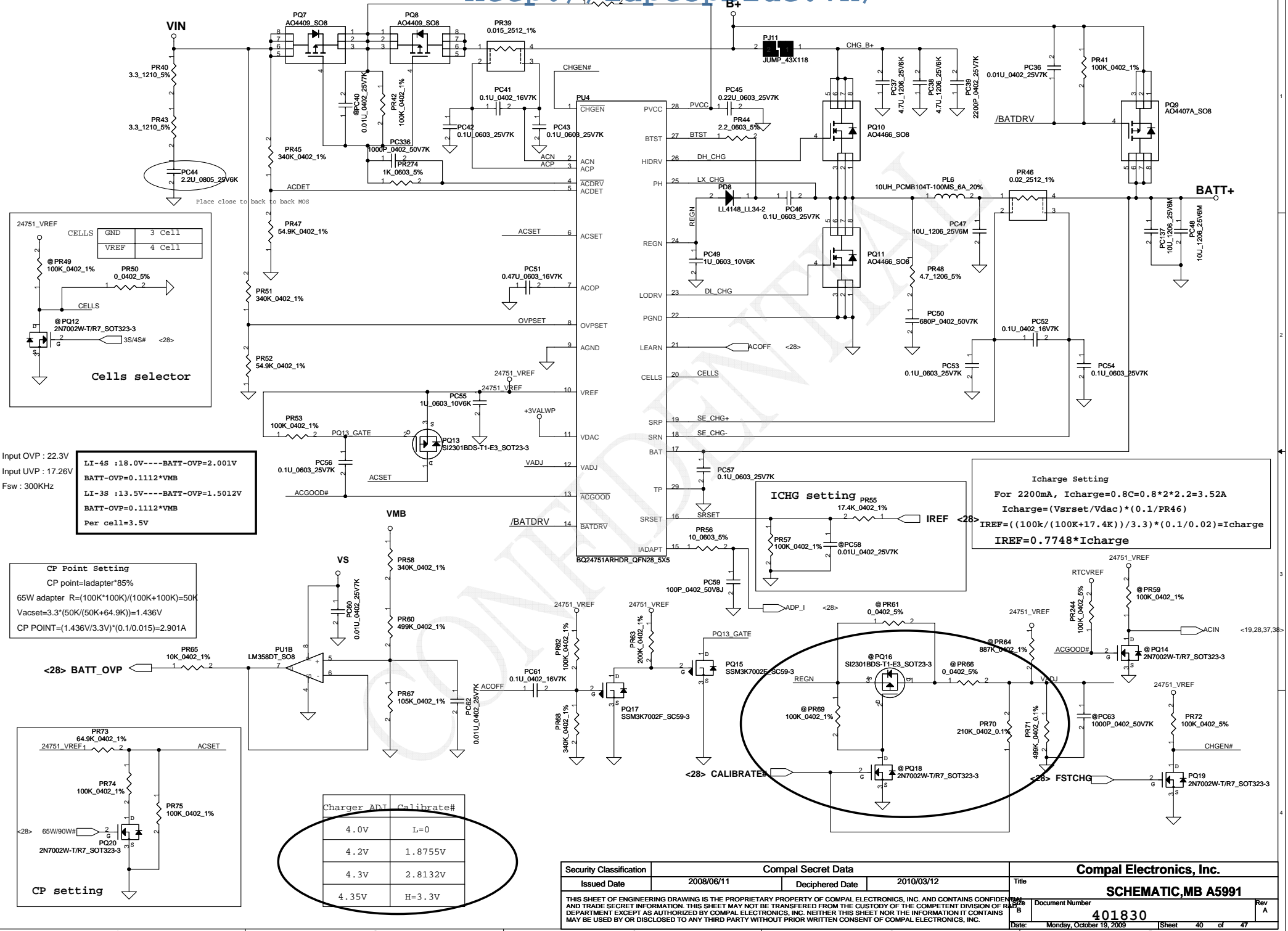


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

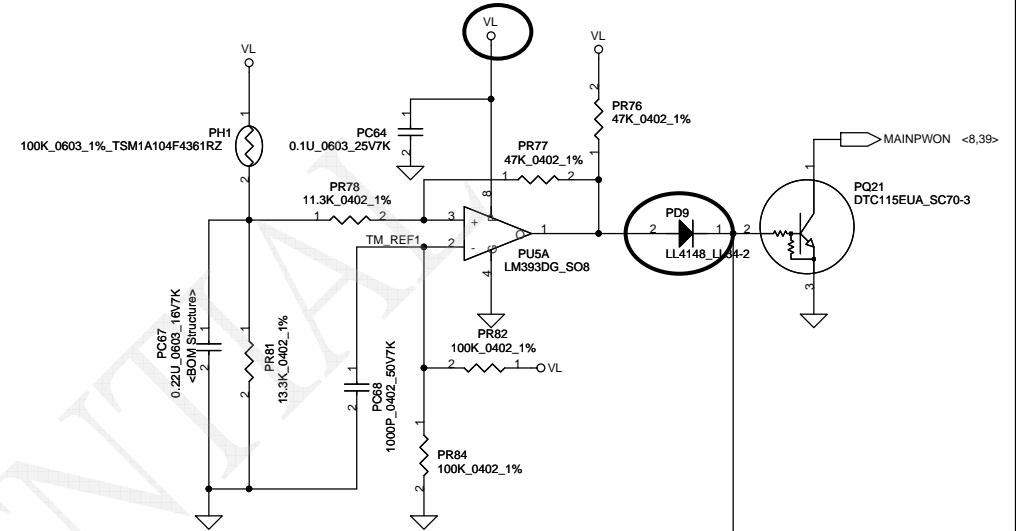




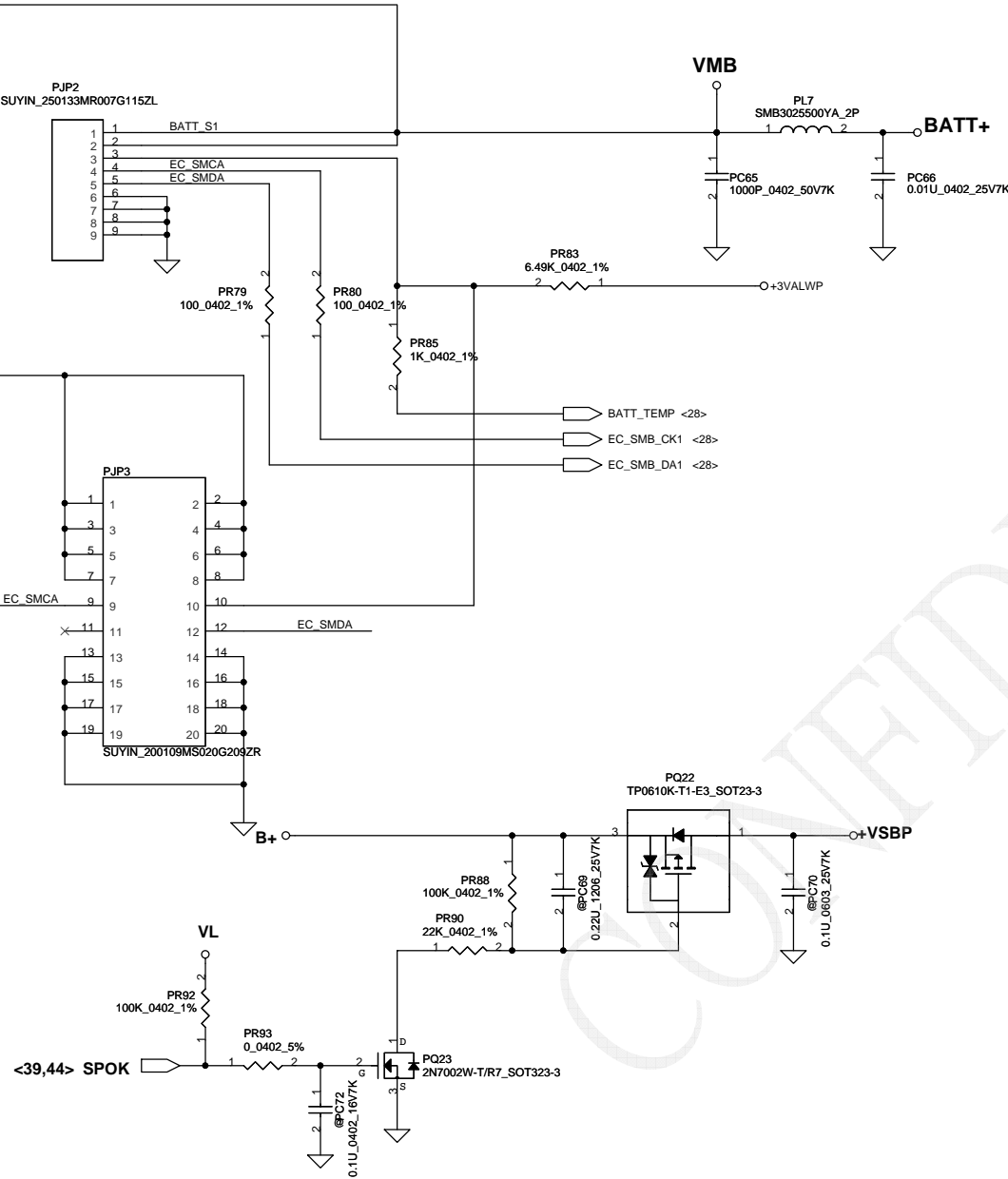
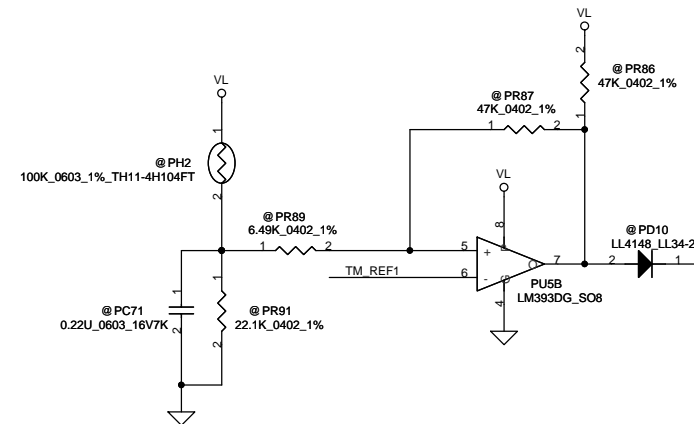
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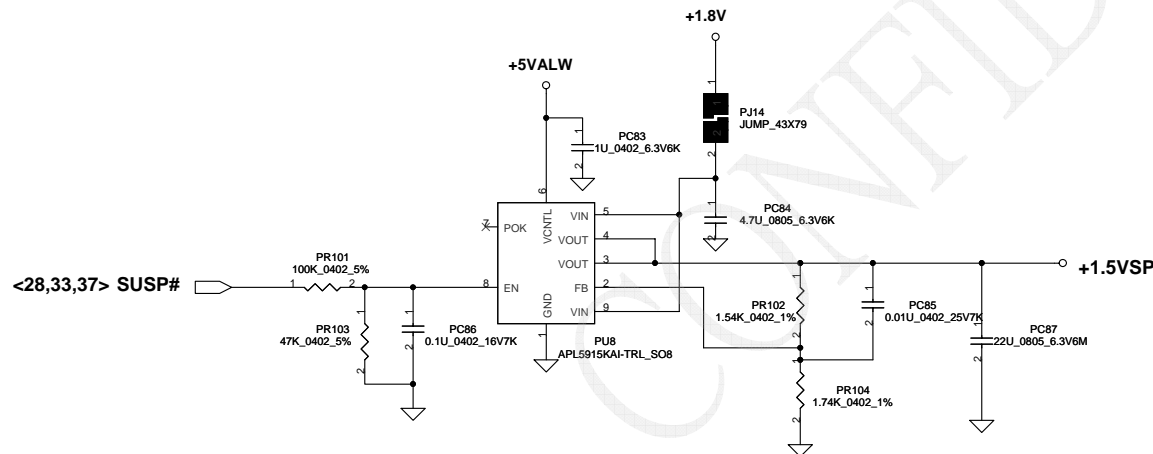
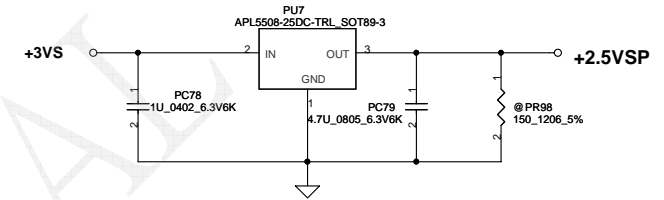
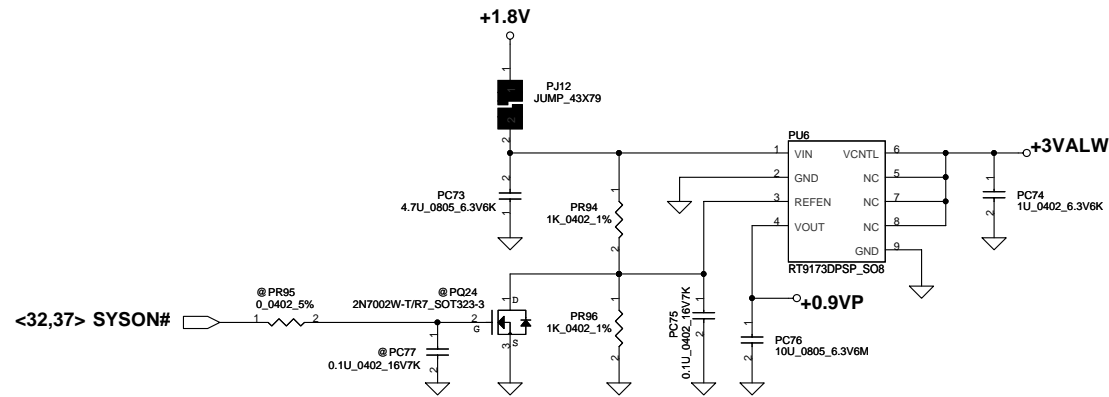
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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<28,37> SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

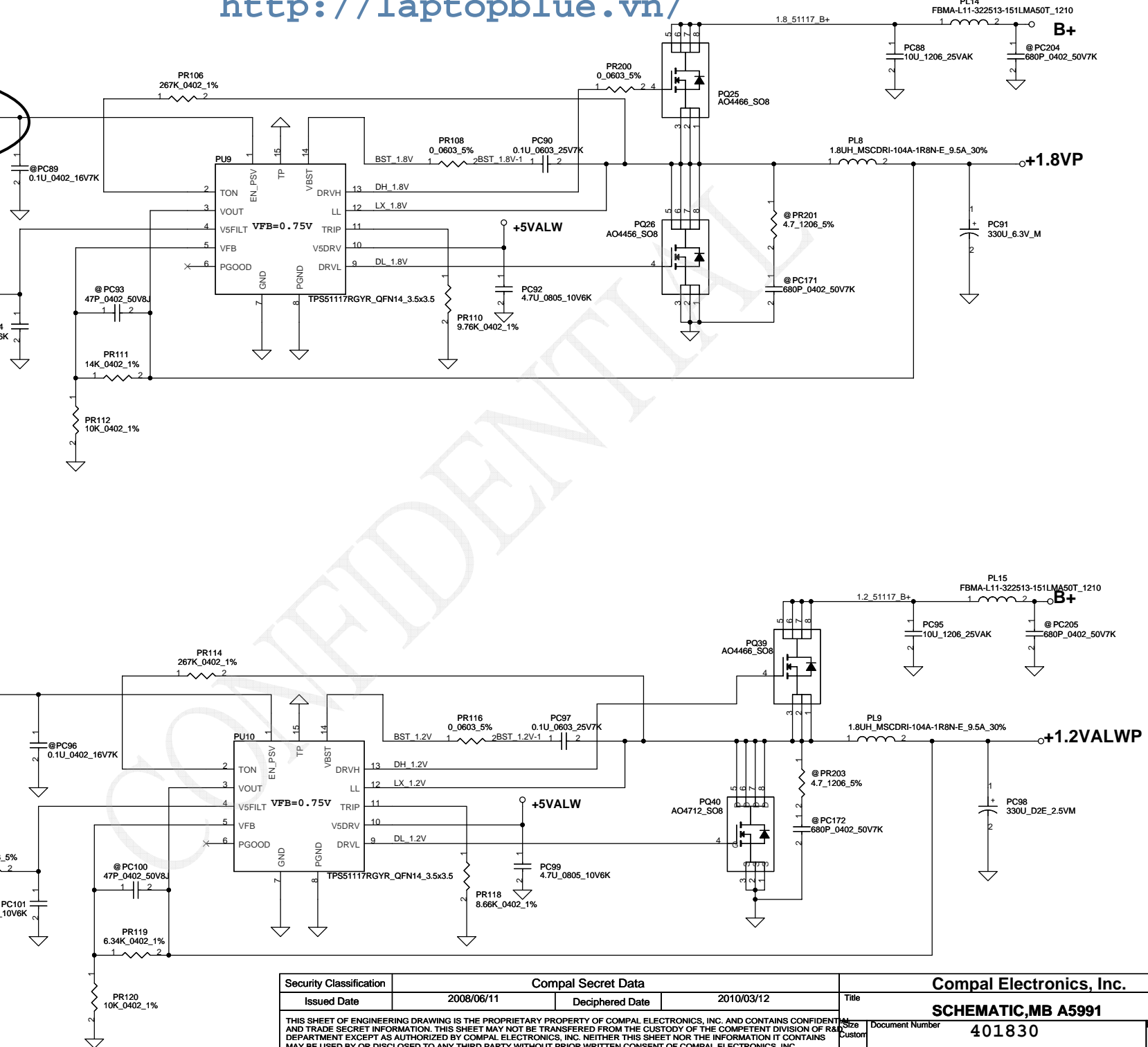
Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$

Rtrip=9.76K
 $I_{ocp} = 15.20A - 24.71A$

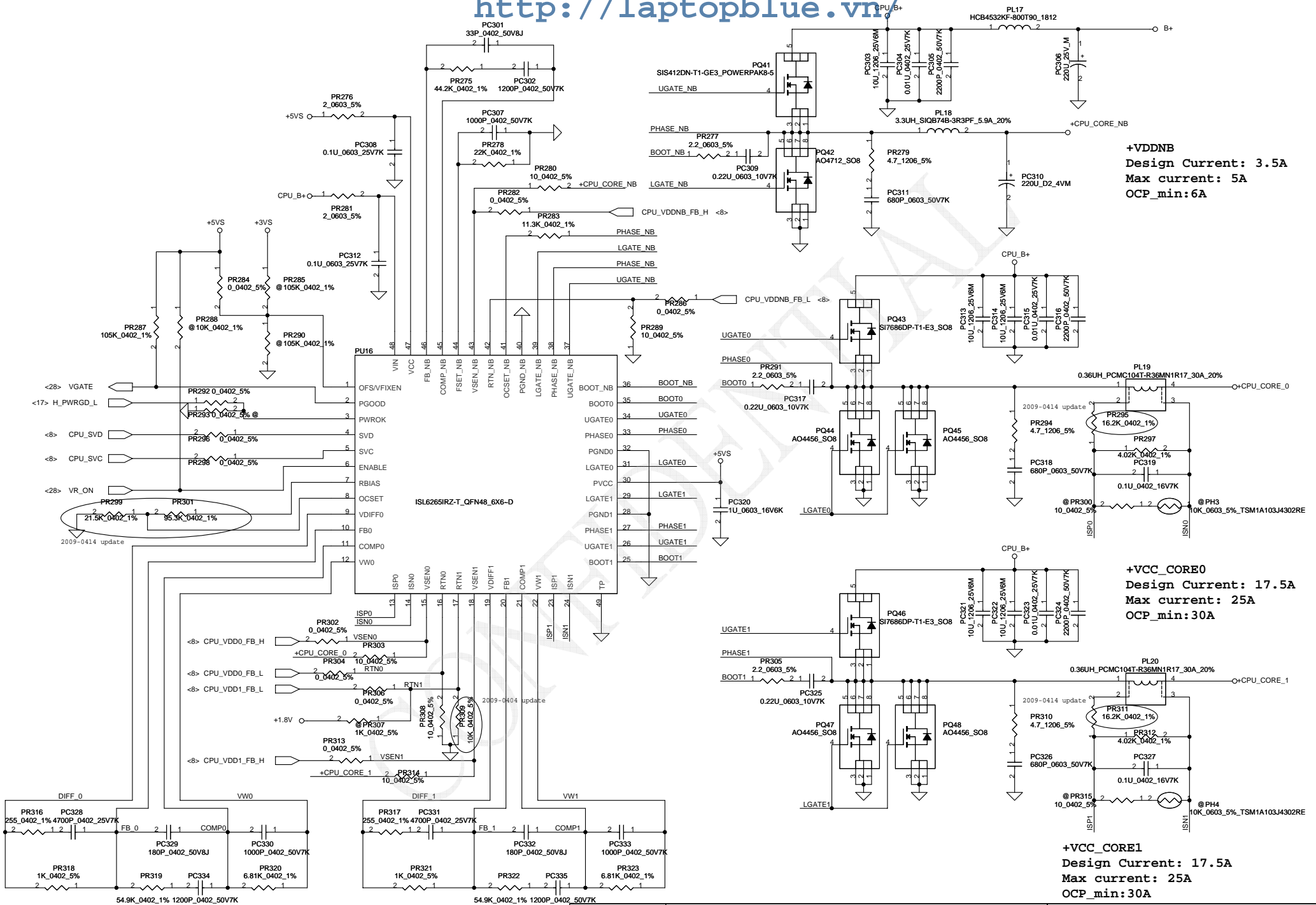
<39,41> SPOK

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A$; $I_{max} = 5.180A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m \text{ ohm}$
 $\Delta I_{set} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$



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