

Compal Confidential

KAWE0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-07-28

REV:1.0

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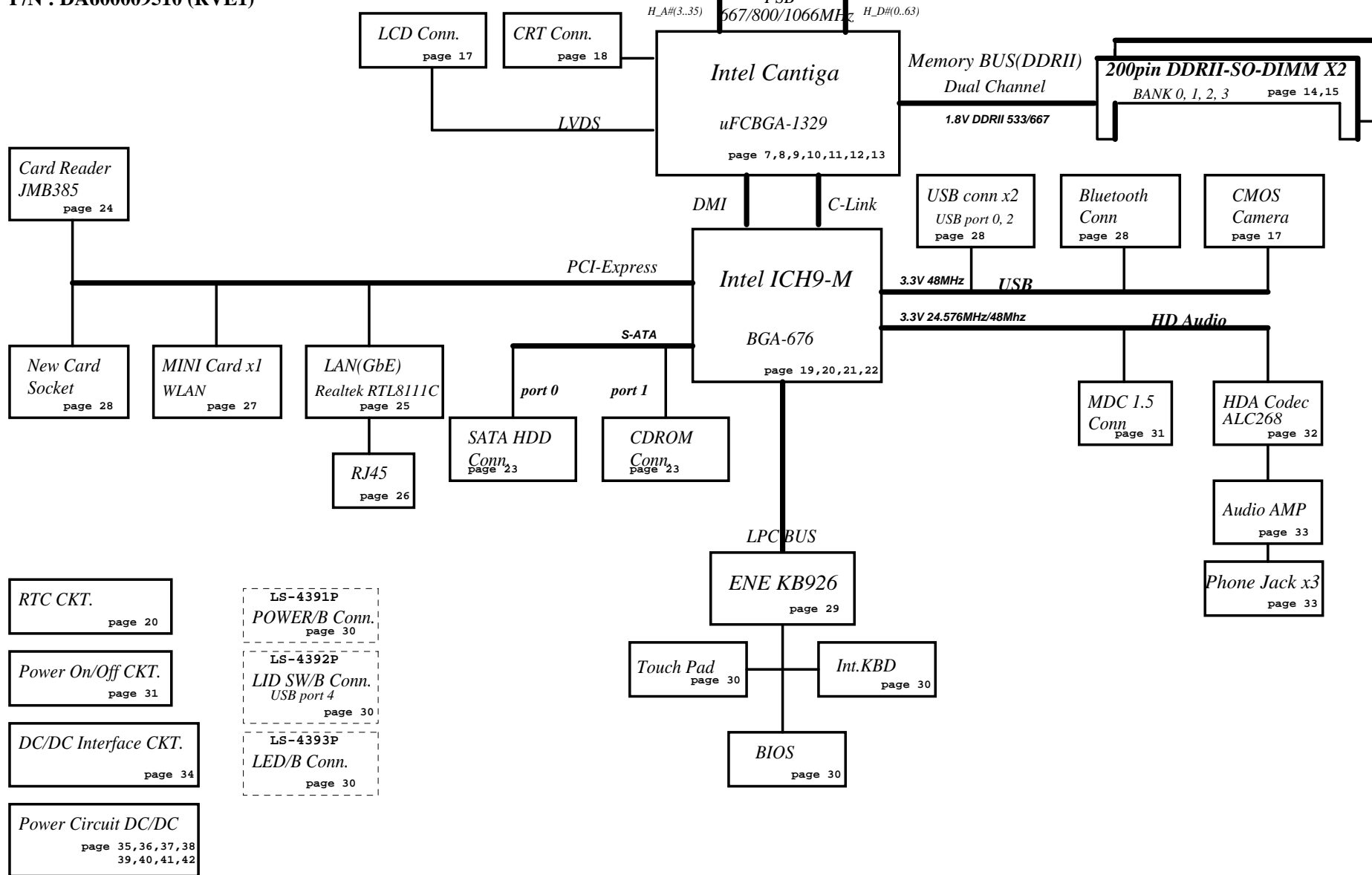
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Model Name : KAWE0

File Name : LA-4431P

P/N : DA600009500 (RVE0)

P/N : DA600009510 (RVE1)



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

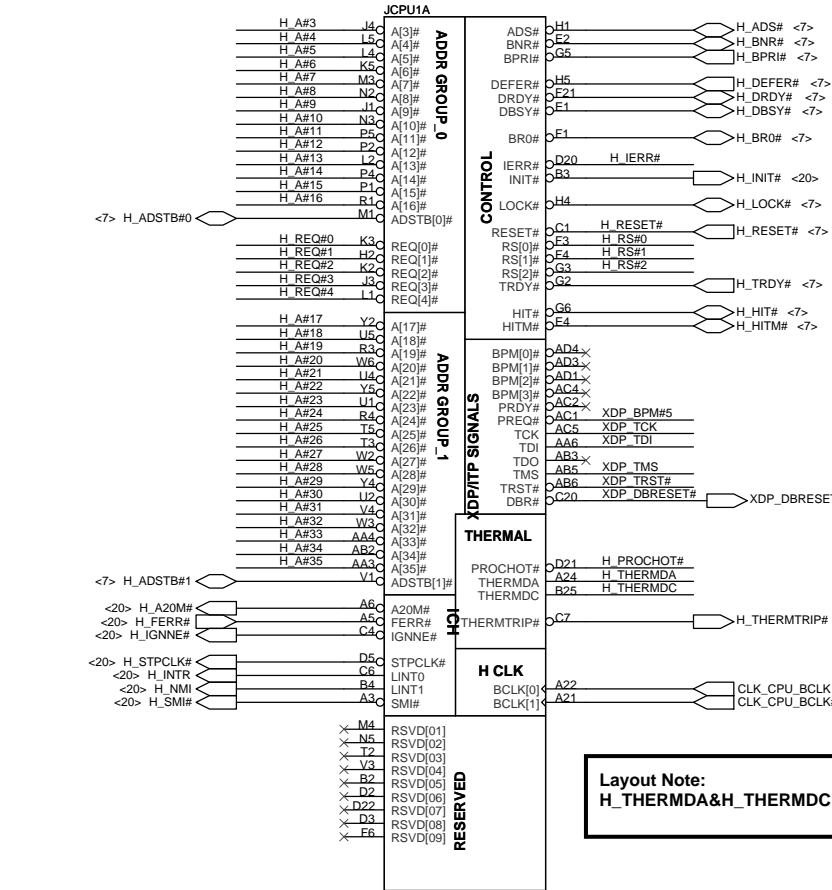
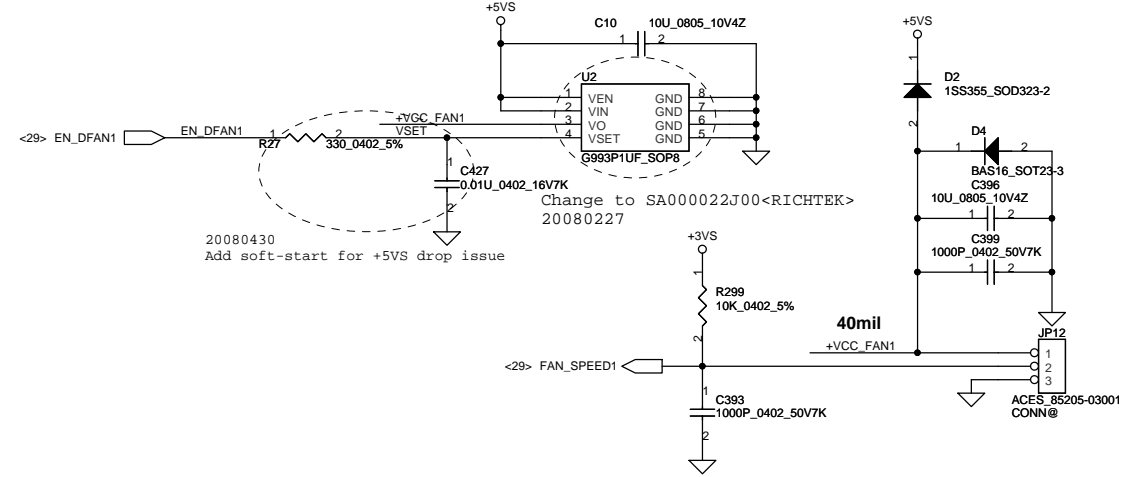
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

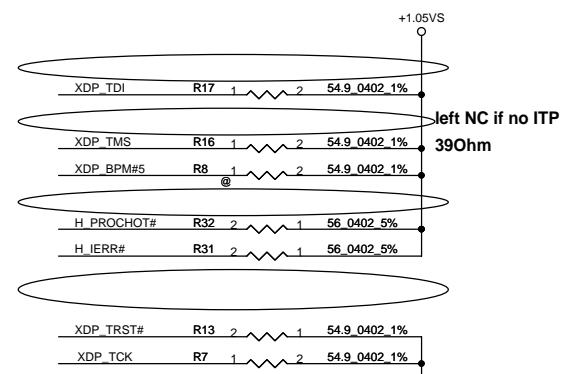
BTO Item	BOM Structure
8111C	8111C@
8102E	8102E@

<7> H_A# [3..35] H_A# [3..35]
 <7> H_REQ# [0..4] H_REQ# [0..4]
 <7> H_RS# [0..2] H_RS# [0..2]

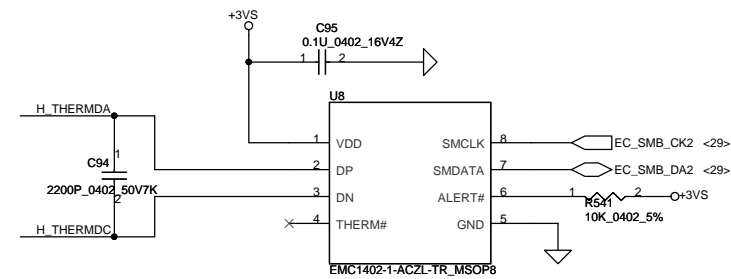
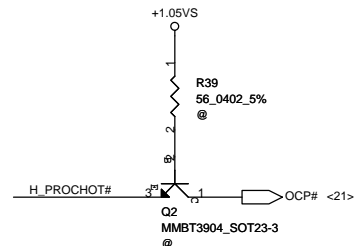
FAN1 Conn

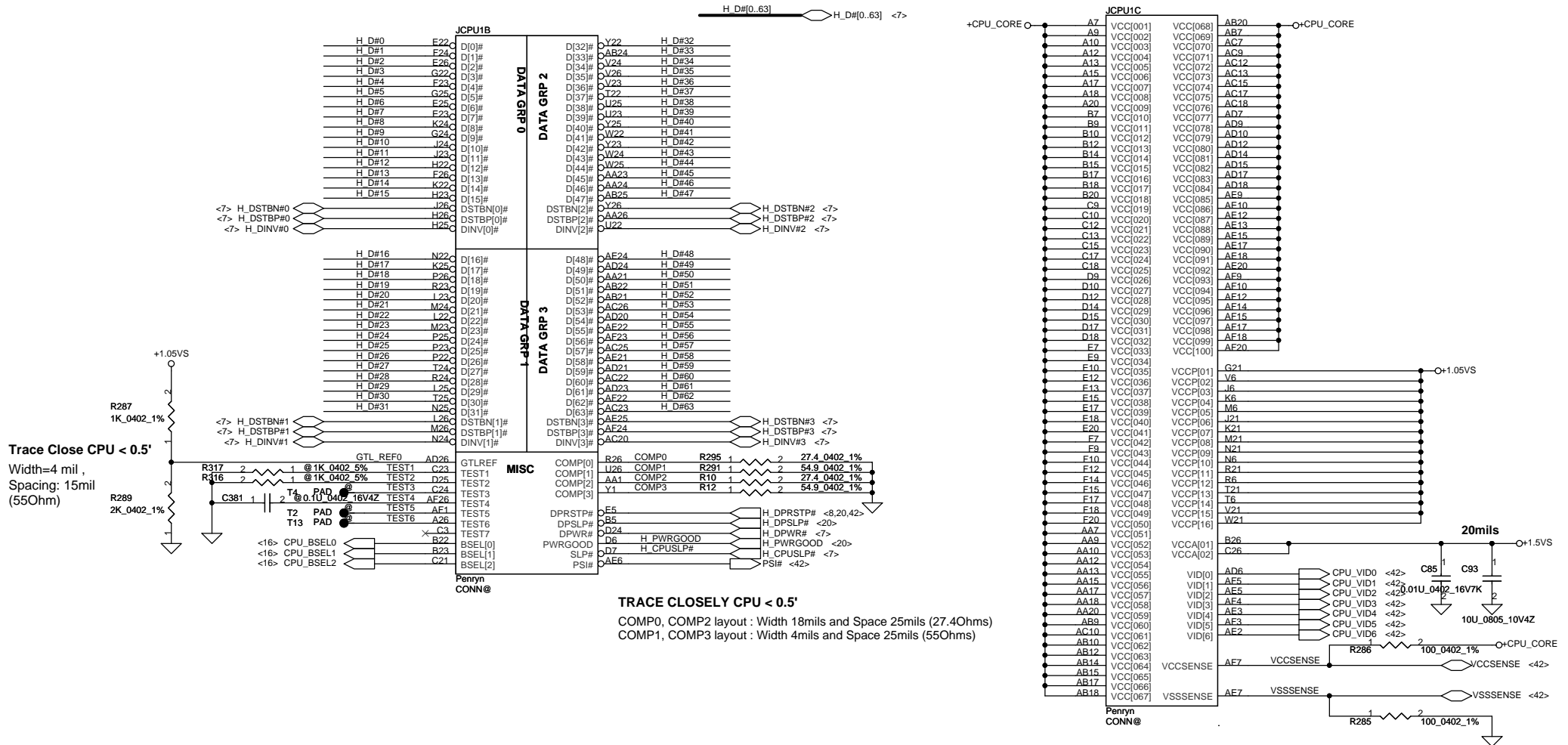


Layout Note:
 H_THERMDA & H_THERMDC Trace / Space = 10 / 10 mil

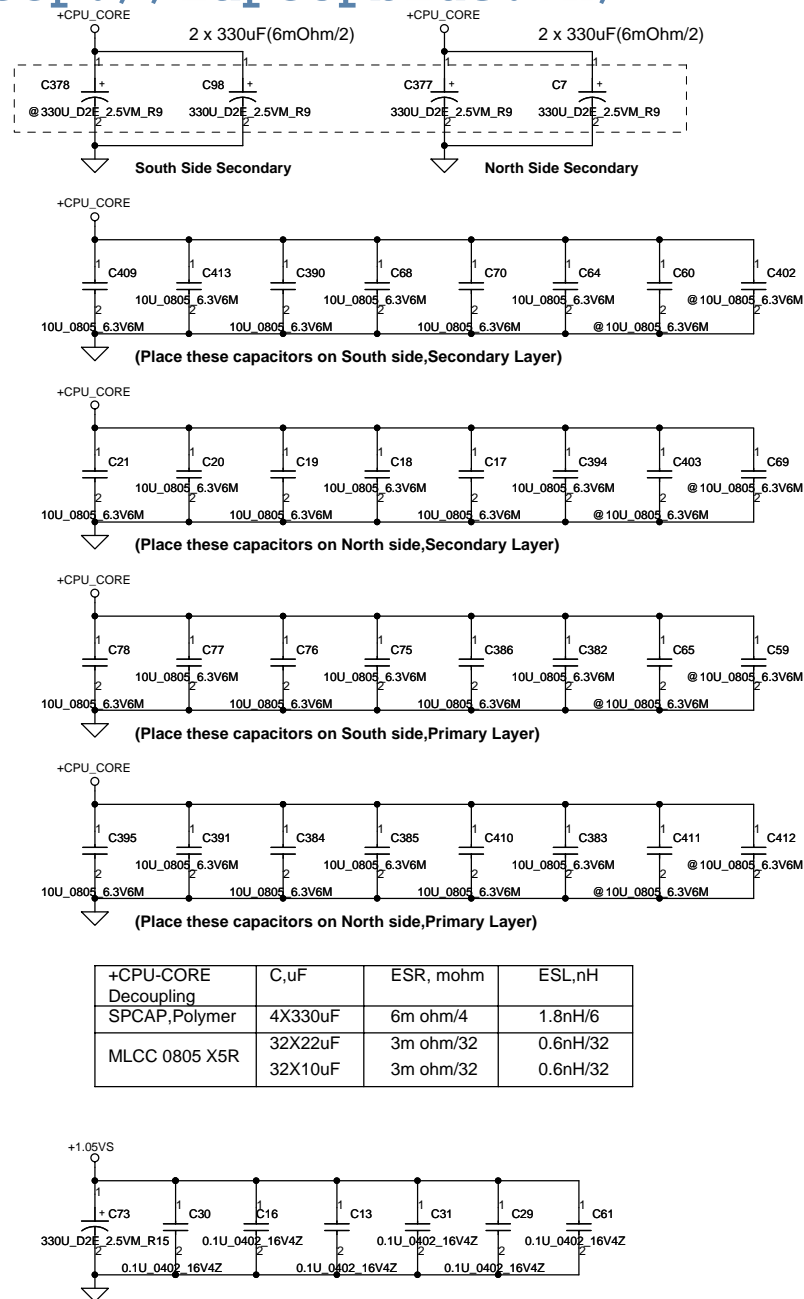
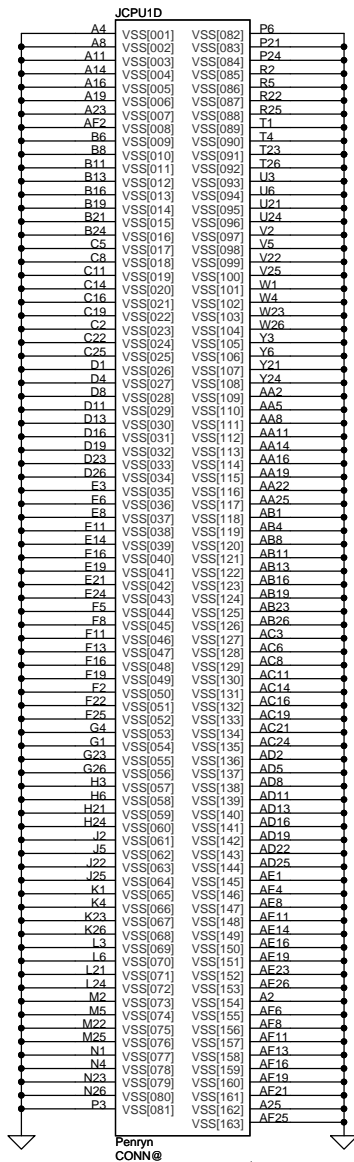


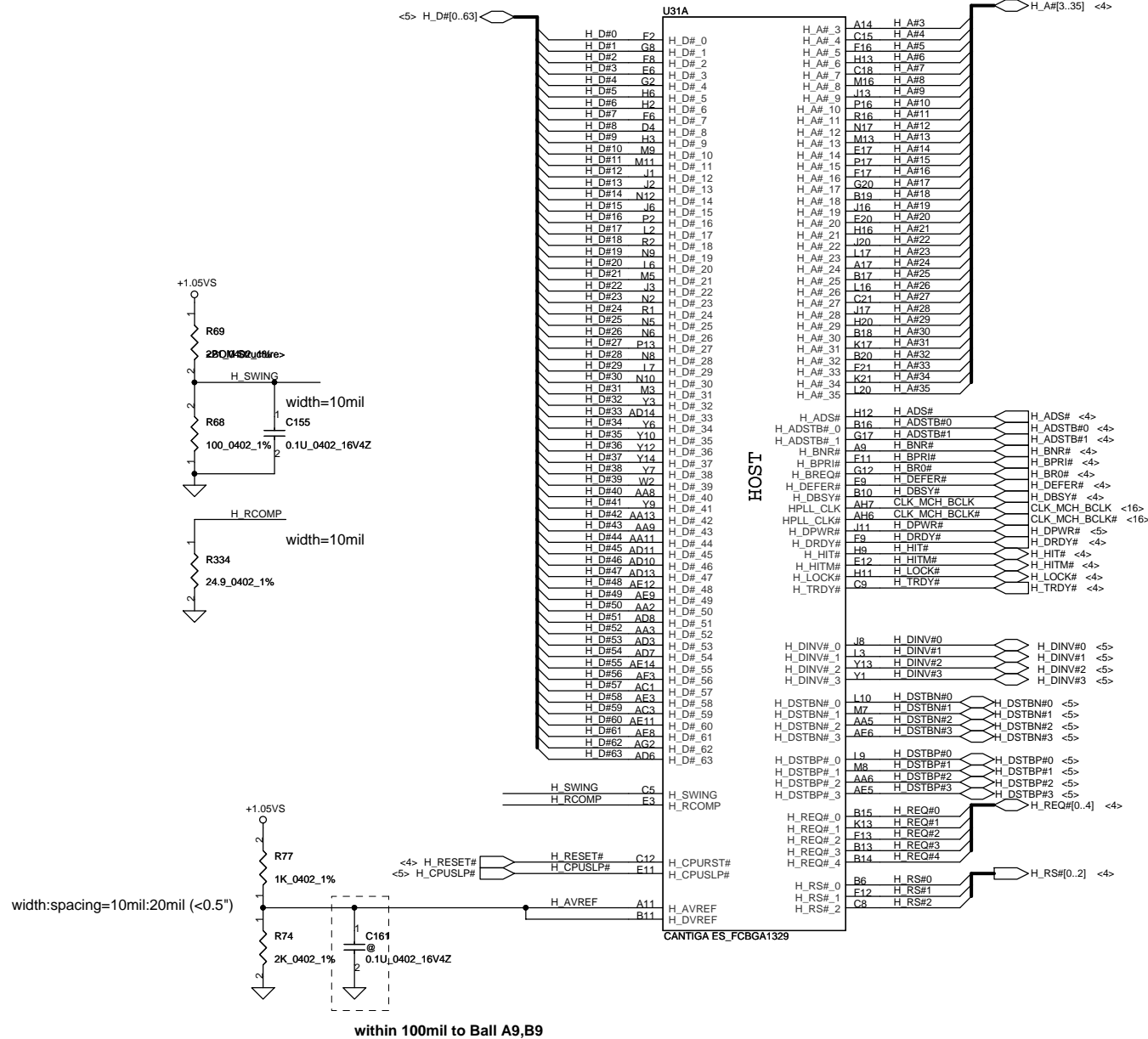
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



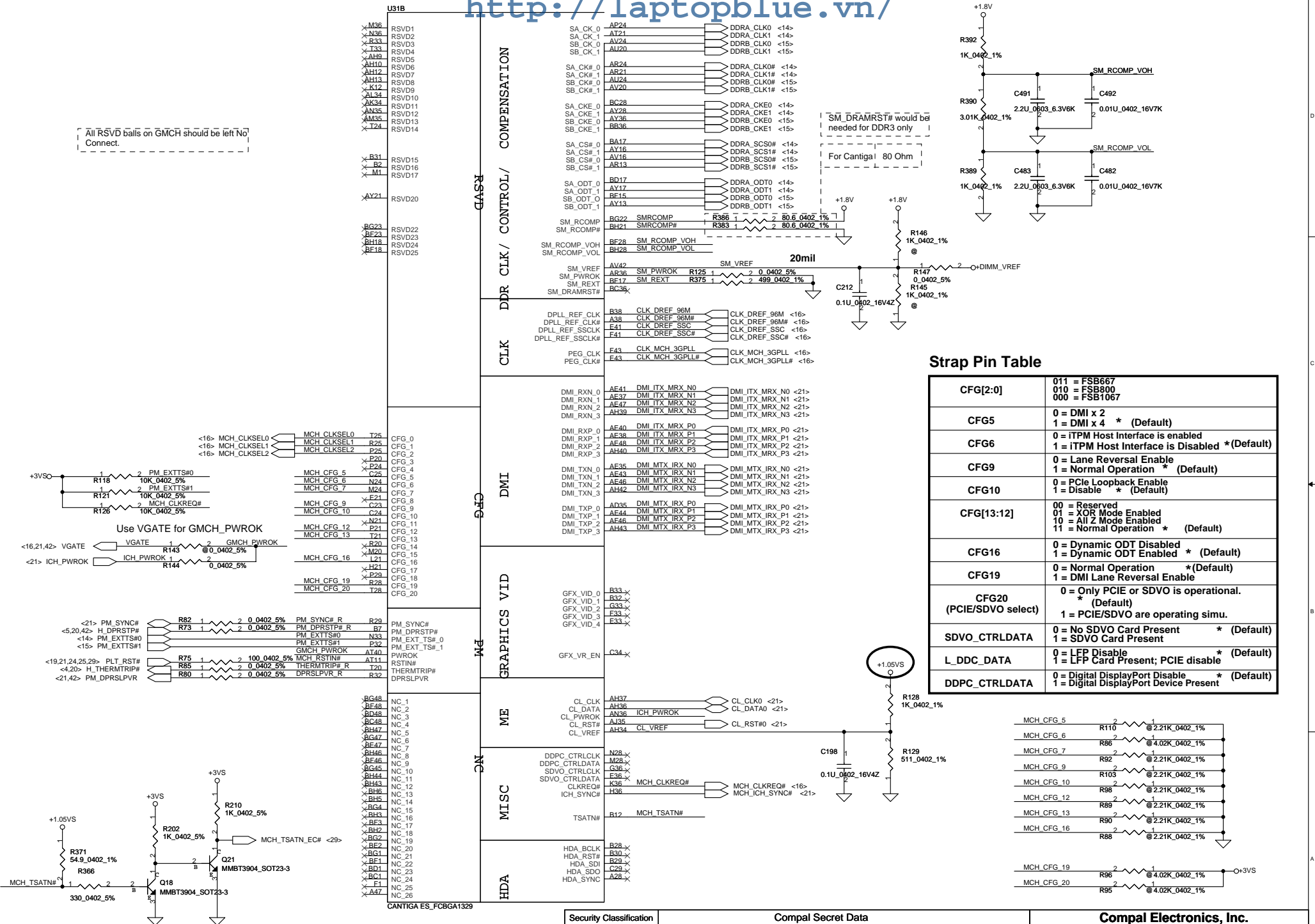


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Strap Pin Table	
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIe disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

MCH_CFG_5 R110 2.21K 0.402_1%

MCH_CFG_6 R86 4.02K 0.402_1%

MCH_CFG_7 R92 2.21K 0.402_1%

MCH_CFG_9 R103 2.21K 0.402_1%

MCH_CFG_10 R89 2.21K 0.402_1%

MCH_CFG_12 R98 2.21K 0.402_1%

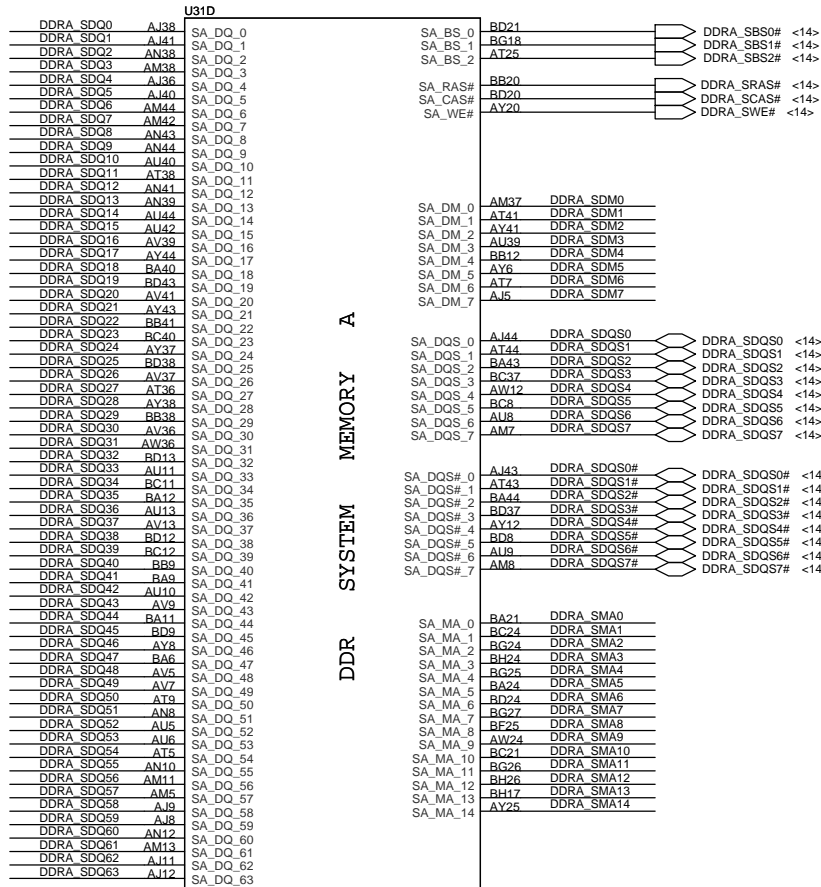
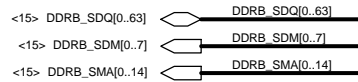
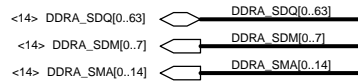
MCH_CFG_13 R90 2.21K 0.402_1%

MCH_CFG_16 R88 2.21K 0.402_1%

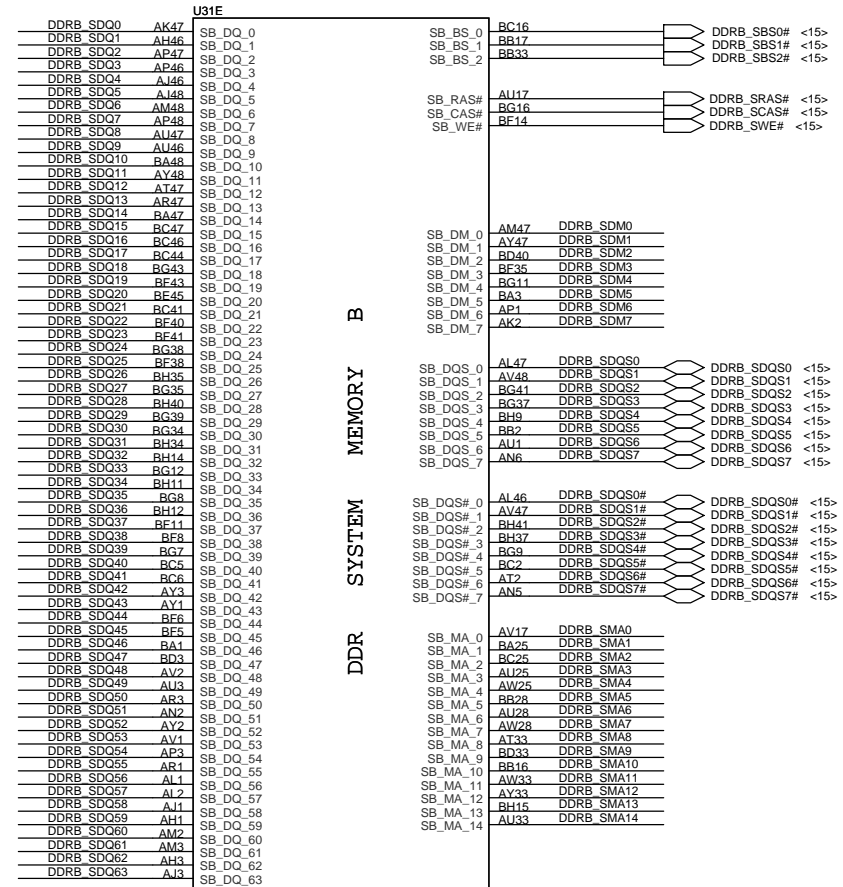
MCH_CFG_19 R96 4.02K 0.402_1%

MCH_CFG_20 2.21K 0.402_1%

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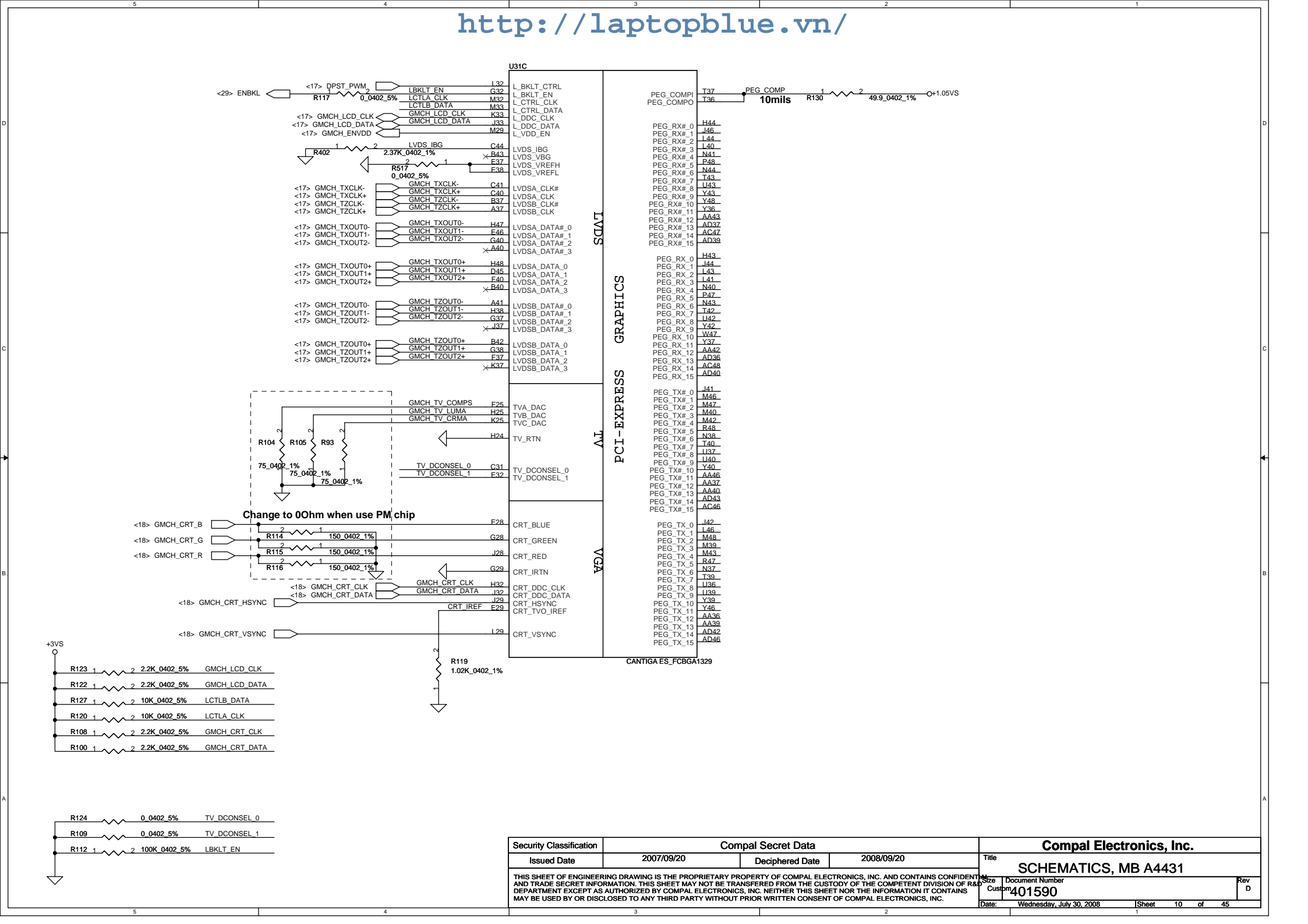


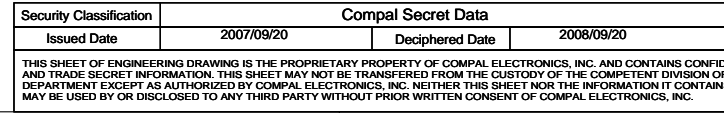
CANTIGA ES_FCBGA1329

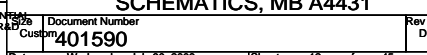


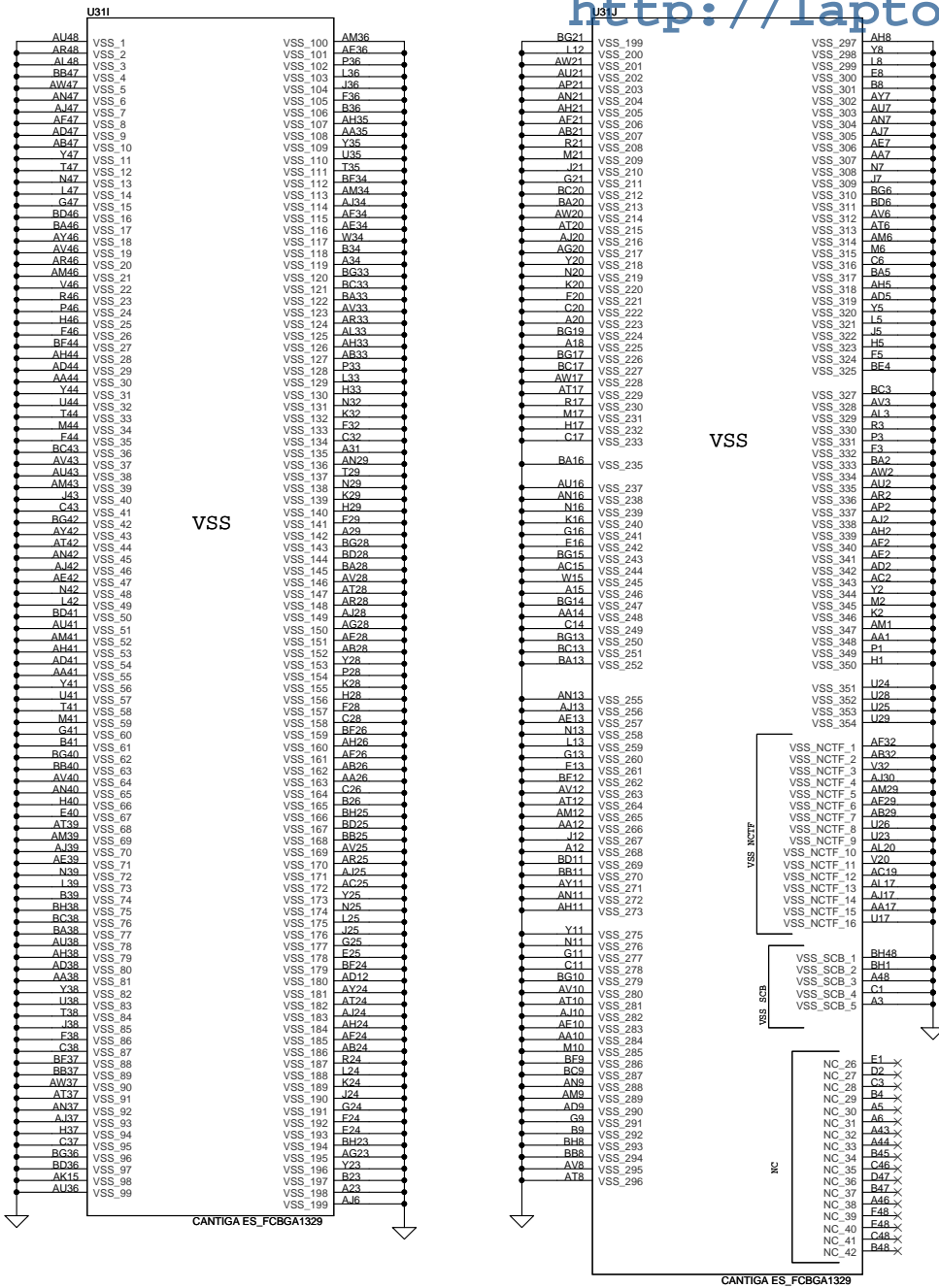
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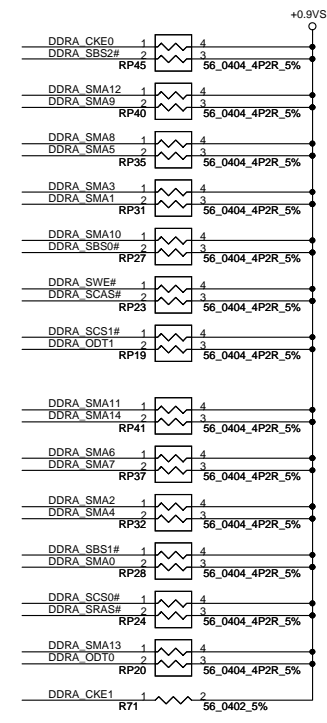
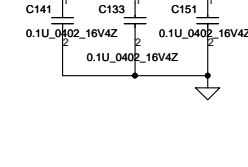
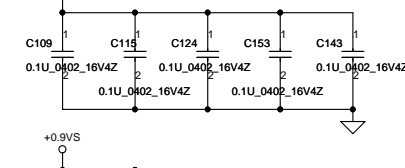
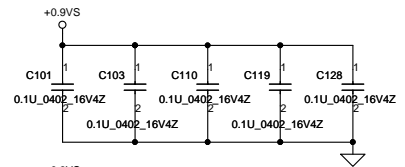
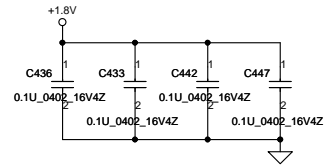
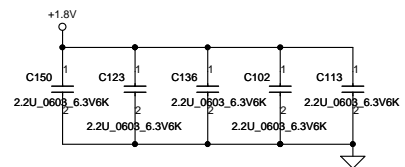
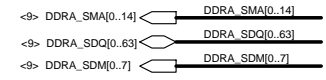
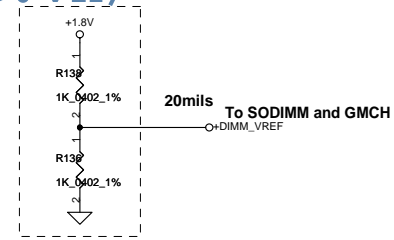
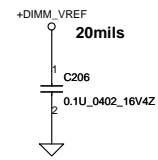
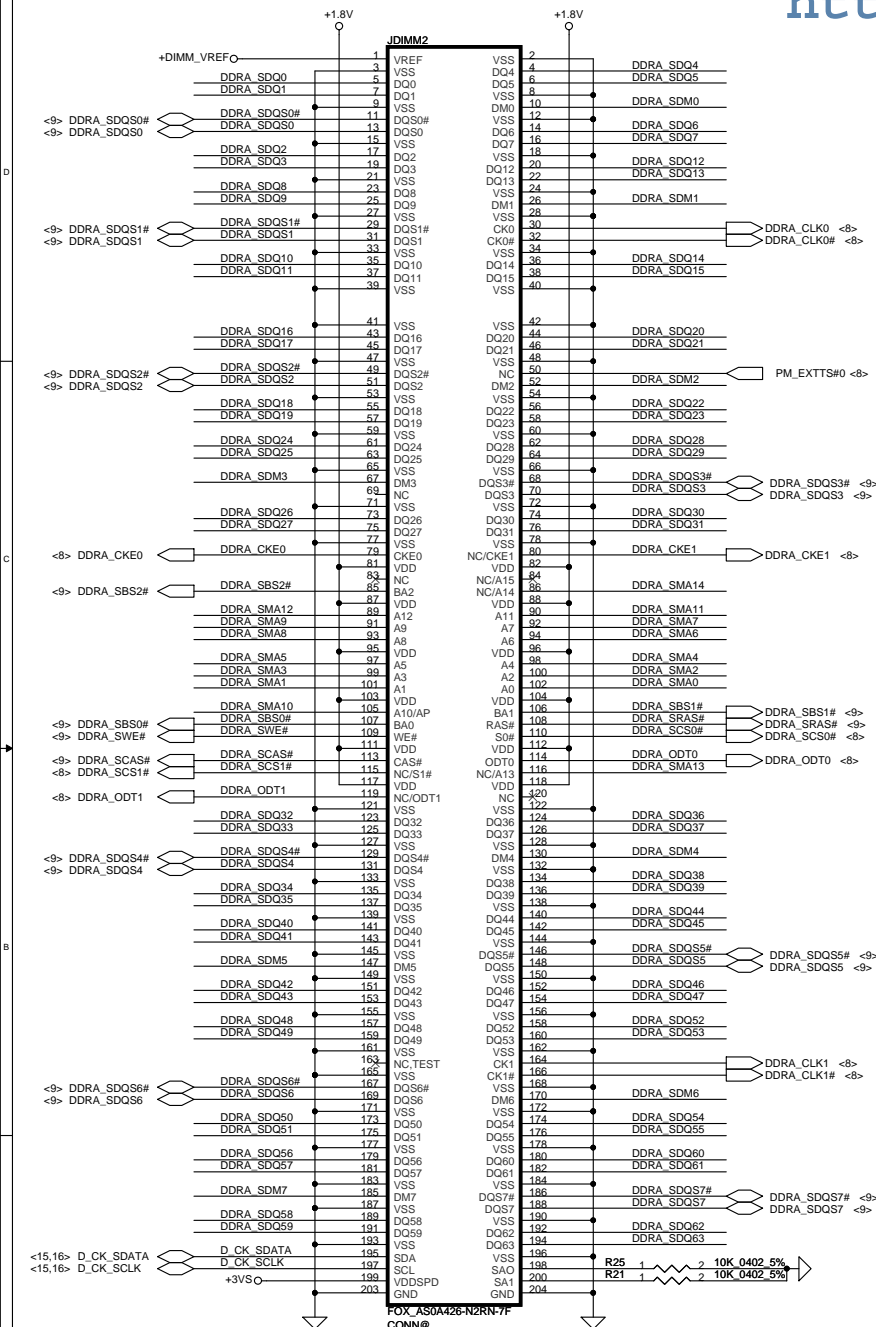
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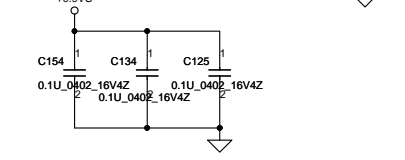
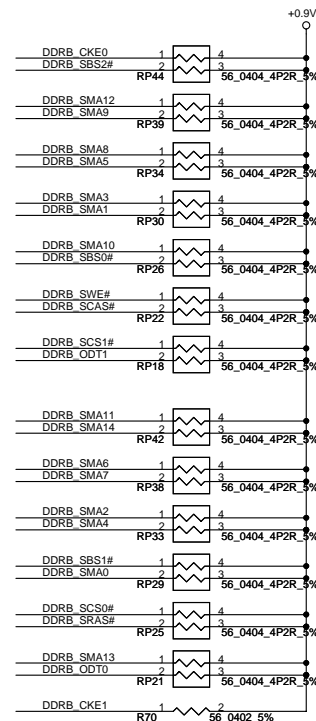
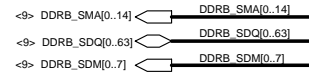
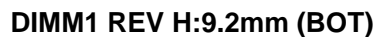






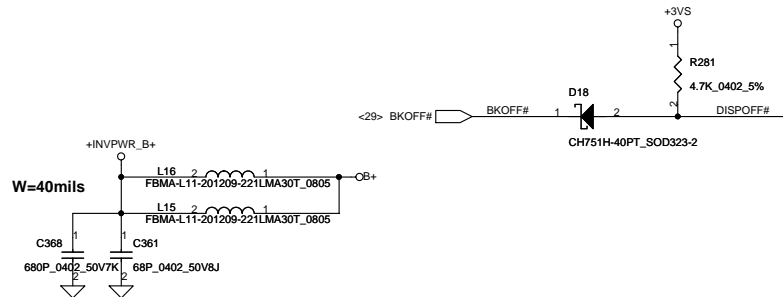
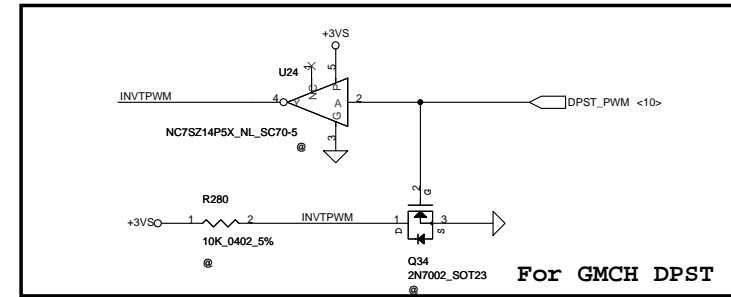
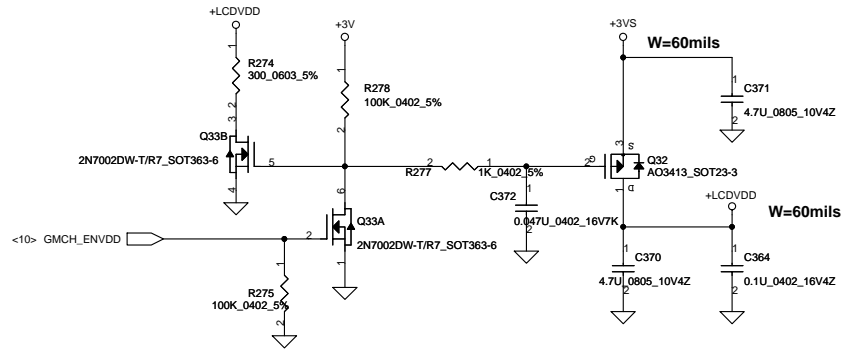
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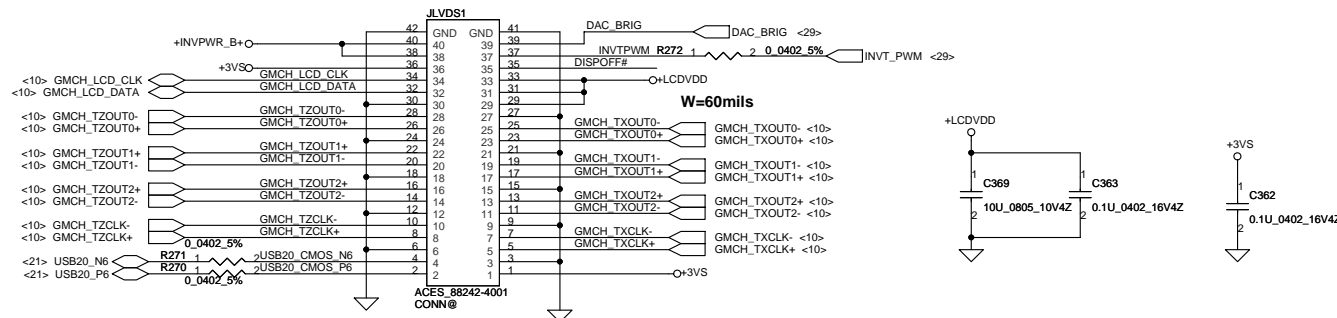


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LCD POWER CIRCUIT

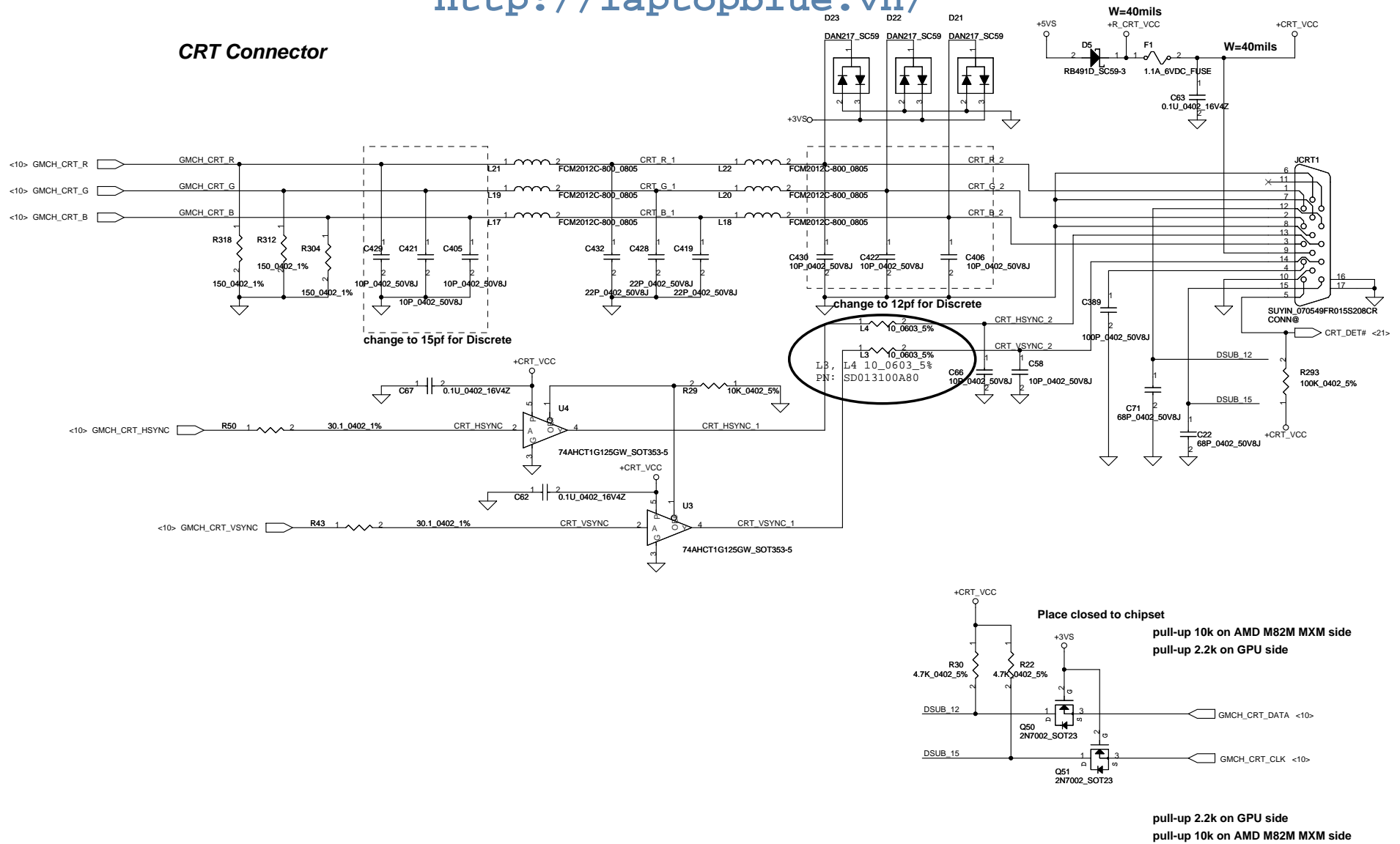


LCD/PANEL BD. Conn.

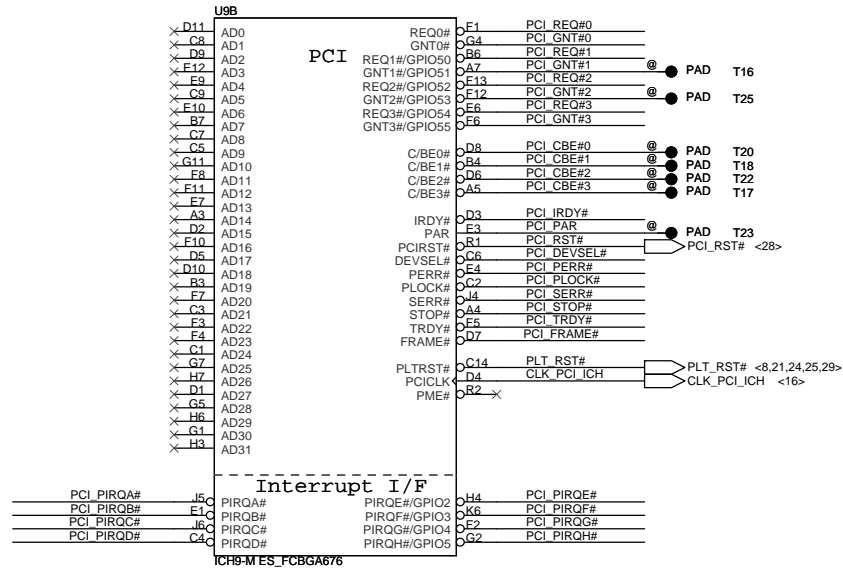
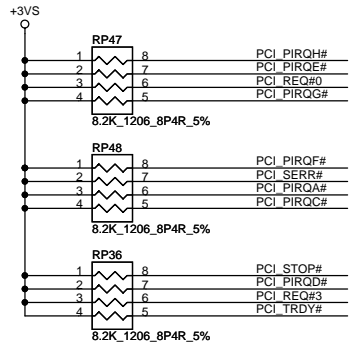
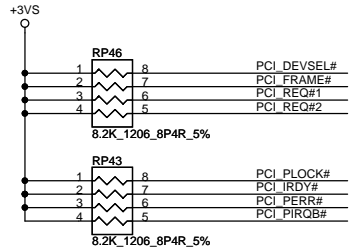


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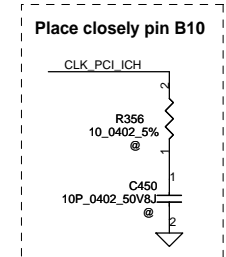
CRT Connector



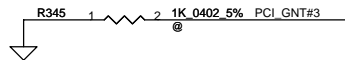
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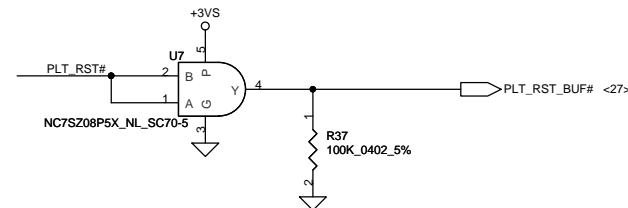
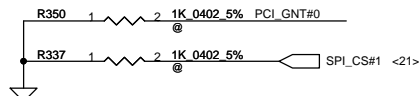
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



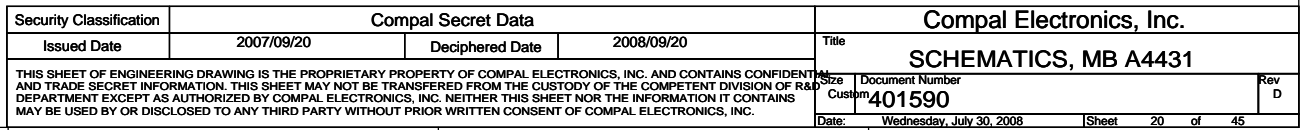
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

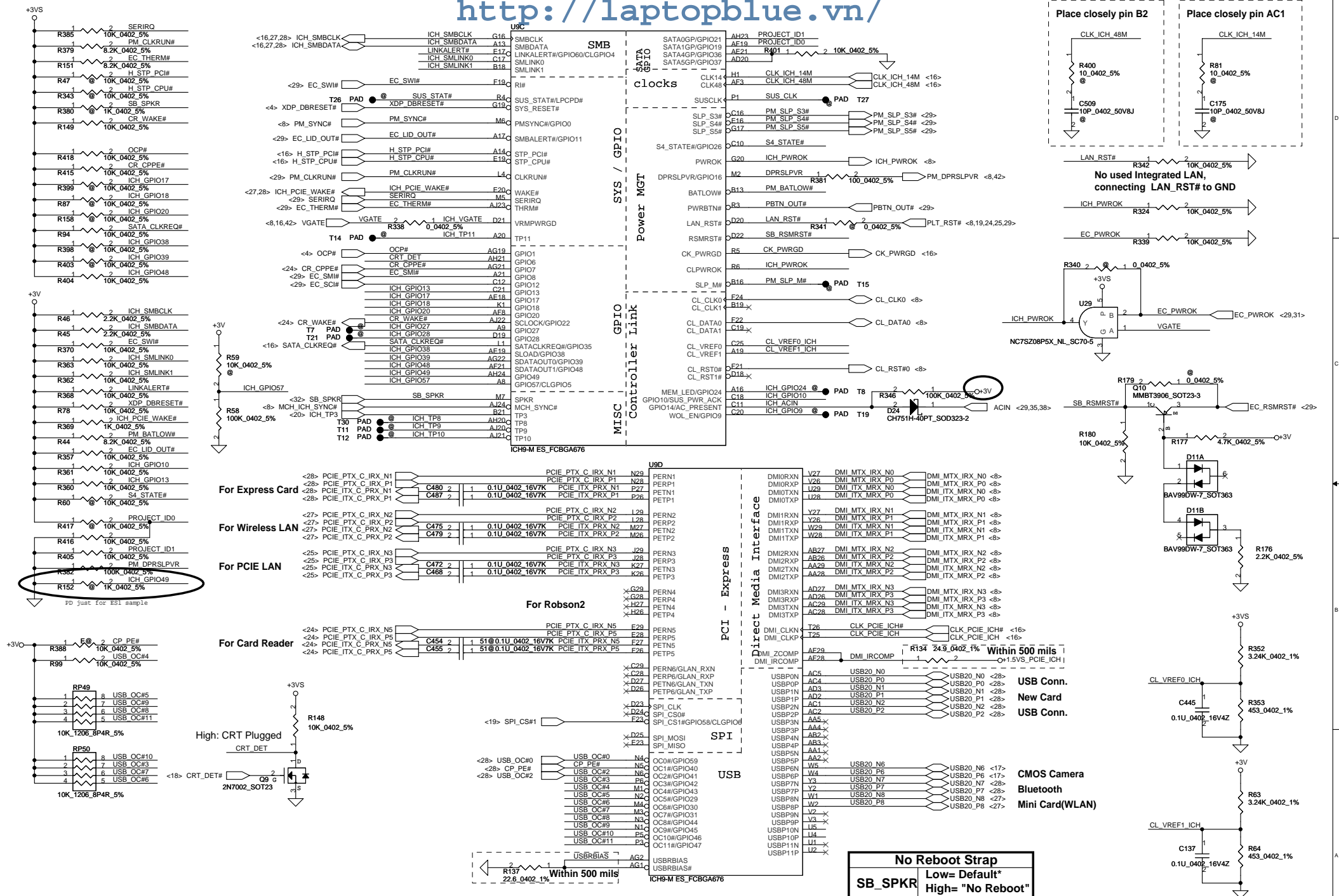


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

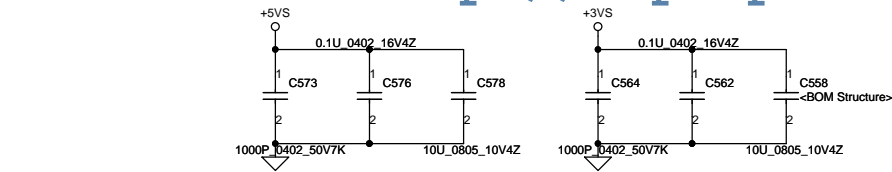


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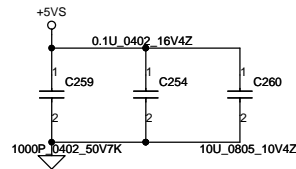
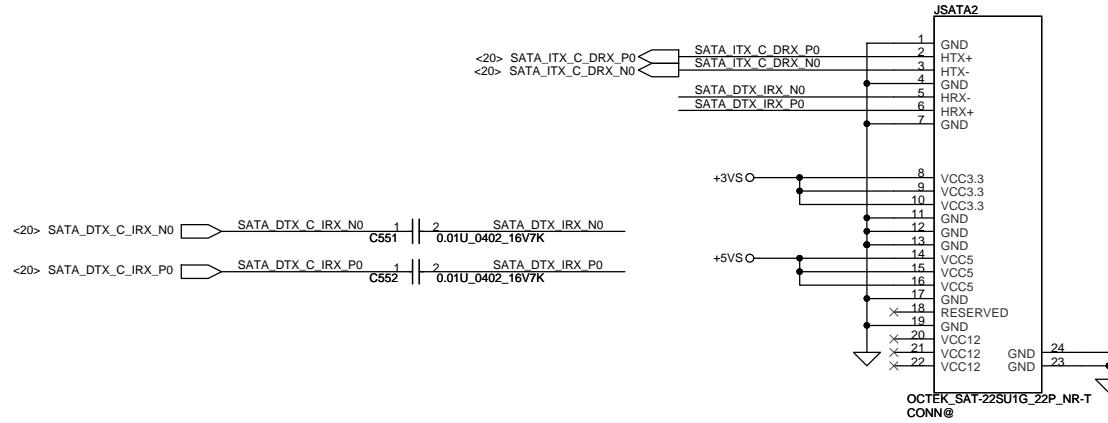




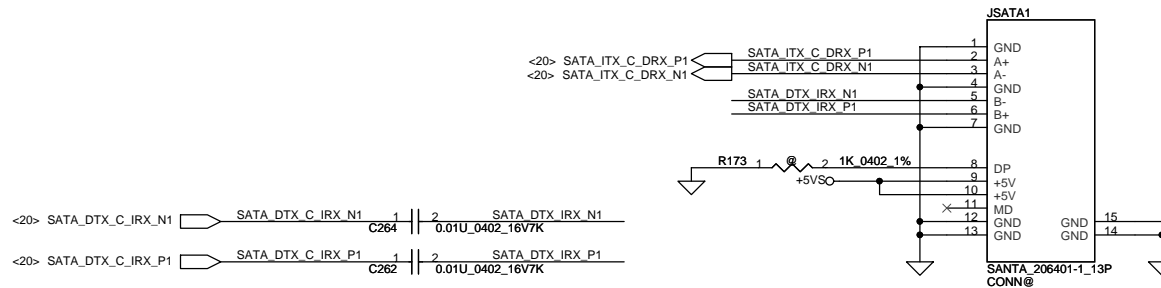
Internal TPM Strap		DMI Termination Voltage		Security Classification				Compal Secret Data				Compal Electronics, Inc.			
SPI_MOSI	Low= Disable*	GPIO49	Low= Desktop used	Issued Date	2007/09/20		Deciphered Date	2008/09/20		Title		SCHEMATICS, MB A4431			
	High= iTPM enable by MCH strap		High= Mobile* (Internal pull-up)		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.										
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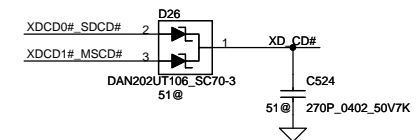
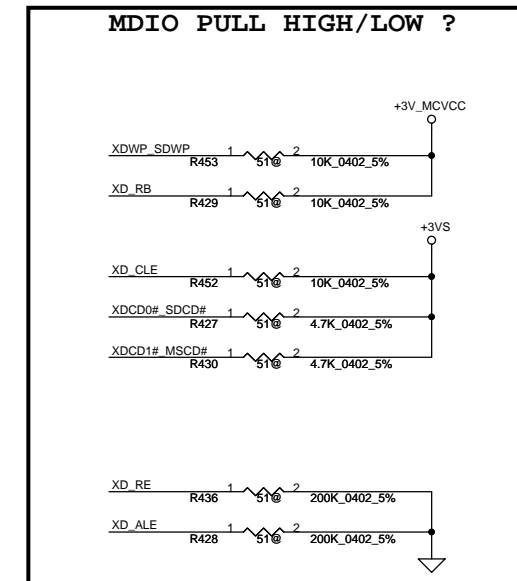
SATA HDD Conn.



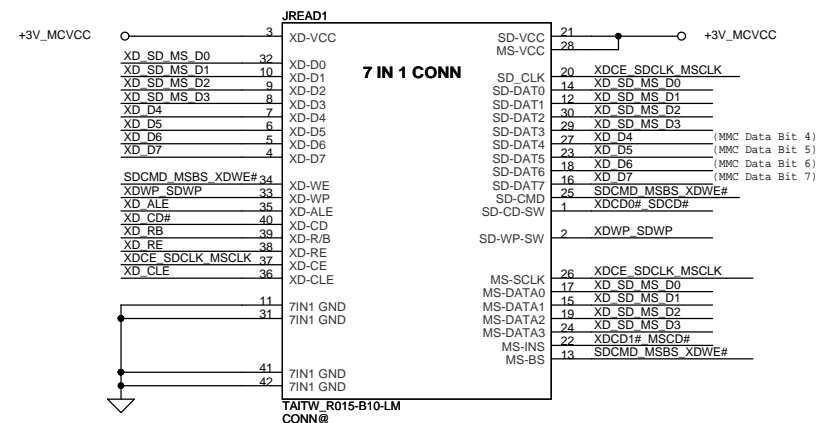
SATA ODD Conn.



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Memory Card Power Switch

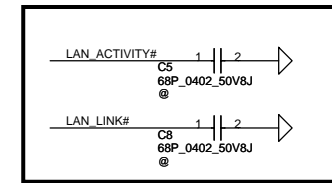
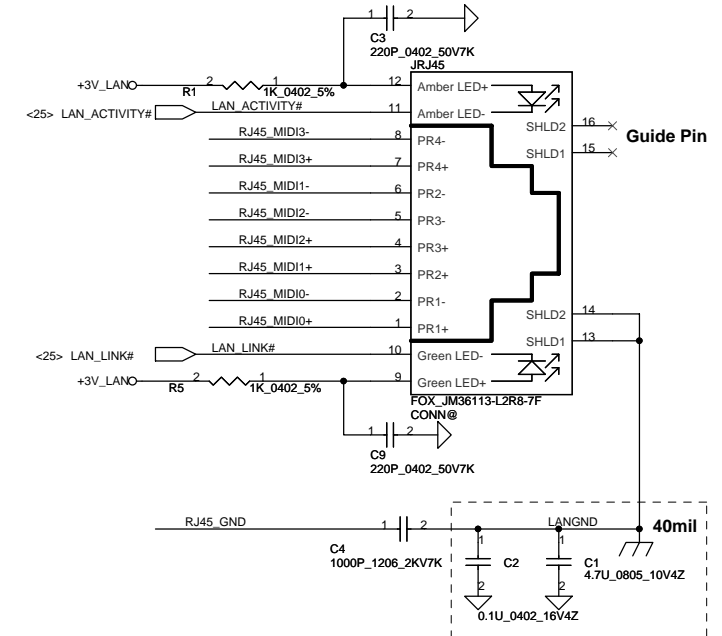
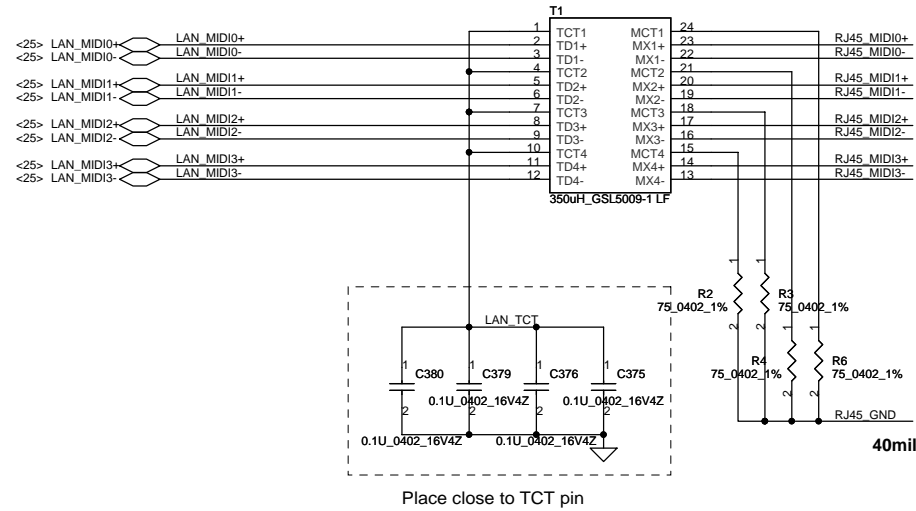


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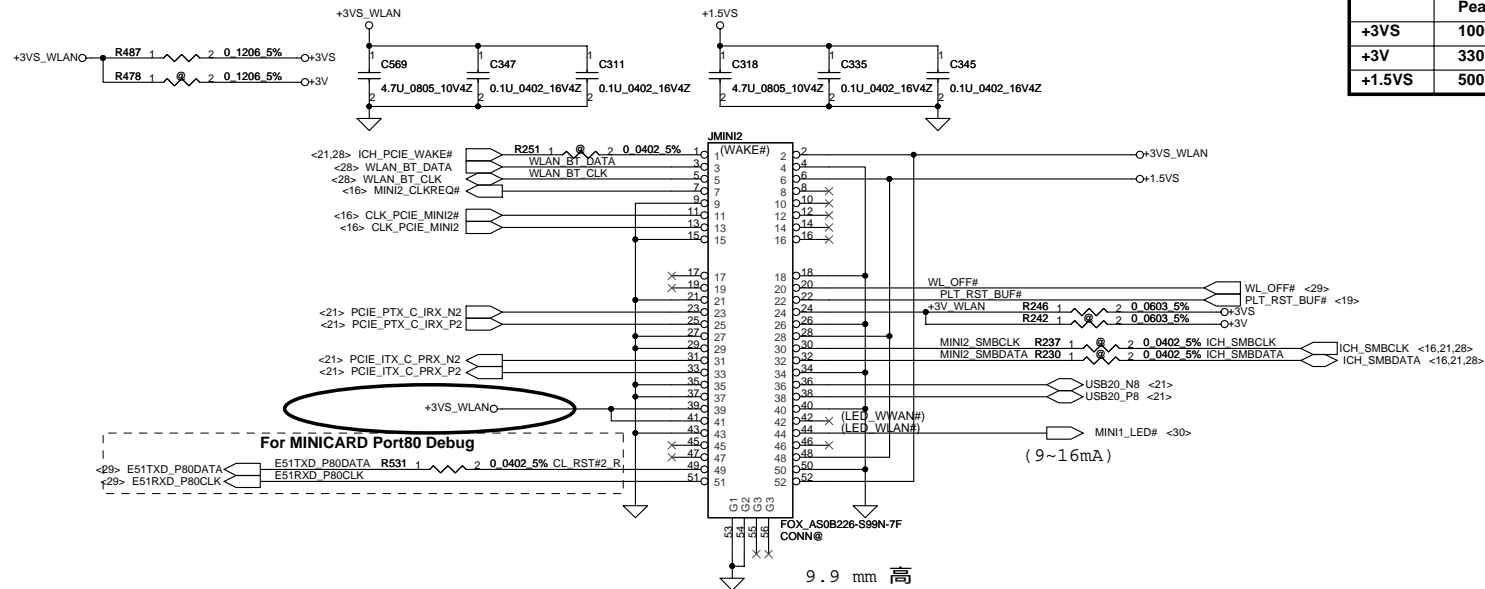
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LAN RTL8111C/8102E

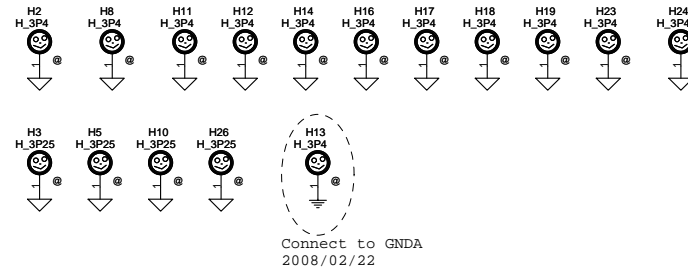
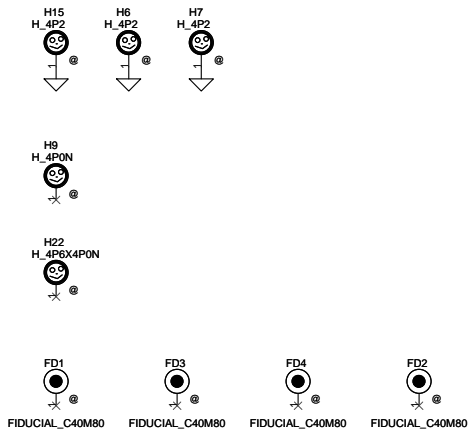


For EMI

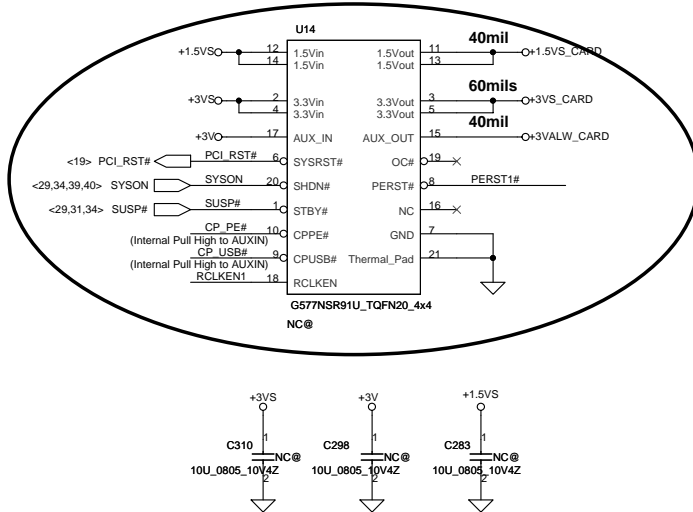
For Wireless LAN



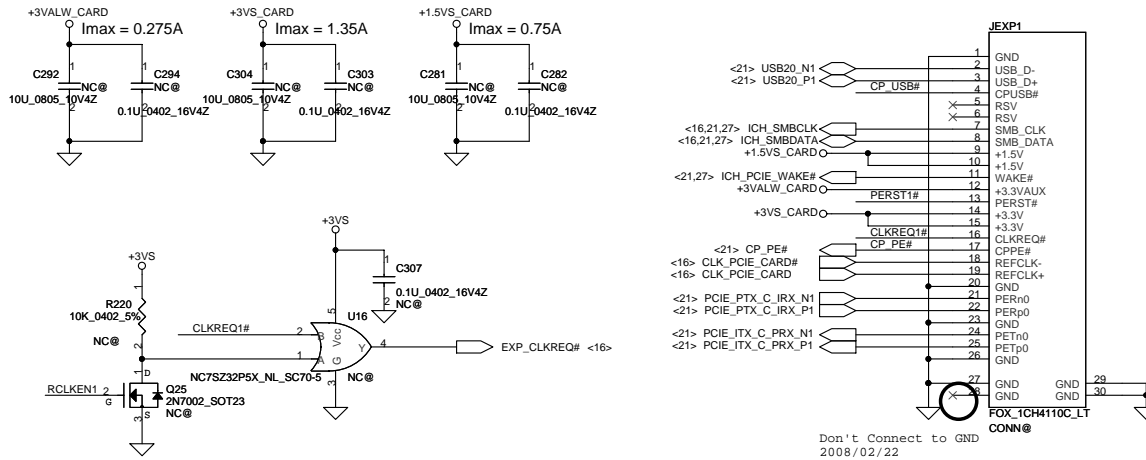
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



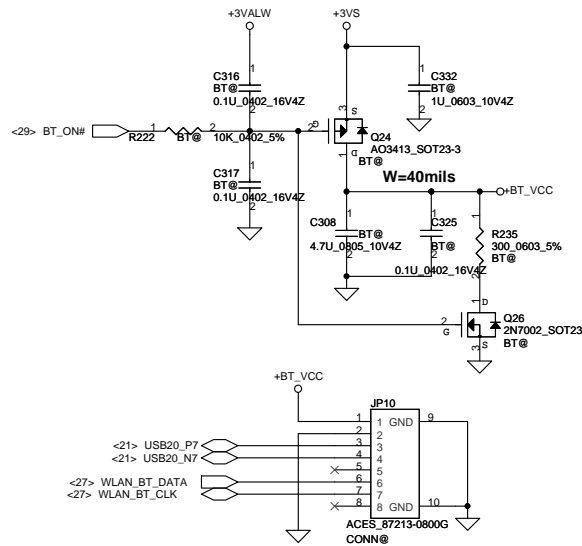
New Card Power Switch



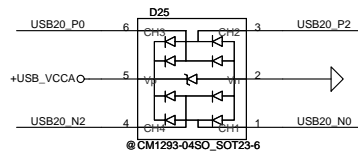
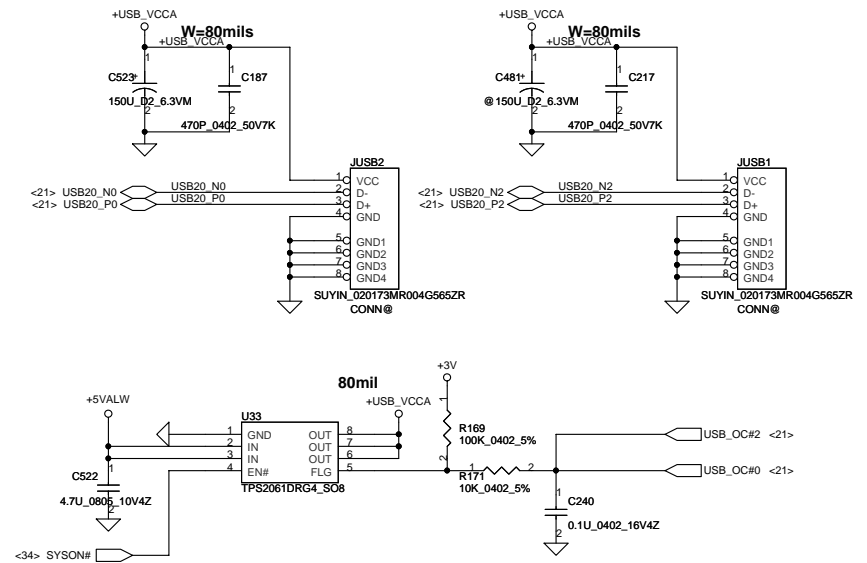
New Card Socket (Left/TOP)



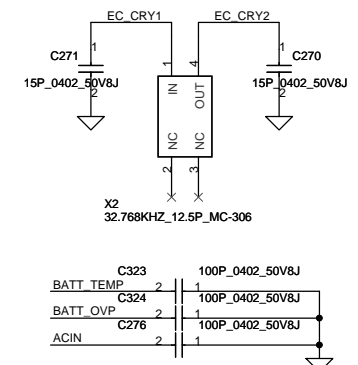
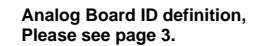
Bluetooth Conn.



USB CONN. (Stack-up Type)

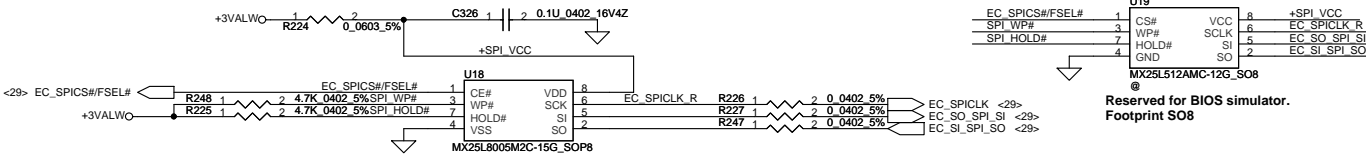


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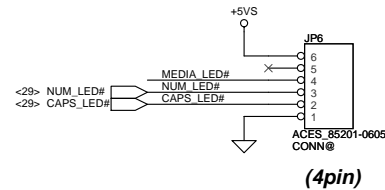
For KB926 C0 reversion

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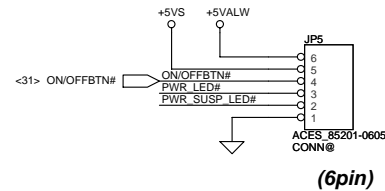


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

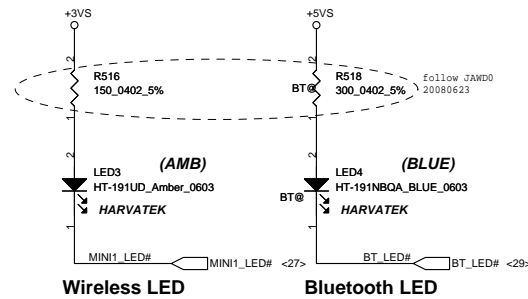
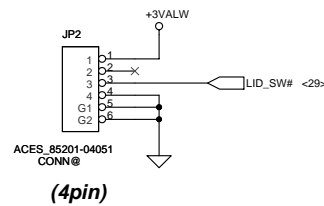
To LED/B



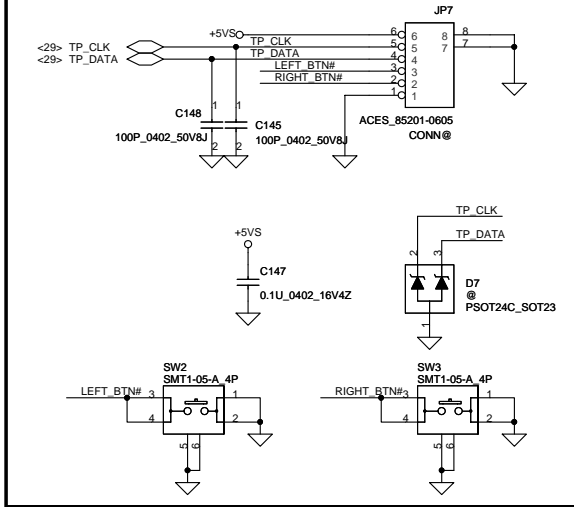
To POWER/B



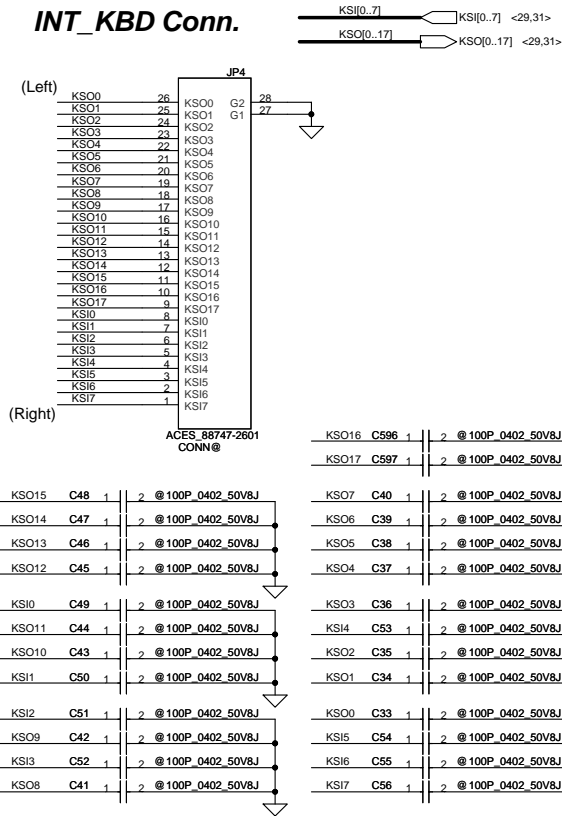
To LID SW/B



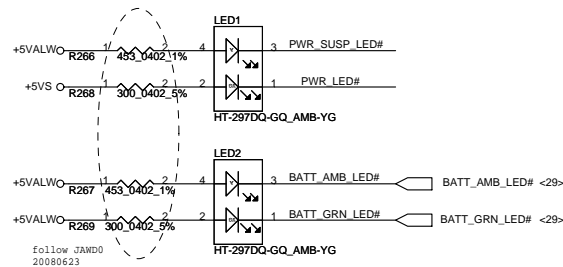
To TP/B Conn.



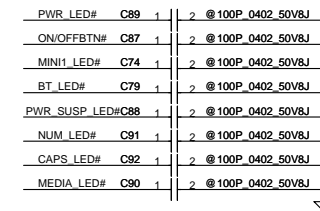
INT_KBD Conn.



Compal Footprint



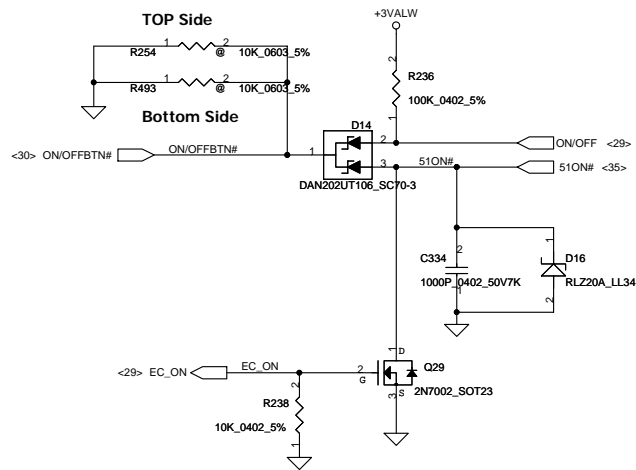
FOR EMI



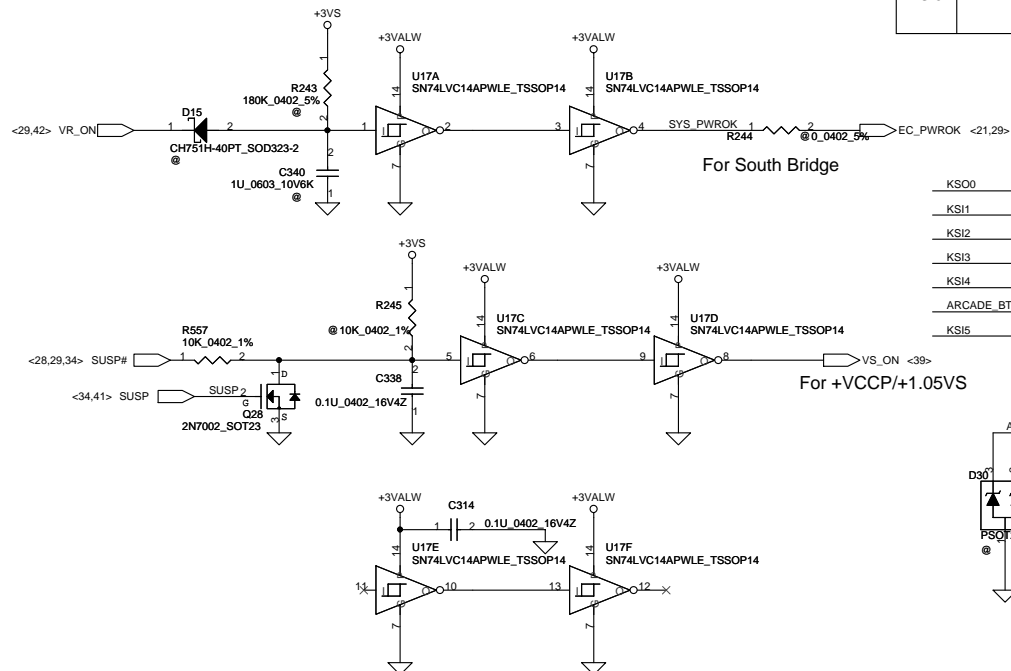
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Power Button

ON/OFF switch



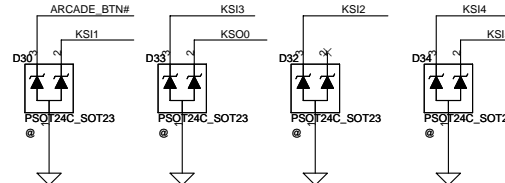
Power ON Circuit



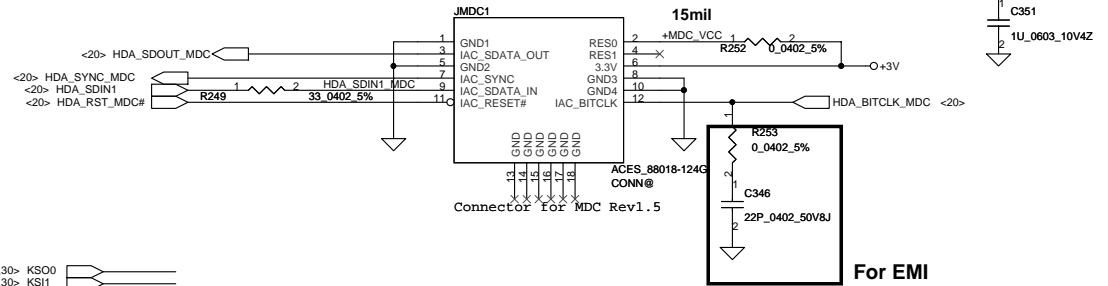
To BTN/B Conn.

	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

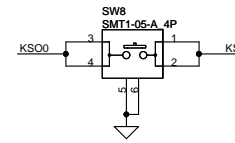
KSO0	C80	1	2	@ 100P_0402_50V8J
KSI1	C81	1	2	@ 100P_0402_50V8J
KSI2	C82	1	2	@ 100P_0402_50V8J
KSI3	C83	1	2	@ 100P_0402_50V8J
KSI4	C84	1	2	@ 100P_0402_50V8J
ARCADE_BTN#	C86	1	2	@ 100P_0402_50V8J
KSI5	C373	1	2	@ 100P_0402_50V8J



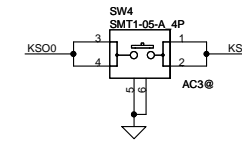
HDA MDC Conn.



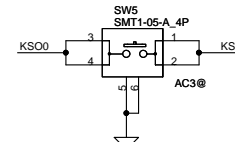
Wireless Button



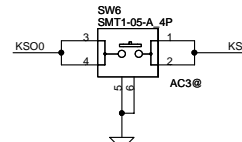
Bluetooth Button



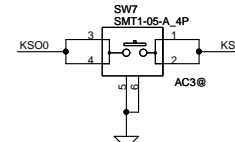
Volume UP BTN



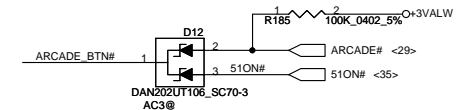
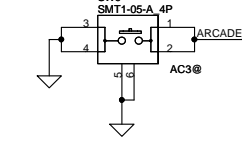
Volume DOWN BTN



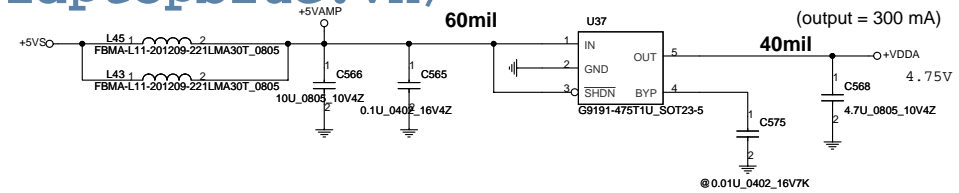
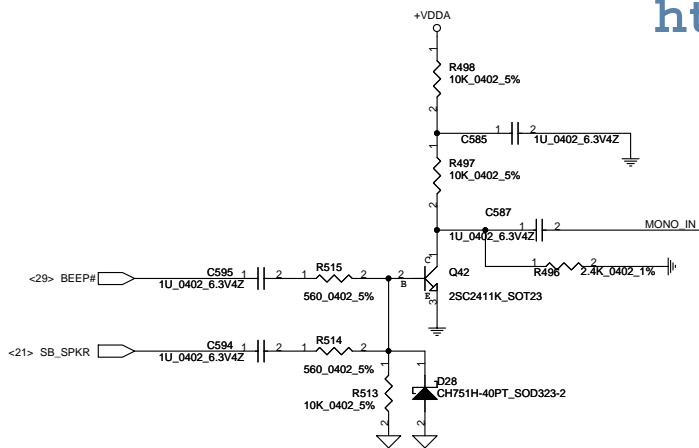
e-Key BTN



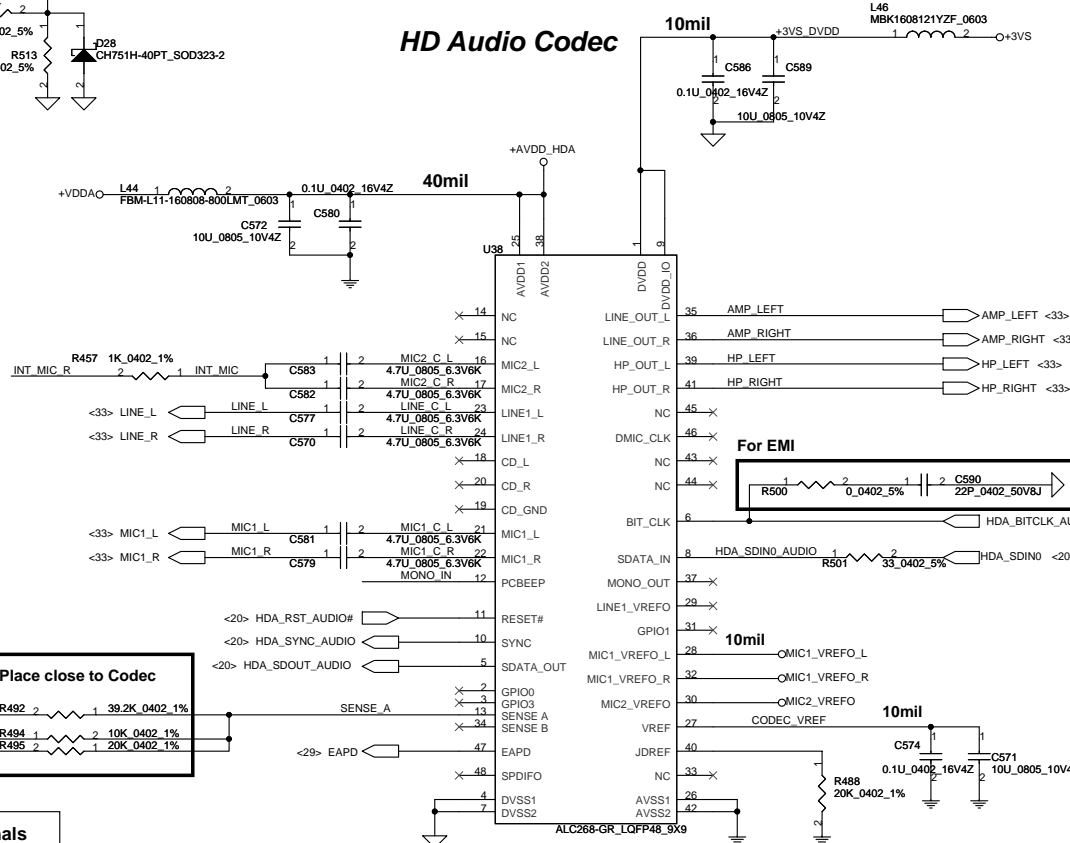
ARCADE BTN

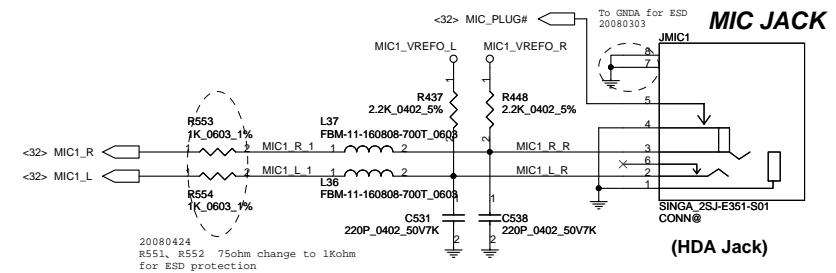
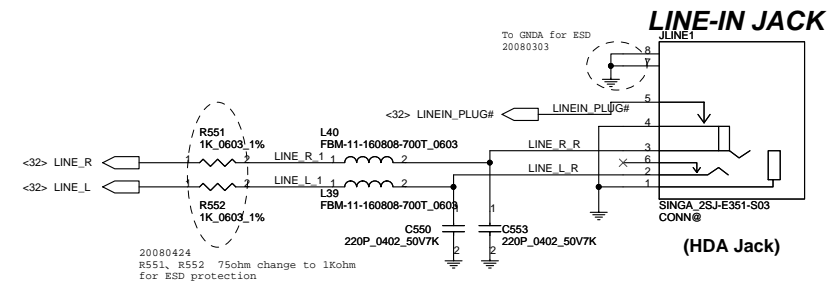
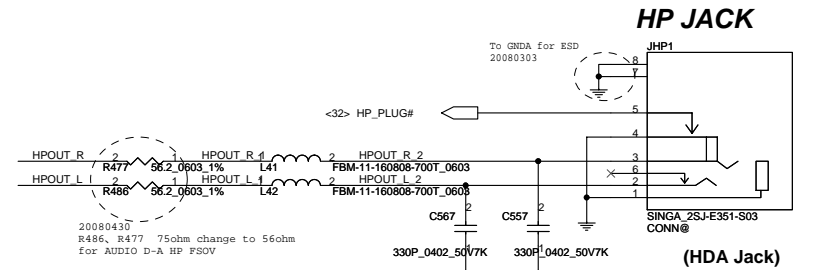
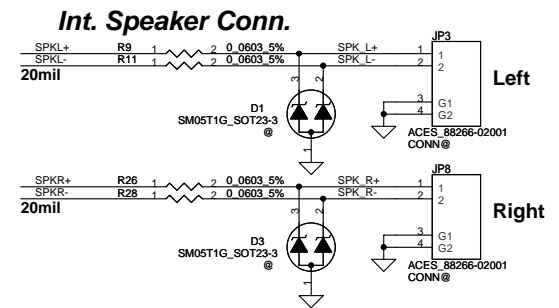
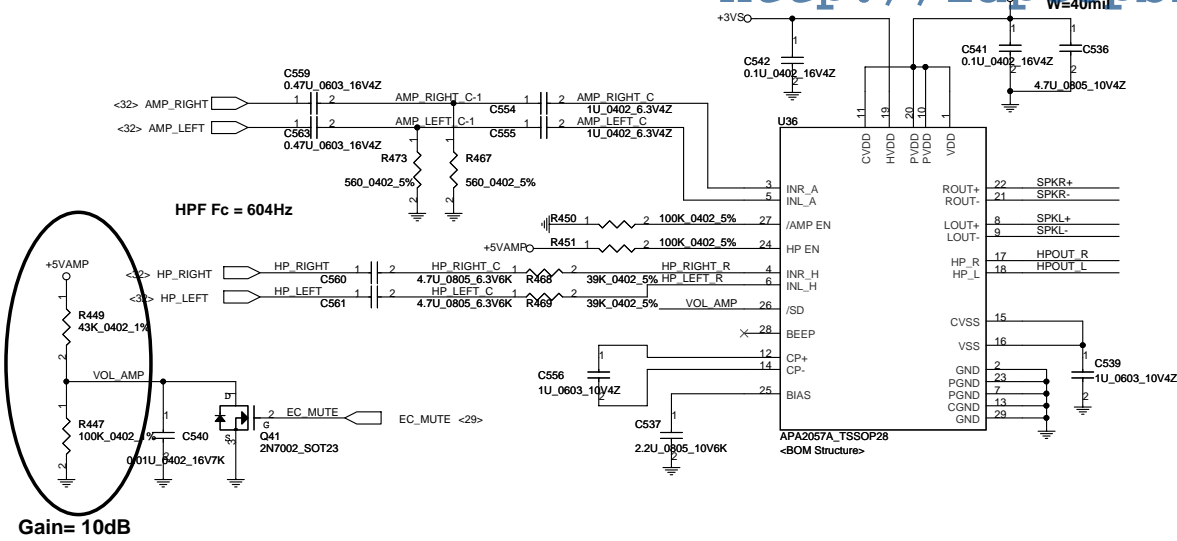


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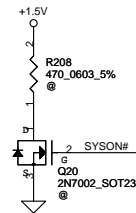
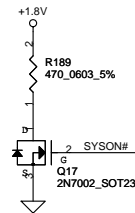
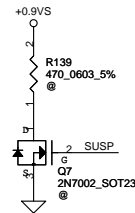
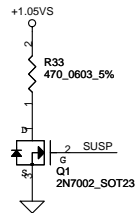
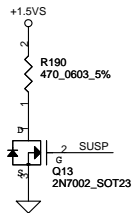
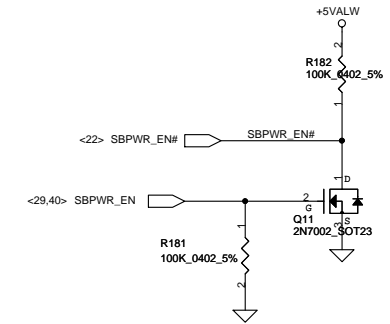
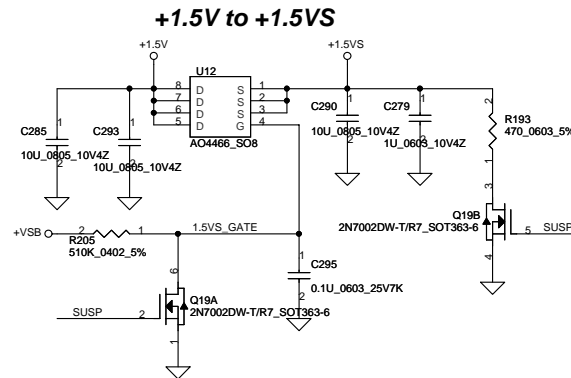
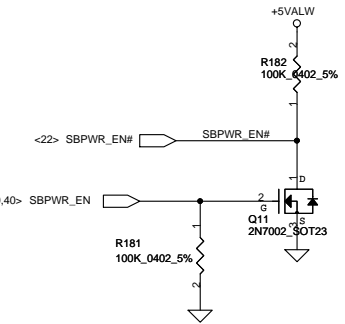
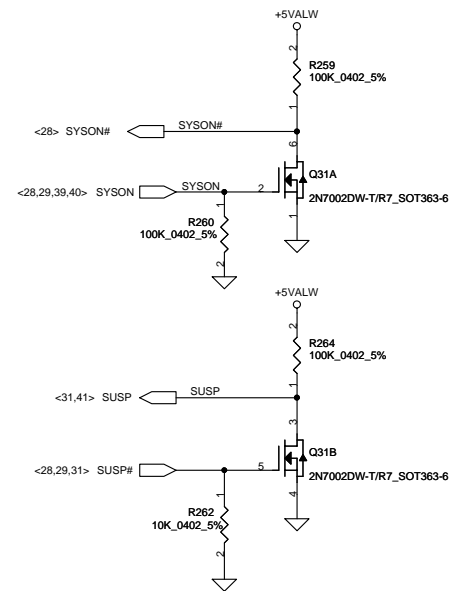
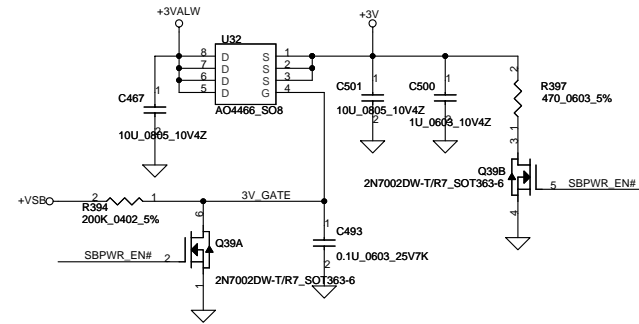
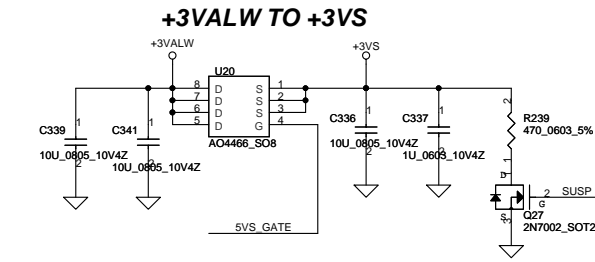
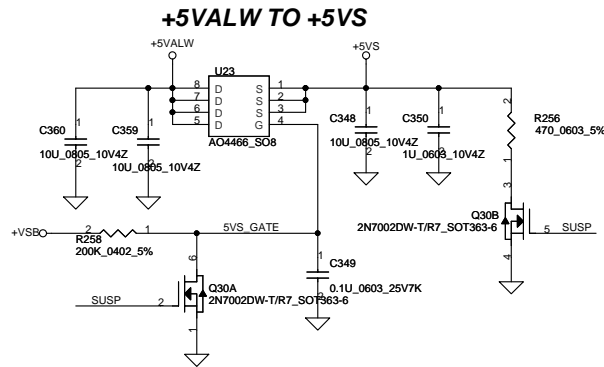


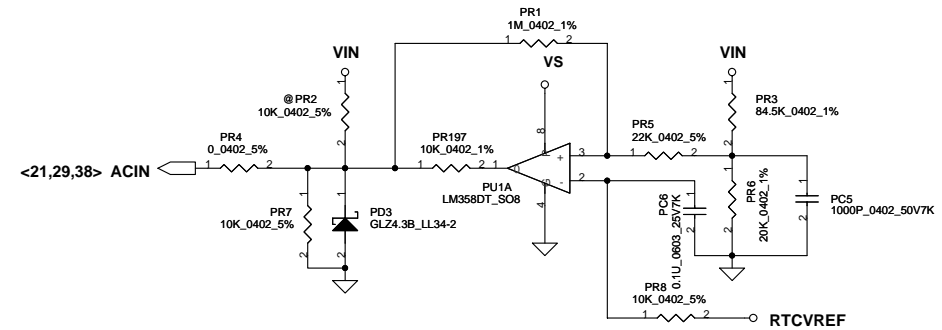
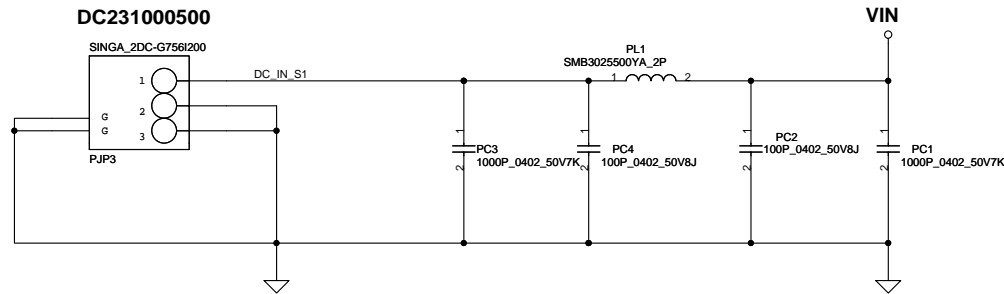
HD Audio Codec





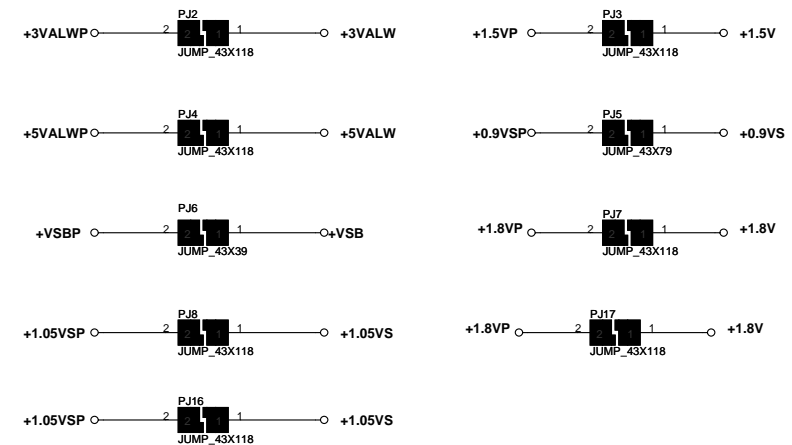
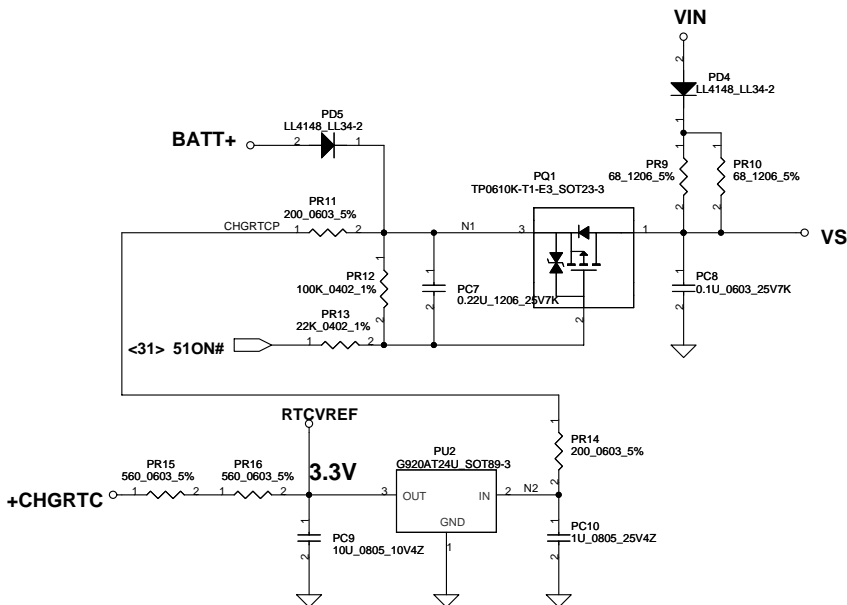
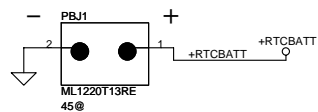
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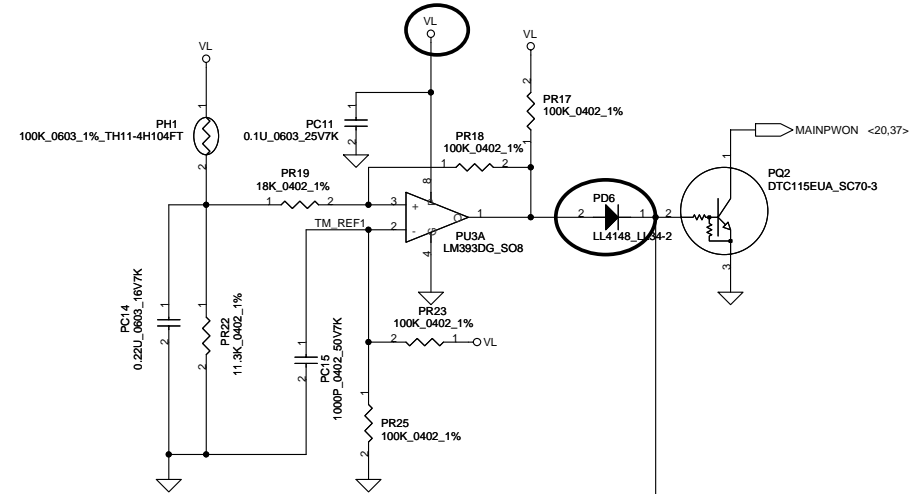
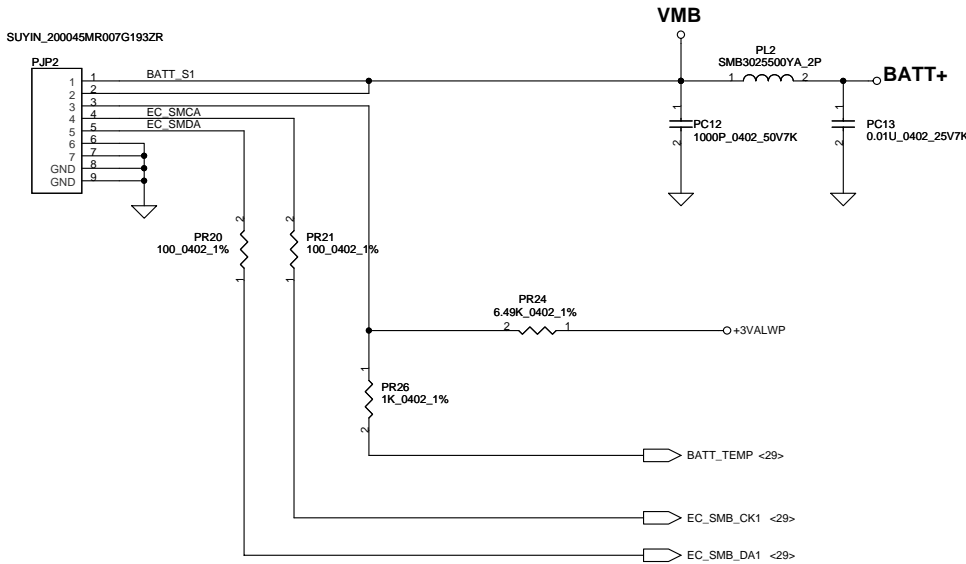
Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

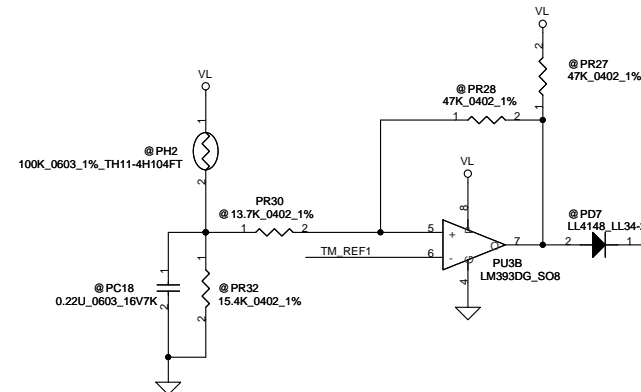
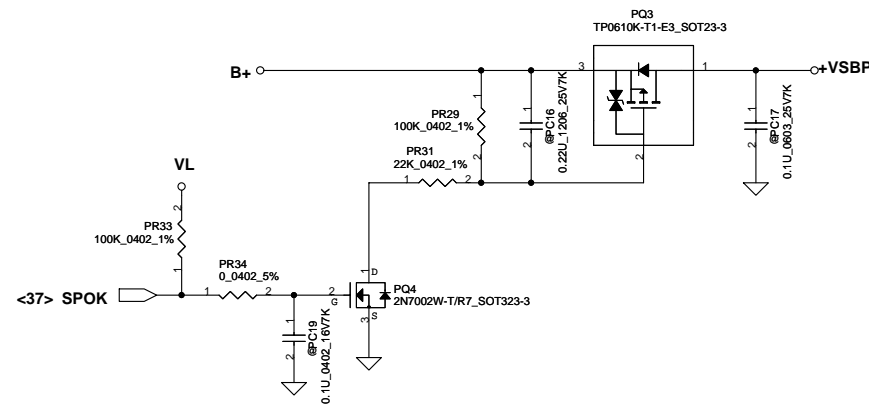


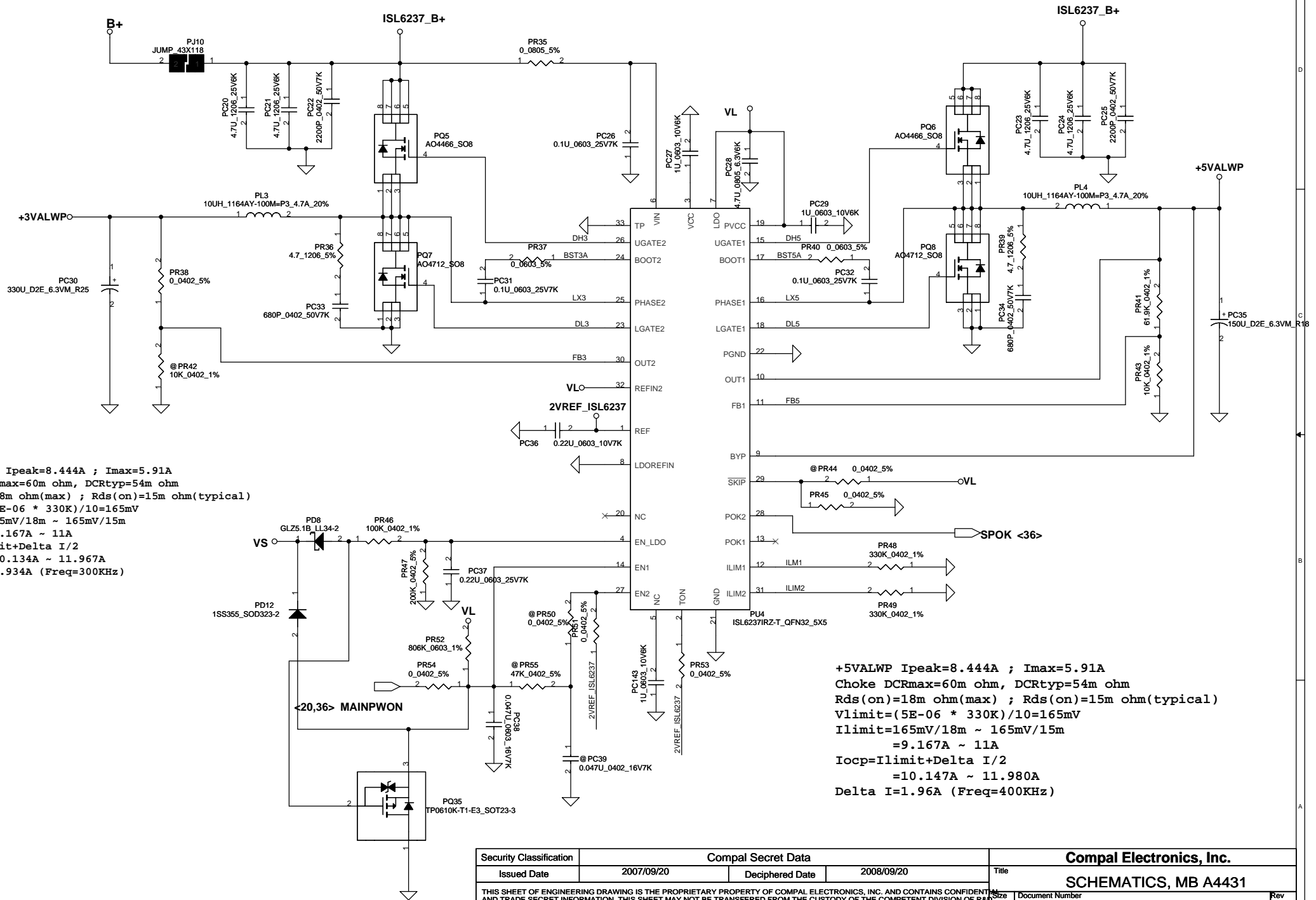
PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C

SUYIN_200045MR007G193ZR



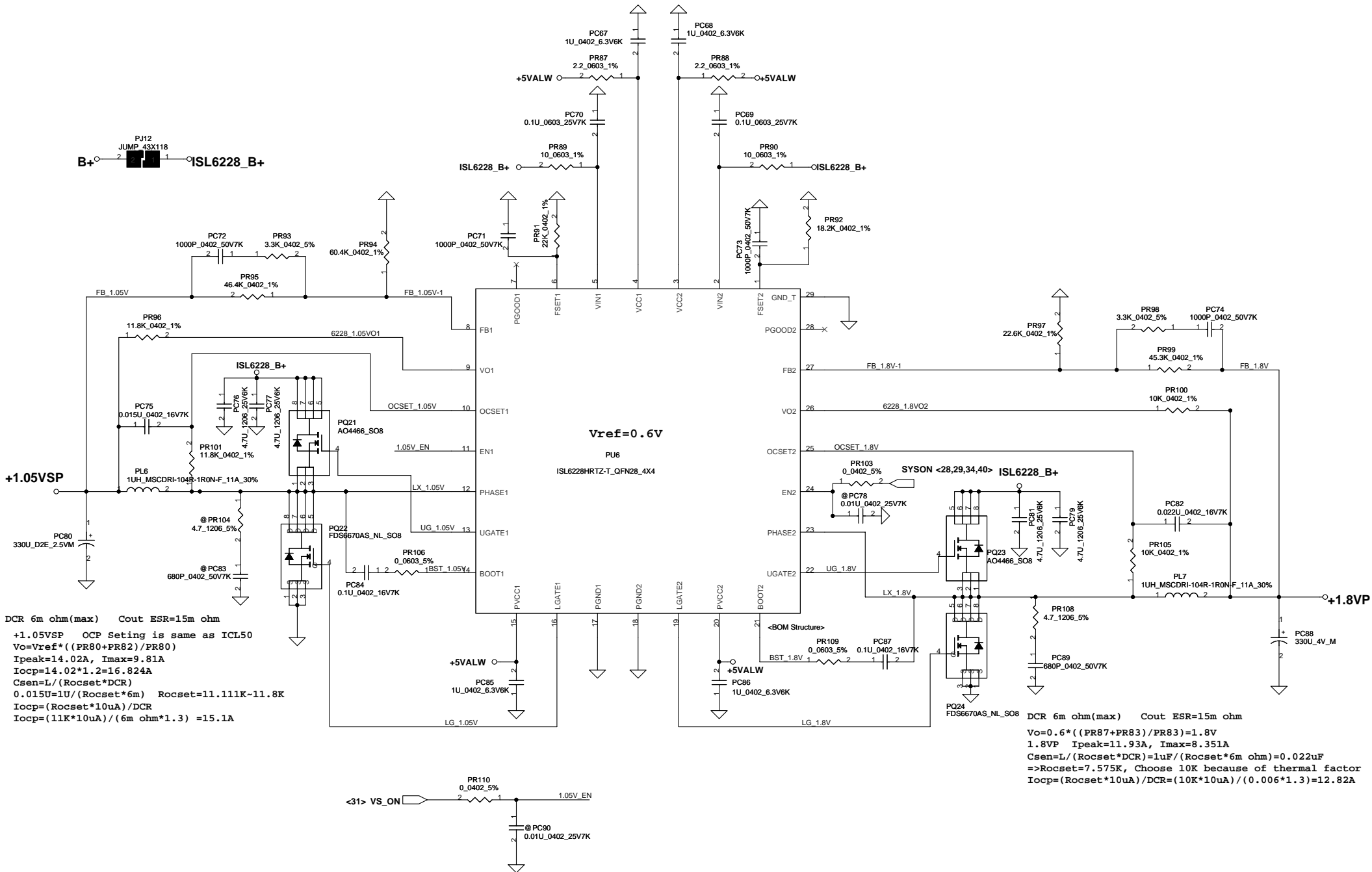
PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 70 degree C

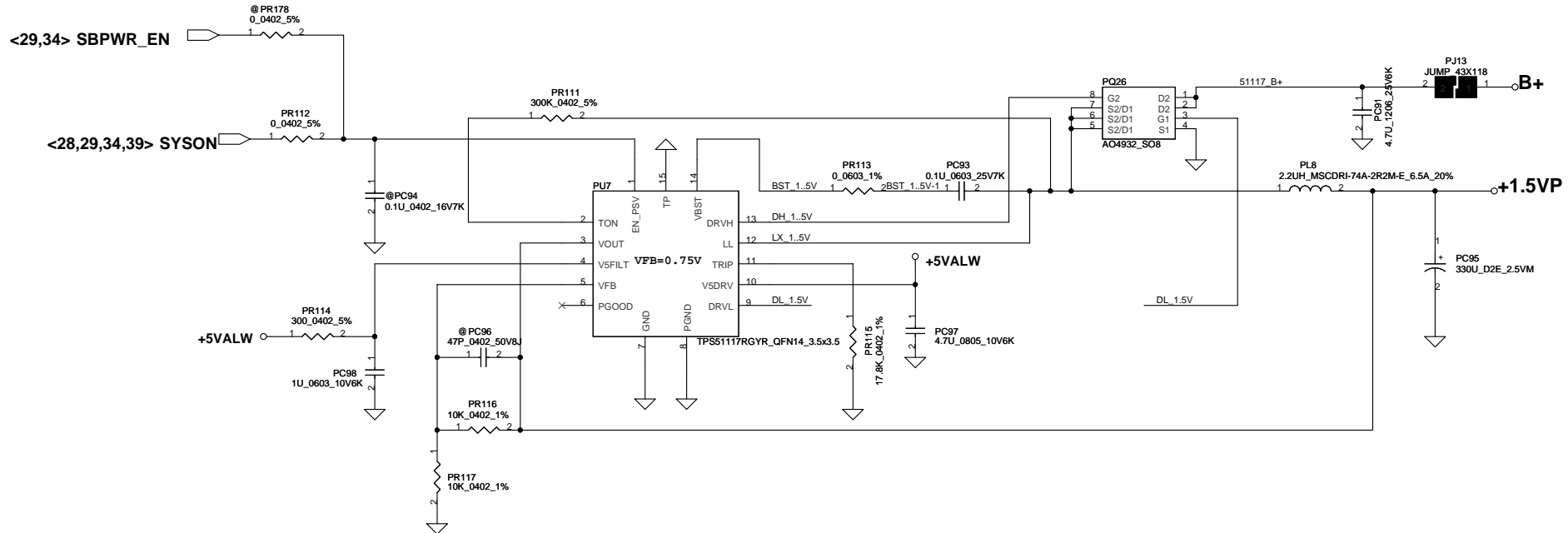




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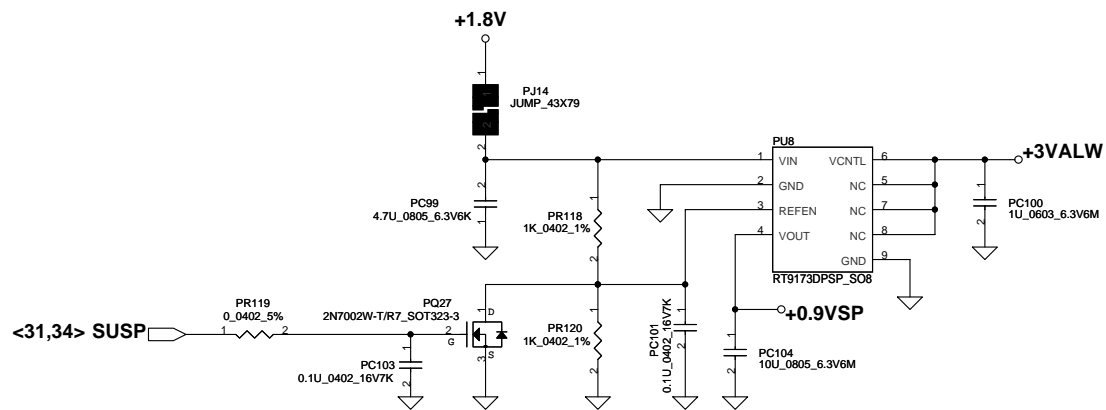




$V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR87/PR88)=0.75 \cdot (1+10K/10K)=1.5V$
 $Ton=19 \cdot e^{-12 \cdot 143000 \cdot ((2/3) \cdot V_o + 100mV) / 19} + 50ns$
 $=2.645e-7 \text{ us}$
 $=>V_o/Vin=D=Ton/Ts \Rightarrow Ts=3.35us$
 $Fsw=298KHz$

$Cout \text{ ESR}=15m \text{ ohm}$
 $I_{peak}=4.71A, I_{max}=3.297A, I_{ocp}=5.652A$
 $\Delta I=((19-1.5) \cdot (1.5/19)) / (L \cdot Fsw)=2.107A$
 $=>1/2 \Delta I=1.053A$
 $V_{trip}=R_{trip} \cdot I_{ocp}=17.8K \cdot 10uA=0.178V$
 $I_{ocpmin}=V_{trip}/R_{dsonmax} \cdot 1.2+1.053A$
 $=0.178 / (0.027 \cdot 1.2) + 1.053=5.493A+1.053A=6.546A$
 $I_{ocpmax}=(0.178 / (0.021 \cdot 1.1)) + 1.053A=7.705A+1.053A$
 $=8.758A$
 $I_{ocp}=6.546A-8.758A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ISL6237 can't shutdown while battery only.	ISL6237 can't shutdown while battery only.	0.1	41	Add PQ35 SB906100210 TP0610K.	20071031	EVT
2	Delete PD1	Because we can cost down and B+ has another one.	0.2	39	Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071115	DVT
3	Change PQ9,PQ10,PQ12 to A04407A	Change PQ9,PQ10,PQ12 to A04407A	0.2	38	Change PQ9,PQ10,PQ12 to A04407A	20080509	DVT
4	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PD2 change to PR197 10K 0402 %1	20080509	DVT
5	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR2 unpop	20080509	DVT
6	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR4 change to 0 0402 %5	20080509	DVT
7	Change PR65	Cells voltage must over 2.5V	0.4	38	PR65 change to 47K 0402 %1	20080613	PVT
8	Node of PR70 is changed	Node of PR70 is changed	0.5	38	Node of PR70_100K_0402_1% change from VREF to RTCVREF	20080620	PVT
9	Add PC89,PR108	for EMI solution	0.6	39	Add PC89:680P_0402_50V7K PR108:4.7_1206_5%	20080620	PVT
10	Add PC169,PC170 on CPUB+	for EMI solution	0.6	42	Add PC169,PC170(470P_0402_50V7K) on CPUB+	20080620	PVT
11	Add PC171 on B+	for EMI solution	0.6	42	Add PC171(1000P_0402_50V7K) on B+	20080620	PVT
12	Change PR138 ,PR152	for EMI solution	0.6	42	PR138 ,PR152 change to 2.2_0603_1%	20080620	PVT
13	Change PR95	pull up the output voltage from 1.05v to 1.06 v	0.7	39	Change PR95 from 45.3K_0402_1% to 46.4K_0402_1%	20080623	PVT
14	Change PR17,PR18,PR19,PR22	Thermal protection 90oC & Recovery at 70oC	0.8	36	Change PR17 and PR18 to 100K_0402_1% Change PR19 to 18K_0402_1% and PR22 to 11.3K_0402_1%	20080701	PVT
15							
16							
17							
18							
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A --> B Change List

4/24
<Page 22>
-R57、 R133 10ohm change to 100ohm
-C135、 C204 0.1u change to 1u
for ICH9 USB1.1 issue
<Page 33>
-R551、 R552、 R553、 R554 75ohm change to 1K
for Audio ESD protection

4/30
-Update Power SCH
<Page 4>
-Add R27、 C427
for +5VS drop issue
-R541 pull high 3.3V
<Page 33>
-R486、 R477 75ohm change to 56.2ohm
for AUDIO D-A HP FSOV

5/2
-Bluetooth USBP5P/5N change to USBP7P/7N

5/5
-Modify LED test value
-Add 51@、 NC@、 GL@

5/6
-Update Power SCH
<Page 25>
-R290 change to L47(SM010014520)
for EMI

5/7
-add BT@、 GM@

B --> C Change List

6/25
<Page 16>
-C301、 C296 33p change to 27p
for RTC issue

C --> Pre MP Change List

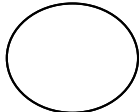
7/14
<Page 16>
-U31 SA00002Q830(QU37) change SA00002Q810(QU56)

7/28
-update Power SCH

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