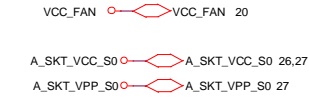
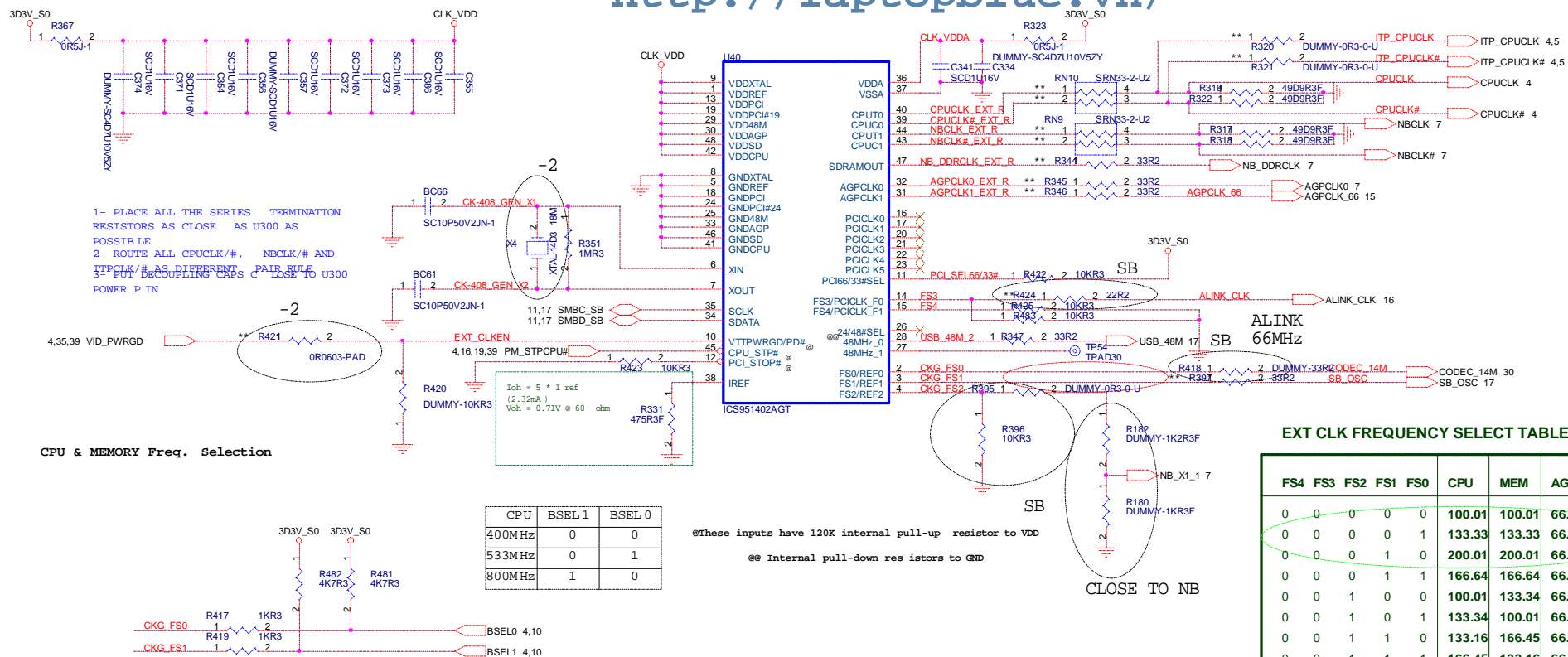


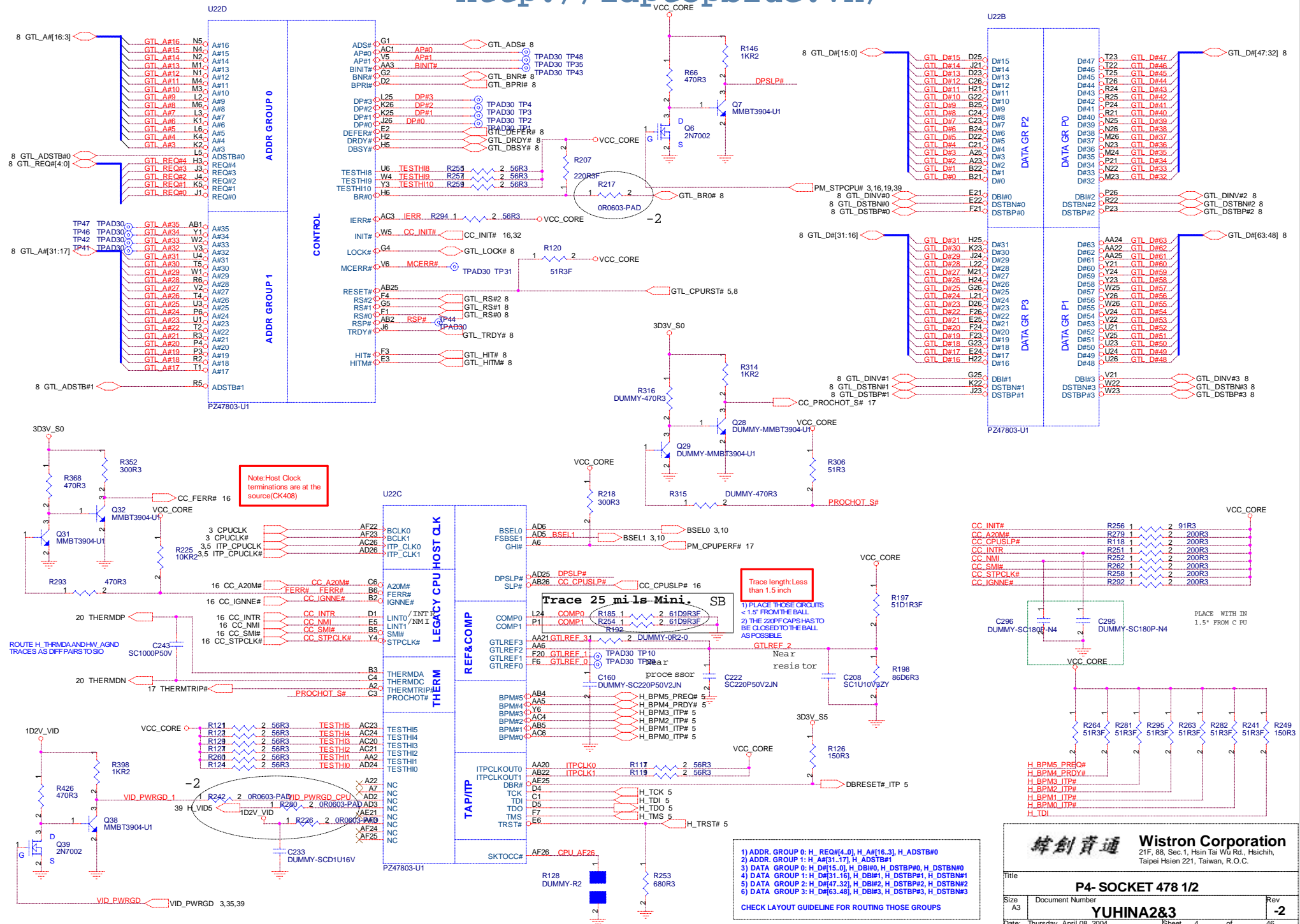
PCI DEVICE RESOURCE ASSIGNMENT

|         | BUS | DEVICE | IDSEL    | PCI_REQ# | PCI_GNT# | INT_IRQ#    |
|---------|-----|--------|----------|----------|----------|-------------|
| LAN     | 1   | 5      | PCI_AD26 | REQ#4    | GNT#4    | IRQD#       |
| CardBus | 1   | 9      | PCI_AD20 | REQ#1    | GNT#1    | IRQB#/IRQA# |
| MiniPCI | 1   | 6      | PCI_AD21 | REQ#2    | GNT#2    | IRQE#       |
|         |     |        |          |          |          |             |
|         |     |        |          |          |          |             |

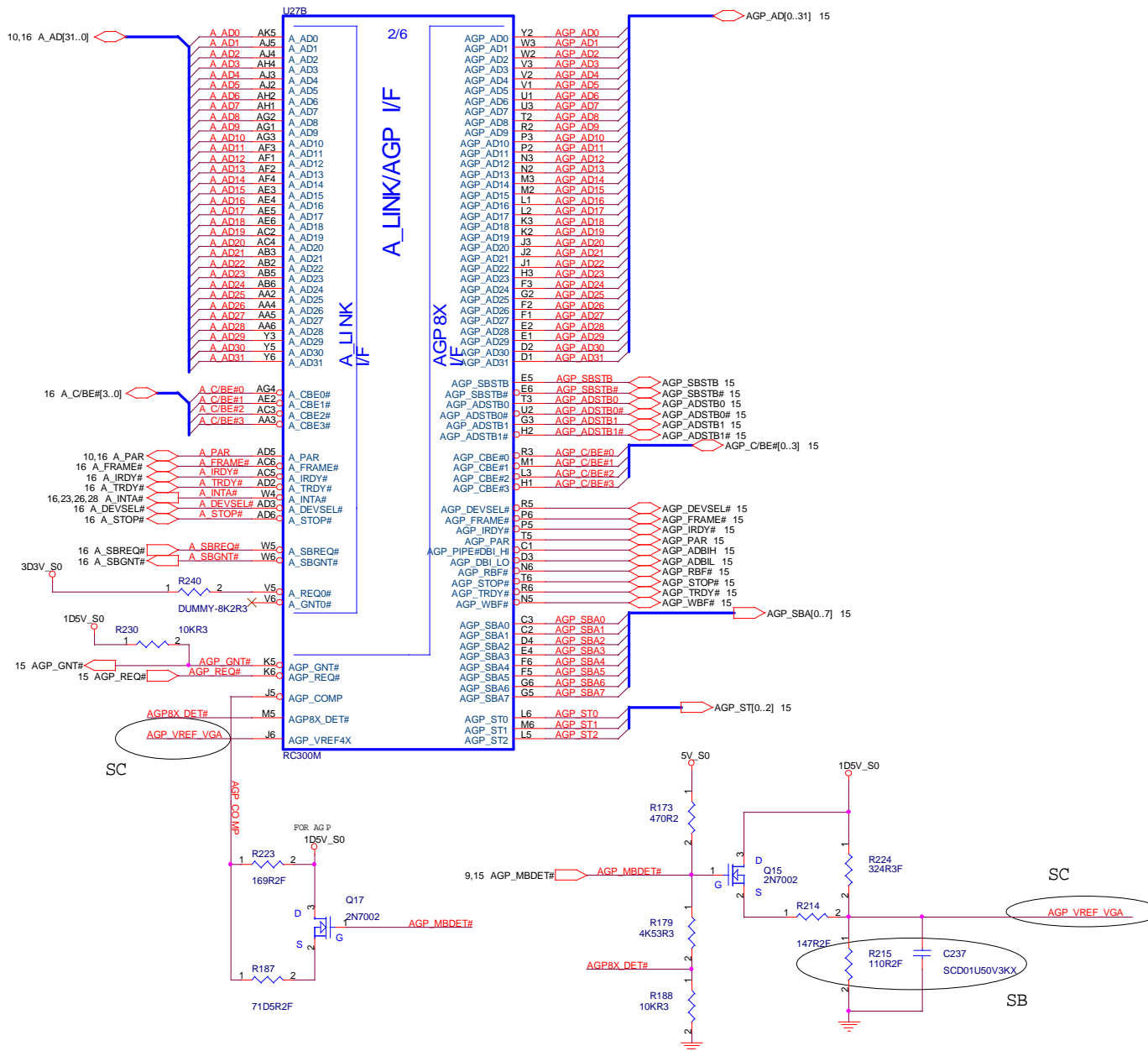




| FS4 | FS3 | FS2 | FS1 | FS0 | CPU    | MEM    | AGP   | PCI   |
|-----|-----|-----|-----|-----|--------|--------|-------|-------|
| 0   | 0   | 0   | 0   | 0   | 100.01 | 100.01 | 66.66 | 33.33 |
| 0   | 0   | 0   | 0   | 1   | 133.33 | 133.33 | 66.66 | 33.33 |
| 0   | 0   | 0   | 1   | 0   | 200.01 | 200.01 | 66.66 | 33.33 |
| 0   | 0   | 0   | 1   | 1   | 166.64 | 166.64 | 66.66 | 33.33 |
| 0   | 0   | 1   | 0   | 0   | 100.01 | 133.34 | 66.66 | 33.33 |
| 0   | 0   | 1   | 0   | 1   | 133.34 | 100.01 | 66.66 | 33.33 |
| 0   | 0   | 1   | 1   | 0   | 133.16 | 166.45 | 66.66 | 33.33 |
| 0   | 0   | 1   | 1   | 1   | 166.45 | 133.16 | 66.66 | 33.33 |

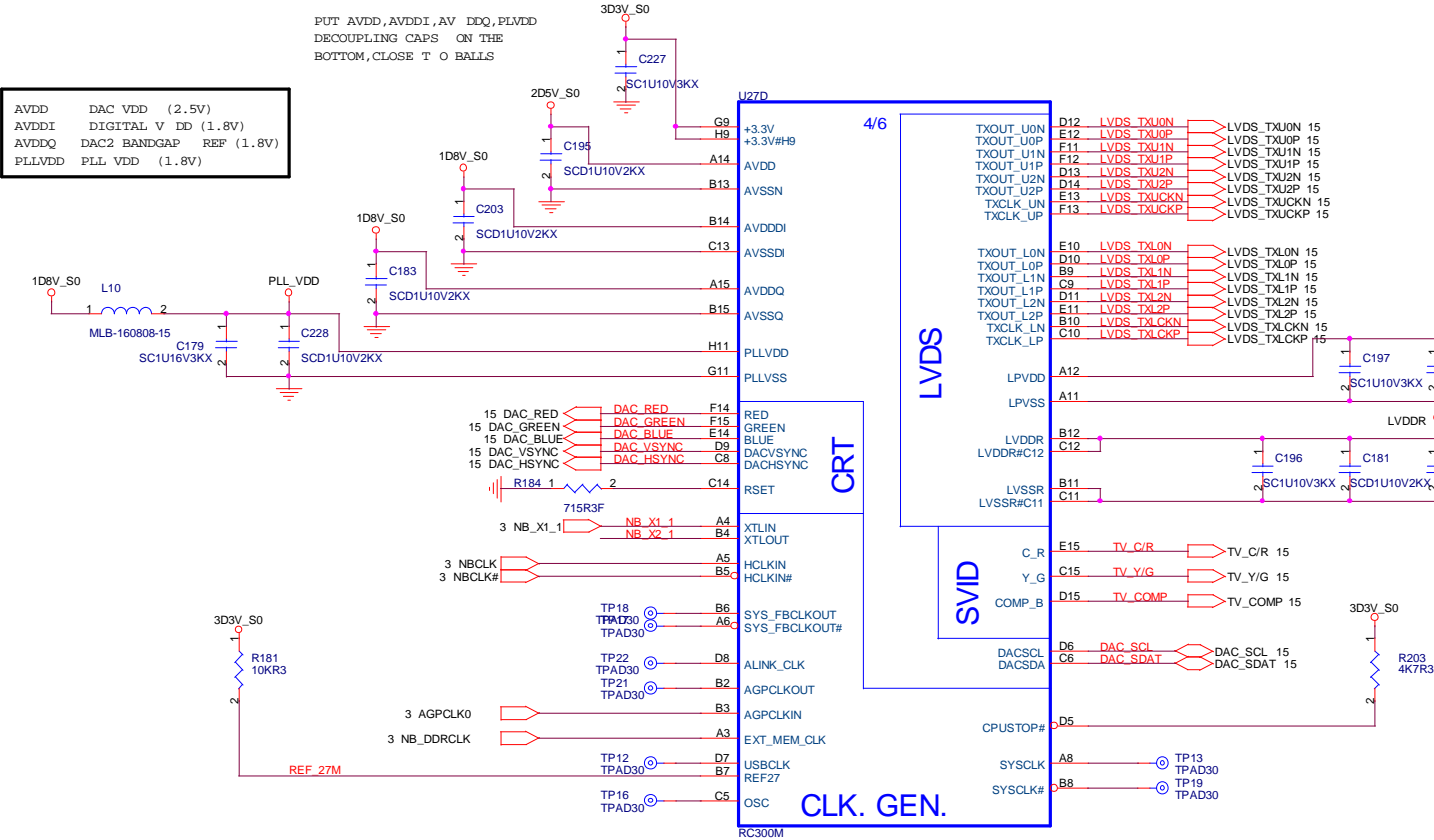




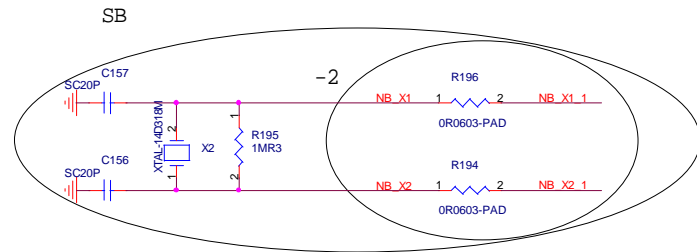


PUT AVDD, AVDDI, AV DDQ, PLVDD  
DECOUPLING CAPS ON THE  
BOTTOM, CLOSE TO BALLS

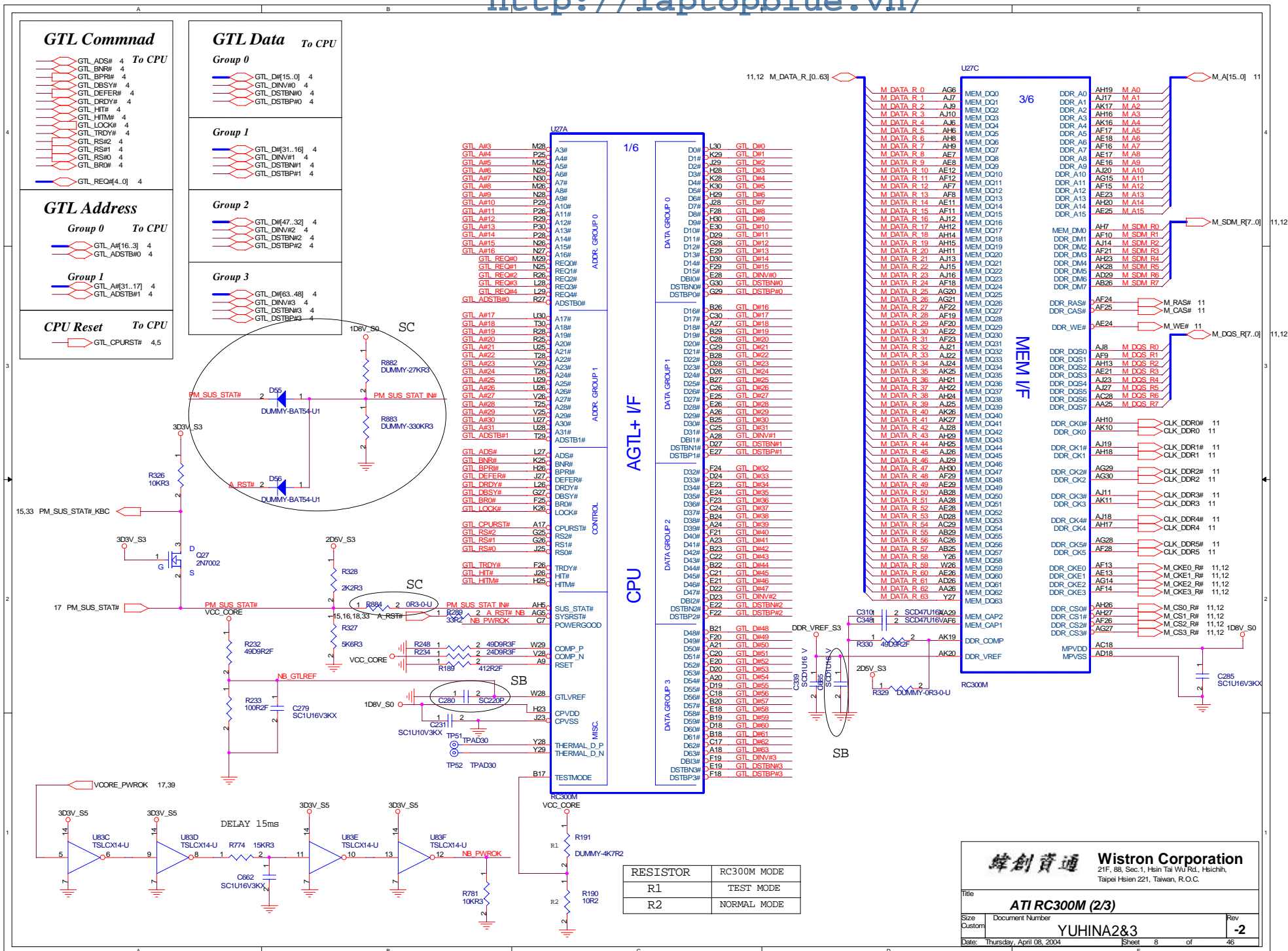
AVDD DAC VDD (2.5V)  
AVDDI DIGITAL V DD (1.8V)  
AVDDQ DAC2 BANDGAP REF (1.8V)  
PLLVD PLL VDD (1.8V)



**Bead Spec:**  
200ohm at 100MHZ  
DCR=0.4ohm  
Current Rating: 200mA



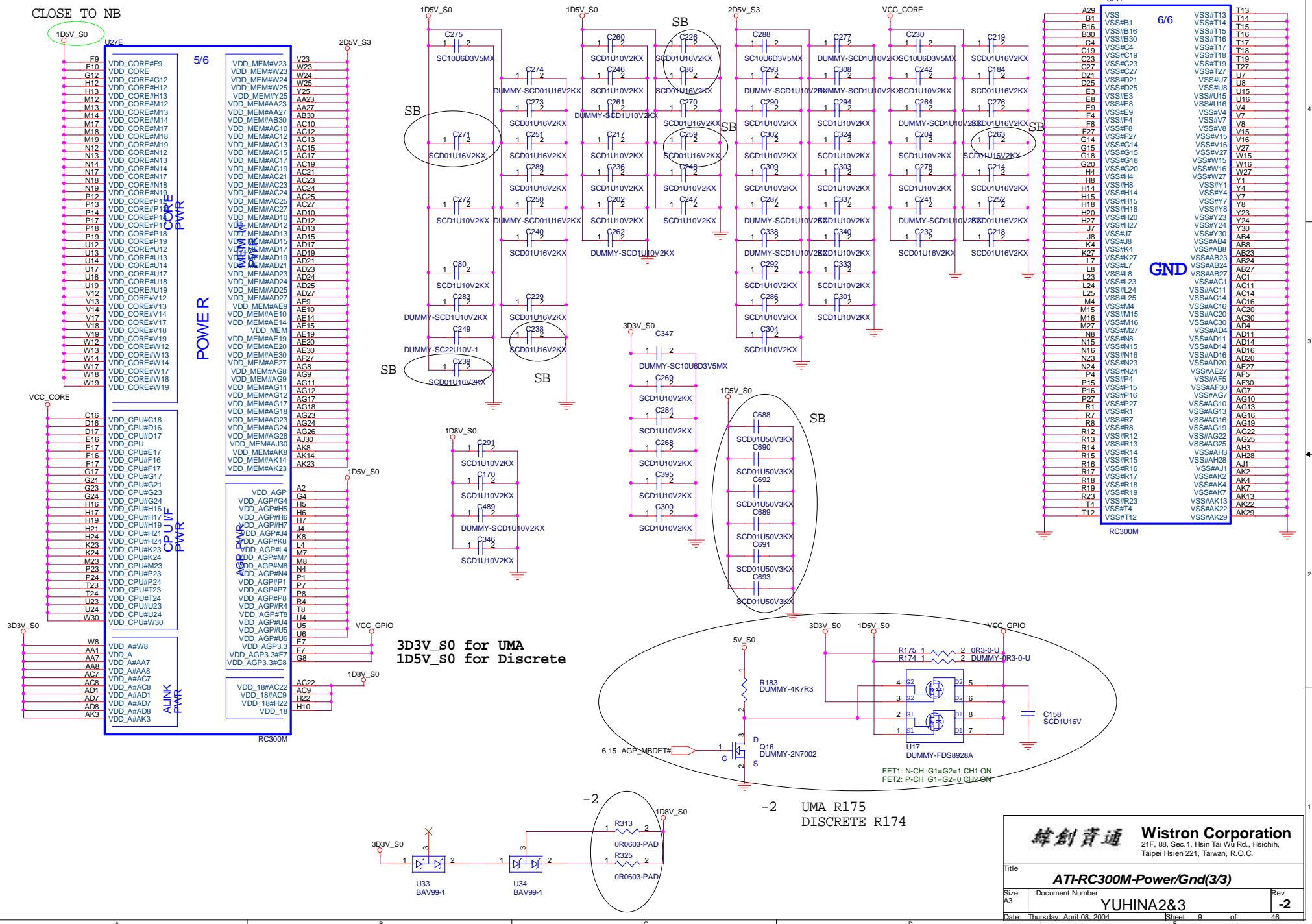




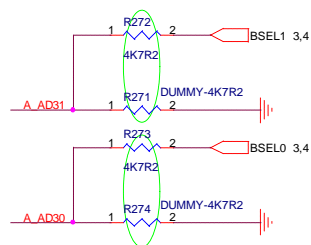
緯創資通 Wistron Corporation  
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Taipei Hsien Z21, Taiwan, R.O.C.



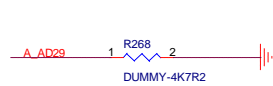
CLOSE TO NB



## RC300M STRAPPING



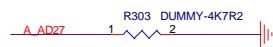
**A\_AD[31..30] : FSB CLK SPEED**  
 Default: 00  
 00: 100MHZ  
 01: 133MHZ  
 10: 200MHZ  
 11: 166MHZ



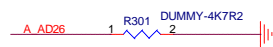
**A\_AD29 : STRAP CONFIGURATION**  
 Default : 1  
 0: REDUCE SET  
 1: FULL SET



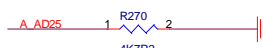
**A\_AD28 :SPREAD SPECTRUM ENABLE**  
 Default : 0  
 0: DISABLE SS  
 1: ENABLE SS



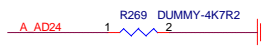
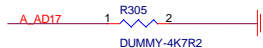
**A\_AD27 :FrcShorttReset#**  
 Default : 1  
 0: TESTE MODE  
 1: NORMAL MODE



**A\_AD26 :ENABLE IOQ**  
 Default : 1  
 0: IOQ=1  
 1: IOQ=12



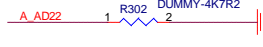
**A\_AD25,A\_AD17 :CPU VOLTAGE[1..0]**  
 Default : 01  
 00: 1.05V (MOBILE CPU)  
 01: 1.35V (MOBILE CPU)  
 10: 1.45V (DESKTOP CPU)  
 11: 1.75V (DESKTOP CPU)



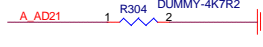
**A\_AD24 :MOBILE CPU SELECT**  
 Default : 1  
 0: BANTAS CPU  
 1: NOT BANTAS CPU



**A\_AD23 :CLOCK BYPASS DISABLE**  
 Default : 1  
 0: TEST MODE  
 1: NORMAL OPERATION

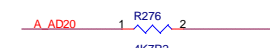


**A\_AD22 :OSC PAD OUTPUT PCICLK**  
 Default : 1  
 0: OSC PIN DRIVES PCICLK  
 1: OSC PIN DRIVES OSC CLK



**A\_AD21 :AUTO\_CAL ENABLE**  
 Default : 1  
 0: DISABLE AUTO\_CAL  
 1: ENABLE AUTO\_CAL

A\_AD[31..0] 6,16



**A\_AD20 :INTERNAL CLK GEN ENABLE**  
 Default : 1  
 0: EXTERNAL CLOCK GENERATOR  
 1: INTERNAL CLOCK GENERATOR

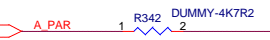


**A\_AD19 :MEMORY IO VOLTAGE SELECTION**  
 Default : 1  
 0: 1.8V  
 1: 2.5V



**A\_AD18 :ENABLE PHASE CALIBRATION**  
 Default : 0  
 0: DISABLE  
 1: ENABLE

6,16 A\_PAR A\_PAR

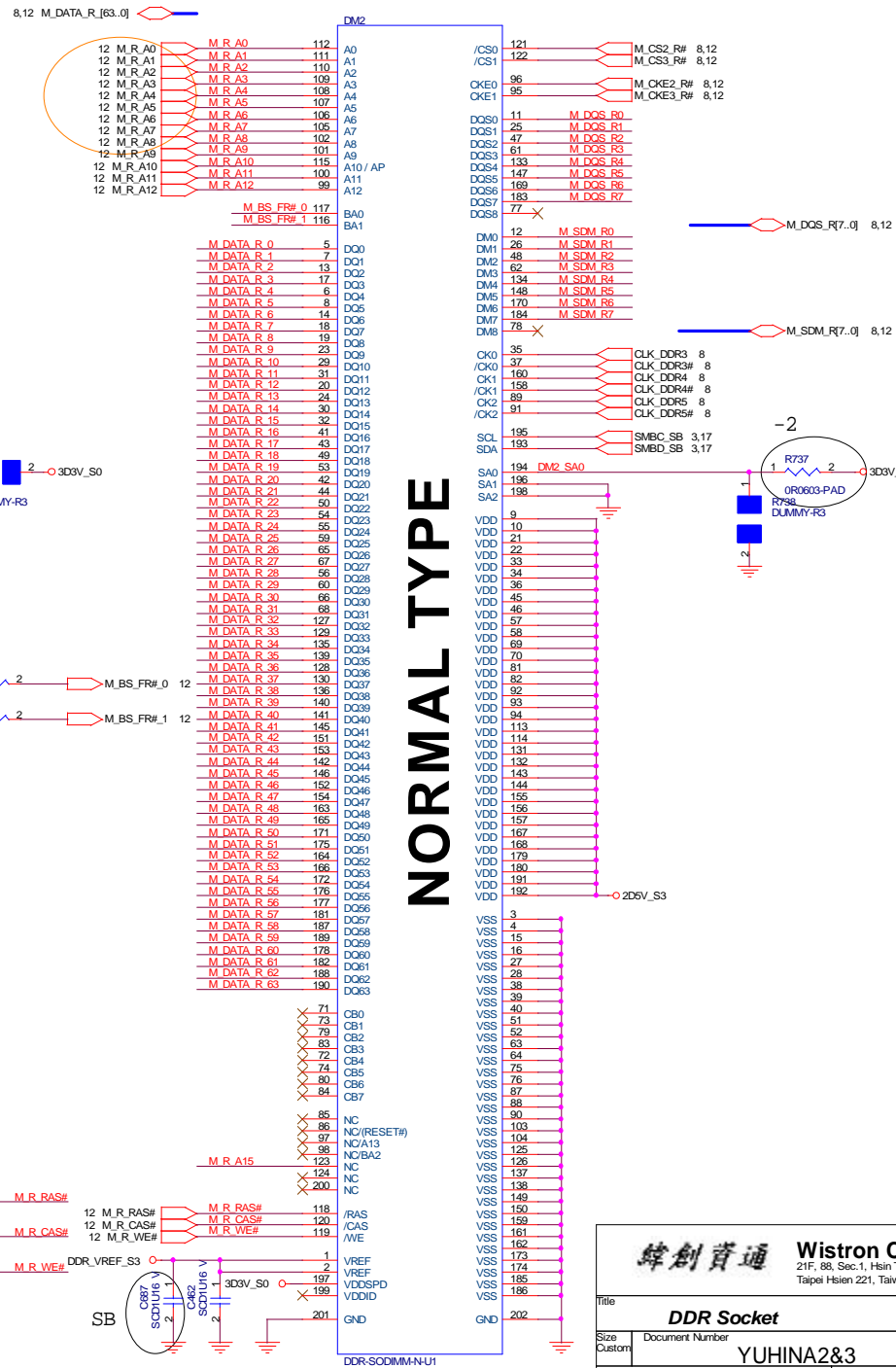
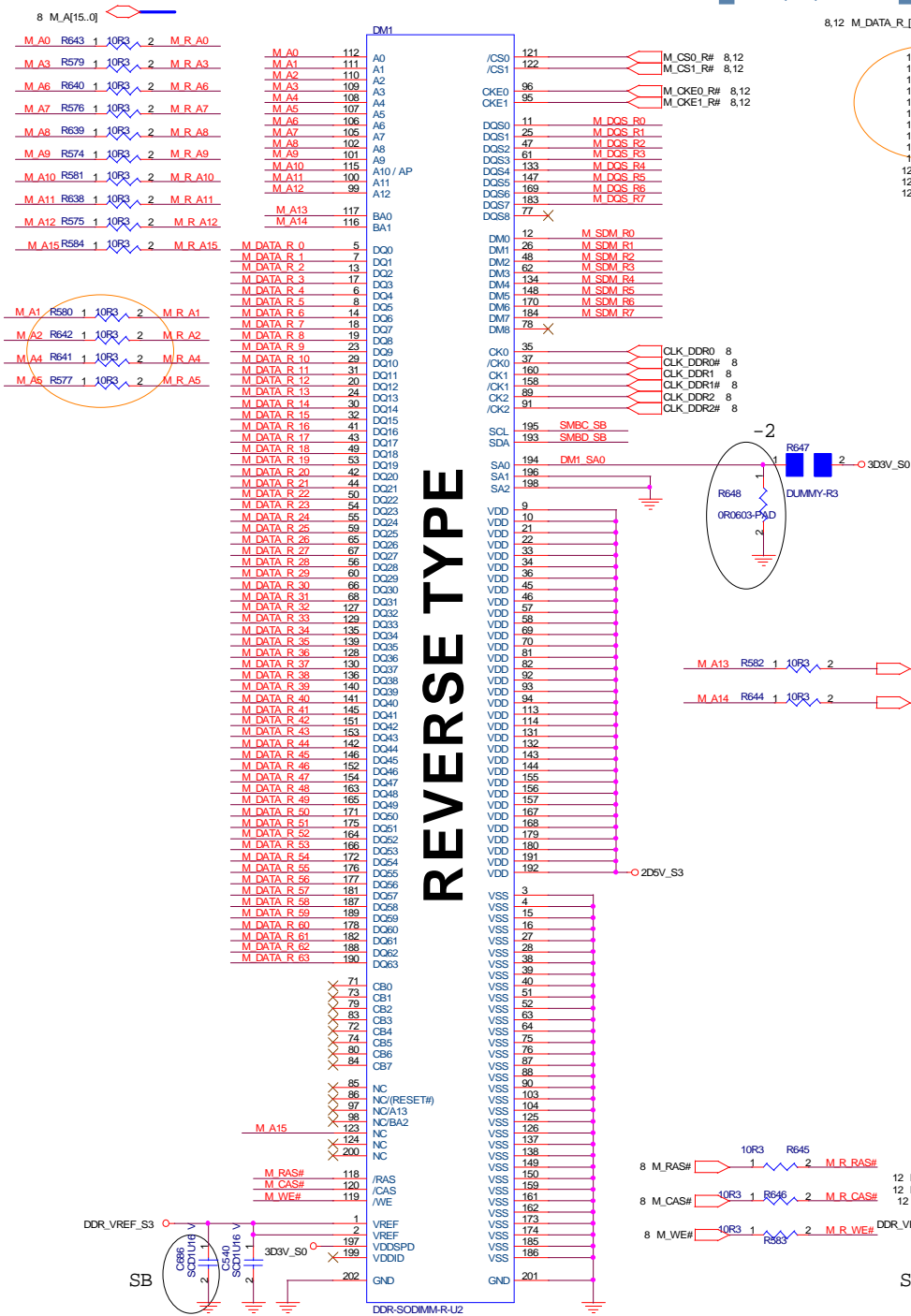


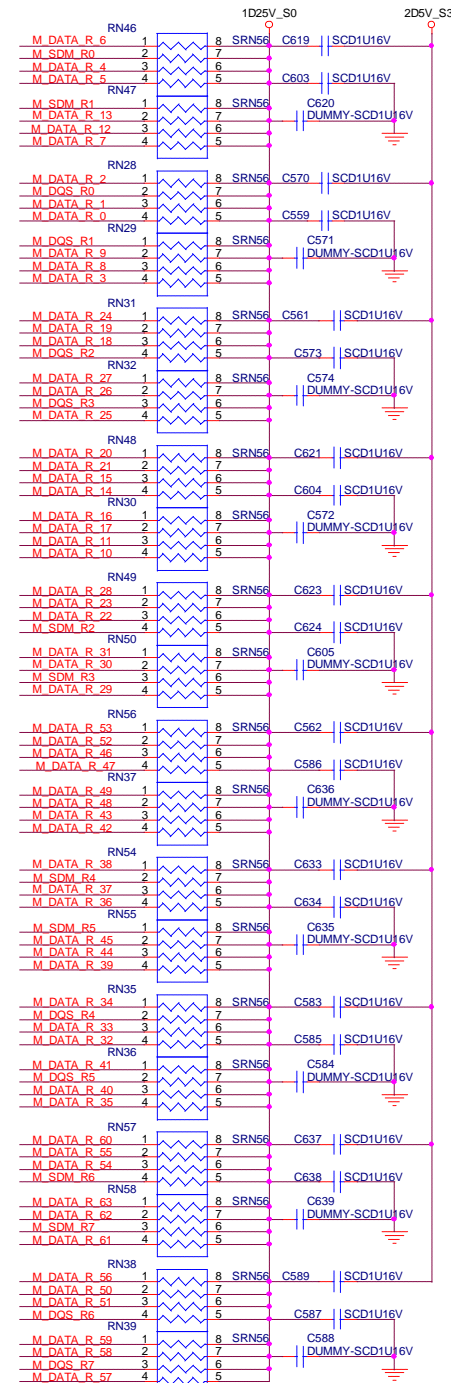
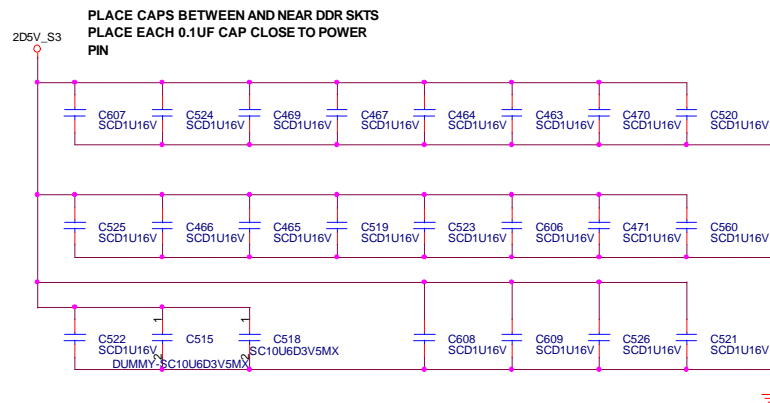
**PAR :EXTENDED DEBUG MODE**  
 Default : 1  
 0: DEBUG MODE  
 1: NORMAL OPERATION

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 Taipei Hsien 221, Taiwan, R.O.C.

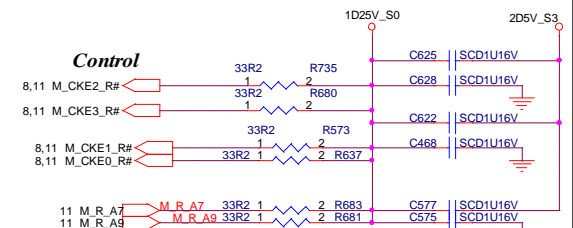
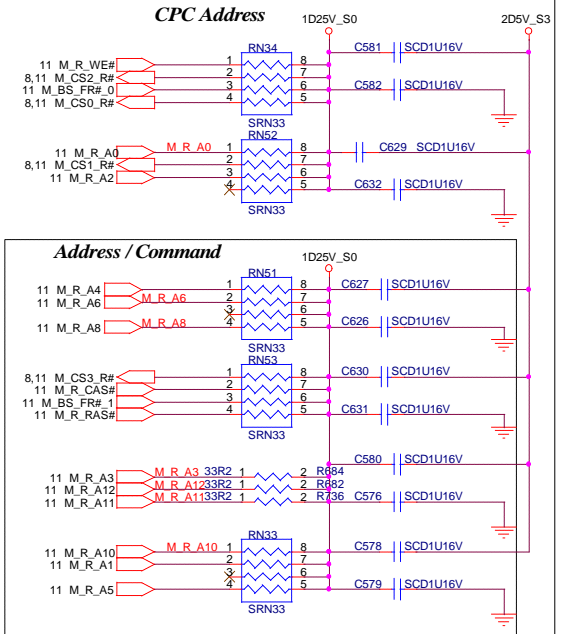
|                                |                 |       |
|--------------------------------|-----------------|-------|
| Title                          |                 |       |
| NB STRAPPING                   |                 |       |
| Size                           | Document Number | Rev   |
| A3                             | YUHINA283       | -2    |
| Date: Thursday, April 08, 2004 | Sheet 10        | of 46 |





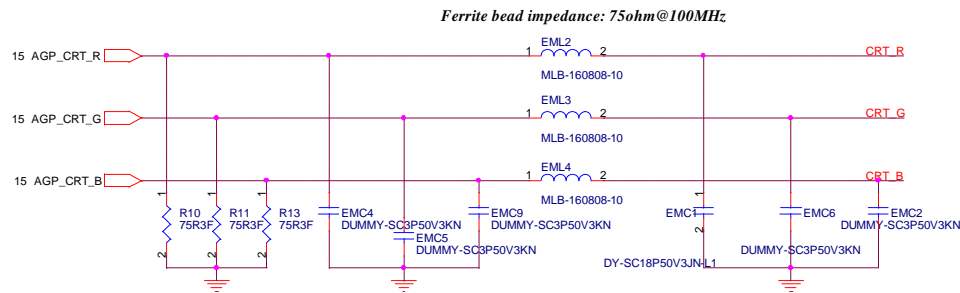
## PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2  
NO EQUAL LENGTH LIMITATION



|                                                                             |                                      |                |
|-----------------------------------------------------------------------------|--------------------------------------|----------------|
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| 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                                      |                |
| Title <b>DDR Serial/Terminator Resistor</b>                                 |                                      |                |
| Size A3                                                                     | Document Number <b>YUHINA2&amp;3</b> | Rev <b>-2</b>  |
| Date: Thursday, April 08, 2004                                              |                                      | Sheet 12 of 46 |

# CRT I/F & CONNECTOR

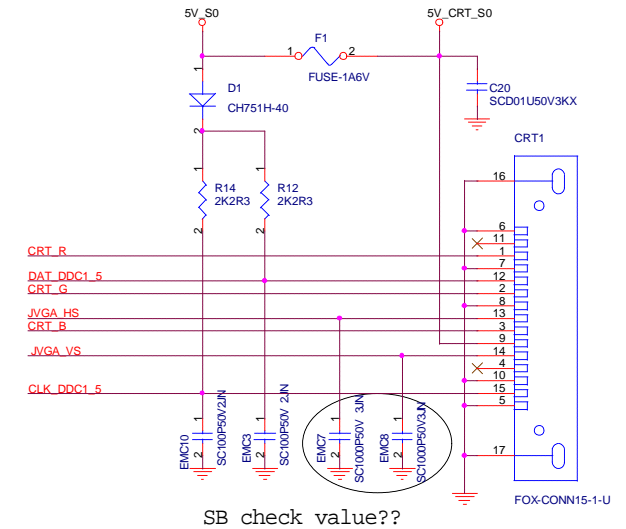


**Layout Note:**

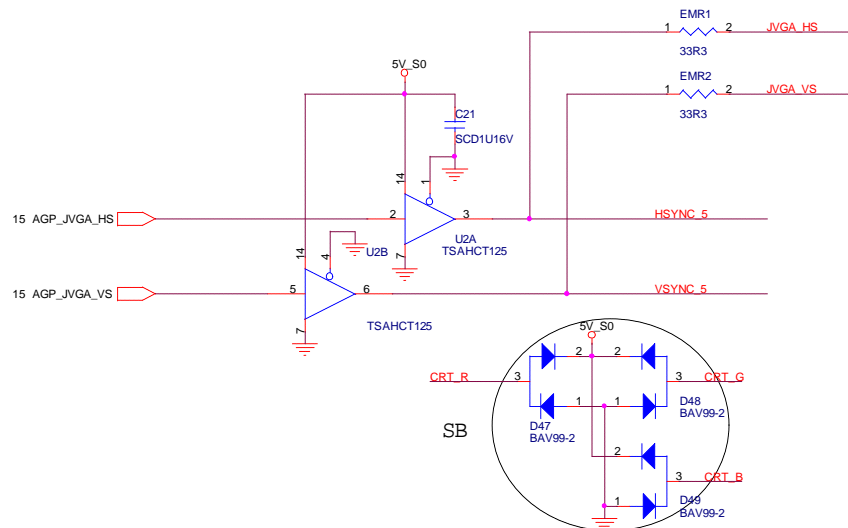
- \* Must be a ground return path between this ground and the ground on the VGA connector.
- \* 37.4\_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

**Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.**

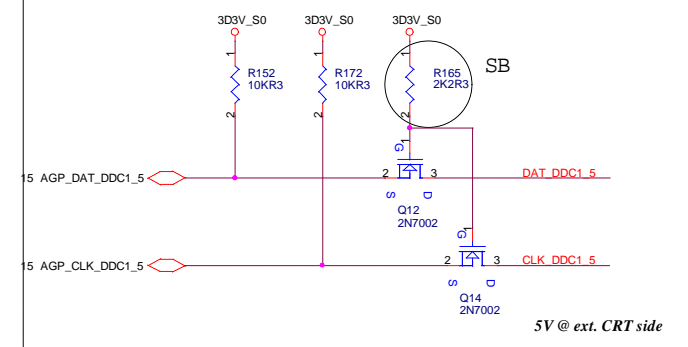
RDDP 1.0



**Hsync & Vsync level shift**



**DDC\_CLK & DATA level shift**

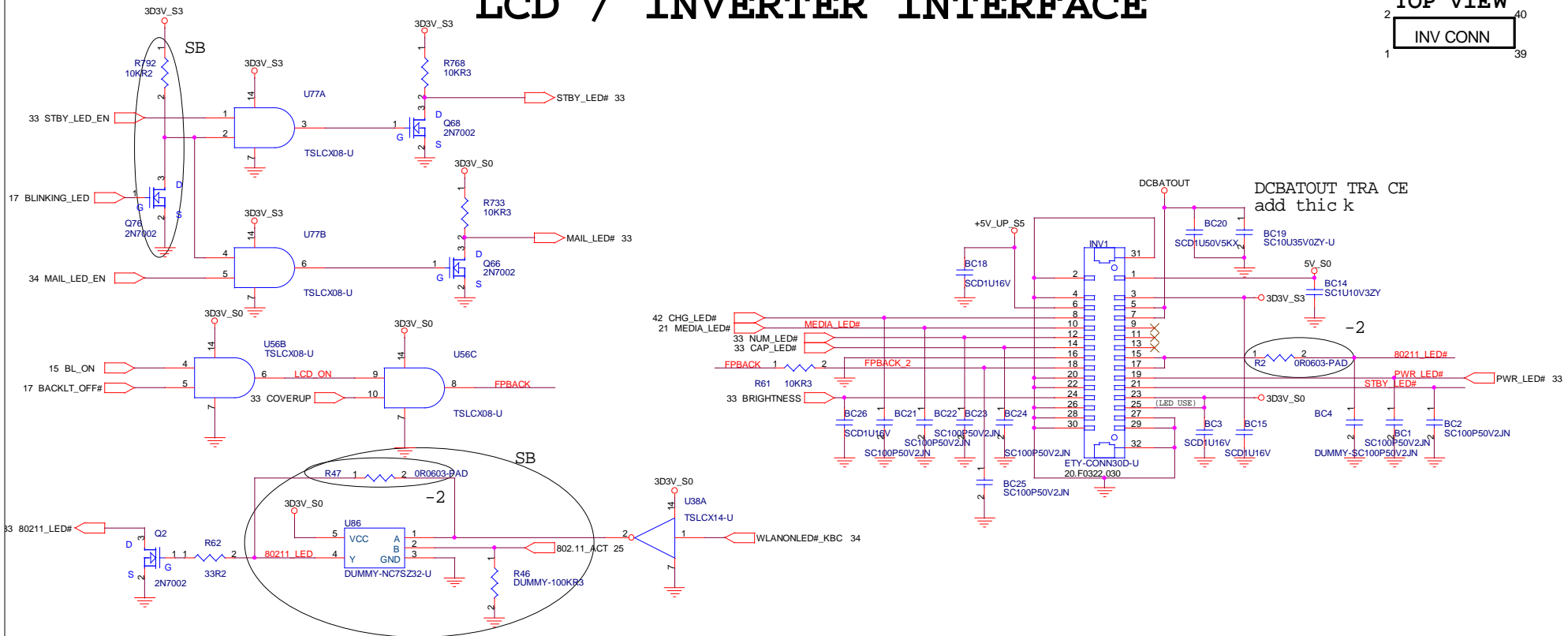


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|                      |                          |                |
|----------------------|--------------------------|----------------|
| Title                |                          |                |
| <b>CRT Connector</b> |                          |                |
| Size                 | Document Number          | Rev            |
| A3                   | YUHINA2&3                | -2             |
| Date:                | Thursday, April 08, 2004 | Sheet 13 of 46 |

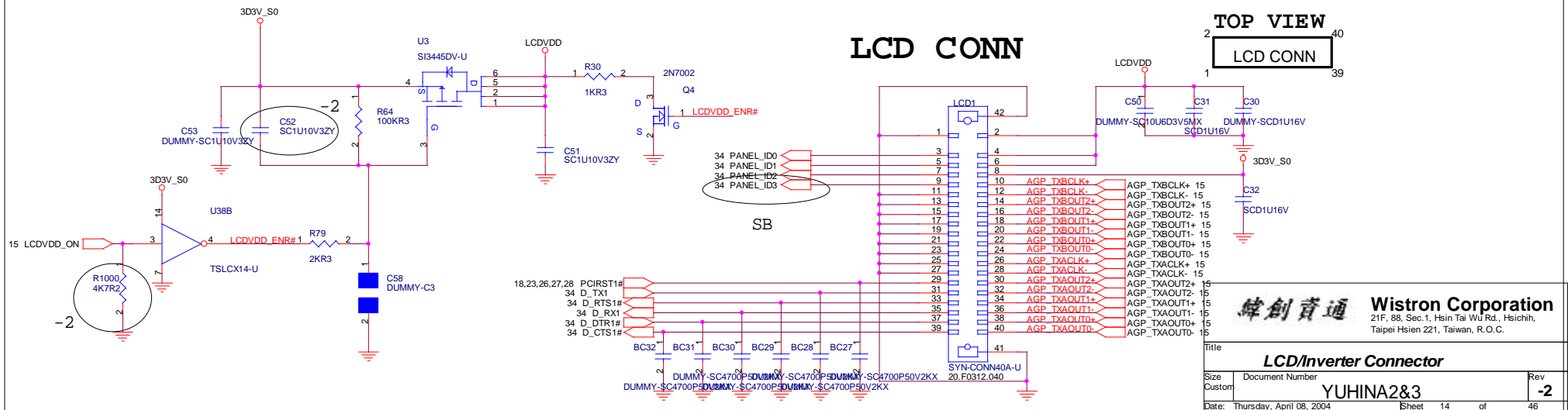
# LCD / INVERTER INTERFACE

TOP VIEW  
INV CONN  
1 2 39 40



## LCD CONN

TOP VIEW  
LCD CONN  
1 2 39 40

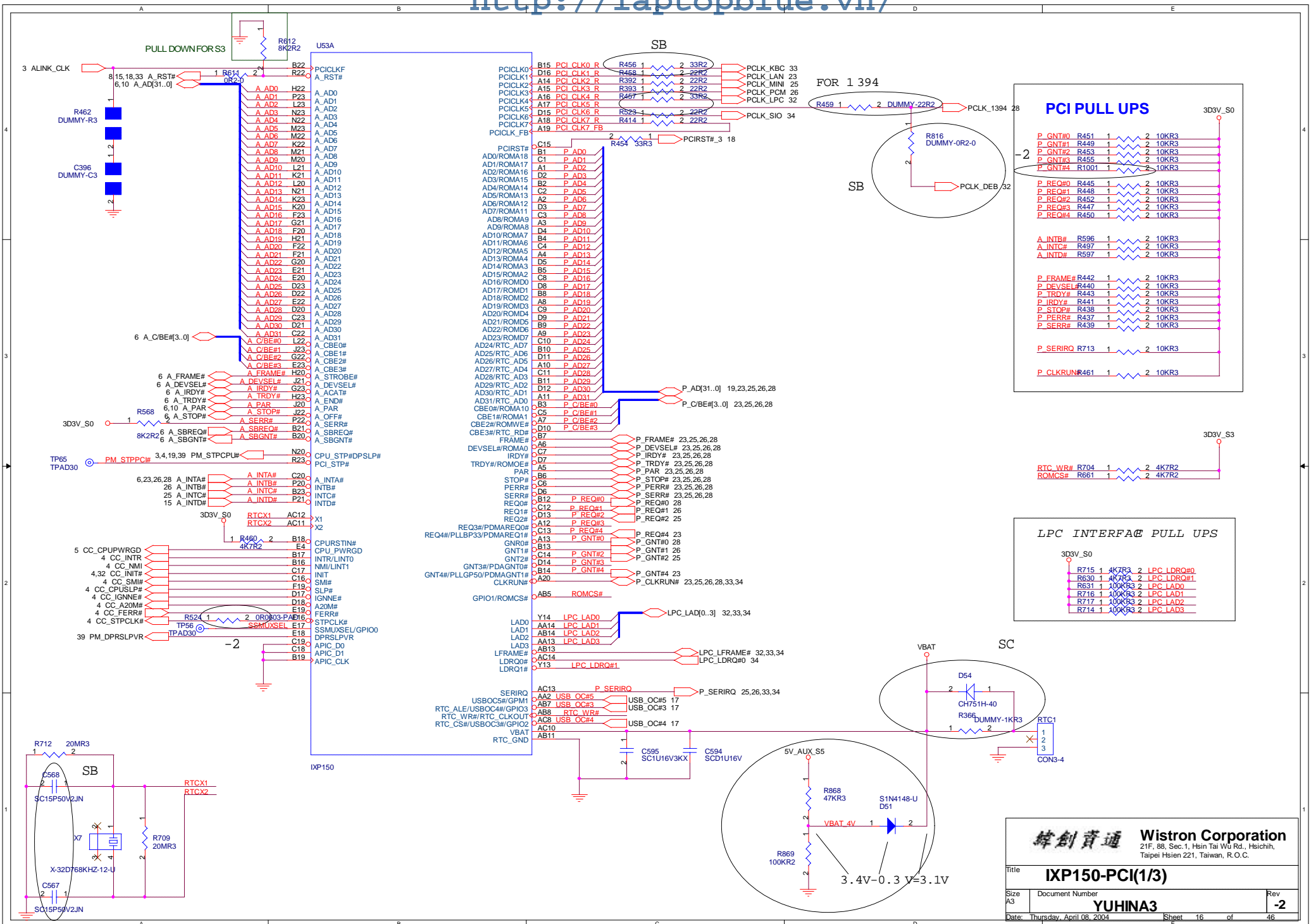


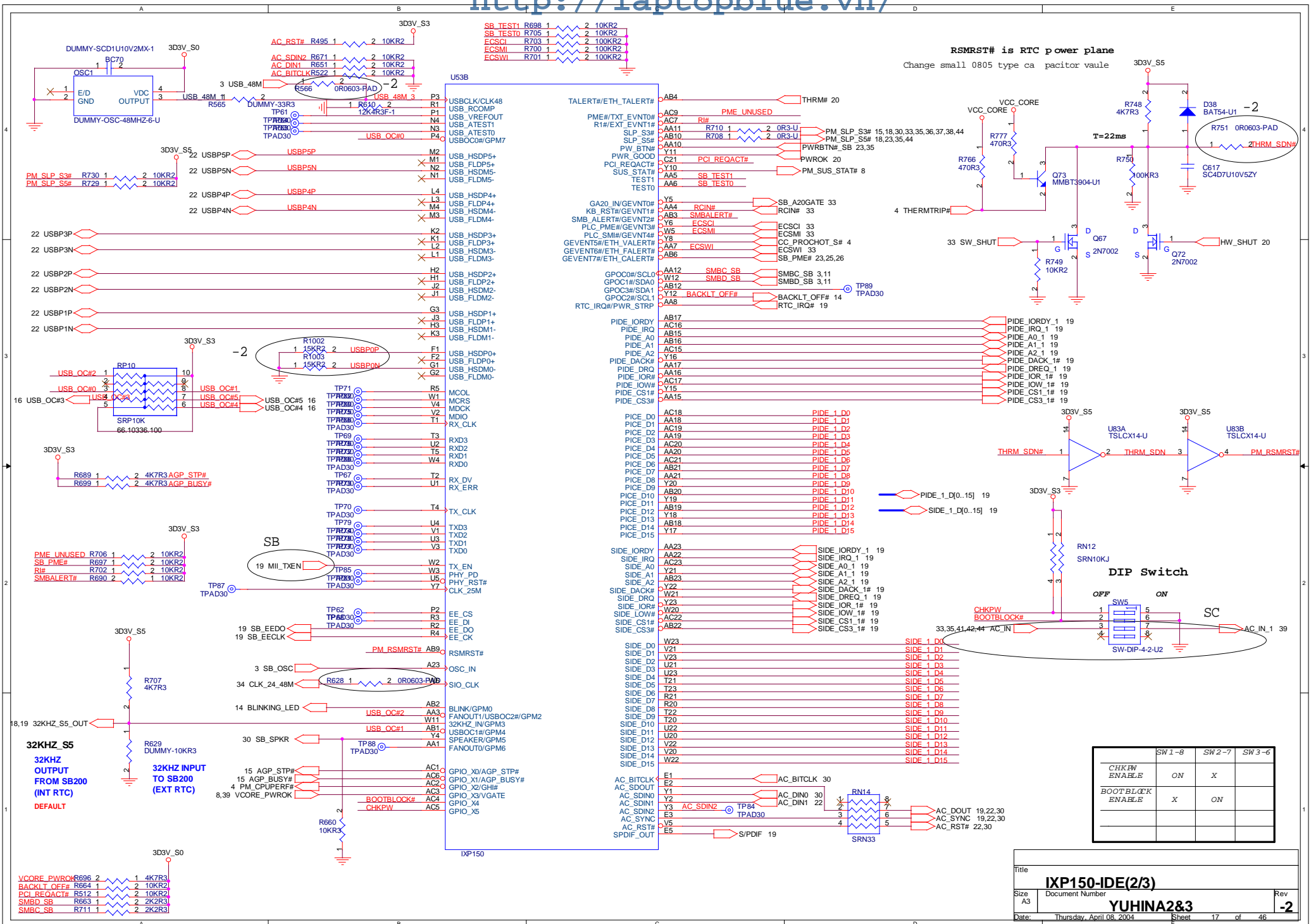
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

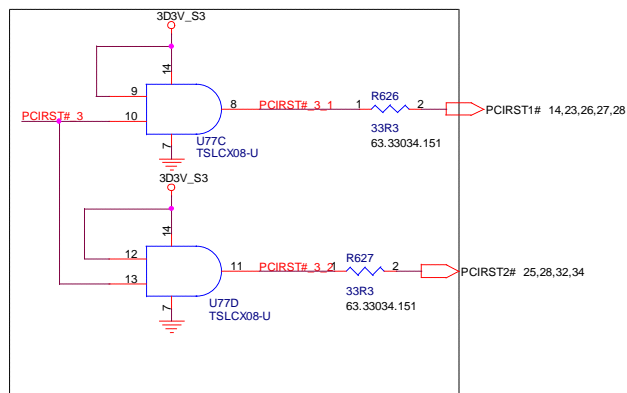
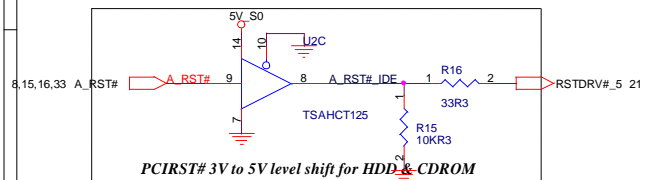
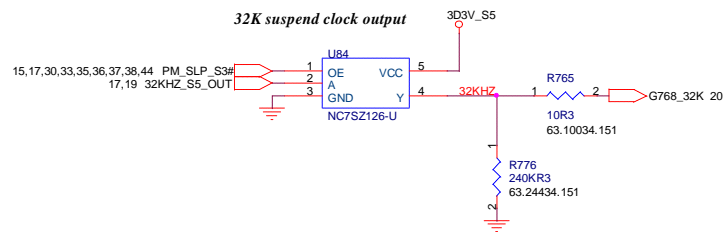
|                                        |                                         |                  |
|----------------------------------------|-----------------------------------------|------------------|
| Title<br><b>LCD/Inverter Connector</b> |                                         |                  |
| Size<br>Custom                         | Document Number<br><b>YUHINA2&amp;3</b> | Rev<br><b>-2</b> |
| Date: Thursday, April 08, 2004         | Sheet 14 of 46                          |                  |





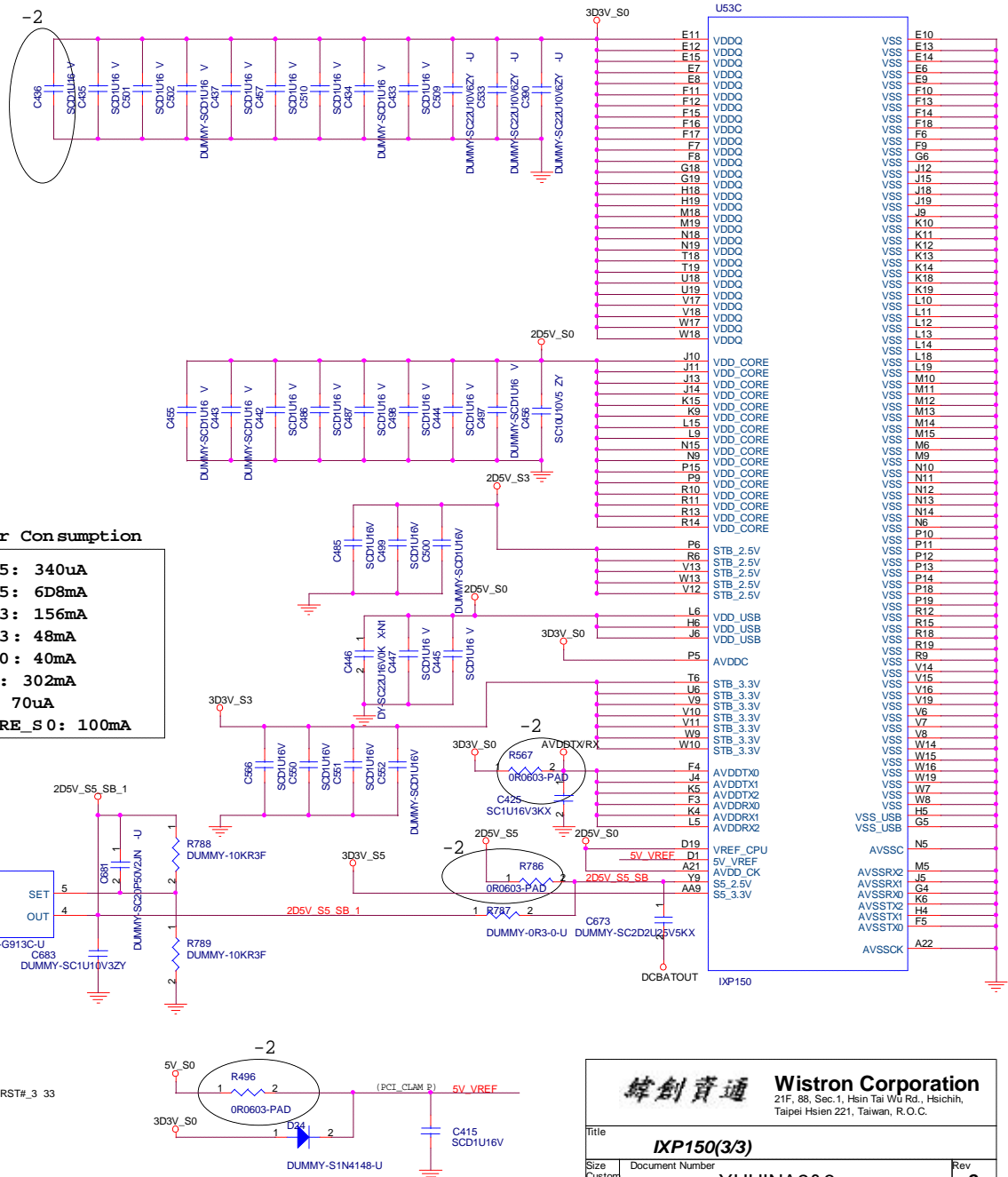
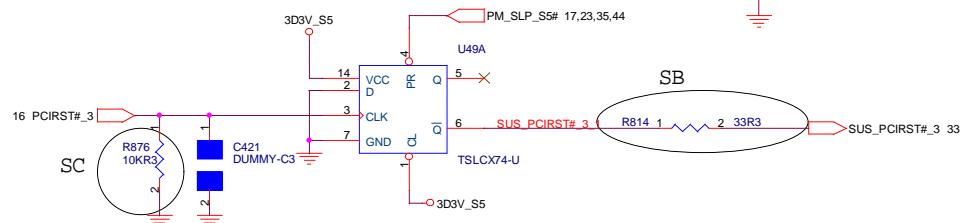
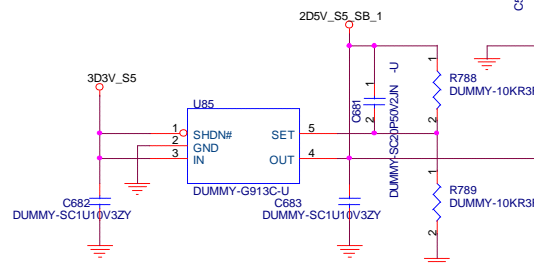






## Power Consumption

```
3D3V_S5: 340uA
2D5V_S5: 6D8mA
3D3V_S3: 156mA
2D5V_S3: 48mA
3D3V_S0: 40mA
2D5_S0: 302mA
5V_S0: 70uA
VCC_CORE_S0: 100mA
```



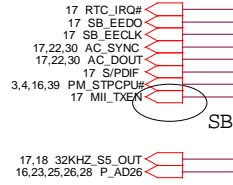
A

B

C

D

E



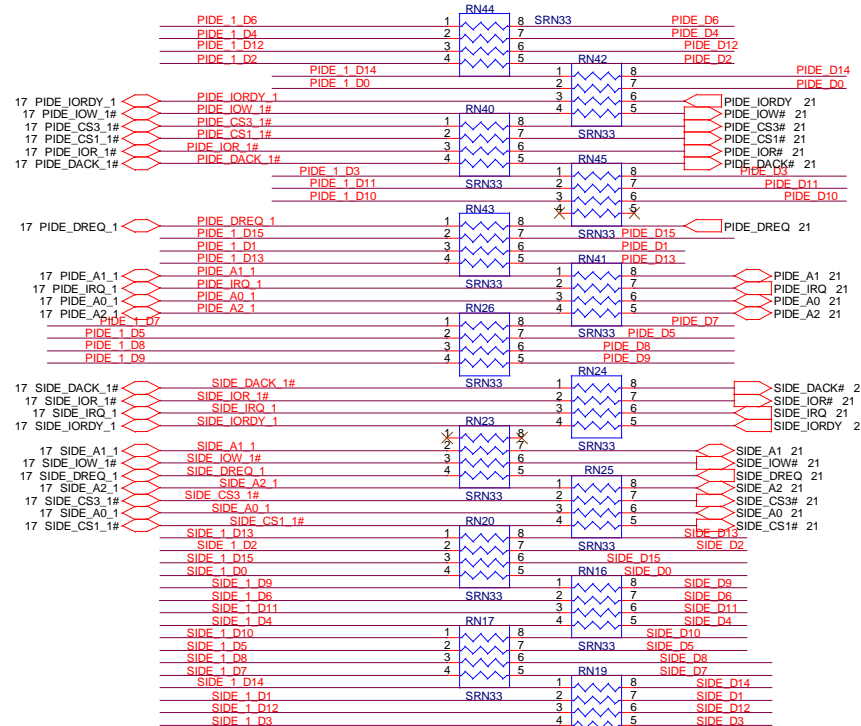
SB

## REQUIRED SYSTEM STRAPS

OVERLAP COMMON PADS  
FOR DUAL-OP  
RESISTORS

|            | ACPWON                   | EEDO                        | EECK                      | AC_SYNC                           | AC_SDOOUT                  | SPDIF_OUT            | CPU_STP#                     | 32KHZ_S5                                     | PCI_AD26                      | TX_EN                               |
|------------|--------------------------|-----------------------------|---------------------------|-----------------------------------|----------------------------|----------------------|------------------------------|----------------------------------------------|-------------------------------|-------------------------------------|
| STRAP HIGH | MANUAL PWR ON<br>DEFAULT | USE DEBUG STRAPS<br>DEFAULT | ROM ON PCI BUS<br>DEFAULT | INIT ACTIVE HIGH(AMD)<br>DEFAULT  | 33MHz NB BUS<br>DEFAULT    | SIO 24MHz<br>DEFAULT | ENABLE SPEED STEP<br>DEFAULT | 32KHZ OUTPUT FROM SB200 (INT RTC)<br>DEFAULT | BIOS use LPC cycle<br>DEFAULT | DISABLE CPU FREQ SETTING<br>DEFAULT |
| STRAP LOW  | AUTO PWR ON              | IGNORE DEBUG STRAPS         | ROM ON LPC BUS<br>DEFAULT | INIT ACTIVE LOW (PIII)<br>DEFAULT | HI SPEED A-LINK<br>DEFAULT | SIO 48MHz<br>DEFAULT | DISABLE SPEED STEP           | 32KHZ INPUT TO SB200 (EXT RTC)               | BIOS uSE FW Cycle             | ENABLE CPU FREQ SETTING             |

SB



PIDE\_1\_D[0..15] 17

SIDE\_1\_D[0..15] 17

PIDE\_D[0..15] 21

SIDE\_D[0..15] 21

A

B

C

D

E

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Title

**SB STRAPPING**

Size A3 Document Number

**YUHINA283**

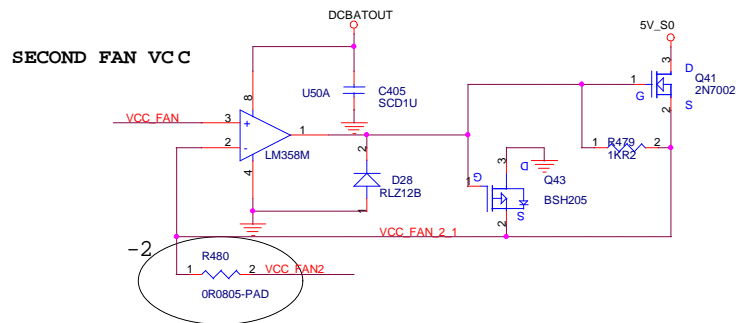
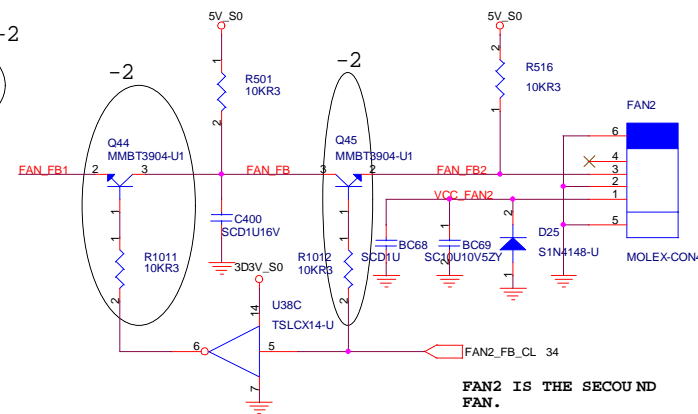
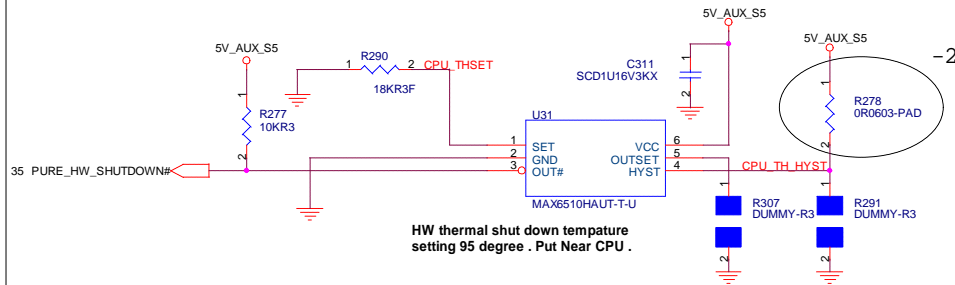
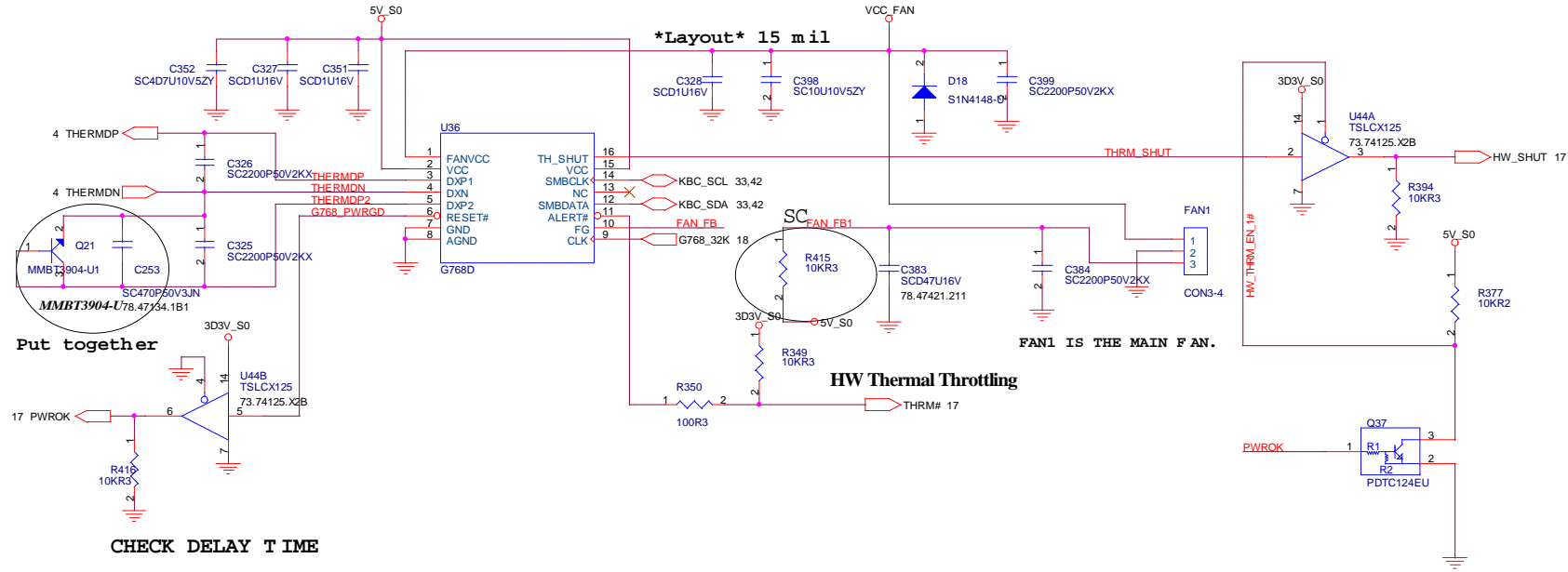
Date: Thursday, April 08, 2004

Rev

**-2**

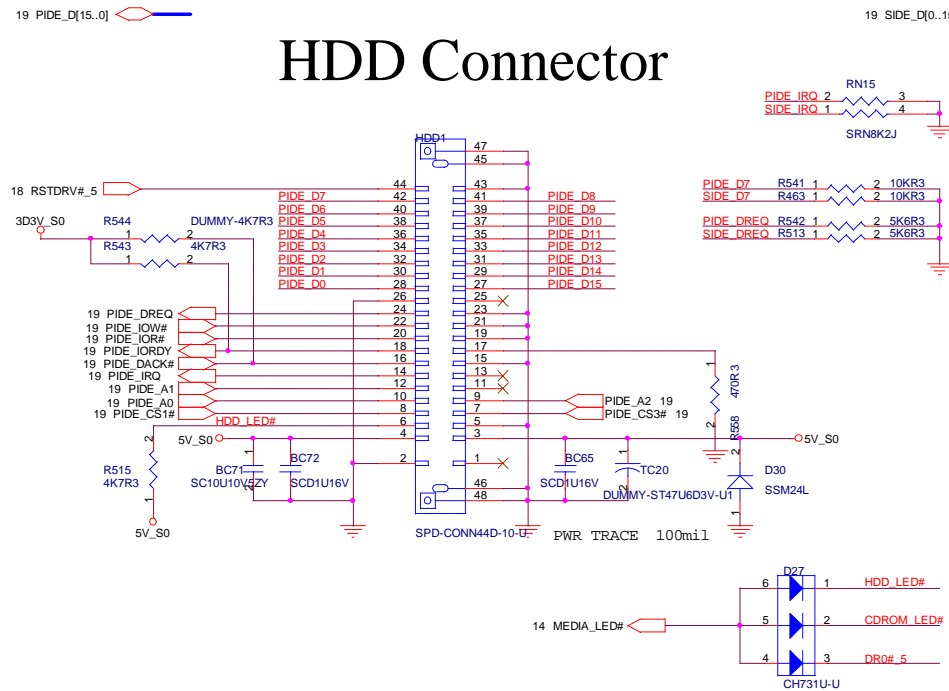
Sheet 19 of 46

<http://laptopblue.vn/>  
**G768D thermal sensor & Fan controller**



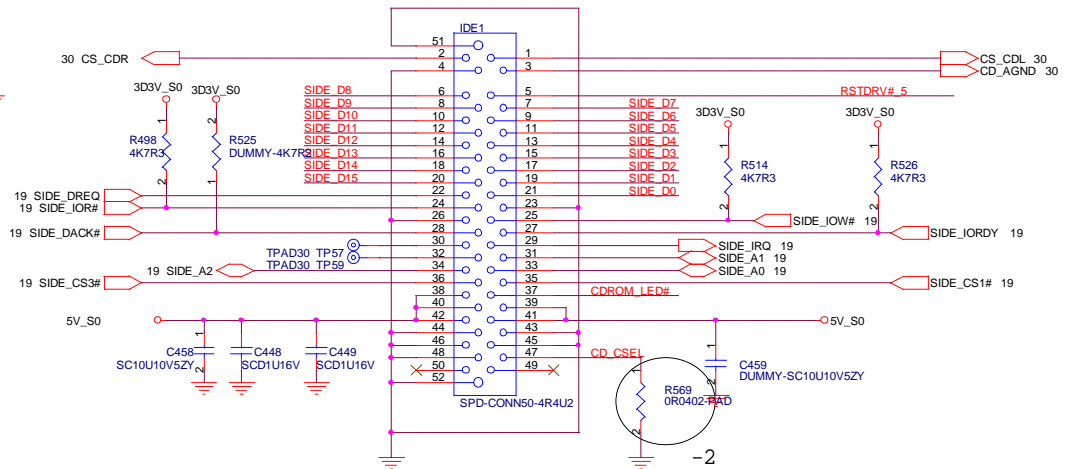


## HDD Connector

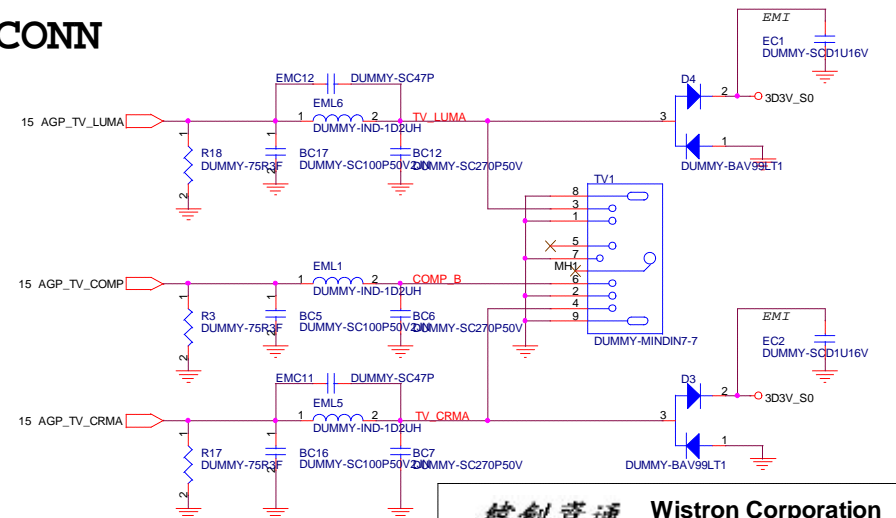
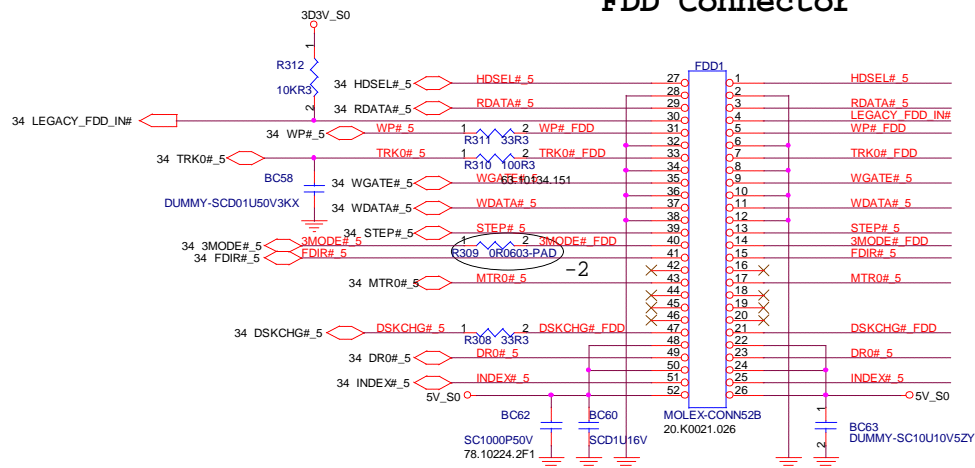


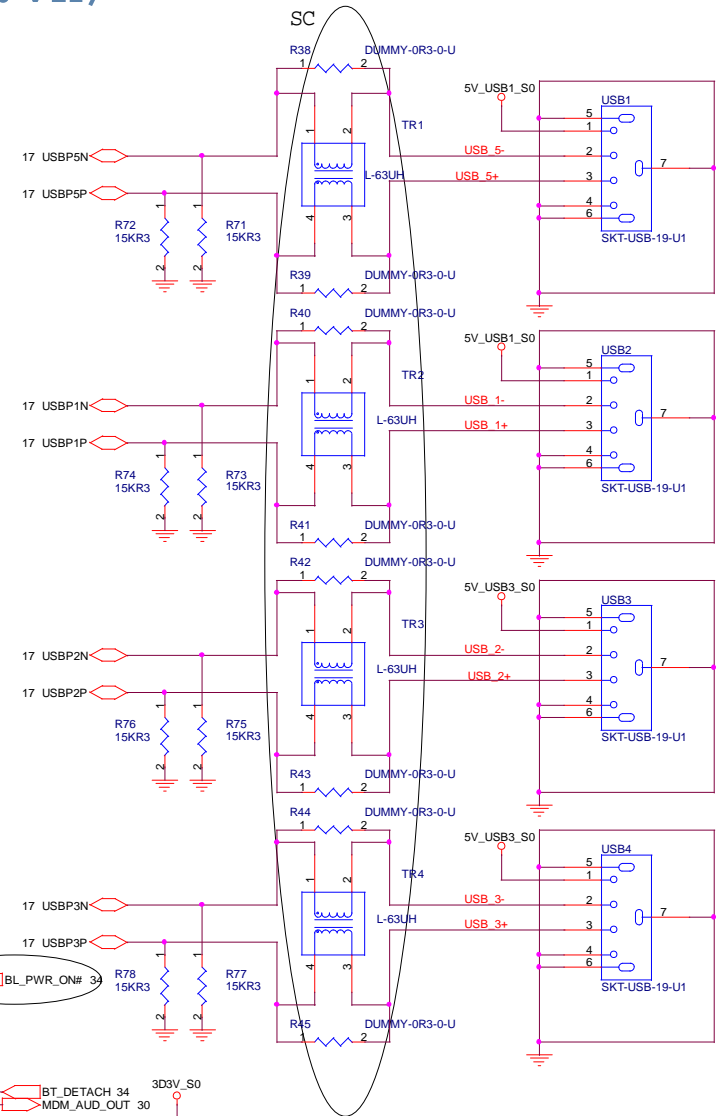
CHECK PIDE/SIDE DIAG# PIN

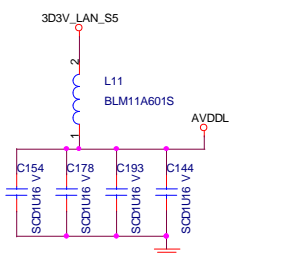
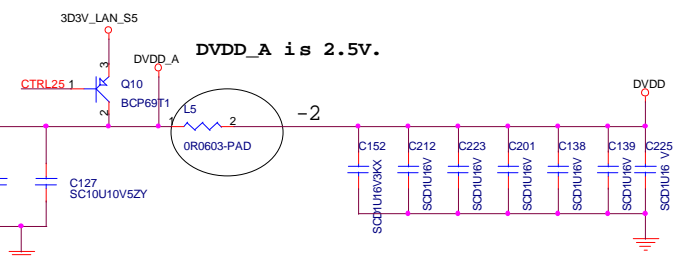
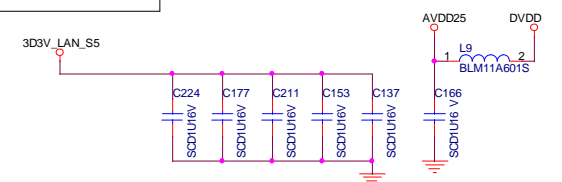
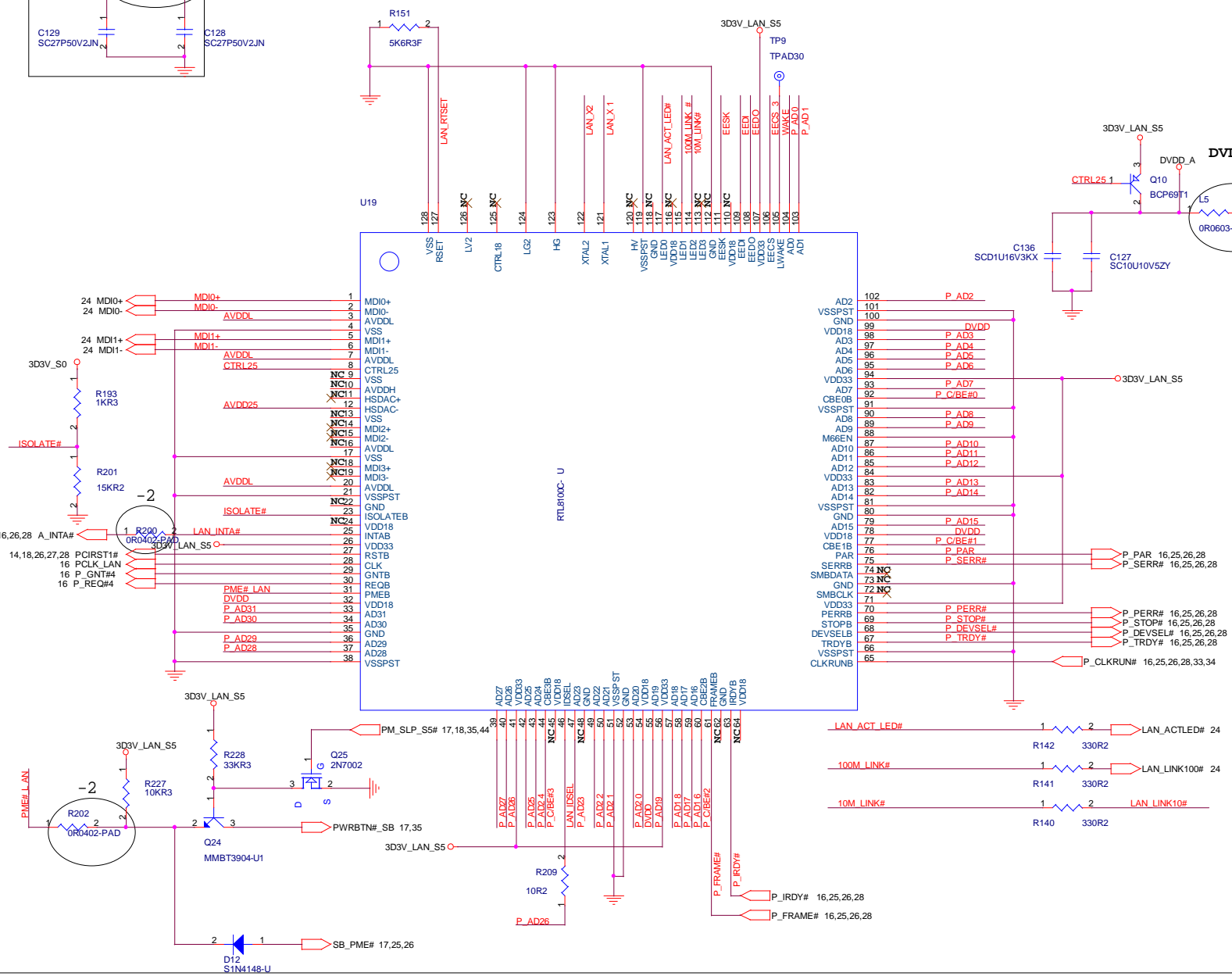
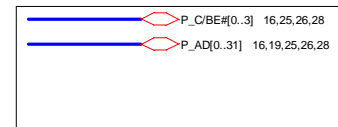
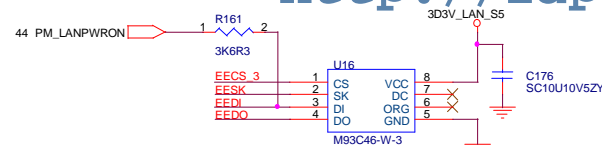
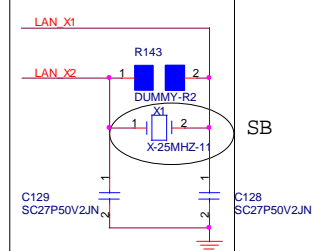
**TV CONN**



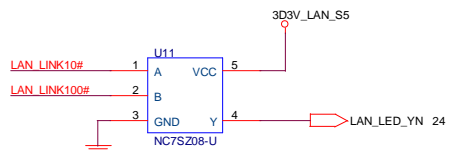
## FDD Connector



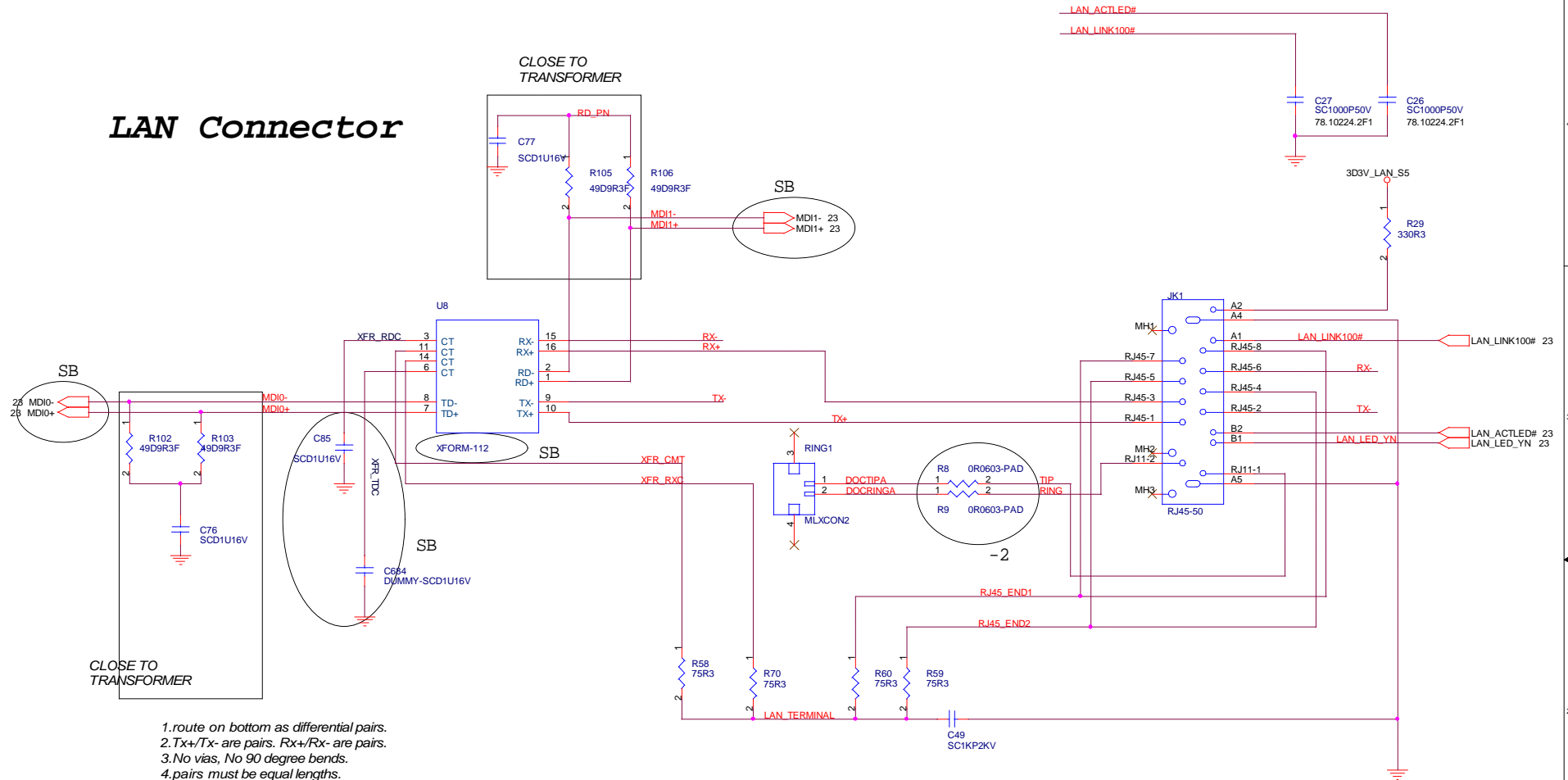




At RTL8100C (10/100)  
application, AVDDL is  
3.3V.



# LAN Connector

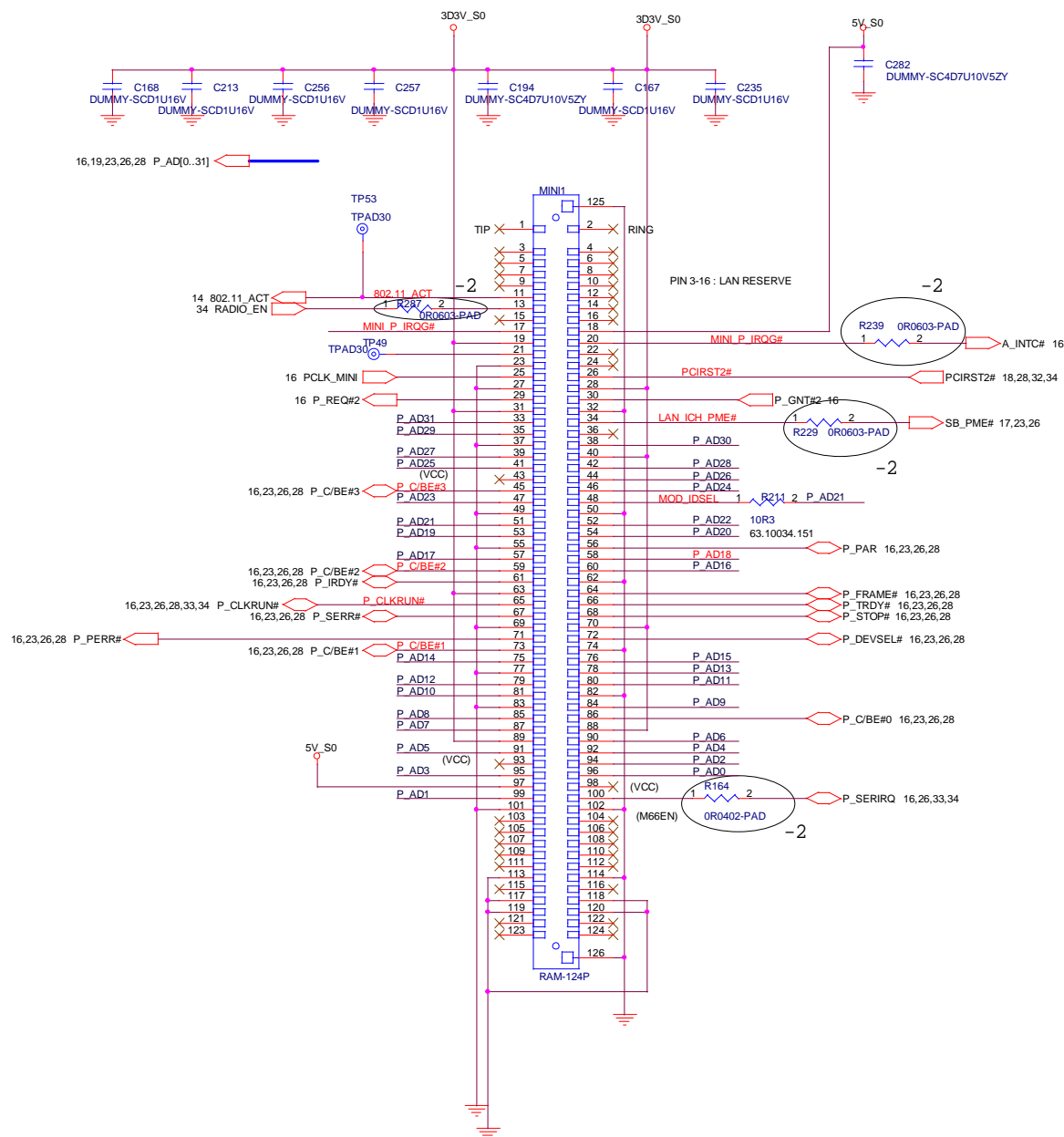


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

Green LED---Speed100:ON/Speed10:OFF  
Yellow LED---Link:ON ,TX/RX:Flash

## Mini PCI



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| Title |
|-------|
|-------|

**MINI-PCI**

Size

|                 |
|-----------------|
| Document Number |
|-----------------|

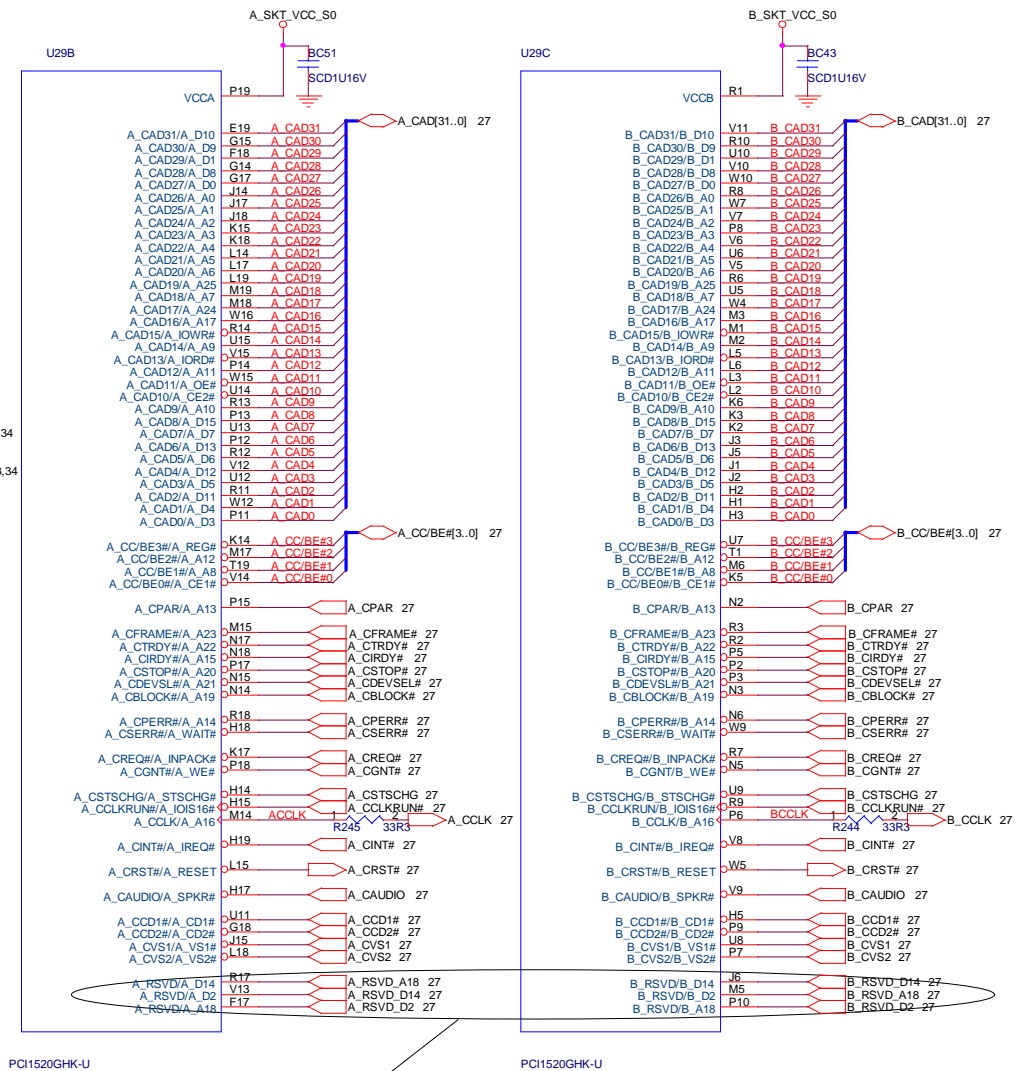
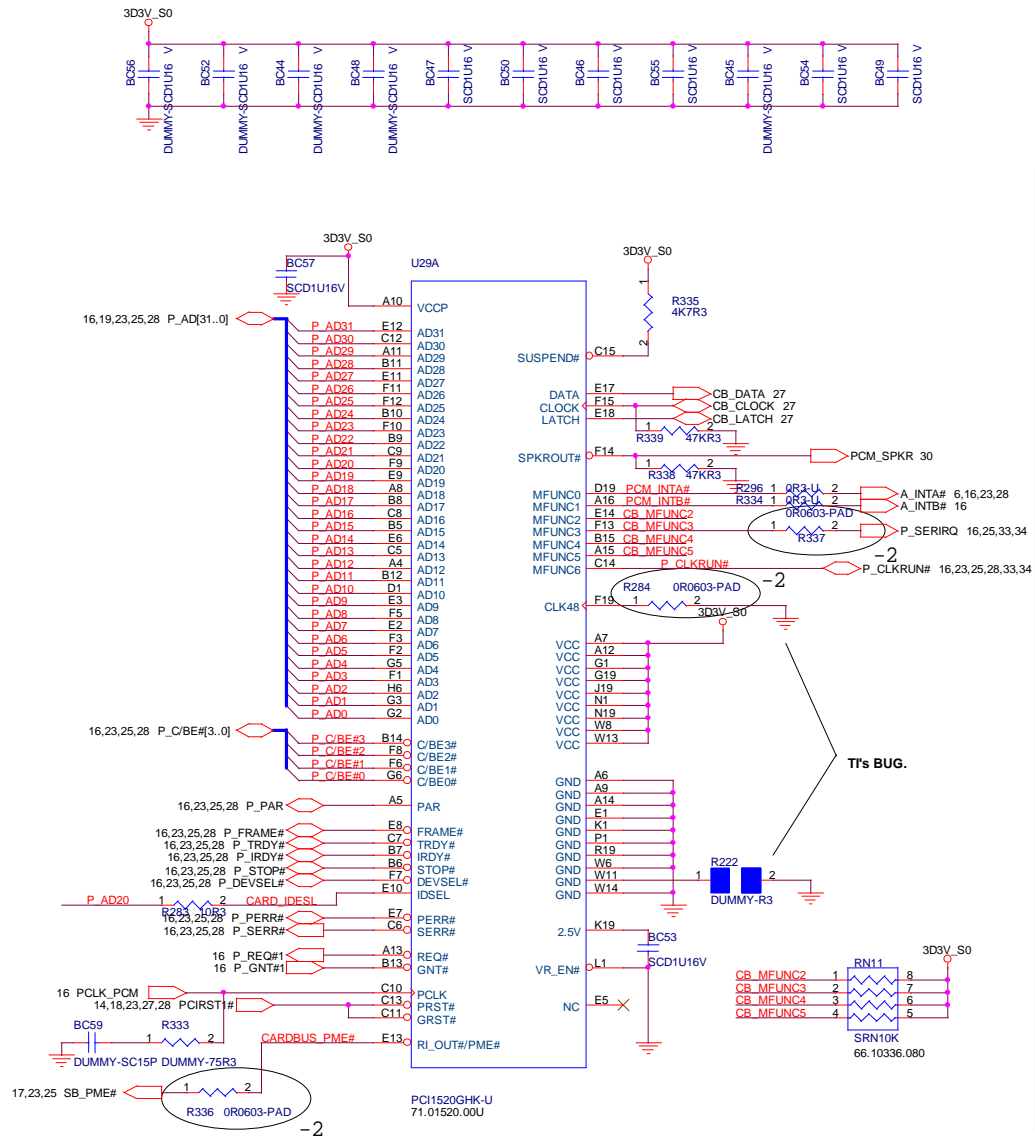
A3

YUHINA2&amp;3

|     |    |
|-----|----|
| Rev | -2 |
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Date: Thursday, April 08, 2004

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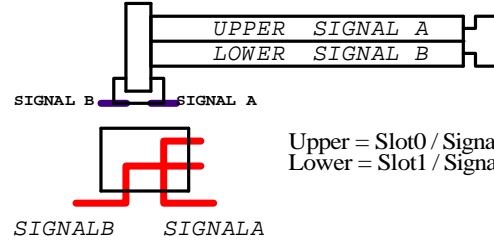
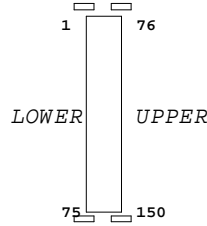


**Library Error !!**

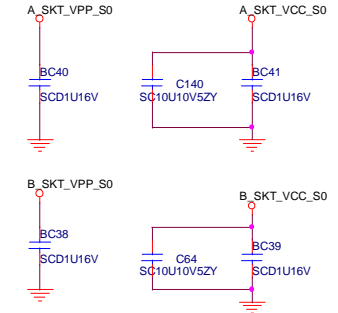
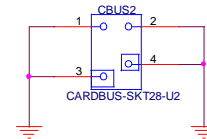
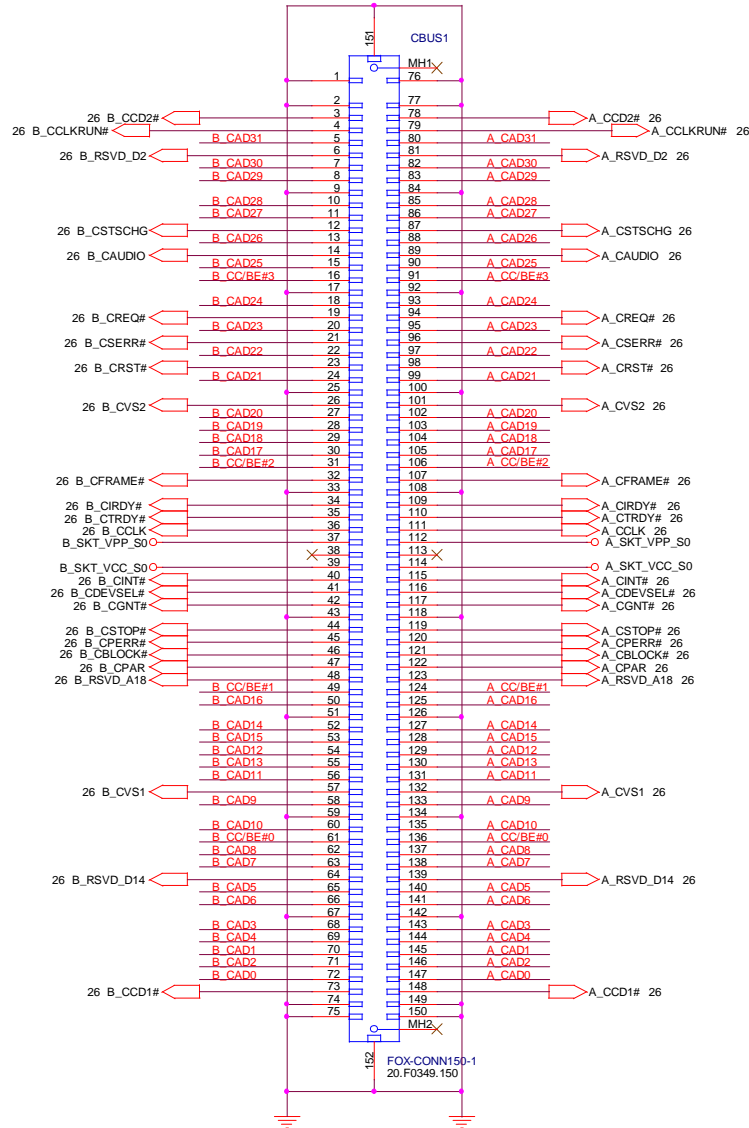
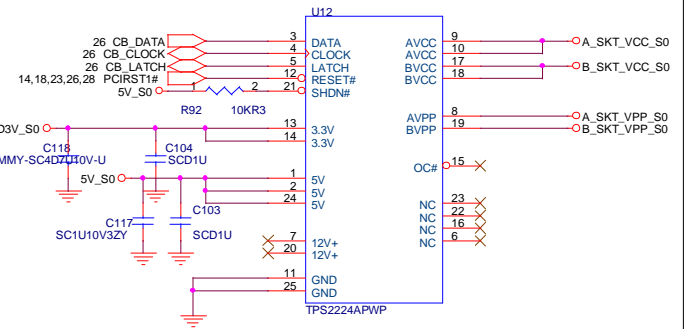
R17 - A\_A18      M5 - B\_A18  
V13 - A\_D14      P10 - B\_D2  
F17 - A\_D2

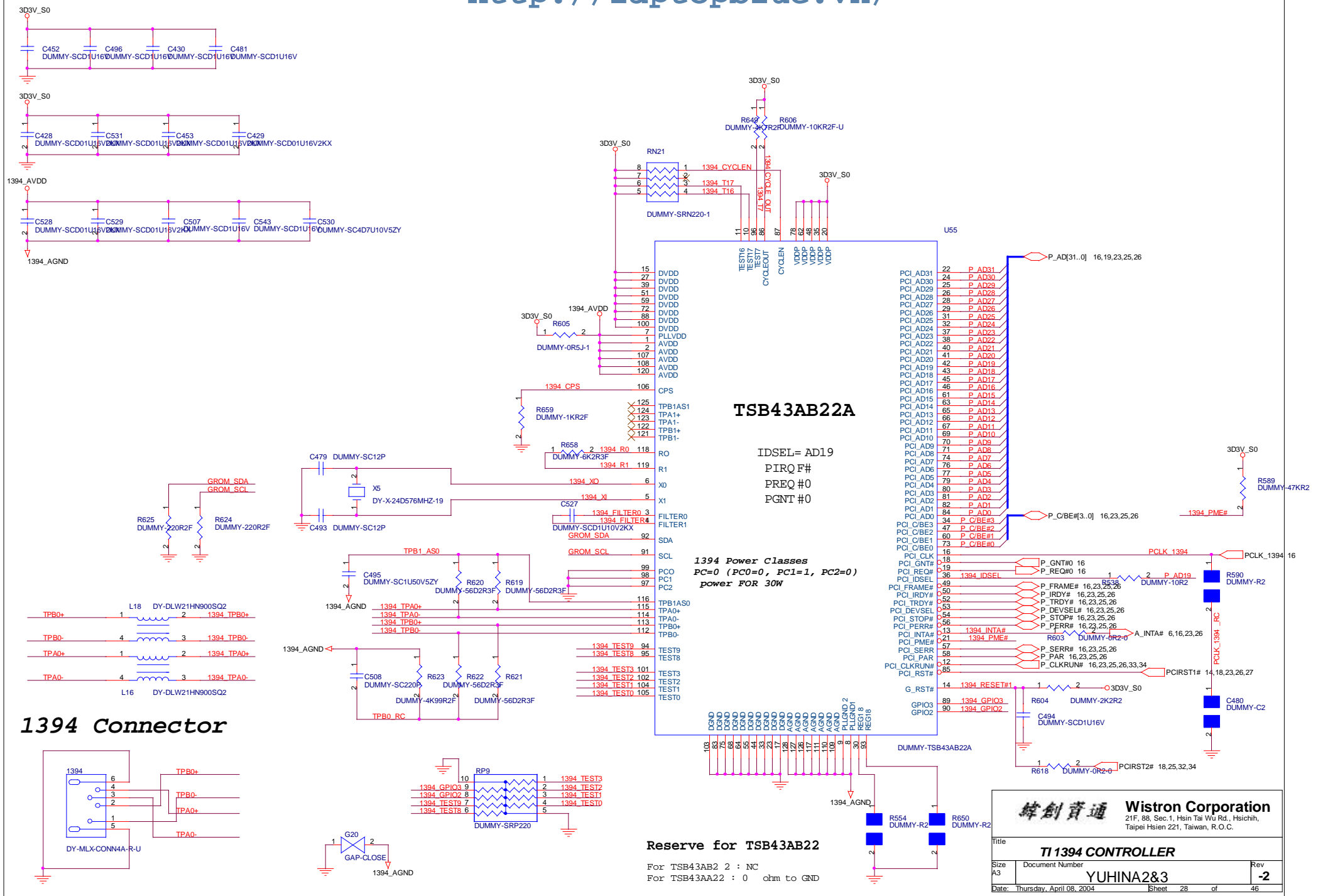


A\_CC/BE#[3..0] 26  
B\_CC/BE#[3..0] 26  
A\_CAD[31..0] 26  
B\_CAD[31..0] 26

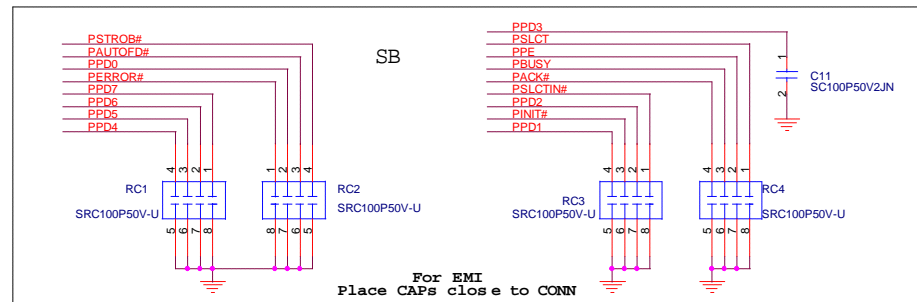
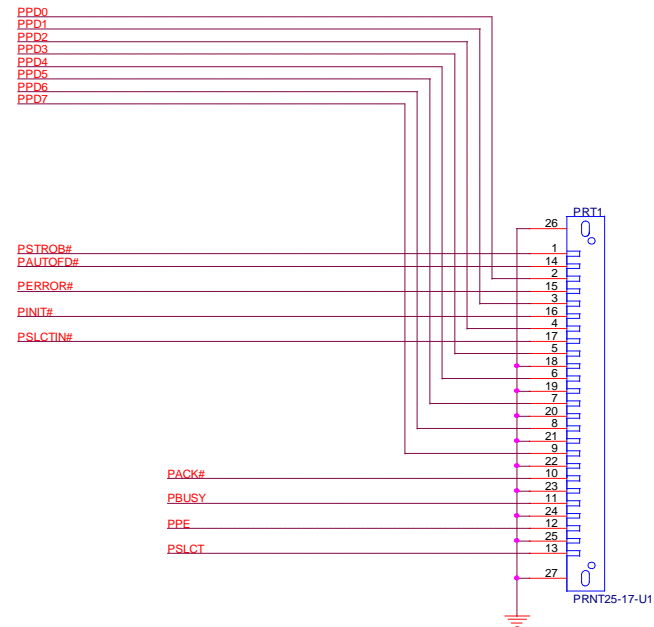
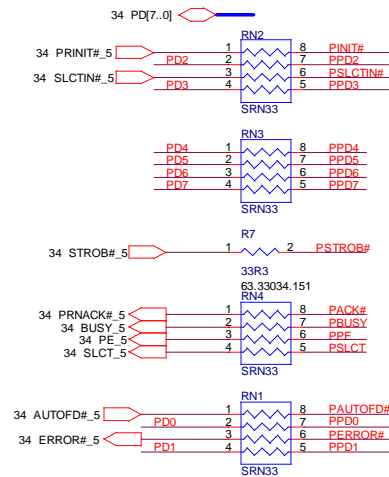
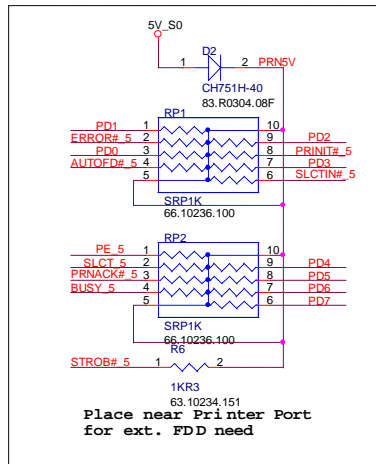


Upper = Slot0 / Signal A = Conn B  
Lower = Slot1 / Signal B = Conn A



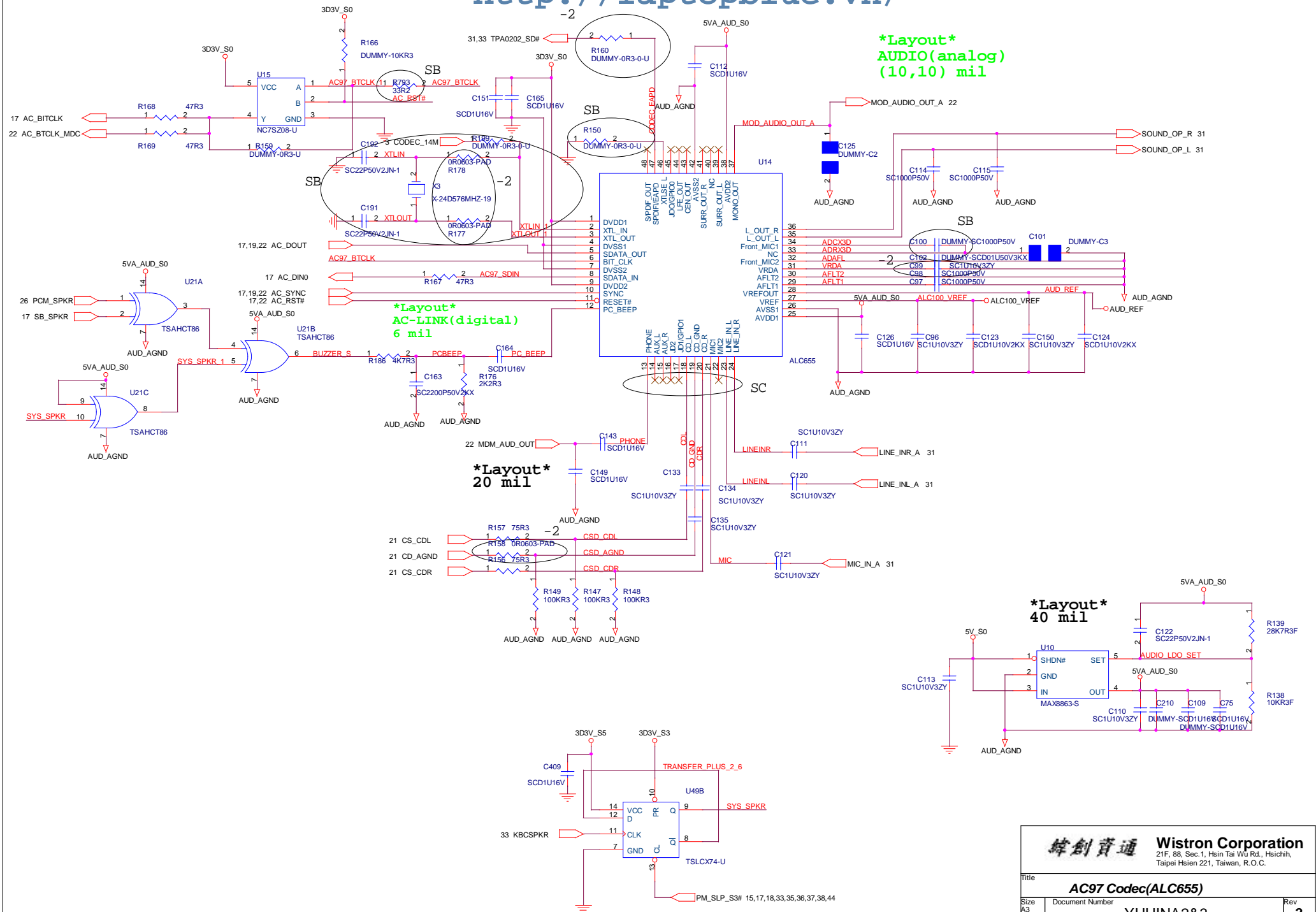


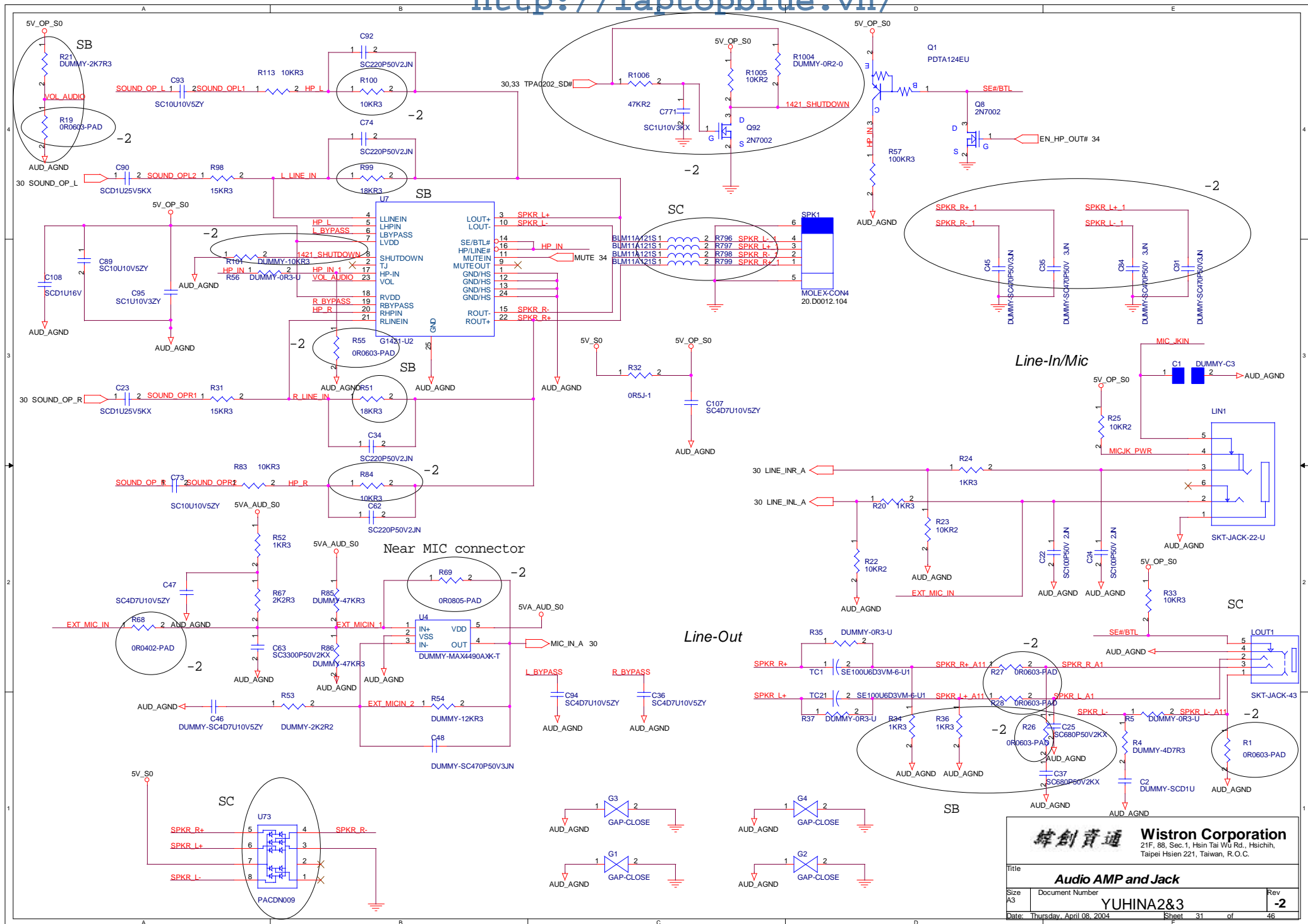
# PRINTER PORT

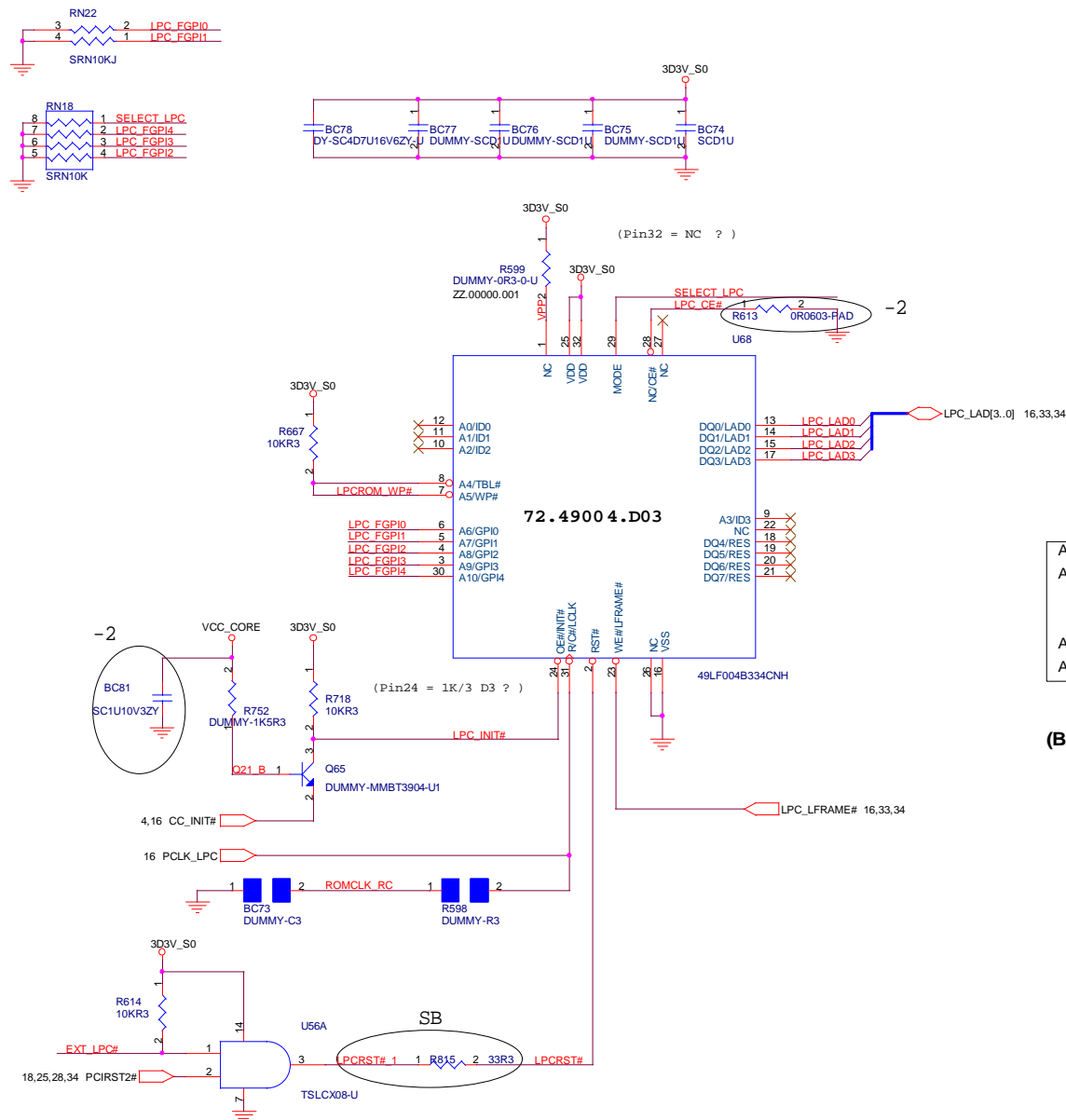


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Taipei Hsien 221, Taiwan, R.O.C.

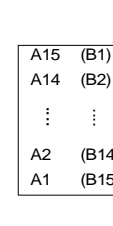
|                                |                                         |                  |
|--------------------------------|-----------------------------------------|------------------|
| Title<br><b>Parallel Port</b>  |                                         |                  |
| Size<br>A3                     | Document Number<br><b>YUHINA2&amp;3</b> | Rev<br><b>-2</b> |
| Date: Thursday, April 08, 2004 | Sheet 29                                | of 46            |





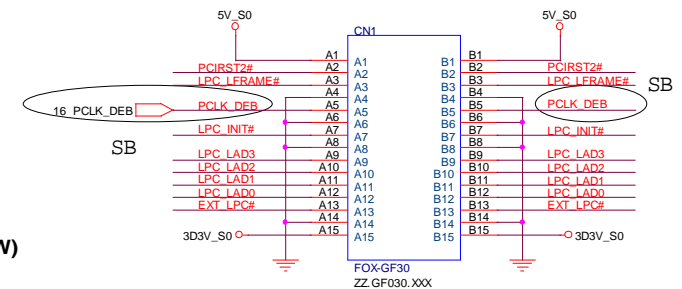


**TOP VIEW**



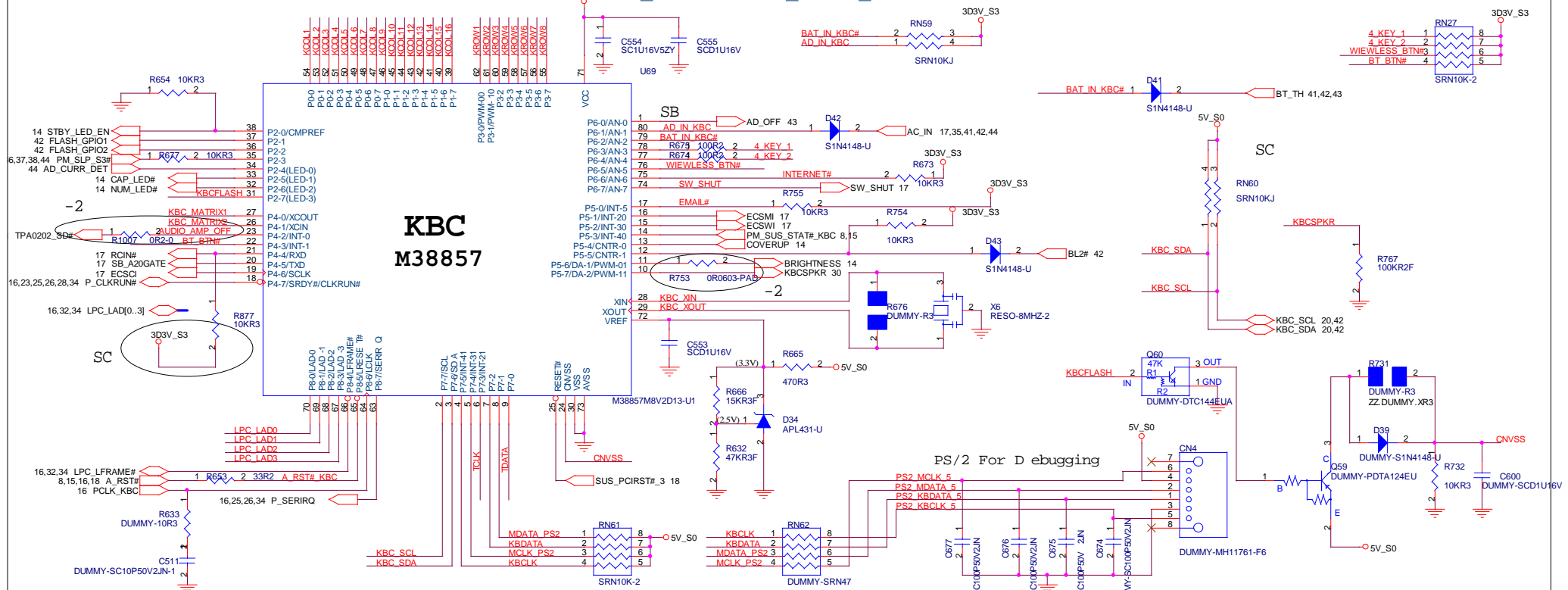
**(BOTTOM VIEW)**

## GOLDEN FINGER FOR DEBUG BOARD

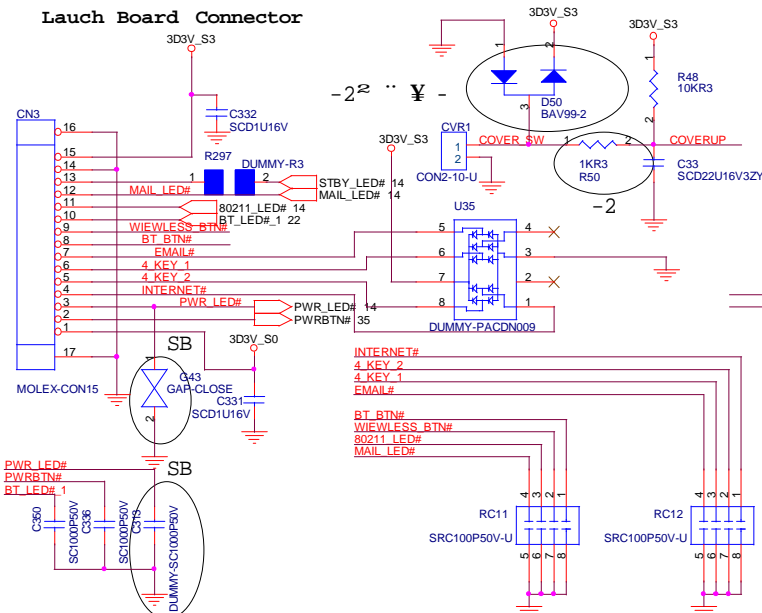


PLCC 32pin ST: 72.50040.003  
PLCC 32pin SST:  
72.49004.B03

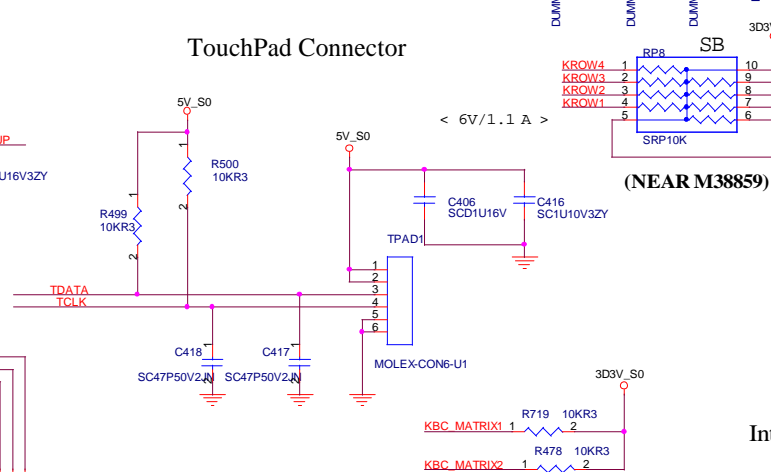




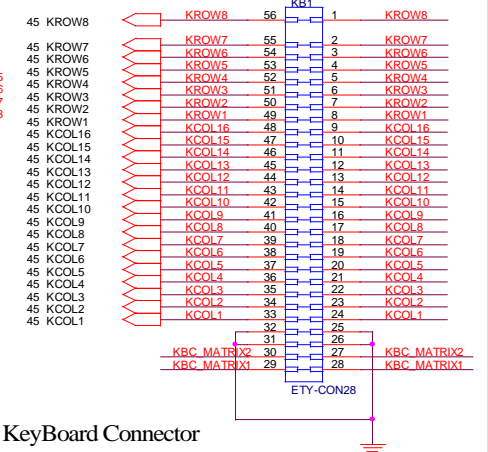
## Lauch Board Connector



## TouchPad Connector



### Internal KeyBoard Connector

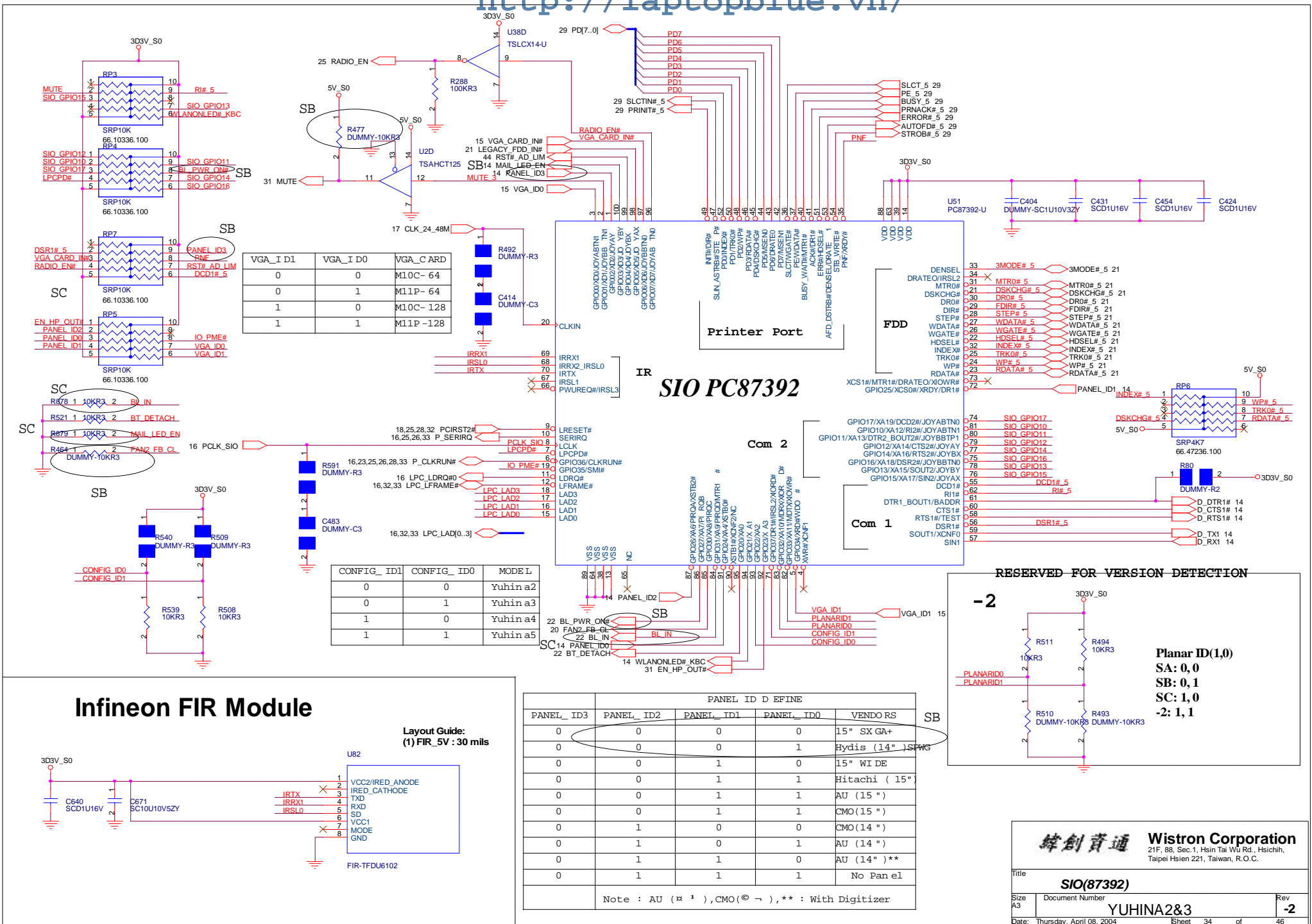
Keyboard matrix

|          |      |        |      |        |
|----------|------|--------|------|--------|
|          | US   | Europe | Jap  | Others |
| MATRI X1 | HIGH | LOW    | HIGH | LOW    |
| MATRI X2 | HIGH | HIGH   | LOW  | LOW    |

緯創資通

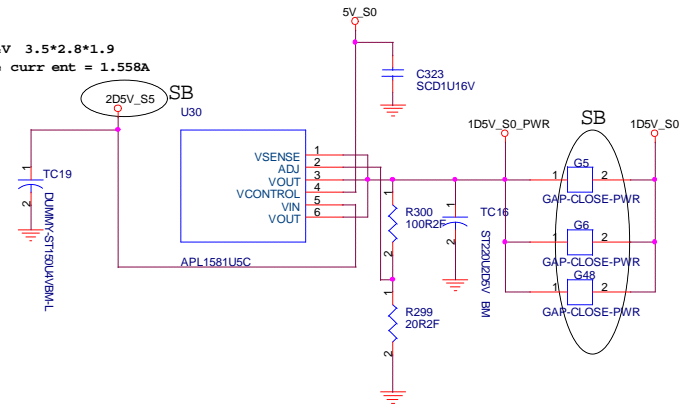
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Taipei Hsien 221, Taiwan, R.O.C.

|                                |                 |    |           |
|--------------------------------|-----------------|----|-----------|
| Title                          |                 |    |           |
| <b>KBC(38857)</b>              |                 |    |           |
| Size<br>A3                     | Document Number |    | Rev       |
|                                | YUHINA2&3       |    | <b>-2</b> |
| Date: Thursday, April 08, 2004 | Sheet           | 33 | of 46     |

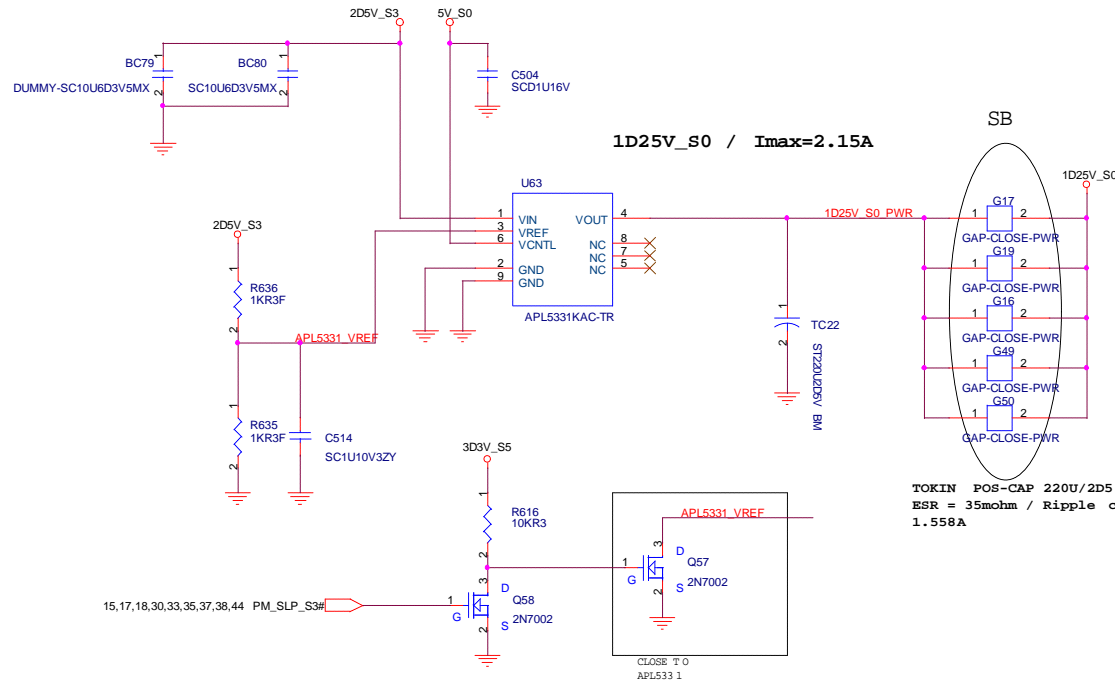




TOKIN POS-CAP 150U/4V 3.5\*2.8\*1.9  
ESR = 35mohm / Ripple current = 1.558A



TOKIN POS-CAP 220U/2D5 3.5\*2.8\*1.9  
ESR = 35mohm / Ripple current = 1.558A



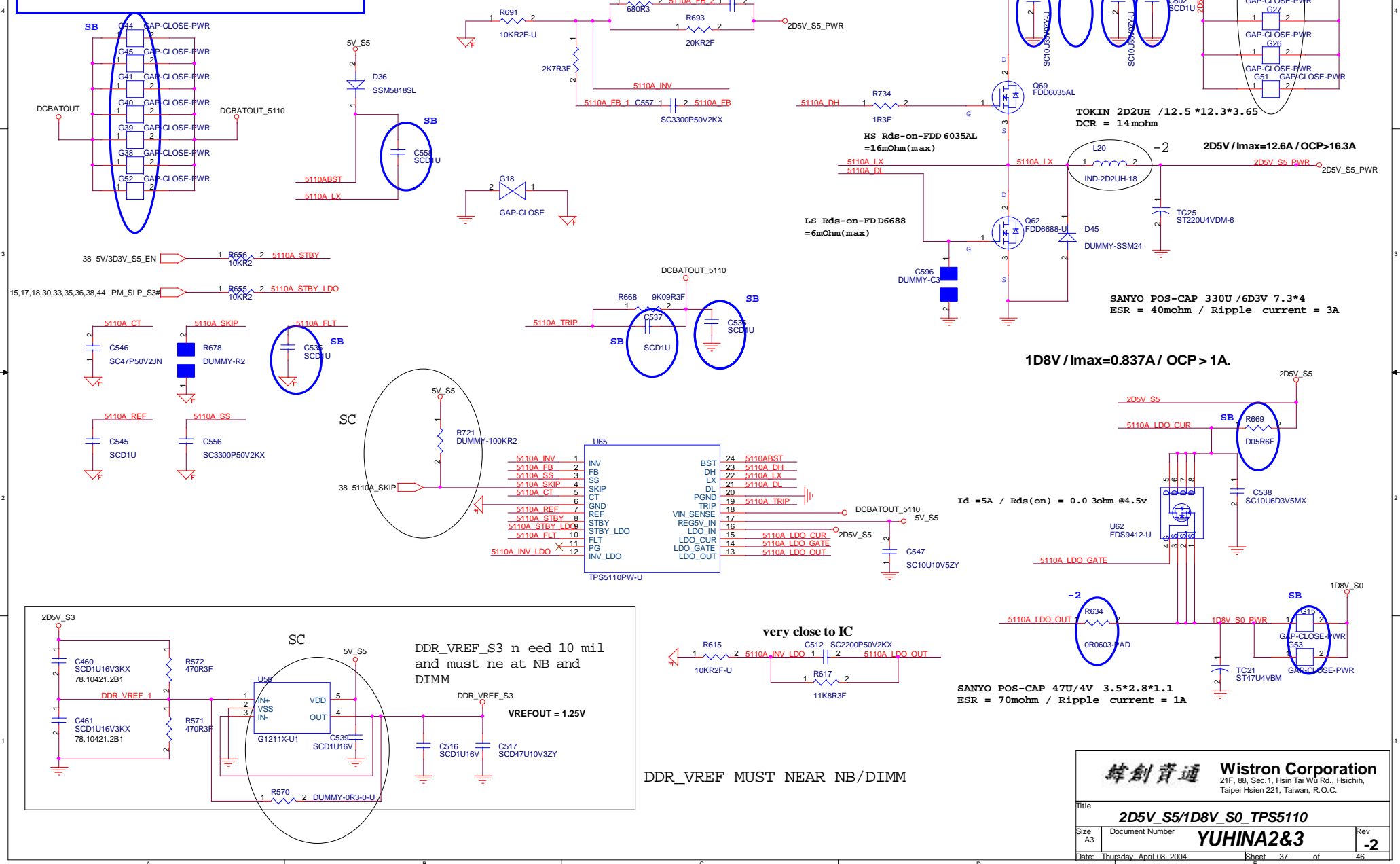
TOKIN POS-CAP 220U/2D5 3.5\*2.8\*1.9  
ESR = 35mohm / Ripple current = 1.558A

# TI TPS5110 for 2.5V and 1.8V

CT = 47pF/300KHz

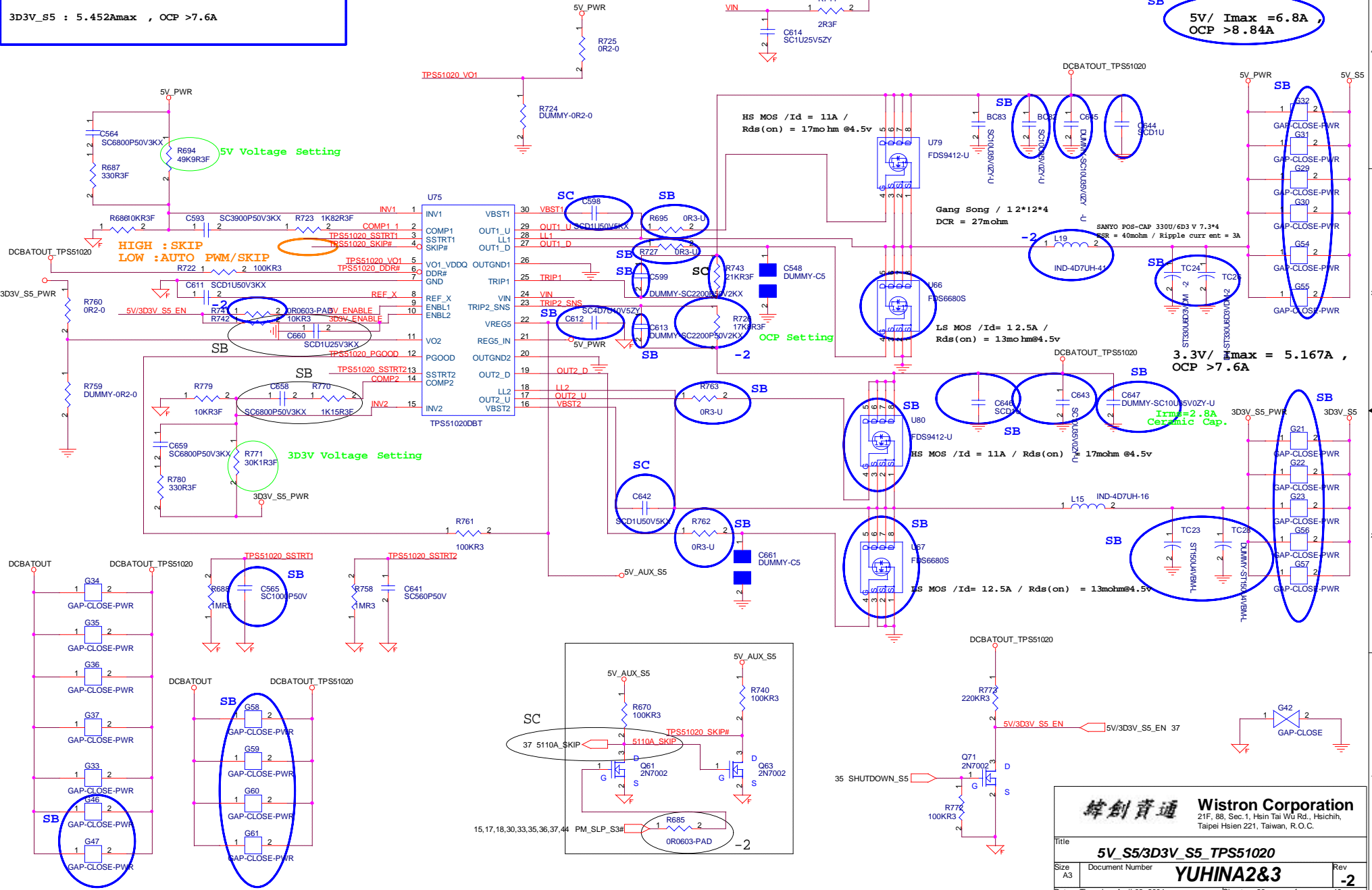
2D5V\_S5: 12.6Amax , OCP > 16.3A

1D8V\_S0: 0.837Amax , OCP > 1A



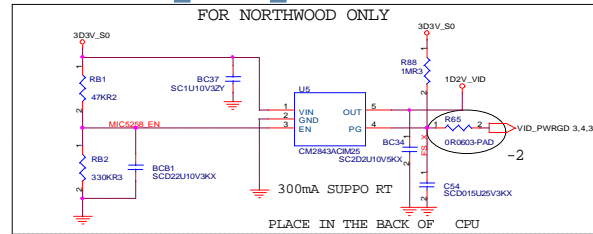
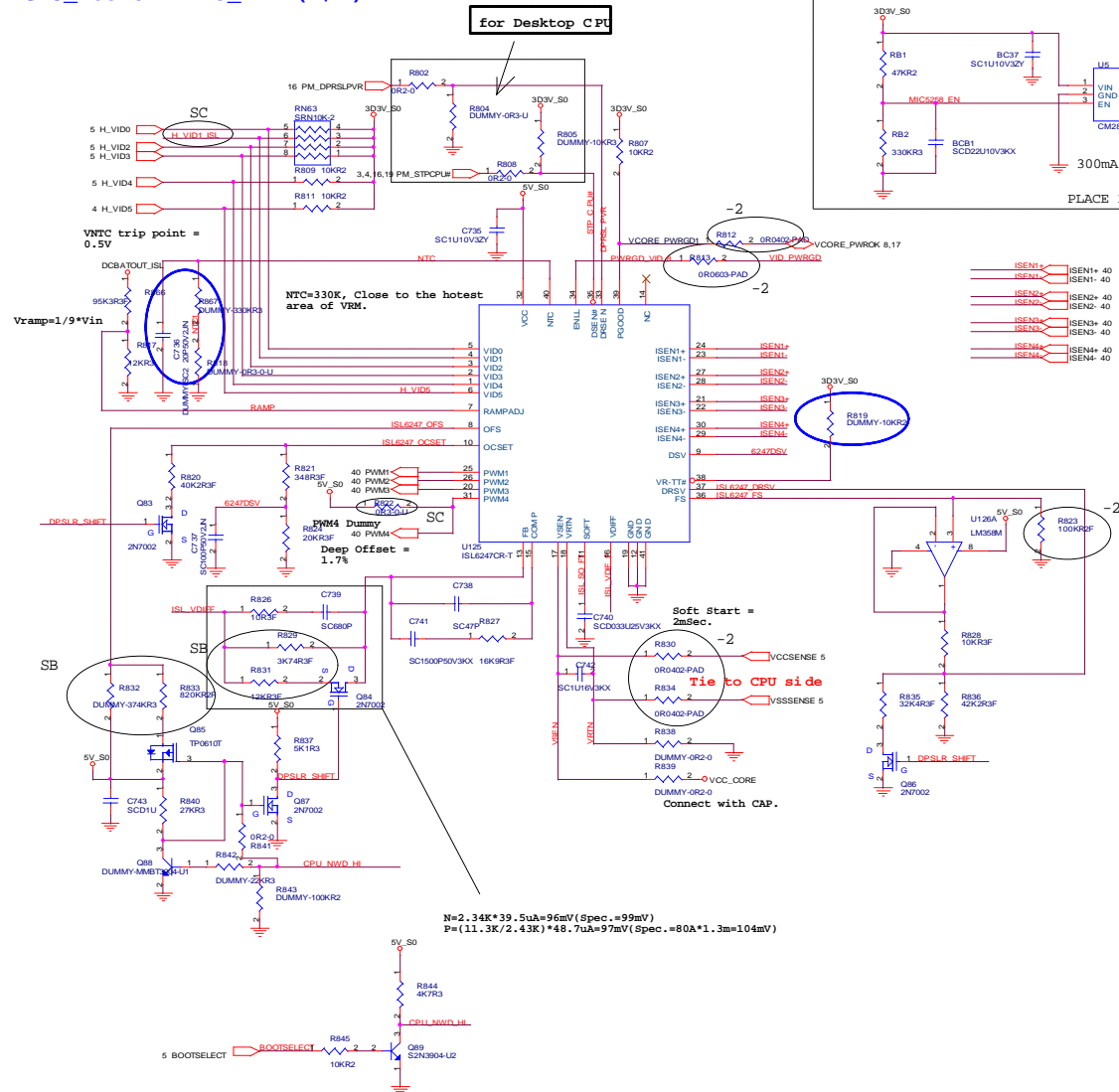
# TI TPS51020 for 5V and 3D3V

SSTRT2 & SSTRT1 = 1M ohm / 270KHz  
 5V\_S0 : 8.625Amax , OCP > 11.2A  
 3D3V\_S5 : 5.452Amax , OCP > 7.6A





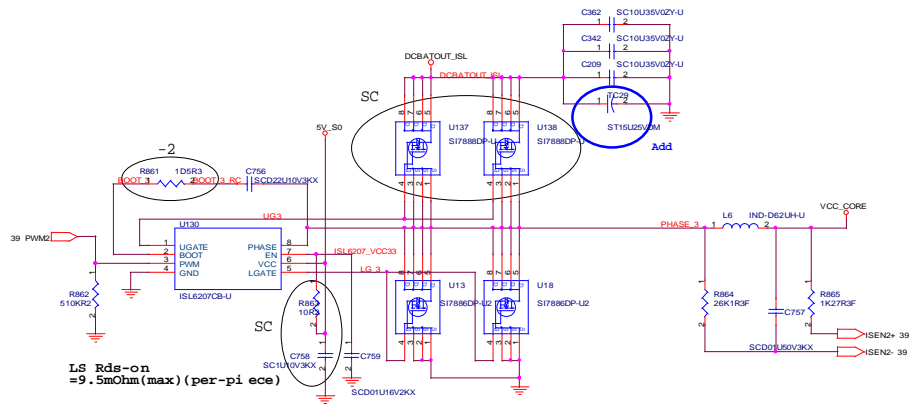
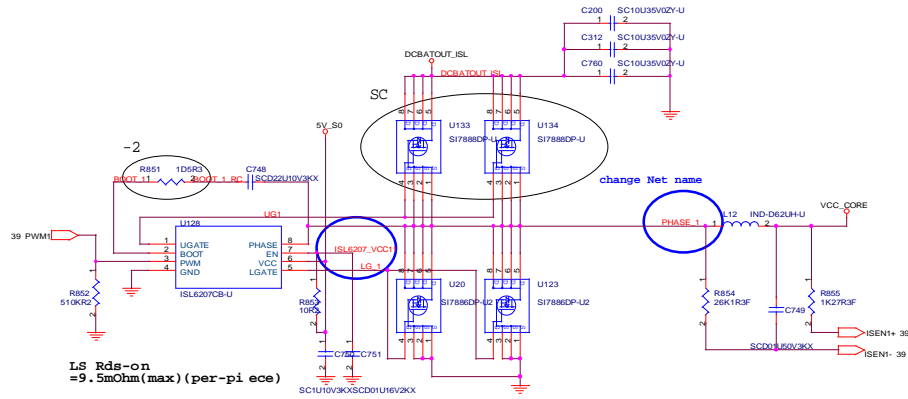
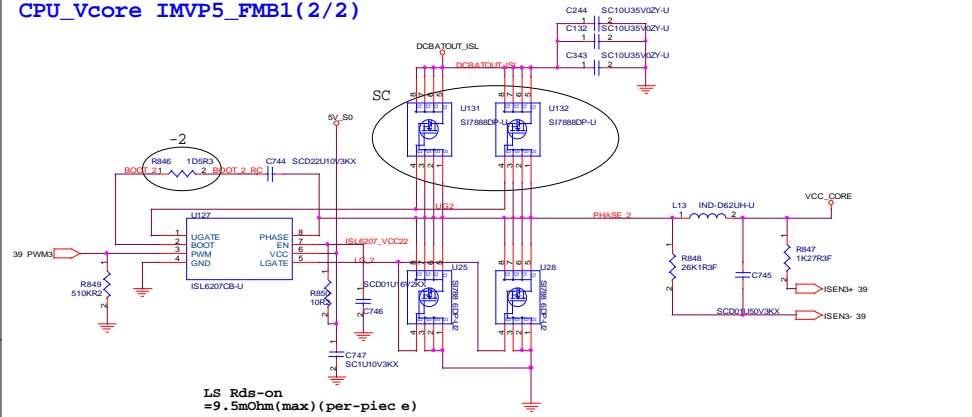
## CPU\_Vcore IMVP5\_FMB1(1/2)



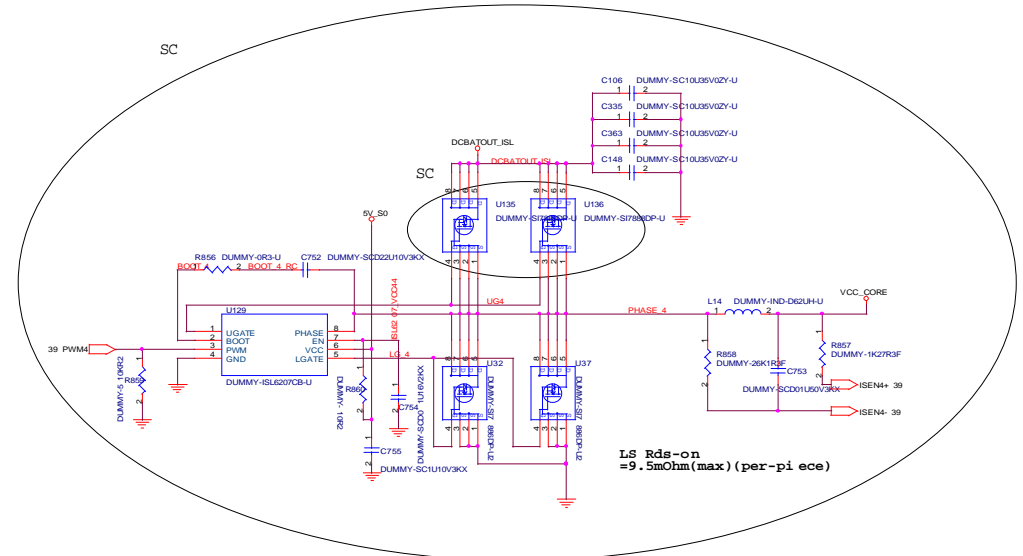
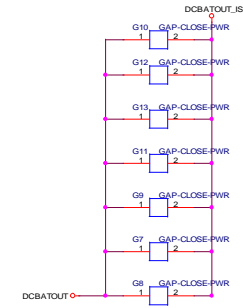
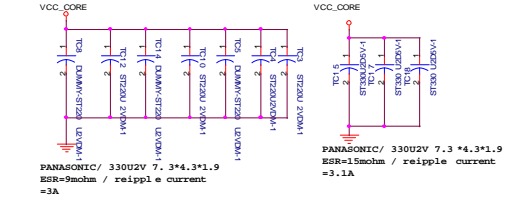
| Voltage Identification Codes |      |      |      |      |      |        |
|------------------------------|------|------|------|------|------|--------|
| VID5                         | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC   |
| X                            | 1    | 1    | 1    | 1    | 1    | OFF    |
| 0                            | 0    | 1    | 0    | 0    | 0    | 0.8375 |
| 1                            | 0    | 1    | 0    | 0    | 1    | 0.8500 |
| 0                            | 0    | 1    | 0    | 0    | 1    | 0.8625 |
| 1                            | 0    | 0    | 1    | 0    | 0    | 0.8750 |
| 0                            | 0    | 1    | 0    | 0    | 0    | 0.8875 |
| 1                            | 0    | 0    | 1    | 1    | 1    | 0.9000 |
| 0                            | 0    | 0    | 1    | 1    | 1    | 0.9125 |
| 1                            | 0    | 0    | 1    | 1    | 0    | 0.9250 |
| 0                            | 0    | 0    | 1    | 1    | 0    | 0.9375 |
| 1                            | 0    | 0    | 1    | 0    | 1    | 0.9500 |
| 0                            | 0    | 0    | 1    | 0    | 1    | 0.9625 |
| 1                            | 0    | 0    | 1    | 0    | 0    | 0.9750 |
| 0                            | 0    | 0    | 1    | 0    | 0    | 0.9875 |
| 1                            | 0    | 0    | 0    | 1    | 1    | 1.0000 |
| 0                            | 0    | 0    | 0    | 1    | 1    | 1.0125 |
| 1                            | 0    | 0    | 0    | 1    | 0    | 1.0250 |
| 0                            | 0    | 0    | 0    | 1    | 0    | 1.0375 |
| 1                            | 0    | 0    | 0    | 0    | 1    | 1.0500 |
| 0                            | 0    | 0    | 0    | 0    | 1    | 1.0625 |
| 1                            | 0    | 0    | 0    | 0    | 0    | 1.0750 |
| 0                            | 0    | 0    | 0    | 0    | 0    | 1.0875 |
| 1                            | 1    | 1    | 1    | 1    | 0    | 1.1000 |
| 0                            | 1    | 1    | 1    | 1    | 0    | 1.1125 |
| 1                            | 1    | 1    | 1    | 0    | 1    | 1.1250 |
| 0                            | 1    | 1    | 1    | 0    | 1    | 1.1375 |
| 1                            | 1    | 1    | 1    | 0    | 0    | 1.1500 |
| 0                            | 1    | 1    | 1    | 0    | 0    | 1.1625 |
| 1                            | 1    | 1    | 0    | 1    | 1    | 1.1750 |
| 0                            | 1    | 1    | 0    | 1    | 1    | 1.1875 |
| 1                            | 1    | 1    | 0    | 1    | 0    | 1.2000 |
| 0                            | 1    | 1    | 0    | 1    | 0    | 1.2125 |
| 1                            | 1    | 1    | 0    | 0    | 1    | 1.2250 |
| 0                            | 1    | 1    | 1    | 1    | 1    | 1.2375 |
| 1                            | 1    | 1    | 0    | 0    | 0    | 1.2500 |
| 0                            | 1    | 1    | 0    | 0    | 0    | 1.2625 |
| 1                            | 1    | 1    | 0    | 1    | 1    | 1.2750 |
| 0                            | 1    | 0    | 1    | 1    | 1    | 1.2875 |
| 1                            | 1    | 0    | 1    | 1    | 0    | 1.3000 |
| 0                            | 1    | 0    | 1    | 1    | 0    | 1.3125 |
| 1                            | 1    | 0    | 1    | 0    | 1    | 1.3250 |
| 0                            | 1    | 0    | 1    | 0    | 1    | 1.3375 |
| 1                            | 1    | 0    | 1    | 0    | 0    | 1.3500 |
| 0                            | 1    | 0    | 1    | 0    | 0    | 1.3625 |
| 1                            | 1    | 0    | 0    | 1    | 1    | 1.3750 |
| 0                            | 1    | 0    | 0    | 1    | 1    | 1.3875 |
| 1                            | 1    | 0    | 0    | 1    | 0    | 1.4000 |
| 0                            | 1    | 0    | 0    | 1    | 0    | 1.4125 |
| 1                            | 1    | 0    | 0    | 0    | 1    | 1.4250 |
| 0                            | 1    | 0    | 0    | 0    | 1    | 1.4375 |
| 1                            | 1    | 0    | 0    | 0    | 0    | 1.4500 |
| 0                            | 1    | 0    | 0    | 0    | 0    | 1.4625 |
| 1                            | 0    | 1    | 1    | 1    | 1    | 1.4750 |

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VDAC   |
|------|------|------|------|------|------|--------|
| 0    | 1    | 1    | 1    | 1    | 1    | 1.4875 |
| 0    | 1    | 1    | 1    | 1    | 0    | 1.5000 |
| 0    | 1    | 1    | 1    | 0    | 1    | 1.5125 |
| 0    | 1    | 1    | 0    | 1    | 1    | 1.5250 |
| 0    | 1    | 1    | 0    | 0    | 1    | 1.5375 |
| 0    | 1    | 1    | 0    | 0    | 0    | 1.5500 |
| 0    | 1    | 1    | 0    | 0    | 0    | 1.5625 |
| 0    | 1    | 0    | 0    | 1    | 1    | 1.5750 |
| 0    | 1    | 0    | 0    | 1    | 1    | 1.5875 |
| 0    | 1    | 0    | 0    | 1    | 0    | 1.6000 |

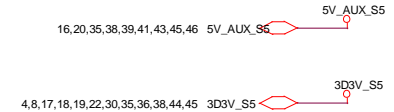
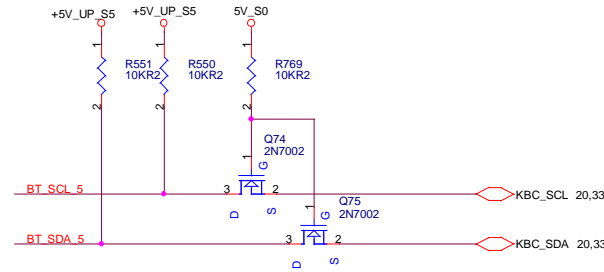
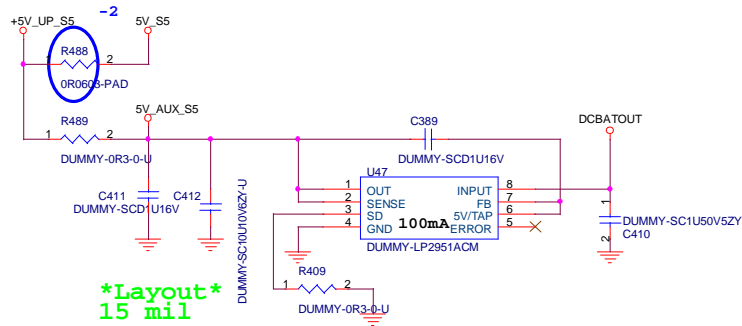
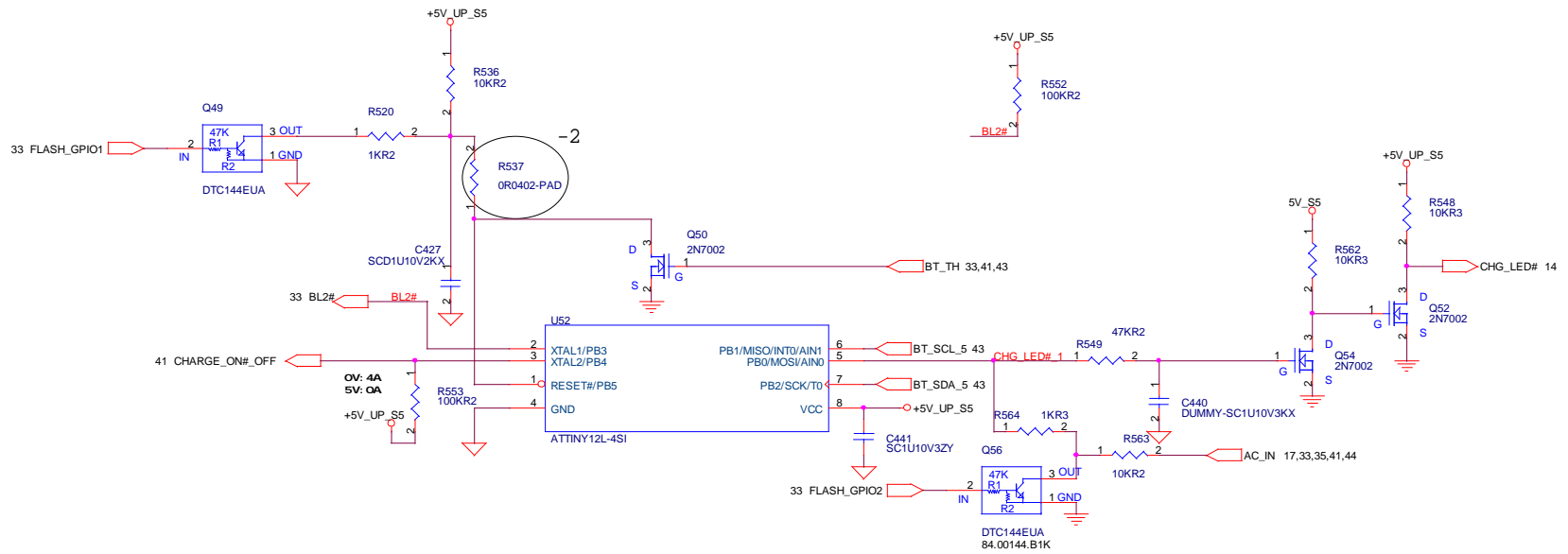
CPU\_Vcore IMVP5\_FMB1(2/2)



PLACE IN THE BACK OF CPU, ESR < (TBD)mOhm,

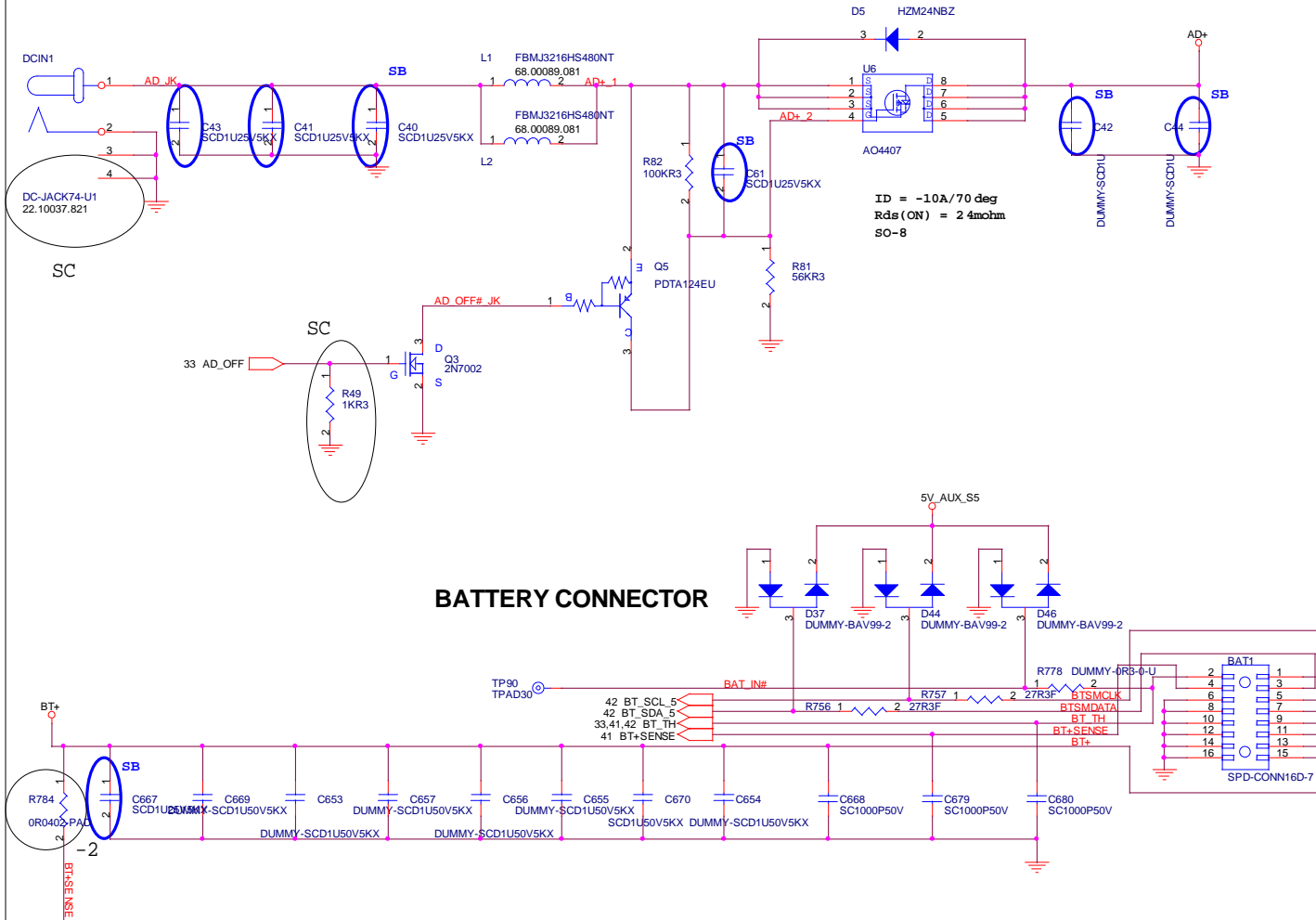


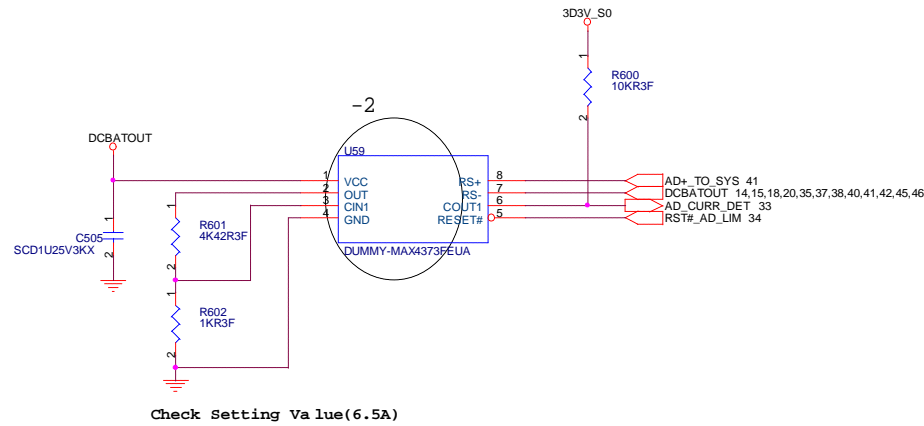




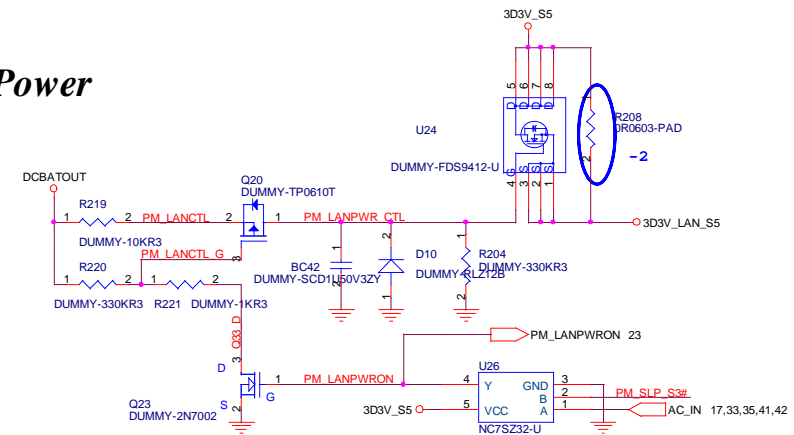
\*Layout\*  
15 mil

# Adaptor in to generate DCBATOUT

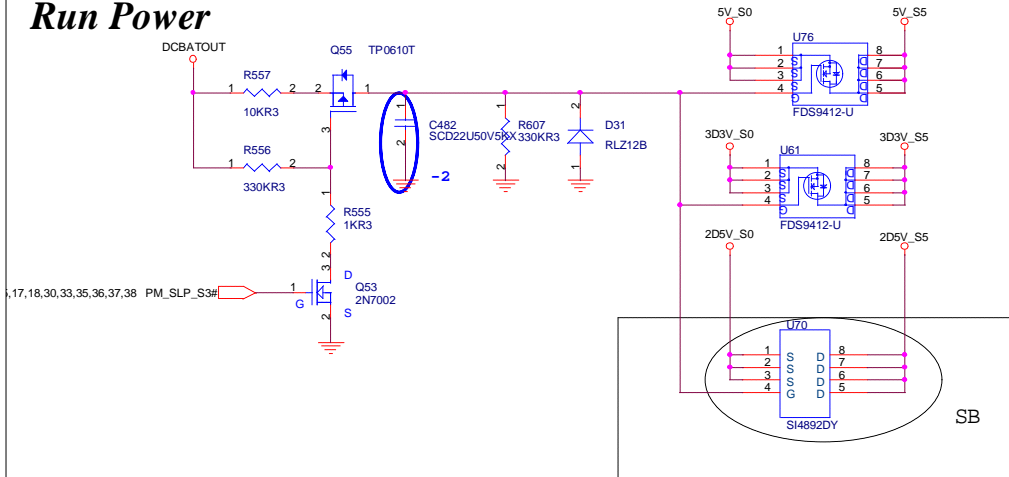




## LAN Power

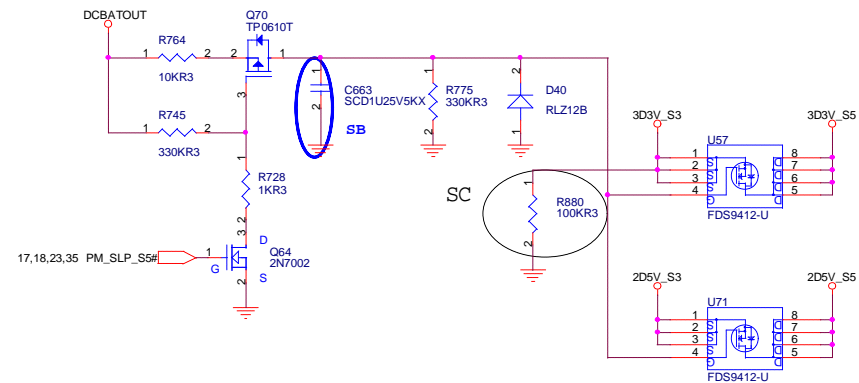


## Run Power



## Suspend Power

Support standby wakeup LAN only





33 KROW8  
33 KROW7  
33 KROW6  
33 KROW5  
33 KROW4  
33 KROW3  
33 KROW2  
33 KROW1  
33 KCOL16  
33 KCOL15  
33 KCOL14  
33 KCOL13

33 KCOL12  
33 KCOL11  
33 KCOL10  
33 KCOL9  
33 KCOL8  
33 KCOL7  
33 KCOL6  
33 KCOL5  
33 KCOL4  
33 KCOL3  
33 KCOL2  
33 KCOL1

RC5  
SRC100P50V-U

RC6  
SRC100P50V-U

RC7  
SRC100P50V-U

RC8  
SRC100P50V-U

RC9  
SRC100P50V-U

RC10  
SRC100P50V-U

-2

-2

SB

SB

SB

SB

SB

SC

SB

SC

SB

SB

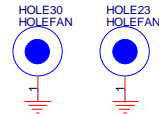
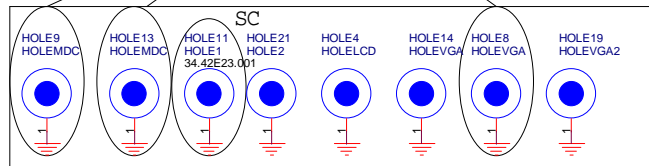
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Taipei Hsien 221, Taiwan, R.O.C.

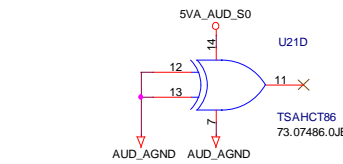
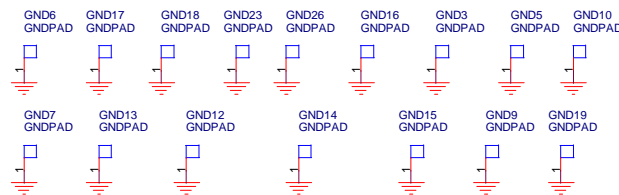
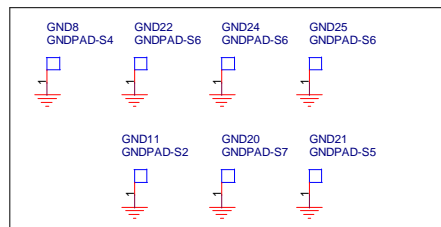
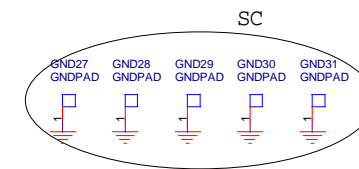
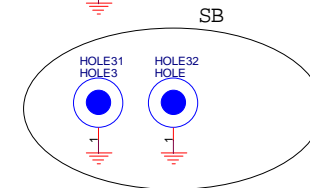
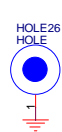
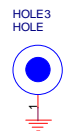
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|--------------------------------|-----------------|----------------|-----|
| Title                          |                 |                |     |
| EMI                            |                 |                |     |
| Size                           | Document Number |                | Rev |
| Custom                         | YUHINA2&3       |                | -2  |
| Date: Thursday, April 08, 2004 |                 | Sheet 45 of 46 |     |

NO USE LOGIC

SB



SPARE GATES



SB

