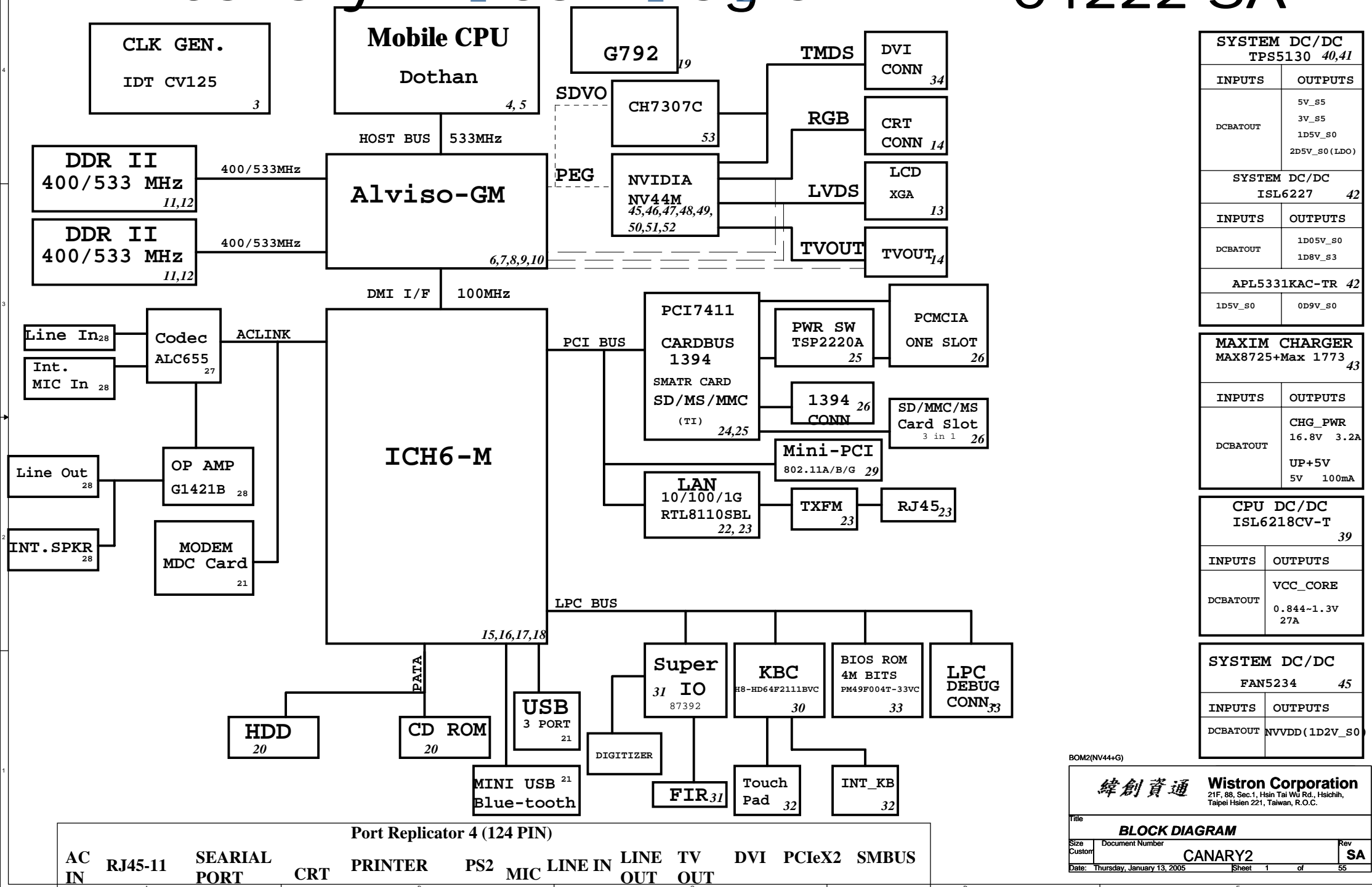


Canary2 Block Diagram



Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH FWORK In signal.

CY28411ZC Spread Spectrum Select

SS3	SS2	SS1	Spread Mode	Spread Amount%
0	0	0	Down	0.8
0	0	1	Down	1.25
0	1	0	Down	1.75
0	1	1	Down	2.5
1	0	0	Center	+~0.3
1	0	1	Center	+~0.5
1	1	0	Center	+~0.8
1	1	1	Center	+~1.25

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
----------------------------------------------------------------------------	----------------------

BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

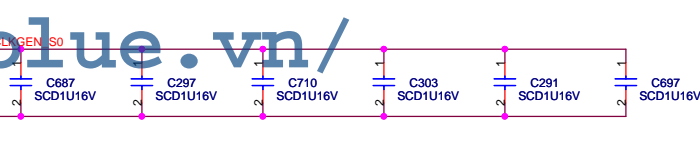
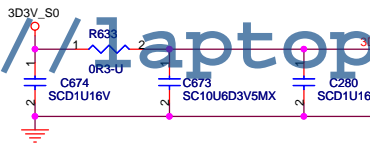
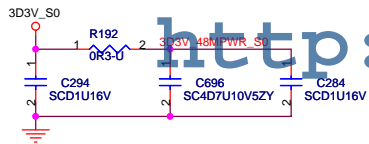
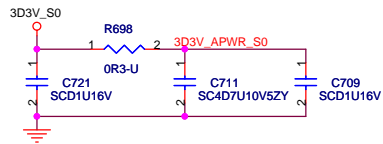
TitleITP

SizeA3

Document NumberCANARY2

RevSA

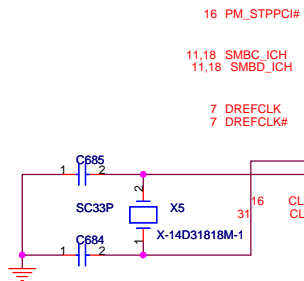
Date: Thursday, January 13, 2005Sheet 2 of 55



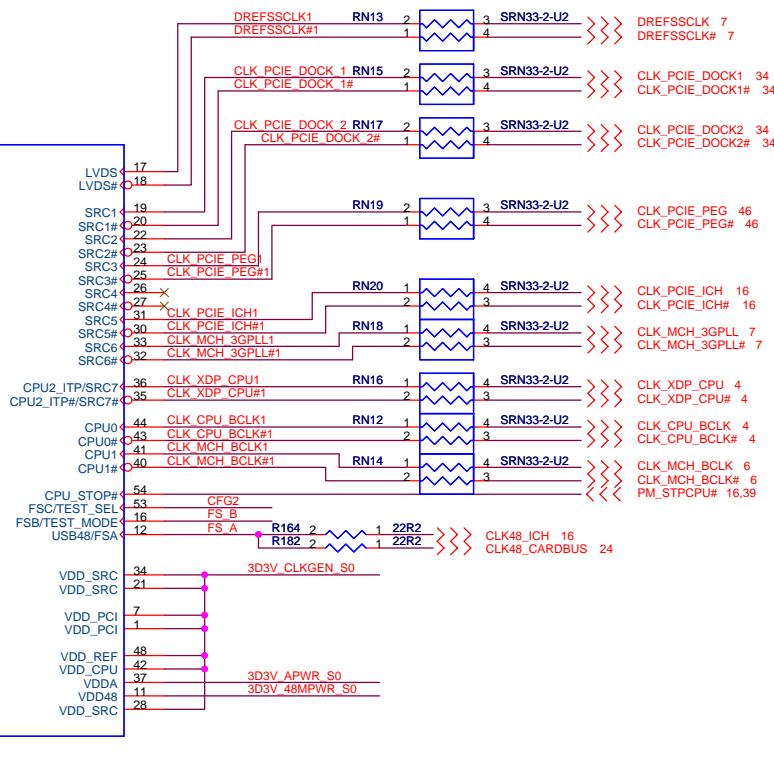
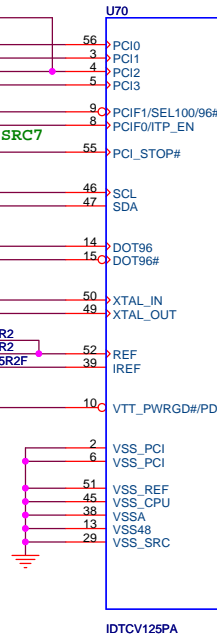
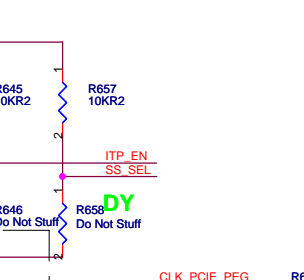
PCLK_PCM & PCLK_SIO
need equal length



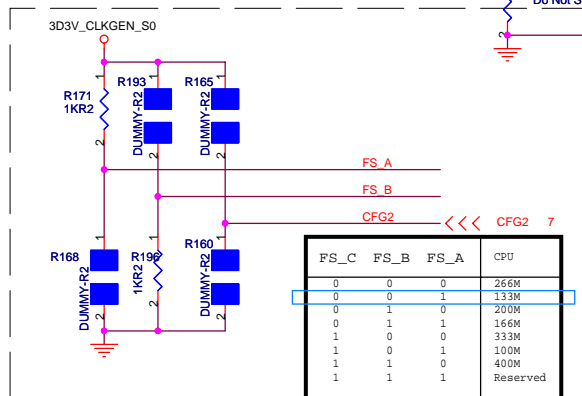
H/T: 100/96MHz
SS_SEL
ITP_EN
H/L : CPU_ITP/SRC7



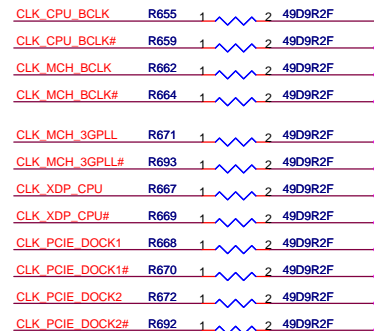
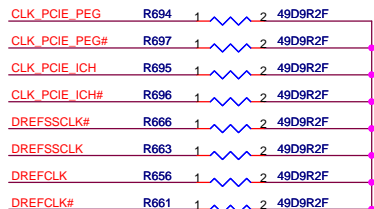
CLK_ICH14 & CLK14_SIO
need equal length



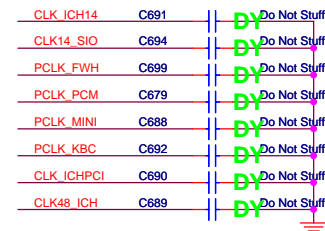
IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



EMI capacitor



BOM2(NV44+G)

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Clock Generator - IDT125

Size
A3

Document Number
CANARY2

Rev
SA

Date

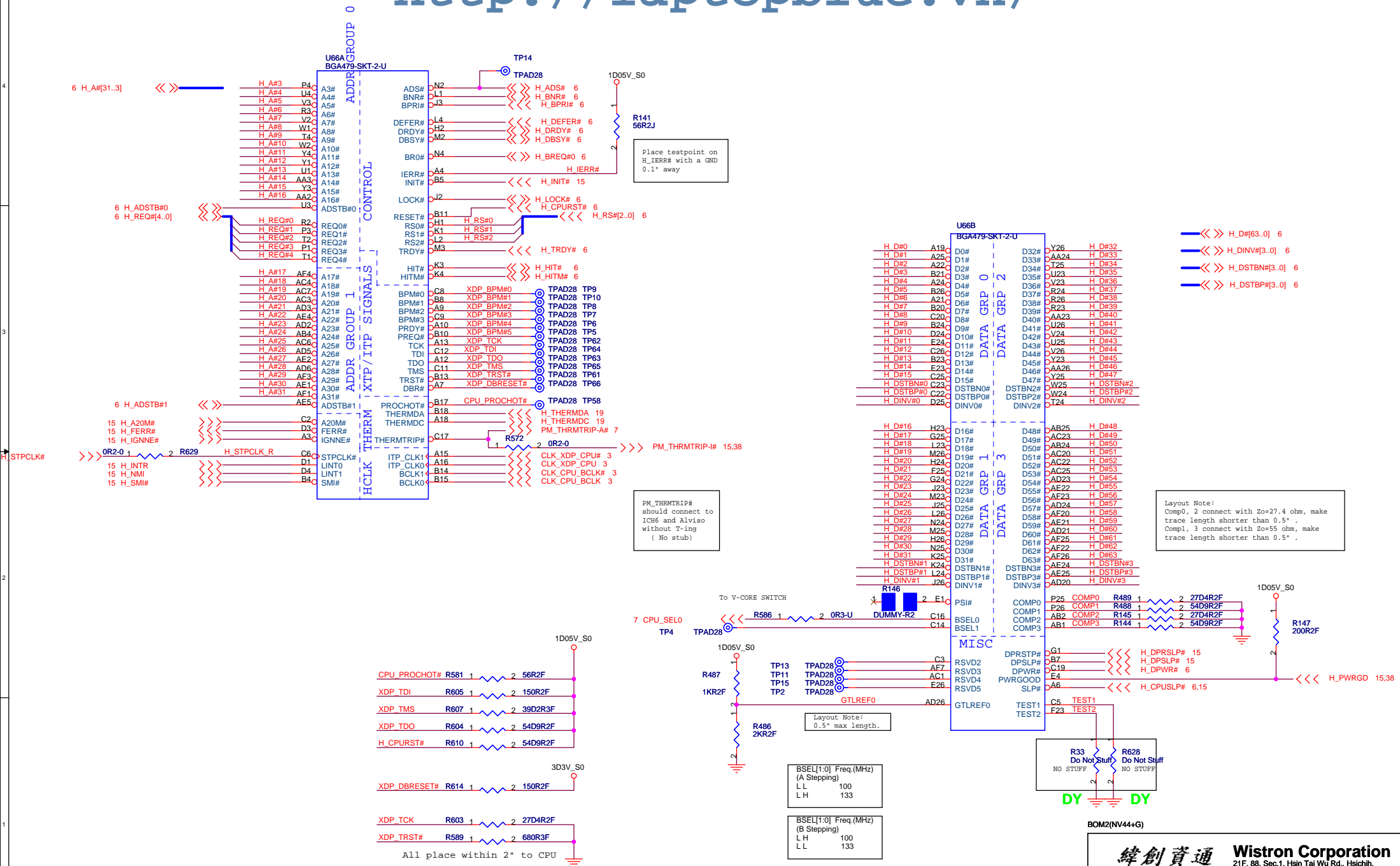
Thursday, January 13, 2005

Sheet

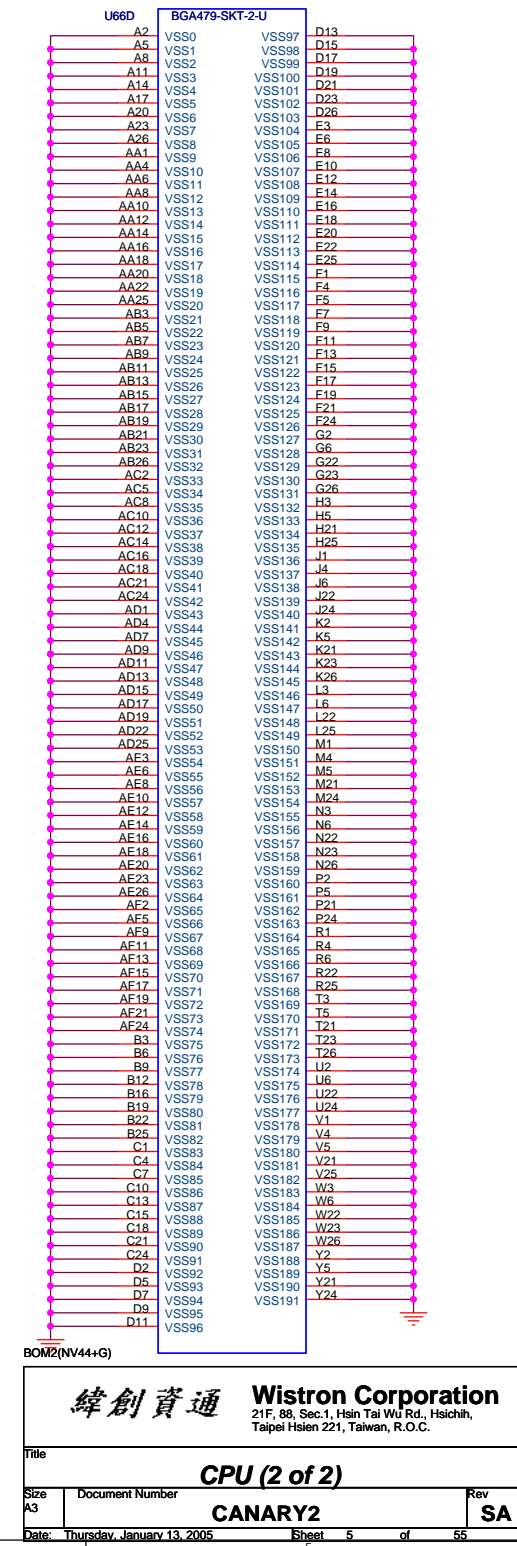
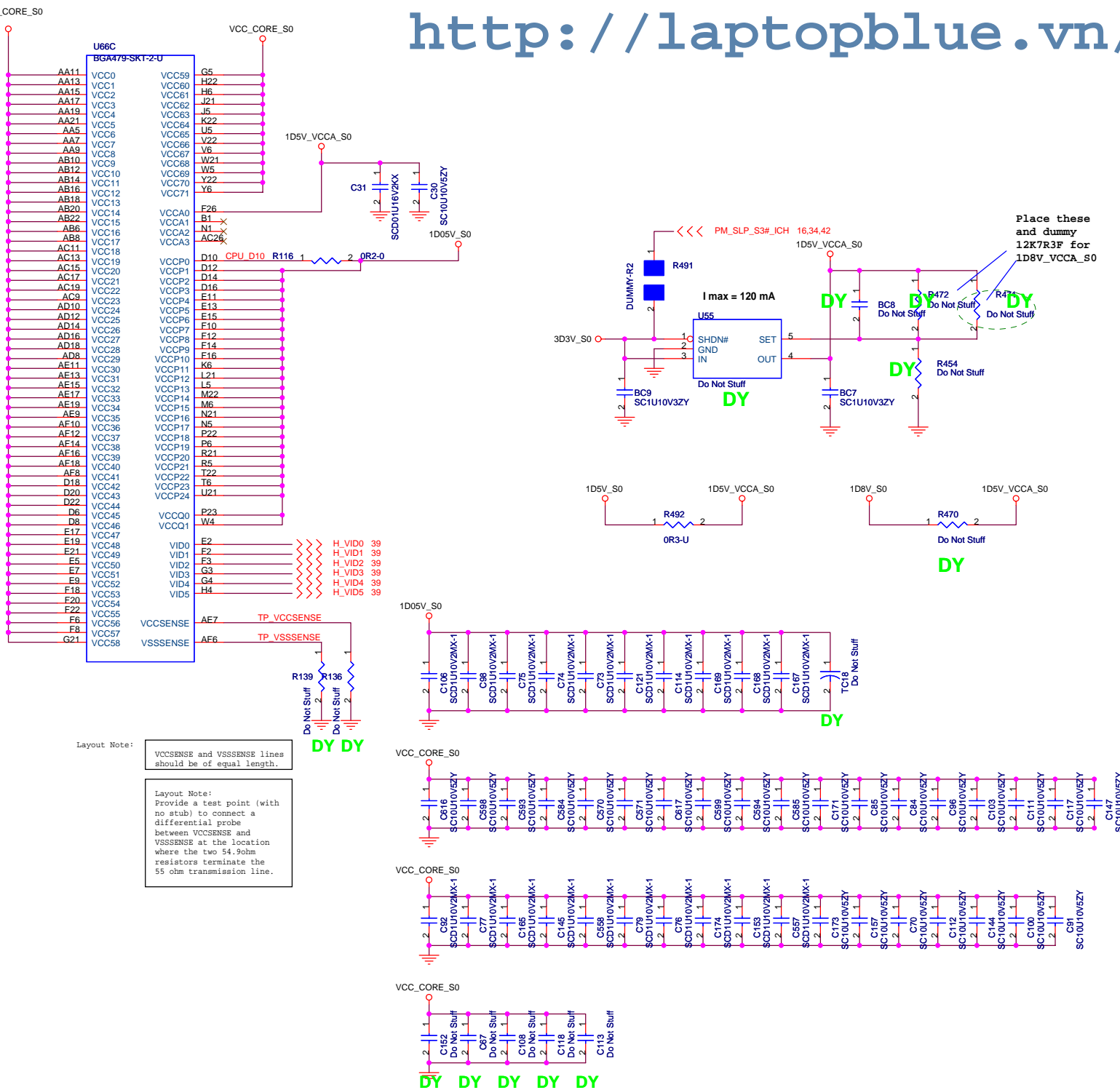
3

of

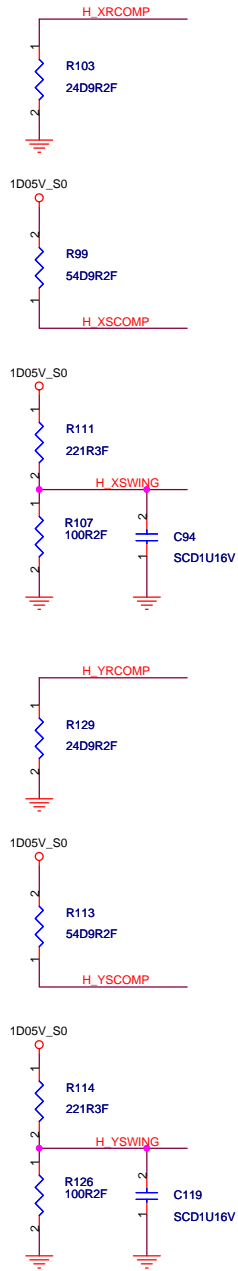
55



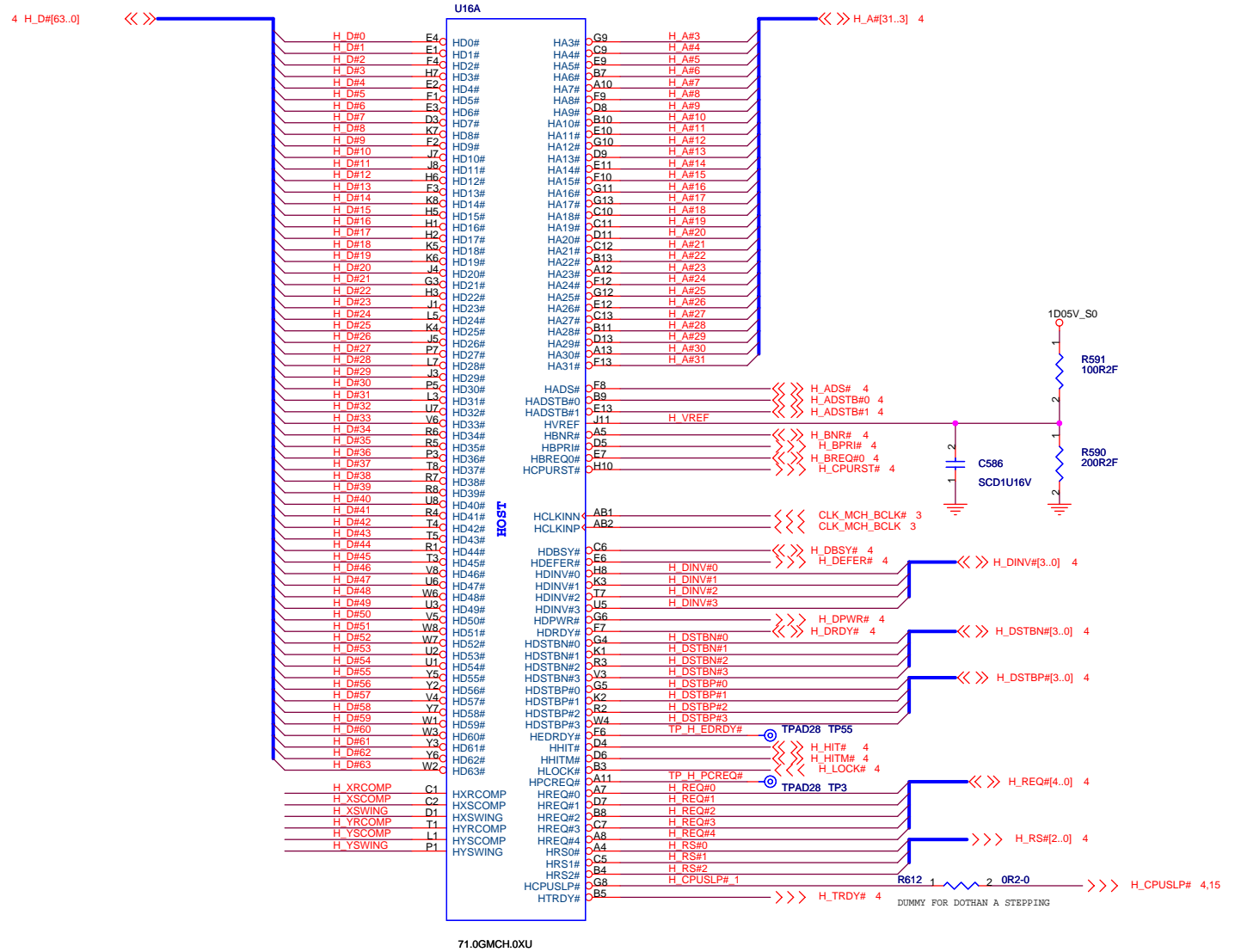
<http://laptopblue.vn/>



<http://laptopblue.vn/>



Place them near to the chip



BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

[illegible]

GMCH (1 of 5)

Size
A3

Document Number

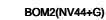
CANARY2

Rev
SA

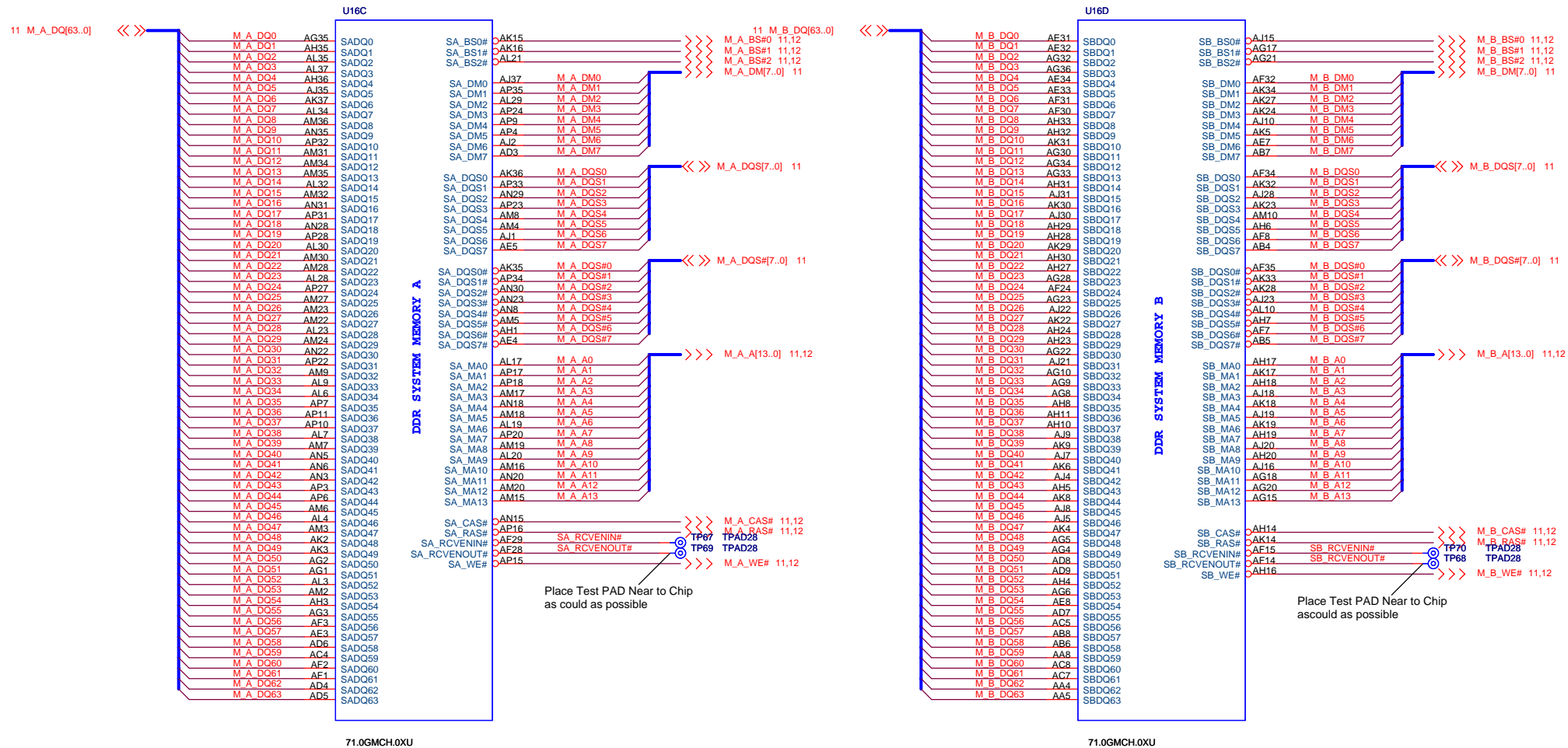
Date: Thursday, January 13, 2005

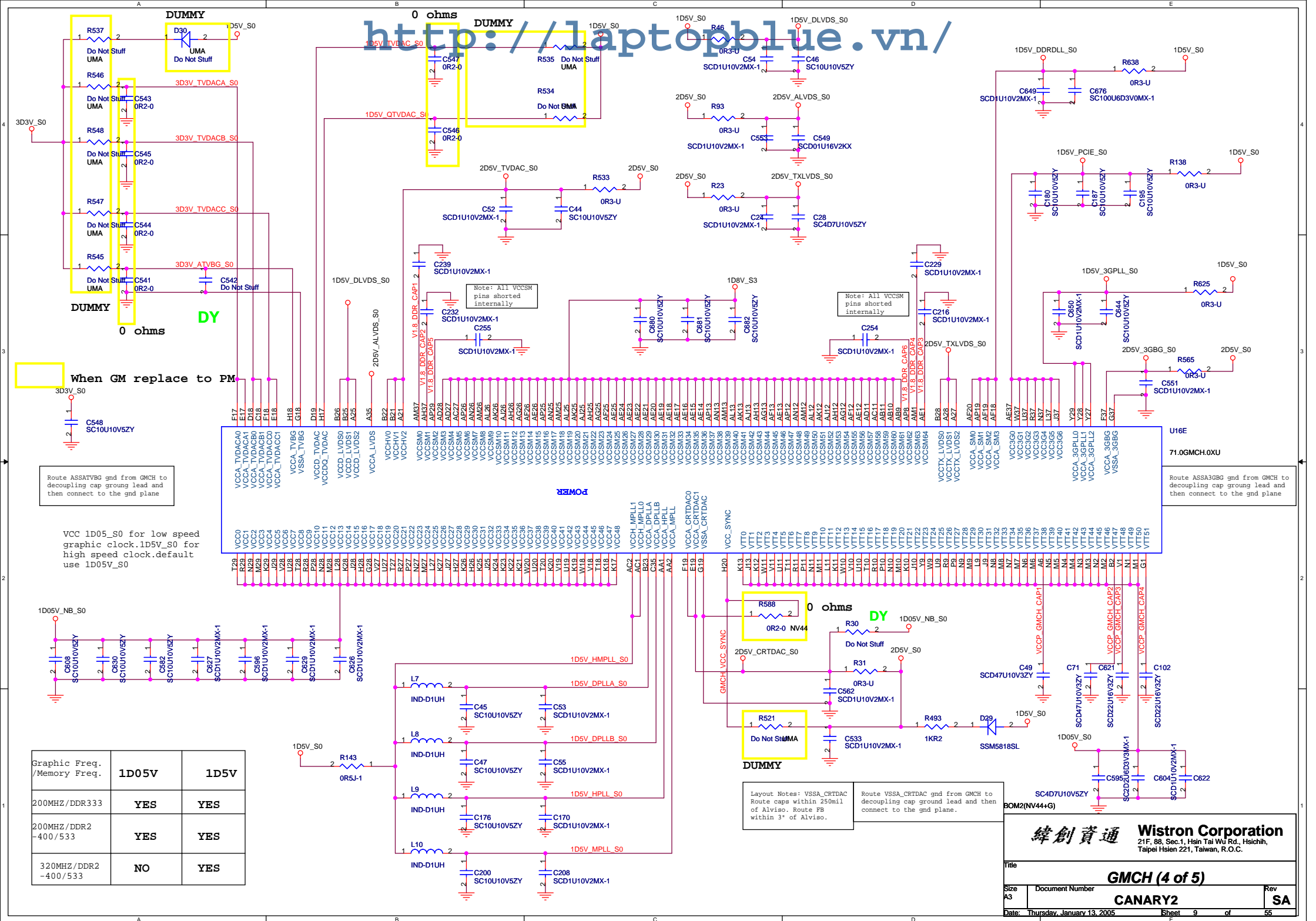
Sheet 6 of 55

1D5V_PCIE_S0



Title			
GMCH (2 of 5)			
Size	Document Number		Rev
Custom	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 7 of	55

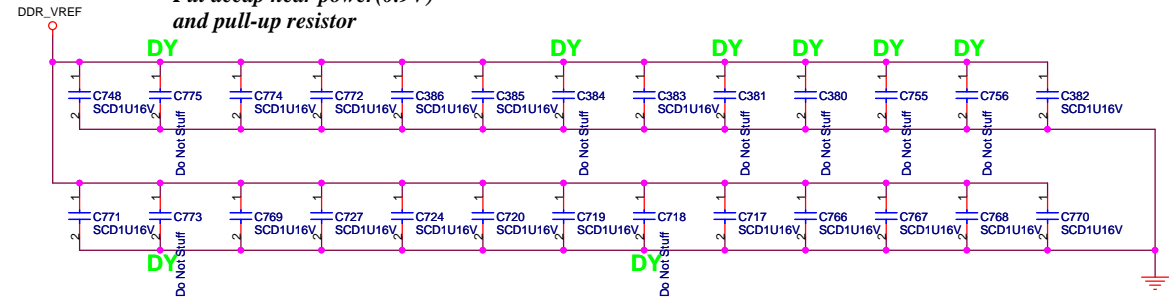




Graphic Freq. /Memory Freq.	1D05V	1D5V
200MHz/DDR333	YES	YES
200MHz/DDR2 -400/533	YES	YES
320MHz/DDR2 -400/533	NO	YES

ON <http://laptopblue.vn/> Decoupling Capacitor

*Put decap near power(0.9V)
and pull-up resistor*



1D8V_S3

Place these Caps near DM2

C746 SC2D2U6D3V3MX-1

C745 SC2D2U6D3V3MX-1

C370 SC2D2U6D3V3MX-1

C740 SC2D2U6D3V3MX-1

C744 SC2D2U6D3V3MX-1

C322 Do Not Stuff

C327 Do Not Stuff

C325 Do Not Stuff

C726 Do Not Stuff

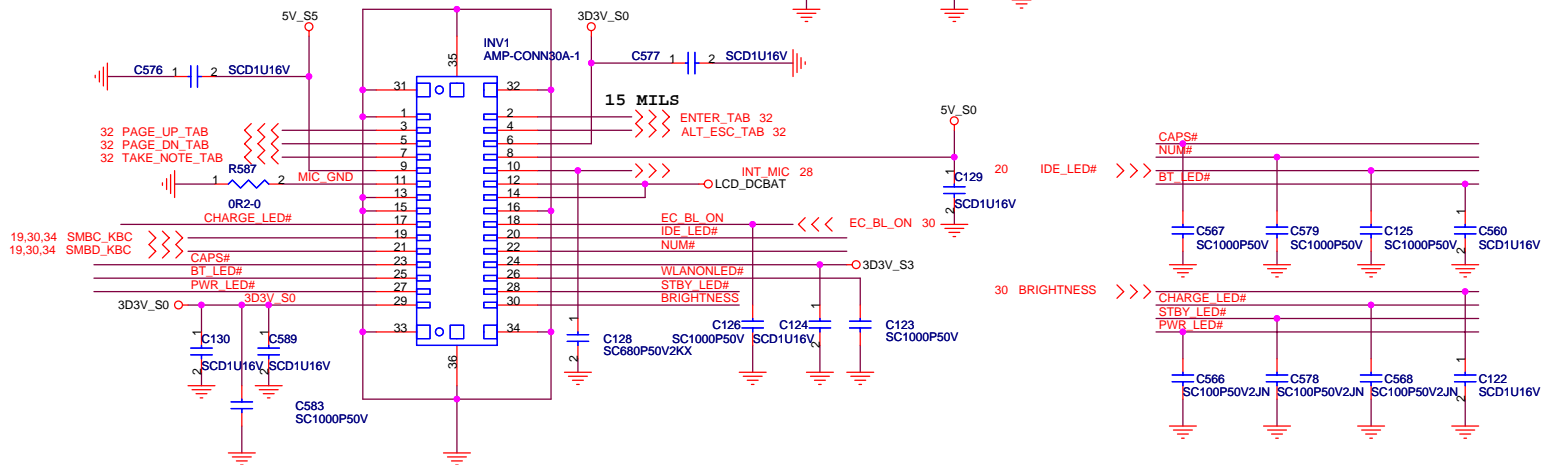
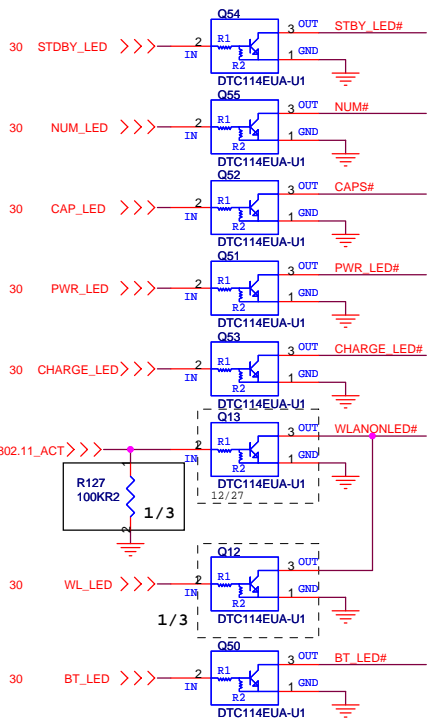
DM2

Ground

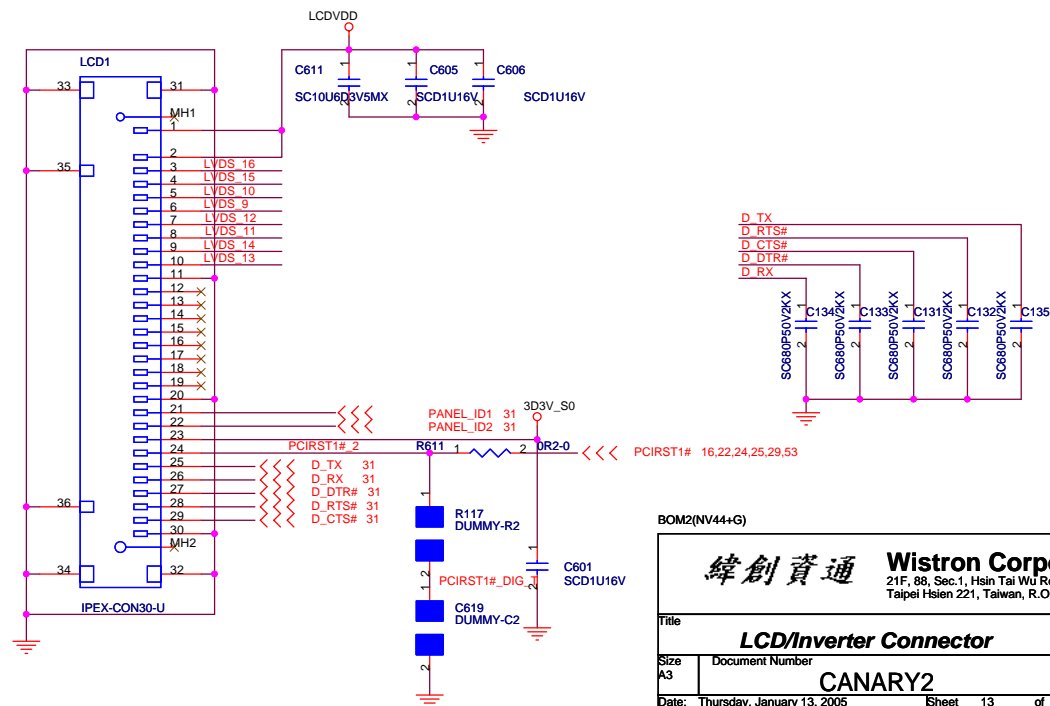
緯創資通

Title DDR2 Termination Resistor			
Size A3	Document Number CANARY2	Rev SA	
Date: Thursday, January 13, 2005	Sheet 12	of 55	

INVERTER INTERFACE



LCD CONN



BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

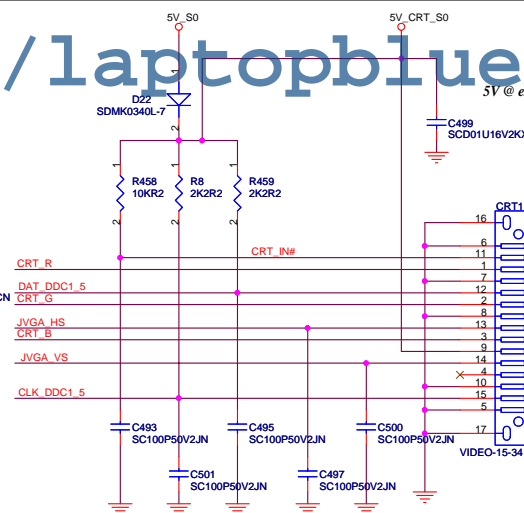
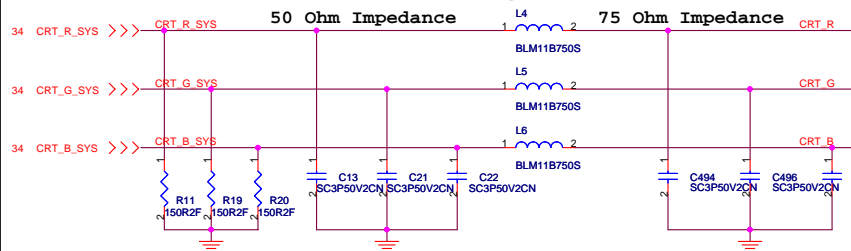
Title		
LCD/Inverter Connector		
Size	Document Number	Rev
A3	CANARY2	SA
Date: Thursday, January 13, 2005	Sheet 13 of	55

CRT I/F & TV CONNECTOR

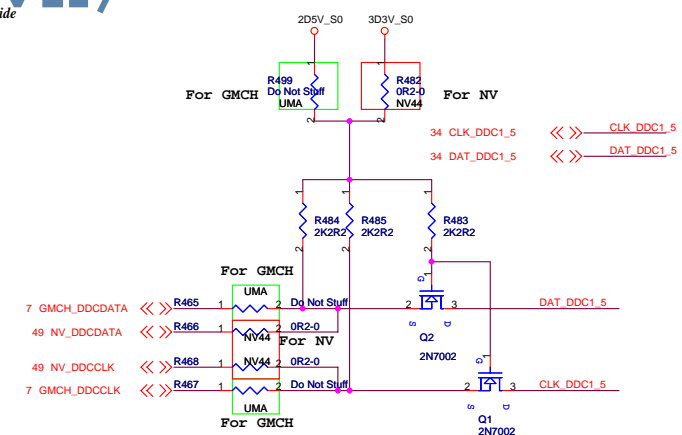
http://laptopblue.vn/

SV @ ext. CRT side

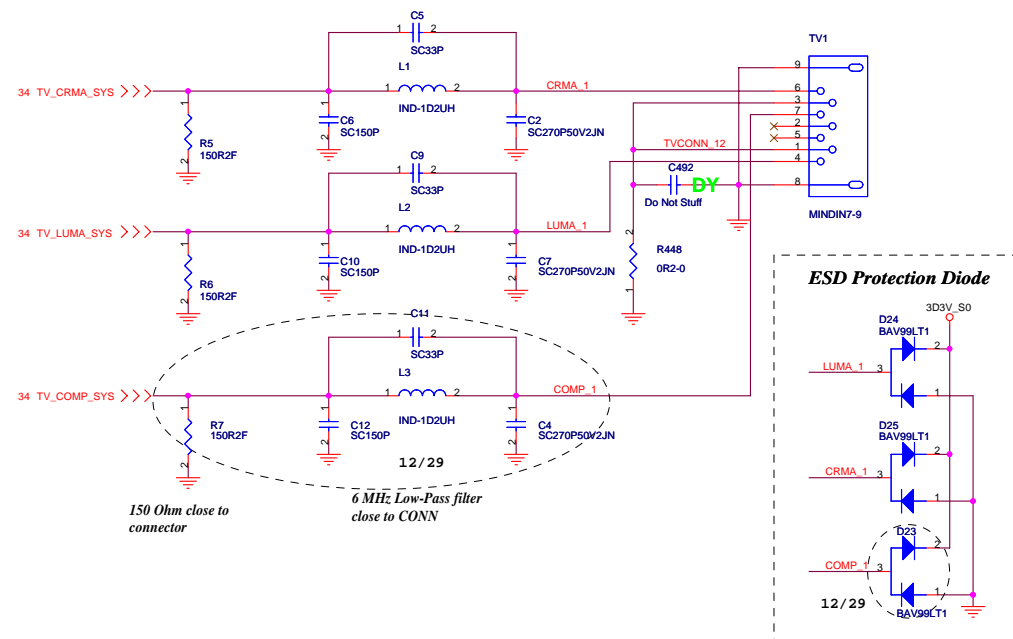
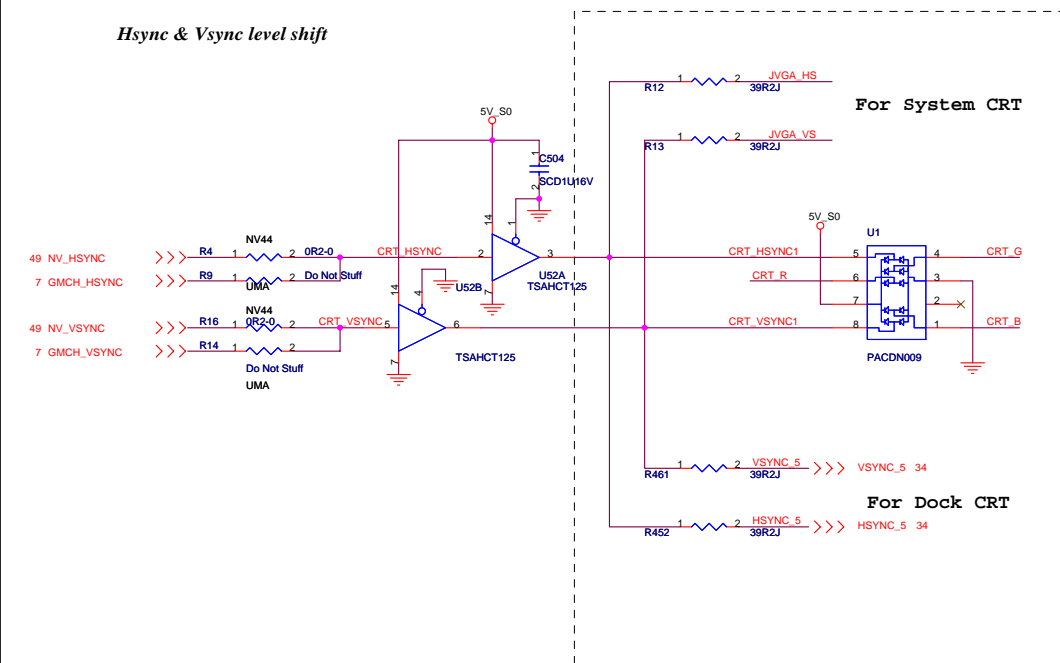
Ferrite bead impedance: 75ohm@100MHz



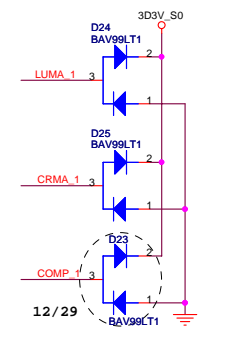
DDC_CLK & DATA level shift



Hsync & Vsync level shift

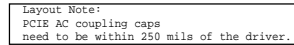


ESD Protection Diode



BOM2(NV44+G)

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector	
Size Custom	Document Number CANARY2
Date: Thursday, January 13, 2005	Sheet 14 of 55



ICH6-M Strapping Options			
REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

BOM2(NV44+E)

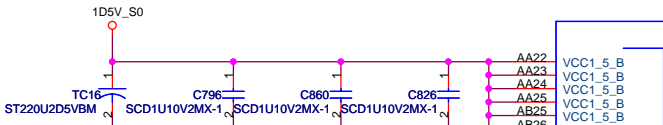
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
ICH6-M (2 of 4)			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 16 of	55

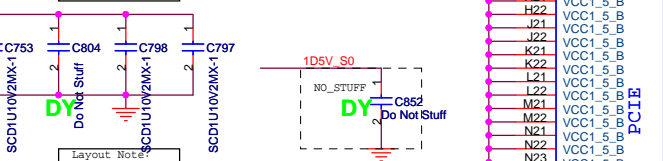
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

1D5V_S0

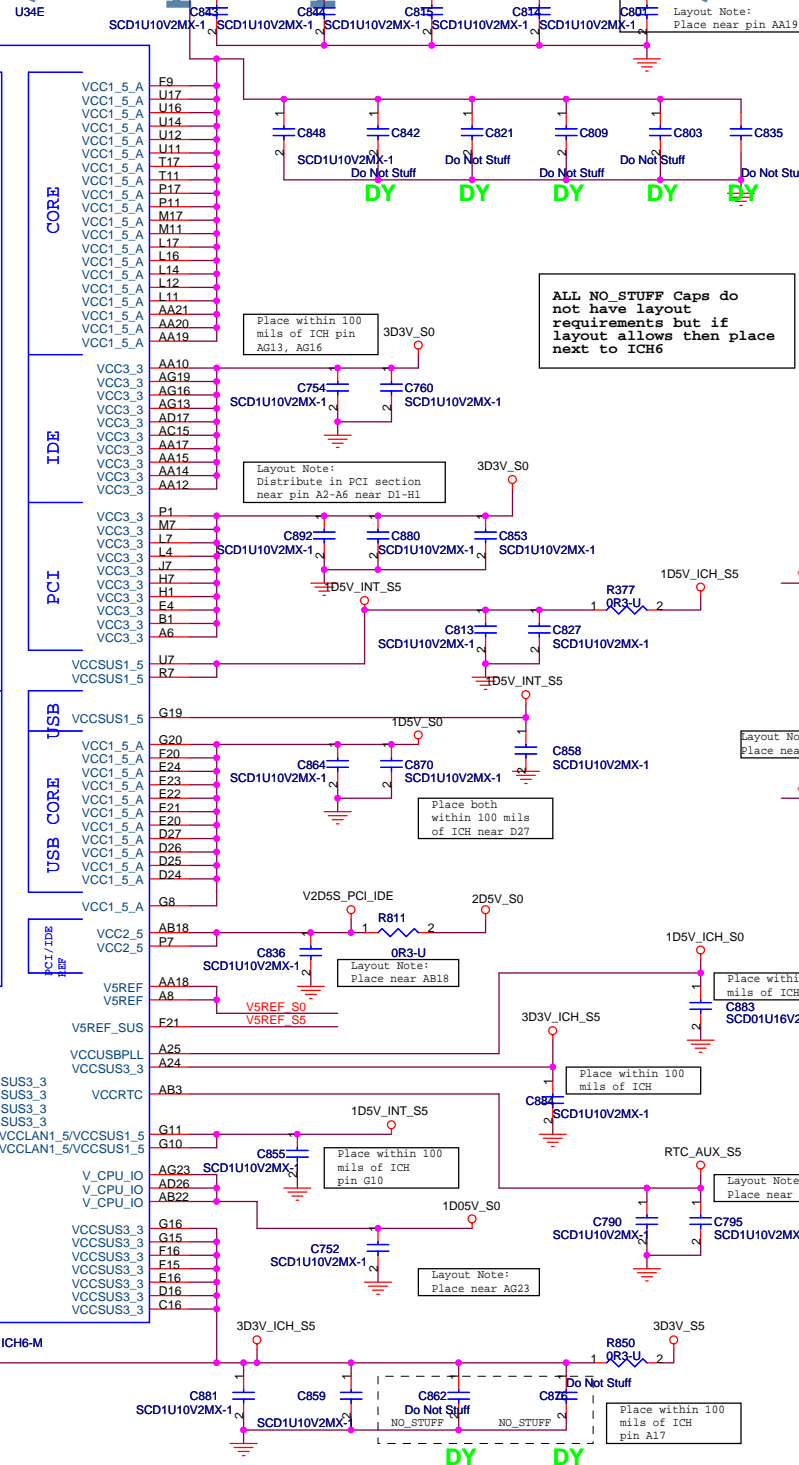
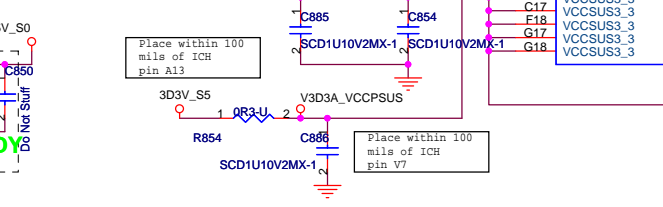
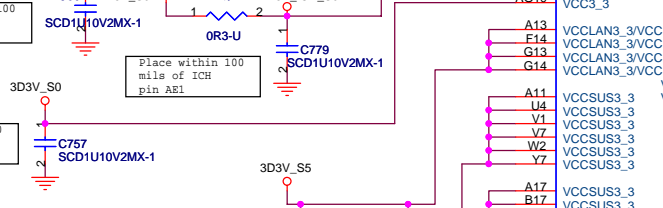
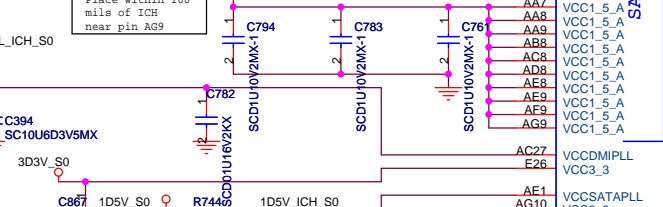
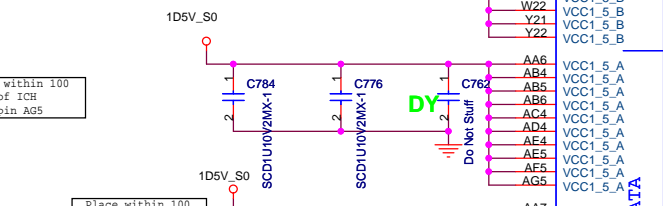
Layout Note:
Place near pin AA19



Layout Note:
IDE decoupling

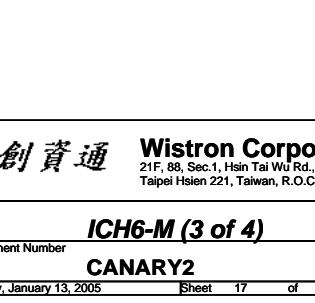
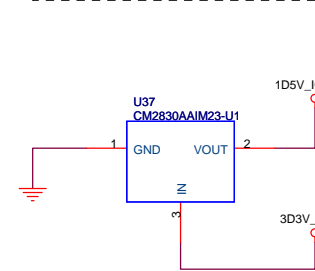
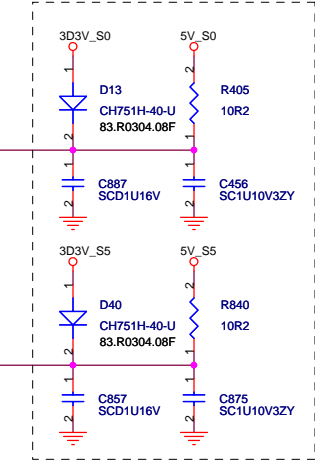


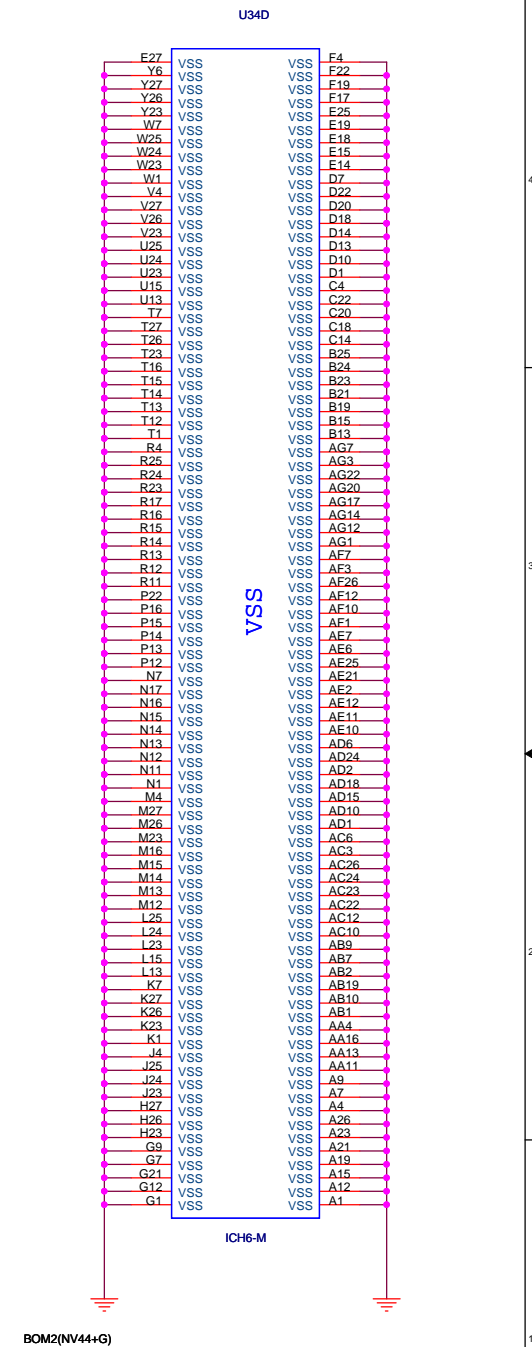
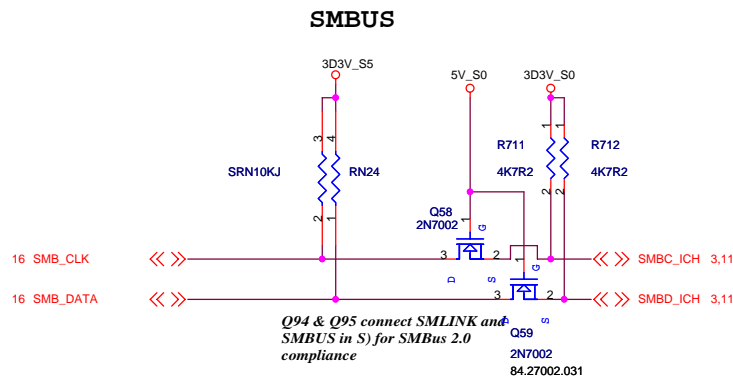
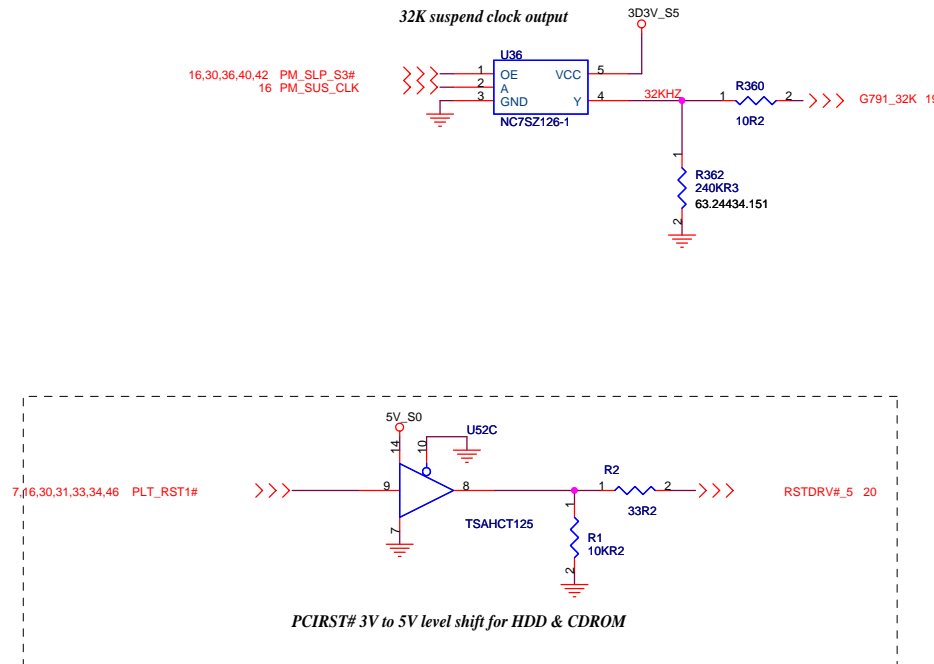
Layout Note:
PCI decoupling



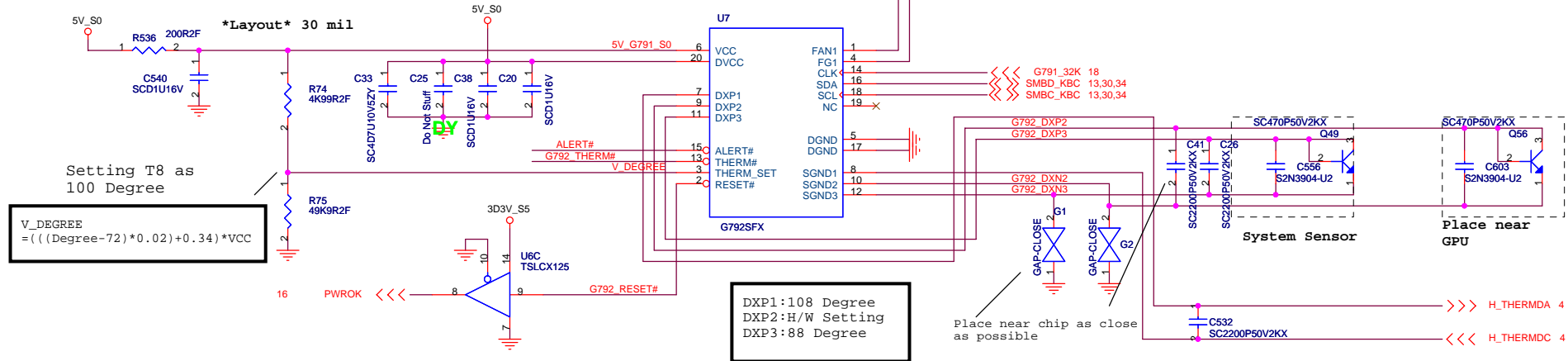
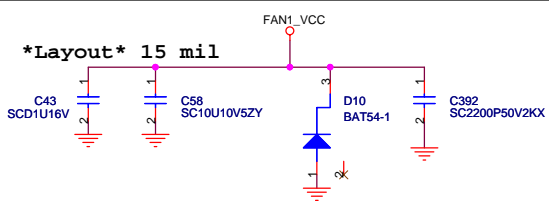
ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail

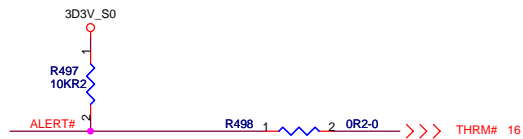




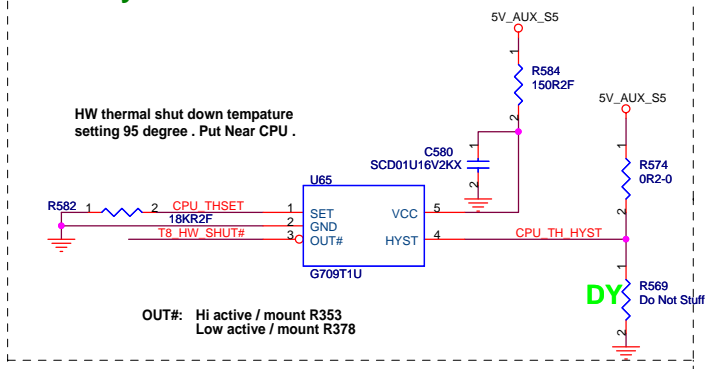
BOM2(NV44+G)



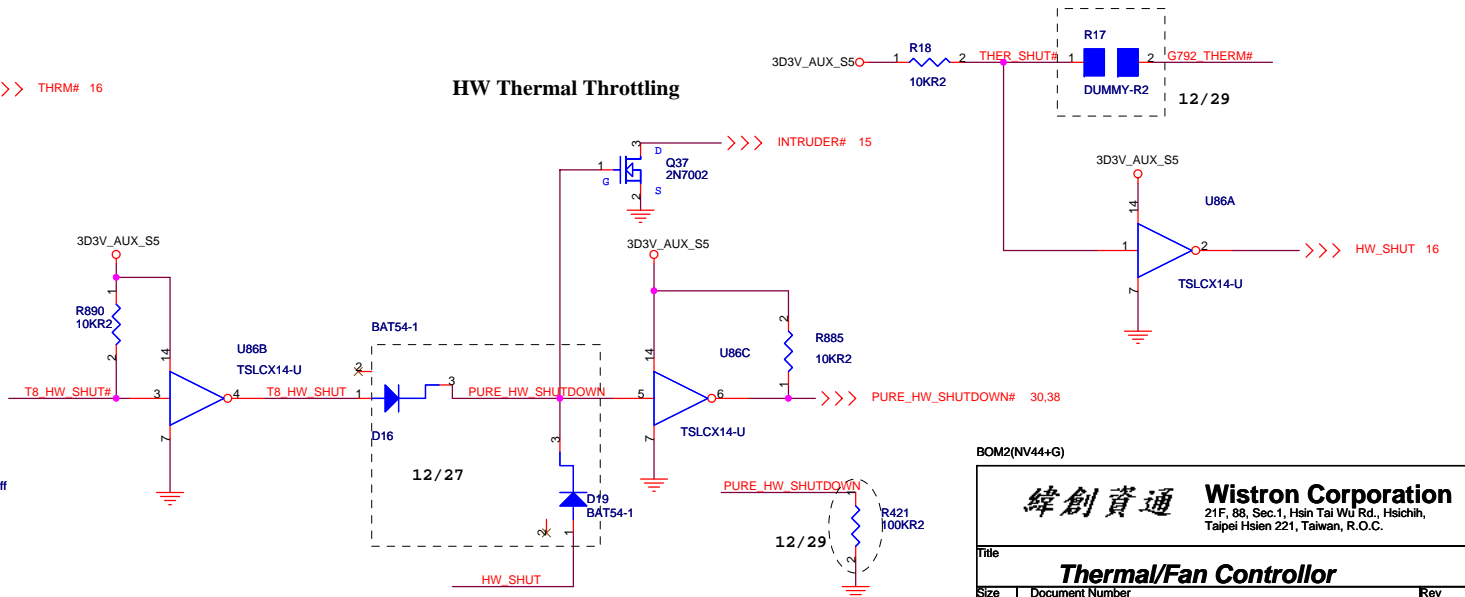
HW thermal shut down tempature setting 95 degree . Put Near CPU .



Dummy when G791 enhanced T8 function



HW Thermal Throttling



BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

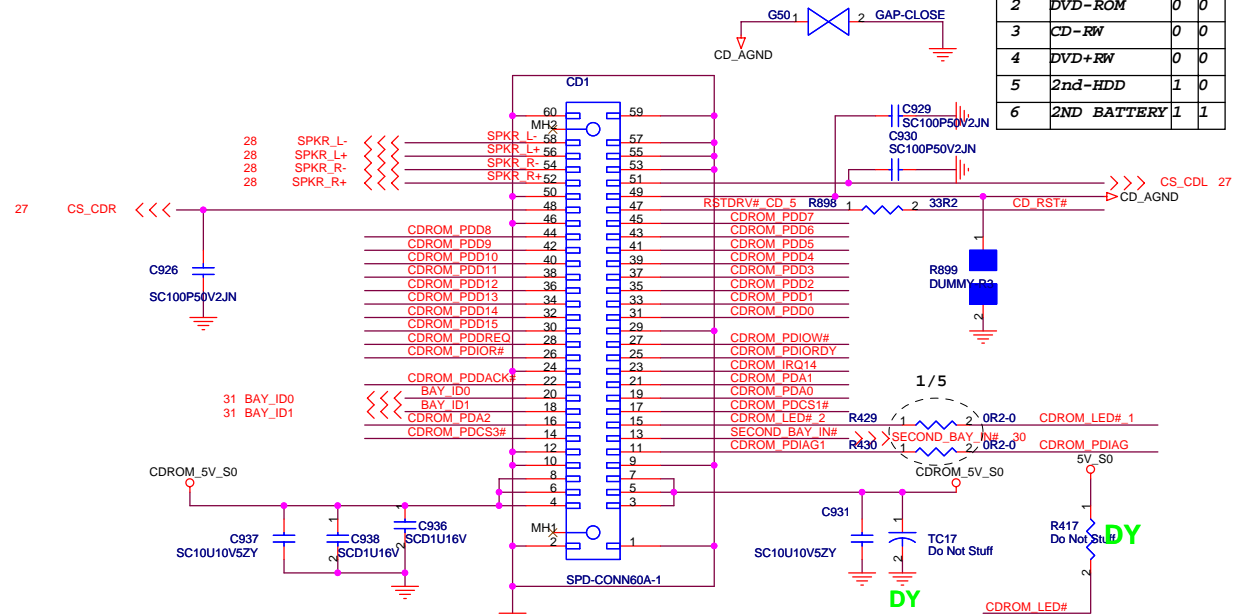
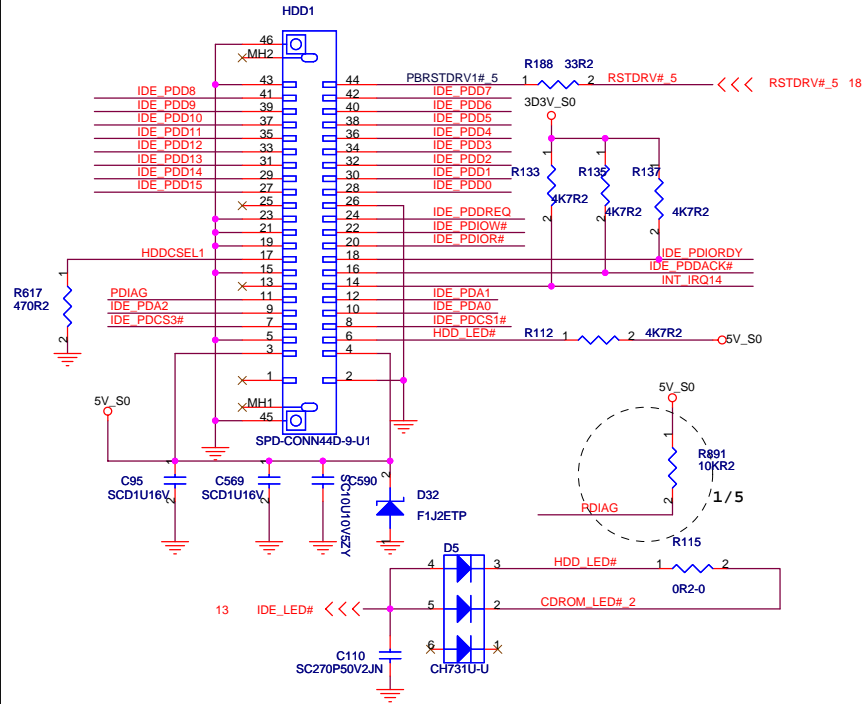
Title			
<i>Thermal/Fan Controllor</i>			
Size	Document Number	Rev	
Custom	CANARY2	SA	
Date: Thursday, January 13, 2005		Sheet 19	of 55

HDD Connector

<http://laptopblue.vn/>

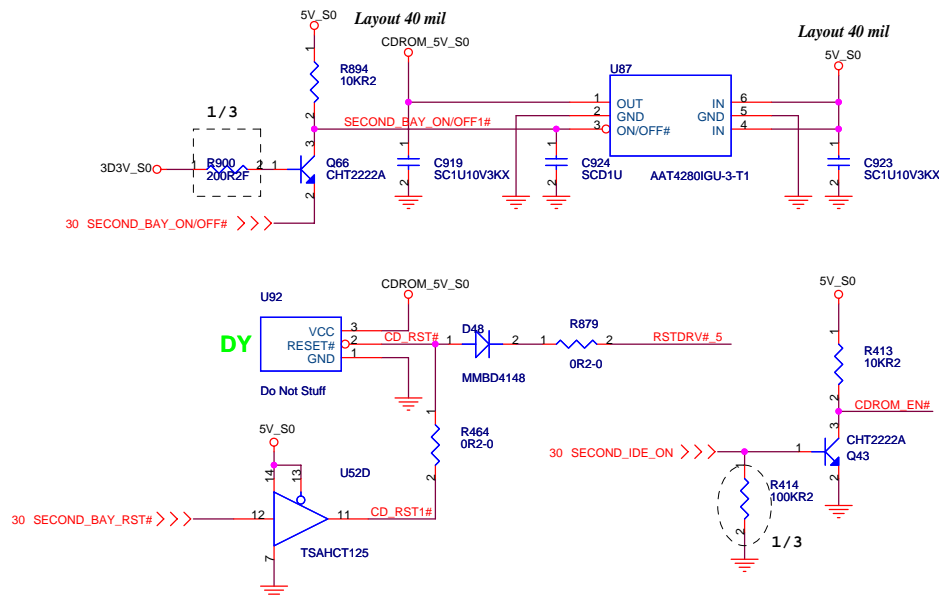
CD-ROM Connector

BAY Option Table			
Type	Device Description	BAYID 0	BAYID 1
1	CD-ROM	0	0
2	DVD-ROM	0	0
3	CD-RW	0	0
4	DVD+RW	0	0
5	2nd-HDD	1	0
6	2ND BATTERY	1	1

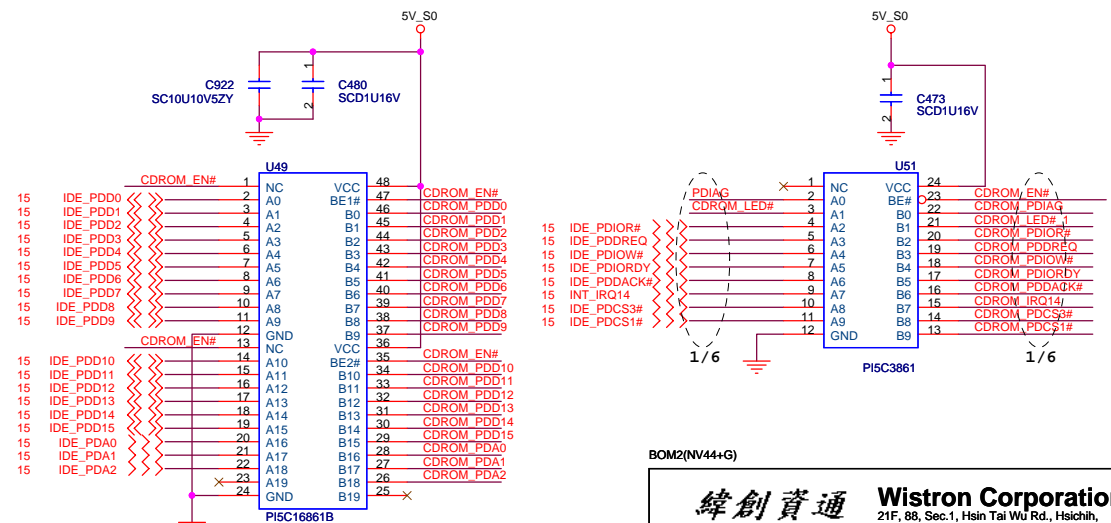


CHECK PIDE/SIDE DIAG# PIN

HOT SWAP CIRCUIT

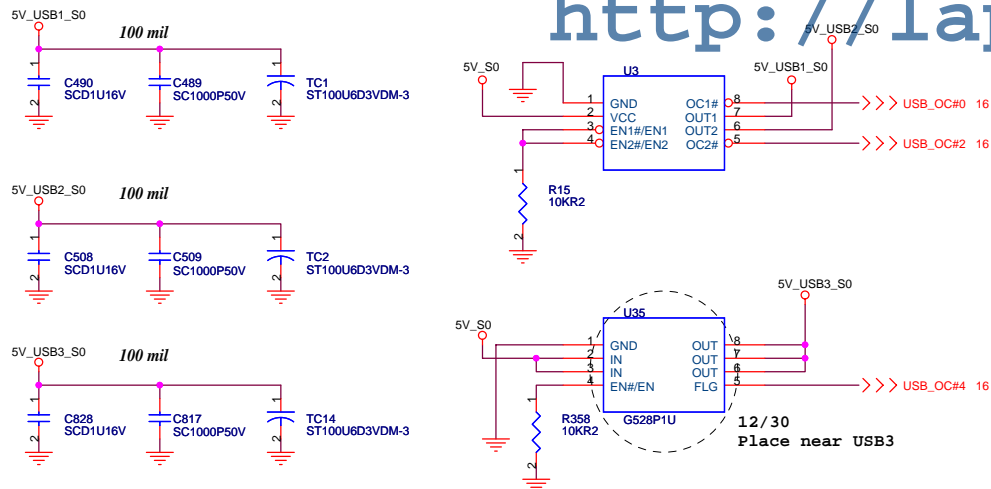


TRI-STATE SWITCH FOR CDROM HOT SWAP

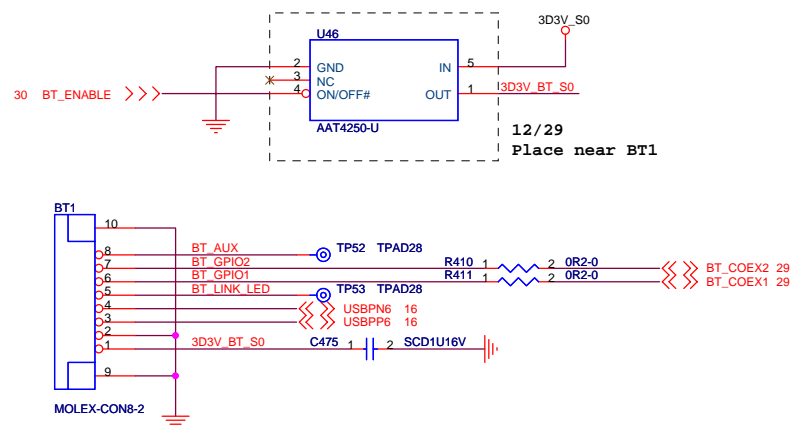


BOM2(NV44+G)

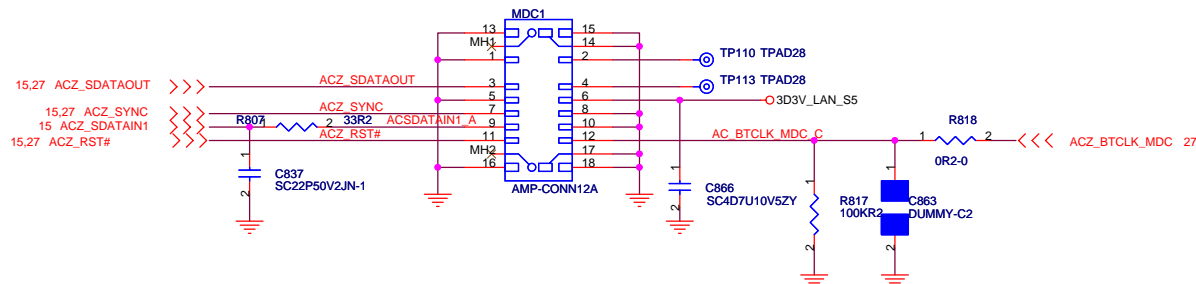
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HDD and CDROM	
Size	Document Number
A3	CANARY2
Date: Thursday, January 13, 2005	Sheet 20 of 55
Rev	SA



BLUETOOTH MODULE CONNECTOR

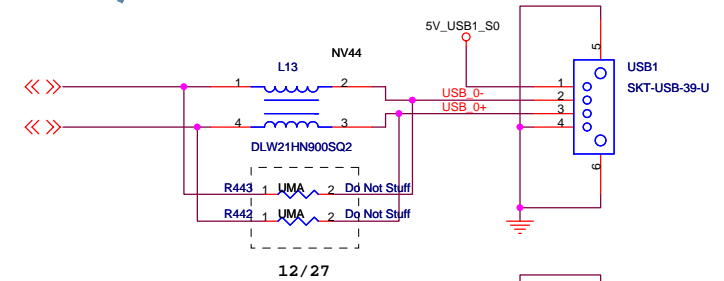


MDC 1.5 CONNECTOR



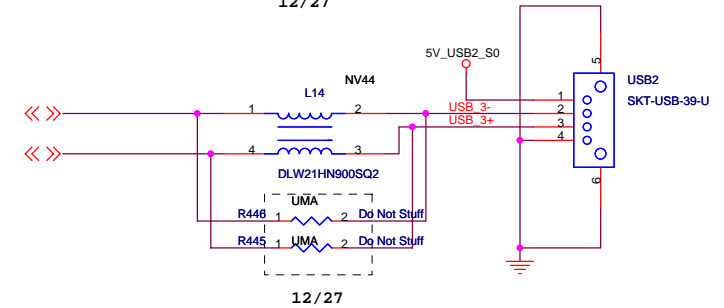
16 USBPN0

16 USBPP0



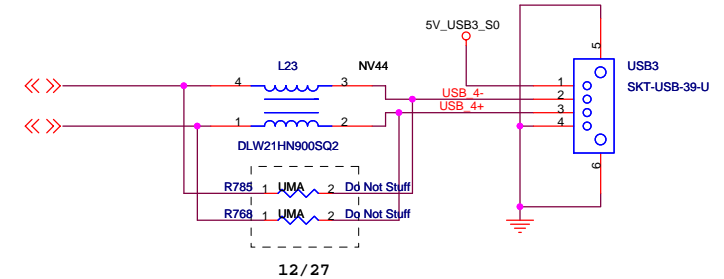
16 USBPN2

16 USBPP2



16 USBPN4

16 USBPP4



BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB & MDC & BTOOTH

Size

Document Number

CANARY2

Rev

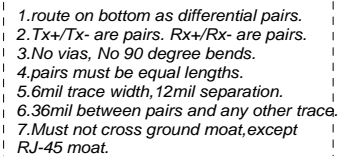
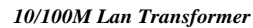
SA

Date: Thursday, January 13, 2005

Sheet 21

of

55

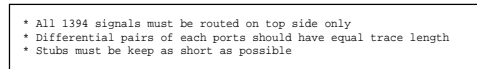


RJ11 signal must leave the other signal or power plane 100mil.

Giga Lan Transformer



BOM2(NV44+G)



3D3V_S0

C404
SC1000P50V

C831
SCD1U16V

C341
SCD1U16V

C747
Do Not Stuff

DY

3D3V_S0

C739
SC1000P50V

C742
SCD1U16V

C749
SCD1U16V

C787
SCD1U16V

3D3V_S0

C448
Do Not Stuff

C452
SCD1U16V

C453
SCD1U16V

C736
Do Not Stuff

DY

BOM2(NV44+G)			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TI PCI7411 GHK (1 of 2)			
Size A3	Document Number	CANARY2	Rev SA
Date: Thursday, January 13, 2005	Sheet	24	of 55

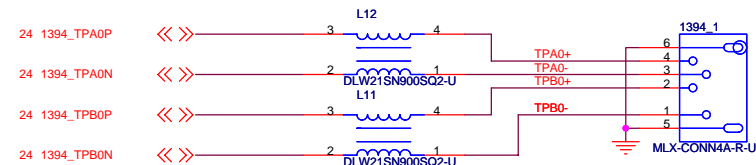
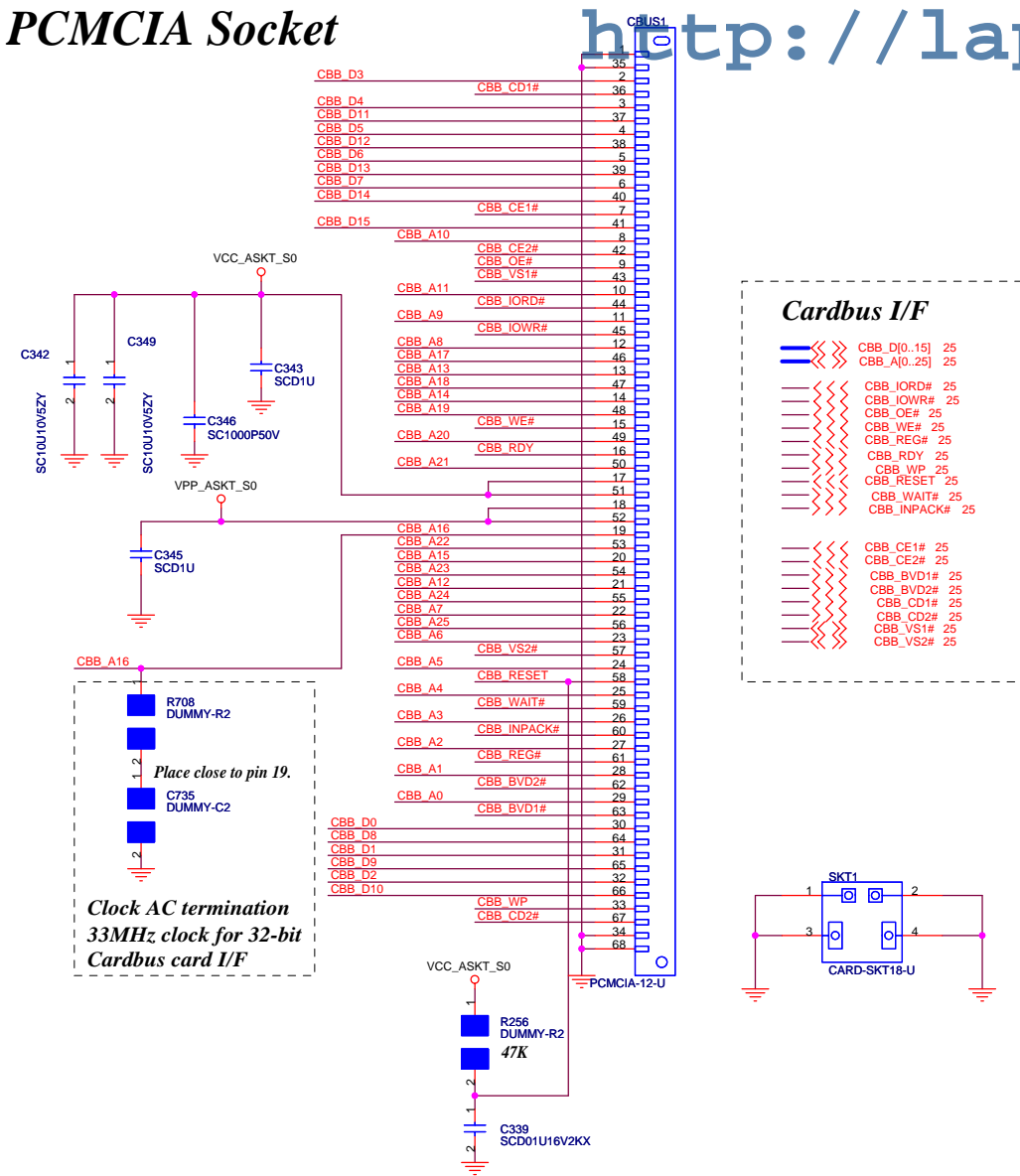
Power switch



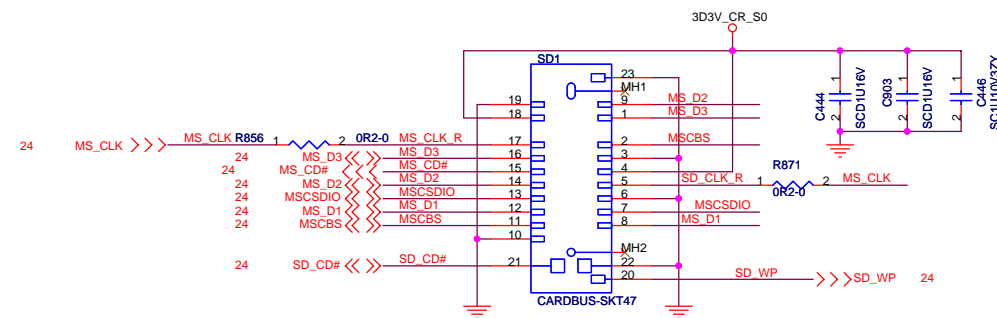
PCMCIA Socket

<http://laptopblue.vn/>

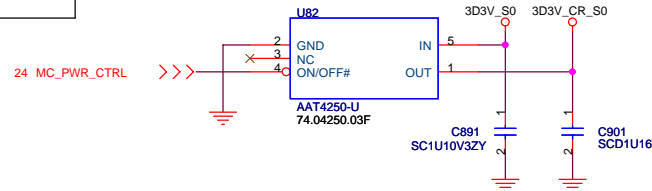
1394 Connector

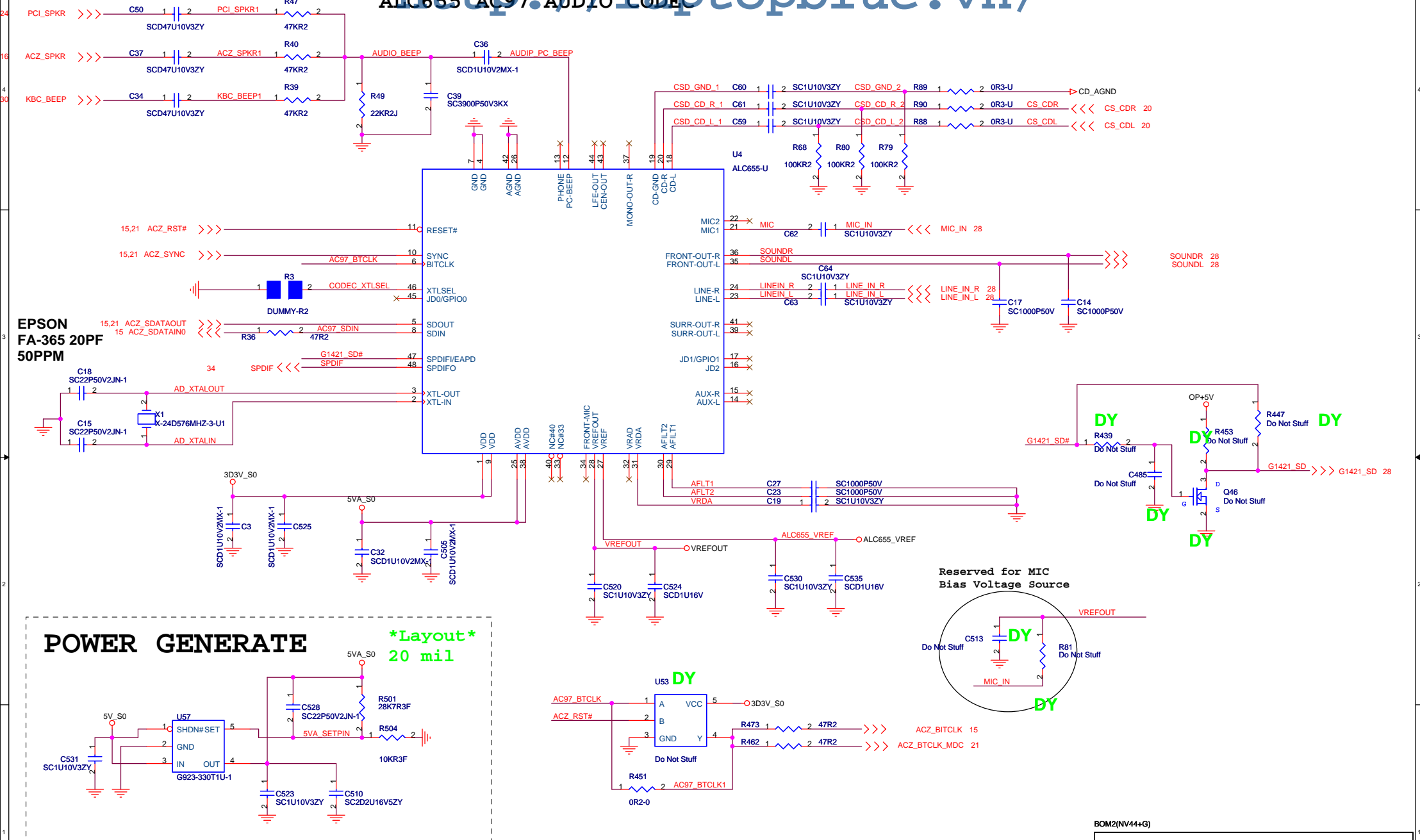


SD/MMC/MS CONN.



POWER SWITCH





BOM2(NV44+G)

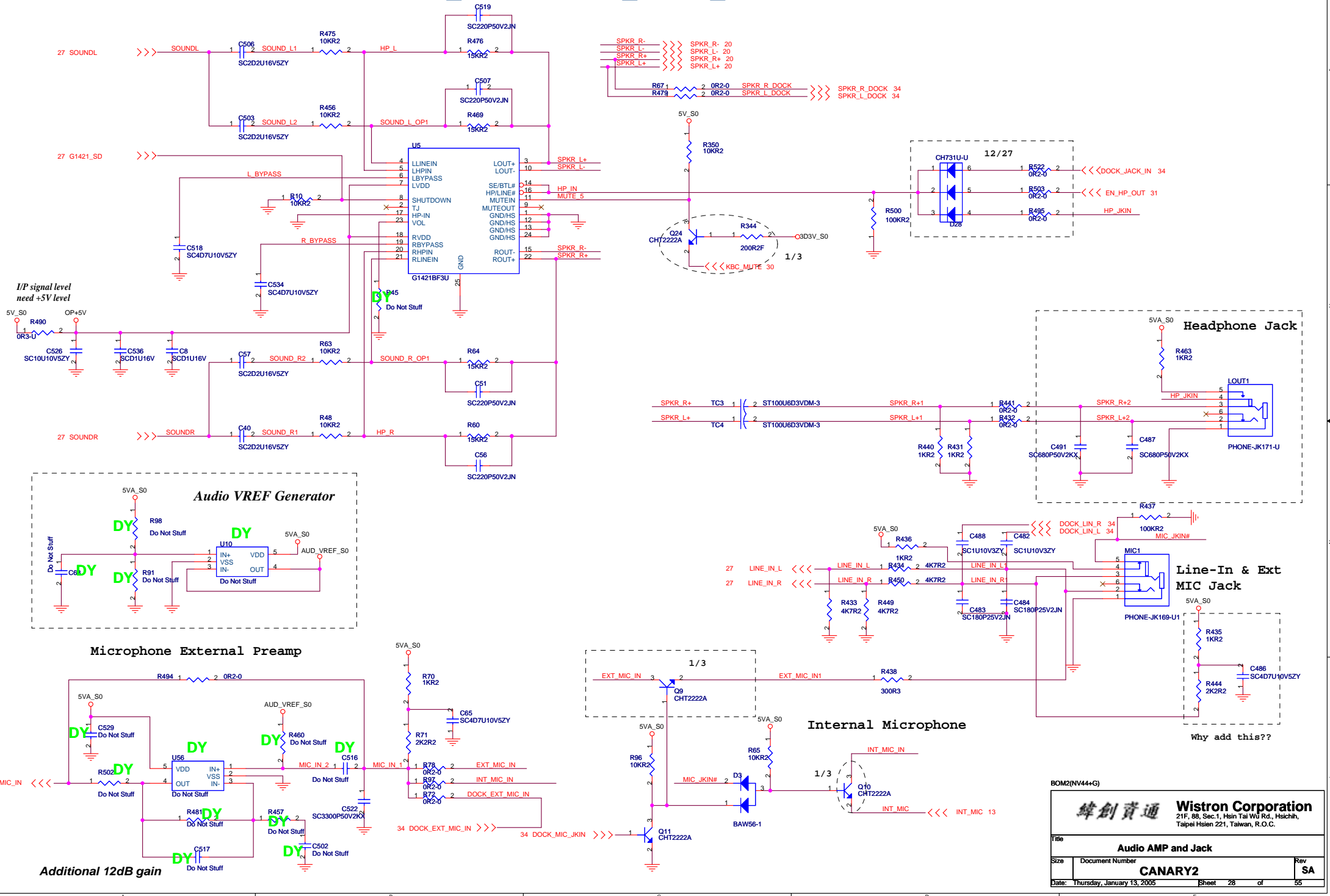
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
AC'97 CODEC - ALC655			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 27 of	55

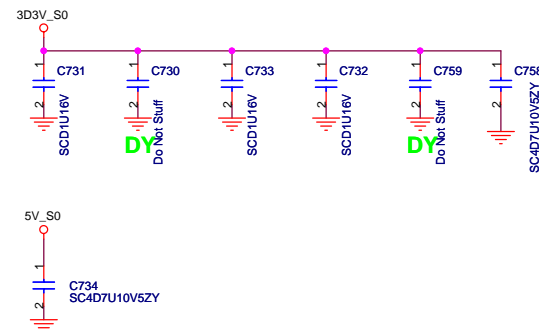
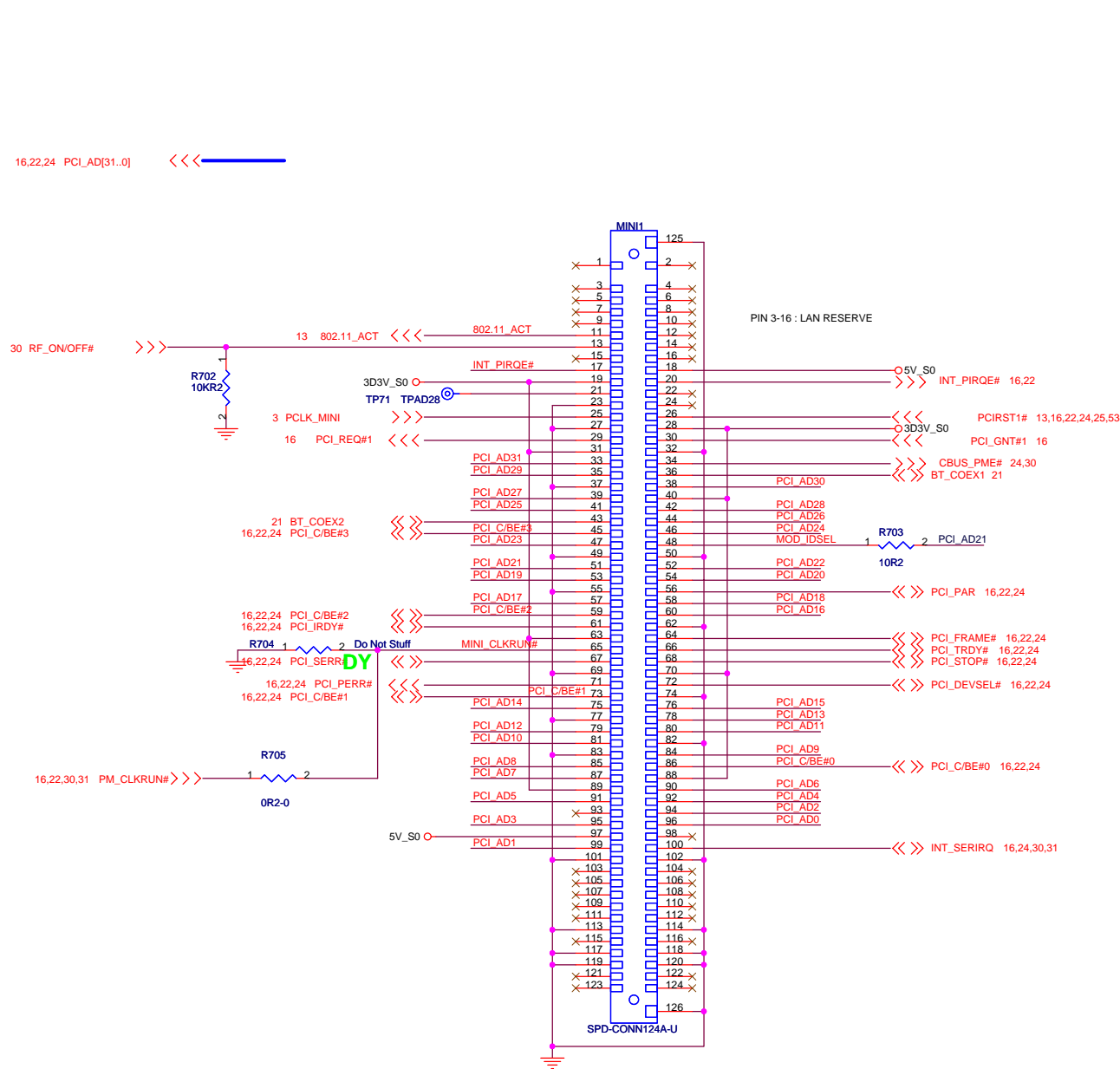
AUDIO OP AMPLIFIER

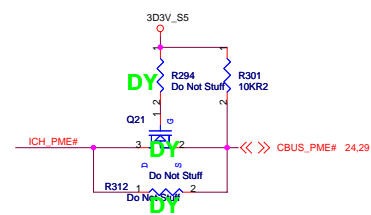
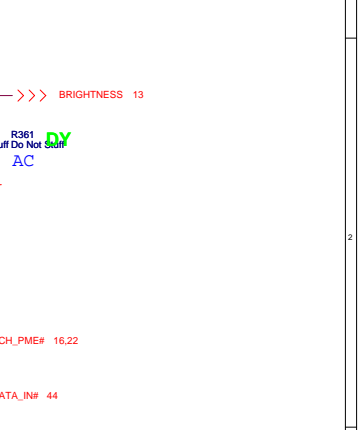
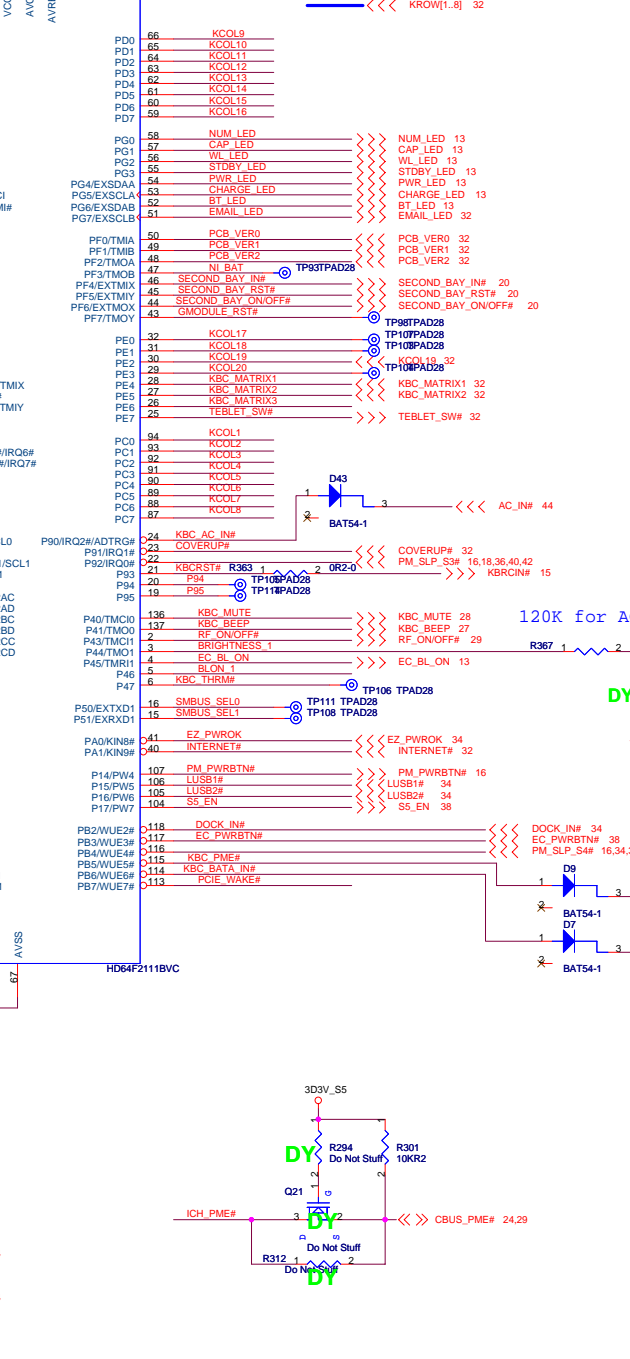
<http://laptopblue.vn/>

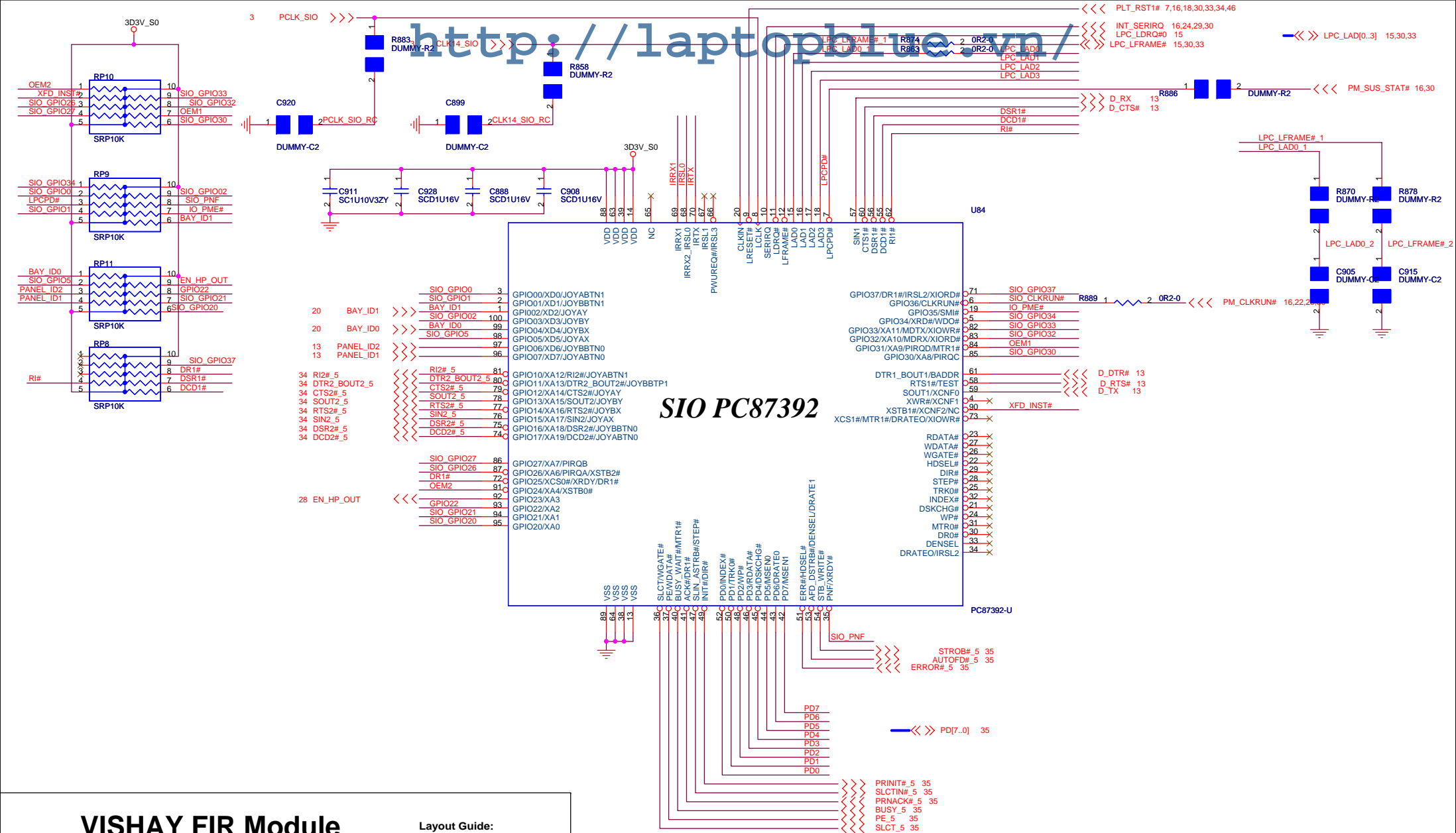


BOM2(NV44+G)

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size		Document Number	
Date: Thursday, January 13, 2005		Sheet 28 of 55	
Rev SA		CANARY2	



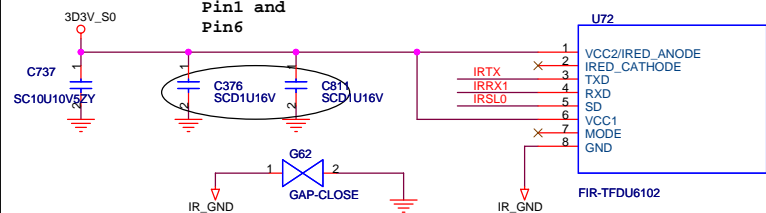




VISHAY FIR Module

Place C857
,C858 near
Pin1 and
Pin6

Layout Guide:
(1) FIR_5V : 30 mils,
(2) BCY1, BC50
close to U3



BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SIO

Size

Document Number

A3

CANARY2

Rev

SA

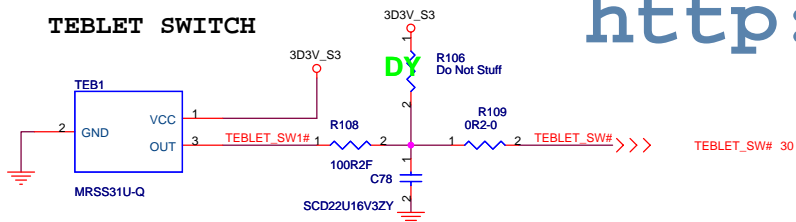
Date: Thursday, January 13, 2005

Sheet 31

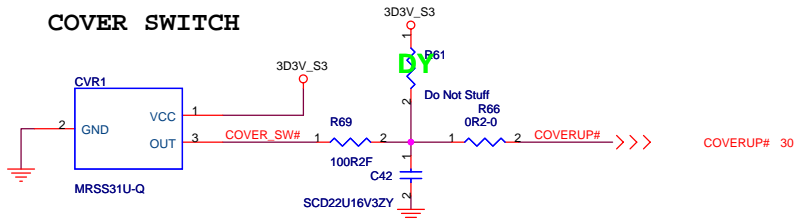
of

55

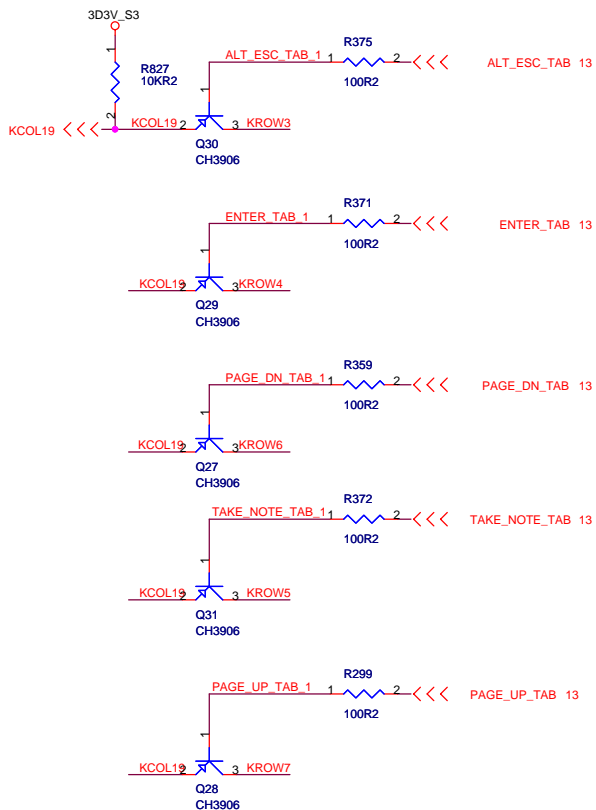
TEBLET SWITCH



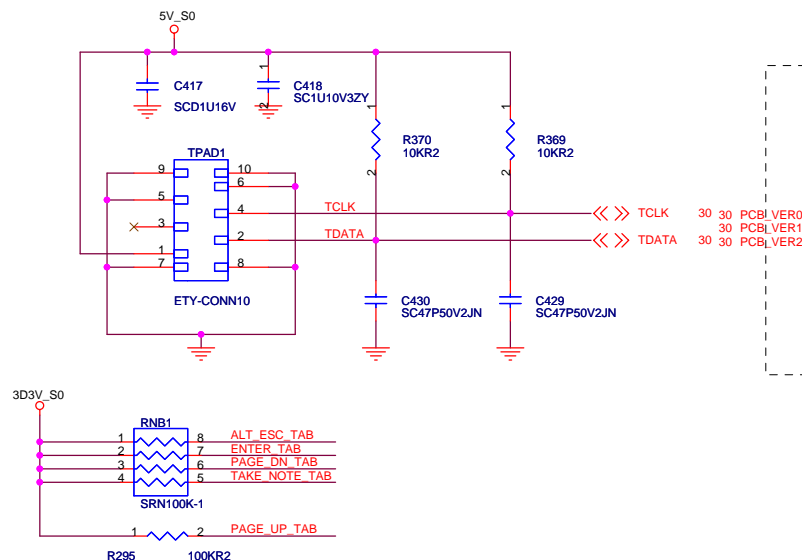
COVER SWITCH



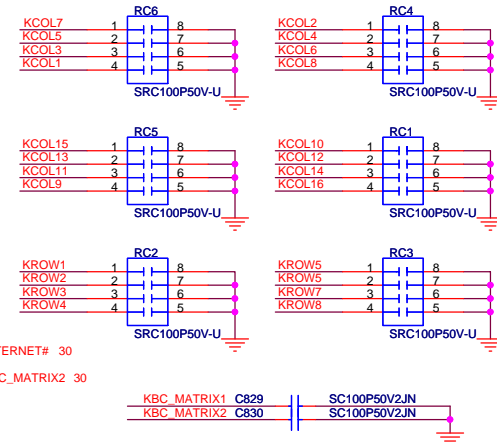
TABLET FUNCTION BUTTON



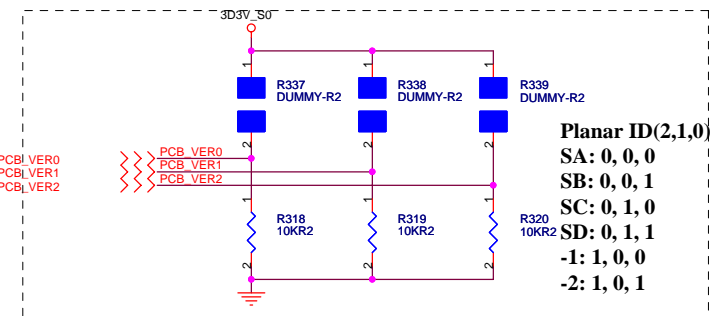
TouchPad Connector



EMI CAPS



Board ID



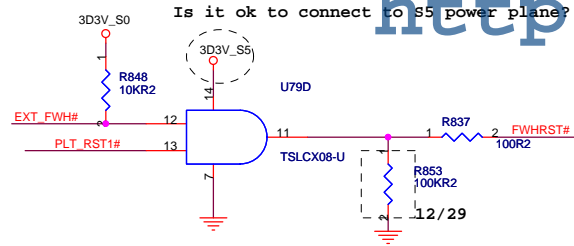
Planar ID(2,1,0)
SA: 0, 0, 0
SB: 0, 0, 1
SC: 0, 1, 0
SD: 0, 1, 1
-1: 1, 0, 0
-2: 1, 0, 1

Keyboard matrix

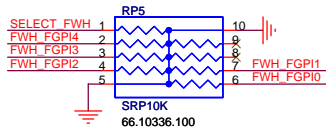
	US	Jap	Europe	US international
MATRIX1	HIGH	LOW	HIGH	HIGH
MATRIX2	HIGH	HIGH	LOW	HIGH

BOM2(NV44+G)

Title		Wistron Corporation	
Size A3		CANARY2	
Date: Thursday, January 13, 2005		Sheet 32 of 55	



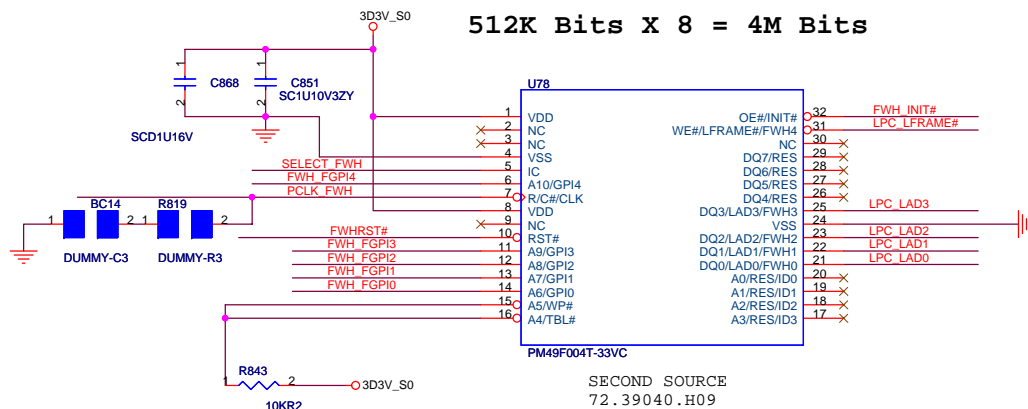
Unused FGPI pins must not be float



15,30,31 LPC_LAD[0:3] << >>

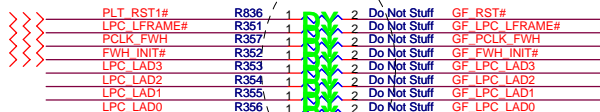
FLASH ROM

512K Bits X 8 = 4M Bits



SECOND SOURCE
72.39040.H09

7,16,18,30,31,34,46 PLT_RST1#
15,30,31 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#



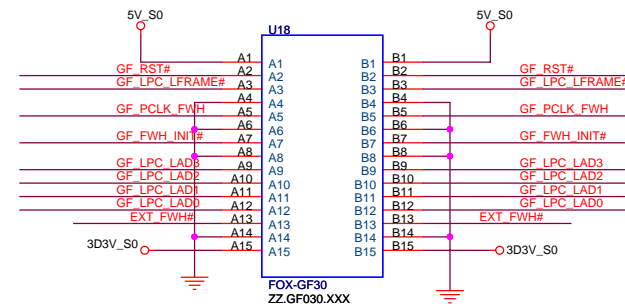
12/30

TOP VIEW

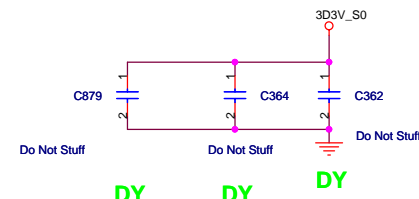
A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

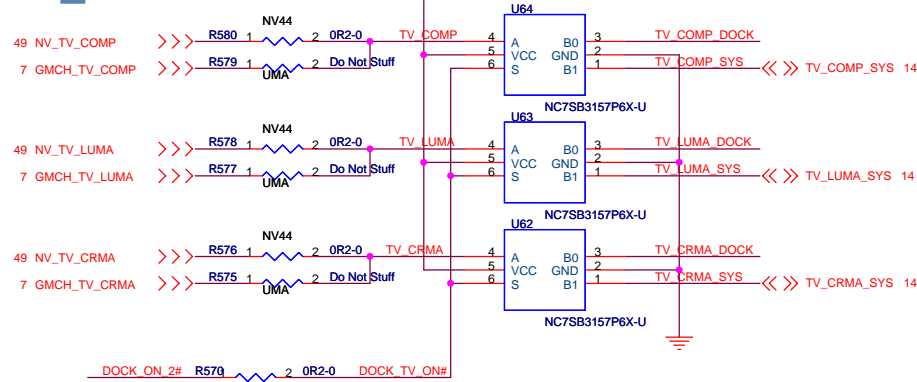
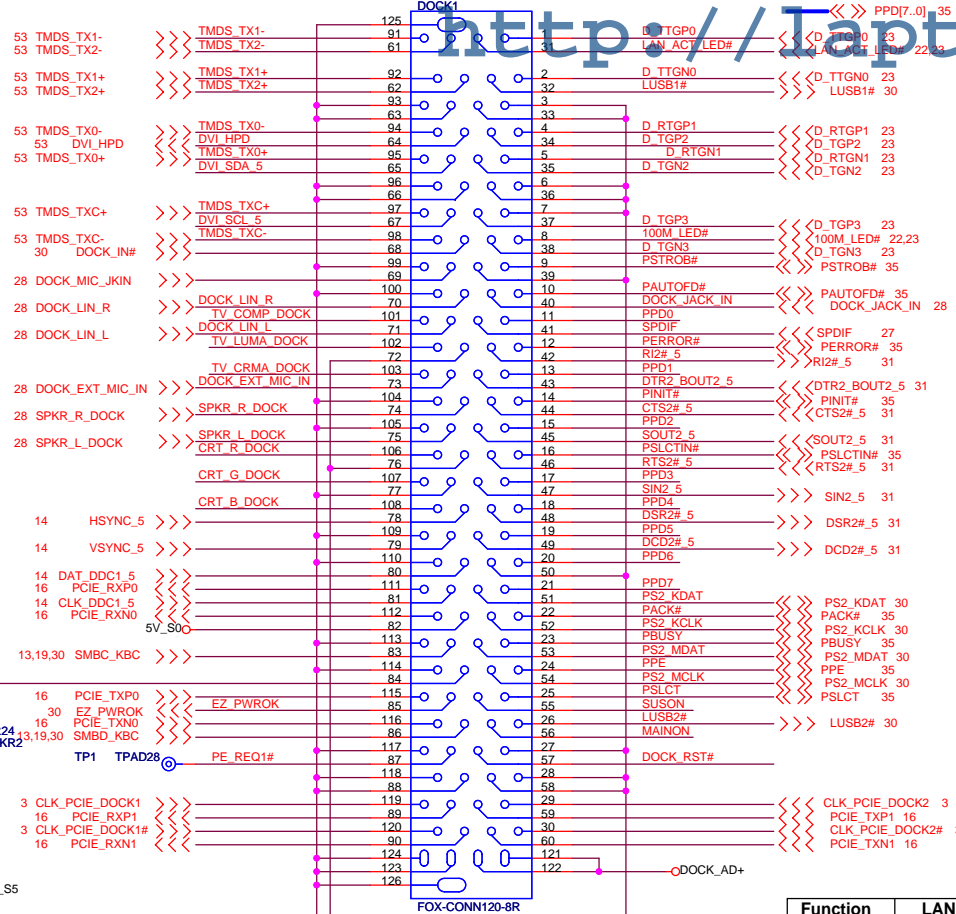


DY DY DY

BOM2(NV44+G)

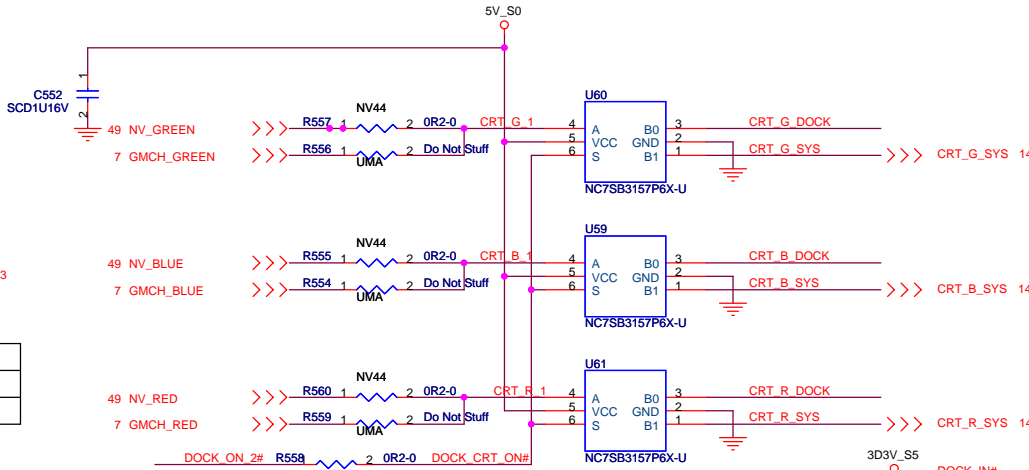
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
FHW and Debug		
Size	Document Number	Rev
A3	CANARY2	SA
Date: Thursday, January 13, 2005	Sheet 33 of 55	



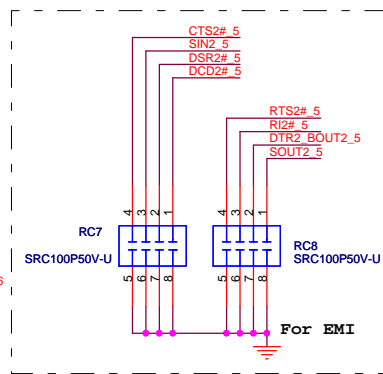
Function	S
A to B0	L
A to B1	H

CRT SWITCH



Function	LAN
SYSTEM	L
DOCK	H

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L



BOM2(NV44+G)

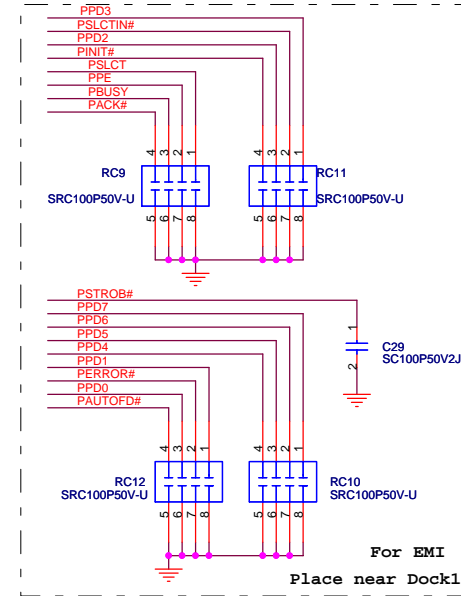
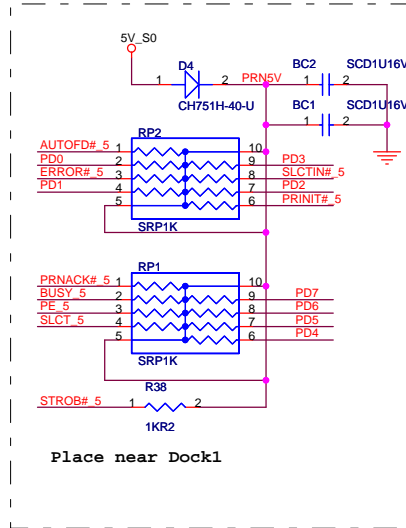
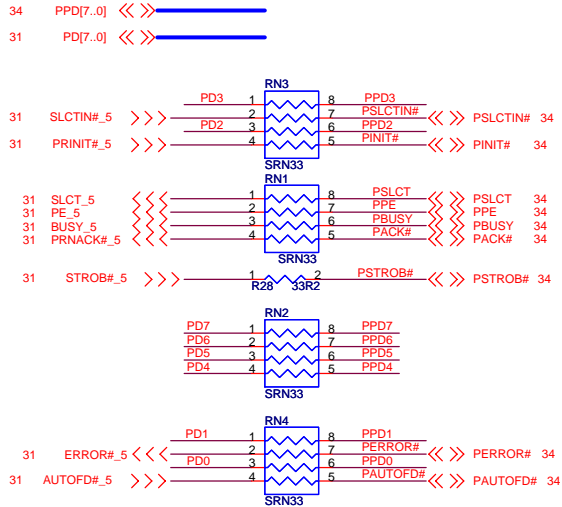
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

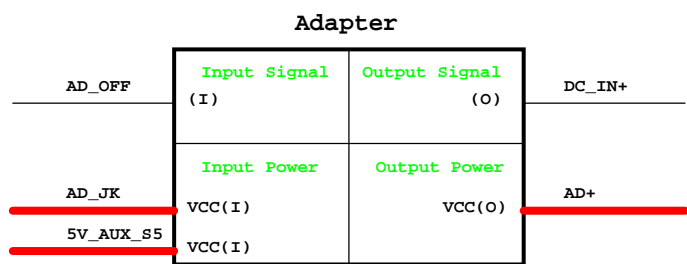
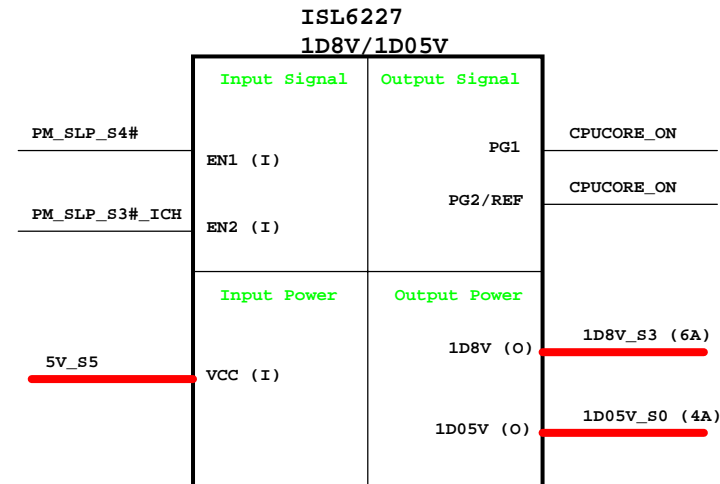
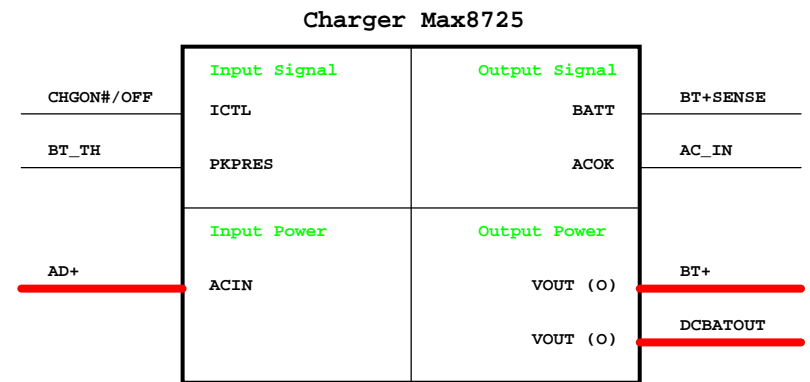
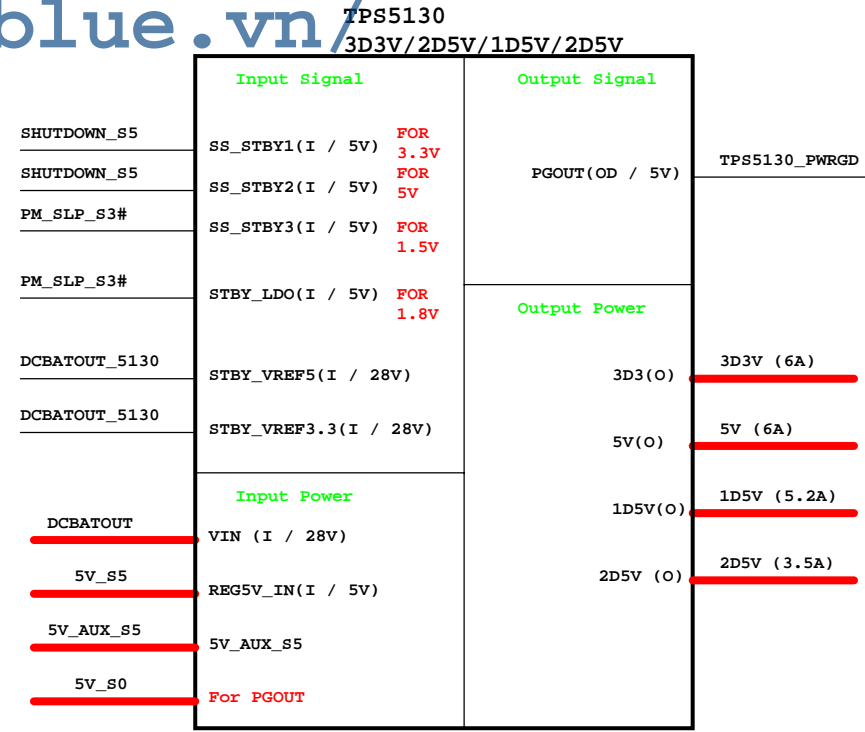
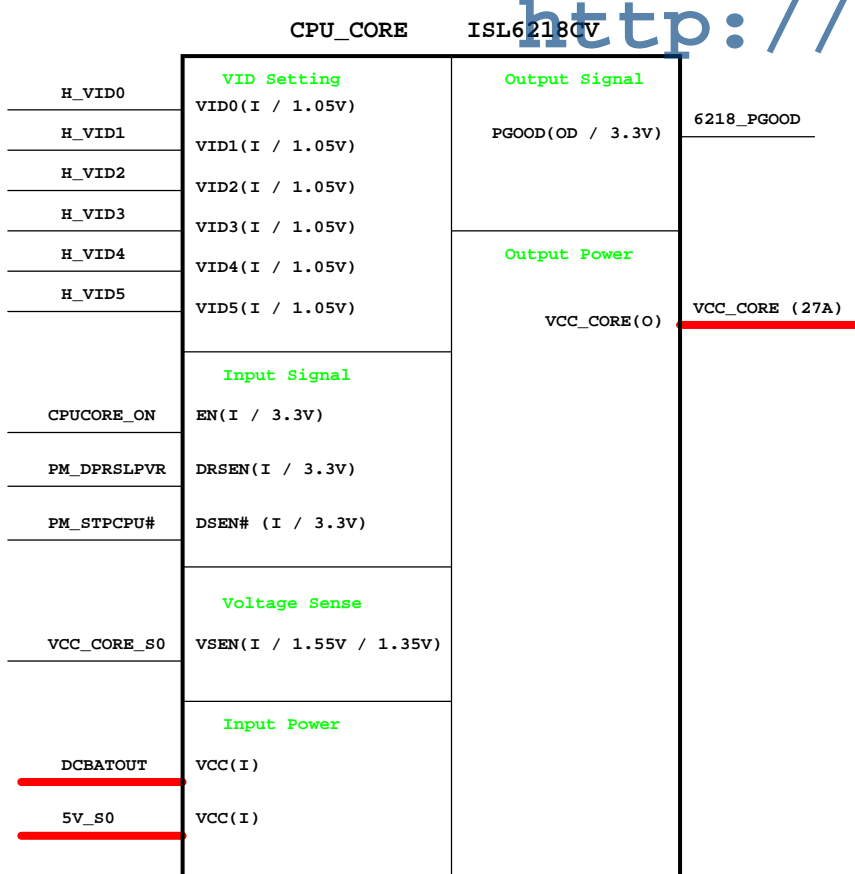
Title: **EASY PORT4 (1/2)**

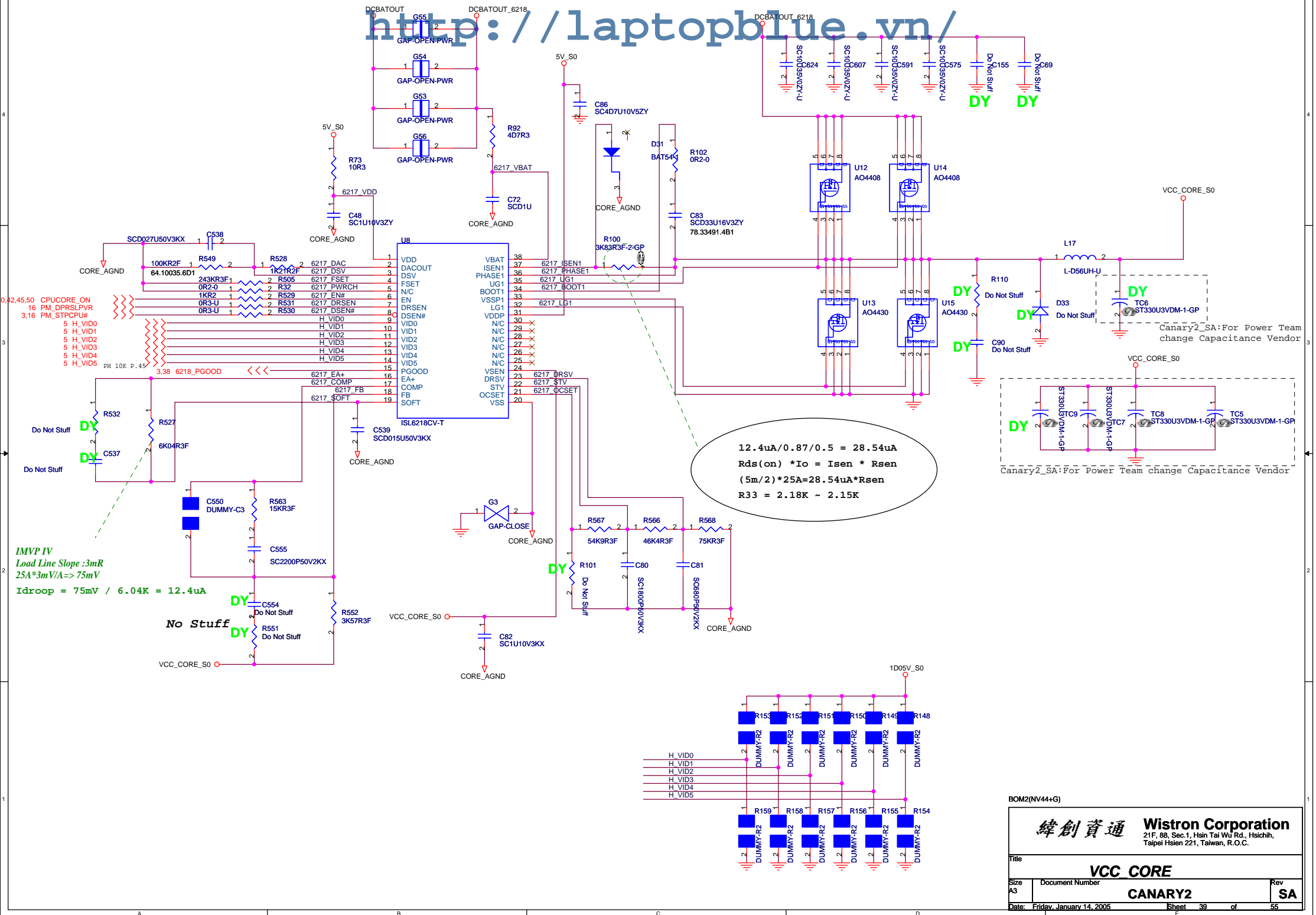
Size: A3 Document Number: **CANARY2** Rev: **SA**

Date: Thursday, January 13, 2005 Sheet: 34 of 55

PRINT PORT

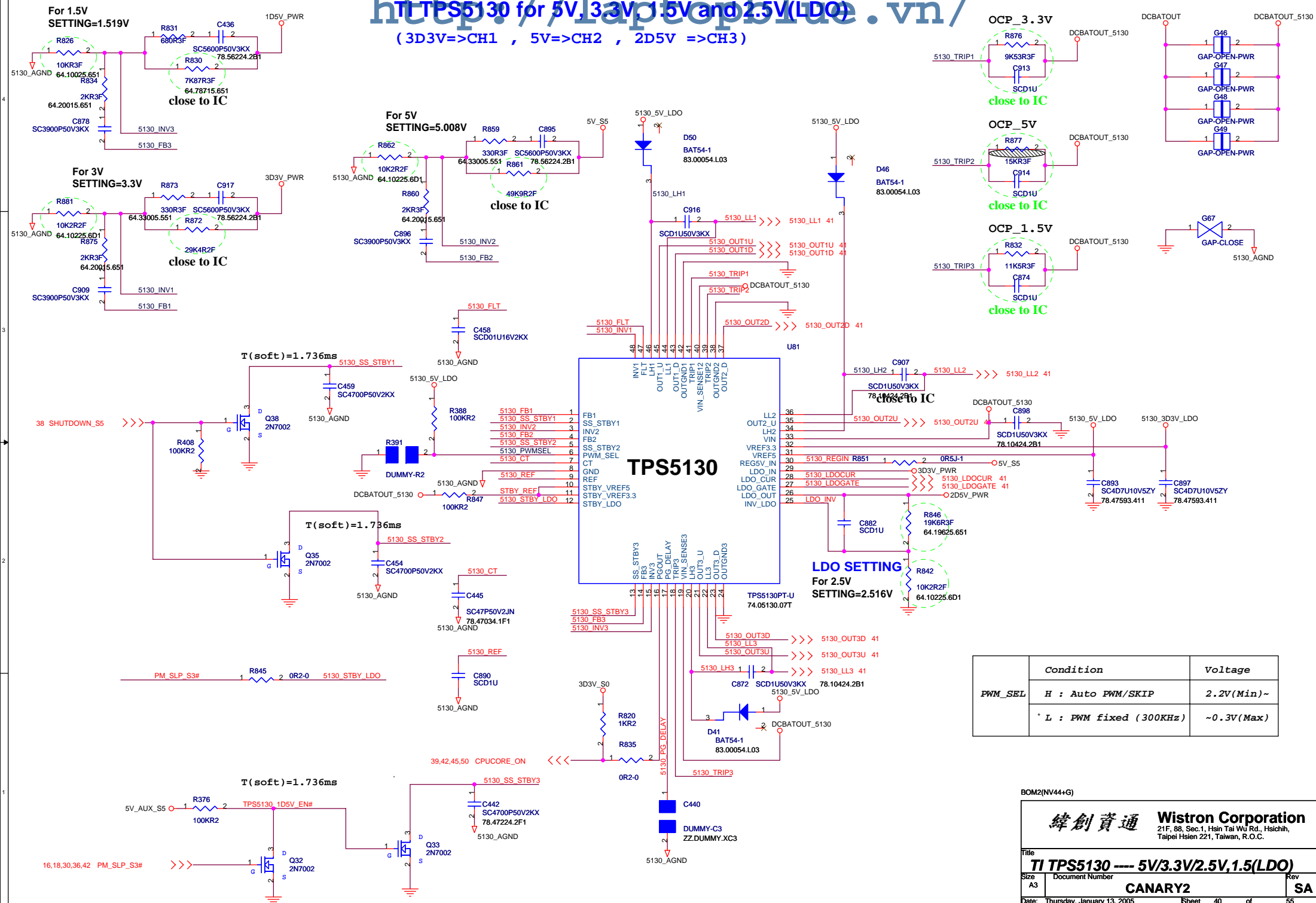






<http://laptopblue.vn/> TI TPS5130 for 5V, 3.3V, 1.5V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)

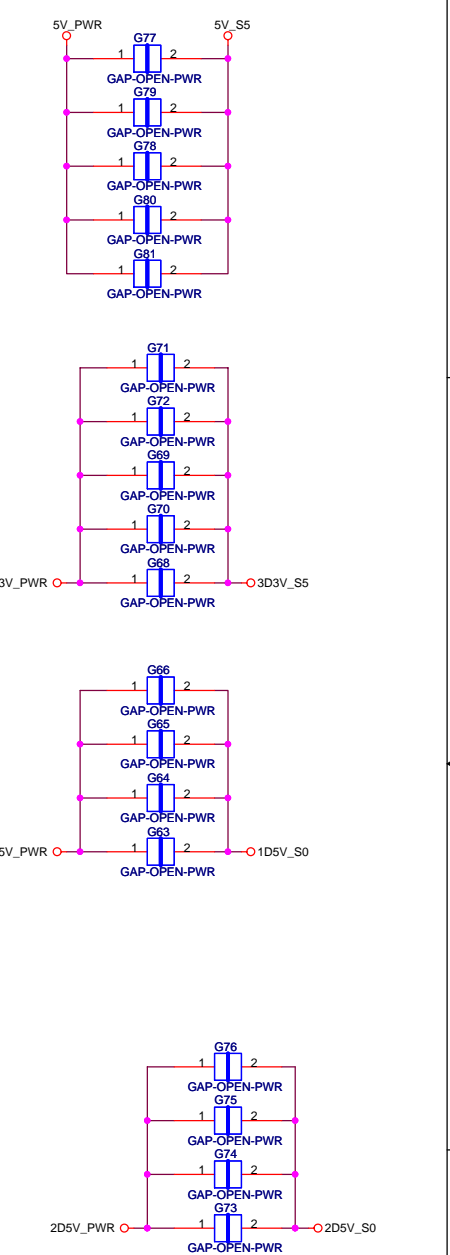
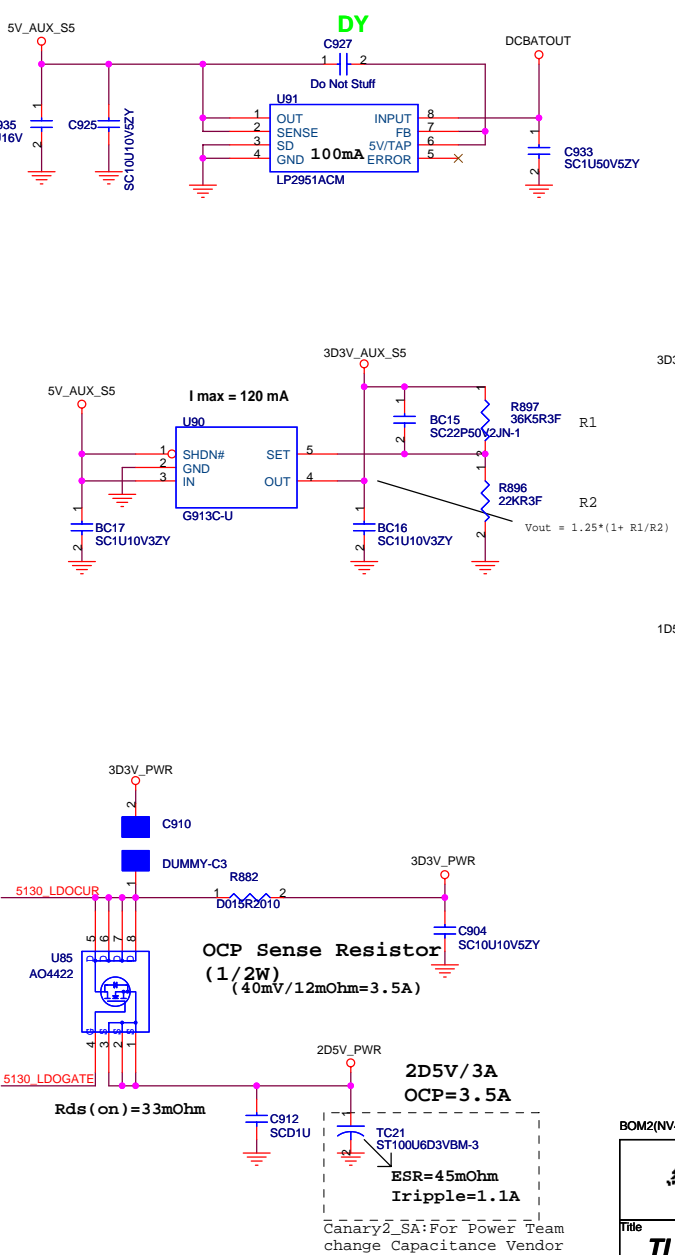
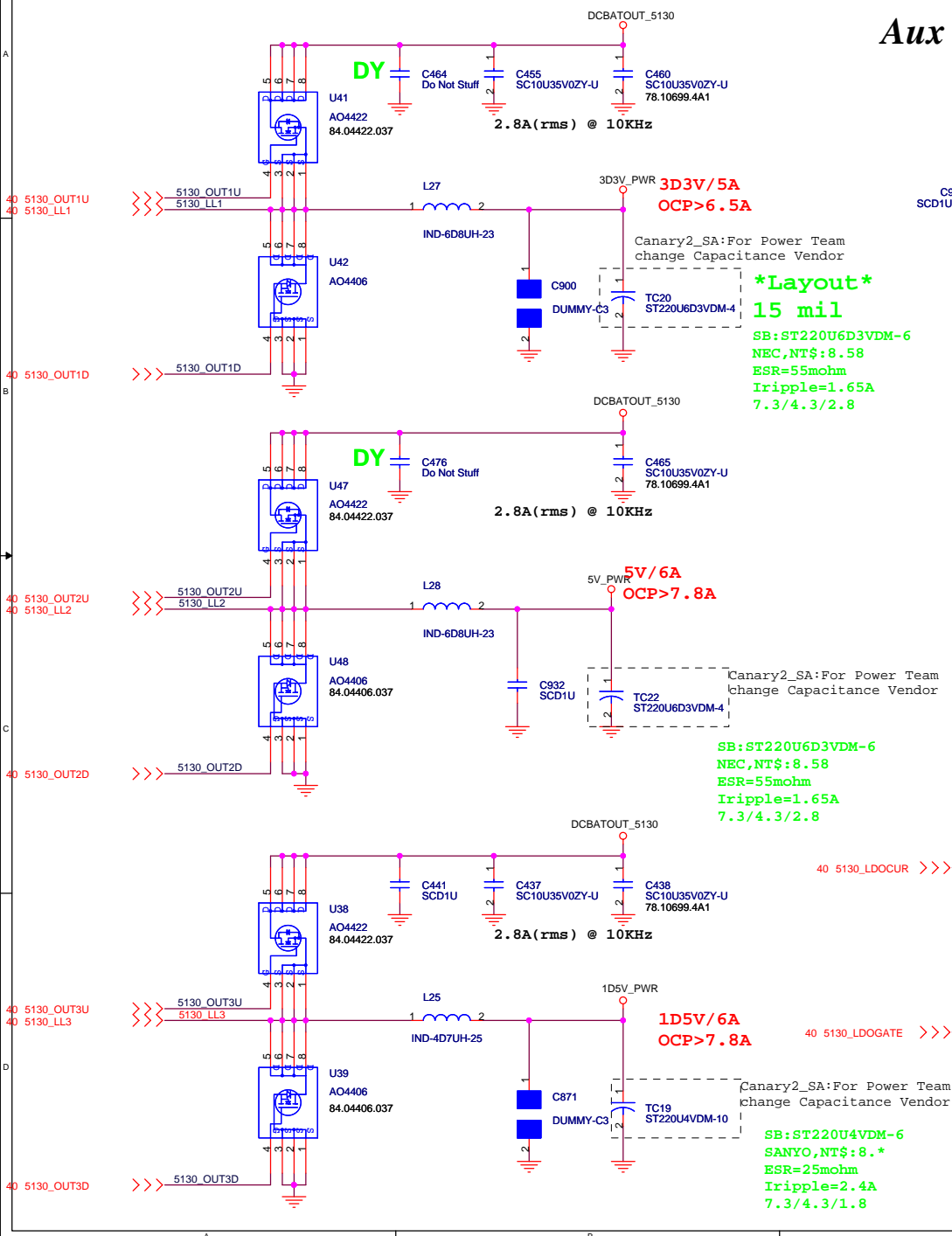


TI TPS5130 for 5V, 3.3V, 1.5V and 2.5V(LDO)

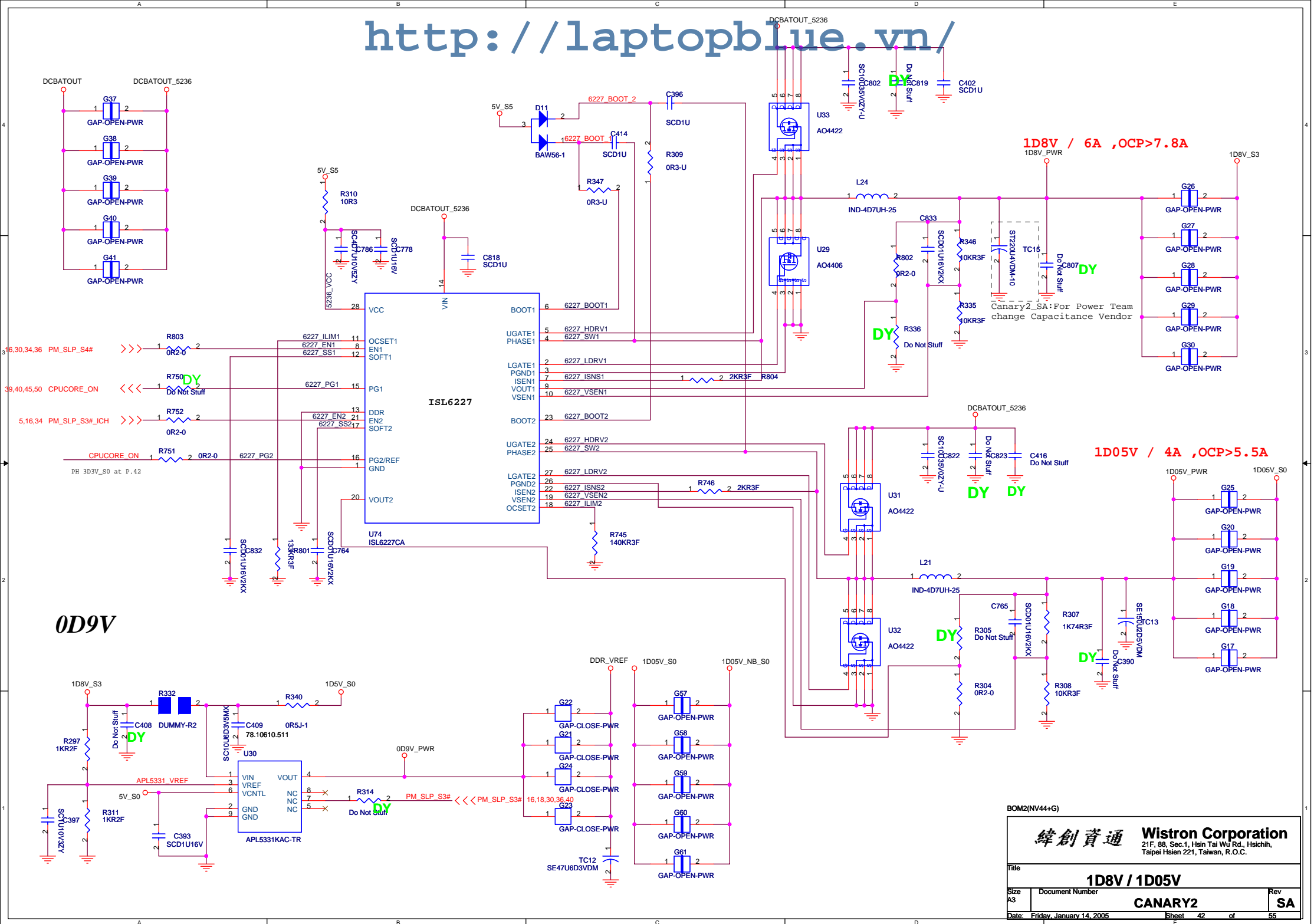
(3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)

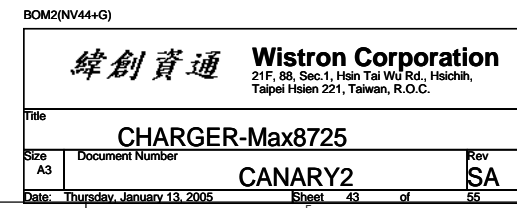
http://laptopblue.vn/

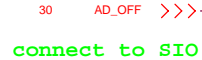
Aux Power



<http://laptopblue.vn/>



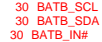




DY



9 Not Stuff



Adaptor IN Detection



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Size	Document Number
------	-----------------

Size A3	Document Number CANARY2
------------	-----------------------------------

Date: Monday, January 17, 2005

Sheet

Rev

55



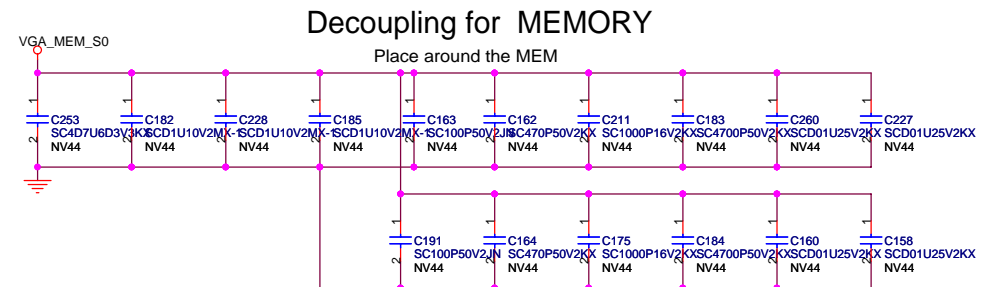
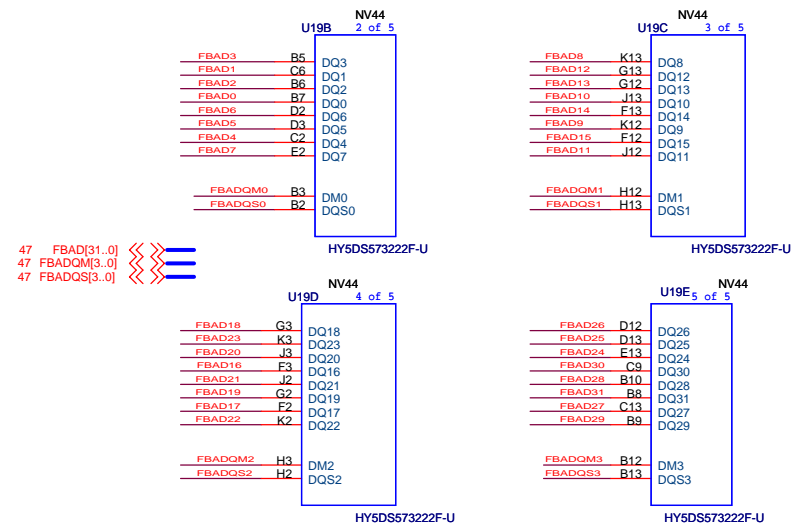
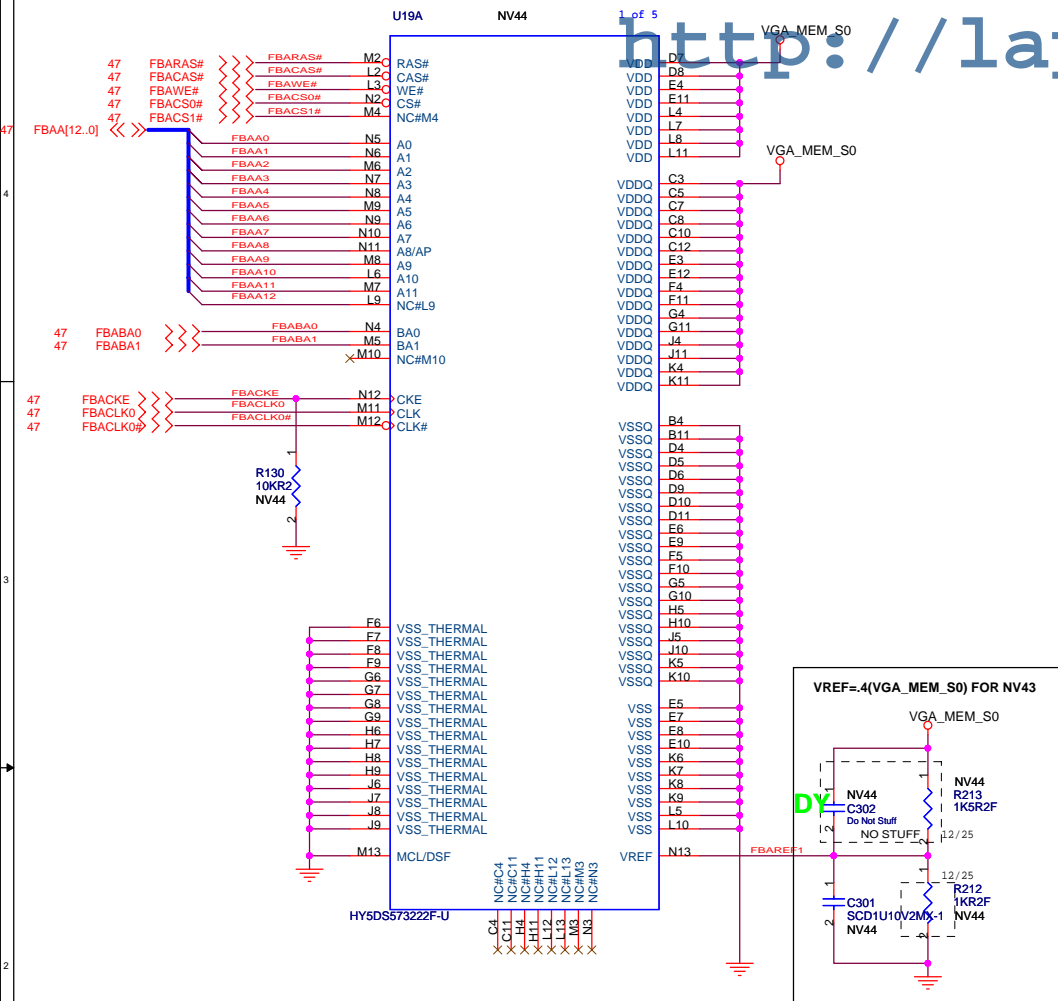
1 of 5

VGA-MEM S0

D7

D8

http://laptopblue.vn/



Must be placed as close as possible to minimize the stub length!!

BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

NV44M-Memory Interface

Size
A3

Document Number

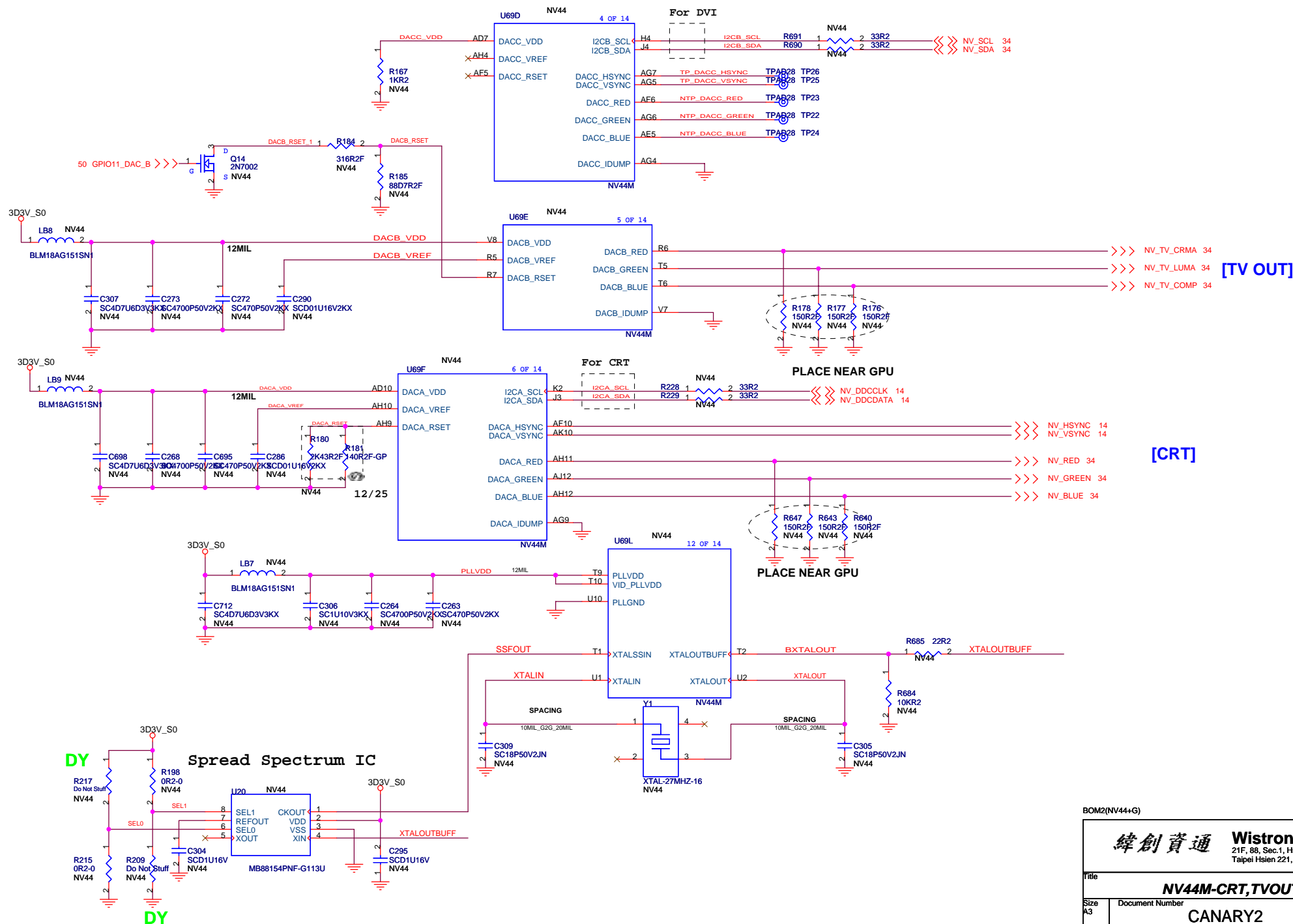
CANARY2

Rev
SA

Date: Thursday, January 13, 2005

Sheet 48

55

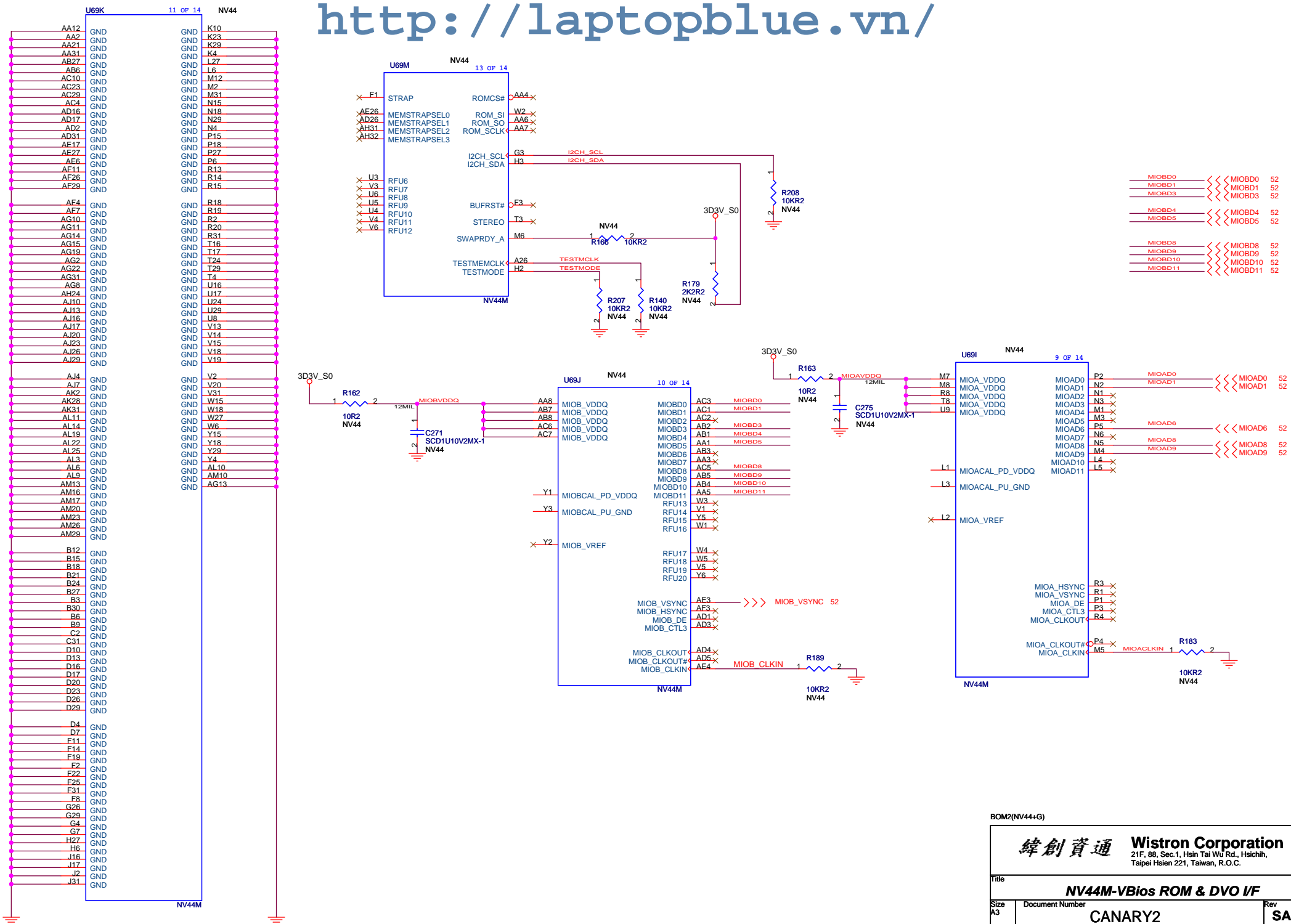


BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
NV44M-CRT,TVOUT			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 49 of	55

<http://laptopblue.vn/>

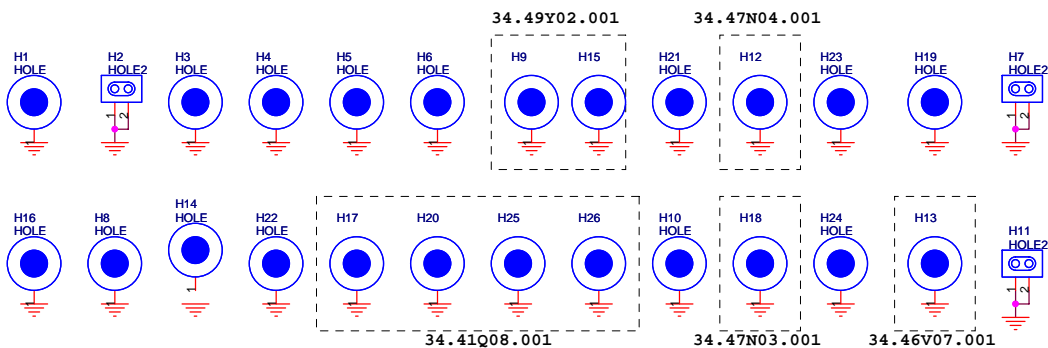
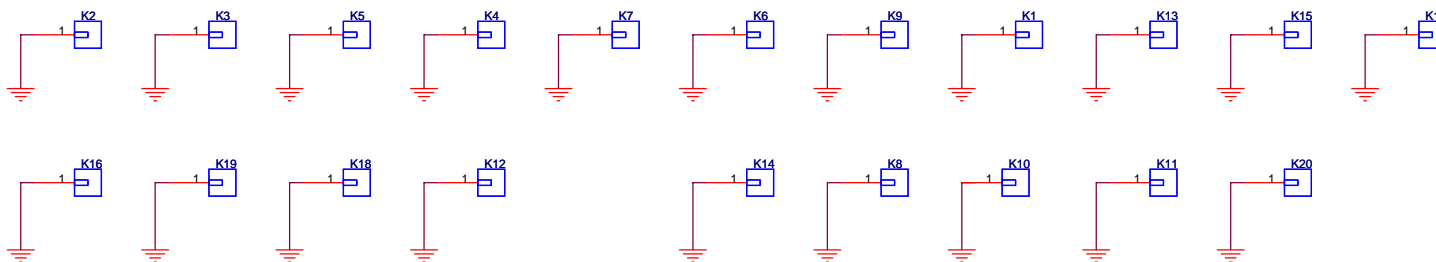
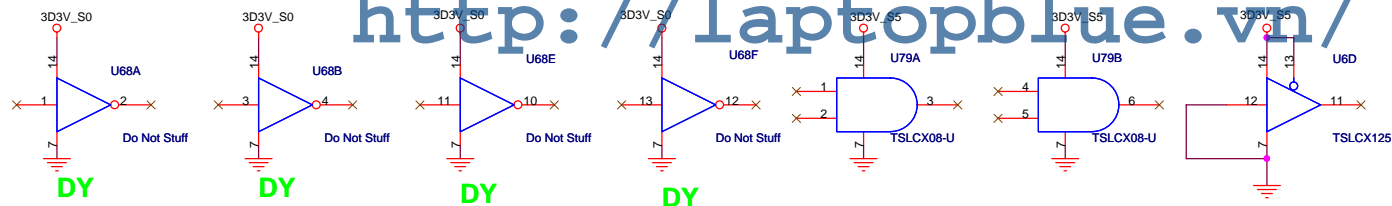


BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			NV44M-VBios ROM & DVO I/F		
Size	Document Number	CANARY2			Rev
A3					SA
Date: Thursday, January 13, 2005			Sheet	51	of 55

<http://laptopblue.vn/>



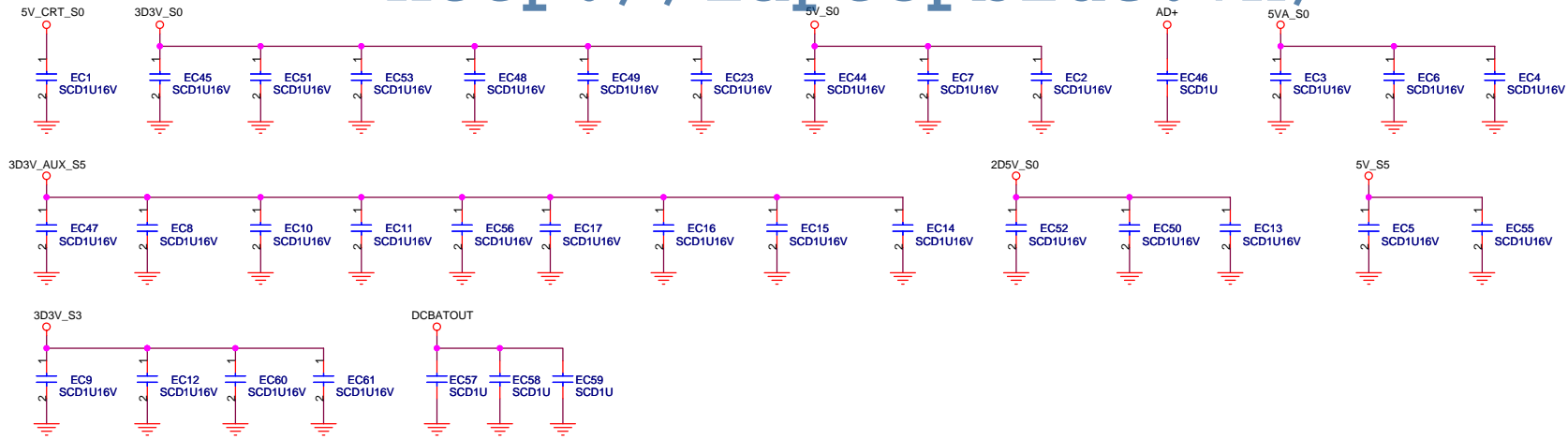
BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		SPRING, BOSS & UNUSED TTL	
Size	Document Number	CANARY2	Rev
A3			SA
Date: Thursday, January 13, 2005		Sheet	54 of 55

BYPASS CAP

<http://laptopblue.vn/>



CROSS PLANE CAP

BOM2(NV44+G)

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
EMI SOLUTION			
Size	Document Number		Rev
A3	CANARY2		SA
Date:	Thursday, January 13, 2005		Sheet 55 of 55