

**ACER_BAP10/BXP10
MAIN BOARD---A01**

2010.04.02

INVENTEC			
TITLE			
ACER_BAP10/BXP10			
TIME			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01
SHEET		1	of 45

1. Schematic Page Description

Montavina Schematic Ver : X01

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Power Block Diagram

5. Annotations

6. Schematic Modify

7. Timing Diagram

8. PWR_Adaptor in/Charge

9. PWR_CPU Core Power

10. PWR_Graphics Core

11. PWR_DDR PWR

12. PWR_1.1VS_VTT/1.1VS

13. PWR_5VA/5VLA/3VA/3VLA

14. PWR_3VS/5VS/1.8VS/5VUSB

15. PWR_Reserve

16. Processor(1/4)
17. Processor(2/4)

18. Processor(3/4)

19. Processor(4/4)

20. PCH_RTC,SATA,PCI-E,CLK

21. PCH_DMI,MISC,LVDS,CRT

22. PCH_USB, PCI,NVRAM,XDP

23. PCH Power 1

24. PCH Power 2

25. PCH Power 3 (GND)

26. Clock Generator

27. DDR3 SDRAM SO-DIMM 0/1

28. LCD,CMA,CRT PLUG

29. USB/MDC

30. LAN(BCM57760)

31. CX20672-11Z / MIC / SPK

32. UMTS/WLAN
33. HDD/BT/TPM/GP/FP/LID

34. CR_AU6437-GEF

35. KBC ITE8502E*

36. EASY PORT

37. Hybrid Switch (1/2)

38. POWER SEQUENCE

39. SW/LED

40. FP board

41. GP Button board

42. SW Button/BAP10 board

43. SW Button/BXP10 board

44. LED Board/BXP10 board

41. TPM board

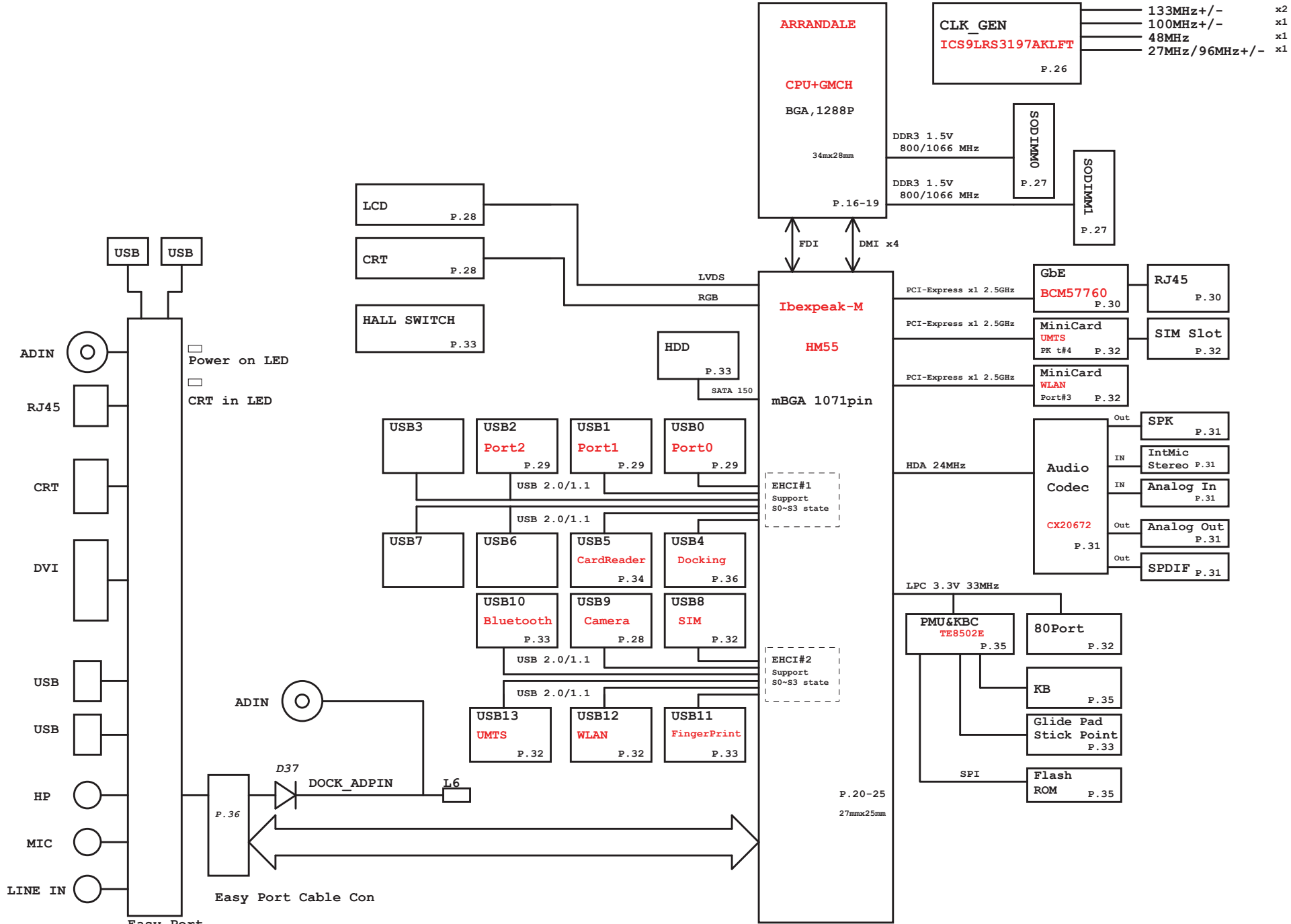
2. PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	Interface	REQ	CHIP
None		None			None	

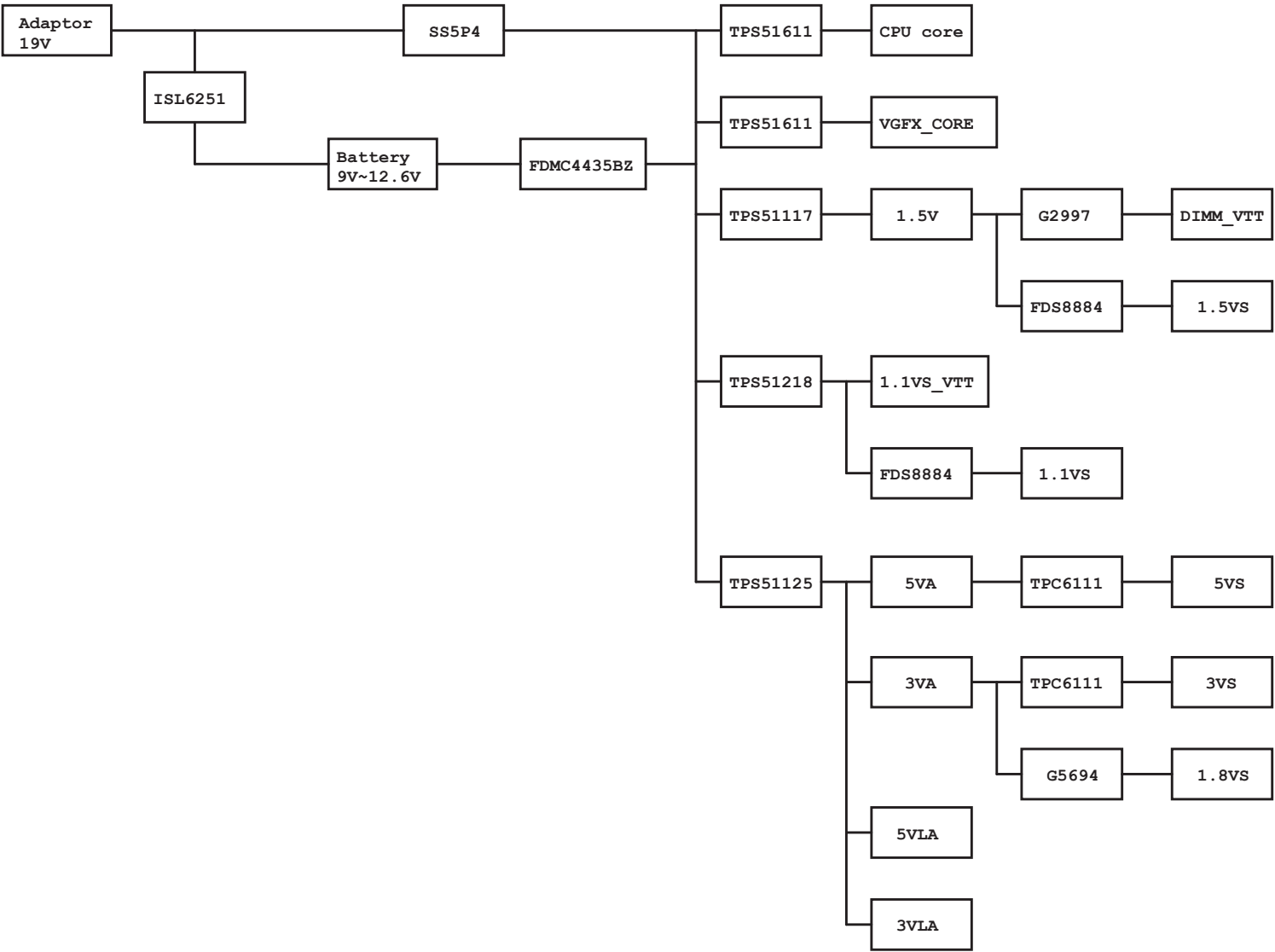
3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE	PCI-E	DEVICE	SATA	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth	Port 1	New Card	Port 1	HDD
Port 1	System	Port 8		Port 2	Docking	Port 2	E-SATA
Port 2	System	Port 9	Web Cam	Port 3	Mini Card(WLAN)	Port 4	BAY
Port 3	System	Port 10		Port 4	Mini Card(3G)	Port 5	None
Port 4	CardReader	Port 11	FingerPrint	Port 5	Mini Card(ROBSON)		
Port 5		Port 12		Port 6	Giga-LAN		
Port 6		Port 13	3G				

3. Block Diagram : <http://laptopblue.vn/>



Power Block Diagram: <http://laptopblue.vn/>



4. Net name Description

Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC 3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG_1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#

Vcore_CPU Core switched power rail for CPU

Part Naming Conventions





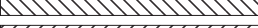


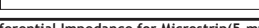
C = Capacitor	Q = Transistor
CN = Connector	R = Resistor
D = Diode	RP = Resistor Pack
F = Fuse	U = Arbitrary Logic Device
L = Inductor	Y = Crystal and Osc

Name Suffix

= Active Low signal
NU = No Stuff

5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM: LFM	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
1.05VS	Penryn: AGTL+ termination Cantiga GM: Core Cantiga GM: PCIE Cantiga GM:Core+IMEL+HSIO Cantiga GM:VCC_GMCH Cantiga GM:VCCA_SM_CK and NCTF Cantiga GM:VCC_DMI Cantiga GM:VCCA_SM Cantiga GM:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn PLL Cantiga GM: QDAC Cantiga GM: LVDS Cantiga GM: TVDAC Cantiga GM: Various PLLS analog supply Cantiga GM: VCC_SM_CK Cantiga GM: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V-1.5V-1.575V	650mA
0.75VDDT_DDRIII:DDRIII Terminator:		0.7125V-0.75V-0.7875V	3.1A(800M) 4.1A(1067M)
3VS	Cantiga GM: HV CMOS Cantiga GM: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS397BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:82567LM Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 1.0V and 1.8V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A Each 1A
5VS	Cardreader: GL827 Azalia Codec: ALC262 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB and ESATA	5VA 5VA	1A 1.5A 2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

TITLE

ACER BAP10/BXP10

SIZE Custom CODE CS DOCNUMBER CS-131 REV A01

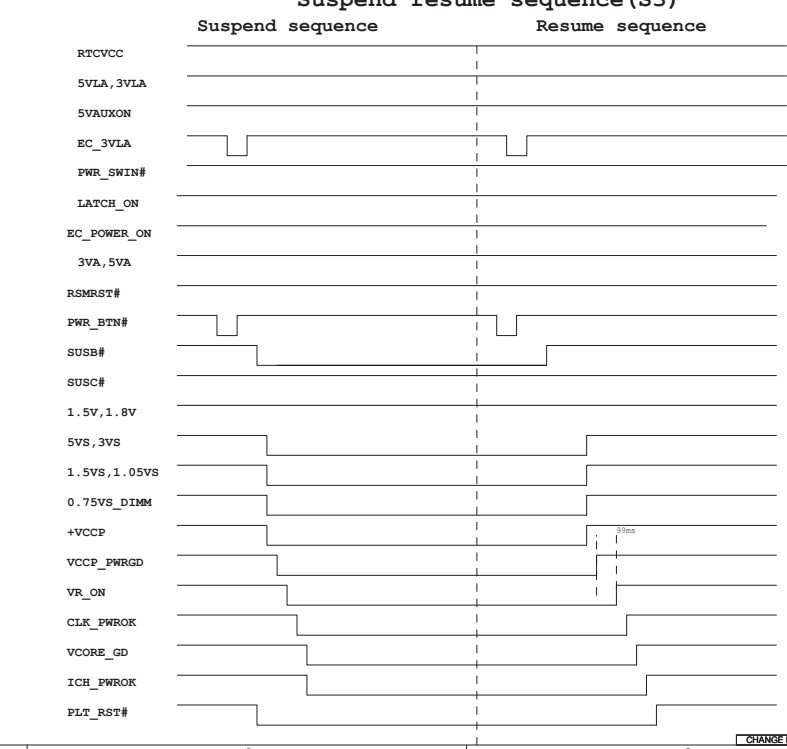
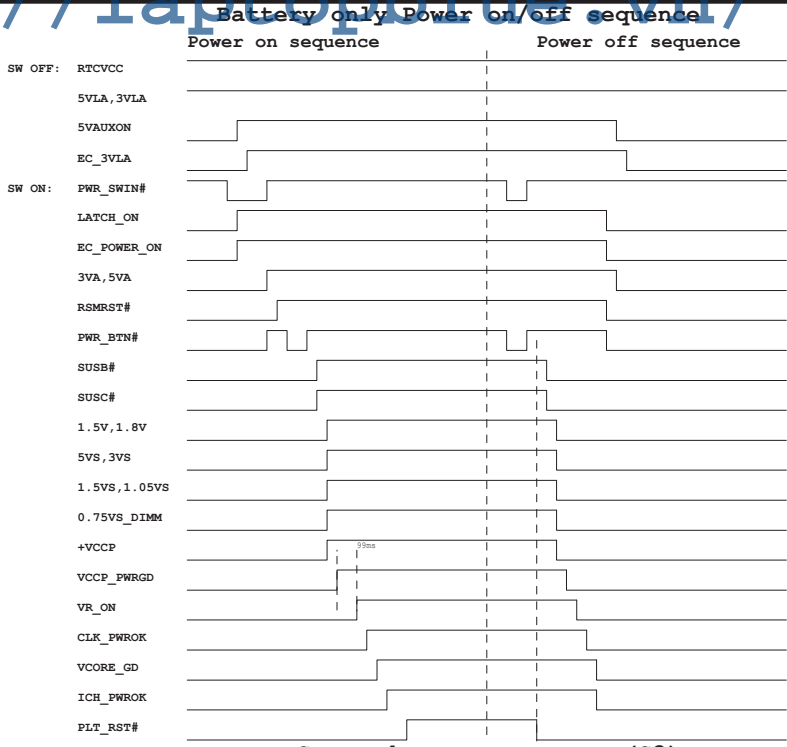
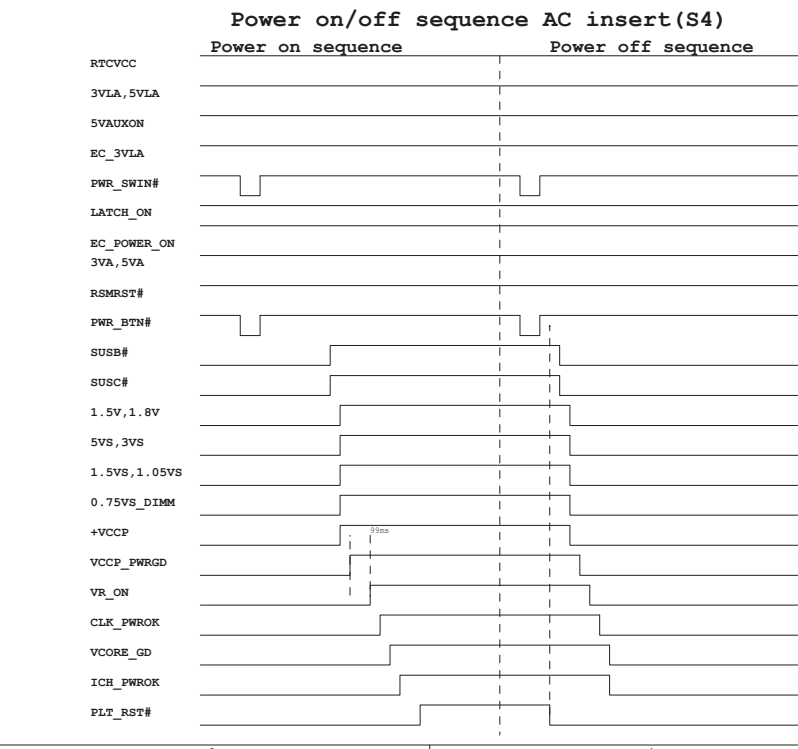
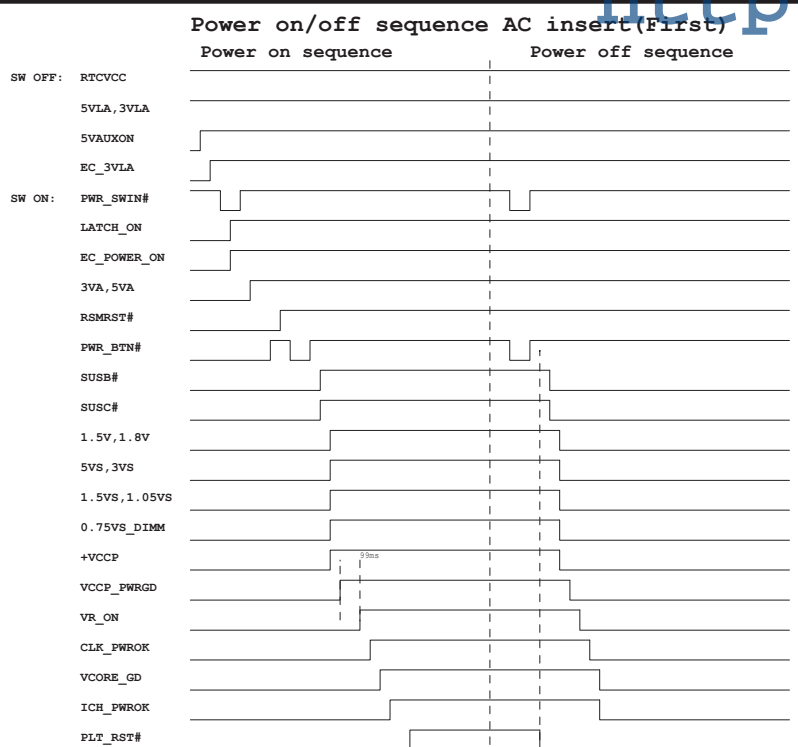
SHEET 5 of 45

6.Schematic modify Item and History :

<http://laptopblue.vn/>

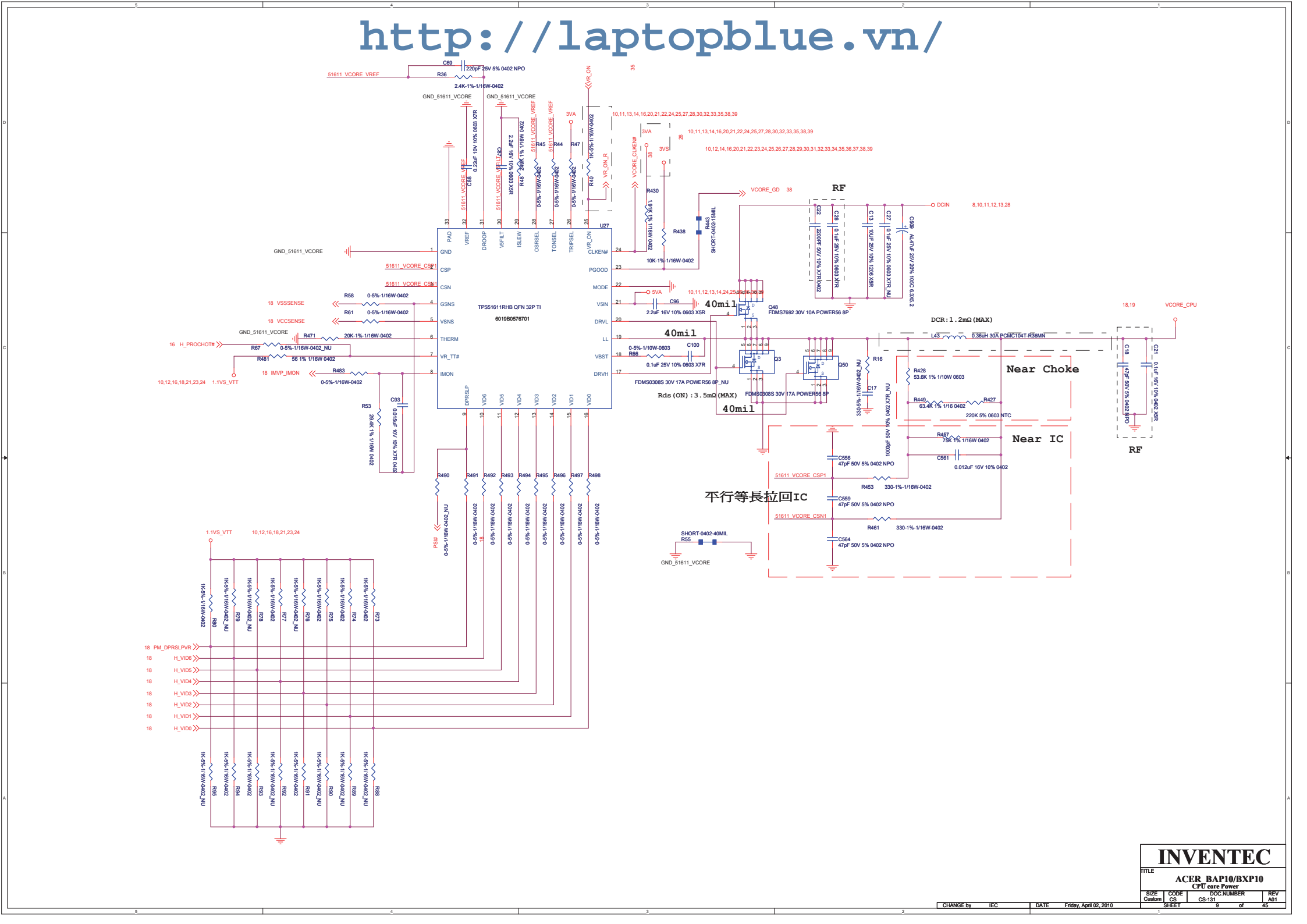
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TITLE			
ACER BAP10/BXP10			
schematic modify			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	AX1
SHEET 8 of 45			

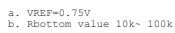
8.SYSTEM POWER SEQUENCE : <http://laptopblue.vn/>





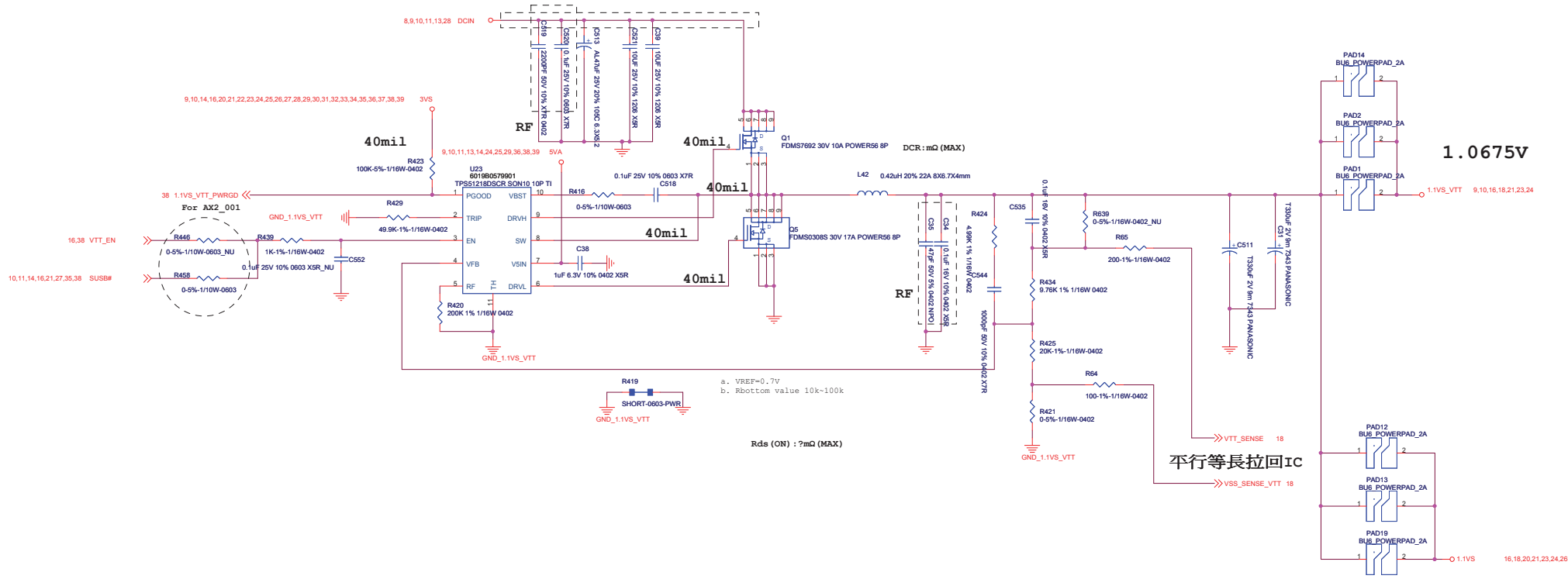
CHANGE by		IEC	DATE	Friday, April 02, 2010	Custom	CA	CA-131	
					SHEET 8 of 45			



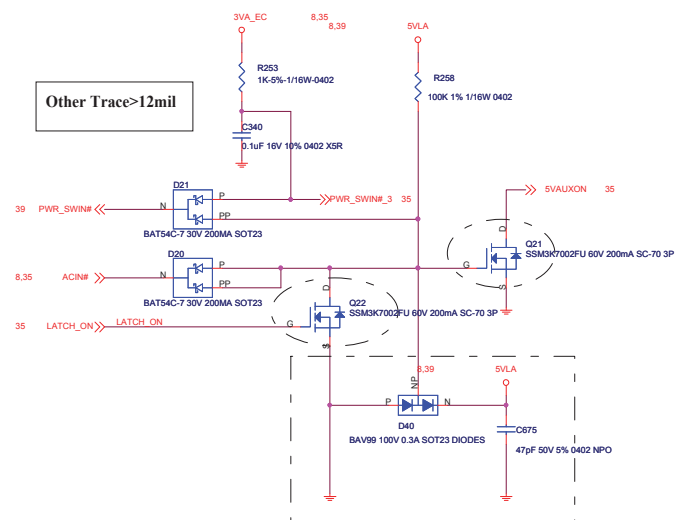
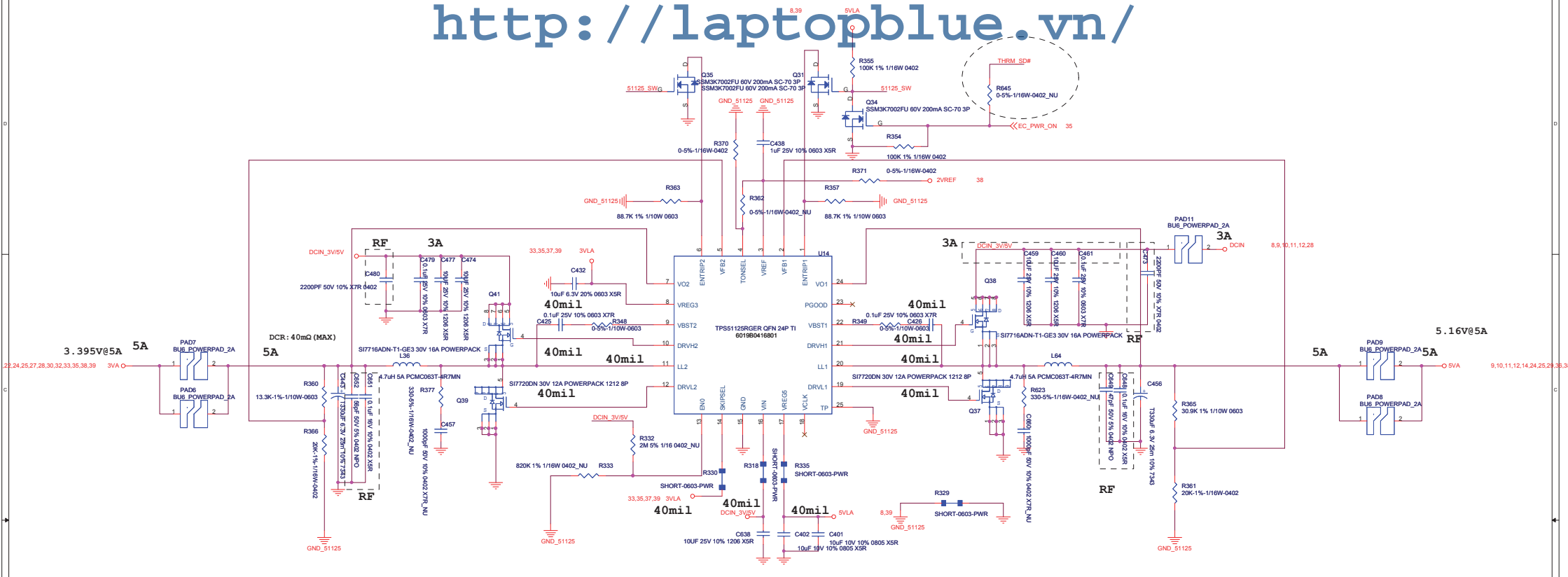


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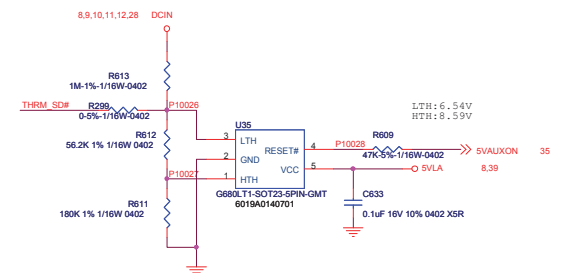
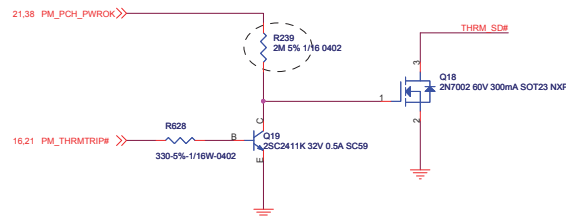
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CHANGE by	IEC	DATE	Friday, April 02, 2010	SHEET		11	of 45



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Temperature Security

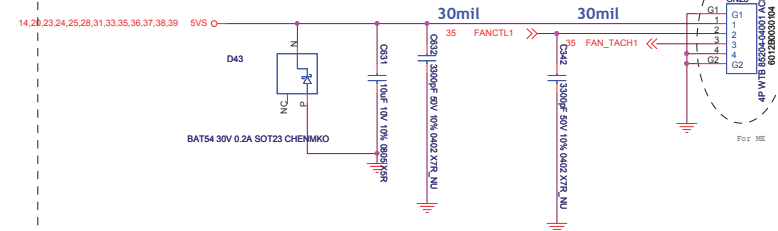


INVENTEC

TITLE			
ACER BAP10/BXP10 5V \bar{A} /5VLA/3VA/3VLA			
SIZE Custom	CODE CS	DOC. NUMBER CS-131	REV A01
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Blank

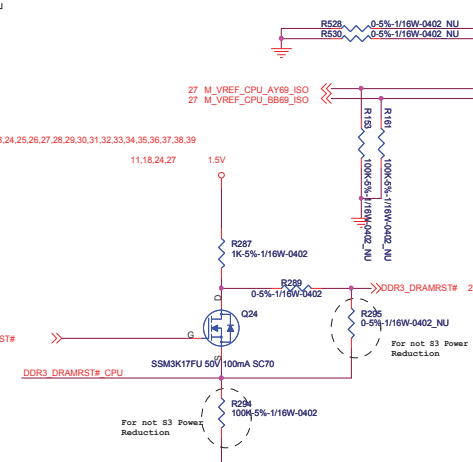
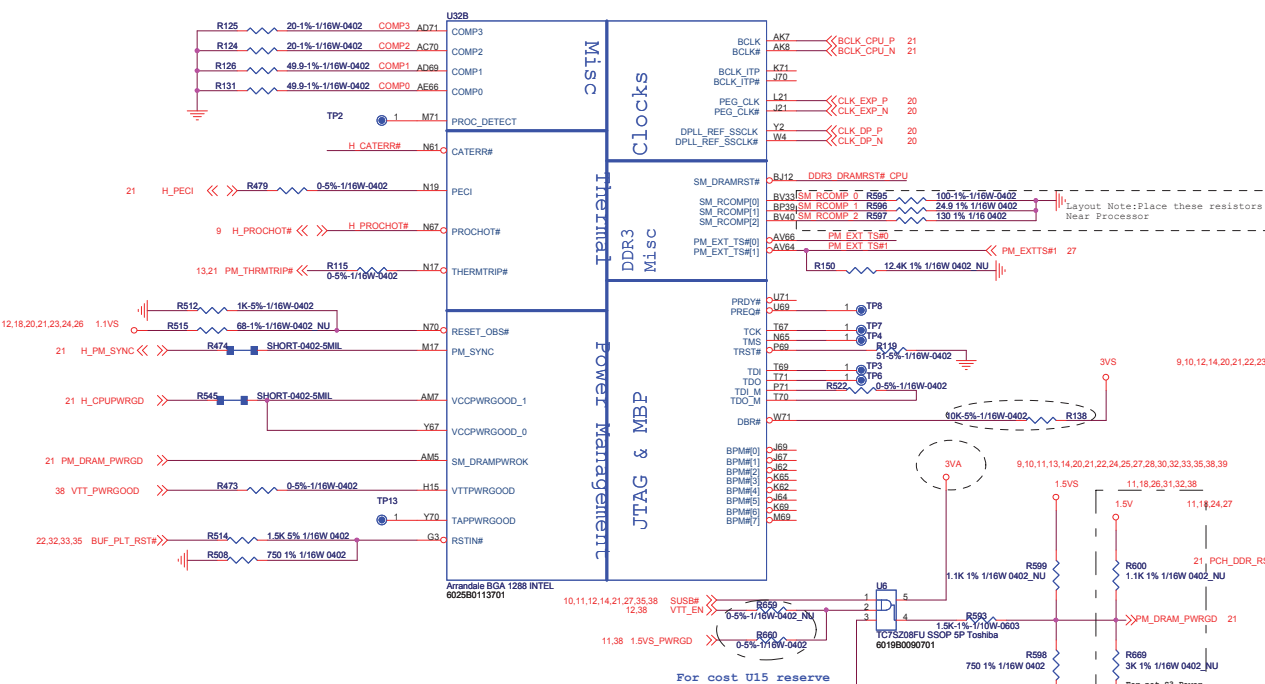
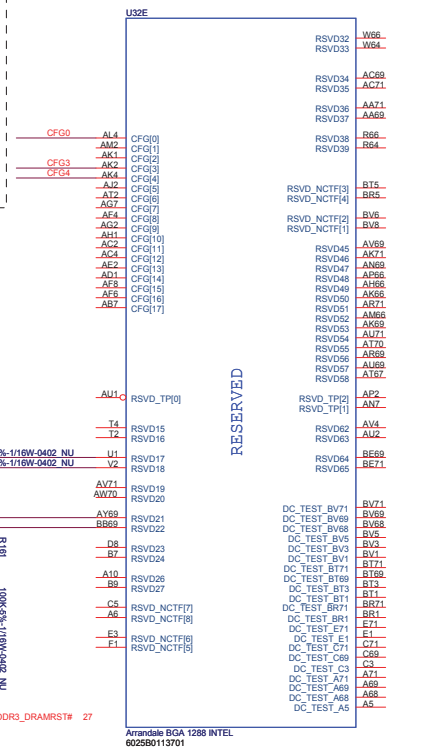


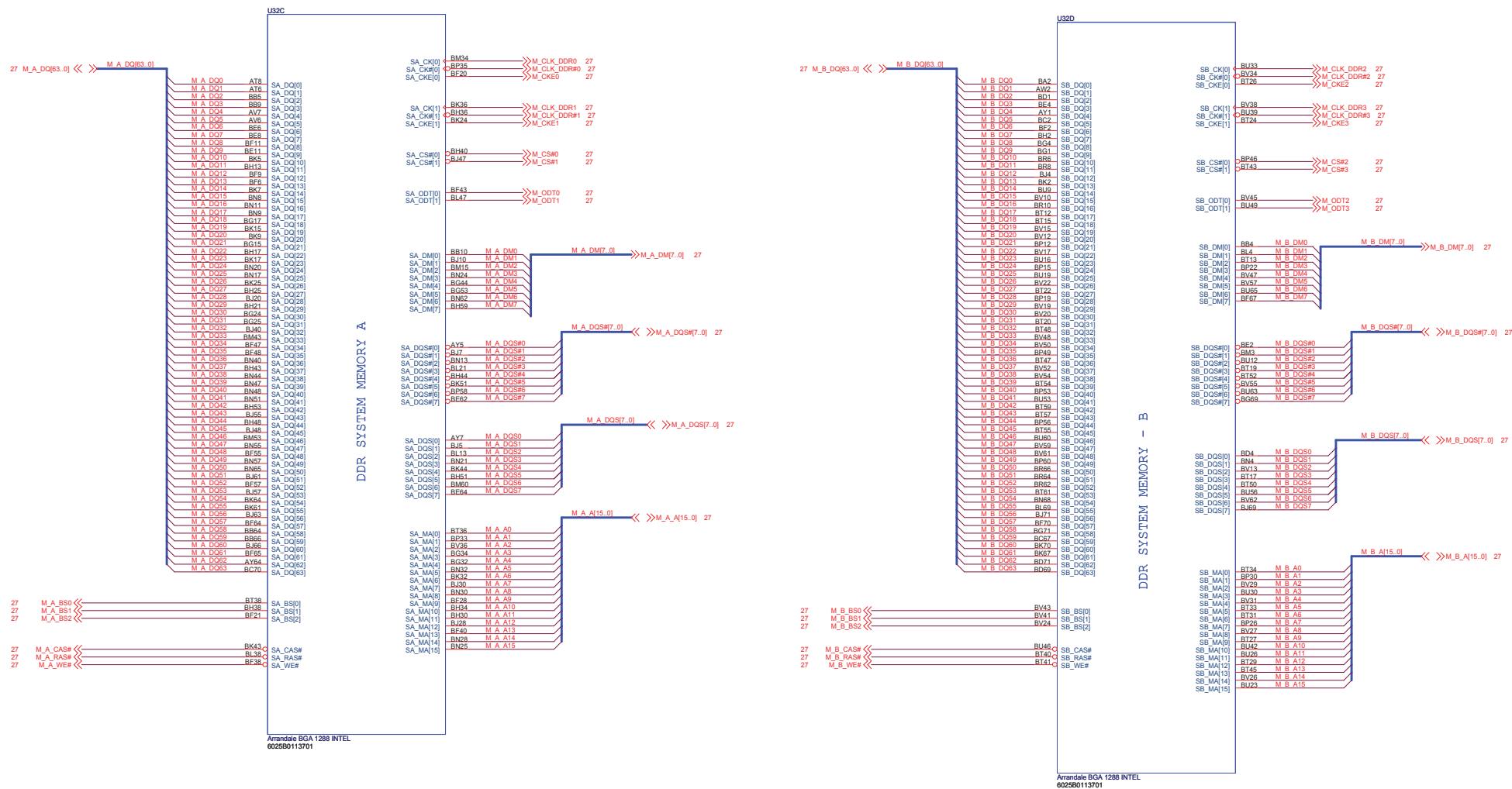
CFG0	R536	3.01K 1% 1/16 0402 NU
CFG3	R538	3.01K 1% 1/16 0402 NU
CFG4	R534	3.01K 1% 1/16 0402 NU

```
CFG0:
1:Single PEG
0:Bifurcation enabled

CFG1:
1 :Normal Operation
0 :Lane Numbers Reversed

CFG4:
1:Disabled; No Physical Display Port
  attached to Embedded Display Port
0:Enabled; An external Display Port
  device is connected to the Embedded
  Display Port
```



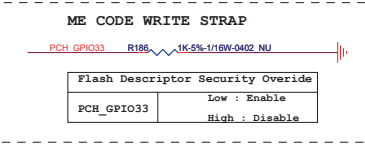
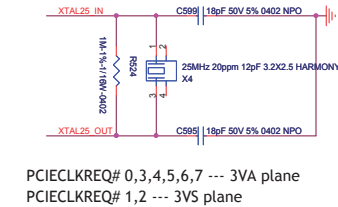
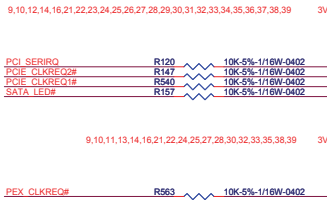
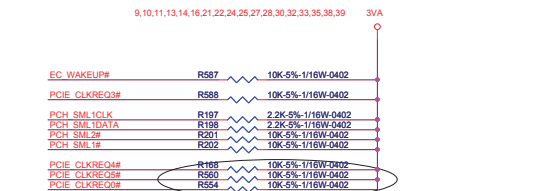
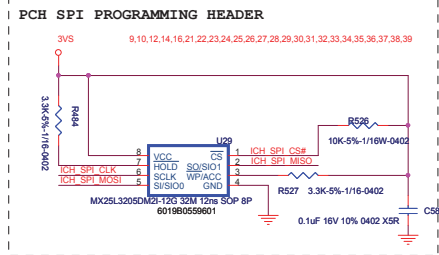
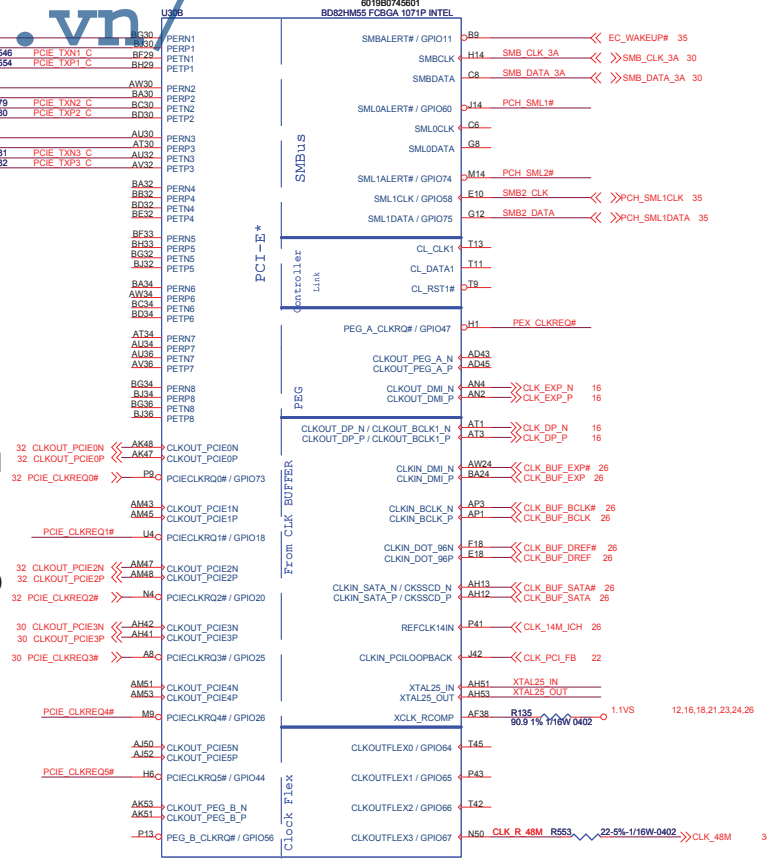
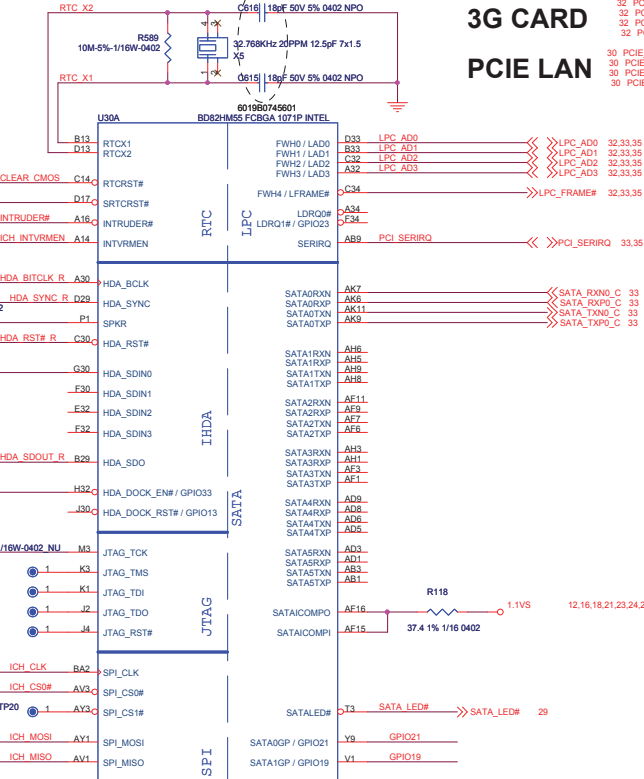




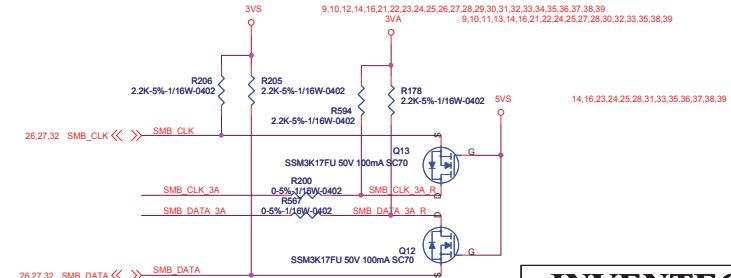
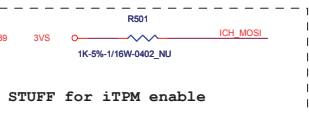
VCORE_CPU 9,18 48000mA



WLAN
3G CARD
PCIE LAN



	Q62	R260	R285
Switchable	Install	Install	NU
Only DIS	NU	NU	Install
Only UMA	NU	Install	NU

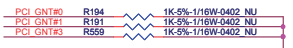
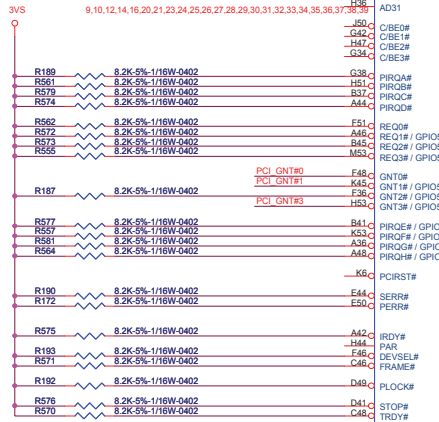


INVENTEC			
TITLE			
ACER BAP10/BXP10 PCH(HDA, JTAG, SATA)			
SIZE Custom	CODE CS	DOC NUMBER CS-131	REV A01
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PCH(FDI,DML,SPM)			
SIZE Custom	CODE CS	DOC NUMBER CS-131	R A
SHEET		21 of	45

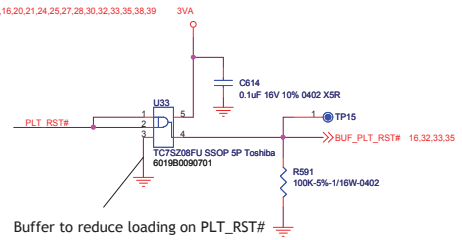
PCI Pull up



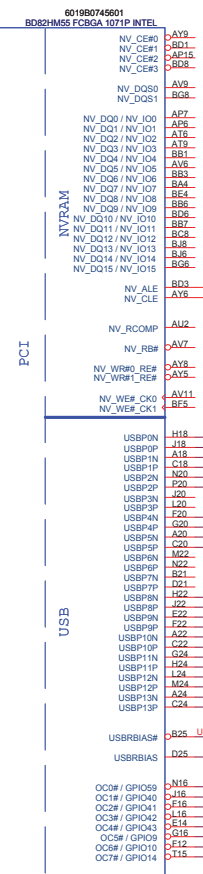
PCI_GNT#3 No stuff : by default
Stuff : For A16 swap override

PCI_GNT#0	PCI_GNT#1	
0	0	LPC
Floating	0	PCI
Floating	Floating	SPI

BIOS type select



Buffer to reduce loading on PLT_RST#



USB

PCI

NVDRAM

5/5 mils spacing on microstrip

BIOS ID setting

Project	MB_ID4	MB_ID3	MB_ID2	MB_ID1	MB_ID0
BAP10 (UMA)	1	1	1	1	1
BXP10 (UMA)	1	1	1	1	0
BAP30 (UMA)	1	1	1	0	1
BXP30 (UMA)	1	1	1	0	0
BAD50 (UMA)	1	1	0	1	1
BXD50 (UMA)	1	1	0	1	0
SJM40 (UMA)	1	1	0	0	1
SJM40 (dGPU)	1	1	0	0	0
BAP30 (dGPU)	1	0	1	1	1
BXP30 (dGPU)	1	0	1	1	0
BAD50 (dGPU)	1	0	1	0	1
BXD50 (dGPU)	1	0	1	0	0
SJM40 (dGPU optimum)	1	0	0	1	1
BAP30 (dGPU optimum)	1	0	0	0	1
BXP30 (dGPU optimum)	1	0	0	0	0

INVENTEC

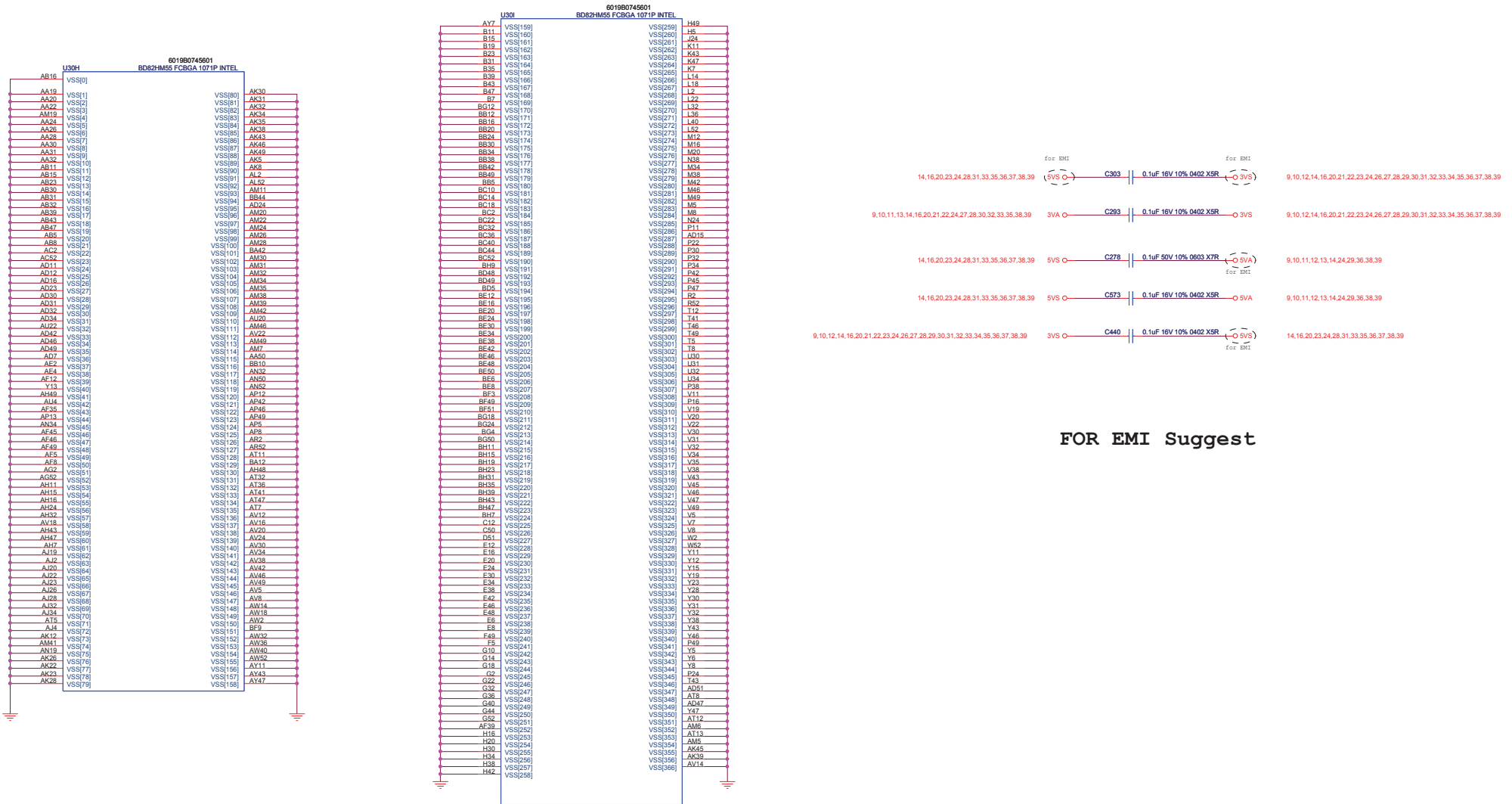
ACER BAP10/BXP10 PCH(USB, PCI)			
SIZE Custom	CODE CS	DOC NUMBER CS-131	REV A01
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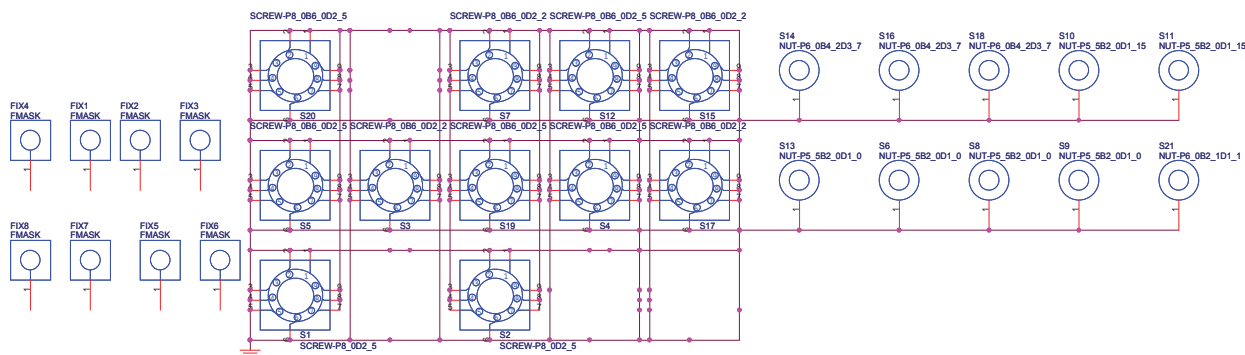
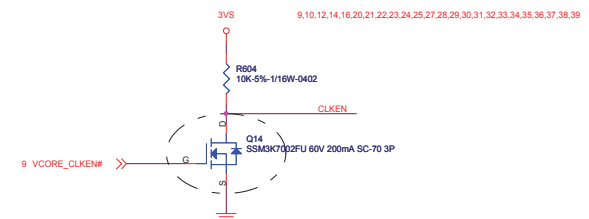
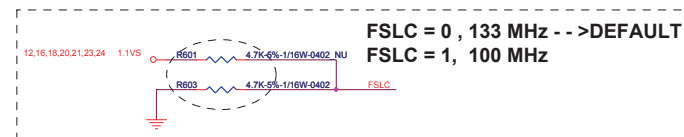
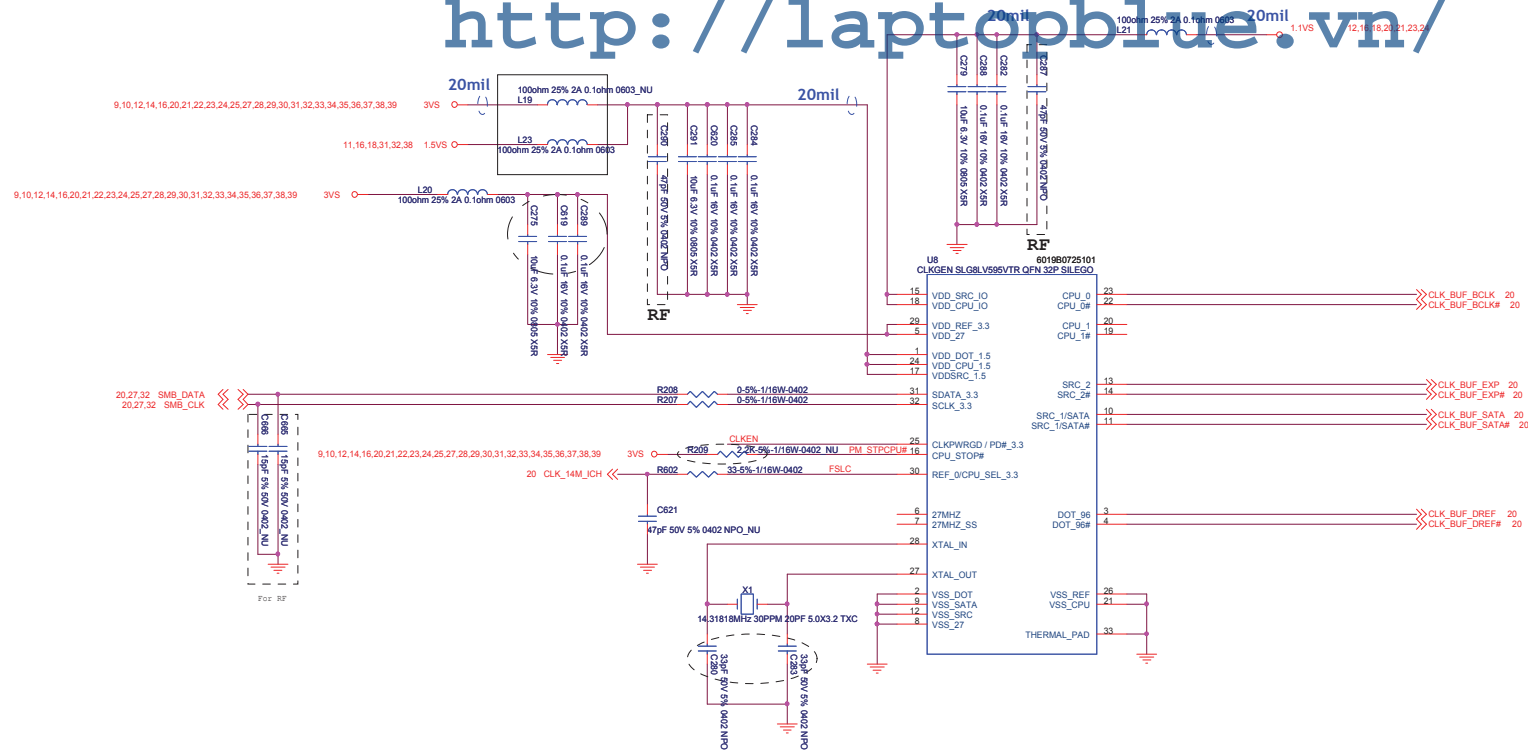
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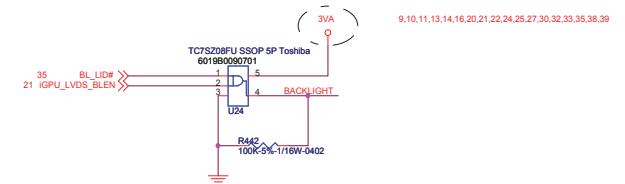
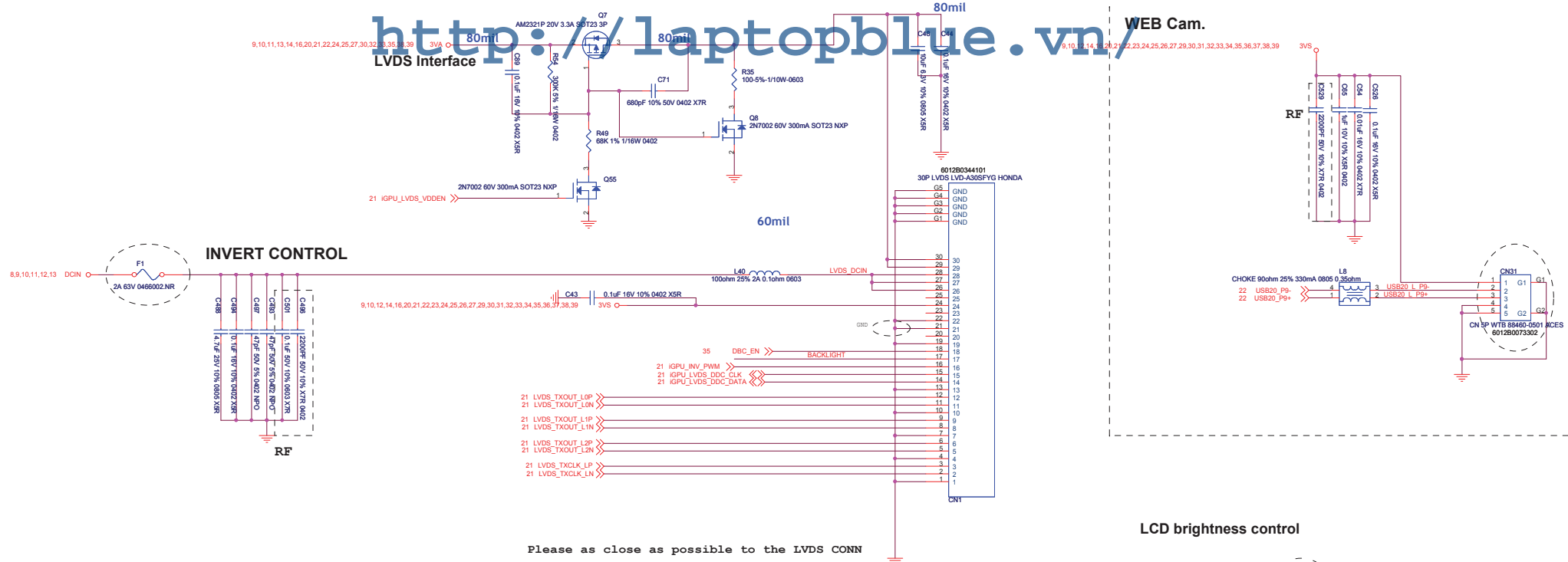
FCH Power I			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01

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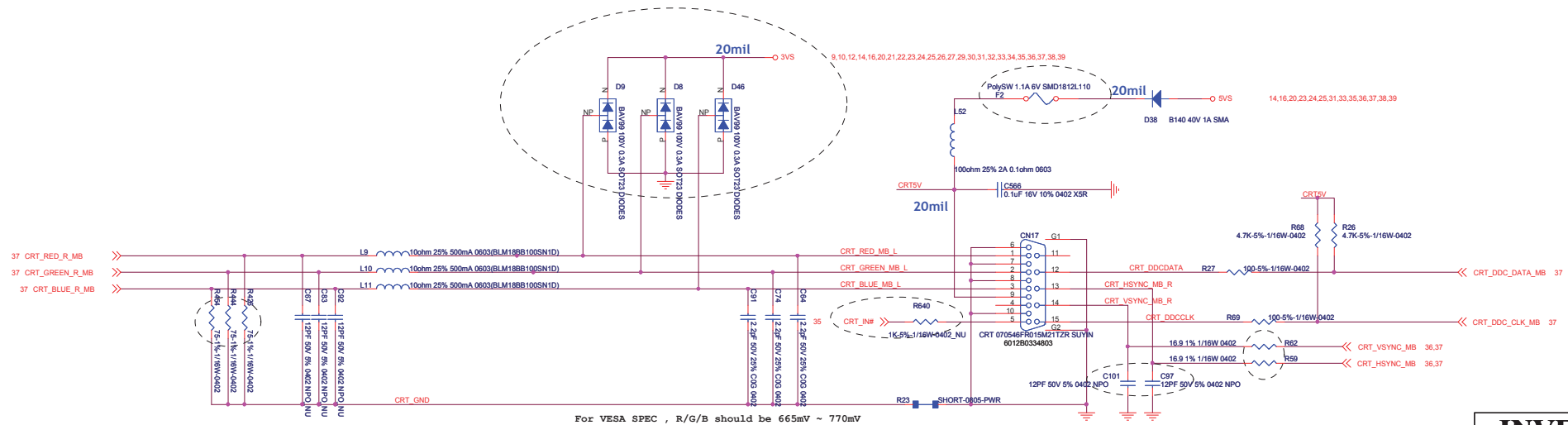


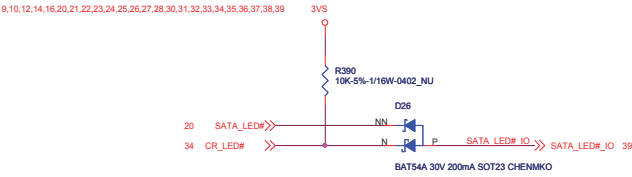






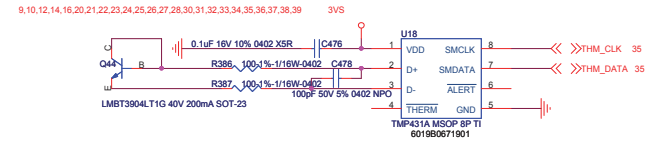
CRT CON.



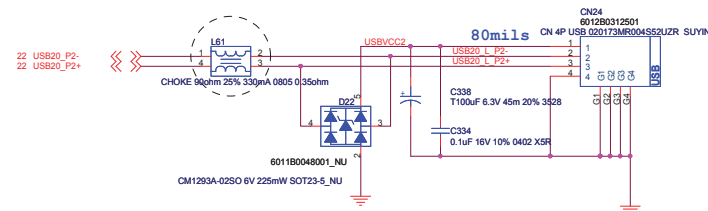
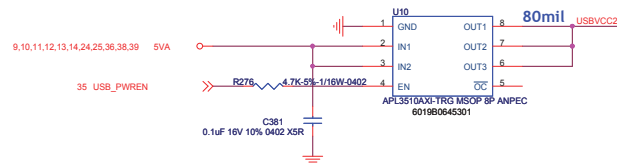
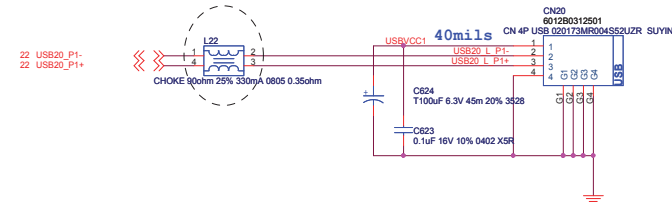
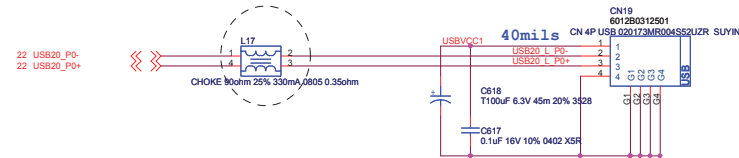
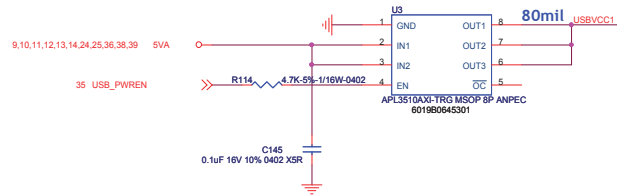


REMOTE thermal sensor

Place near the hottest spot area under Palm-rest



USB



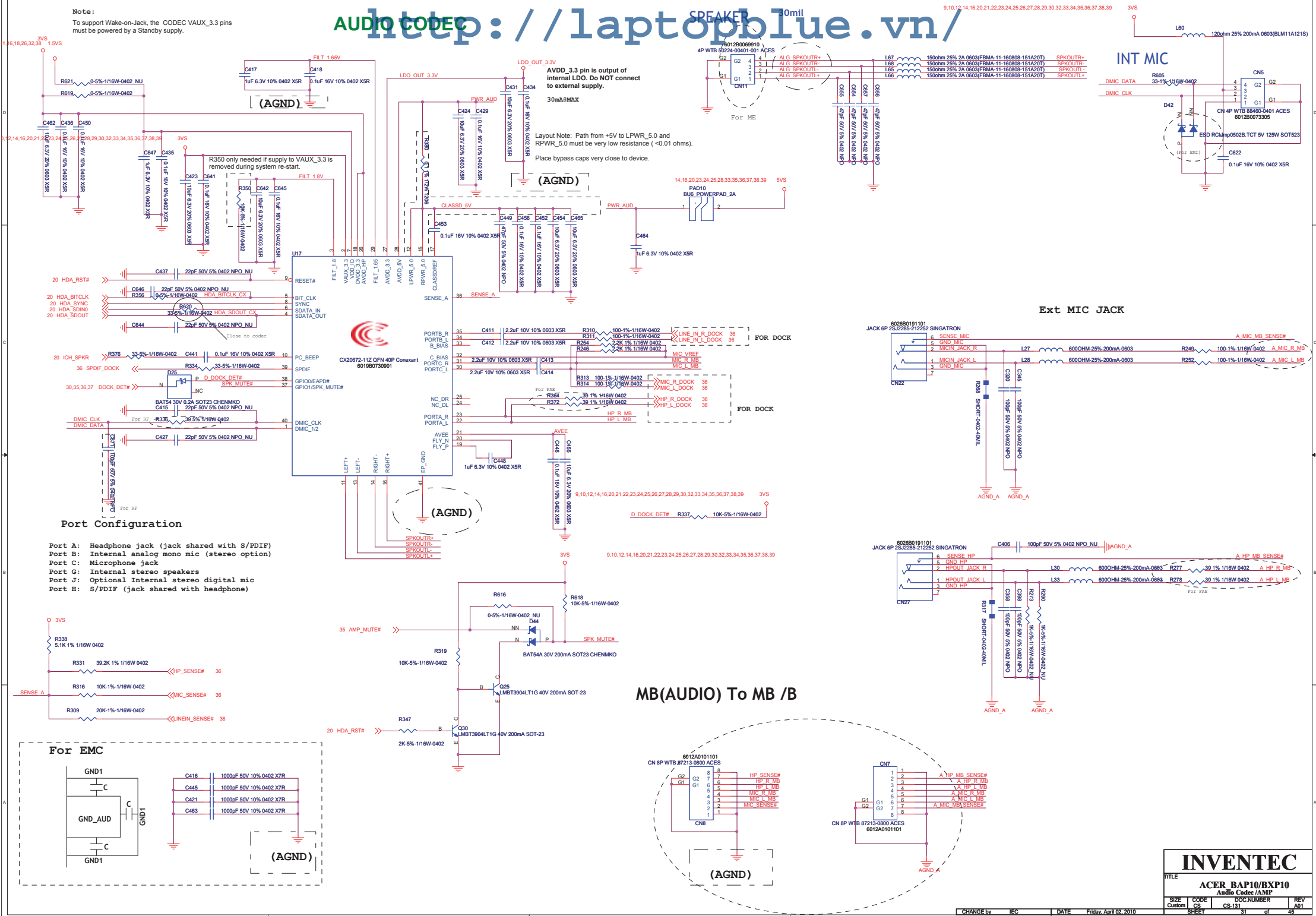
INVENTEC

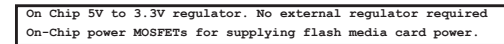
TITLE
ACER BAP10/BXP10
USBSensor

SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01

CHANGE	by	IEC	DATE	Friday, April 02, 2010	SHEET	29	of	45
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Note:
To support Wake-on-Jack, the CODEC VAUX_3.3 pins must be powered by a Standby supply.



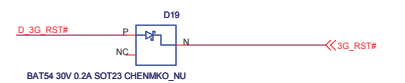


The diagram illustrates the electrical schematic for a PCIE Mini Card designed for 3G connectivity. It features a central IC, the MINI PCIE 52P 88E15-5204M H=5.2mm ACES 60269142001, which is connected to various external components and signals.

Key Components and Connections:

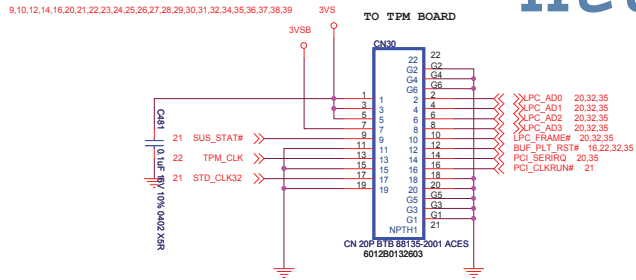
- Power and Ground:** The card is powered by a 3V_3G supply. Key capacitors include C388, C373, C355, C367, C380, C364, C369, C356, C386, and C365. Inductors L321 and L322 are used for power filtering. A 120mil trace width is specified for the power lines.
- Signal Lines:** The card has multiple signal pins, including PCIE_WAKE#, BT_PRI, WLAN_ACT, PCIE_CLKREQ2#, CLKOUT_PCIE2N, CLKOUT_PCIE2P, PCIE_RXN2_3G, PCIE_RXP2_3G, PCIE_TXN2_3G, and PCIE_TXP2_3G. These are connected to various internal and external components.
- Internal Connections:** The card's internal connections are detailed in the "KEY" section, showing the mapping of pins to internal components and signals. For example, pin 1 is connected to WAKE#, pin 2 to RSV01, and pin 3 to RSV02.
- External Connections:** The card is connected to external components such as the BAT54 30V 0.2A 50723 CHERMOKU_NU, which is used for power regulation. The card also has connections for RF signals (RF_3G_IN#, RF_3G_OUT#, RF_3G_RST#) and other control signals (USIM_VCC, USIM_DATA, USIM_CLK, USIM_RST, USIM_VPP).

The schematic includes detailed component values, pin numbers, and trace widths, providing a comprehensive view of the card's internal and external electrical architecture.



INVENTEC			
TITLE			
ACER BAP10/BXP10 3G/WLAN			
SIZE Custom	CODE CS	DOC.NUMBER CS-131	REV A01
SHEET		32	of 45

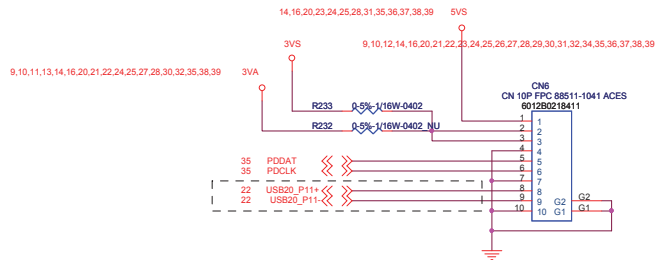
TO TPM CNN.



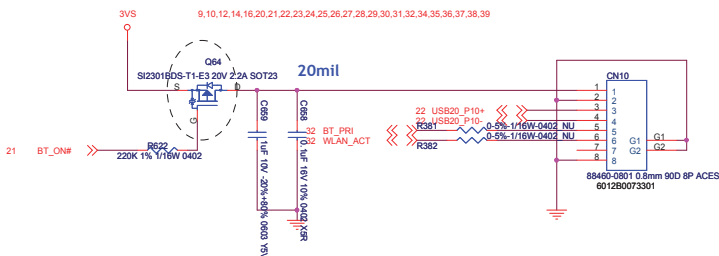
IN TPM SKU STUFF



GP + FP CNN.

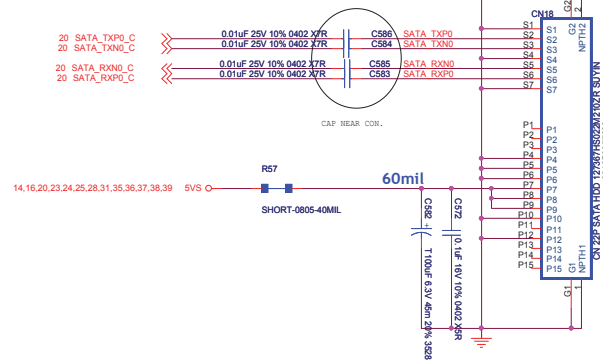


Bluetooth CNN.

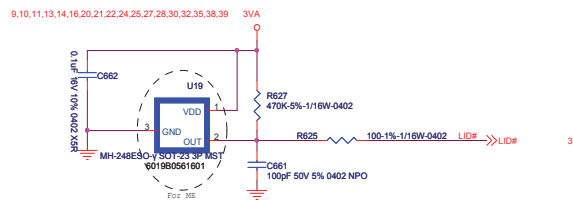


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HDD I/F



HALL Switch



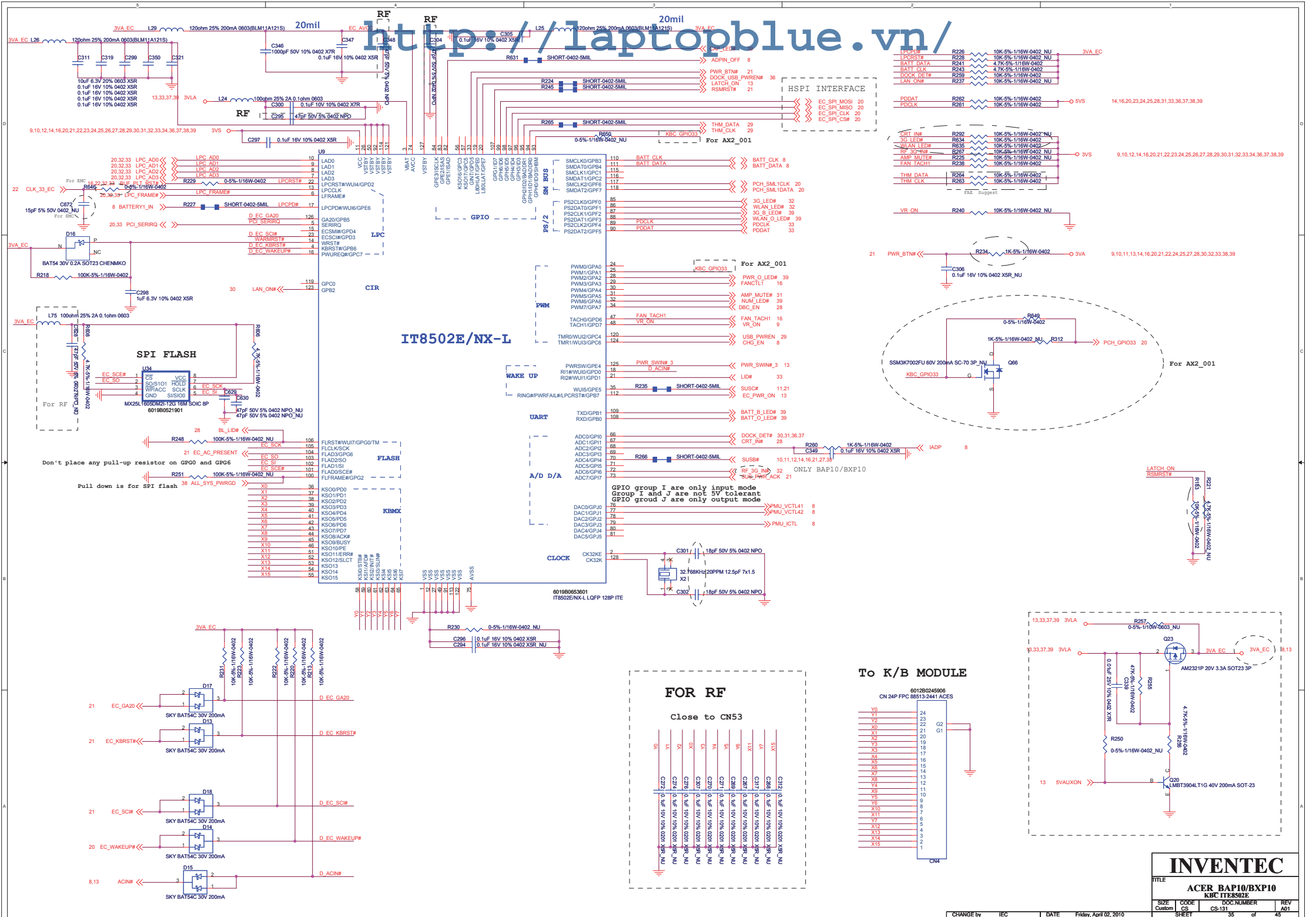
INVENTEC

TITLE
ACER BAP10/BXP10
USB+SATA/AC+HDD+CON

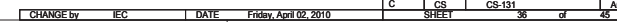
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01

CHANGE by IEC DATE Friday, April 02, 2010

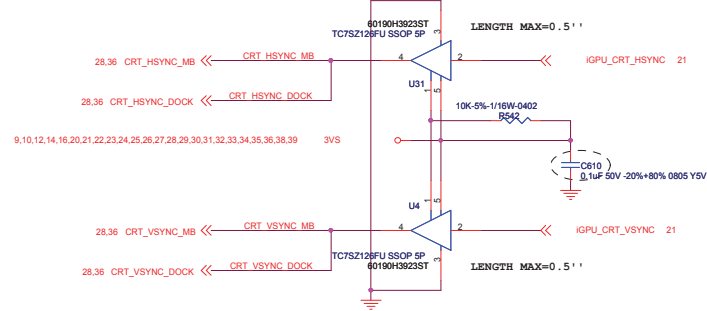
SHEET 33 of 45



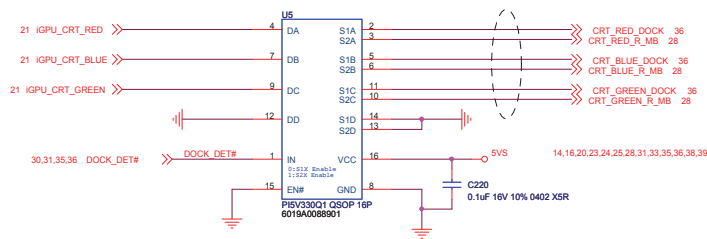
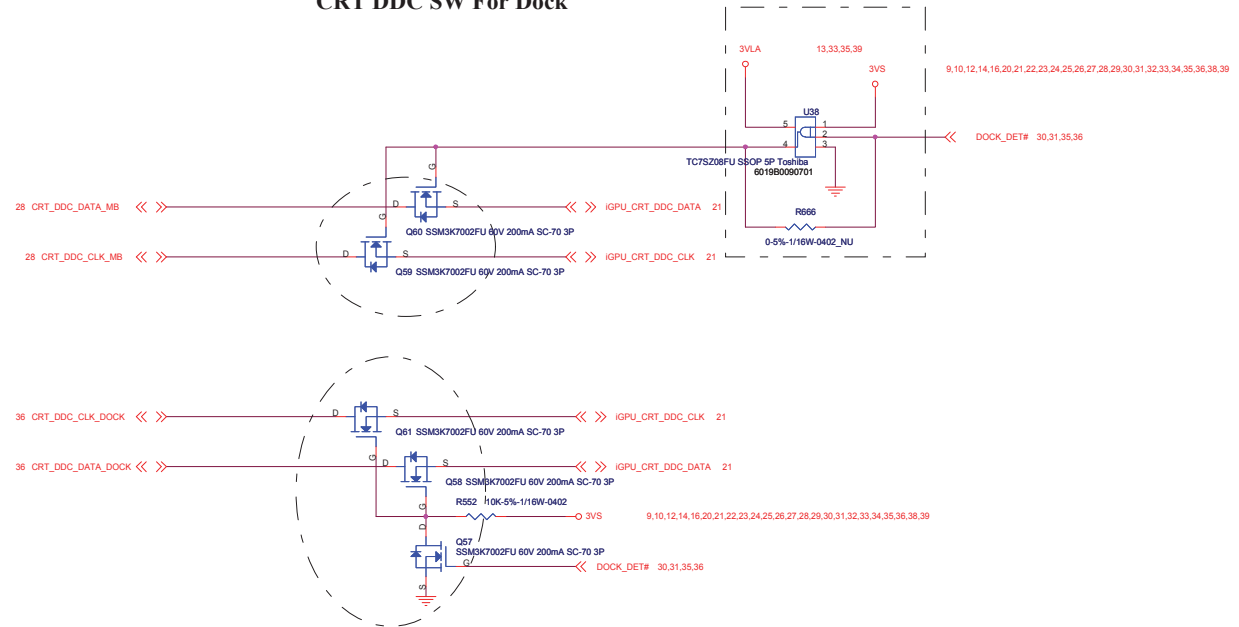
9,10,11,12,13,14,24,25,29,38,39



CRT HSYNC/VSYNC SW For Dock



CRT DDC SW For Dock

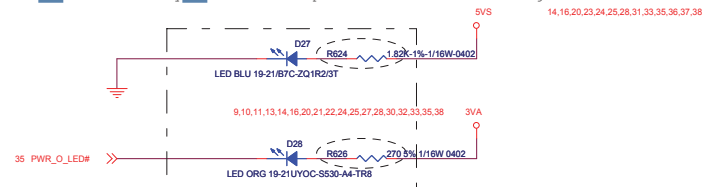



For cost U15 reserve




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Project	MB_ID0
BAP10 (UMA)	1
BXP10 (UMA)	0



35 BATT_0_LED# 
LED ORG 19-21UVOC-S530-A4-TR8
13.33,35,37
9,10,11,13,14,16,20,21,22,24,25,27,28,30,32,33,35,38

35 BATT_0_LED# 
LED BLU 19-21/87C-20-0237
9,10,11,12,13,14,24,25,29,36,38
8,13

5V

14, 16, 20, 23, 24, 25, 28, 31, 33, 35, 36, 37, 38

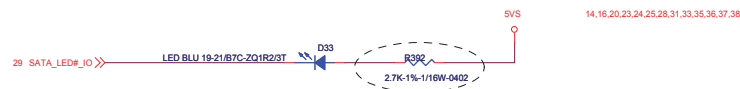
1 2 3 4

G1 G2

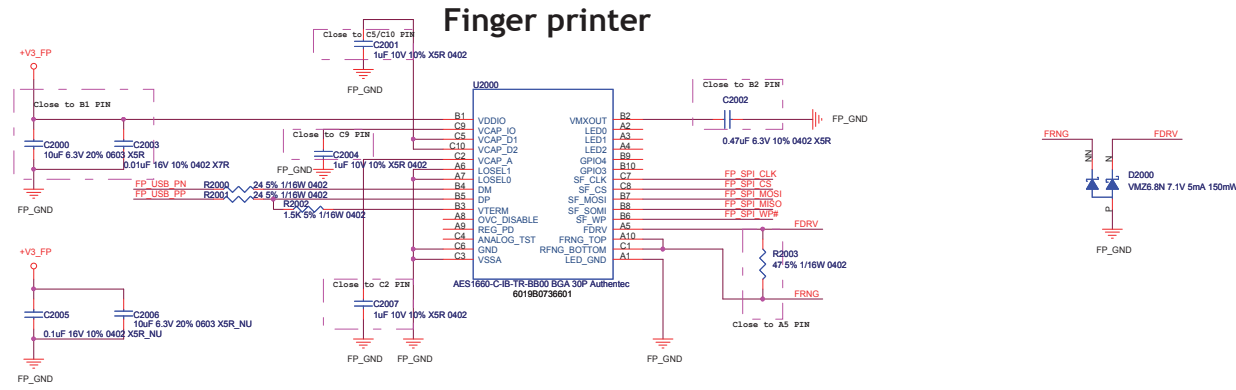
4F FPG 88513-044N ACES 601280245893

13 PWR_SW_IN

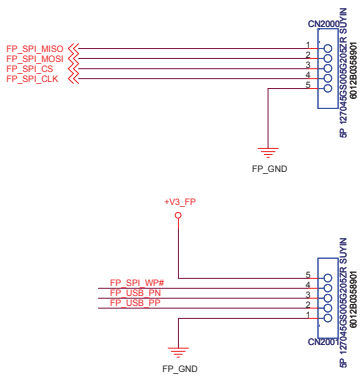
Ground



w/ Fingerprint: Stuff
w/o Fingerprint: OPEN



TO GP PIN HEADER



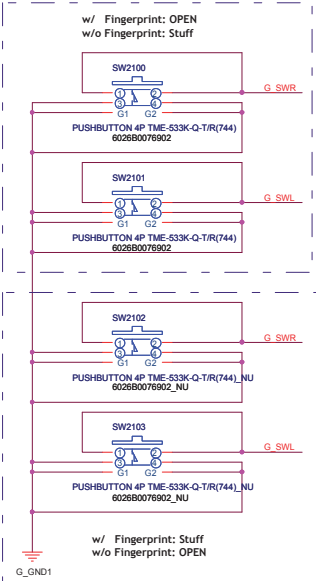
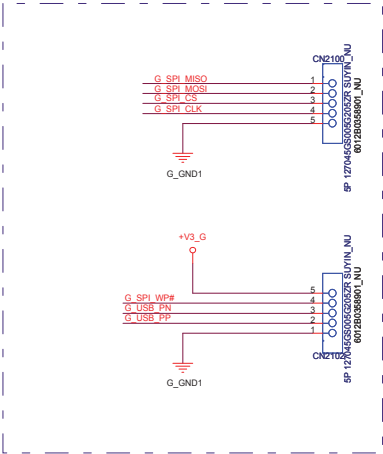
INVENTEC				
TITLE				
ACER BAP10/BXP10				
GP Button				
SIZE	CODE	DOC. NUMBER		REV
Custom	CS	CS-131		A01
SHEET		40	of	45

GP Board

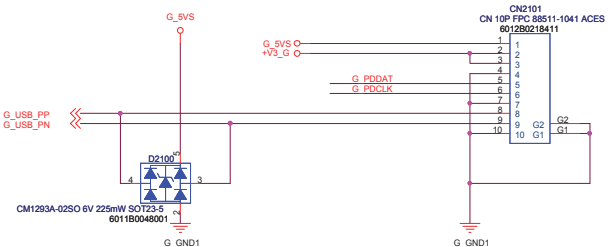
http://laptopblue.vn/

GP Button

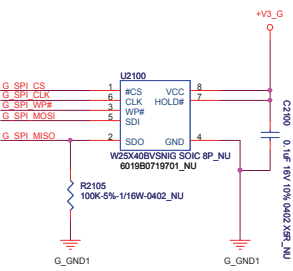
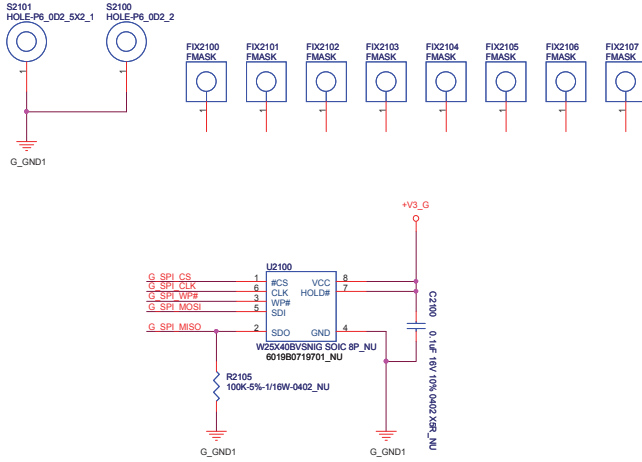
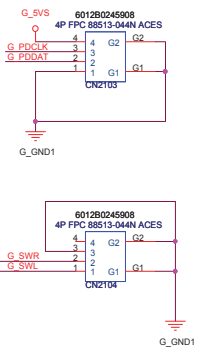
TO FP PIN HEADER



TO MB



TO touch Pad



INVENTEC

TITLE ACER_BAP10/BXP10

GP

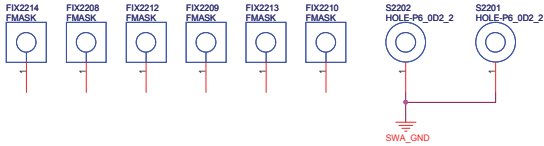
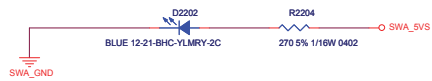
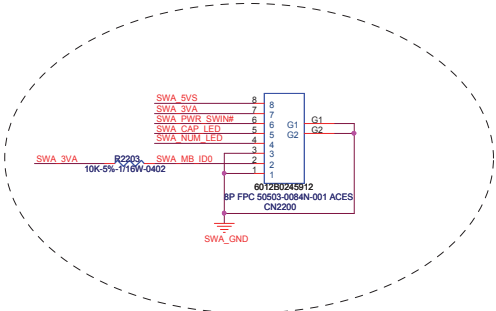
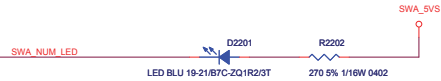
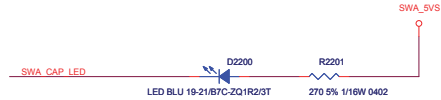
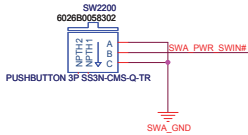
SIZE Custom CS DOCNUMBER CS-131 REV A01

BAP10 1 SW+3 LED Board

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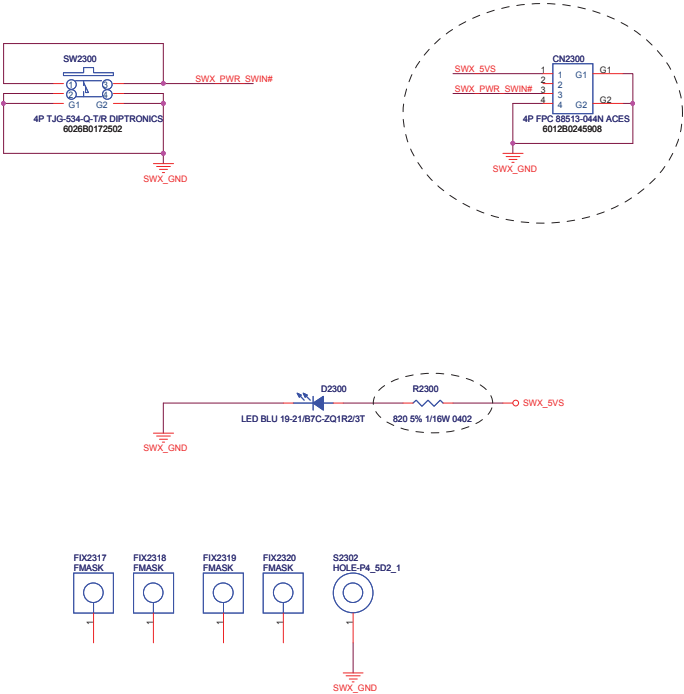
Pin2 for BIOS ID setting

Project	MB_ID0
BAP10 (UMA)	1
BXP10 (UMA)	0



BXP10 1 SW+1 LED Board

<http://laptopblue.vn/>



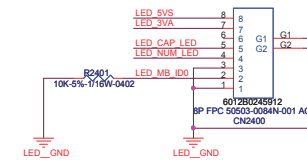
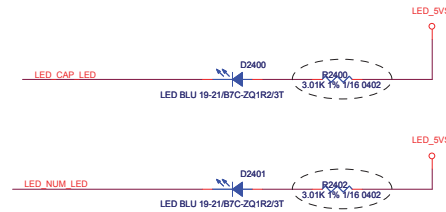
INVENTEC			
TITLE			
ACER BXP10			
SW			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01
SHEET		43	of 45

BXP10 2 LED Board

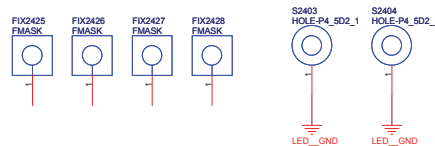
<http://laptopblue.vn/>

Pin2 for BIOS ID setting

Project	MB_ID0
BAP10 (UMA)	1
BXP10 (UMA)	0



CO-LAYOUT for BAP SW Board



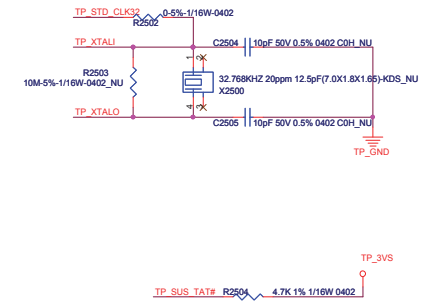
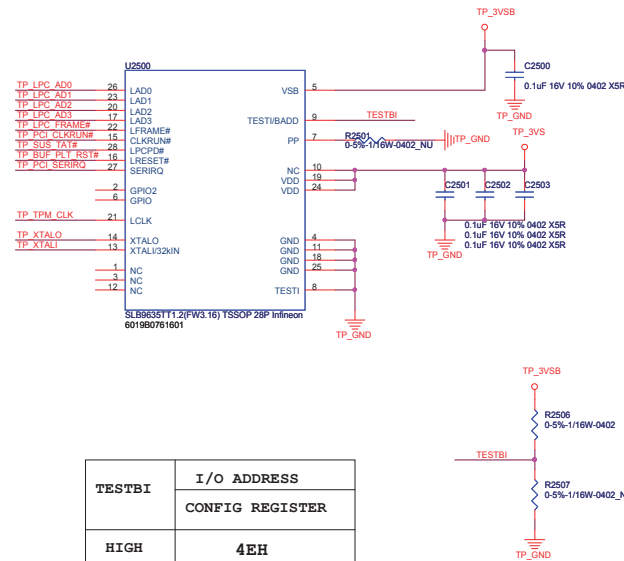
INVENTEC			
TITLE			
ACER BXP10			
LED			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	A01
SHEET		44	of 45

CHANGE by IEC DATE Friday, April 02, 2010

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The diagram shows the CN2500 connector with the following pin connections:

- TP_3VS: Pin 1
- TP_3VSB: Pin 2
- TP_SUS_TAT#: Pin 3
- TP_TPM_CLK: Pin 4
- TP_STD_CLK32: Pin 5
- TP_GND: Pin 6
- TP_LPC_AD0: Pin 7
- TP_LPC_AD1: Pin 8
- TP_LPC_AD2: Pin 9
- TP_LPC_AD3: Pin 10
- TP_LPC_FRAMES#: Pin 11
- TP_BUF_PL1_TST#: Pin 12
- TP_PCI_SERIRQ: Pin 13
- TP_PCI_CLKRQ#: Pin 14
- NPTH1: Pin 15
- TP_GND: Pin 16



TESTBI	I/O ADDRESS
	CONFIG REGISTER
HIGH	4EH
LOW	2EH

