

# Acer Flamingo

## 01200\_SD

CLK GEN.  
ICS

PAGE:03

Mobile CPU  
Tualatin  
version :

PAGE:4~5

Project code:  
PCB P/N:  
REVISION:

PCB LAYER

L1: Signal 1(X)  
L2: GND  
L3: Signal 2 (Y)  
L4: Signal 3 (X/Y)  
L5: GND  
L6: POWER  
L7: Signal 4(weak)  
L8: Signal 5 (X)  
L9: GND  
L10:Signal 6 (Y)

DC/DC&CHARGER  
Switching Power  
MAX1632/MAX1772

INPUTS	OUTPUTS
DCBATOUT	+6V
AD+	+5VSB
	+3.3V
	+5V
	+12V
	CD+5V

PAGE:32

CPU DC/DC  
Switching Power  
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE
	+VCCT

PAGE:30/31

OTHER DC/DC  
MAX1644/MAX1792  
MAX8863

INPUTS	OUTPUTS
+5V	+1.8V
+3.3V	+1.5V
LAN_+3.3V	+3VSB
+5VSB	+1.8VSB
	+3.3V

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CMOS  
BAT



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Title Block Diagram			
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SO-DIMM\*2

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(133M)  
MEM BUS

Almador-M  
GMCH  
Version : A4

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HOST BUS (133M)

RAM BUFFER  
(2\*32bit)\*2

VGA  
ATI Mobility  
M6S  
version:

DOCK V

CRT

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LCD

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TV OUT

ATA100

PRIMARY EIDE  
HDD

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HOT PLUG

SECONDARY EIDE  
CDROM

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USB 1.0X2

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ICH3-M

Version :

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HUB I/F (66M)

LAN  
82562EM

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PCI BUS (33M)

DOCK V

QSW

POWER SW  
MIC2564A

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CARDBUS  
OZ6933T

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CARDBUS  
SLOT A,B

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AC-Link

LPC BUS (33M)

AC'97 CODEC  
ALC200

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MODEM  
Daughter  
Card

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SMsC  
SIO  
LPC47N267

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KBC  
M38859

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FWH  
82802AB

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LPC DEBUG  
CONN.

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FIR

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FLOPPY

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PRINTER

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SERIAL

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FINGER  
PRINTER

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TOUCH PAD

PAGE:28

INT. KB

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PS/2 CONN

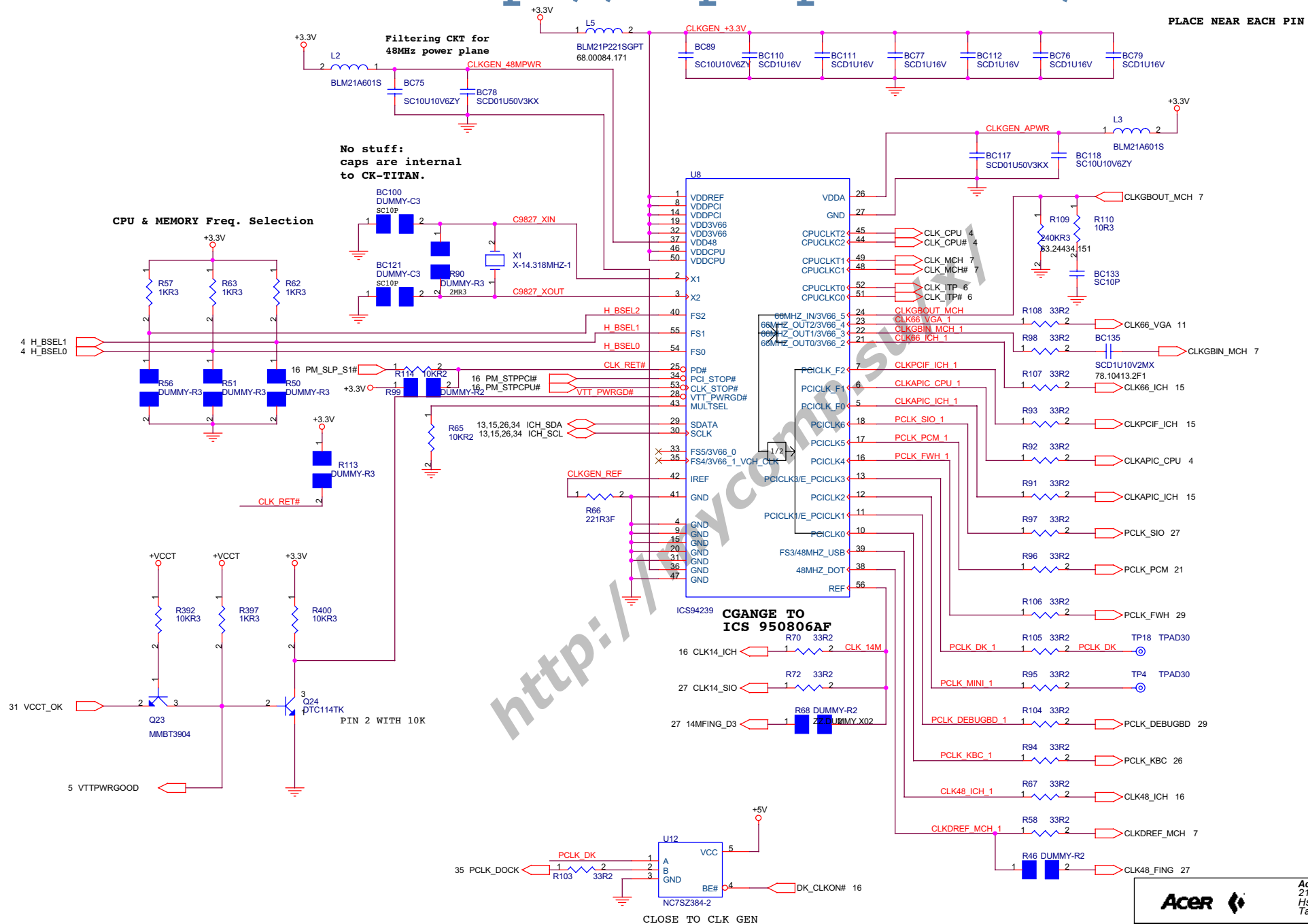
PAGE:26

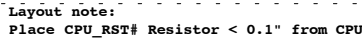
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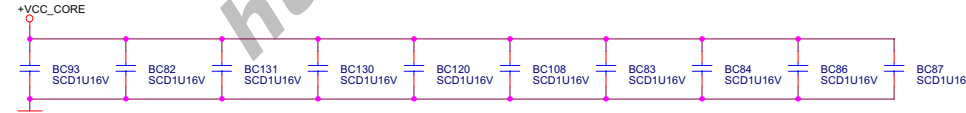
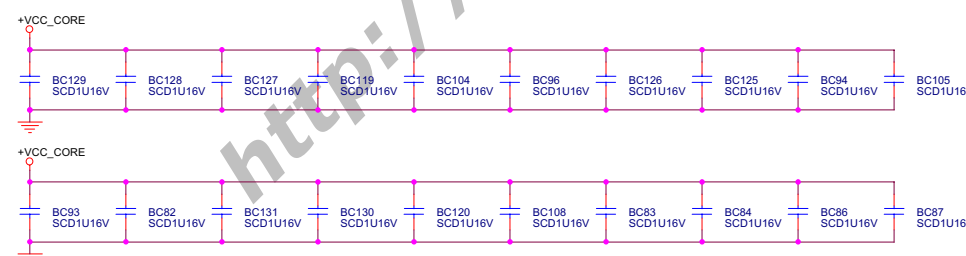
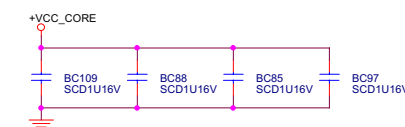
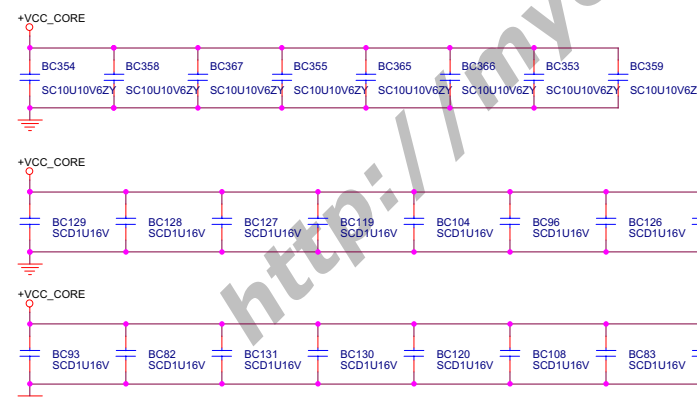
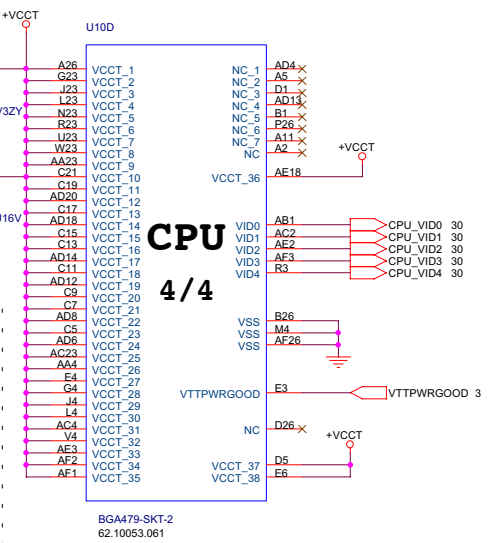
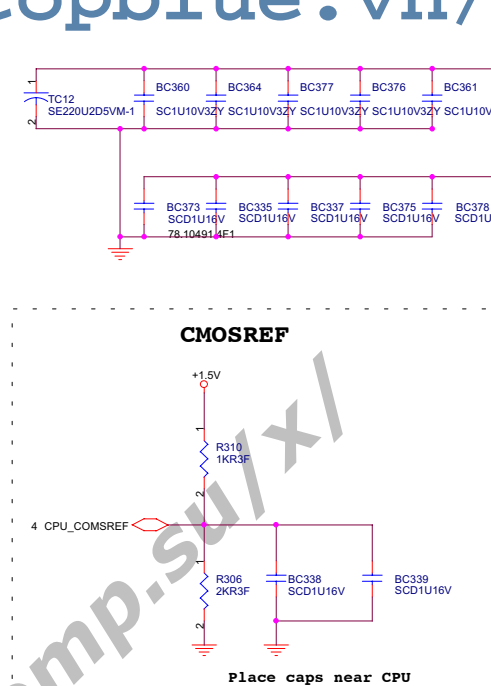
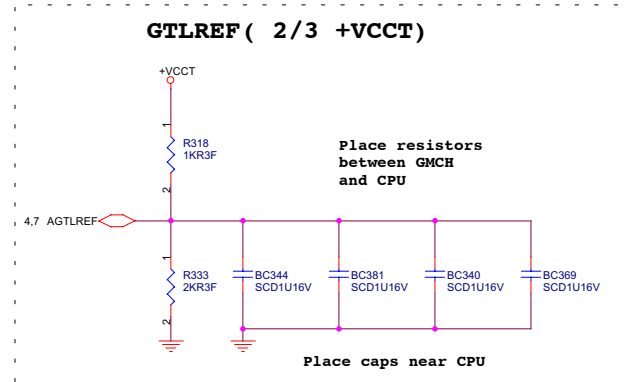
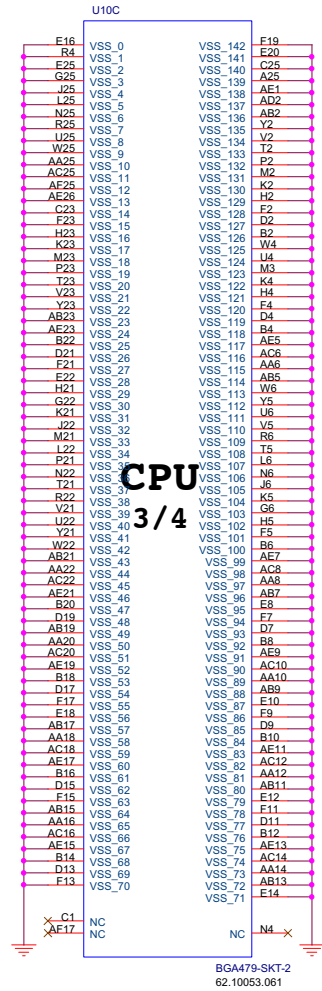


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Title		
REVISION HISTORY		
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Decoupling Recommendation

VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all
	Bulk Caps		
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout
	Bulk Caps		

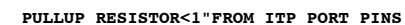
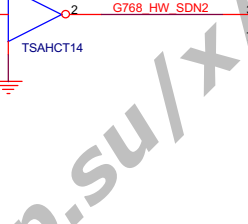
Freeza

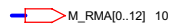
0.1uF * 24	10uF / 10V * 10	220uF / 2.5V * 8	1uF * 10	220uF / 2.5V * 2
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Kodiak Ver. 0.5

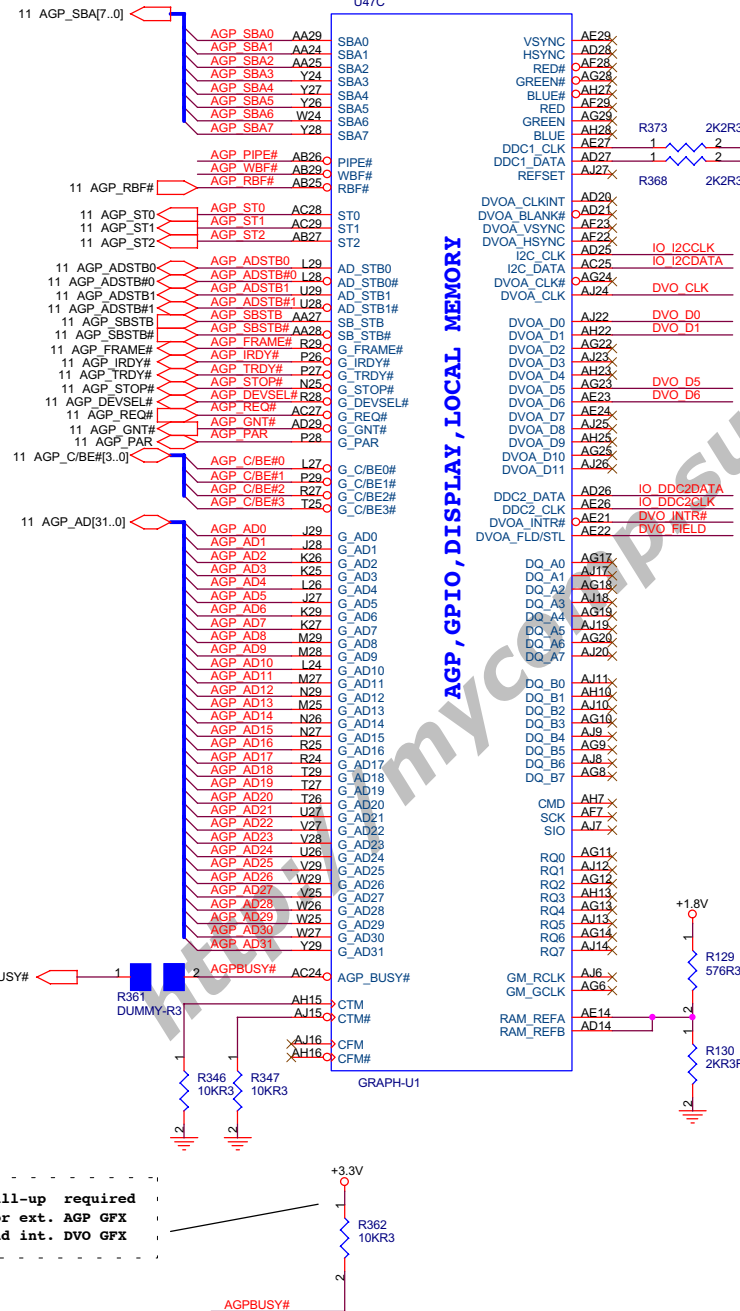
10uF / 6.3V * 12	10uF / 6.3V * 10 + 6 * NS	150uF / 4V * 12 + 2 * NS	1uF * 10 + 2 * NS	150uF / 4V * 5 + 1 * NS
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**SB**









Pull-up required  
for ext. AGP GFX  
and int. DVO GFX

AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached
Strapping Option for SW detection of AGP or DVO device		
DVOA_D5	0 = DESKTOP	Pull-up 2.2K to V1.5S
Int. P/D	1 = MOBILE	
DVOA_D6	0 = Dual ended term.	Pull-up 2.2K to V1.5S
Int. P/D	1 = Single ended term.	
DVOA_D0	0 = 200MHz	Pull-down 2.2K to GND
Int. P/U	1 = 133MHz	
DVOA_D1	0 : IOQD = 1	Pull-down 2.2K to GND
Int. P/U	1 : IOQD = 8	
DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	
DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	



(1.8A)

(800mA)

POWER

CHECK

(250mA)

(500mA)

Place C near AE16 and AE15 on GMCH

## Decoupling Recommendation

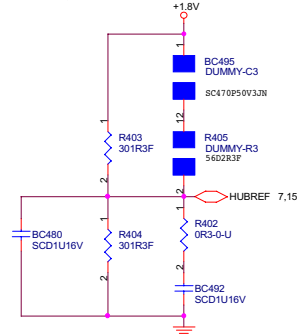
Freeza

Kodiak Ver. 0.5

	Decoupling Caps				
V1.2S_GMCH	0.1uF * 20	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20	1uF * 20	
	Bulk Caps		100uF / 10V * 2	150uF / 4V * 5 + 1 * NS	
V1.2S_GMCHCORE	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador	68pF * 1	68pF * 1	
	0.1uF * 40			1uF * 40	
	Bulk Caps			150uF / 4V * 10 + 1 * NS	
V1.5S_GMCH	0.1uF * 9	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 8	0.1uF * 9	
	82pF * 4		0.01uF * 3	82pF * 4	
	Bulk Caps		100uF / 10V * 1	22uF / 20V * 1	
V1.8S_GMCH	0.1uF * 4 + 4	Distribute as close as possible to GMCH-M Local Memory Quadrant	0.1uF * 2	0.1uF * 4 + 2	
	82pF * 2	Additional 4 * 0.1uF shall be distributed as close as possible to VCCPCHOS LM		82pF * 2	
	Bulk Caps			22uF / 20V * 2	
V3_GMCH	0.1uF * 12 + 2	Distribute as close as possible to GMCH-M System Memory Quadrant	0.1uF * 20	0.1uF * 12 + 2	
	82pF * 4	Additional 4 * 0.1uF shall be distributed as close as possible to IO Quadrant	100uF / 10V * 1	82pF * 4	
	Bulk Caps			22uF / 20V * 2	

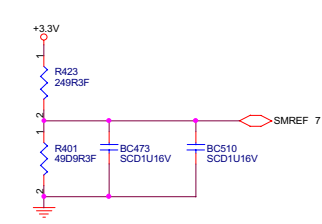
Almador-M Checklist Ver. 0.5 8/28

## HUB INTERFACE REF 1/2\*1.8V



Layout Note:  
Place divider pair in middle of bus.  
Place capacitors near GMCH.

## SYSTEM MEMORY REF 0.55V



Place capacitor near GMCH.

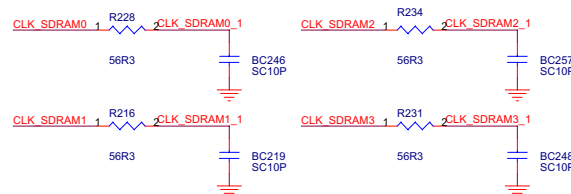
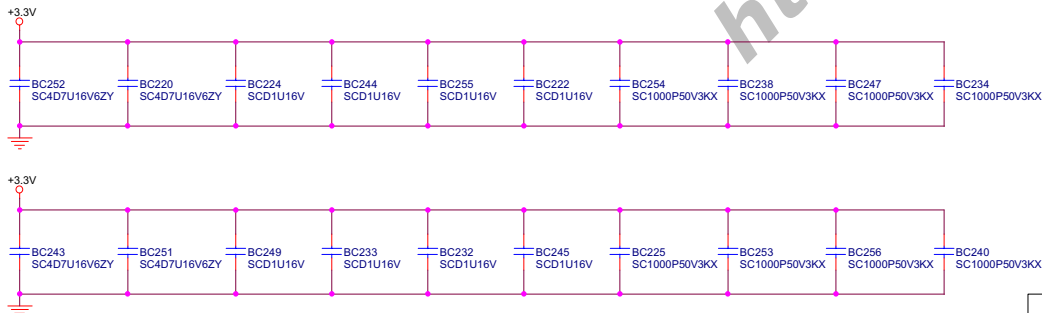
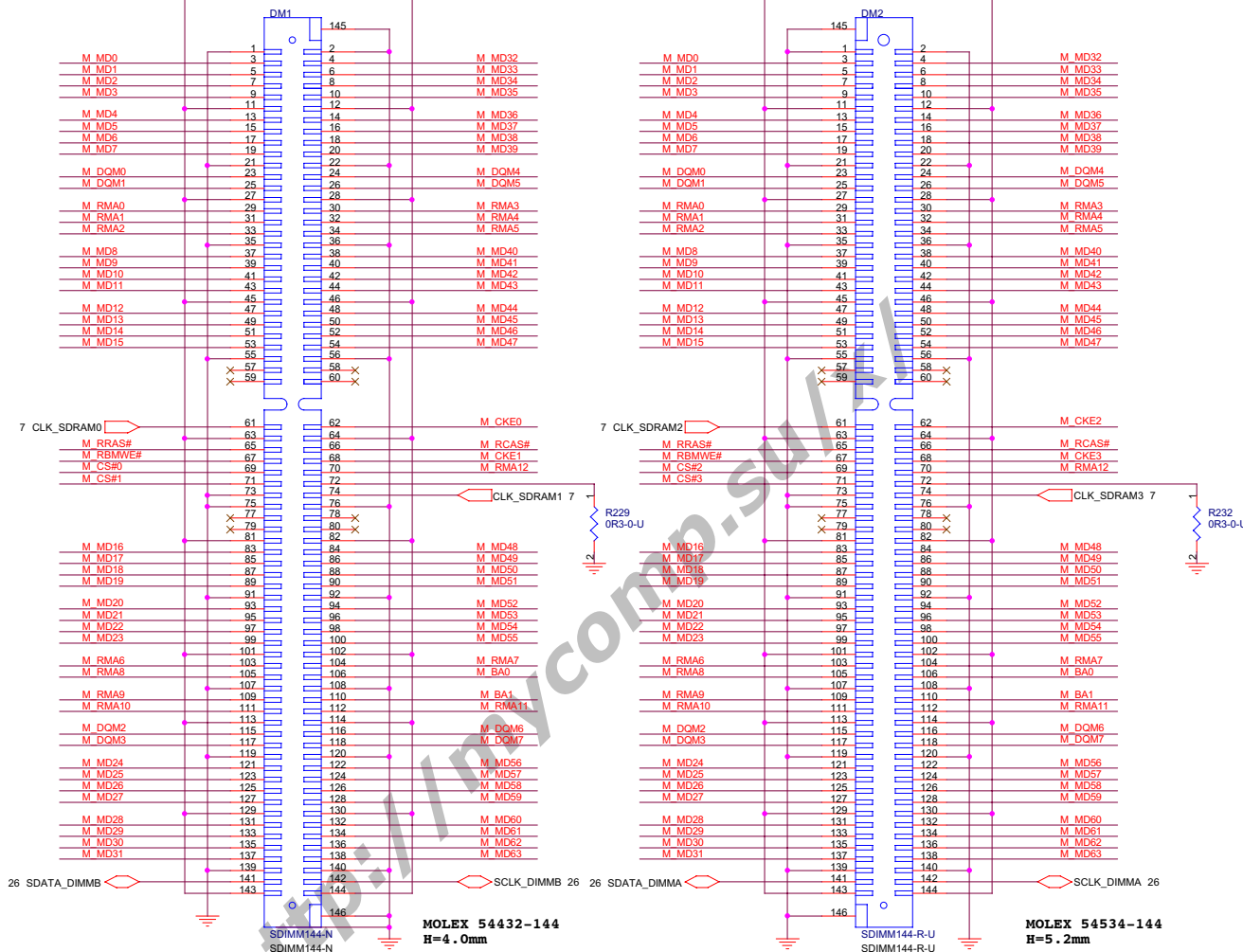
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Title		GMCH(3/3)	Rev
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Date	Friday, July 13, 2001	Sheet 9 of 38	

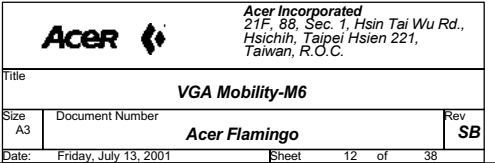
7 M\_RMA[0..12] 7 M\_RCAS# 7 M\_RRAS# 7 M\_BA0 7 M\_CSH[0..3] 7 M\_BA1 7 M\_DQM[0..7] 7 M\_RBMWE#

http://laptopblue.vii/ (Normal Type) (Reverse Type)



NOTE: NETWORK RESISTOR NEAR GMCH < 1.5 inch.







(5V to +INV\_VCC3.3v)

U41  
SET SHDN#  
GND  
IN  
OUT  
MAX8863-S

+3VSB\_SET\_INV  
INV\_VCC  
+5V

BC114 SC20P  
R100 16K5R3F  
R88 10KR3F  
BC370 SC1U10V3ZY  
BC362 SC1U10V3ZY

Near CN3 Inverter connector

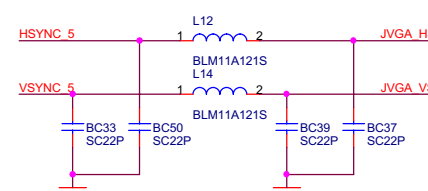
## CRT

CRT\_R  
CRT\_G  
CRT\_B

BC35 SC10P  
BC36 SC10P  
BC38 SC10P

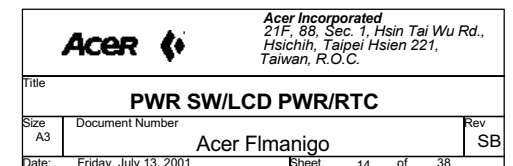
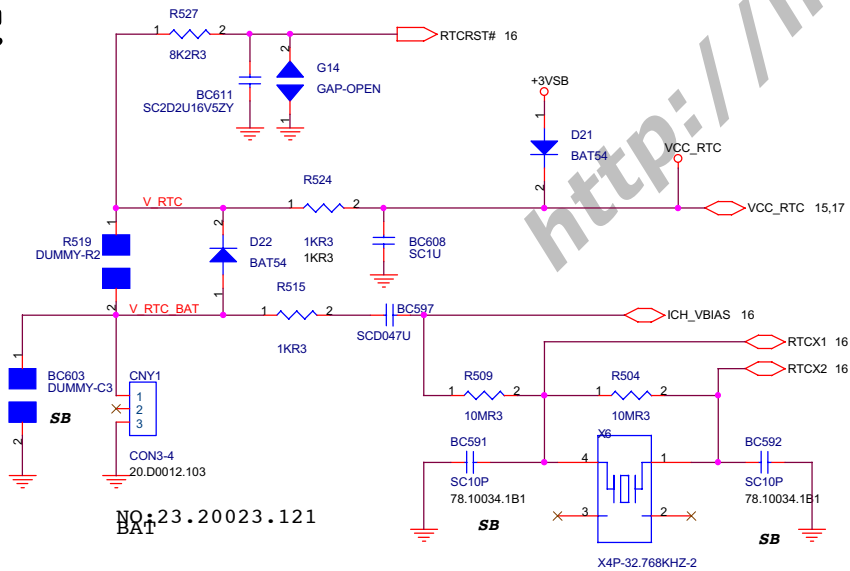
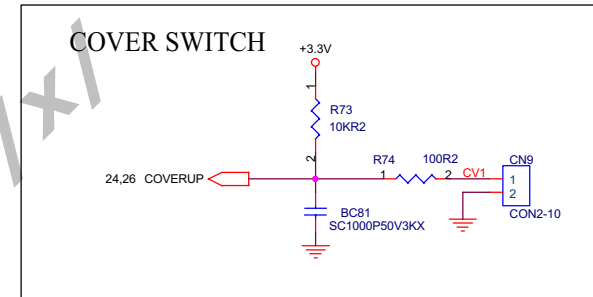
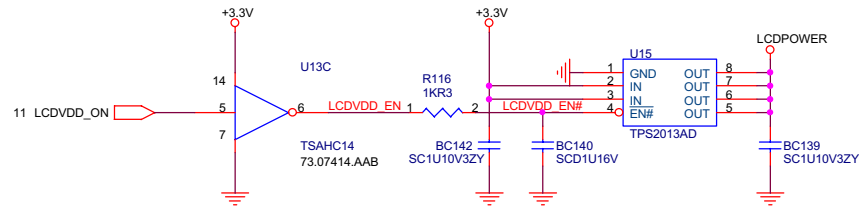
Near CN3 Inverter connector

HSYNC 5 L12 1 2 JVGA\_HS



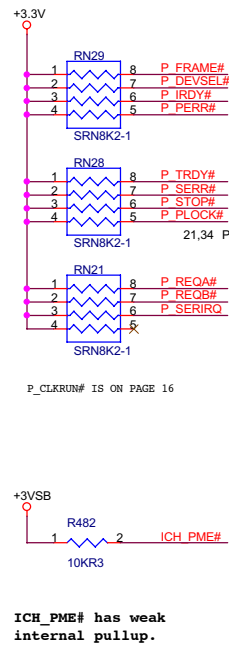
37.4\_1% resistors must be placed after RGB pi filter ,near CRT connector.







## PCI I/F Pullups



## ICH3-M

### PART A

U55A ICH3-M-U

### System Management I/F

SM\_INTRUDER#  
SMLINK0  
SMLINK1  
SMB\_CLK  
SMB\_DATA  
SMB\_ALERT#/GPIO1#

Y22  
Y23  
AB22  
J22  
AA21  
AB23  
Y21  
W23  
U22  
W21X  
U23

INTRUDER#  
SMLINK0  
SMLINK1  
ICH\_SDA  
ICH\_SCL

AC3  
AC4  
AC5

Y22  
Y23  
AB22  
J22  
AA21  
AB23  
Y21  
W23  
U22  
W21X  
U23

ICH\_A20GATE 26  
CPU\_A20M# 4  
CPU\_DPLSP# 4  
CPU\_FERR# 4  
CPU\_IGNNE# 4  
CPU\_INTR# 4  
CPU\_NMI 4  
CPU\_PWRGOOD 4  
CPU\_RCIN# 26  
CPU\_SLP# 4  
CPU\_STPCLK# 4

CC\_FERR# 4  
CC\_IGNNE# 4  
CC\_INTR# 4  
CC\_NMI 4  
CC\_CPUPWRGD 4  
RCIN# 26  
CC\_SM# 4.37  
CC\_STPCLK# 4

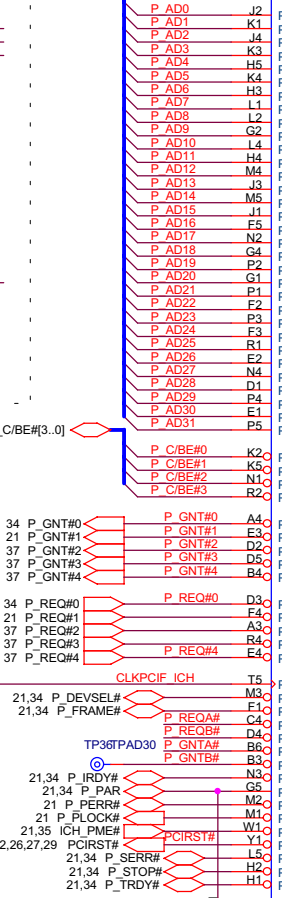
### CPU Interface

### HUB Interface

### INTERRUPT Interface

### EEPROM I/F

### LAN I/F



21,34 P\_AD[31..0]

21,34 P\_CBE#[3..0]

3 CLKPCIF\_ICH

21,34 P\_DEVSEL#

21,34 P\_FRAME#

TP36TPAD30

21,34 P\_IRDY#

21,34 P\_PERR#

21 P\_PLOCK#

21,35 ICH\_PME#

7,11,21,22,26,27,29 PCIRST#

21,34 P\_SERR#

21,34 P\_STOP#

21,34 P\_TRDY#

3V TO 5V

TSAHCT14

TSAHCT14

RSTDRV\_5 18

RSTDRV#\_5

Kodiak Ver 0.7  
Pull up to  
VCC\_RTC

VCC\_RTC

R505 100KR3

ICH\_SCL 3,13,26,34

ICH\_SDA 3,13,26,34

R510 10KR2

+3VSB

R493 DUMMY-R3

0R3-0-U

CC\_DPSLP# 4,30

(for use if CPU unable to support DPSLP#)

ICH\_A20GATE 26

CC\_FERR# 4

CC\_IGNNE# 4

CC\_INTR# 4

CC\_NMI 4

CC\_CPUPWRGD 4

RCIN# 26

CC\_SM# 4.37

CC\_STPCLK# 4

HL\_0

HL\_1

HL\_2

HL\_3

HL\_4

HL\_5

HL\_6

HL\_7

HL\_8

HL\_9

HL\_10

CLK66 ICH

HL\_STB 7

HL\_STB# 7

HUB\_RCOMP\_1SH

HUB\_VSWING

APICCLK\_ICH

CC\_PICD0 4

CC\_PICD1 4

P\_IRQA# 11

P\_IRQB# 31

P\_IRQC# 27

P\_IRQD# 21

P\_IRQE# 37

P\_IRQF# 34

P\_IRQG# 37

P\_IRQH# 34

P\_IRQI# 18

P\_IRQJ# 18

P\_IRQK# 18

P\_IRQL# 18

P\_IRQM# 18

P\_IRQN# 18

P\_IRQO# 18

P\_IRQP# 18

P\_IRQQ# 18

P\_IRQR# 18

P\_IRQS# 18

P\_IRQT# 18

P\_IRQU# 18

P\_IRQV# 18

P\_IRQW# 18

P\_IRQX# 18

P\_IRQY# 18

P\_IRQZ# 18

P\_IRQAA# 18

P\_IRQAB# 18

P\_IRQAC# 18

P\_IRQAD# 18

P\_IRQAE# 18

P\_IRQAF# 18

P\_IRQAG# 18

P\_IRQAH# 18

P\_IRQAI# 18

P\_IRQAJ# 18

P\_IRQAK# 18

P\_IRQAL# 18

P\_IRQAM# 18

P\_IRQAN# 18

P\_IRQAO# 18

P\_IRQAP# 18

P\_IRQAQ# 18

P\_IRQAR# 18

P\_IRQAS# 18

P\_IRQAT# 18

P\_IRQAU# 18

P\_IRQAV# 18

P\_IRQAW# 18

P\_IRQAX# 18

P\_IRQAY# 18

P\_IRQAZ# 18

P\_IRQBA# 18

P\_IRQBB# 18

P\_IRQBC# 18

P\_IRQBD# 18

P\_IRQBE# 18

P\_IRQBF# 18

P\_IRQBG# 18

P\_IRQBH# 18

P\_IRQBI# 18

P\_IRQBJ# 18

P\_IRQBK# 18

P\_IRQBL# 18

P\_IRQBM# 18

P\_IRQBN# 18

P\_IRQBO# 18

P\_IRQBP# 18

P\_IRQBQ# 18

P\_IRQBR# 18

P\_IRQBS# 18

P\_IRQBT# 18

P\_IRQBU# 18

P\_IRQBV# 18

P\_IRQBW# 18

P\_IRQBX# 18

P\_IRQBY# 18

P\_IRQBZ# 18

P\_IRQCA# 18

P\_IRQCB# 18

P\_IRQCC# 18

P\_IRQCD# 18

P\_IRQCE# 18

P\_IRQCF# 18

P\_IRQCG# 18

P\_IRQCH# 18

P\_IRQCI# 18

P\_IRQCJ# 18

P\_IRQCK# 18

P\_IRQCL# 18

P\_IRQCM# 18

P\_IRQCN# 18

P\_IRQCO# 18

P\_IRQCP# 18

P\_IRQCQ# 18

P\_IRQCR# 18

P\_IRQCS# 18

P\_IRQCT# 18

P\_IRQCU# 18

P\_IRQCV# 18

P\_IRQCW# 18

P\_IRQCX# 18

P\_IRQCY# 18

P\_IRQCZ# 18

P\_IRQDA# 18

P\_IRQDB# 18

P\_IRQDC# 18

P\_IRQDD# 18

P\_IRQDE# 18

P\_IRQDF# 18

P\_IRQDG# 18

P\_IRQDH# 18

P\_IRQDI# 18

P\_IRQDJ# 18

P\_IRQDK# 18

P\_IRQDL# 18

P\_IRQDM# 18

P\_IRQDN# 18

P\_IRQDO# 18

P\_IRQDP# 18

P\_IRQDQ# 18

P\_IRQDR# 18

P\_IRQDS# 18

P\_IRQDT# 18

P\_IRQDU# 18

P\_IRQDV# 18

P\_IRQDW# 18

P\_IRQDX# 18

P\_IRQDY# 18

P\_IRQDZ# 18

P\_IRQEA# 18

P\_IRQEB# 18

P\_IRQEC# 18

P\_IRQED# 18

P\_IRQEF# 18

P\_IRQEG# 18

P\_IRQEH# 18

P\_IRQEI# 18

P\_IRQEJ# 18

P\_IRQEK# 18

P\_IRQEL# 18

P\_IRQEM# 18

P\_IRQEN# 18

P\_IRQEO# 18

P\_IRQEP# 18

P\_IRQEQ# 18

P\_IRQER# 18

P\_IRQES# 18

P\_IRQET# 18

P\_IRQEU# 18

P\_IRQEV# 18

P\_IRQEW# 18

P\_IRQEX# 18

P\_IRQEY# 18

P\_IRQEZ# 18

P\_IRQFA# 18

P\_IRQFB# 18

P\_IRQFC# 18

P\_IRQFD# 18

P\_IRQFE# 18

P\_IRQFF# 18

P\_IRQFG# 18

P\_IRQFH# 18

P\_IRQFI# 18

P\_IRQFJ# 18

P\_IRQFK# 18

P\_IRQFL# 18

P\_IRQFM# 18

P\_IRQFN# 18

P\_IRQFO# 18

P\_IRQFP# 18

P\_IRQFQ# 18

P\_IRQFR# 18

P\_IRQFS# 18

P\_IRQFT# 18

P\_IRQFU# 18

P\_IRQFV# 18

P\_IRQFW# 18

P\_IRQFX# 18

P\_IRQFY# 18

P\_IRQFZ# 18

P\_IRQGA# 18

P\_IRQGB# 18

P\_IRQGC# 18

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P\_IRQGE# 18

P\_IRQGF# 18

P\_IRQGG# 18

P\_IRQGH# 18

P\_IRQGI# 18

P\_IRQGJ# 18

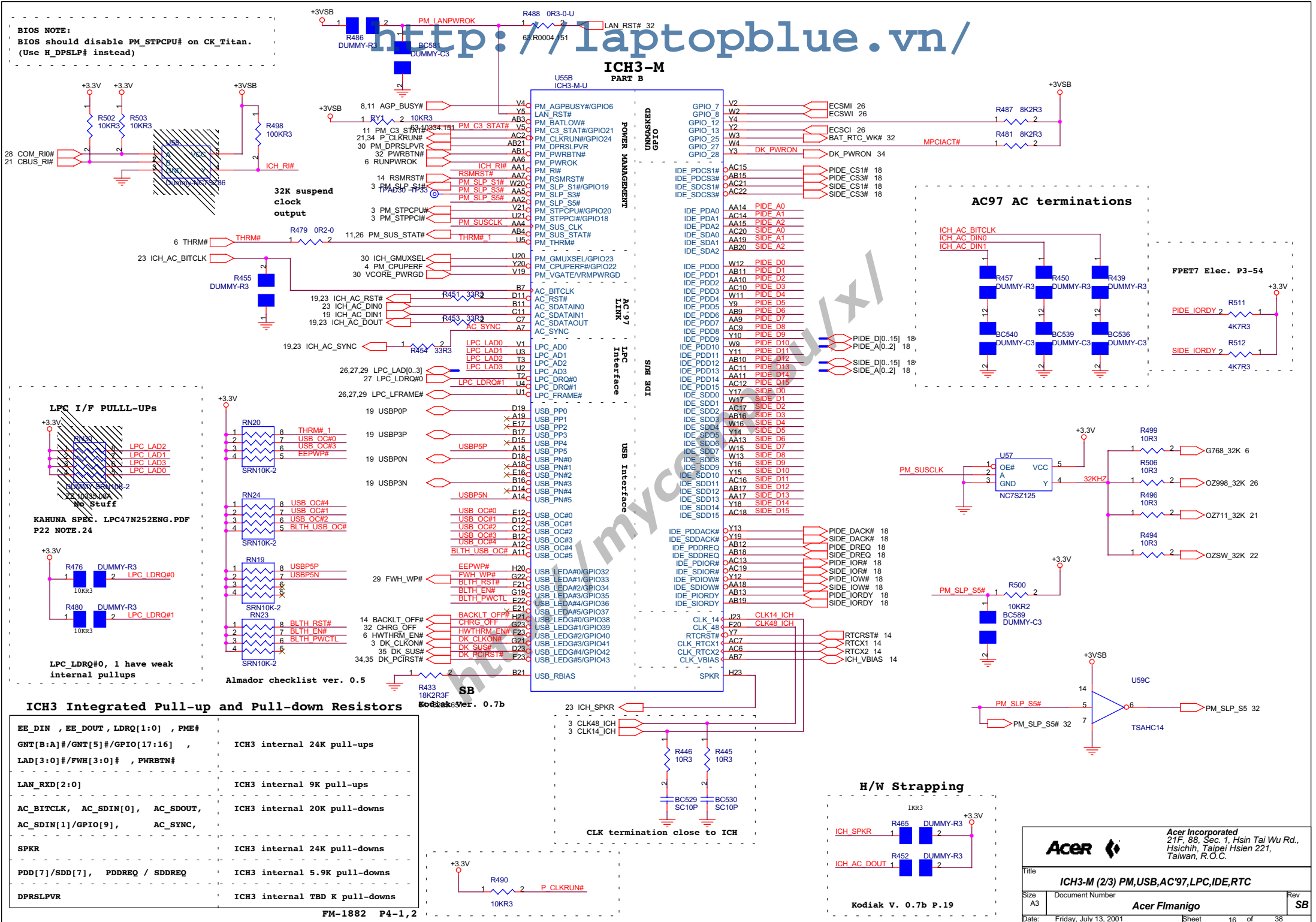
P\_IRQGK# 18

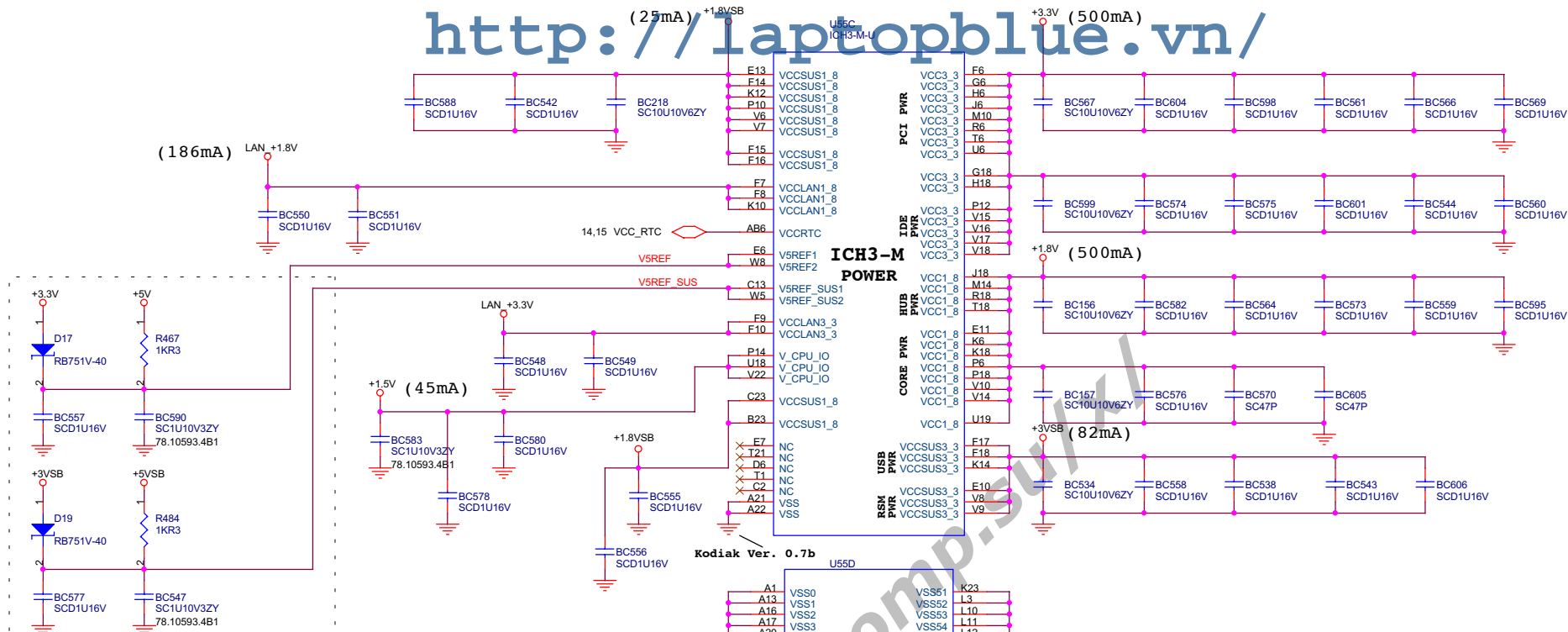
P\_IRQGL# 18

P\_IRQGM# 18

P\_IRQGN# 18

BIOS NOTE:  
BIOS should disable PM\_STPCPU# on CK\_Titan.  
(Use H\_DPSLP# instead)





\*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail  
FPET7 Elec. P3-62

### ICH3 H/W Pin Straps

### FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode (ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH3 will disable the TXO Timer system reboot feature).

### ICH3-M VSS

A1	VSS0	VSS51	K23
A13	VSS1	VSS52	L3
A16	VSS2	VSS53	L10
A17	VSS3	VSS54	L11
A20	VSS4	VSS55	L12
A23	VSS5	VSS56	L13
B8	VSS6	VSS57	L14
B10	VSS7	VSS58	L21
B13	VSS8	VSS59	L23
B14	VSS9	VSS60	M11
B15	VSS10	VSS61	M12
B18	VSS11	VSS62	M13
B19	VSS12	VSS63	M20
B20	VSS13	VSS64	M22
B22	VSS14	VSS65	N5
C3	VSS15	VSS66	N10
C6	VSS16	VSS67	N11
F19	VSS17	VSS68	N12
C14	VSS18	VSS69	N13
C15	VSS19	VSS70	N14
C16	VSS20	VSS71	N21
C17	VSS21	VSS72	N23
C18	VSS22	VSS73	P11
C19	VSS23	VSS74	P13
C20	VSS24	VSS75	P20
C21	VSS25	VSS76	P22
C22	VSS26	VSS77	R3
D9	VSS27	VSS78	R5
D13	VSS28	VSS79	R21
D16	VSS29	VSS80	R23
D17	VSS30	VSS81	T4
D20	VSS31	VSS82	T20
D21	VSS32	VSS83	T22
D22	VSS33	VSS84	V3
E5	VSS34	VSS85	AC23
E15	VSS35	VSS86	V20
E18	VSS36	VSS87	W6
F22	VSS37	VSS88	W7
E19	VSS38	VSS89	W10
E20	VSS39	VSS90	W14
F22	VSS40	VSS91	W18
G3	VSS41	VSS92	W22
G20	VSS42	VSS93	Y8
H19	VSS43	VSS94	AA3
AA22	VSS44	VSS95	AA8
J5	VSS45	VSS96	AA12
K11	VSS46	VSS97	AA16
K13	VSS47	VSS98	AA20
K20	VSS48	VSS99	AB8
K21	VSS49	VSS100	AC1
K22	VSS50	VSS101	AC8

### Decoupling Recommendation

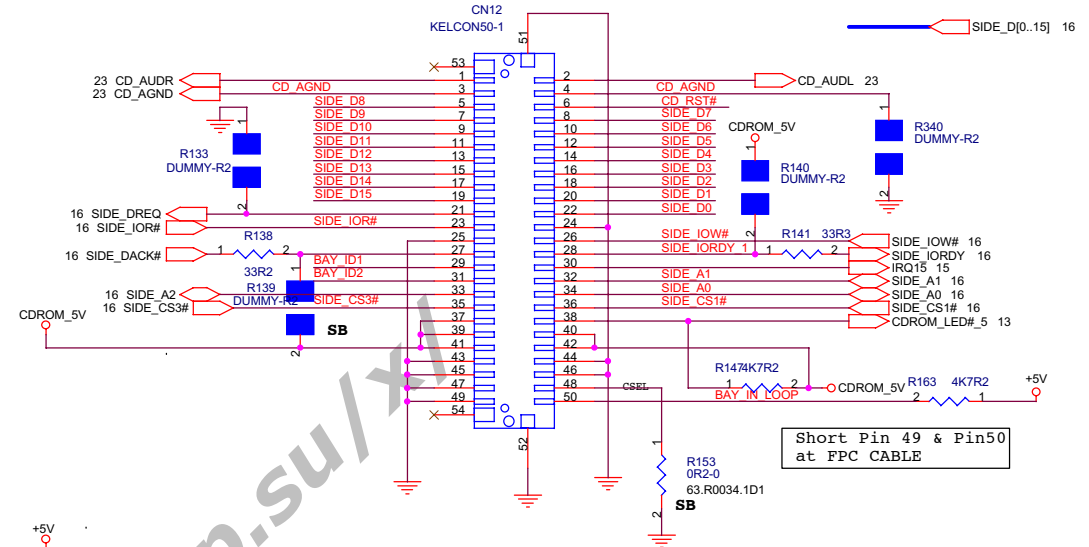
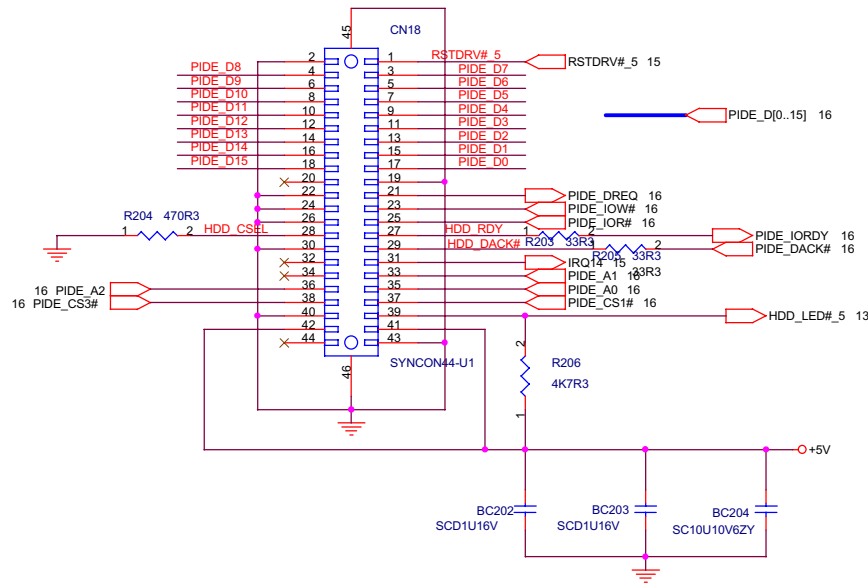
+1.5V	0.1uF * 2 1uF / 16V * 1
+1.8V	0.1uF * 5 47pF * 2
+1.8VSB	0.1uF * 3
1.8V_ICHLAN	0.1uF * 2
+3.3V	0.1uF * 13 47pF * 5
+3.3VSB	0.1uF * 8
3.3V_ICHLAN	0.1uF * 2 47pF * 1

From Kris 8/10

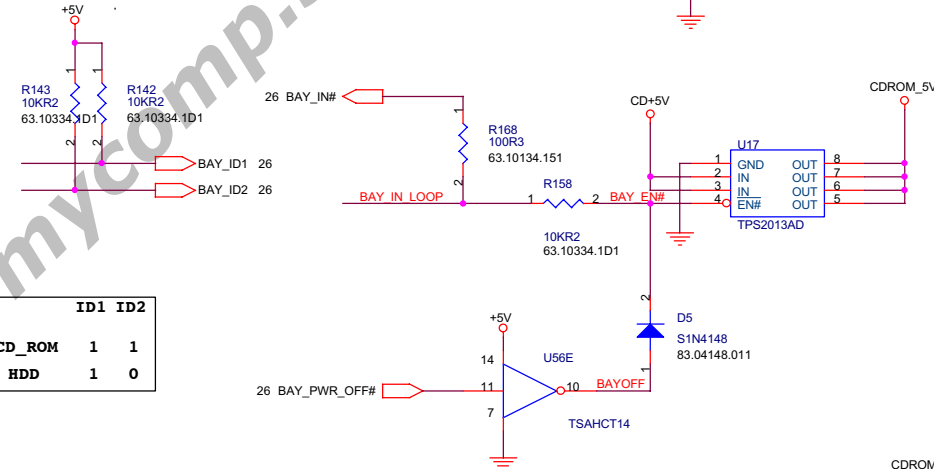
# HDD

<http://laptopblue.vn/>

# CDROM

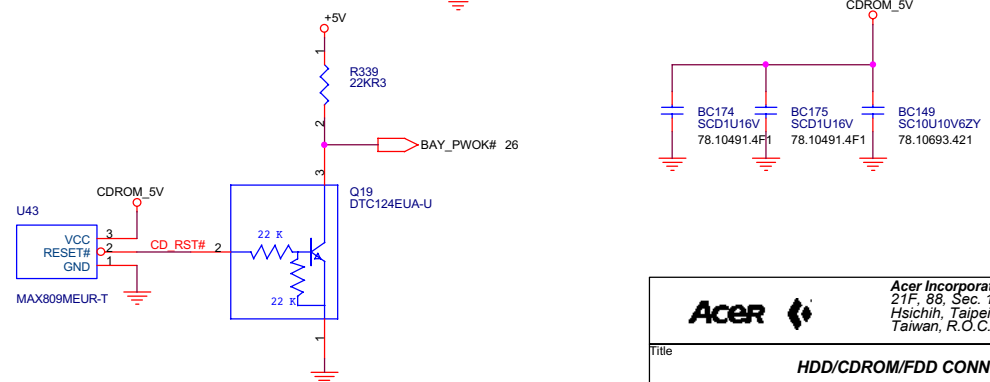
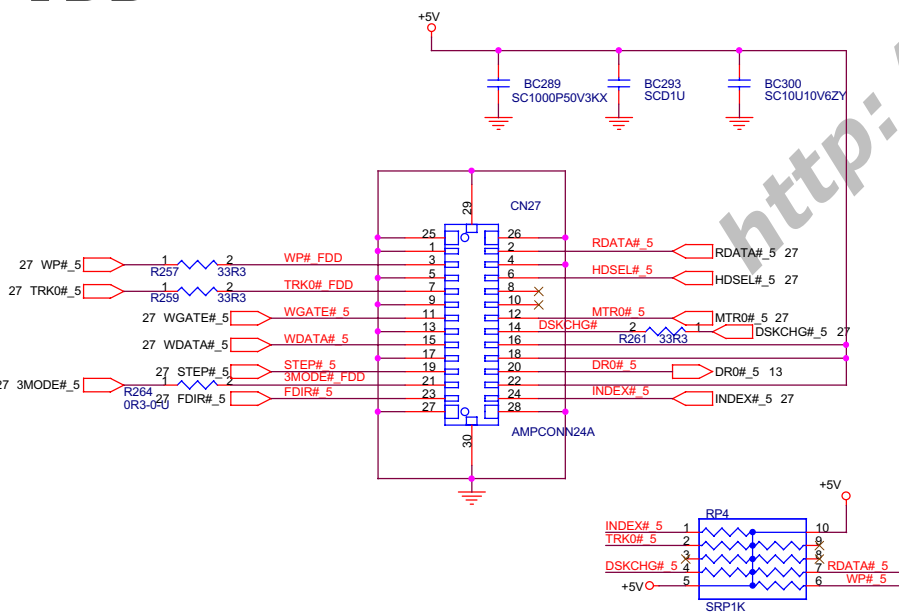


Short Pin 49 & Pin50 at FPC CABLE



	ID1	ID2
CD_ROM	1	1
HDD	1	0

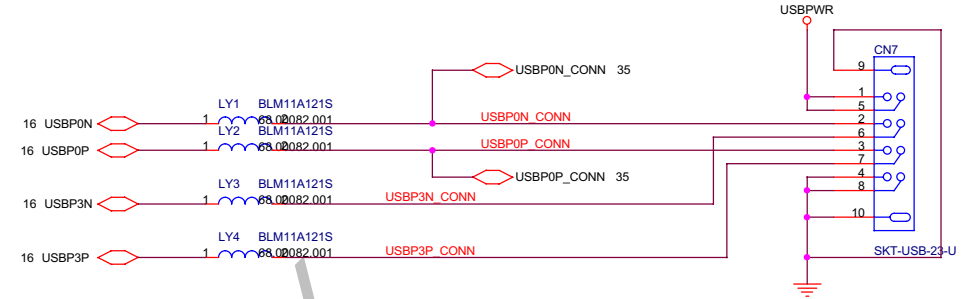
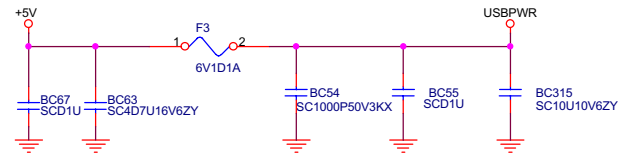
# FDD



Acer Incorporated  
21F, 88, Sec. 1, Hsin Tai Wu Rd.,  
Hsichin, Taipei Hsien 221,  
Taiwan, R.O.C.

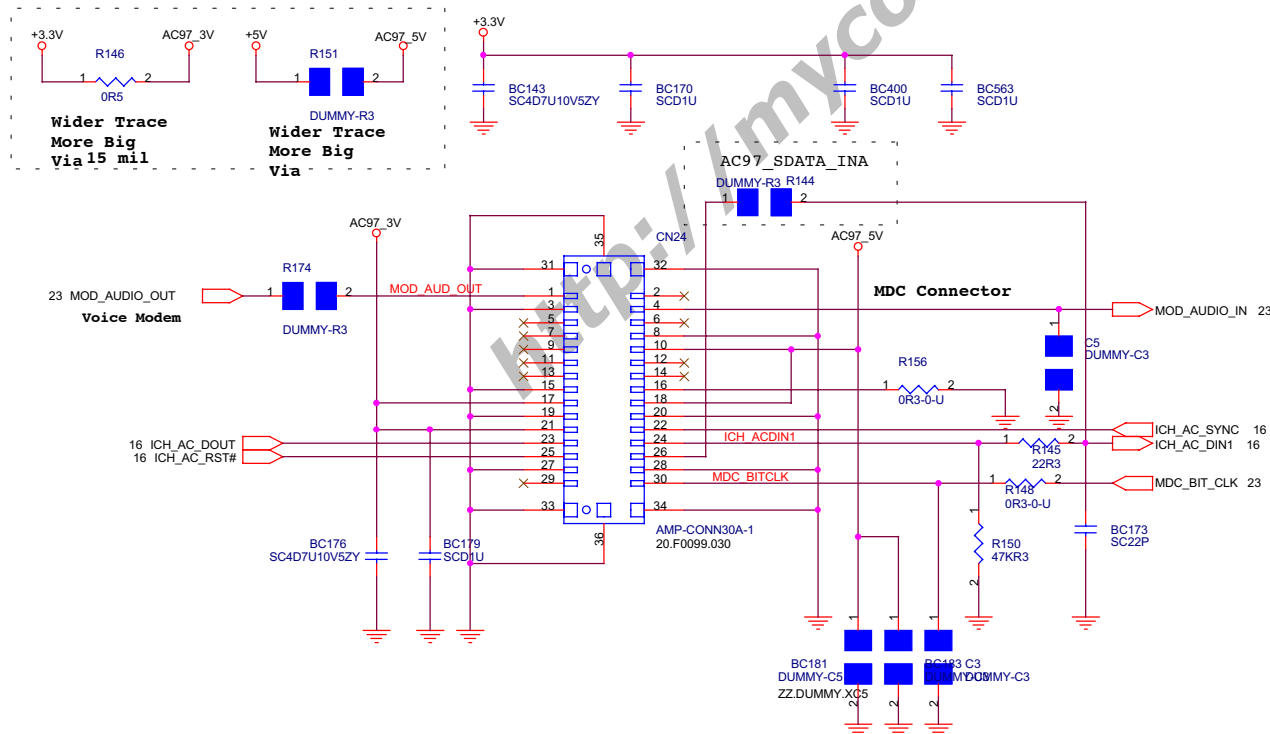
Title <b>HDD/CDROM/FDD CONN.</b>			
Size A3	Document Number <b>Acer Flmanigo</b>	Rev <b>SB</b>	
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Filtering RC network located near ICH3-M  
FPET7 Elec. P3-14

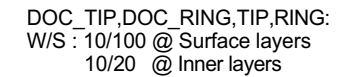
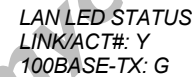
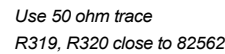
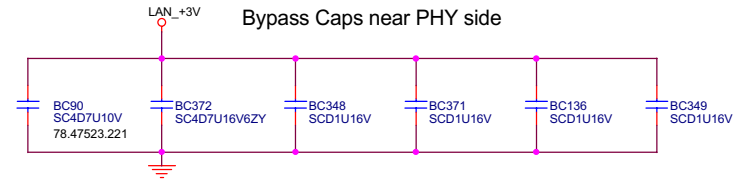


Filtering RC network located near ICH3-M  
FPET7 Elec. P3-14

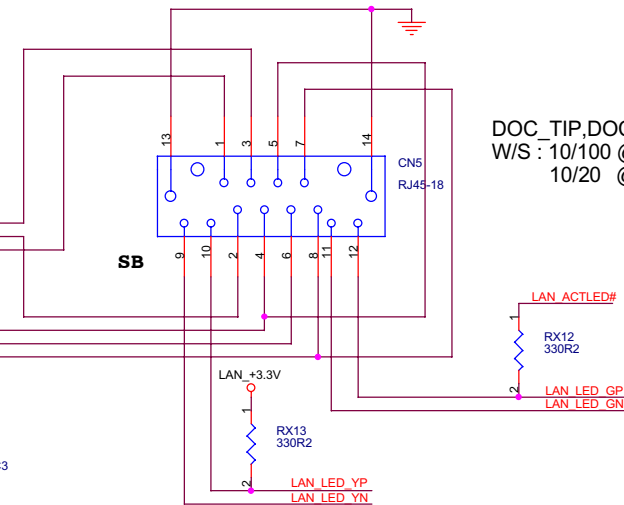
USB Common mode choke  
MURATA  
PLW3216S900SQ2



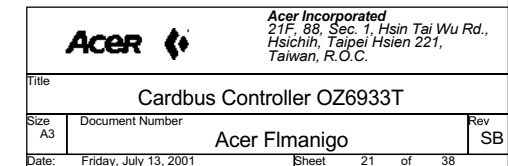
## MDC

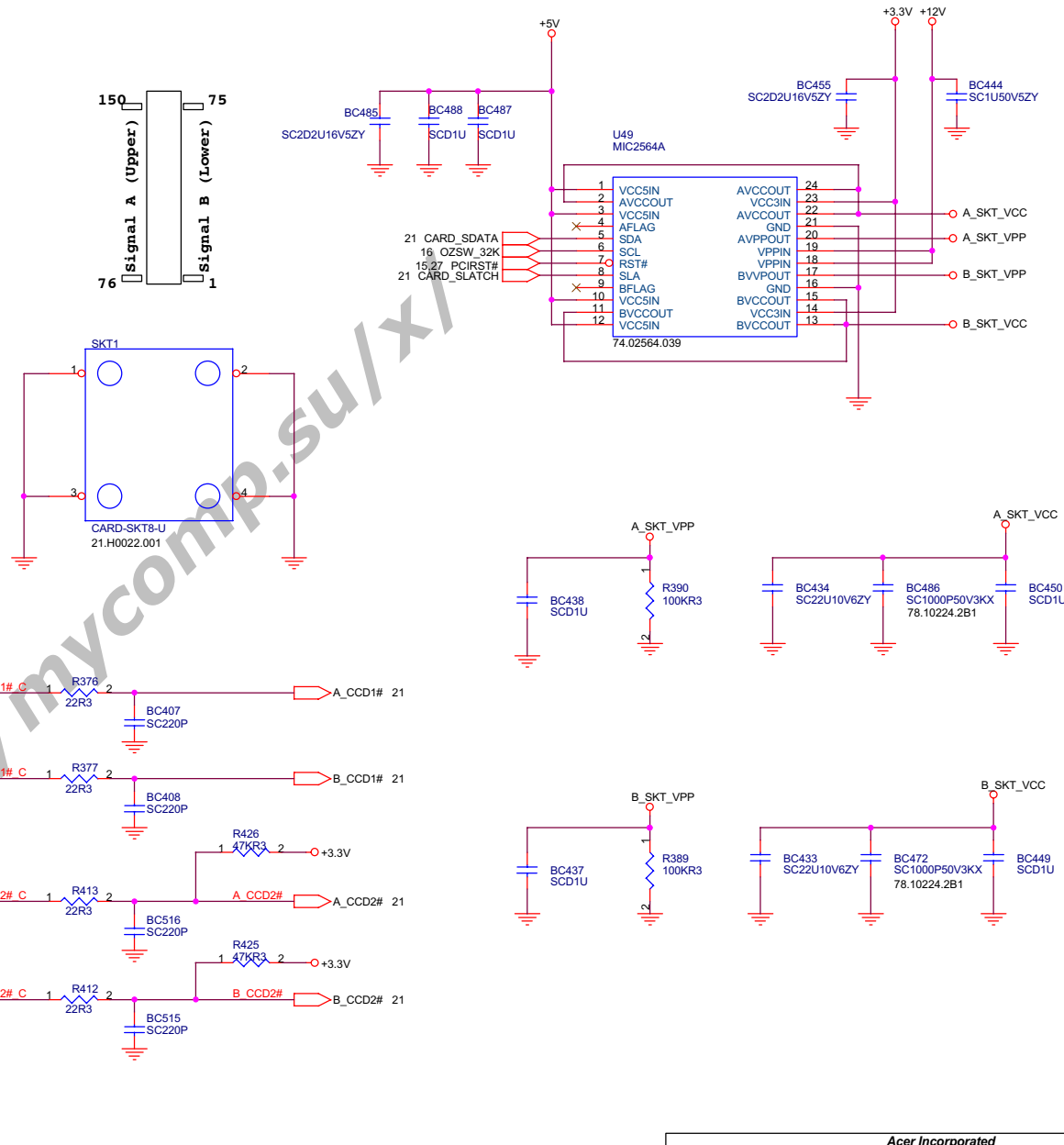


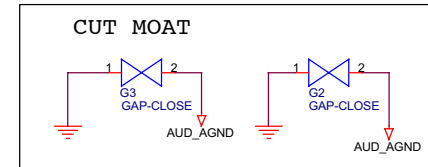
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

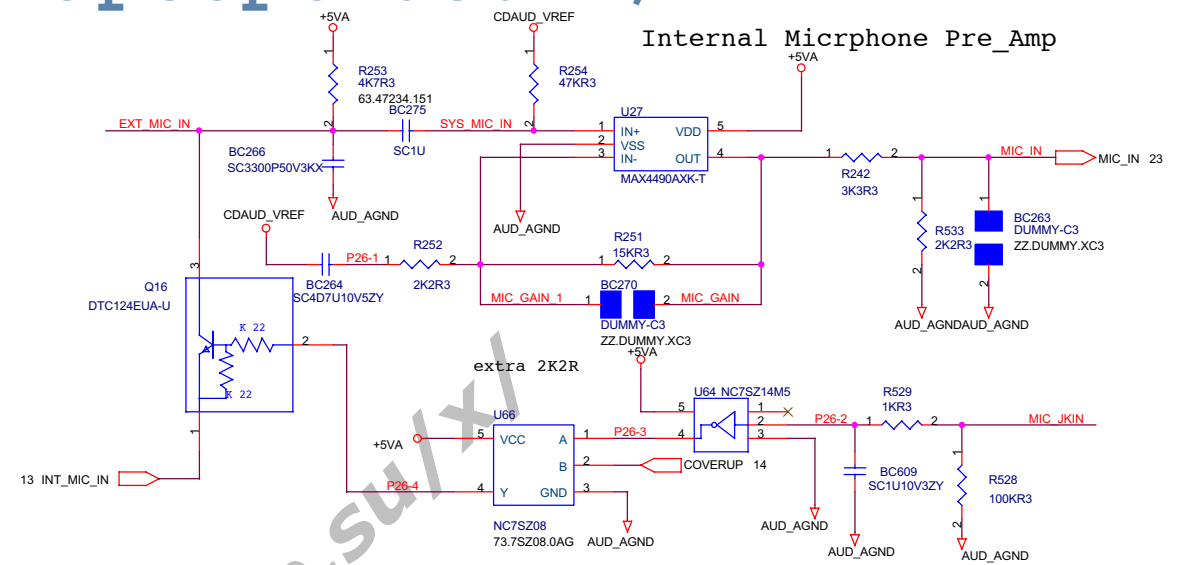




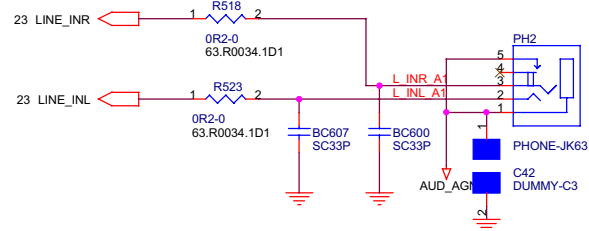




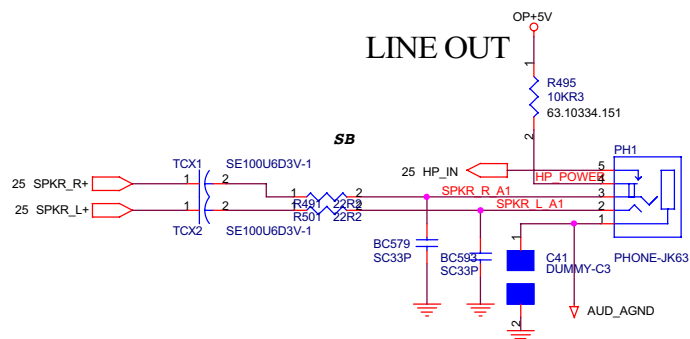




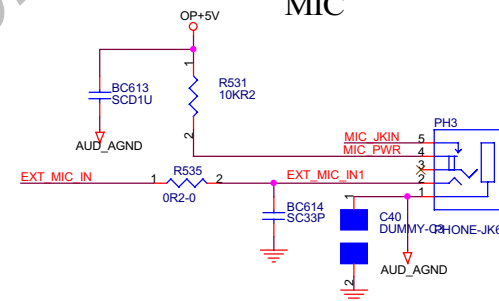
LINE IN



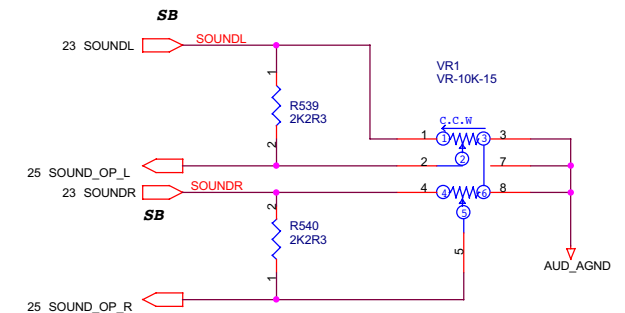
LINE OUT

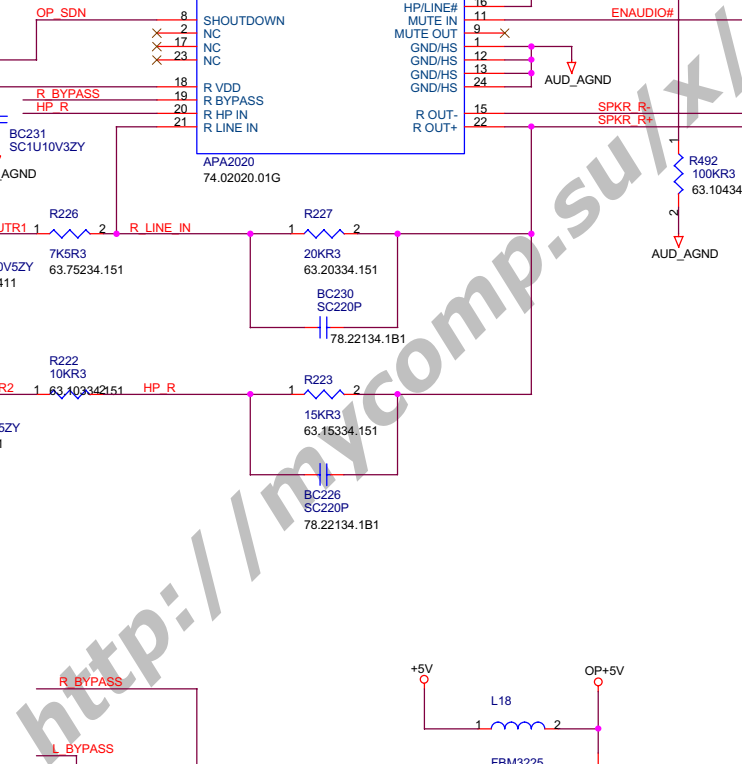


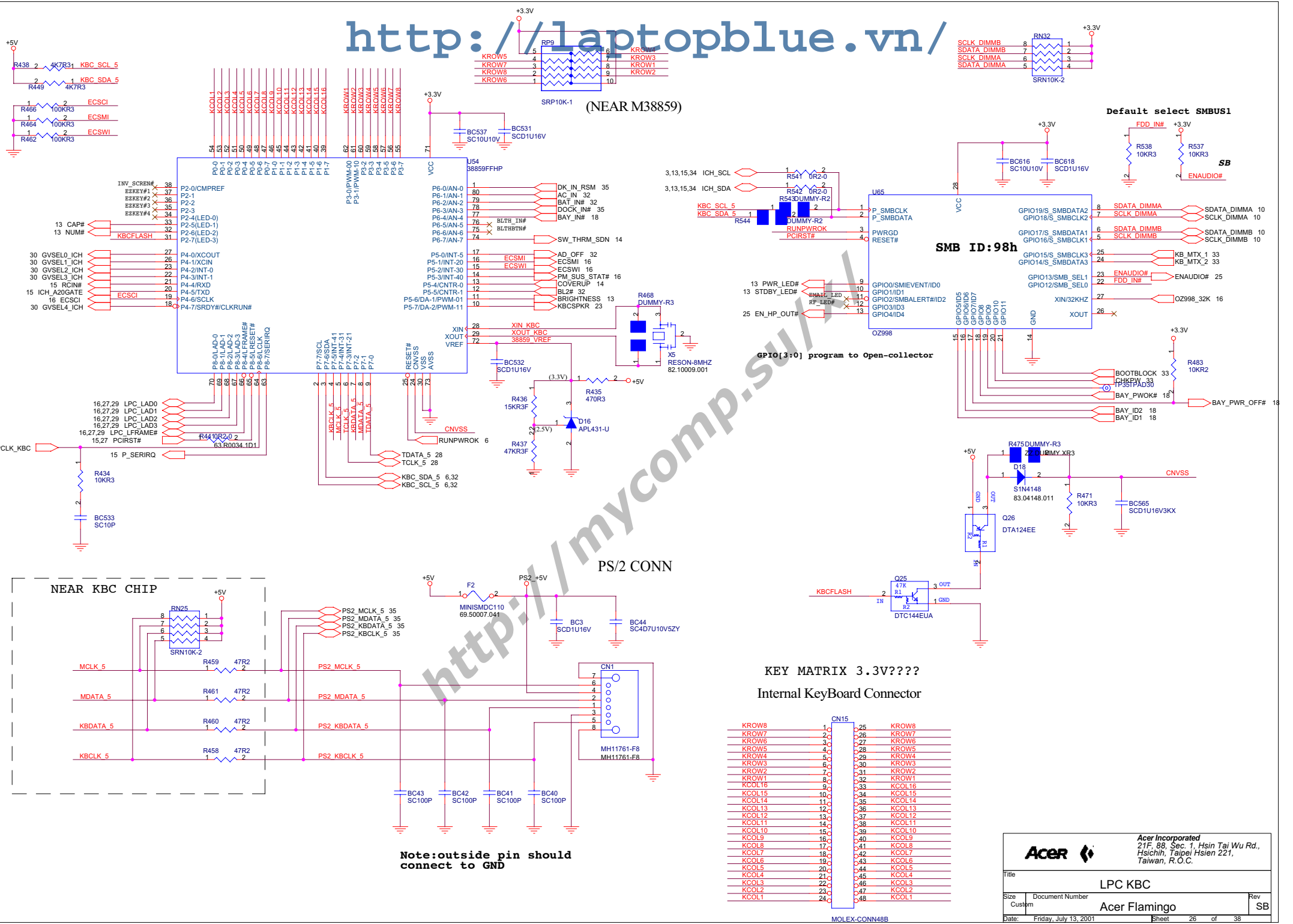
MIC



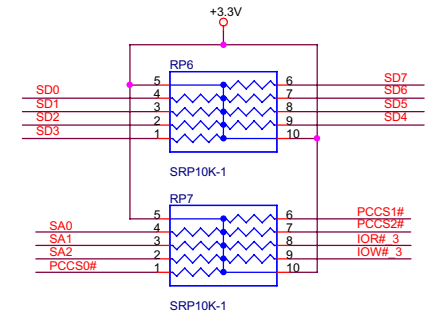
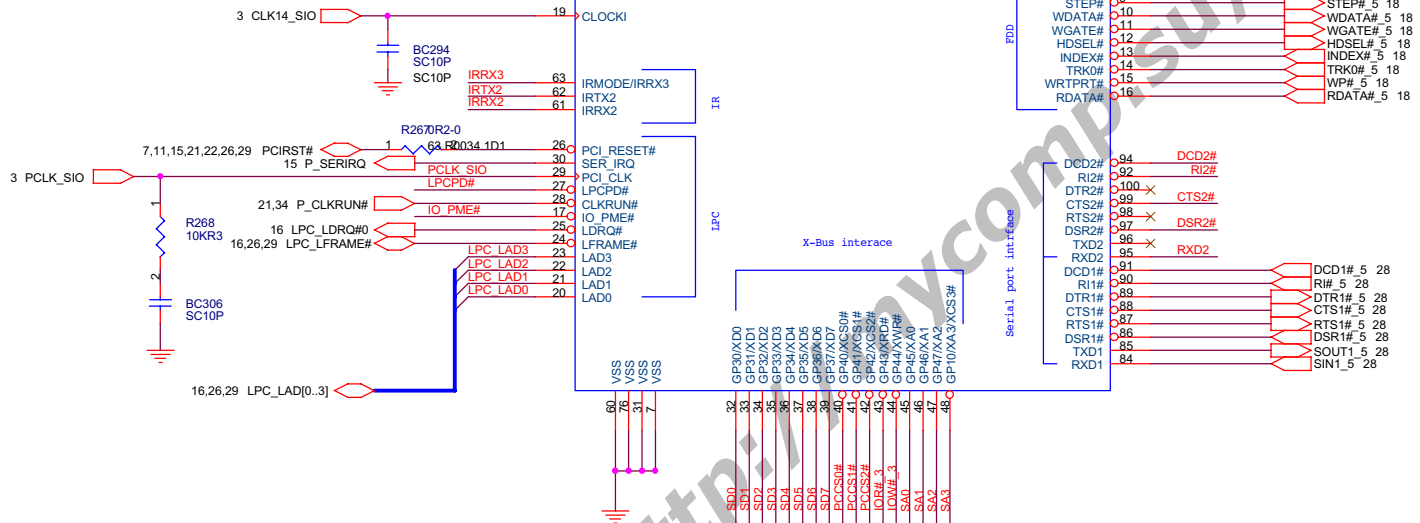
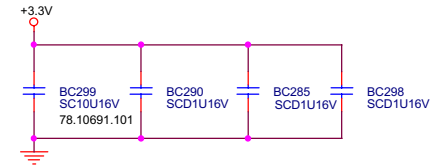
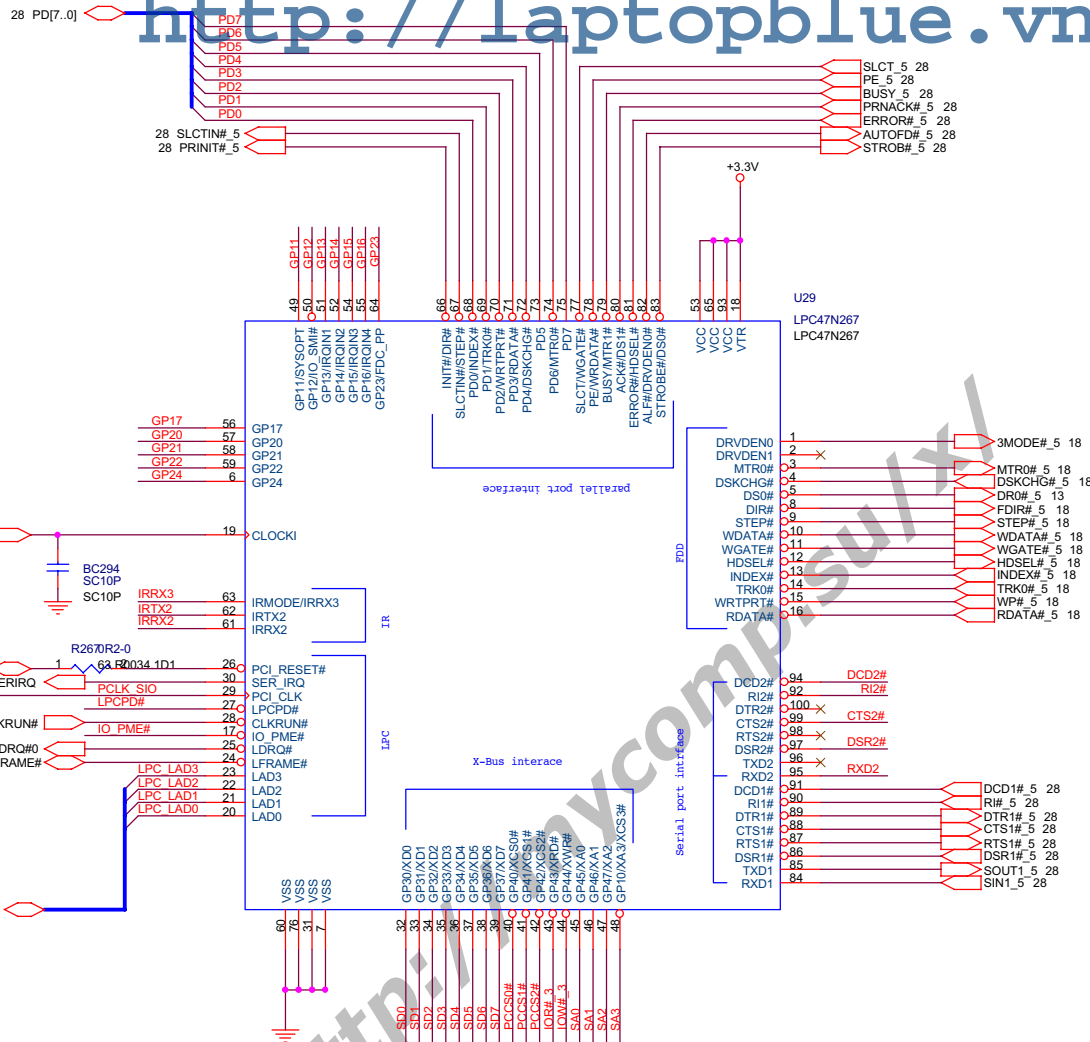
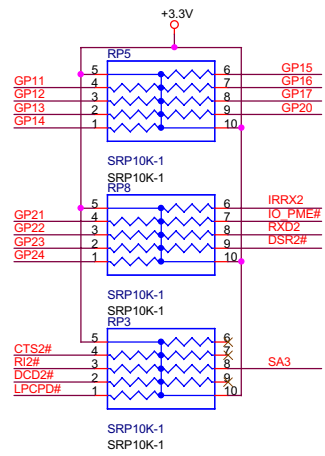
VR



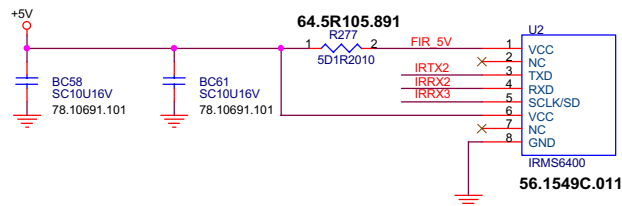






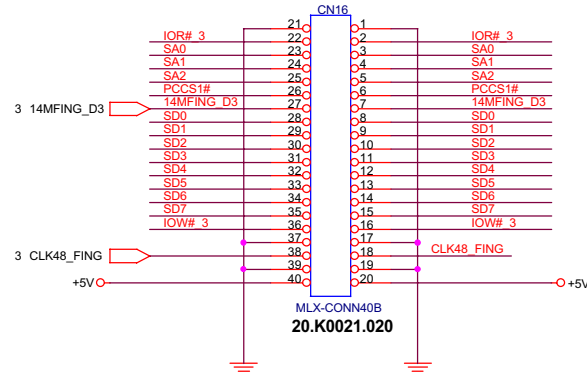


# Infineon FIR Module



**Layout Guide:**  
(1) FIR\_5V : 30 mils,  
(2) BCY1, BC50  
close to U3

**FINGER PRINTER**

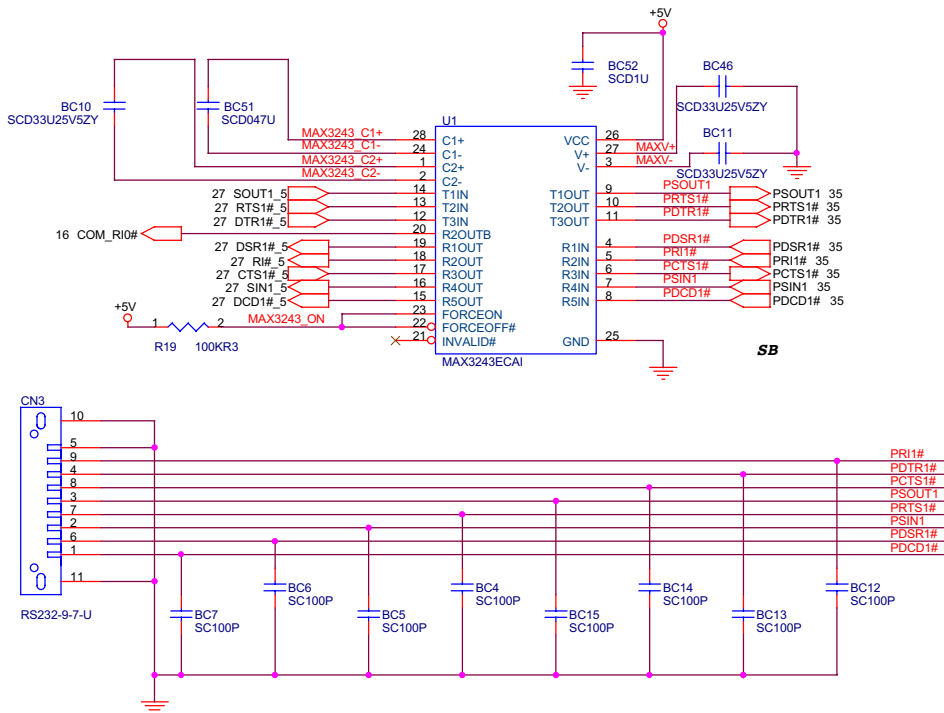


		<b>Acer Incorporated</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LPC SIO			
Size A3	Document Number		Rev
Acer Flamingo		SB	
Date:	Friday, July 13, 2001	Sheet	27 of 38

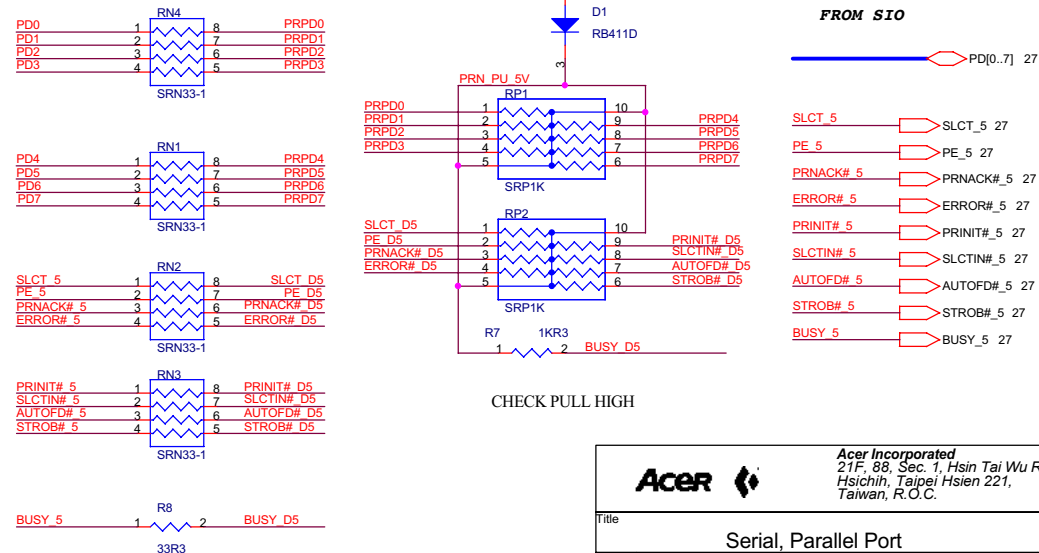
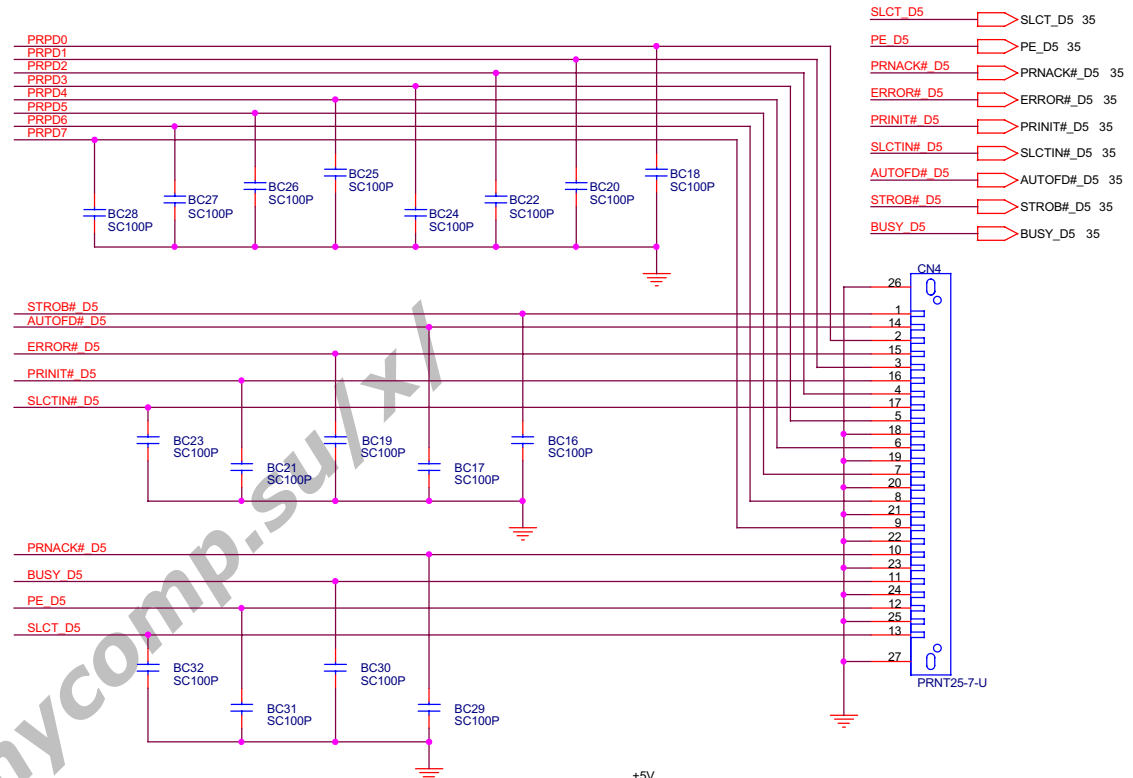
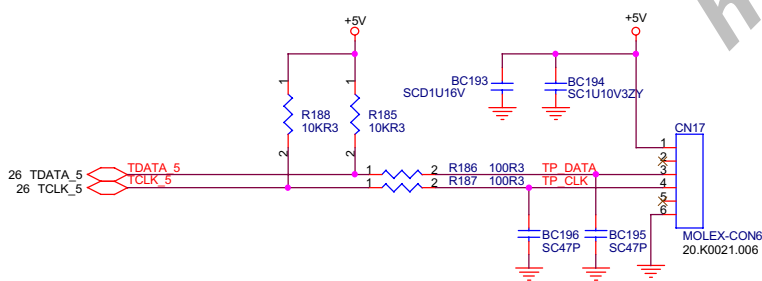
# SERIAL PORT

<http://laptopblue.com/>

# PRINTER PORT



# TOUCH PAD



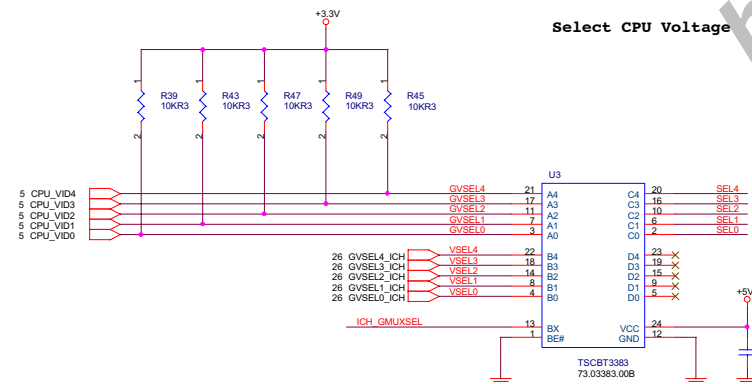
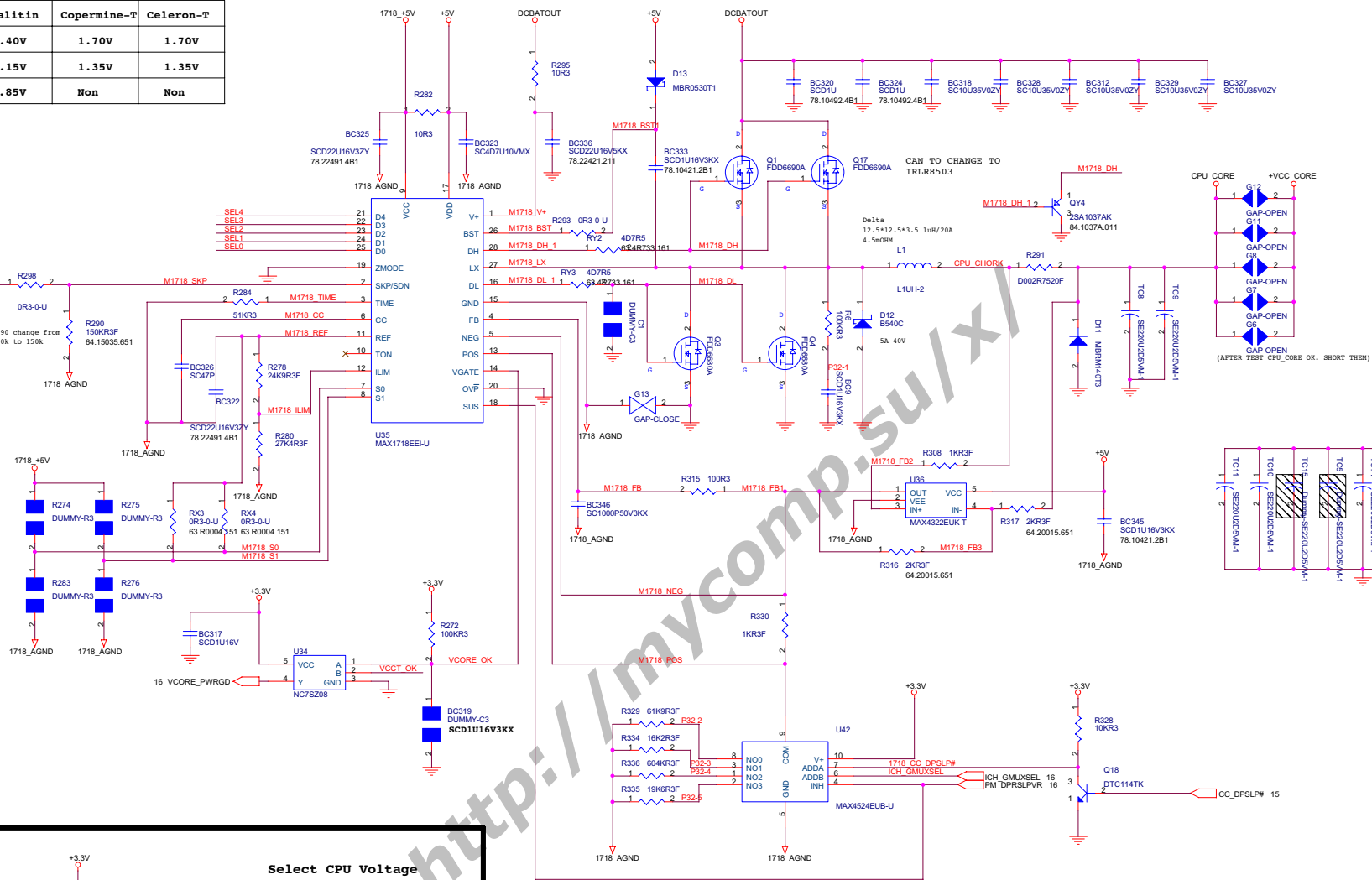
CHECK PULL HIGH

A15	(B1)
A14	(B2)
$\vdots$	$\vdots$
A2	(B14)
A1	(B15)

Mode	Tualitin	Copermine-T	Celeron-T
PERFORMANCE	1.40V	1.70V	1.70V
BATTERY	1.15V	1.35V	1.35V
Deep Sleep	0.85V	Non	Non

D4	D3	D2	D1	D0	
0	0	0	0	1	1.70V
0	0	1	0	1	1.50V
0	0	1	1	1	1.40V
0	1	0	0	1	1.30V
0	1	0	1	0	1.25V
0	1	1	0	0	1.15V

S1	S0	
REF	REF	0.850V
REF	FLOAT	0.825V
REF	VCC	0.800V
FLOAT	FLOAT	0.725V
FLOAT	VCC	0.700V
VCC	FLOAT	0.625V



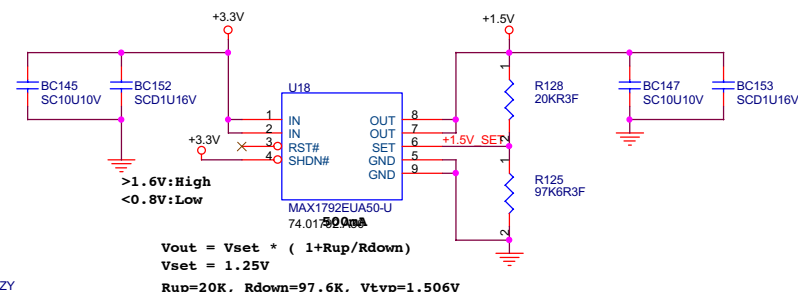
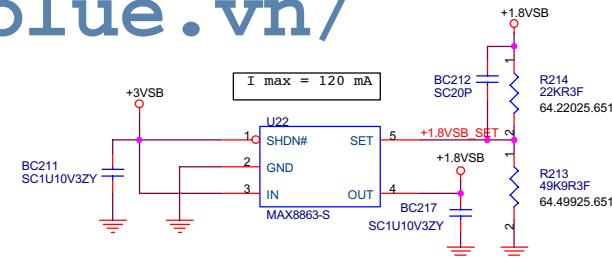
TRUE TABLE

BE#	BX	A0~A4	B0~B4
H	X	HIGH-Z	HIGH-Z
L	L	C0~C4	D0~D4
L	H	D0~D4	C0~C4

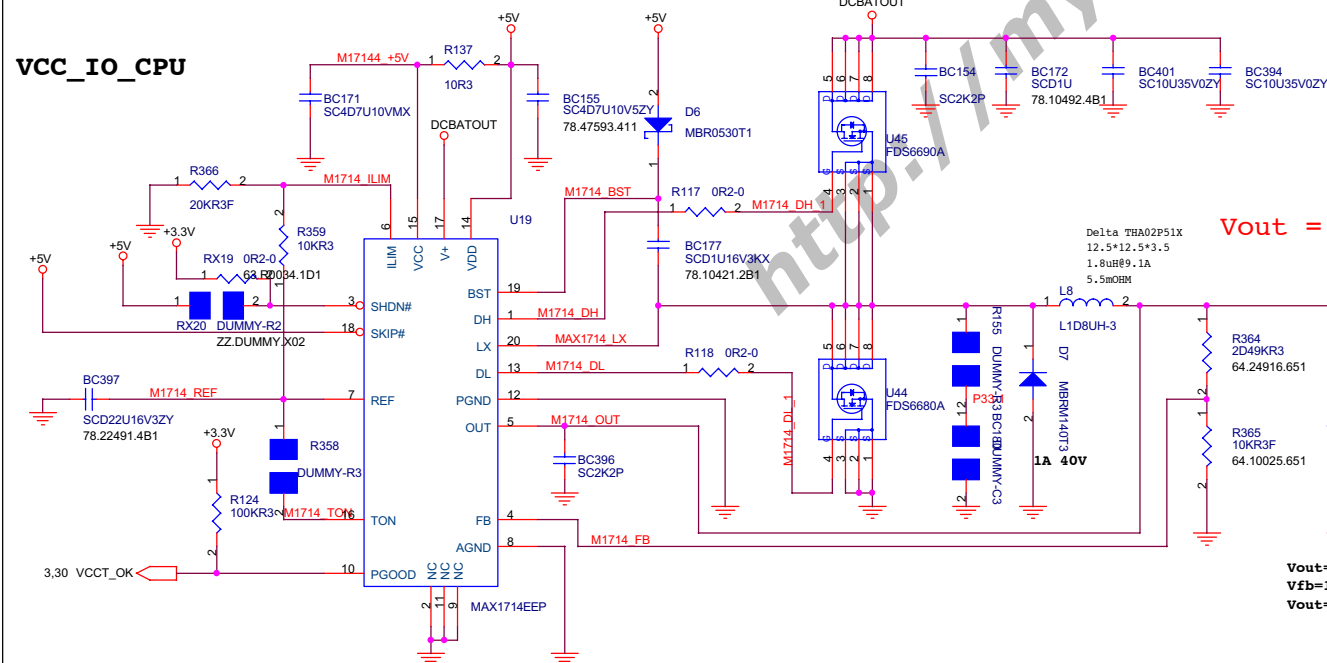
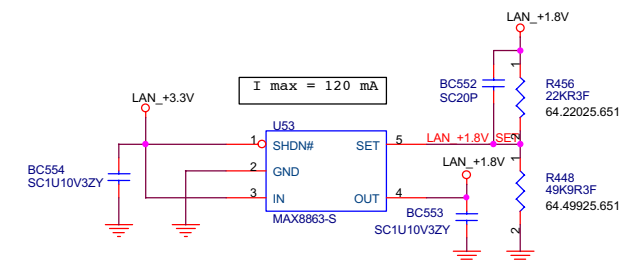
Offset Truth Table


PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

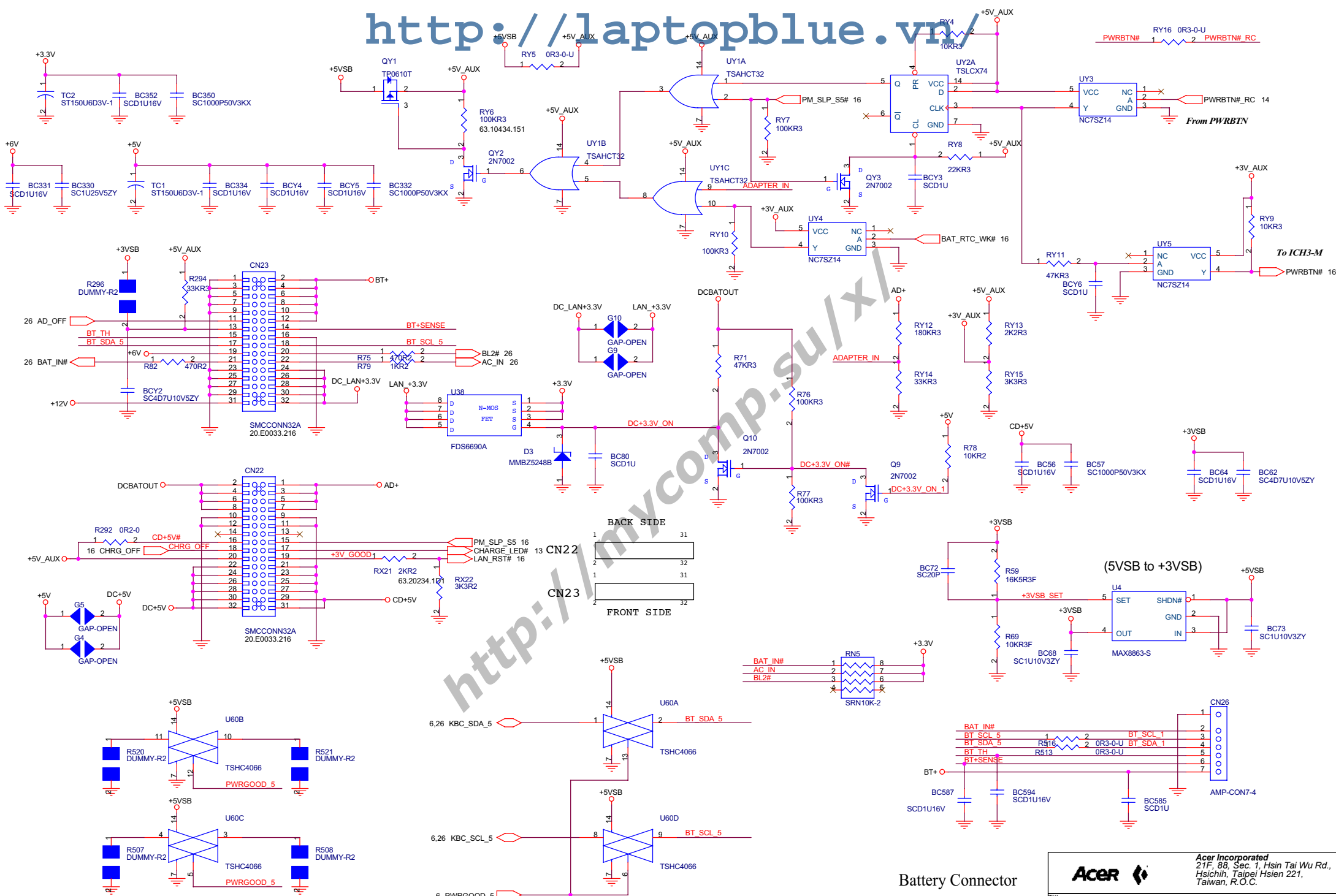
SUMIDA CDRH6D38 6R2  
6.2UH ±20%MIN.2.5A  
6.7\*6.7\*4



**SB**  
**Vout = 1.25V**



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Title			
<b>CPUIO,1.5V,1.8V,1.2V</b>			
Size A3	Document Number		Rev S1
<b>Acer Flamingo</b>			
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#### CHKPW

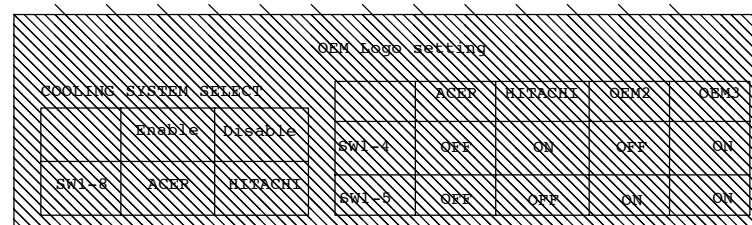
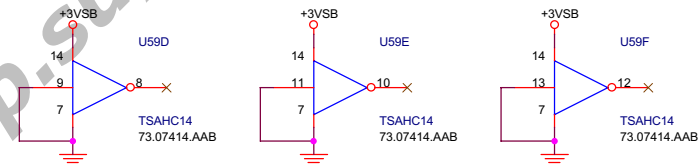
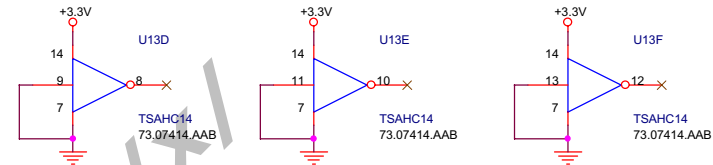
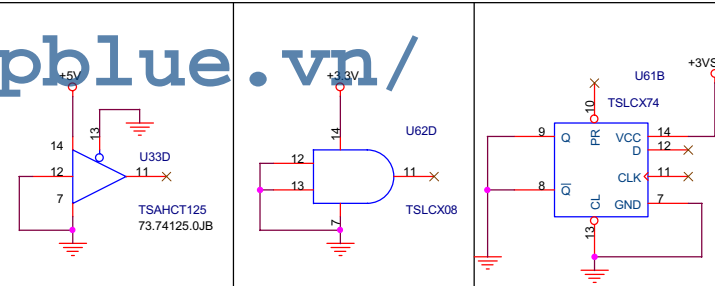
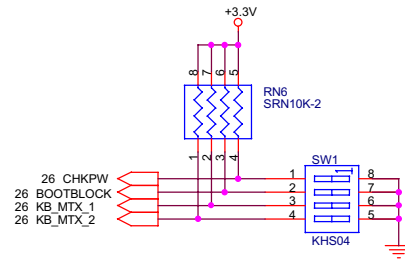
	Enable	Disable
SW1-1	ON	OFF

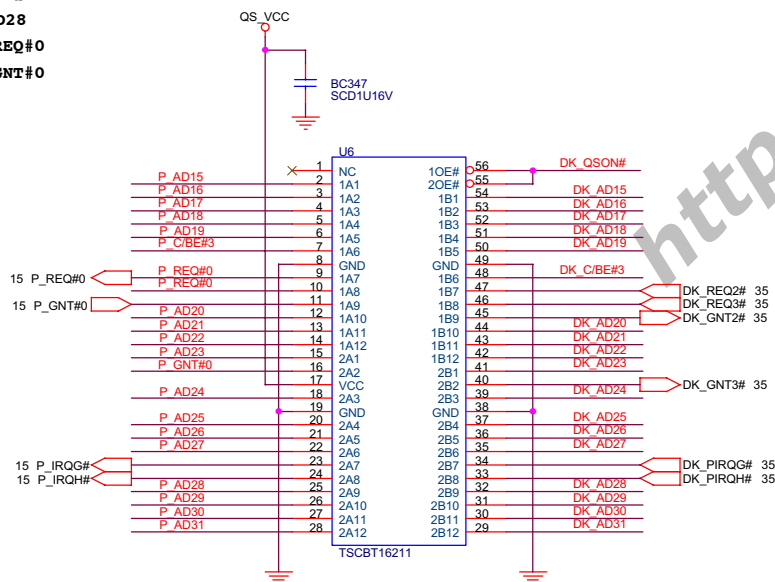
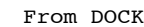
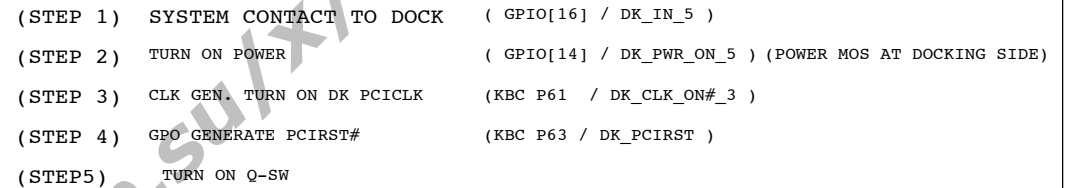
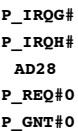
#### BIOS Bootblock erasable

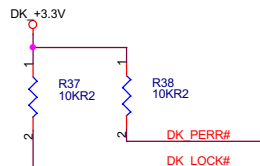
	Enable	Disable
SW1-2	ON	OFF

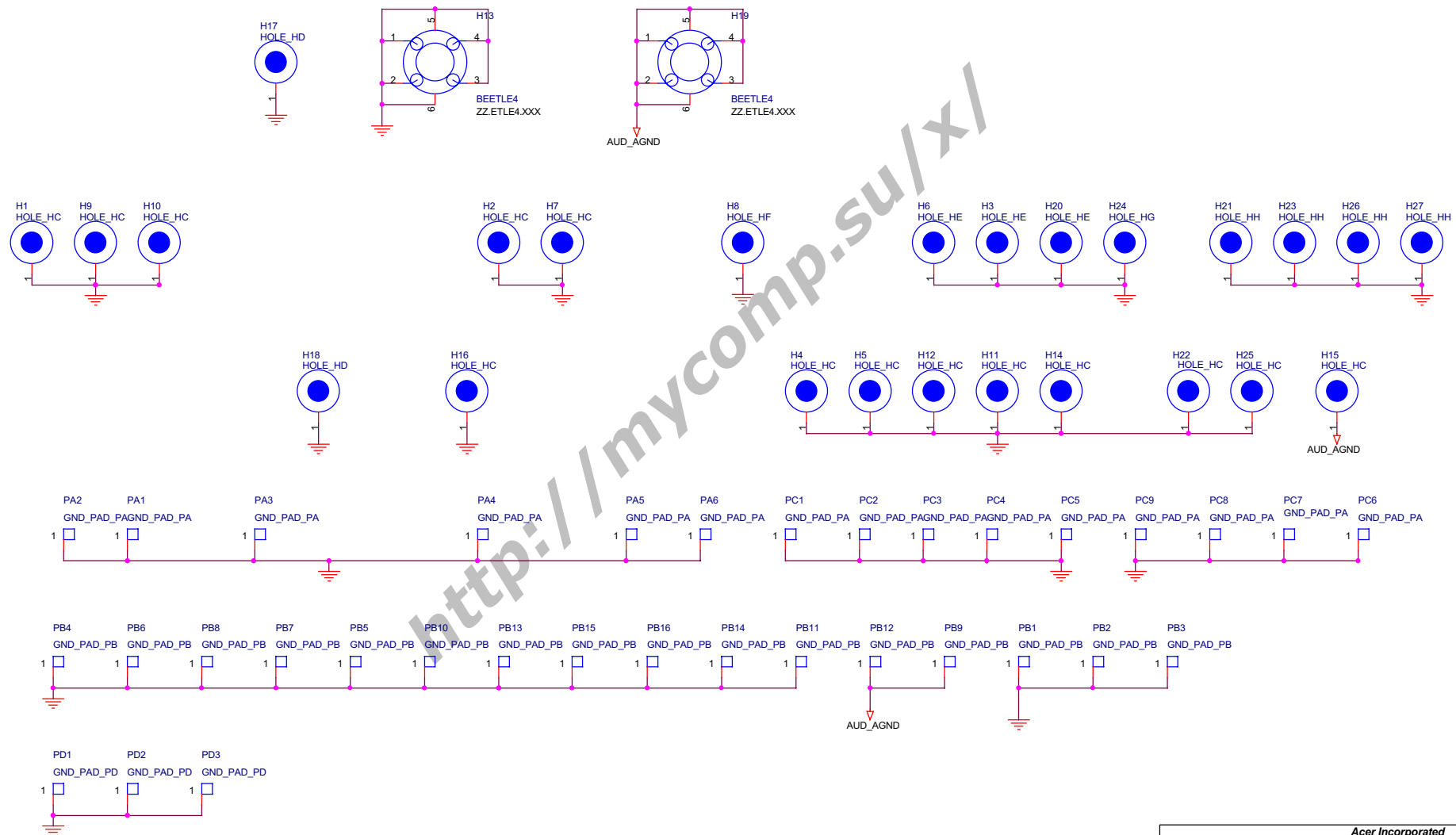
#### Keyboard matrix

	US	Jap	Europe	US international
SW1-3	OFF	ON	OFF	OFF
SW1-4	OFF	OFF	ON	OFF









## NEAR CPU

TP23 TPAD30  
ZZ.PAD30.XXX CC\_SMI# 15

## NEAR GMCH

## NEAR VGA


TP22 TPAD30  
ZZ.PAD30.XXX VGA\_MEM\_CS1# 12

## NEAR ICH3-M

TP24 TPAD30  
ZZ.PAD30.XXX P\_IRQC# 15 15 P\_REQ#2 TP25 TPAD30  
ZZ.PAD30.XXX  
TP26 TPAD30  
ZZ.PAD30.XXX P\_IRQE# 15 15 P\_REQ#3 TP27 TPAD30  
ZZ.PAD30.XXX  
TP28 TPAD30  
ZZ.PAD30.XXX P\_IRQF# 15 15 P\_REQ#4 TP29 TPAD30  
ZZ.PAD30.XXX  
15 P\_GNT#2 TP30 TPAD30  
ZZ.PAD30.XXX  
15 P\_GNT#3 TP31 TPAD30  
ZZ.PAD30.XXX  
15 P\_GNT#4 TP32 TPAD30  
ZZ.PAD30.XXX

## NEAR IEEE1394

## NEAR CARDBUS

<b>Acer</b> 		<b>Acer Incorporated</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichlin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TEST POINT			
Size A3	Document Number Acer Flamingo		Rev SB
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