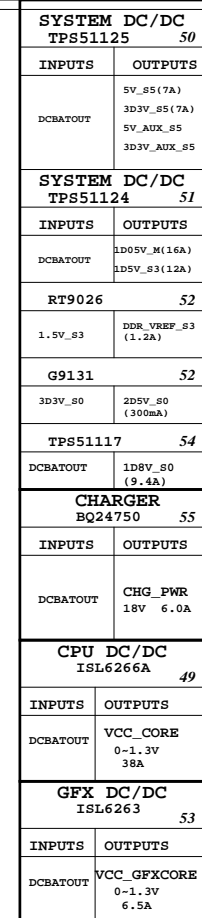


Crystal
14.318MHz



TOP _____
VCC _____
S _____
S _____
GND _____
BOTTOM _____

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

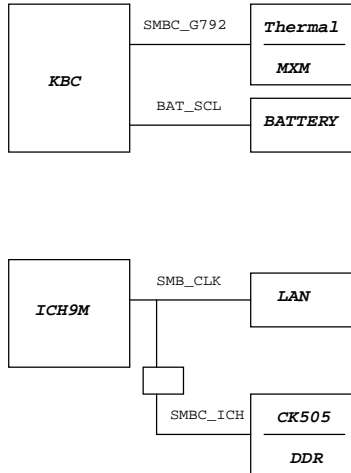
PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	NC
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(Default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:

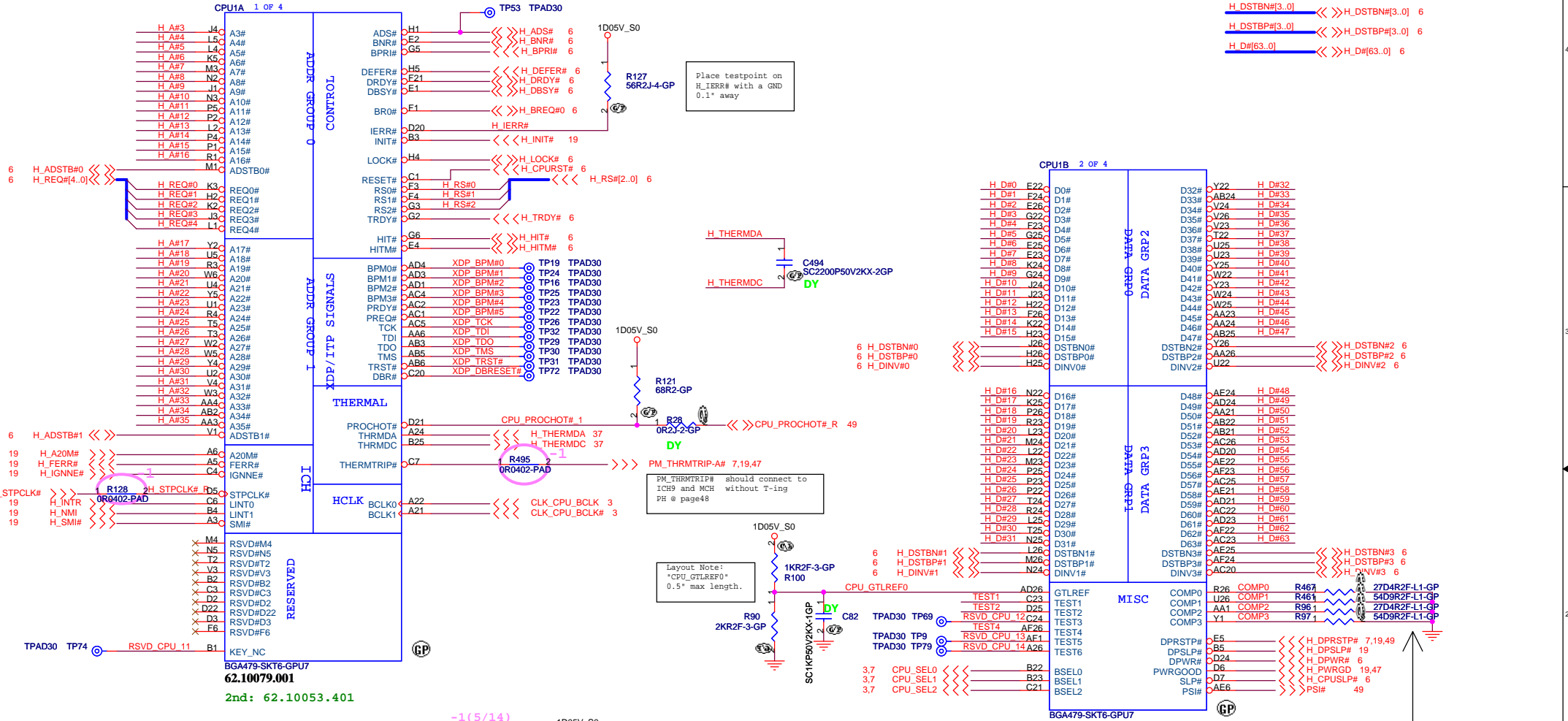
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

Four Peaks

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	Rev	
Four Peaks		-1M	
Date: Friday, November 21, 2008	Sheet 2	of	57

6 H_A#(35..3) <<>> H_A#(35..3)

H_DINV#(3..0) <<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6



Layout Note:
"CPU_GTLREF0"
0.5" max length.

PM_THRMTRIP-A# should connect to
ICH9 and MCH without T-ing
PH @ page48

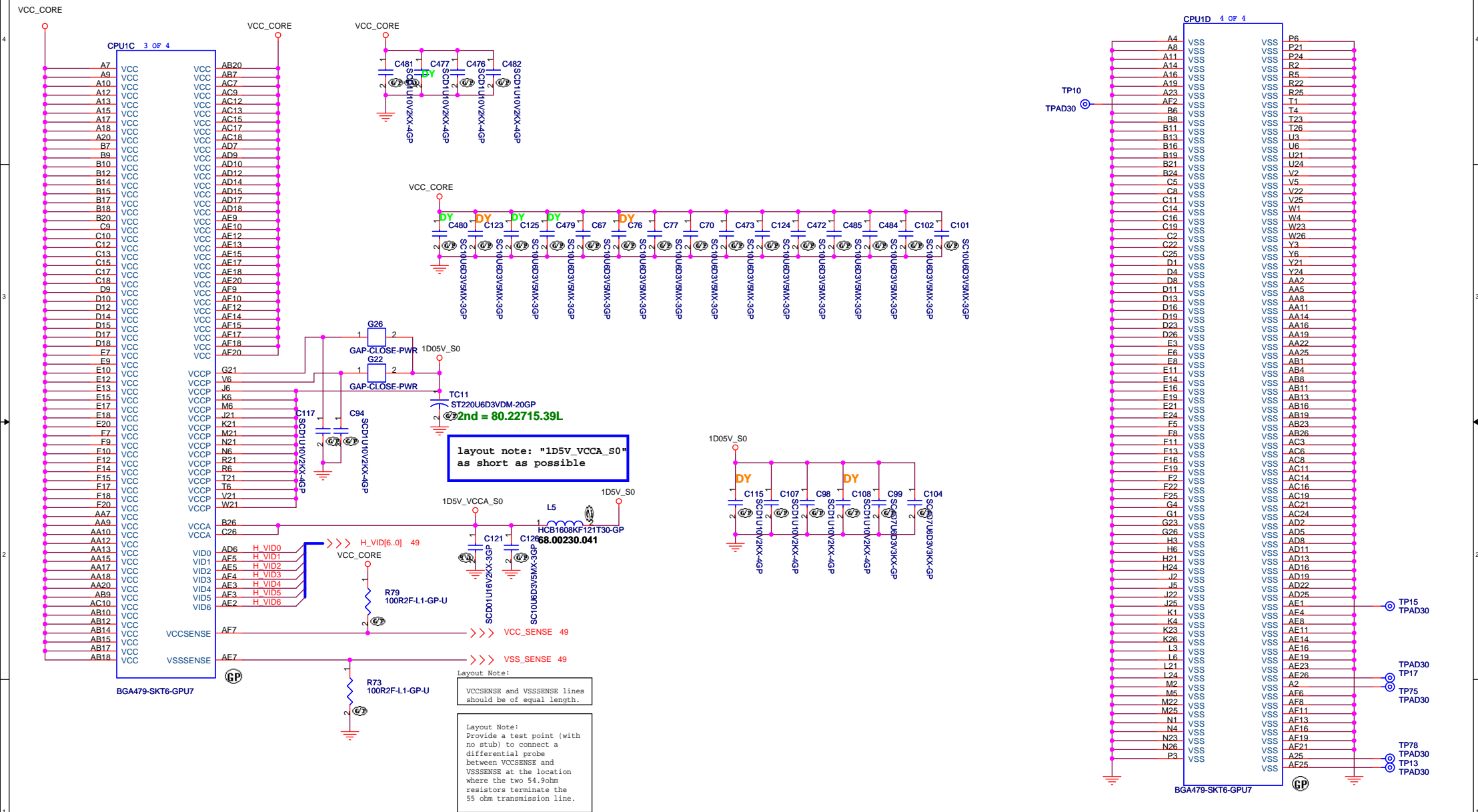
Place testpoint on
H_IERR# with a GND
0.1" away

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5"

Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals

H_DPRSTP# TP66 TPAD30
H_DPSP# TP76 TPAD30
H_DPWR# TP94 TPAD30
H_PWRGD TP105 TPAD30
H_CPUSLP# TP92 TPAD30
H_INIT# TP187 TPAD30
H_CPURST# TP71 TPAD30

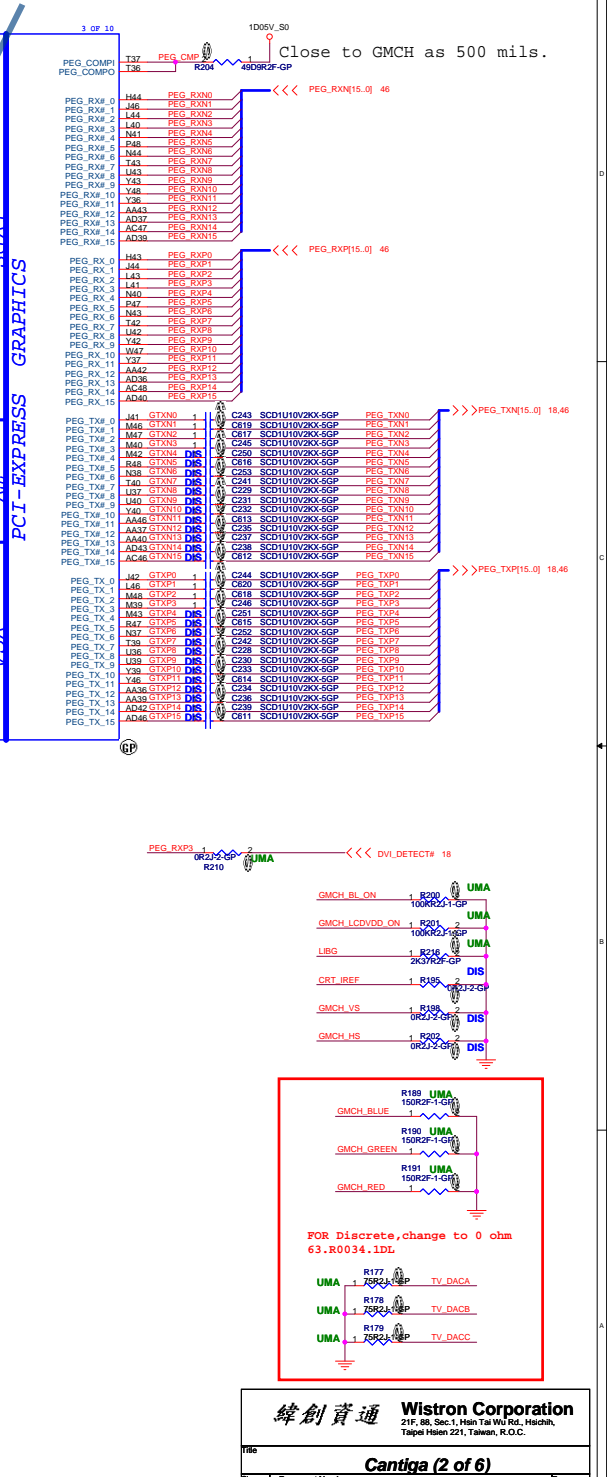
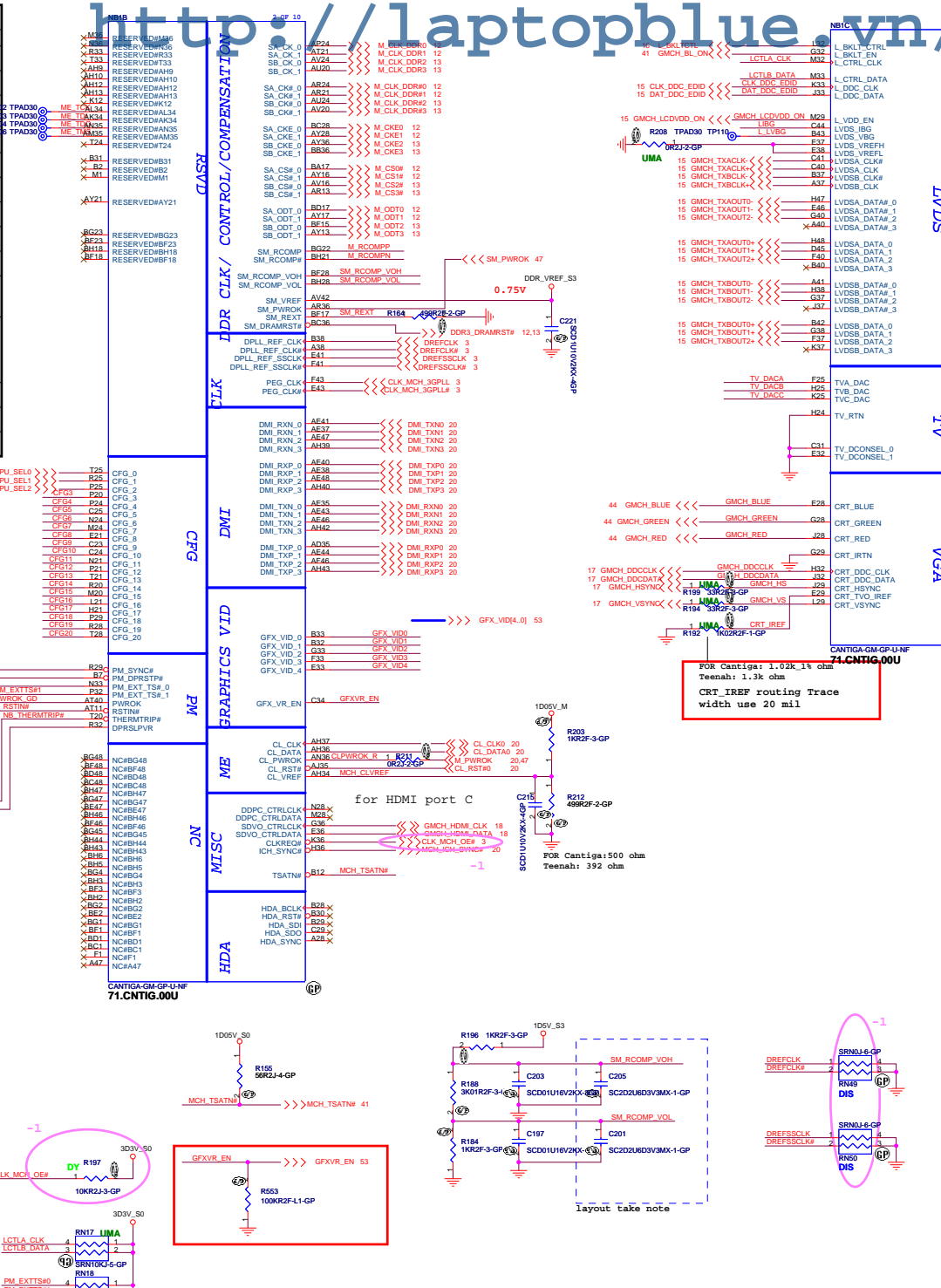
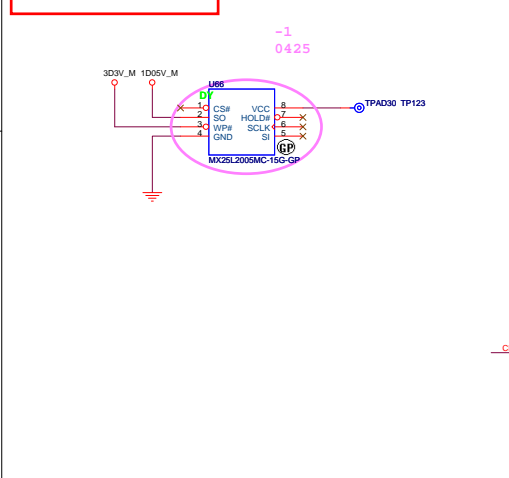
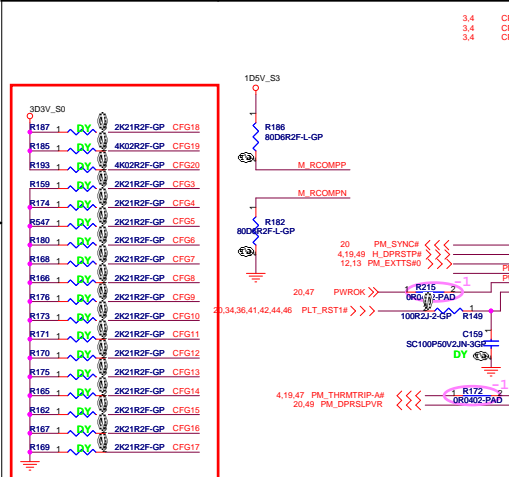
Place these TP on button-side,
easy to measure.

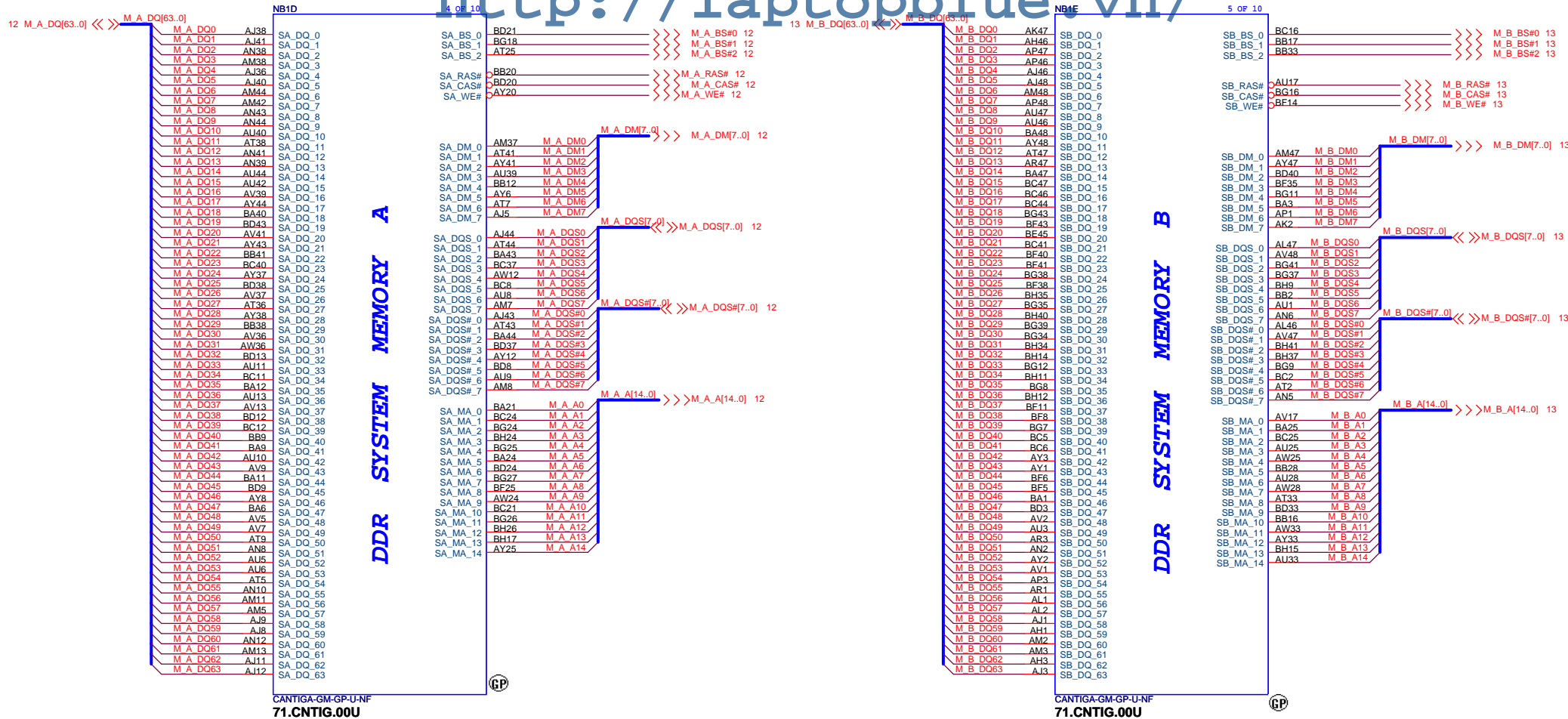


Title			
<i>Cantiga (1 of 6)</i>			
Size	Document Number		Rev
	Four Peaks		-1M
Date:	Friday, November 21, 2008	Sheet 6 of	57

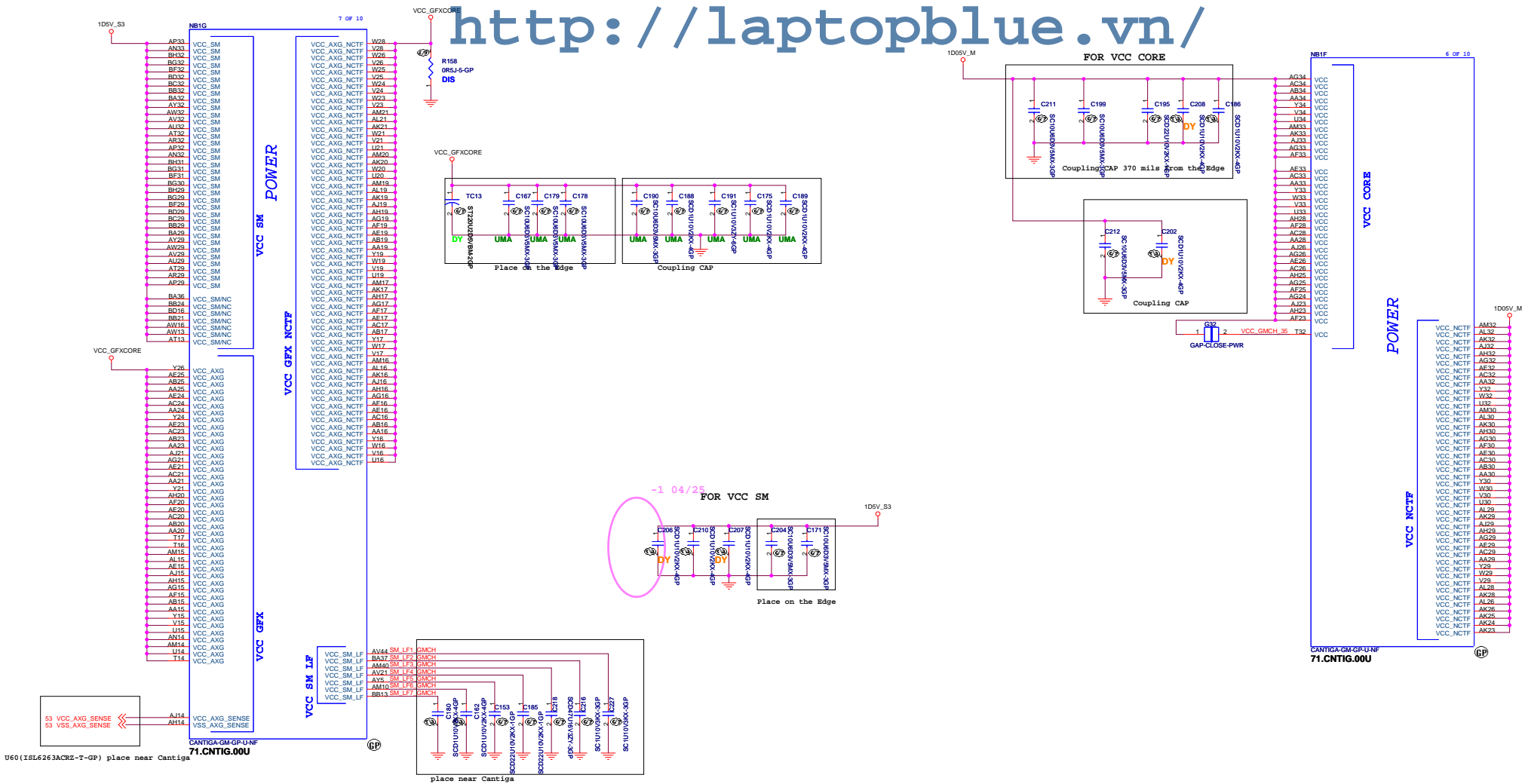
Strap Pin Table

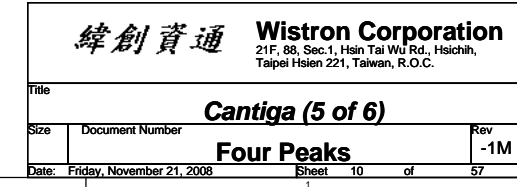
CFG2(2.0) FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4;3; 8; 11; 14; 15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x2 High = DMI x4
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality
CFG9 (PCIe Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order
CFG10 (PCIe Loopback enable)	Low = Enabled High = Disabled
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order High = Reverse Lanes DMI x4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /HDMI) Concurrent with PCIe)	Low = Only Digital Display Port (SDVO/HDMI) or PCIe is operational High = Digital Display Port (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled High = LFP Card Present; PCIe disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled High = DisplayPort Device Present



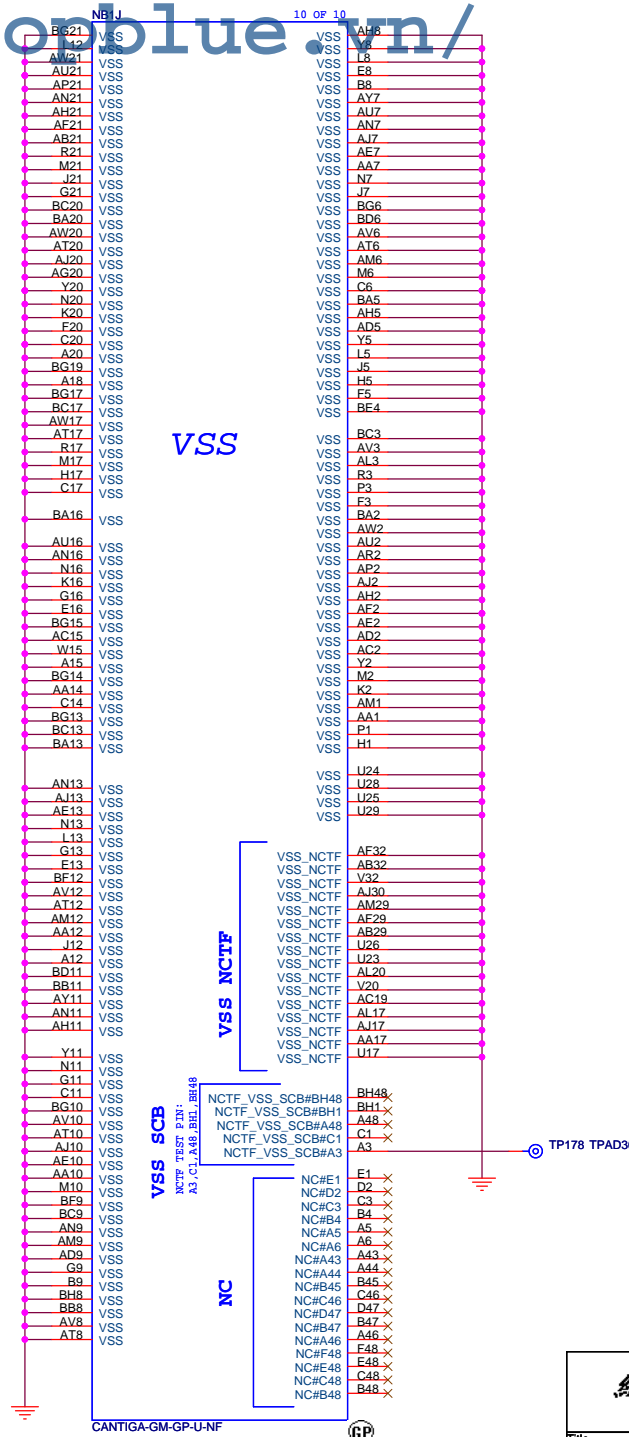
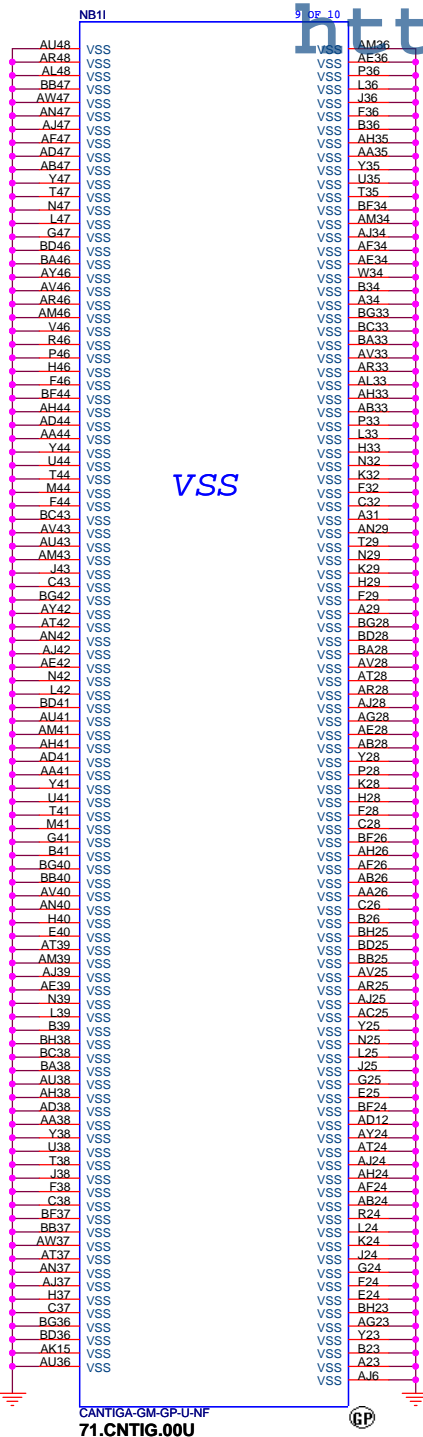


http://laptopblue.vn/

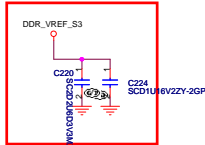




http://laptopblue.vn/

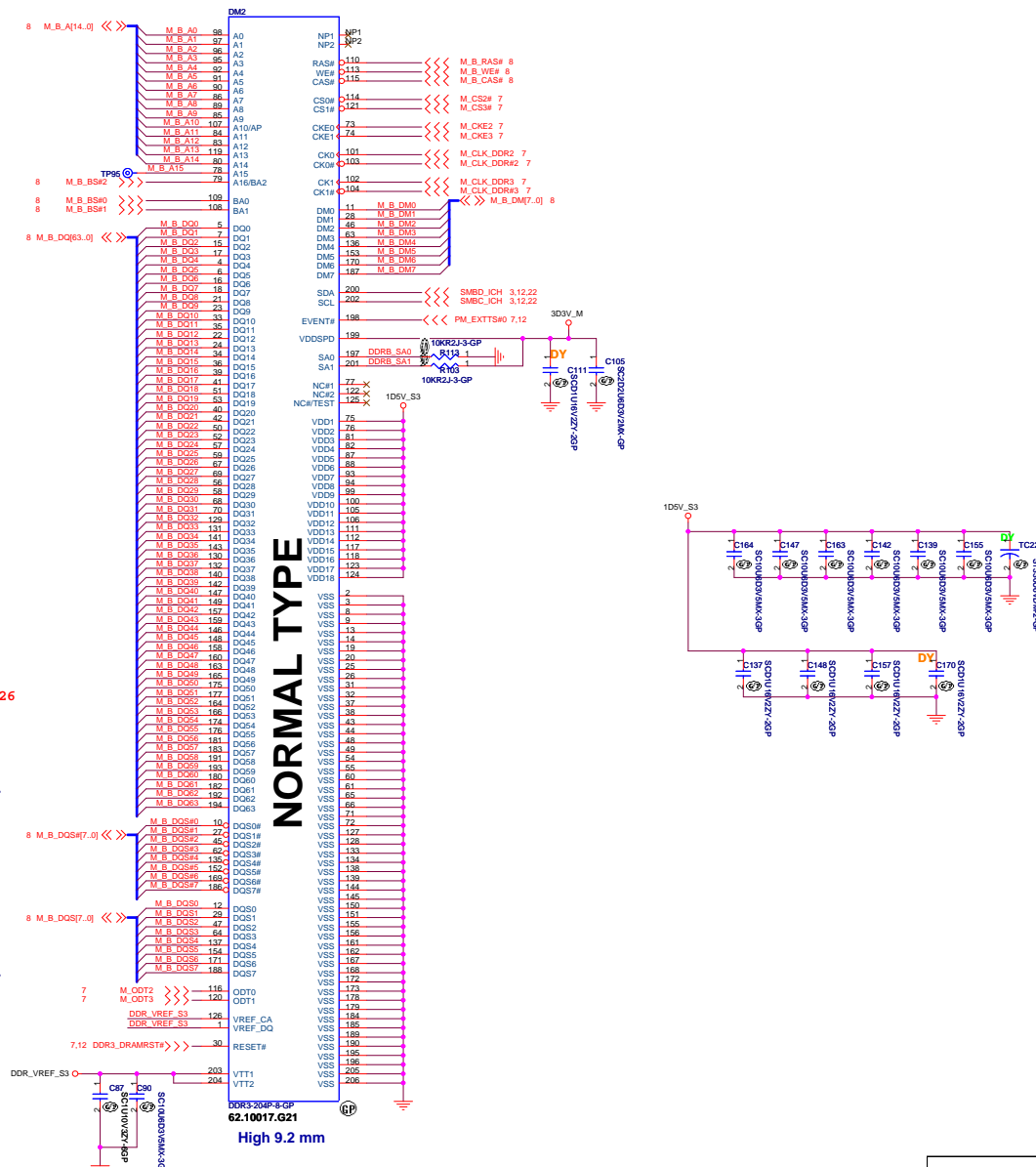


DDR3 SOCKET_1

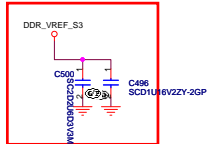


High 5.2mm

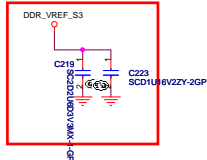
DDR3 SOCKET_2



Layout Note : Near Pin 126



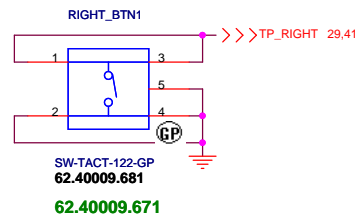
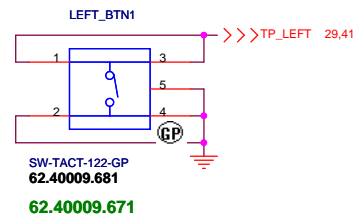
Layout Note : Near Pin 1



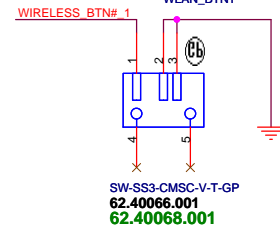
緯創資通 **Wistron Corporation**
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Title			
DDR3 Termination Resistor			
Size	Document Number		Rev
	Four Peaks		-1M
Date: Friday, November 21, 2008	Sheet 13	of	57

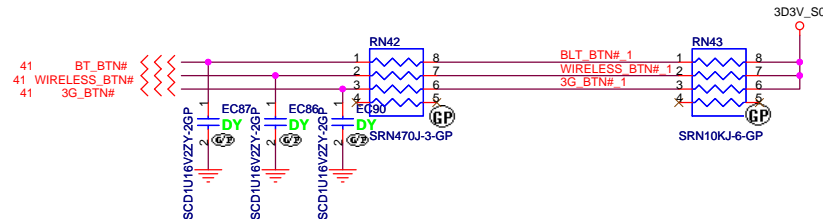
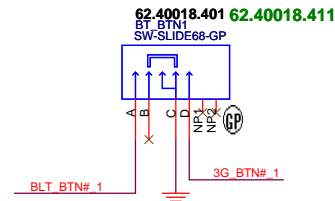
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BlueTooth ON/OFF



Wireless ON/OFF
Check Wireless Button left or right



Four Peaks

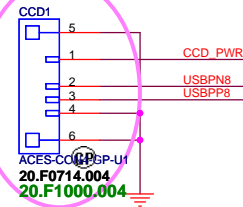
緯創資通 Wistron Corporation
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Title			
SWITCH / Button			
Size	Document Number		Rev
	Four Peaks		-1M
Date:	Friday, November 21, 2008	Sheet 14 of	57

LCD/INVERTER/CCD CONN

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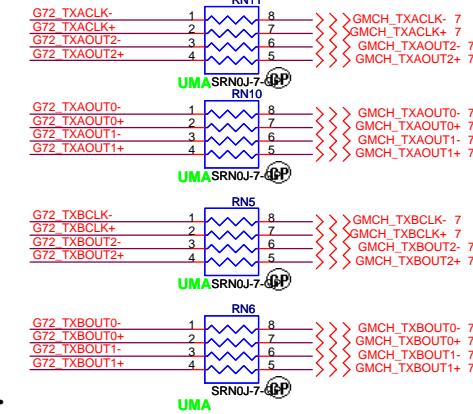
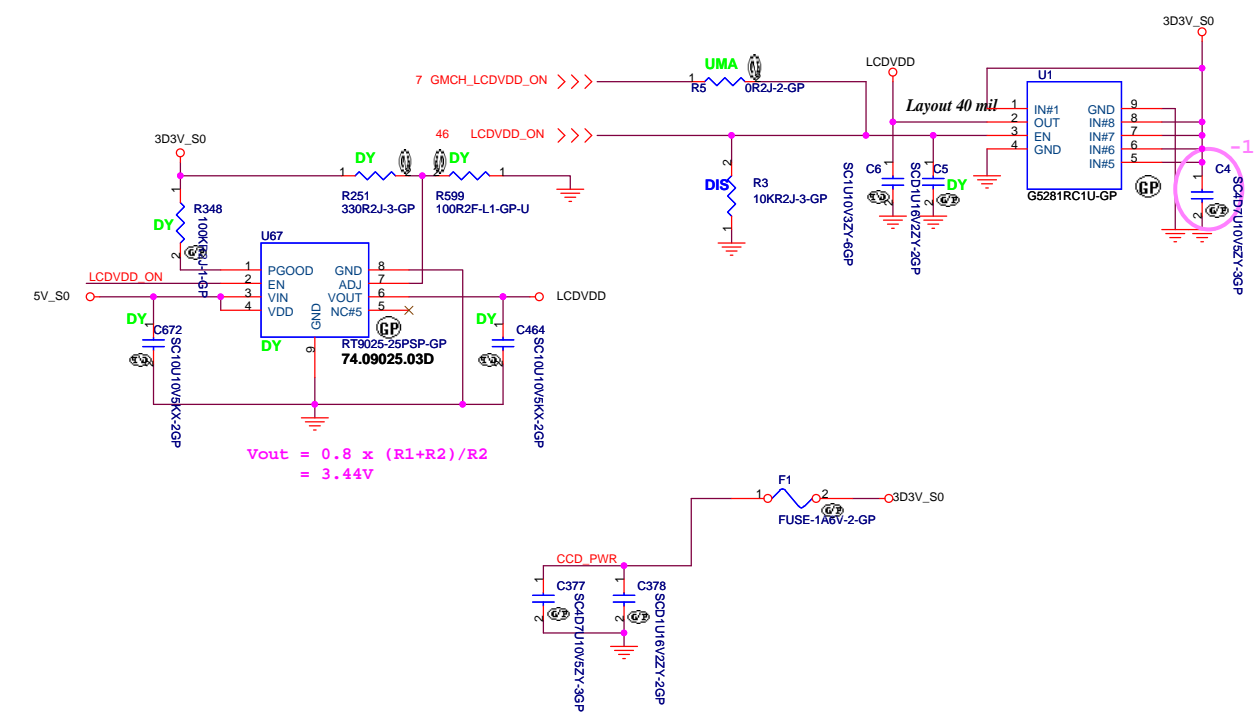
-1
04/23



CCD1 Conn. Test Point

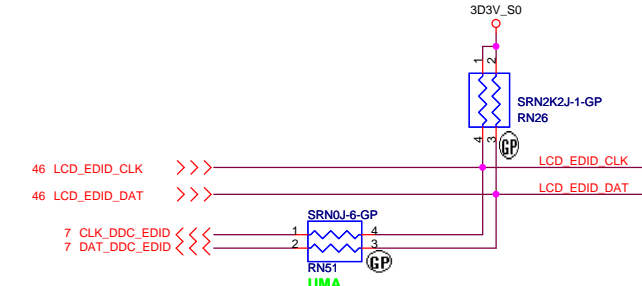


-1M(5/27)



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	GND
2	GND
3	5V
4	USB-
5	USB+



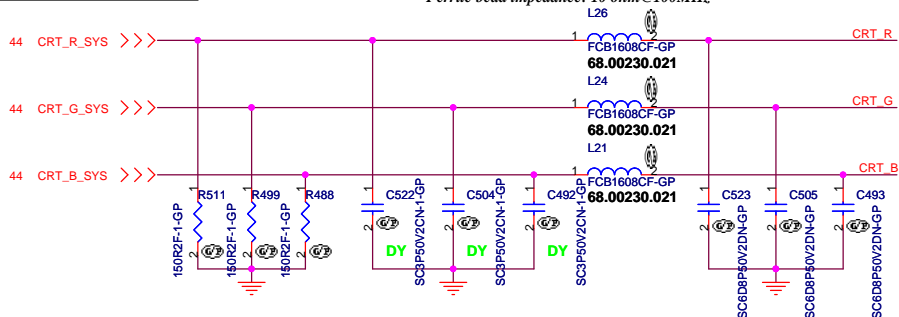
Four Peaks

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Title LCD CONN	
Size	Document Number
Four Peaks	
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Layout Note:
Place these resistors
close to the CRT-out
connector

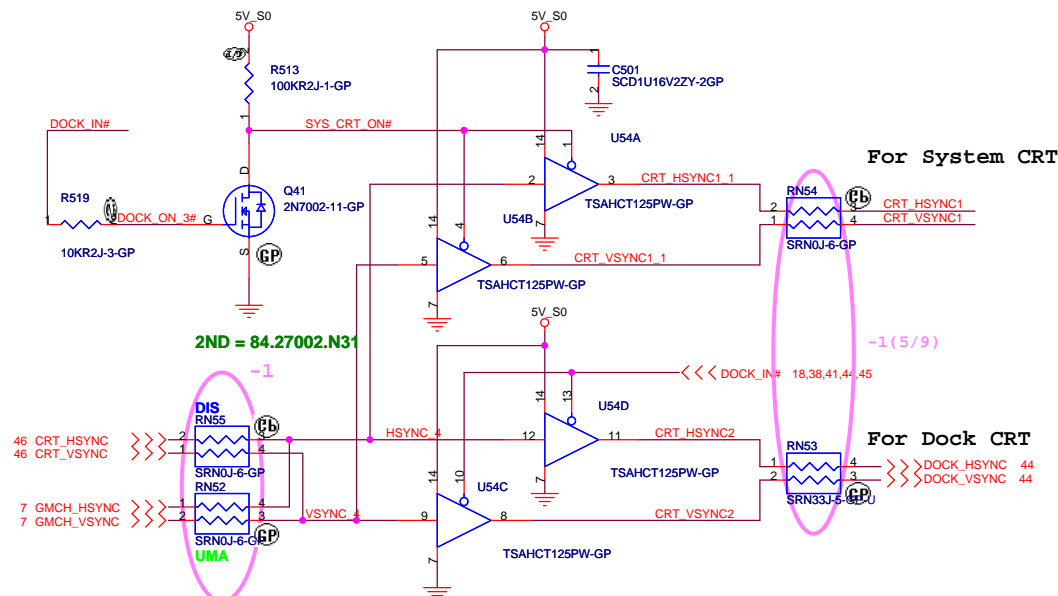
Ferrite bead impedance: 10 ohm@100MHz.



Layout Note:

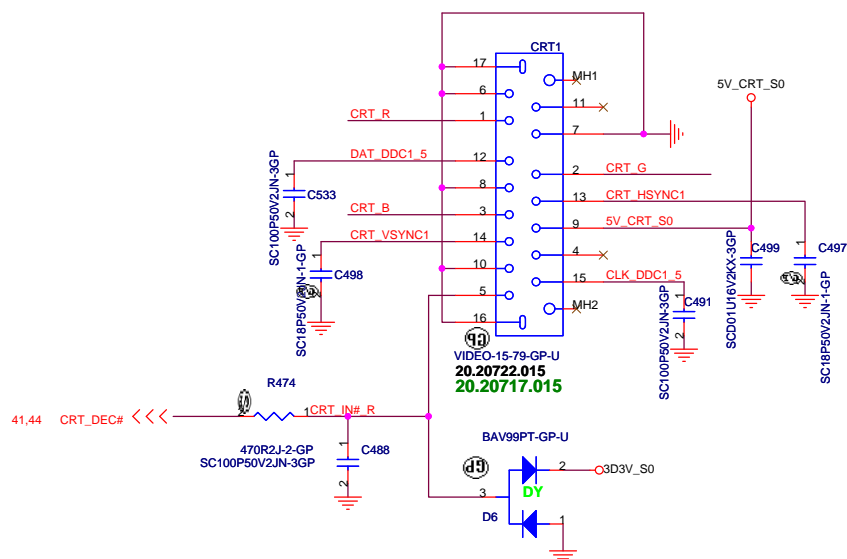
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

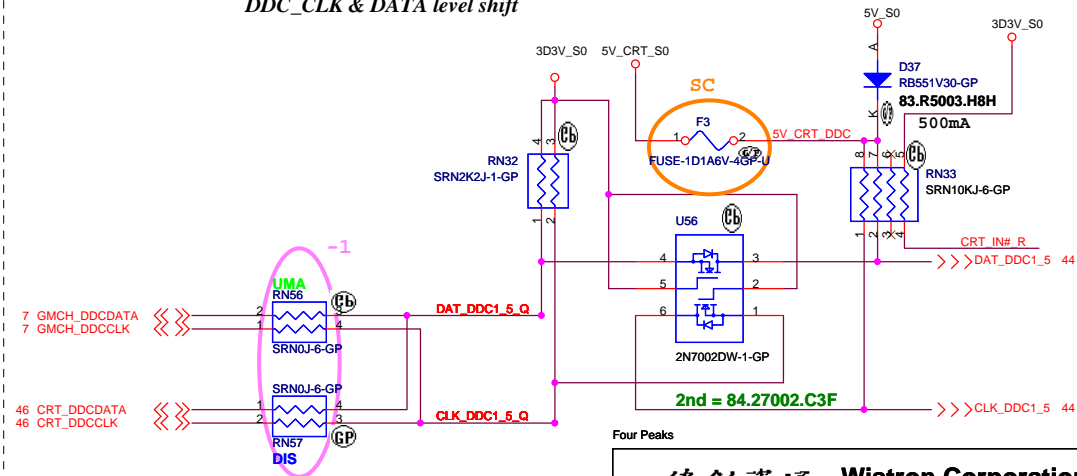


Function	DOCK_CRT_SEL#
SYSTEM	H
DOCK	L

CRT I/F & CONNECTOR

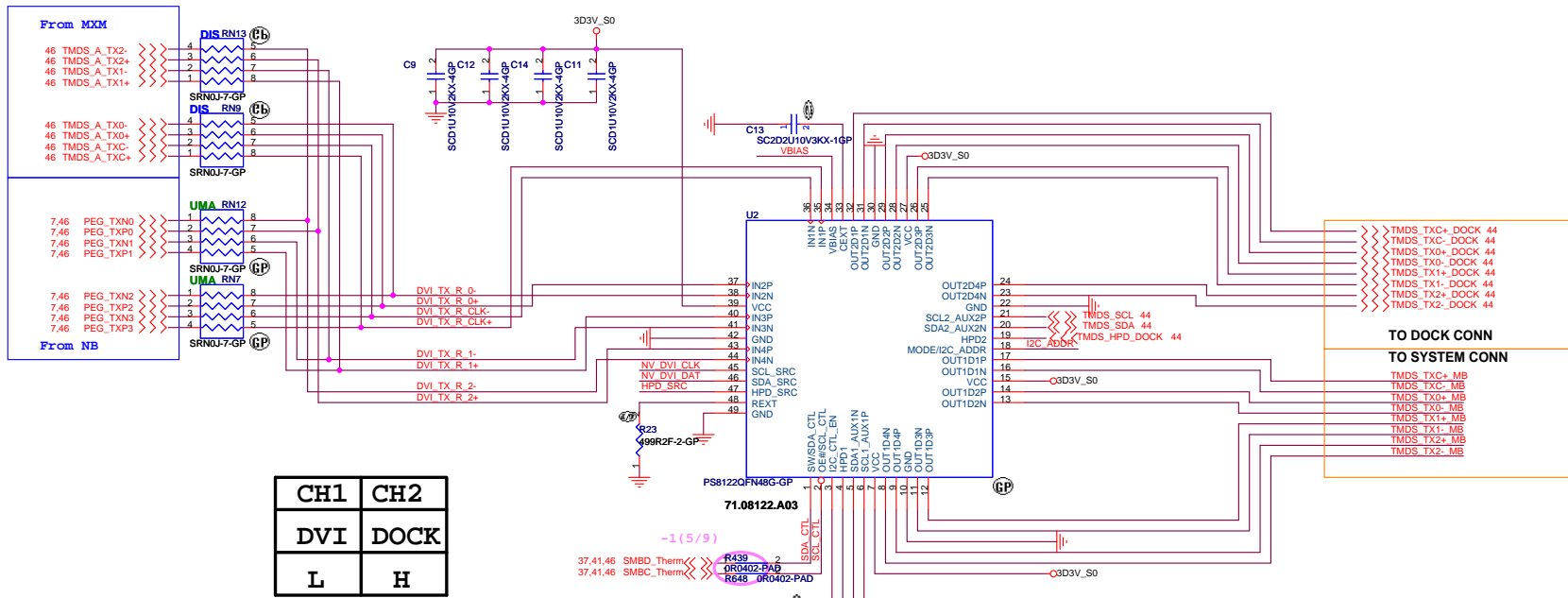
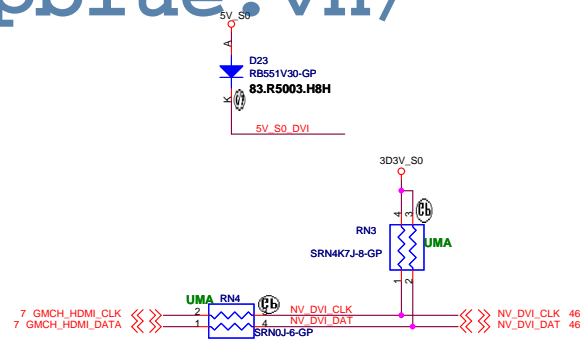
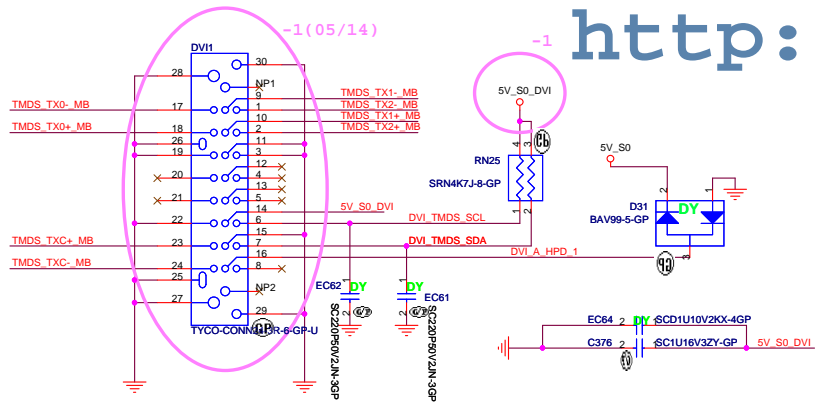


DDC_CLK & DATA level shift

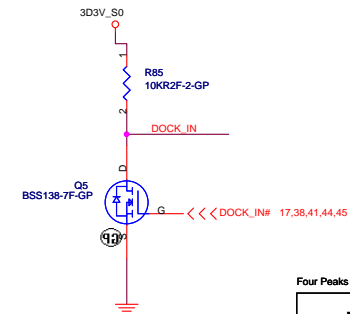
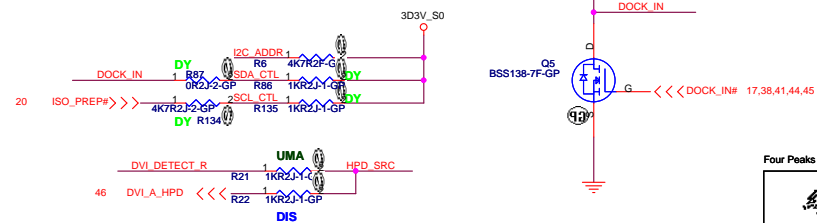
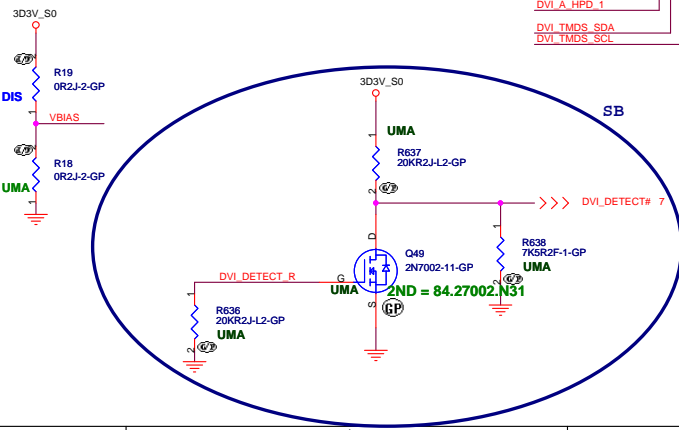


Four Peaks

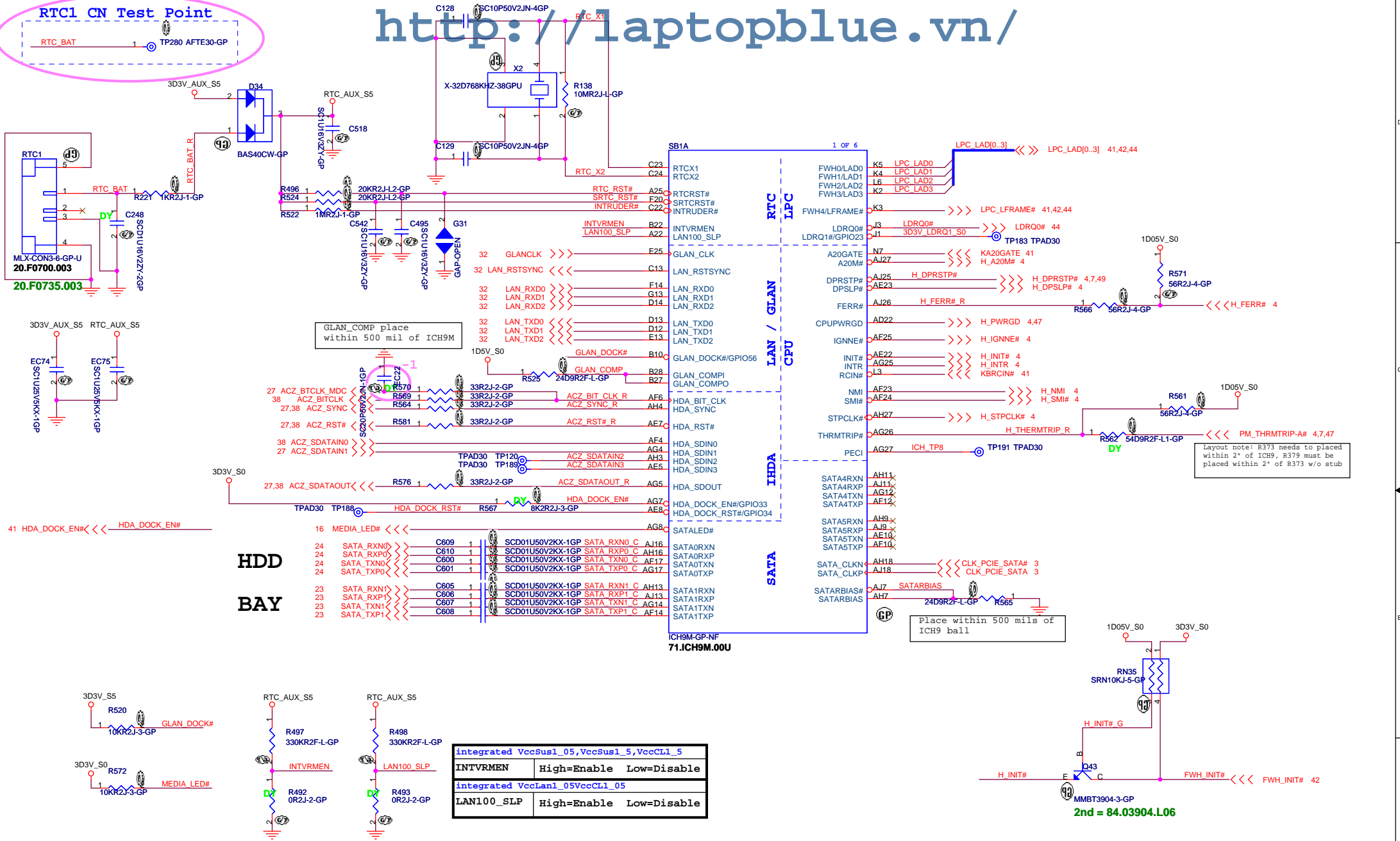
<http://laptopblue.vn/>



CH1	CH2
DVI	DOCK
L	H



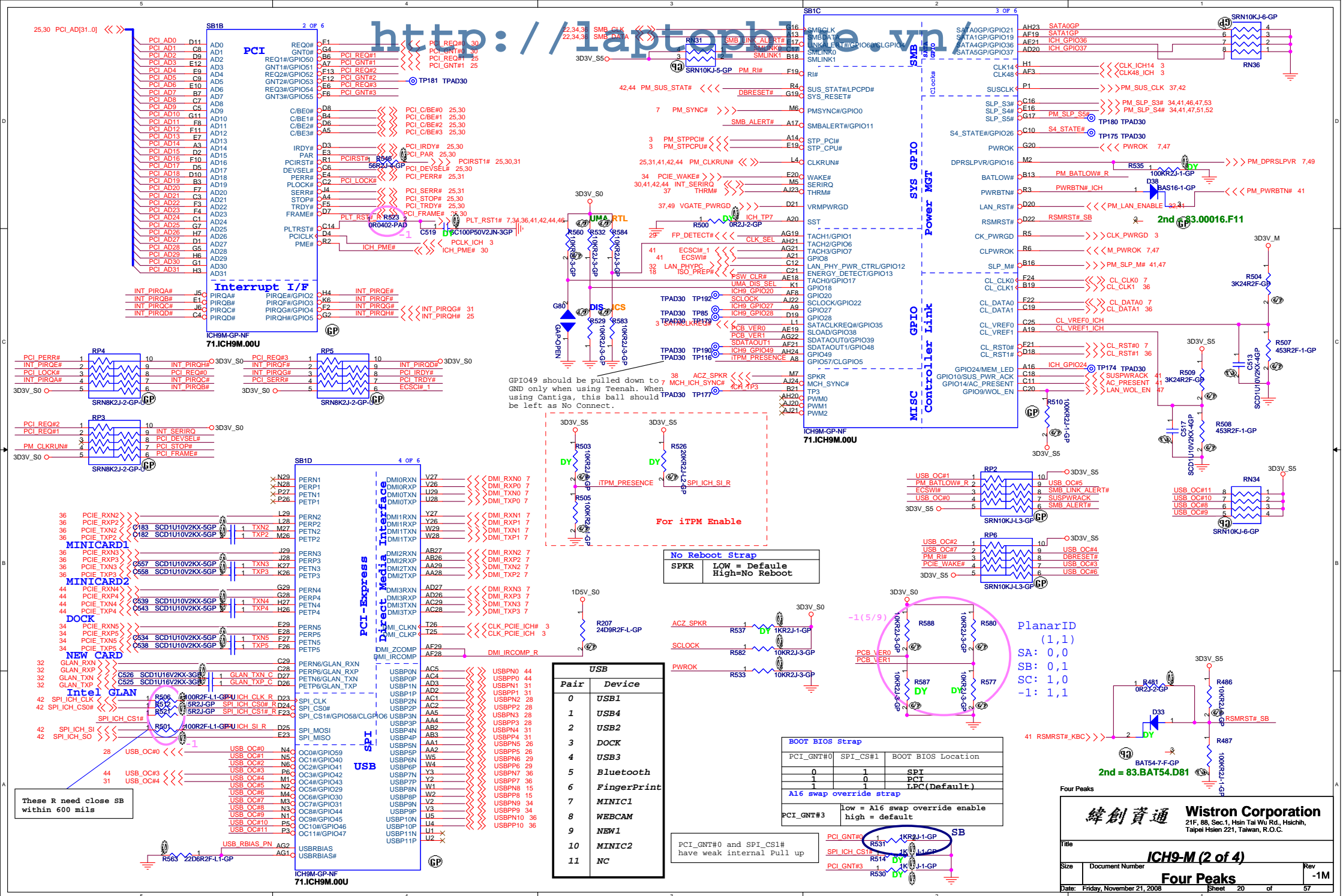
RTC1 CN Test Point

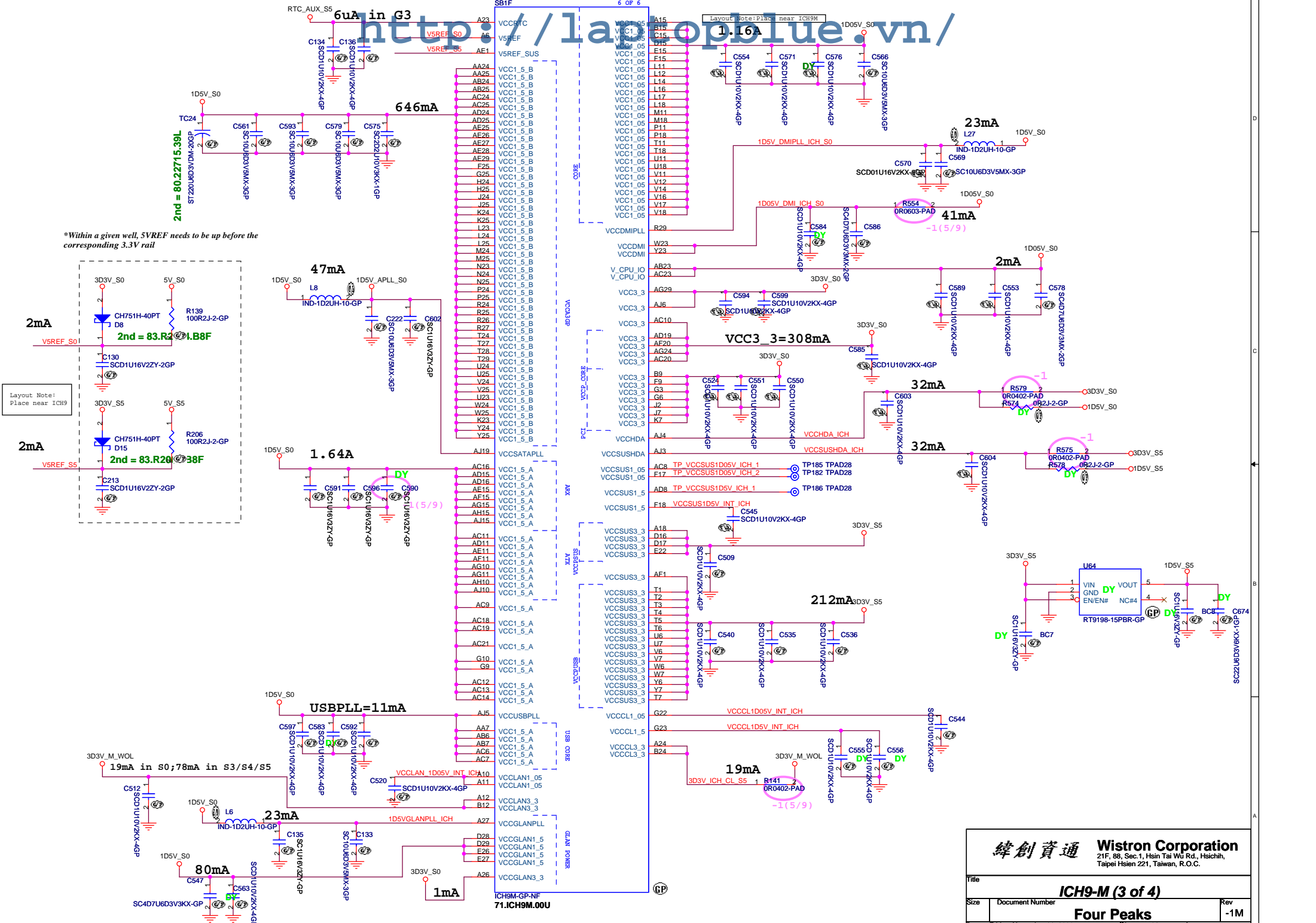


Four Peaks

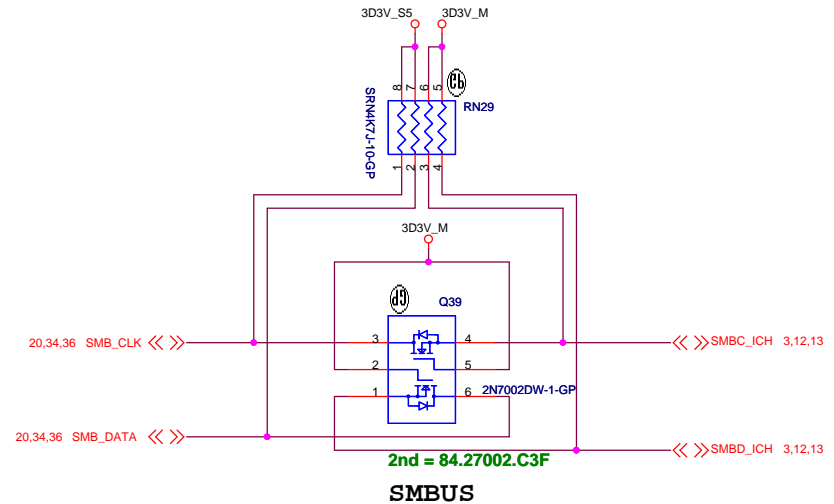
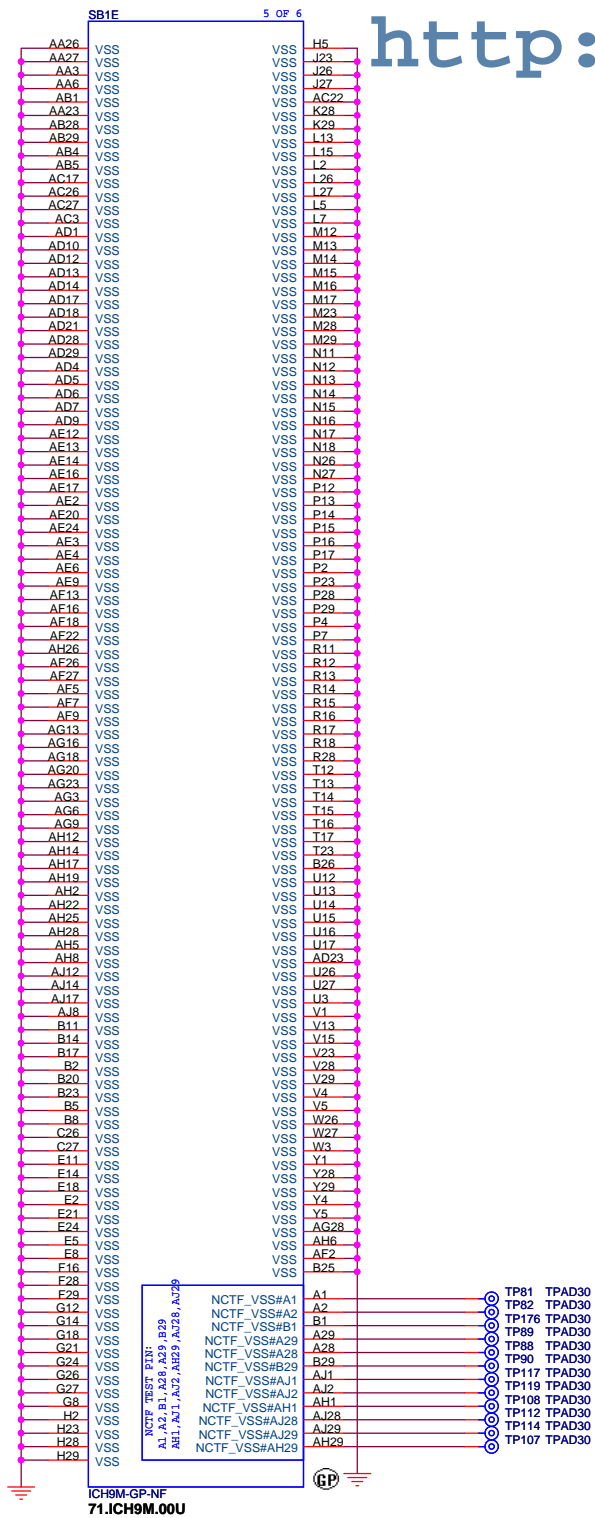
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ICH9-M (1 of 4)
Size Document Number
Date: Friday, November 21, 2008 Sheet 19 of 57
Rev -1M
Four Peaks





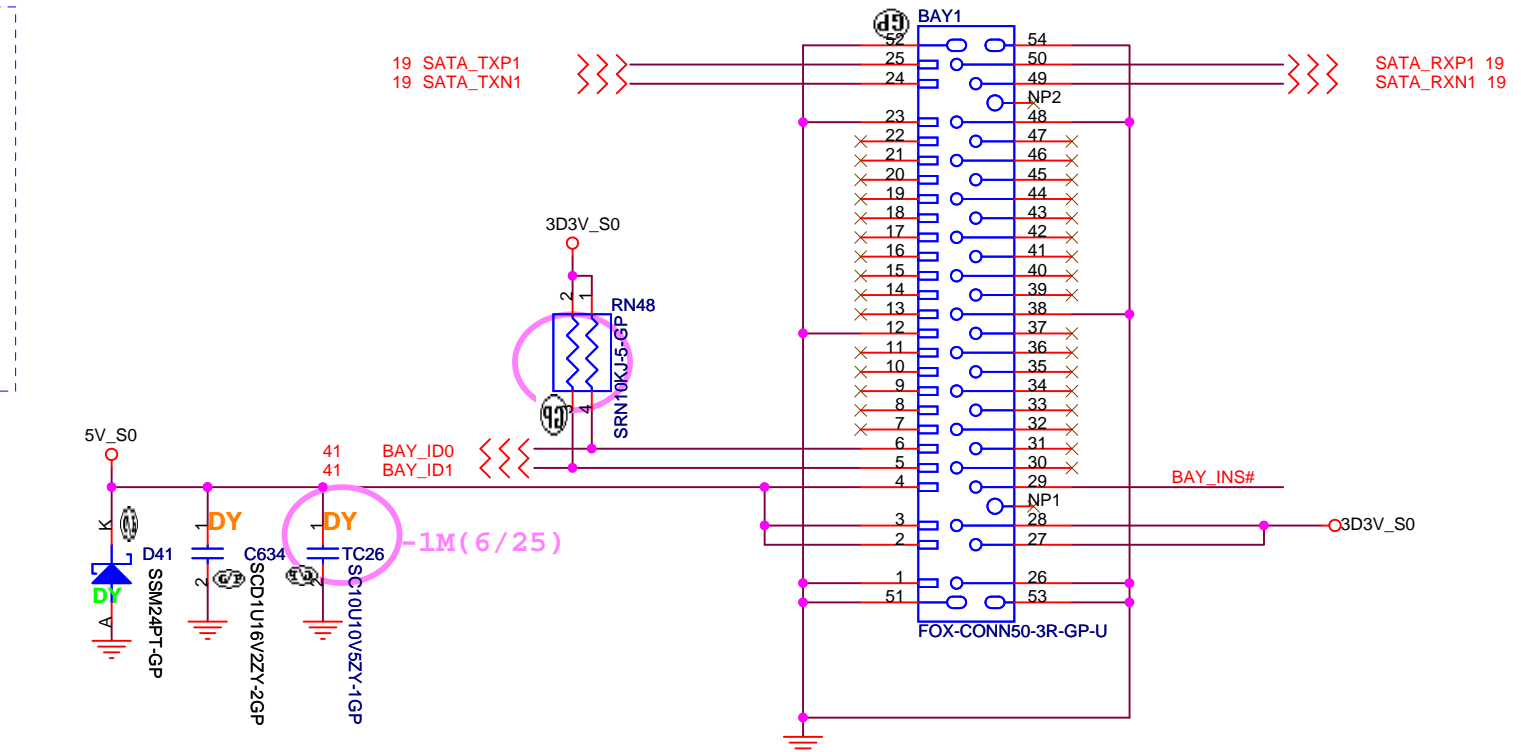
<http://laptopblue.vn/>



ODD Connector


ODD Conn. Test Point

SATA_TXP1	TP125 TPAD30
SATA_TXN1	TP124 TPAD30
SATA_RXP1	TP127 TPAD30
SATA_RXN1	TP126 TPAD30
BAY_ID0	TP194 TPAD30
BAY_ID1	TP195 TPAD30
BAY_INS#	TP193 TPAD30
3D3V_S0	TP277 TPAD30
5V_S0	TP278 TPAD30

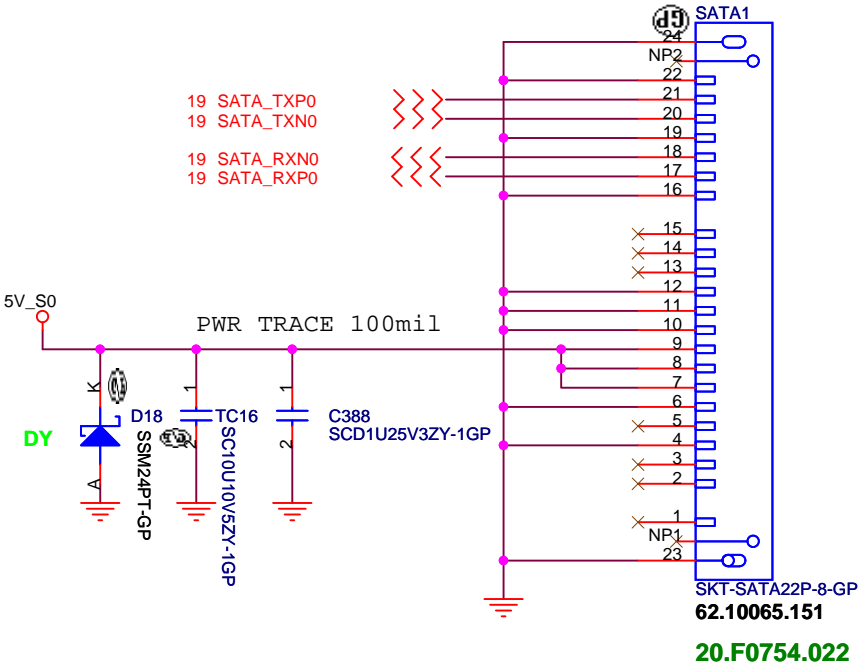


	BAY_ID0	BAY_ID1
SATA ODD	0	0
SATA HDD	1	1

Four Peaks

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ODD	
Size	Document Number
Four Peaks	
Date: Friday, November 21, 2008	Rev -1M
Sheet 23	of 57


SATA Connector

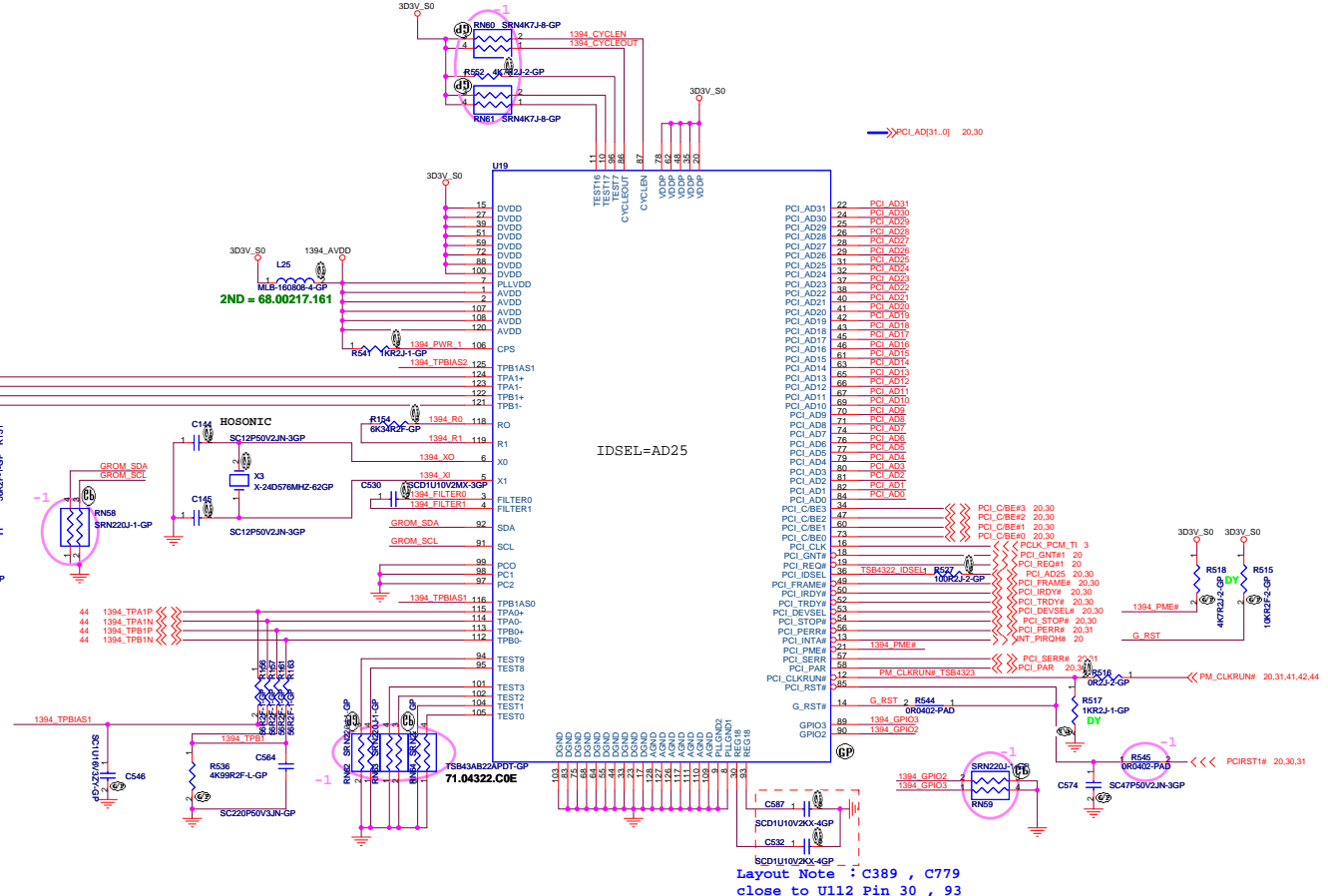
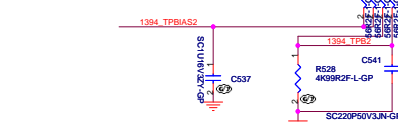
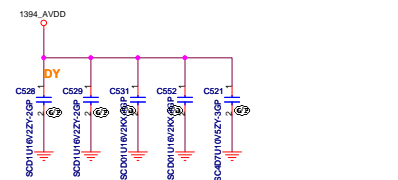


HDD Conn. Test Point

SATA_TXP0	TP132 TPAD30
SATA_TXN0	TP131 TPAD30
SATA_RXN0	TP130 TPAD30
SATA_RXP0	TP128 TPAD30
5V_S0	TP99 TPAD30

Four Peaks

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD CONN			
Size	Document Number		Rev
	Four Peaks		-1M
Date:	Friday, November 21, 2008	Sheet 24 of	57



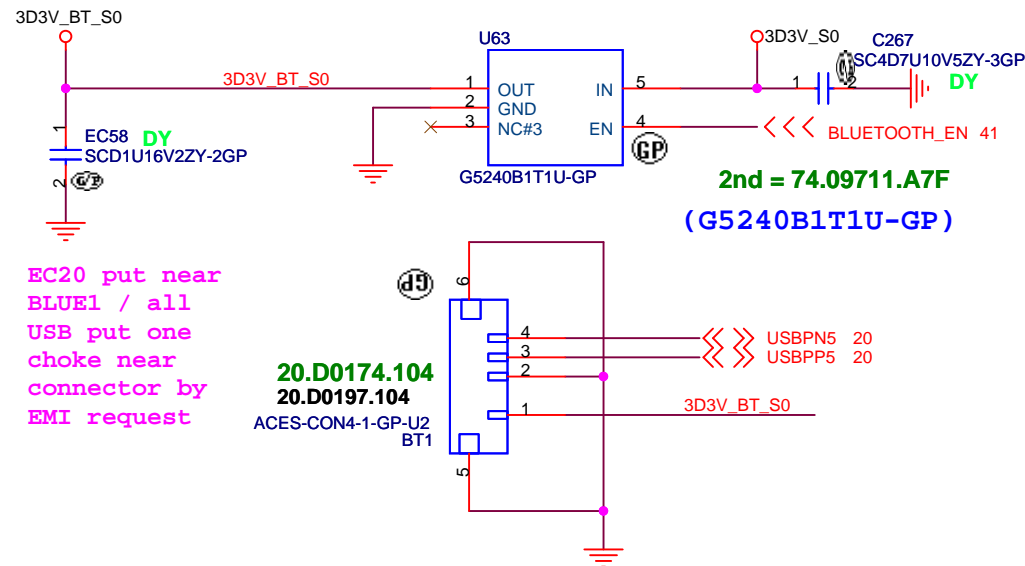
Layout Note : C389 , C779
close to U112 Pin 30 , 93

BLUETOOTH MODULE

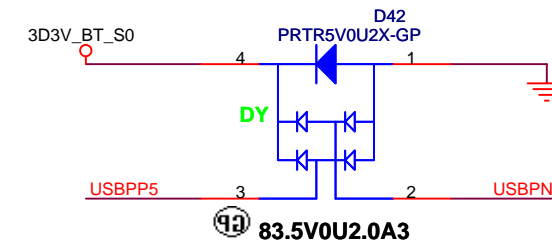
BT Conn. Test Point

USBPN5	1	TP207 AFTE30-GP
USBPP5	1	TP205 AFTE30-GP
3D3V_BT_S0	1	TP136 AFTE30-GP

-1M(5/27)



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



Need check conn.

Four Peaks

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

Rev

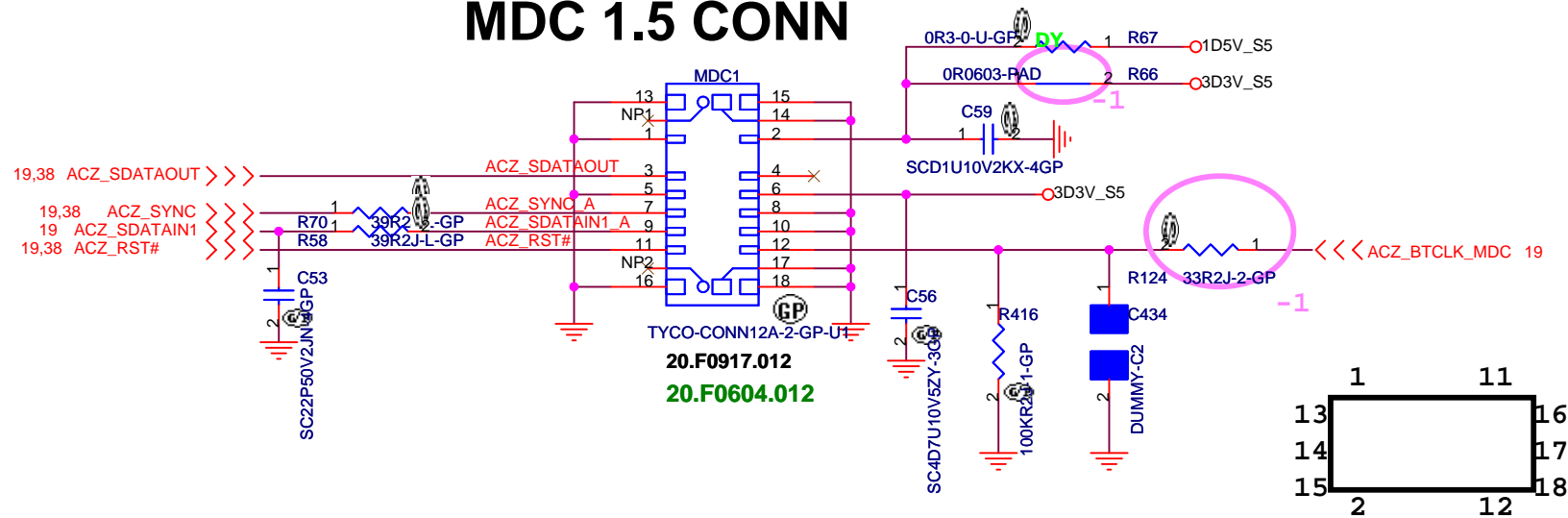
Four Peaks

-1M

Date: Friday, November 21, 2008

Sheet 26 of 57

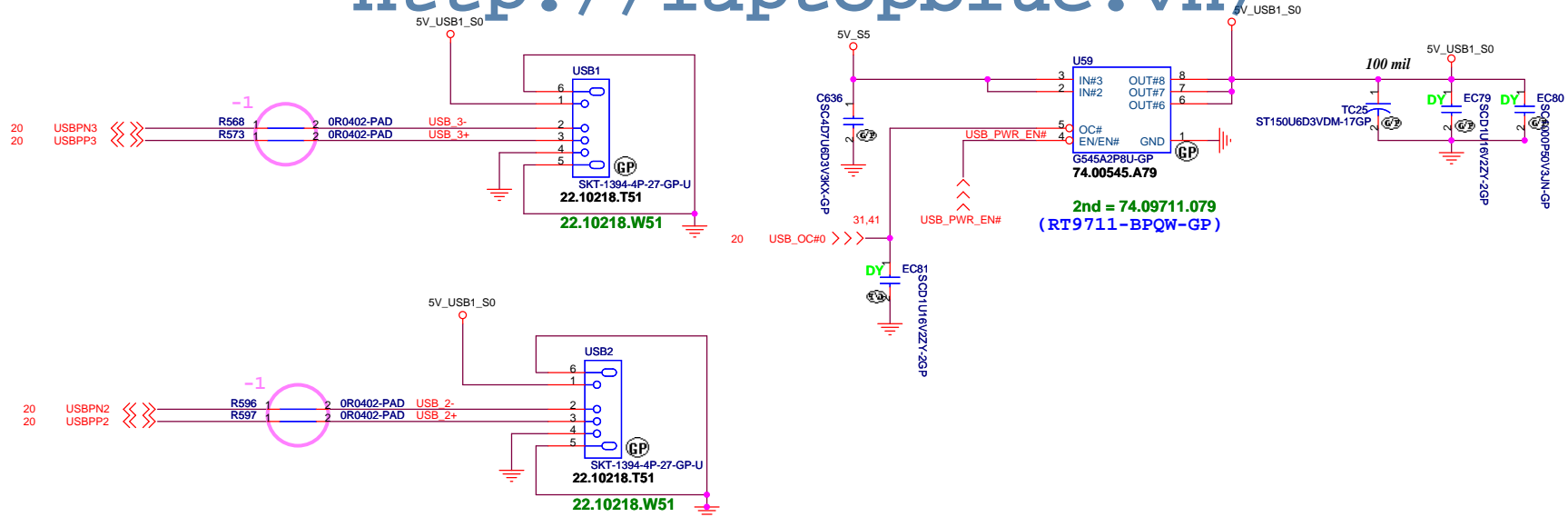
MDC 1.5 CONN



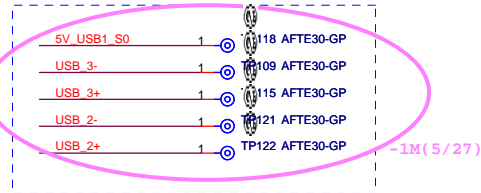
Four Peaks

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
<div>MDC</div>	
Size	Document Number
	<div>Four Peaks</div> <div>-1M</div>
Date:	Friday, November 21, 2008
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USB Conn. Test Point



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Title	<i>USB</i>
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Size	Document Number
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Four Peaks

Rev	
-1M	

Date: Friday, November 21, 2008

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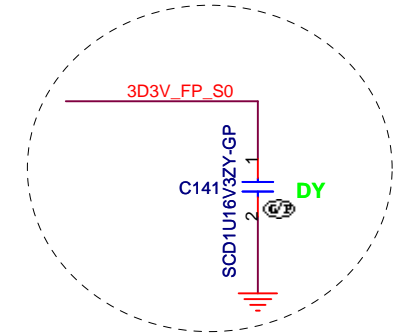
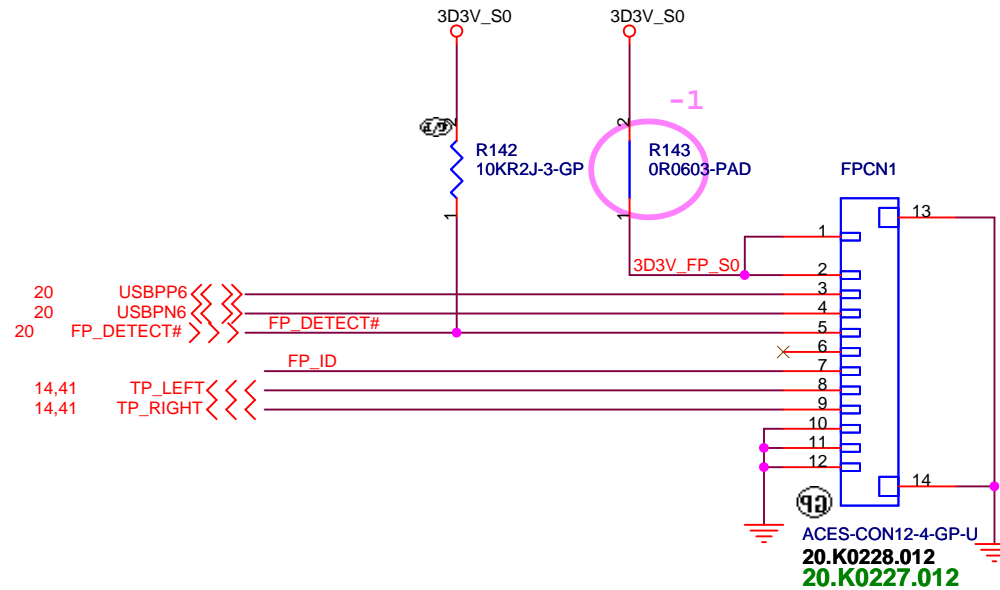
57

http://laptopblue.vn/ Finger printer

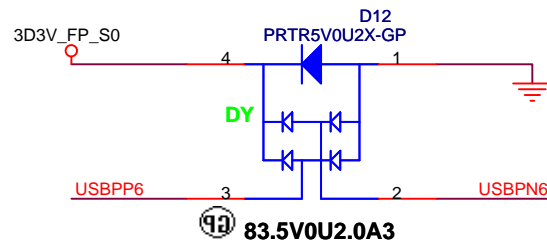
FP Conn. Test Point

3D3V_FP_S0	1	TP01	AFTE30-GP
USBPP6	1	TP00	AFTE30-GP
USBPN6	1	TP91	AFTE30-GP
FP_DETECT#	1	TP93	AFTE30-GP
FP_ID	1	TP84	AFTE30-GP
TP_LEFT	1	TP83	AFTE30-GP
TP_RIGHT	1	TP87	AFTE30-GP

-1M(5/27)



For EMI



Four Peaks

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Title

Finger Printer

Size

Document Number

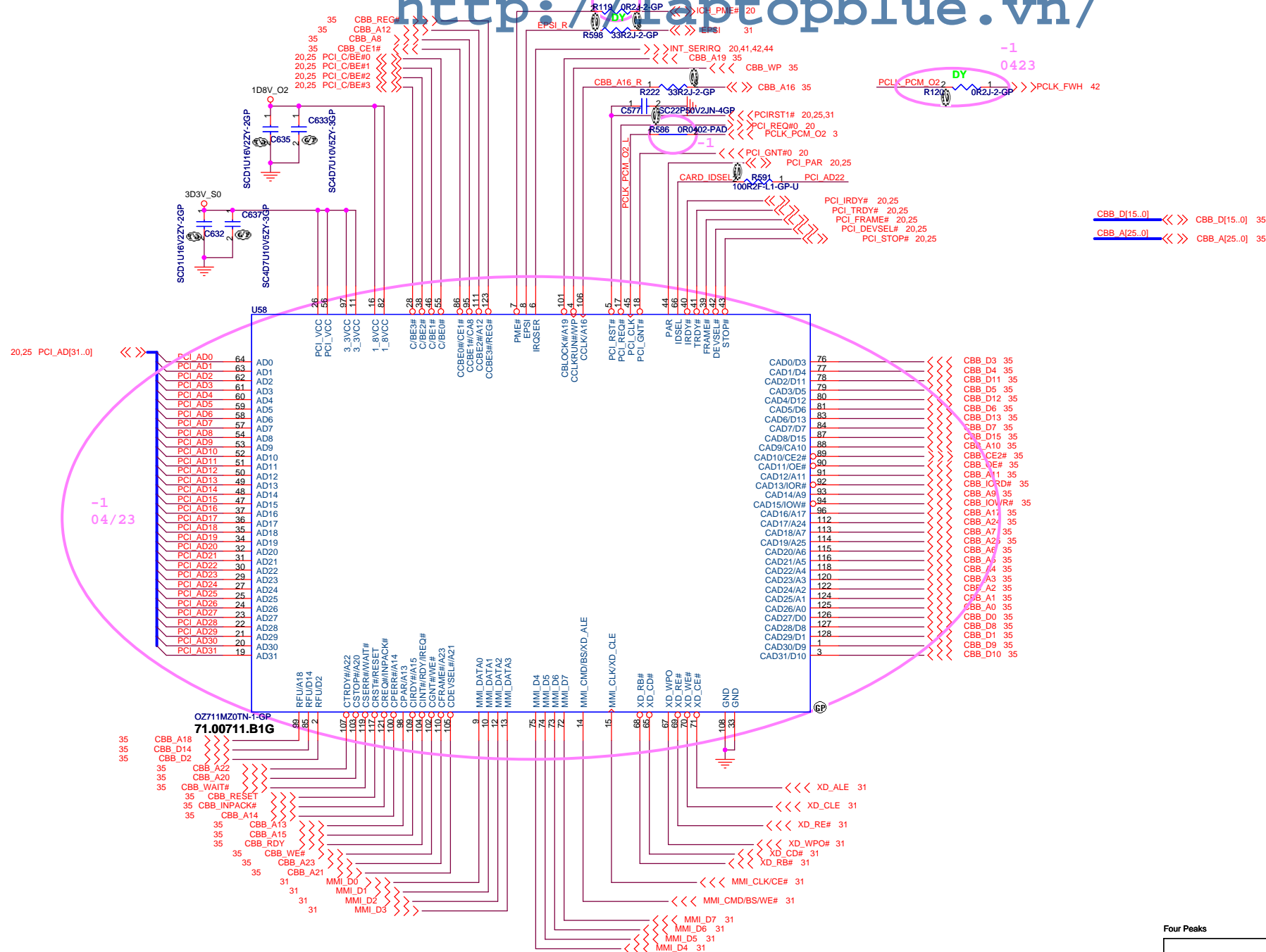
Rev

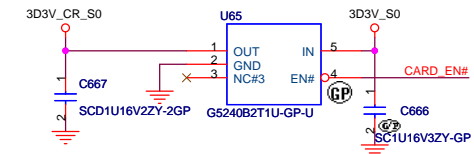
-1M

Four Peaks

Date: Friday, November 21, 2008

Sheet 29 of 57

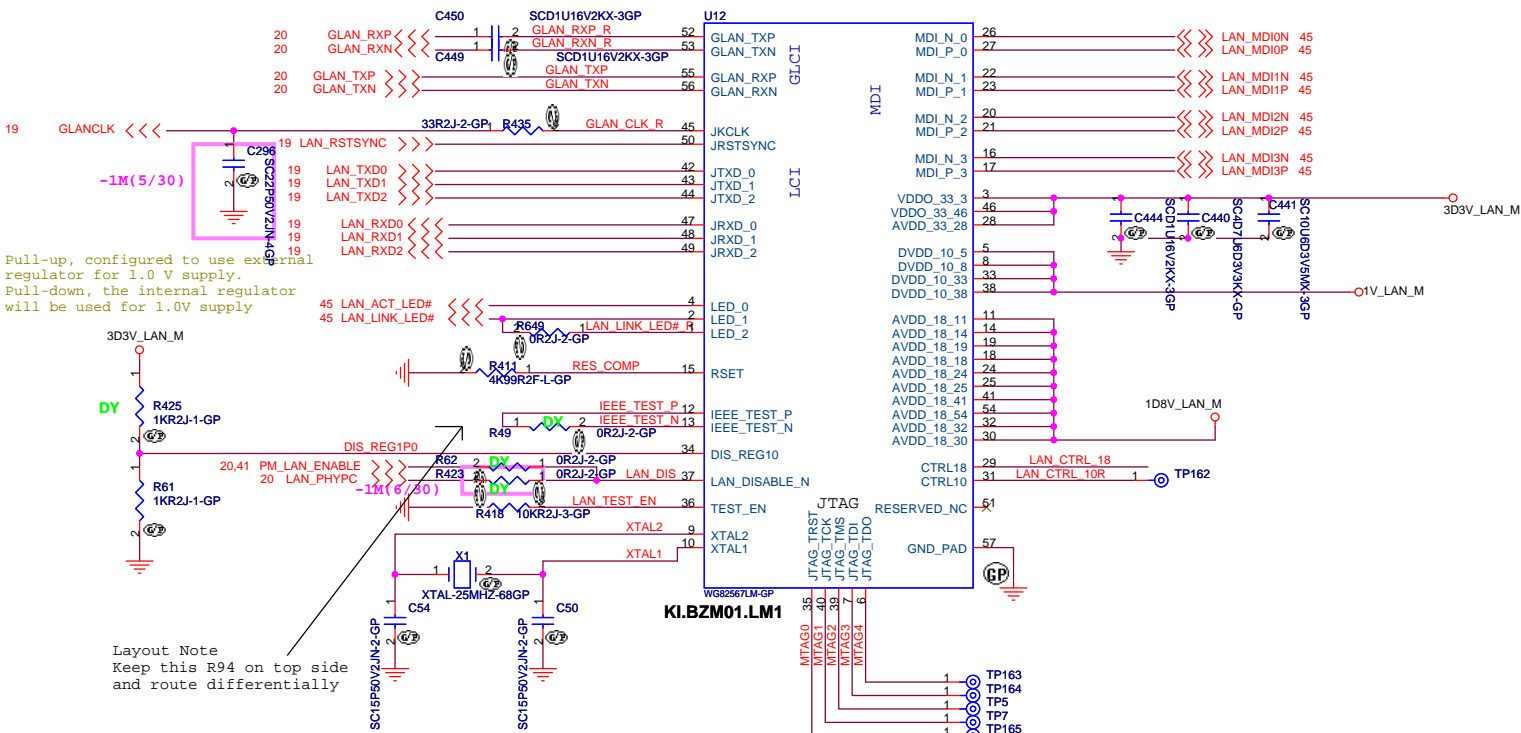
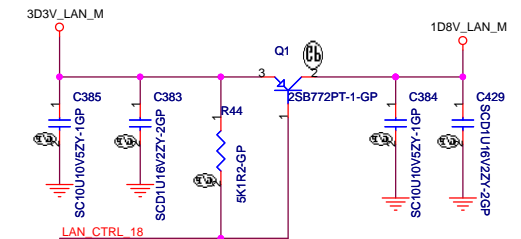
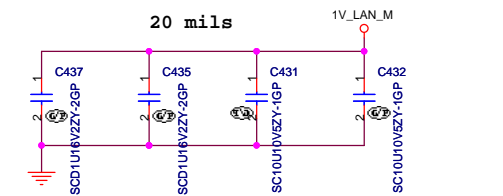
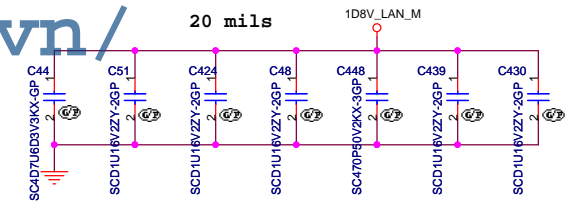
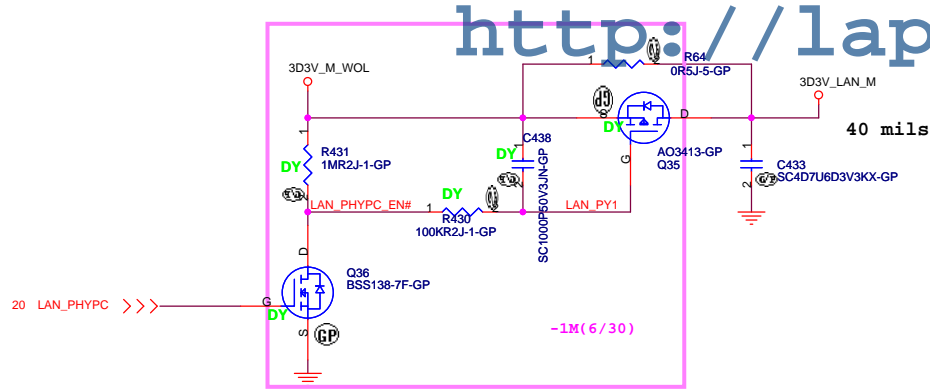




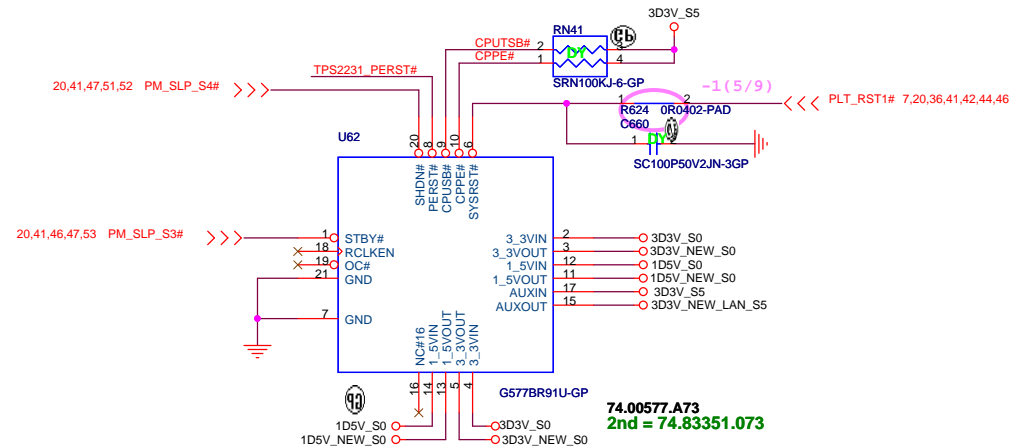
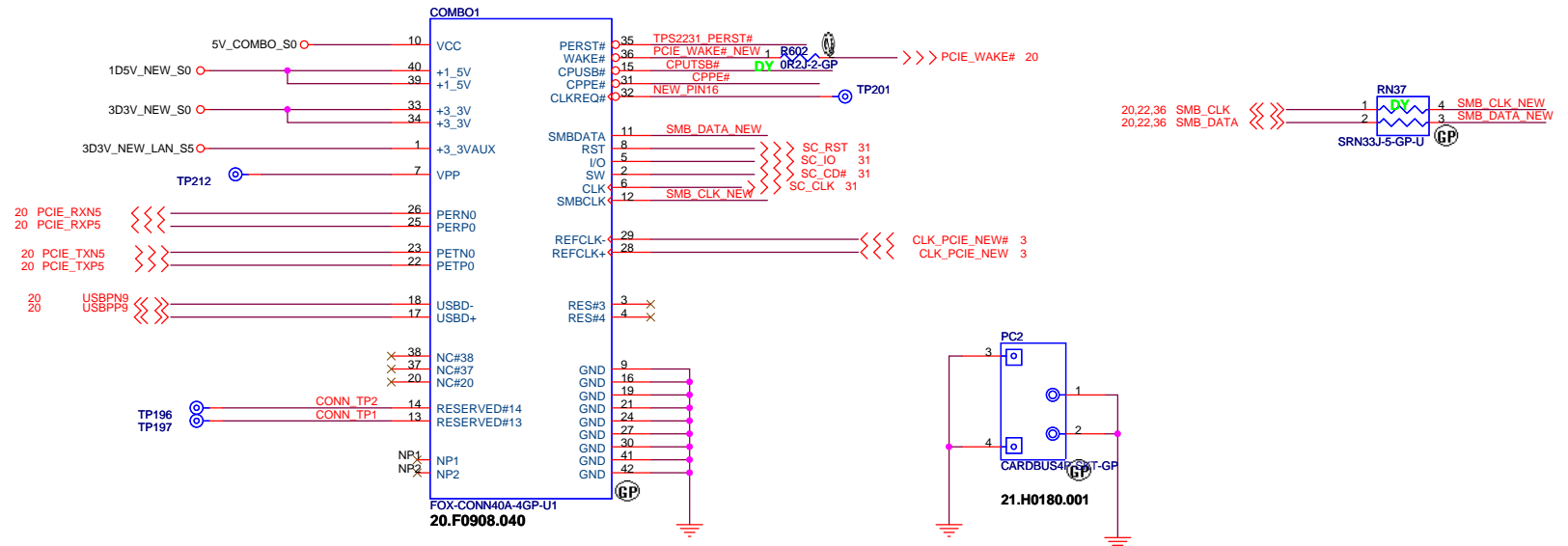
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Rev	
-1M	

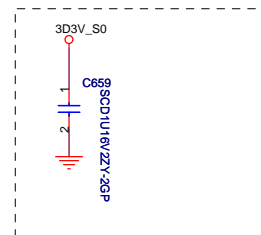
57



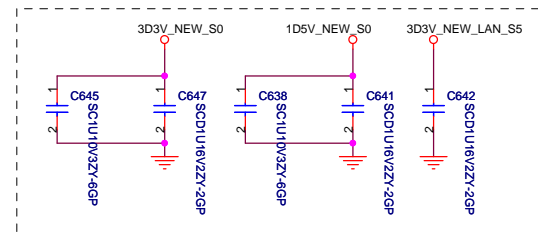
Layout Note
Keep this R94 on top side
and route differentially



Place them Near to Chip



Place them Near to Connector



Four Peaks

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: NEW CARD	
Size: Document Number	Rev: -1M
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http://laptopblue.vn/ PCMCIA Socket

Cardbus I/F

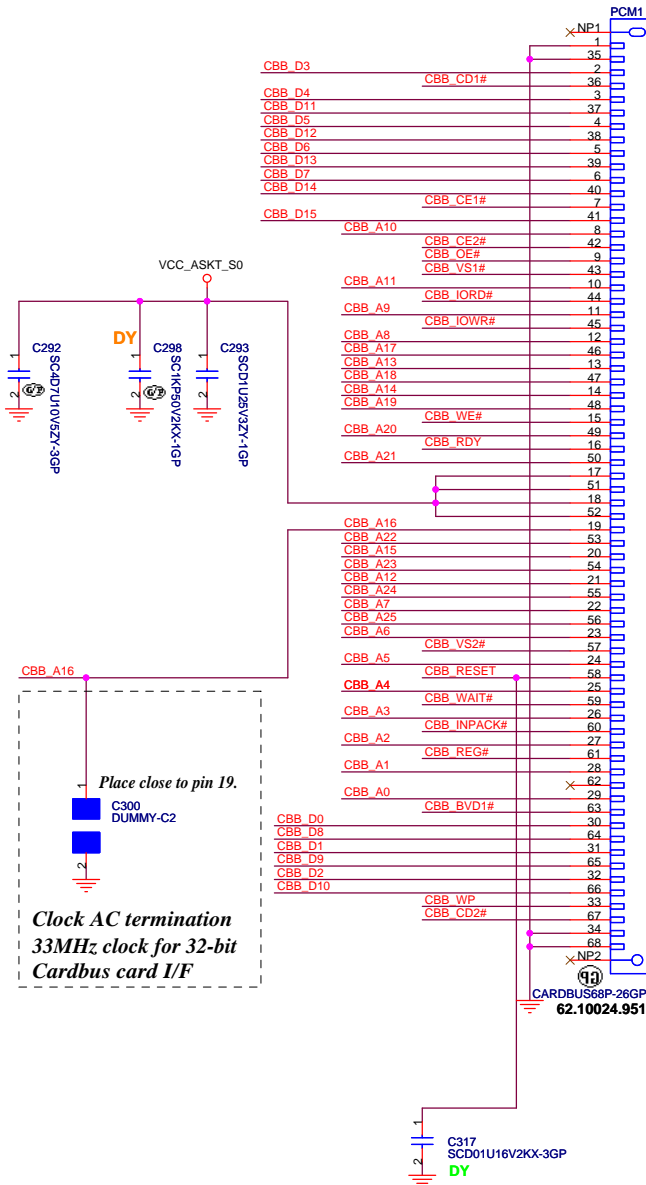
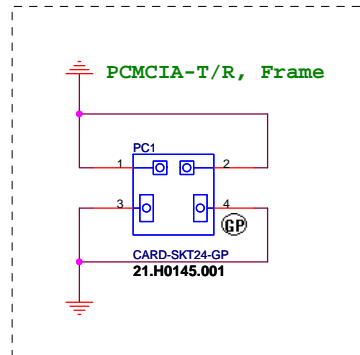
CBB_D[15..0] << CBB_D[15..0] 30

CBB_A[25..0] << CBB_A[25..0] 30

CBB_IORD# 30
CBB_IOWR# 30
CBB_OE# 30
CBB_WE# 30
CBB_REG# 30
CBB_RDY 30
CBB_WP 30
CBB_RESET# 30
CBB_WAIT# 30
CBB_INPACK# 30

CBB_CE1# 30
CBB_CE2# 30

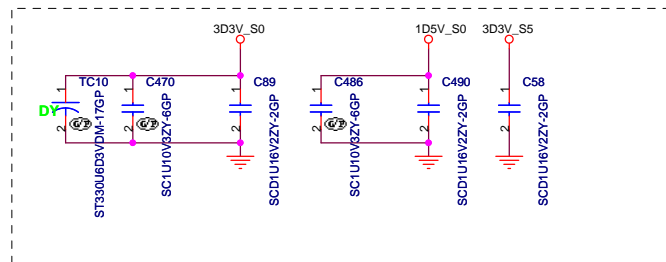
CBB_CD1# 31
CBB_CD2# 31
CBB_VS1# 31
CBB_VS2# 31
CBB_BVD1# 31



Four Peaks

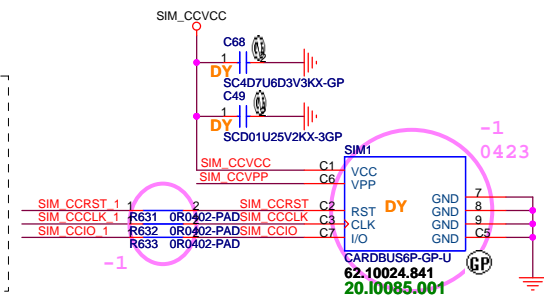
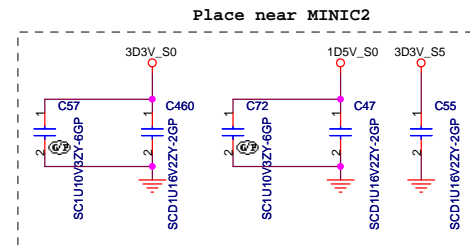
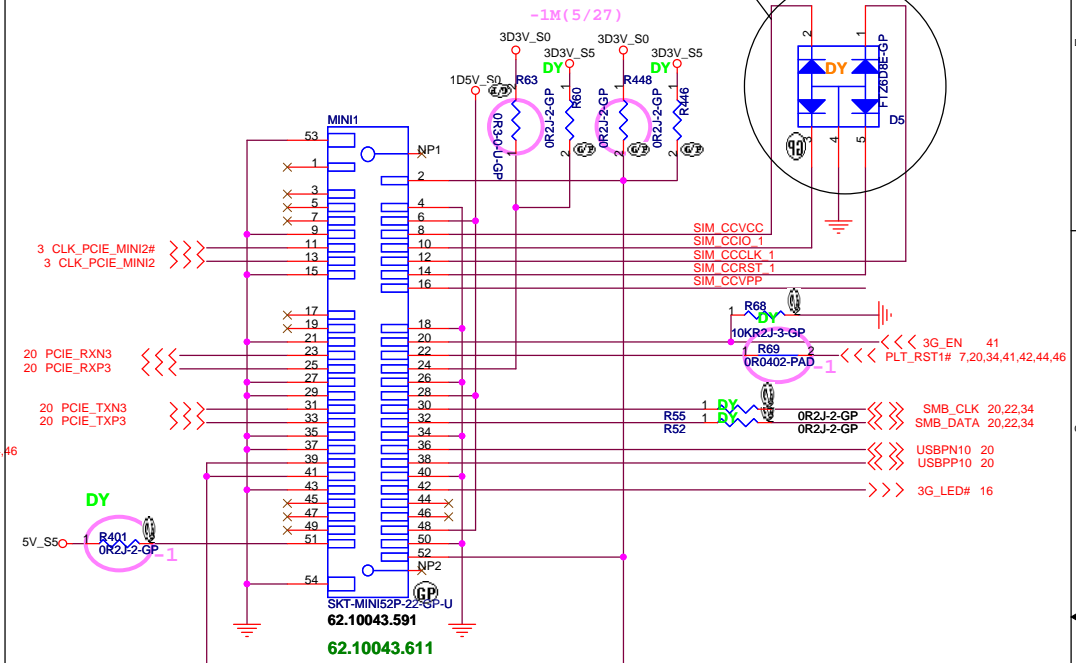
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			PCMCIA	
Size	Document Number	Four Peaks		Rev
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Mini Card Connector(Robson2 and 3G)
Support debug-card

Close to SKT1 (SIM socket).



Four Peaks

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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARDSize
A3

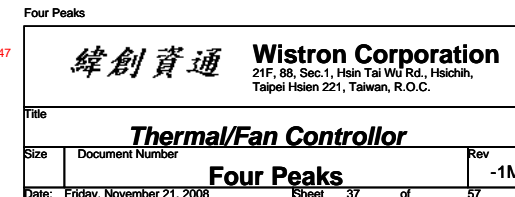
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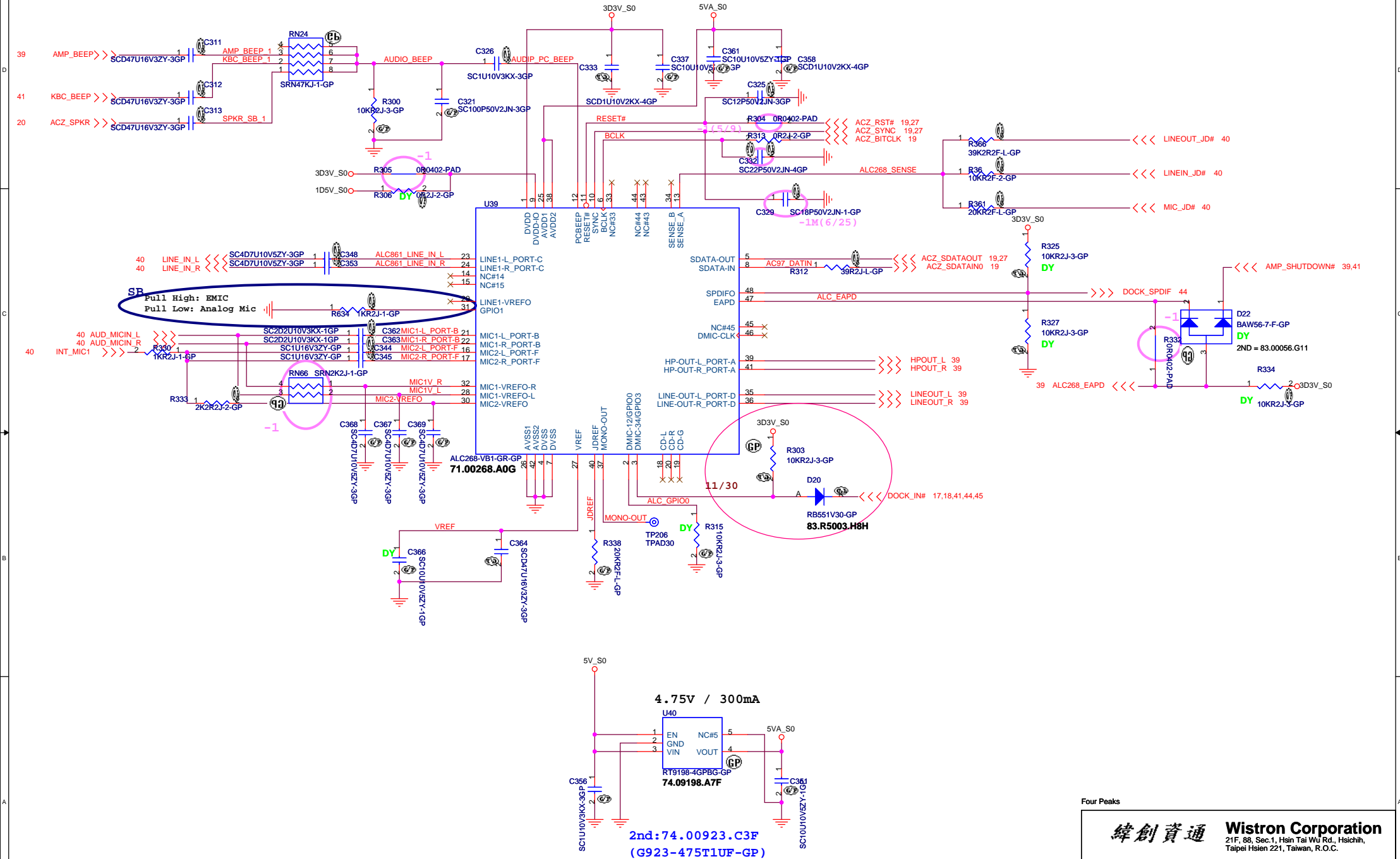
Four Peaks

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-1 M	

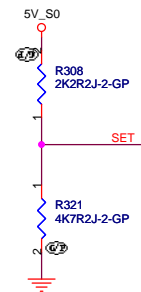
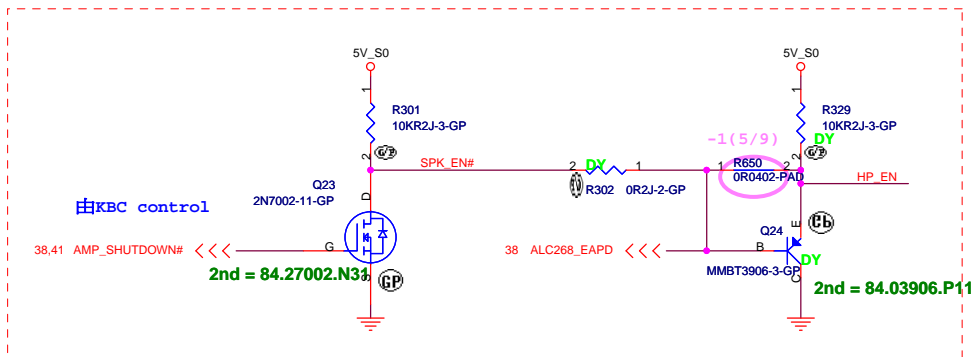
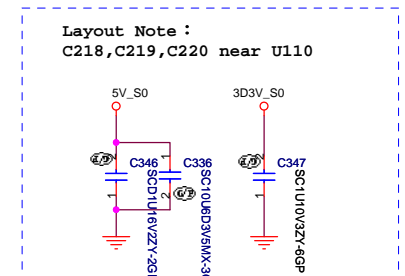
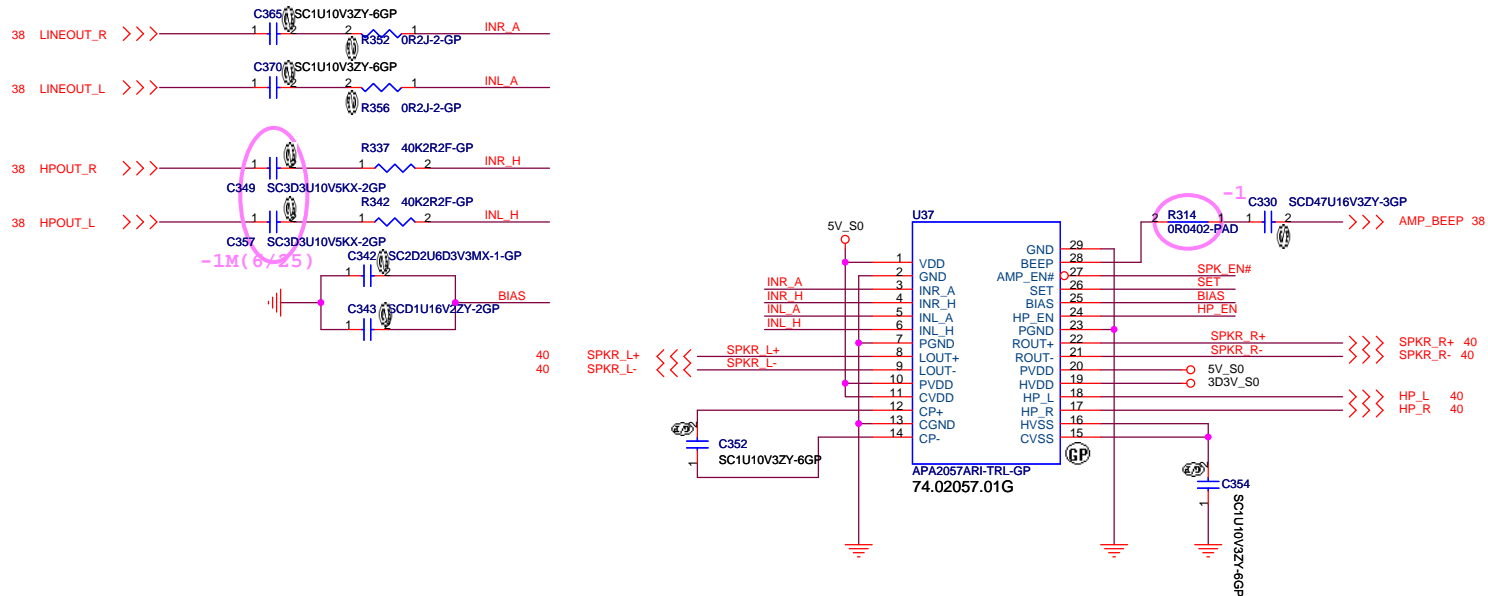




Four Peaks

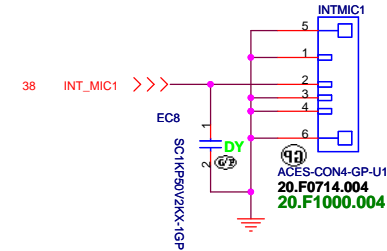
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Azalia codec ALC268		
Size	Document Number	Rev
A3	Four Peaks	-1M
Date: Friday, November 21, 2008		
Sheet	38	of 57



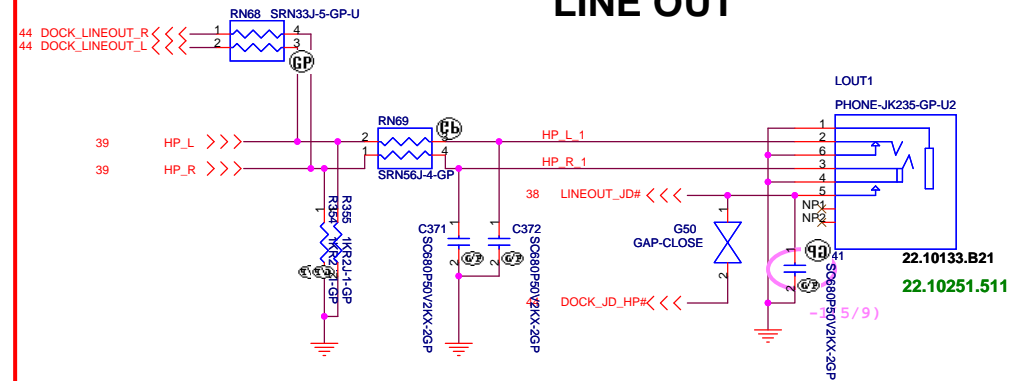
Four Peaks

INTMIC1 Conn. Test Point

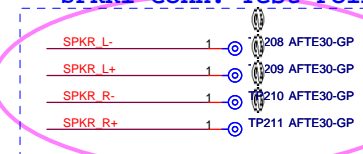


-1M(5/27)

LINE OUT



SPKR1 Conn. Test Point



-1M(5/27)

Four Peaks

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

AUDIO JACK

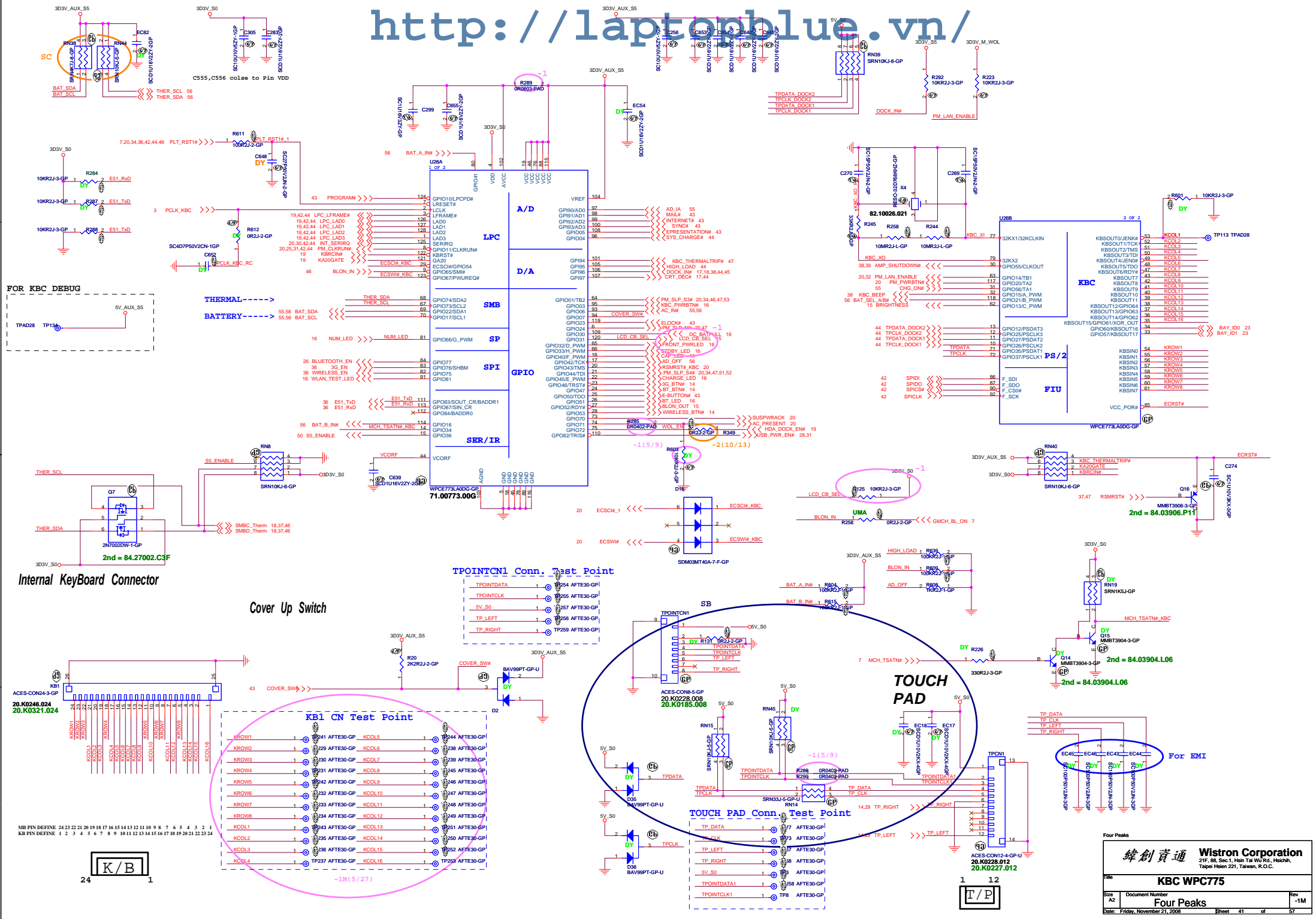
Size	Document Number
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Four Peaks

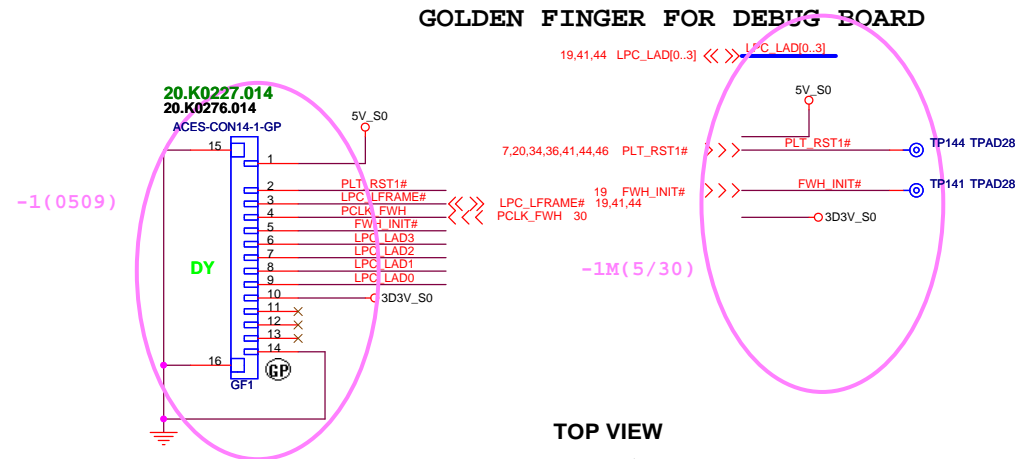
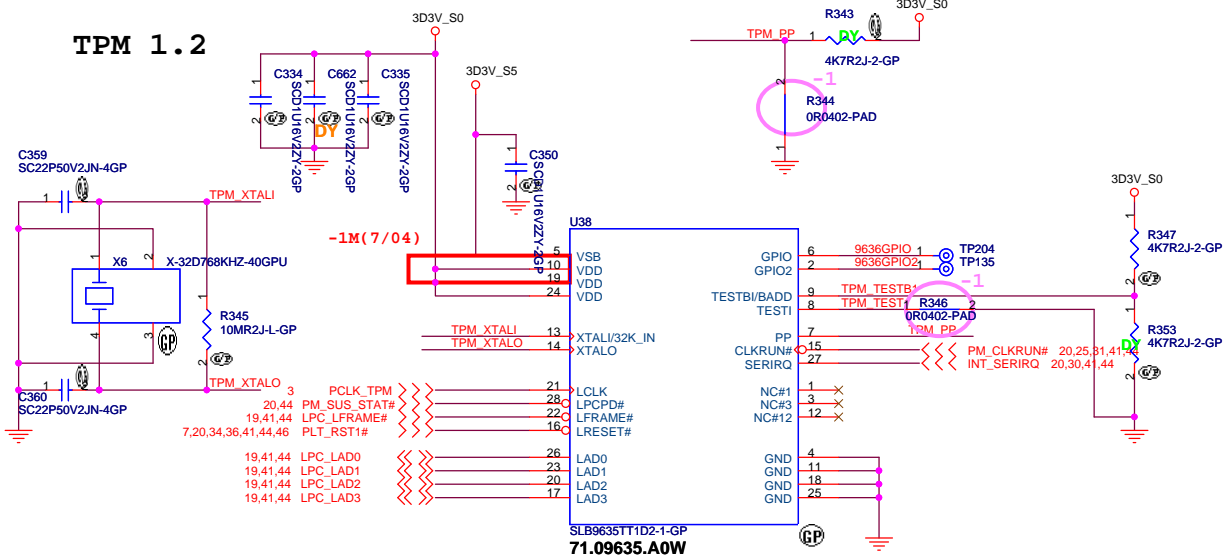
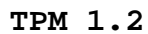
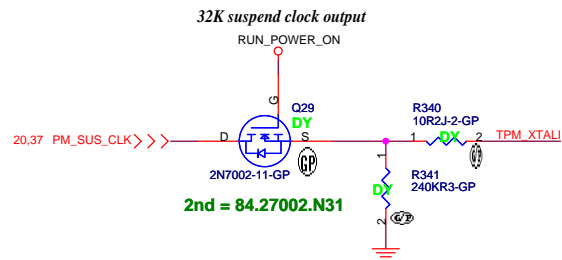
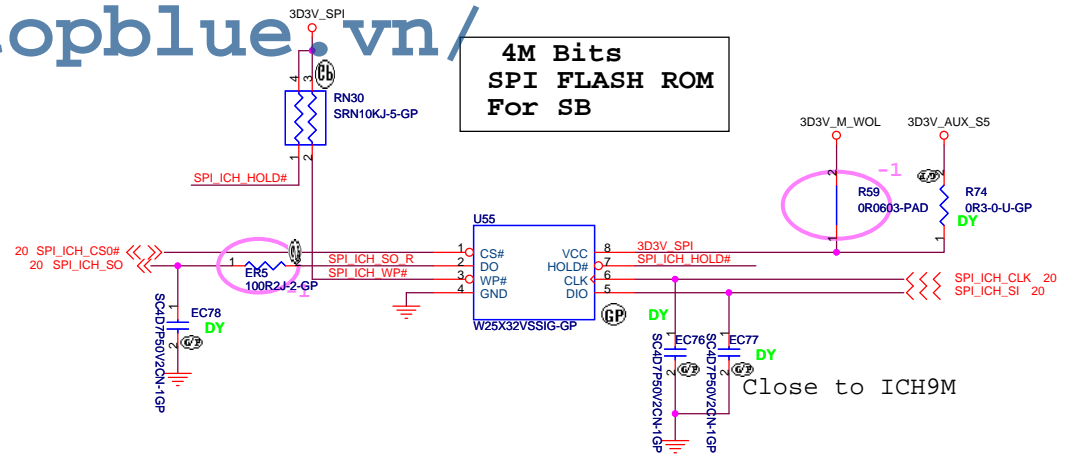
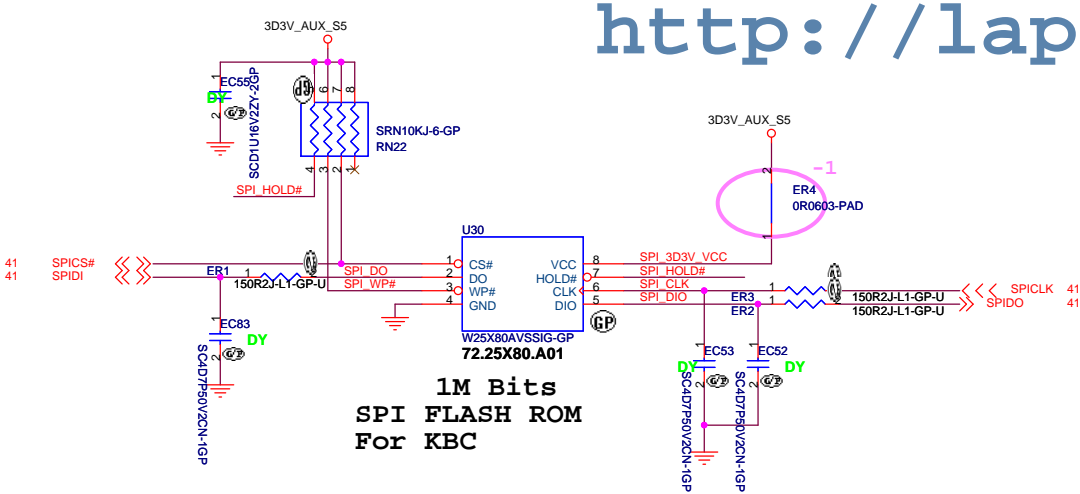
Date: Friday, November 21, 2008

Sheet 40

Rev	-1M
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TOP VIEW

A15	(B1)
A14	(B2)

A2	(B14)
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(BOTTOM VIEW)

Four Peaks

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Title

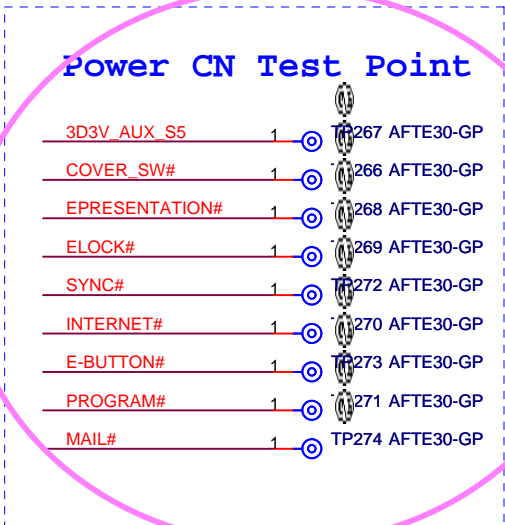
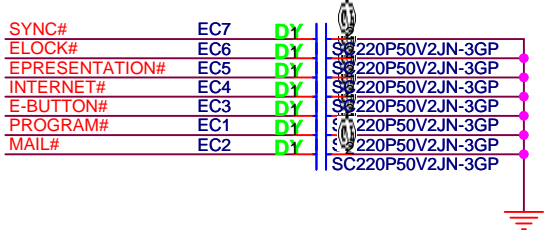
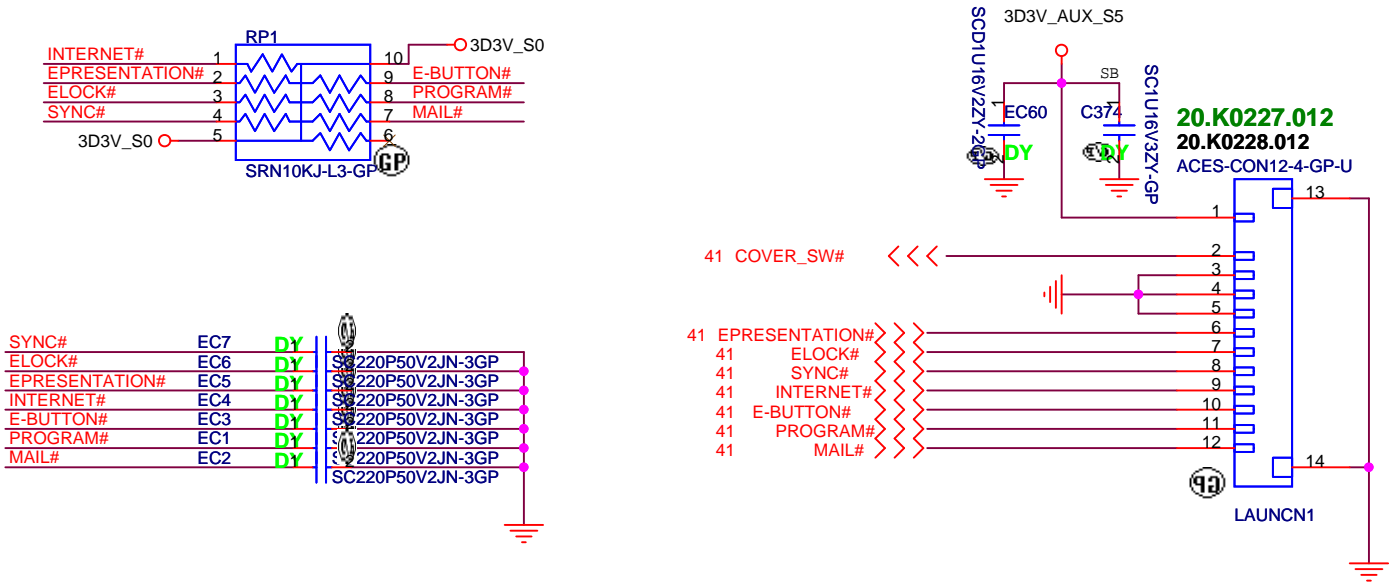
BIOS & TPM

Size	Document Number
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Four Peaks

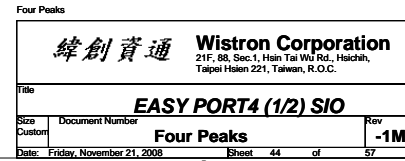
Date: Friday, November 21, 2008

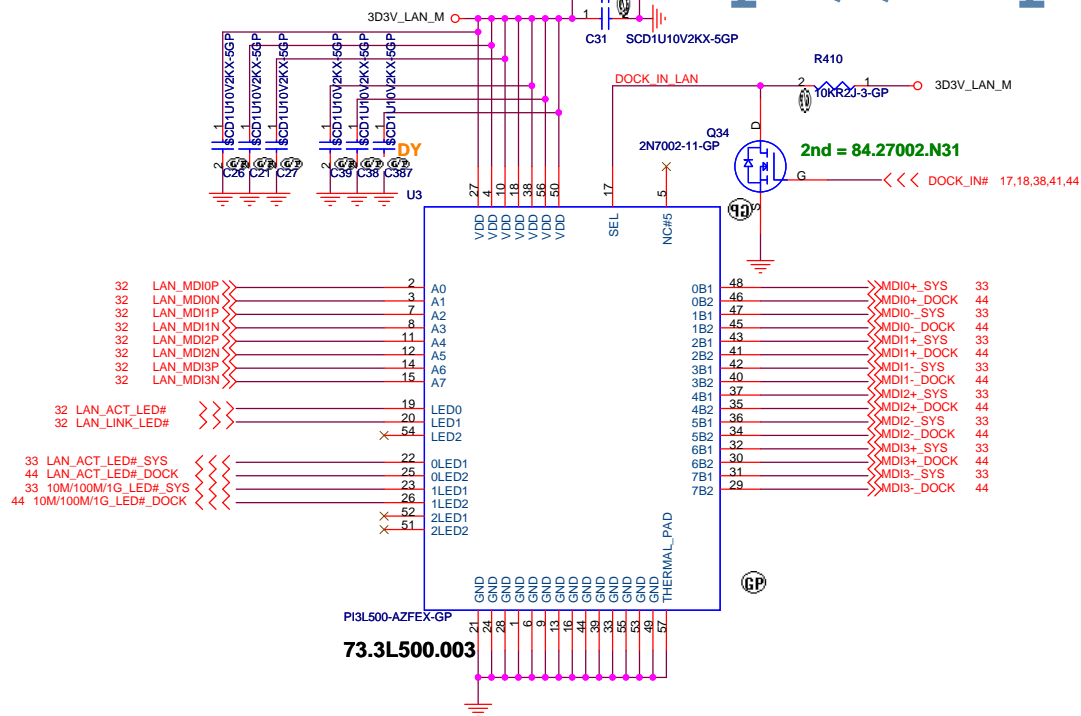
Sheet	42	of	57
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
LAUNCH			
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Function	SEL	
to An	L	DOCK
to Bn	H	SYSTEM

Four Peaks

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Title			
EASY PORT4 (2/2)			
Size A3	Document Number		Rev
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Put near graphic connector

7,18 PEG_TXP[15.0] <<>>
7,18 PEG_TXN[15.0] <<>>
7 PEG_RXP[15.0] <<>>
7 PEG_RXN[15.0] <<>>

15 G72_TXBOUT0+
15 G72_TXBOUT0-
15 G72_TXBOUT1+
15 G72_TXBOUT1-
15 G72_TXBOUT2+
15 G72_TXBOUT2-

15 G72_TXBCLK+
15 G72_TXBCLK-

44 CRT_BLUE
44 CRT_GREEN
44 CRT_RED

G72_TXACLK- 15
G72_TXACLK+ 15
G72_TXAOUT2- 15
G72_TXAOUT2+ 15
G72_TXAOUT1- 15
G72_TXAOUT1+ 15
G72_TXAOUT0- 15
G72_TXAOUT0+ 15

>>>LCD_EDID_DAT 15
>>>LCD_EDID_CLK 15

LCDVDD_ON 15
BLON_IN 41

NV_DVI_DAT 18
NV_DVI_CLK 18

2D5V_S0

R122 0R0603-PAD
DIS

C109
DIS

49-1-Z55A0100JS

SCD1U25V3KX-GP

MXM1
TYCO-CONN230A-GP-U3

18 TMD5_A_TX0+ 18
18 TMD5_A_TX0- 18
18 TMD5_A_TX1+ 18
18 TMD5_A_TX1- 18
18 TMD5_A_TX2+ 18
18 TMD5_A_TX2- 18
18 TMD5_A_TXC+ 18
18 TMD5_A_TXC- 18

<<<DVI_A_HPD 18

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG

3 MXM_CLKREQ#

PLT_RST1# MXM

HDMI_CEC
SMBD_MXM

SMBD_MXM

17 CRT_HSYNC
17 CRT_VSYNC

TPAD30 TP64
TPAD30 TP70
TPAD30 TP177
TPAD30 TP177

SPDIF_HDMI
GPU_BUFRST#
MP_INT
GPU_PRGM#

303V_S0
IGP_UTC2#
IGP_UTC2
TMD5_GPIO6_SW

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
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TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

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TPAD30 TP167

TPAD30 TP172
TPAD30 TP166
TPAD30 TP168
TPAD30 TP167

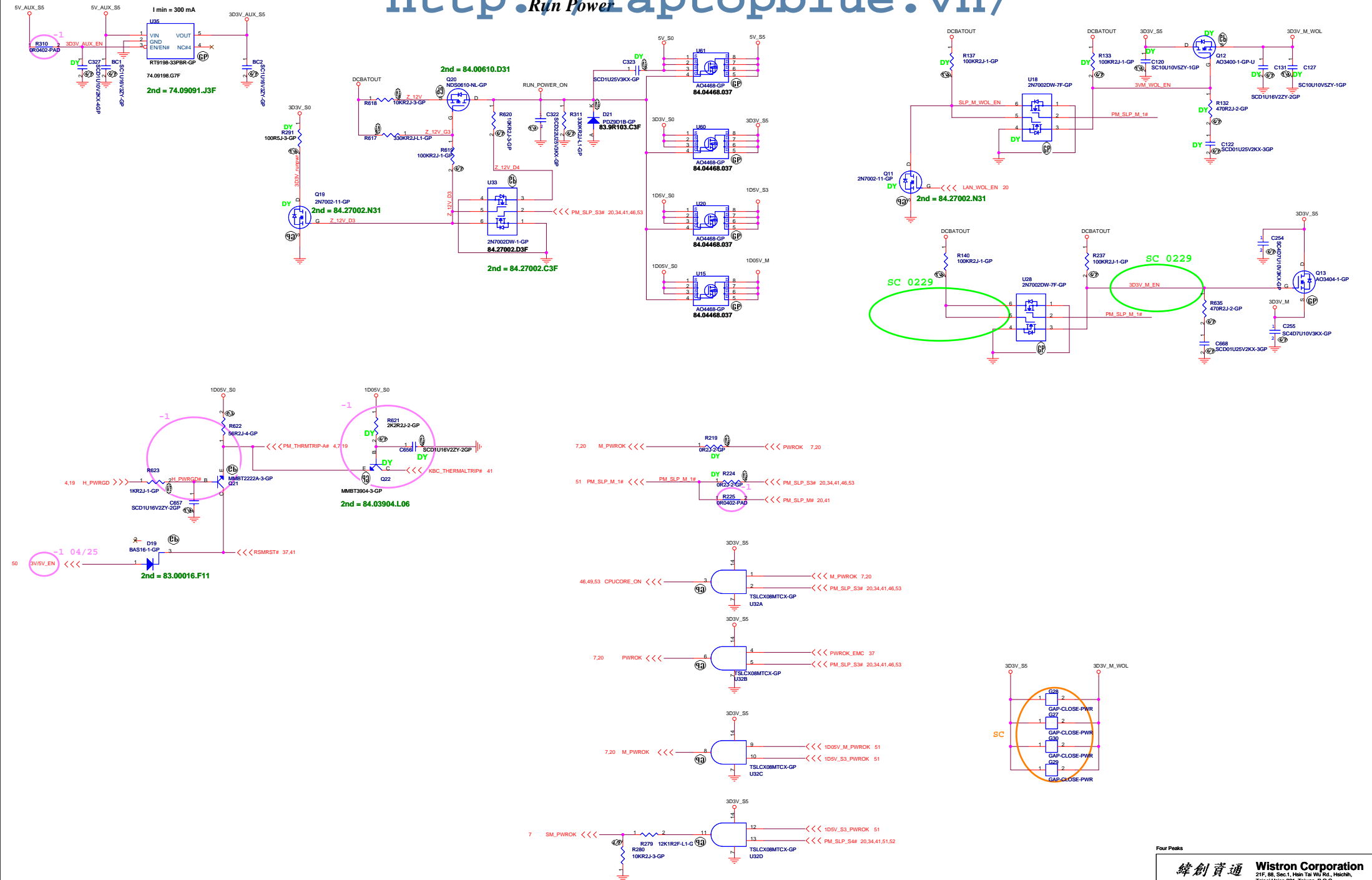
Four Peaks

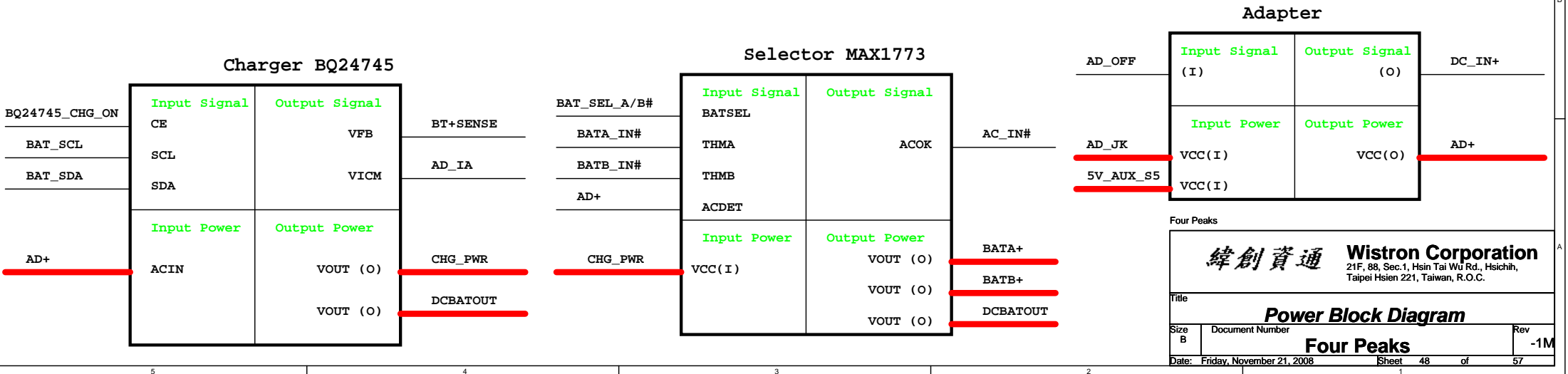
Aux Power

3D3V_AUX_S5

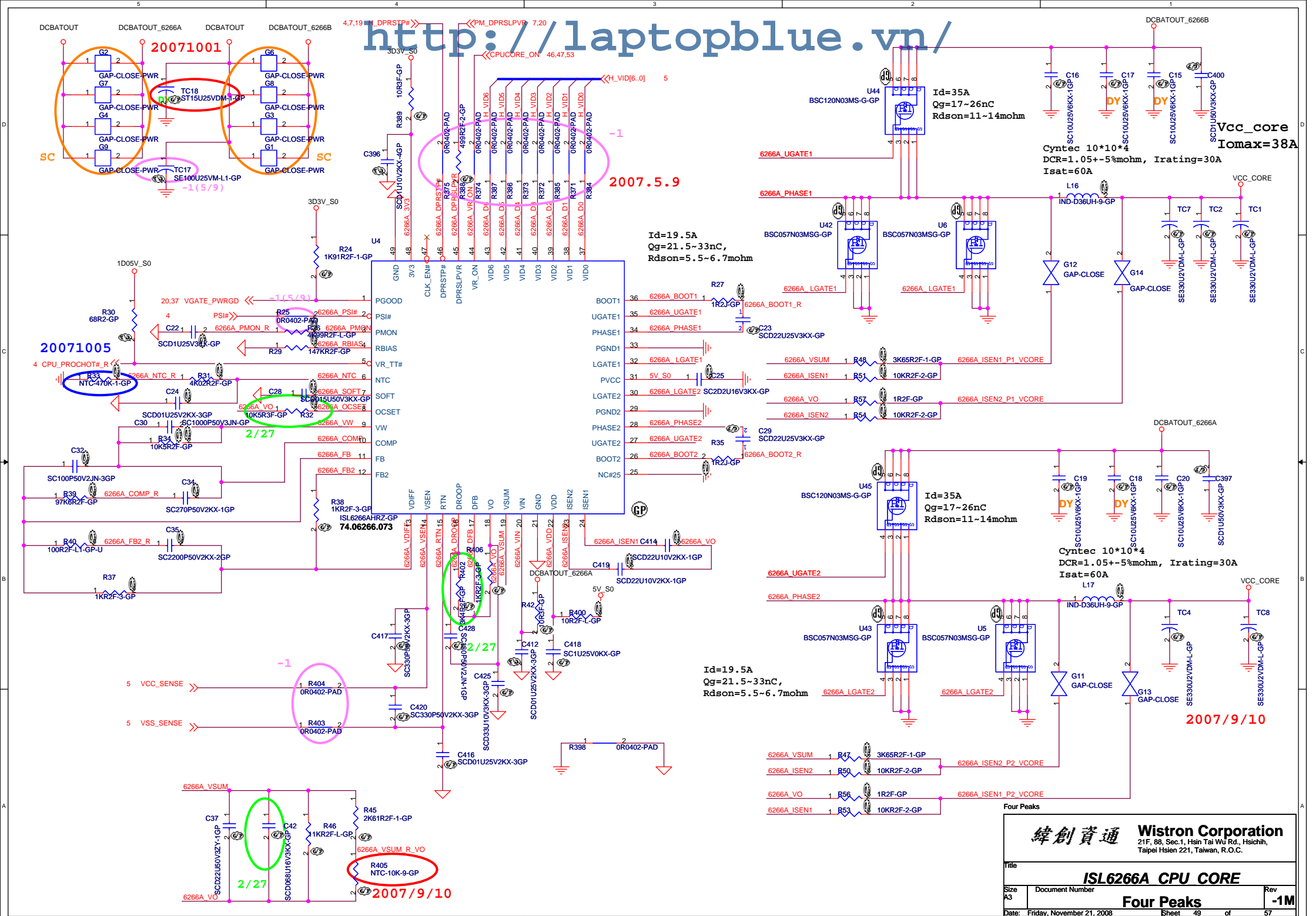
<http://laptopblue.vn/>

Run Power



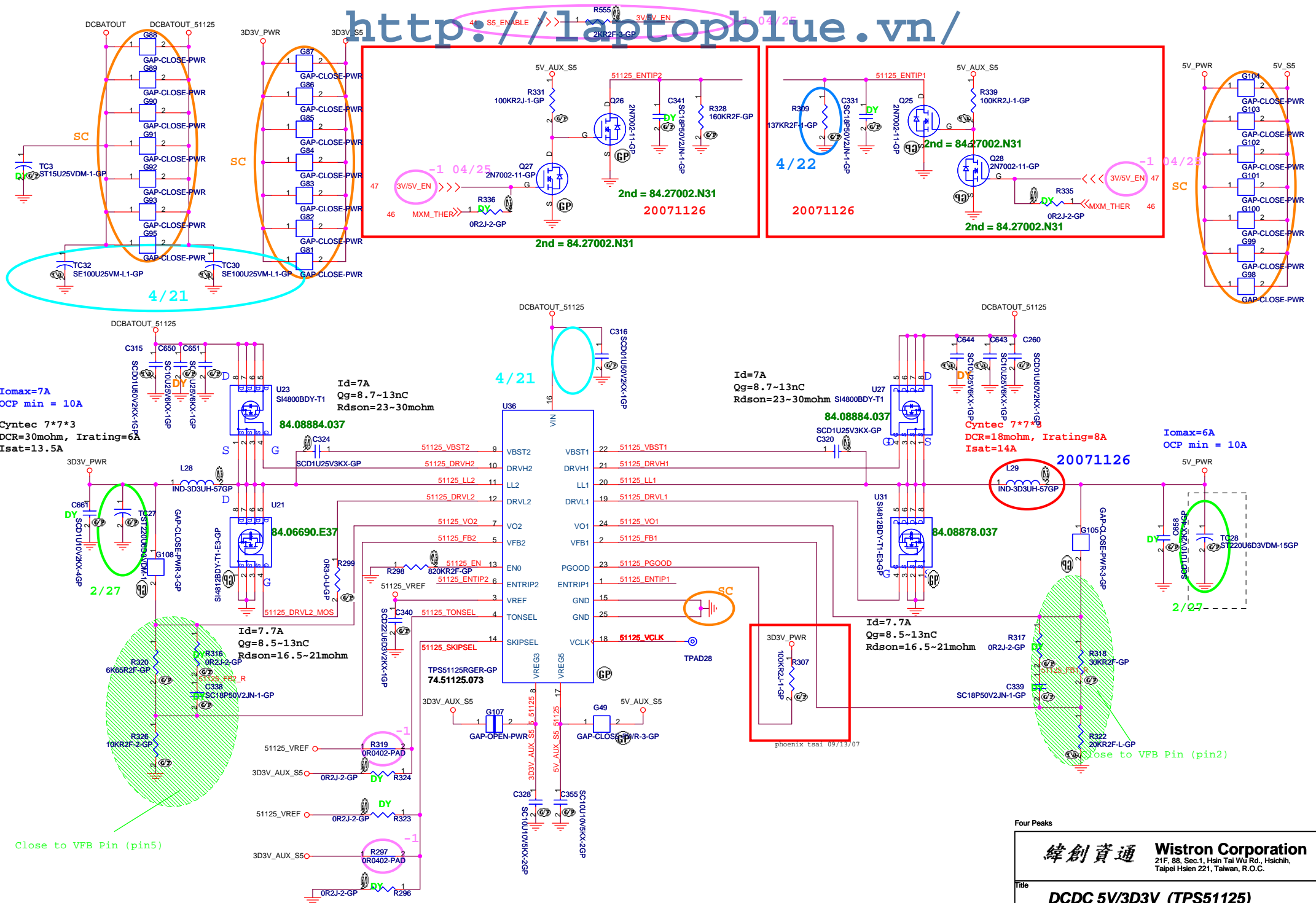


9<PM_DPRSTP#>> 7.20
3D3V_S0
<<CPUCORE ON 46.47.53



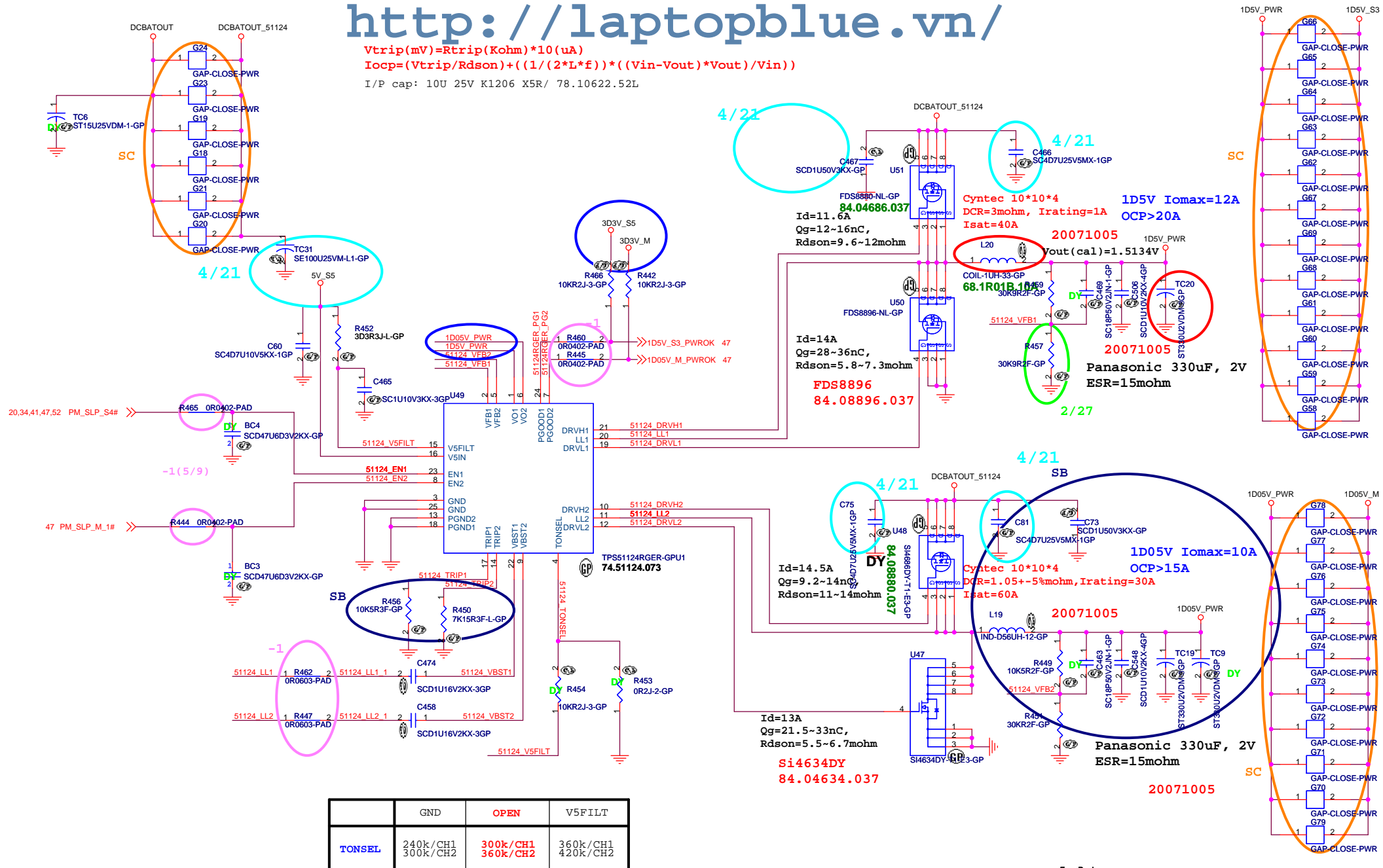
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
ISL6266A CPU CORE			
Size A3	Document Number	Four Peaks	Rev -1M
Date: Friday, November 21, 2008	Sheet 49	of	57

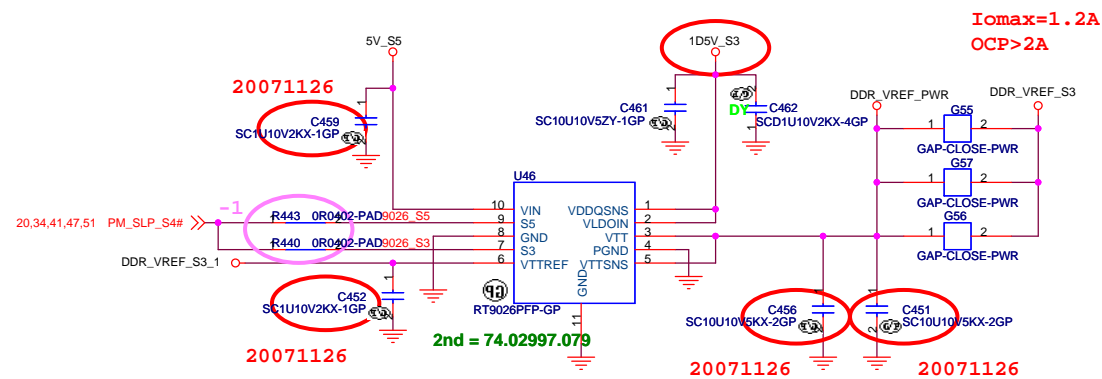


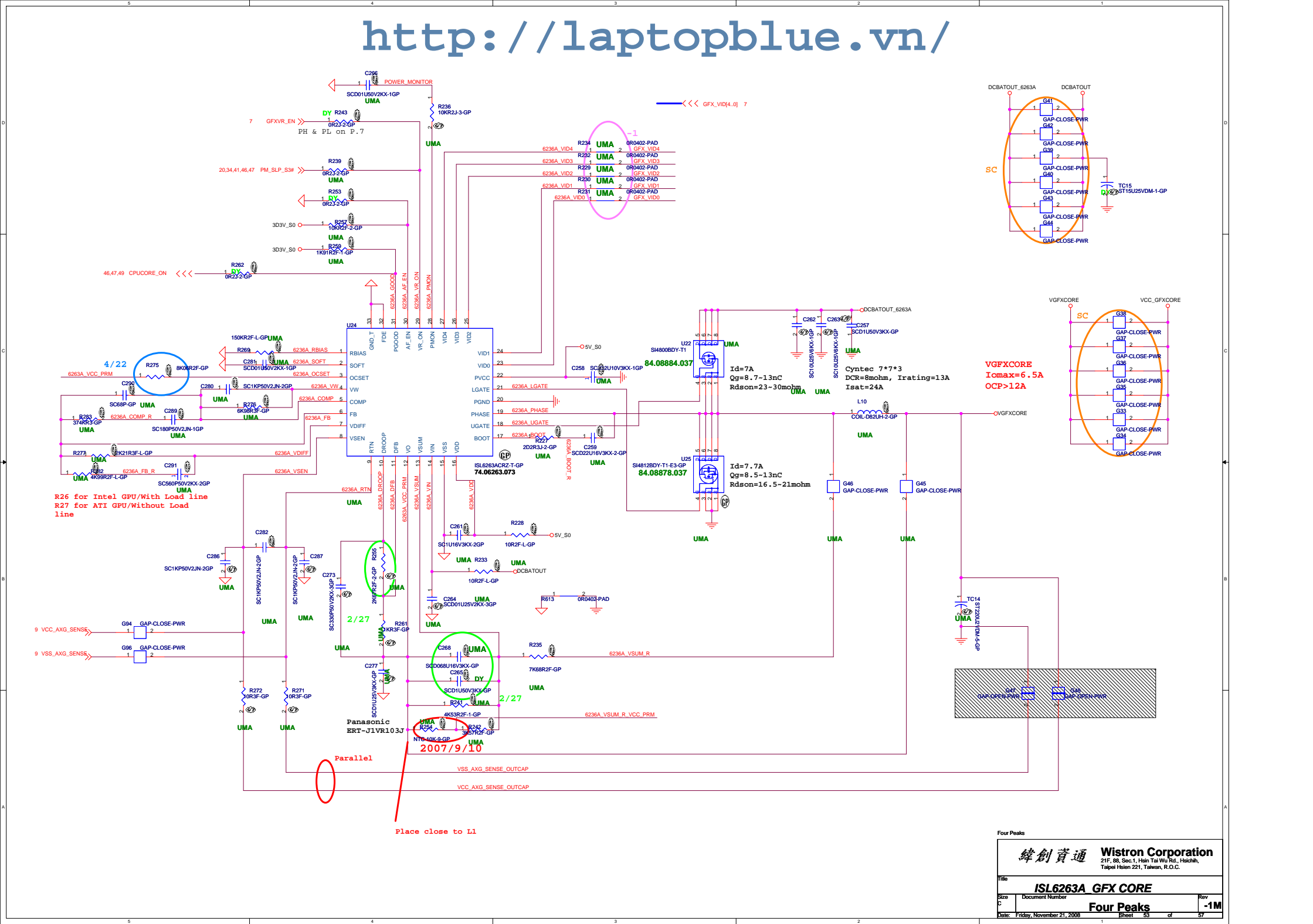
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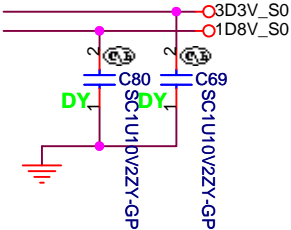
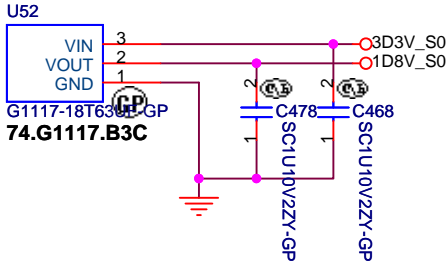
$V_{trip}(mV) = R_{trip}(Kohm) * I_0(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



Four Peaks

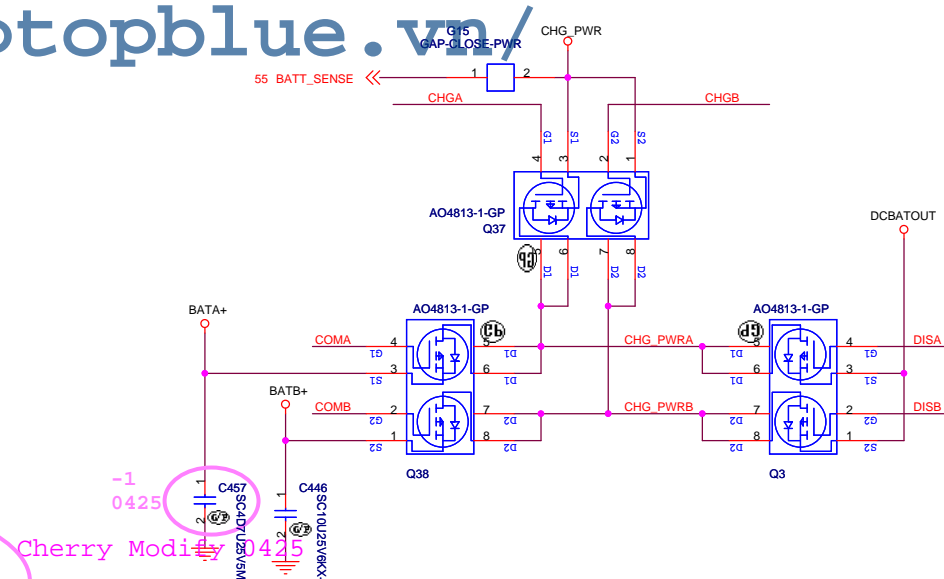






Four Peaks

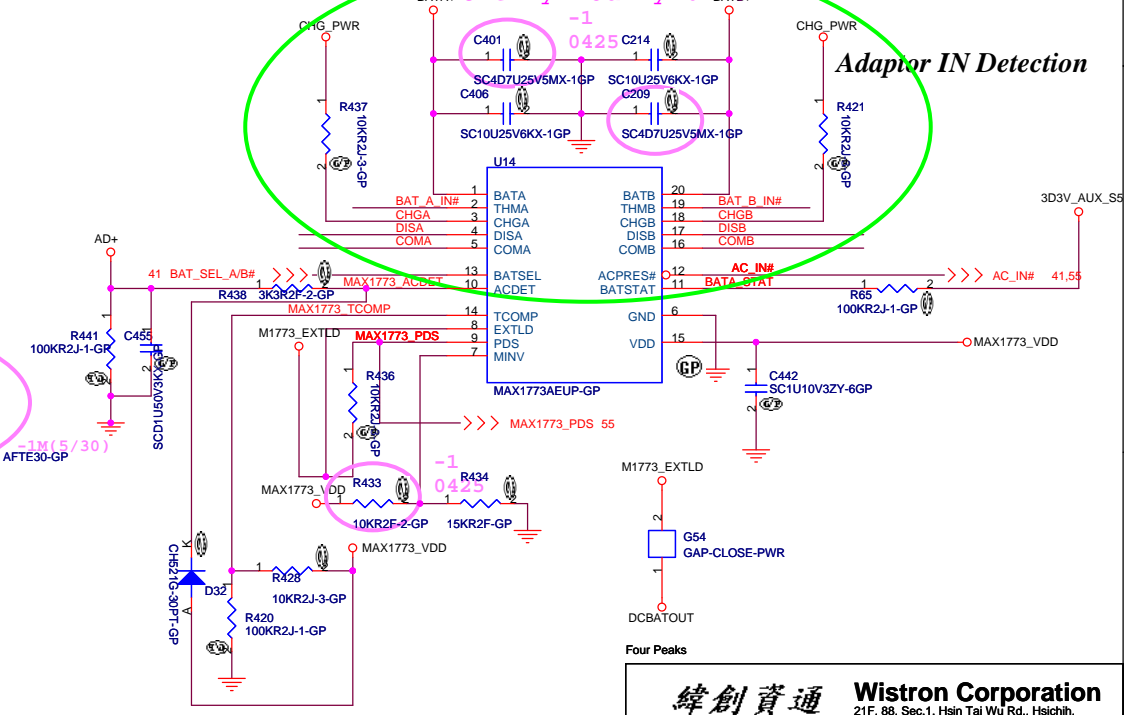
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VGA CORE S0 (UMA)			
Size A4	Document Number		Rev
	Four Peaks		-1M
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BAT1 Conn. Test Point



~~Adaptor IN Detection~~



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Stand off Location

SC

Four Peaks

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Title
EMI/Spring/Boss

Size Document Number Rev
Four Peaks -1M

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Stand off Location

