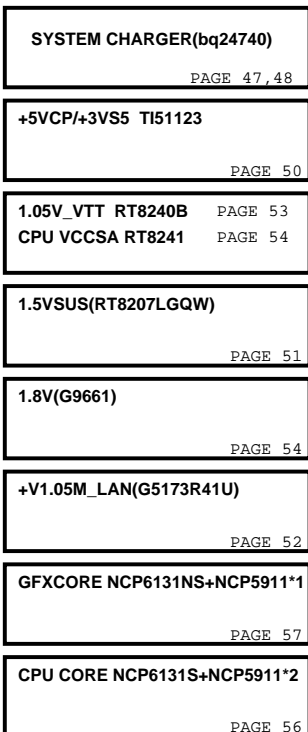
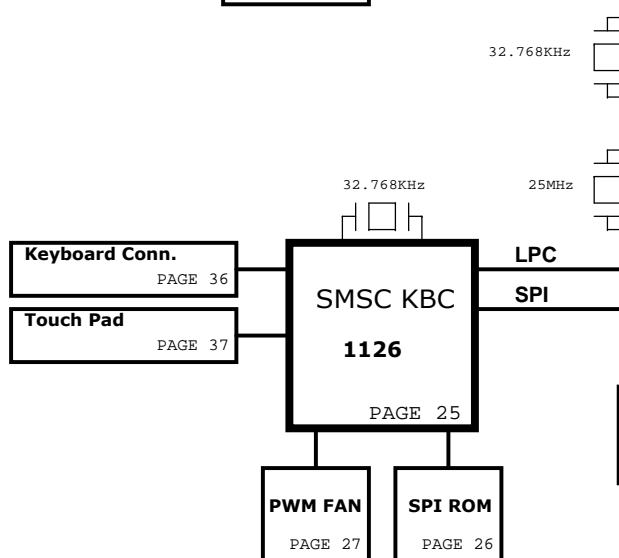
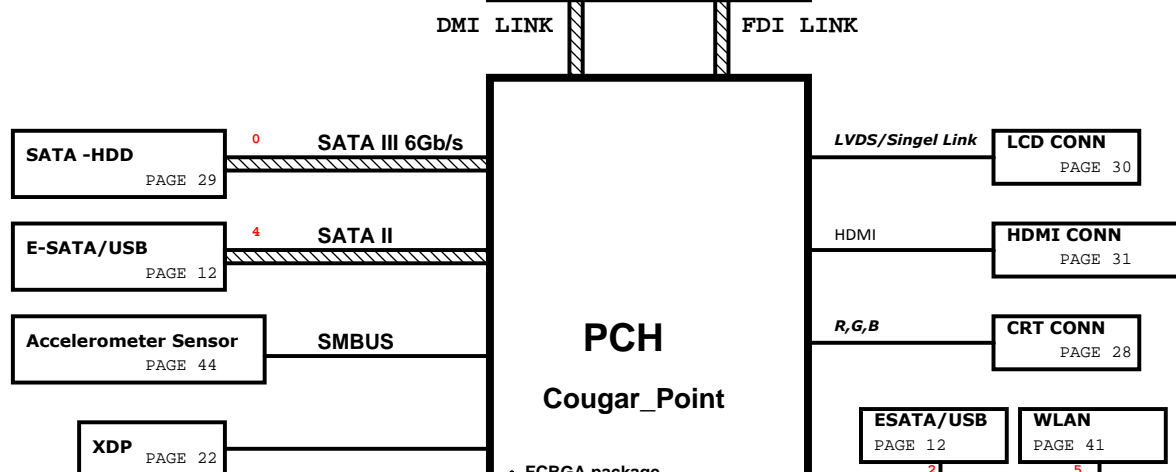
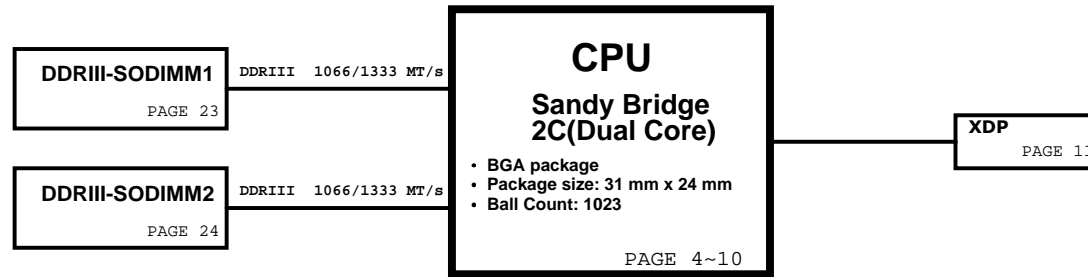


PCB STACK UP  
8L UMA. PV

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT

# F11, Foreigner (Huron River) BLOCK DIAGRAM 01



power State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

PCIE	Foreigner
1	X
2	X
3	JMB709
4	WLAN
5	X
6	NIC
7	WWAN
8	X

SATA	Foreigner
0	HDD
1	X
2	X
3	X
4	eSATA
5	X

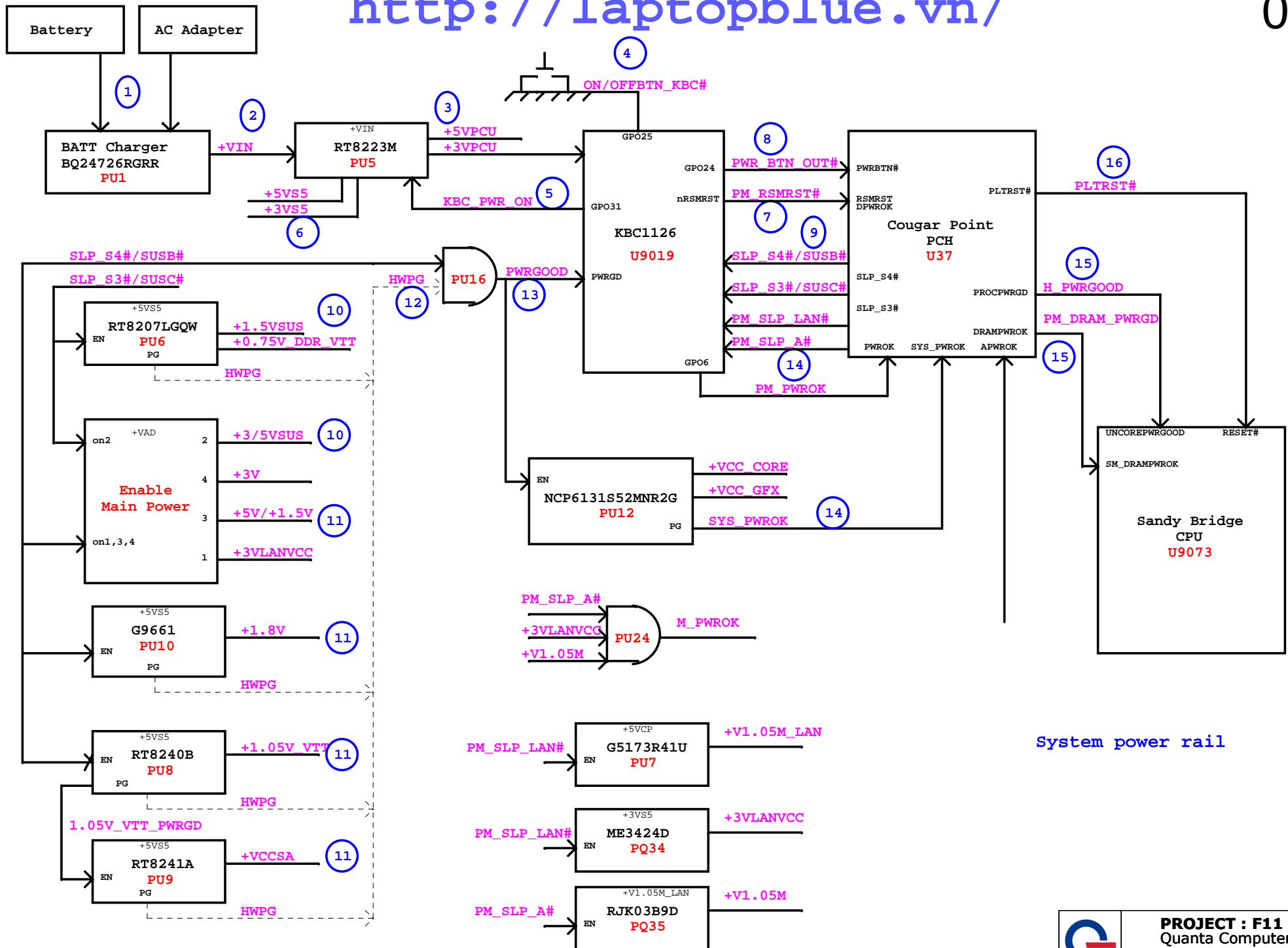
USB	Foreigner
0	CONN(USB Charger)
1	CONN
2	eSATA
3	CAMERA
4	X
5	BT or WLAN
6	X
7	X
8	Finger print
9	WWAN
10	X
11	X
12	X
13	X

	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) / 0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA4	SMSC 1126	Intel Lan Gbe PHY:0x64 Gbe MAC:0x70
SMB_PCH_CLK SMB_PCH_DAT	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_ME0_CLK SMB_ME0_DAT	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1126	Y	X	X	X	X	X	X	X



**PROJECT : F11**  
Quanta Computer Inc.

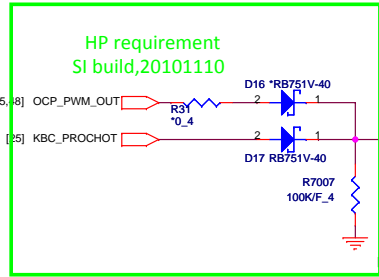
Size Custom	Document Number <b>power rails</b>	Rev 1A
Date: Wednesday, January 19, 2011	Sheet 2 of 58	



System power rail

PEG\_COMP connect to PIN G2&F3 W:4mils/S:15mils/L: 500mils.  
PEG\_COMP connect to PIN H1 W:12mils/S:15mils/L: 500mils.



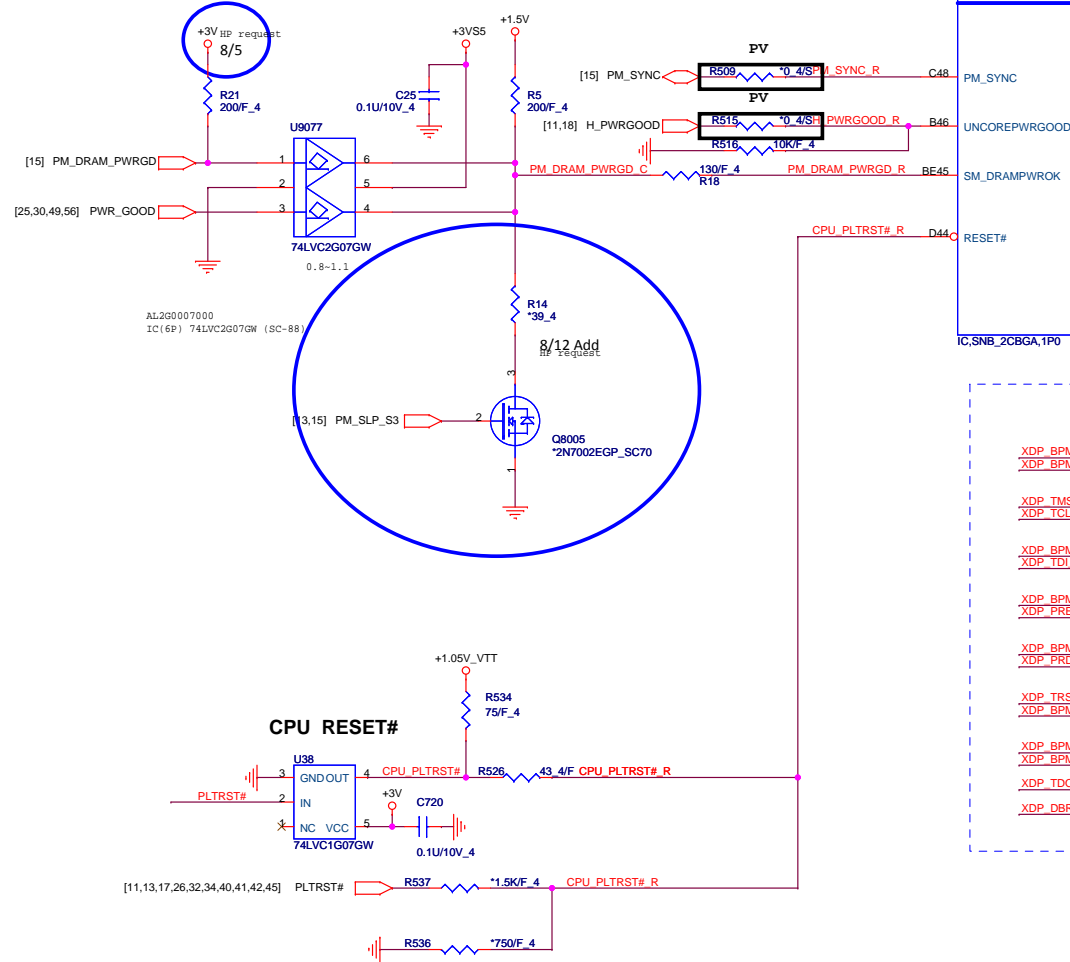


HP requirement  
SI build,20101110

SNB\_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

## SM\_DRAMPWROK Processor Input.



MISC

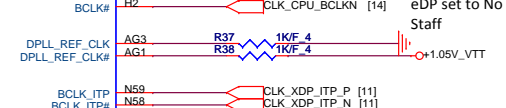
THERMAL

PWR MANAGEMENT

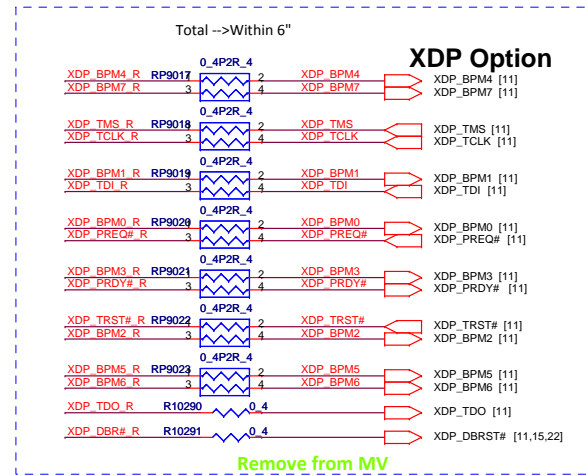
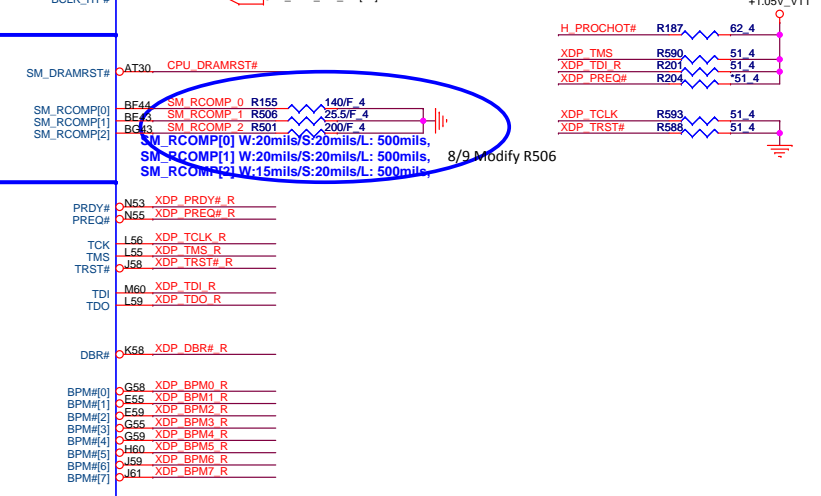
CLOCKS

DDR3

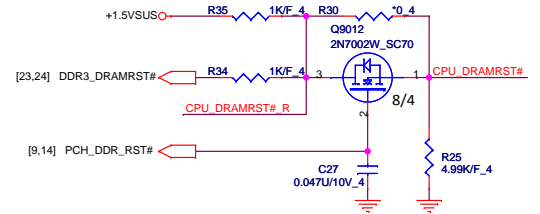
JTAG & BPM



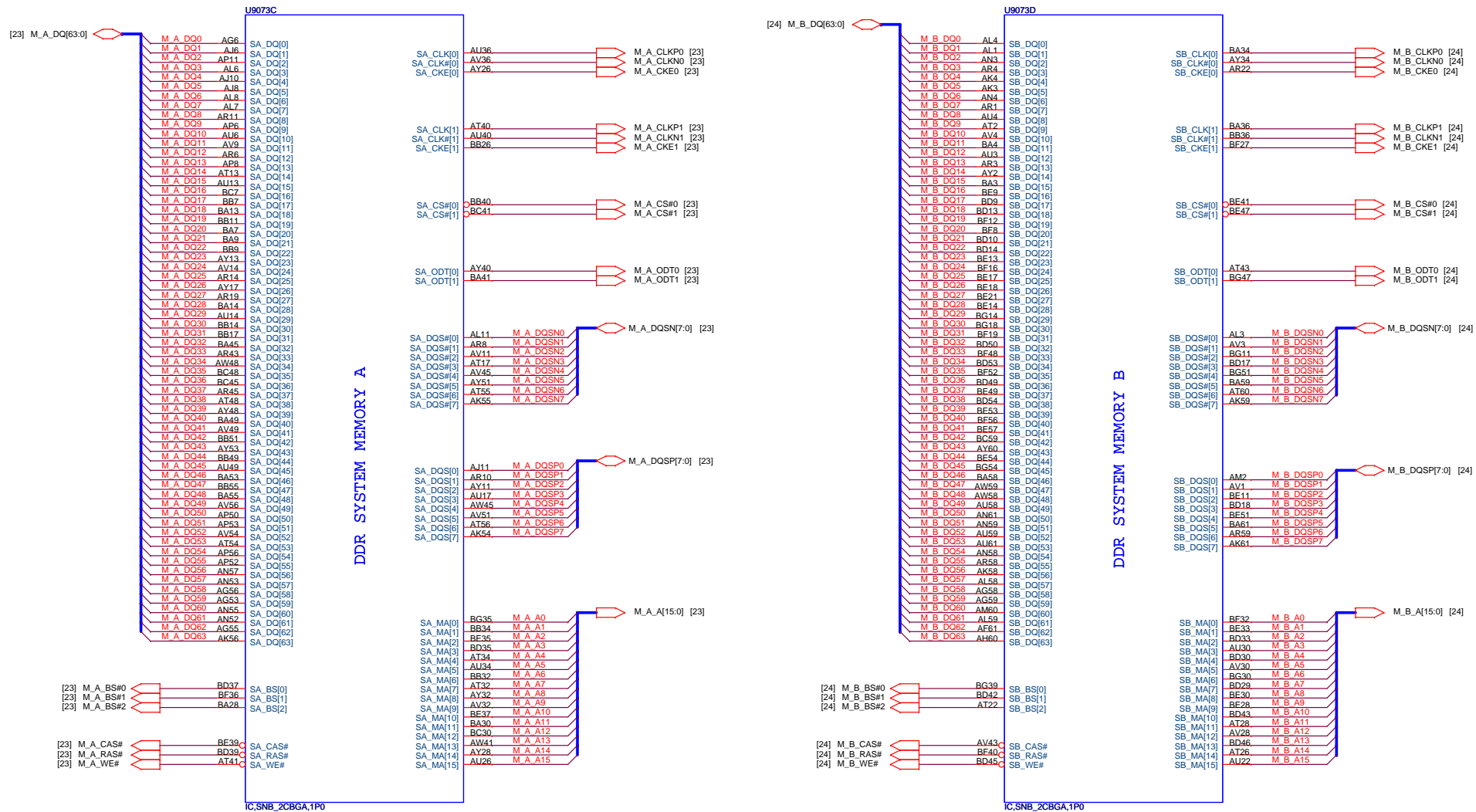
## Processor pull-up (CPU)

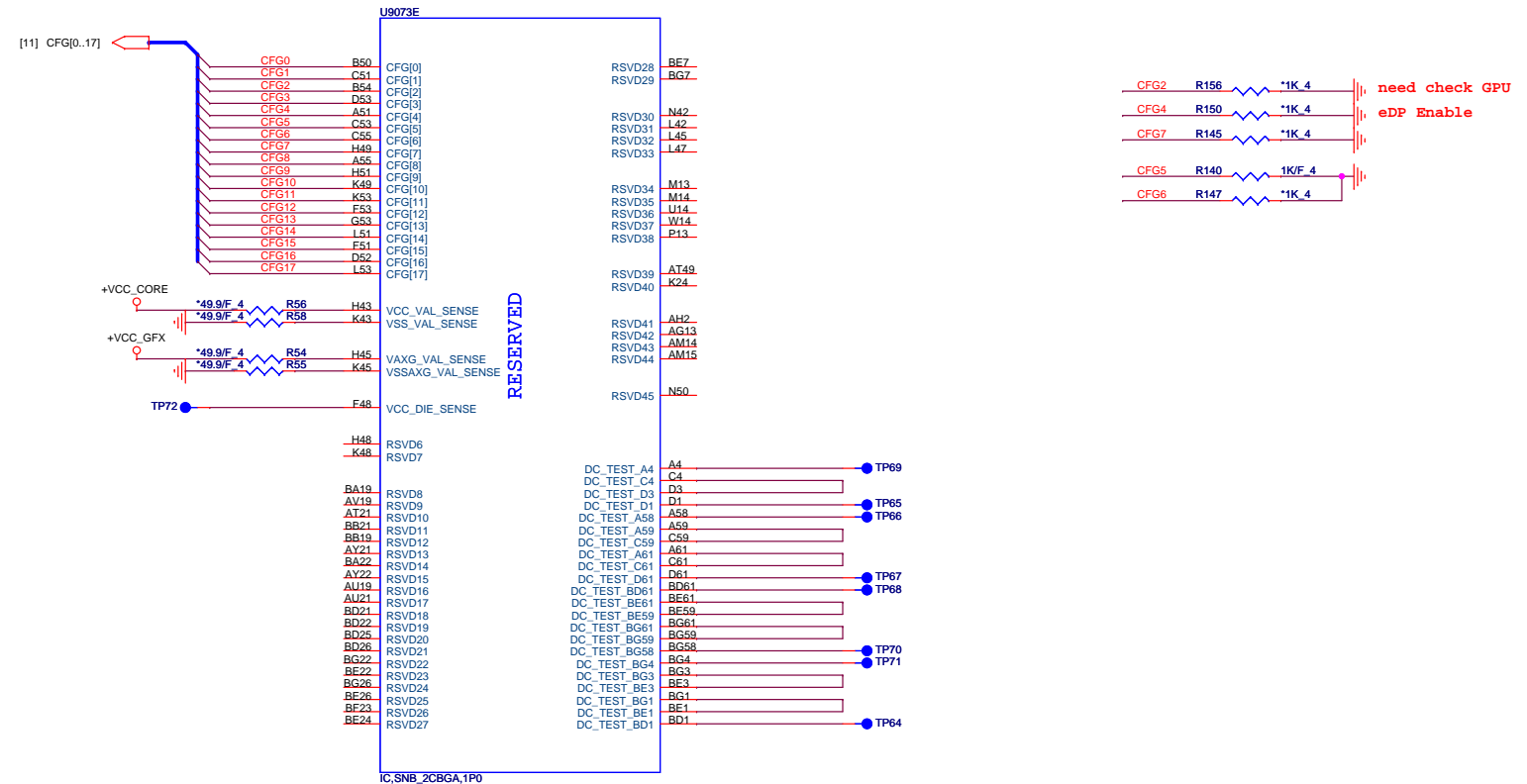


## DDR3 DRAM RESET



# Sandy Bridge Processor (DDR3)





#### CFG[6:5] (PCIe Port Bifurcation Straps)

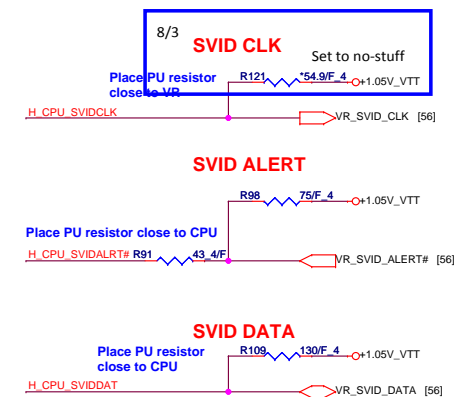
11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

#### Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

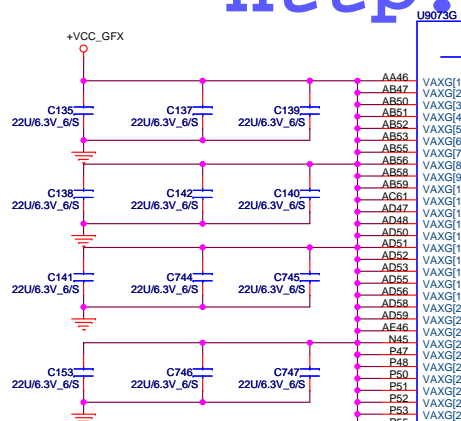
330uf \*4





22uf \*12

330uf \*3



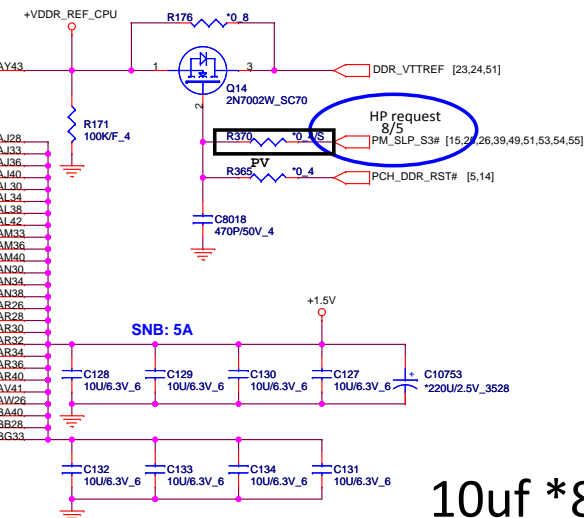
U9073G  
VAXG[1]  
VAXG[2]  
VAXG[3]  
VAXG[4]  
VAXG[5]  
VAXG[6]  
VAXG[7]  
VAXG[8]  
VAXG[9]  
VAXG[10]  
VAXG[11]  
VAXG[12]  
VAXG[13]  
VAXG[14]  
VAXG[15]  
VAXG[16]  
VAXG[17]  
VAXG[18]  
VAXG[19]  
VAXG[20]  
VAXG[21]  
VAXG[22]  
VAXG[23]  
VAXG[24]  
VAXG[25]  
VAXG[26]  
VAXG[27]  
VAXG[28]  
VAXG[29]  
VAXG[30]  
VAXG[31]  
VAXG[32]  
VAXG[33]  
VAXG[34]  
VAXG[35]  
VAXG[36]  
VAXG[37]  
VAXG[38]  
VAXG[39]  
VAXG[40]  
VAXG[41]  
VAXG[42]  
VAXG[43]  
VAXG[44]  
VAXG[45]  
VAXG[46]  
VAXG[47]  
VAXG[48]  
VAXG[49]  
VAXG[50]  
VAXG[51]  
VAXG[52]  
VAXG[53]  
VAXG[54]  
VAXG[55]  
VAXG[56]

POWER

DDR3 - 1.5V RAILS

GRAPHICS

CAD Notes: +VDDR\_REF\_CPU should have 10mil trace width

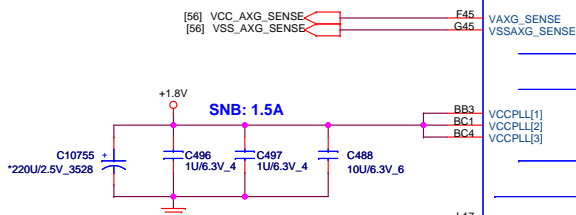


10uf \*8  
330uf \*1

10uf \*1

1uf \*2

330uf \*1



VAXG\_SENSE  
VSSAXG\_SENSE

SENSE LINES  
1.8V RAIL

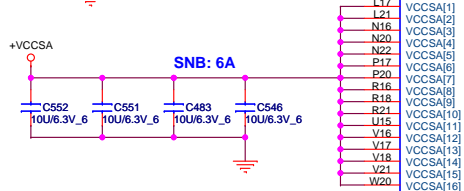
QUIET RAILS

SENSE LINES

SA RAIL

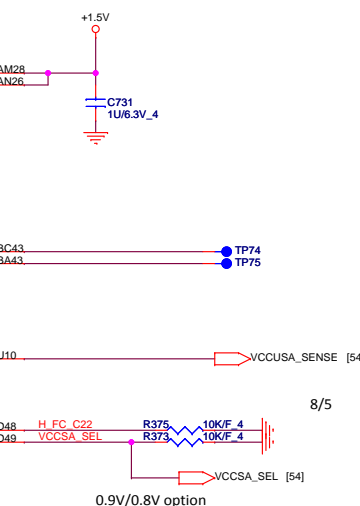
10uf \*4

330uf \*1

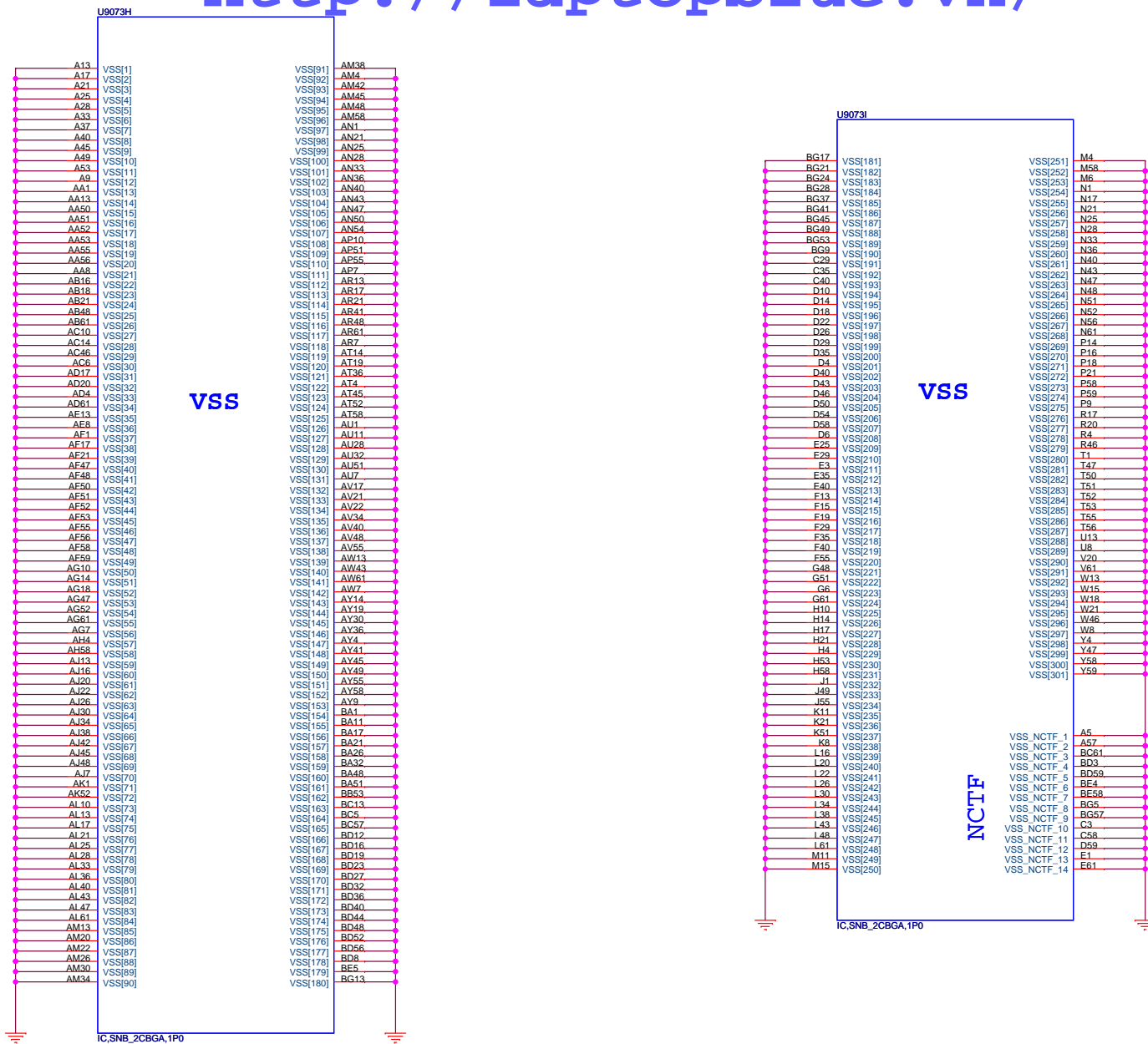


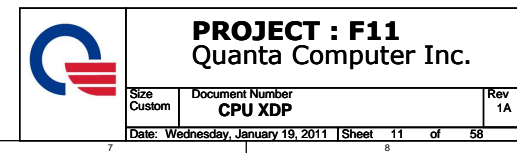
VCCSA[1]  
VCCSA[2]  
VCCSA[3]  
VCCSA[4]  
VCCSA[5]  
VCCSA[6]  
VCCSA[7]  
VCCSA[8]  
VCCSA[9]  
VCCSA[10]  
VCCSA[11]  
VCCSA[12]  
VCCSA[13]  
VCCSA[14]  
VCCSA[15]  
VCCSA[16]

IC:SNB\_2CBGA,1P0

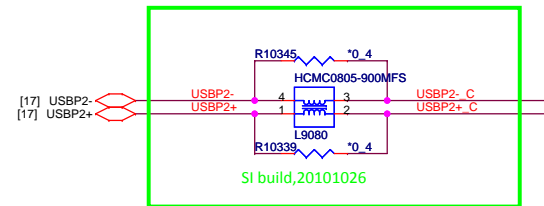
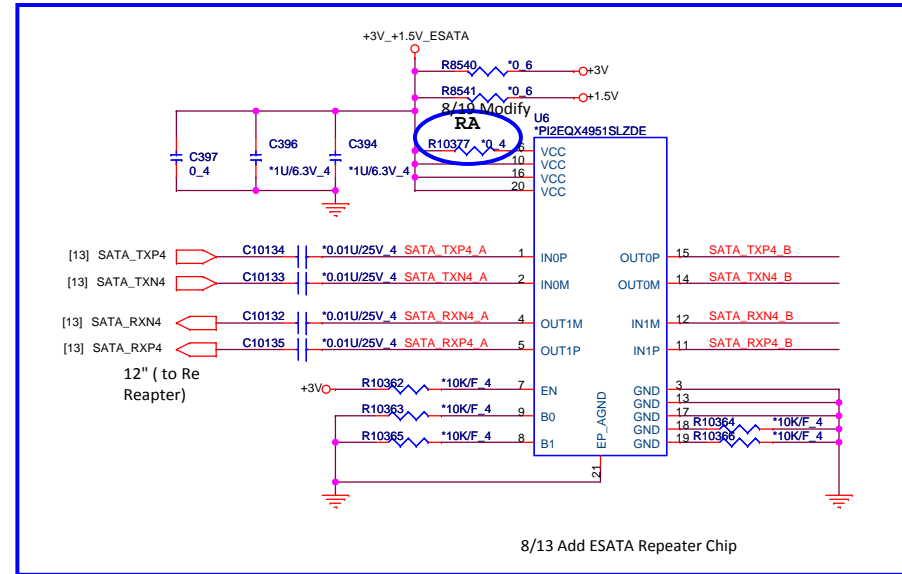


VCCSA\_SEL: Low -->0.9V  
VCCSA\_SEL: High -->0.8V

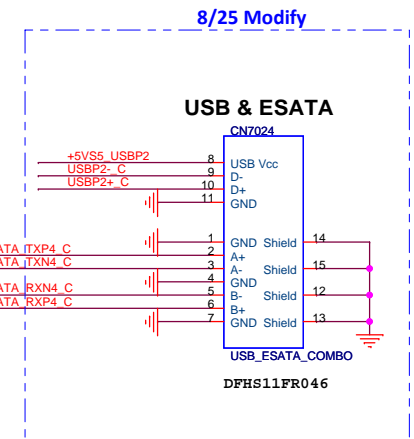
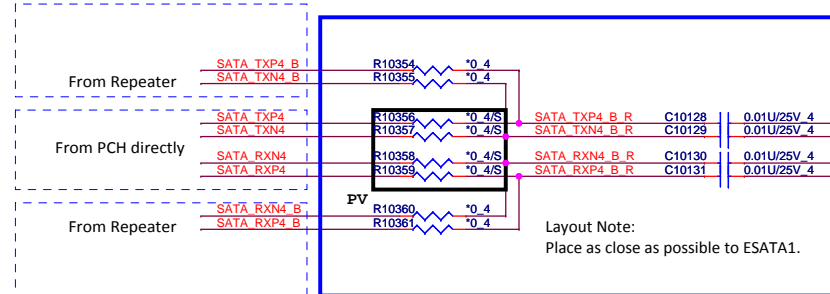
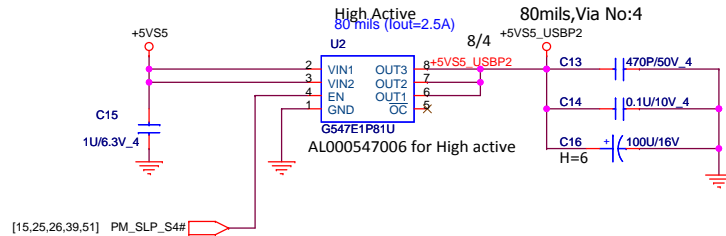


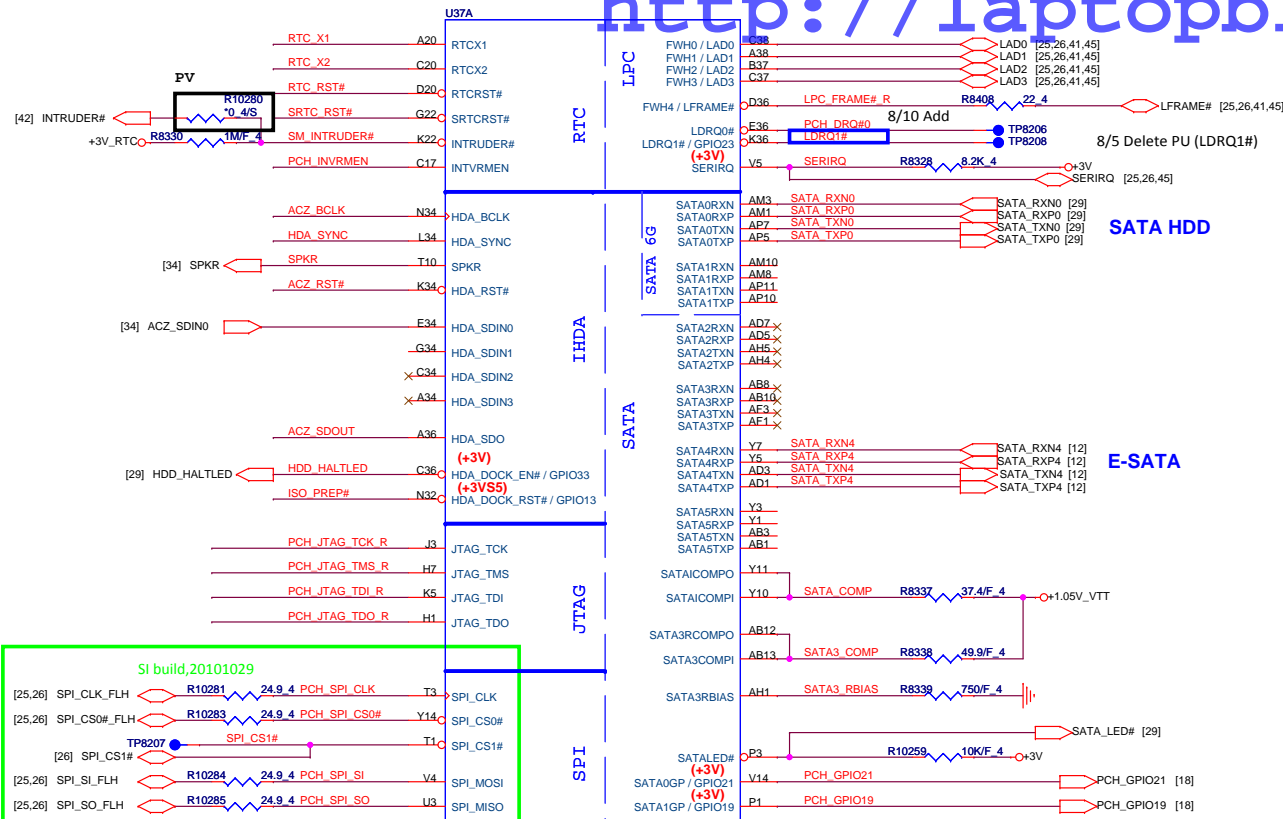


Signals		2EQX4951SL	3EQX4951ST
U6#6	RA	0 ohm	NC



## Standard USB





Close to PCH

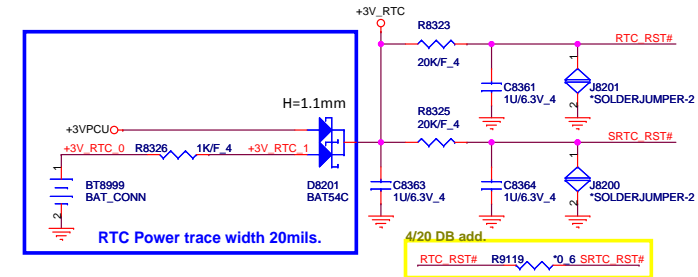
CougarPoint\_Rev\_Dp7  
fcbg989-intel-cougarpoint  
A10QNF0100  
IC CTRL(989P) COUGARPOINT QNLF TOP B/S

Remove from MV

PCH Strap Table

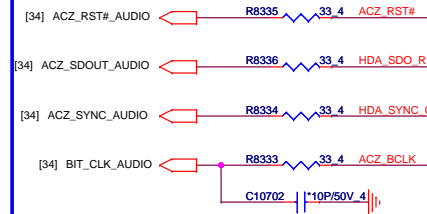
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8348 1K 4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K/F 4 +3V_RTC
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 1K 4 NV_ALE [17]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K 4 R8361 4.7K/F 4 NV_CLE [17] H_SNB_IVB# [5] N.A at CPT EDS 0.7
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	SPI_SI_FLH R8398 1K/F 4 +3V

RTC Circuitry(RTC)

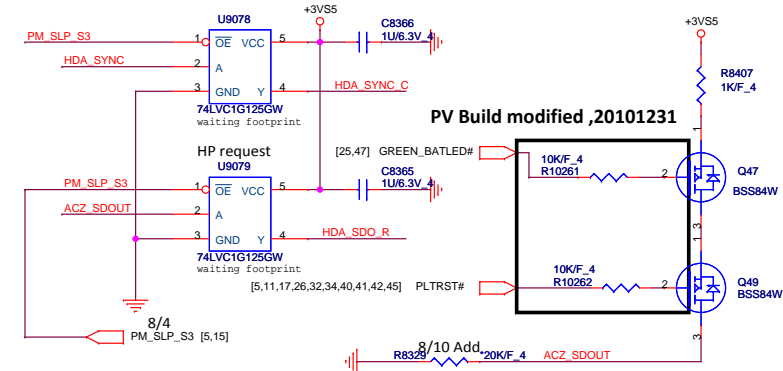
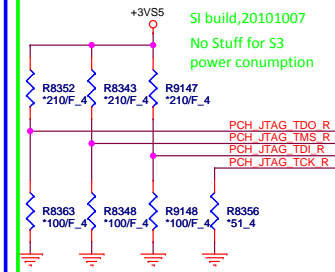


HDA Bus(CLG)

For Audio

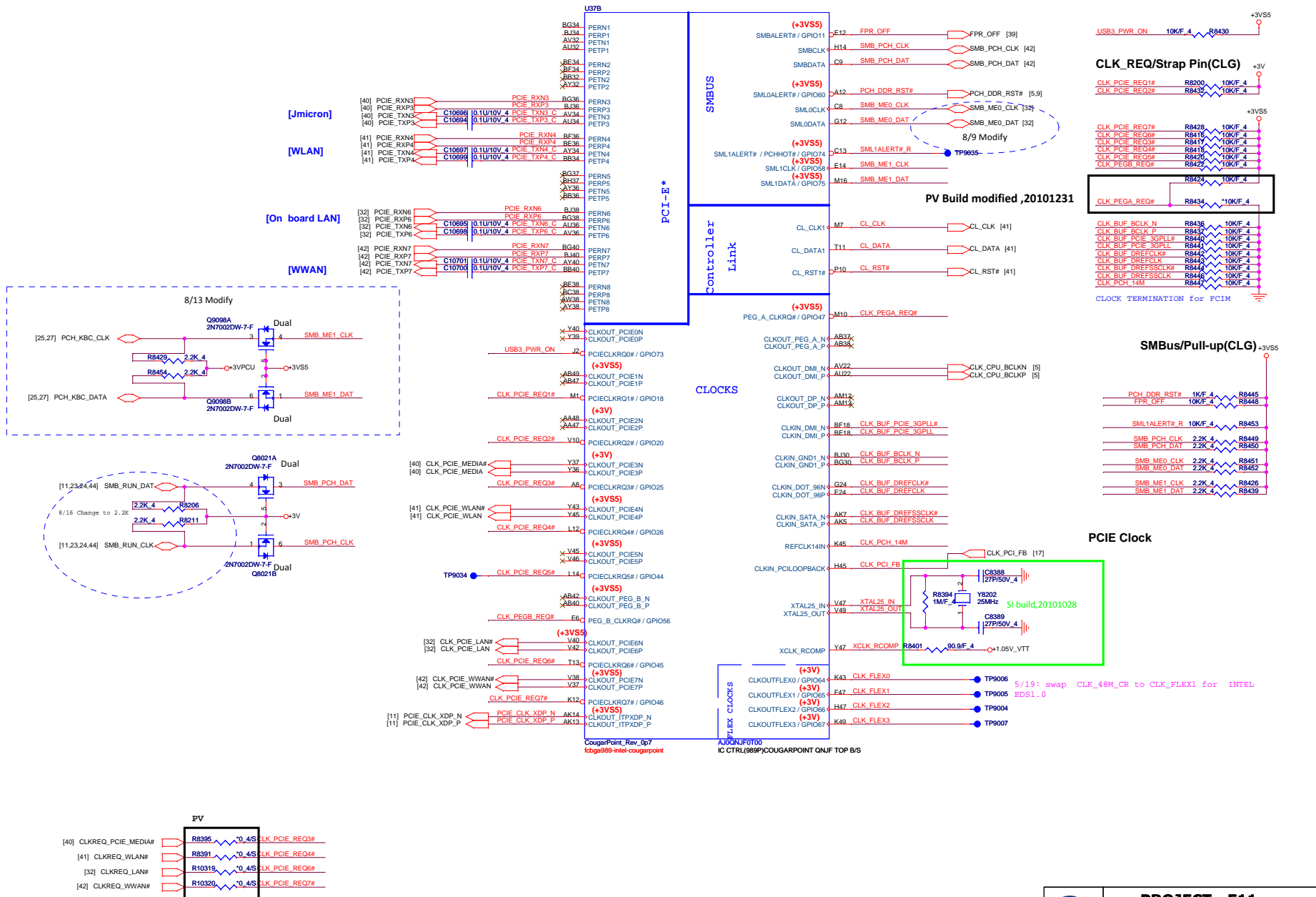


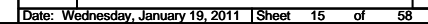
PCH JTAG Debug(CLG)

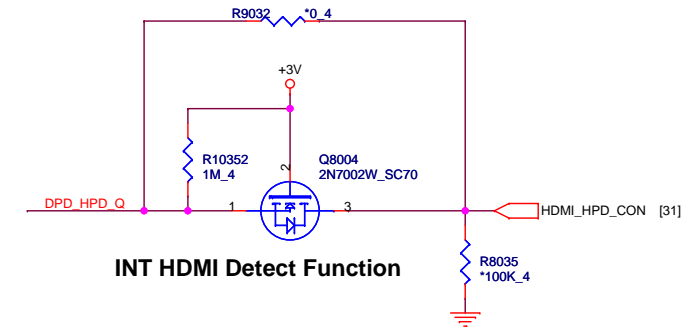
PROJECT : F11  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/9 (SATA/HDA/SPI)	1A
Date: Wednesday, January 19, 2011	1 Sheet	13 of 58

Cougar Point-M (PCI-E,SMBUS,CLK)







## INT HDMI Detect Function

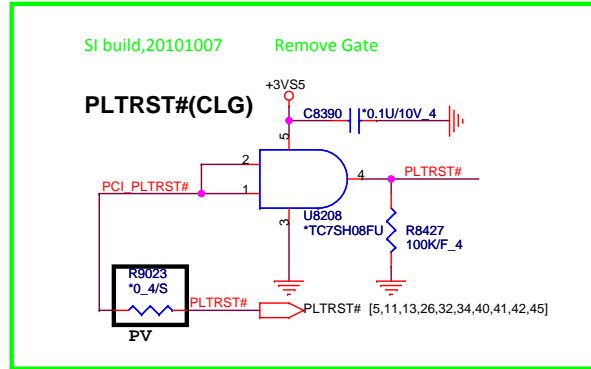
8/16 Delete Shortpad due layout routing



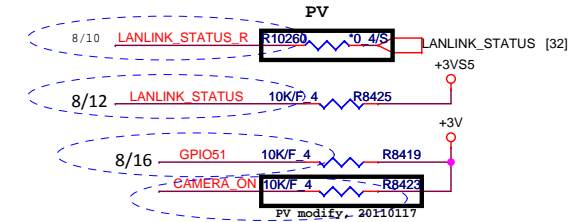
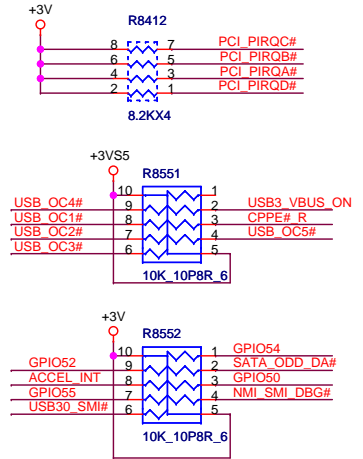
**PROJECT : F11**  
Quanta Computer Inc.

Size B	Document Number PCH 4/9 (LVDS/DDP/CRT)	Rev 1A
Date: Wednesday, January 19, 2011		Sheet 16 of 58

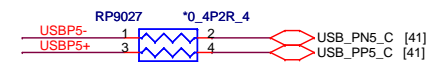




**PCI/USBOC# Pull-up(CLG)**

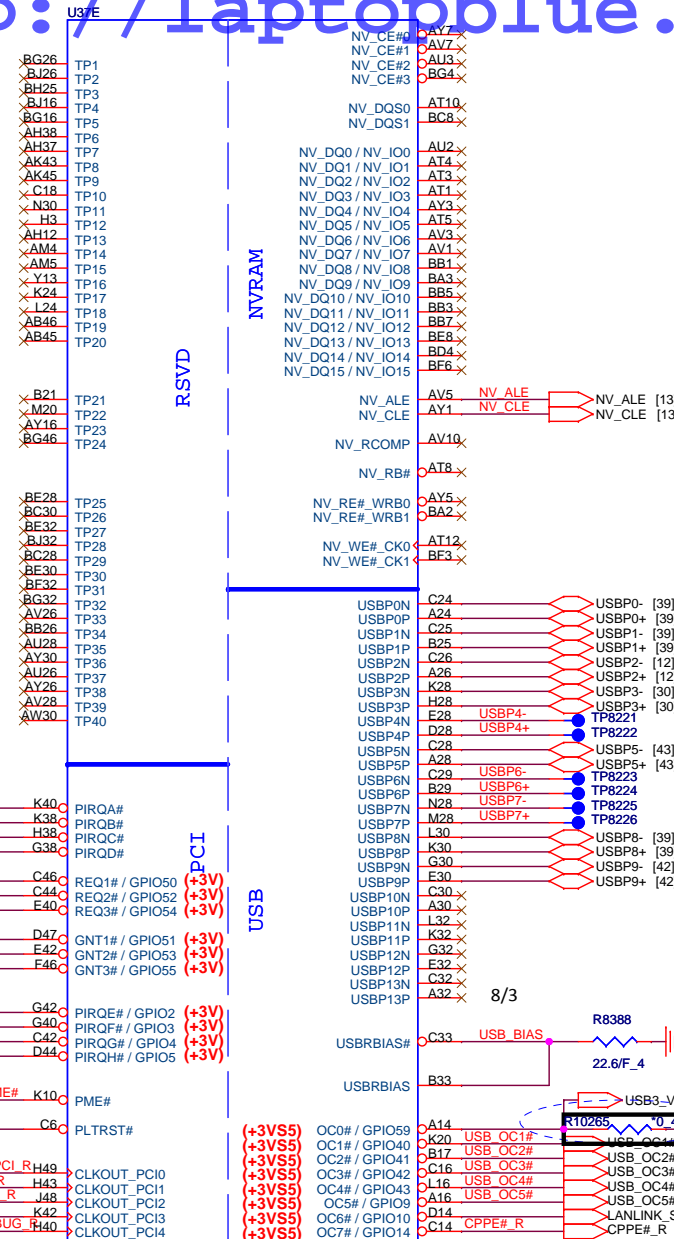


**WLAN/BT Option**

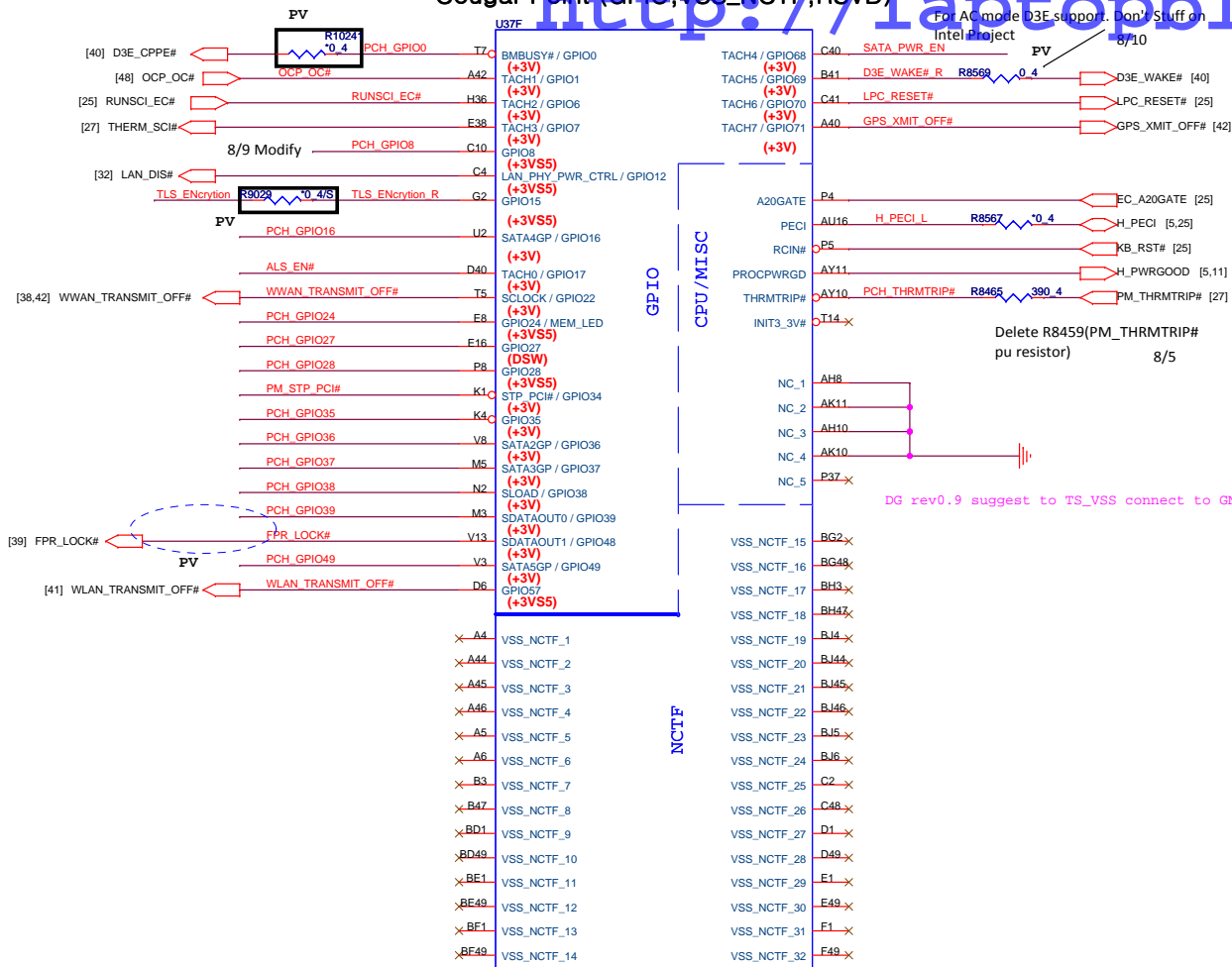


**PROJECT : F11**  
**Quanta Computer Inc.**

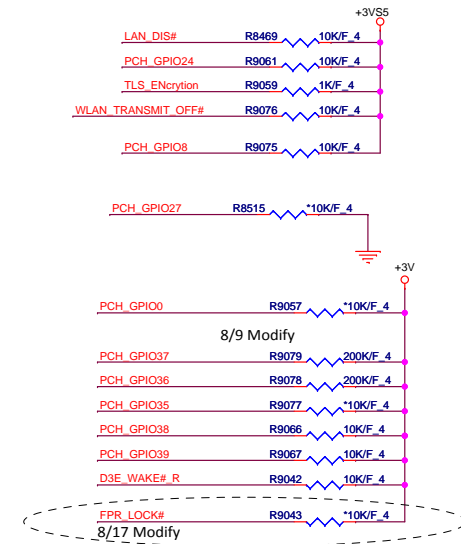
Size	Document Number	Rev
B	PCH 5/9 (PCI/USB/NVM)	1A
Date: Wednesday, January 19, 2011 Sheet 17 of 58		



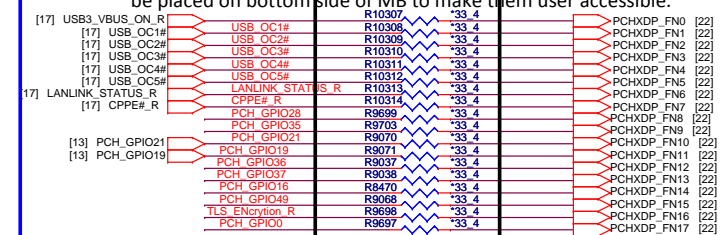
CougarPoint\_Rev\_0p7  
 fcbga989-intel-cougarpoint  
 AJQJN.F0T00  
 IC CTRL(989P)COUGARPOINT QNJF TOP B/S



## GPIO Pull-up/Pull-down(CLG)



Layout note: 33 and 0 ohm related to XDP connector should be placed in close proximity to each other. In addition, these should be placed on bottom side of MB to make them user accessible.

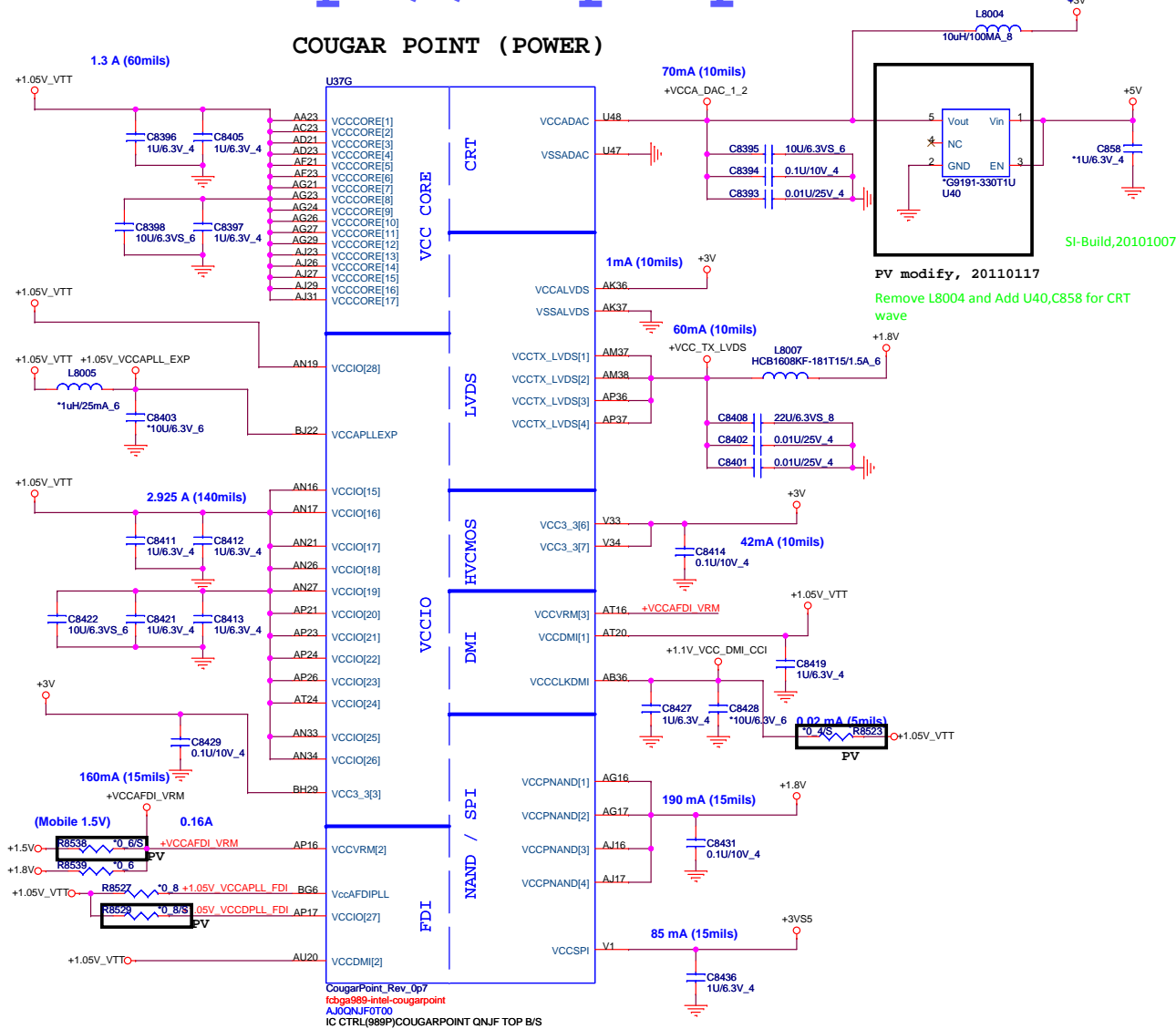


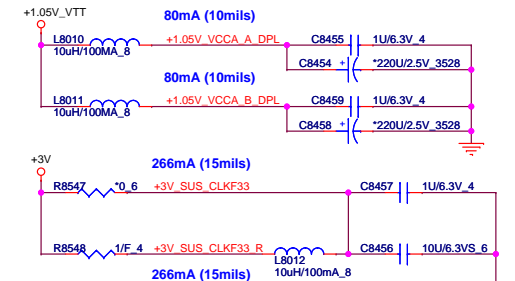
Place close to PCH within 1"

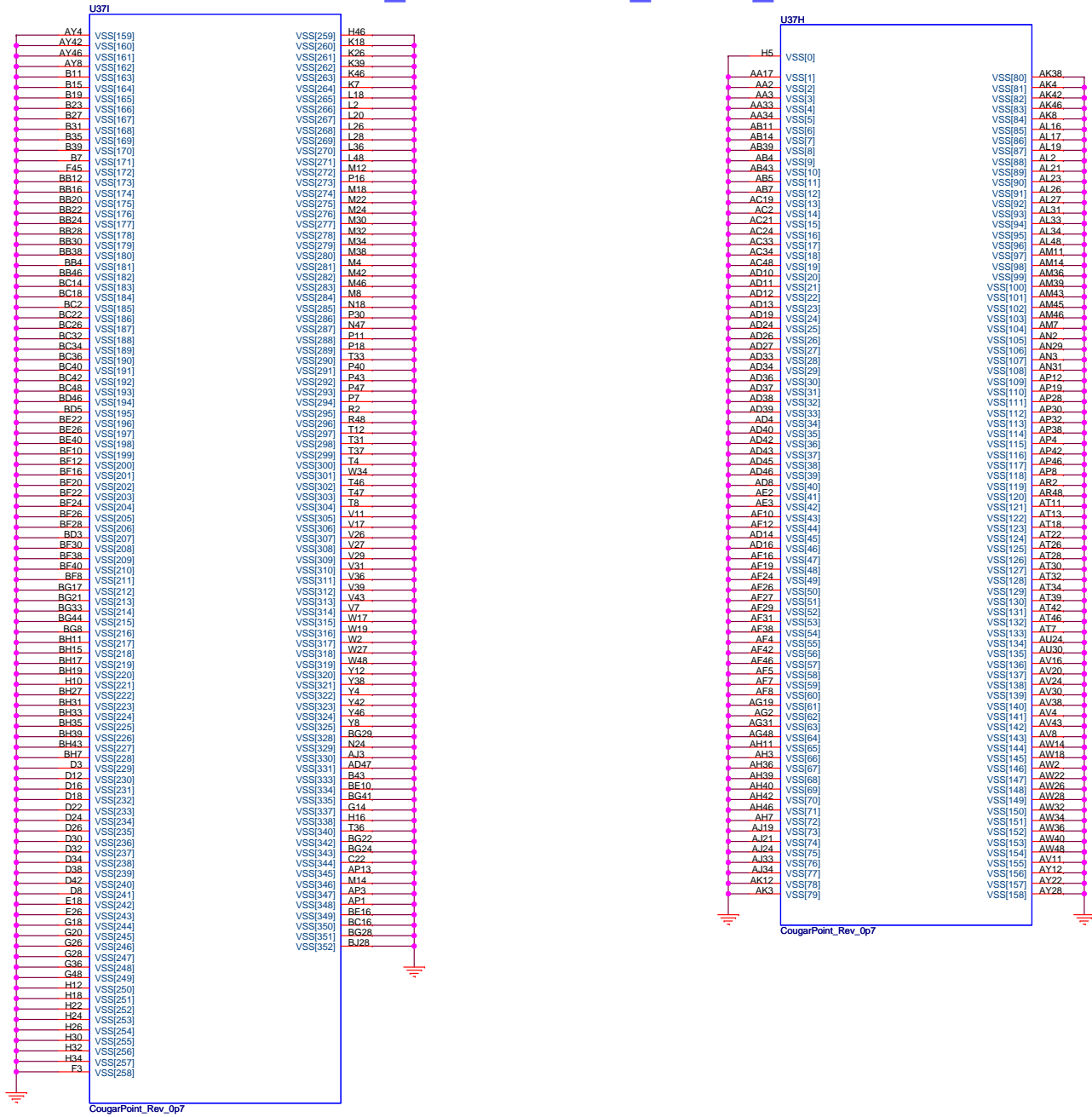
Remove from MV

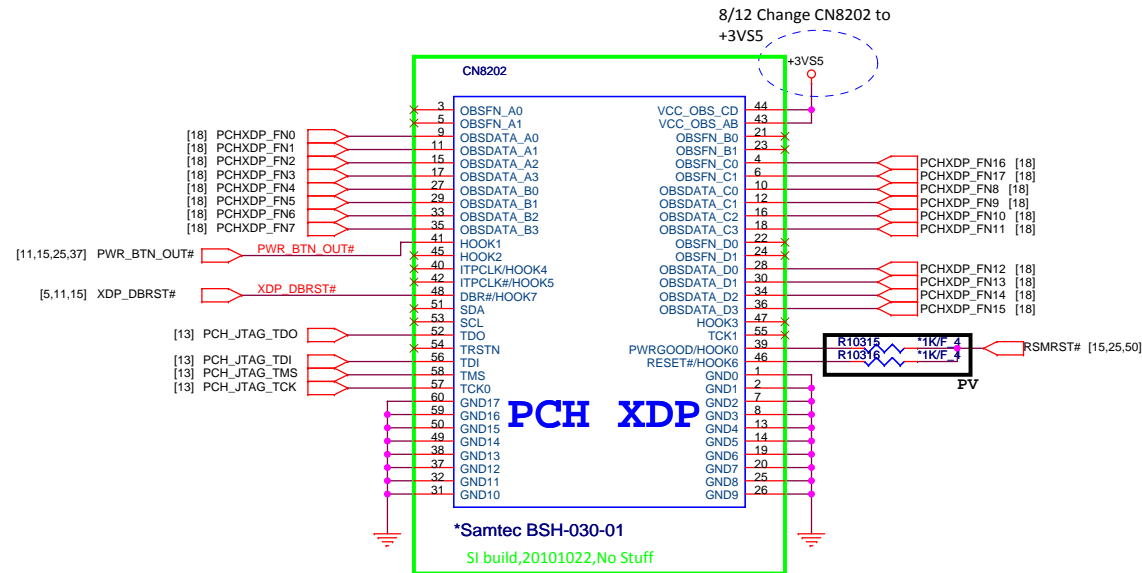
PV

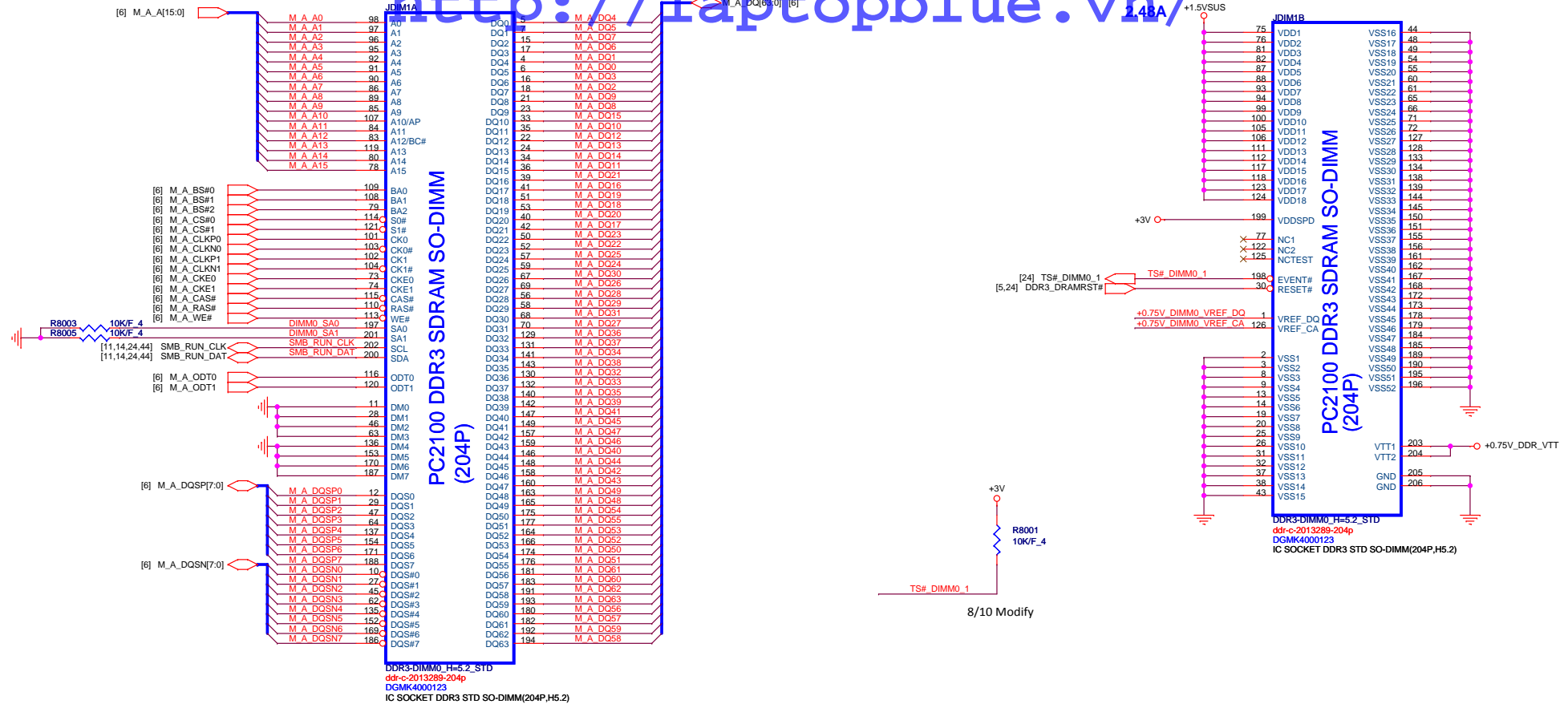
## COUGAR POINT (POWER)



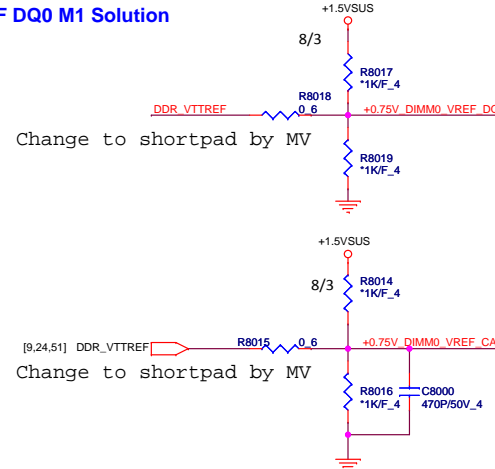




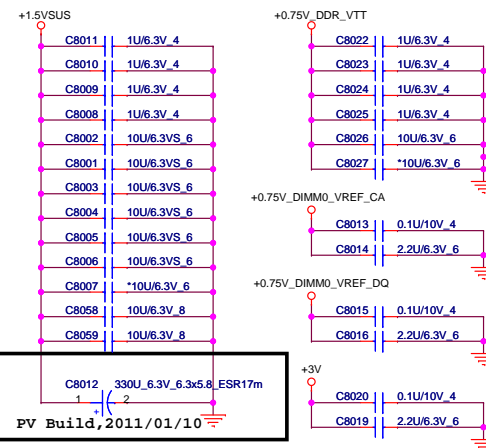




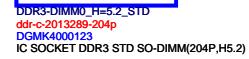
### VREF DQ0 M1 Solution



### Place these Caps near So-Dimm0.

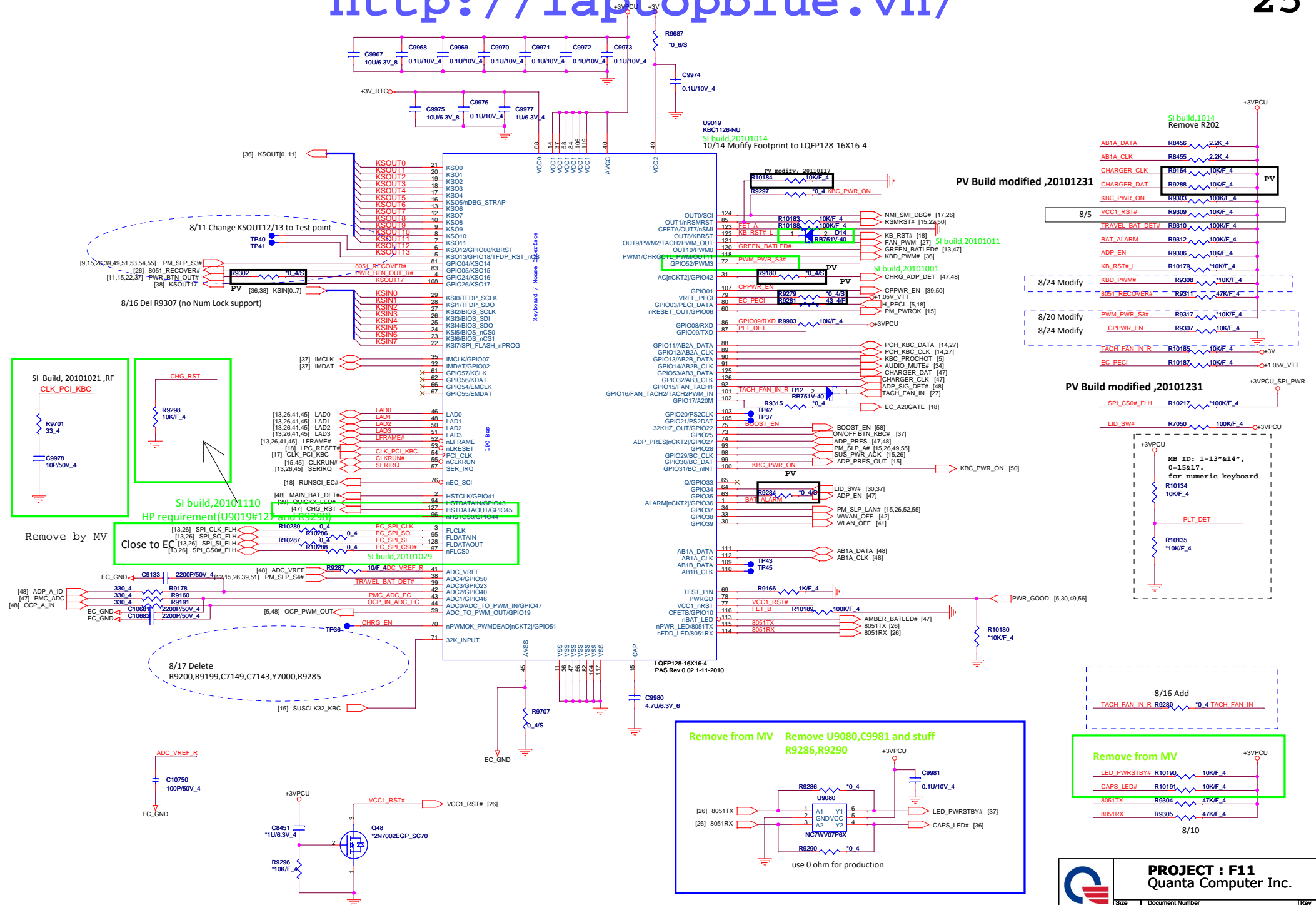




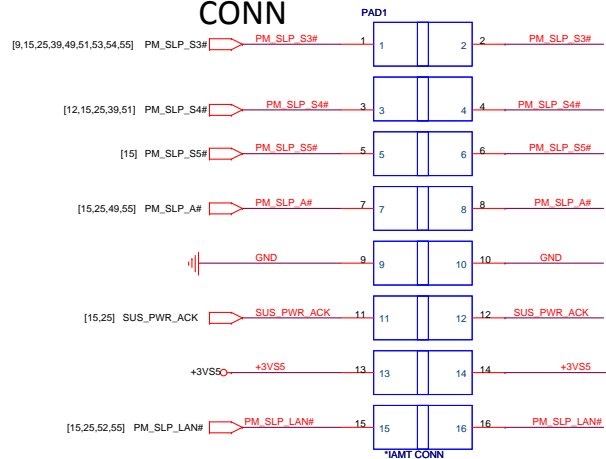


Size Custom	Document Number DDR3 DIMM1-STD (5.2H)	Rev 1A
Date: Wednesday, January 19, 2011		Sheet 24 of 58

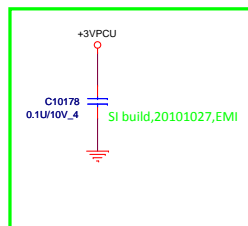




# AMT/ME COMPLIANCY TEST CONN

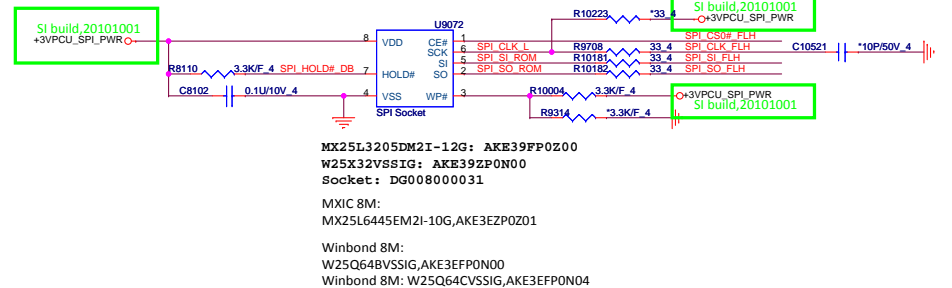


To place this on bottom side on M/B beneath door to make this user accessible. In addition, all signals should be routed within close proximity of each other (~10cm/4.5in)



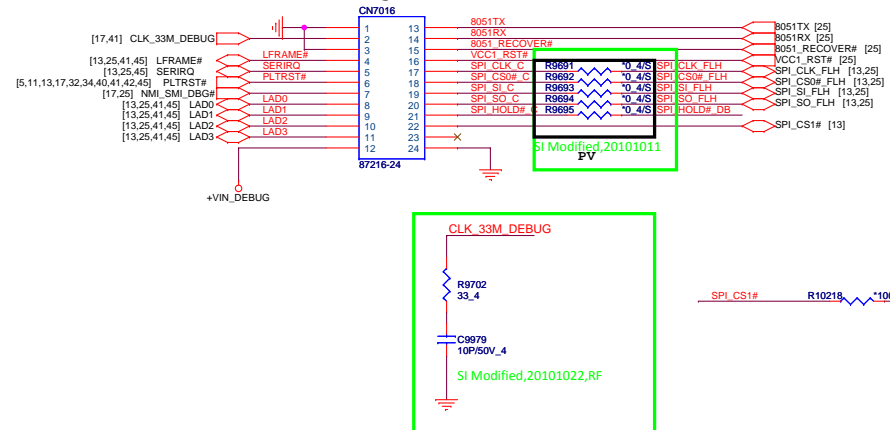
09/01 Modify

## SYSTEM SPI ROM SOCKET H=5.0

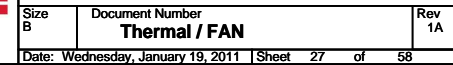


debug connector CN7016 within  
1" of both U9072 and KBC1126

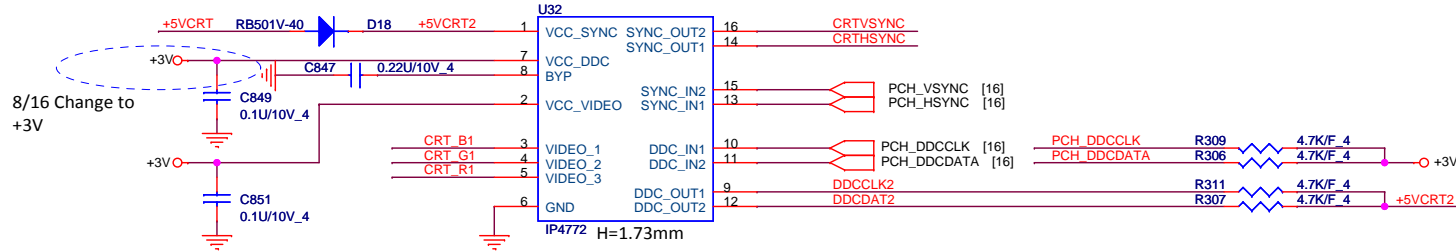
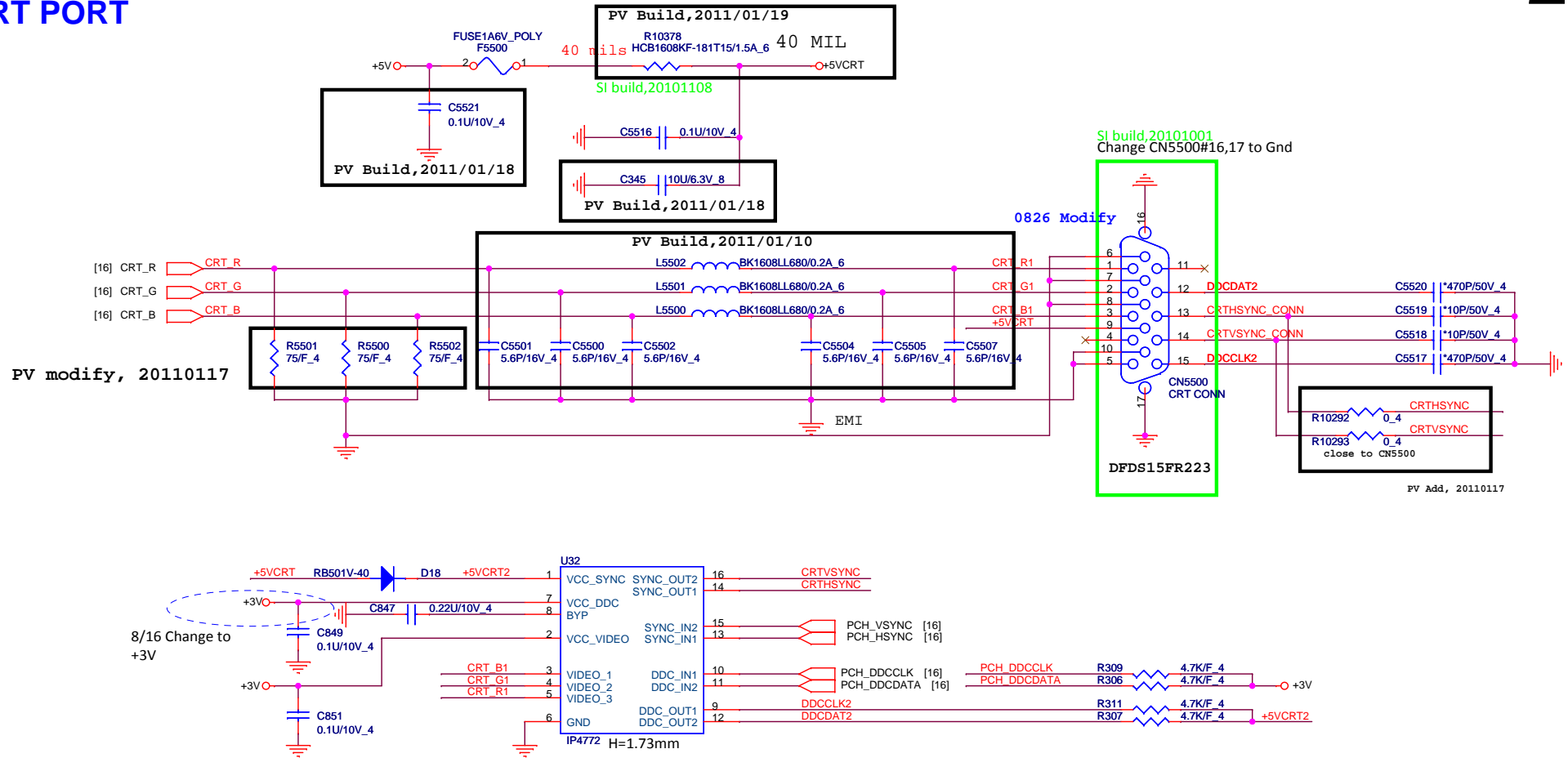
## For debug (BIOS)



NAND GATE  
KBC Control signal is low, Fan turn on



# CRT PORT



**PROJECT : F11**  
Quanta Computer Inc.

Size	Document Number	Rev
B	CRT	1A

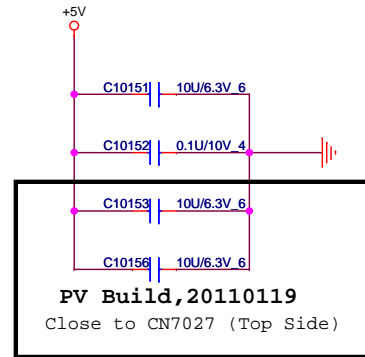
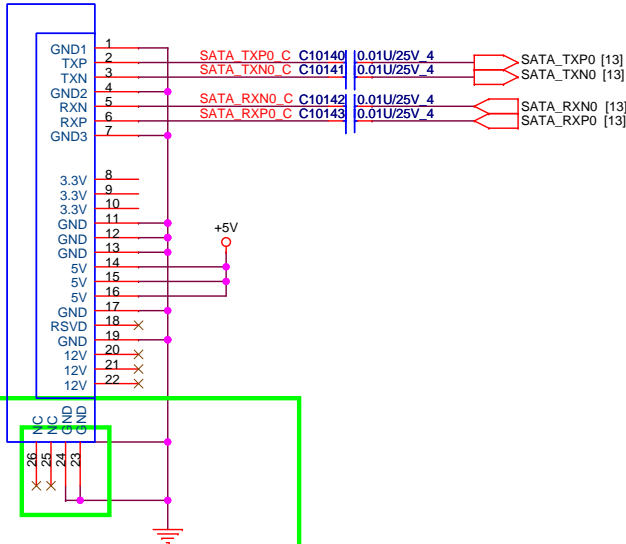
Date: Wednesday, January 19, 2011 Sheet 28 of 58

# SATA HDD CONNECTOR

<http://laptopblue.vn/>

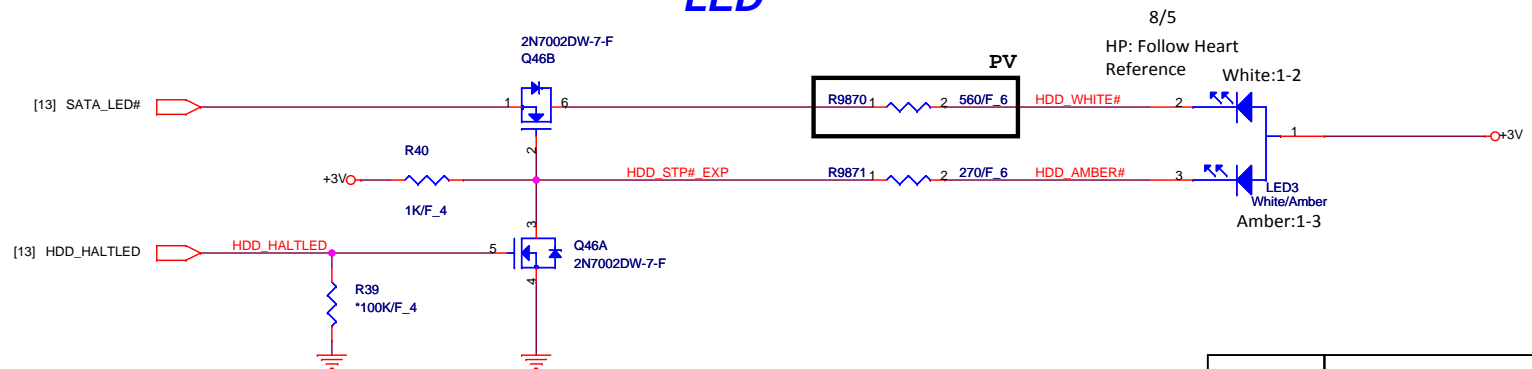
29

DFHD22MR015  
CN7027 LD2722F-SRLL6



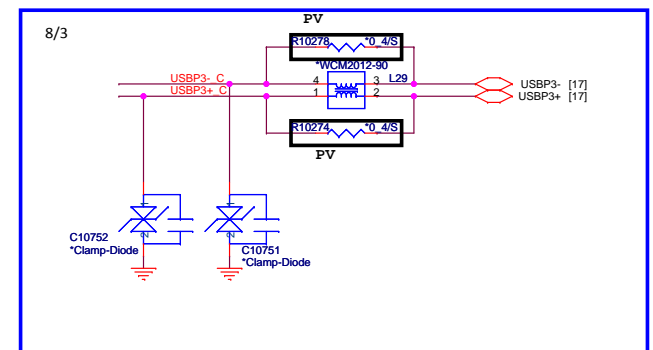
## LED


8/10

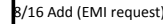
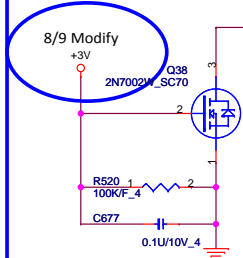
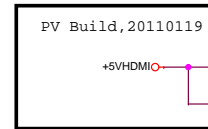


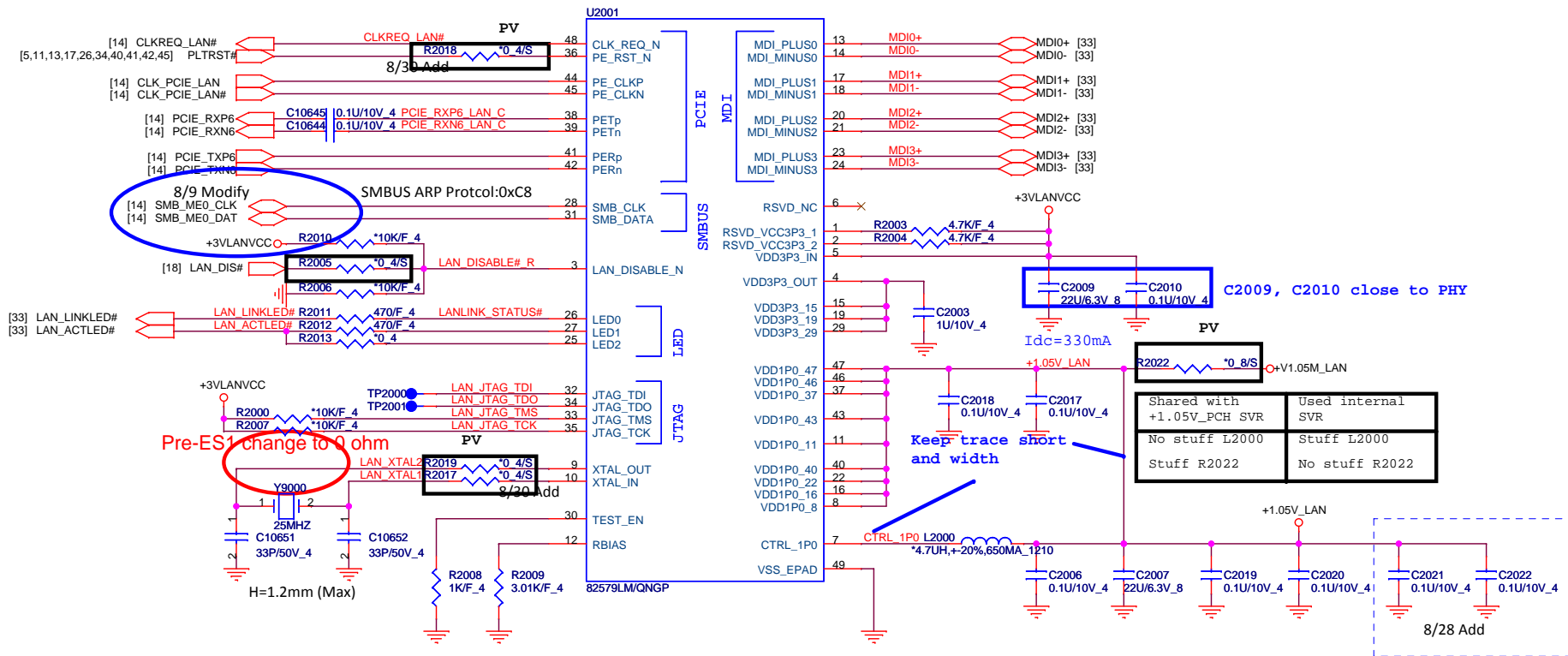
**PROJECT : F11**  
Quanta Computer Inc.

Size	Document Number	Rev
B	HDD/HDD LED	1A
Date: Wednesday, January 19, 2011	Sheet 29 of 58	

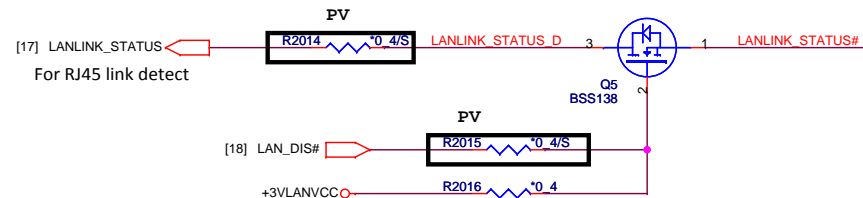


	<b>PROJECT : F11</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>LCD CONN/LID/CAM/DMIC</b>	Rev 1A
	Date: Wednesday, January 19, 2011   Sheet 30 of 58		





SI Build, 20101021, Stuff C2020,C2018.C2022,C2019,C2017-->RF

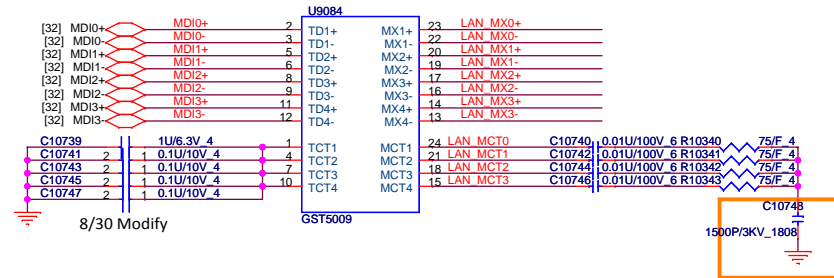


**PROJECT : F11**  
Quanta Computer Inc.

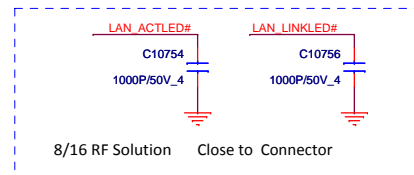
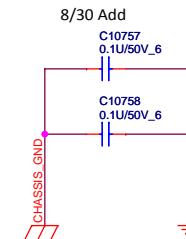
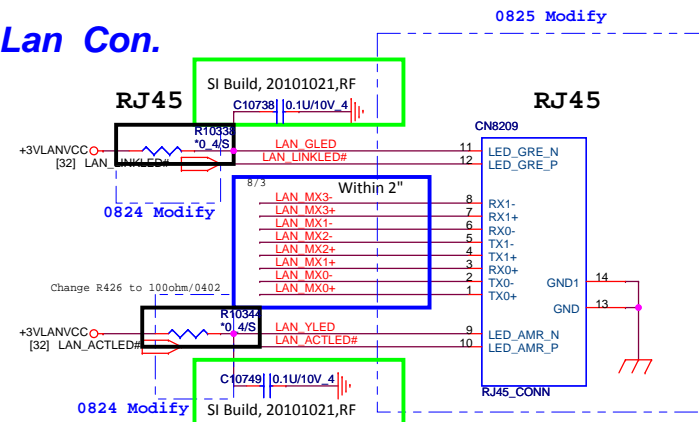
Size B	Document Number	Rev 1A
	Intel Lewisville 82579LM	
Date: Wednesday, January 19, 2011	Sheet 32 of 58	

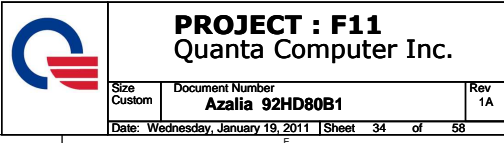


### Transformer for 10/100/1000



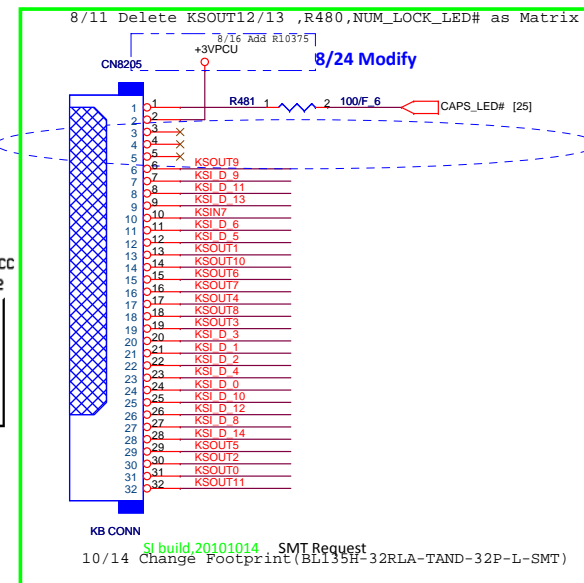
### Lan Con.



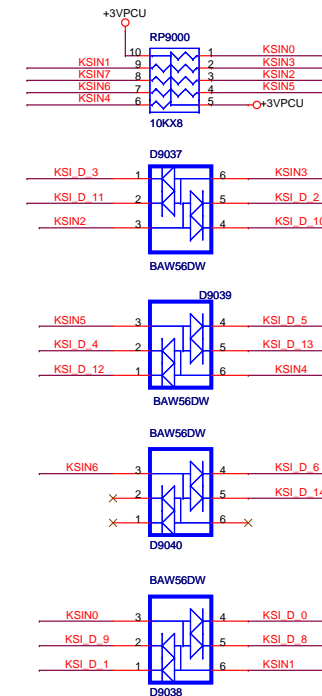




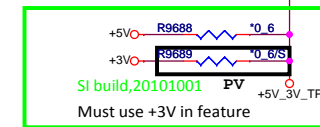
[25] KSOUT[0..11]  $\rightarrow$  KSOUT10..11  
[25..38] KSIN[0..7]  $\leftarrow$  KSIN0..7



KSI_JN(0)	24	46	47	48	133	42	21	22	53	54	29	43	
KSI_JN(1)	21	17	18	19	125	26	20	23	24	25	76	129	
KSI_JN(2)	22	31	32	33	117	40	5	8	38	39	13	27	
KSI_JN(3)	20	2	3	4	80	11	34	37	9	10	120	121	
KSI_JN(4)	23	1	30	110	75	12	50	51	81	14	89	123	
KSI_JN(5)	12	114		112	84	28	35	36	86	127	79	15	
KSI_JN(6)	11	113	115	16	61	119	49	52	118	56	85	122	
KSI_JN(7)	10	45		116	131	55	6	7	41	126	132	83	
KSI_JN(8)	27											44	
KSI_JN(9)	7											57	
KSI_JN(10)	25											60	
KSI_JN(11)	8											62	
KSI_JN(12)	26											59	
KSI_JN(13)	9											64	
KSI_JN(14)	28											58	
		31	13	30	19	17	29	15	16	18	6	14	32
		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)



Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	Right
Pin6	Left

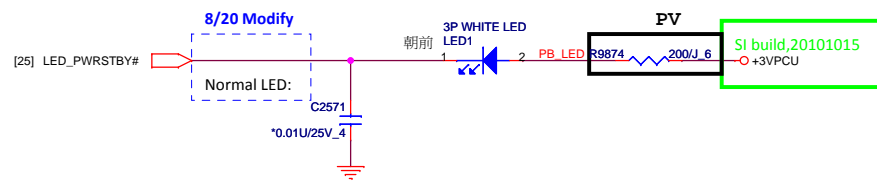
TOUCH PAD CONN  
C10

Must use +3V in feature



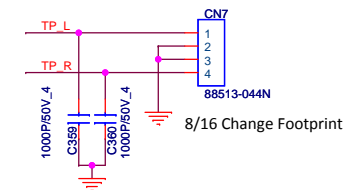
Close to BEAD

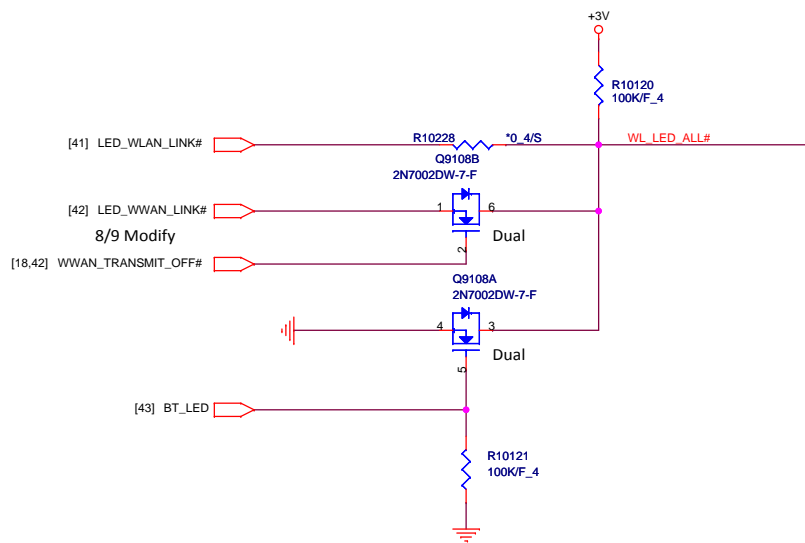
**PWR LED**



SI build,20101001

***TOUCH PAD SW CONN***





## Function Board(Mute/Quickweb/Wireless)

### KSIO (MUTE)

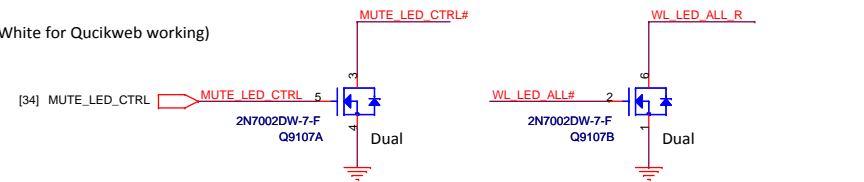
Mute LED: Amber when  
Mute(Single Color)

### KS1 (WIRELESS)

Dual Color (White/Amber)  
Wireless LED: Wireless ON(White) and Wireless OFF(Amber)

### KS13 (QUICKX)

Quickweb LED: (White for Qucikweb working)

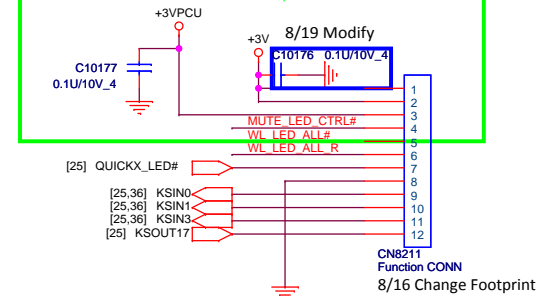


SI build,1001

Change CN8211#3 to +3VPCU  
from MUTE\_LED\_CTRL due  
QUICKX\_LED# power source  
change to +3VPCU , Also add  
C10177 and close to CN8211

SI build,20101001

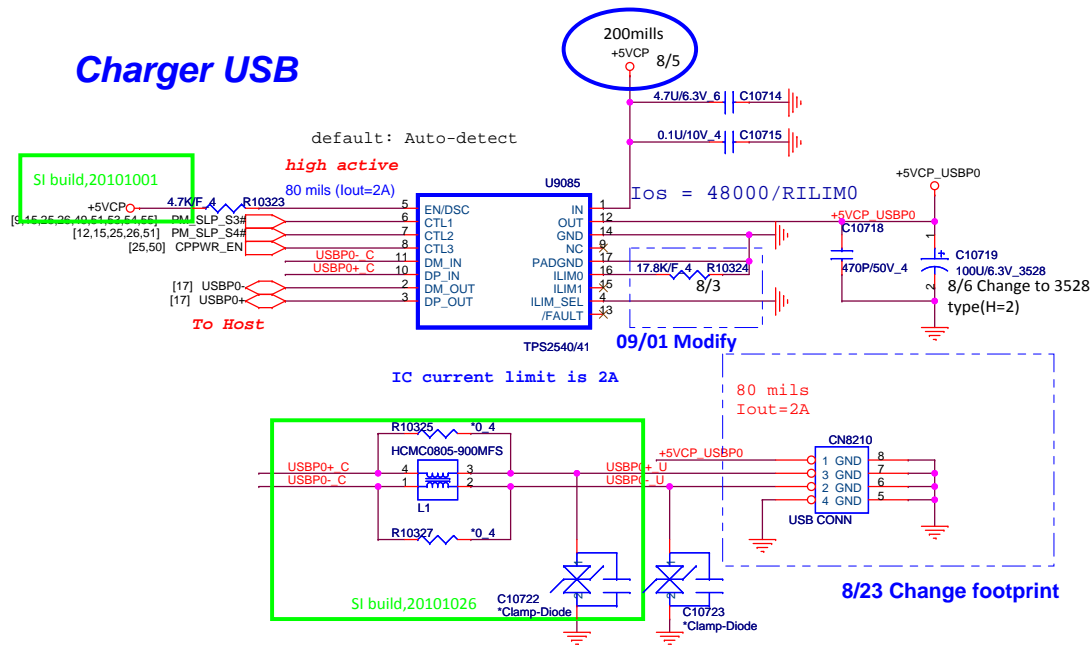
8/19 Modify



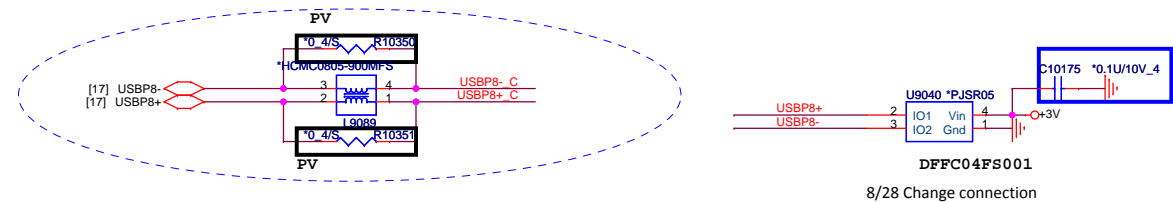
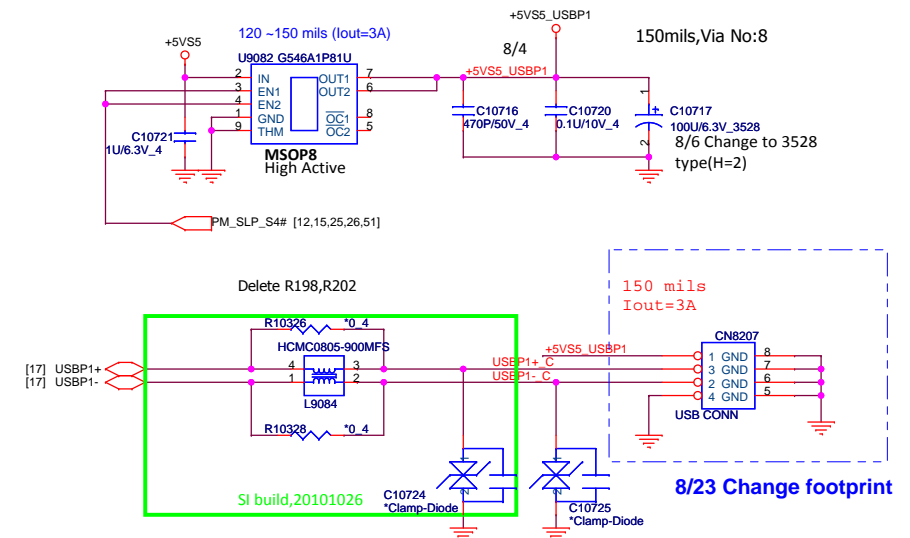
**PROJECT : F11**  
Quanta Computer Inc.

Size Custom	Document Number <b>FUNCTION BOARD</b>	Rev 1A
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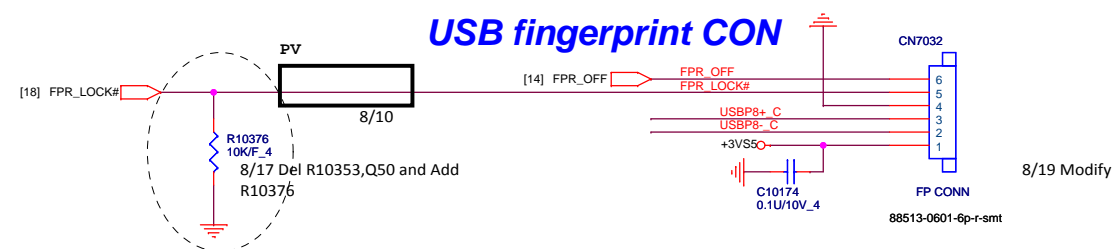
## Charger USB

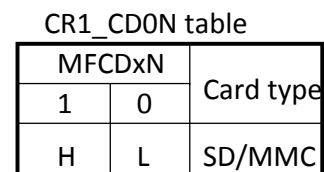


## Powered USB



CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated Charging Port,Auto
X	1	0	Standard Downstream Port ,USB 2.0
1	0	0	Dedicated Charging Port, BC Specification 1.1
1	0	1	Dedicated Charging Port, Apply
1	1	1	Only Downstream Port, BC Specification 1.1

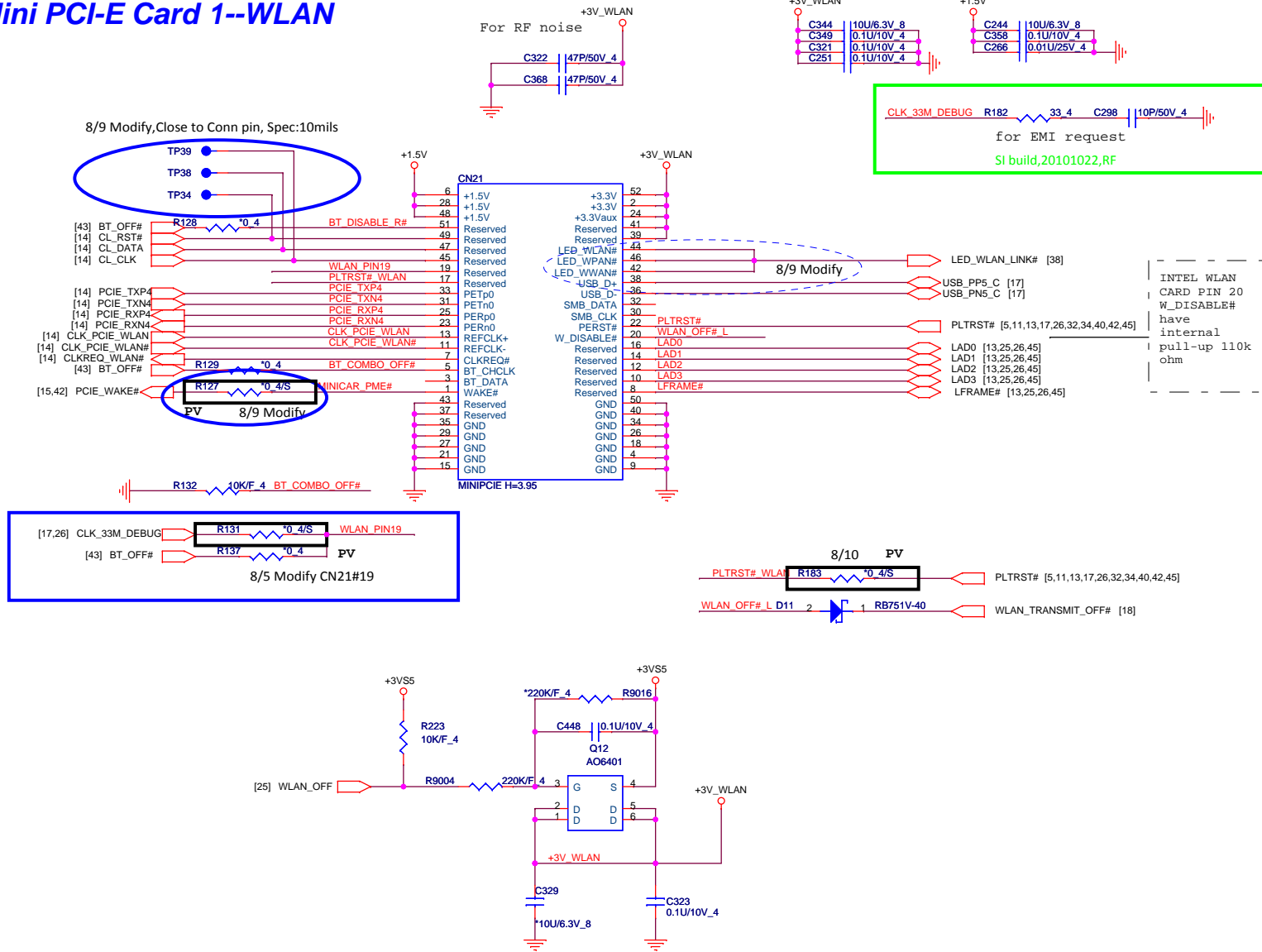




MDIF		MMC
00	SD	
00	D0	D0
01	D1	D1
02	D2	D2
03	D3	D3
04	CMD	CMD
05	CLK	CLK
06	WP	WP

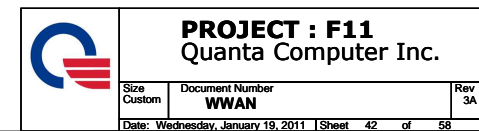
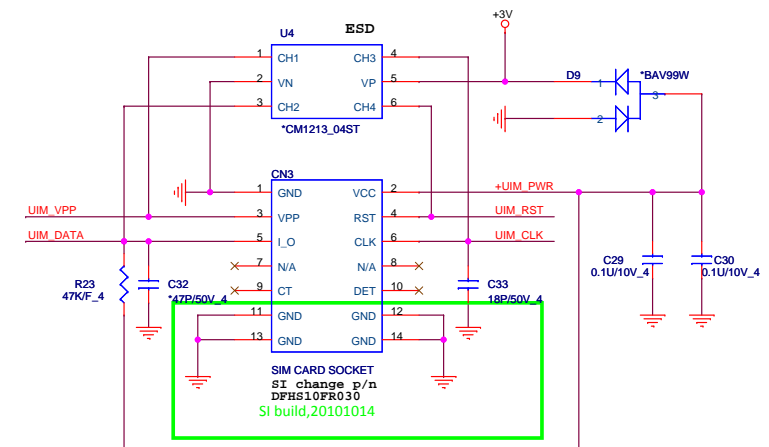


# Mini PCI-E Card 1--WLAN



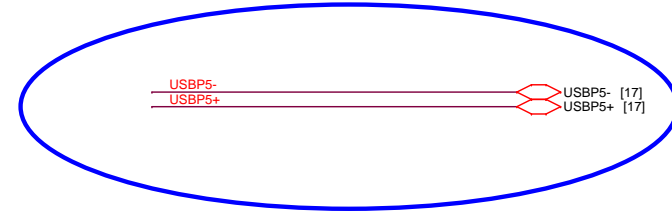
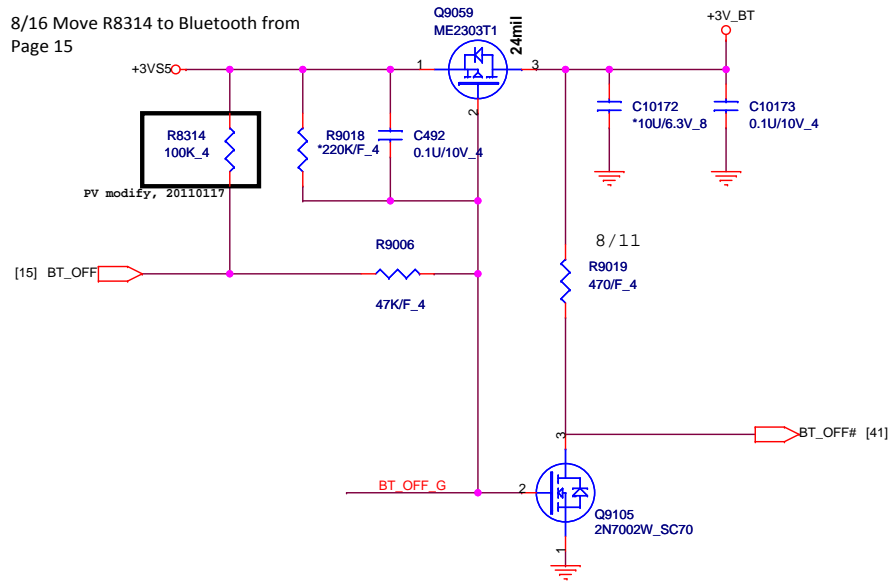
Quanta  
Debug Card:

Pin16,14,12,10,8,19,17

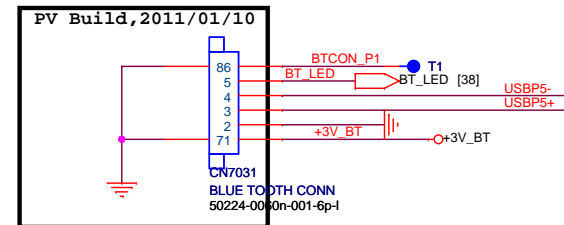


BLUETOOTH

8/16 Move R8314 to Bluetooth from  
Page 15



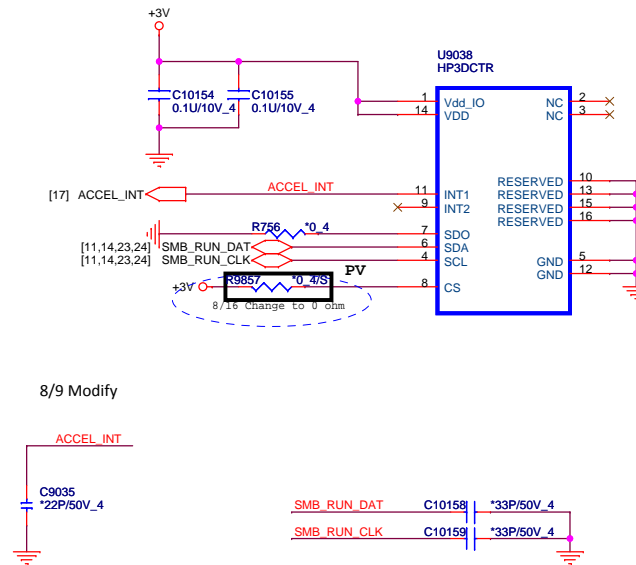
Remove L9081,R10347,R10346 by PV Build  
PV Build,2011/01/18

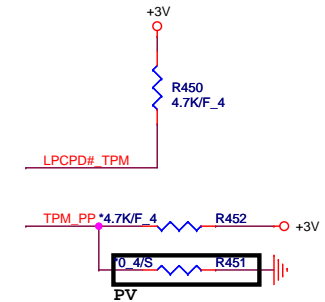
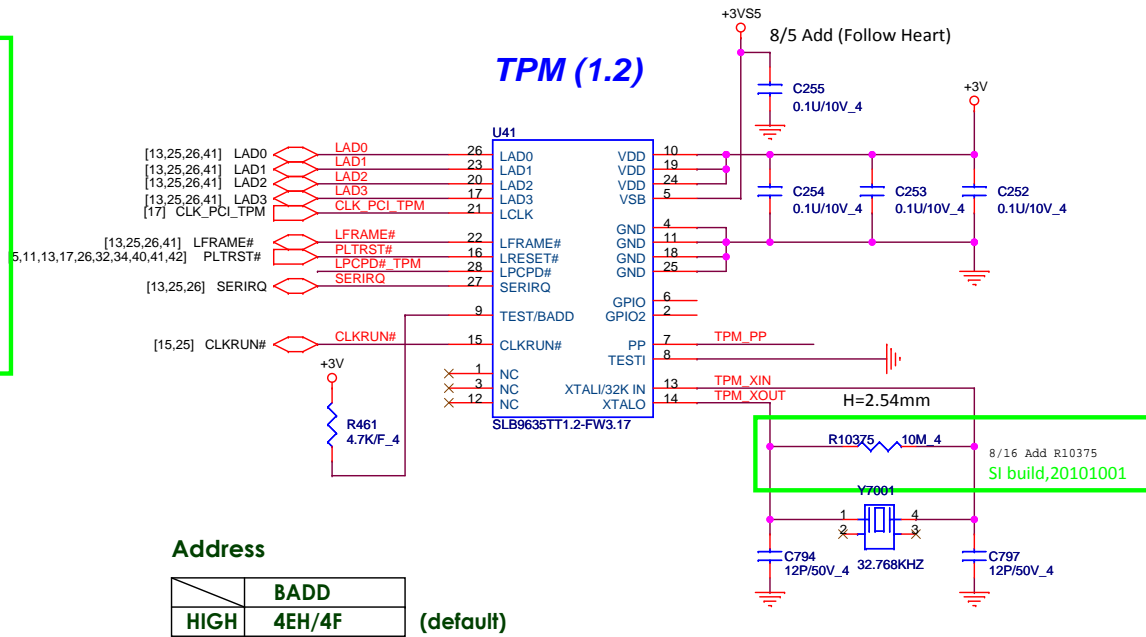
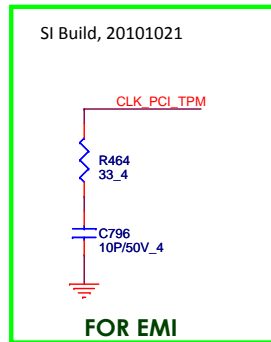


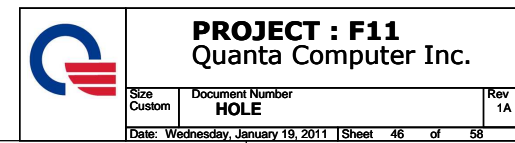
**PROJECT : F11**  
**Quanta Computer Inc.**

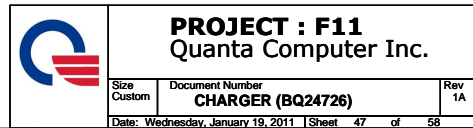
Size B	Document Number <b>LCD CONN</b>	Rev 1A
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### Accelerometer Sensor



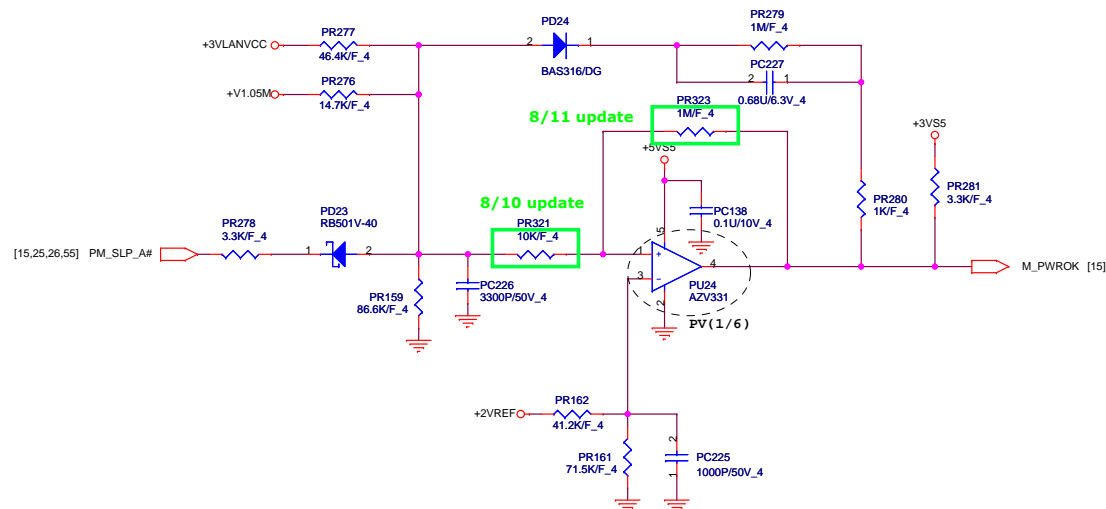










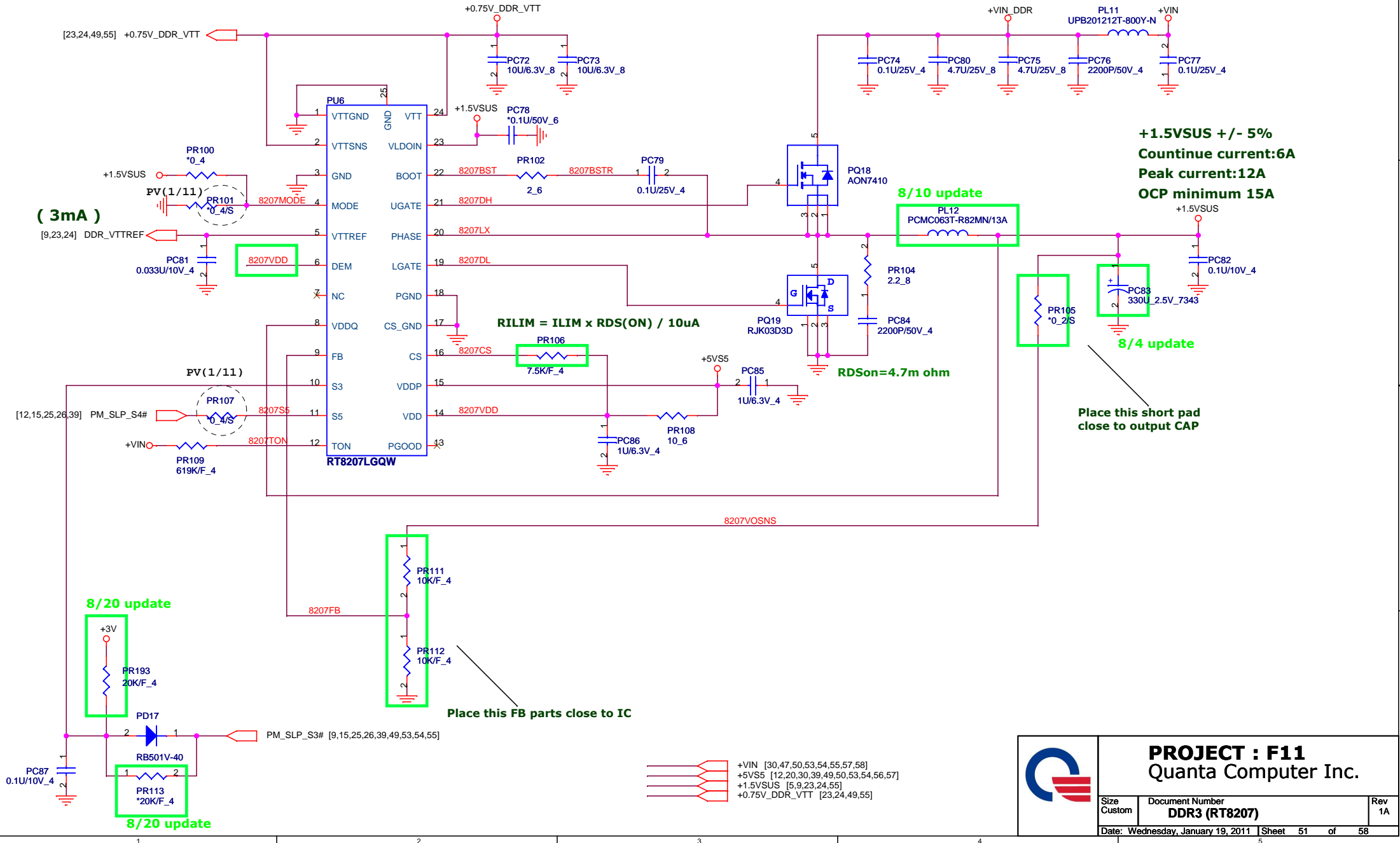


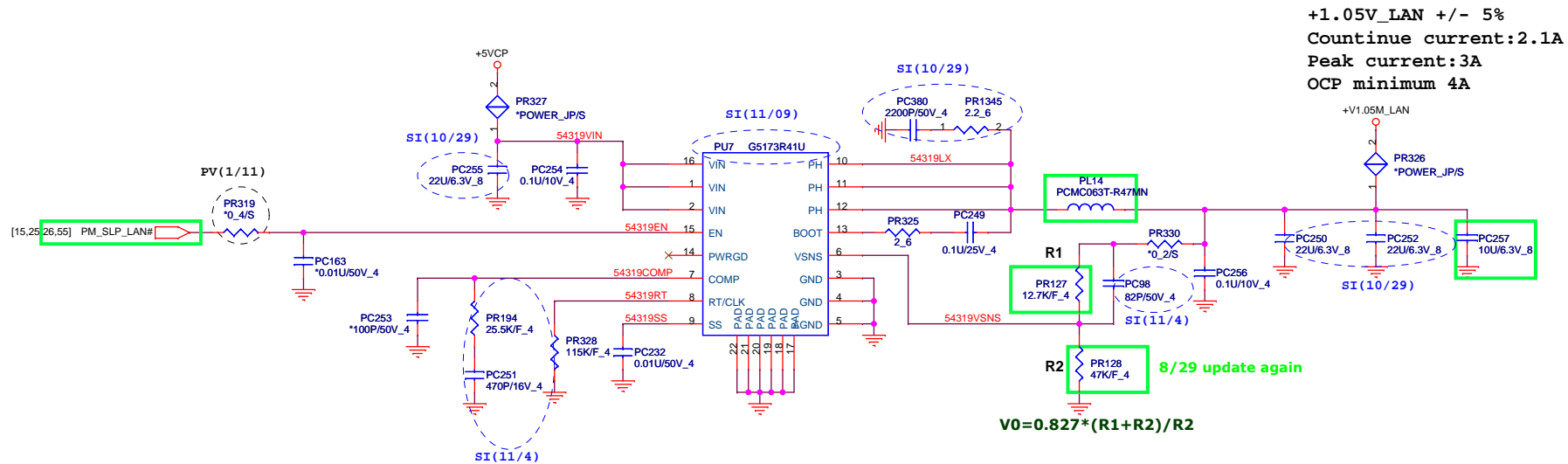
**PROJECT : F11**  
Quanta Computer Inc.

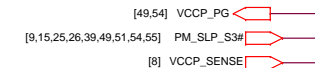
Size Custom	Document Number <b>CHARGERII</b>	Rev 1A
Date: Wednesday, January 19, 2011 Sheet 49 of 58		

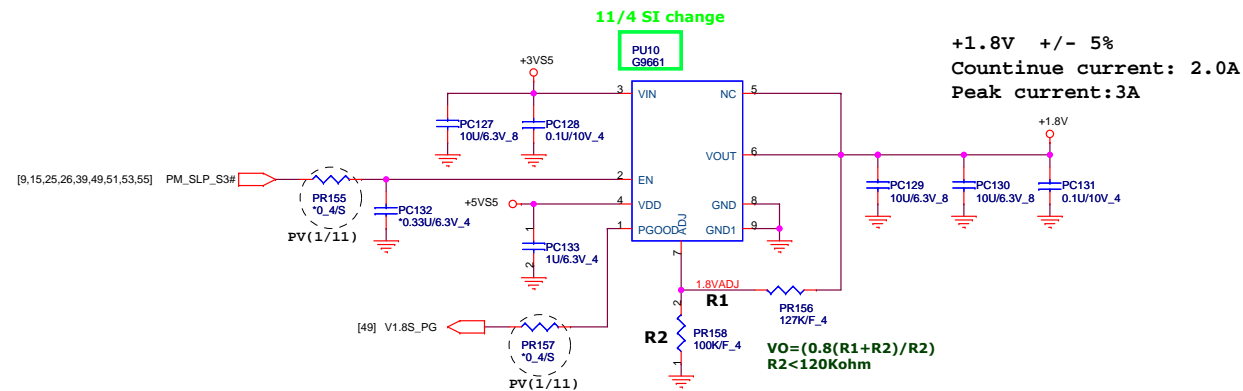
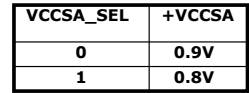
VS5 PD19 BAS316/DG PR164 PV17/11  
 EVIN 0.2 1 0.23PVRIN 0.4/S

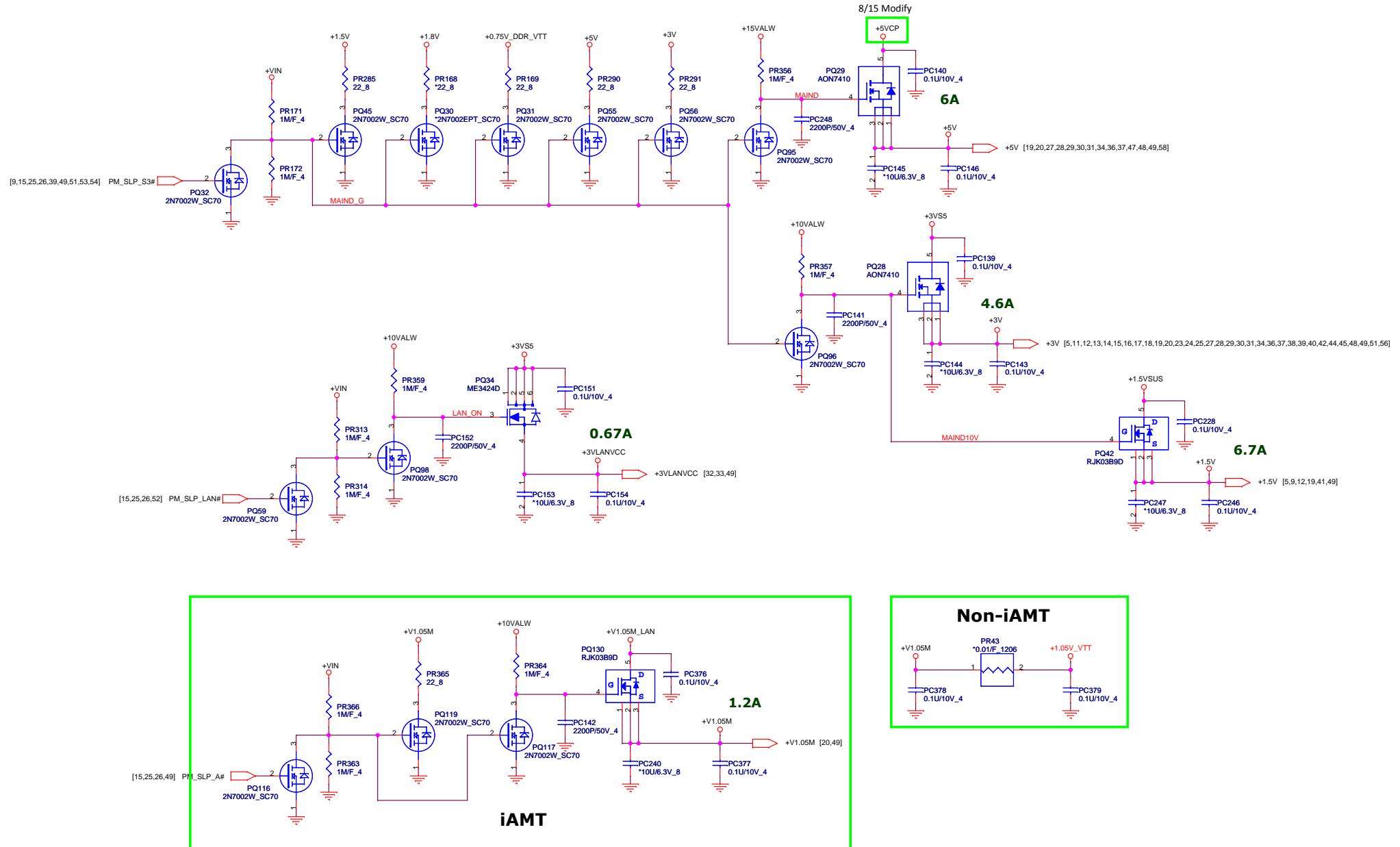












<http://laptopblue.vn/>

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- Alert trace routing (between data and clock trace)
- Refer to ground
- Keep out 20 mils

**Key Components and Connections:**

- Vcore Regulation:** Includes a feedback network with PR173, PR174, PR175, and PC229. A DB2 update is noted for the feedback capacitor.
- Vgt Regulation:** Features a feedback network with PR176, PR177, PR178, and PC157. A DB2 update is noted for the feedback capacitor.
- Current Sense:** IMON and IMONA pins are connected to current sense resistors (PR239, PR240) and capacitors (PC179, PC180).
- Output Stages:** The 2-phase/3-phase output section includes CSNA, CSPPA, CSSMA, and CSCOMPA pins, connected to various capacitors and inductors.
- Protection and Monitoring:** Pins like VSP, TSENSEA, and DROOPA are connected to monitoring circuitry.

2phase/3phase option			
	PR379, PR382	PR357, PR393	PC329
2phase	POP	NA	Change to 0ohm

UMA(Switchable)/Discrete Only option		
PC336, PC340 PC343, PC337 PC342	PR427, PR433, PR430, PR431, PR423, PR435 PC338, PR424, PR428, PR432, PC339, PC341 PR425, PR426, PR429, PR420, PR422, PR380 PR399, PR421, PC352, PR417, PR418, PC354	PR434, PR436 PR378

2phase/3phase option			
	PR379,PR382	PR357,PR393	PC329
2phase	POP	NA	Change to 0ohm

UMA(Switchable)/Discrete Only option			
	PC336,PC340 PC343,PC337 PC342	PR427,PR433,PR430,PR431,PR423,PR435 PC338,PR424,PR428,PR432,PC339,PC341 PR425,PR426,PR429,PR420,PR422,PR380 PR399,PR421,PC352,PR417,PR418,PC354 PC419	PR434,PR436 PR378
UMA	POP	POP	NA
Discrete	Change to 0 ohm	NA	POP



**PROJECT : F11**  
Quanta Computer Inc.

Size Custom	Document Number <b>CPU Core1 (NCP6131S)QC</b>
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