Compal Confidential

VAWGA/B Schematics Document

AMD "Kabini" Platform

AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun

LA-9911P REV: 1.0

2013-04-01

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date	2015/04/22	Title: COVER PAGE
Size: B	Document Number: VAWGA/GB			Rev: 1.0
Date: Monday, April 01, 2013	Sheet 1 of 48			

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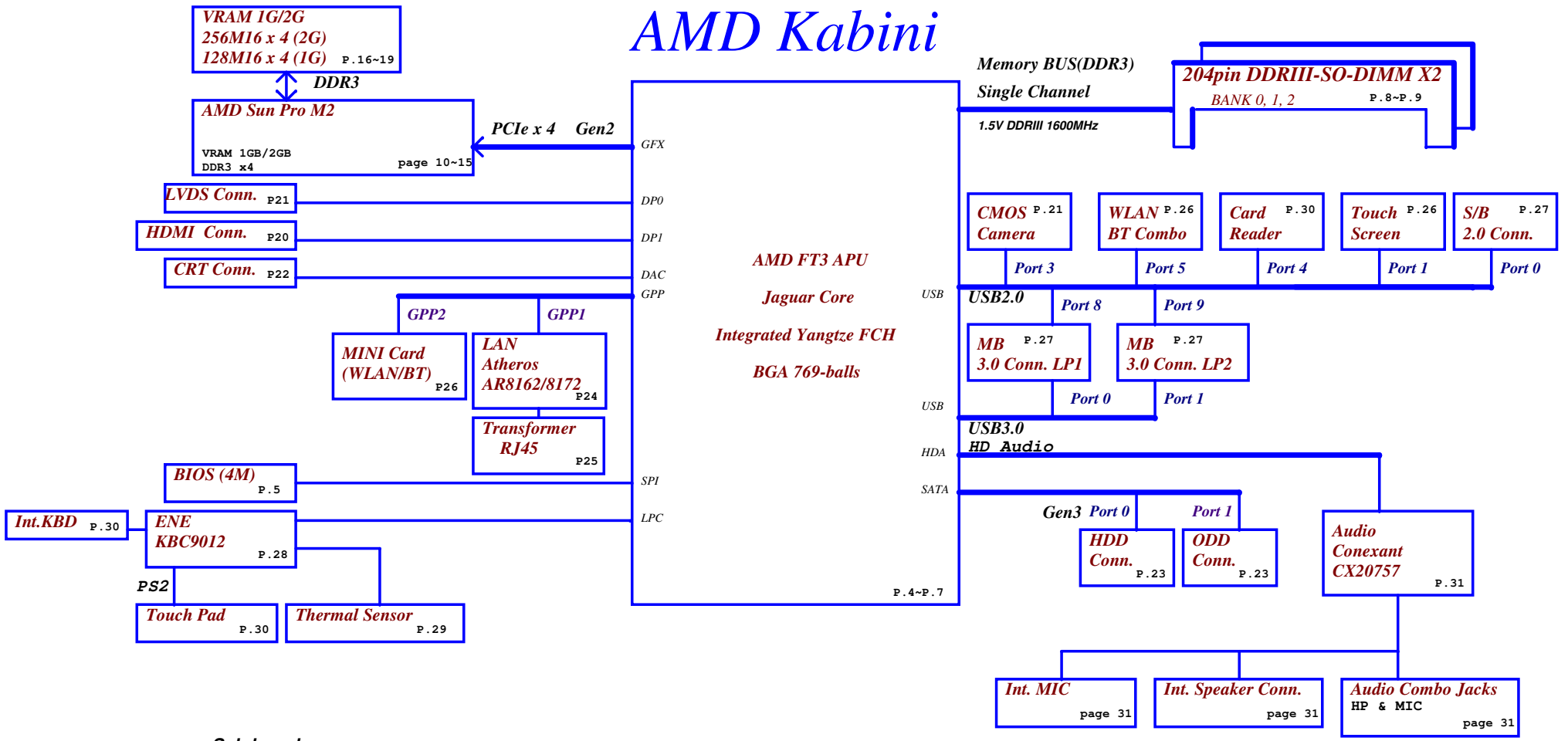
Model Name : VAWGA/B



Sub-borad

15"

14"

- IO/B LS9633P page 30
- ODD/B LS9634P page 23
- Power/B LS9631P page 30
- LED/B LS9635P page 30
- USB/B LS9632P page 27

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: BLOCK DIAGRAMS

Size: B | Document Number: VAWGA/GB | Rev: 1.0

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.5VGS	1.5V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB OC MAPPING

OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

BOM Structure Table

BOM Structure	BTO Item
A6@	A6 R3 BGA APU
A4@	A4 R3 BGA APU
E2@	E2 R3 BGA APU
E1@	E1 R3 BGA APU
E1PC@	E1 PC BGA APU
X4@	X4 ES2 BGA APU
X5@	X5 ES2 BGA APU
X2@	X2 ES2 BGA APU
EMICU@	CardReader EMI Un pop
EMICP@	CardReadear EMI pop
EMIUSB2RU@	Right USB2.0 port EMI un pop
EMIUSB2RP@	Right USB2.0 port EMI pop
USB2R@	Right USB2.0 port component
SUN@	SUN PRO GPU (R3 compal part)
MARS@	MARS XT GPU (R1 compal part)
14@	for 14" componect
15@	for 15" componect
PX@	Common VGA circuit
CMOS@	CMOS Camera part
HDMI@	HDMI part
EMIGASP@	Gastube
8162@	Ateros AR8162 LAN Chip
8172@	Ateros AR8172 LAN Chip
SWR@	LAN Switching mode
LDO@	LAN LDO mode
THERMAL@	Lenovo Thermal Sensor
ME@	ME part
UMA@	UMA part
@	Unpop
ZODD@	Zero Power ODD part
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

USB Port Table

USB 2.0	USB 3.0		Port	3 External USB Port
			0	RIGHT USB
			1	Touch Screen
			2	
			3	Camera
			4	CardReader
			5	WLAN/BT Combo
			6	LEFT USB (for colay)
			7	LEFT USB (for colay)
	XHCI	0	8	LEFT USB3.0
		1	9	LEFT USB3.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date 2015/04/22	Title: NOTES LIST
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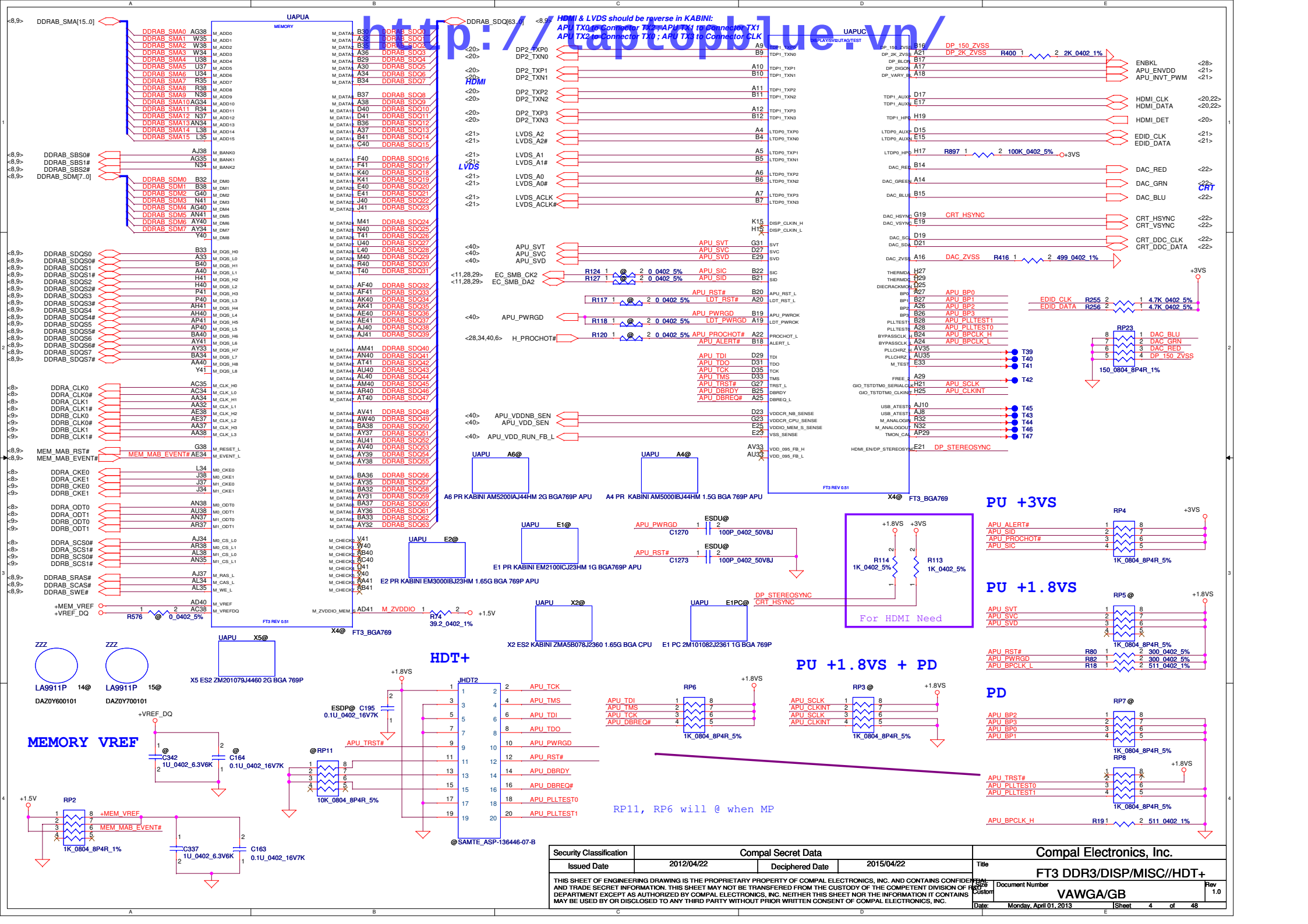
Date: Monday, April 01, 2013	Sheet 3 of 48		



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	FT3 DDR3/DISP/MISC//HDT+
Size: B25 Custom	Document Number: VAWGA/GB
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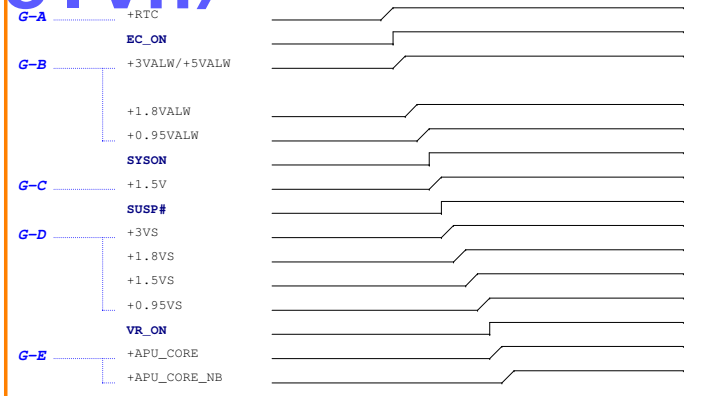
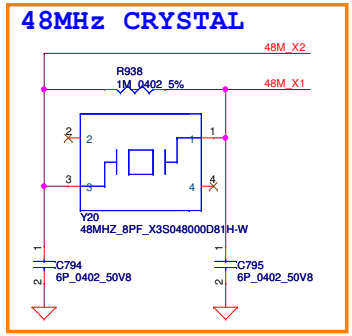
Date: Monday, April 01, 2013	Sheet 4 of 48

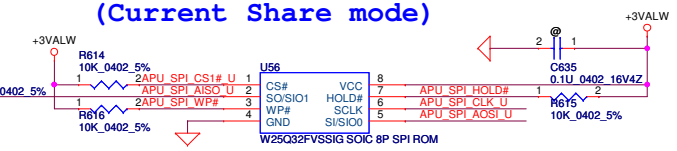
APU POWER SEQUENCE



48MHz CRYSTAL



4MB SPI ROM (Current Share mode)



R103 R104 for EMI

R109,R110,R111 close to APU

R108 close to ROM

APU->EC->ROM must route as Daisy Chain for Share ROM quality (RP12 was request to added for the recoverable solution as original method--backup)

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Compal Electronics, Inc.

Title: FT3 PCIE/SATA/CLK/USB/SPI

Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

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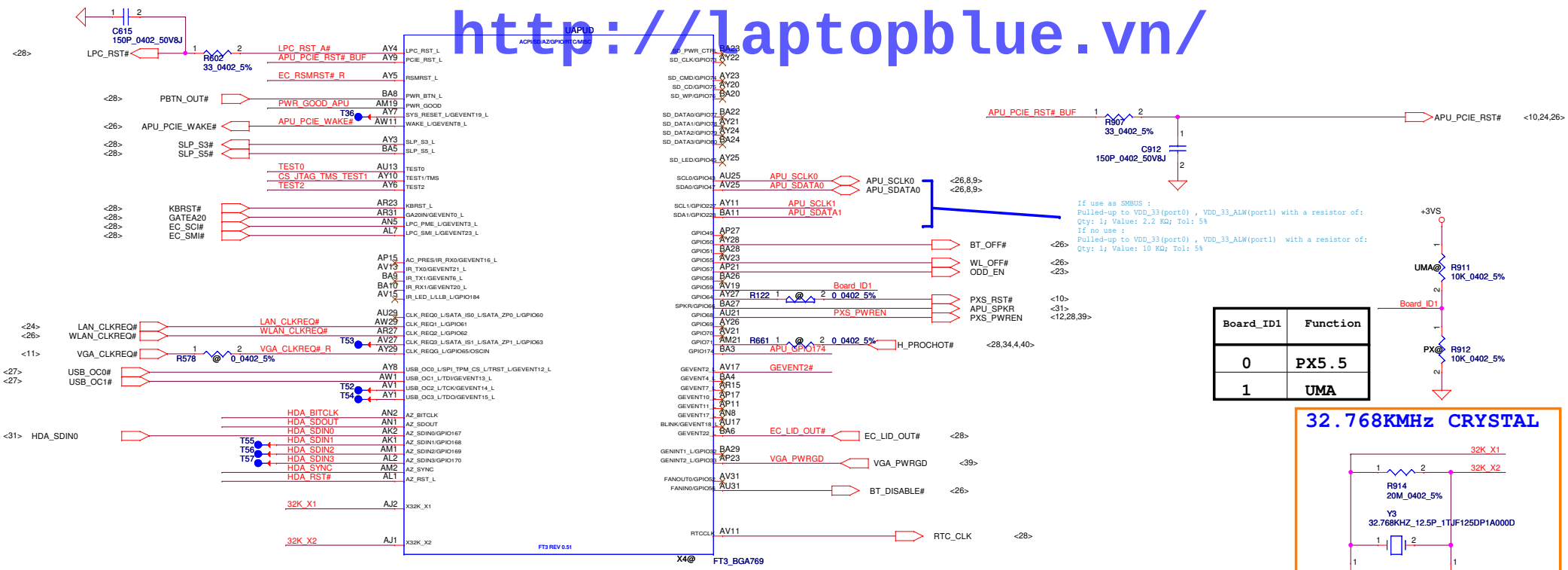
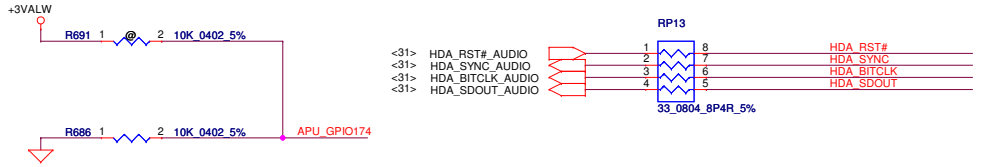


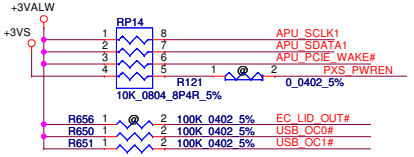
Board_ID1	Function
0	PX5.5
1	UMA

32.768KMHz CRYSTAL

PU +3VALW + PD

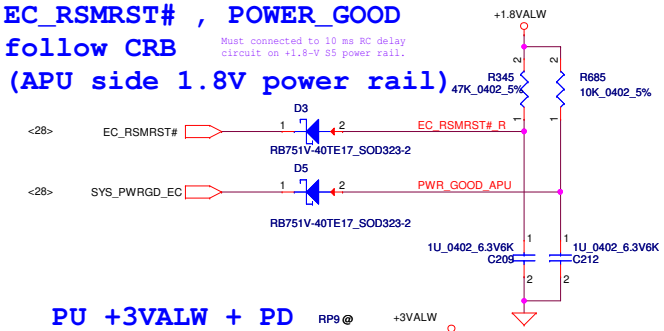


PU +3VALW

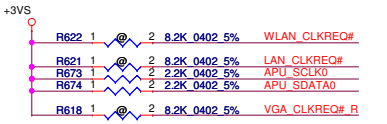


EC_RSMRST# , POWER_GOOD follow CRB (APU side 1.8V power rail)

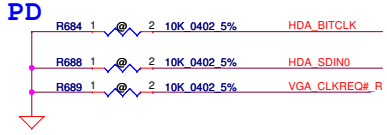
Must connected to 10 ms RC delay circuit on +1.8-V S5 power rail.



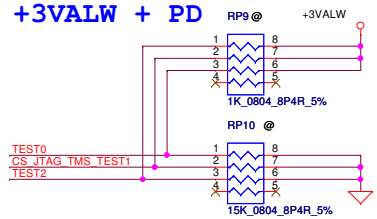
PU +3VS



PD

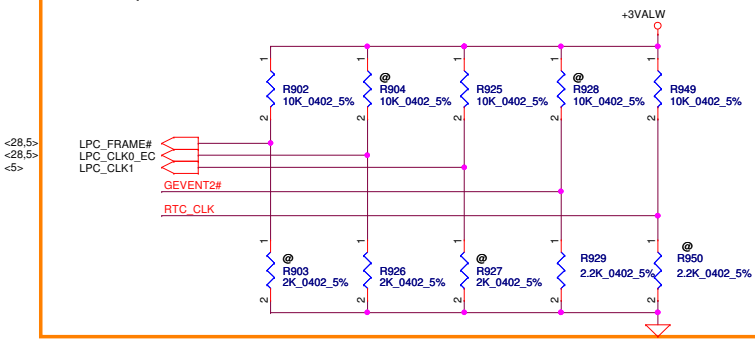


PU +3VALW + PD



STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION



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Compal Electronics, Inc.	
Title	FT3 GPIO/AZ/MISC
Size: Custom	Document Number: VAWGA/GB
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CORE POWER OF APU

+APU_CORE — VDDCR_CPU

C175 10U_0402_6.3V6K; C180 10U_0402_6.3V6K; C181 10U_0402_6.3V6K; C182 10U_0402_6.3V6K; C183 10U_0402_6.3V6K; C184 10U_0402_6.3V6K; C185 10U_0402_6.3V6K; C187 10U_0402_6.3V6K; C188 10U_0402_6.3V6K; C189 10U_0402_6.3V6K; C190 180P_0402_50V8J; @

RTC OF APU

VDDBT_RTC_G — +RTCBATT

+RTCBATT_R — W=20mils — R93 10K_0402_5%

C166 0.22U_0402_10V6K

CLRP1 J@ SHORT PADS — Need OPEN

for Clear CMOS

INTEGRATED GPU POWER OF APU

+APU_CORE_NB — VDDCR_NB

C200 10U_0402_6.3V6K; C201 10U_0402_6.3V6K; C202 10U_0402_6.3V6K; C190 10U_0402_6.3V6K; C191 10U_0402_6.3V6K; C193 10U_0402_6.3V6K; C194 10U_0402_6.3V6K; C197 180P_0402_50V8J

+3VALW/+3VS OF APU

+3VS — C249 10U_0402_6.3V6K; C257 180P_0402_50V8J — VDD_33

+3VALW_APU — R582 @ 0_0603_5% — +3VALW — C252 10U_0402_6.3V6K; C253 10U_0402_6.3V6K — VDD_33_ALW

+1.5V/+1.5VS OF APU

+1.5V — VDDIO_MEM_S — PLANE SPLIT

C224 10U_0603_6.3V6M; C225 10U_0603_6.3V6M; C949 10U_0603_6.3V6M; C223 0.1U_0402_16V7K; C225 0.1U_0402_16V7K; C227 0.1U_0402_16V7K; C228 0.1U_0402_16V7K; C229 0.1U_0402_16V7K; C930 0.1U_0402_16V7K; C932 0.1U_0402_16V7K; C211 180P_0402_50V8J; C210 180P_0402_50V8J; C208 180P_0402_50V8J; C207 180P_0402_50V8J; C230 180P_0402_50V8J; C231 180P_0402_50V8J; C258 180P_0402_50V8J; C259 180P_0402_50V8J; @

VDDIO_AZ_ALW (Could be S0 or S5 power rail)

+1.5VS — C161 4.7U_0603_6.3V6K; C253 10U_0402_6.3V6K; C254 10U_0402_6.3V6K; C255 10U_0402_6.3V6K; C232 180P_0402_50V8J; @

+0.95VALW/+0.95VS OF APU

VDD_095_GFX

+0.95VS — VDD_095 — L22 FBMA-L11-201209-121LMA50T_0805 — +0.95VS_APU_GFX

C935 10U_0603_6.3V6M; C934 10U_0603_6.3V6M; C198 10U_0402_6.3V6K; C199 10U_0402_6.3V6K; C205 10U_0402_6.3V6K; C204 10U_0402_6.3V6K; C206 10U_0402_6.3V6K; C260 10U_0402_6.3V6K; C213 180P_0402_50V8J; C936 10U_0603_6.3V6M; C203 10U_0402_6.3V6K; @

+0.95VALW — C937 10U_0603_6.3V6M; C938 10U_0603_6.3V6M; C216 10U_0402_6.3V6K; C214 10U_0402_6.3V6K; C221 10U_0402_6.3V6K; C218 180P_0402_50V8J; @

VDD_095_USB3_DUAL

+0.95VALW — C220 10U_0402_6.3V6K; C217 10U_0402_6.3V6K; C219 10U_0402_6.3V6K; C222 10U_0402_6.3V6K; @

VDD_095_ALW

+1.8VALW/+1.8VS OF APU

VDD_18

+1.8VS — C933 10U_0603_6.3V6M; C236 10U_0402_6.3V6K; C237 10U_0402_6.3V6K; C238 10U_0402_6.3V6K; C240 10U_0402_6.3V6K; C233 180P_0402_50V8J; C203 10U_0402_6.3V6K

+1.8VALW — C160 4.7U_0603_6.3V6K; C244 10U_0402_6.3V6K; C250 10U_0402_6.3V6K; C246 10U_0402_6.3V6K; C243 10U_0402_6.3V6K; C245 180P_0402_50V8J

VDD_18_ALW

UAPUF

POWER

+1.5V: J35 L32 L37 N35 R31 R37 U32 U35 W31 W32 W37 AA31 AA35 AC32 AC37 AE31 AE35 AG32 AG37 AJ35 AL32 AL37 AR35 VDDIO_MEM_S_1..23

+APU_CORE: VDDCR_CPU_1..26 L21 L23 L25 L27 L29 N21 N23 N27 R21 R23 R27 U21 U23 U27 W21 W23 W27 AA21 AA23 AA27 AC21 AC23 AC27 AE21 AE23 AE27

+APU_CORE_NB: VDDCR_NB_1..21 L13 L17 N11 N13 N17 R11 R13 R17 U13 U17 W13 W17 AA13 AA17 AC13 AC17 AE15 AE17 AE19 AG17 AG21

+1.5VS: AL10 AL11 VDDIO_AZ_ALW_1..2

+1.8VALW: B1 B2 VDD_18_ALW_1..2

+1.8VS: VDD_18_1..4 A2 A3 B3 C3

+3VALW_APU: AL13 AM13 VDD_33_ALW_1..2

+3VS: VDD_33_1..2 AM15 AM17

+0.95VALW: AR5 AU4 AV7 AW5 VDD_095_USB3_DUAL_1..4

+0.95VS: VDD_095_1..9 AG23 AG27 AJ21 AJ27 AL21 AL23 AL27 AM23 AM25

+0.95VALW: AE11 AE13 AJ11 AJ13 VDD_095_ALW_1..4

+0.95VS_APU_GFX: VDD_095_GFX_1..3 U10 W10 AA10

+RTCBATT_R: AN4 VDDBT_RTC_G

FT3 REV 0.51 — X4@ — FT3_BGA769

UAPUG

GND

A8 A13 A23 A31 A35 A39 B8 B13 B23 B31 B39 C1 C2 C5 C7 C9 C11 C13 C15 C17 C19 C21 C23 C25 C27 C29 C31 C33 C35 C37 C39 C41 D9 D11 D13 E3 E4 E9 E11 E13 E27 E31 E35 E38 E39 G3 G7 G11 G13 G15 G17 G21 G25 G29 G35 G37 G39 G41 H11 H13 H23 H31 VSS_1..62

J3 J7 J8 J39 K11 K13 K17 K19 K21 K23 K25 K27 K29 K31 L3 L7 L8 L10 L11 L15 L19 L31 L39 L41 M1 M2 N3 N7 N15 N19 N25 N29 N31 N39 P1 P2 R3 R7 R15 R19 R25 R29 R39 R41 U1 U2 U3 U7 U8 U11 U15 U19 U25 U29 U31 U37 U39 W3 W5 W11 W15 W19 W25 VSS_63..124

FT3 REV 0.51 — X4@ — FT3_BGA769

UAPUH

GND

W29 W39 W41 Y1 Y2 AA3 AA7 AA8 AA11 AA15 AA19 AA25 AA29 AA39 AC3 AC7 AC11 AC15 AC19 AC25 AC29 AC31 AC39 AC41 AE3 AE7 AE25 AE29 AE32 AE39 AG3 AG5 AG10 AG11 AG13 AG15 AG19 AG25 AG29 AG31 AG39 AG41 AH1 AH2 AJ3 AJ7 AJ15 AJ17 AJ19 AJ23 AJ25 AJ29 AJ31 AJ32 AJ39 AL3 AL8 AL15 AL17 AL19 AL25 AL29 VSS_125..186

AL39 AL41 AM11 AM27 AM31 AN3 AN7 AN39 AP31 AR3 AR13 AR17 AR21 AR25 AR29 AR39 AR41 AU1 AU2 AU3 AU15 AU19 AU23 AU27 AU39 AV9 AW3 AW7 AW13 AW15 AW17 AW19 AW21 AW23 AW25 AW27 AW31 AW33 AW35 AW37 AW39 AW41 AY13 AY15 AY18 AY30 BA2 BA7 BA13 BA15 BA18 BA21 BA25 BA31 BA35 BA39 A15 AL31 AM29 VSS_187..242 VSSBG_DAC VBURN PSEN

FT3 REV 0.51 — X4@ — FT3_BGA769

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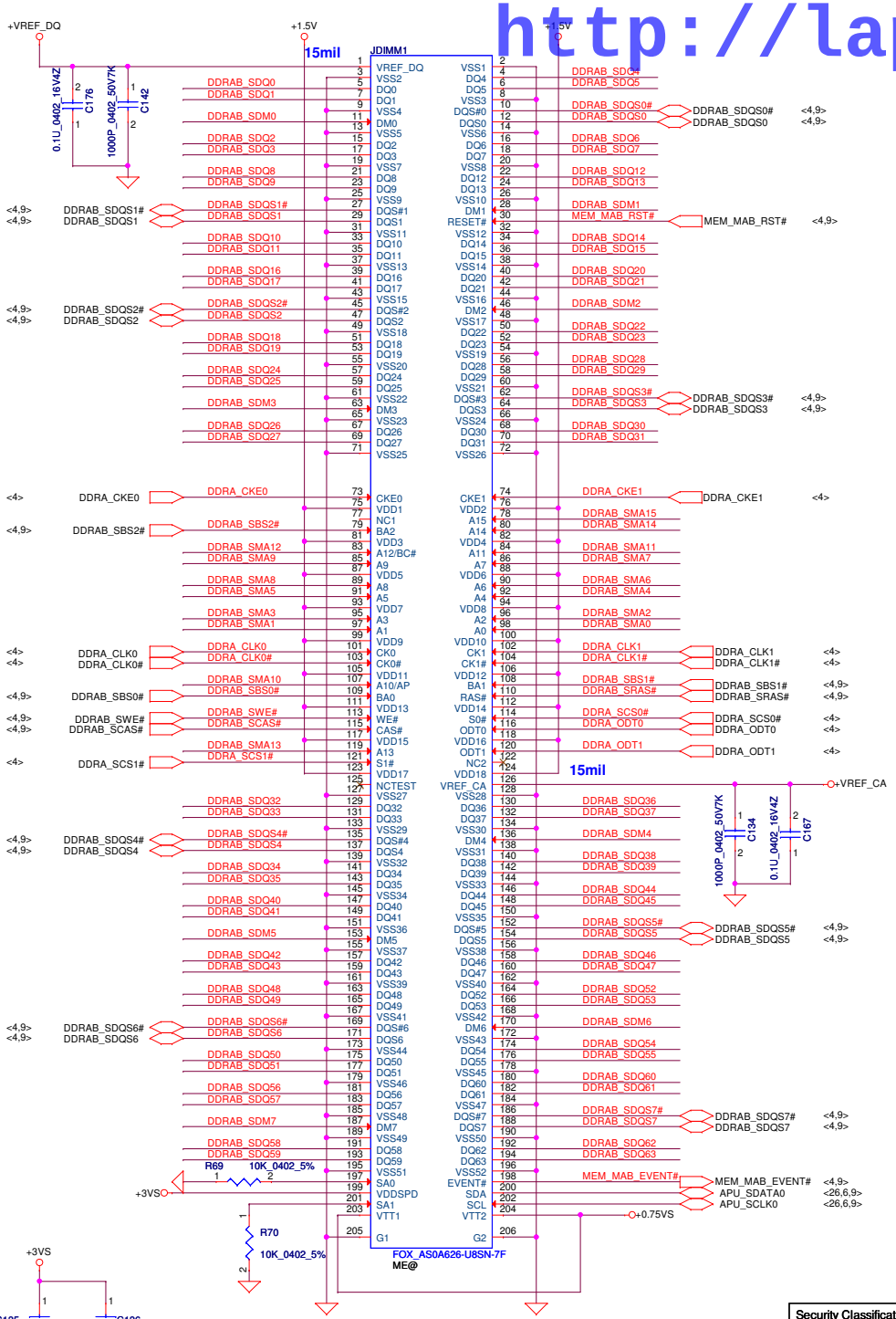
Compal Electronics, Inc.

Title: FT3 PWR/GND

Size: B25 Custom | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 7 of 48



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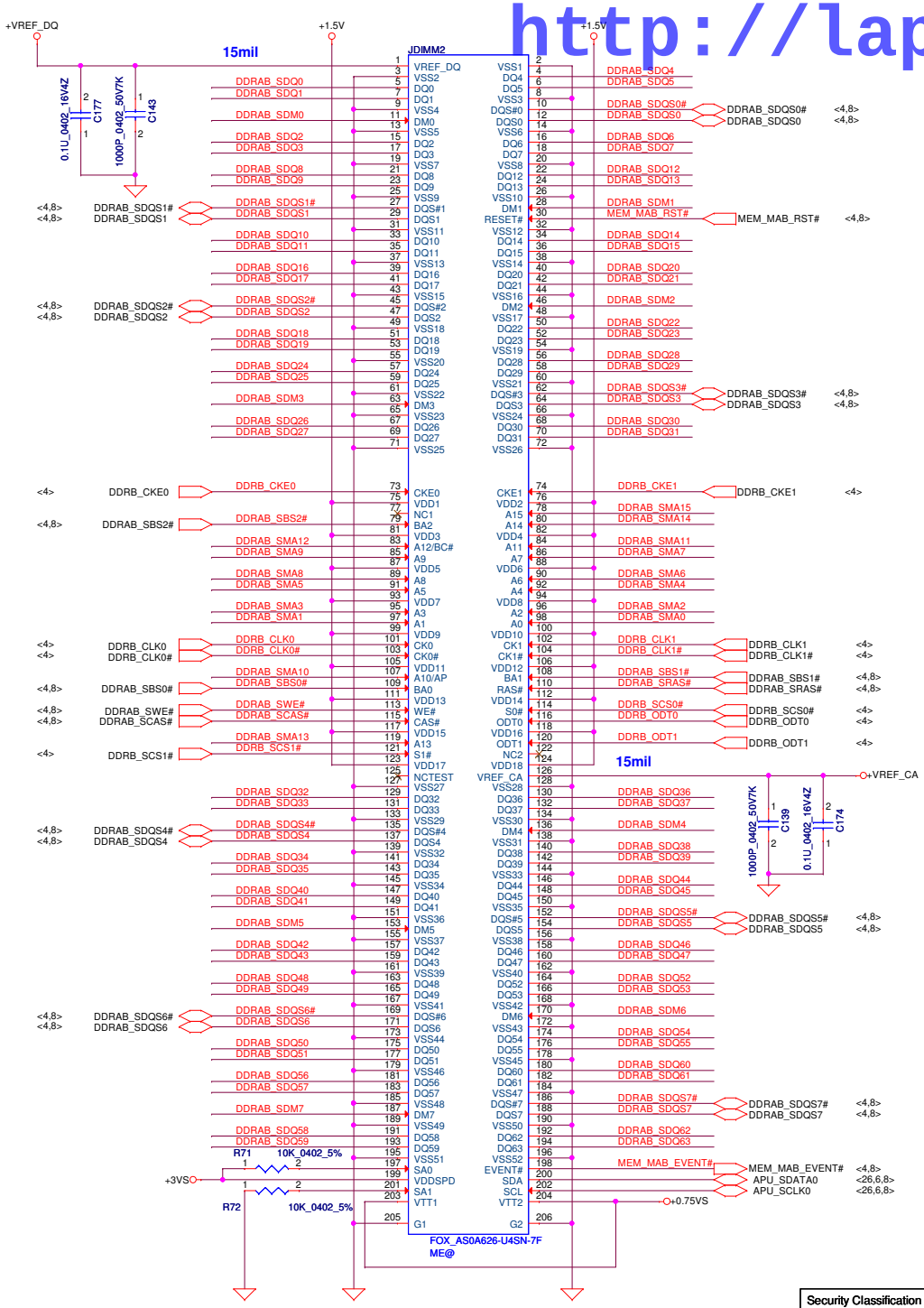
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

Size	Document Number	Rev
Custom	VAWGA/GB	1.0

Date: Thursday, March 28, 2013 | Sheet 8 of 48

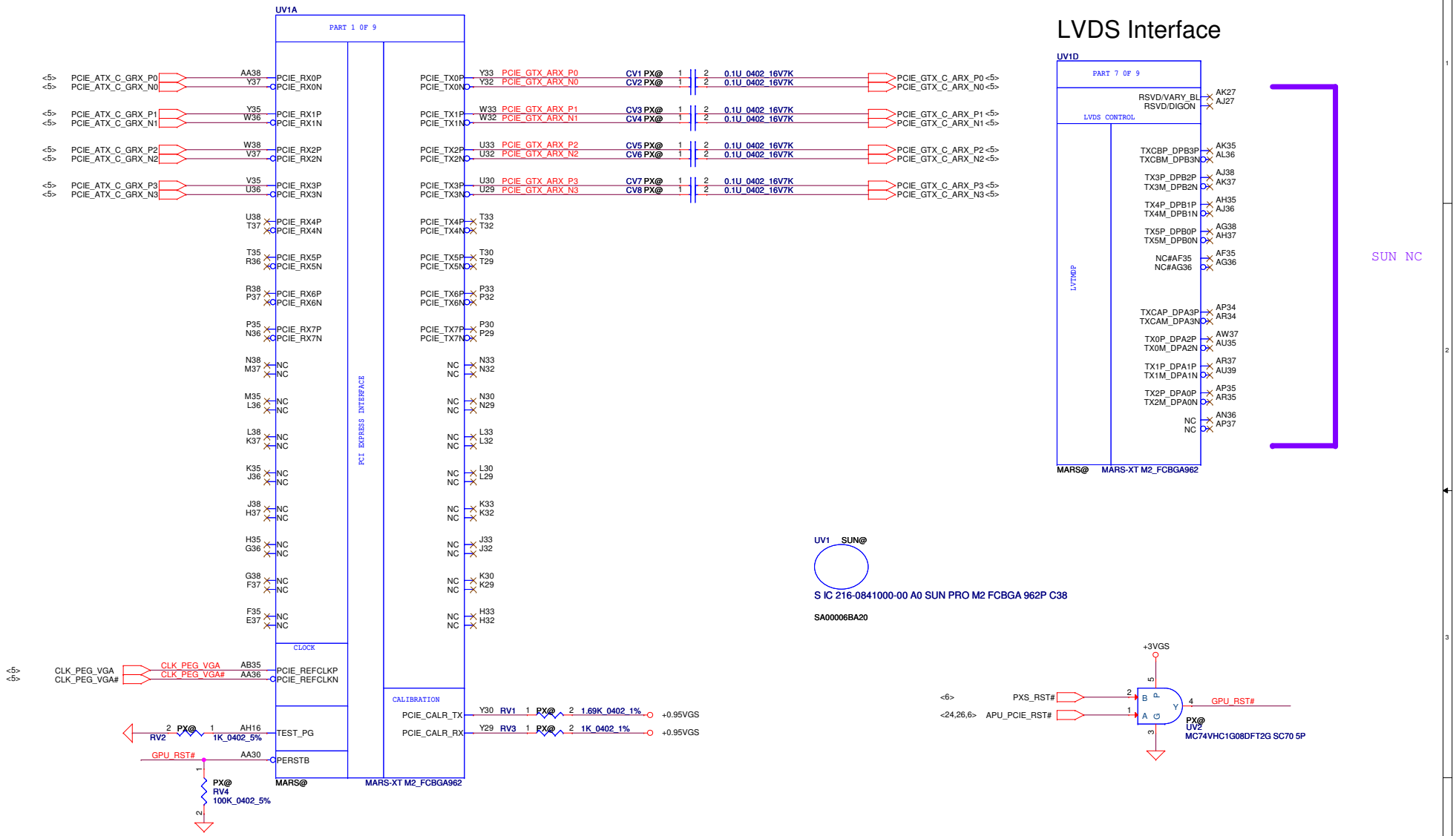


DIMM_B H:4mm

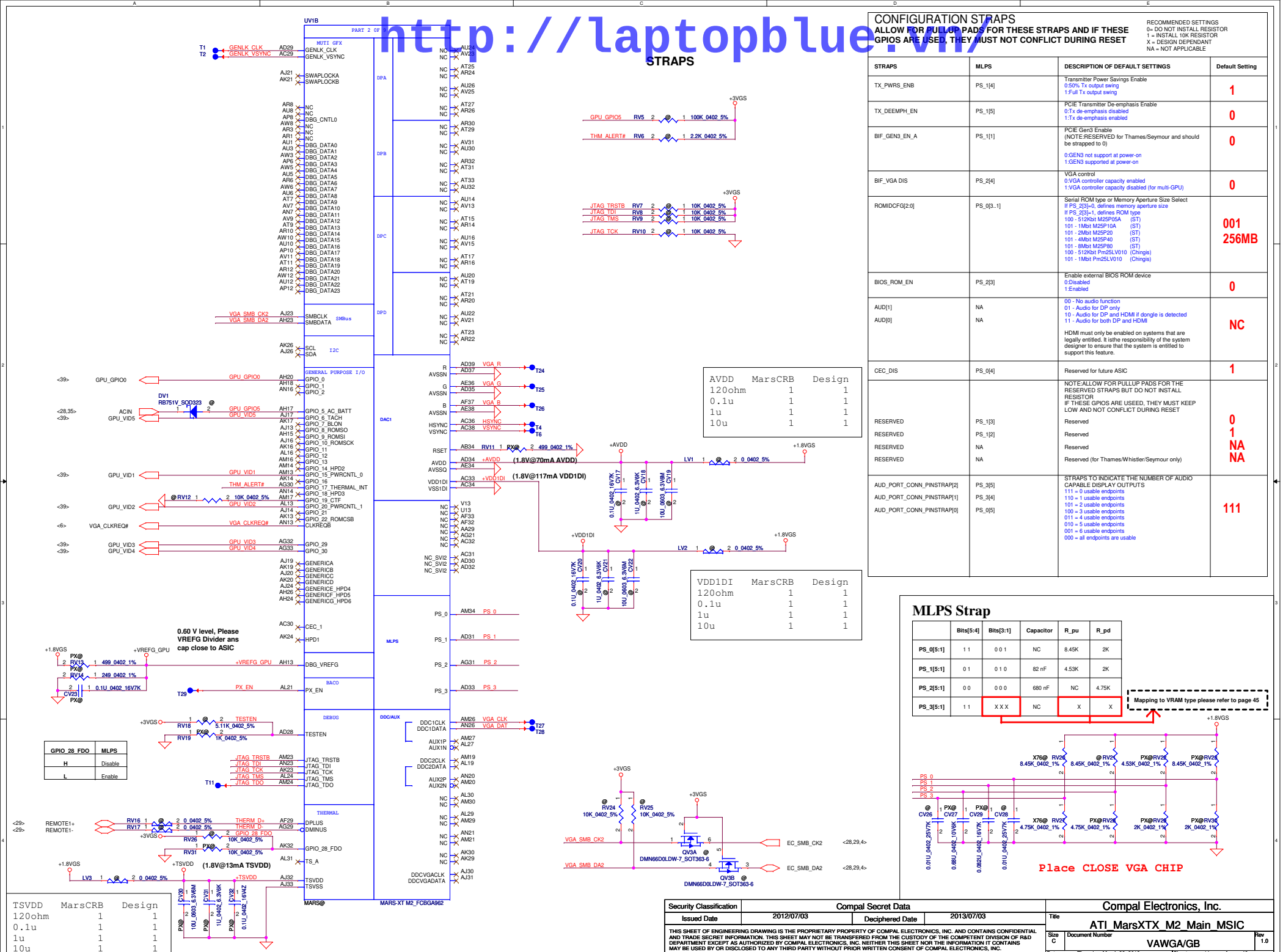
<Address: 10>

Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Compal Electronics, Inc.			
Title: DDR3 SODIMM-II Socket			
Size: Custom	Document Number: VAWGA/GB		Rev: 1.0
Date: Thursday, March 28, 2013	Sheet 9 of 48		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/03	Deciphered Date 2013/07/03	Title: ATI_MarsXTX_M2_PCIE/LVDS
			Size: Custom; Document Number: VAWGA/GB; Rev: 1.0
			Date: Monday, April 01, 2013; Sheet 10 of 48



STRAPS

GPIO_28_FDO	MLPS
H	Disable
L	Enable

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	0
BIF_VGA DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001 256MB
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1] AUD[0]	NA NA	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature.	NC
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 1 NA NA
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	0 1	0 1 0	82 nF	4.53K	2K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 45

Security Classification	Compal Secret Data
Issued Date	2012/07/03
Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_Main_MSIC

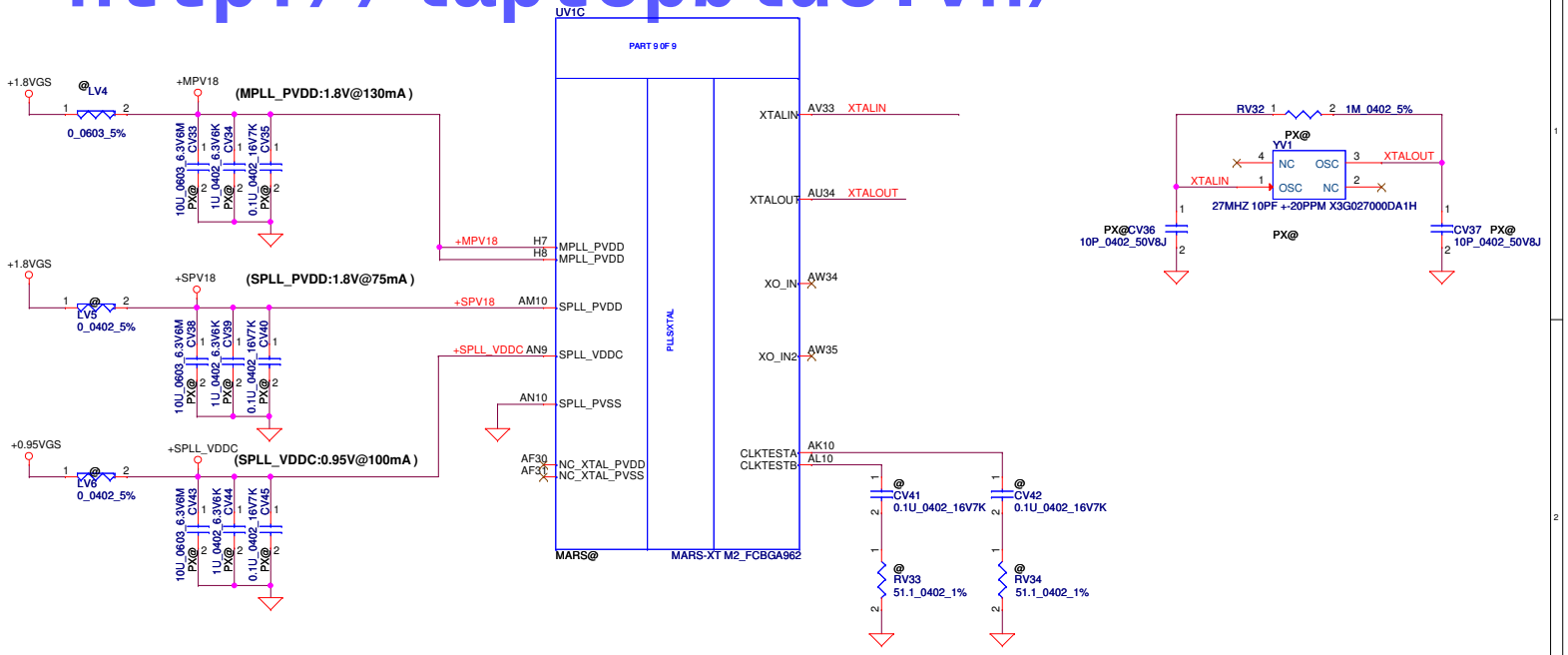
Size: C | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 11 of 48

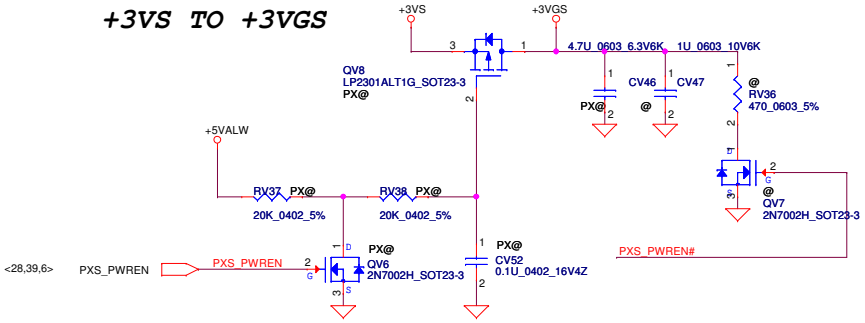
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

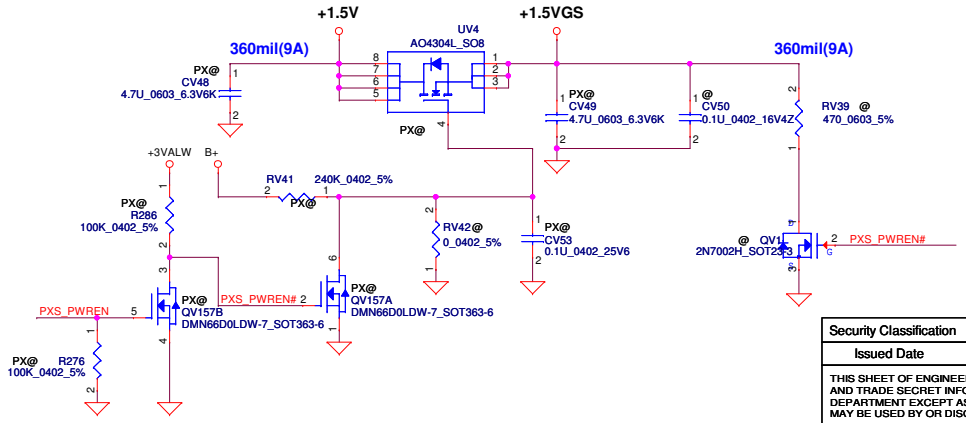


+3VS TO +3VGS

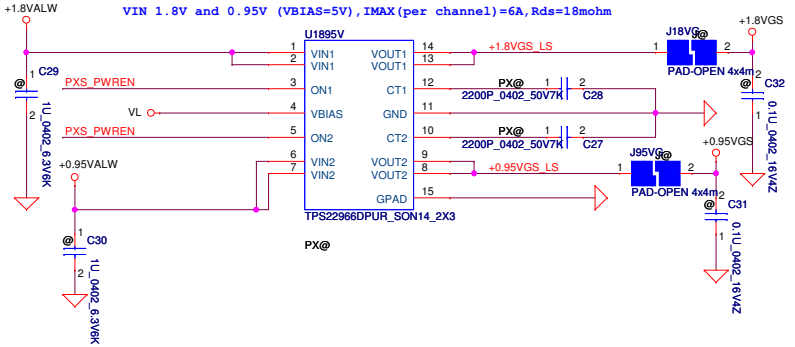


+1.5V TO +1.5VGS

AO4430: Rdson: 5.5mohm @ VGS=10V



+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch



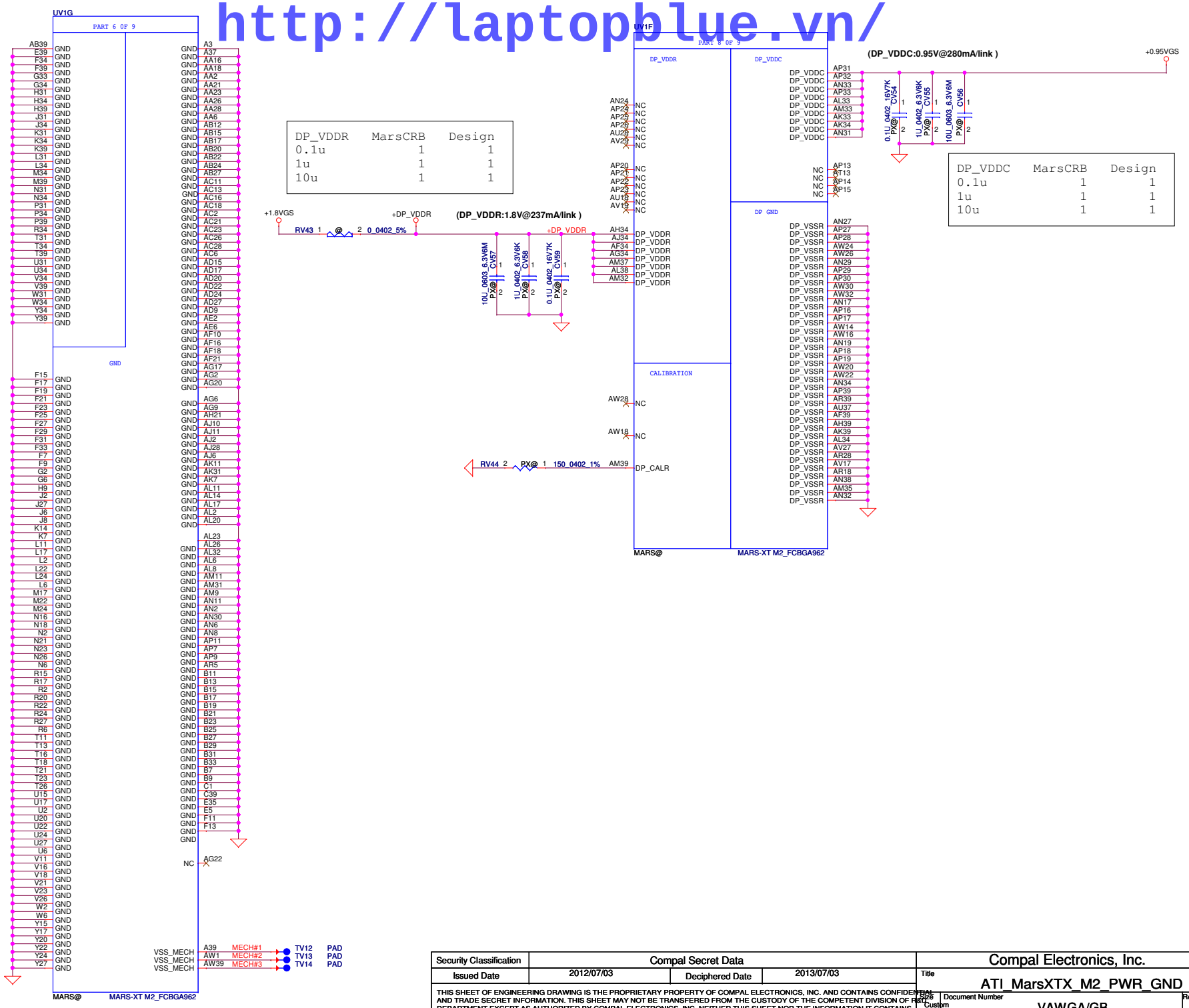
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_BACO POWER

Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 12 of 48



DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

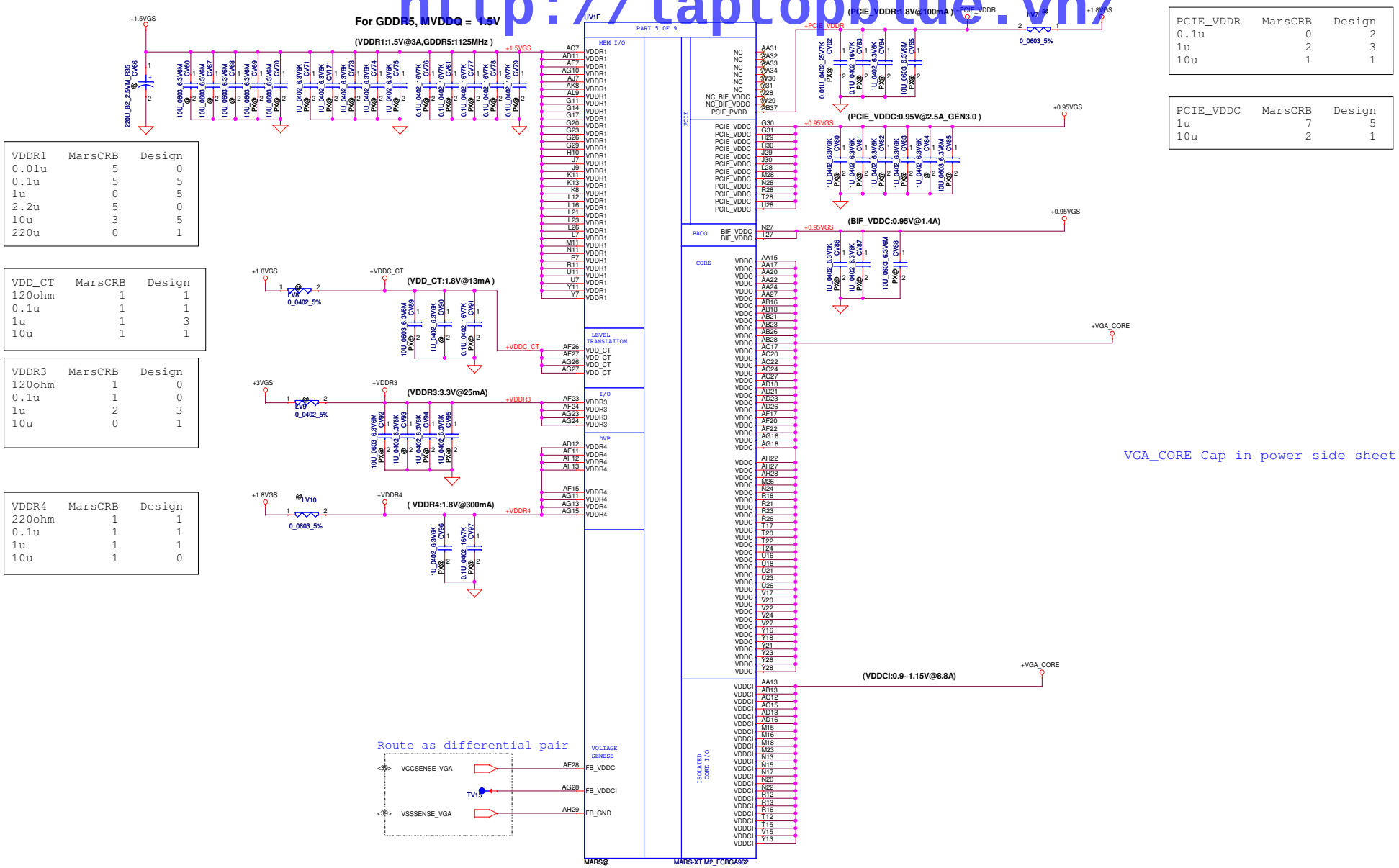
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_PWR_GND

Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 13 of 48



VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

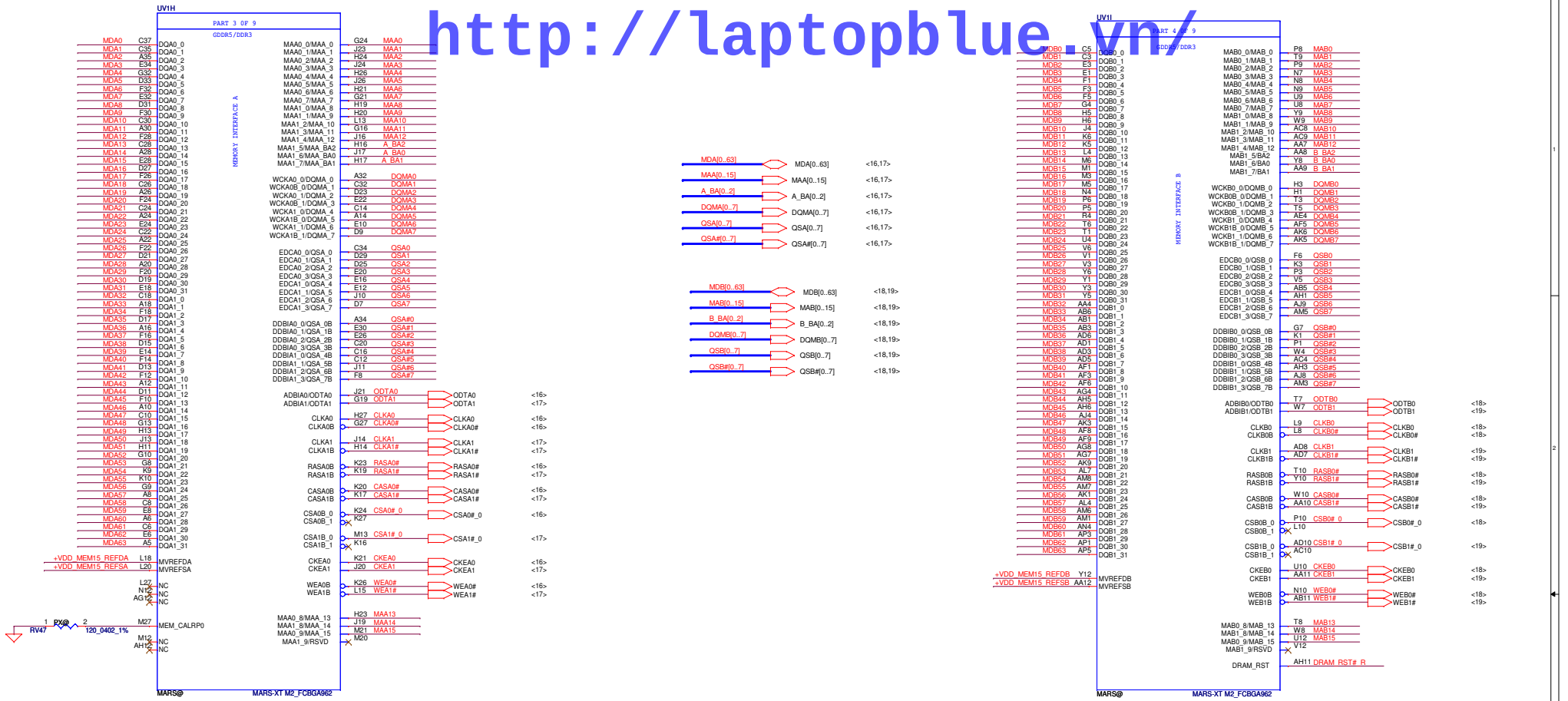
VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

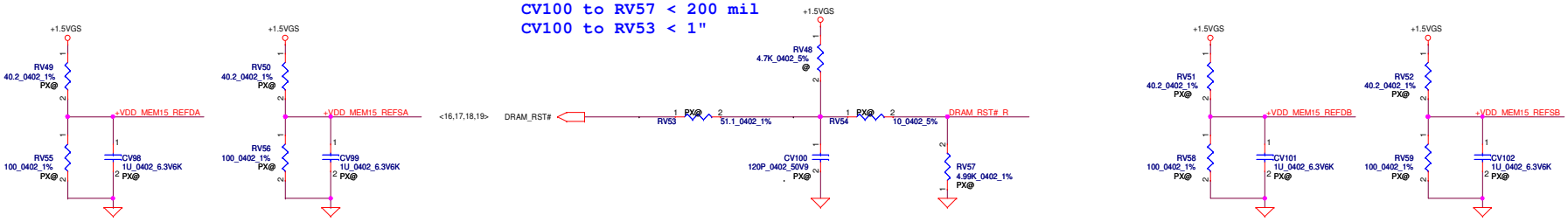
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/03	Deciphered Date	2013/07/03
Title	ATI_MarsXTX_M2_Power		
Size C	Document Number VAWGA/GB		Rev 1.0
Date: Thursday, March 28, 2013	Sheet 14 of 48		



Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"

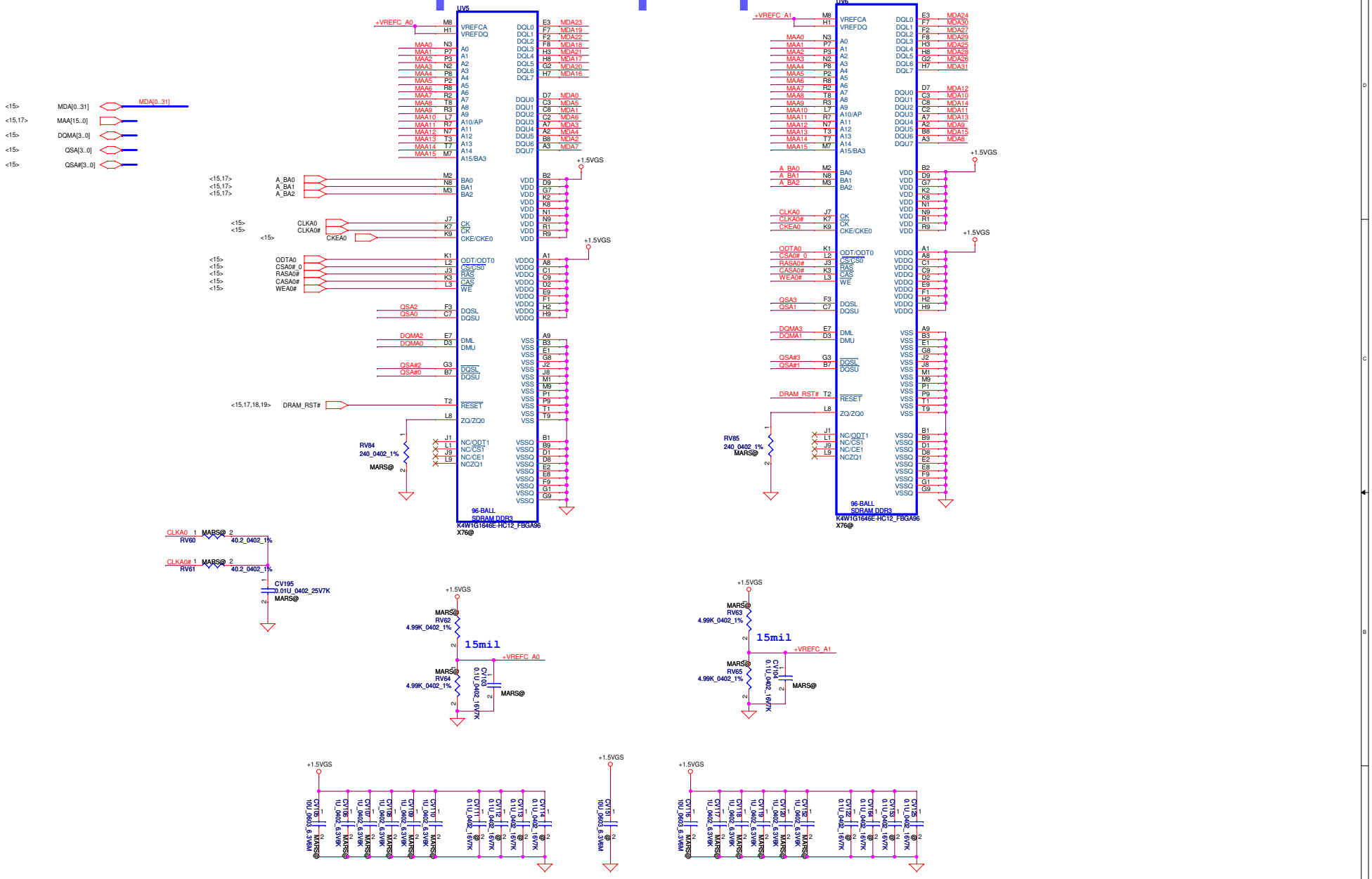


DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.			
Title	ATI_MarsXTX_M2_MEM IF		
Size C	Document Number VAWGA/GB		Rev 1.0
Date: Thursday, March 28, 2013	Sheet 15 of 48		



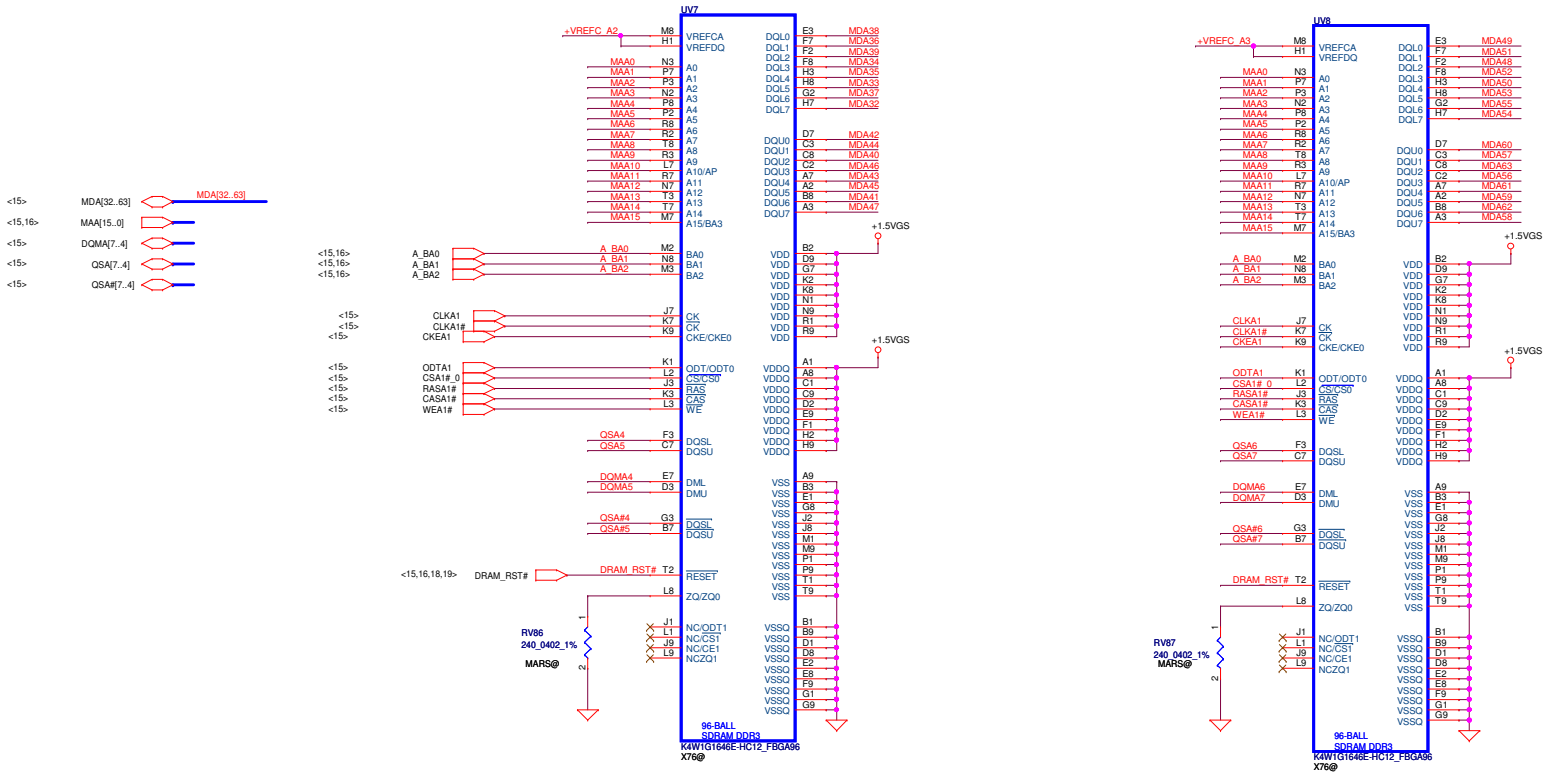
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

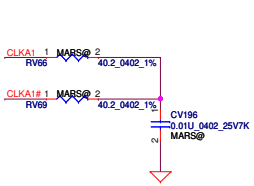
Compal Electronics, Inc.

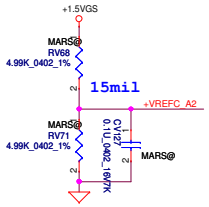
Title: ATI_Whistler_M2_VRAM_A

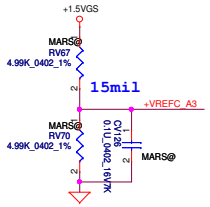
Size	Document Number	Rev
C	VAWGA/GB	1.0

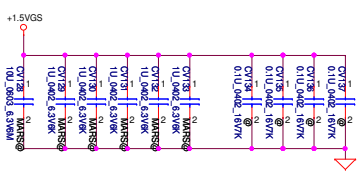
Date: Thursday, March 28, 2013 | Sheet 16 of 48

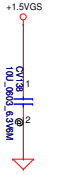


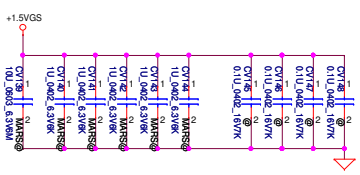












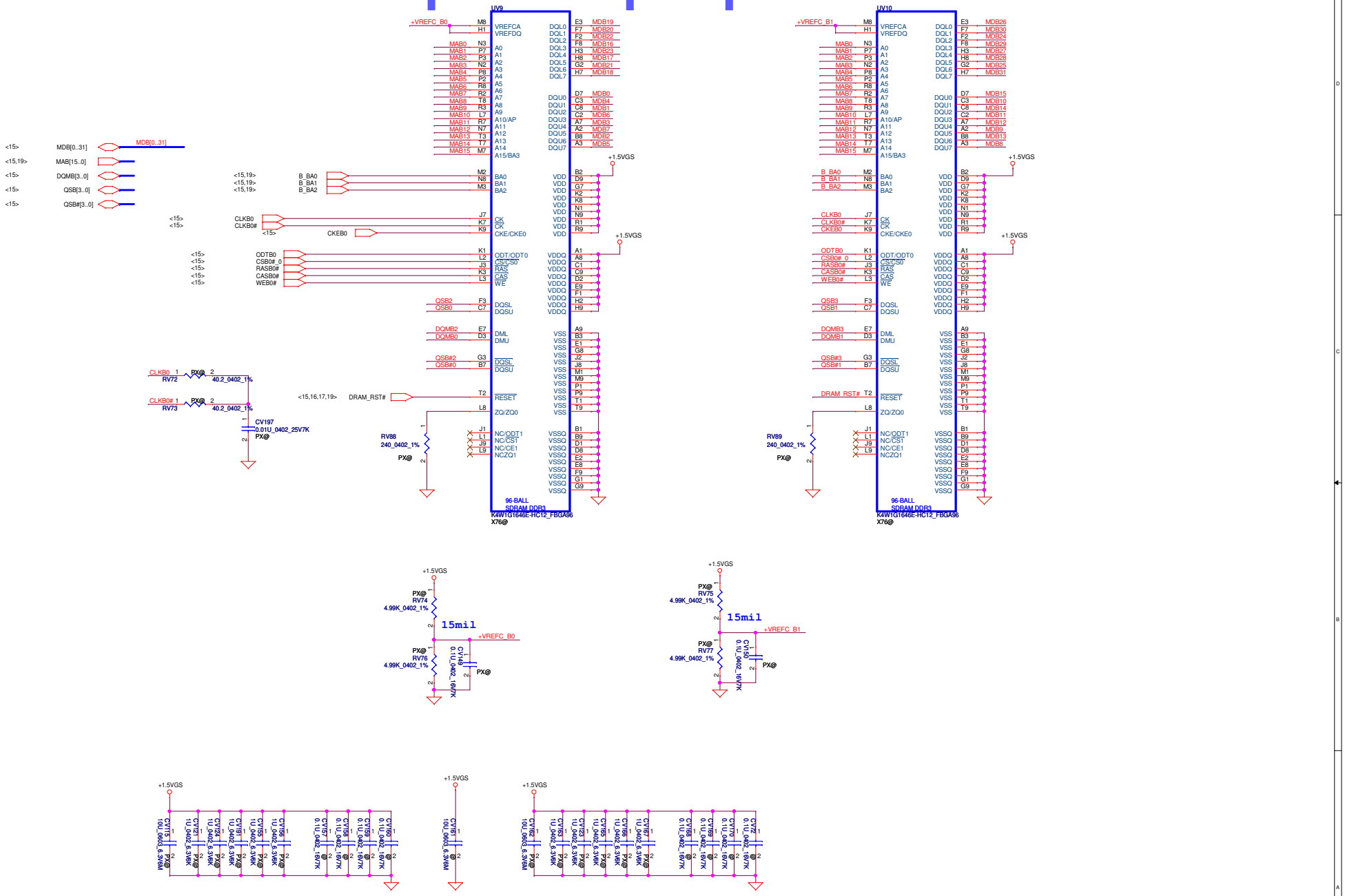
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	VAWGA/GB	1.0

Date: Thursday, March 28, 2013 | Sheet 17 of 48



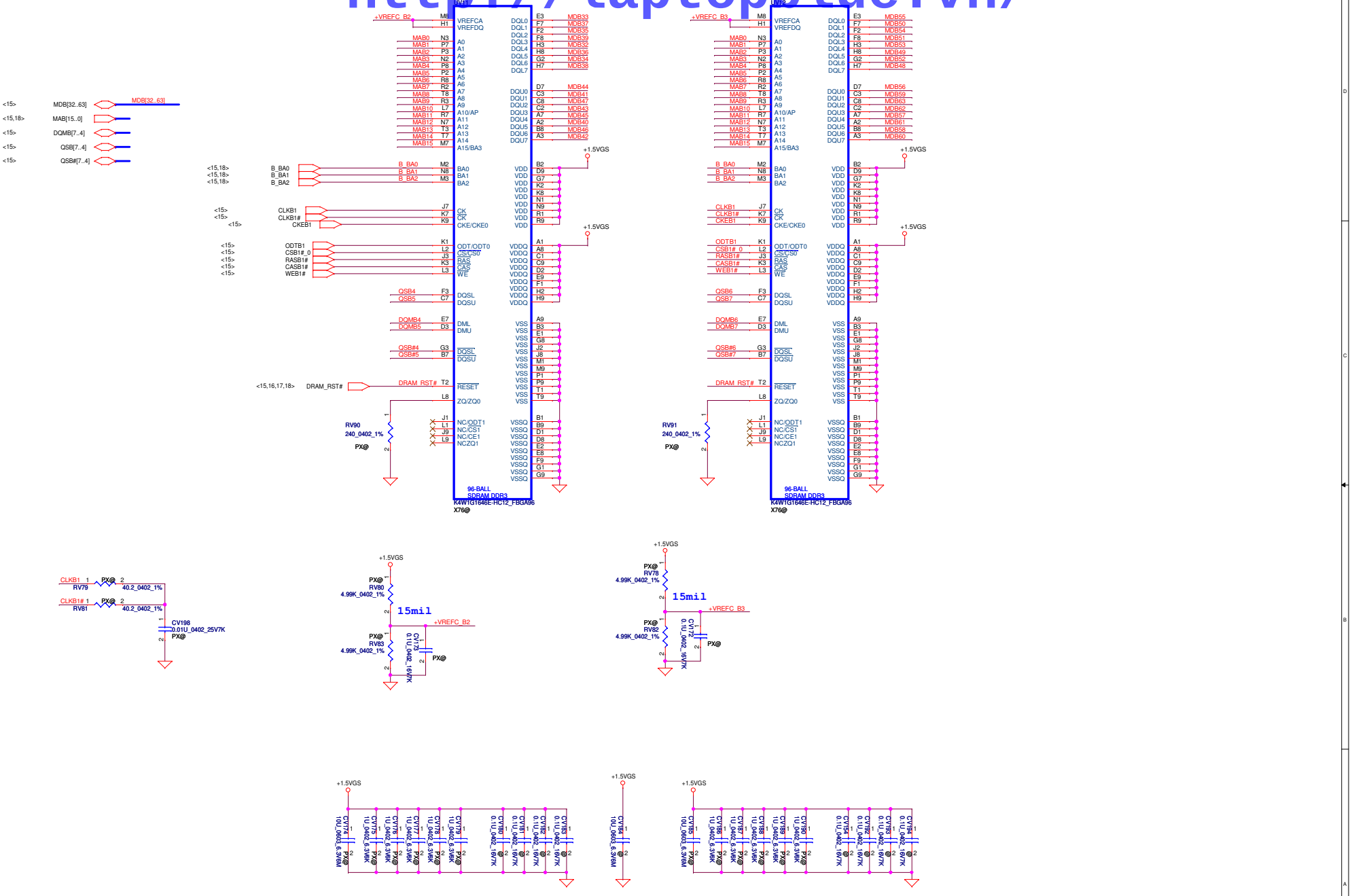
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B

Size	Document Number	Rev
C	VAWGA/GB	1.0

Date: Thursday, March 28, 2013 | Sheet 18 of 48



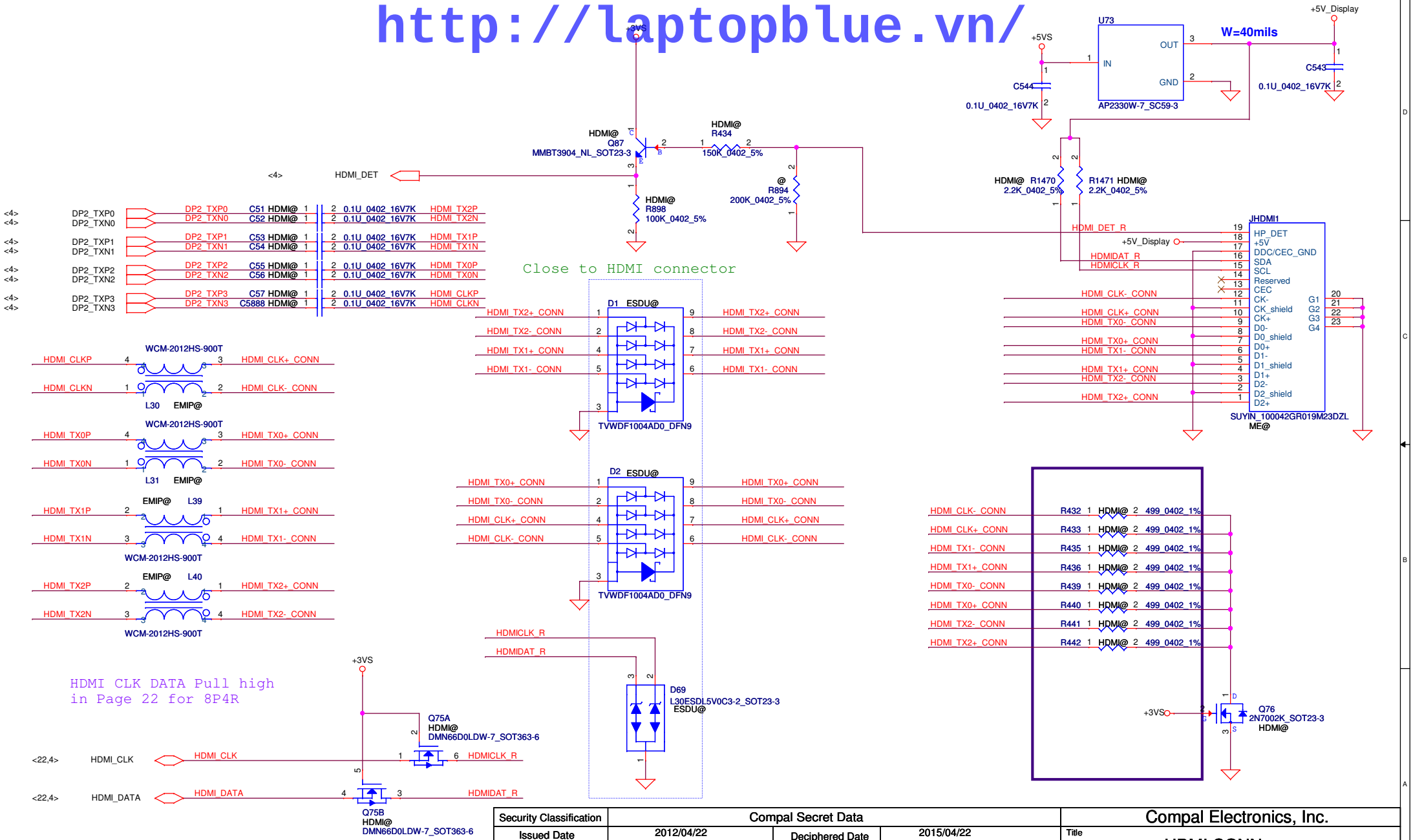
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	VAWGA/GB	1.0

Date: Thursday, March 28, 2013 | Sheet 19 of 48



Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

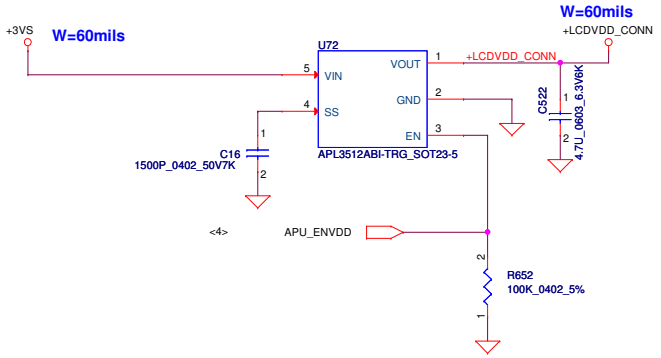
Compal Electronics, Inc.

Title: HDMI CONN

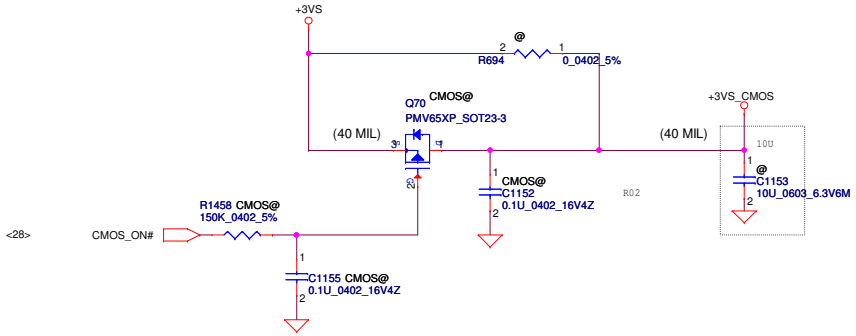
Size	Document Number	Rev
B	VAWGA/GB	1.0

Date: Monday, April 01, 2013 Sheet 20 of 48

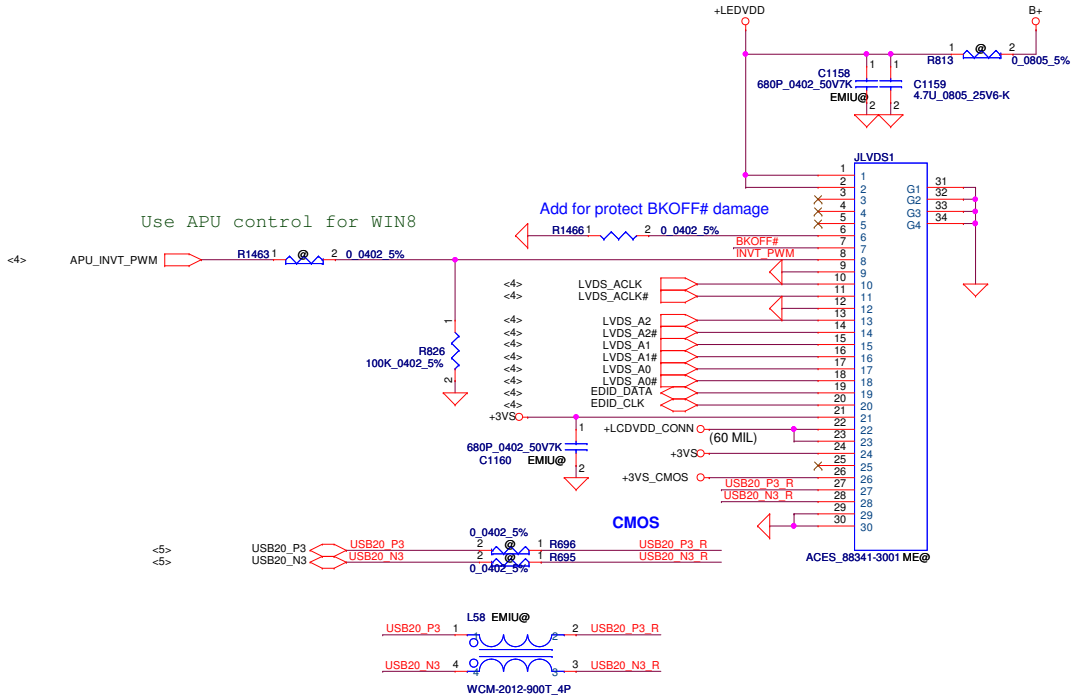
LCD POWER CIRCUIT



CMOS Camera

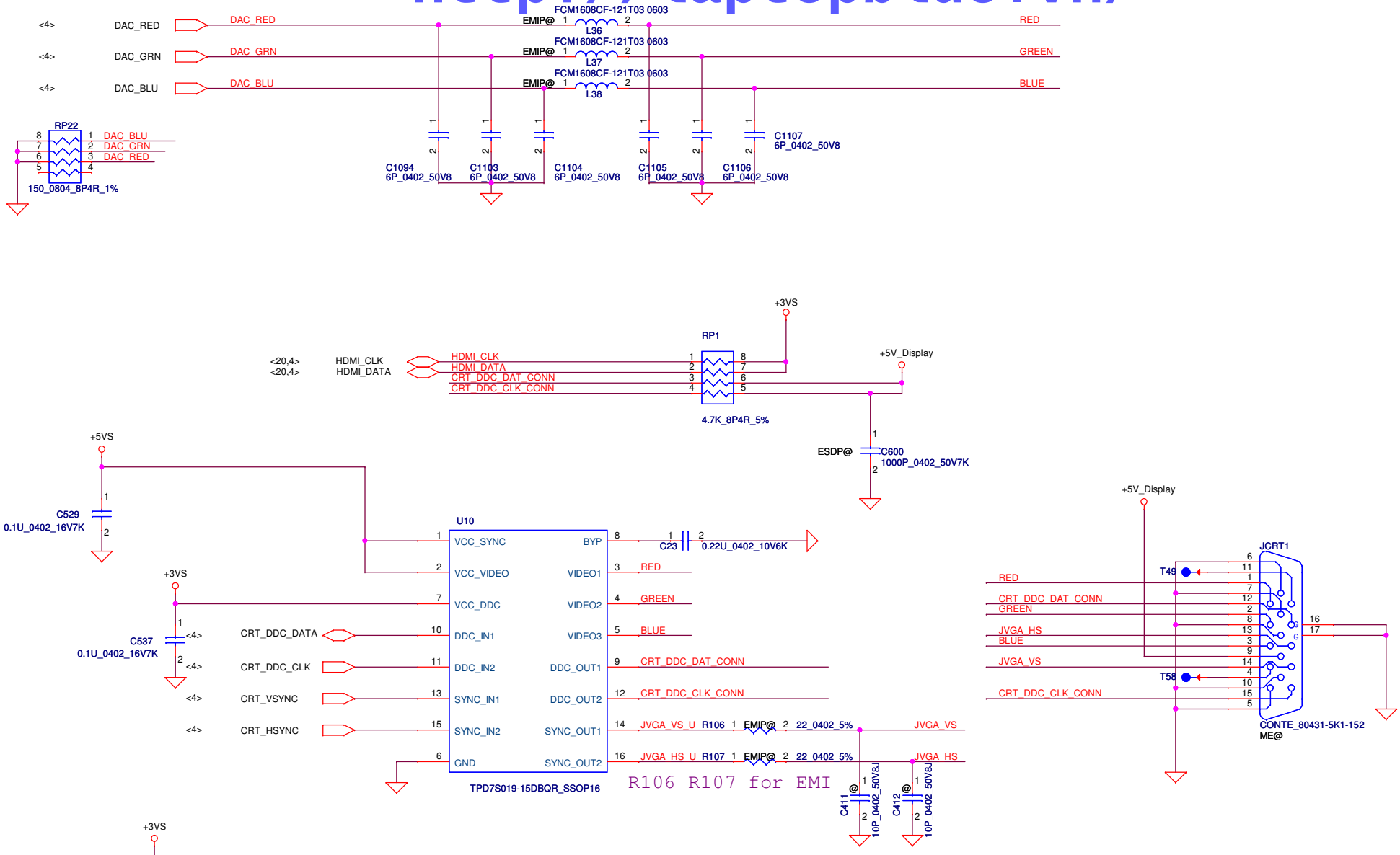


VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

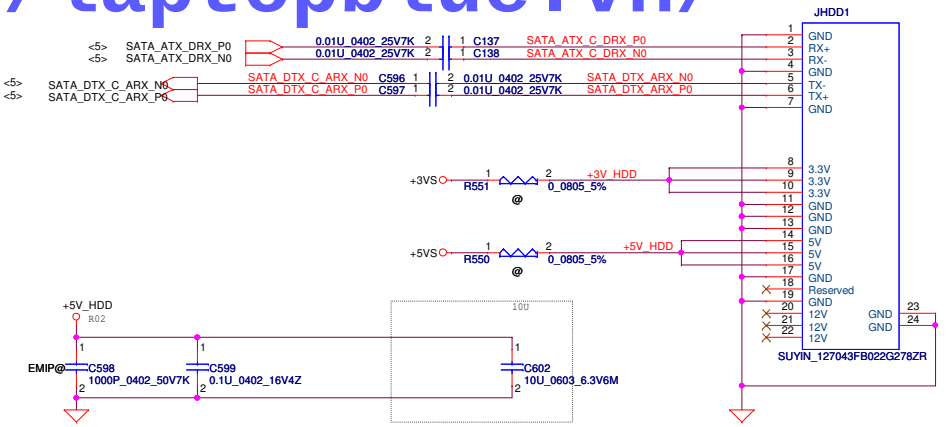
Compal Electronics, Inc.	
Title	LVDS CONN / Camera
Size: B	Document Number: VAWGA/GB
Rev	1.0
Date: Thursday, March 28, 2013	Sheet 21 of 48



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date	2015/04/22

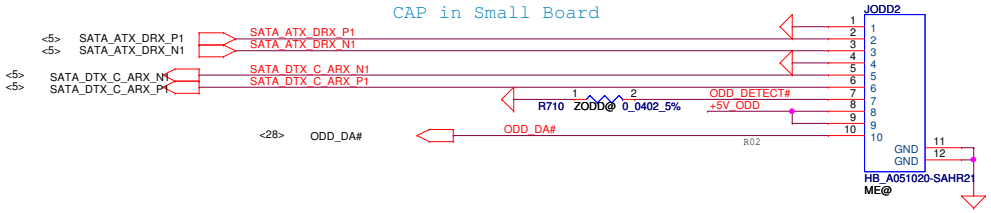
Title	CRT CONN		
Size B	Document Number VAWGA/GB		Rev 1.0
Date: Thursday, March 28, 2013	Sheet 22 of 48		

SATA HDD Conn.



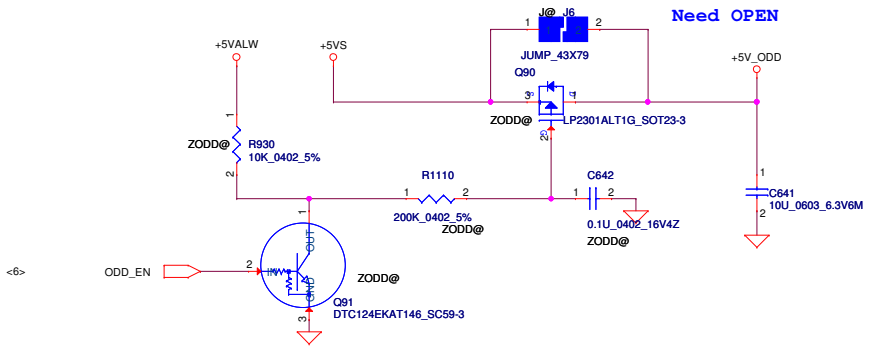
FOR 15"

SATA ODD FFC Conn.



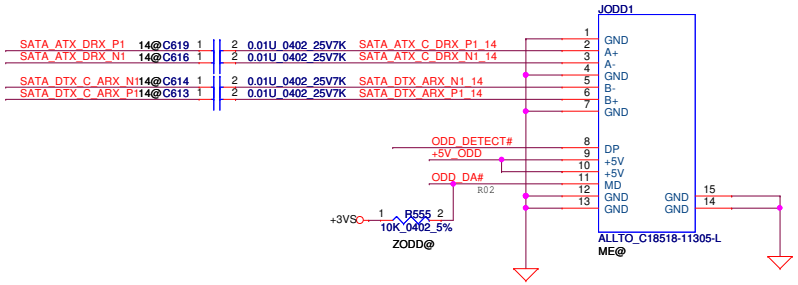
Co-lay

ODD Power Control



FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date 2015/04/22	Title HDD/ODD/FAN/SCREW
Size B	Document Number VAWGA/GB		Rev 1.0
Date: Thursday, March 28, 2013	Sheet 23 of 48		

Layout Notice : Place as close chip as possible.

+3VALW

+3V_LAN

J10 J@ JUMP_43X79

Close together

+LX_R

LL1 SWR@ 4.7UH_SIA4012-4R7M_20%

CL1 1000P_0402_50V7K

CL2 0.1U_0402_16V7K

CL3 10U_0603_6.3V6M

SWR@SWR@SWR@

Close to Pin40

Note: Place Close to LAN chip
LL1 DCR< 0.15 ohm
Rate current > 1A

LL2 FBMA-L11160808601LMA10T_2P

LL3 SWR@ FBMA-L11160808601LMA10T_2P

+1.1_AVDDL_L

+1.1_AVDDL

+LX_R

CL4 0.1U_0402_16V7K

CL5 1U_0402_6.3V4Z

CL6 4.7U_0603_6.3V6K

Place close to Pin34

<28> LAN_PWR_ON#

LAN_PWR_ON# RL3 10K_0402_5% CL7 0.1U_0402_16V7K

QL1 PMV65XP_SOT23-3~D

LAN Chip Vendor recommand reserve the
PU resistor close LAN chip
AMD recommand reserve Diode

UL1 8172@ AR8172-AL3A-R

+3V_LAN

<10,6> APU_PCIE_RST#

RL4 4.7K_0402_5%

D4 RB751V-40TE17_SOD323-2

LAN_PERST#

R577 0_0402_5%

Place Close to Chip

UL1 Atheros AR8151/AR8161

<5> PCIE_DTX_C_ARX_N1 CL9 0.1U_0402_16V7K PCIE_DTX_ARX_N1 29 TX_N

<5> PCIE_DTX_C_ARX_P1 CL11 0.1U_0402_16V7K PCIE_DTX_ARX_P1 30 TX_P

<5> PCIE_ATX_C_DRX_N1 36 RX_N

<5> PCIE_ATX_C_DRX_P1 35 RX_P

<5> CLK_PCIE_LAN# 32 REFCLK_N

<5> CLK_PCIE_LAN 33 REFCLK_P

LAN_PERST# 2 PERST#

<28> LAN_WAKE# 3 WAKE#

25 SMCLK

26 SMDATA

28 NC

27 TESTMODE

LAN_XTALO 7 XTLO

LAN_XTALI 8 XTLI

<6> LAN_CLKREQ# 4 CLKREQ#

+1.1_AVDDL 13 AVDDL

+1.1_AVDDL 19 AVDDL

+1.1_AVDDL 31 AVDDL

+1.1_AVDDL_L 34 AVDDL

+1.1_AVDDL 6 AVDDL

AVDDL_REG/AVDDL

41 GND

AR8162-AL3A-R_QFN40_5X5

8162@

LED_0 38

LED_1 39

LED_2 23

RL12 LDO@ 10K_0402_5%

mount RL12 if use LDO modue

TRXN0 12 MDI0- <25>

TRXP0 11 MDI0+ <25>

TRXN1 15 MDI1- <25>

TRXP1 14 MDI1+ <25>

TRXN2 18

TRXP2 17

TRXN3 21

TRXP3 20

RBIAS 10 LAN_RBIAS RL9 2.37K_0402_1%

Place Close to PIN1

VDD33 1 +3V_LAN

LX 40 +LX

VDDCT/ISOLAN 5 +1.7_VDDCT

RL10 30K_0402_5% +3V_LAN

DVDDL/PPS 24

DVDDL_REG/DVDDL 37 +LX_R

AVDDH/AVDD33 16 +3V_LAN

AVDDH 22 +2.7_AVDDH

AVDDH_REG 9 +2.7_AVDDH

+2.7_AVDDH

Place Close to PIN1

+3V_LAN

CL12 1000P_0402_50V7K

CL13 0.1U_0402_16V7K

CL14 1U_0402_6.3V4Z

CL15 10U_0603_6.3V6M

CL16 10U_0603_6.3V6M

CL17 0.1U_0402_16V7K

CL18 0.1U_0402_16V7K

CL19 0.1U_0402_16V7K

CL20 1U_0402_6.3V4Z

CL21 0.1U_0402_16V7K

Near Pin6

Near Pin13

Near Pin19

Near Pin31

CL22 0.1U_0402_16V7K

CL23 1U_0402_6.3V4Z

CL24 0.1U_0402_16V7K

Near Pin9

Near Pin22

CL25 0.1U_0402_16V7K

CL26 1U_0402_6.3V4Z

Near Pin37

+3V_LAN

CL10 0.1U_0402_16V7K

CL8 1U_0402_6.3V4Z

Place close to Pin16

LAN_XTALI

LAN_XTALO

YL1 25MHZ_20PF_FSX3M-25.M20FDO

NC OSC NC OSC

CL28 15P_0402_50V8J

CL29 15P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Compal Electronics, Inc.

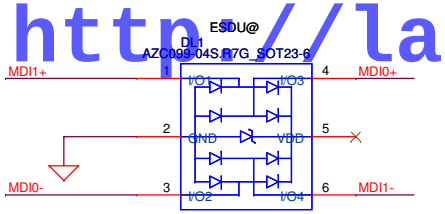
Title: LAN-AR8151

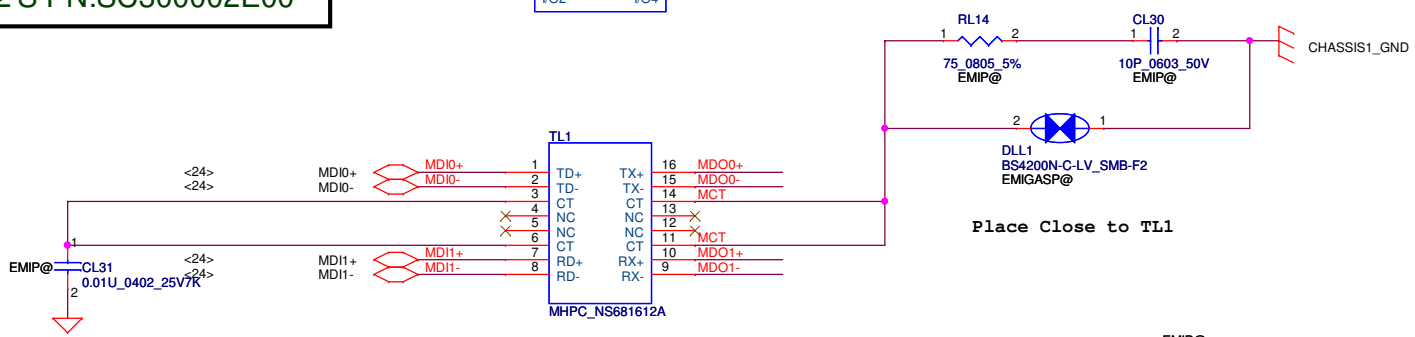
Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 24 of 48

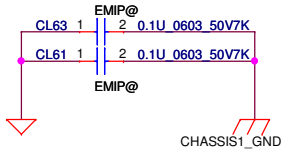
Place Close to TL1

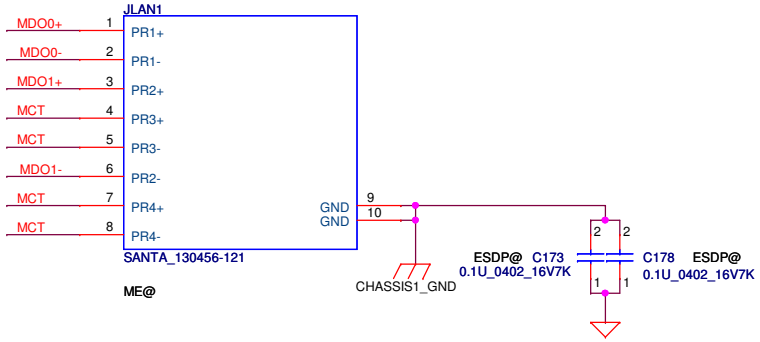
DL1
1'S PN:SC300001G00
2'S PN:SC300002E00





Place Close to TL1





Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

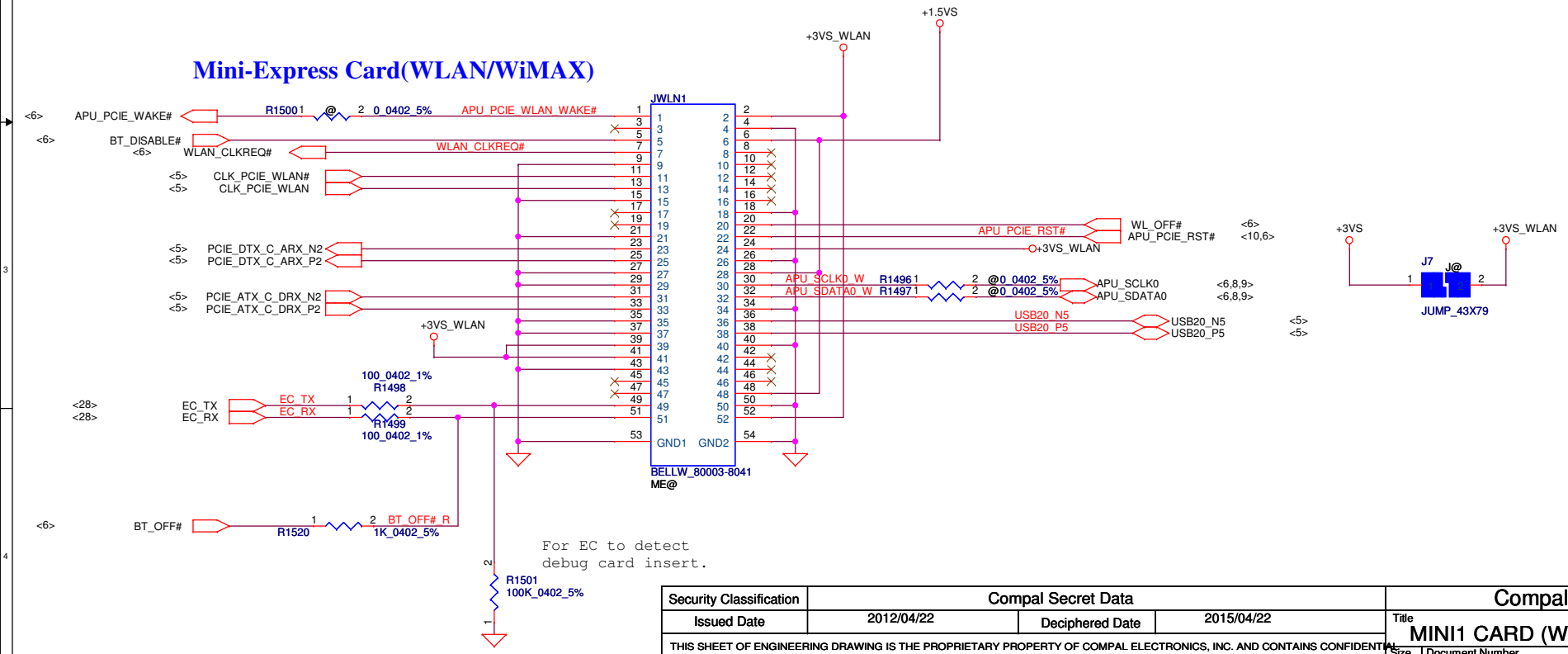
Compal Electronics, Inc.

Title: LAN_Transformer

Size: B | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 25 of 48

Mini-Express Card(WLAN/WiMAX)



Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

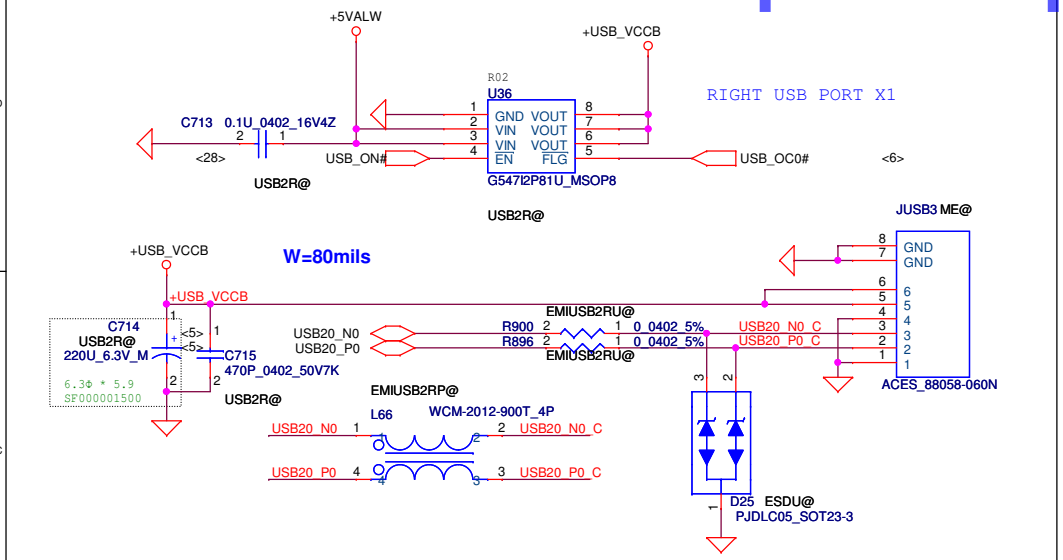
Compal Electronics, Inc.

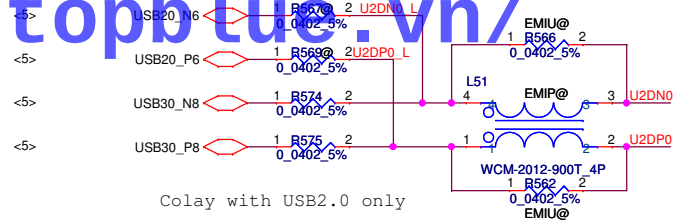
Title: MINI1 CARD (WLAN) / MINI2 CARD (Option)

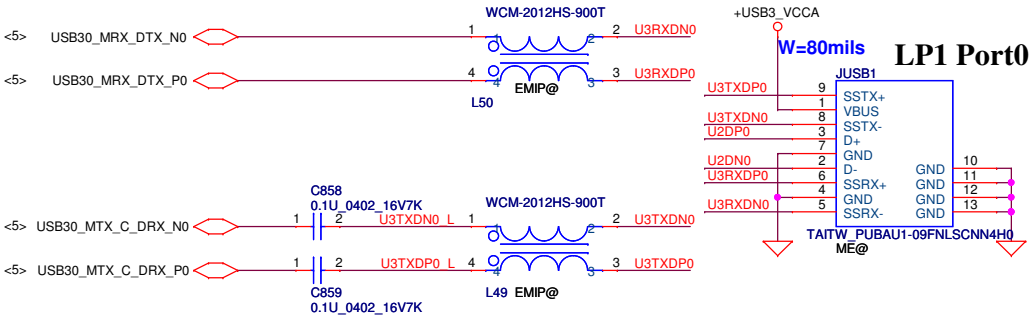
Size	Document Number	Rev
B	VAWGA/GB	1.0

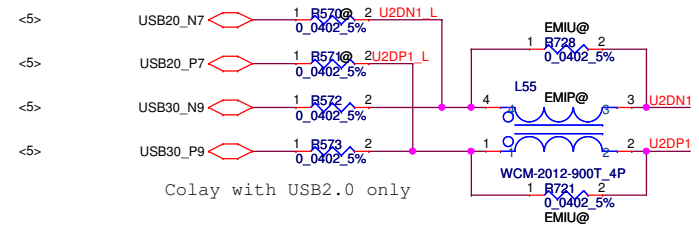
Date: Thursday, March 28, 2013 Sheet 26 of 48

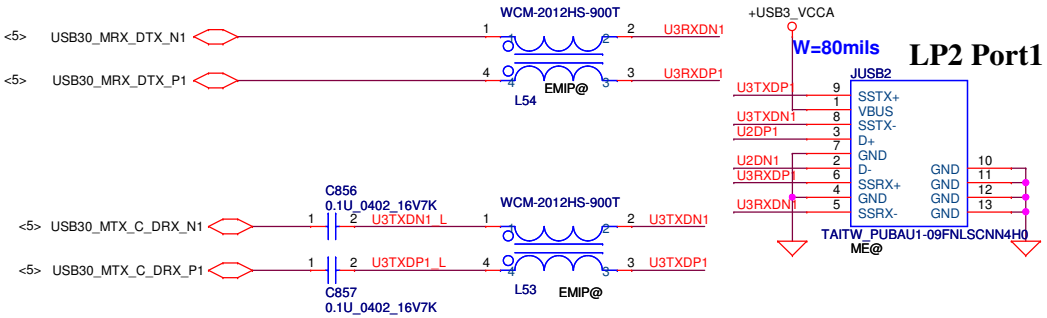
Right Ext.USB Conn.

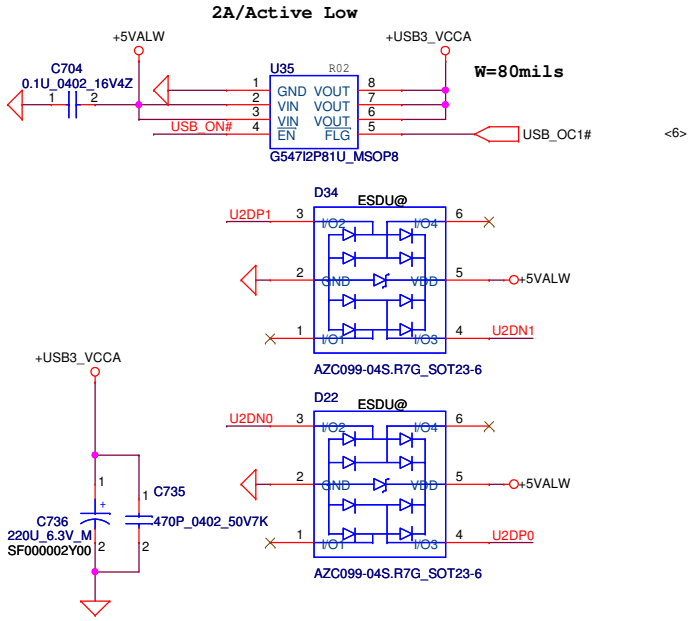


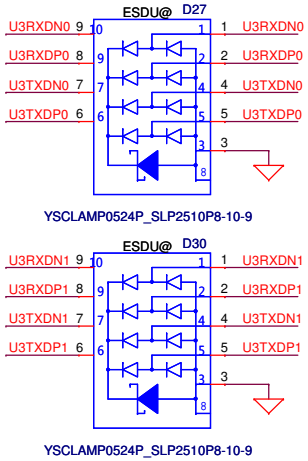












Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Compal Electronics, Inc.

Title: USB2.0 / USB3.0 / BT

Size: B | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 27 of 48

Vcc	3.3V +/- 5%				
R1562	100K +/- 5%				
Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

U44 KB9012QF-A3_LQFP128_14X14
Part Number = SA00004OB30

LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI

Pull high in APU side

Pull high in ODD side

For share ROM need

Security Classification	Compal Secret Data		
Issued Date	2012/04/22	Deciphered Date	2015/04/22

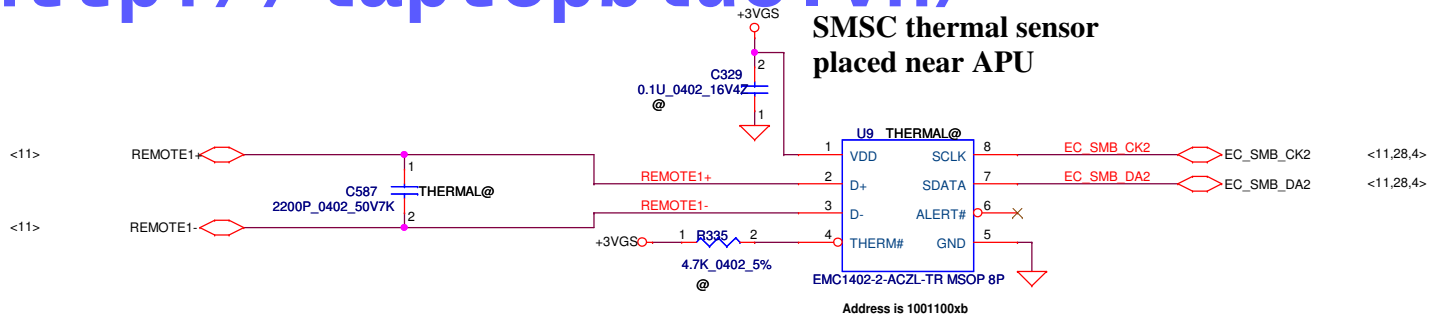
Compal Electronics, Inc.

Title: EC ENE KB930/9012

Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

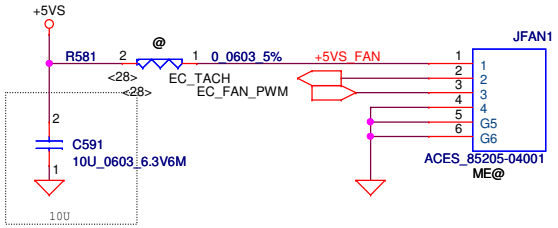
Date: Thursday, March 28, 2013 | Sheet 28 of 48

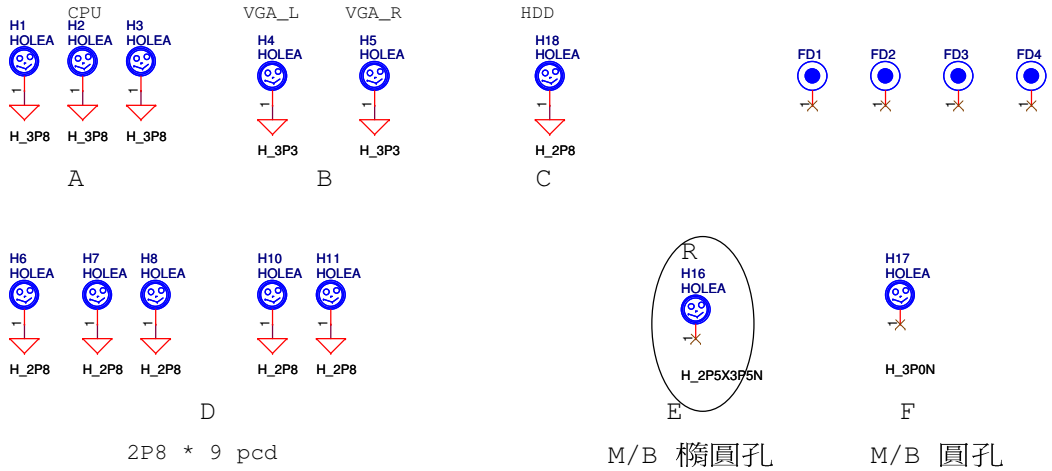
SMSC thermal sensor placed near APU



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn





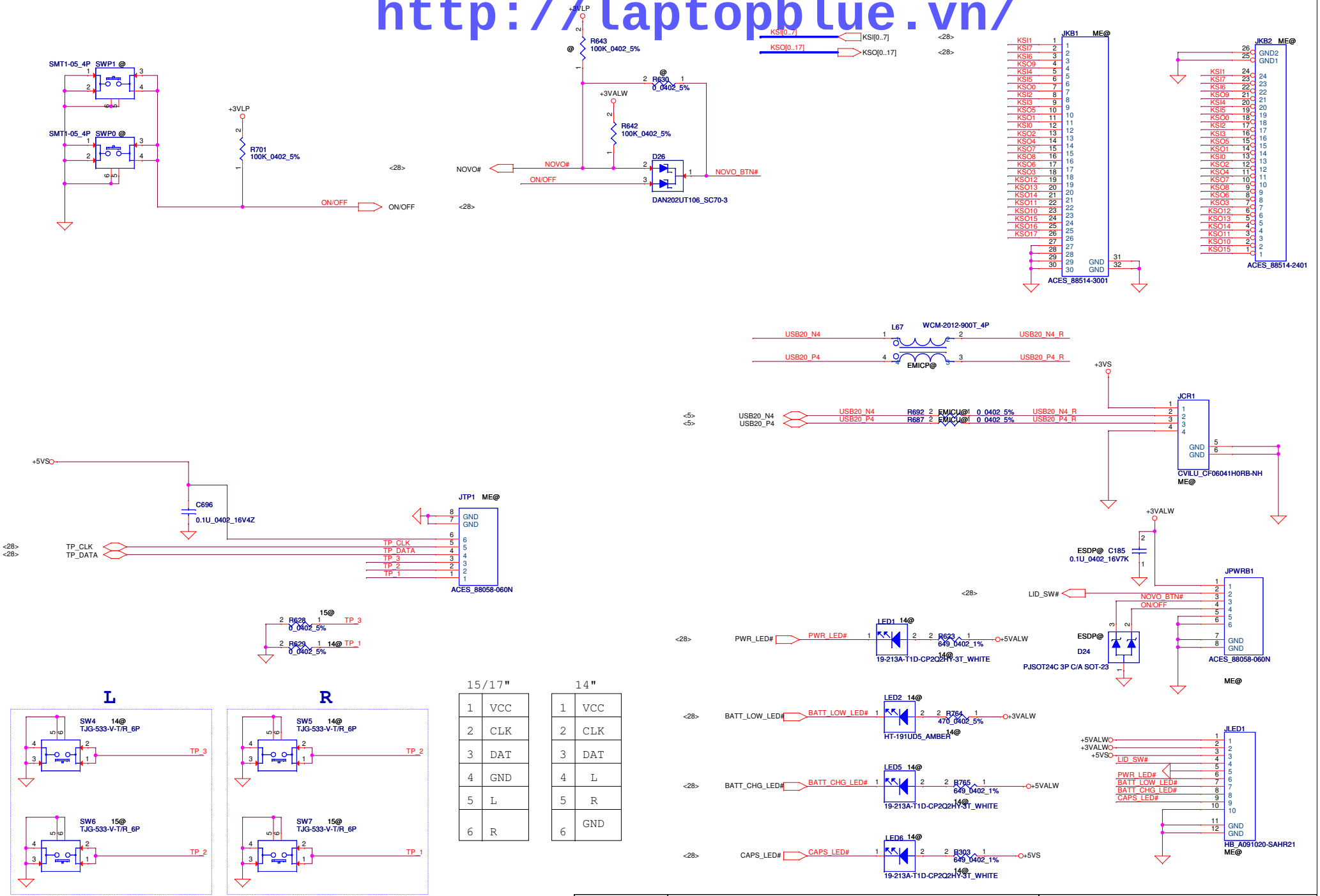
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size: B | Document Number: **VAWGA/GB** | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 29 of 48



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Title: BIOS, I/O Port & K/B CONN/TP CONN/PBTN

Size	Document Number	Rev
B	VAWGA/GB	1.0

Date: Thursday, March 28, 2013 Sheet 30 of 48

Sense resistors must be connected same power that is used for VAUX_3.3

AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

CA3 vendor suggest change to 2.2U

mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

Don't support LINE_IN function RA7 could be @

Should be same supply rail as used for PCH HDA bus controller section

Layout Note:Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

10 mils

Please bypass caps very close to device.

HGNDA, HGNDB 80mils

For EMI

Combo Jack (Normal Open)

Universal Jack

External MIC

Internal analog MIC

Headphone

Internal SPEAKER

For Universal jack

CX20751-11Z_QFN40

using wide copper bridge under codec (100 mils or more)

PC Beep

EC Beep

ICH Beep

CA30 vendor suggest change to 2.2U

ESD

Place colose to Codec chip

CA41 vendor suggest change to 1U

LA1~LA4 vendor suggest mount 0 ohm first~ Bead reserve for EMI if needed

wide 30MIL

vendor suggest change to 1000p

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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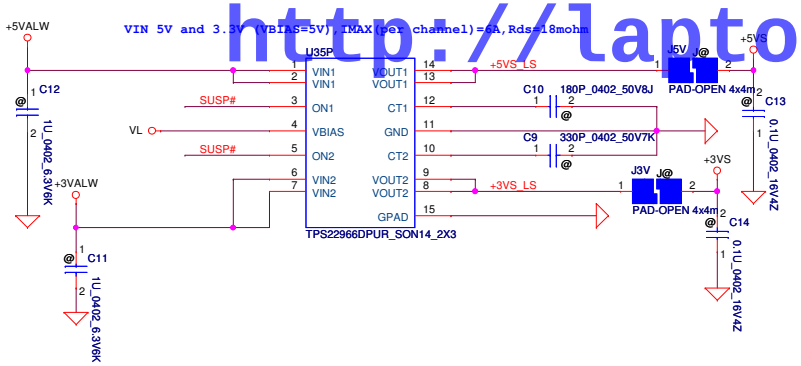
Compal Electronics, Inc.

Title: CX20751 Codec

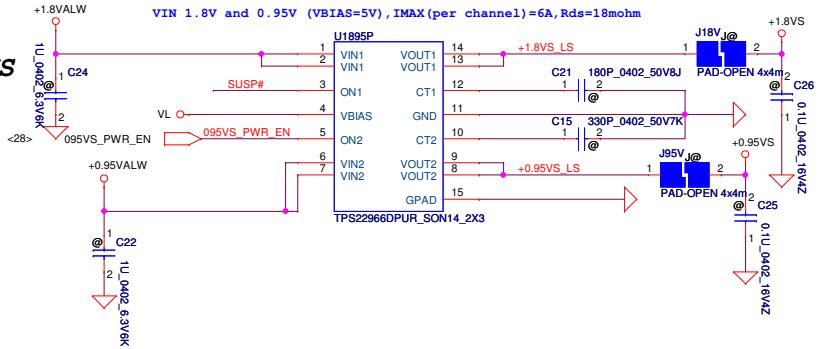
Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

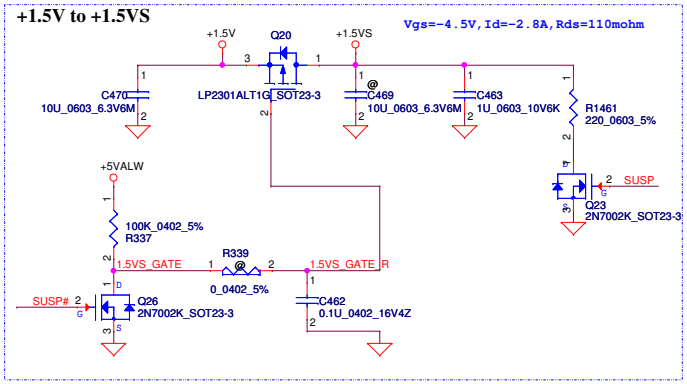
Date: Thursday, March 28, 2013 | Sheet 31 of 48

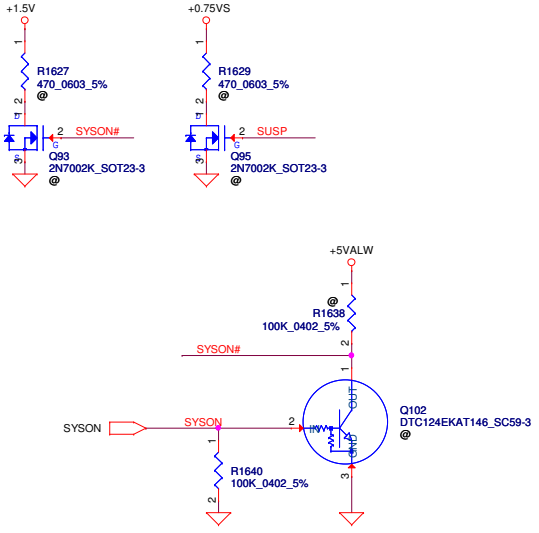
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch

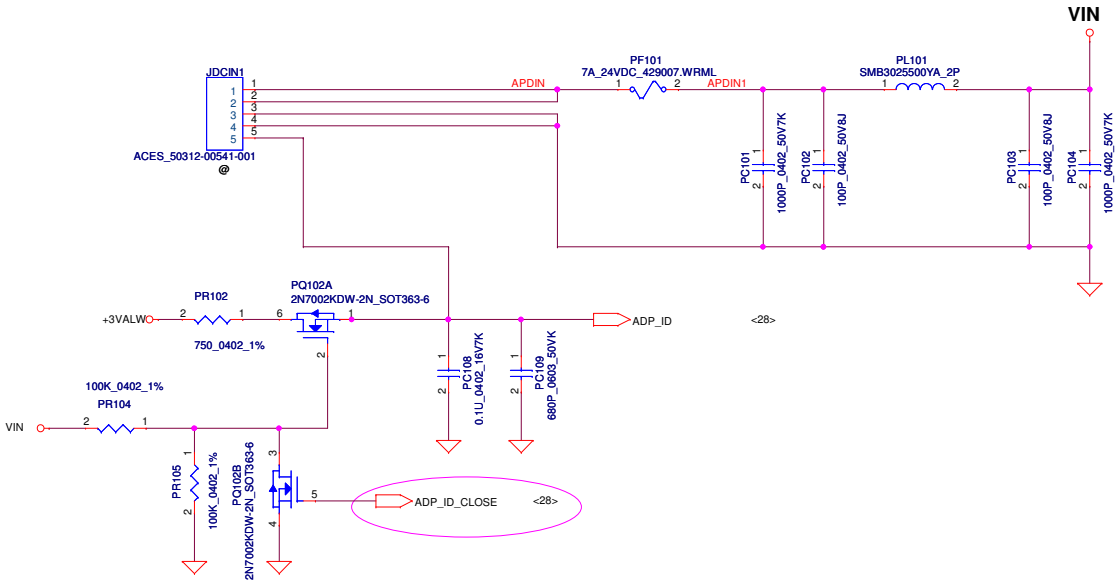


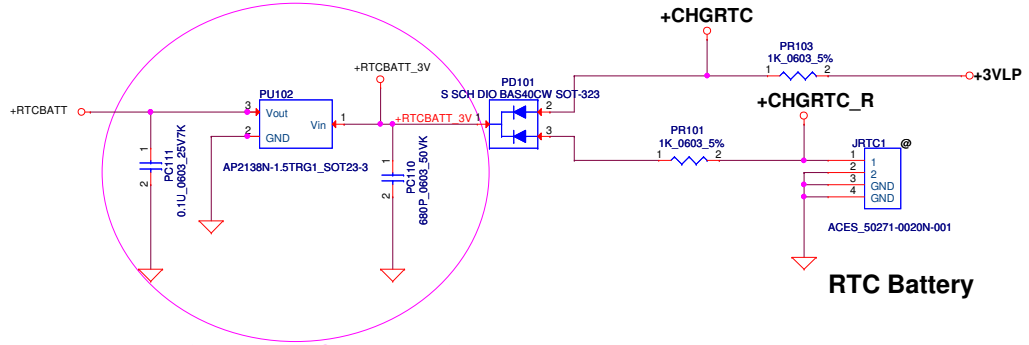




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date	2015/04/22

Title	DC Interface		
Size B	Document Number VAWGA/GB		Rev 1.0
Date: Thursday, March 28, 2013	Sheet 32 of 48		





Need use+3.3V transfer to +1.5V LDO to APU side for Kaibini

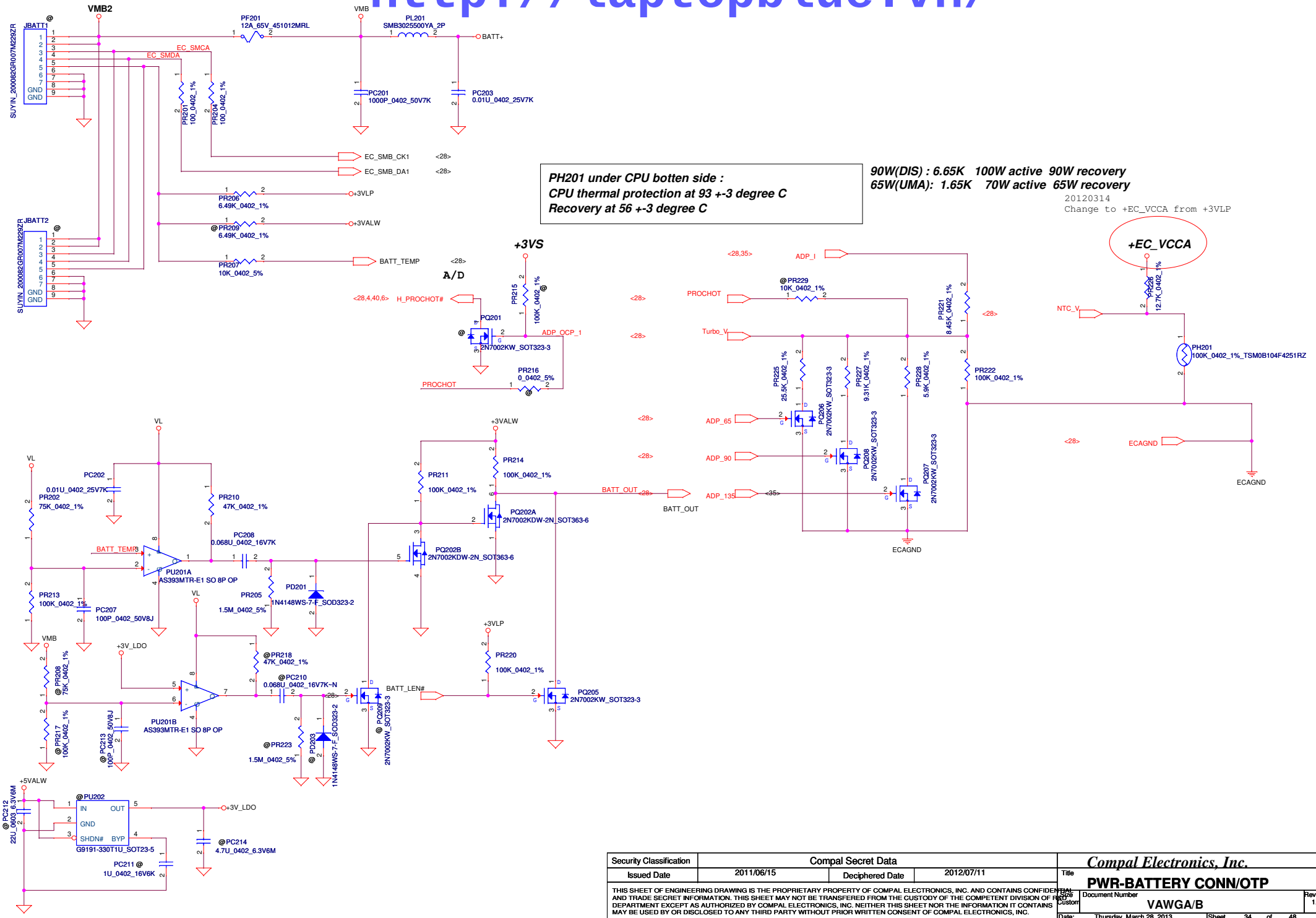
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-DCIN / RTC Battery

Size: Custom | Document Number: VAWGA/B | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 33 of 48



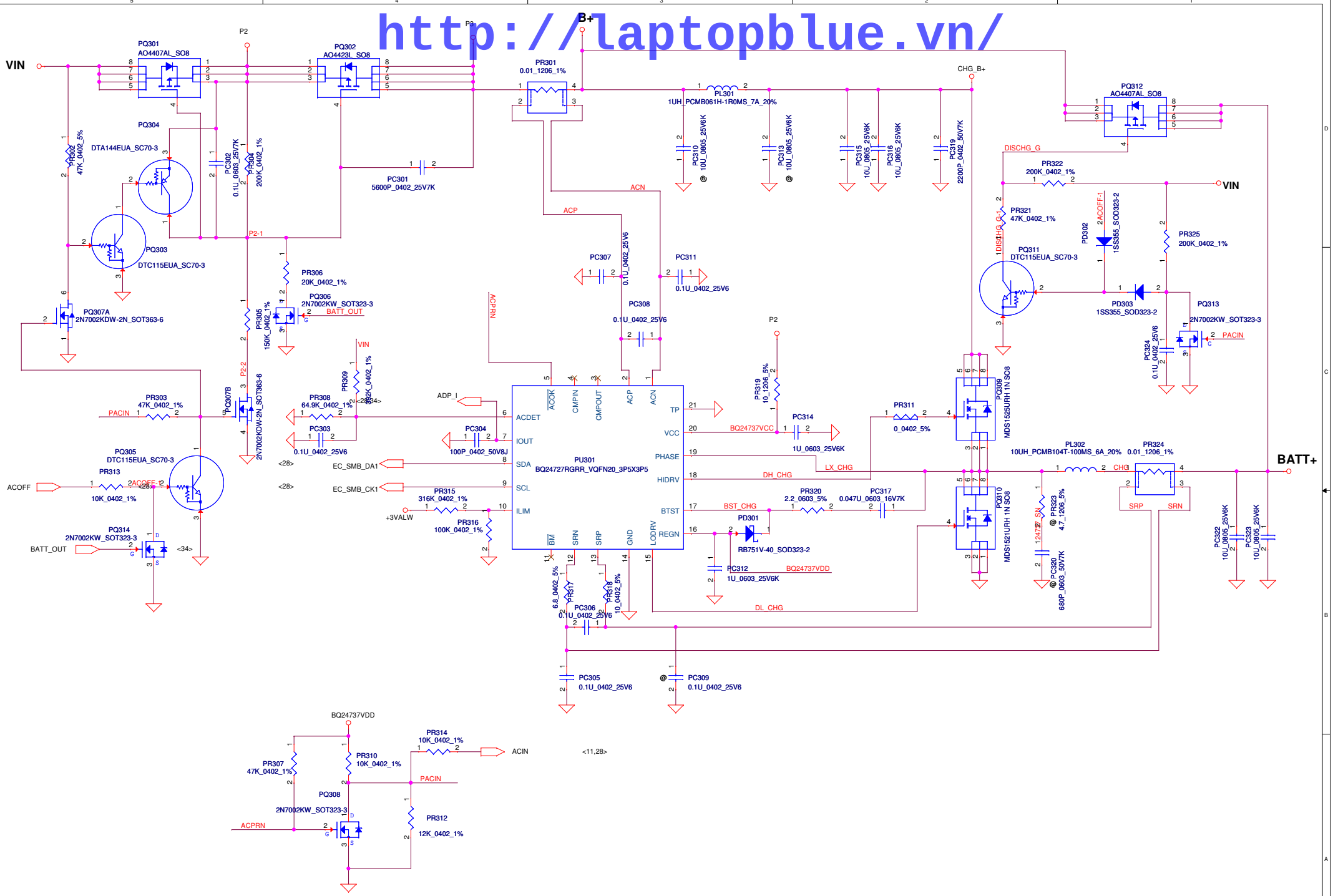
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

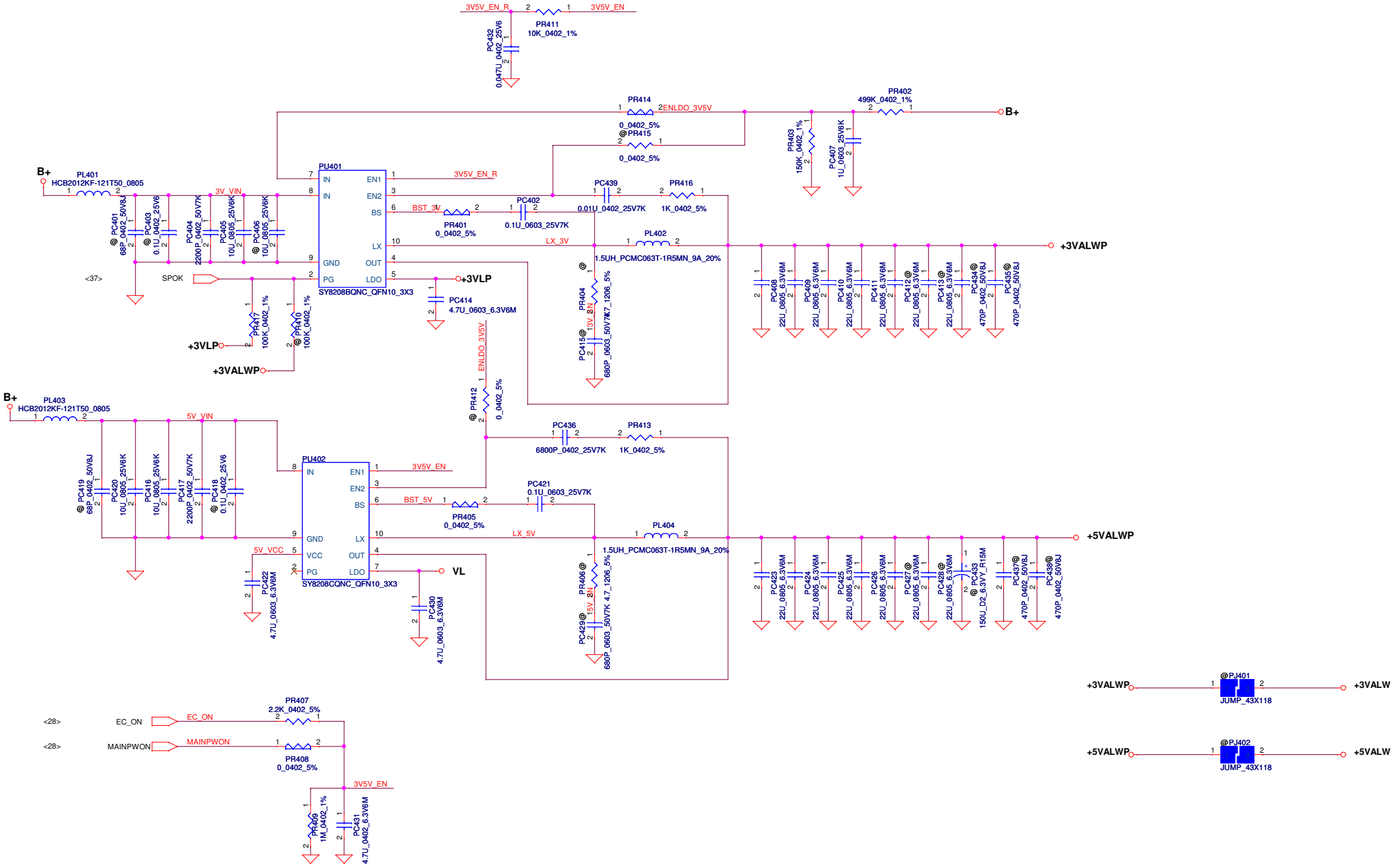
Size: Custom | Document Number: VAWGA/B | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 34 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PWR-CHARGER		
Size	Document Number	VAWGA/B	Rev 1.0
Date: Thursday, March 28, 2013	Sheet 35 of 48		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

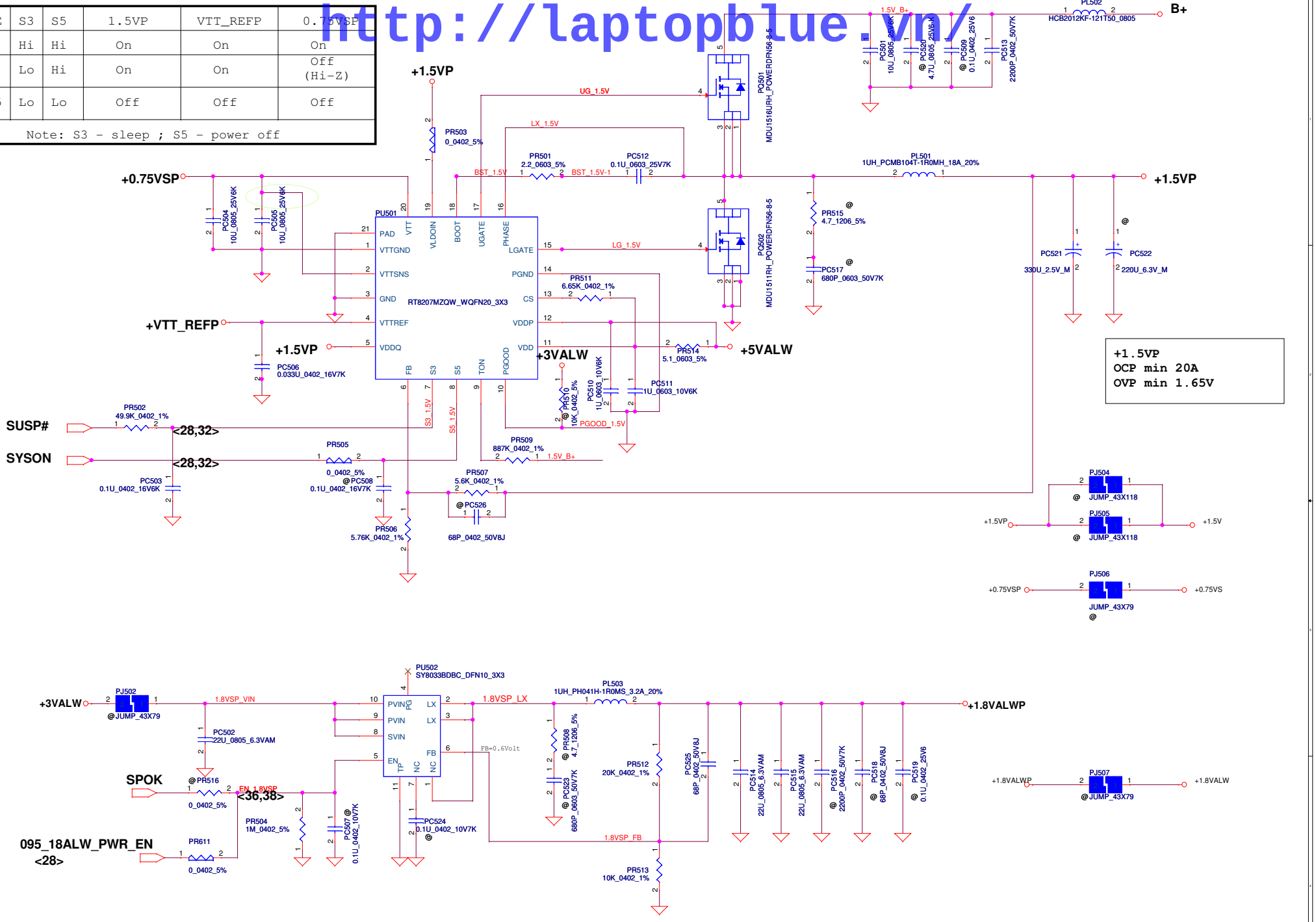
Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Size: Custom | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 36 of 48

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



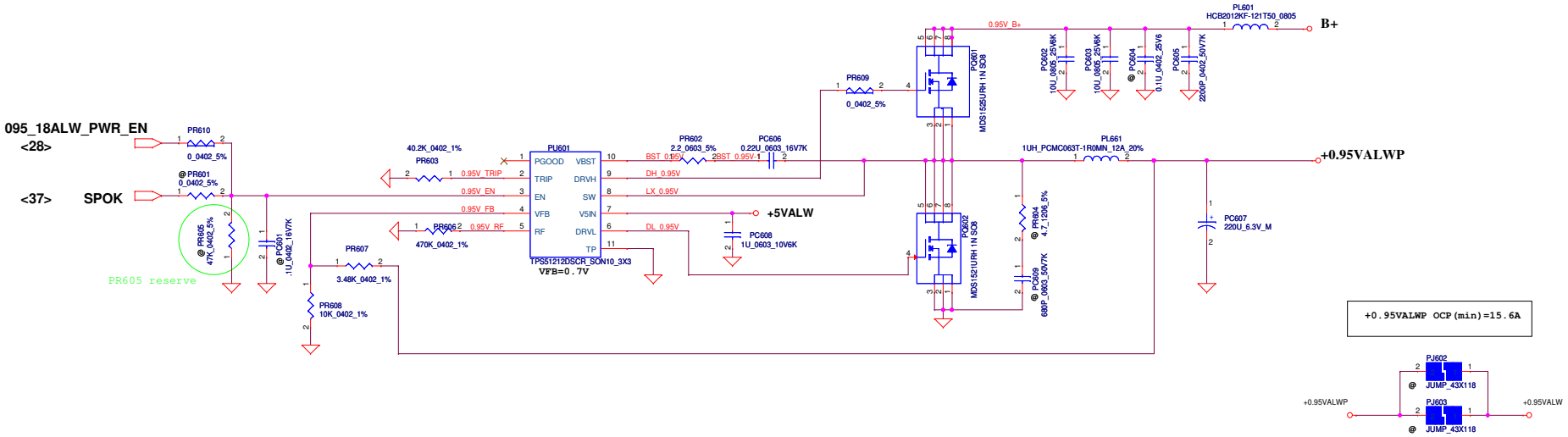
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PWR-+1.5VP/+1.8VALWP**

Size: Custom | Document Number: **VAWGA/GB** | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 37 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

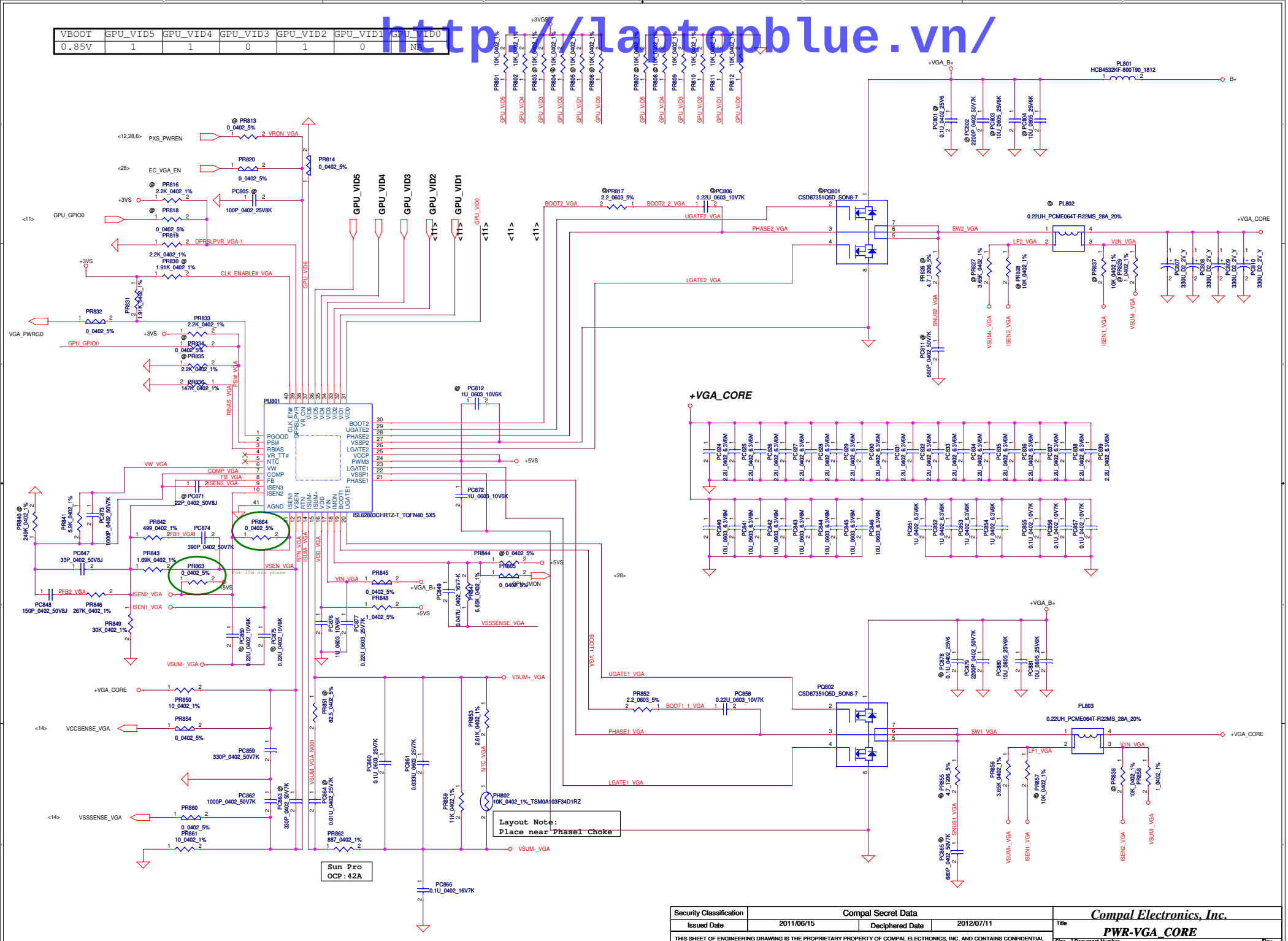
Compal Electronics, Inc.

Title: **PWR-+0.95VALWP**

Size	Document Number	Rev
C	VAWGA/B	1.0

Date: Thursday, March 28, 2013 Sheet 38 of 48

VBOOT	GPU_VID5	GPU_VID4	GPU_VID3	GPU_VID2	GPU_VID1	GPU_VID0
0.85V	1	1	0	1	0	NC



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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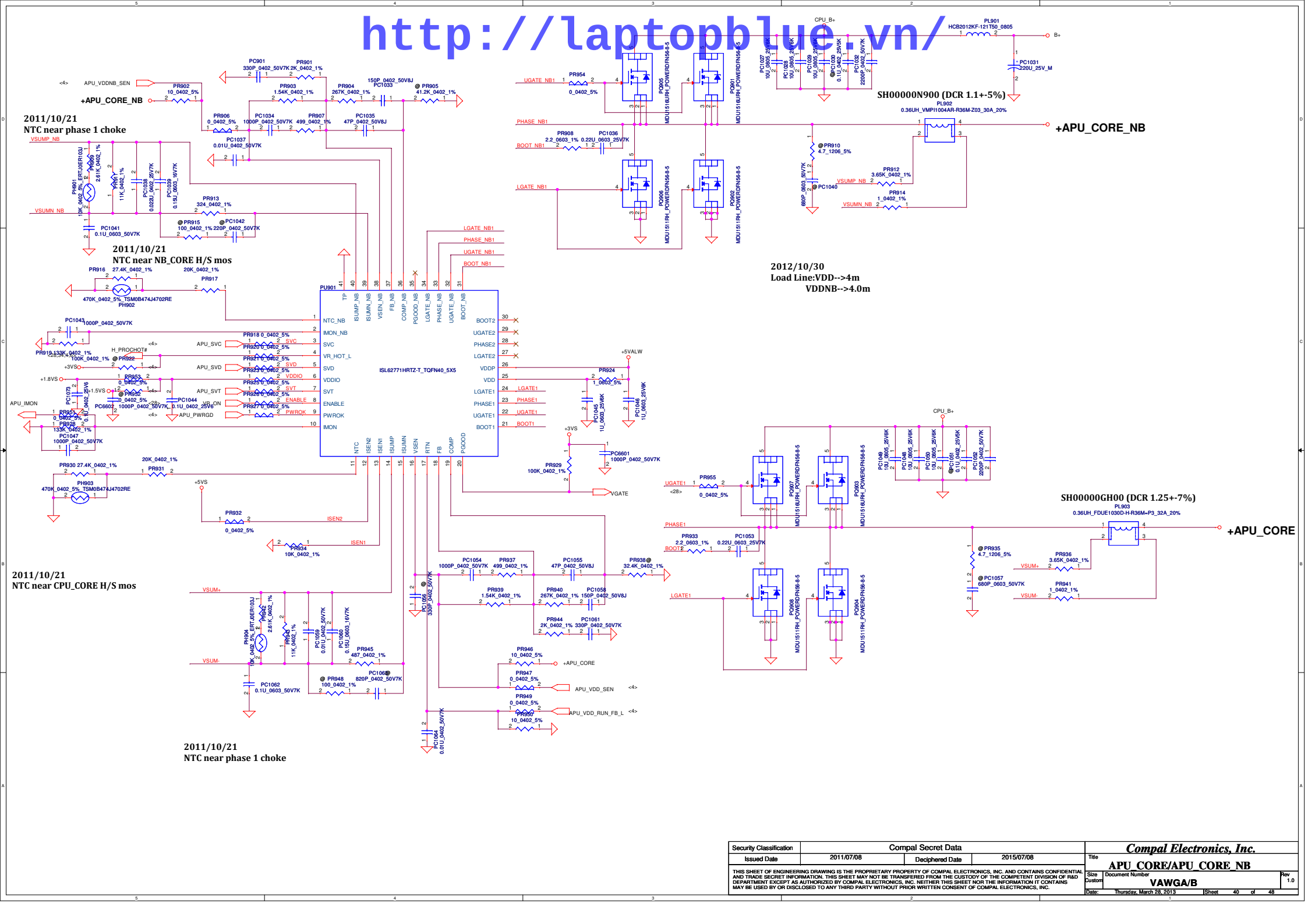
Compal Electronics, Inc.

Title: **PWR-VGA_CORE**

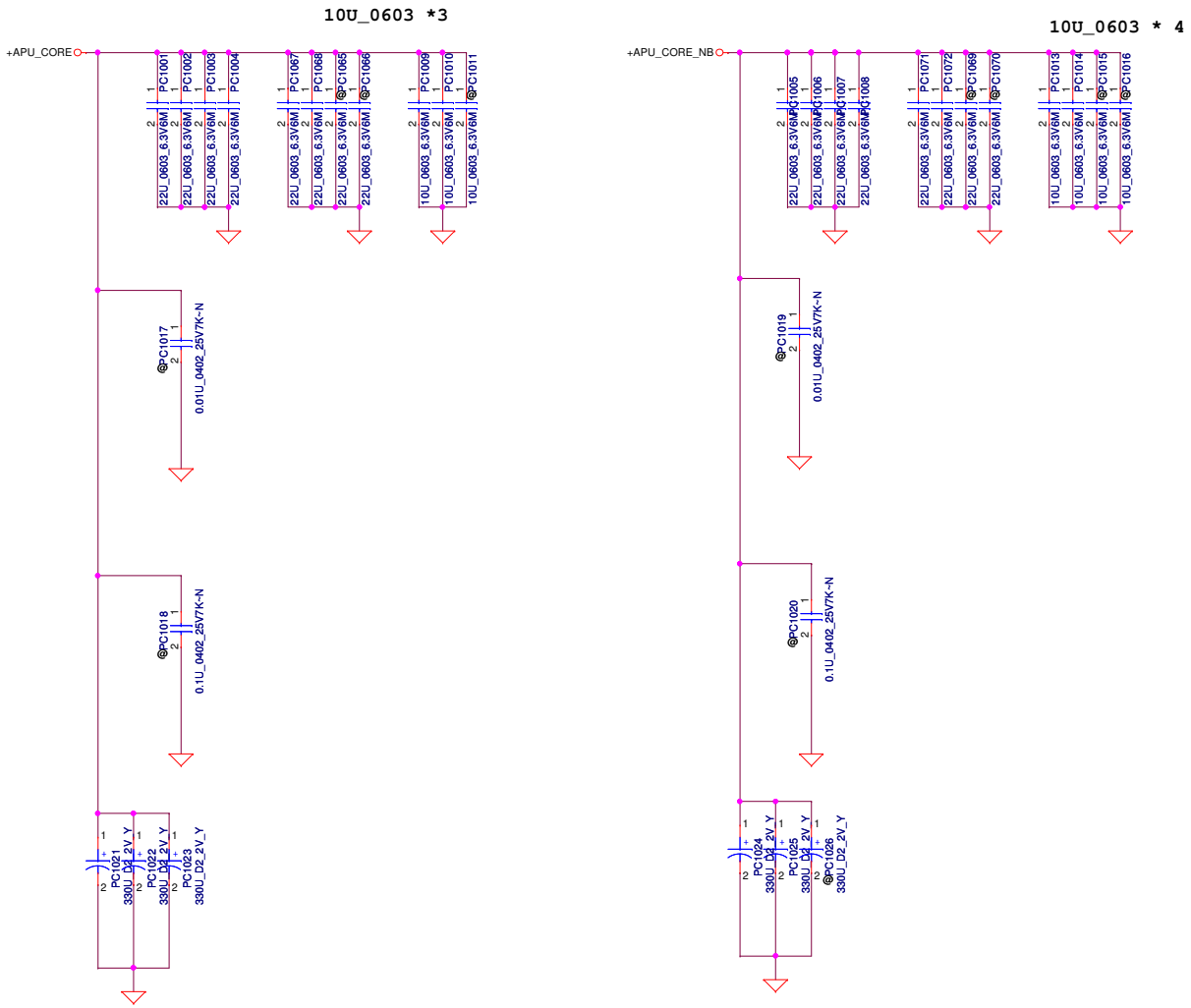
Size: C | Document Number: VAWGA/GB | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 39 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title	APU_CORE/APU_CORE_NB		
Size: Custom	Document Number: VAWGA/B		Rev: 1.0
Date: Thursday, March 28, 2013	Sheet 40 of 48		



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWR-PROCESSOR DECOUPLING

Size: Custom	Document Number: VAWGA/B	Rev: 1.0
Date: Thursday, March 28, 2013	Sheet 41 of 48	

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 1.0

Date: Thursday, March 28, 2013 | Sheet 42 of 48

Item	Reason for change	PG#	Modify List	Date	Phase
1	For share rom	28	Change SYS_PWRGD_EC from pin 86 to pin 32	12/17	DVT
2	For 095VS_PWR_EN pull down	28	Add R207	12/17	DVT
3	For VBIAS first raise up	12, 32	Change U1895V, U35P, U1895P VBIAS from +5VALW to VL	12/17	DVT
4	For follow VIWGP design	27	Change JUSB3 pin define	12/18	DVT
5	For Audio Precision	31	Change CA36, CA46 from 1U to 2.2U	12/21	DVT
6	For SYS_PWRGD_EC pull down	28	Add R208	12/24	DVT
7	For share rom	28	Change R1575, R1576 to 100K	12/24	DVT
8	For reserve EC +3VL	28 05	Add J11, J12 and modify +3VALW to +3V_EC	12/24	DVT
9	For share ROM	05	modify ROM net-name & resistor value	12/24	DVT
10	For common VIWGP design	22	modify R106, R107 to 22ohm	12/24	DVT
11	For power S3 reduction	28	Change EC_INVT_PWM to ADP_ID_CLOSE	12/25	DVT
12	For common VIWGP design	23	Change JODD1 symbol	12/27	DVT
13	For reserve wake on wlan function	26	Add R1500	12/27	DVT
14	For 1.5VS discharge	32	Change R339 to 0ohm, mount Q23 & R1461	12/29	DVT
15	For AMD suggest	4	Change R576 to 0ohm	12/29	DVT
16	For VGA sequence	12	Delete R123 & C40, change C28, C27 to 2200P	12/29	DVT
17	For +3VALW APU Power Consumption	7	Add R582	01/03	DVT
18	For ESD request	22 28 40	Add C600, C601, PC6601, PC6602	01/03	DVT
19	For no support DC wake & LID function	28	Pull high only SMB & RST use +3V_EC, other use +3VALW	01/04	DVT
20	For reserve cost down experiment	30	Add R630, R643	01/04	DVT
21	For Common VIWGP	30	Change SW4,SW5,SW6,SW7 footprint	01/04	DVT
22	For instant plug/unplug AC has beep sound	31	@RA22	01/04	DVT
23	For Crystal Capactance fine tune	5 6 12	Modify C794,C795,C682,C686,CV36,CV37 value	01/09	DVT

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EMI request	30	Change L67 to EMICP@, Change R692,R687 to EMICU@	02/02	PVT
2	For Share ROM recoverable solution as original method	05	Add RP12	02/02	PVT
3	For BIOS post time	06	Pull high PXS_PWREN to +3VS by RP14	02/02	PVT
4	For ZiZi noise	31	Change AVDD_HP from +3VS to +3VLP	02/02	PVT
5	For follow KABINI latest CRB	04	@ R576,C164,C342	02/02	PVT
6	For APU control PWM only	21	Delete R1465	02/02	PVT
7	For Corret Net-name to prevet confuse	04 21	Change TL_INVT_PWM, TL_ENVDD to APU_INVT_PWM, APU_ENVDD	02/02	PVT
8	For Reserve DDC CLK DATA pull high	22	Add R693, R697	02/02	PVT
9	For Common Intel project	30	Change R623,R765,R303 to 620ohm	02/02	PVT
10	For Common Intel project	23	Reserve R551	02/02	PVT
11	For reduce BOM	31	Delete RA3, and Change RA4 to short-pad	02/05	PVT
12	For reduce BOM	26	Change R1498,R1499 from 0 ohm to 100 ohm	02/05	PVT
13	For reduce BOM	11 12 13 14	Change RV43,LV1,LV2,LV3,LV4,LV5,LV6,RV16,RV17,LV7,LV8,LV9,LV10 to short-pad	02/05	PVT
14	For better location	14 18 19	CV72 <-> CV171 ; CV60 <-> CV70 ; CV154 <-> CV191	02/05	PVT
15	For reduce BOM	21	Change R1463 from 0 ohm to short-pad	02/06	PVT
16	For better audio precision performance	31	Change CA27,CA28 from 1U to 2.2U	02/08	PVT
17	For reduce BOM & layout concern	07	Delete C195	02/16	PVT
18	For test point request	22	Add T49, T58 on JCRT1	02/18	PVT
19	For ESD request	25	Add C173, C178	02/18	PVT
20	For reduce BOM	05	Change R112, R115, R116, R119, R125, R126 to short-pad	02/18	PVT
21	For Crystal timming	06	Change C682 from 18P to 22P	02/20	PVT
22	For ESD request	30	Change D24 from ESDU@ to ESDP@, Part number from SCA00000E00 to SCA00001G00	02/23	PVT
23	For EMI request	21 27 30	Change L58,L51,L55,L66,L67 from SM070000K00 to SM070000Z00	02/23	PVT

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Item	Reason for change	PG#	Modify List	Date	Phase
1	For Common Intel project	30	Change R623,R765,R303 to 649ohm	03/05	PreMP
2	For VGA Clock Request	06	Reserve R578,R689	03/05	PreMP
3	For Reduce BOM	05	Change R103, R104 to short-pad	03/11	PreMP
4	For Reduce BOM	21	Change R696, R695, R813 to short-pad	03/11	PreMP
5	For Reduce BOM	23	Change R550 to short-pad	03/11	PreMP
6	For Reduce BOM	28	Change R1564 to short-pad	03/11	PreMP
7	For Reduce BOM	29	Change R581 to short-pad	03/11	PreMP
8	For Reduce BOM	31	Change RA11 to short-pad	03/11	PreMP
9	For Reduce BOM	32	Change R339 to short-pad	03/11	PreMP
10	For Reduce BOM	06	Change R121 to short-pad	03/11	PreMP
11	For Reduce BOM	07	Change R582 to short-pad	03/11	PreMP
12	For ESD require	30	Add C185	03/25	PreMP
13	For Module Design	22	Change R693, R697 from 10k to 4.7k	03/25	PreMP
14	For ESD require	04	Add C195	03/26	PreMP
15	For Reduce BOM	04	@ RP11	03/26	PreMP
16	For Board ID	28	@ R1562 and change R1564 to 0ohm	03/28	PreMP
17					

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Mars XT VRAM STRAP

	Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
2G	K4W2G1646E-BC1A SA000068U00	0	0	0	RV20 NC	RV27 4.75K
	MT41J128M16JT-093G:K SA000067500	0	0	1	RV20 8.45K	RV27 2K
	H5TQ2G63DFR-N0C SA000065300	0	1	0	RV20 4.53K	RV27 2K
1G	H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
	K4W1G1646G-BC11 SA00004GS00	0	1	1	RV20 6.98K	RV27 4.99K
	H5TQ1G63EFR-11C SA000041SB0	1	1	1	RV20 4.75K	RV27 NC

MS2G@ X7646738L01
MM2G@ X7646738L02
OLDMH2G@ X7646738L09
NEWMH2G@ X7646738L10
MS1G@ X7646738L03
MH1G@ X7646738L04

SUN PRO VRAM STRAP

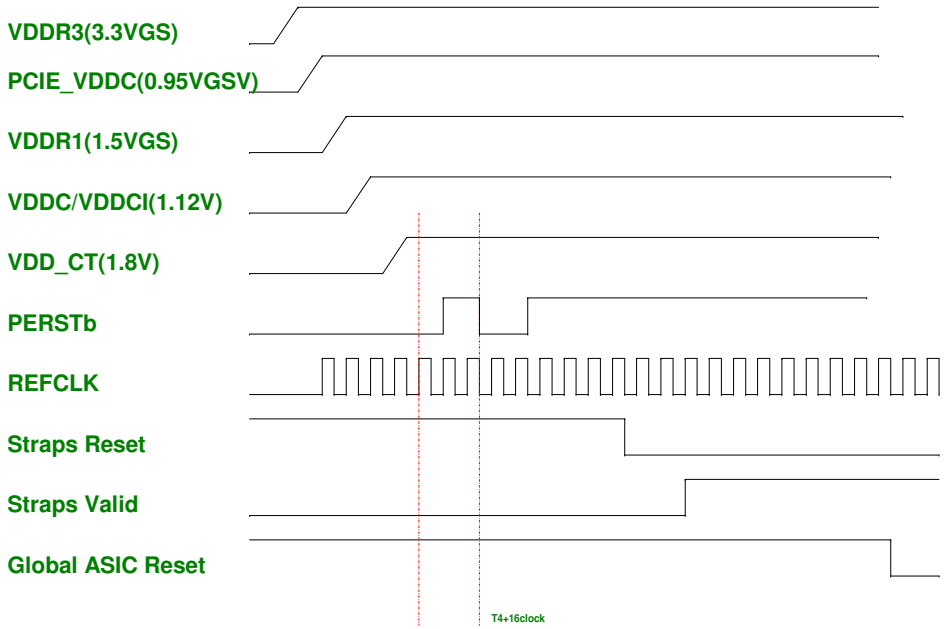
	Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
2G	K4W4G1646B-HC11 SA000068R00	0	0	0	RV20 NC	RV27 4.75K
	MT41K256M16HA-107G:E SA000065D00	0	0	1	RV20 8.45K	RV27 2K
	H5TQ4G63MFR-11C SA00006DG00	0	1	0	RV20 4.53K	RV27 2K
1G	K4W2G1646E-BC1A SA000068U00	0	1	1	RV20 6.98K	RV27 4.99K
	MT41J128M16JT-093G:K SA000067500	1	1	0	RV20 3.4K	RV27 10K
	H5TC2G63FFR-11C SA00006H400	1	0	0	RV20 4.53K	RV27 4.99K
	H5TQ2G63DFR-N0C SA000065300	1	1	1	RV20 4.75K	RV27 NC

SS2G@ X7646738L05
SM2G@ X7646738L06
SH2G@ TBD
SS1G@ X7646738L07
SM1G@ X7646738L08
NEWSH1G@ X7646738L13
OLDSH1G@ X7647538L01

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



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Issued Date	2011/06/15	Deciphered Date 2012/07/11	Title: VGA Notes List
			Size: Custom; Document Number: VAWGA/GB; Rev: 1.0
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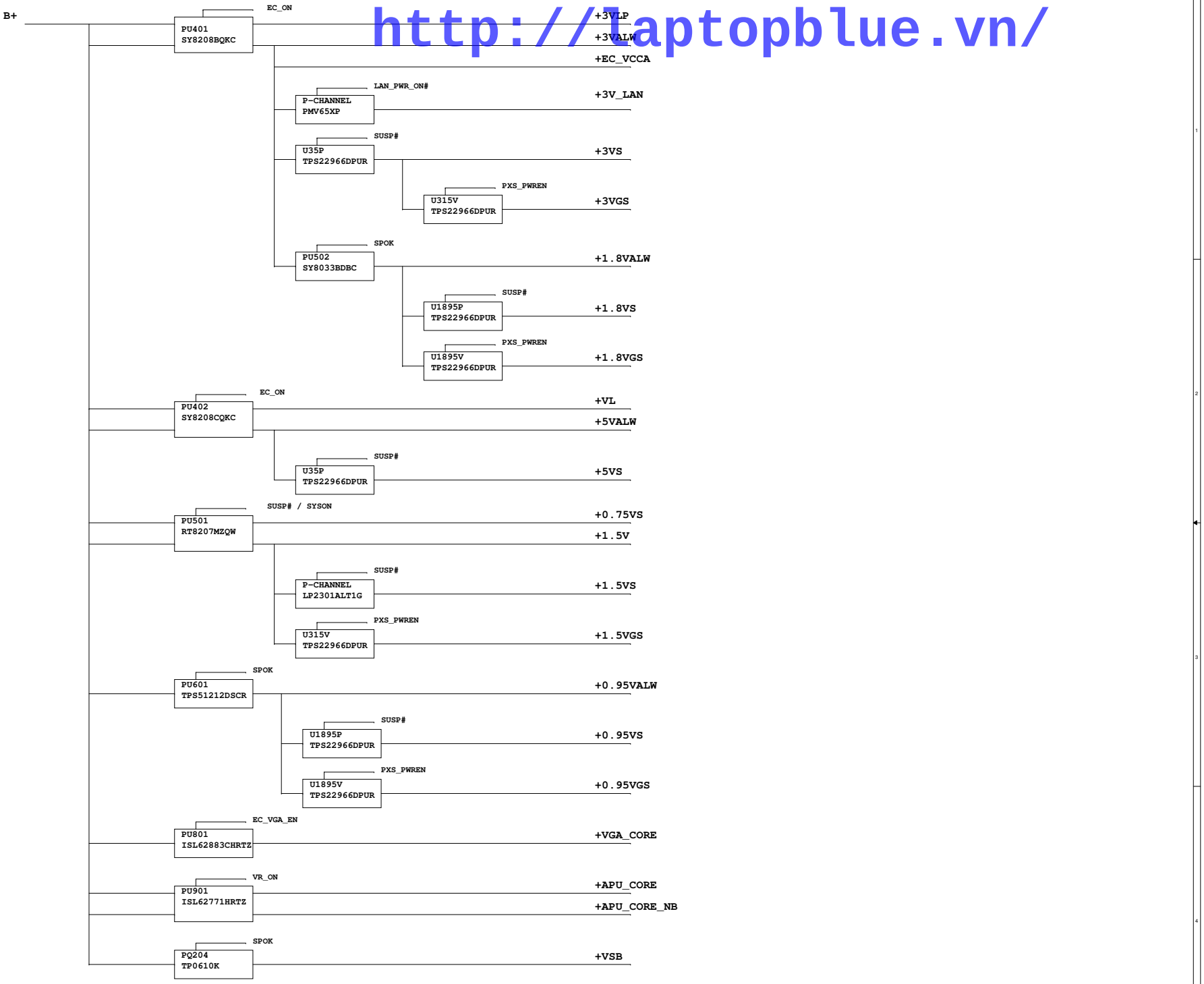

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **Power Map**

Size	Document Number	Rev
Custom	VAWGA/GB	1.0

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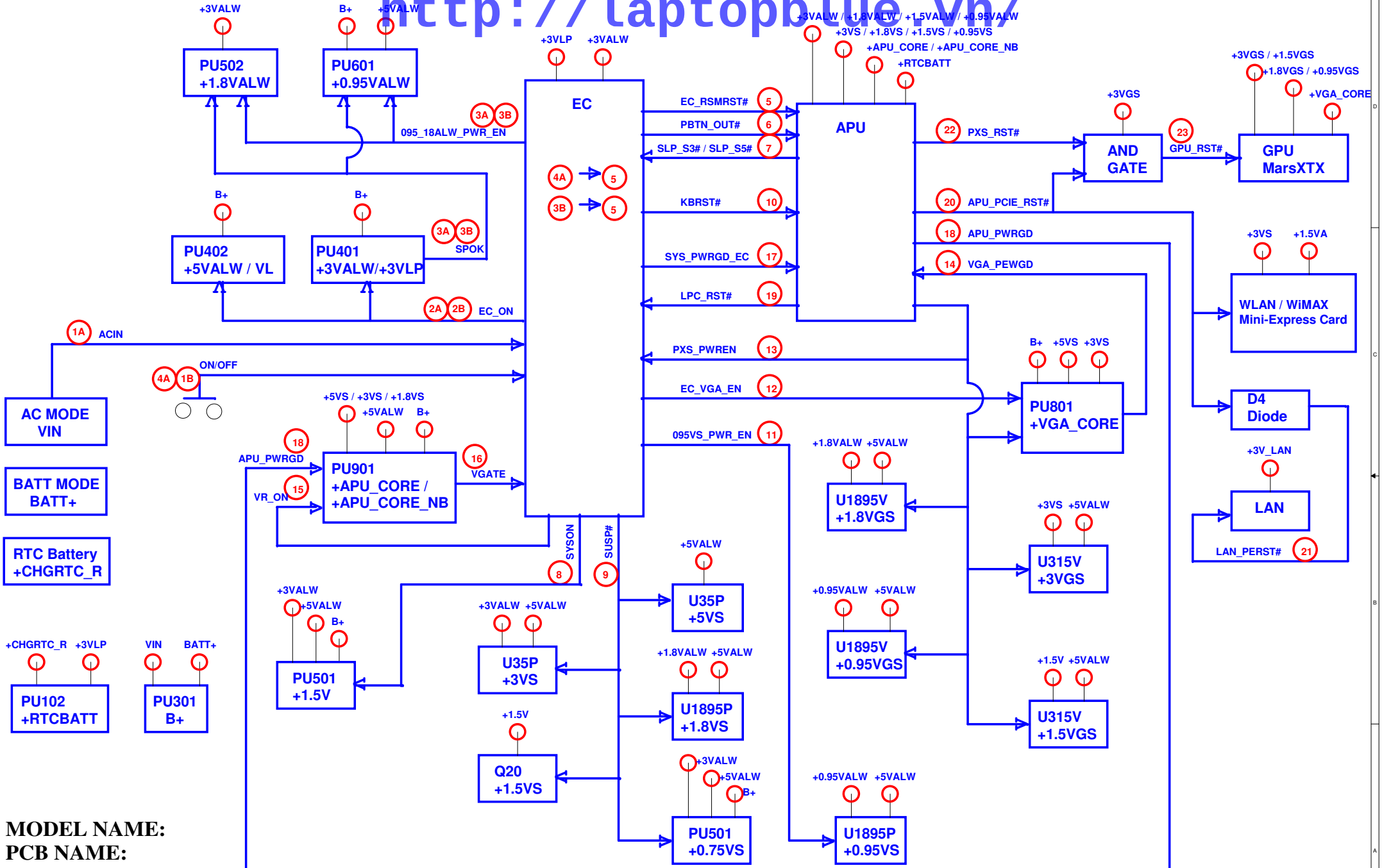

MODEL NAME:
PCB NAME:
REVISION:
DATE: *2011/11/23*

COMPAL CONFIDENTIAL

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Issued Date		Deciphered Date	Title: Power sequence
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Date:		Sheet of	