

Model Name : VILE1 & VILE2
File Name : NM-A043, NM-A044
BOM P/N:

VILE1:

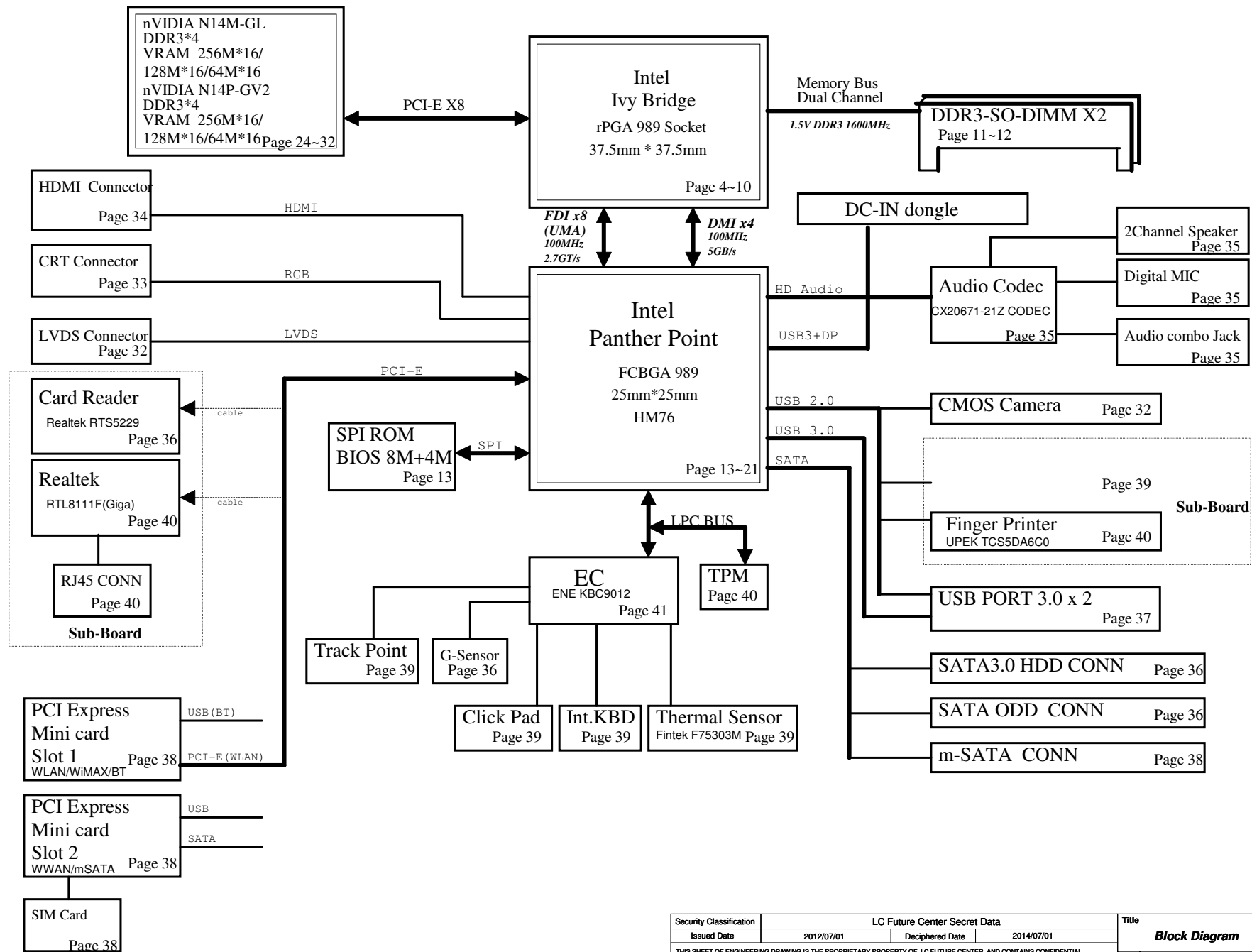
VILE2:

M/B Schematics Document
Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU nVIDIA N14M-GL / N14P-GV2

2012-11-07

REV:0.1

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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0	O	O	O	O	O M3 Supported
S3	O	O	O	X	O M3 Supported
S5 S4/AC	O	O	X	X	O M3 Supported
S5 S4/ Battery only	X	X	X	X	
S5 S4/AC & Battery don't exist	X	X	X	X	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M1001_101xb	

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0 USB 3.0 Port (Left Side)
		1
	UHCI1	2 USB 3.0 Port (Left Side)
		3 USB 3.0 Port
	UHCI2	4 Touch Panel
		5
EHCI2	UHCI3	6
		7
	UHCI4	8
		9 USB Port (Right Side)
	UHCI5	10 Mini Card(WLAN/BT)
		11 FPR
	UHCI6	12 Mini Card(WWAN)
		13 Camera

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
NVidia	DIS@
PCH AUX Power	+3V_PCH@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N14M-GL	N14MGL@
GPU N14P-GV2	N14PGV2@
SIM Card Slot	3G@
Touch Panel	Touch@
Finger Print Board	FP@
SSD	SSD@

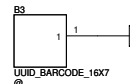
SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

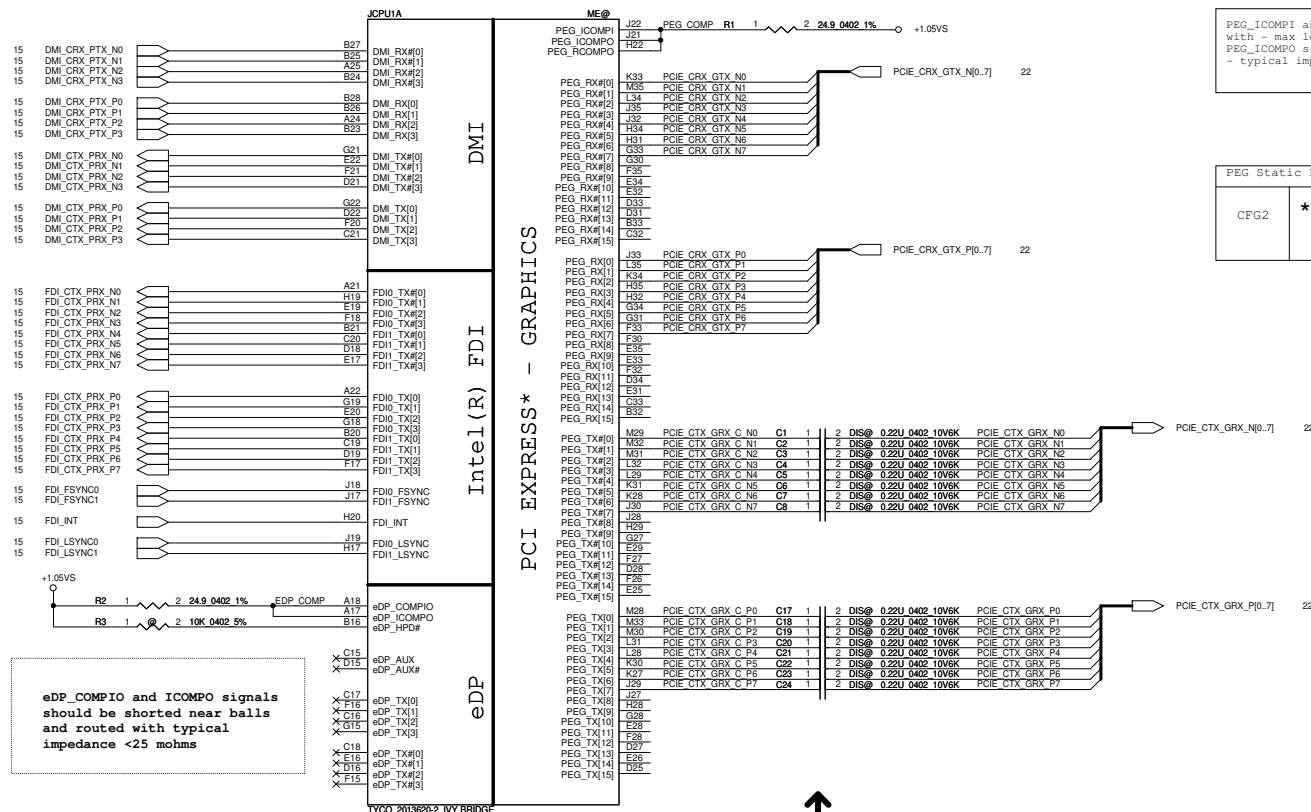
ZZZ5



DA PCB
DA80000TG00
NM-A043



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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

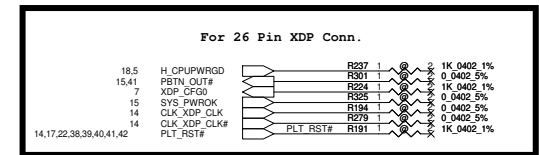
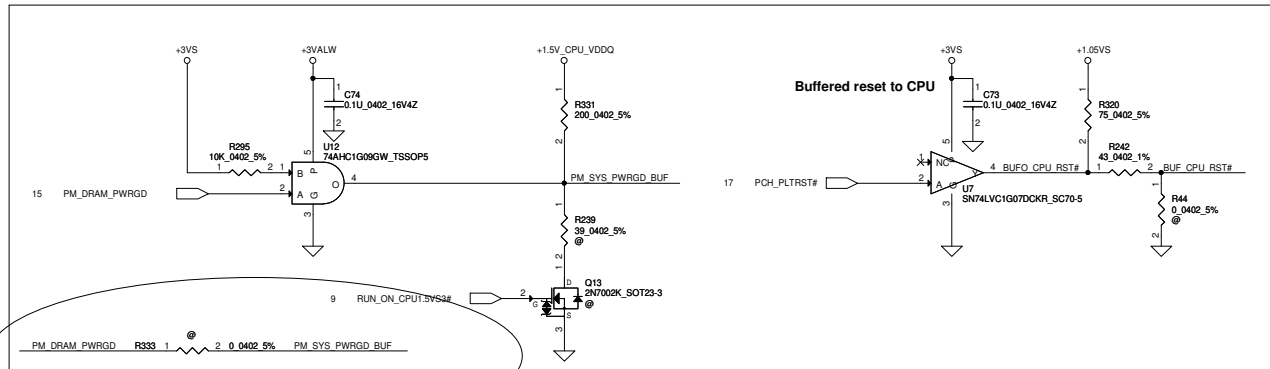
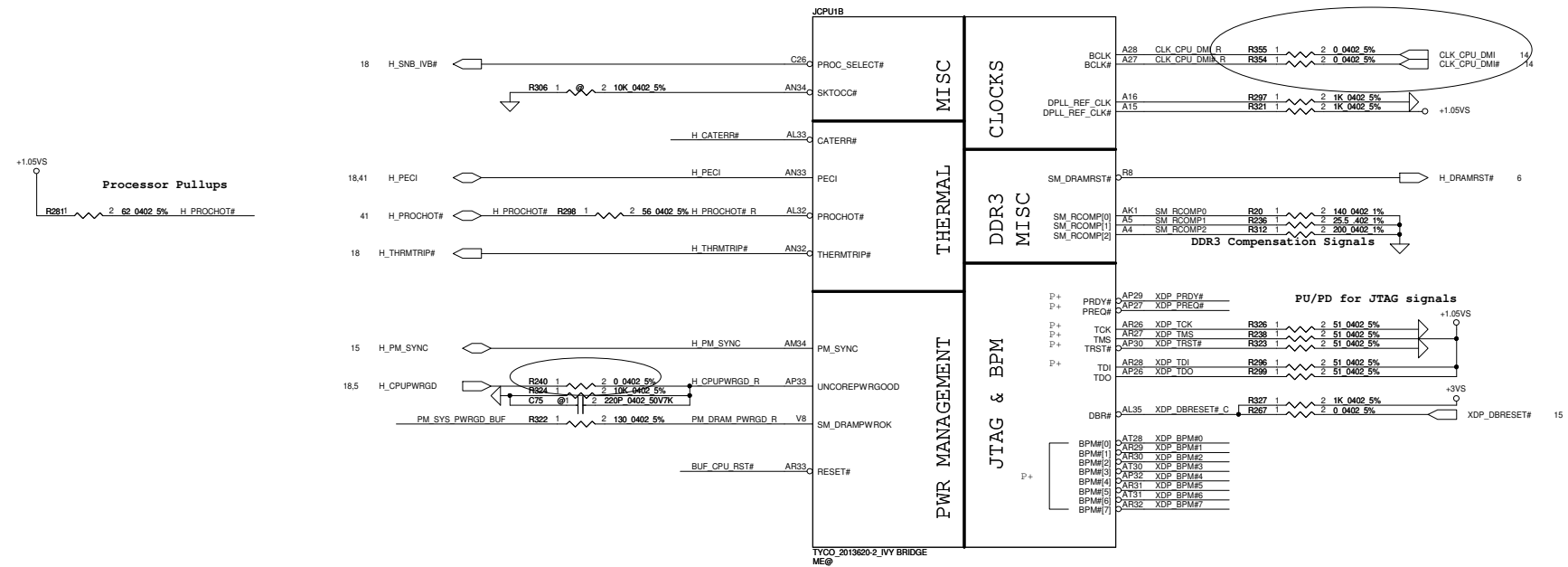
PEG Static Lane Reversal - CFG2 is for the 16x

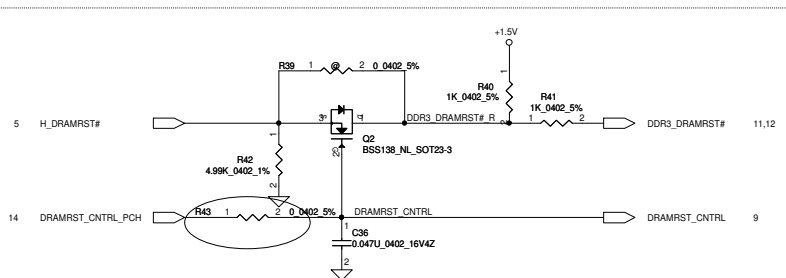
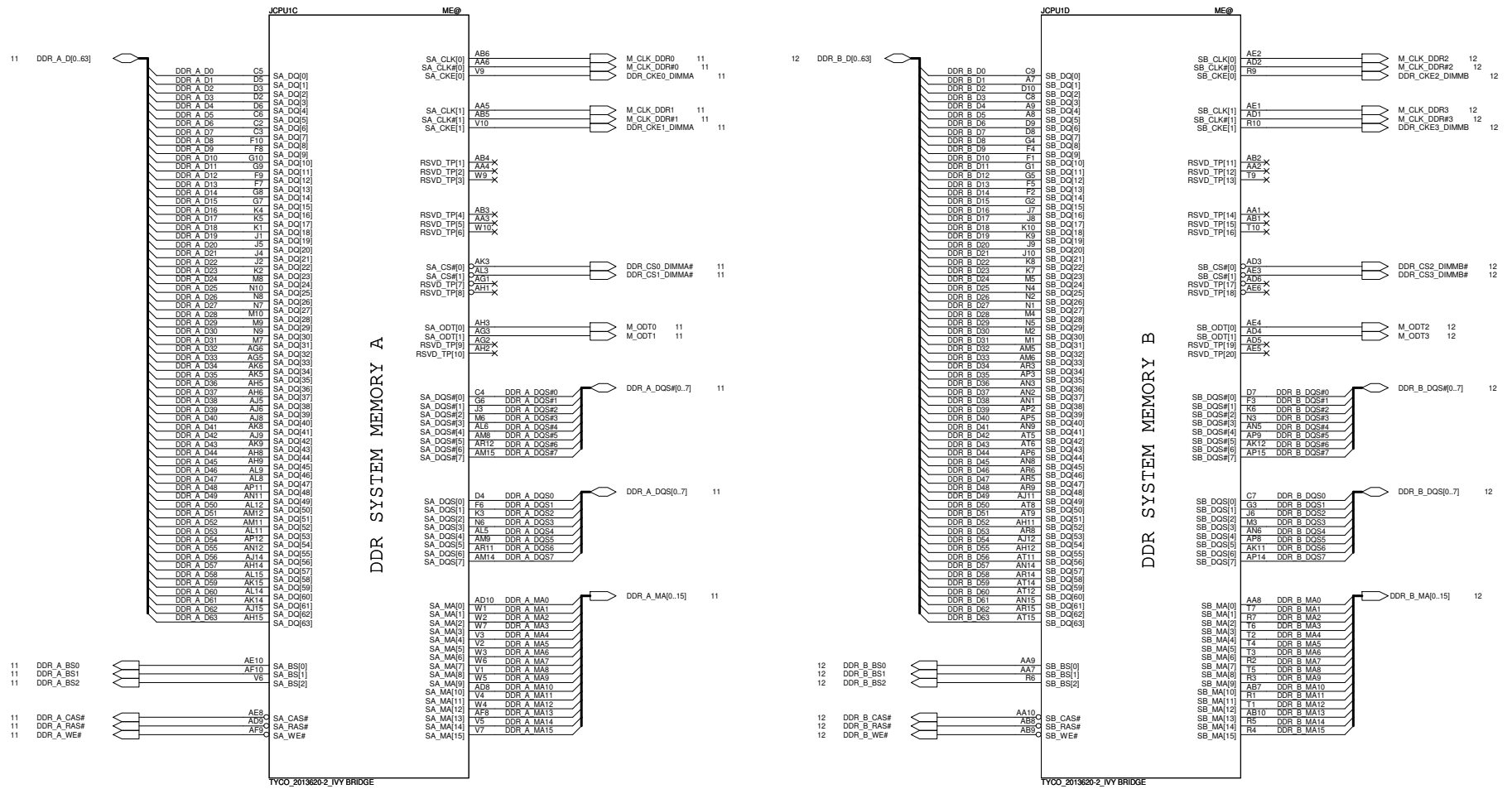
CFG2

- * 1: Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

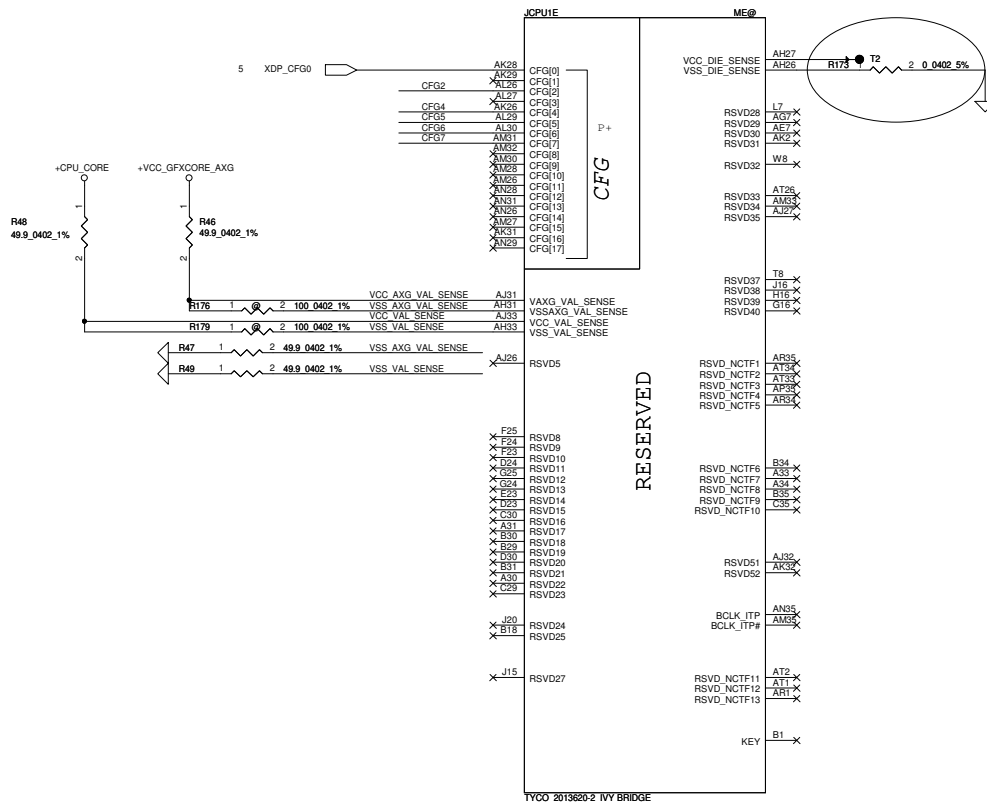
Nvidia support PCIe Gen2

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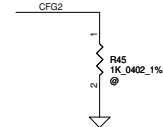




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PEG Static Lane Reversal - CFG2 is for the 16x

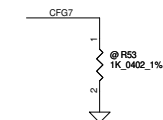


CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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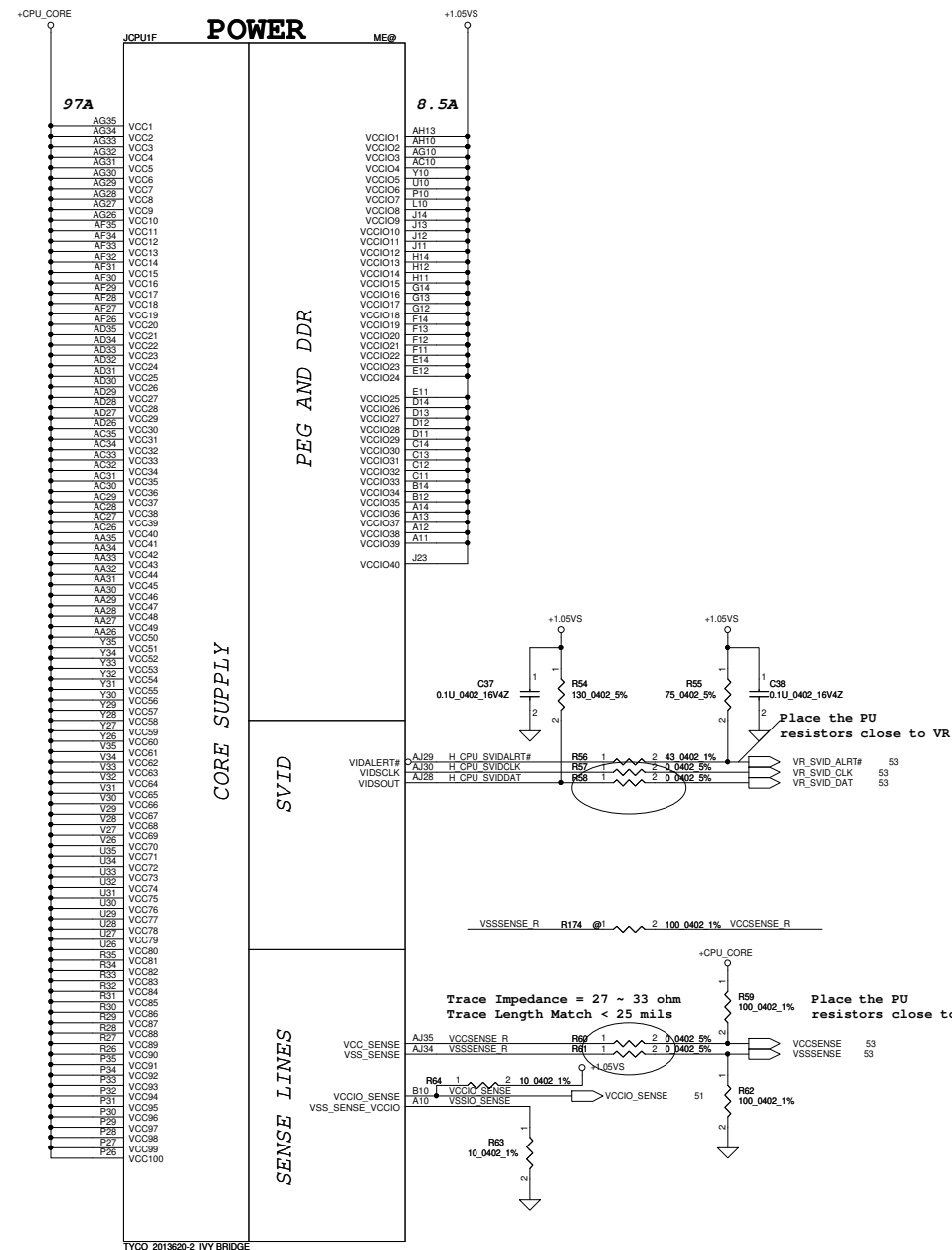
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
------	--

* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

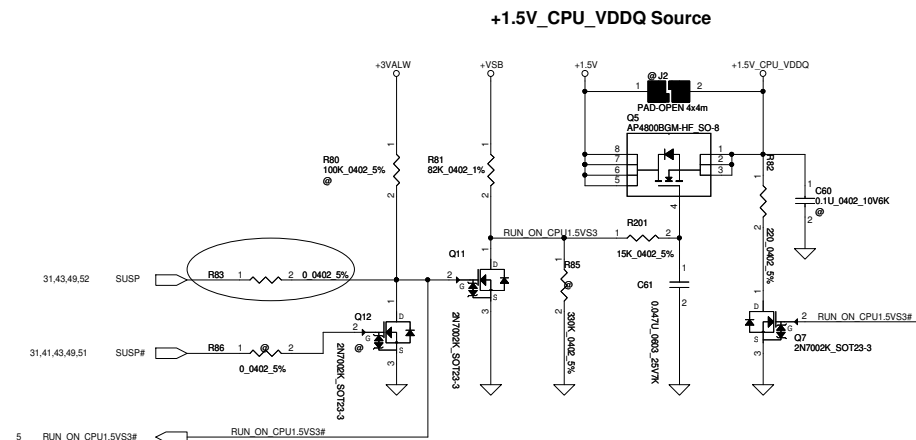
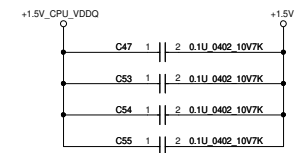
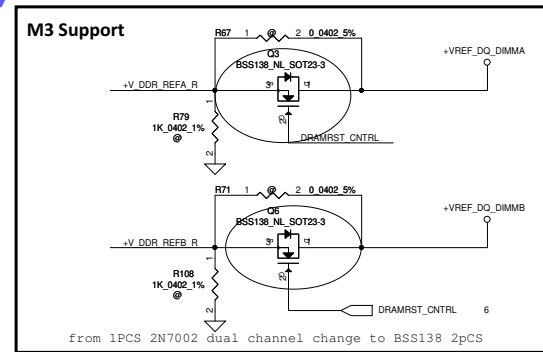
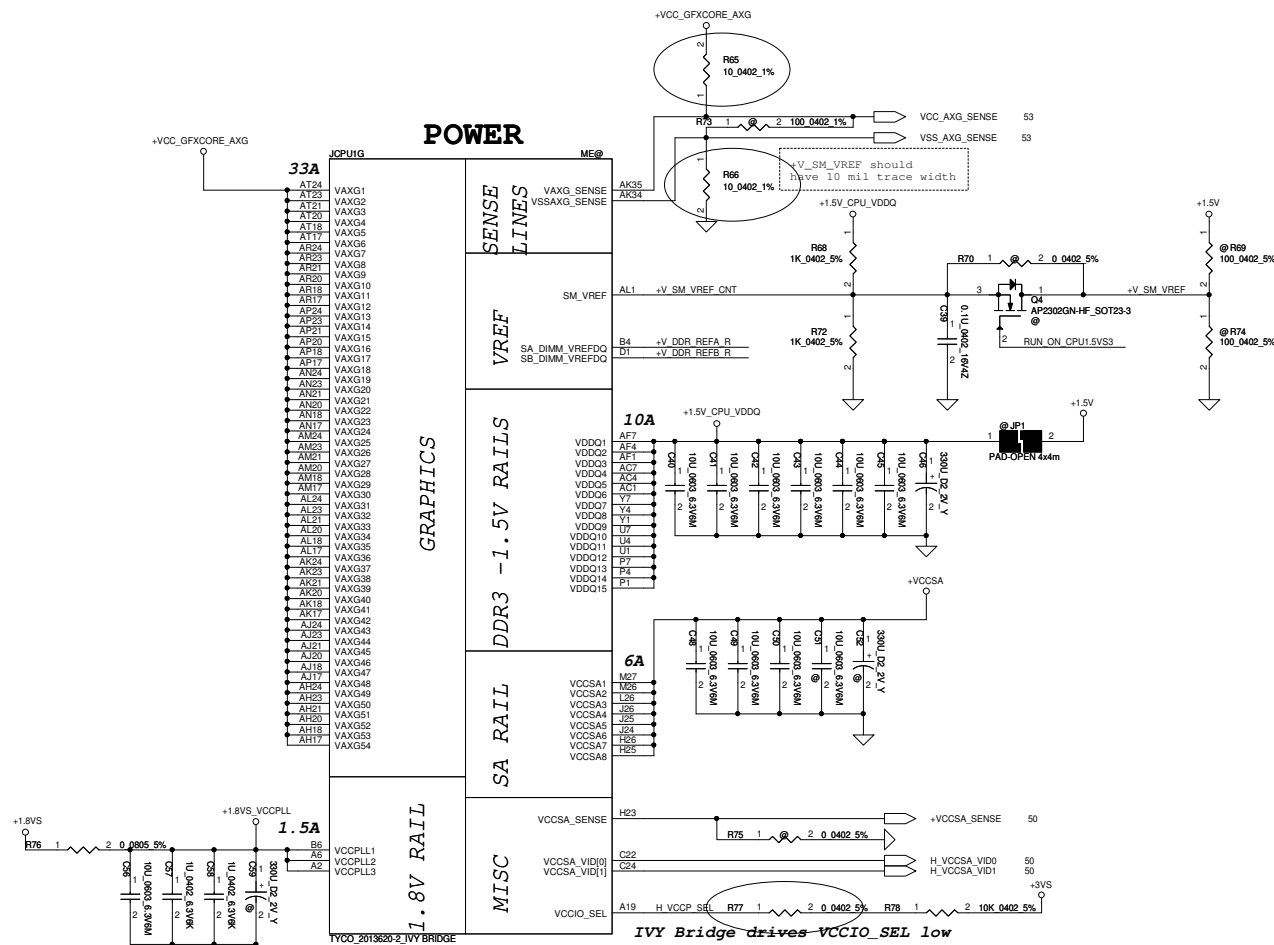
```
CFG[6:5] *10: x8, x8 - Device 1 function 1 enabled ; function 2
disabled
01: Reserved - (Device 1 function 1 disabled ; function
2 enabled)
```



PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>




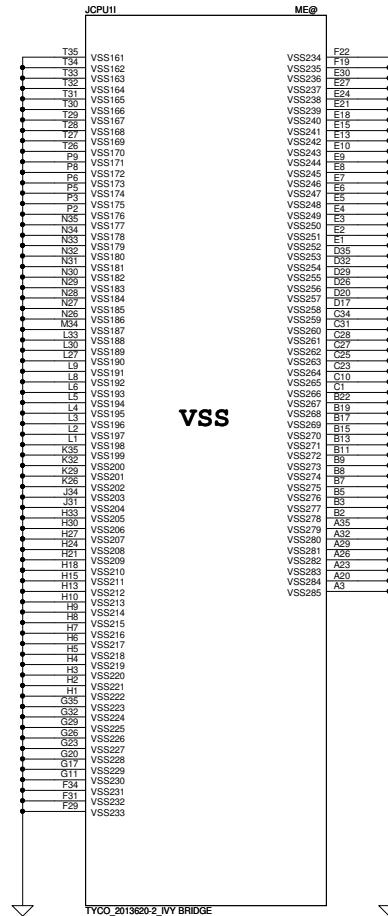
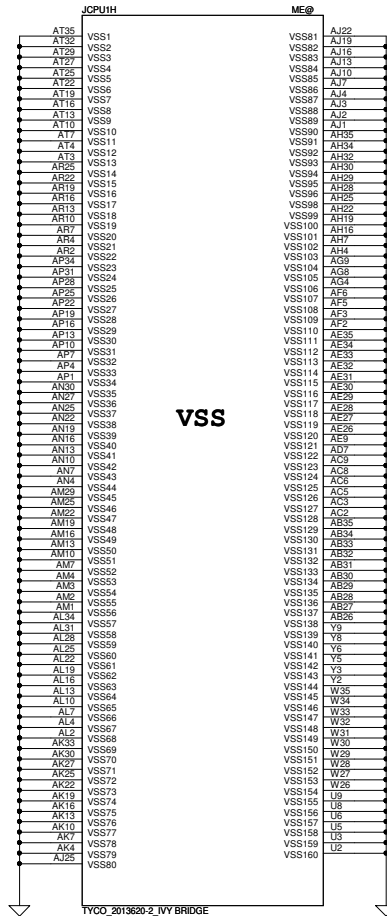
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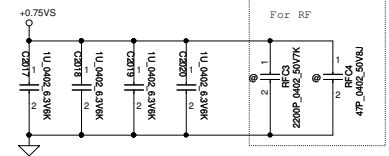
Vauxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

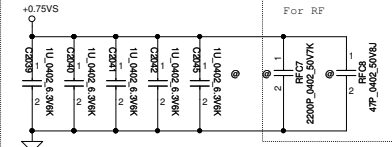
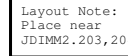
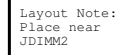
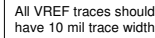
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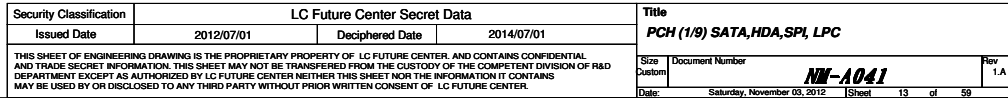
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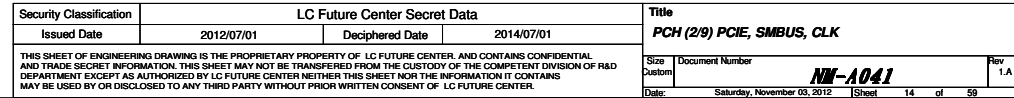


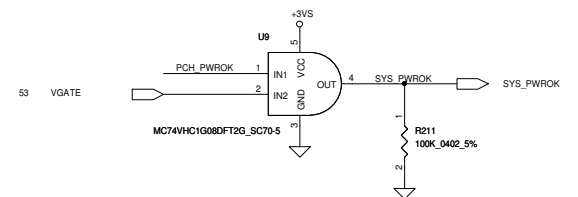
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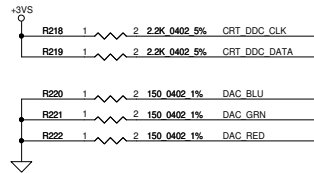
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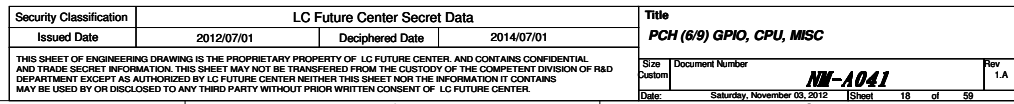


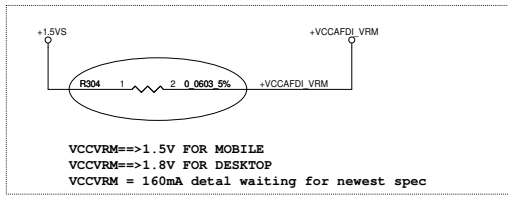


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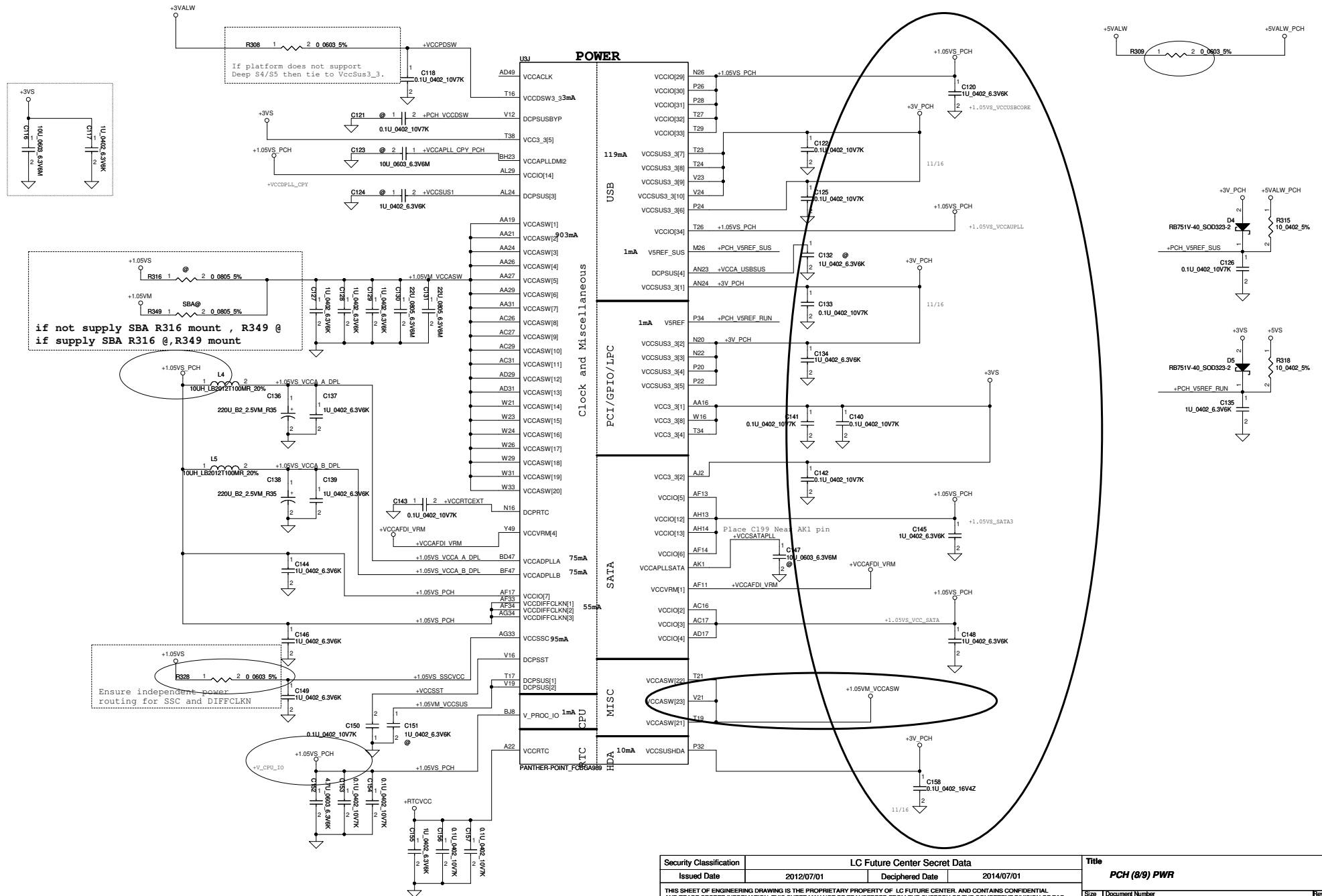
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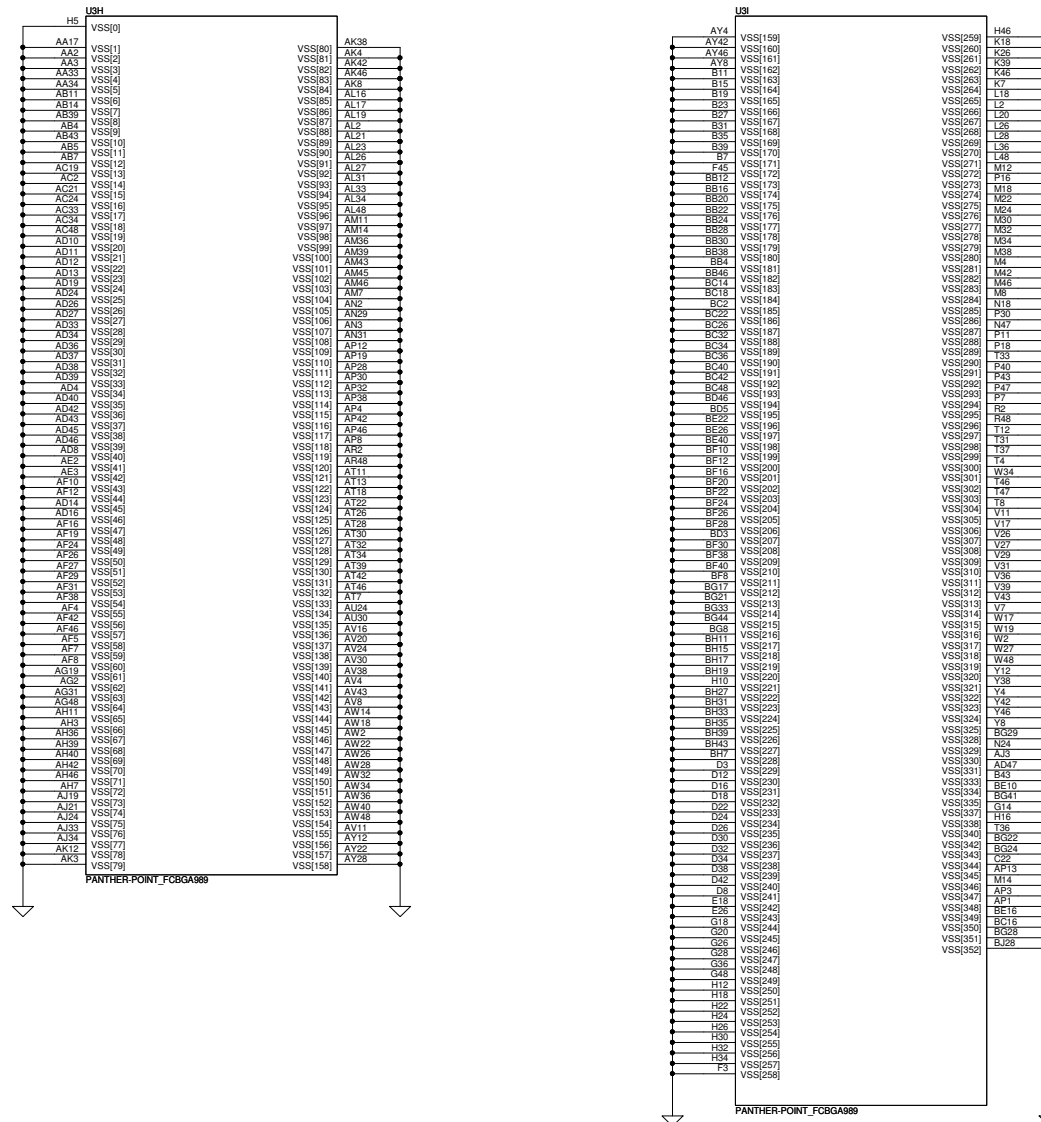


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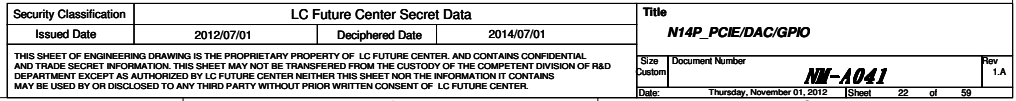
```
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
```

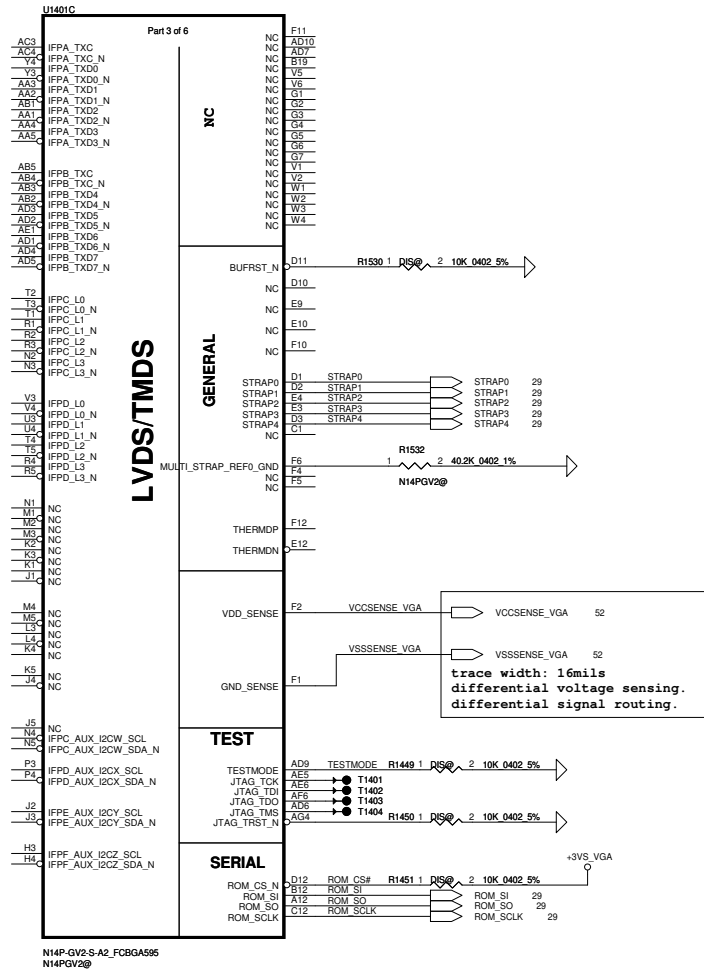


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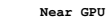


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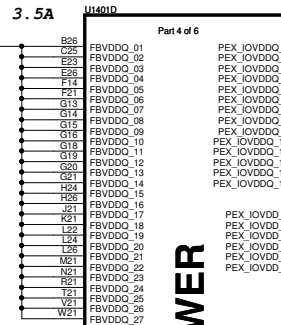




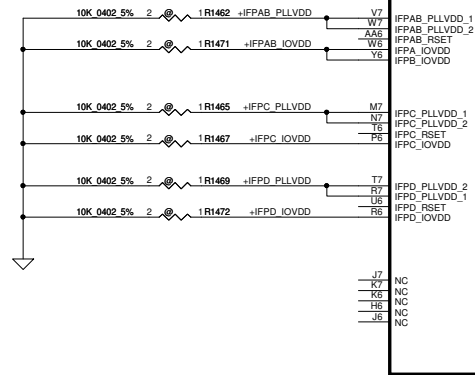
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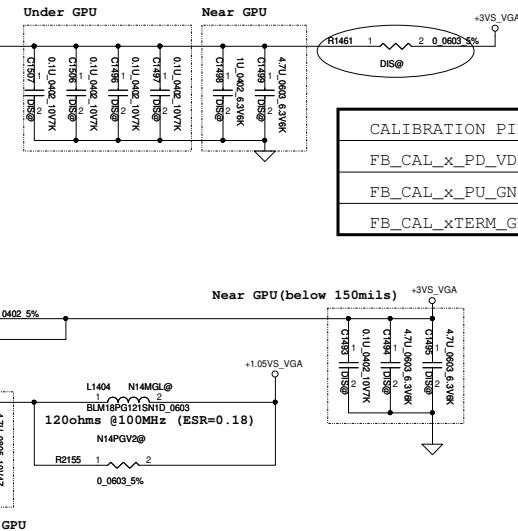
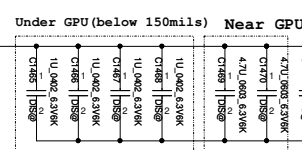
3.5A



POWER

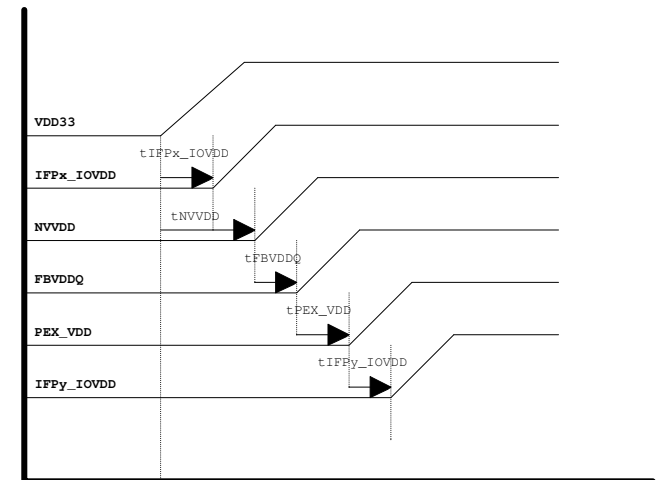
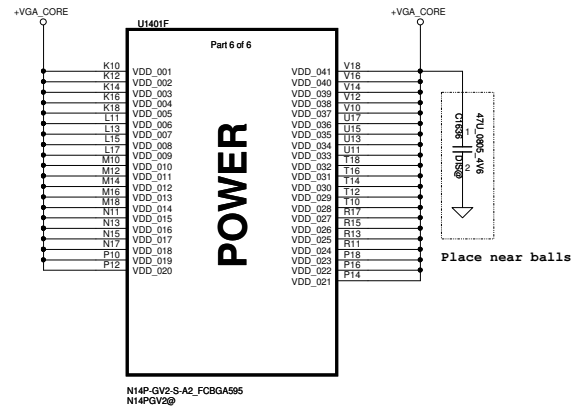
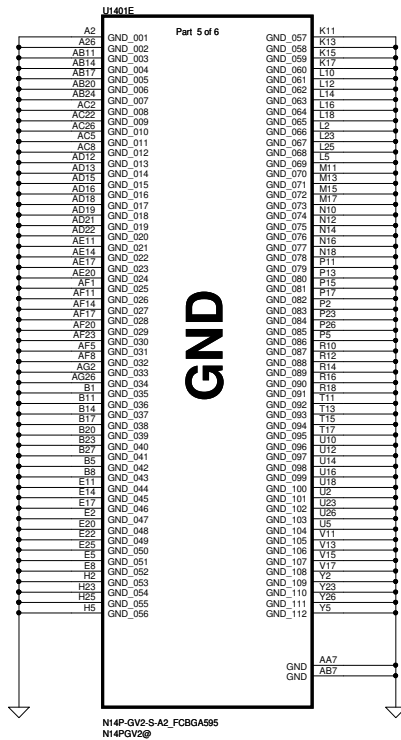


N14P-GV2-S-A2_FCBGA595
N14PGV2@



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2ohm
FB_CAL_x_PU_GND	42.2ohm
FB_CAL_xTERM_GND	51.1ohm

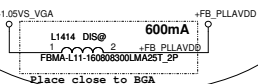
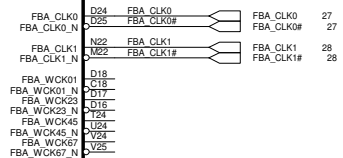
Security Classification	LC Future Center Secret Data			Title N14P_Power
Issued Date	2012/07/01	Deciphered Date	2014/07/01	
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NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

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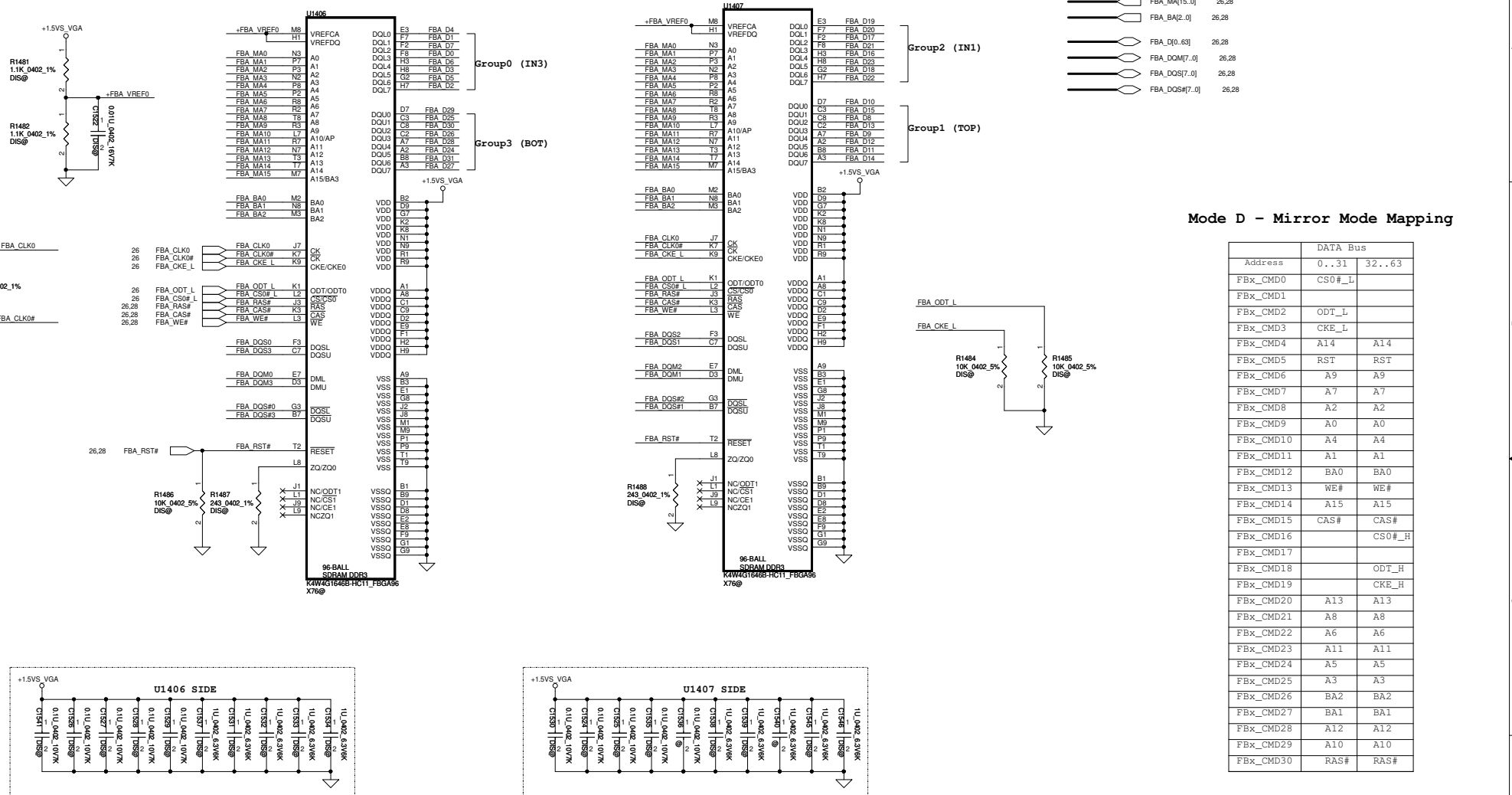


Mode D - Mirror Mode Mapping

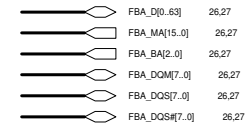
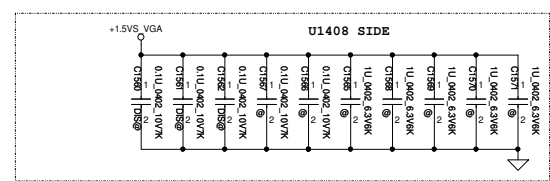
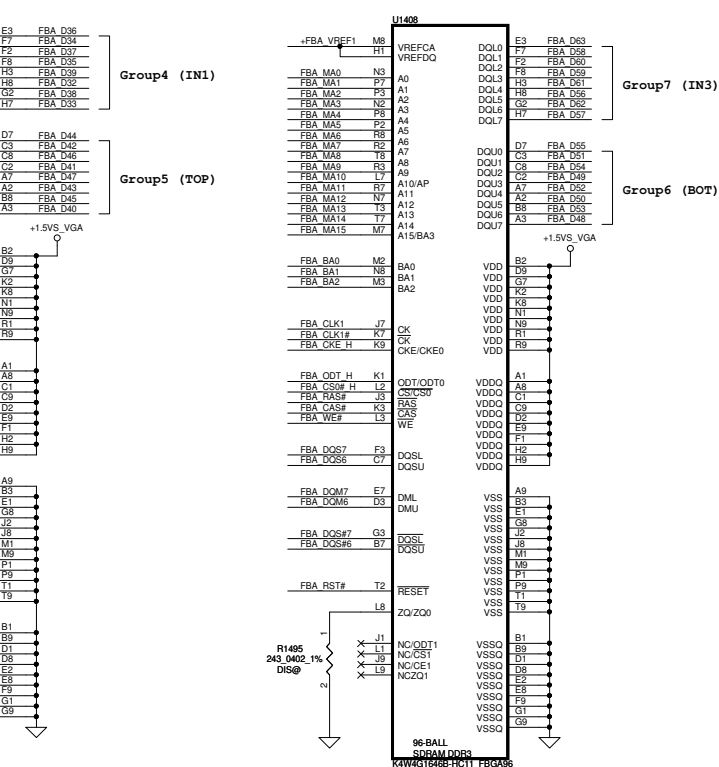
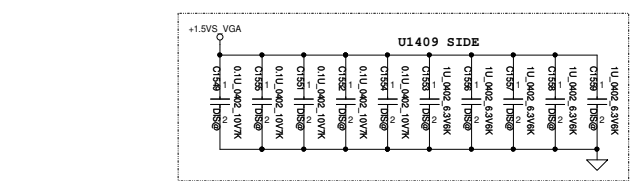
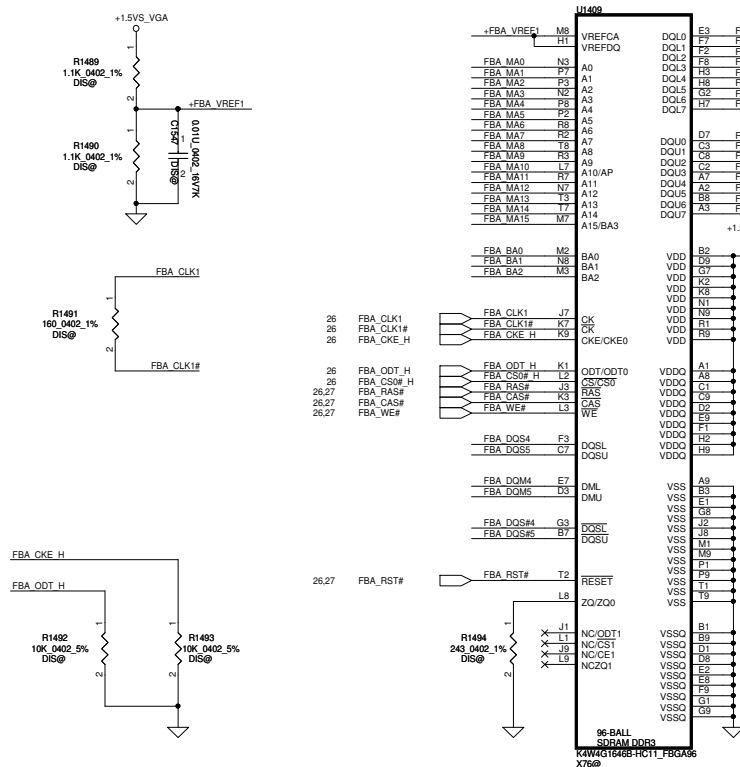
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RA5#	RA5#

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Issued Date	2012/07/01	Deciphered Date	2014/07/01	N14P_MEM Interface		
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Memory Partition A - Lower 32 bits



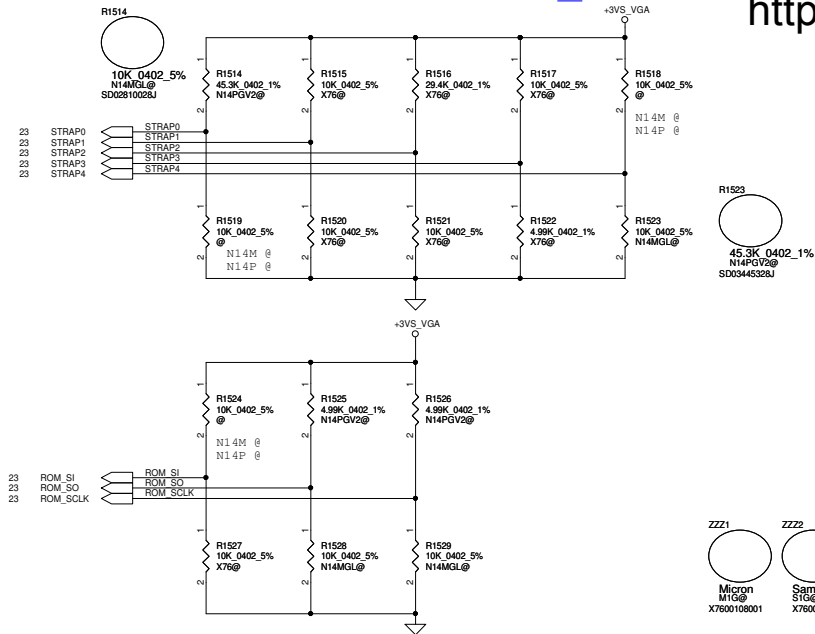
Memory Partition A - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

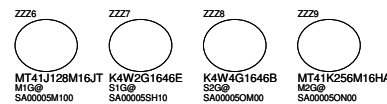
USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default



For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K

GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PU 5K	PD 45K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PU 5K	PU 5K	PD 30K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PU 5K	PU 5K	PD 20K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PU 5K	PU 5K	PD 10K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K
		256Mx16								

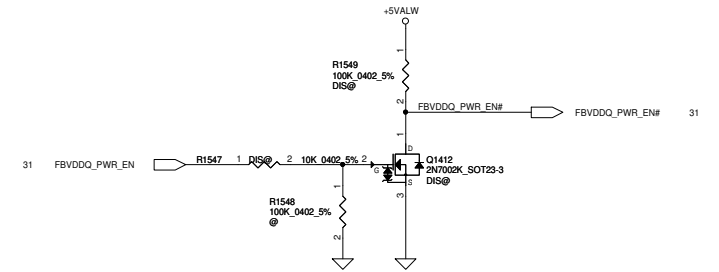
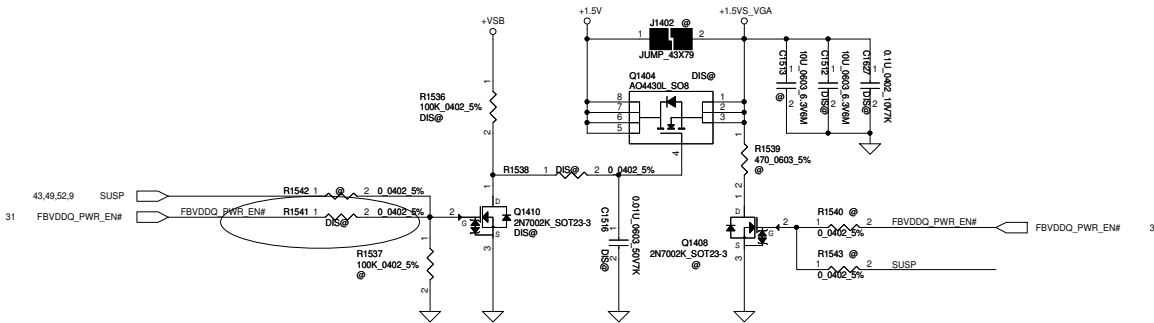
GPU	FB Memory gDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14M-GL	Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Hynix 1000MHz	H5TQ2G63DFR-N0C	PD 10K	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K
		128Mx16								
	Micron 1000MHz	MT41J128M16JT-093G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PU 10K	PD 10K
		256Mx16								
	Hynix 900MHz	H5TQ4G63MFR-11C	PD 10K	PD 10K	PD 10K	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PD 10K	PD 10K	PD 10K	PU 10K	PD 10K	PU 10K	PU 10K	PD 10K
		256Mx16								

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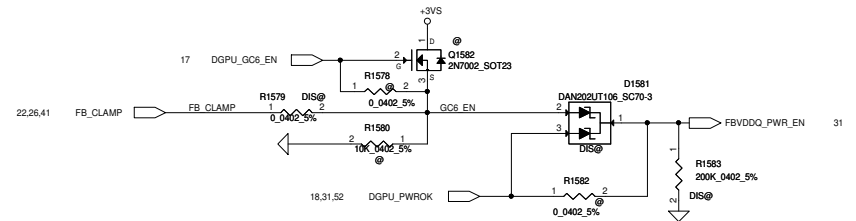
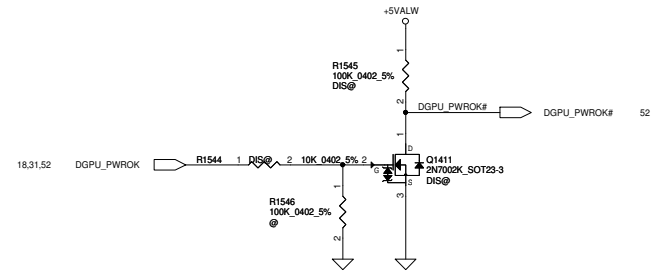
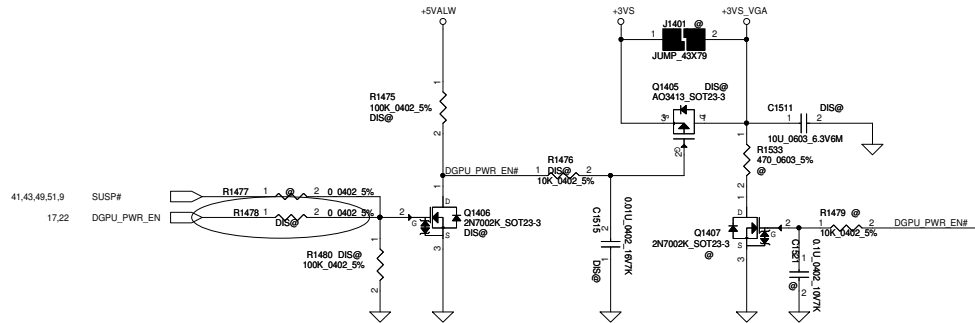
<http://laptopblue.vn/>
<http://adf.ly/3o8pJ>

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+1.5V to +1.5VS_VGA

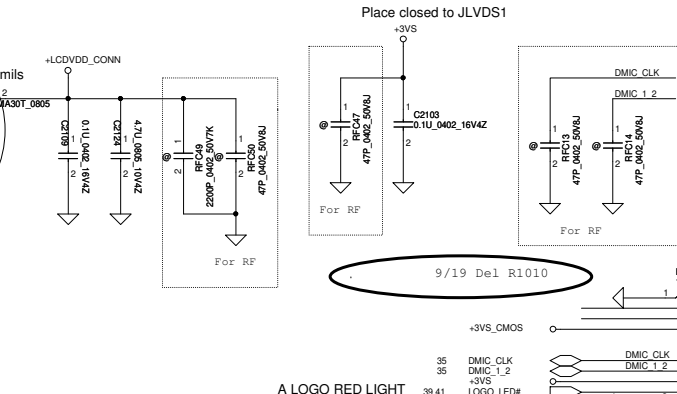
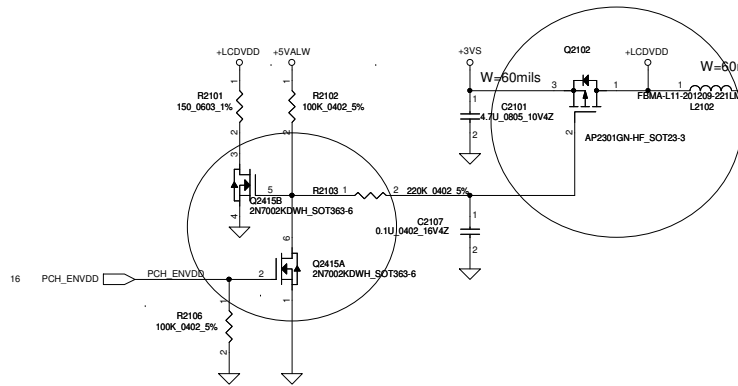


+3VS to +3VS_VGA



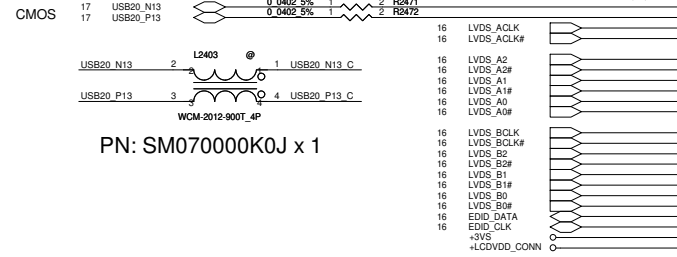
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LCD POWER CIRCUIT

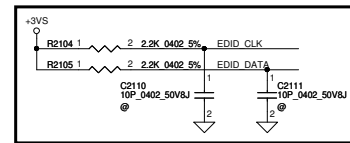
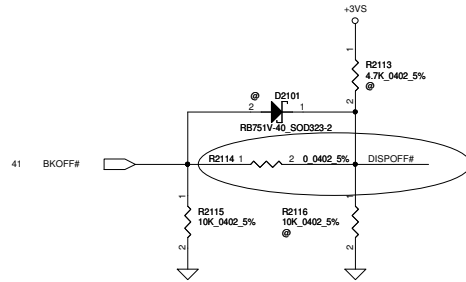


LCD/LED PANEL Conn.

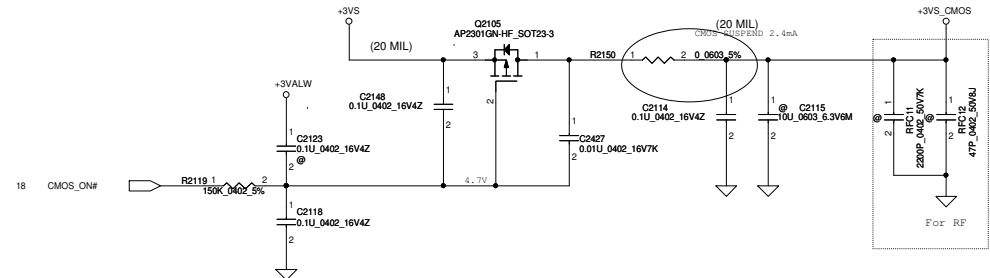
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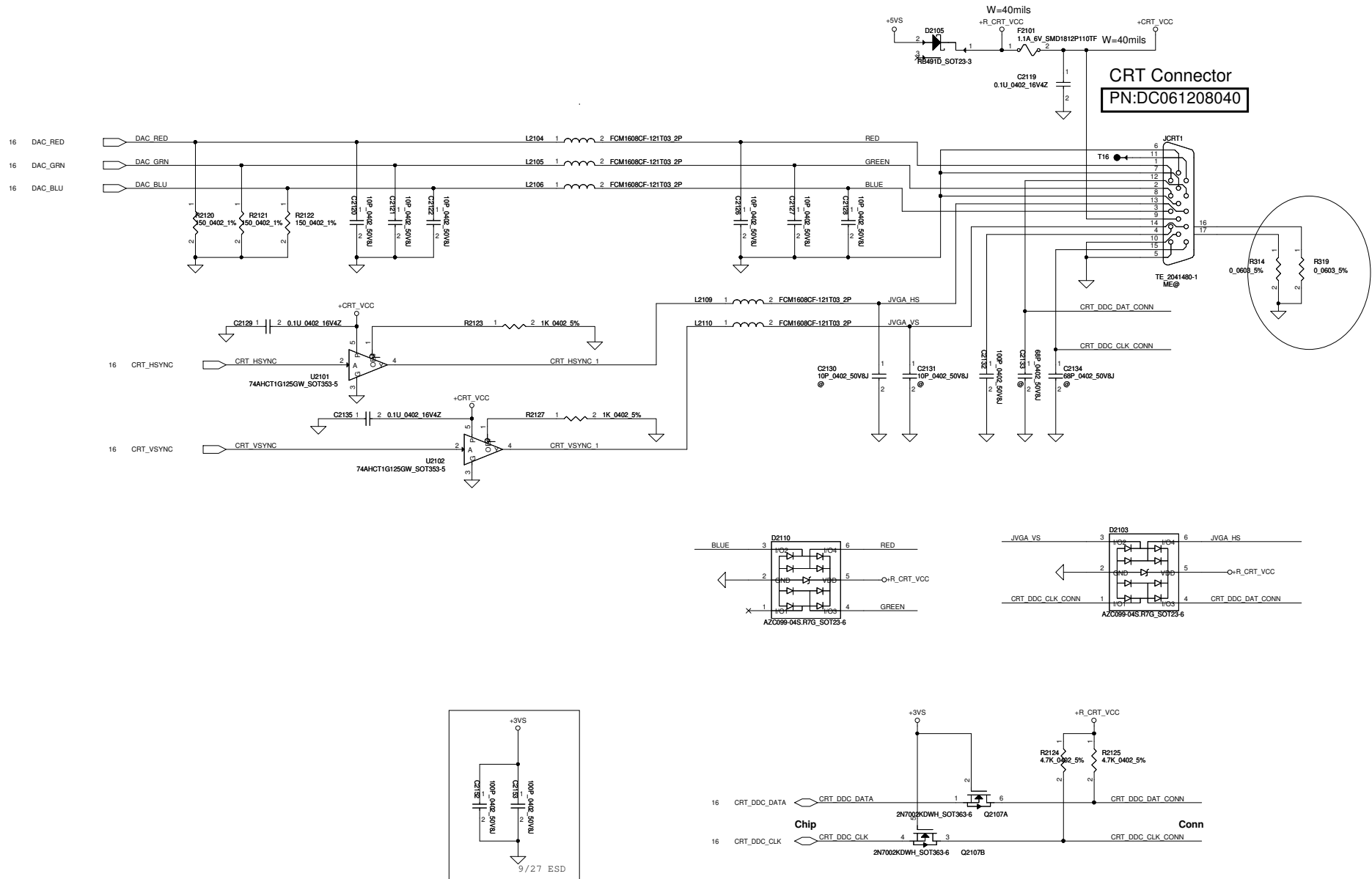
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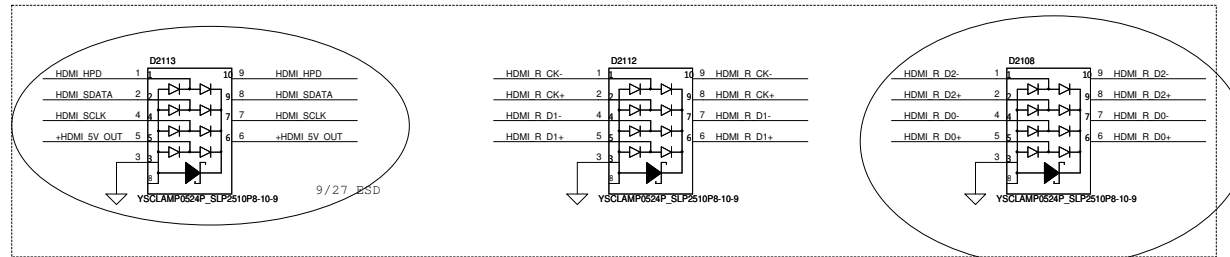
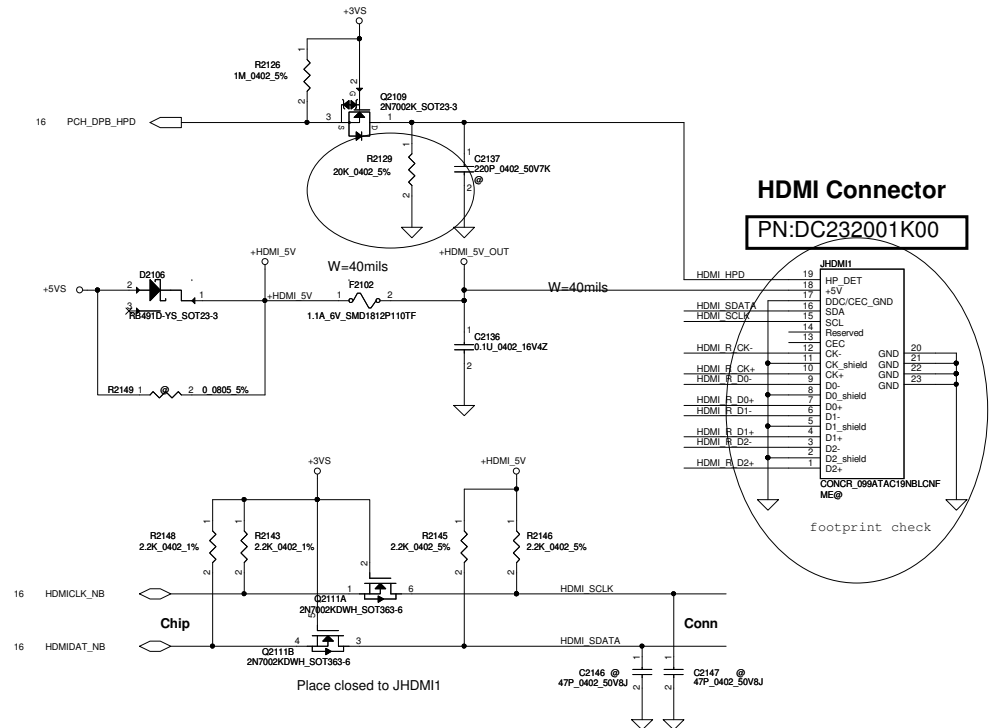
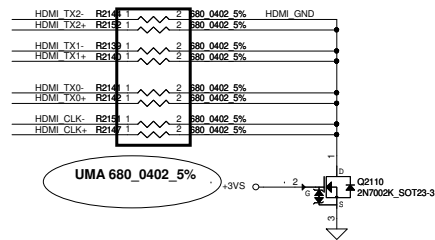
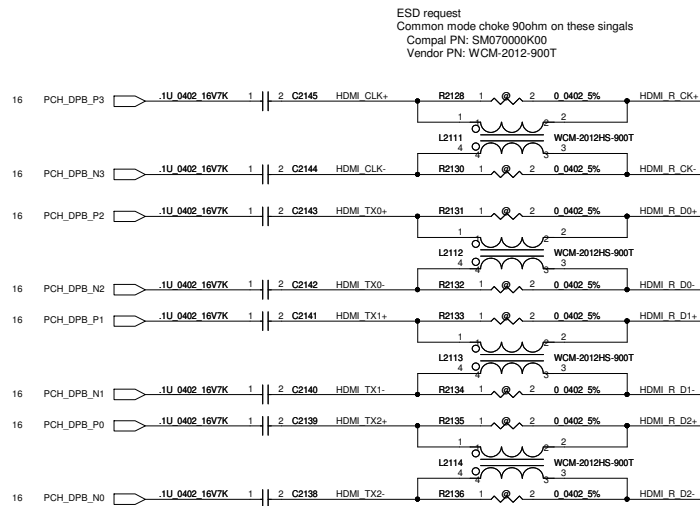
CMOS Camera Conn



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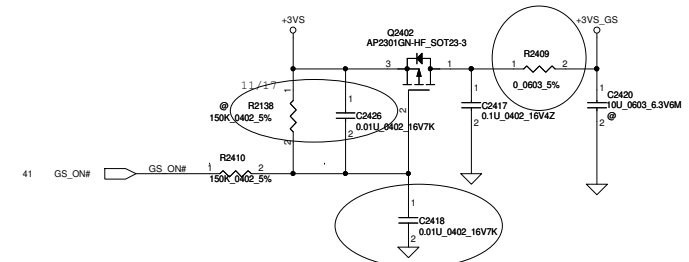
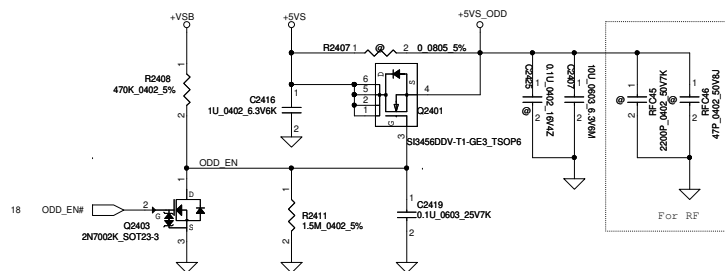
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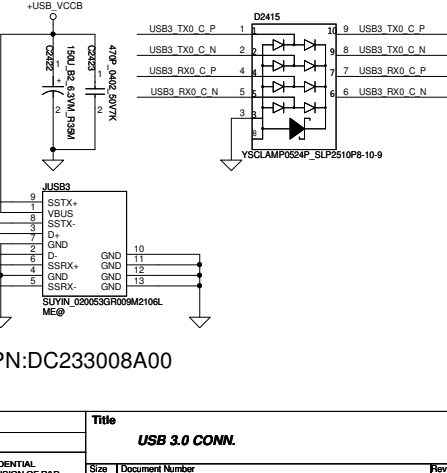
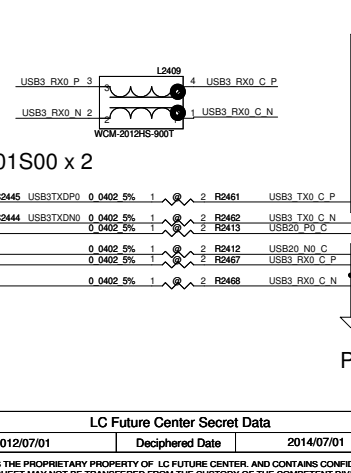
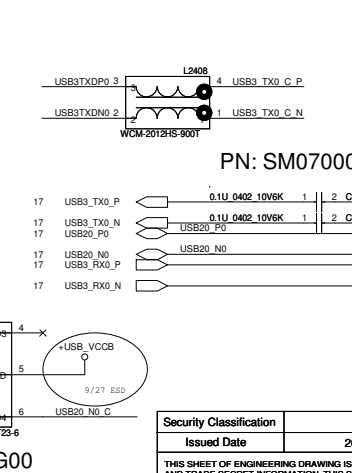
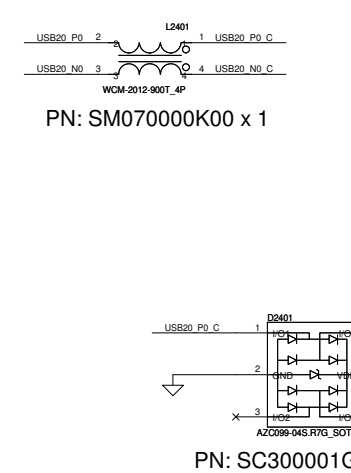
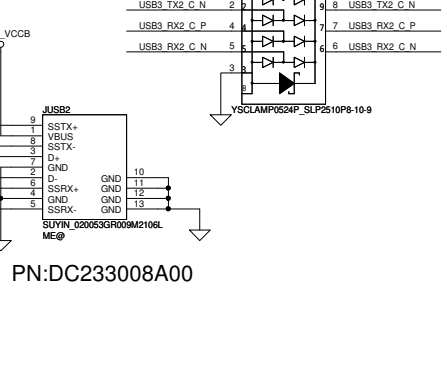
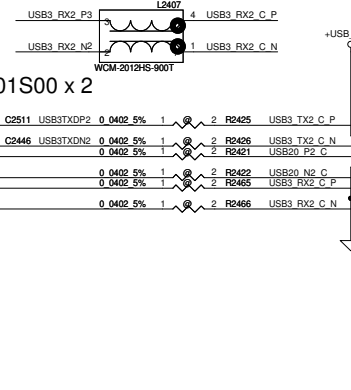
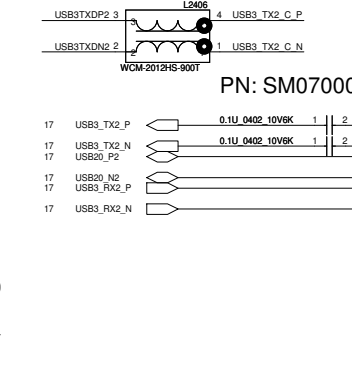
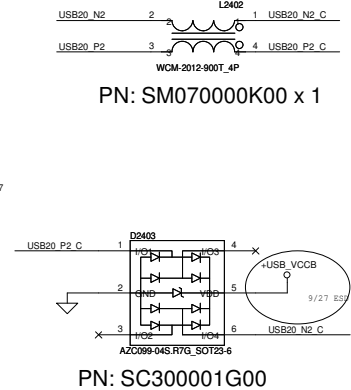
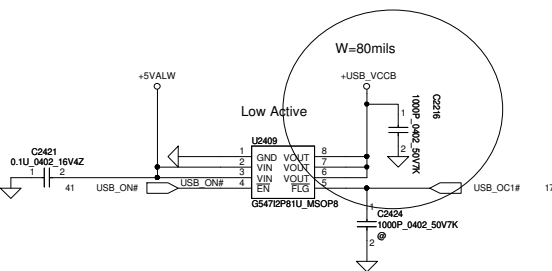
To support Wake-on-Jack or Wake-on-Ring, the CO#
VAUX_3.3 & VDD_IO pins must be powered by a rail
is not removed unless AC power is removed.
*DSH page42 has more detail.

Pin 18 to GND for Gen 3



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USB 3.0 Conn.

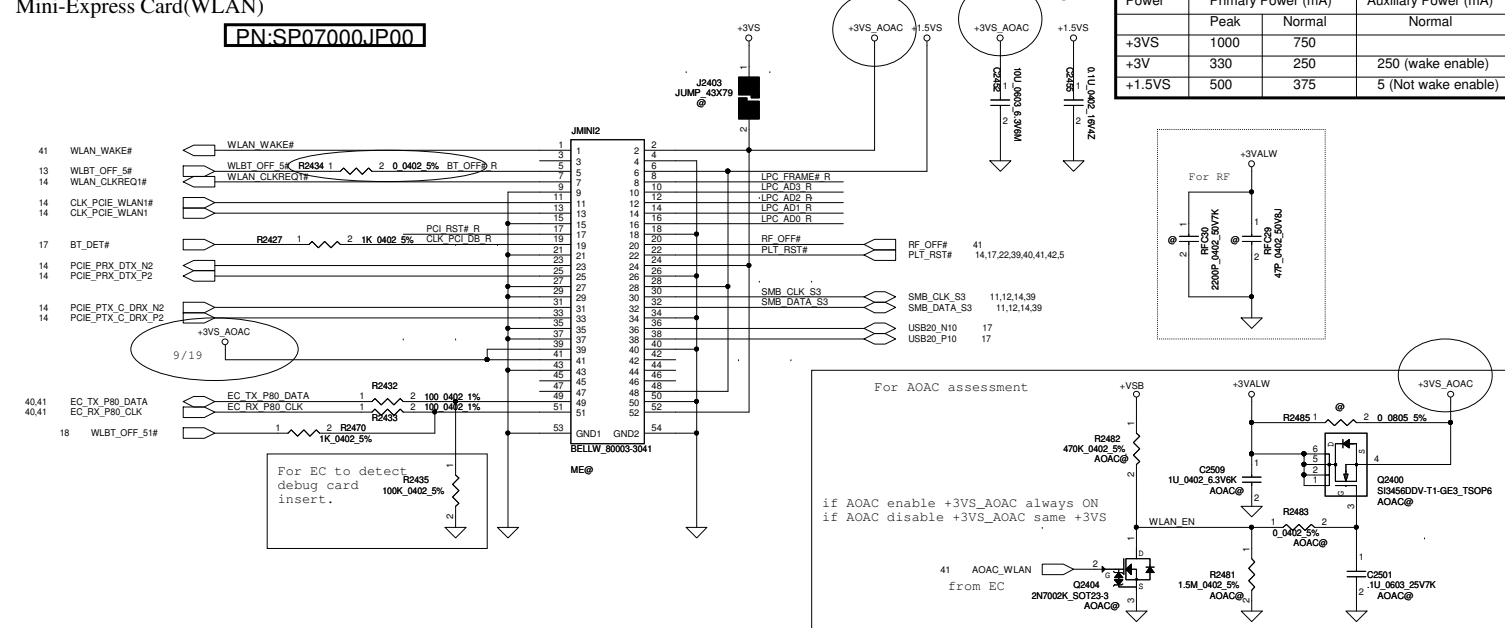


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						Size		Document Number		Rev	
						Date		Thursday, November 01, 2012		Sheet	
Custom		NW-A041		1.A		37 of 59					

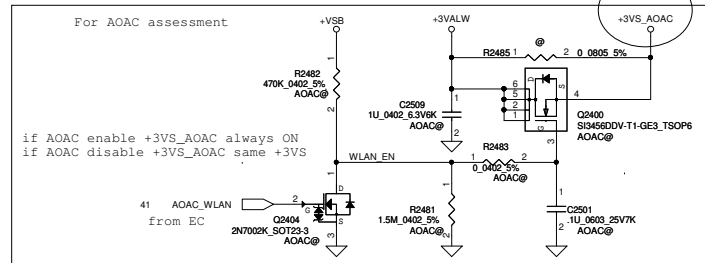
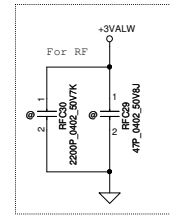
BT Connector

Mini-Express Card(WLAN)

PN:SP07000JP00



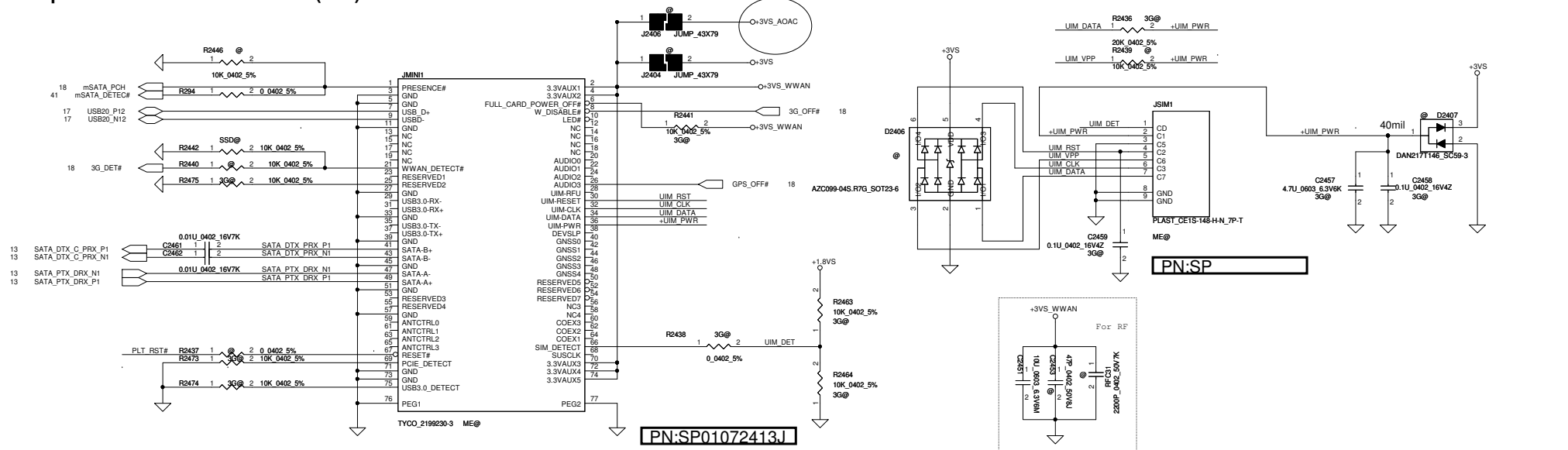
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

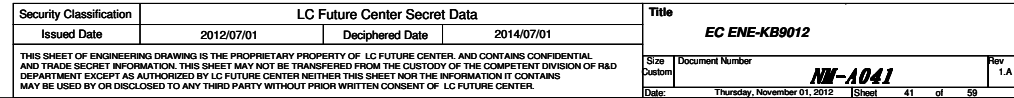
LPC_FRAME# R	R2449	2	0	0402	5%	LPC_FRAME#		LPC_FRAME#	13,40,41
LPC_A03 R	R2455	2	0	0402	5%	LPC_A03		LPC_A03	13,40,41
LPC_A02 R	R2456	2	0	0402	5%	LPC_A02		LPC_A02	13,40,41
LPC_A01 R	R2457	2	0	0402	5%	LPC_A01		LPC_A01	13,40,41
LPC_A00 R	R2458	2	0	0402	5%	LPC_A00		LPC_A00	13,40,41
PLT_RST# R	R2459	2	0	0402	5%	PLT_RST#		PLT_RST#	13,40,41
CLK_PCI_DB R	R2426	2	0	0402	5%	CLK_PCI_DB		CLK_PCI_DB	17,40

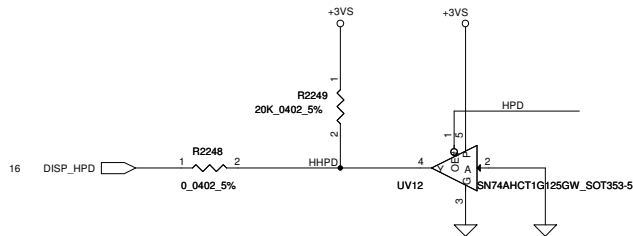
Mini-Express Card for WWAN/mSATA(Full)



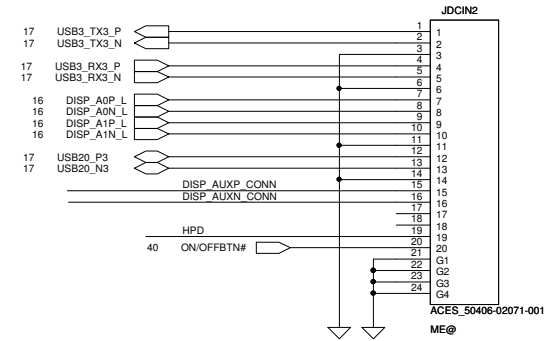
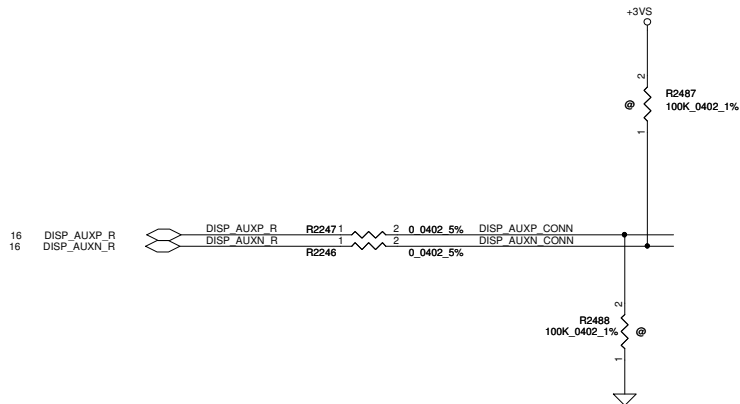
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PCle-WLAN and WWAN_mSATA	
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Custom				1.A	
Date:	Thursday, November 01, 2012	Sheet	38	of 50	

Power Button

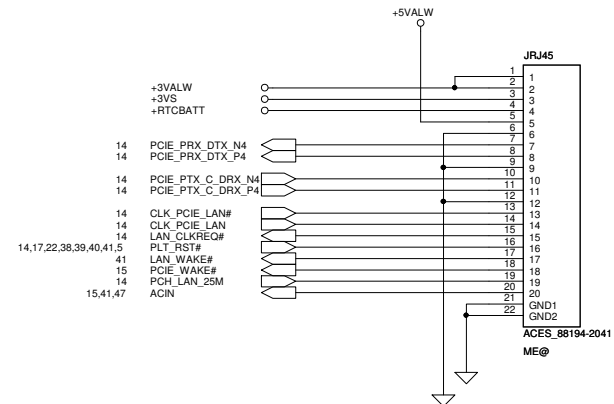




DP/TMDS Switch Circuit (1)

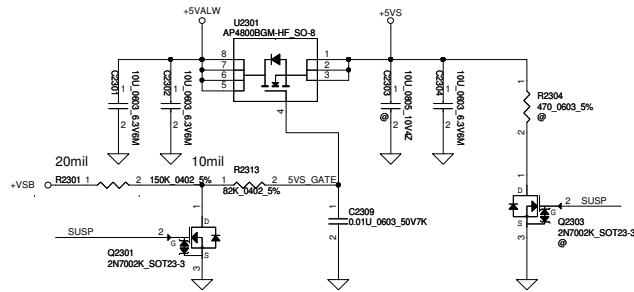


RJ45 Board

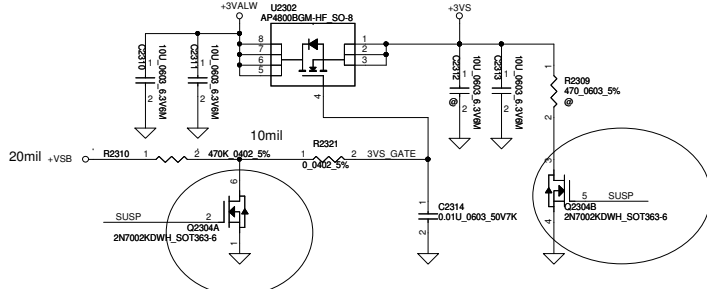


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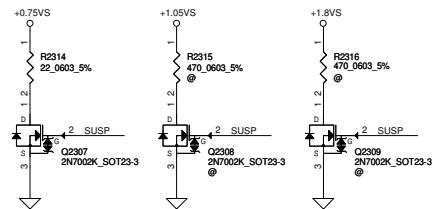
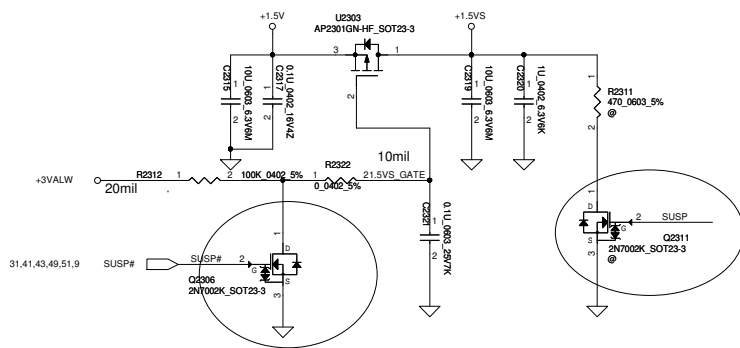
+5VALW TO +5VS



+3VALW TO +3VS

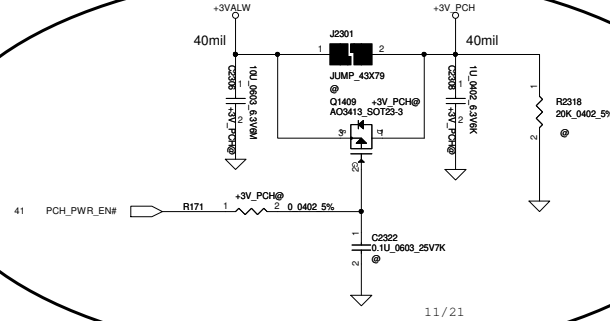


+1.5V to +1.5VS

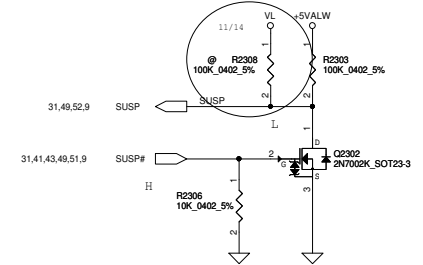
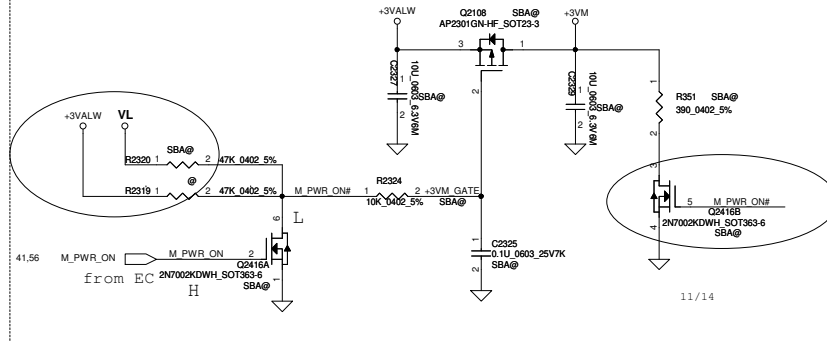


+3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3

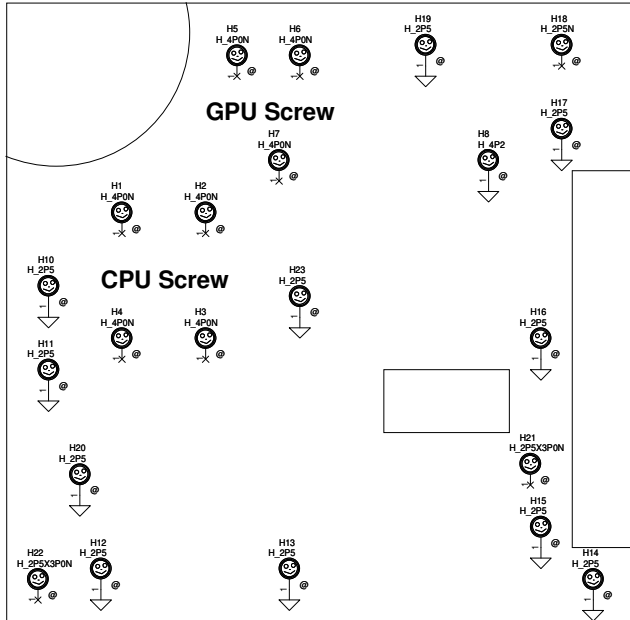


FOR SBA Function POWER(always mount)

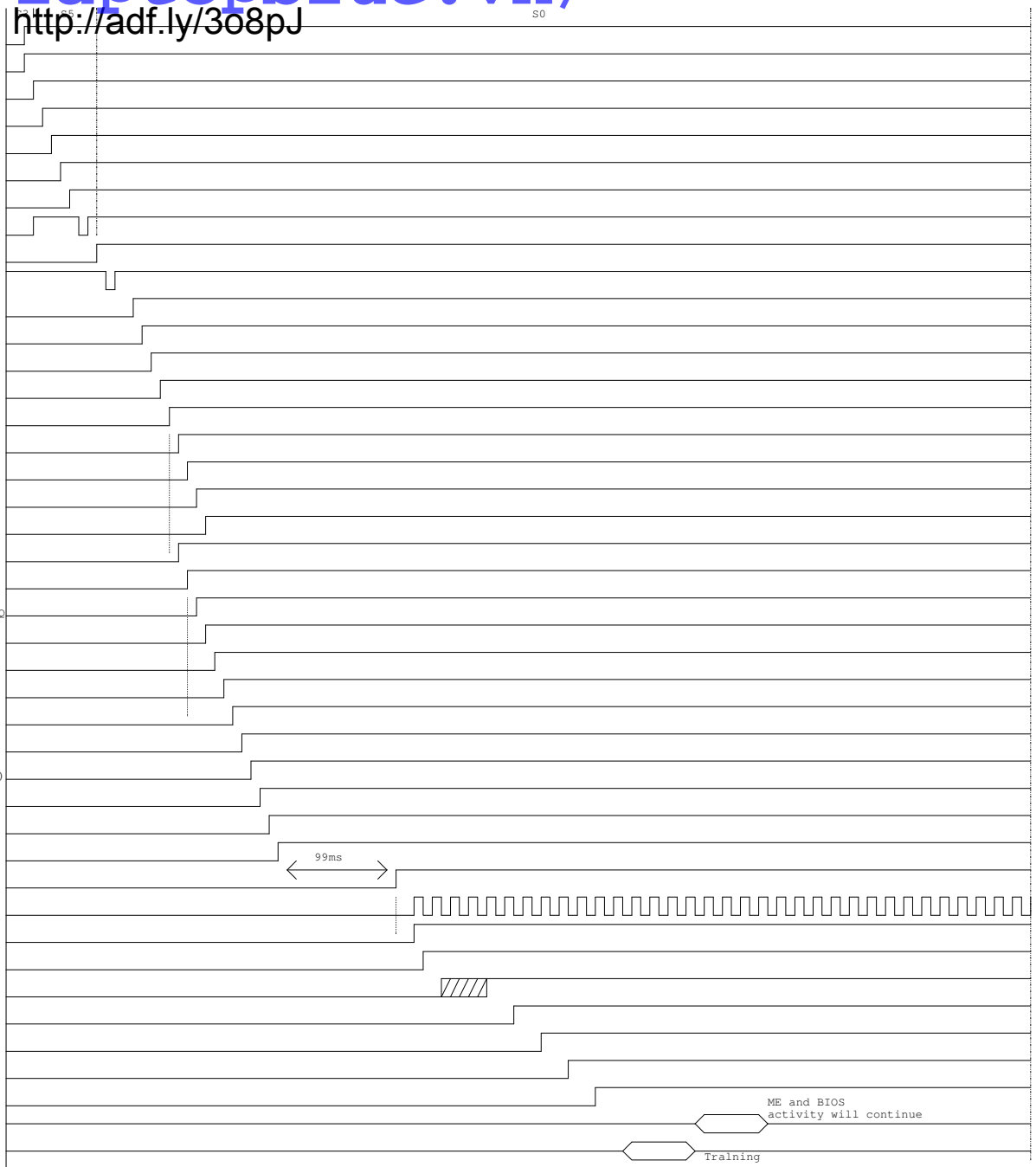


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Size		Document Number			
Custom		NW-A041			
Date		Thursday, November 01, 2012		Sheet	43 of 59

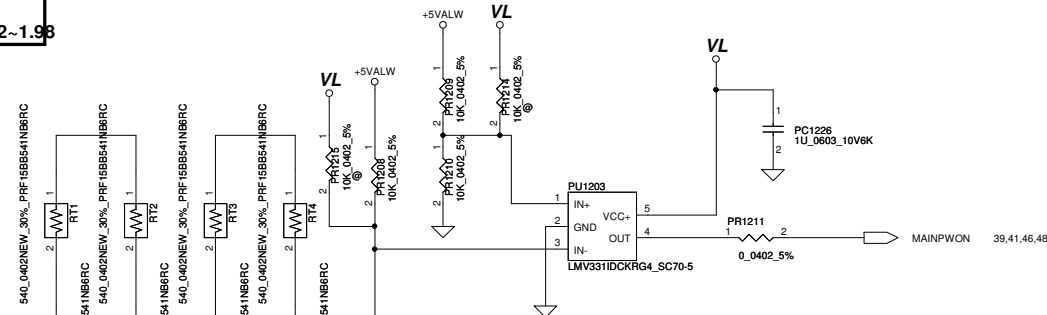
Screw Hole & FD



RTC
RTCRST
EC_111 pin
EC_ON
MAINPWON
+5VALW
+3VALW/VCCDSW
ON/OFF#
EC_RSMRST#
PBTN_OUT#
SLP_S5#
SLP_S4#
SYSON
SYSON
PCH_SLPA#
M_PWR_ON
+3VM
+1.05VM
PCH_APWROK
SLP_S3#
SUSP#
+1.5V_CPU_VDDQ
+1.8VS
+5VS
+3VS
+1.5VS
+0.75VS
+V1.05VS (VCCP)
+VCCSA
SA_PGOOD
VR_ON
PCH_POK
PCH_CLKOUT
DRAMPWROK
H_CPUPWRGD
CPU_VID
CPU_CORE
VGATE
SYS_PWROK
BUF_PLT_RST#
SPI
DMI



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Custom		Rev 1.A	
Date	Monday, November 05, 2012	Sheet	44 of 59

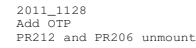
[illegible]

RTC Battery

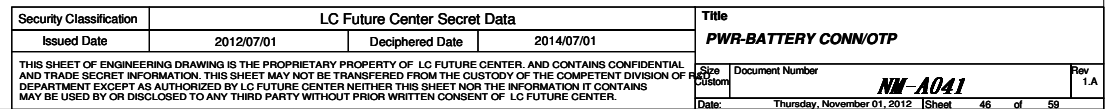
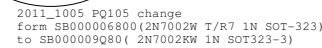
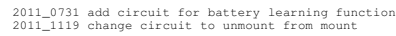
2011_0728 del PR130 and +3VLP
add PR? 1K_0603_5%
change place for R132,R133, +CHGRTC,PD107

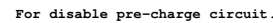
2011_0808 PU102 change
form SA00001PE00 (APL5156-33DI-TRL)
to SA00002E280 (BIT3021A-ST9)

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Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-DCIN / Vin Detector	
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				Custom	NW-A041
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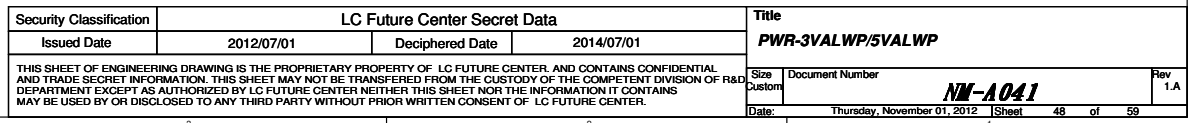
VL

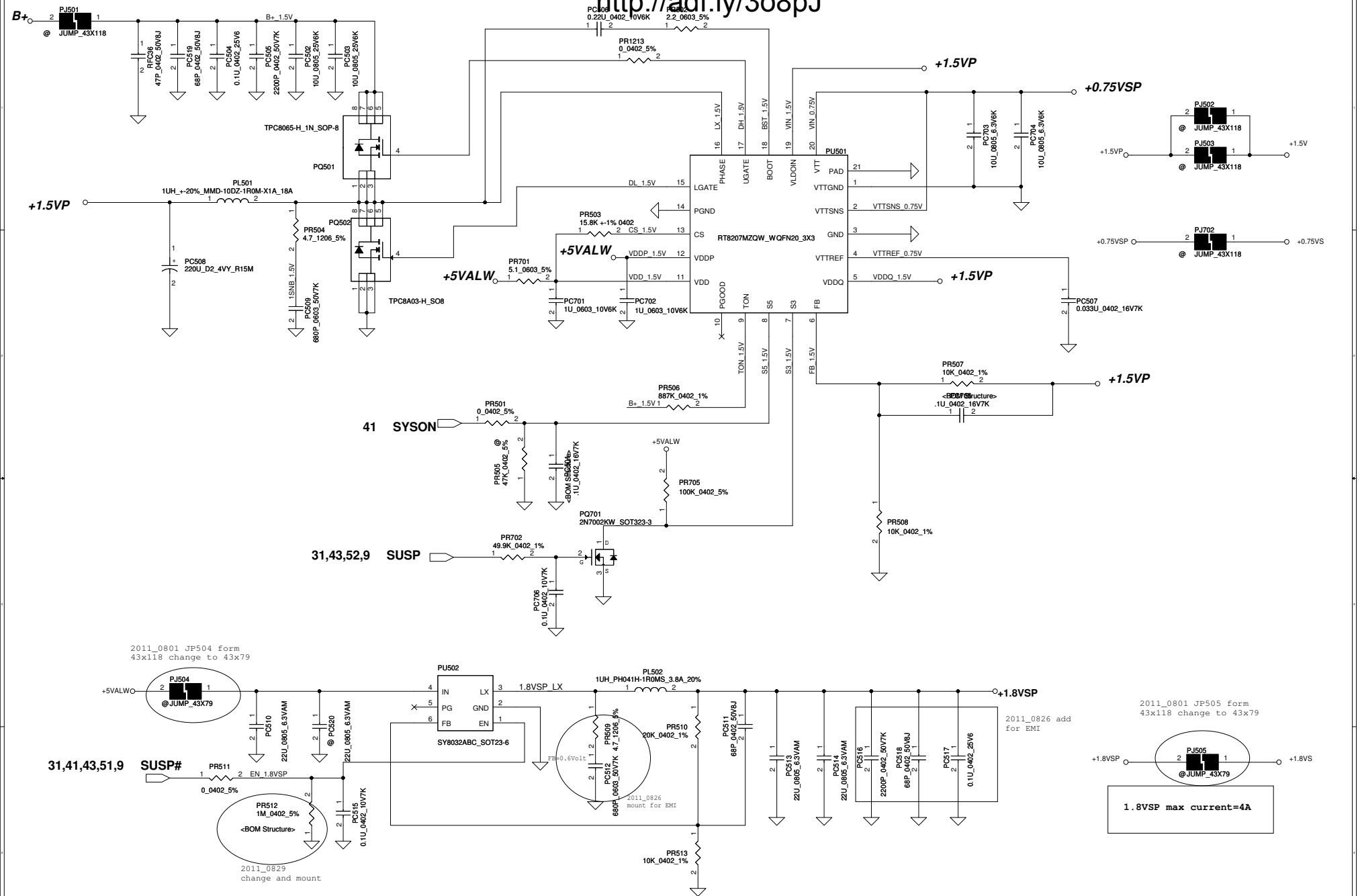




CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Title			
PWR-CHARGER-BQ24737			
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		NW-A041			1.A
Date:		Thursday, November 01, 2012		Sheet	49 of 59

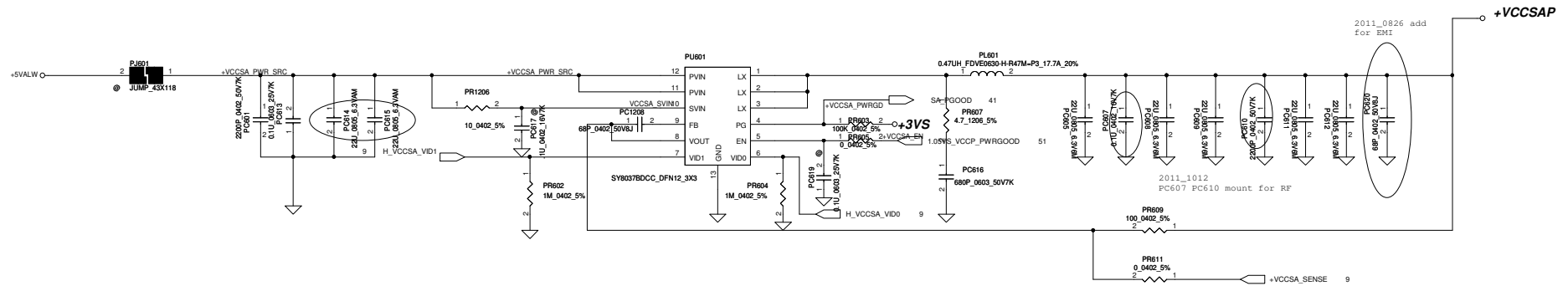
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V


output voltage adjustable network

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```

+VCCSA ○ — 2 **PJ602** 1 — ○ **+VCCSA**
⊕ **JUMP_43X118**

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

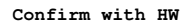
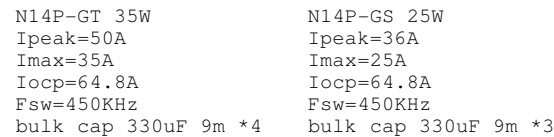


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					 NA-A041
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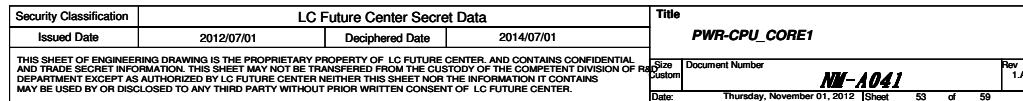


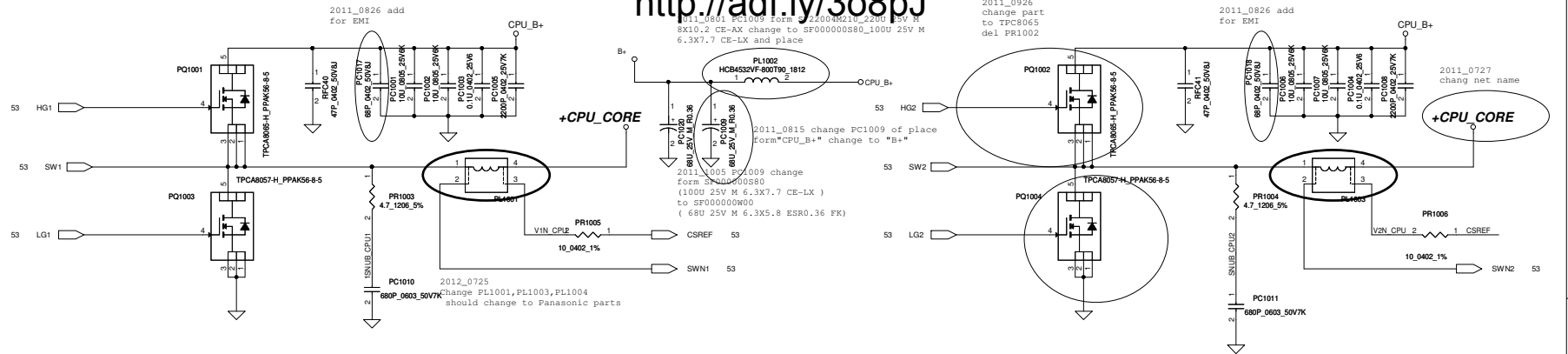
Ivy Bridge CPU ES2 Using

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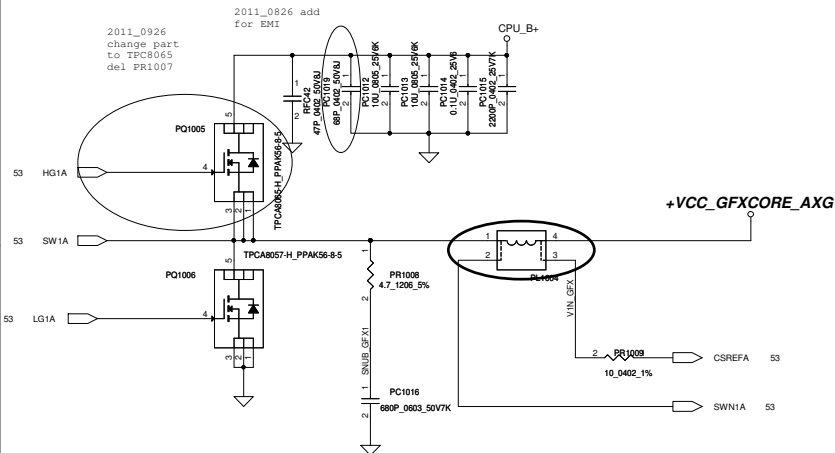
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				PWR-VGA_COREP-ISL62883			
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		NW-A041				1A	
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QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

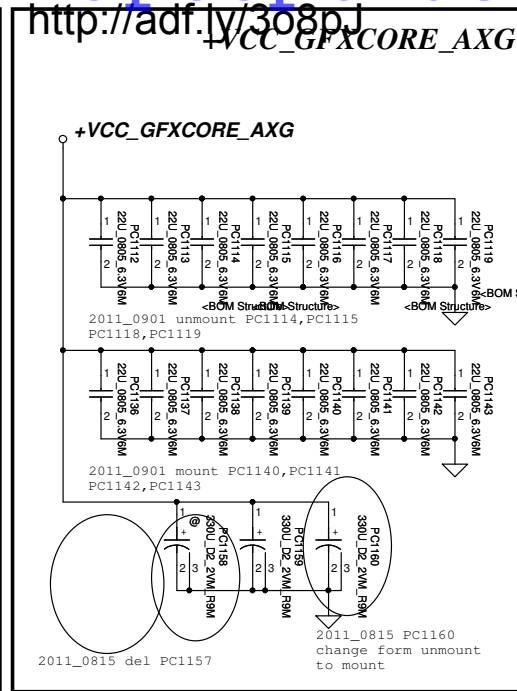
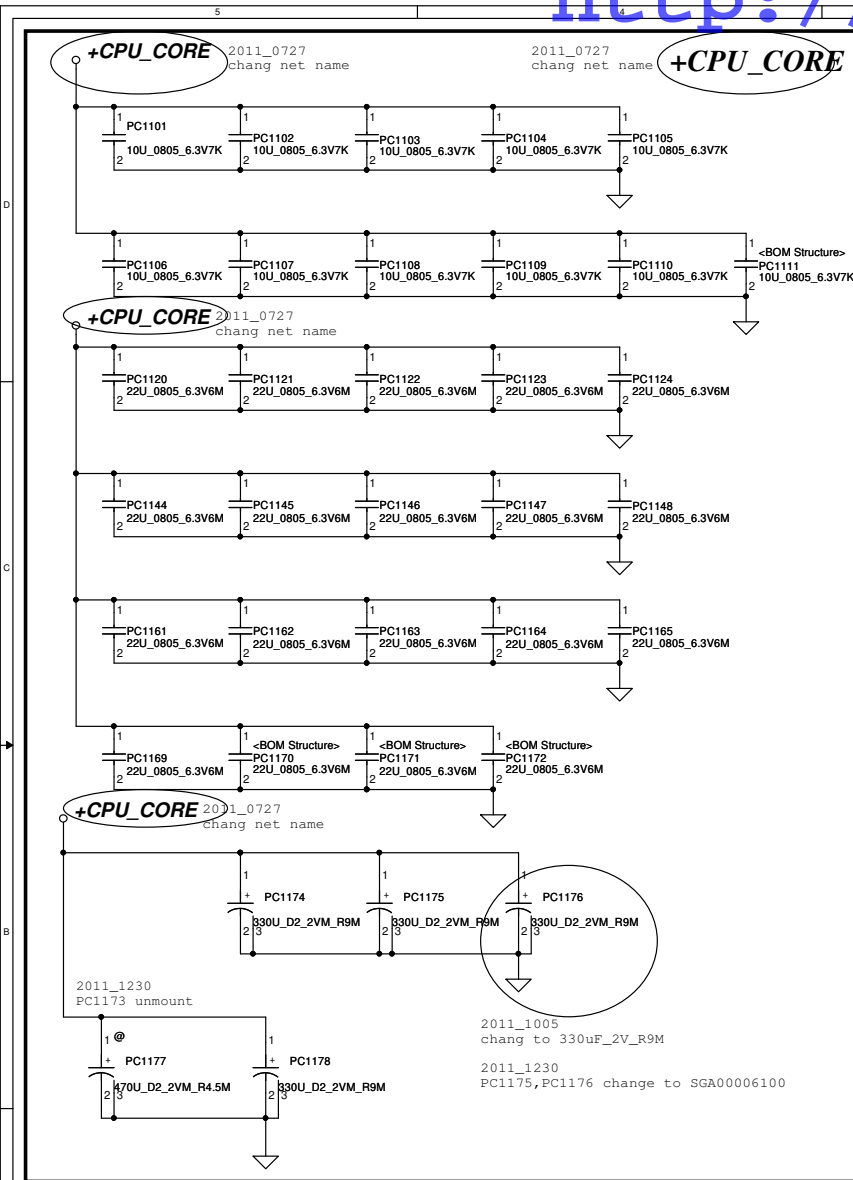
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

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			Document Number
			Rev
			Date

PWR-CPU_CORE2

NW-A041

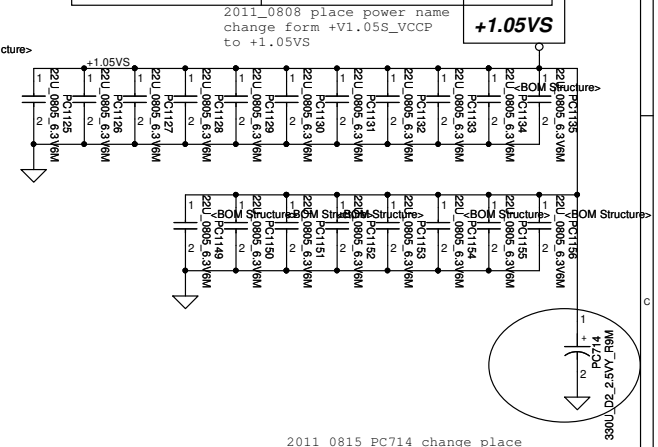
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2011_07929
PC1158 non-mount

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



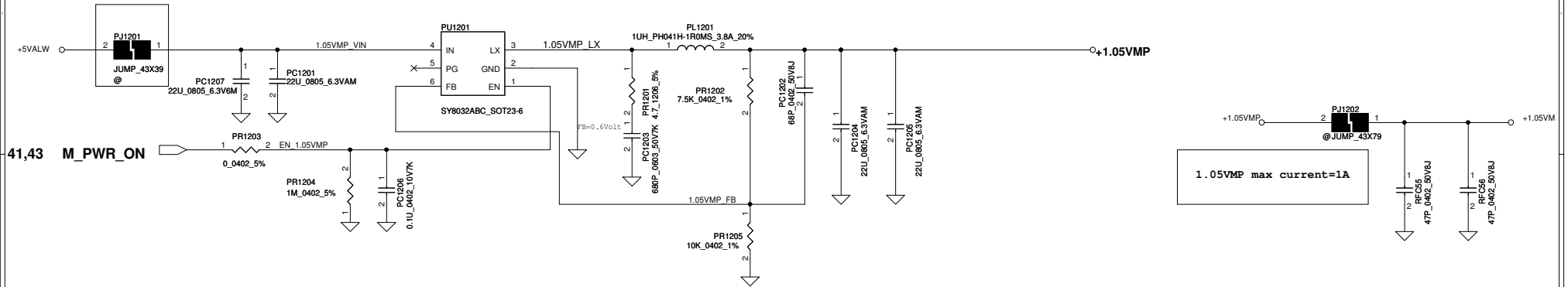
2011_0815 PC1160 change form unmount to mount

2011_1005 PC1160 change to 330uF_2V_R9M

2011_1007
PC1160
form SGA00001Q802
(S POLY C 330U 2V M X LESR6M SX H1.9)
change to SGA00002680
(330U_D2_2.5VY_R9M)

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2011_0923 JUMP form 43X79 change to 43X79



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<http://laptopblue.vn/>
<http://adf.ly/3o8pJ>

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-PIR	
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				Sheet	58 of 59
				Rev	1.A

Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2012/09/XX	No1	V	V	V	Add CXXX, CXXX	Add XXX function

Security Classification		LC Future Center Secret Data		Title	
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2012/07/01		2014/07/01			
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