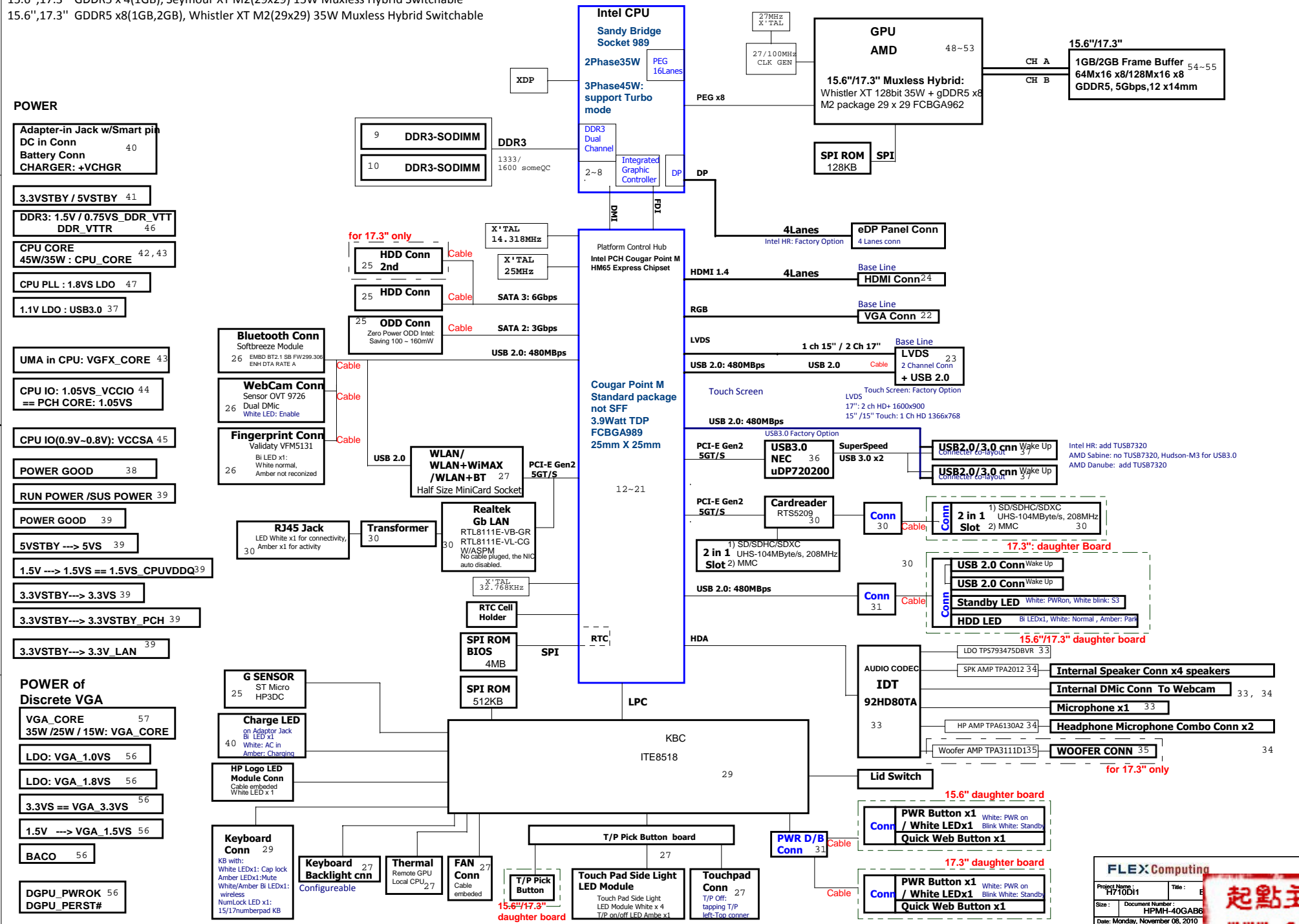


Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

15.6",17.3" GDDR5 x 4(1GB), Seymour XT M2(29x29) 15W Muxless Hybrid Switchable
15.6",17.3" GDDR5 x8(1GB,2GB), Whistler XT M2(29x29) 35W Muxless Hybrid Switchable



DMI
Differential 85ohm (single 50)
n,p mismatch <5mils
maximum mis-match between inter-pairs :
7000 mils (177.8 mm)
Max: [2000 to 8000 mils, 3vias]
436735 Huron River Design Guide 1.0

FDI
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
3vias : 2000 to 8000 mils
4vias : 2000 to 6500 mils

436735 Huron River Design Guide 1.0

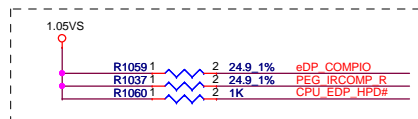
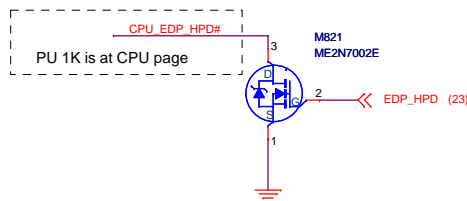
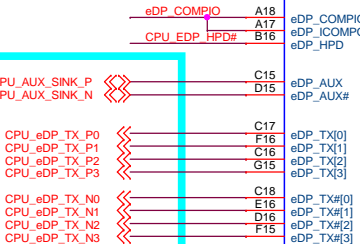
DP_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

DP_COMPIO :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
2vias : 2000 - 8000 mils
4vias : 2000 - 8000 mils

436735 Huron River Design Guide 1.0

eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
4vias : 2000 - 5000 mils
436735 Huron River Design Guide 1.0

[illegible]

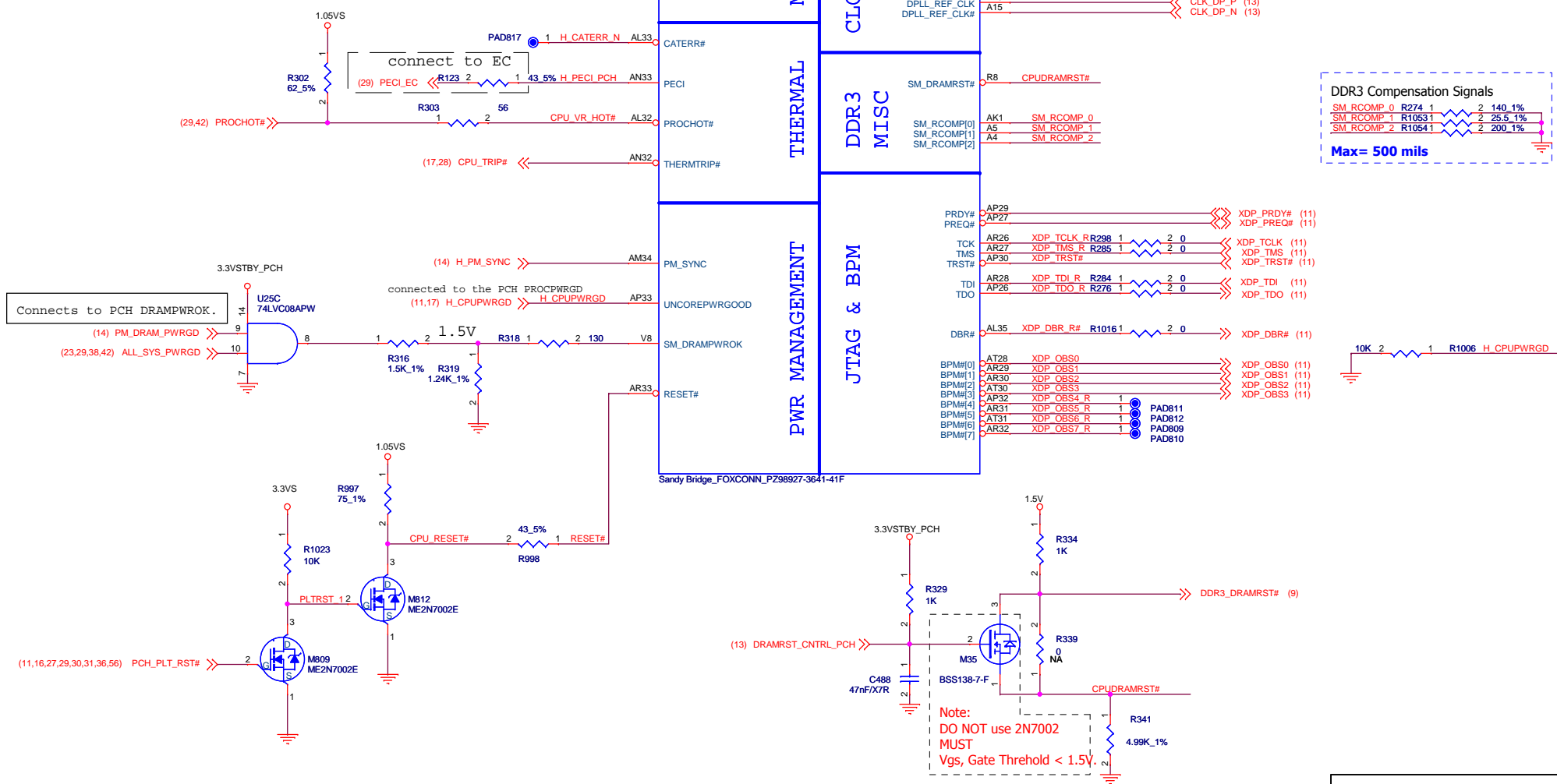
The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

HPMH-11-0010000110G	IC	CPU	SNB	1G8	Q15M	D0	rPGA988B
HPMH-11-00100000111G	IC	CPU	SNB	2G	Q15C	D0	rPGA988B
HPMH-11-00100000112G	IC	CPU	SNB	2G2	Q154	D0	rPGA988B
HPMH-11-00100000113G	IC	CPU	SNB	2G5	Q17N	J0	rPGA988B
HPMH-11-00100000114G	IC	CPU	SNB	2G6	Q16P	J0	rPGA988B
HPMH-11-00100000115G	IC	CPU	SNB	2G7	Q16M	J0	rPGA988B
HPMH-11-00100000116G	IC	CPU	SNB	2G5	Q17N	J0	rPGA988B
HPMH-11-00100000117G	IC	CPU	SNB	2G2	Q1CL	D1	rPGA988B
HPMH-11-00100000118G	IC	CPU	SNB	2G3	Q1CG	D1	rPGA988B
HPMH-11-00100000119G	IC	CPU	SNB	2G	Q1CN	D1	rPGA988B
HPMH-11-00100000120G	IC	CPU	SNB	2G	Q1NS	D2	rPGA988B
HPMH-11-00100000121G	IC	CPU	SNB	2G2	Q1NN	D2	rPGA988B
HPMH-11-00100000122G	IC	CPU	SNB	2G3	Q1NC	D2	rPGA988B
HPMH-11-00100000123G	IC	CPU	SNB	2G1	Q1SP	J1	rPGA988B
HPMH-11-00100000124G	IC	CPU	SNB	2G3	Q1SD	J1	rPGA988B
HPMH-11-00100000125G	IC	CPU	SNB	2G5	Q1RX	J1	rPGA988B
HPMH-11-00100000126G	IC	CPU	SNB	2G6	Q1S6	J1	rPGA988B
HPMH-11-00100000127G	IC	CPU	SNB	2G7	Q1S2	J1	rPGA988B
HPMH-11-00100000128G	IC	CPU	SNB	2G	SR02Y	D2	rPGA988B
HPMH-11-00100000129G	IC	CPU	SNB	2G2	SR014	D2	rPGA988B
HPMH-11-00100000130G	IC	CPU	SNB	2G3	SR012	D2	rPGA988B

PEG_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length :500 mils (12.7 mm)

PEG_ICOMPI :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

Intel PEG
Differential 80ohm(single 48ohm)

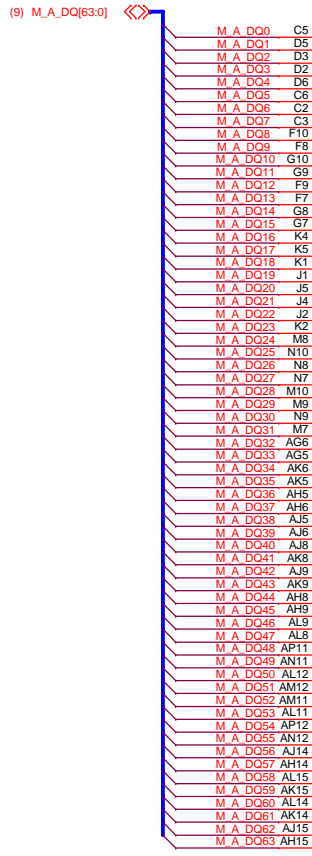


DDR3 Compensation Signals

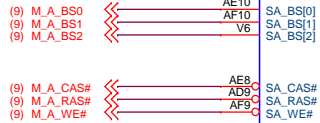
Signal	Value	Max
SM_RCOMP_0	R274 1	2 140.1%
SM_RCOMP_1	R1053 1	2 25.5.1%
SM_RCOMP_2	R1054 1	2 200.1%

Max= 500 mils

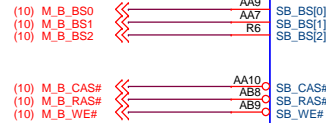
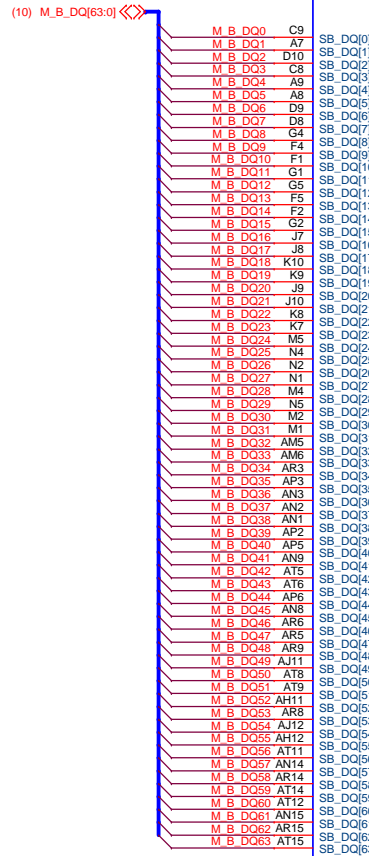
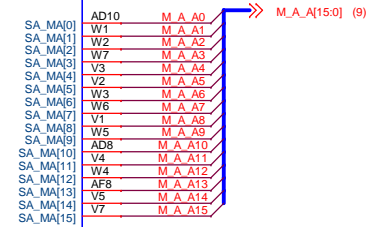
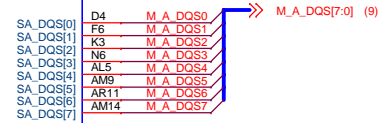
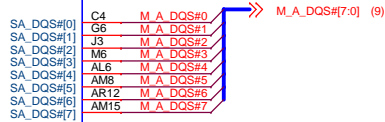
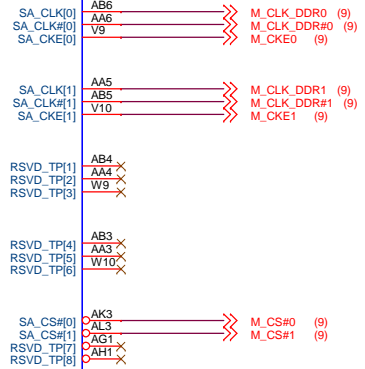
FLEX Computing			
Project Name : H710DI1		Title : CPU_2/7_CLK_MISC_THERM	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 3	of 63



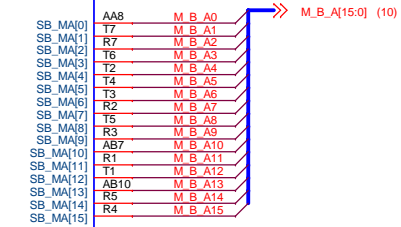
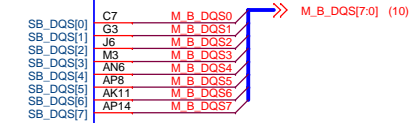
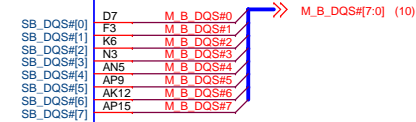
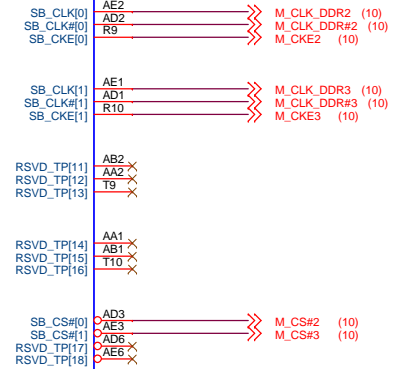
DDR SYSTEM MEMORY A



Sandy Bridge_FOXCNN_P298927-3641-41F



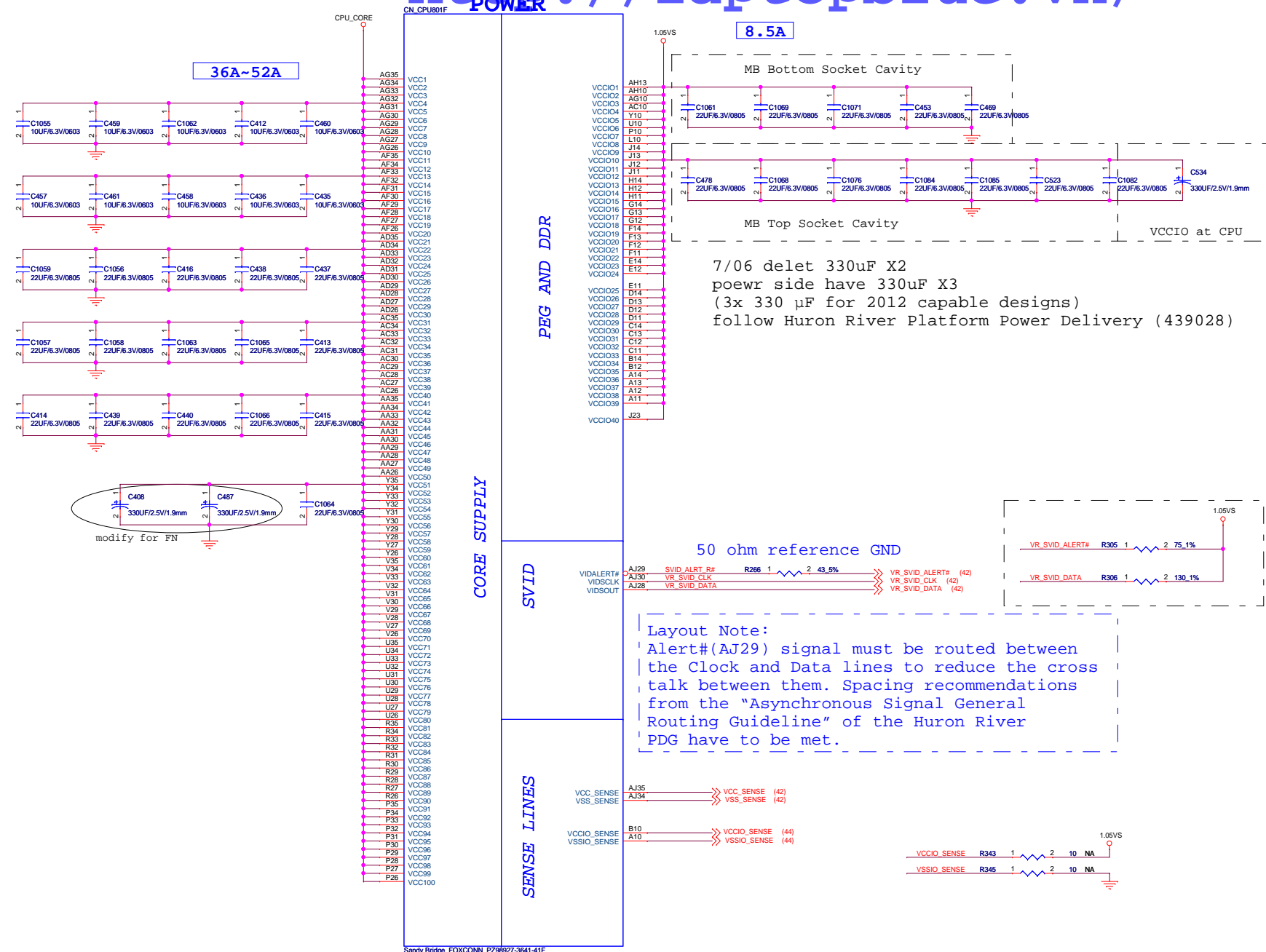
Sandy Bridge_FOXCNN_P298927-3641-41F

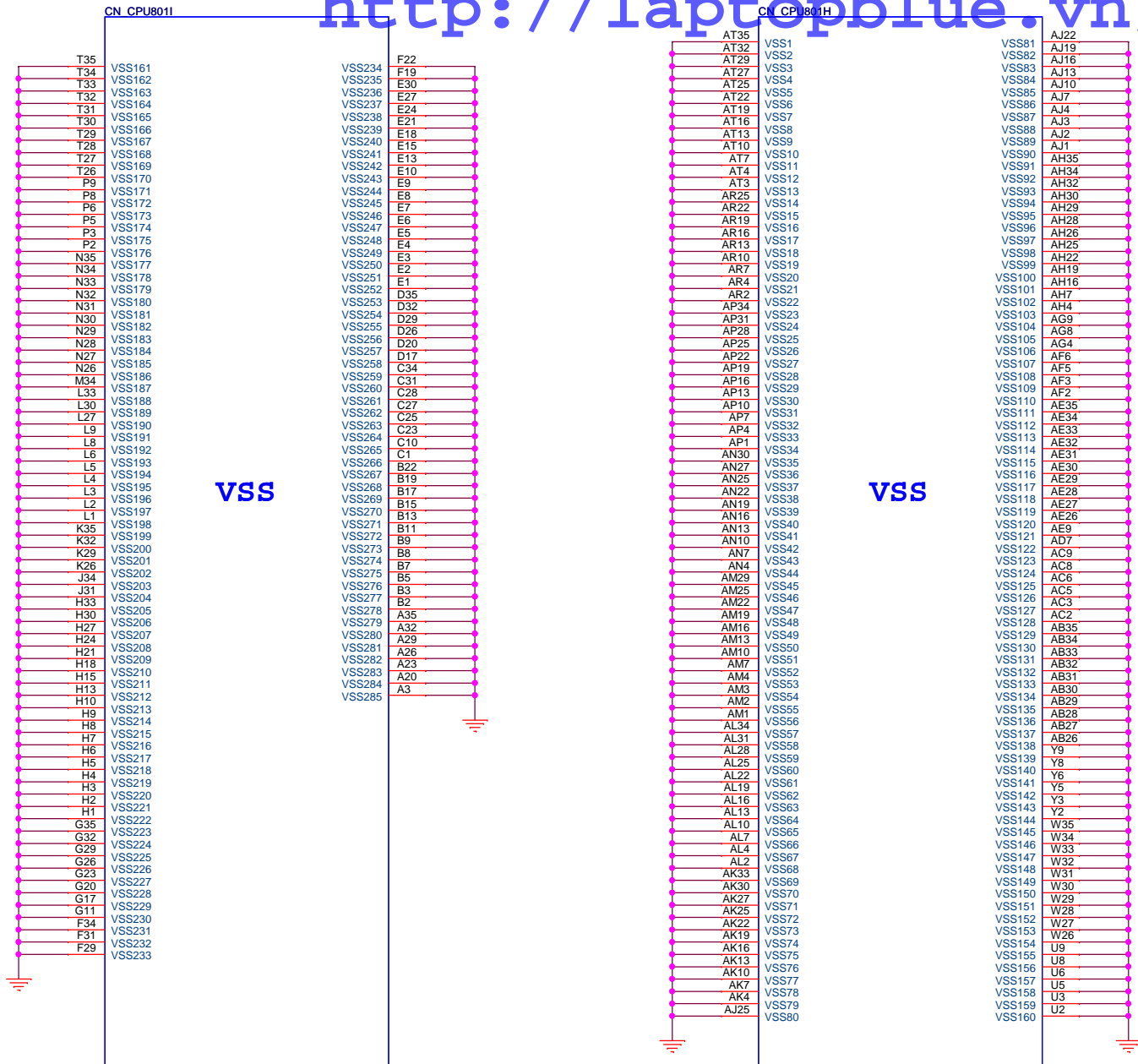


FLEX Computing

Project Name : H710D11		Title : CPU_3/7_DDR3	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 4	of 63



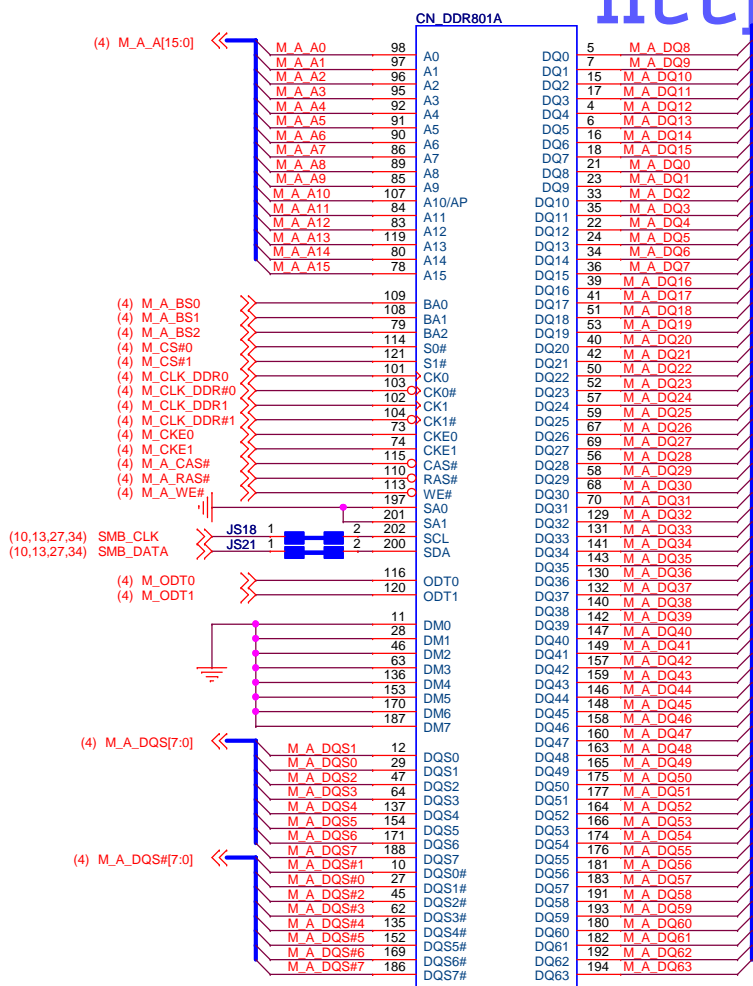




Sandy Bridge_FOXCONN_PZ98927-3641-41F

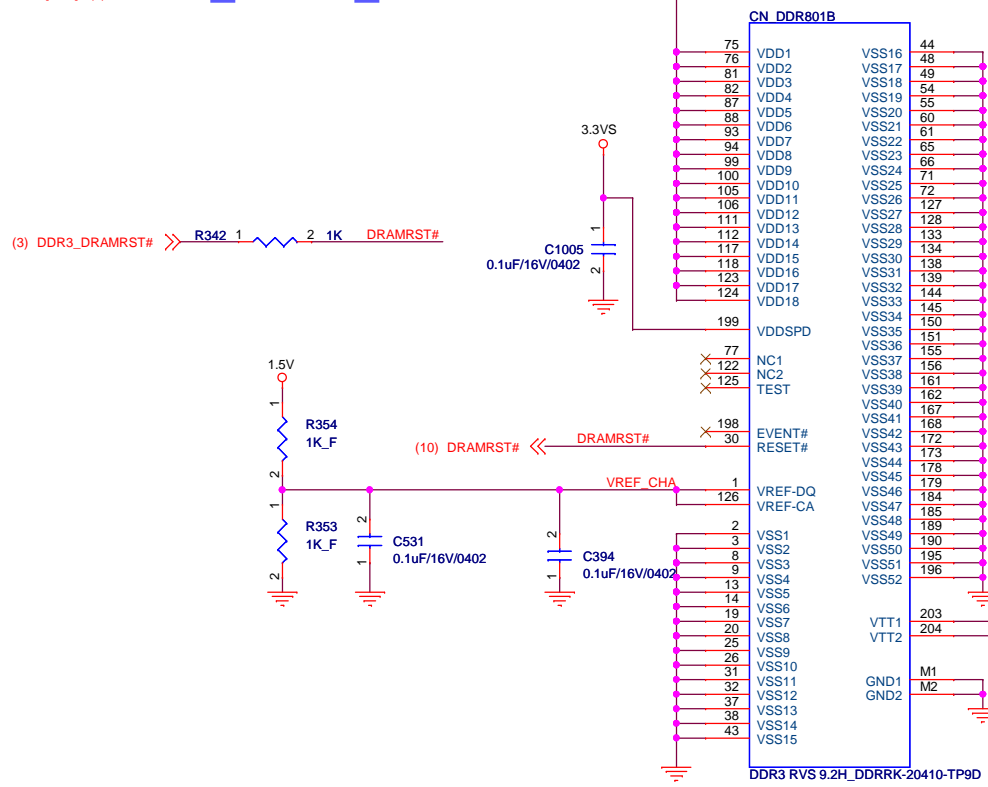
Sandy Bridge_FOXCONN_PZ98927-3641-41F

FLEX Computing		
Project Name : H710DI1		Title : CPU_7/7_VSS
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010		Sheet: 8 of 63



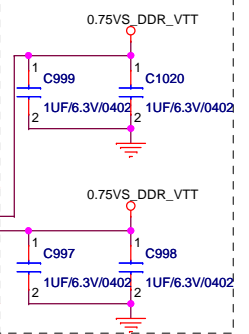
DDR3 RVS 9.2H_DDRRK-20410-TP9D
CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H

Note:
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

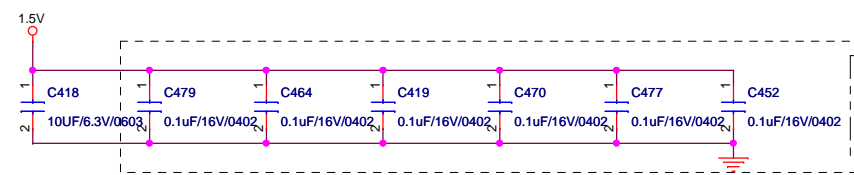


CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H

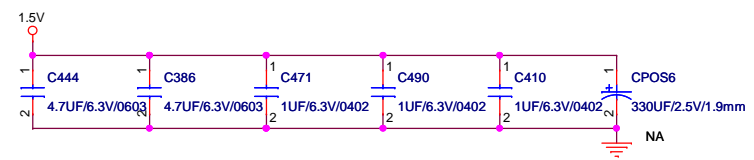
Layout
Place these caps close to Pin203 and 204.



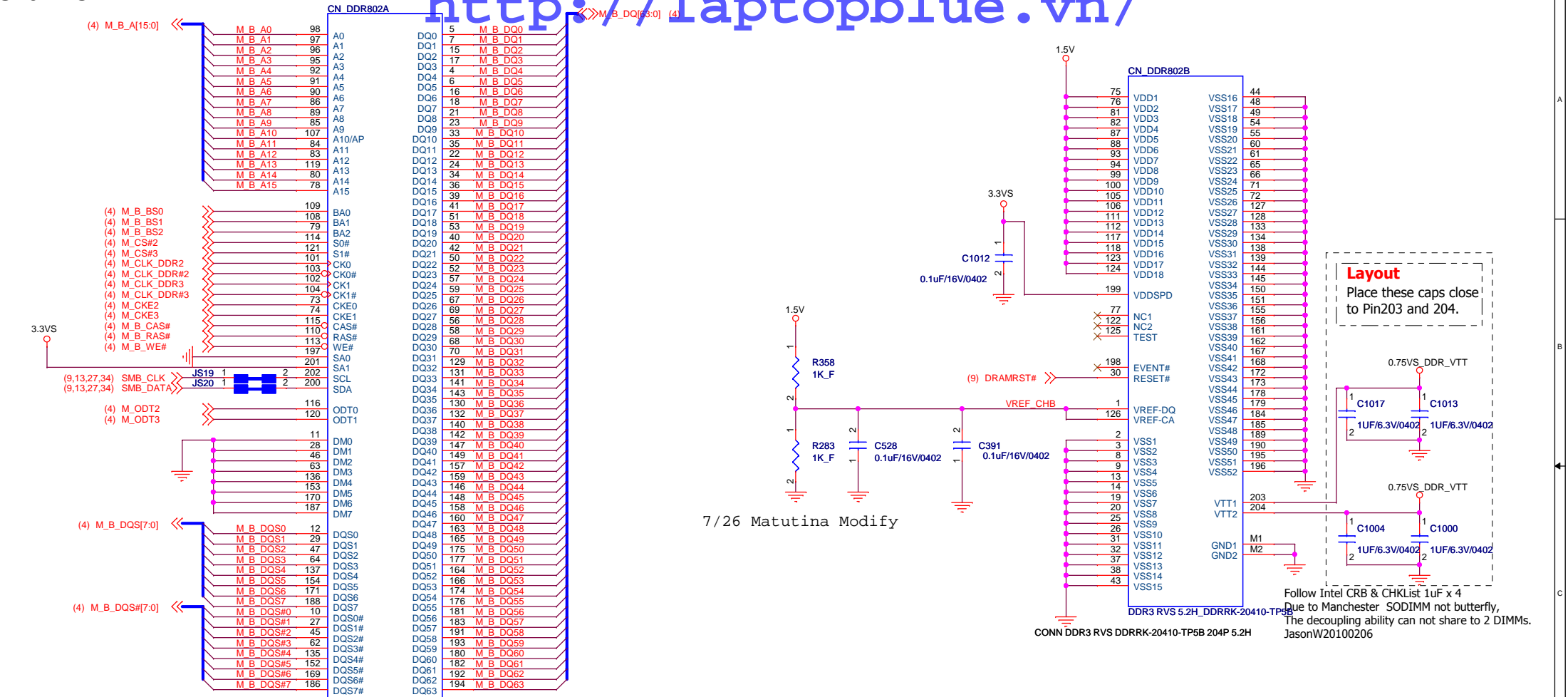
Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin.



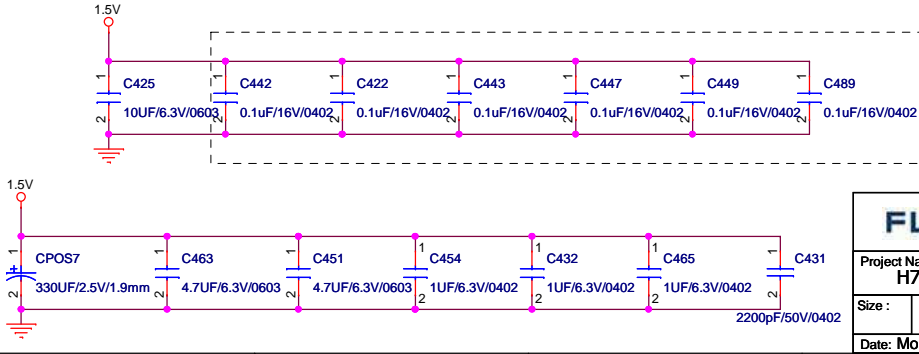
FLEXComputing		
Project Name :		Title :
H710DI1		DDR3_SO-DIMM1_CHA(9H2)
Size :	Document Number :	Rev :
	HPMH-40GAB6600-B130	B
Date: Monday, November 08, 2010		Sheet: 9 of 63



7/26 Matutina Modify

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMM Address			
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0	
	TS	0x30	
SA0_DIM1 = 0, SA1_DIM1 = 1	SPD	0xA4	
	TS	0x34	



Layout
Place these caps close to Pin203 and 204.

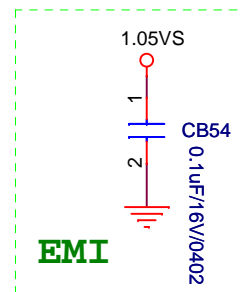
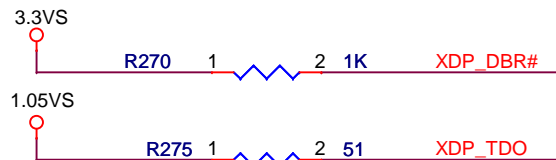
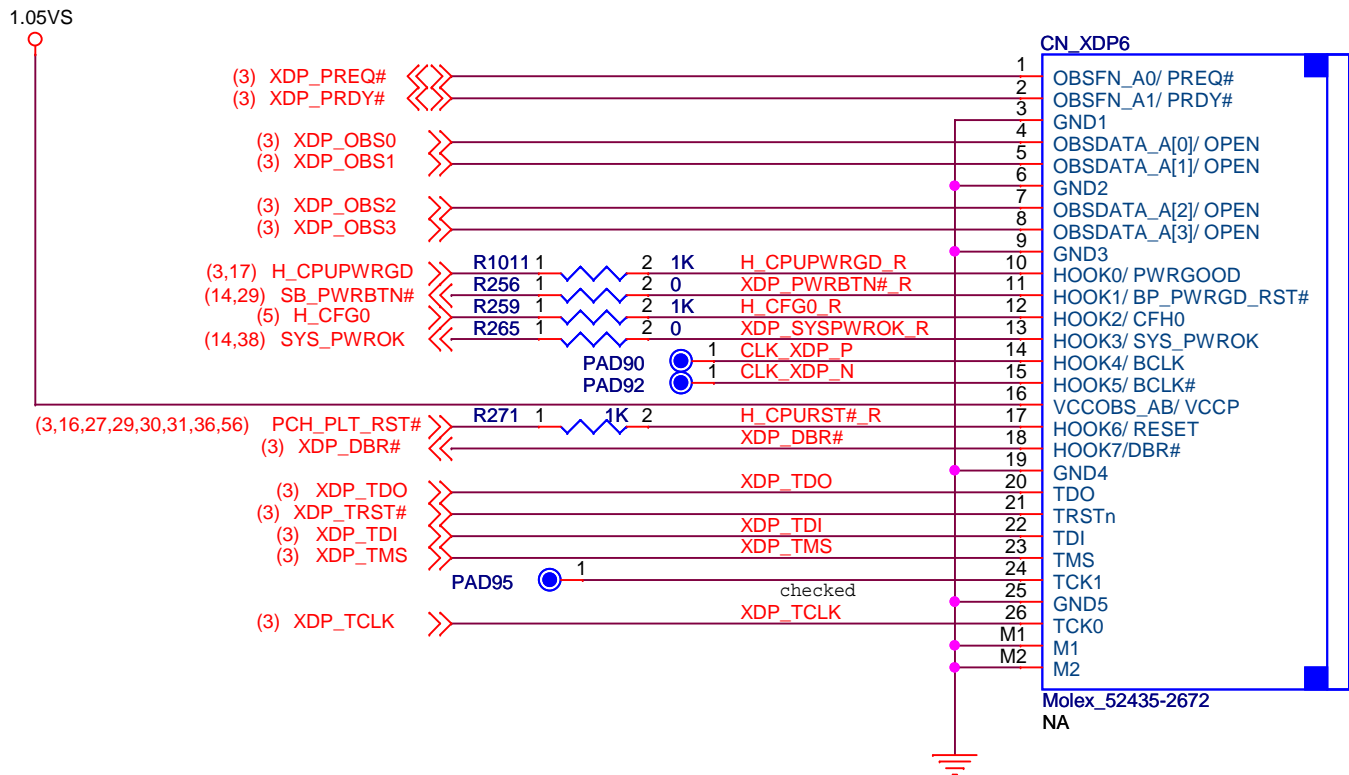
Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206

Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM
and close to VDD Pin .

FLEXComputing

Project Name :	H710DI1	Title :	DDR3_SO-DIMM2 CHB(5H2)
Size :	Document Number :	HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010		Sheet: 10	of 63

Debug Port



FLEX Computing

Project Name :
H710DI1

Title :
XDP(PROCESSOR / PCH)

Size :

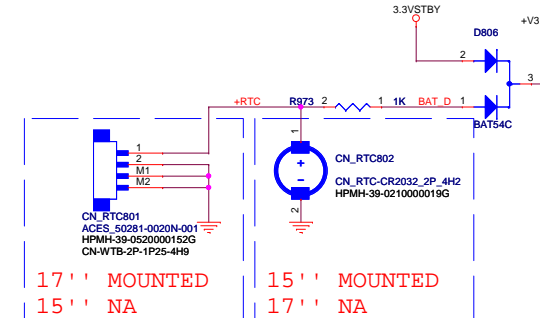
Document Number :
HPMH-40GAB6600-B130

Date: Monday, November 08, 2010

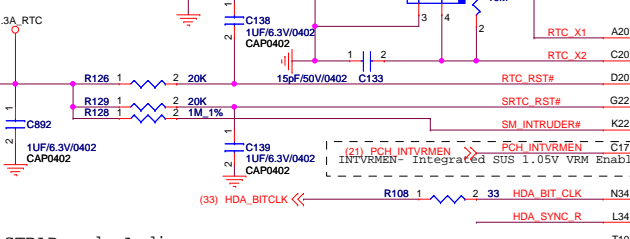
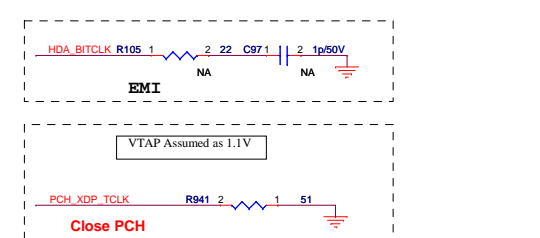
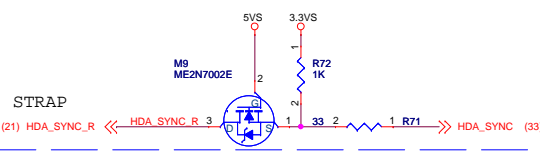
起點主板維修網
www.qdzbxw.com

	Mark
Pull-Up	P+
Pull-Down	P-

COUGARPOINT (HDA,JTAG,SPI,SATA)



Design Guide 1.2 (#436735)
HDA_SYNC Potential Leakage Concern



STRAP and Audio



STRAP (21,29) PCH_HDA_SDO



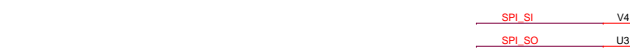
(17) PCH_GPI3



(11) PCH_XDP_TCLK



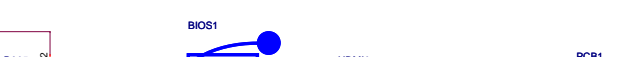
(11) PCH_XDP_TMS



(11) PCH_XDP_TDI



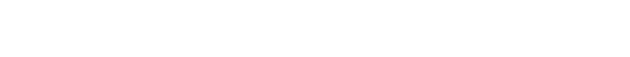
(11) PCH_XDP_TDO



(11) PCH_XDP_TDO



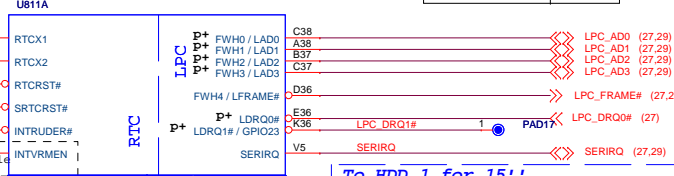
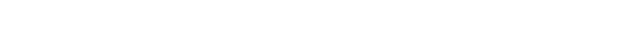
(11) PCH_XDP_TDO



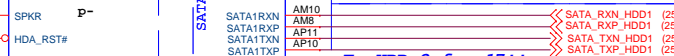
(11) PCH_XDP_TDO



(11) PCH_XDP_TDO



RTC



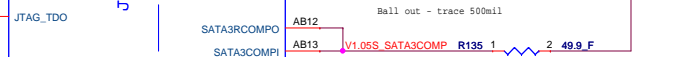
RTC



RTC



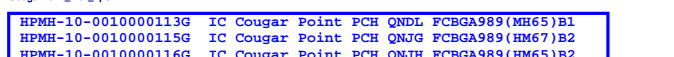
RTC



RTC



RTC



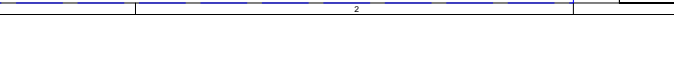
RTC



RTC



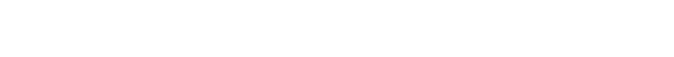
RTC



RTC



RTC



RTC



LPC



LPC



LPC



LPC



LPC



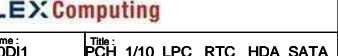
LPC



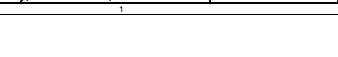
LPC



LPC



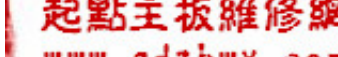
LPC



LPC

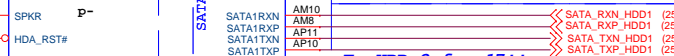


LPC



LPC

SATA 6G



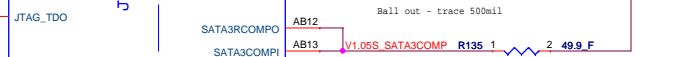
SATA 6G



SATA 6G



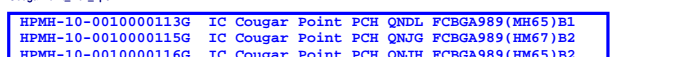
SATA 6G



SATA 6G



SATA 6G



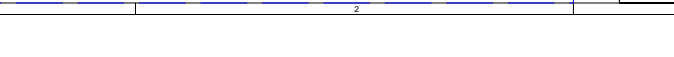
SATA 6G



SATA 6G



SATA 6G



SATA 6G



SATA 6G



SATA 6G

To HDD 1 for 15''



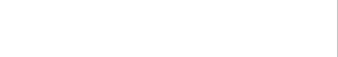
To HDD 1 for 15''



To HDD 1 for 15''



To HDD 1 for 15''



To HDD 1 for 15''



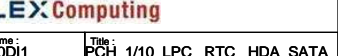
To HDD 1 for 15''



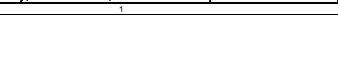
To HDD 1 for 15''



To HDD 1 for 15''



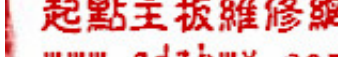
To HDD 1 for 15''



To HDD 1 for 15''

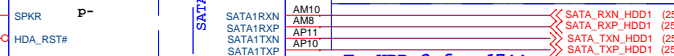


To HDD 1 for 15''



To HDD 1 for 15''

To HDD 2 for 17''



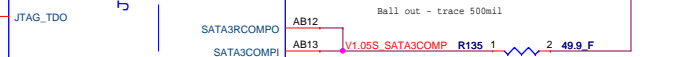
To HDD 2 for 17''



To HDD 2 for 17''



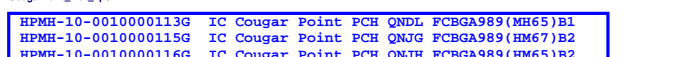
To HDD 2 for 17''



To HDD 2 for 17''



To HDD 2 for 17''



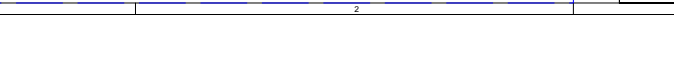
To HDD 2 for 17''



To HDD 2 for 17''



To HDD 2 for 17''



To HDD 2 for 17''



To HDD 2 for 17''



To HDD 2 for 17''

H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



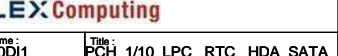
H61 SATA ports 2 and 3 are disabled



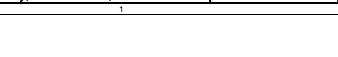
H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled

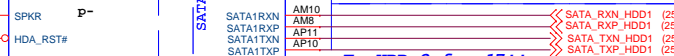


H61 SATA ports 2 and 3 are disabled



H61 SATA ports 2 and 3 are disabled

For BIOS power saving check



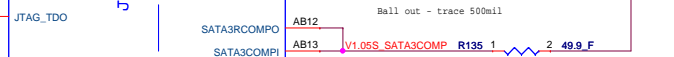
For BIOS power saving check



For BIOS power saving check



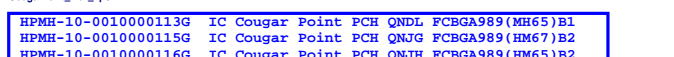
For BIOS power saving check



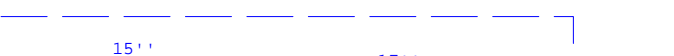
For BIOS power saving check



For BIOS power saving check

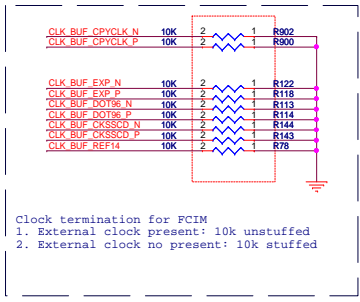
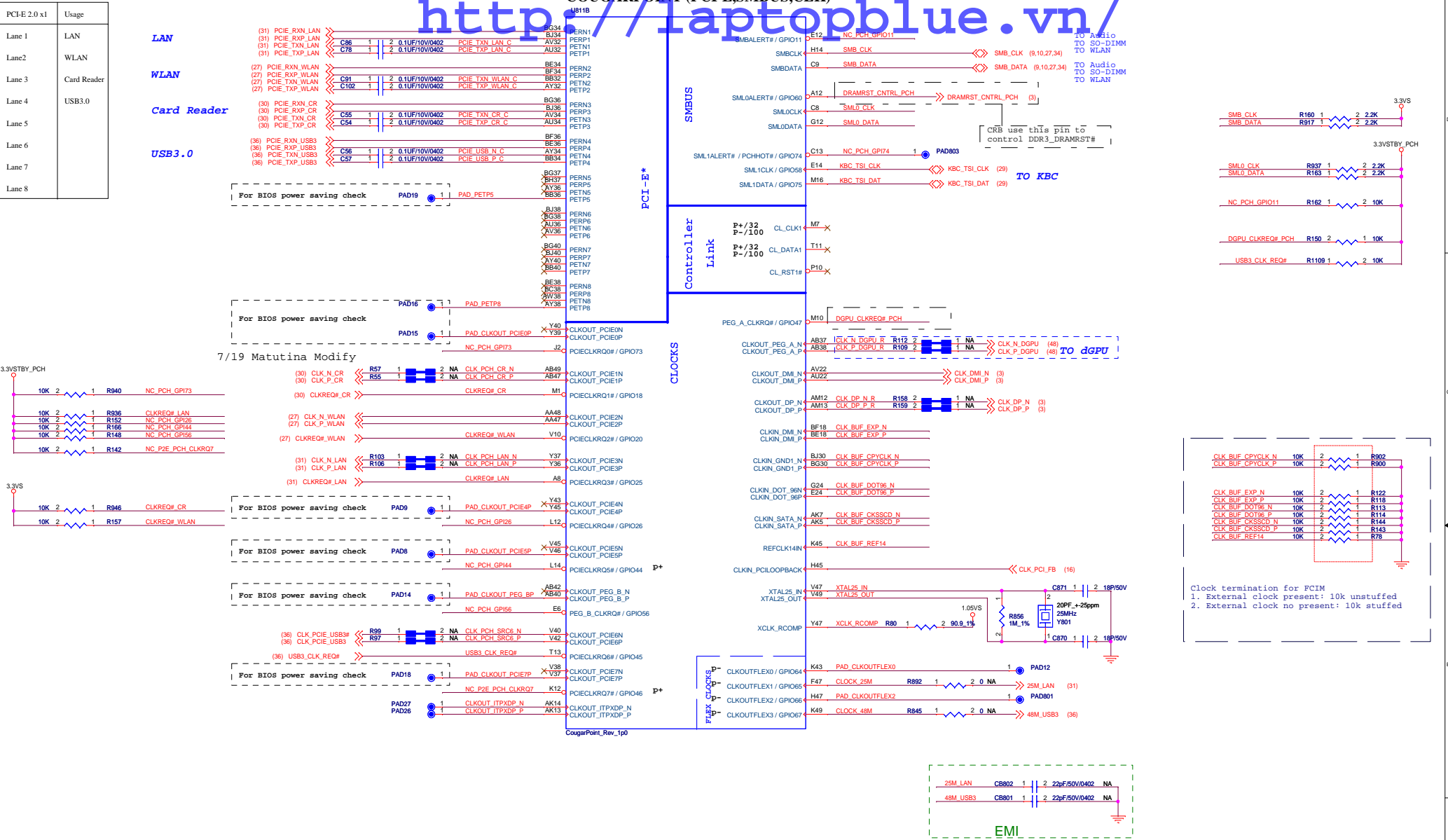


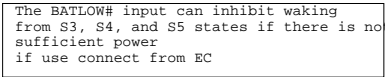
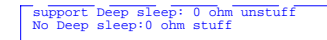
For BIOS power saving check

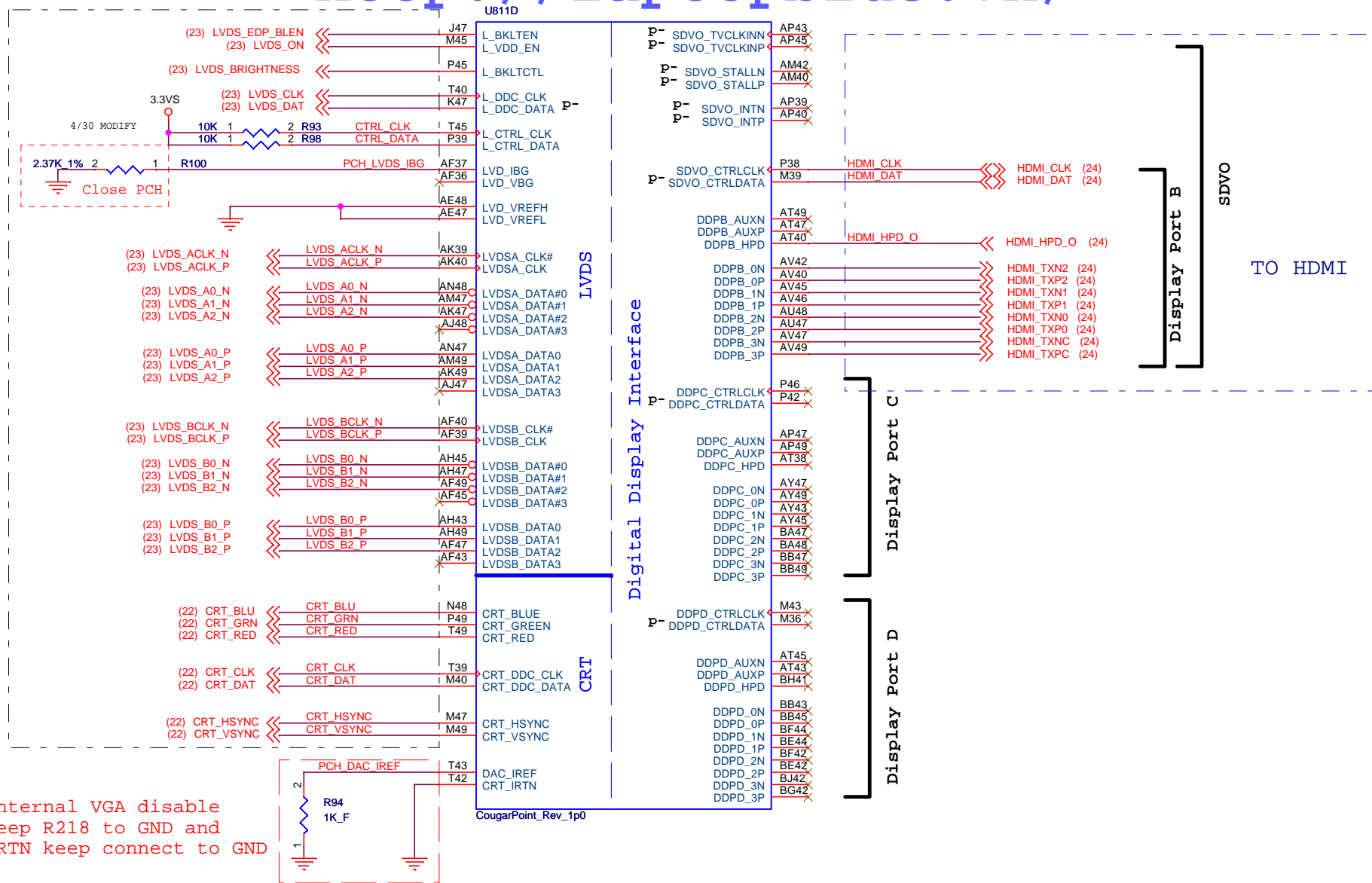


For BIOS power saving check

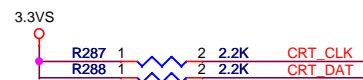
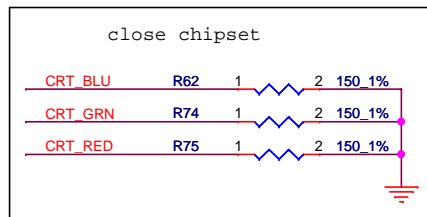
PCI-E 2.0 x1	Usage
Lane 1	LAN
Lane 2	WLAN
Lane 3	Card Reader
Lane 4	USB3.0
Lane 5	
Lane 6	
Lane 7	
Lane 8	

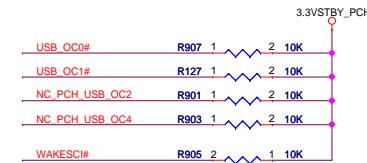


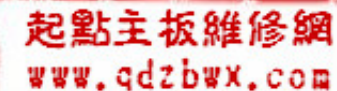


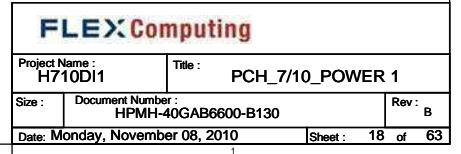


Internal VGA disable
keep R218 to GND and
IRTN keep connect to GND











U811I

U811H

H5

CougarPoint_Rev_1p0

FLEX Computing

Project Name :
H710D11Title :
PCH_9/Size : Document Number :
HPMH-40GAB6600-B13

Date: Monday, November 08, 2010

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Signal	Usage	When Sampled	Internal PULL	Comment
SPKR	No Reboot	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers' Offset (3410h:Bit 5). Default
INIT3_3V#	Reserved	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	This signal should not be pulled low
GNT[3]#/GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Top Block Swap Mode disabled Default L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	NA	H: Integrated 1.05V VRMs enabled Default This signal should always be External pulled high L: Integrated 1.05V VRMs disabled
GNT1#/GPIO51/ BBS[1]	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	GNT1# SATA1GP Boot BIOS Location 0 0 LPC 0 1 Reserved 1 0 PCI 1 1 SPI Default
SATA1GP/ GPIO19	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	
GNT2#/GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Should not be pulled low for desktop and mobile Default ESI compatible mode is for server platforms only. L: Configures DMI for ESI compatible operation
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Internal PD	H: If sampled high, the Flash Descriptor Security will be overridden. L: If strap is sampled low, (Default) the security measures defined in the Flash Descriptor will be in effect. This signal should not be pulled high
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	Internal PD	The internal pull-down is disabled after PLTRST# deasserts
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Internal PU	H: The On-Die PLL voltage regulator is enabled when sampled high Default L: When sampled low the On-Die PLL Voltage Regulator is disabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Internal PD	H: On-Die PLL VR is supplied by 1.5 V Default L: On-Die PLL VR is supplied by 1.8 V
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Internal PD The weak internal pull-down is disabled after RSMRST# deasserts	H: Intel ME Crypto TLS cipher suite with confidentiality Default L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	Internal PD The internal pull-down is disabled after PLTRST# deasserts.	H: LVDS is detected Default L: LVDS is not detected
SDVO_CTLRDATA	Port B Detected	Rising Edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port B is detected Default L: Port B is not detected
DDPC_CTLRDATA	Port C Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port C is detected Default L: Port C is not detected
DDPD_CTLRDATA	Port D Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port D is detected Default L: Port D is not detected
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	NA	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: NOTE: This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	Internal PU (Pull-up is disabled after RSMRST# is deasserted.)	NOTE: This signal should not be pulled low

NO REBOOT	
NA	Low=Disable(Default)
MOUNTED	High=Enable

PAD24 1 SPKR (12,33)

PAD21 1 INIT3_3V# (17)

R70 1 2 1K NA STRAP_GNT3# (16)

+V3.3A_RTC
R896 1 2 330K PCH_INTVRMEN (12)

R69 1K NA R943 1K NA
STRAP_GNT1# (16)
STRAP_SATA1GP (12)

PAD10 1 STRAP_GNT2# (16)

3.3VS
R1115 1 2 1K NA PCH_HDA_SDO (12,29)

1.8VS
R933 2 2.2K
PLACE 2.2K CLOSE TO THE BRANCHING POINT
(3) H_SNB_IVB# R929 1 2 1K DF_TVS (17)

PAD35 1 PLL_ODVR_EN (17)

3.3VSBY_PCH
R107 1 2 1K HDA_SYNC_R (12)

3.3VSBY_PCH
R939 1 2 1K NA STRAP_PCH_GPI15 (17)

A16 swap override Strap	
STP_A160VR	Low = A16 swap override High = Default

INTVRMEN- Integrated SUS
1.05V VRM Enable

Flash Descriptor Security Override	
PCH_HDA_SDO	NA Low=Disable(Default) MOUNTED High=Enable

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

PLL ON DIE VR ENABLE	
PLL_ODVR_EN	ENABLE- UNSTUFF DISABLE-STUFF

HR only support 1.5 V
HDA_SYNC need PU to HDA SUS rail through 1k ohm
for 451710_451710 SPEC

+V3.3A_RTC
R1067 1 2 330K
R899 1 2 330K NA DSWODVRN (14)

R1110 1 2 10K NC_PCH_GPI36 (17)

R151 1 2 10K FDI_OVRVLTG (17)

R918 1 2 1K STRAP_PCH_GPO8 (17)

DSWODVRN - On Die DSW VR Enable	
Pull High	Enable (Default)
Pull Down	Disable

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

GPIO8 Integrated Clock Chip Enable	
High	Disable
Low	Enable(default)

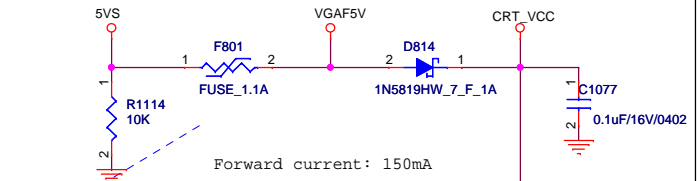
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Project Name :	H710DI1
Size :	Document Number : HPM
Date :	Monday, November

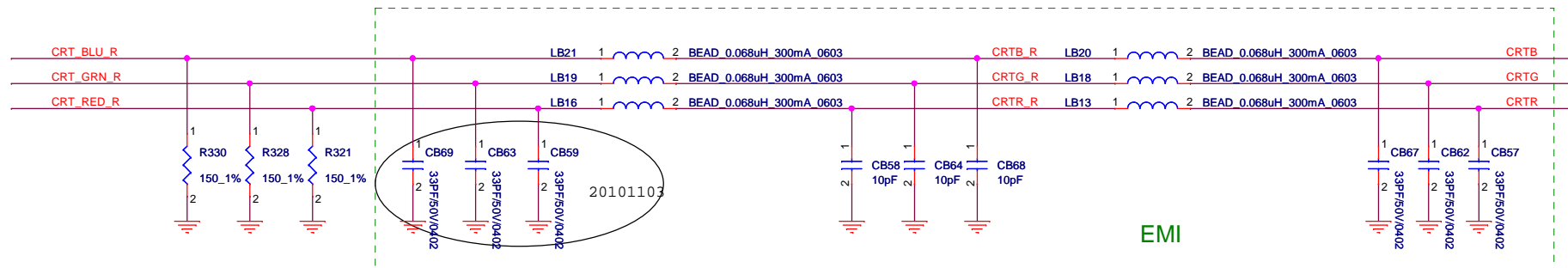
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for CRT Conn




Check with Connector spec



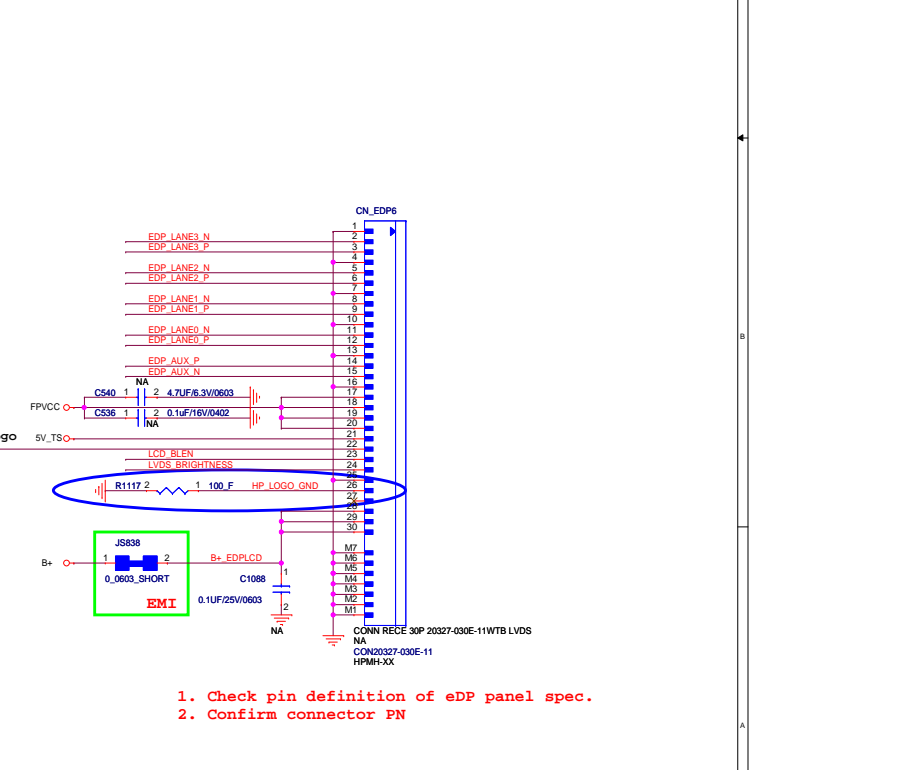
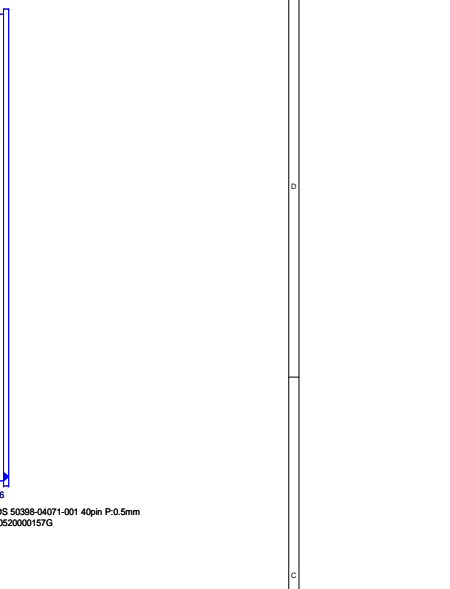
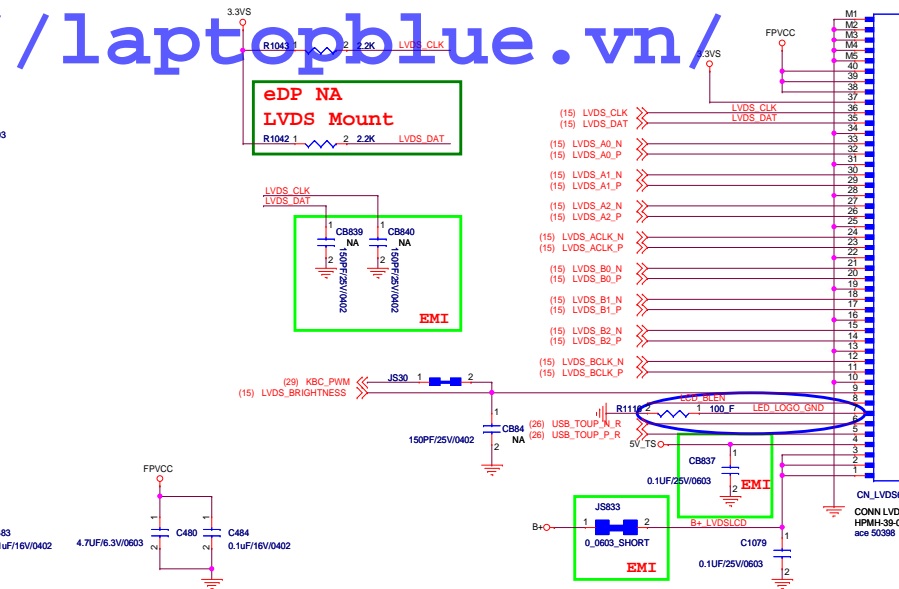
(15) CRT_BLU << JS832 1  2 NA CRT_BLU_R

(15) CRT_GRN << JS831 1  2 NA CRT_GRN_R

(15) CRT_RED << JS829 1  2 NA CRT_RED_R

Project Name : H710DI1		Title : CRT CONN	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet :	22 of 63

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|---------------------------|-----------------------------|
| FLEX Computing | |
| Project Name :
H710DI1 | |
| Size : | Document Number :
HPMH-4 |
| Date: Monday, November | |

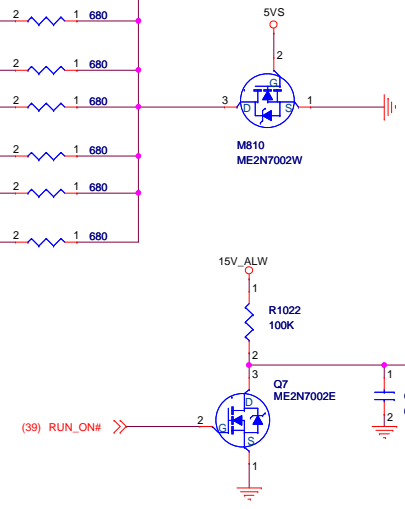
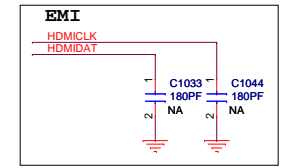
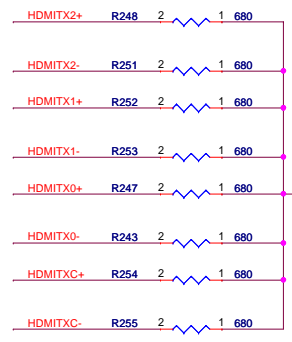
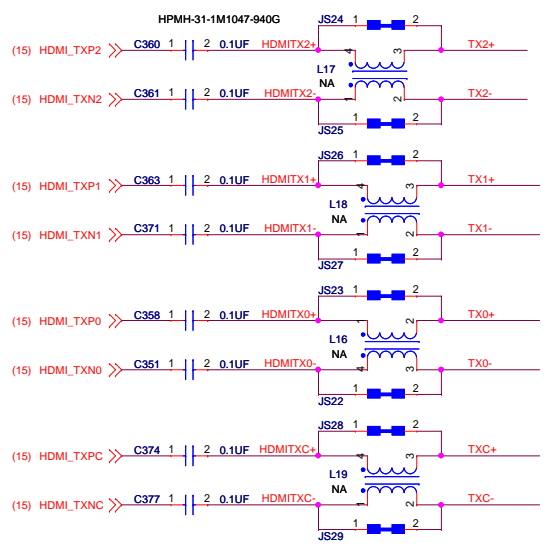
HDMI

<http://laptopblue.vn/>

CLOSE to CN_HDMI1

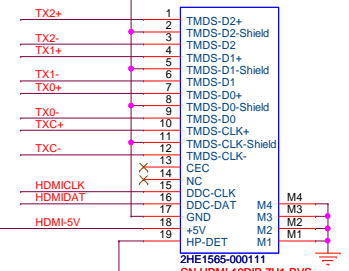
HPMH-32-4000000104G

Intel Huron River: 680 ohm
AMD Danube: 715 ohm
AMD Sabine: 715 ohm

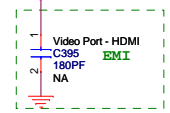
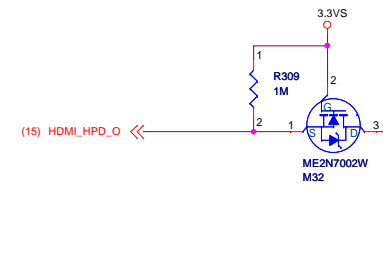
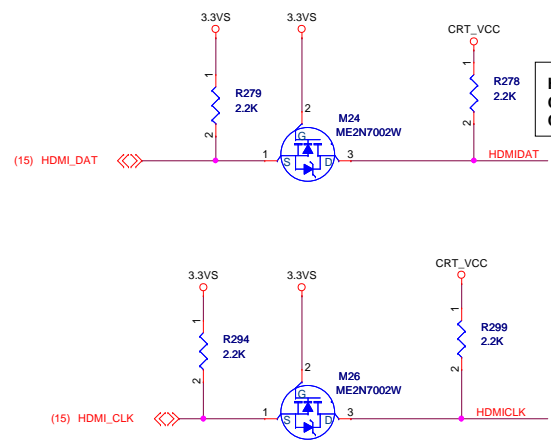


HDMI

CN_HDMI801



2HE1565-000111
CN-HDMI-19DIP-7H1-RVS
HPMH-38-00F0000017G

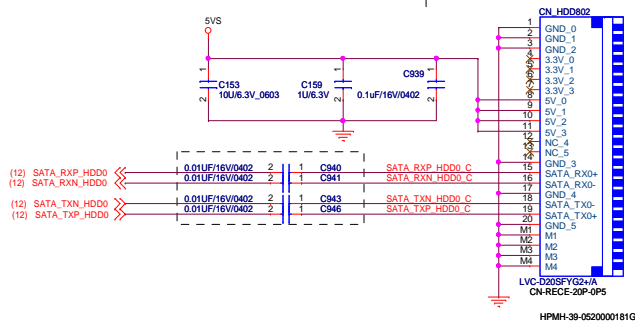


FLEX Computing			
Project Name : H710DI1		Title : HDMI CONN	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date : Monday, November 08, 2010		Sheet : 24 of 63	

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HDD

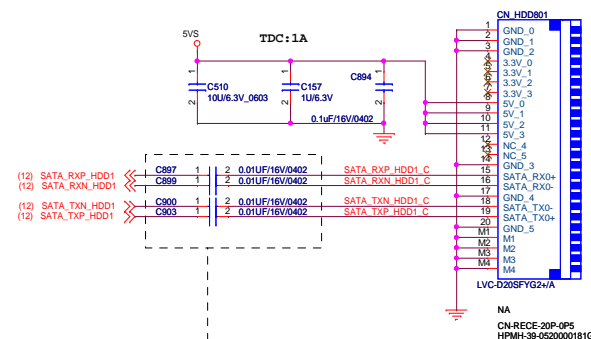
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist



2nd HDD

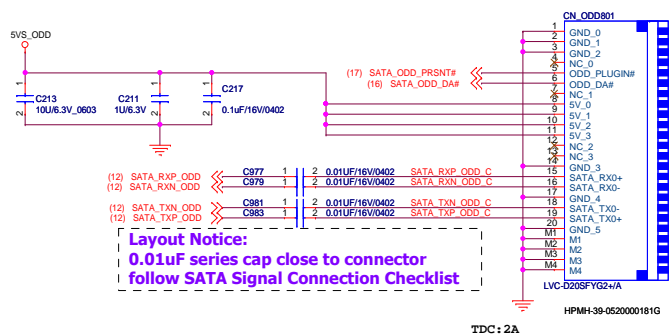
FOR 17" MB USE WTB CONNECTOR

CONN SPEC:0.3A/PIN



Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

ODD



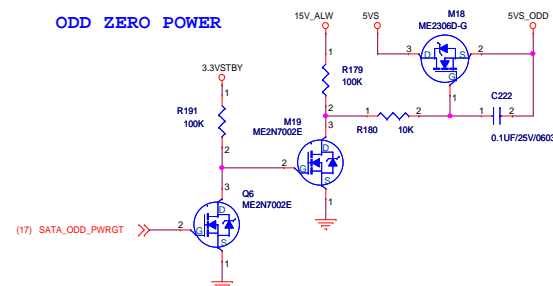
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

TDC: 2A

Change to Cable type Conn

ODD Zero Power

Check if meet max current!!



G-Sensor

G-SENSOR

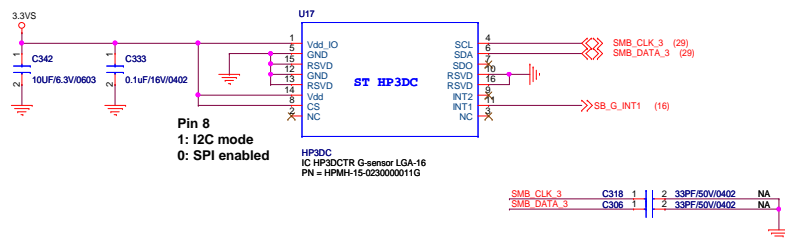
ST HP3DC

3.3VS

ADDR: 0011000x(30h) - SDO PD

ADDR: 0011010x(32h) - SDO NC

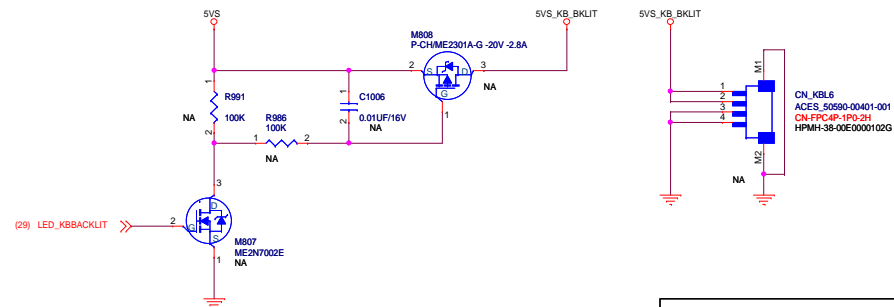
SINK: ??mA@VoL=0.33V(MAX)



Pin 8
1: I2C mode
0: SPI enabled

HP3DC
IC HP3DCTR G-sensor LGA-16
PN = HPMH-15-023000011G

KB Backlit



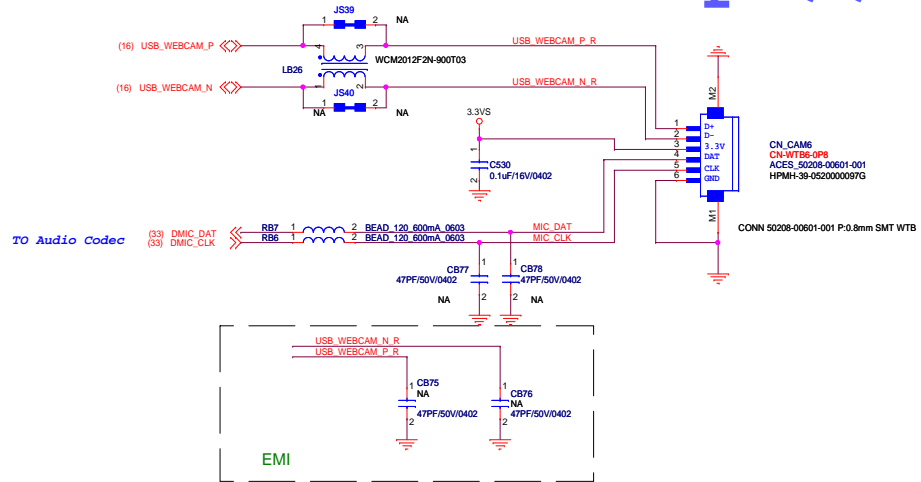
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Project Name :
H710D11
Size :
Document Number :
HPMH-
Date: Monday, November

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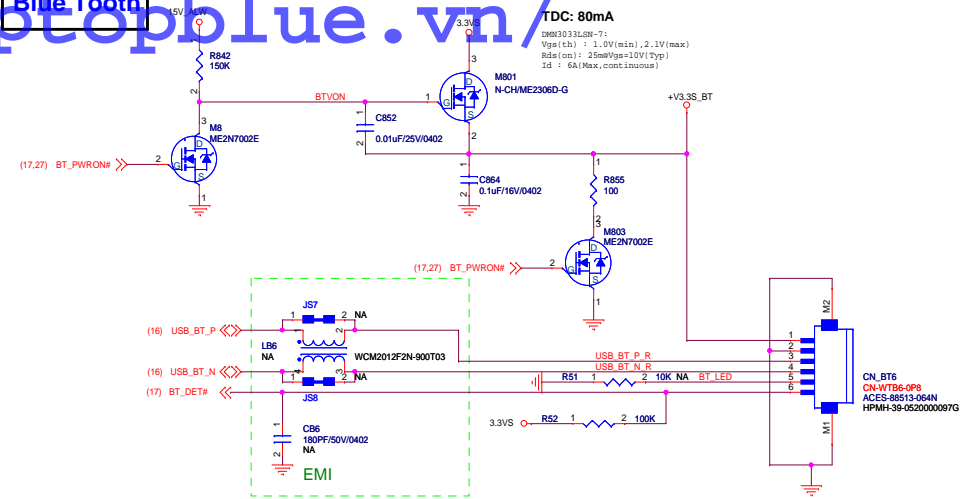
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Web CAM



<http://laptopblue.vn/>

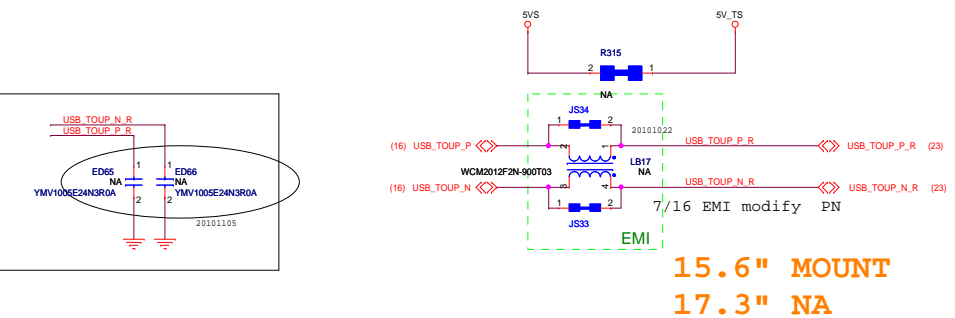
Blue Tooth



TouchScreen (Module CONN)

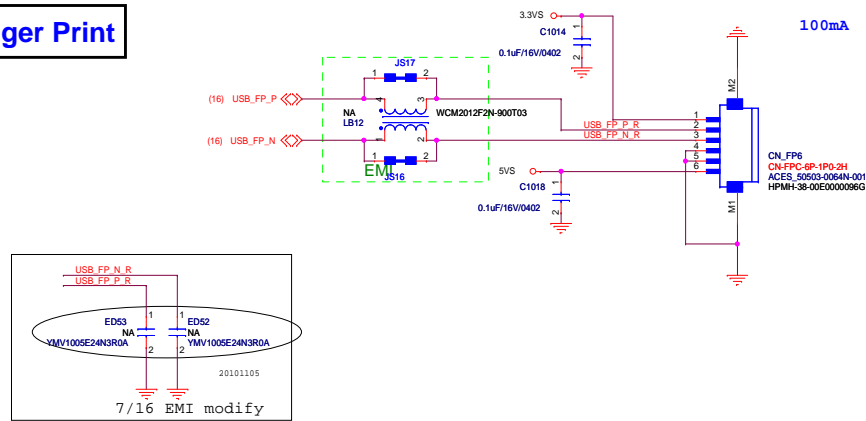
Touch Screen power is 5V type

Peak 200mW 40mA

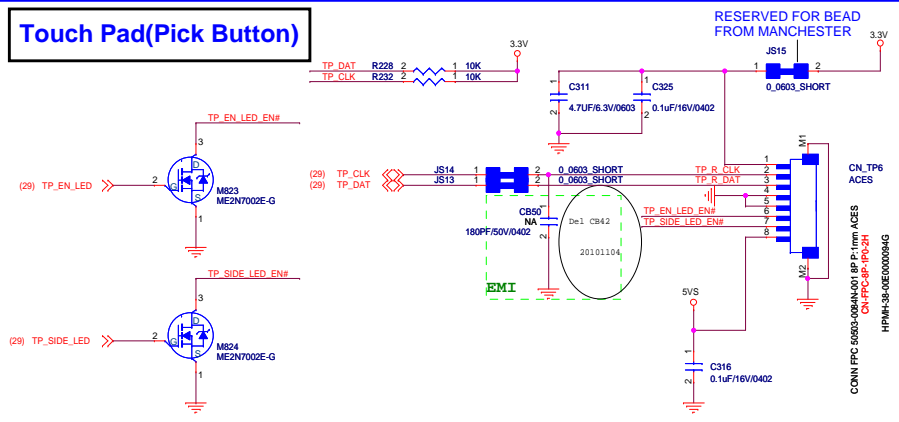


15.6" MOUNT
17.3" NA

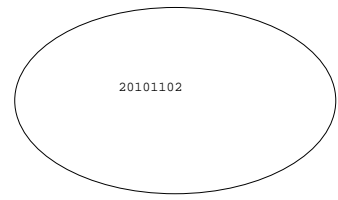
Finger Print



Touch Pad(Pick Button)



LID

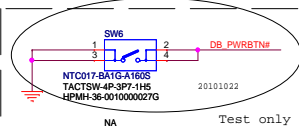
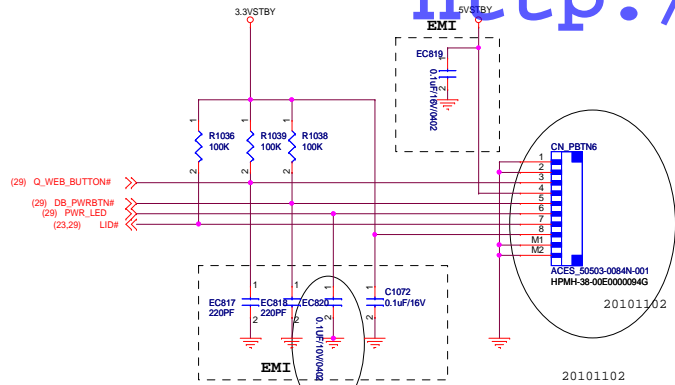


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Project Name :	H710D11
Size :	Document Number :
Date :	Monday, November

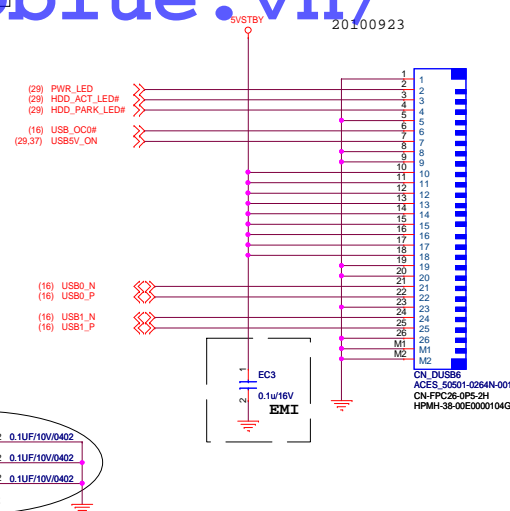
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PWRBTN BOARD

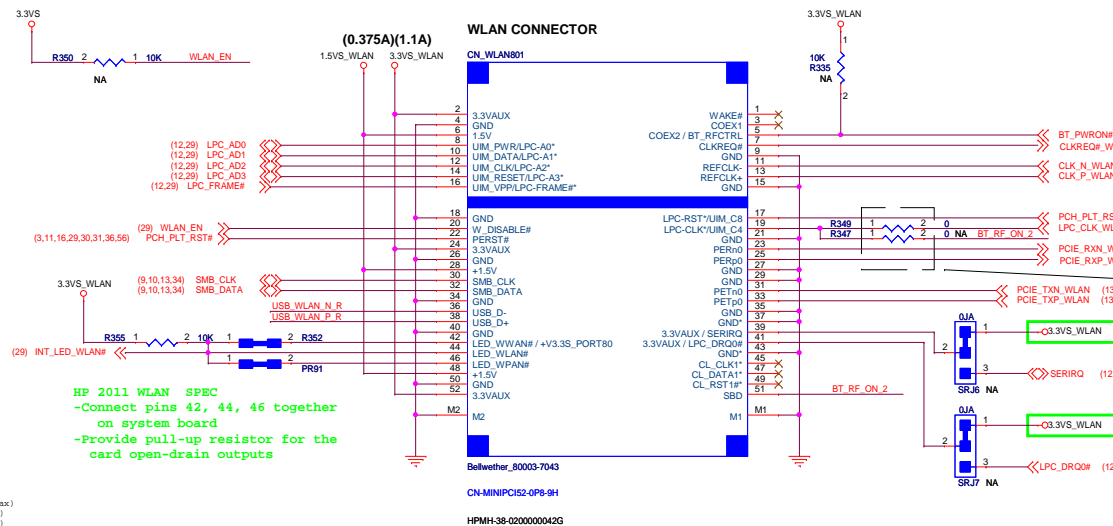
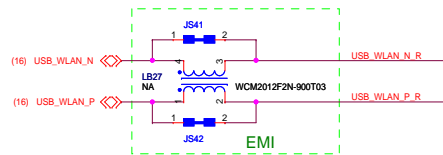


connector on Mother Board for
Power Button/LED/LID Daughter board

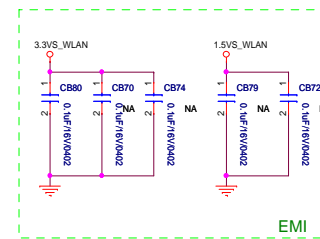
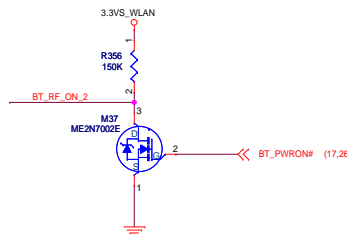
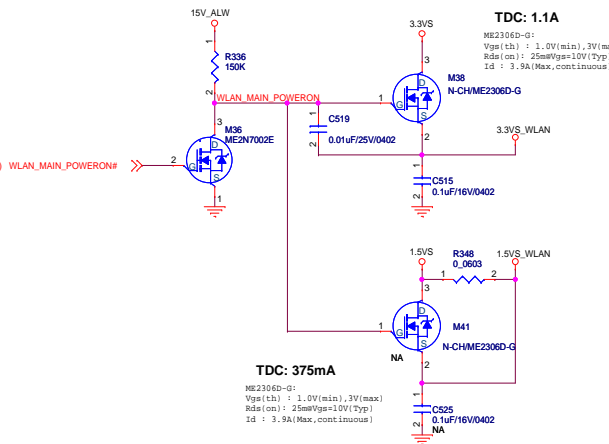
USB BOARD



Mini-PCIE - WLAN (Half size)



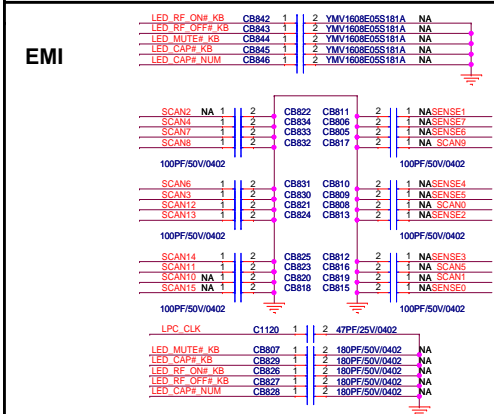
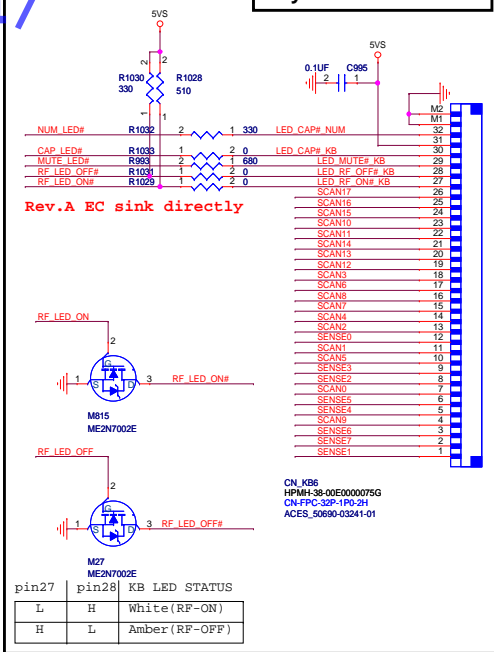
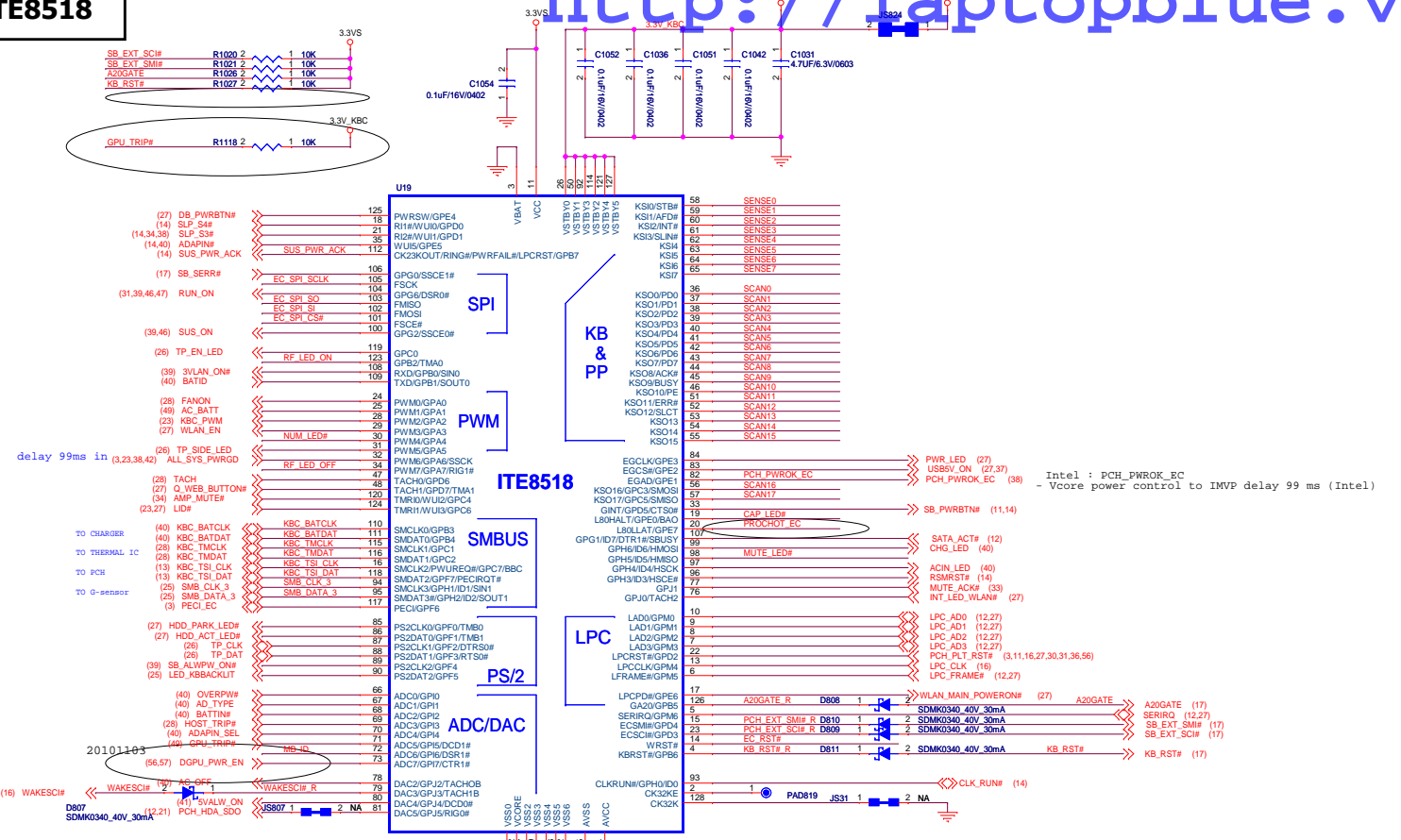
HP 2011 WLAN SPEC 2nd RF ON/OFF Pin
Primary path is to implement it on pin 51,
but 0 Ohm strap to pin 19 required for
Intel Rainbow Peak ES2 cards use
(QS will transition to pin 51).



KBC
ITE8518

http://laptopblue.vn/

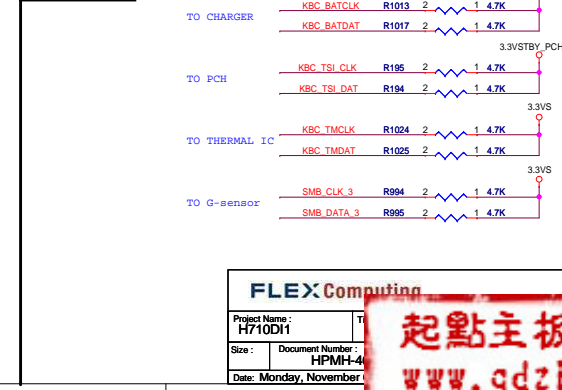
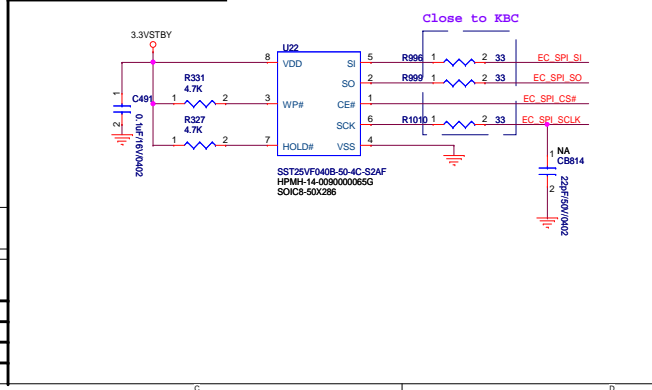
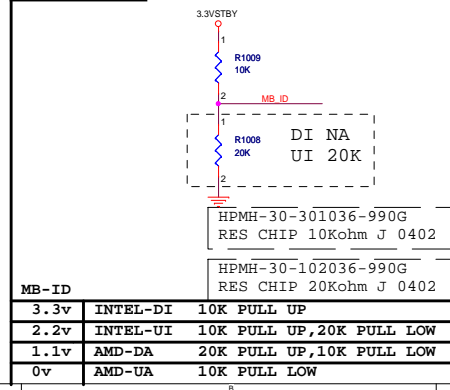
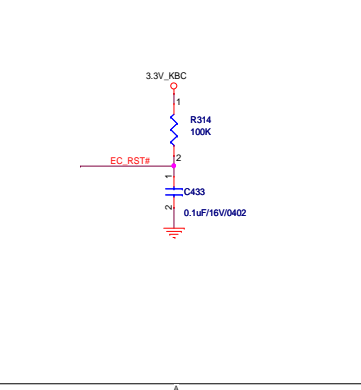
Keyboard Connector



Board ID

SPI ROM (512KB)

SM BUS



FLEX Computing

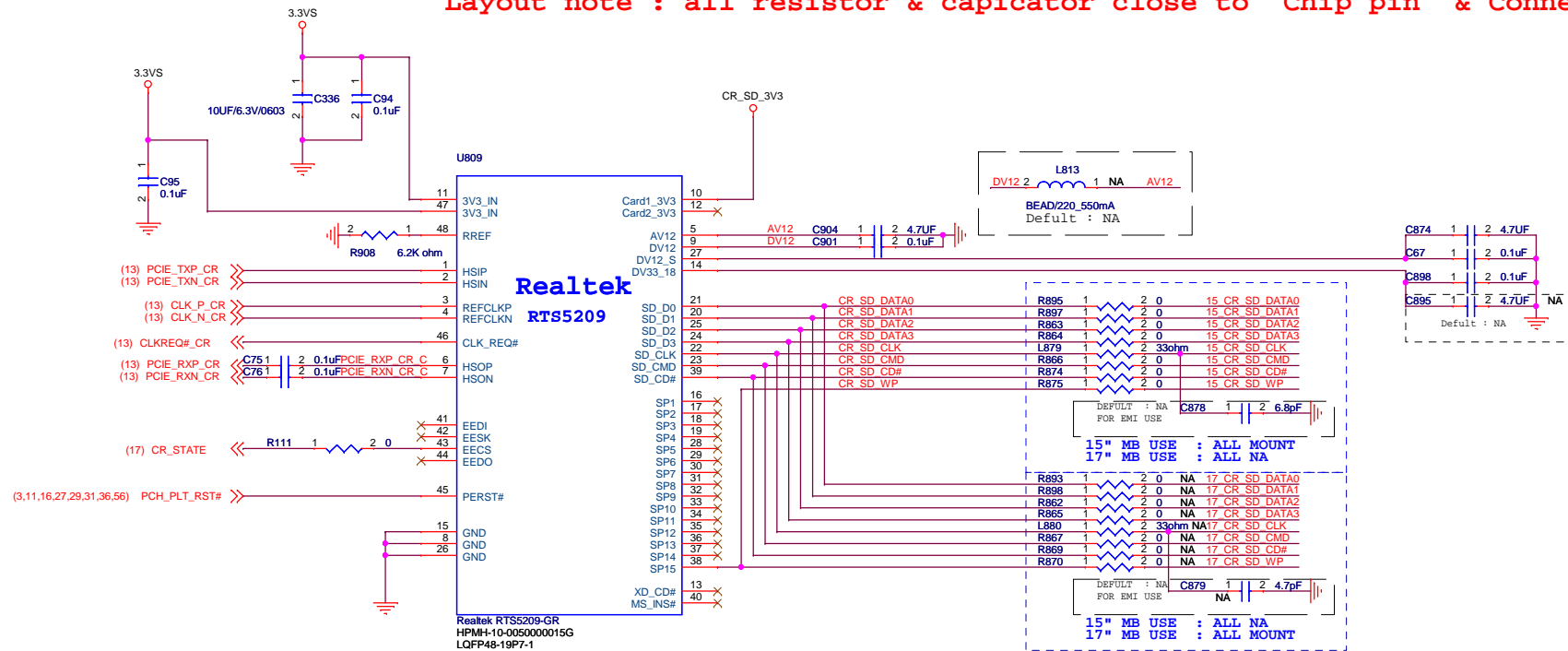
Project Name: H710DI1
Size: Document Number: HPMH-4
Date: Monday, November

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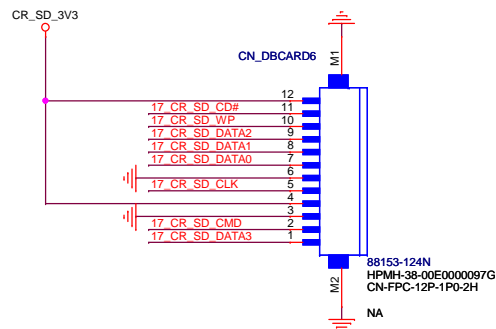
Card Reader

<http://laptopblue.vn/>

Layout note : all resistor & capicator close to Chip pin & Connector pin

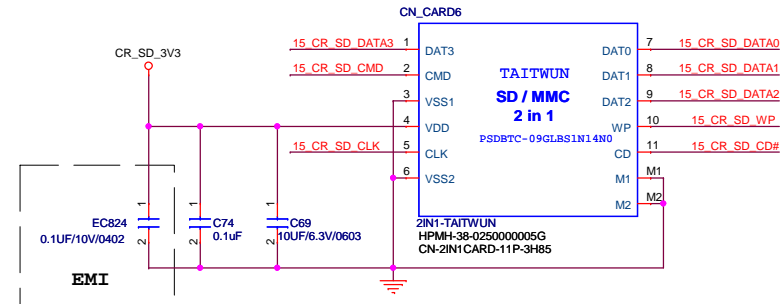


FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA
FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



FOR 15" MB ALL COMPONENT : MOUNT
FOR 17" MB ALL COMPONENT : NA

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Project Name : H710DI1
Title : Card Reader
Size :
Document Number : HPMH-40GAB660
Date : Monday, November 08, 2010

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www.qdzbxw.com

<http://laptopblue.vn/>

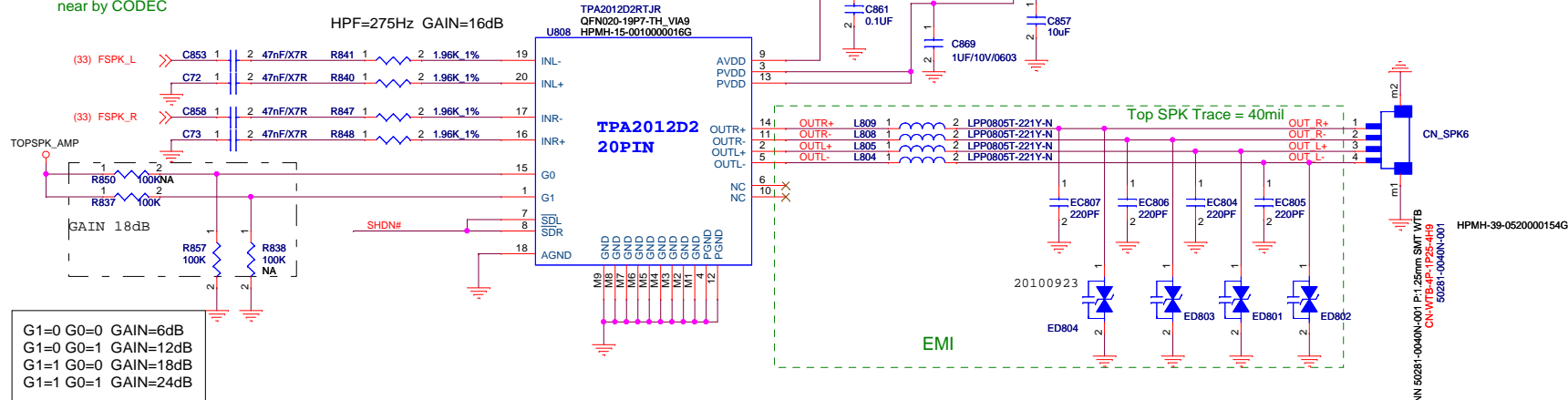
FLEX Computing	
Project Name : H710DI1	Title : RESERVE
Size :	Document Number : HPMH-40GAB6600-B130
Date: Monday, November 08, 2010	

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Front Speaker AMP

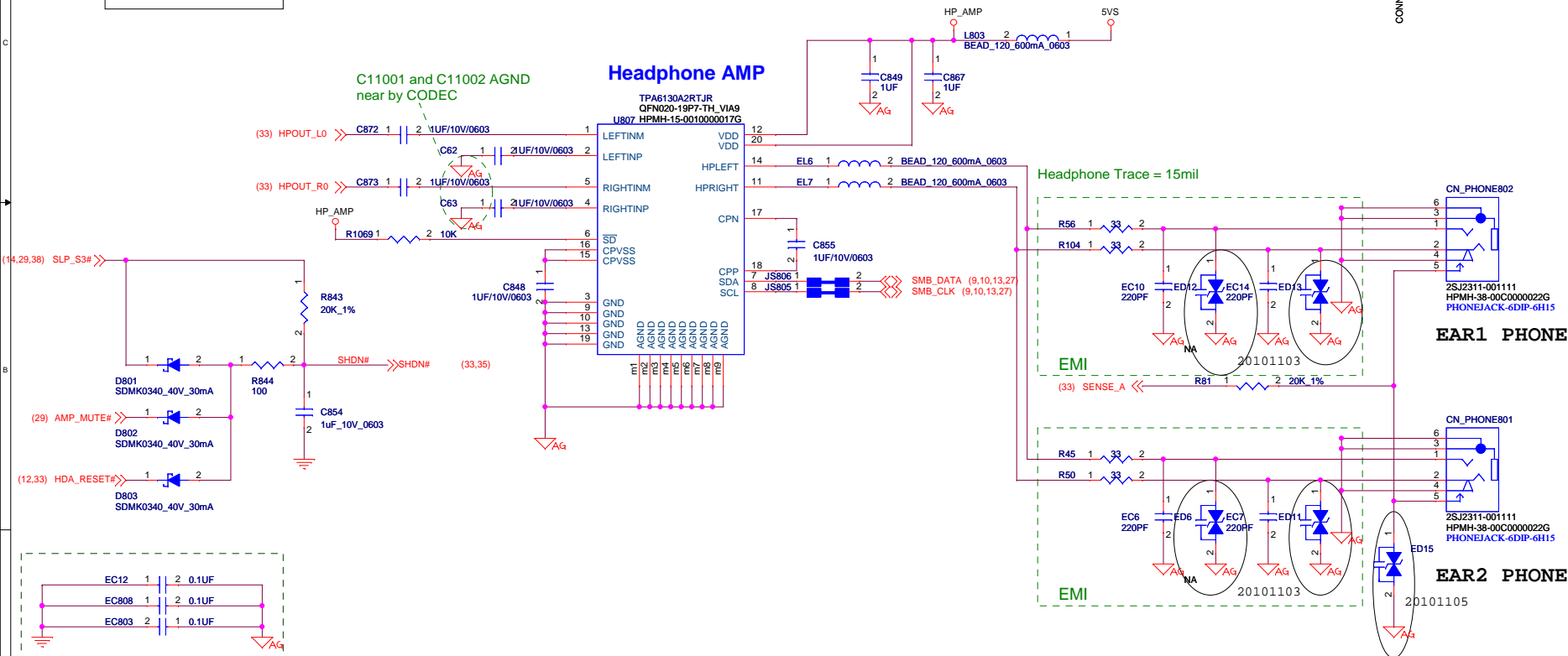
C9722 and C9725 GND near by CODEC

HPF=275Hz GAIN=16dB



Headphone AMP

C11001 and C11002 AGND near by CODEC



FLEX Computing

Project Name :	H710D11	Title :	Audio 2/3 SPK AMP
Size :	Document Number :	Rev :	B
Date :	Monday, November 08, 2010	Sheet :	34 of 6

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If without supply Woofer all page NA

WOOFER AMP

HPA00836PWPR
HTSSOP28-25P6X220-TH

HPA00836PWPR
28PIN

C9742 GND
near by CODEC

GAIN 20dB

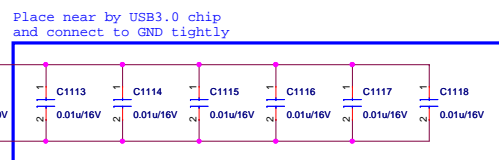
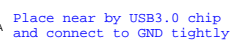
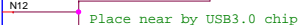
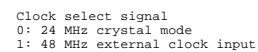
G1=0 G0=0 GAIN=20dB
G1=0 G0=1 GAIN=26dB
G1=1 G0=0 GAIN=32dB
G1=1 G0=1 GAIN=36dB

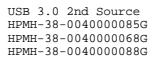
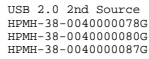
Kevin modify-0909

FLEX Computing

Project Name : H710DI1		Title : Audio 3/3 WOOFER AMP	
Size :	Document Number :	HPMH-40GAB6600-B130	
Date : Monday, November 08, 2010	Sheet : 35	of 63	

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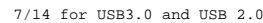
500mW / 3.3V
(0.151Amp)



593mW / 1.05V
(0.72Amp)



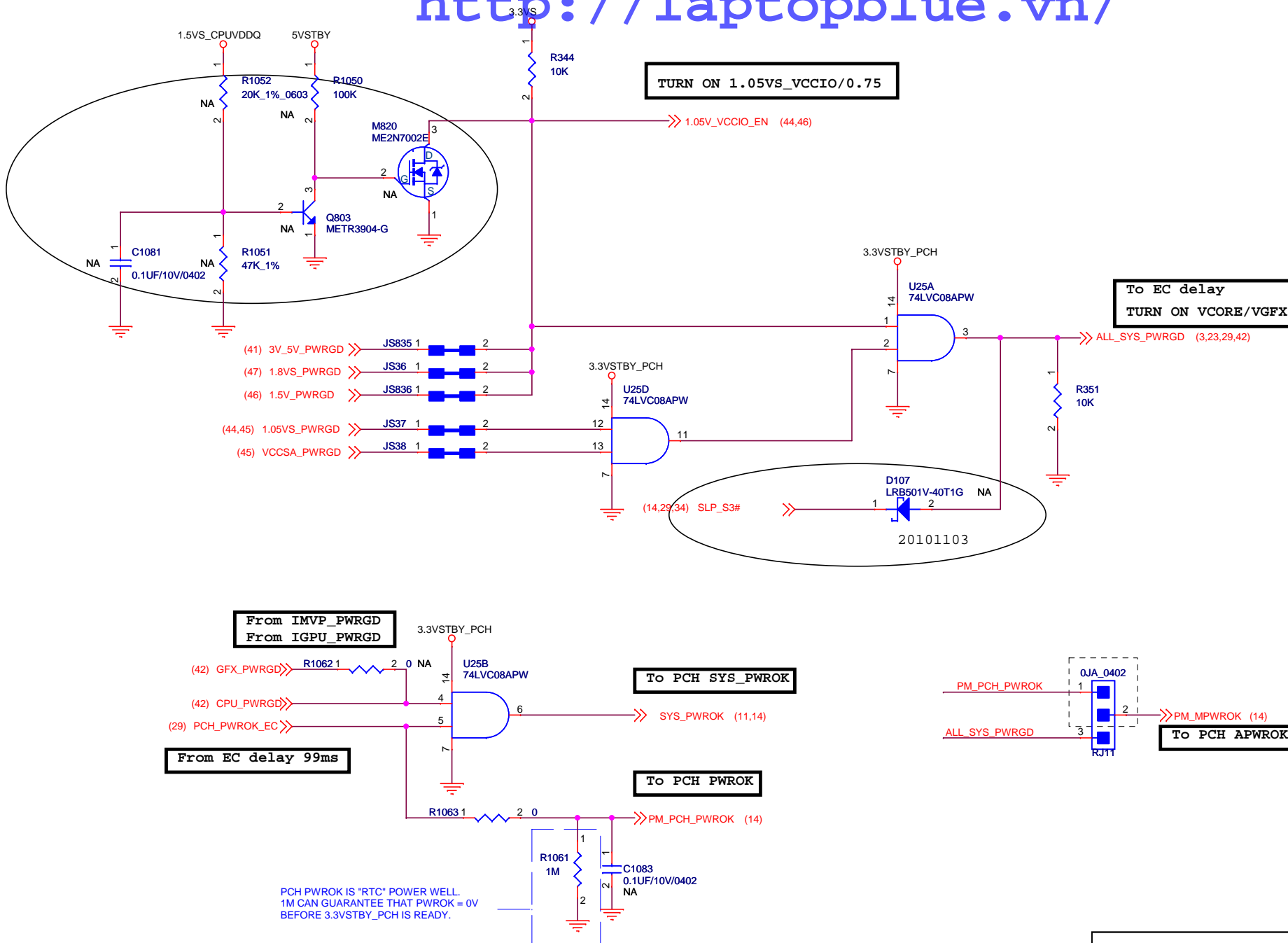
USB POWER SW



7/14 for USB3.0 (A) and USB 2.0 (B)

Project Name : H710DI1		Title : USB30_CNN/PV
Size :	Document Number : HPMH-40GAB6600-B130	
Date: Monday, November 08, 2010		S

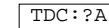
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FLEXComputing

Project Name : H710D11		Title : POWER
Size : Custom	Document Number : HPMH-40GAB6	
Date: Monday, November 08, 2010		

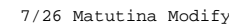
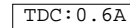
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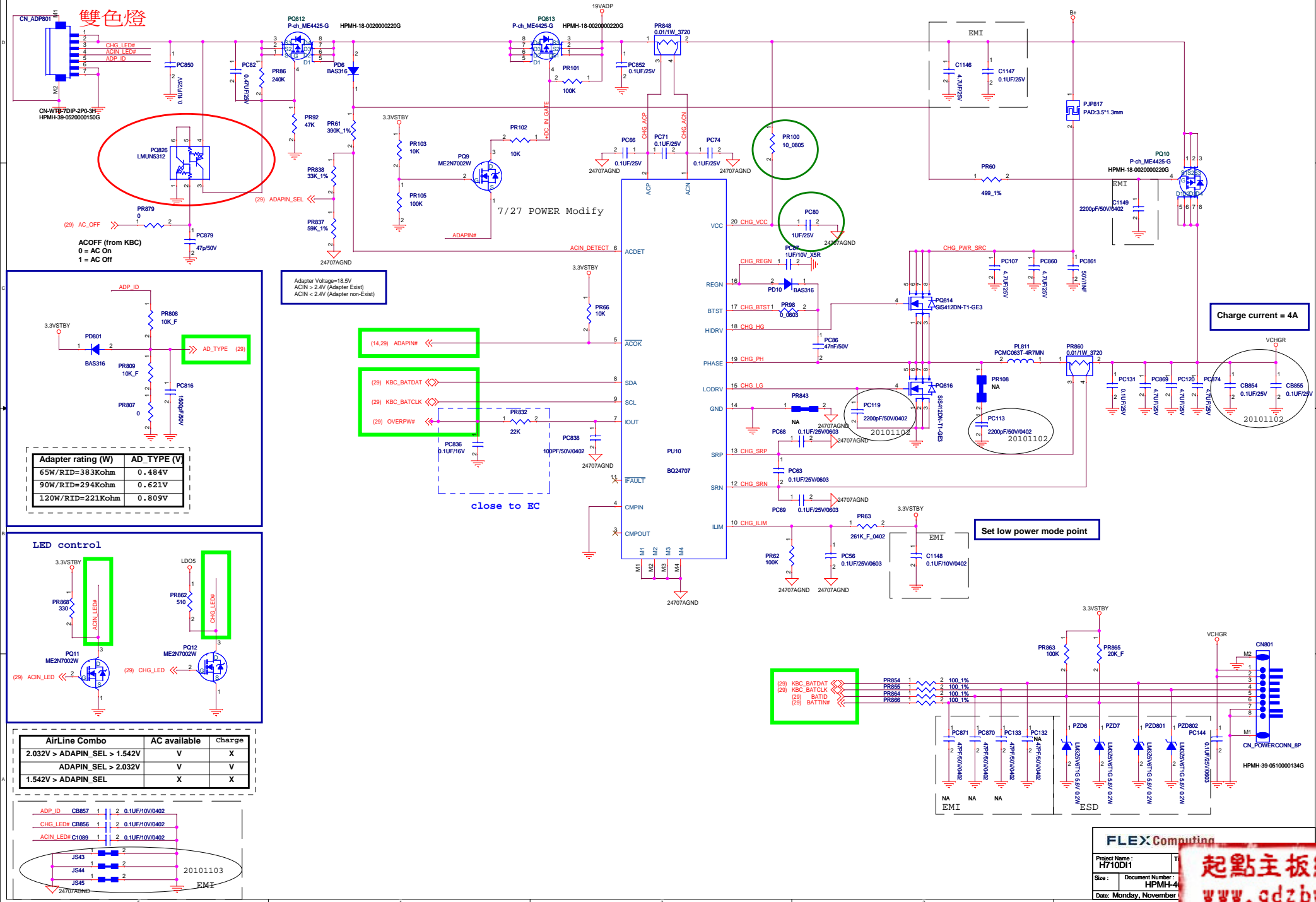
TDC: 5A



500mW / 3.3V



Vgs(th) : -0.9V(max)
Rds(on) : 75m@Vgs = -4.5V(MAX)
Id : -2.8A(Max)



5V / 3.3VSTBY

<http://laptopblue.vn/>

Freq=300KHz
TDC = 7 A
OCP = 10 A

* Options 1.
5VSTBY

* Options 2.

* Options 3.

* Options 4.

* Options 5.

* Options 6.

* Options 7.

* Options 8.

* Options 9.

* Options 10.

* Options 11.

* Options 12.

* Options 13.

* Options 14.

* Options 15.

* Options 16.

* Options 17.

* Options 18.

Freq=375KHz
TDC = 4 A
OCP = 5.7 A

INTEL HR / AMD DANUBE
Options 1 - 5VSTBY / 5V
Options 2 - 5VALW_ON / SUS_ON
Options 3 - 3V_5V_PWRGD / 3.3V_5V_PWRGD
Options 4 - 15V_ALW / 15VSTBY
Options 5 - 5VSTBY / 5V

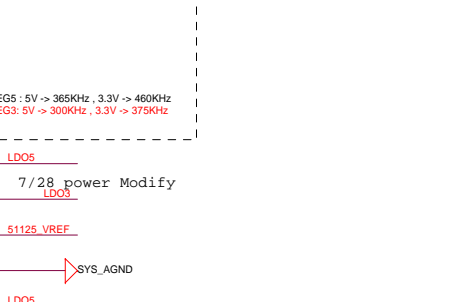
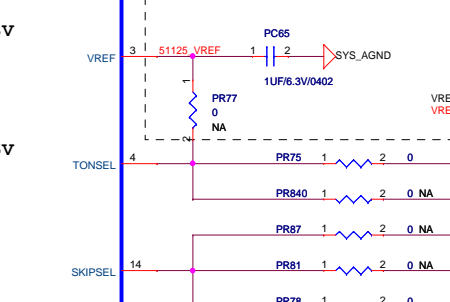
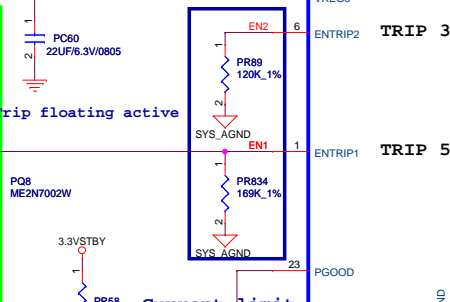
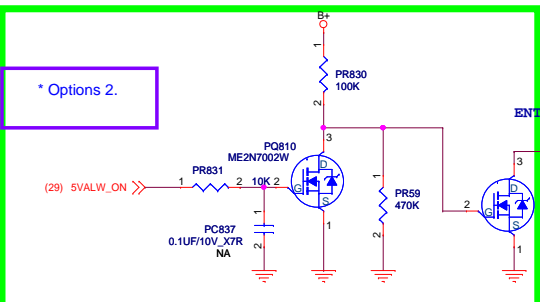
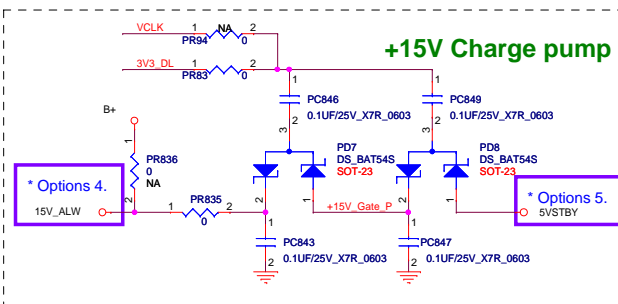


Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	Off



FLEX Computing

Project Name: H710D11 Title: 5VSTBY_3VSTBY(TPSS)

Size: Document Number: HPMH-40GAB6600-B130

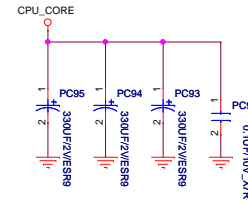
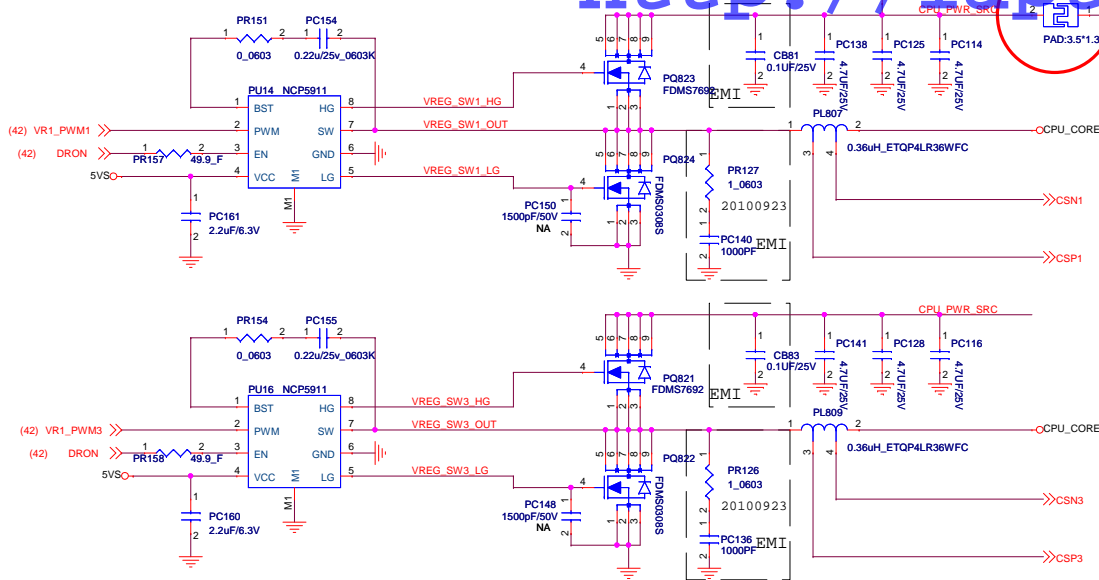
Custom Date: Monday, November 08, 2010 Sheet: 41

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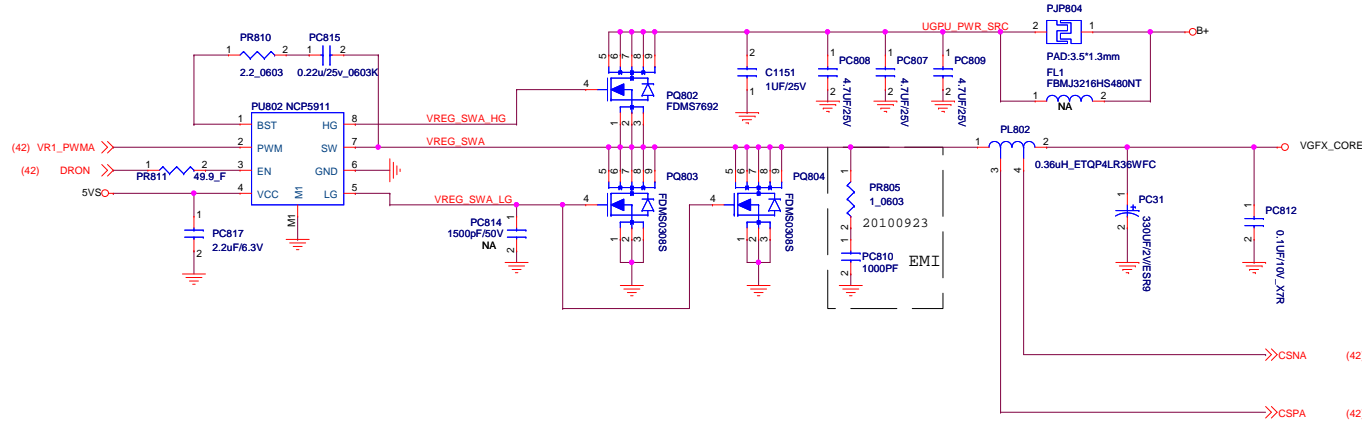
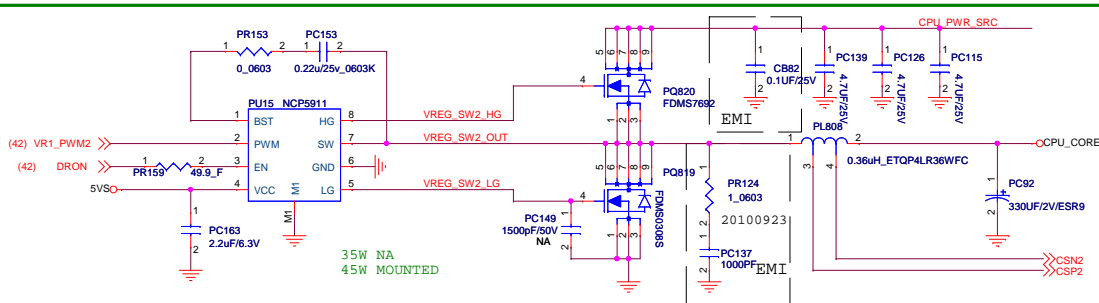


FLEX Computing

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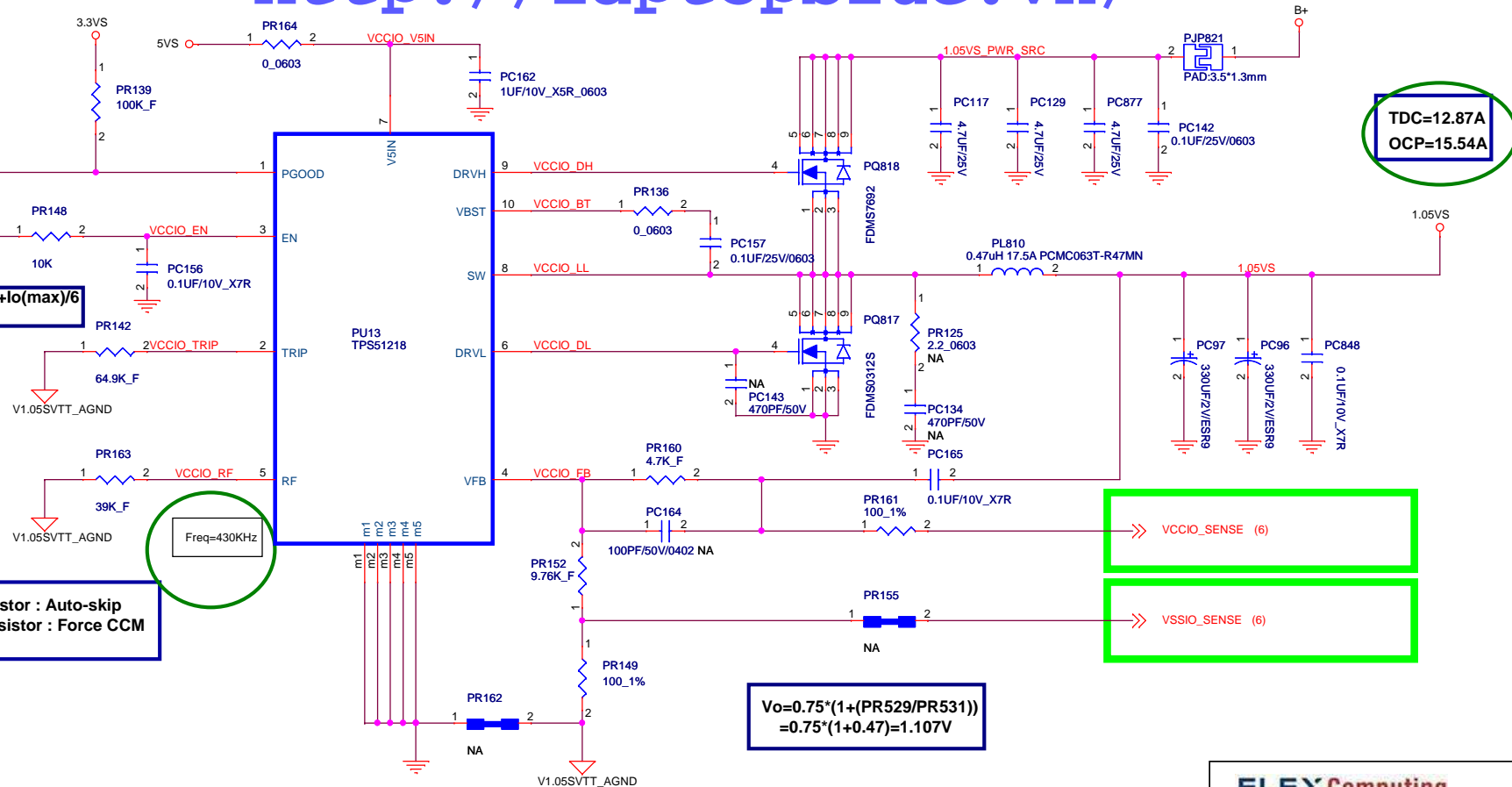


Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PU15	NCP5911	NA	
PR153	0_0603_5%	NA	
PC153	0.22UF_25V_0603	NA	
PR159	49.9_0402_1%	NA	
PC163	2.2UF_6.3V_0603	NA	
PQ820	FDMS7692	NA	
PQ819	FDMS0308S	NA	
PL808	0.36uH	NA	
PR874	73.2K_0402_1%	41.2K_0402_1%	HPMH-30-141221-990G
PR861	24K_0402_1%	24.9K_0402_1%	HPMH-30-124921-990G
PR867	21K_0402_1%	12.4K_0402_1%	HPMH-30-112421-990G



1.05VS_VCCIO
1.05VS

<http://laptopblue.vn/>

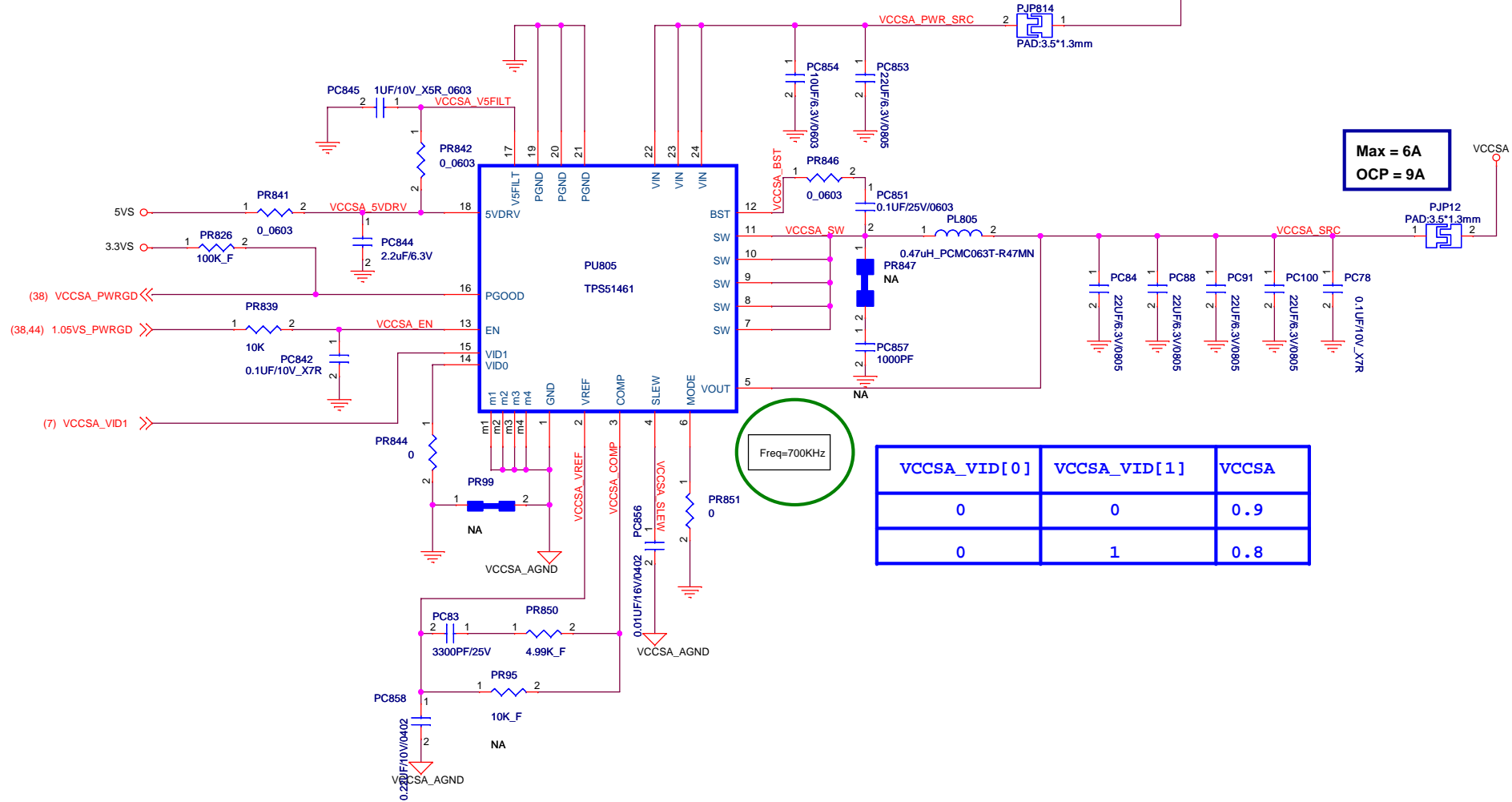


RF pull down to GND with resistor : Auto-skip
RF connect to PGOOD with resistor : Force CCM

$$V_o = 0.75 * (1 + (PR529 / PR531)) \\ = 0.75 * (1 + 0.47) = 1.107V$$

FLEX Computing

Project Name : H710DI1		Title : 1.05VS(TPS51218)	
Size : Custom	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet: 44 of 63	



Max = 6A
OCP = 9A

Freq=700KHz

VCCSA_VID[0]	VCCSA_VID[1]	VCCSA
0	0	0.9
0	1	0.8

FLEXComputing

Project Name :
H710D11

Title :
ITE8509E/ 1.1VS

Size :
B

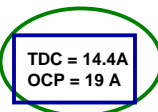
Document Number :
HPMH-40GAB6600-B130

Rev :
B

Date: Monday, November 08, 2010

Sheet : 45 of 63

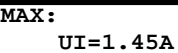
<http://laptopblue.vn/>



STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

Options 1 - INTEL HR / AMD DANUBE
Options 2 - 3.3VSTBY / 3.3V
Options 3 - RUN_ON / SUS_ON
Options 4 - DDR_VTTR / V_DDR_VTT
Options 5 - 5VSTBY / 5V
Options 6 - 0.75VS_DDR_VTT / 0.75V_DDR_VTT


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1.8VS for CPU & PCH

$$V_{out} = 0.8 * (R1 + R2) / R2$$

SOP8-50X236-TH
IC G9661-25ADJF11U LDO REGULAT SOP8
7/20 change LDO IC / wait for PN by wayler

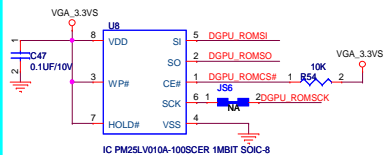
			
Project Name : H710DI1		Title : 1.8VS	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 47 of 63	



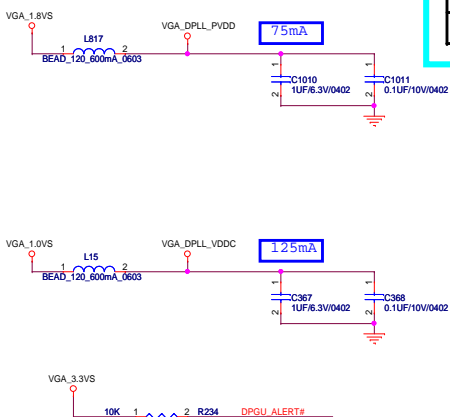
FLEX Computing		
Project Name : H710DI1	Title : Capilano_1/5_PCIE/LVDS	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Mon	02/08/2016	15:00

For del vBIOS ROM design:
1.P49 -U8,C47,R54
2.P53 -R1001,R1002,R1015

For GDDR5 used



NA for del vBIOS ROM design.

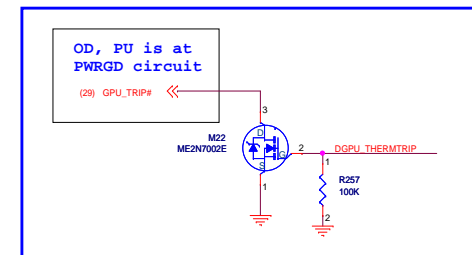
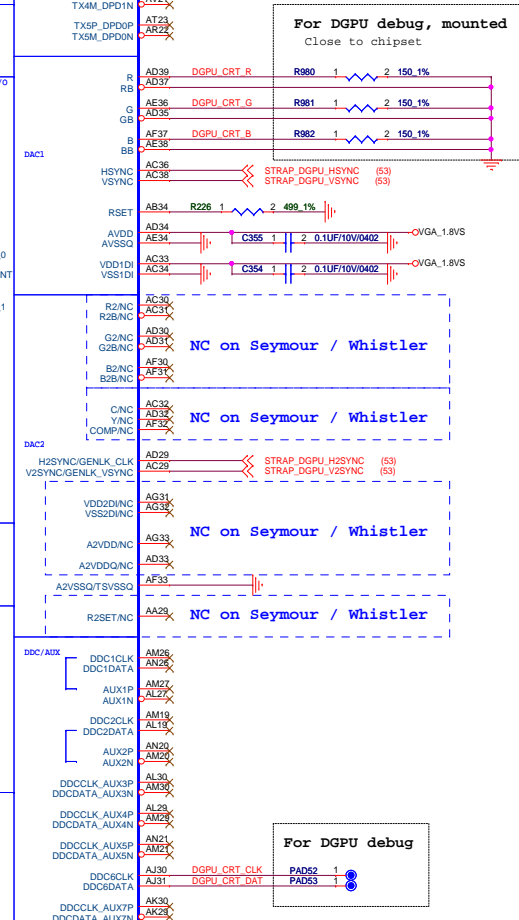
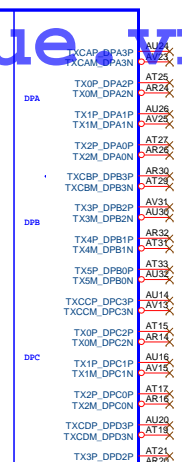
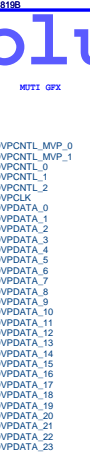
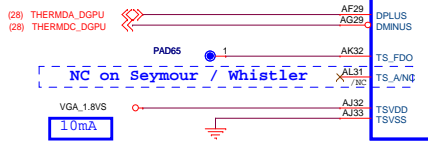
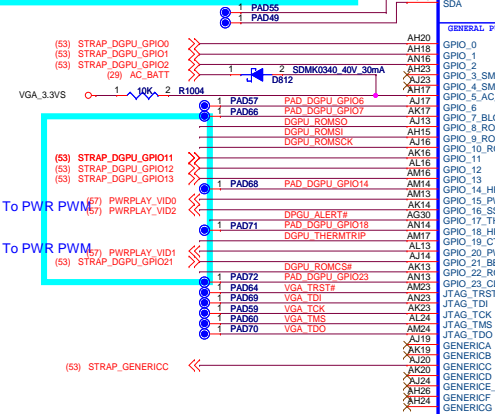
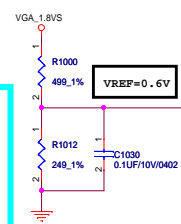
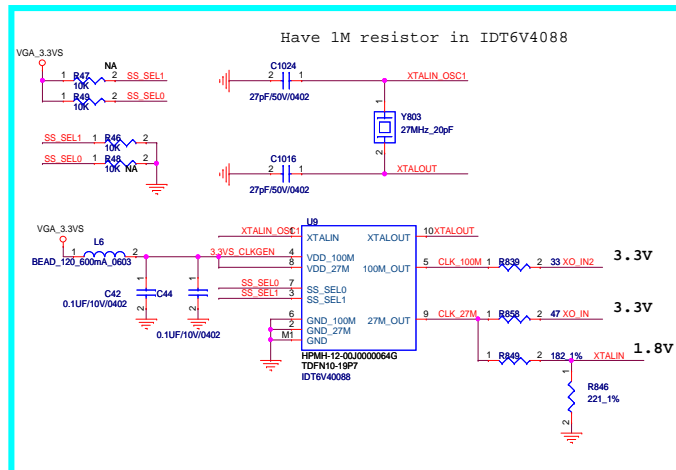


VMEM ID

	DVPDATA_2	DVPDATA_1	DVPDATA_0
Seymour Hynix H5GQ2H24MFR-T2C (128Mx16) x4pcs	0	0	0
Seymour Samsung K4G20325FC-HC04 (128Mx16) x4pcs	0	0	1
Whistler Hynix H5GQ1H24AFR-T2C (64Mx16) x8pcs	0	1	0
Whistler Samsung K4G10325FE-HC04 (64Mx16) x8pcs	0	1	1
Seymour Hynix H5GQ1H24AFR-T2C (64Mx16) x4pcs	1	0	0
Seymour Samsung K4G10325FE-HC04 (64Mx16) x4pcs	1	0	1
Seymour Elpida EDW2032BABG-50-F(128Mx16) x4pcs	1	0	1
Whistler Elpida EDW1032BABG-50-F(64Mx16) x8pcs	1	1	1

100 MHz Spread Selection Table

PIN3	PIN7	PIN5	
S1	S0	Down	Spread%
L	L	OFF	
L	M	-0.5	
L	H	-2.5	
M	L	-0.25	
M	M	-0.75	
M	H	-1.0	
H	L	-1.5	
H	M	-2.0	Default
H	H	-3.0	



For DGPU debug, mounted
Close to chipset

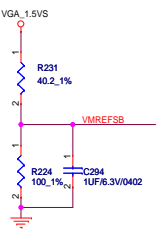
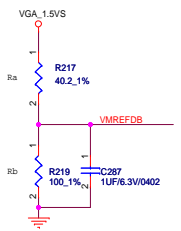
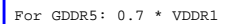
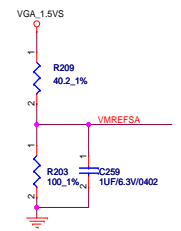
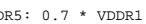
NC on Seymour / Whistler

NC on Seymour / Whistler

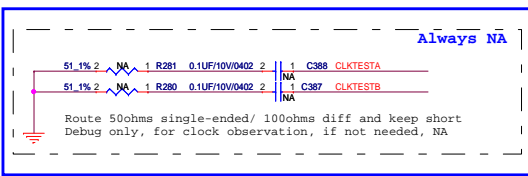
33 NC on Seymour / Whistler

29 NC on Seymour / Whistler

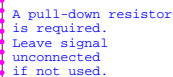
For DGPU debug



VRAM TYPE		PN
Hynix H5GQ1H24AFR-T2C	64MX16(32MX32)	HPMH-14-00300000001G
Hynix H5GQ2H24MFR-T2C	128MX16(64MX32)	HPMH-14-00300000002G
SAMSUNG K4G10325FE-HC04	64MX16(32MX32)	HPMH-14-00300000003G
SAMSUNG K4G20325FC-HC04	128MX16(64MX32)	HPMH-14-00300000004G
Elpida EDW1032BABG-50-F	64MX16(32MX32)	HPMH-14-00300000005G
Elpida EDW2032BABG-50-F	128MX16(64MX32)	HPMH-14-00300000006G



U8195



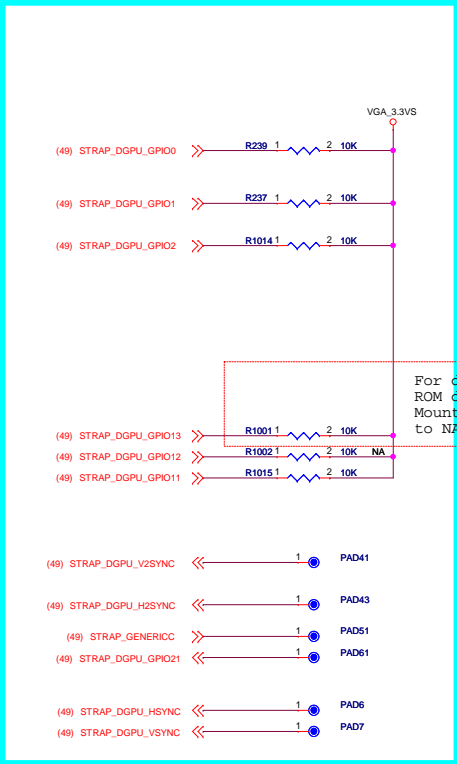
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Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33 AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK: (3.3V) Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V) Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

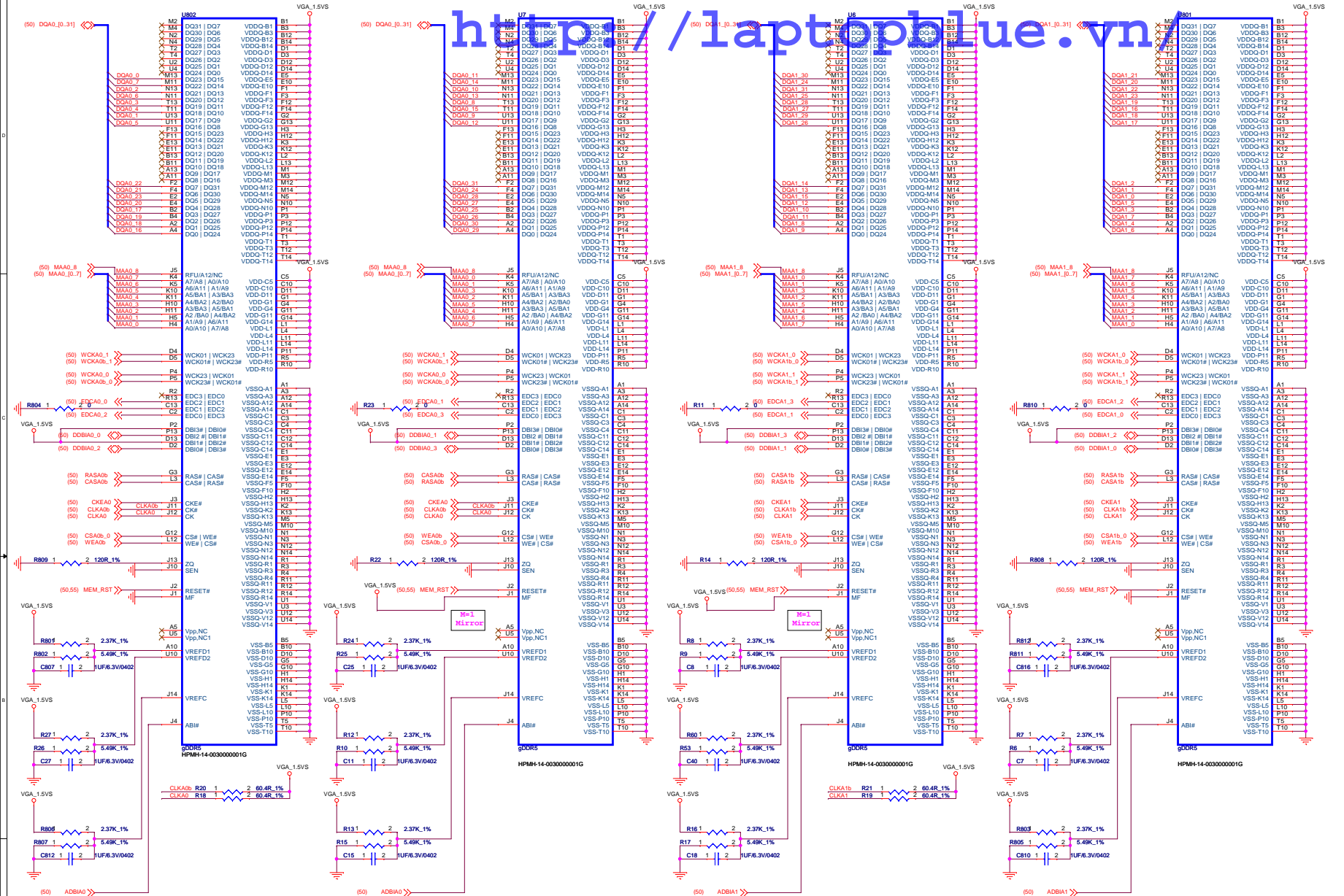
Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AJ21 on M2 Ball AG13 on S3	<p>SWAPLOCKA SwaplockA/B signals can be optionally used</p> <p>on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/right stereo timing.</p> <p>Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred but not required. SwaplockA/B are open drain, 3.3V signals.</p> <p>If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.</p>	<p>Ball AJ21 is NC on M2 packages</p> <p>Ball AG13 is R2SET on S3 package</p>
Ball AK21 on M2 Ball H12 on S3	<p>SWAPLOCKB - see above</p> <p>On a multi-gpu design, SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms).</p> <p>If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.</p>	<p>Ball AK21 is NC on M2 packages</p> <p>Ball AH12 is DAC2 Output- on S3 package</p>

CONFIGURATION STRAPS				
STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPI00	Transmitter (Tx) power savings enable. 0: 50% Tx output swing 1: Full Tx output swing (DEFAULT)	0 Internal Pull Down	Mounted
TX_DEEMPH_EN	GPI01	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (DEFAULT)		Mounted
RESERVED	GPI02	0 : PCIe device as 2.5 GT/s capable 1 : PCIe device as 5.0 GT/s capable (DEFAULT)		Mounted
VGA_DIS	GPI09	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0 - VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA NA
BIOS_ROM_EN	GPI0_22_ROMCSB	Enable the external BIOS ROM device: 0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		Mounted
CONFIG[2] CONFIG[1] CONFIG[0]	GPI013 GPI012 GPI011	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 (DEFAULT) 64 MB 010 32 MB 011		Mounted NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RESERVED RESERVED RESERVED RESERVED	H2SYNC GENERICC GPI06 GPI021_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function (DEFAULT) 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI if dongle is detected 1 1 Audio for both DisplayPort and HDMI		NA NA

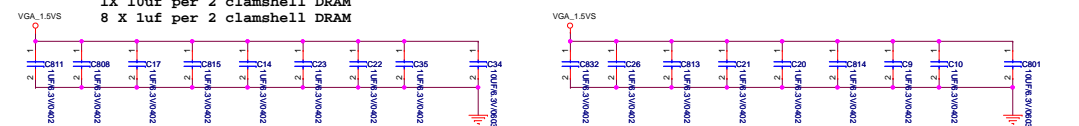


```
GPIO 13,12,11 CONFIG[2:0]
=>101 for PM25LV010
```

FLEX Computing	
Project Name : M720D14	Title : Capitane STRAPS/ChieDi#
Size :	
Date :	



Decoupling caps for clamshell configuration:
1X 10uf per 2 clamshell DRAM
8 X 1uf per 2 clamshell DRAM



NA for Seymour

GDDR5 Memory Channel A X16 Mode

FLEX Computing			
Project Name: H710D11		Title: Capitan_VRAM GDDR5 64MX16 A	
Size:	Document Number: HPMH-40GAB6600-B130		Rev: B
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起點主板維修網
www.qdzbwx.com

<http://laptopblue.vn/>

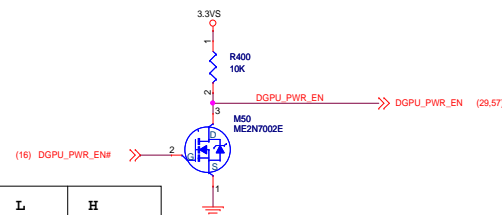
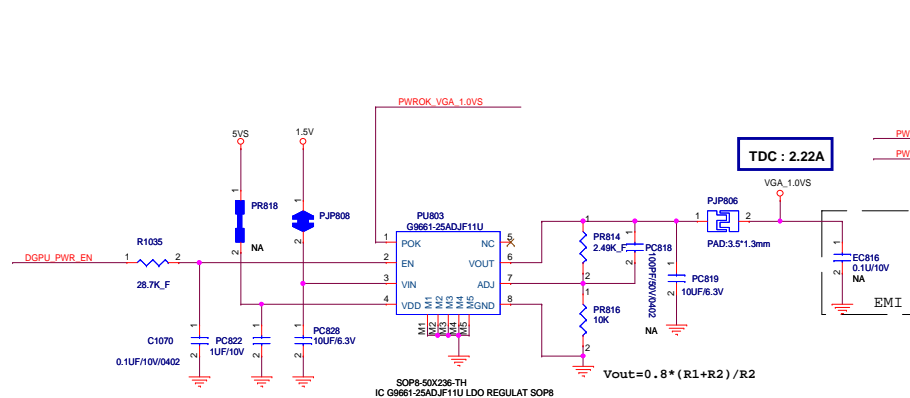
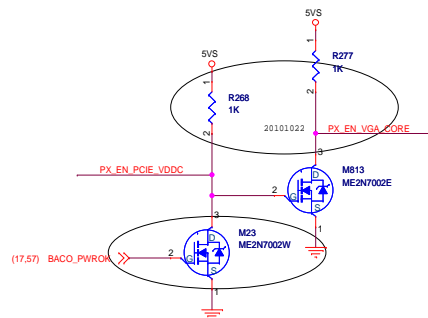


Diagram of the UI NA DI Mount (B) connector. The connector has three pins labeled 1, 2, and 3. Pin 1 is connected to PCH_PLT_RST# (3, 11, 16, 27, 29, 30, 31, 36). Pin 2 is connected to DGPU_PERST# (48). Pin 3 is connected to DGPU_HOLD_RST# (16). The connector is labeled RJB and 0JB.

	15W	15W
TDC	15A	35A
OCF	22.5A	50A

VID4 (PP2) (GPIO16)	VID3 (PP1) (GPIO20)	VID2 (PP0) (GPIO15)	VGA_CORE
0	0	1	1.05V
1	0	0	0.900V

VID							V _{DAC} (V)
6	5	4	3	2	1	0	
0	1	0	0	1	0	0	1.0500
0	1	1	0	0	0	0	0.9000

5VS PU maybe leakage in BACO. Change to VGA_3.3VS

VGA_CORE EN change R and C for power down

PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE

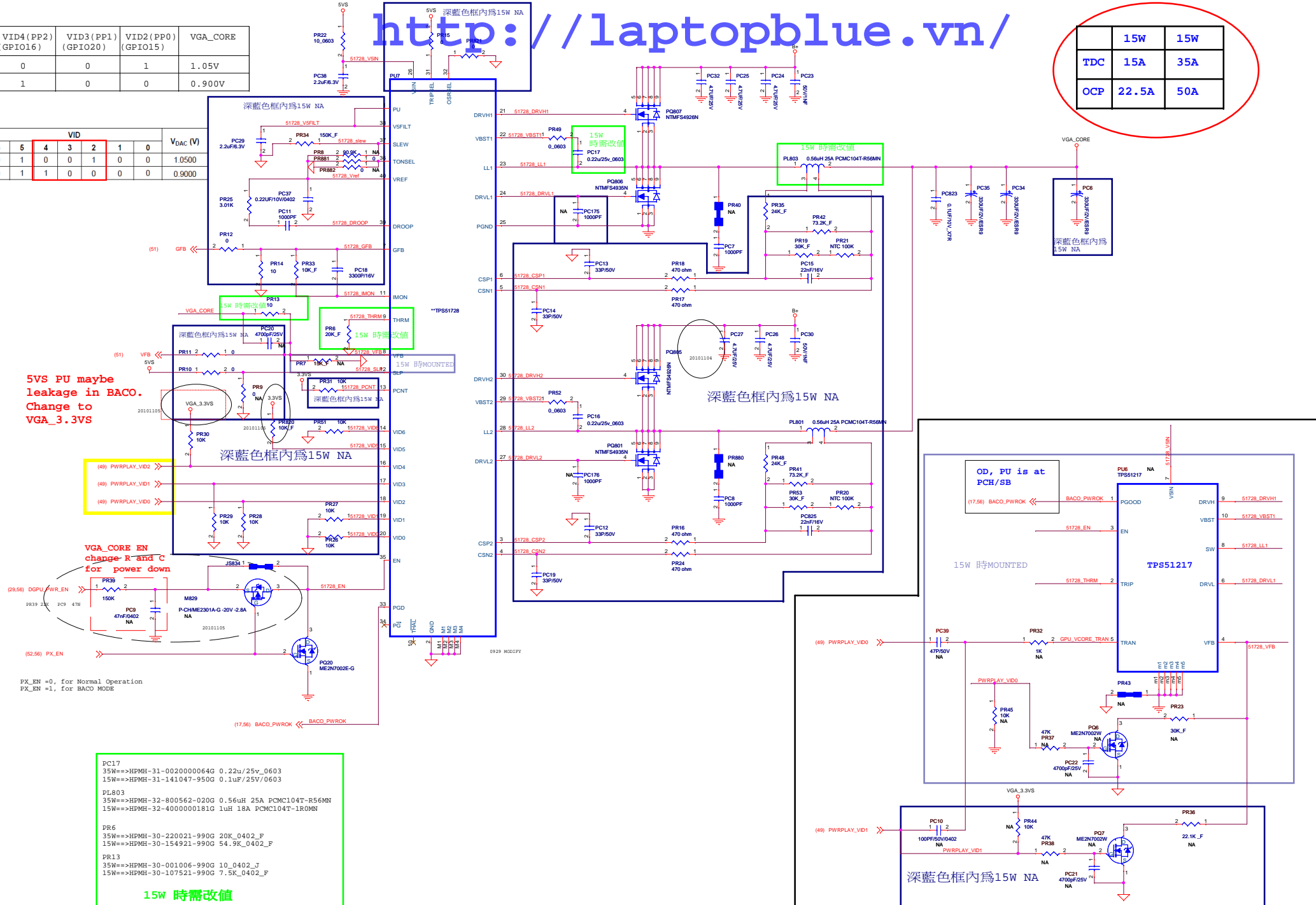
PC17
35W==>HIPMH-31-0020000064G 0.22u/25v_0603
15W==>HIPMH-31-141047-950G 0.1uF/25V/0603

PL803
35W==>HIPMH-32-800562-028Q 0.56uH 25A PCMC104T-R56MN
15W==>HIPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN

PR6
35W==>HIPMH-30-220021-990G 20K_0402_F
15W==>HIPMH-30-154921-990G 54.9K_0402_F

PR13
35W==>HIPMH-30-001006-990G 10_0402_J
15W==>HIPMH-30-107521-990G 7.5K_0402_F

15W 時需改值



Seymour GDDR5 (15W)

VID0	VGA_CORE
0	0.9
1	1.1

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Project Name: H710
Size: Custom
Date: Monday, 1

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FID9 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID802 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID11 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

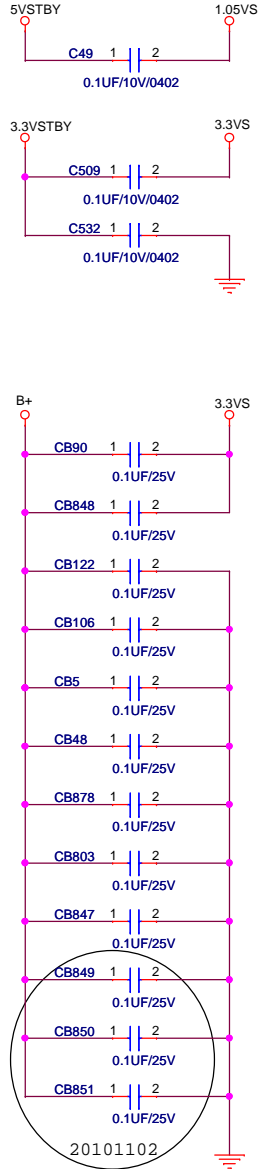
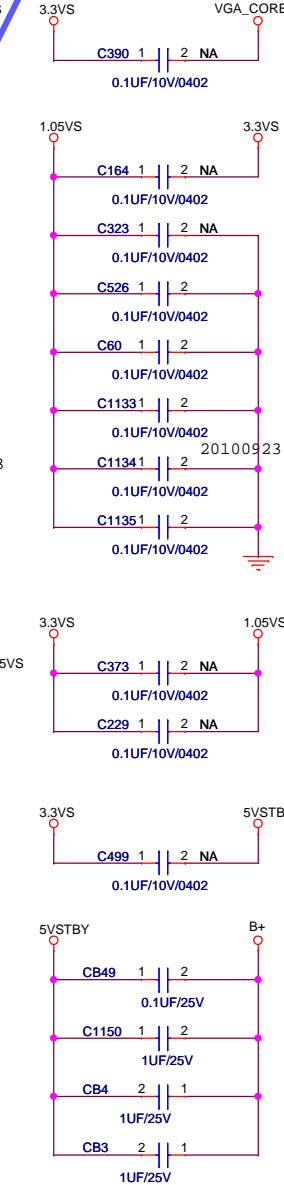
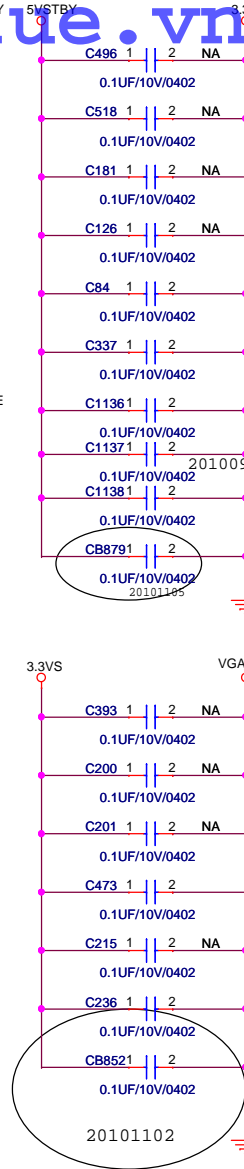
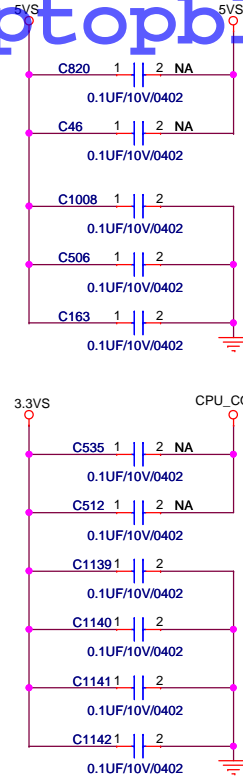
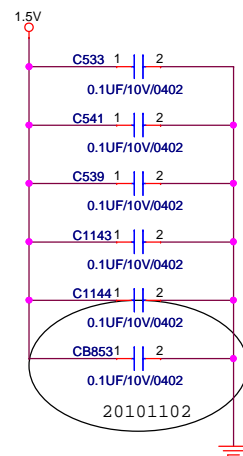
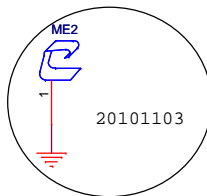
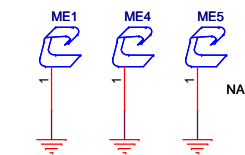
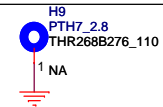
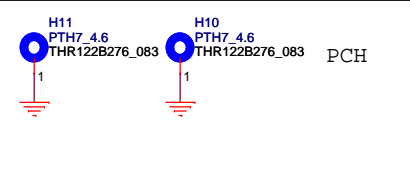
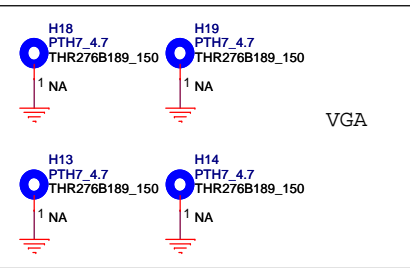
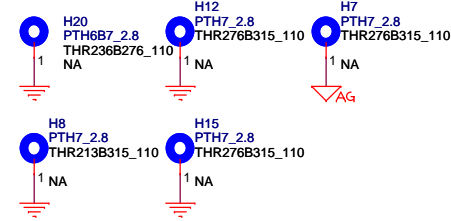
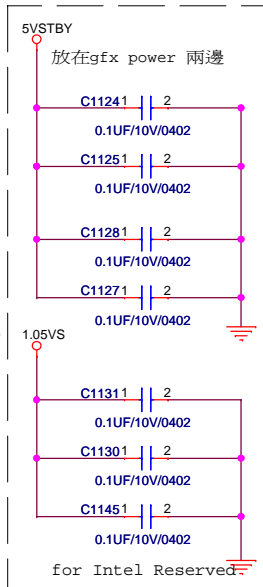
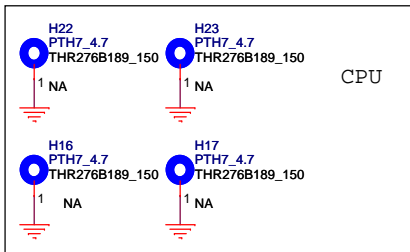
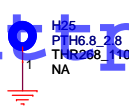
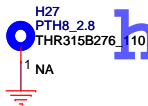
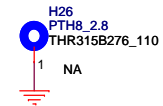
FID804 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID801 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID10 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID803 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID7 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

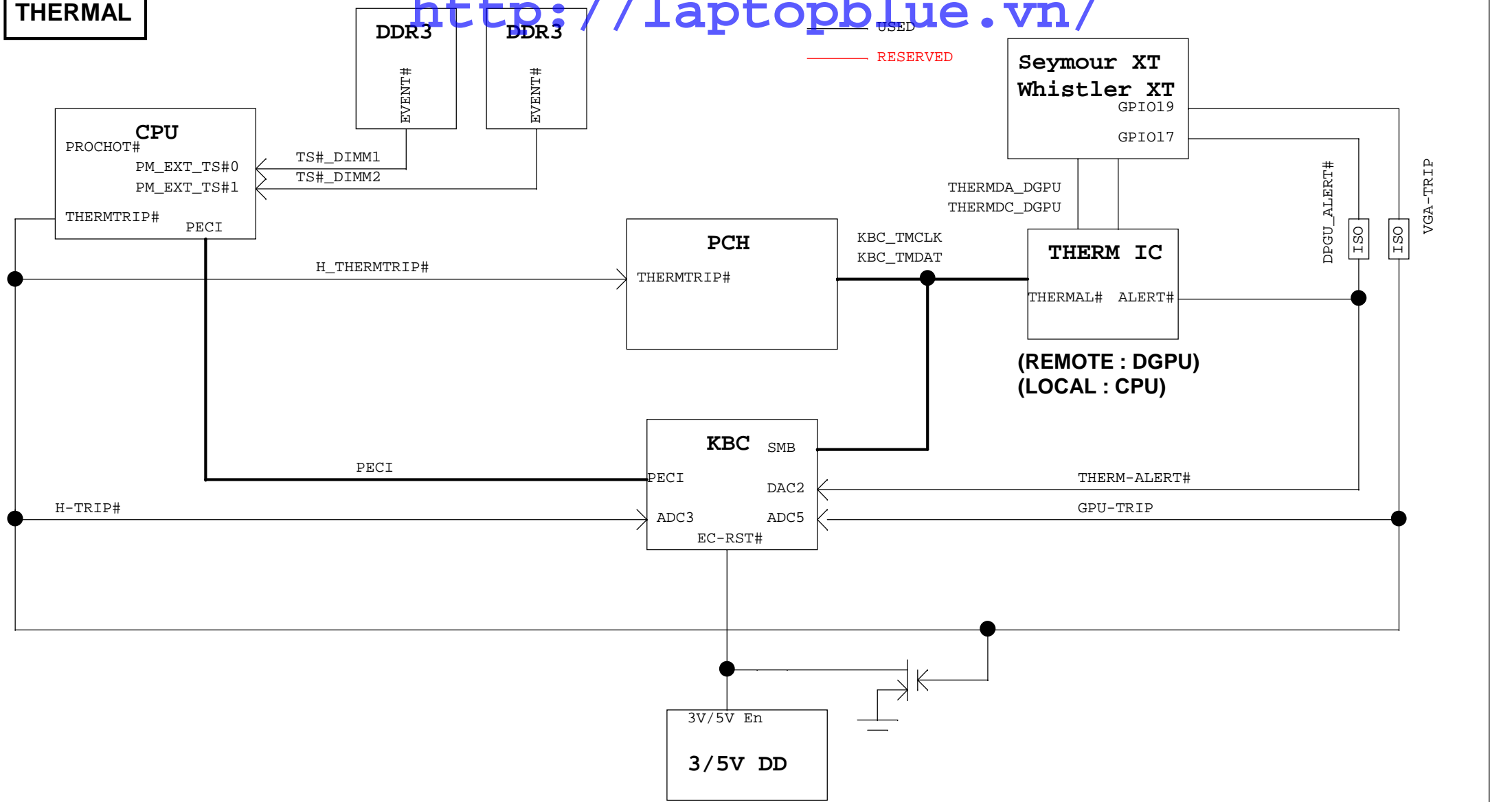


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Project Name : H710D11		Title : PAD_SCREW_ Moat Cap	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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THERMAL

<http://laptopblue.vn/>

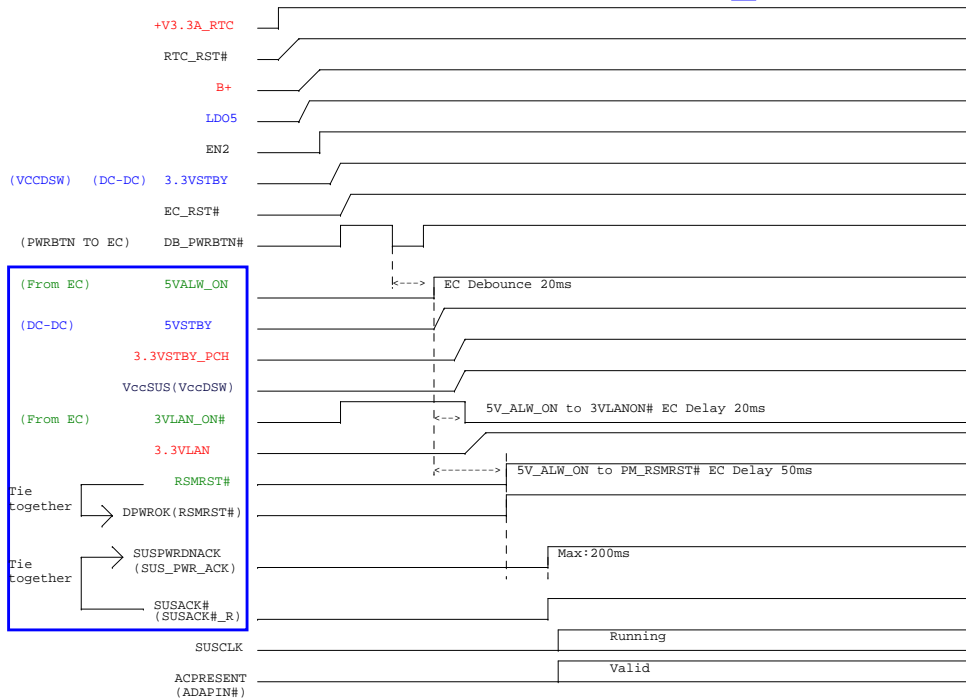


FLEX Computing			
Project Name : H710D11		Title : Thermal Policy	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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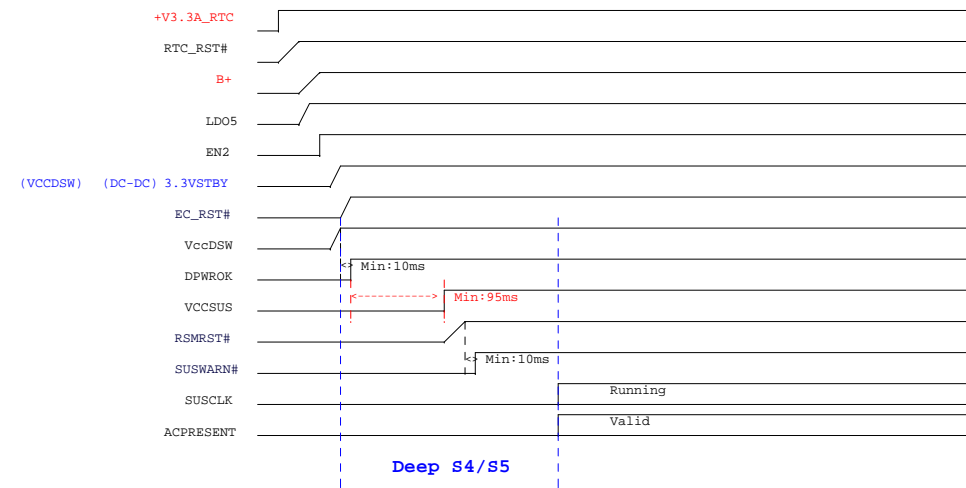
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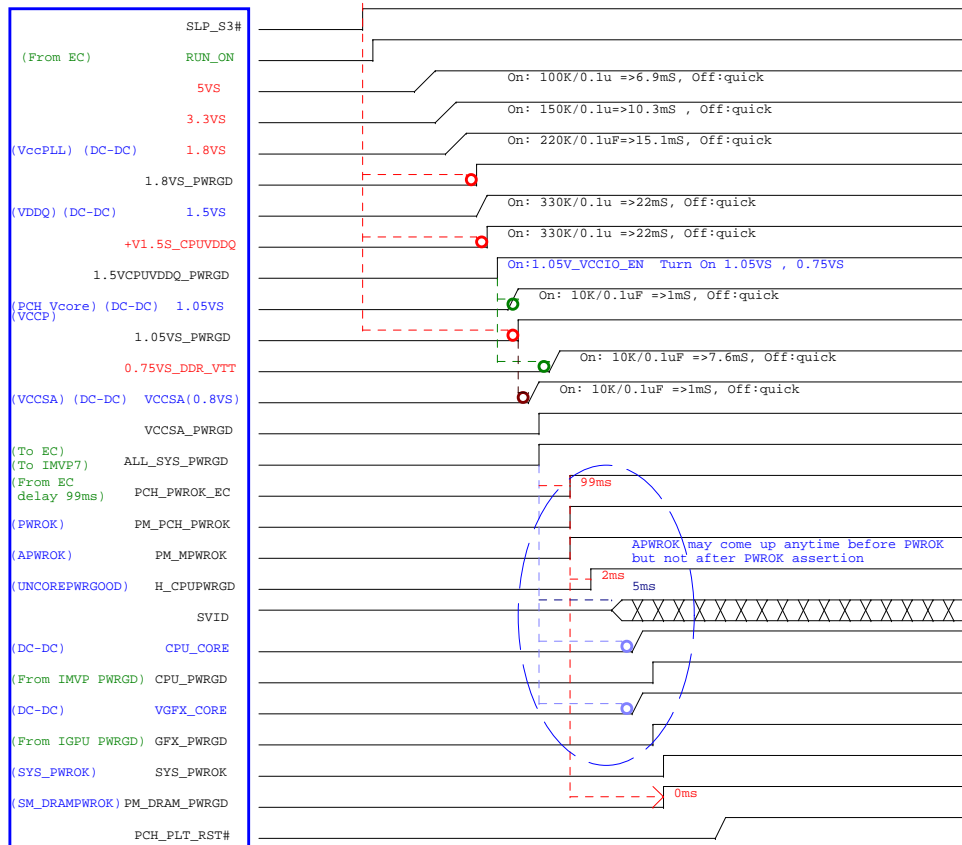
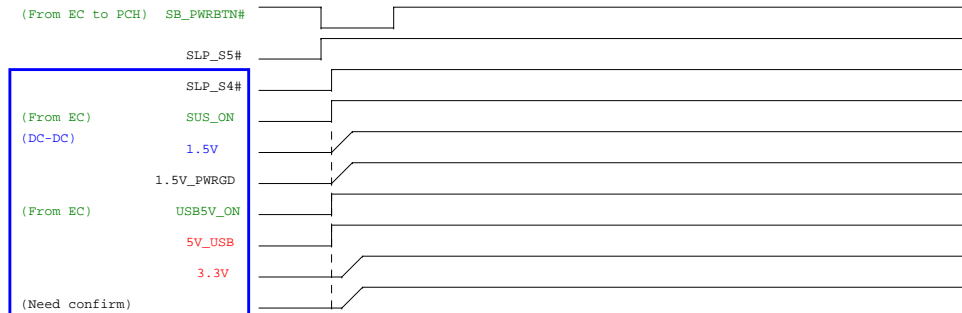
G3 to S0 (without Deep S4/S5) <http://laptopblue.vn/>



G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT

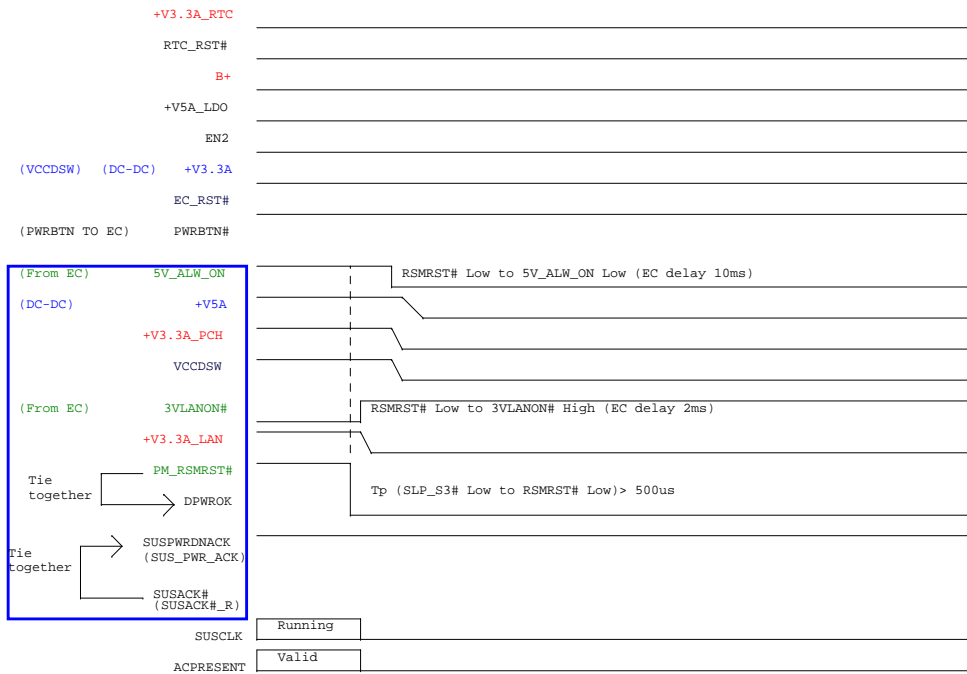


S5 to S0

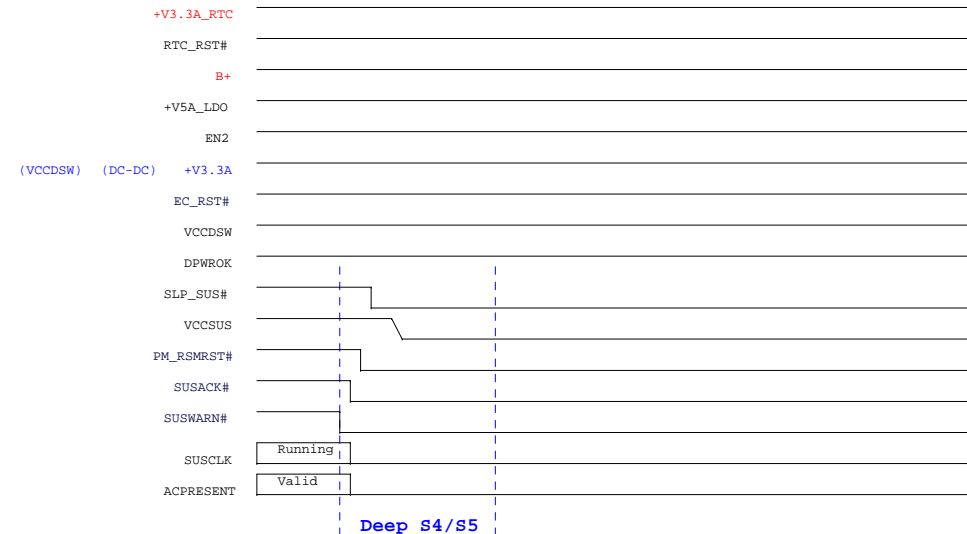


Blue: PWM
Green: EC
RED: MOSFET or Others

S0 to S5 (WoLAN Disable) (without Deep S4/S5)



S0 to S5 (support Deep S4/S5)



Blue: PWM
Green: EC
RED: MOSFET or Others

S0 to S4/S5

