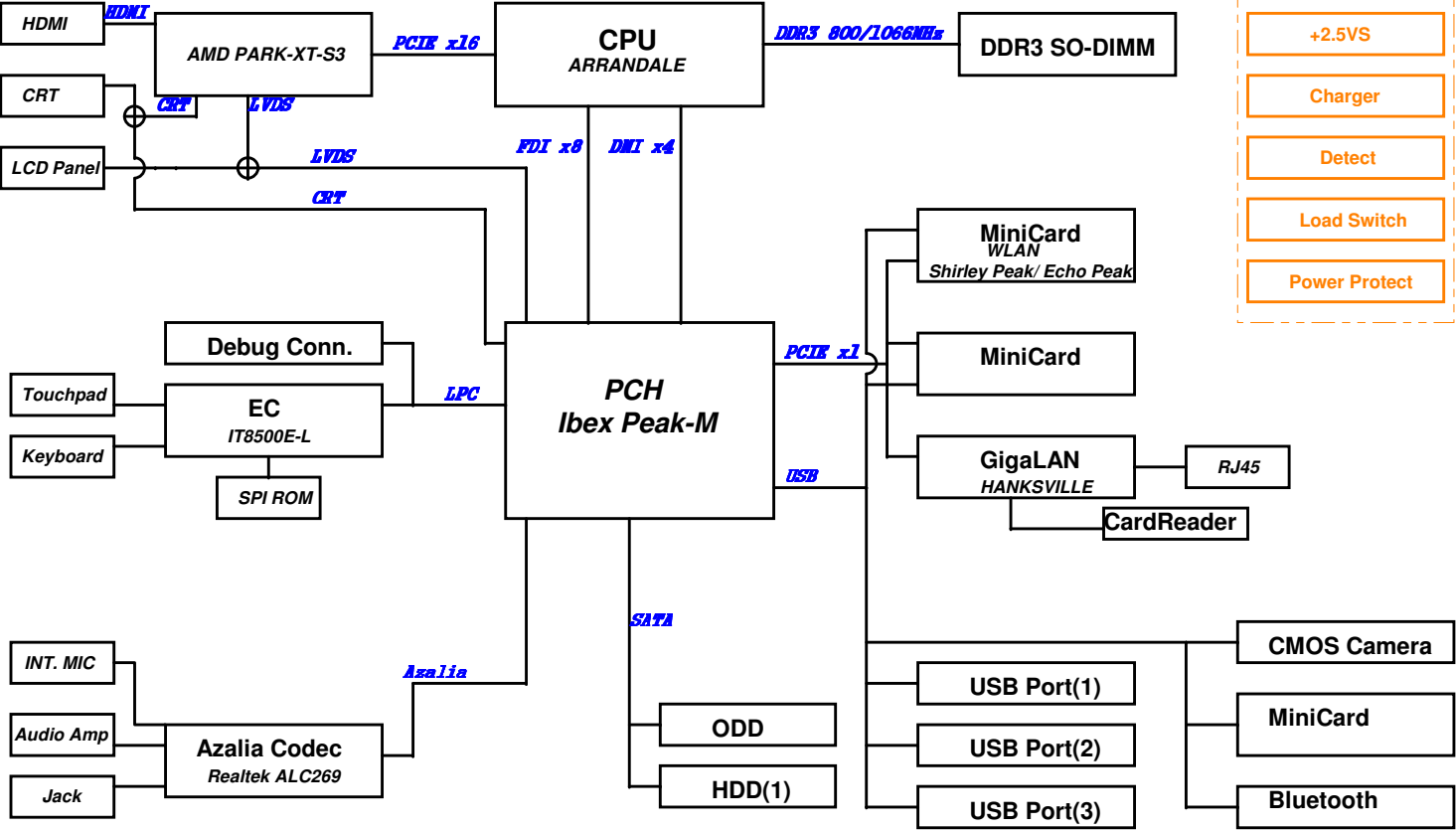


# K42Jr SCHEMATIC Revision 2.0

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## BLOCK DIAGRAM



Power

VCORE

System

1.5VS & 1.05VS

DDR & VTT

+2.5VS

Charger

Detect

Load Switch

Power Protect

Clock Generator  
ICS ICS9LPR427

VID controller

PWM Fan

Discharge Circuit

Reset Circuit

DC & BATT. Conn.

Skew Holes

PCH\_IBEX  
GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSENT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC

IT8512/

EC GPIO	Use As	Signal Name
GP0	O	PWR_LED#
GP1	O	CNC_LED#
GPA2	-	-
GPA3	-	-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	O	SUSC_EC#
GPB1	O	SUSB_EC#
GPB2	-	-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RC_IN#
GPB7	O	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	-	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	-	-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPFO	-	-
GPFI	-	-
GPF2	I	EXP_GATE#
GPF3	-	-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	-	-
GPFO	-	-
GPG1	I	PM_SUSB#
GPG2	-	-
GPG6	-	-
GPHO	IO	PM_CLKRUN#
GPH1	-	-
GPH2	O	GFX_VR_ON
GPH3	O	BAT_LEARN
GPH4	-	-
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0	-	-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6	-	-
GPI7	-	-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISSET_EC
GPJ4	O	TP_LED
GPJ5	-	-

EC

IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	O	ME_PWROK
GPIO13	-	-
GPIO14	O	ME_SLP_M_EC#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
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GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

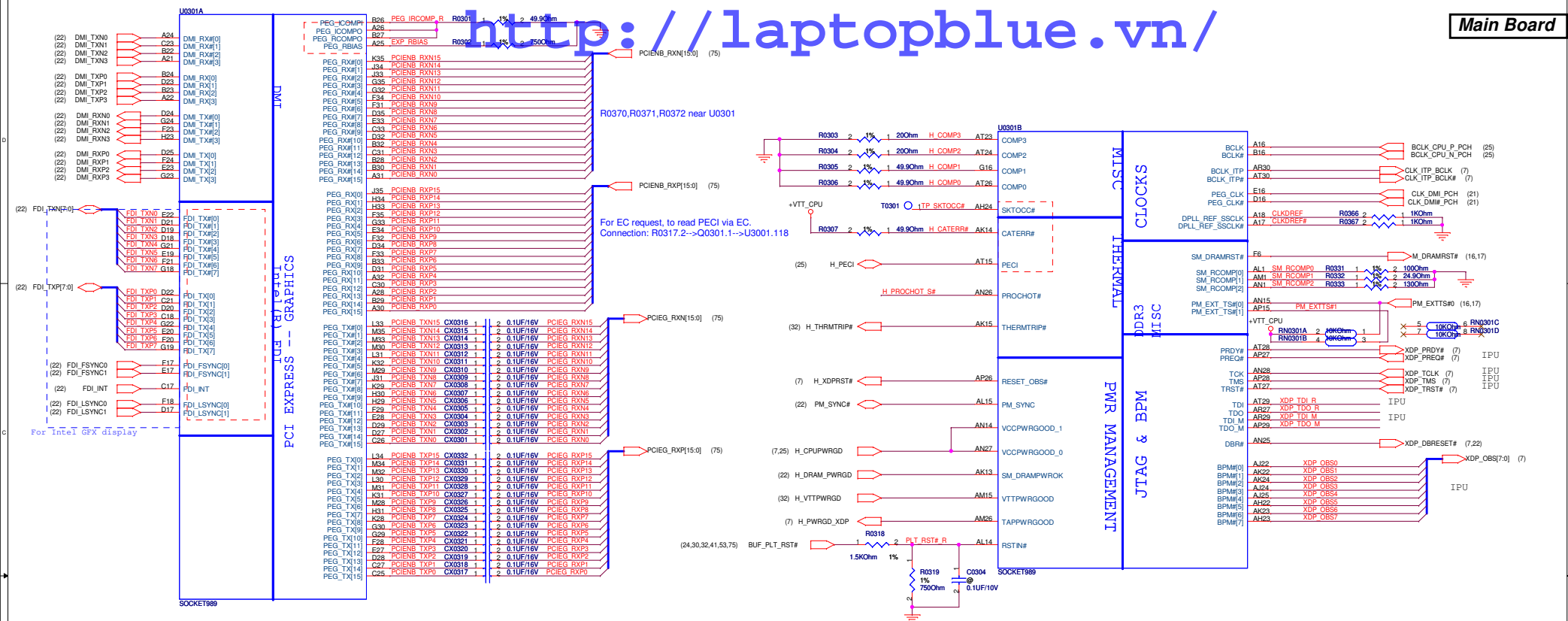
SM\_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(ICS9LPR362)	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
VID Controller(ASM8272)	0011011x ( 36 )
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor(G780)	1001100x ( 98 )
VGA Thermal IC(G781-1)	1001101x ( 9A )

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	ESATA (for pre-ES1)
PCIE 6	GLAN
PCIE 7	
PCIE 8	

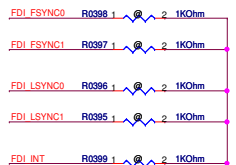
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	
USB 8	
USB 9	WLAN
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA



For Intel GFX display

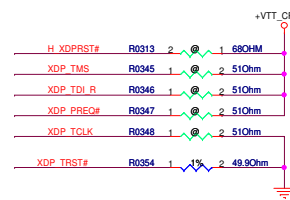
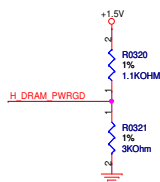
Stuff these resistors for disable IGPU



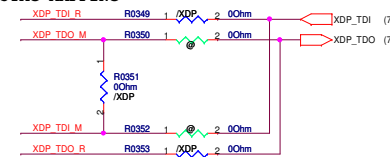
### DRAMPWROK: (WW35 MoW)

Choose either one solution: --> Choose solution 2

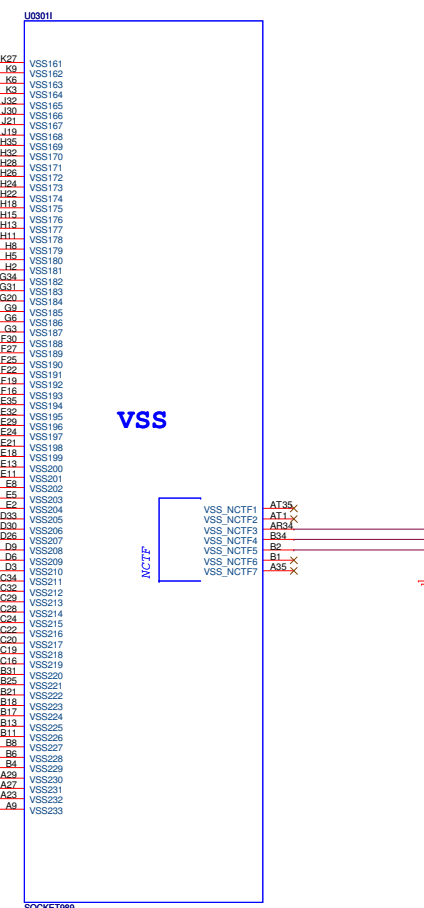
- This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
- Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.



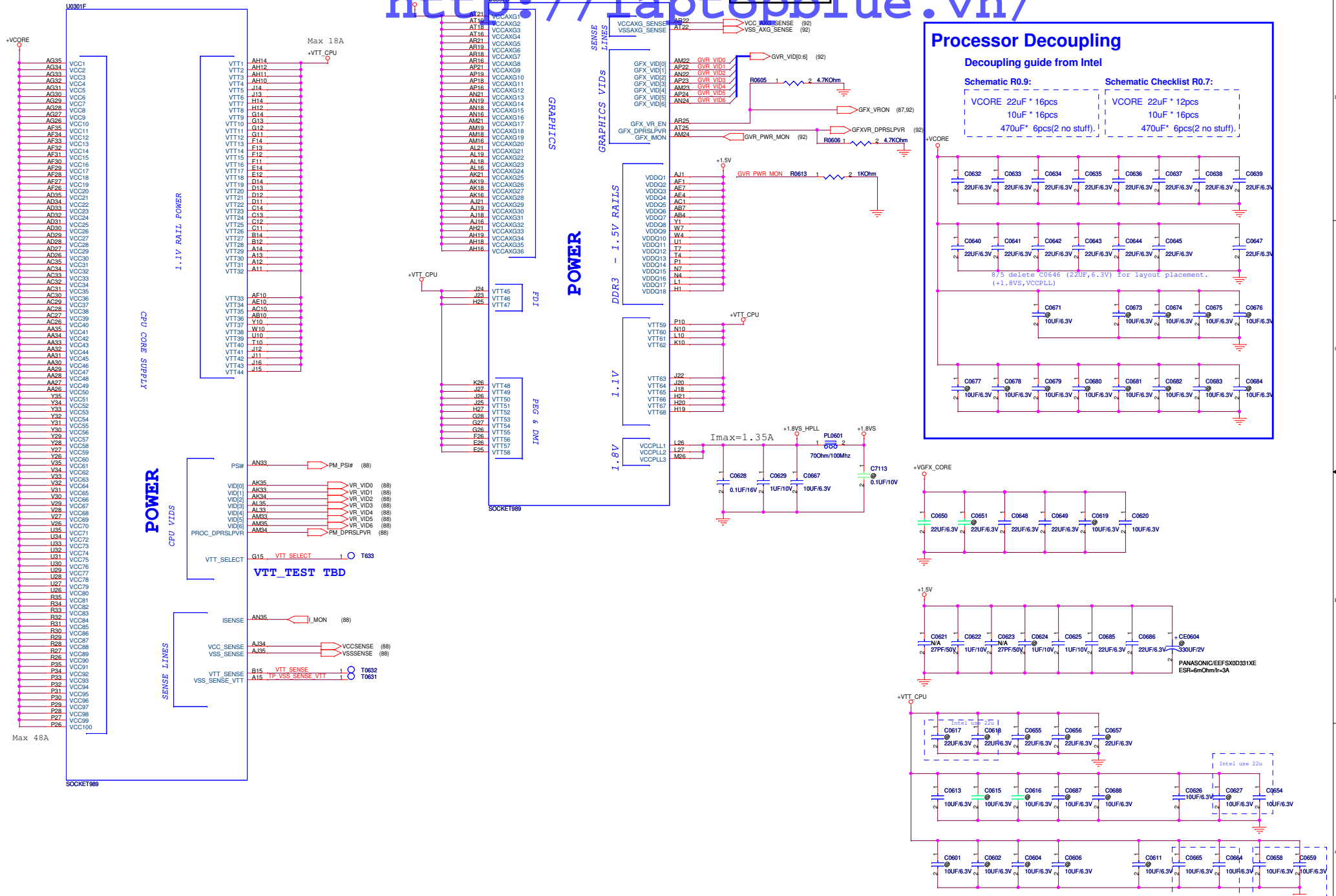
### JTAG MAPPING



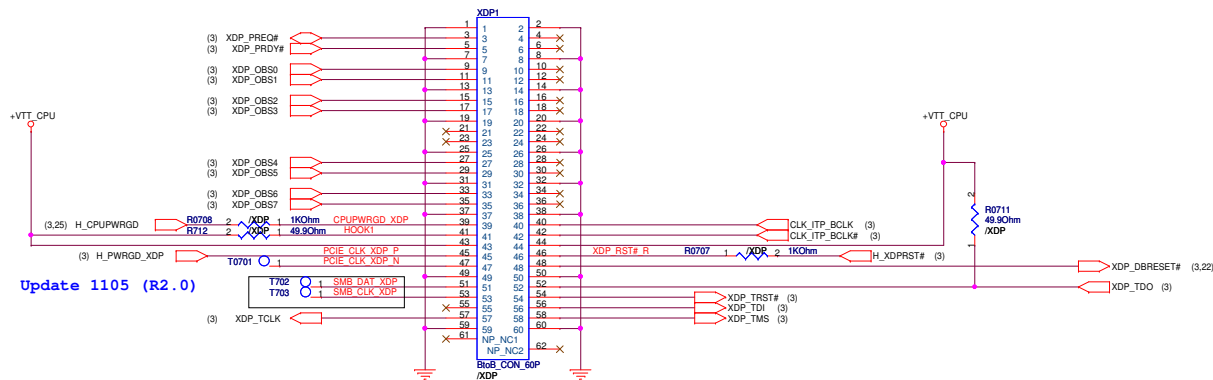




CFG3 R0544 1 1% 2 3KOhm  
CFG7 R0538 2 1 3KOhm 1% @



## CPU XDP connector



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		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: CH_Lin	
Size	Project Name		Rev
A	M60JV		1.01
Date: Thursday, November 12, 2009		Sheet	14 of 96

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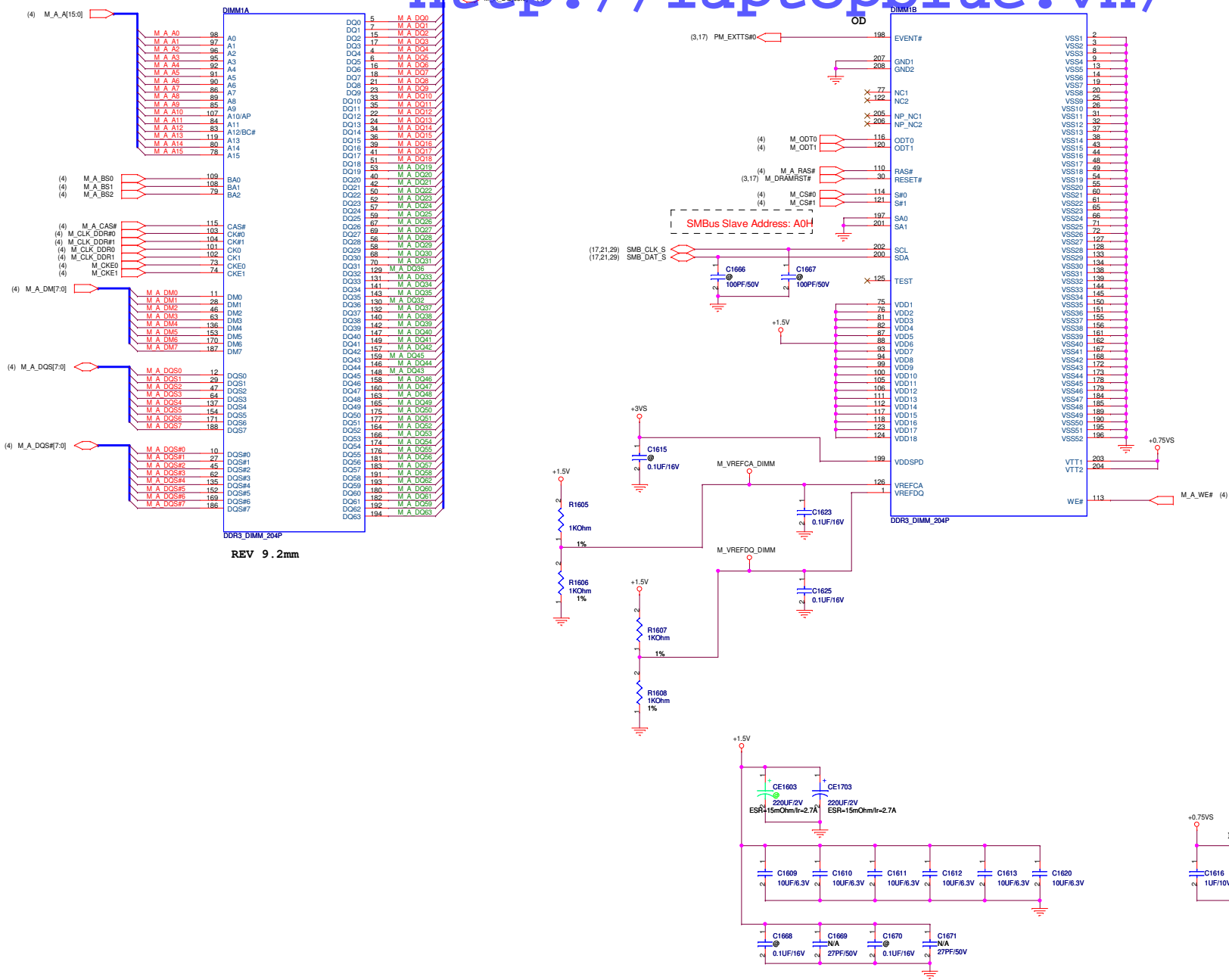
Title :

ASUSTeK COMPUTER INC. NB6

Engineer: CH\_Lin

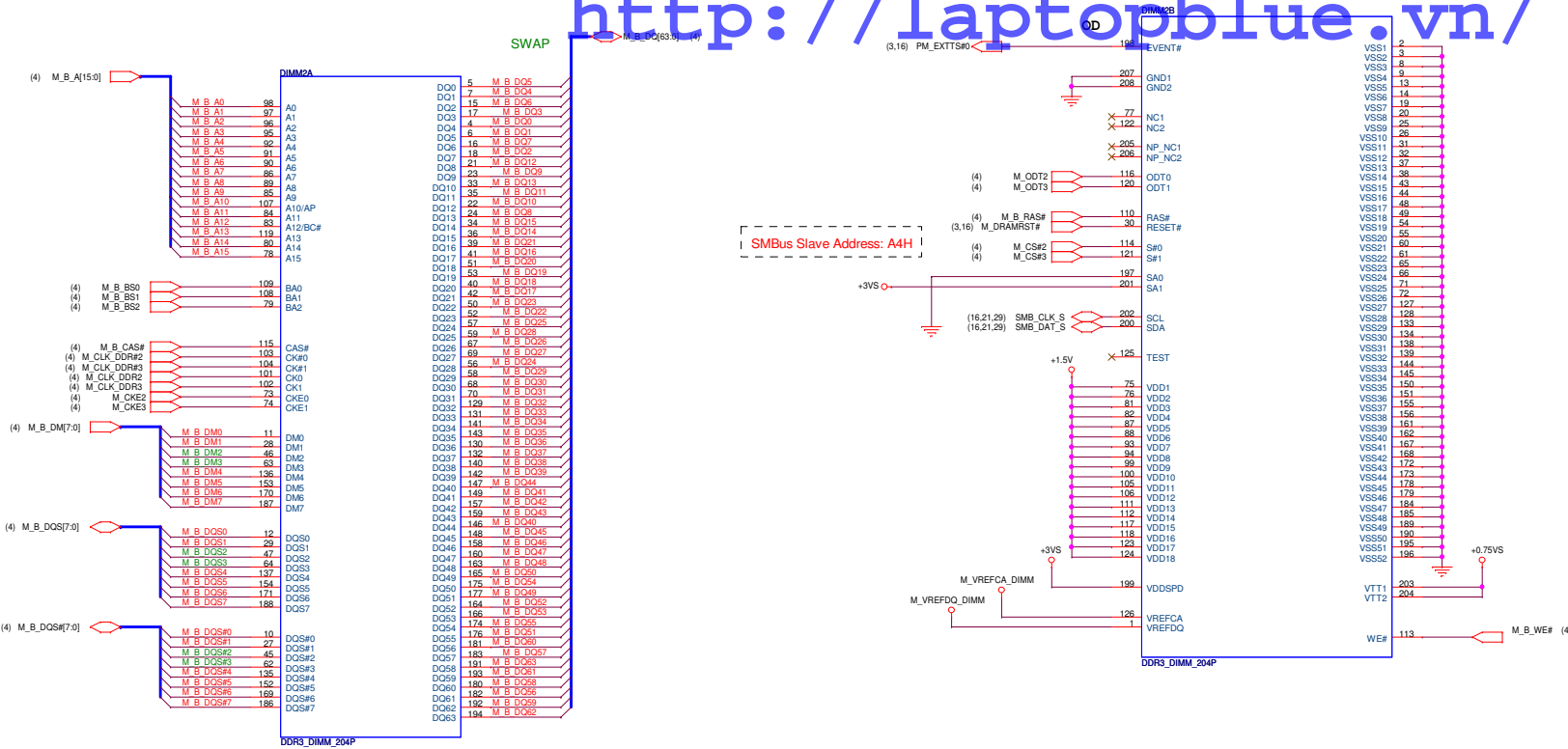
Size	Project Name	Rev
A	M60JV	1.01

Date: Thursday, November 12, 2009Sheet 15 of 96



Layout Note: Place these caps near SO DIMMS





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Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO_REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. <b>NOTE:</b> This signal should not be pulled low.
GNT[3]# / GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. <b>NOTE:</b> This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment															
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts.															
			This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers/Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.															
			<table><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
			Bit11	Bit 10	Boot BIOS Destination													
			0	1	Reserved													
1	0	PCI																
1	1	SPI																
0	0	LPC																
<b>NOTE:</b> If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot.																		
<b>NOTE:</b> Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.																		

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDA TA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDA TA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDA TA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment															
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	<p>This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.</p> <table><thead><tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr></thead><tbody><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table> <p><b>NOTE:</b> If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.</p> <p><b>NOTE:</b> Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.</p>	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
			Bit11	Bit 10	Boot BIOS Destination													
0	1	Reserved																
1	0	PCI																
1	1	SPI																
0	0	LPC																
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	<p>This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts.</p> <p>Tying this strap low configures DMI for ESI compatible operation.</p> <p><b>NOTE:</b> ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.</p>															
NV_ALE	Reserved	Rising edge of PWROK	<p>This signal has a weak internal pull down. <b>NOTE:</b> This signal should not be pulled high</p>															

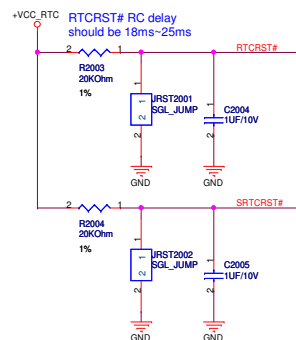
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN# / GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. <b>NOTE:</b> Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SP1_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. <b>NOTE:</b> This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. <b>NOTE:</b> This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	<b>This signal should be left as a No Connect.</b>
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. <b>NOTE:</b> A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

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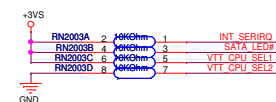
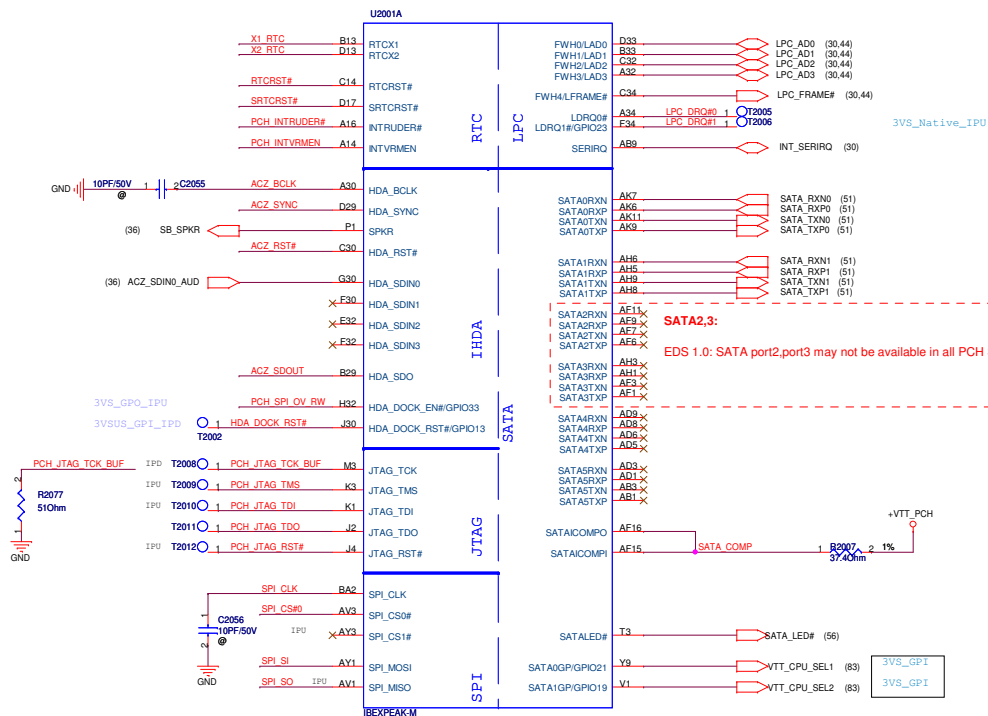
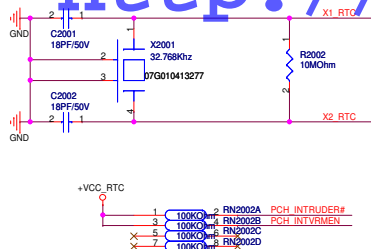
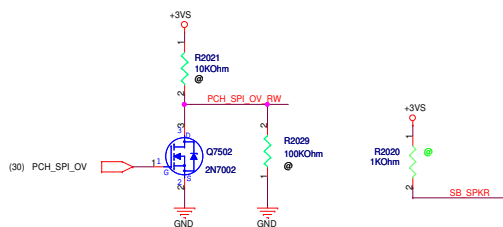
<i>CMOS Settings</i>	<i>JRST2001</i>
<i>Clear CMOS</i>	<i>Shunt</i>
<i>Keep CMOS</i>	<i>Open (Default)</i>

<b>TPM Settings</b>	<b>JRST2002</b>
<b>Clear ME RTC Registers</b>	<b>Shunt</b>
<b>Keep ME RTC Registers</b>	<b>Open (Default)</b>

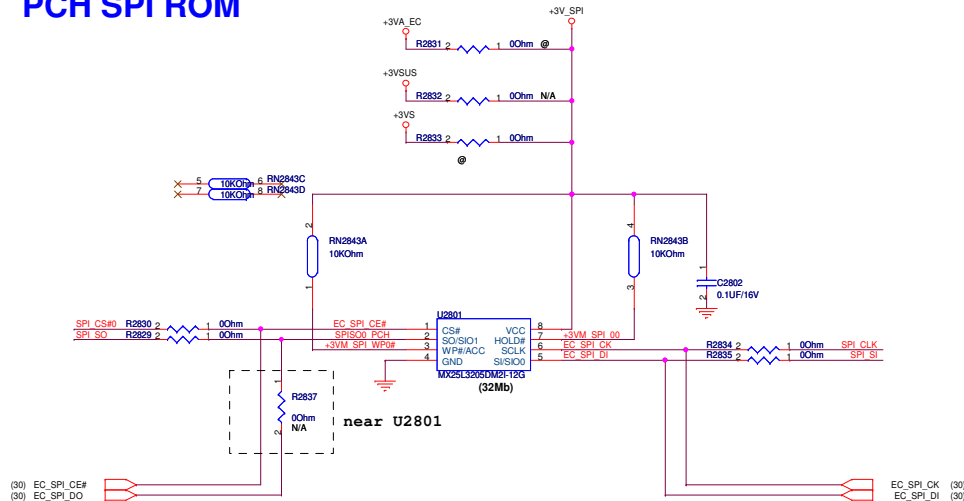


Strap information:

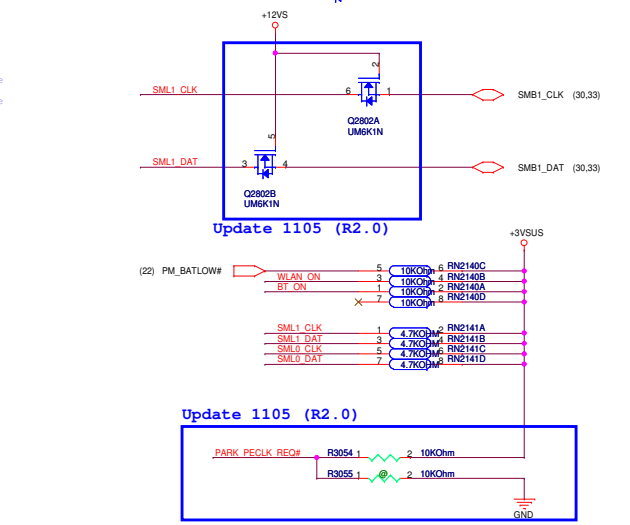
	H	L
ACT_SYNC: Select VCCVRRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SFPR: No reboot strap (IPD)	No reboot	Disable No reboot
PCR_SPI_OV_RM: (IPU)	No Flash ME FW	Flash ME FW
SPI_S1: 1TPW strap. (IPD)	Enable	Disable
PCR_INTVSMEN Integrated 1.05 V VRRM Enable /Disable	Enable	Disable



## PCH SPI ROM

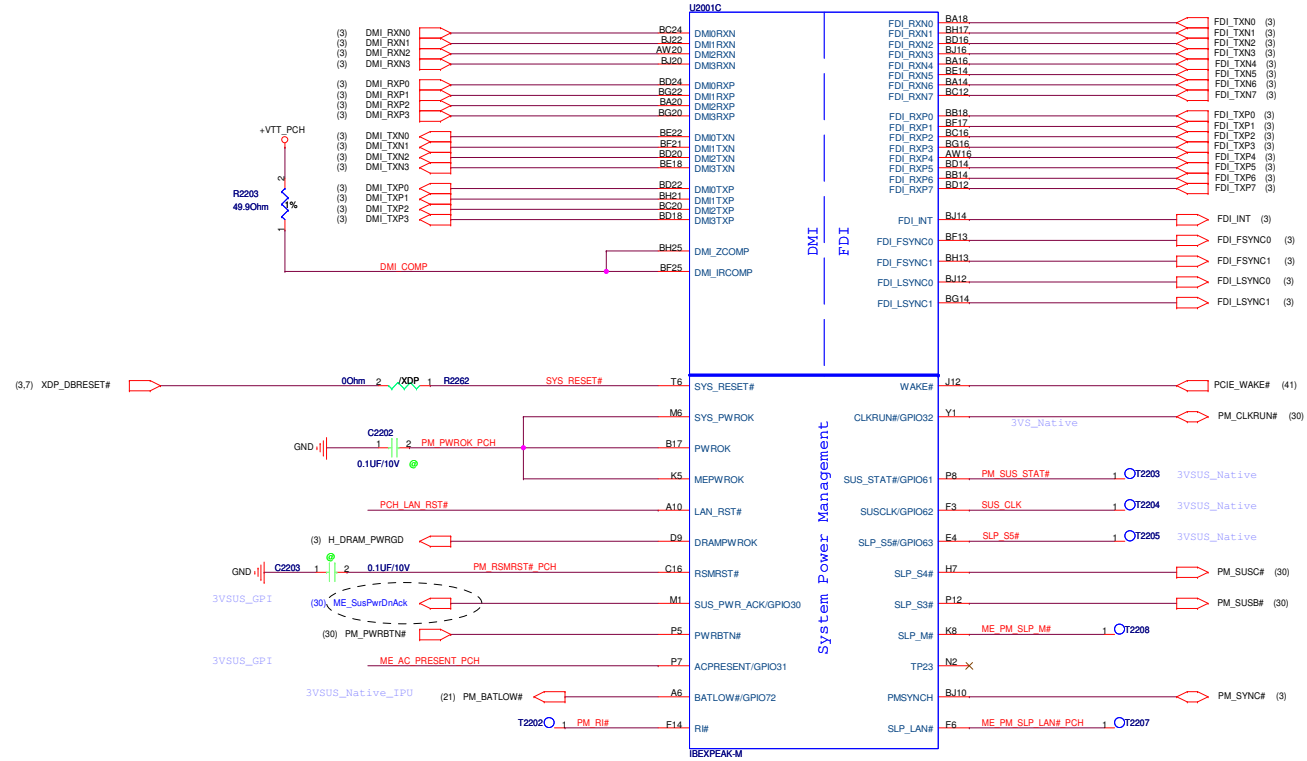
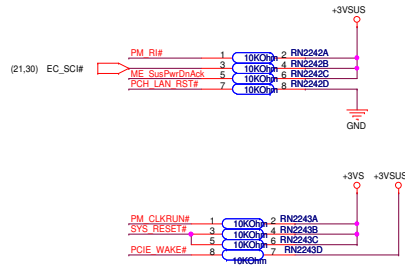


Update 1105 (R2.0)



Pin connection diagram for the ADXL345 accelerometer. The top section shows connections for CLK\_REQ# (pin 1), CLK\_REQ# (pin 3), CLK\_REQ# (pin 5), and CLK\_REQ# (pin 7) to pins 2, 4, 6, and 8 of the ADXL345. The bottom section shows connections for CLK\_REQ# (pin 1), CLK\_REQ# (pin 3), CLK\_REQ# (pin 5), and CLK\_REQ# (pin 7) to pins 2, 4, 6, and 8 of the ADXL345. The diagram also shows a +3V5 supply and a GND connection.

WW35 Update: Integrated Graphics platforms that use onlyLVDS and/or VGA Displays may use Buffer Through Mode (BTM) and leave 25-MHz crystal and RC components unstuffed



#### R1.1,item L15

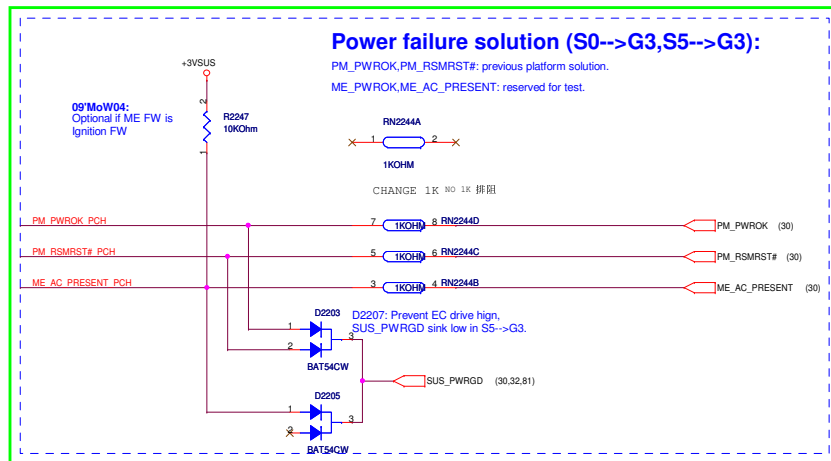
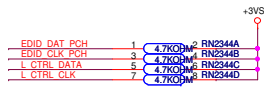


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.



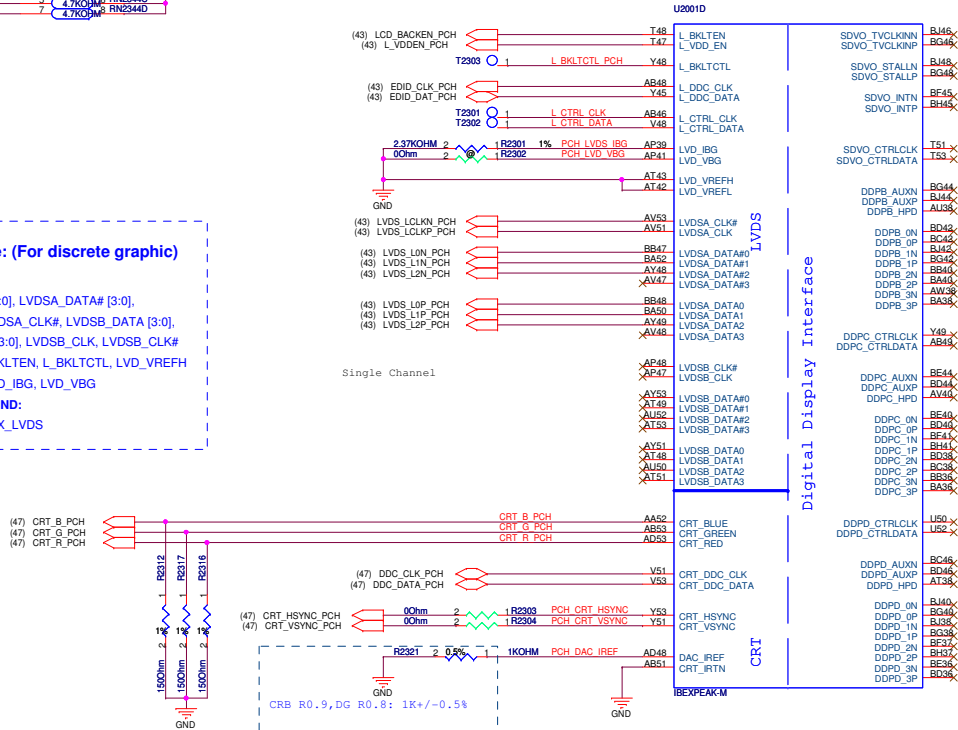
## LVDS Disable: (For discrete graphic)

### 1. NC:

LVDSA\_DATA [3:0], LVDSA\_DATA# [3:0],  
LVDSA\_CLK, LVDSA\_CLK#, LVDSB\_DATA [3:0],  
LVDSB\_DATA# [3:0], LVDSB\_CLK, LVDSB\_CLK#  
L\_VDD\_EN, L\_BKLTEN, L\_BKLTCTL, LVD\_VREFH  
LVD\_VREFL, LVD\_IBG, LVD\_VBG

### 2. Connected to GND:

VccALVDS, VccTX\_LVDS



## CRT Disable: (For discrete graphic)

### 1. NC:

CRT\_RED, CRT\_GREEN, CRT\_BLUE  
CRT\_HSYN, CRT\_VSYN

### 2. 1-kΩ ±0.5% pull-down to GND:

DAC\_IREF

### 3. Connected to GND:

CRT\_ITRN

### 4. Connect to +V3.3:

VCCADAC

DGPU\_SELECT#:  
0=GPU, 1=GPU

PCI\_PME#: Internal PU to suspend plane.  
change to PCI\_CLK4 to sync ICS364

GNT0#,GNT1#: Boot BIOS Strap.

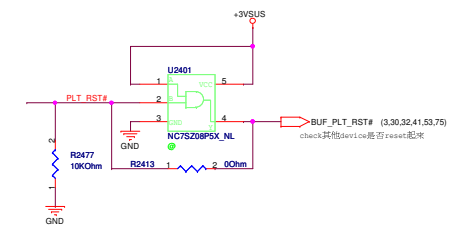
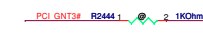
Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

Sampled on rising edge of PWROK.



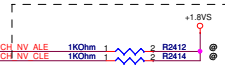
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default



Strap information:

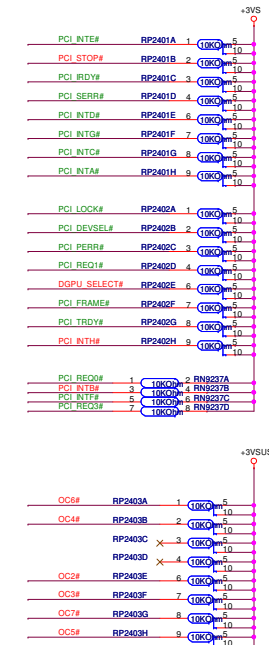
	H	L
PNL_NV_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable	Enable	Disable
NV_CLE: Strap DMI Termination Voltage		



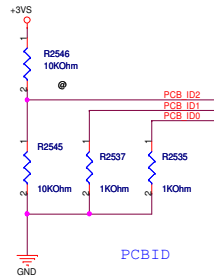
NV\_ALE: Strap Intel Anti-Theft Technology HDD Data Protection Enable. (H: enable)  
NV\_CLE: Strap DMI Termination voltage

K82JR	Recommend settings
0 USB port	
1 USB port	
2 USB port	
3	
4 WiFi/WiMax	
5	
6	
7	
8	
9 Camera	
10	
11	
12 BT (1.1)	
13	

3VSUS\_Native [9,10,14,40,41,42,43,59]

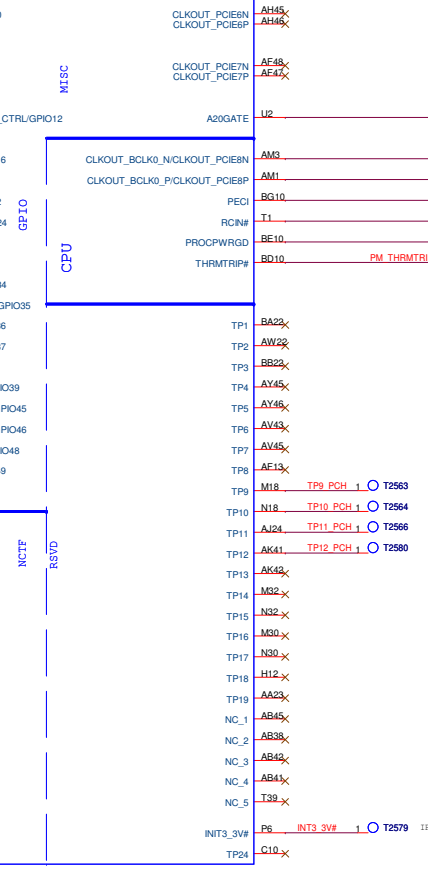
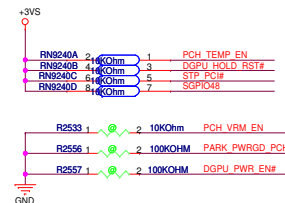
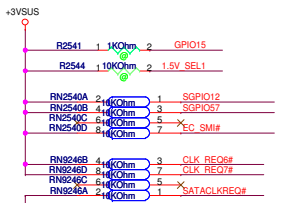
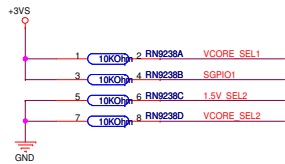




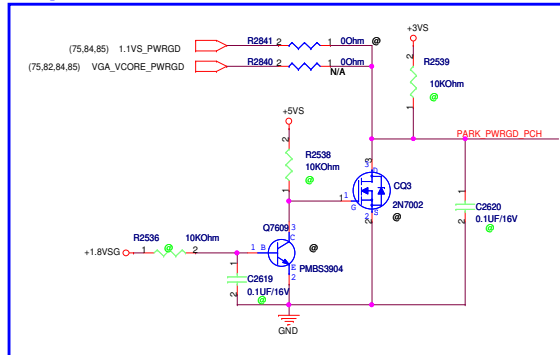


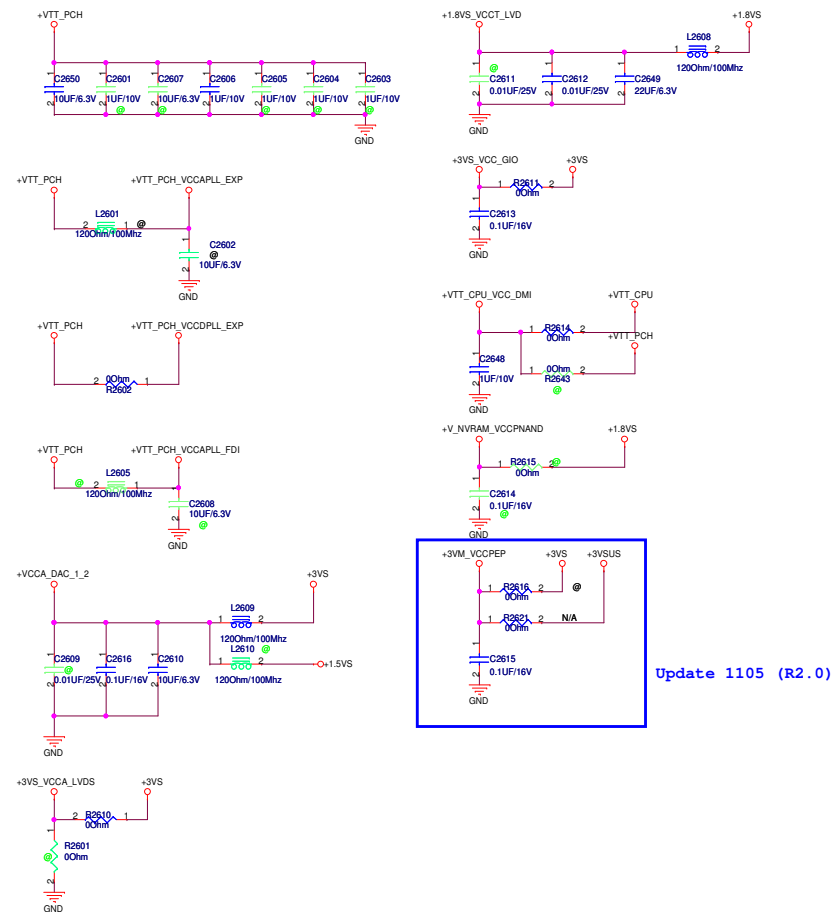
All GPIOs are reset to the default state by CF9h reset except GPIO24.

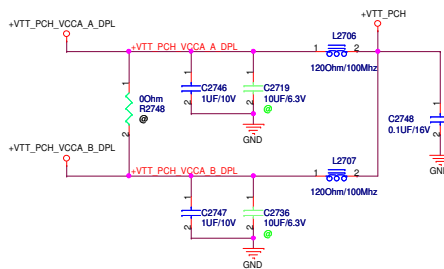
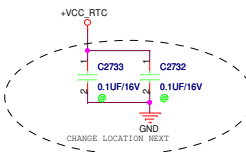
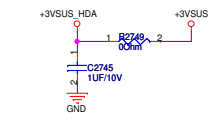
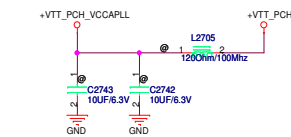
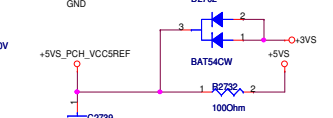
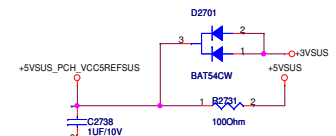
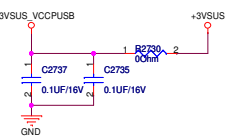
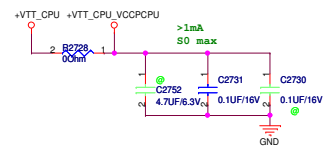
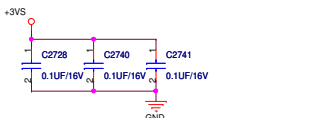
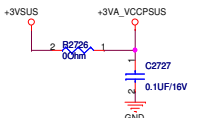
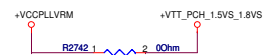
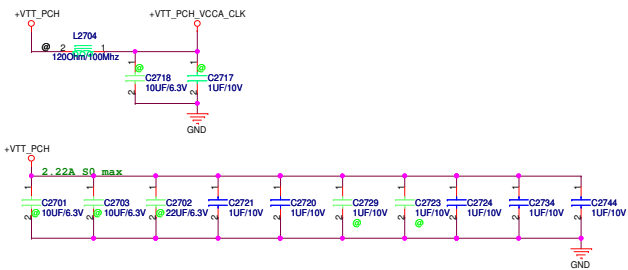
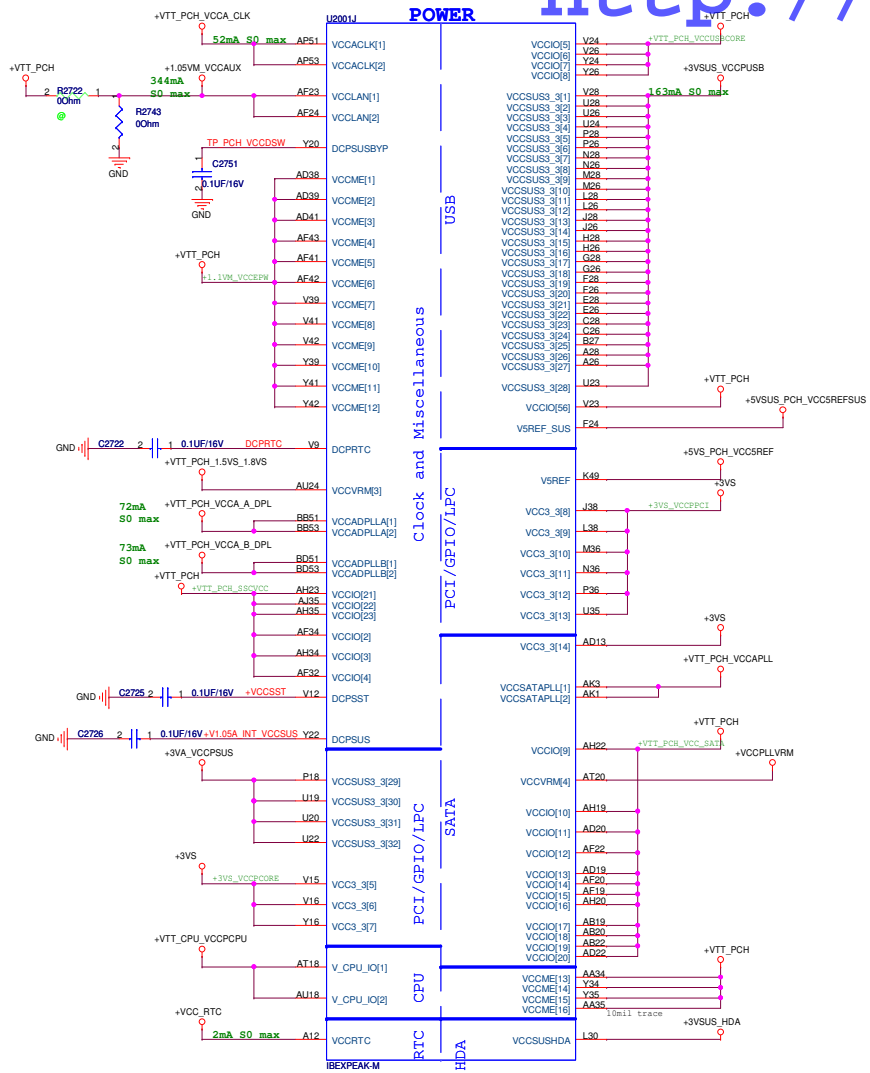
GPIO 27: Enable VCCVRM, Low=disable. Default internal pull up.

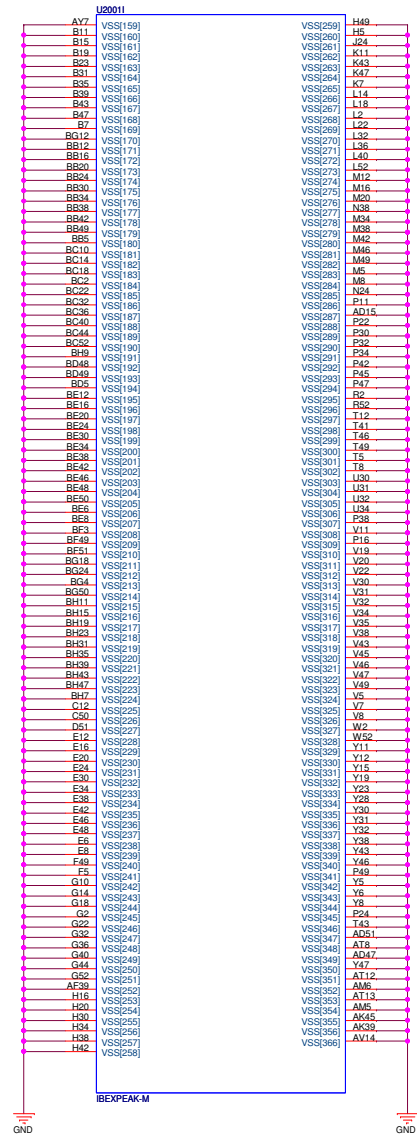
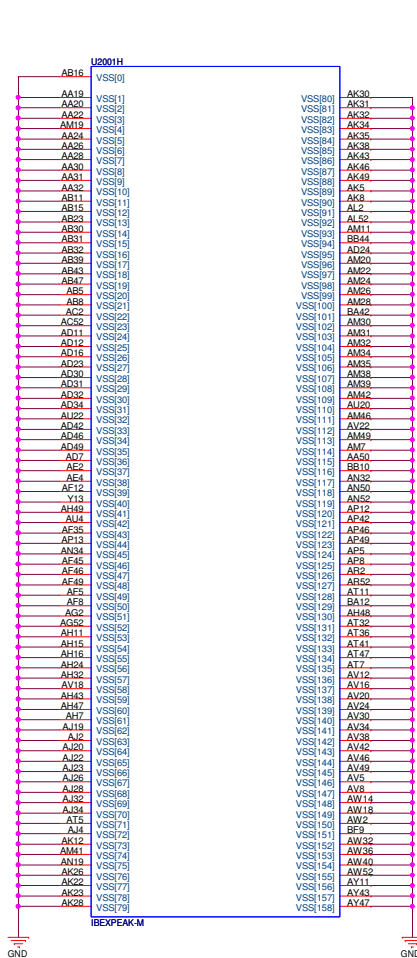


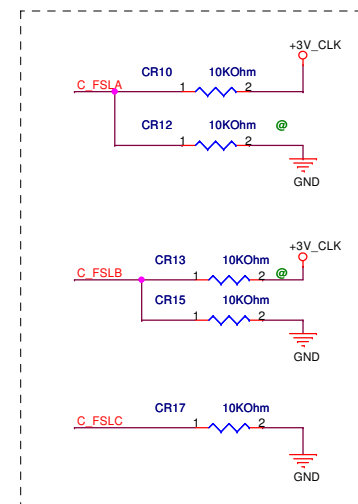
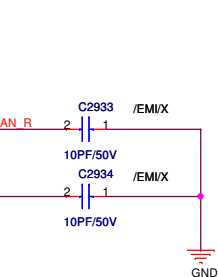
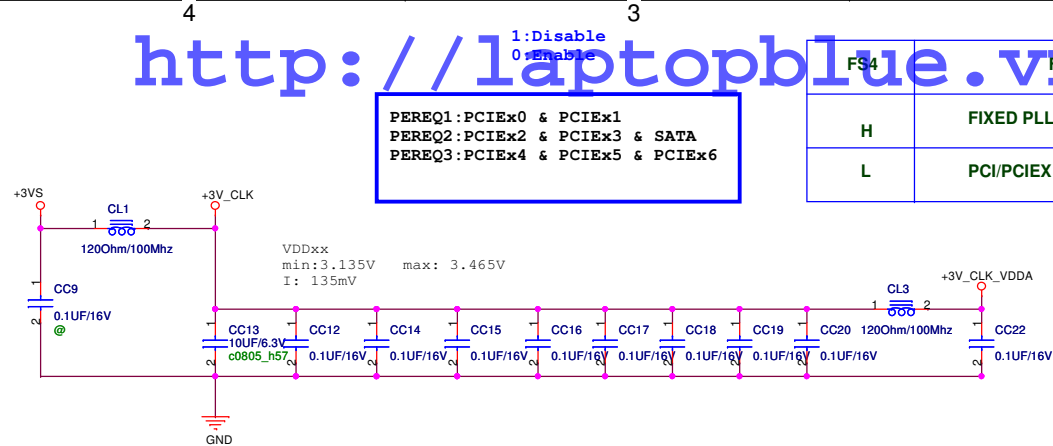
## Update 1109, R2.0

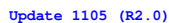


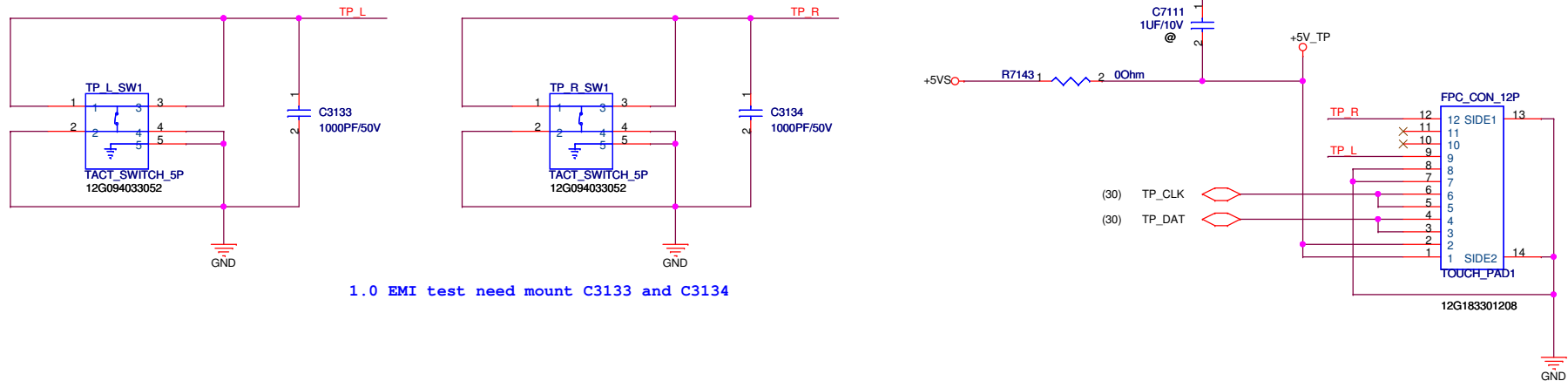






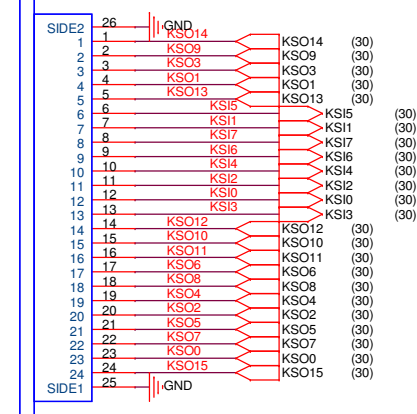






## Keyboard Connector

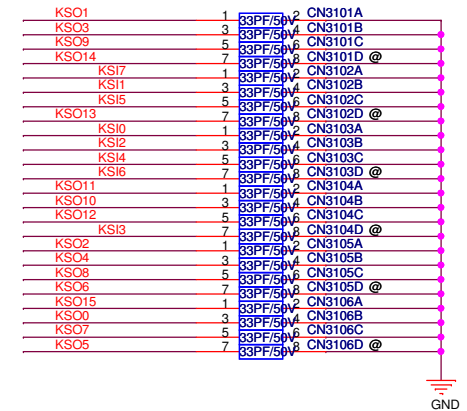
KB\_CON1



FPC\_CON\_24P

12G182102402

EMI Request



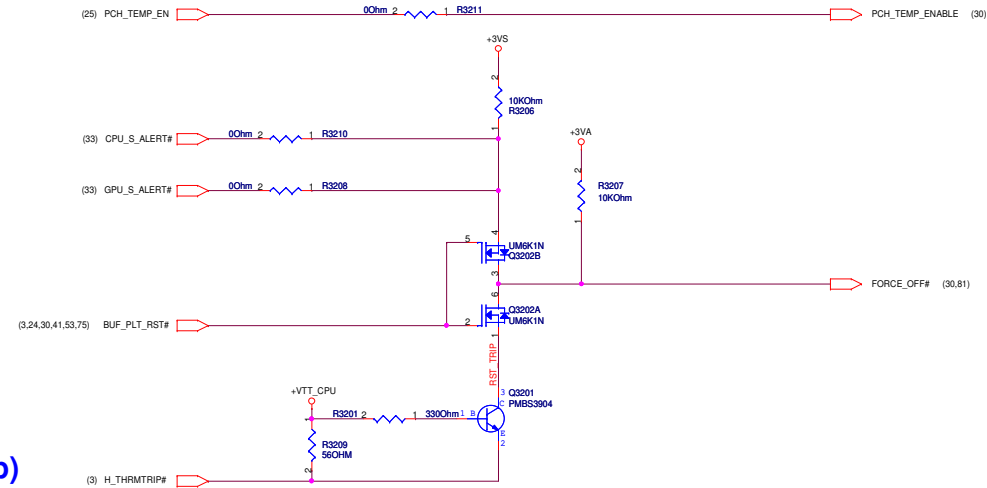
&lt;Variant Name&gt;

<http://laptopblue.vn/>

## Thermal Policy

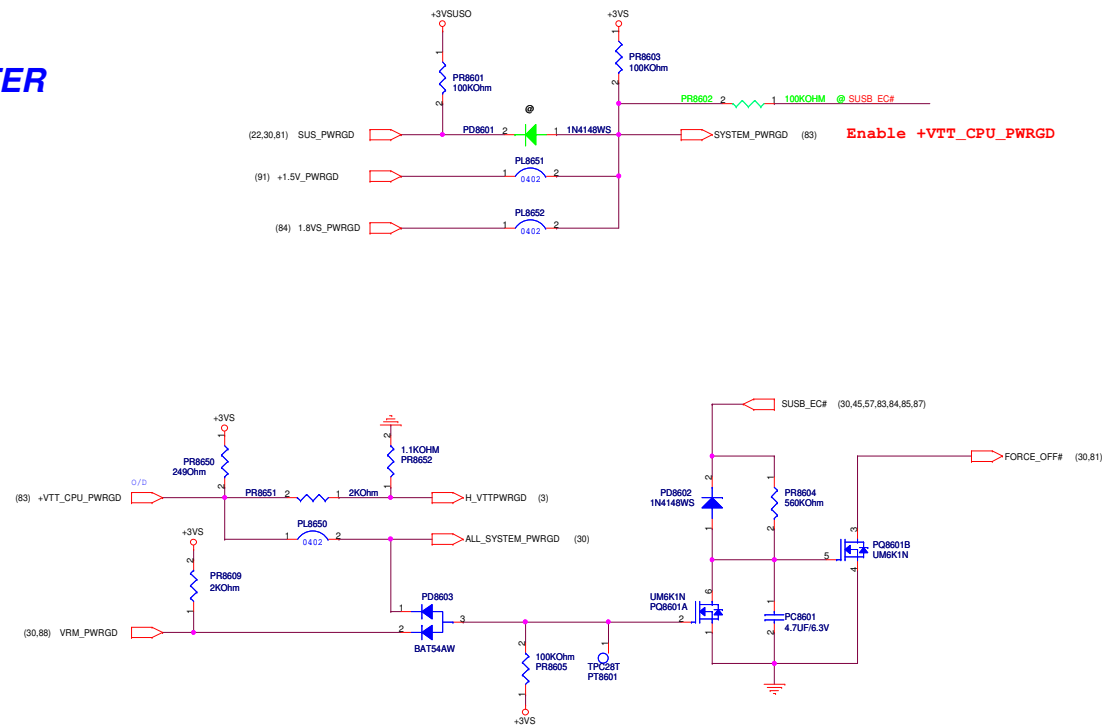
Input 1(sensor)

Input 2(thermtrip)



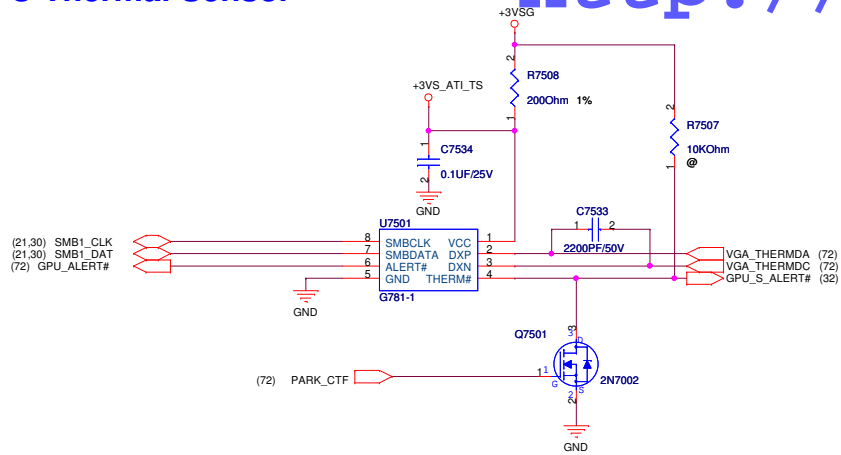
Output (shut down)

## POWER GOOD DETECTOR



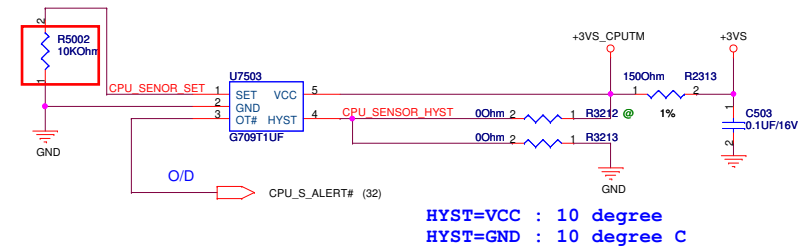


## GPU Thermal Sensor



## CPU Thermal Sensor

Update 1108 (R2.0)

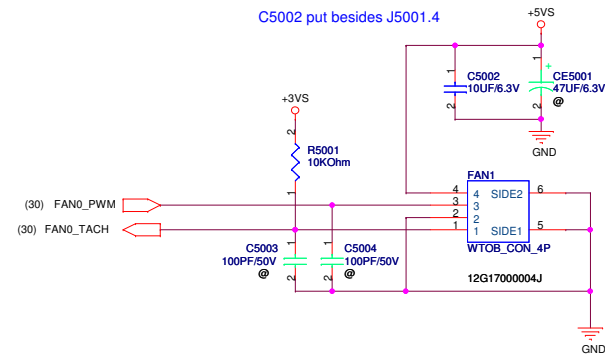


HYST=VCC : 10 degree  
HYST=GND : 10 degree C

U7503 under CPU socket

## PWM Fan

Remove diode(+5Vs to GND)  
for using 4-wires PWM FAN.



<b>ASUS</b>		Title : AR8131	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	LAN Design IP	108	
Date: Thursday, November 12, 2009		Sheet 33 of 96	

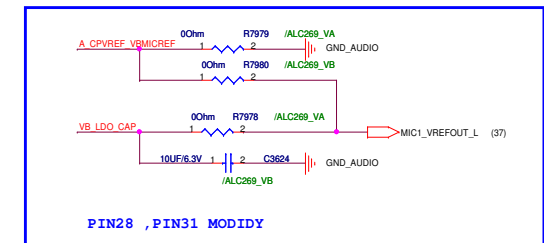
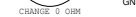
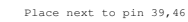
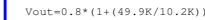
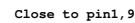
http://laptopblue.vn/

移至 USB BOARD

<Variant Name>		
		Title : 8131
ASUSTeK COMPUTER INC		Engineer:
Size Custom	Project Name LAN Design IP	Rev 108
Date: Thursday, November 12, 2009		Sheet 34 of 96

http://laptopblue.vn/

Main Board

[illegible]

```
269_VA : 02G611005006
269_VB : 02G611005010
```

(20) SB\_SPKR

SB\_SPKR

R3643  
4.7KOhm

2

PC\_BEEP\_C

1

C3646  
0.1uF/25V

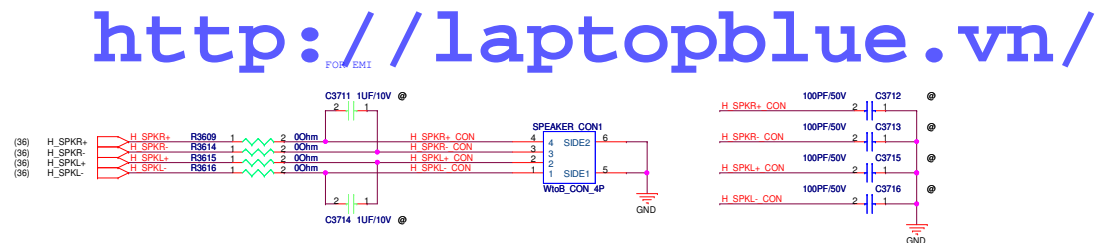
2

PC\_BEEP

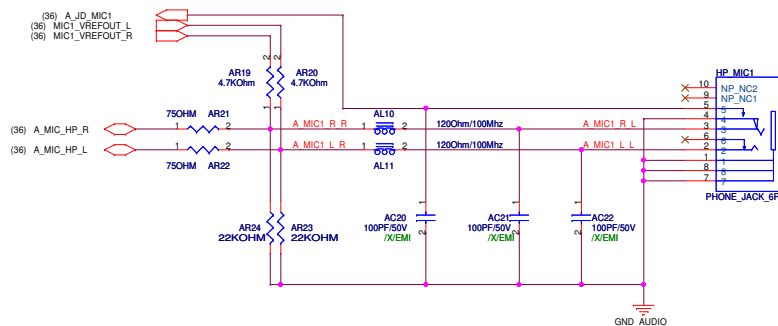
R3642  
4.7KOhm

GND

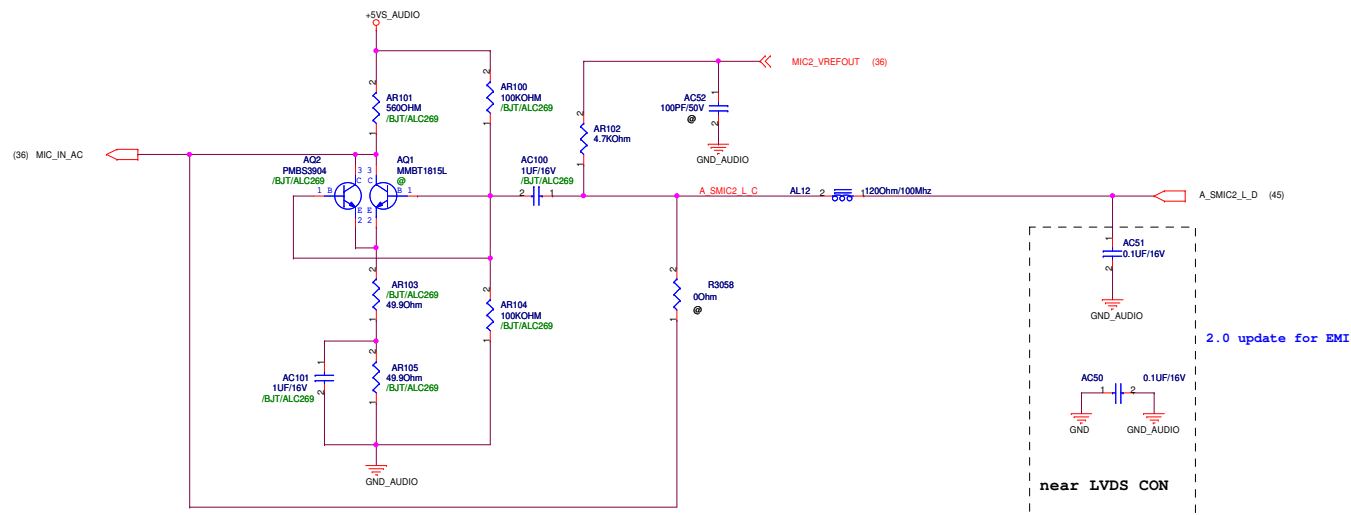
## SPEAKER



## HP and MIC



## Internal MIC and AMP



<http://laptopblue.vn/>


Main Board

http://laptopblue.vn/

http://laptopblue.vn/

Card Insert: Pin.10 and Pin.12 are Shorted.  
Card not Insert: Pin.10 and Pin.12 are Opened.  
Write Protect: Pin.11 and Pin.12 are Opened.  
Write Enable: Pin.11 and Pin.12 are Shorted.

<Variant Name>



Title : AU6433D53-GLF

ASUSTek Computer Inc.

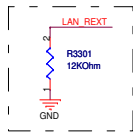
Engineer: Fehling\_Wang

Size	Project Name	Rev
A3	1008P Card Reader	1.0G

Date: Thursday, November 12, 2009Sheet 40 of 96

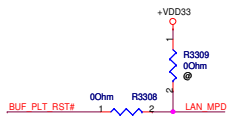


# Reference Resistance

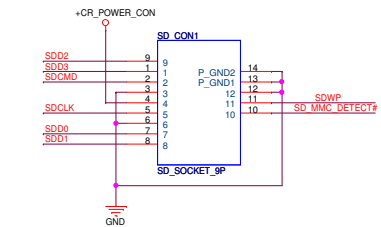
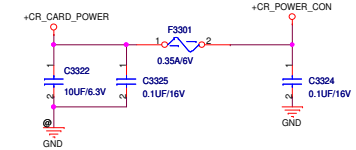
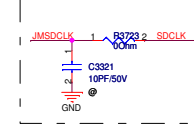
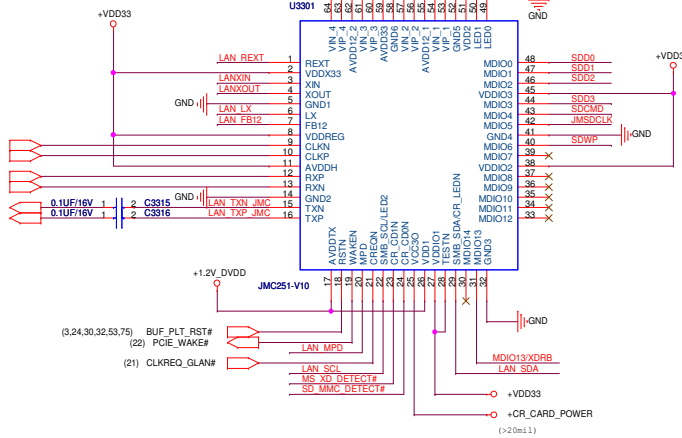


# D3E Enable/Disable

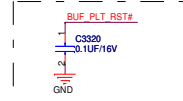
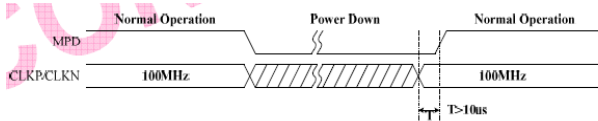
R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable



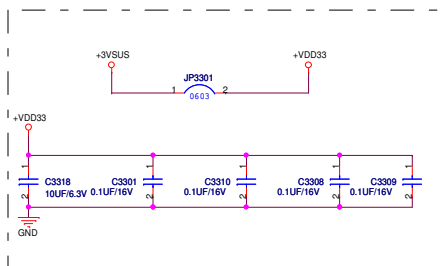
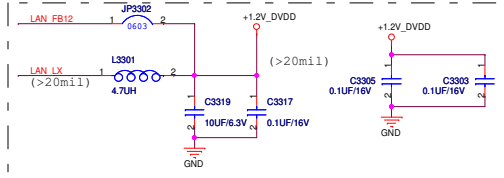
- (21) PCH\_C\_LAN\_N
- (21) PCH\_C\_LAN\_P
- (21) POE\_TX\_LAN\_P
- (21) POE\_TX\_LAN\_N
- (21) POE\_RX\_LAN\_N
- (21) POE\_RX\_LAN\_P



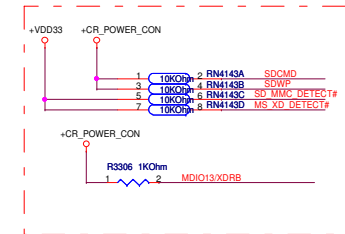
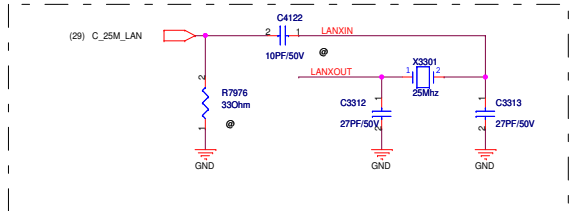
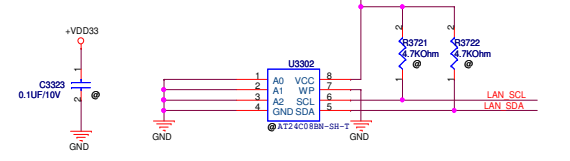
Card Insert: Pin.10 and Pin.12 are Shorted.  
Card not Insert: Pin.10 and Pin.12 are Opened.  
Write Protect: Pin.11 and Pin.12 are Opened.  
Write Enable: Pin.11 and Pin.12 are Shorted.




# Switch Regulator

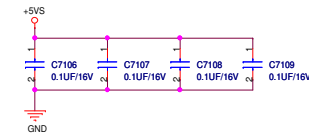
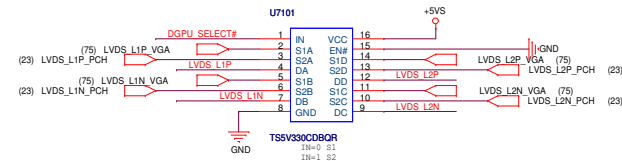
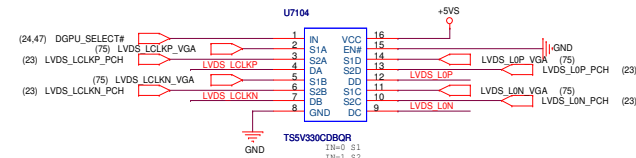
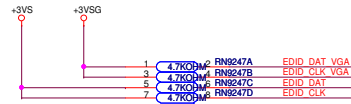
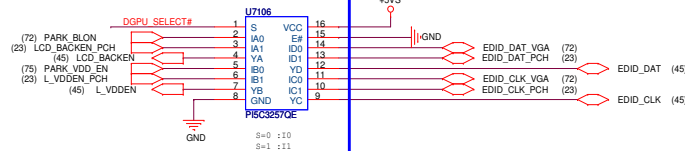
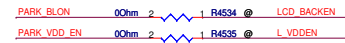
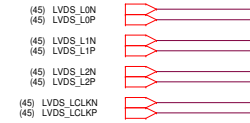


# Serial EEPROM



http://laptopblue.vn/

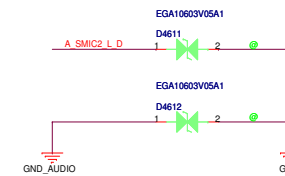
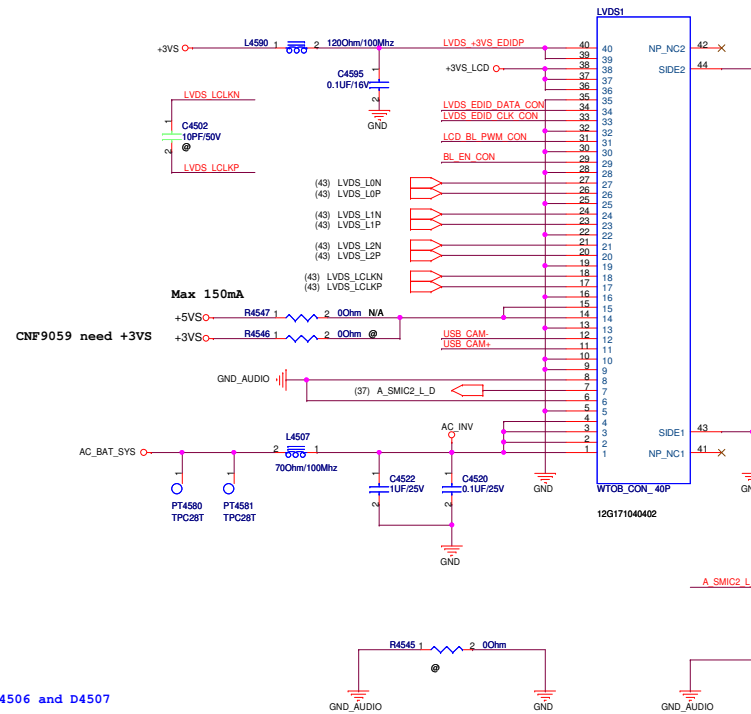
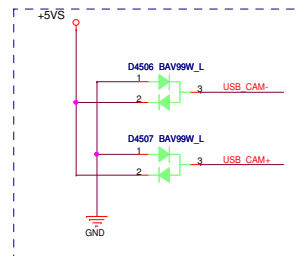
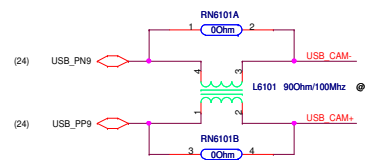
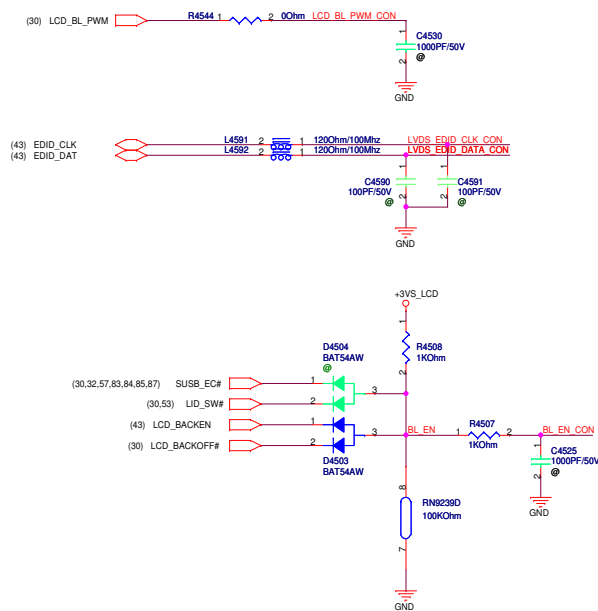
		Title : LAN_RJ45	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size Custom	Project Name M52J		Rev 1.3
Date: Thursday, November 12, 2009		Sheet 42 of 99	

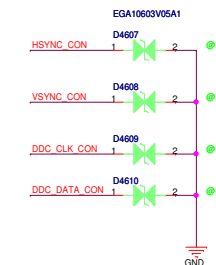
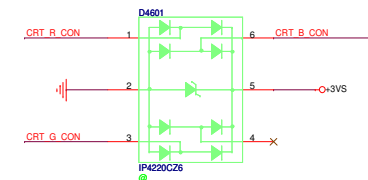
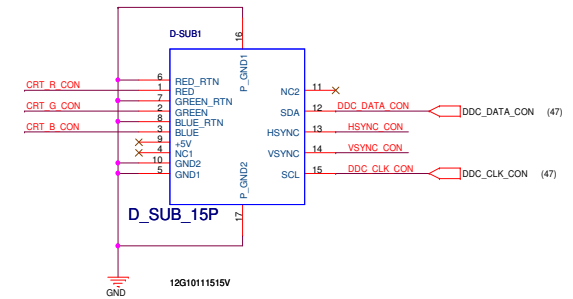


Pin 13 and 14 connections for the DEBUG1 and DEBUX headers. The diagram shows the following connections:

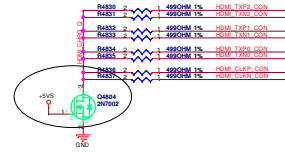
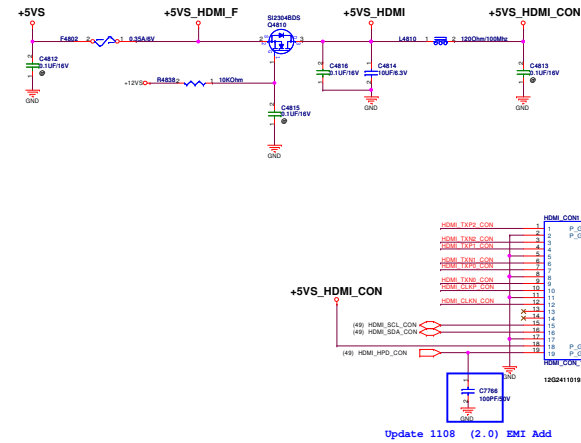
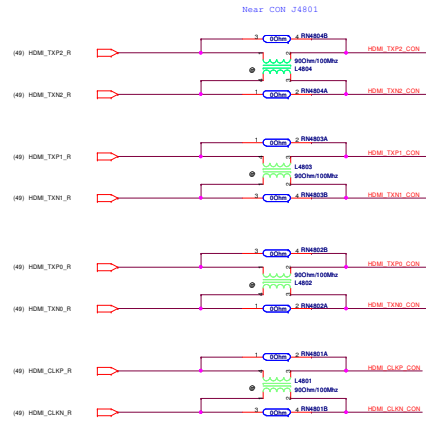
- Pin 13 (DEBUX1): Connected to LPC\_AD0 (20,30), LPC\_AD1 (20,30), LPC\_AD2 (20,30), LPC\_AD3 (20,30), and LPC\_FRAME# (20,30).
- Pin 14 (DEBUX2): Connected to LPC\_FRAME# (20,30) and CLK\_DEBUG (24).

The DEBUX1 header is labeled with pins 1 through 12. The DEBUX2 header is labeled with pins 1 through 12. The DEBUX1 header is also labeled with pins 13 and 14. The DEBUX2 header is labeled with pins 13 and 14. The DEBUX1 header is also labeled with pins 13 and 14. The DEBUX2 header is labeled with pins 13 and 14.

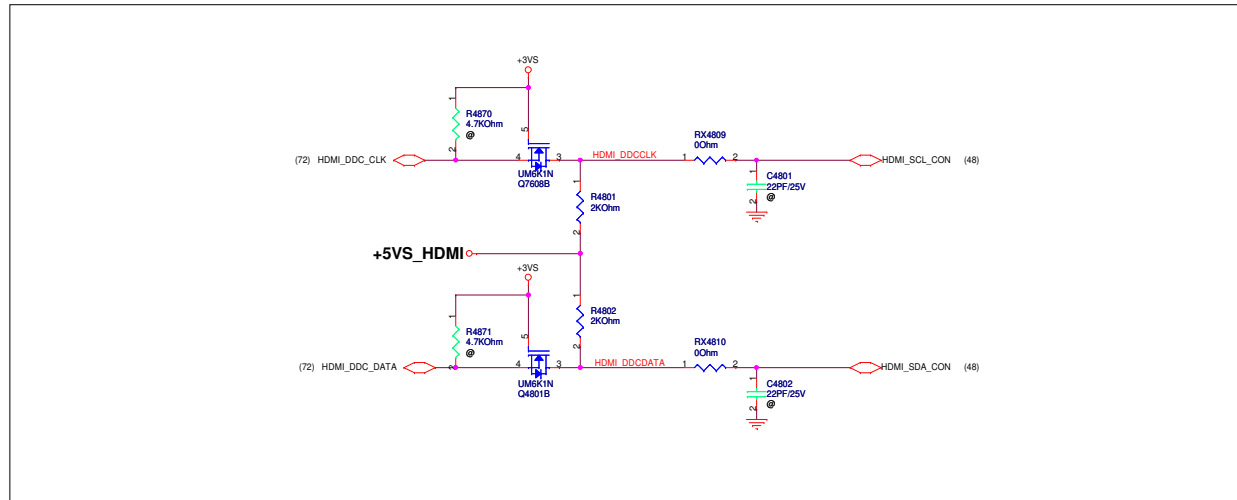
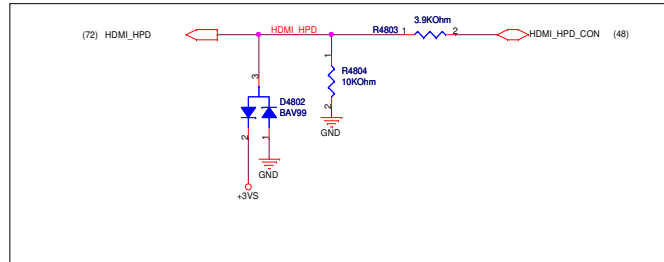
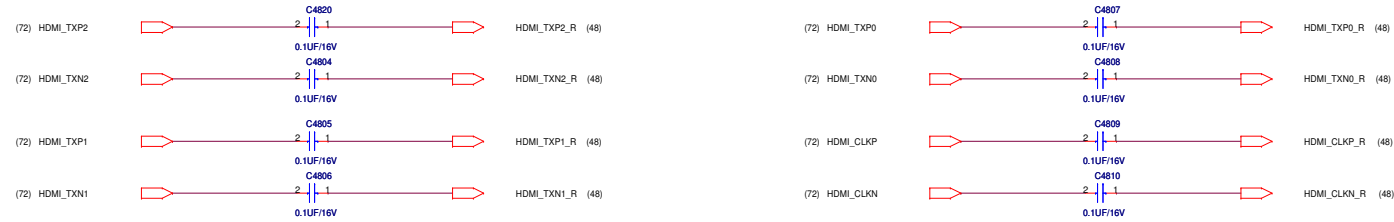
[illegible]



		<b>Title :</b> Display Port	
ASUSTeK COMPUTER INC. NB4		<b>Engineer:</b> CH_Lin	
Size C	Project Name  <b>M60JV</b>		Rev 1.01
Date: Thursday, November 12, 2009		Sheet	47 of 96



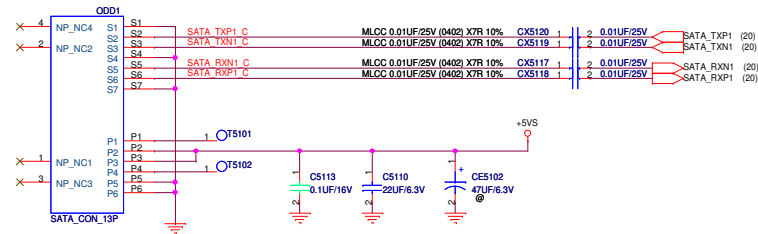




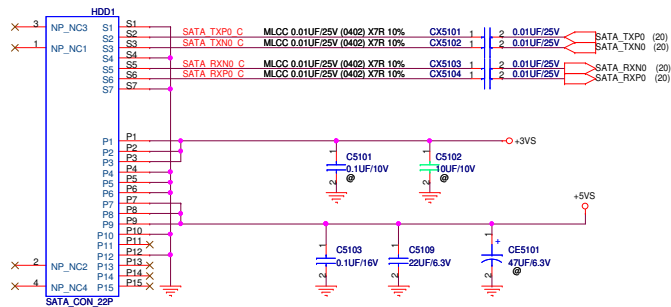
<http://laptopblue.vn/>

Main Board

## ODD

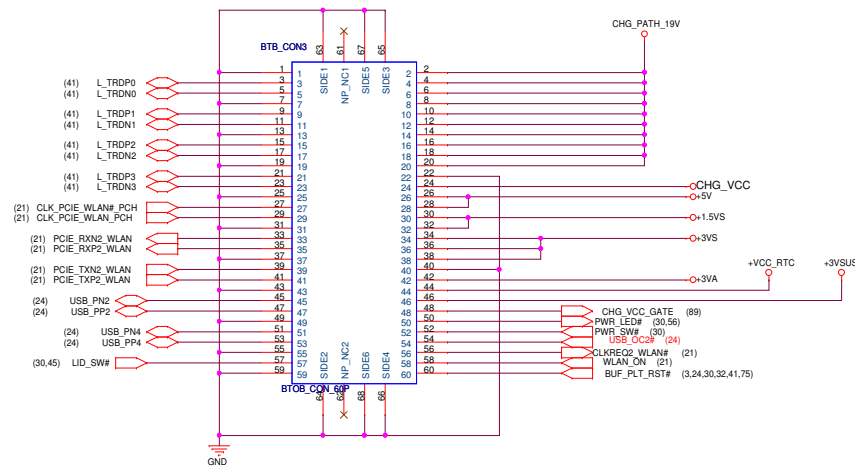


## HDD (1st)



[illegible][illegible]

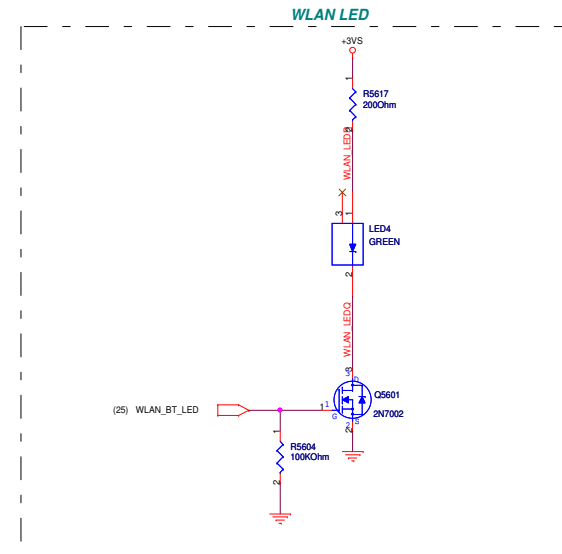
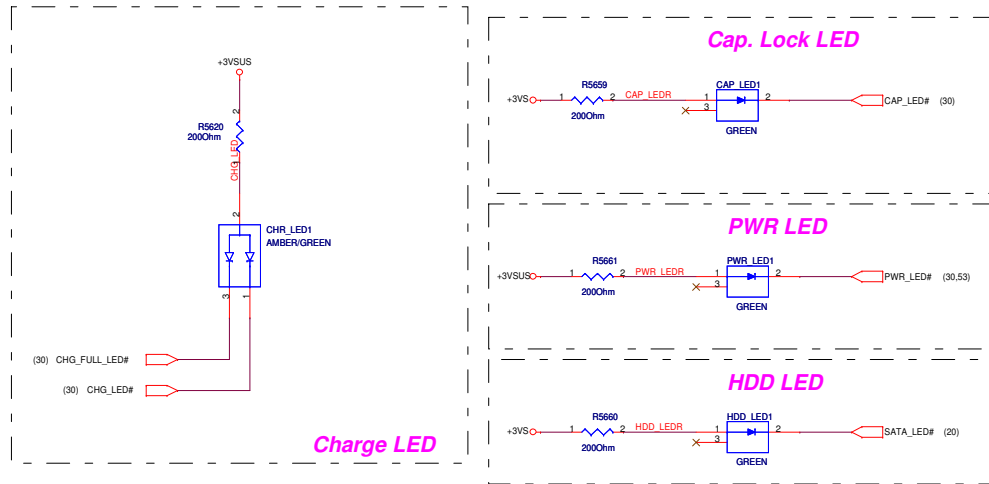
<http://laptopblue.vn/>



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Main Board

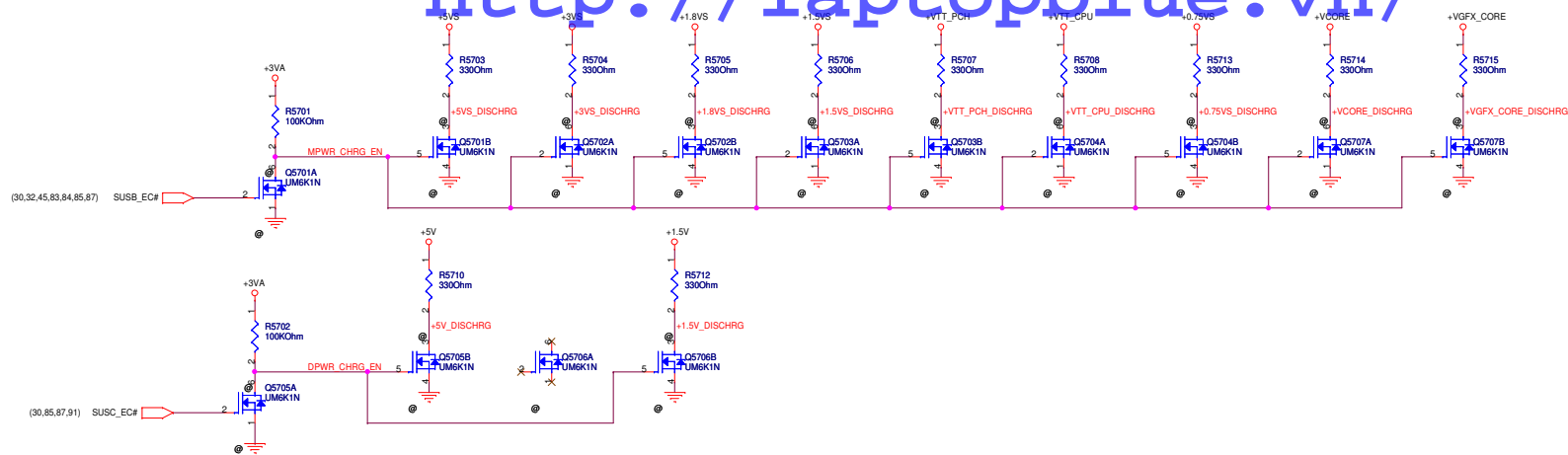


Change LED part number



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Main Board



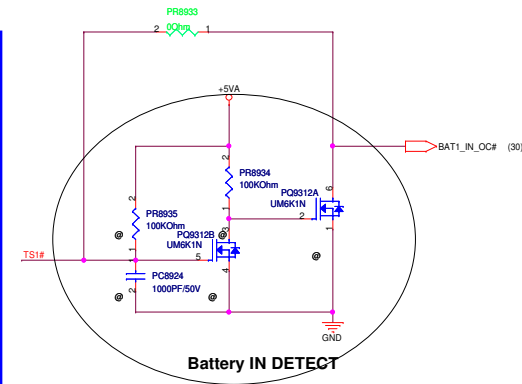
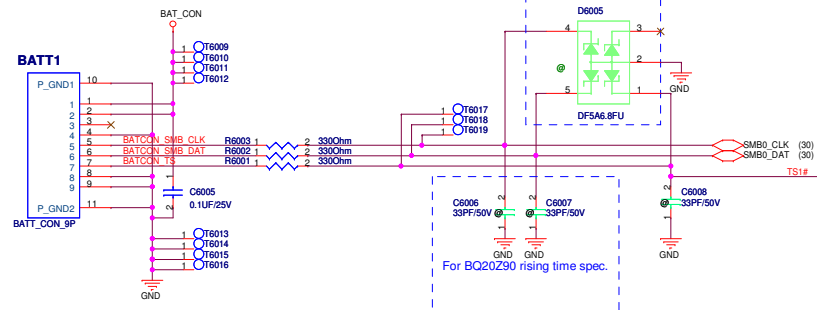
<http://laptopblue.vn/>

Main Board

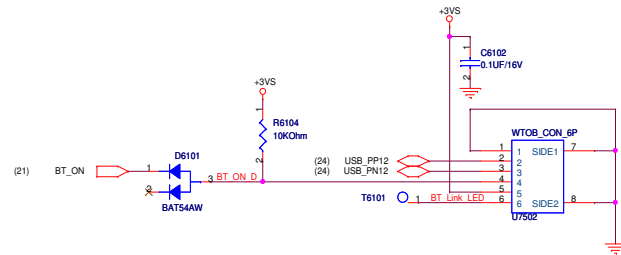
<http://laptopblue.vn/>

Main Board

## Battery Connector



## BLUETOOTH



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Main Board

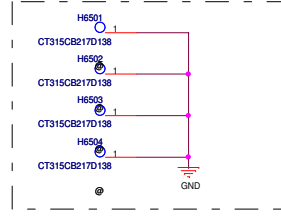
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Main Board

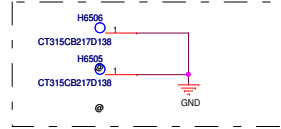
http://laptopblue.vn/



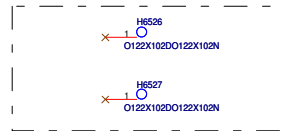
For CPU



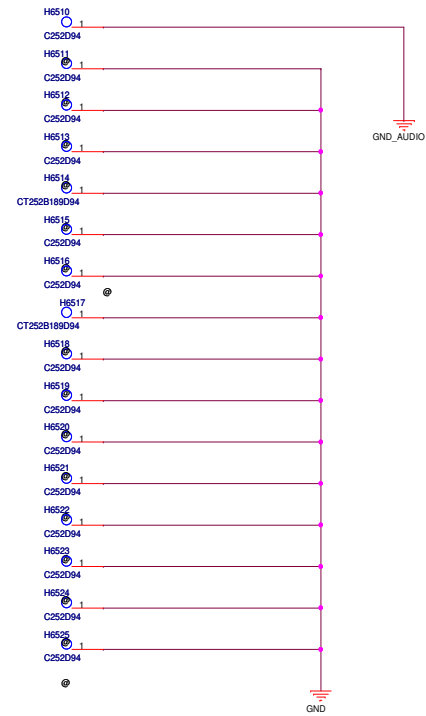
For GPU

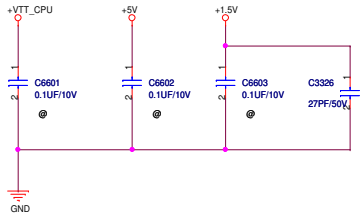


For 橢圓定位孔



HHD 呼吸孔





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Title :

ASUSTeK COMPUTER INC. NB4

Engineer:

Size	Project Name	Rev
Custom	M60JV	1.01

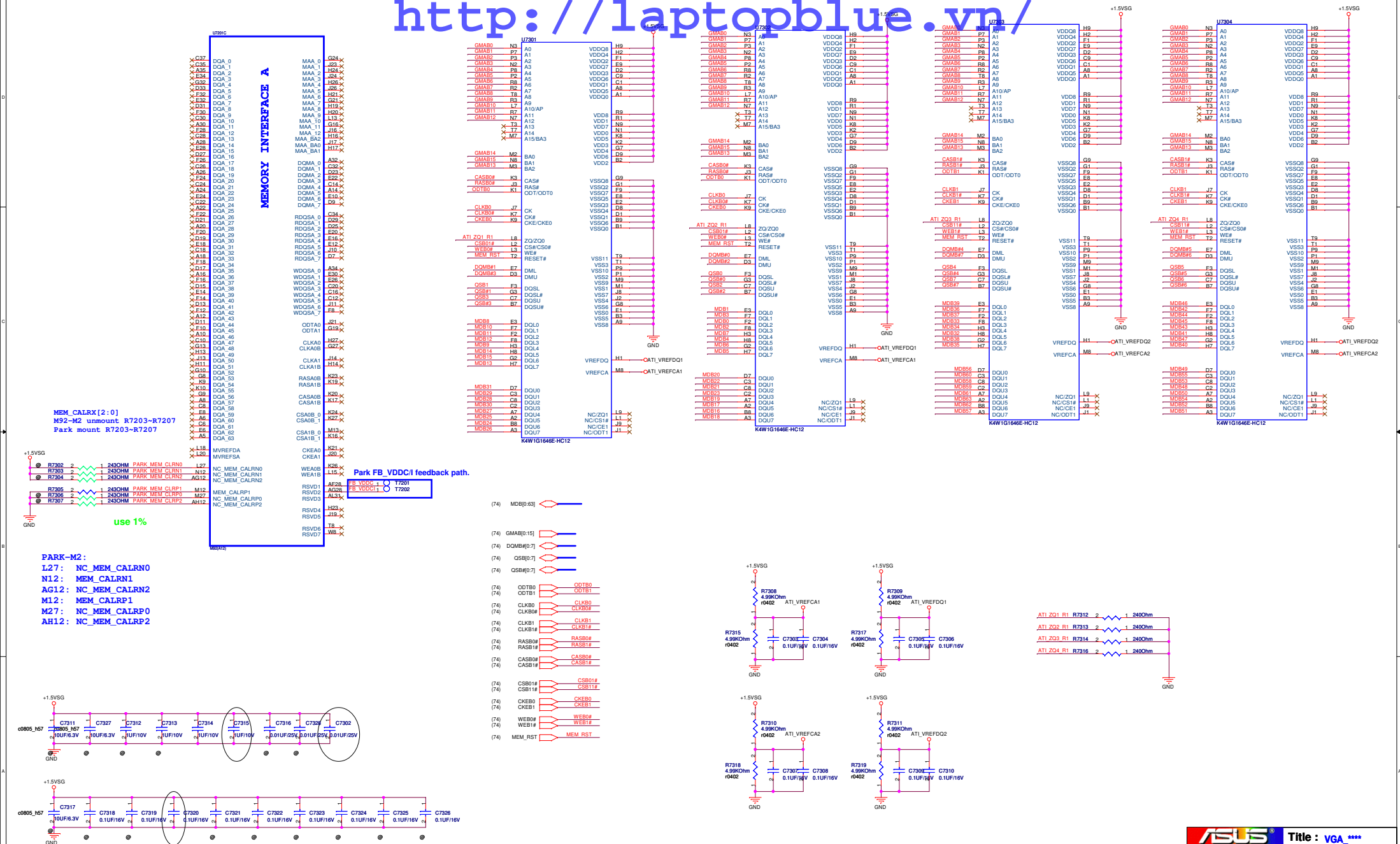
Date: Thursday, November 12, 2009

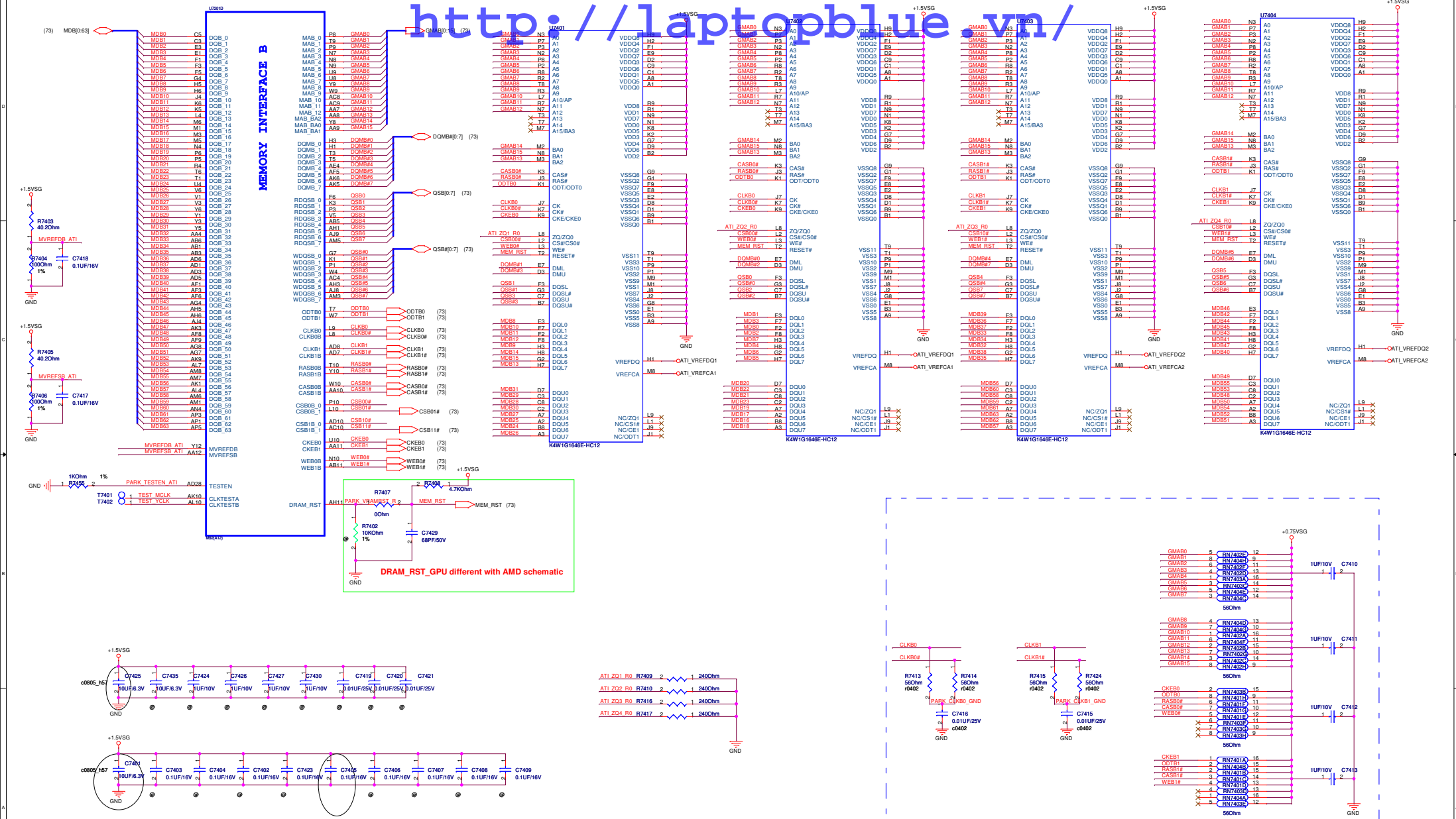
Sheet 70 of 96

http://laptopblue.vn/





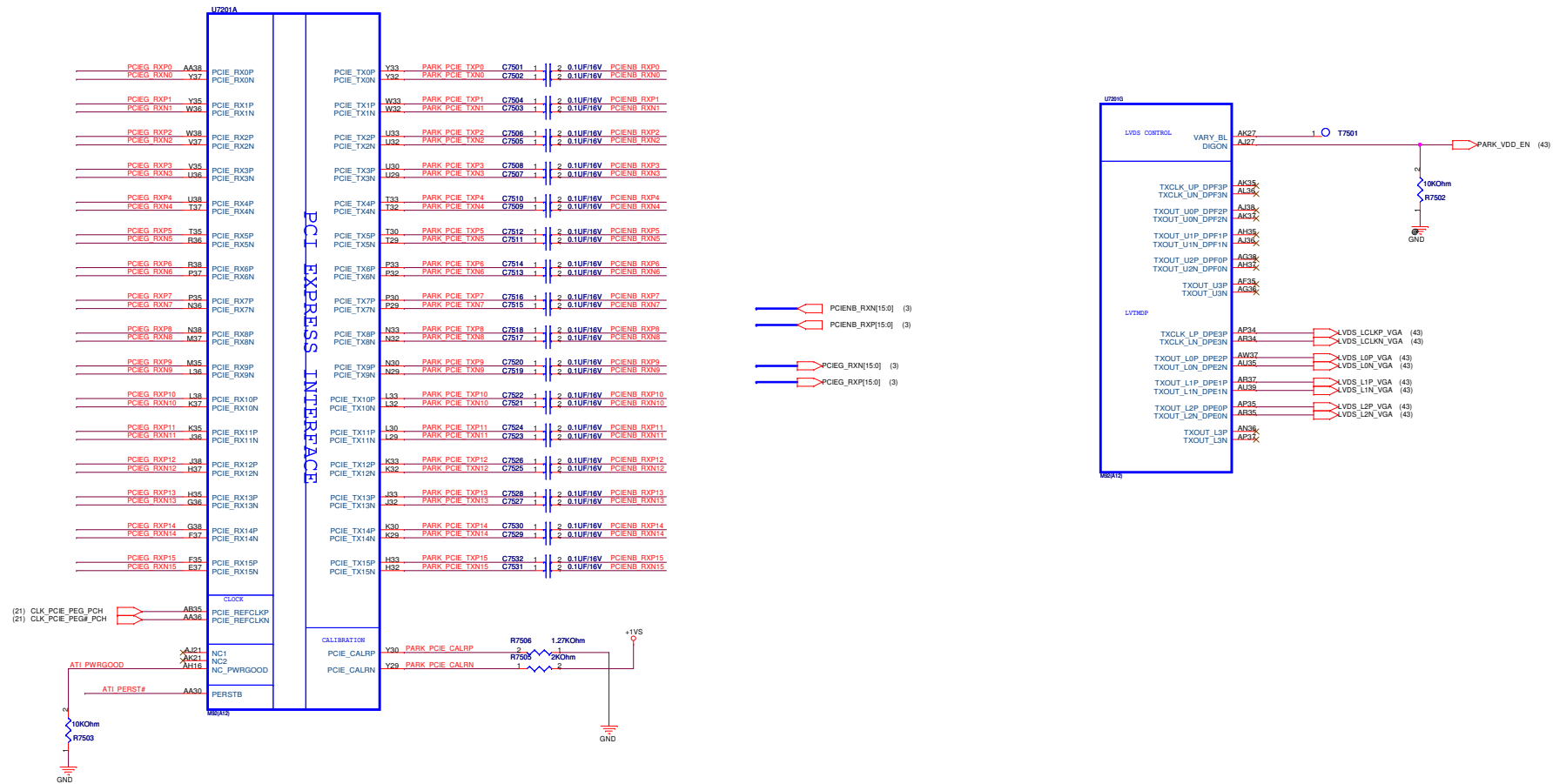




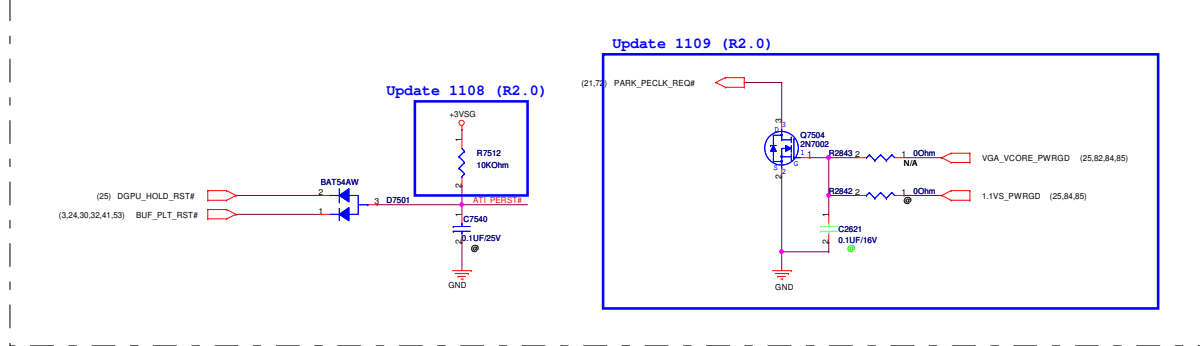
Dual RANK termination might be required.

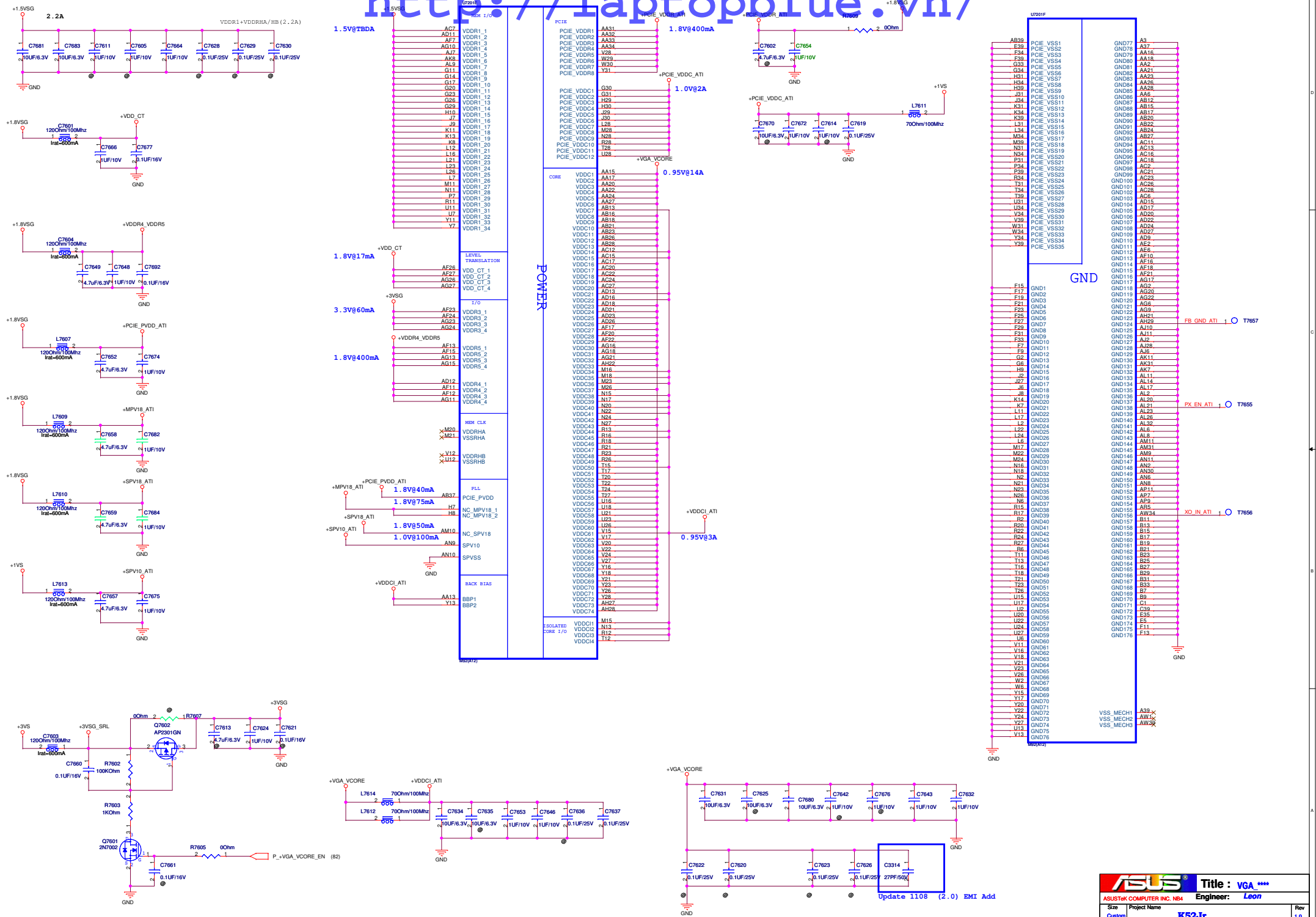
# PCI EXPRESS

<http://laptopblue.vn/>

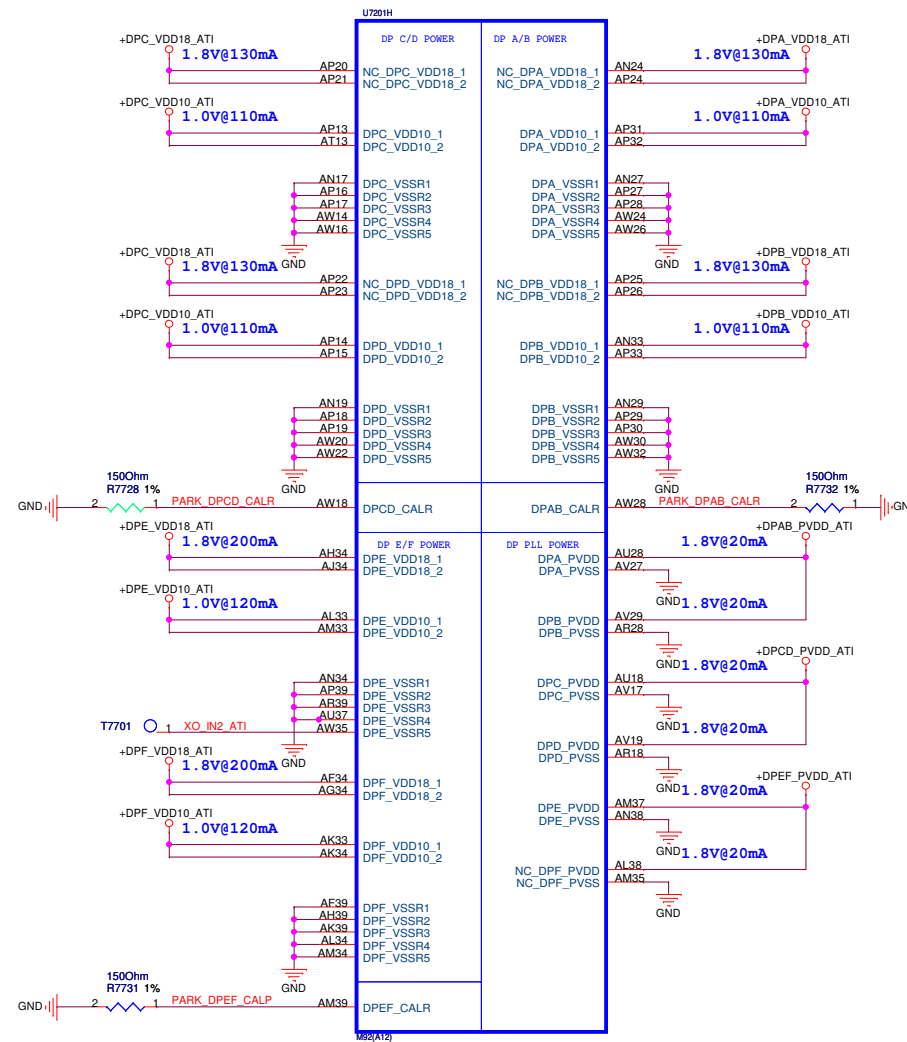


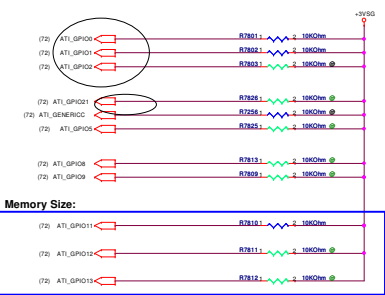
For switchable graphic





**http://laptopblue.vn/**

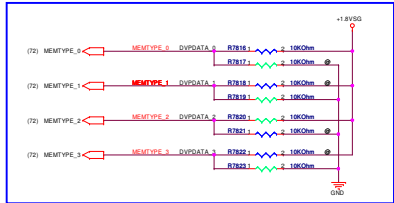




## Audio function:



## Memory Type:



Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM  
 03G151638020 DDR3 64M\*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12  
 03G151638421 DDR3 64M\*16-1.2 FBGA-96 HYNIX/H5TQ1G638FR-12C

Memory ID Board Straps				
Vendor	DVPDATA32(1,0)	ID	DDR Memory Type	Channel Size
Infineon (Gimonde)	0000	0	32M*16 (256Mb)	A channel(M0-M3)
	0001	1	32M*16 (512Mb)	2-A channel
	0010	2	64M*16 (512Mb)	A channel(M0-M3)
Samsung	0100	0	32M*16 (256Mb)	A channel(M0-M3)
	0101	1	64M*16 (512Mb)	2-A channel
	0110	2	32M*16 (256Mb)	A channel(M0-M3)
Hynix	1000	0	32M*16 (256Mb)	A channel(M0-M3)
	1001	1	64M*16 (512Mb)	2-A channel
	1010	2	32M*16 (256Mb)	A channel(M0-M3)
Elpida	1100	0	32M*16 (256Mb)	A channel(M0-M3)
	1101	1	64M*16 (512Mb)	2-A channel
	1110	2	32M*16 (256Mb)	A channel(M0-M3)

Memory ID Board Straps				
Vendor	DVPDATA32(1,0)	ID	DDR Memory Type	Channel Size
Oimonde	0000	0	32M*16 (256Mb)	B channel
	0001	1	32M*16 (512Mb)	B channel dual link
	0010	2	64M*16 (512Mb)	B channel
Samsung	0100	0	32M*16 (256Mb)	B channel
	0101	1	64M*16 (512Mb)	B channel dual link
	0110	2	32M*16 (256Mb)	B channel
Hynix	1000	0	32M*16 (256Mb)	B channel
	1001	1	64M*16 (512Mb)	B channel dual link
	1010	2	32M*16 (256Mb)	B channel
Elpida	1100	0	32M*16 (256Mb)	B channel
	1101	1	64M*16 (512Mb)	B channel dual link
	1110	2	32M*16 (256Mb)	B channel

TX_PWRIS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing. 1: The setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express - Mobile Graphics Low-Power Addendum). 1: Full Tx output swing.	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express - Mobile Graphics Low-Power Addendum). Otherwise: 1: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor.
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express - Mobile Graphics Low-Power Addendum). 1: Tx de-emphasis enabled.	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express - Mobile Graphics Low-Power Addendum). Otherwise: 1: Must be pulled to 3.3 V at reset using ~3-K (5%) resistor (e.g. MCM and add-in boards).
BF_0EN2_EN_A	GPIO_2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.  Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).	0 (Internal pull-down)	0 5.0 GT/s capability will be controlled by software.
VGA_DIS	GPIO_9_ROMSI	VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller.	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
CONFIO[2] CONFIO[1] CONFIO[0]	GPIO_13 GPIO_12 GPIO_11	a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. See " <i>ROM Configurations</i> " on page 3-33. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. See " <i>Primary Memory Aperture size requested at PCI Configuration</i> " on page 3-33.	0 (Internal pull-down)	Design dependent. See description for more information.

BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0: Disable external BIOS ROM device 1: Enable external BIOS ROM device  Note that when an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	0 (Internal pull-down)	Design dependent. See description for more information.
AUD[1] AUD[0]	H2SYNC V2SYNC	AUD[1:0] 00: No audio function; 01: Audio for DisplayPort only; 10: Audio for DisplayPort and HDMI if dongle is detected; 11: Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	0 (Internal pull-down)	Design dependent. See description for more information.
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host Interface. 0: Driver would ignore the value sampled on VHAD_0 during reset. 1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, VHAD_0 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card.  Note: If the strap is needed, it must be placed between the ball and the V2SYNC output buffer. This output buffer prevents monitors from affecting the value at reset.	0 (Internal pull-down)	Design dependent. See description for more information.

## RESERVED CONFIGURATION STRAPS

Allow for pull-up pads for these straps and if these GPIOs are used, they must not conflict during reset

RESERVED	H2SYNC	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
----------	--------	--	---------------------------	---

Pull-up pads are not required for these straps but if these GPIOs are used, they must not conflict during reset.

RESERVED	GPIO_8_ROMSO GPIO_21_BB_EN	Internal use only. THESE PADS HAVE INTERNAL PULL-DOWNS AND MUST BE 0 V AT RESET. These pads may be left unconnected, however, if they are connected to additional logic on the board, the logic must not allow these signals to be driven or pulled to any value except GND at reset.	0 (Internal pull-down)	No PAD required. Ensure that no logic conflicts with these signals during Reset.
----------	-------------------------------	---	---------------------------	--

64 MB	010
32 MB	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

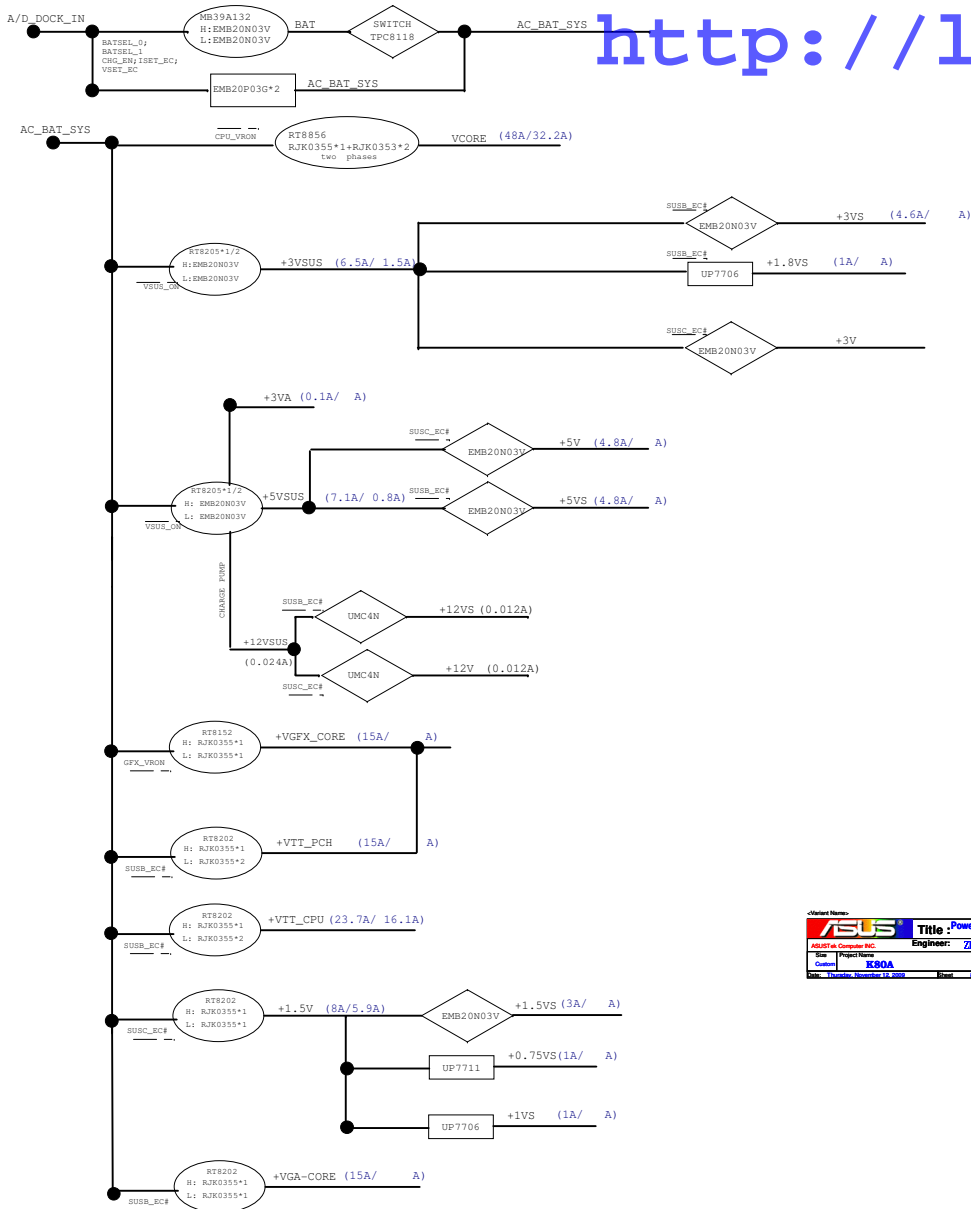
POWERPLAY Interface				
Pin Name	Type	PDPV	Description	
GPIO_15_PWRCNTL_0 GPIO_16_SSN GPIO_20_PWRCNTL_1	I/O VDDR3	PC-resist	GPIO_15_PWRCNTL_0 is an optional pin that allows the system to request a fast power reduction by setting GPIO_15_PWRCNTL_0 to low (0V). The resulting state transition may disturb the display momentarily.  Power reductions that are less time critical should use the standard software methods only in order to prevent display disturbances.  Voltage control signals for the core VDDC and VDDCI. At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define all voltage control signals to be either 3.3V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PowerPlay state.  (Optional) Voltage control signal for memory voltage regulator. Note that this signal must be low (0 V) at reset (failure to do so will prevent booting).	
GPIO_21_BB_EN	I/O			

CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS X = DO NOT INSTALL RESISTOR + = INSTALL IN RESISTOR - = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRIS_ENB	GPIO0	PCI FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS ENABLED	X
RESERVED	GPIO8	RESERVED	0
RESERVED	GPIO21	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X X
ROMCFGQ[2:0]	GPIO[3:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RESERVED	H2SYNC	RESERVED	0
AUD[1]	GENERIC	RESERVED	0
AUD[0]	H2SYNC	RESERVED	0
V2SYNC	V2SYNC	SEE DATABOOK FOR DETAIL	X

AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
H2SYNC	GENERIC	GPIO2	GPIO1

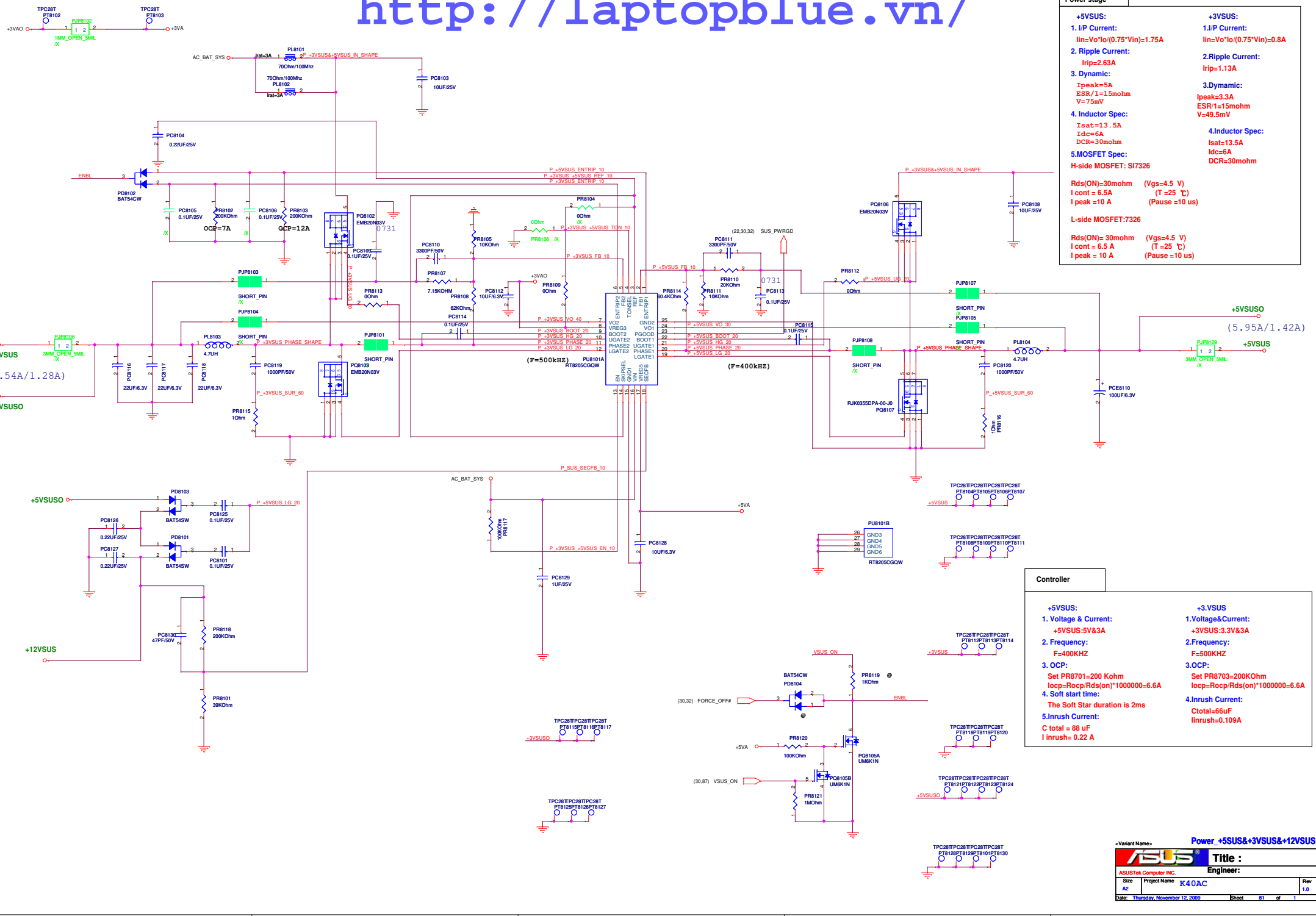
<http://laptopblue.vn/>

<http://laptopblue.vn/>



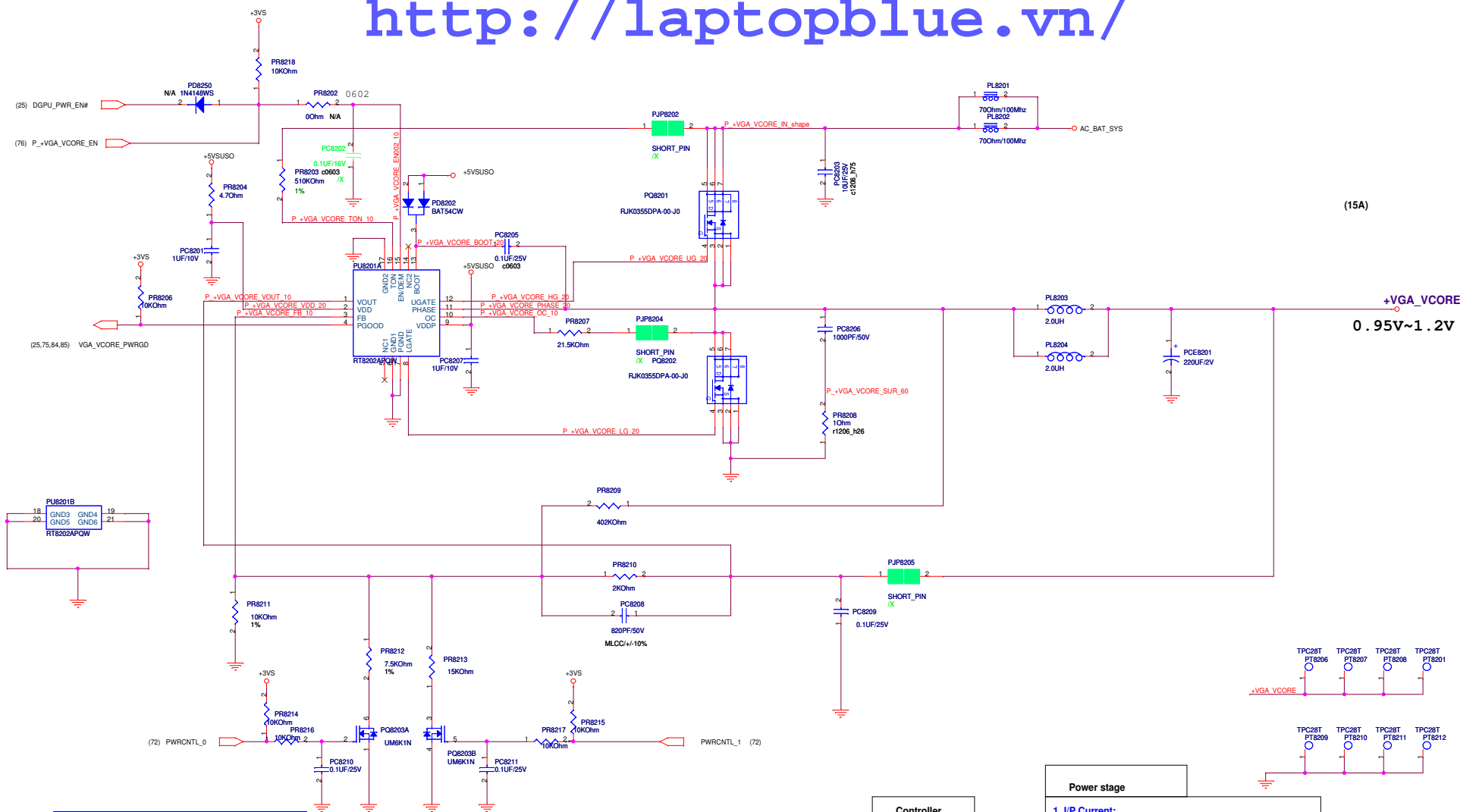
ASUS		Title: Power Flow	
ASUS Computer Inc.		Engineer: ZHA KIM LUU	
Date	Project Name	Rev	1.0
Checked	NOVA		
Date: 10/10/2018 10:00:00 AM			





Power stage	
<b>+5VSUS:</b> 1. I/P Current: $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 1.75A$ 2. Ripple Current: $I_{peak} = 5A$ $ESR / 1 = 1.5mohm$ $V = 75mV$ 3. Dynamic: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 4. Inductor Spec: $R_{ds(ON)} = 30mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 6.5A$ ( $T = 25^\circ C$ ) $I_{peak} = 10A$ (Pause = 10 us)	<b>+3VSUS:</b> 1. I/P Current: $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 0.8A$ 2. Ripple Current: $I_{rip} = 1.13A$ 3. Dynamic: $I_{peak} = 3.3A$ $ESR / 1 = 15mohm$ $V = 49.5mV$ 4. Inductor Spec: $R_{ds(ON)} = 30mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 6.5A$ ( $T = 25^\circ C$ ) $I_{peak} = 10A$ (Pause = 10 us)

Controller	
<b>+5VSUS:</b> 1. Voltage & Current: $+5VSUS: 5V \& 3A$ 2. Frequency: $F = 400KHZ$ 3. OCP: $Set PR8701 = 200Kohm$ $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Soft start time: The Soft Star duration is 2ms 5. Inrush Current: $C_{total} = 88uF$ $I_{inrush} = 0.22A$	<b>+3VSUS:</b> 1. Voltage & Current: $+3VSUS: 3.3V \& 3A$ 2. Frequency: $F = 500KHZ$ 3. OCP: $Set PR8703 = 200Kohm$ $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1000000 = 6.6A$ 4. Inrush Current: $C_{total} = 66uF$ $I_{inrush} = 0.109A$



(15A)

+VGA\_VCORE  
0.95V~1.2V

PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	0.9	-5%
0	1	1.0	Normal
1	0	1.1	+5%
1	1	1.2	+10%

#### Controller

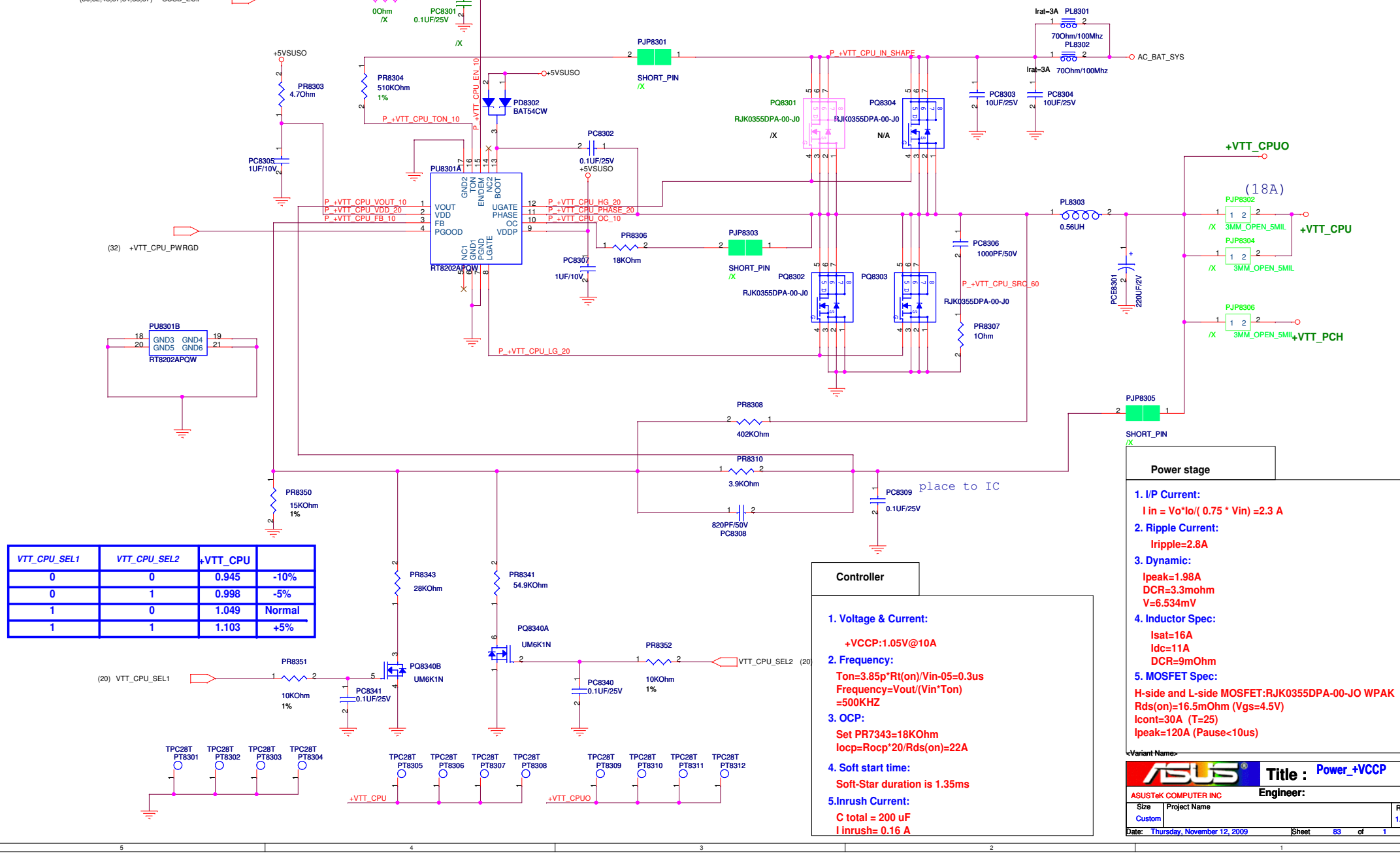
- 1. Voltage & Current:**  
+1.2VSUS: 16A
- 2. Frequency:**  
 $T_{on} = 3.85p \cdot R_{t(on)} / V_{in} - 0.5 = 0.3us$   
Frequency =  $V_{out} / (V_{in} \cdot T_{on}) = 500KHZ$   
Set PR8107=21.5kohm  
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)} = 26A$
- 4. Soft start time:**  
Soft-Star duration is 1.35ms
- 5. Inrush Current:**  
C total = 220uF  
I inrush = 0.163A

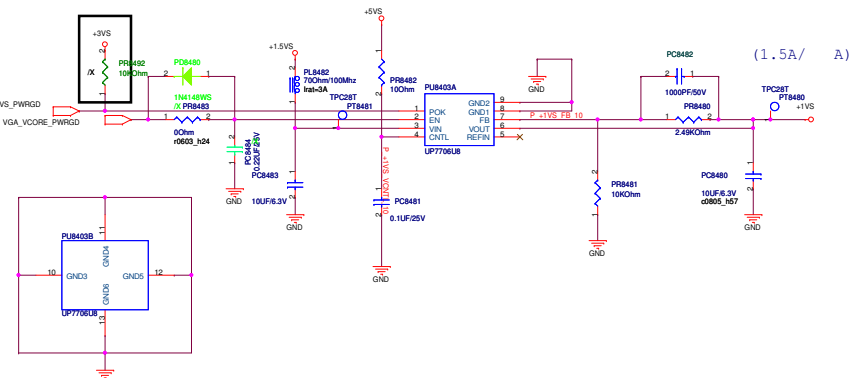
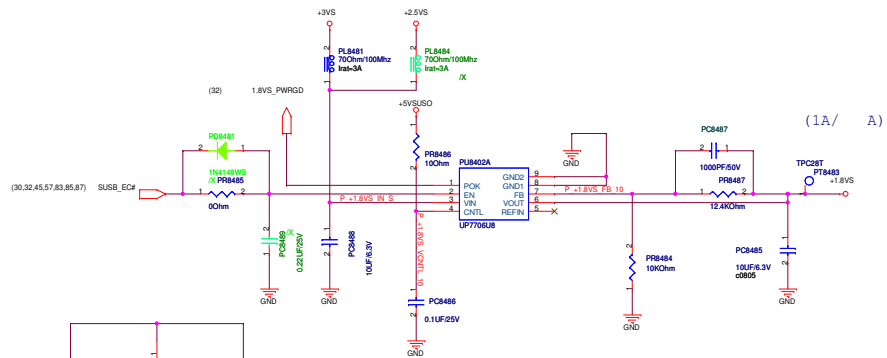
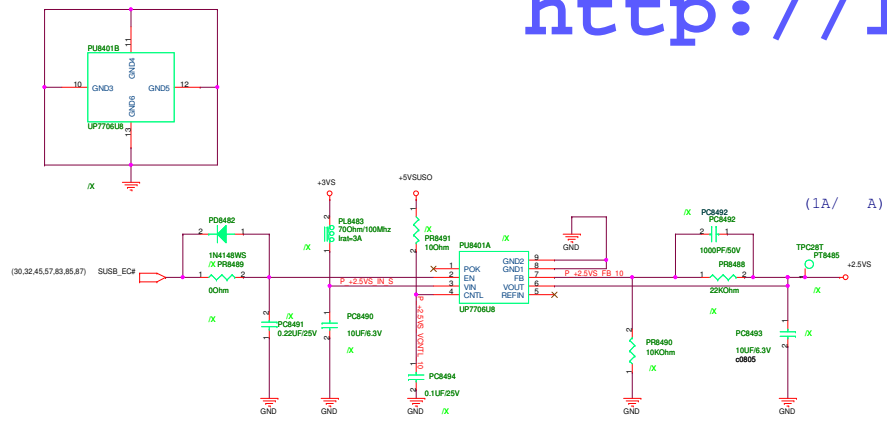
#### Power stage

- 1. I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.85A$
- 2. Ripple Current:**  
Iripple = 3.74A
- 3. ripple voltage:**  
 $I_{peak} = (V_{in} - V_o) \cdot D / (L \cdot F_{sw}) = 2.07A$   
DCR = 3.3mohm  
 $V = 6.831mV$
- 4. Inductor Spec:**  
 $I_{sat} = 25A$   
 $I_{dc} = 15.5A$   
DCR = 5.5mohm
- 5. MOSFET Spec:**  
H-side and L-side MOSFET:  
 $R_{ds(on)} = 16.5m\Omega$  (Vgs=4.5V)  
 $I_{cont} = 30A$  (T=25)  
 $I_{peak} = 120A$  (Pause < 10us)

<Variant Name>

<b>ASUS</b>		<b>Title : Power_+VGA_VCORE</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
C	Oemga	1.0	
Date: Thursday, November 12, 2009	Sheet 82 of 1		





#### Controller

##### 1. Voltage & Current:

+1.8V/+1.8V&12A

##### 2. Frequency:

Ton=3.85p\* $R_{(on)}$ \*Vo/Vin-05  
Frequency=Vout/(Vin\*Ton)  
=500KHZ

##### 3. OCP:

Set PR7343=18kohm  
Iocp=Rocp\*20/Rds(on)  
=20\*1.5/16.5=26A

##### 4. Soft start time:

Soft-Start duration is 1.35ms

##### 5. Inrush Current:

C total =100uF

Inrush=0.133A

#### Power stage

##### 1. I/P Current:

$I_{in} = V_o/I_o/(0.8 * V_{in}) = 0.947A$

##### 2. Ripple Current:

Iripple=2.342A

##### 3. Ripple Voltage:

Ipeak=(vin-v0)\*D/(L\*Fsw)=3.25A  
DCR=3.3mohm  
V=10.75mV

##### 4. Inductor Spec:

Isat=36A  
Idc=18A  
DCR=3.3mohm

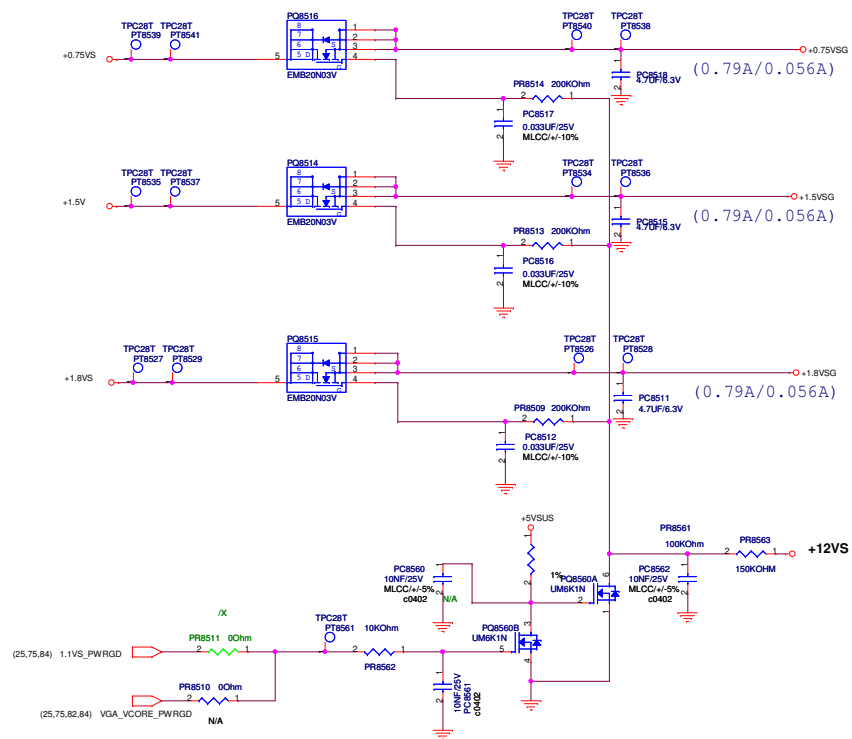
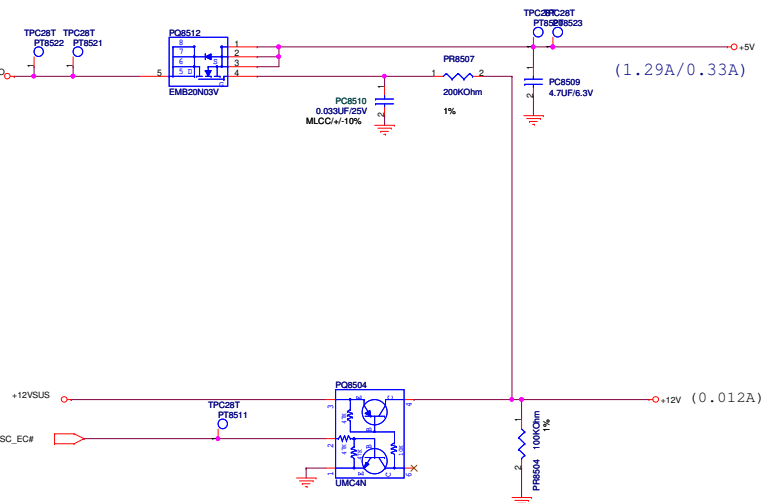
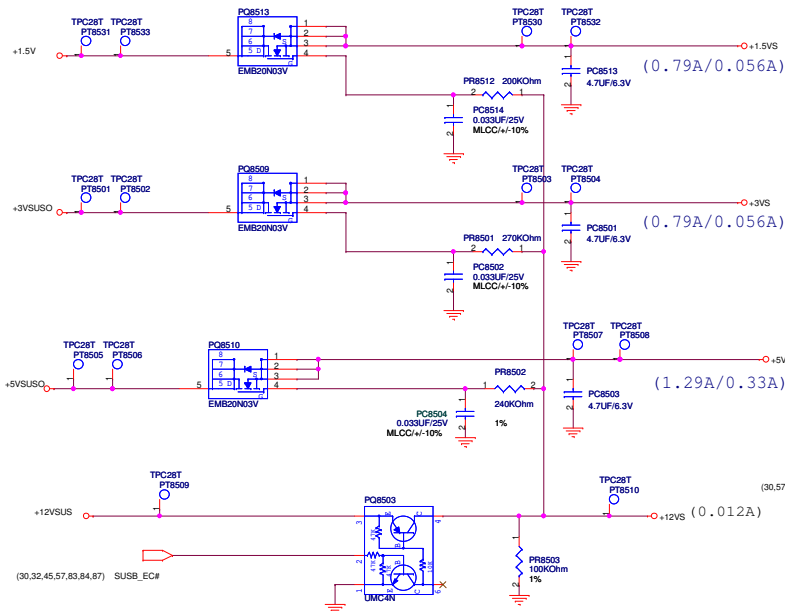
##### 5. MOSFET Spec:

H-side and L-side MOSFET:  
Rds(on)=16.5mohm (Vgs=4.5V)  
Icont=30A (T=25)  
Ipeak=120A (Pause<10us)

<Variant Name>

<b>ASUS</b>		<b>Title : Power +1.8V&amp;+0.9V</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Thursday, November 18, 2009	Sheet	84	of 1


SUSB#\_PWR POWER



<Variant Name>

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<Variant Name>



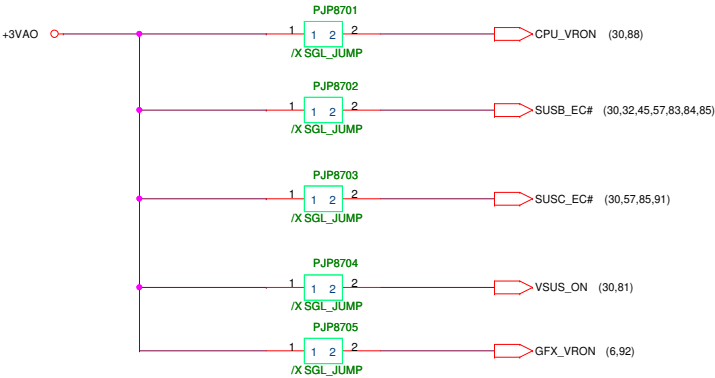
Title : **Power\_good\_detector**

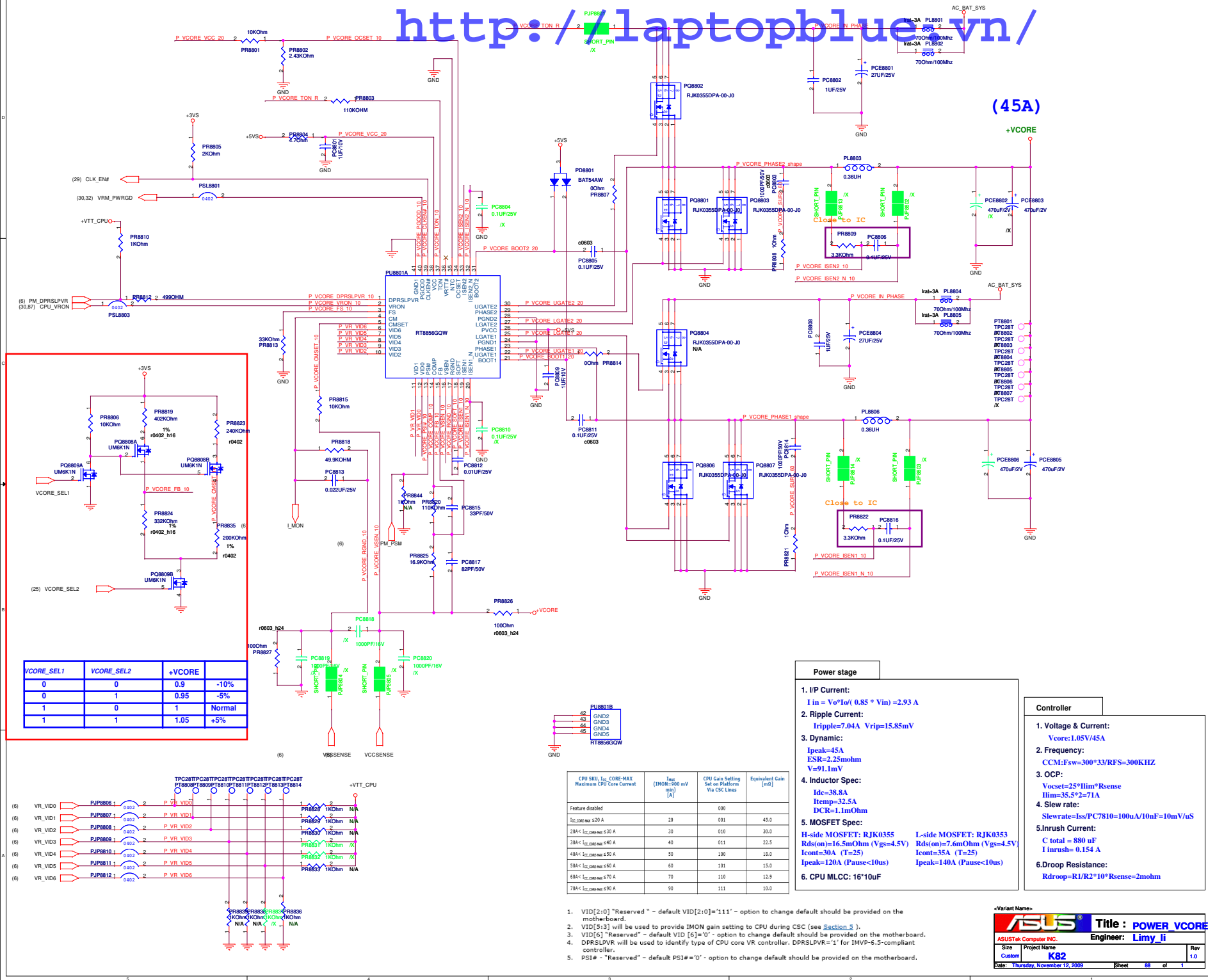
ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: **Thursday, November 12, 2009** Sheet **86** of **1**





### Power stage

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.85 \cdot V_{in}) = 2.93 \text{ A}$
- Ripple Current:**  
 $I_{ripple} = 7.04 \text{ A}$     $V_{ripple} = 15.85 \text{ mV}$
- Dynamic:**  
 $I_{peak} = 45 \text{ A}$   
 $ESR = 2.25 \text{ mohm}$   
 $V = 91 \text{ mV}$
- Inductor Spec:**  
 $I_{dc} = 38.8 \text{ A}$   
 $I_{temp} = 32.5 \text{ A}$   
 $DCR = 1 \text{ mOhm}$
- MOSFET Spec:**  
H-side MOSFET: RJK0355  
 $R_{ds(on)} = 16.5 \text{ mOhm}$  ( $V_{gs} = 4.5 \text{ V}$ )  
 $I_{cont} = 30 \text{ A}$  ( $T = 25$ )  
 $I_{peak} = 120 \text{ A}$  (Pause < 10us)  
L-side MOSFET: RJK0353  
 $R_{ds(on)} = 7.6 \text{ mOhm}$  ( $V_{gs} = 4.5 \text{ V}$ )  
 $I_{cont} = 35 \text{ A}$  ( $T = 25$ )  
 $I_{peak} = 140 \text{ A}$  (Pause < 10us)
- CPU MLCC: 16\*10uF**

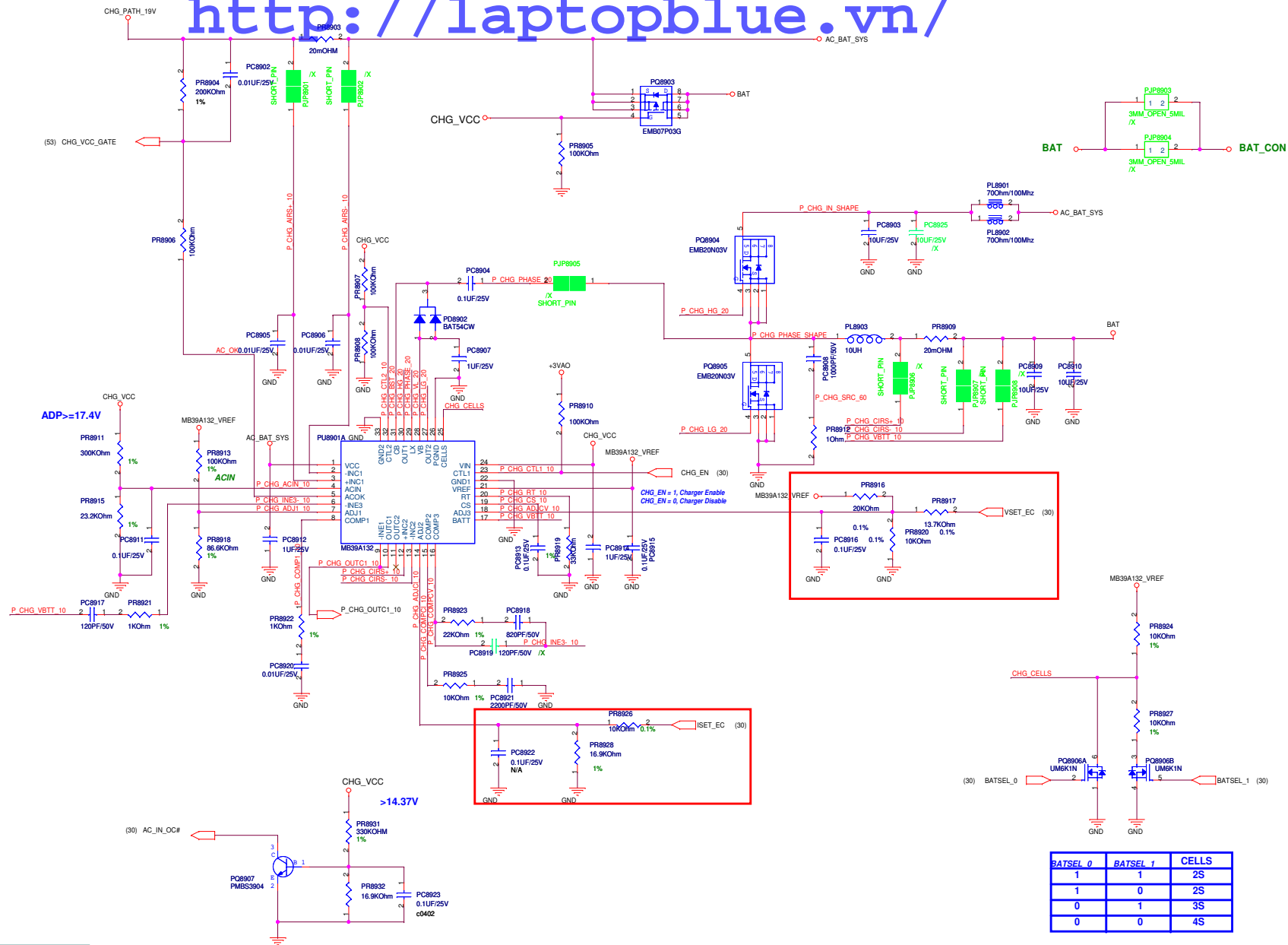
### Controller

- Voltage & Current:**  
 $V_{core} = 1.05 \text{ V} / 45 \text{ A}$
- Frequency:**  
 $CCM: F_{sw} = 300 \cdot 33 / R_{FS} = 300 \text{ KHZ}$
- OCP:**  
 $V_{ocst} = 25 \cdot I_{lim} \cdot R_{sense}$   
 $I_{lim} = 35.5 \cdot 2 = 71 \text{ A}$
- Slew rate:**  
 $Slewrate = I_{ss} / PC7810 = 100 \text{ uA} / 10 \text{ nF} = 10 \text{ mV/uS}$
- Inrush Current:**  
 $C_{total} = 880 \text{ uF}$   
 $I_{inrush} = 0.154 \text{ A}$
- Droop Resistance:**  
 $R_{droop} = R1 / R2 \cdot 10 \cdot R_{sense} = 2 \text{ mohm}$

CPU SKU	I <sub>cc</sub> CORE-MAX	I <sub>cc</sub>	CPU Gain Setting	Equivalent Gain
Maximum CPU Core Current	(10mV=900 mV min)	[A]	Set on Platform Via CSC Lines	[m]
Feature disabled			000	
50A < I <sub>cc</sub> < 60A	30	001		45.0
30A < I <sub>cc</sub> < 50A	30	010		30.0
40A < I <sub>cc</sub> < 50A	40	011		22.5
40A < I <sub>cc</sub> < 50A	50	100		18.0
50A < I <sub>cc</sub> < 60A	60	101		15.0
60A < I <sub>cc</sub> < 70A	70	110		12.9
70A < I <sub>cc</sub> < 80A	80	111		10.0

- VID[2:0] "Reserved" - default VID[2:0]="111" - option to change default should be provided on the motherboard.
- VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 3).
- VID[6] "Reserved" - default VID [6] = "0" - option to change default should be provided on the motherboard.
- DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR="1" for IMVP-5.5-compliant controller.
- PSI# - "Reserved" - default PSI#="0" - option to change default should be provided on the motherboard.





1. Adapter Threshold: 17.41V  
 $17.41 = (PR9213 + PR9216) / PR9216 * 1.25$
2. AP4835 ID=9.2A
3. MB39A132\_VREF= 5.0V
4. Input limit:  
65W:  $I_{limit\_current} = (V_{adj} - 1.075) / (25 * R_s) = (1.646 - 0.075) / 25 * 0.02 = 3.14A$   
330K-162K  
90W: 100K-86.6K :  $I_{limit\_current} = 4.49A$

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	3.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:  
 $f_{osc}(KHz) = 17000 / RT (KOhm)$   
 $f_{osc}(KHz) = 17000 / 33K = 515KHz$
2. OCP:  
 $I_{oc} = 0.2 / R_s = 10A$
3. Soft start time:  
 $t_s(s) = 0.26 * CS(uF) * 0.26 * 0.1 = 26ms$
4. Inrush current(3S):  
 $I_{inrush} = C * V / t = 9.7mA$

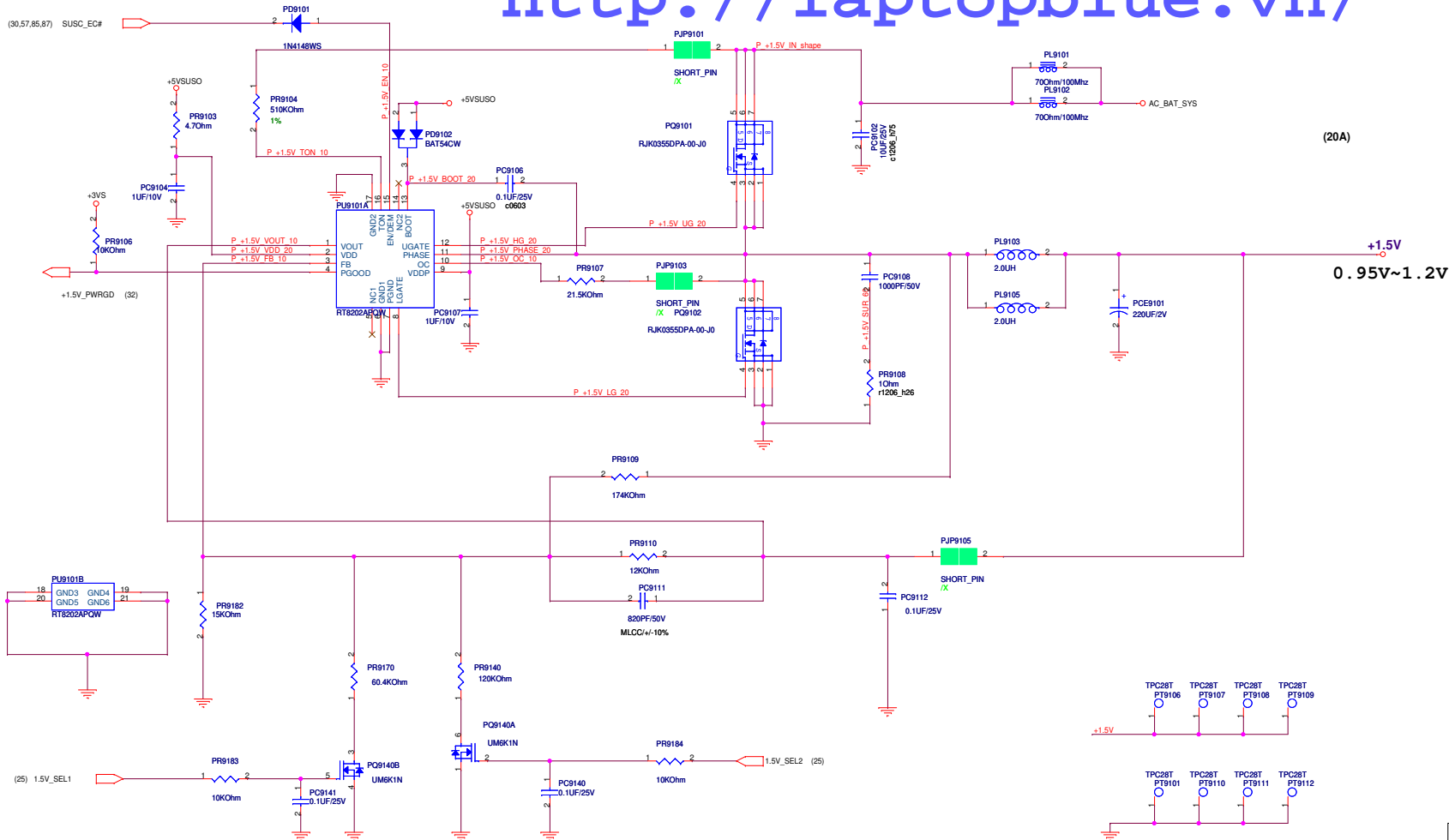
Power stage

1. I/P Current(3S2P):  
 $I_{in} = V_o * I_o / (0.75 * V_{in}) = 2.21A$
2. Ripple Current(3S2P):  
 $I_{ripple} = 1.18A$
3. Inductor Spec:  
 $I_{sat} = 4.4A$   
 $I_{dc} = 3.8A$   
 $DCR = 35mohm$
4. MOSFET Spec:  
 $I_{dc} = 6.5A / 5.0A$   
 $R_{dson} = 22 / 30mohm$   
 $V_{gsth} = 0.8 - 1.8V$

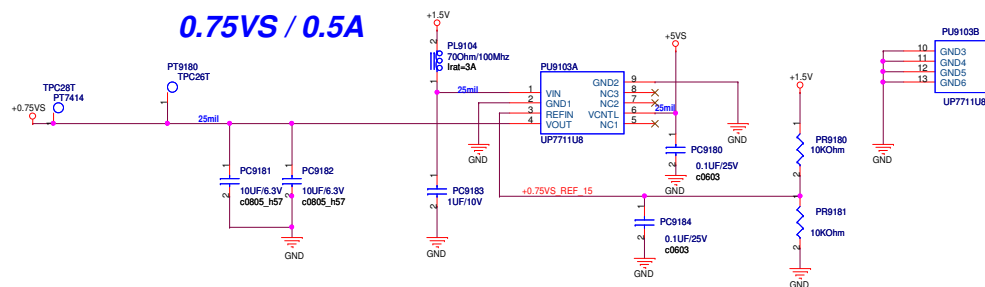
EC Code: 202

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**0.75VS / 0.5A**



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

### Controller

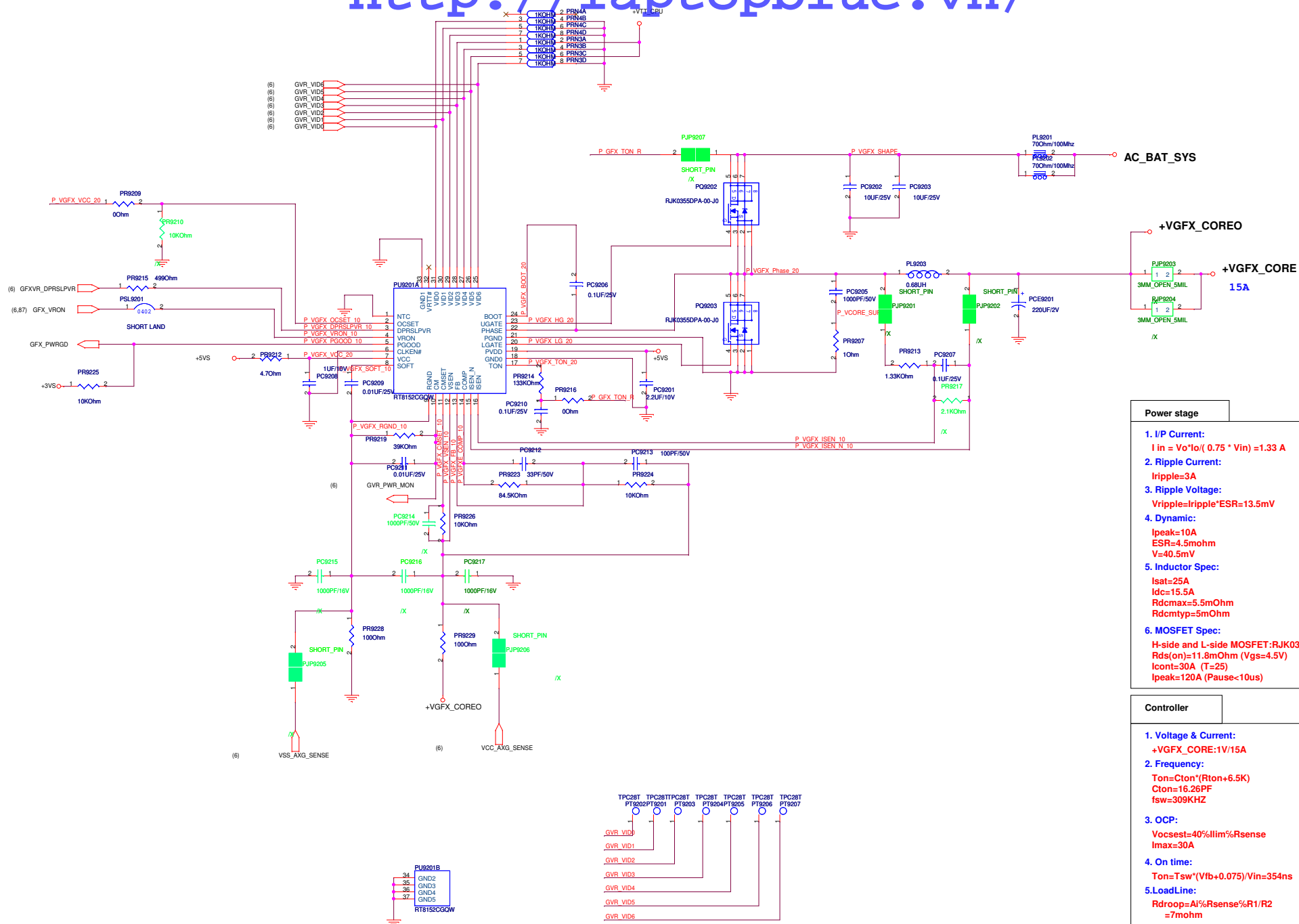
- 1. Voltage & Current:**  
+1.2VSUS: 16A
- 2. Frequency:**  
 $Ton = 3.85 \mu s \cdot R_t(ON) / Vin - 0.5 = 0.3 \mu s$   
 $Frequency = Vout / (Vin \cdot Ton) = 500KHZ$
- 3. OCP:**  
Set  $PR8107 = 21.5k\Omega$   
 $I_{OCP} = R_{OCP} \cdot I_{RDS(ON)} = 26A$
- 4. Soft start time:**  
Soft-Star duration is 1.35ms
- 5. Inrush Current:**  
C total = 220uF  
 $I_{inrush} = 0.163A$

### Power stage

- 1. I/P Current:  
 $I_{in} = V_o I_o / (0.75 \times V_{in}) = 0.85A$
- 2. Ripple Current:  
ripple=3.74A
- 3.ripple voltage:  
 $I_{peak} = (v_{in} - v_o) D / (L \times F_{sw}) = 2.07A$   
DCR=3.3mohm  
 $V = 6.831mV$
- 4. Inductor Spec:  
 $I_{sat} = 25A$   
IDC=15.5A  
 $V = 5.5mohm$
- 5. MOSFET Spec:  
H-side and L-side MOSFET:  
 $R_{ds(on)} = 16.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25$ )  
 $I_{peak} = 120A$  (Pause=10us)

<Variant Name>



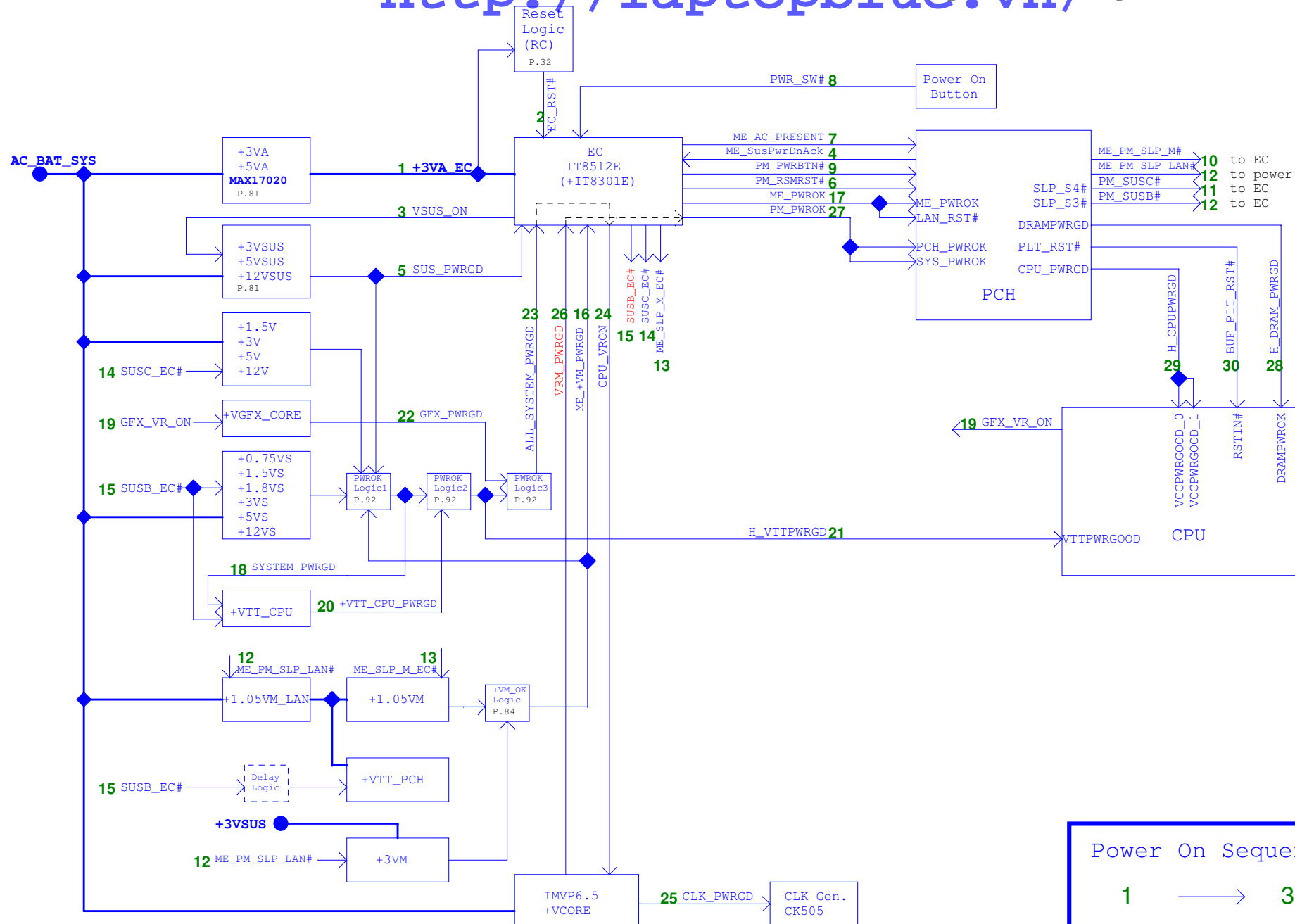


- Power stage**
- I/P Current:**  
 $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 1.33 \text{ A}$
  - Ripple Current:**  
 $I_{ripple} = 3 \text{ A}$
  - Ripple Voltage:**  
 $V_{ripple} = I_{ripple} \cdot ESR = 13.5 \text{ mV}$
  - Dynamic:**  
 $I_{peak} = 10 \text{ A}$   
 $ESR = 4.5 \text{ mohm}$   
 $V = 40.5 \text{ V}$
  - Inductor Spec:**  
 $I_{sat} = 25 \text{ A}$   
 $I_{dc} = 15.5 \text{ A}$   
 $R_{dcmax} = 5.5 \text{ mOhm}$   
 $R_{dcmtyp} = 5 \text{ mOhm}$
  - MOSFET Spec:**  
H-side and L-side MOSFET: RJK0355  
 $R_{ds(on)} = 11.8 \text{ mOhm}$  ( $V_{gs} = 4.5 \text{ V}$ )  
 $I_{cont} = 30 \text{ A}$  ( $T = 25$ )  
 $I_{peak} = 120 \text{ A}$  (Pause  $< 10 \mu\text{s}$ )

- Controller**
- Voltage & Current:**  
 $+VGFX\_CORE: 1 \text{ V}/15 \text{ A}$
  - Frequency:**  
 $T_{on} = C_{ton} \cdot (R_{ton} + 6.5 \text{ K})$   
 $C_{ton} = 16.26 \text{ PF}$   
 $f_{sw} = 309 \text{ KHZ}$
  - OCP:**  
 $V_{ocset} = 40\% I_{lim} \cdot R_{sense}$   
 $I_{max} = 30 \text{ A}$
  - On time:**  
 $T_{on} = T_{sw} \cdot (V_{fb} + 0.075) / V_{in} = 354 \text{ ns}$
  - Load Line:**  
 $R_{droop} = A_i \cdot R_{sense} \cdot R1 / R2$   
 $\approx 7 \text{ mohm}$

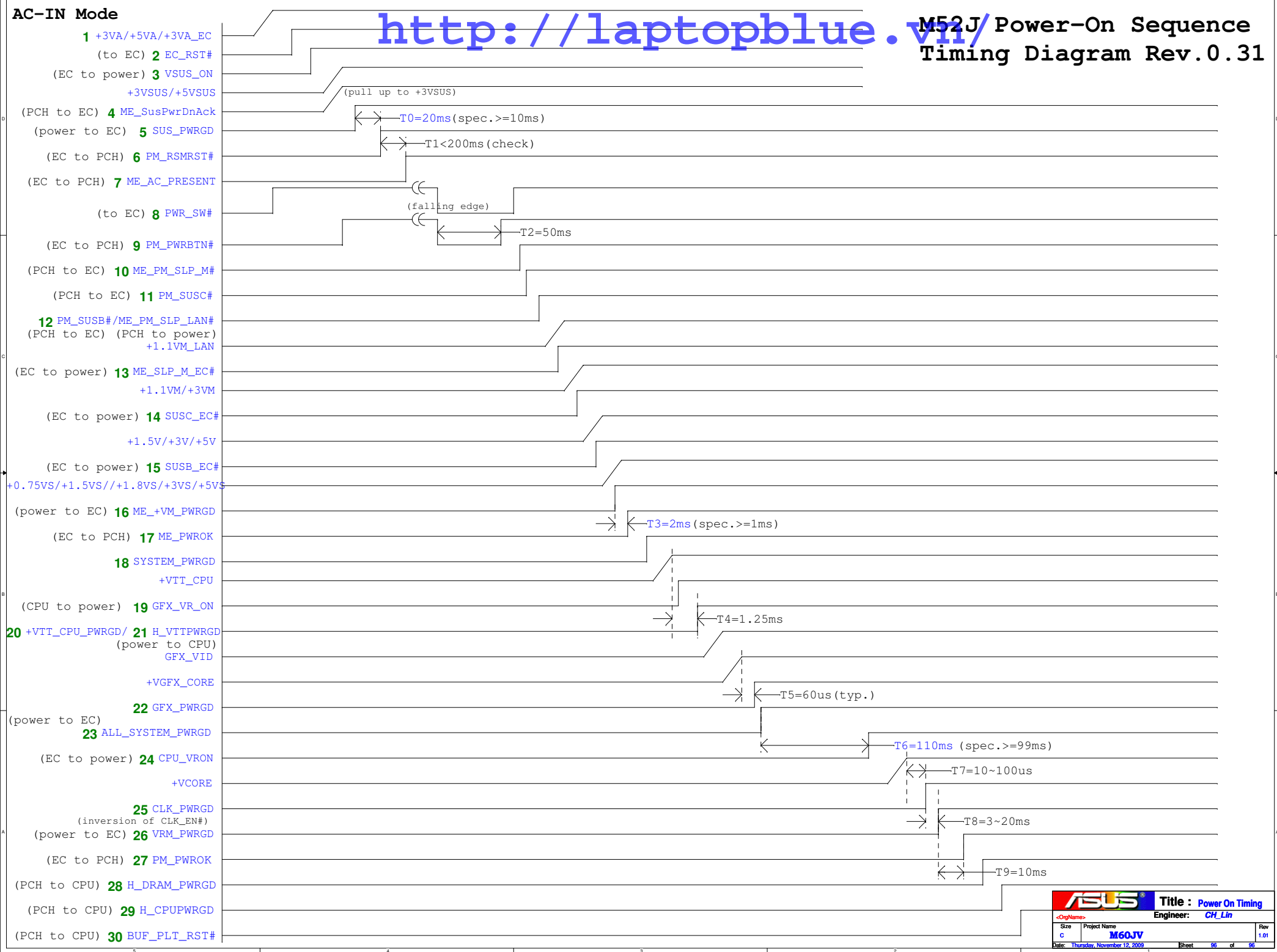
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# M52J Power-On Sequence Timing Diagram Rev.0.31





DC-IN Mode

- 1 +3VA/+5VA/+3VA\_EC  
(to EC) 2 EC\_RST#  
(to EC) 3 PWR\_SW#
- (EC to power) 4 VSUS\_ON  
+3VSUS/+5VSUS  
(PCH to EC) 5 ME\_SusPwrDnAck  
(power to EC) 6 SUS\_PWRGD  
(EC to PCH) 7 PM\_RSMRST#  
(EC to PCH) 8 ME\_AC\_PRESENT  
(EC to PCH) 9 PM\_PWRBTN#  
(PCH to EC) 10 ME\_PM\_SLP\_M#  
(PCH to EC) 11 PM\_SUSC#  
12 PM\_SUSB#/ME\_PM\_SLP\_LAN#  
(PCH to EC) (PCH to power)  
+1.1VM\_LAN  
(EC to power) 13 ME\_SLP\_M\_EC#  
+1.1VM/+3VM  
(EC to power) 14 SUSC\_EC#  
+1.5V/+3V/+5V  
(EC to power) 15 SUSB\_EC#  
+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS  
(power to EC) 16 ME\_+VM\_PWRGD  
(EC to PCH) 17 ME\_PWROK  
18 SYSTEM\_PWRGD  
+VTT\_CPU  
(CPU to power) 19 GFX\_VR\_ON  
20 +VTT\_CPU\_PWRGD/ 21 H\_VTTPWRGD  
(power to CPU)  
GFX\_VID  
+VGFX\_CORE  
22 GFX\_PWRGD  
(power to EC)  
23 ALL\_SYSTEM\_PWRGD  
(EC to power) 24 CPU\_VRON  
+VCORE  
25 CLK\_PWRGD  
(inversion of CLK\_EN#)  
(power to EC) 26 VRM\_PWRGD  
(EC to PCH) 27 PM\_PWROK  
(PCH to CPU) 28 H\_DRAM\_PWRGD  
(PCH to CPU) 29 H\_CPUPWRGD  
(PCH to CPU) 30 BUF\_PLT\_RST#

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M52J Power-On Sequence  
Timing Diagram Rev.0.31

