UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-08-16

REV : SB

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

<Core Design>

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Block Diagram (UMA/Optimus co-lay)

Project code : 91.4KZ01.001
PCB P/N : 48.4KZ01.0SB
Revision : 10250-SB

Audio BD
POWER BD
Finger Printer BD
IO BD (Cardreader+Audio+USB)
LED BD
USB

##OnMainBoard

VRAM 2GB/1GB/512MB 88,89,90,91
DDR3 800MHz
NVIDIA N12P-GE/GV N12M-GE 83.84,85,86,87
PCIe x 16 (Discrete only)

Intel CPU
Sandy Bridge
DDRIII: 1066/1333/1666 MHz 4,5,6,7,8,9,10
DDRIII 1066/1333/1666 Channel A
DDRIII 1066/1333/1666 Channel B
DDRIII Slot 0 1066/1333/1666 14
DDRIII Slot 1 1066/1333/1666 15

FDI x 4 x 2 (UMA only)
DMI x 4

HDMI 51
LCD 49
CRT 50
HDMI
LVDS
RGB CRT

Intel PCH Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25

Bluetooth 63
CAMERA 49
Finger Print BD
Finger Print 64
USB2.0 x 3
SD/MMC+/MS/MS Pro/xD 74
I/O BD
CardReader Realtek RTS5139
USB 2.0 x 1

PCIE x 1
GLAN RTL8111E 31
RJ45 CONN 55
PCIE x 1/USB2.0 x 1
Mini-Card WLAN 65
SATA x 1/USB2.0 x 1
Mini-Card WWAN 66
SIM 66
USB 2.0 x 3
MB USB x 3
USB 2.0 x 1/SATA x 1
E-SATA/USB comb 57
SATA x 2
HDD 56
ODD 56

AZALIA
Azalia CODEC Codec_ALC272 29
Internal DMIC
I/O BD
HP1
MIC IN
2CH SPEAKER

SPI
Flash ROM 4MB 60
LPC Bus
LPC debug port 71

KBC NUVOTON NPCE795G 27
SMBus
G-Sensor 79
Touch PAD 69
Int. KB 69
Thermal EMC2103-2-AP 28
Fan 28

SYSTEM DC/DC RT8208A 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51218 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8015B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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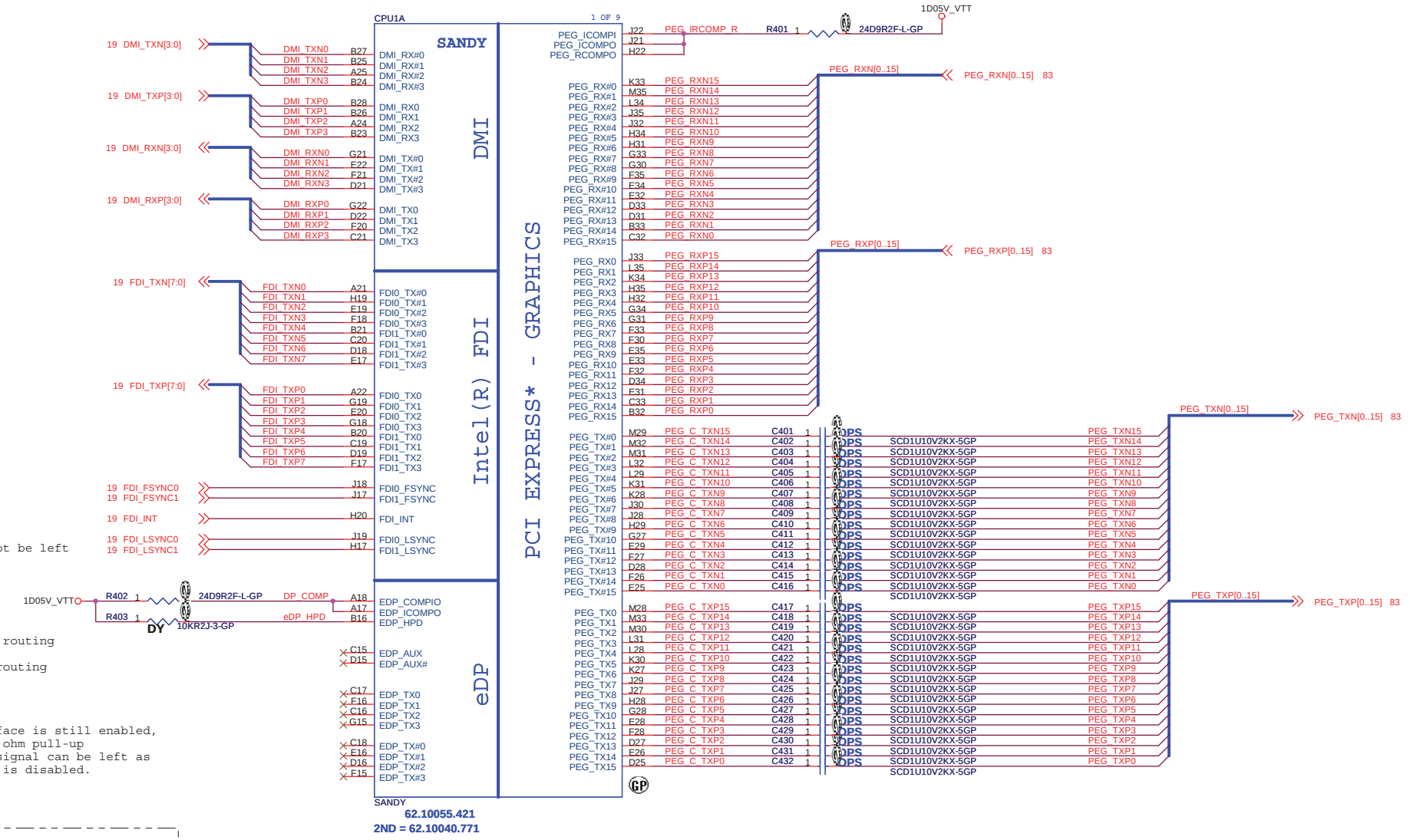
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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Title: CPU (PCIE/DMI/FDI)

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SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 CLK_DP_P_R CLK_DP_N_R 1D05V_VTT SRN1KJ-7-GP DY SB_0830

CPU1A SANDY

MISC
18 H_SNB_IVB# C26 SNB_IVB#
TPAD14-GP TP501 SKTOCC# R AN34 SKTOCC#

THERMAL
TPAD14-GP TP502 H_CATERR# AL33 CATERR#
22,27 H_PECI AN33 PECI
27,42 H_PROCHOT# R513 56R2J-4-GP H_PROCHOT# R AL32 PROCHOT#
22,36 H_THERMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
R503 10KR2J-3-GP H_CPUPWRGD_R
19 H_PM_SYNC AM34 PM_SYNC
11,22,36,97 H_CPUPWRGD R504 0R2J-2-GP H_CPUPWRGD_R AP33 UNCOREPWRGOOD
19,37 PM_DRAM_PWRGD R505 0R2J-2-GP DY VDDPWRGOOD V8 SM_DRAMPWROK
37 VDDPWRGOOD
BUF_CPU_RST# AR33 RESET#
TPAD14-GP TP518 VDDPWRGOOD

SANDY
62.10055.421
2ND = 62.10040.771

CLOCKS
BCLK A28 CLK_EXP_P 20
BCLK# A27 CLK_EXP_N 20
DPLL_REF_SSCLK A16 CLK_DP_P_R CLK_DP_P_R 20
DPLL_REF_SSCLK# A15 CLK_DP_N_R CLK_DP_N_R 20

DDR3 MISC
SM_DRAMRST# R8 R502 4K99R2F-L-GP SM_DRAMRST# 37
SM_RCOMP0 AK1 SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

JTAG & BPM
PRDY# AP29 XDP_PRDY# TP511 TPAD14-GP
PREQ# AP27 XDP_PREQ# TP512 TPAD14-GP
TCK AR26 XDP_TCLK TP513 TPAD14-GP
TMS AR27 XDP_TMS TP514 TPAD14-GP
TRST# AP30 XDP_TRST# TP515 TPAD14-GP
TDI AR28 XDP_TDI TP516 TPAD14-GP
TDO AP26 XDP_TDO TP517 TPAD14-GP
DBR# AL35 XDP_DBRESET#
BPM#0 AT28 XDP_BPM0 TP503 TPAD14-GP
BPM#1 AR29 XDP_BPM1 TP504 TPAD14-GP
BPM#2 AR30 XDP_BPM2 TP505 TPAD14-GP
BPM#3 AT30 XDP_BPM3 TP506 TPAD14-GP
BPM#4 AP32 XDP_BPM4 TP507 TPAD14-GP
BPM#5 AR31 XDP_BPM5 TP508 TPAD14-GP
BPM#6 AT31 XDP_BPM6 TP509 TPAD14-GP
BPM#7 AR32 XDP_BPM7 TP510 TPAD14-GP

SB_0820

1D05V_VTT RN501 XDP_TDO XDP_TMS XDP_TDI XDP_TCLK SRN51J-1-GP XDP_TRST# R511 51R2J-2-GP

3D3V_S0 22,36 XDP_DBRESET# XDP_DBRESET# R516 1KR2J-1-GP

11,18,27,31,36,65,66,71,83,97 PLT_RST# R510 1K5R2F-2-GP BUF_CPU_RST# R509 750R2F-GP

SB_0805

<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)

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SSID = CPU

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SANDY

DDR SYSTEM MEMORY A

14 M_A_DQ[63:0]

M_A_DQ0 C5 SA_DQ0
M_A_DQ1 D5 SA_DQ1
M_A_DQ2 D3 SA_DQ2
M_A_DQ3 D2 SA_DQ3
M_A_DQ4 D6 SA_DQ4
M_A_DQ5 C6 SA_DQ5
M_A_DQ6 C2 SA_DQ6
M_A_DQ7 C3 SA_DQ7
M_A_DQ8 F10 SA_DQ8
M_A_DQ9 F8 SA_DQ9
M_A_DQ10 G10 SA_DQ10
M_A_DQ11 G9 SA_DQ11
M_A_DQ12 F9 SA_DQ12
M_A_DQ13 F7 SA_DQ13
M_A_DQ14 G8 SA_DQ14
M_A_DQ15 G7 SA_DQ15
M_A_DQ16 K4 SA_DQ16
M_A_DQ17 K5 SA_DQ17
M_A_DQ18 K1 SA_DQ18
M_A_DQ19 J1 SA_DQ19
M_A_DQ20 J5 SA_DQ20
M_A_DQ21 J4 SA_DQ21
M_A_DQ22 J2 SA_DQ22
M_A_DQ23 K2 SA_DQ23
M_A_DQ24 M8 SA_DQ24
M_A_DQ25 N10 SA_DQ25
M_A_DQ26 N8 SA_DQ26
M_A_DQ27 N7 SA_DQ27
M_A_DQ28 M10 SA_DQ28
M_A_DQ29 M9 SA_DQ29
M_A_DQ30 N9 SA_DQ30
M_A_DQ31 M7 SA_DQ31
M_A_DQ32 AG6 SA_DQ32
M_A_DQ33 AG5 SA_DQ33
M_A_DQ34 AK6 SA_DQ34
M_A_DQ35 AK5 SA_DQ35
M_A_DQ36 AH5 SA_DQ36
M_A_DQ37 AH6 SA_DQ37
M_A_DQ38 AJ5 SA_DQ38
M_A_DQ39 AJ6 SA_DQ39
M_A_DQ40 AJ8 SA_DQ40
M_A_DQ41 AK8 SA_DQ41
M_A_DQ42 AJ9 SA_DQ42
M_A_DQ43 AK9 SA_DQ43
M_A_DQ44 AH8 SA_DQ44
M_A_DQ45 AH9 SA_DQ45
M_A_DQ46 AL9 SA_DQ46
M_A_DQ47 AL8 SA_DQ47
M_A_DQ48 AP11 SA_DQ48
M_A_DQ49 AN11 SA_DQ49
M_A_DQ50 AL12 SA_DQ50
M_A_DQ51 AM12 SA_DQ51
M_A_DQ52 AM11 SA_DQ52
M_A_DQ53 AL11 SA_DQ53
M_A_DQ54 AP12 SA_DQ54
M_A_DQ55 AN12 SA_DQ55
M_A_DQ56 AJ14 SA_DQ56
M_A_DQ57 AH14 SA_DQ57
M_A_DQ58 AL15 SA_DQ58
M_A_DQ59 AK15 SA_DQ59
M_A_DQ60 AL14 SA_DQ60
M_A_DQ61 AK14 SA_DQ61
M_A_DQ62 AJ15 SA_DQ62
M_A_DQ63 AH15 SA_DQ63

14 M_A_BS0 AE10 SA_BS0
14 M_A_BS1 AF10 SA_BS1
14 M_A_BS2 V6 SA_BS2

14 M_A_CAS# AE8 SA_CAS#
14 M_A_RAS# AD9 SA_RAS#
14 M_A_WE# AF9 SA_WE#

SA_CLK0 AB6 M_A_DIM0_CLK_DDR0 14
SA_CLK#0 AA6 M_A_DIM0_CLK_DDR#0 14
SA_CKE0 V9 M_A_DIM0_CKE0 14

SA_CLK1 AA5 M_A_DIM0_CLK_DDR1 14
SA_CLK#1 AB5 M_A_DIM0_CLK_DDR#1 14
SA_CKE1 V10 M_A_DIM0_CKE1 14

SA_CLK2 AB4
SA_CLK#2 AA4
SA_CKE2 W9

SA_CLK3 AB3
SA_CLK#3 AA3
SA_CKE3 W10

SA_CS#0 AK3 M_A_DIM0_CS#0 14
SA_CS#1 AL3 M_A_DIM0_CS#1 14
SA_CS#2 AG1
SA_CS#3 AH1

SA_ODT0 AH3 M_A_DIM0_ODT0 14
SA_ODT1 AG3 M_A_DIM0_ODT1 14
SA_ODT2 AG2
SA_ODT3 AH2

SA_DQS#0 C4 M_A_DQS#0
SA_DQS#1 G6 M_A_DQS#1
SA_DQS#2 J3 M_A_DQS#2
SA_DQS#3 M6 M_A_DQS#3
SA_DQS#4 AL6 M_A_DQS#4
SA_DQS#5 AM8 M_A_DQS#5
SA_DQS#6 AR12 M_A_DQS#6
SA_DQS#7 AM15 M_A_DQS#7
M_A_DQS#[7:0] 14

SA_DQS0 D4 M_A_DQS0
SA_DQS1 F6 M_A_DQS1
SA_DQS2 K3 M_A_DQS2
SA_DQS3 N6 M_A_DQS3
SA_DQS4 AL5 M_A_DQS4
SA_DQS5 AM9 M_A_DQS5
SA_DQS6 AR11 M_A_DQS6
SA_DQS7 AM14 M_A_DQS7
M_A_DQS[7:0] 14

SA_MA0 AD10 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 W2 M_A_A2
SA_MA3 W7 M_A_A3
SA_MA4 V3 M_A_A4
SA_MA5 V2 M_A_A5
SA_MA6 W3 M_A_A6
SA_MA7 W6 M_A_A7
SA_MA8 V1 M_A_A8
SA_MA9 W5 M_A_A9
SA_MA10 AD8 M_A_A10
SA_MA11 V4 M_A_A11
SA_MA12 W4 M_A_A12
SA_MA13 AF8 M_A_A13
SA_MA14 V5 M_A_A14
SA_MA15 V7 M_A_A15
M_A_A[15:0] 14

SANDY
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2ND = 62.10040.771

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SANDY

DDR SYSTEM MEMORY B

M_B_DQ[63:0]

M_B_DQ0 C9 SB_DQ0
M_B_DQ1 A7 SB_DQ1
M_B_DQ2 D10 SB_DQ2
M_B_DQ3 C8 SB_DQ3
M_B_DQ4 A9 SB_DQ4
M_B_DQ5 A8 SB_DQ5
M_B_DQ6 D9 SB_DQ6
M_B_DQ7 D8 SB_DQ7
M_B_DQ8 G4 SB_DQ8
M_B_DQ9 F4 SB_DQ9
M_B_DQ10 F1 SB_DQ10
M_B_DQ11 G1 SB_DQ11
M_B_DQ12 G5 SB_DQ12
M_B_DQ13 F5 SB_DQ13
M_B_DQ14 F2 SB_DQ14
M_B_DQ15 G2 SB_DQ15
M_B_DQ16 J7 SB_DQ16
M_B_DQ17 J8 SB_DQ17
M_B_DQ18 K10 SB_DQ18
M_B_DQ19 K9 SB_DQ19
M_B_DQ20 J9 SB_DQ20
M_B_DQ21 J10 SB_DQ21
M_B_DQ22 K8 SB_DQ22
M_B_DQ23 K7 SB_DQ23
M_B_DQ24 M5 SB_DQ24
M_B_DQ25 N4 SB_DQ25
M_B_DQ26 N2 SB_DQ26
M_B_DQ27 N1 SB_DQ27
M_B_DQ28 M4 SB_DQ28
M_B_DQ29 N5 SB_DQ29
M_B_DQ30 M2 SB_DQ30
M_B_DQ31 M1 SB_DQ31
M_B_DQ32 AM5 SB_DQ32
M_B_DQ33 AM6 SB_DQ33
M_B_DQ34 AR3 SB_DQ34
M_B_DQ35 AP3 SB_DQ35
M_B_DQ36 AN3 SB_DQ36
M_B_DQ37 AN2 SB_DQ37
M_B_DQ38 AN1 SB_DQ38
M_B_DQ39 AP2 SB_DQ39
M_B_DQ40 AP5 SB_DQ40
M_B_DQ41 AN9 SB_DQ41
M_B_DQ42 AT5 SB_DQ42
M_B_DQ43 AT6 SB_DQ43
M_B_DQ44 AP6 SB_DQ44
M_B_DQ45 AN8 SB_DQ45
M_B_DQ46 AR6 SB_DQ46
M_B_DQ47 AR5 SB_DQ47
M_B_DQ48 AR9 SB_DQ48
M_B_DQ49 AJ11 SB_DQ49
M_B_DQ50 AT8 SB_DQ50
M_B_DQ51 AT9 SB_DQ51
M_B_DQ52 AH11 SB_DQ52
M_B_DQ53 AR8 SB_DQ53
M_B_DQ54 AJ12 SB_DQ54
M_B_DQ55 AH12 SB_DQ55
M_B_DQ56 AT11 SB_DQ56
M_B_DQ57 AN14 SB_DQ57
M_B_DQ58 AR14 SB_DQ58
M_B_DQ59 AT14 SB_DQ59
M_B_DQ60 AT12 SB_DQ60
M_B_DQ61 AN15 SB_DQ61
M_B_DQ62 AR15 SB_DQ62
M_B_DQ63 AT15 SB_DQ63

15 M_B_BS0 AA9 SB_BS0
15 M_B_BS1 AA7 SB_BS1
15 M_B_BS2 R6 SB_BS2

15 M_B_CAS# AA10 SB_CAS#
15 M_B_RAS# AB8 SB_RAS#
15 M_B_WE# AB9 SB_WE#

SB_CLK0 AE2 M_B_DIM0_CLK_DDR0 15
SB_CLK#0 AD2 M_B_DIM0_CLK_DDR#0 15
SB_CKE0 R9 M_B_DIM0_CKE0 15

SB_CLK1 AE1 M_B_DIM0_CLK_DDR1 15
SB_CLK#1 AD1 M_B_DIM0_CLK_DDR#1 15
SB_CKE1 R10 M_B_DIM0_CKE1 15

SB_CLK2 AB2
SB_CLK#2 AA2
SB_CKE2 T9

SB_CLK3 AA1
SB_CLK#3 AB1
SB_CKE3 T10

SB_CS#0 AD3 M_B_DIM0_CS#0 15
SB_CS#1 AE3 M_B_DIM0_CS#1 15
SB_CS#2 AD6
SB_CS#3 AE6

SB_ODT0 AE4 M_B_DIM0_ODT0 15
SB_ODT1 AD4 M_B_DIM0_ODT1 15
SB_ODT2 AD5
SB_ODT3 AE5

SB_DQS#0 D7 M_B_DQS#0
SB_DQS#1 F3 M_B_DQS#1
SB_DQS#2 K6 M_B_DQS#2
SB_DQS#3 N3 M_B_DQS#3
SB_DQS#4 AN5 M_B_DQS#4
SB_DQS#5 AP9 M_B_DQS#5
SB_DQS#6 AK12 M_B_DQS#6
SB_DQS#7 AP15 M_B_DQS#7
M_B_DQS#[7:0] 15

SB_DQS0 C7 M_B_DQS0
SB_DQS1 G3 M_B_DQS1
SB_DQS2 J6 M_B_DQS2
SB_DQS3 M3 M_B_DQS3
SB_DQS4 AN6 M_B_DQS4
SB_DQS5 AP8 M_B_DQS5
SB_DQS6 AK11 M_B_DQS6
SB_DQS7 AP14 M_B_DQS7
M_B_DQS[7:0] 15

SB_MA0 AA8 M_B_A0
SB_MA1 T7 M_B_A1
SB_MA2 R7 M_B_A2
SB_MA3 T6 M_B_A3
SB_MA4 T2 M_B_A4
SB_MA5 T4 M_B_A5
SB_MA6 T3 M_B_A6
SB_MA7 R2 M_B_A7
SB_MA8 T5 M_B_A8
SB_MA9 R3 M_B_A9
SB_MA10 AB7 M_B_A10
SB_MA11 R1 M_B_A11
SB_MA12 T1 M_B_A12
SB_MA13 AB10 M_B_A13
SB_MA14 R5 M_B_A14
SB_MA15 R4 M_B_A15
M_B_A[15:0] 15

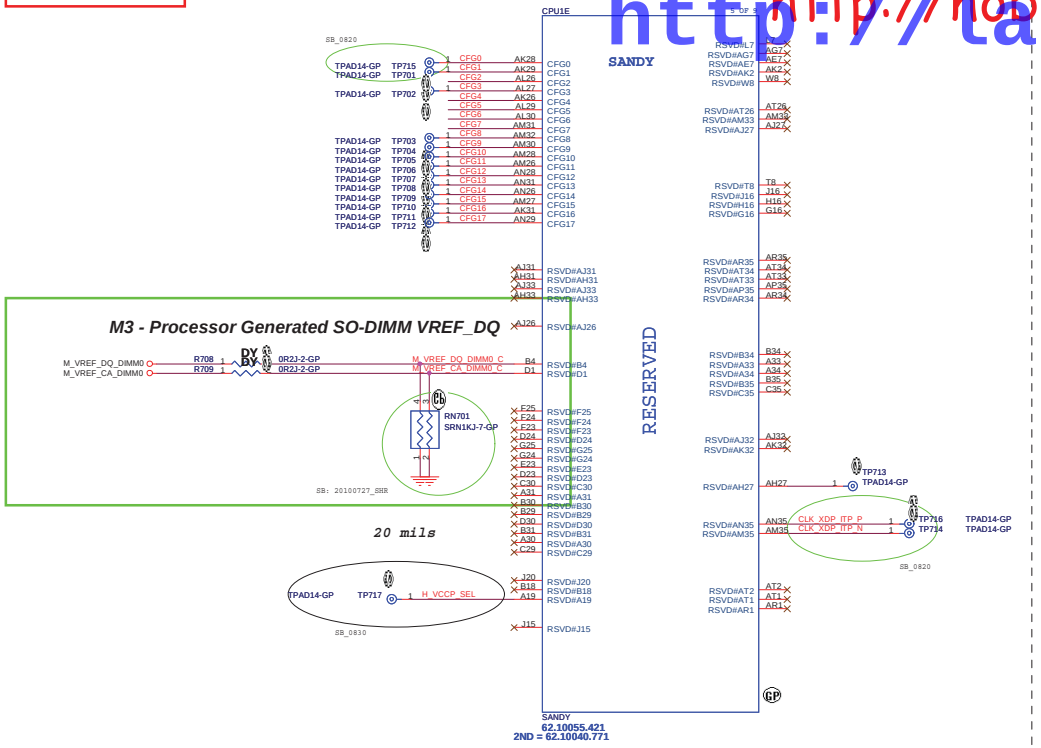
SANDY
62.10055.421
2ND = 62.10040.771

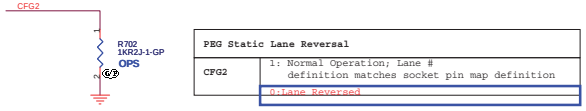
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

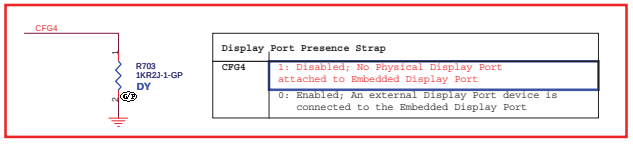
Title: CPU (DDR)		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 6 of 103	

SSID = CPU

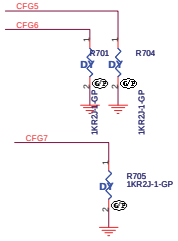




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

Size: A2 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 7 of 103

SSID = CPU

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

CPU1F

SANDY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
→ VCC

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

1D05V_VTT

VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

C812 C813 C814 C829 C830 C842 C843 C844 C845 SC10U6D3V5KX-1GP

VCCIO: J23

R804 need to close to CPU

1D05V_VTT

SB_0819

H_CPU_SVIDDAT_R R804 1 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP → VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 1 0R2J-2-GP → H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 1 0R2J-2-GP → H_CPU_SVIDDAT 42

SB_0819

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 → VCCSENSE 42
VSS_SENSE AJ34 → VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 → VCCIO_SENSE 45
VSSIO_SENSE A10 → VSSIO_SENSE 45

SANDY
62.10055.421
2ND = 62.10040.771

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 8 of 103

SSID = CPU

POWER

CPU1G — SANDY — GRAPHICS — 7 OF 9

VCC_GFXCORE

PROCESSOR VAXG: 24A

VAXG pins: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP
RC901 SC33P50V2JN-3GP DY
C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP
RC902 SC33P50V2JN-3GP DY
SB_0831

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ pins: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA pins: M27, M26, L26, J26, J25, J24, H26, H25

C916 C915 C917 — SC10U6D3V5KX-1GP
TC903 ST330U2VDM-4-GP DY

0D85V_S0
R902 10R2J-2-GP — R902 need be close to pin H23.

VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48

MISC

FC_C22 — C22
VCCSA_VID1 — C24
H_FC_C22 — H_FC_C22 48
VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL pins: B6, A6, A2

C925 C923 — SC10U6D3V5KX-1GP
C922 C924 — SC1U10V2KX-1GP

SANDY
62.10055.421
2ND = 62.10040.771

Close to CPU

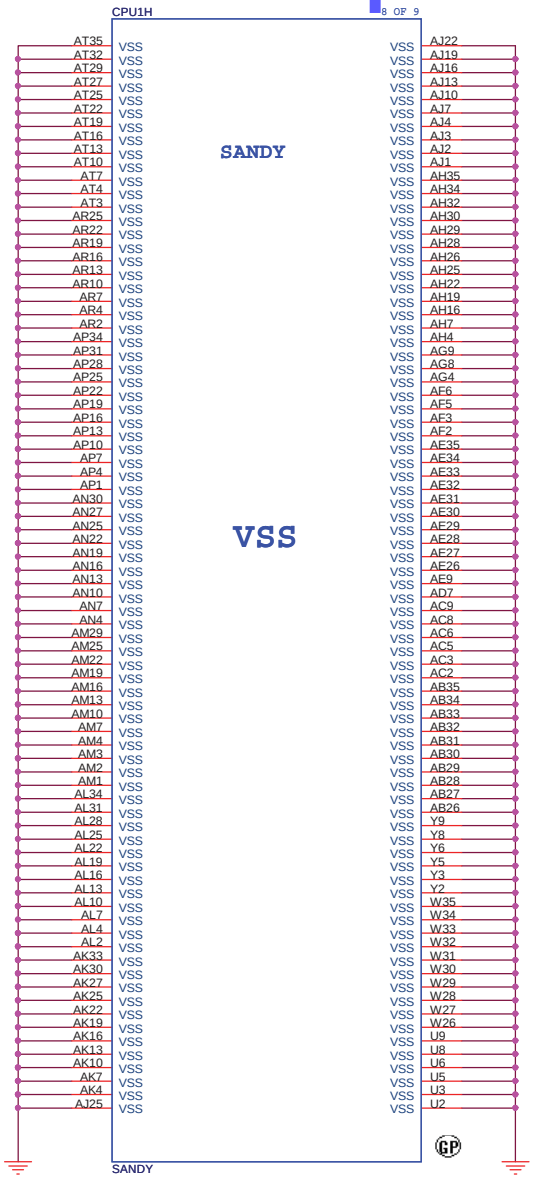
VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

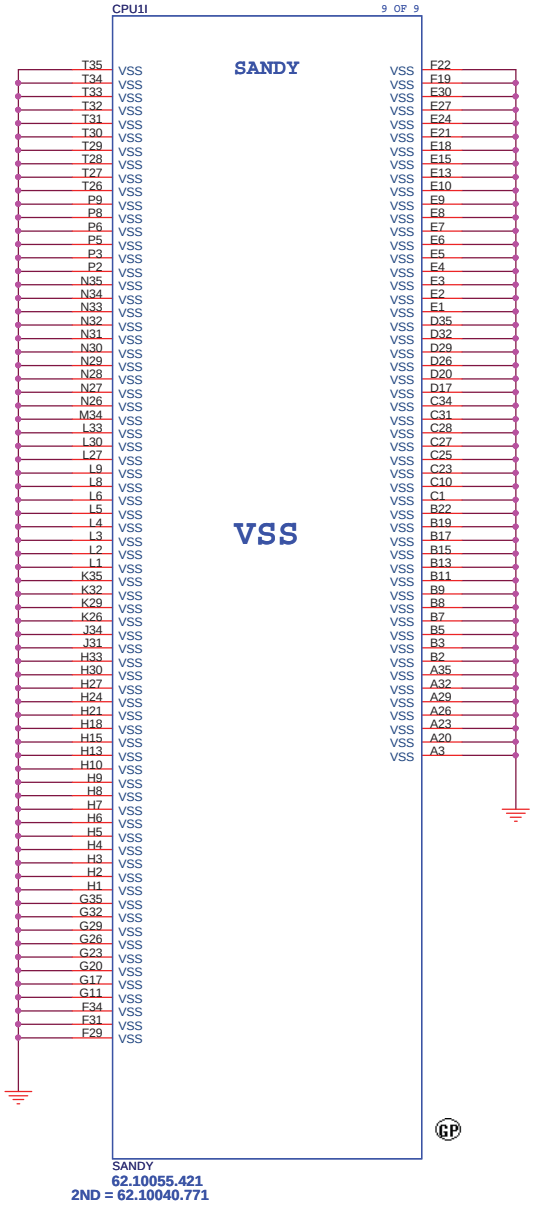
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 9 of 103

SSID = CPU





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 10 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 11 of 103	

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 12 of 103

(Blanking)

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A4	Document Number: **LA470**
Rev: **SB**	
Date: Tuesday, September 07, 2010	Sheet 13 of 103

SSID = MEMORY

DDR_VREF_S3
R1405 0R2J-2-GP
M_VREF_CA_DIMM0
C1423 SCD1U10V2KX-5GP
C1425 SC2D2U10V3KX-1GP
C1424 SCD1U10V2KX-5GP

DDR_VREF_S3
R1404 0R2J-2-GP
M_VREF_DQ_DIMM0
C1411 SCD1U10V2KX-5GP
C1412 SC2D2U10V3KX-1GP
C1413 SCD1U10V2KX-5GP

0D75V_S0
Place these caps close to VTT1 and VTT2.
C1419 SC1U6D3V2KX-GP
C1420 SC1U6D3V2KX-GP
C1421 SC1U6D3V2KX-GP
C1422 SC1U6D3V2KX-GP
C1418 SC10U6D3V5KX-1GP

M_A_A[15:0] 6
M_A_BS2 6
M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6
M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6
M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0
15,37 DDR3_DRAMRST#
0D75V_S0

DM1
NP1 NP2

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
	79	A16/BA2	
	109	BA0	
	108	BA1	

M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	

M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	

	116	ODT0	
	120	ODT1	
M_VREF_CA_DIMM0	126	VREF_CA	
M_VREF_DQ_DIMM0	1	VREF_DQ	
	30	RESET#	
0D75V_S0	203	VTT1	
	204	VTT2	

	110	RAS#	M_A_RAS# 6
	113	WE#	M_A_WE# 6
	115	CAS#	M_A_CAS# 6
	114	CS0#	M_A_DIM0_CS#0 6
	121	CS1#	M_A_DIM0_CS#1 6
	73	CKE0	M_A_DIM0_CKE0 6
	74	CKE1	M_A_DIM0_CKE1 6
	101	CK0	M_A_DIM0_CLK_DDR0 6
	103	CK0#	M_A_DIM0_CLK_DDR#0 6
	102	CK1	M_A_DIM0_CLK_DDR1 6
	104	CK1#	M_A_DIM0_CLK_DDR#1 6

DM0	11	
DM1	28	
DM2	46	
DM3	63	
DM4	136	
DM5	153	
DM6	170	
DM7	187	

SDA	200	PCH_SMBDATA 15,20,65,66
SCL	202	PCH_SMBCLK 15,20,65,66
EVENT#	198	TS#_DIMM0_1 15
VDDSPD	199	
SA0	197	SA0_DIM0
SA1	201	SA1_DIM0
NC#1	77	
NC#2	122	
NC#/TEST	125	

1D5V_S3

VDD1	75	VSS	2	VSS	127	VSS	173
VDD2	76	VSS	3	VSS	128	VSS	178
VDD3	81	VSS	8	VSS	133	VSS	179
VDD4	82	VSS	9	VSS	134	VSS	184
VDD5	87	VSS	13	VSS	138	VSS	185
VDD6	88	VSS	14	VSS	139	VSS	189
VDD7	93	VSS	19	VSS	144	VSS	190
VDD8	94	VSS	20	VSS	145	VSS	195
VDD9	99	VSS	25	VSS	150	VSS	196
VDD10	100	VSS	26	VSS	151	VSS	205
VDD11	105	VSS	31	VSS	155	VSS	206
VDD12	106	VSS	32	VSS	156	VSS	
VDD13	111	VSS	37	VSS	161		
VDD14	112	VSS	38	VSS	162		
VDD15	117	VSS	43	VSS	167		
VDD16	118	VSS	44	VSS	168		
VDD17	123	VSS	48	VSS	172		
VDD18	124	VSS	49	VSS	173		
		VSS	54	VSS	178		
		VSS	55	VSS	179		
		VSS	60	VSS	184		
		VSS	61	VSS	185		
		VSS	65	VSS	189		
		VSS	66	VSS	190		
		VSS	71	VSS	195		
		VSS	72	VSS	196		

DDR3-204P-109-GP
62.10017.X51
2nd = 62.10017.R91
3rd = 62.10017.V61
SB_0819

SA0_DIM0
SA1_DIM0
R1401 10KR2J-3-GP
R1402 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT
TS#_DIMM0_1
R1403 10KR2J-3-GP
3D3V_S0

3D3V_S0
C1401 SCD1U10V2KX-5GP
C1402 SC2D2U10V3KX-1GP

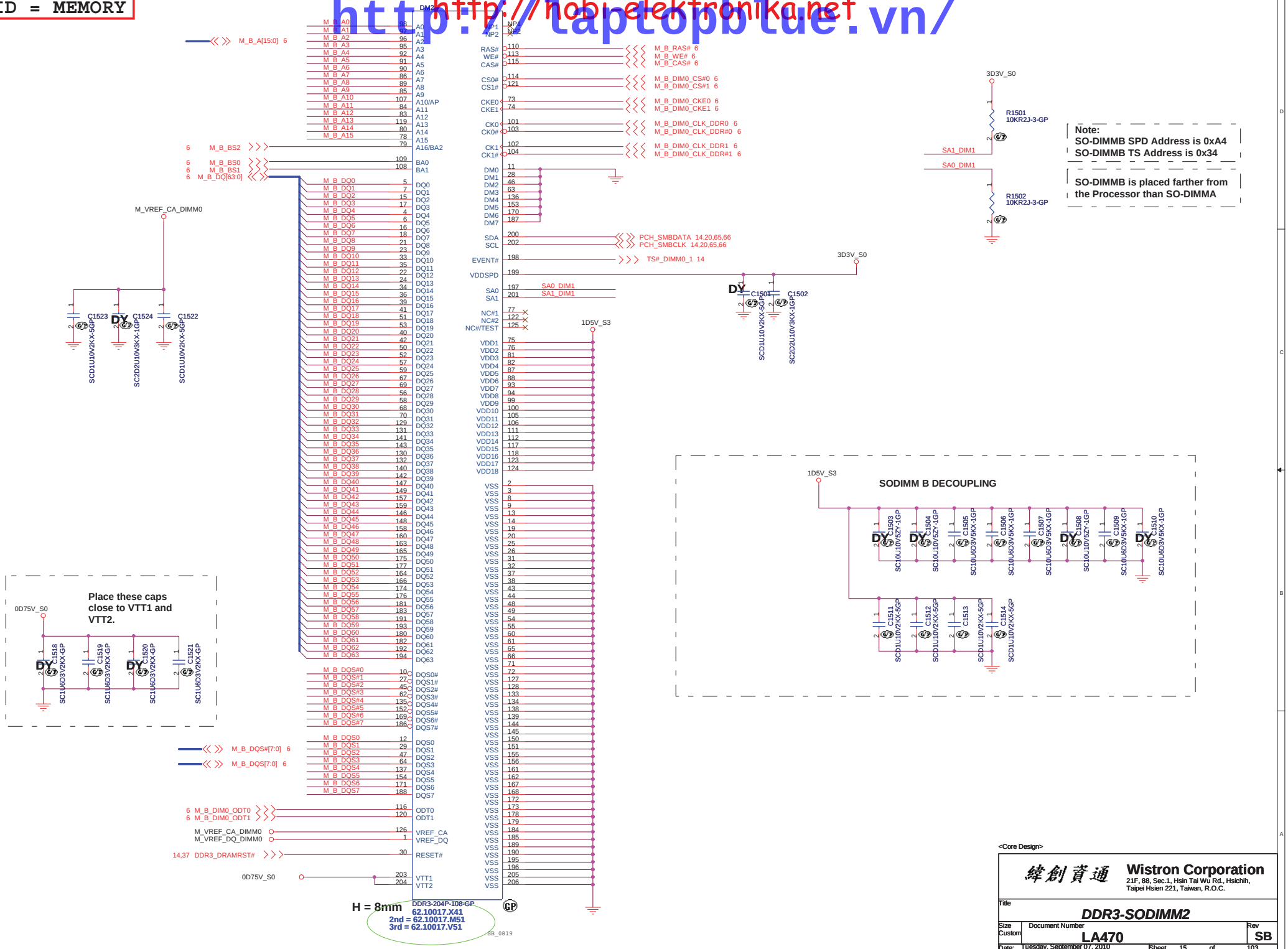
SODIMM A DECOUPLING
1D5V_S3
TC1401 ST330U2VDM-4-GP
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 SC10U10V5ZY-1GP
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP
C1408 SC10U10V5ZY-1GP
C1409 SC10U6D3V5KX-1GP
C1410 SC10U6D3V5KX-1GP
C1414 SCD1U10V2KX-5GP
C1415 SCD1U10V2KX-5GP
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1
Size: Custom
Document Number: LA470
Rev: SB
Date: Tuesday, September 07, 2010
Sheet 14 of 103

SSID = MEMORY



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 15 of 103

(Blanking)

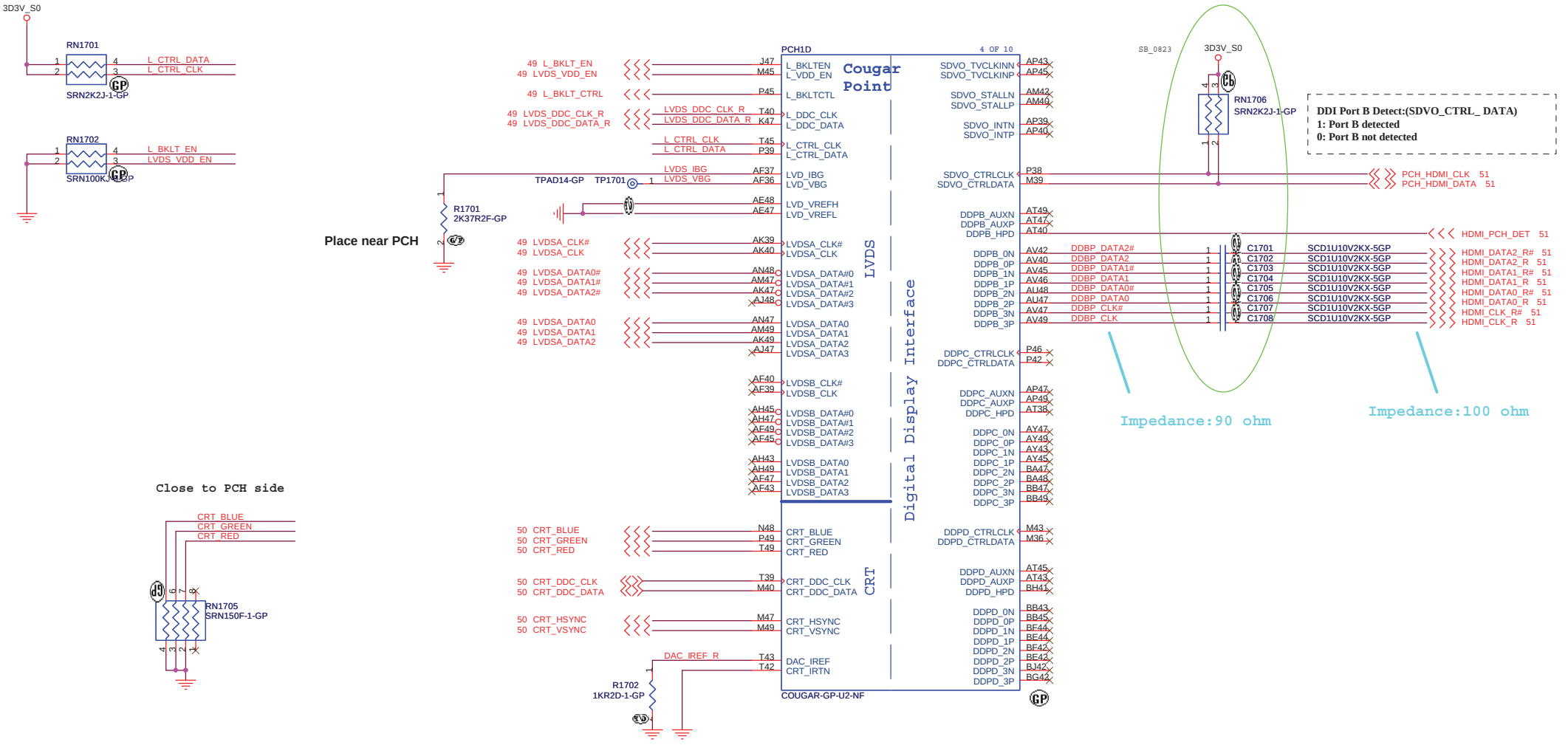
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 16 of 103



<Core Design>

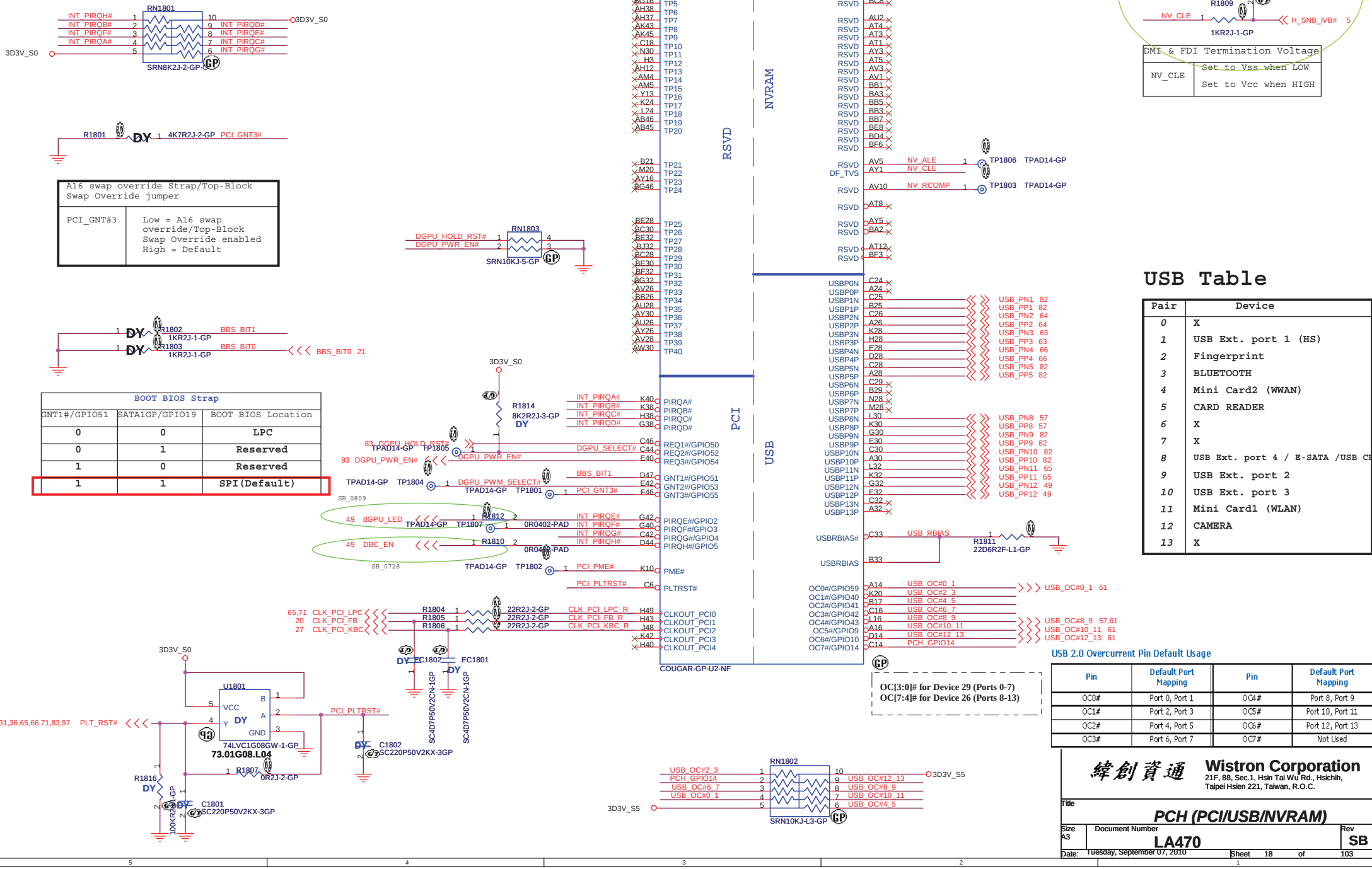
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 17 of 103

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI_RXN[3:0], DMI_RXP[3:0], DMI_TXN[3:0], DMI_TXP[3:0]
FDI: FDI_RXN[7:0], FDI_RXP[7:0], FDI_TXN[7:0], FDI_TXP[7:0], FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

1D05V_VTT
R1901 49D9R2F-GP DMI_COMP_R
R1902 750R2F-GP RBIAS_CPY

System Power Management

SUS_PWR_ACK
R1903 0R0402-PAD
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
RUNPWROK
PM_DRAM_PWRGD
PM_RSMRST#
SUS_PWR_ACK
PM_PWRBTN#
AC_PRESENT
BATLOW#
PM_RI#
SUSWARN#/SUSPWRDNACK/GPIO30
DSWVRMEN
DSWODVREN
DPWROK
PCH_DPWROK
WAKE#
PCIE_WAKE# 31,65,66
CLKRUN#/GPIO32
PM_CLKRUN# 27
SUS_STAT#/GPIO61
PM_SUS_STAT#
SUSCLK/GPIO62
SUS_CLK
SLP_S5#/GPIO63
PM_SLP_S5#
SLP_S4#
SLP_S4#_R
SLP_S3#
SLP_S3#_R
SLP_A#
PM_SLP_A#
SLP_SUS#
PM_SLP_SUS#
PMSYNCH
H_PM_SYNC
SLP_LAN#/GPIO29
PM_SLP_LAN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
COUGAR-GP-U2-NF

TP1901 TPAD14-GP
TP1902 TPAD14-GP
TP1903 TPAD14-GP
TP1904 TPAD14-GP
TP1905 TPAD14-GP
TP1906 TPAD14-GP

R1910 0R2J-2-GP PM_RSMRST#
R1911 10KR2J-3-GP
RTC_AUX_S5

R1913 0R2J-2-GP PCH_SUSCLK_KBC 27
R1914 0R2J-2-GP PM_SLP_S4# 27,46
R1915 0R2J-2-GP PM_SLP_S3# 27,36,37,47,92

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 330KR2J-L1-GP
DSWODVREN
R1918 330KR2J-L1-GP

3D3V_S0
PM_CLKRUN# R1919 8K2R2J-3-GP

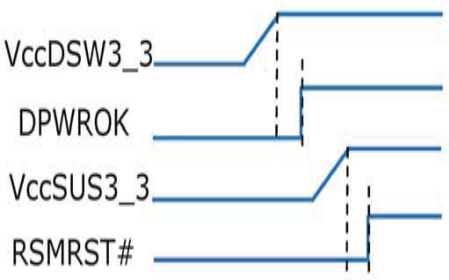
3D3V_S5
RN1901 SRN10KJ-6-GP
BATLOW#
PM_RI#
AC_PRESENT
SUS_PWR_ACK
R1921 10KR2J-3-GP PCIE_WAKE#
R1922 10KR2J-3-GP PM_PWRBTN#
R1920 10KR2J-3-GP PM_SLP_LAN#

This signal has an internal pull-up resistor

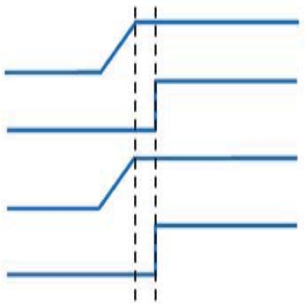
R1908 10KR2J-3-GP PM_RSMRST#

3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
PM_RSMRST#
R1912 1KR2J-1-GP
RSMRST#_KBC 27
3V_5V_POK_# 3V_5V_POK 41

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 19 of 103

SSID = PCH

PCH1B

2 OF 10

Cougar Point

W-WAN

WLAN

LAN

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

COUGAR-GP-U2-NF

WLAN CLK

LAN CLK

PCIECLKRQ1# and PCIECLKRQ2# support S0 power only

PL 10K FOR Integrated CLOCK GEN mode.

need very close to PCH

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

CRB: 1K
CHKLT: 10K

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

R2008 and C2008 CO-LAY

82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

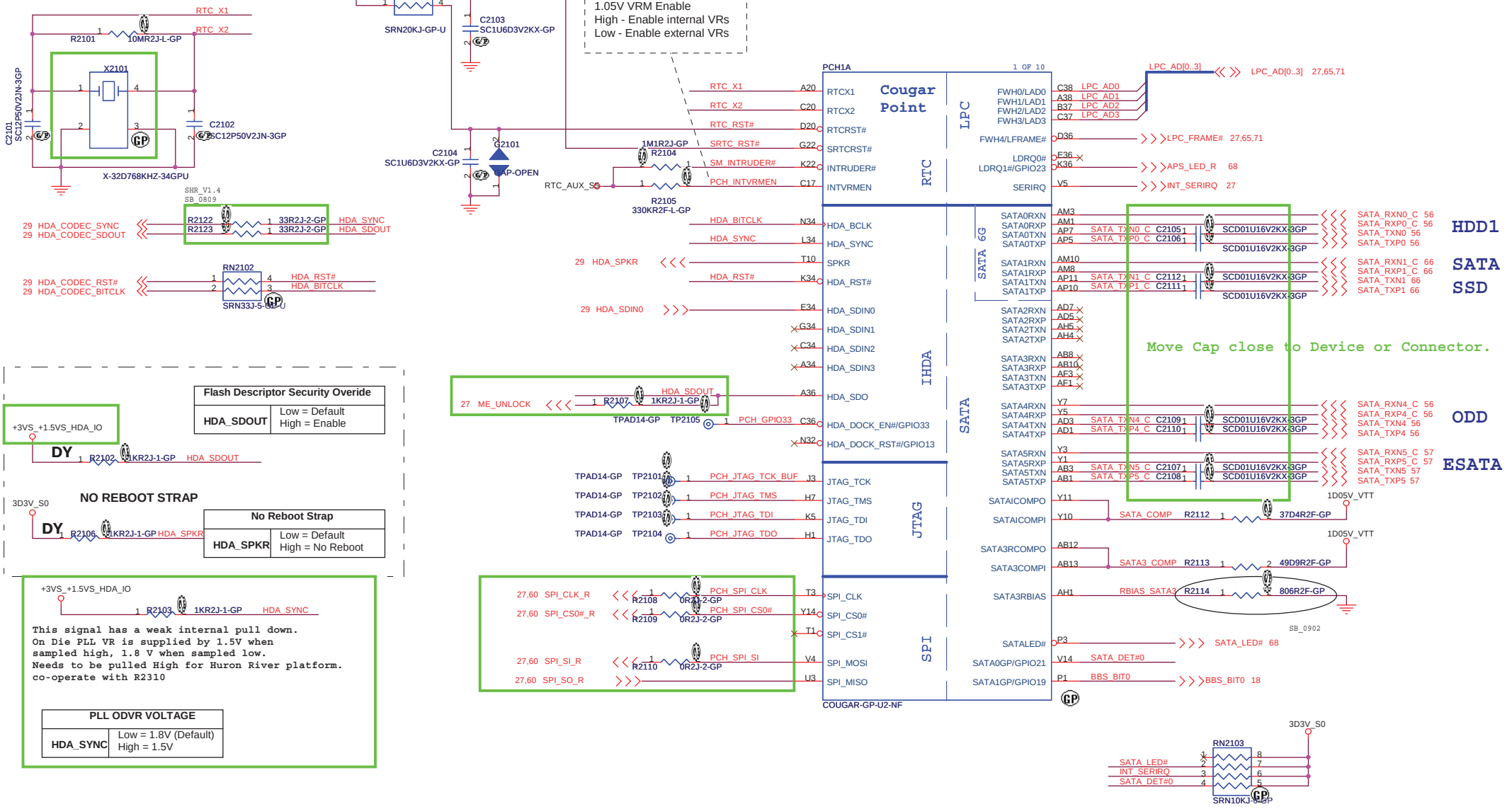
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 20 of 103

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 21 of 103

PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 200KR2F-L-GP SATA_ODD_PRSNT#

20100625 V1.2

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
PCH_GPIO27 — DY R2223 10KR2J-3-GP
DY R2225 10KR2J-3-GP

3D3V_S0 — RN2201 — PSW_CLR#, DGPU_HPD_INTR#, EC_SMI# — SRN10KJ-8-GP

RN2202 — MFG_MODE, S_GPIO, EC_SCI#, PCH_GPIO22 — SRN10KJ-8-GP
PCH_GPIO48 — R2227 10KR2J-3-GP

3D3V_S5 — RN2205 — PCH_GPIO12, USB3_PWR_ON — SRN10KJ-8-GP

PCH_GPIO15 — R2201 1KR2J-1-GP
PCH_GPIO24 — R2221 10KR2J-3-GP
20100625 V1.2
PLL_ODVR_EN — R2226 10KR2J-3-GP

NC_FP_DET# — R2220 10KR2J-3-GP
20100705

PCH1F — 6 OF 10 — Cougar Point — COUGAR-GP-U2-NF

S_GPIO — R2218 100R2J-2-GP	GPIO0 T7
	BMBUSY#/GPIO0
	TACH1/GPIO1 A42
DGPU_HPD_INTR#	TACH2/GPIO6 H36
27 EC_SCI#	EC_SCI# TACH3/GPIO7 E38
	ICC_EN# GPIO8 C10
	PCH_GPIO12 LAN_PHY_PWR_CTRL/GPIO12 C4
	PCH_GPIO15 GPIO15 G2
56 SATA_ODD_PRSNT# — R2213 0R2J-2-GP	PCH_GPIO16 SATA4GP/GPIO16 U2
92,93 DGPU_PWROK — R2228 0R2J-2-GP	DGPU_PWROK TACH0/GPIO17 D40
49 Color_Engine# — TPAD14-GP TP2202	PCH_GPIO22 SCLOCK/GPIO22 T5
	PCH_GPIO24 GPIO24/MEM_LED E8
	PCH_GPIO27 GPIO27 E16
	PLL_ODVR_EN GPIO28 P8
	PSW_CLR# STP_PCI#/GPIO34 K1
TPAD14-GP TP2204	NC_FP_DET# GPIO35 K4
GAP-OPEN G2201	DMI_OVRVLTG SATA2GP/GPIO36 V8
	FDI_OVRVLTG SATA3GP/GPIO37 M5
	MFG_MODE SLOAD/GPIO38 N2
	GFX_CRB_DET SDATAOUT0/GPIO39 M3
TP2209	PCH_GPIO48 SDATAOUT1/GPIO48 V13
	PCH_TEMP_ALERT# SATA5GP/GPIO49 V3
TPAD14-GP	USB3_PWR_ON GPIO57 D6
TP2205	NCTF_VSS#A4 A4
TPAD14-GP	NCTF_VSS#A44 A44
TP2206	NCTF_VSS#A45 A45
TPAD14-GP	NCTF_VSS#A46 A46
	NCTF_VSS#A5 A5
	NCTF_VSS#A6 A6
	NCTF_VSS#B3 B3
	NCTF_VSS#B47 B47
	NCTF_VSS#BD1 BD1
	NCTF_VSS#BD49 BD49
TPAD14-GP TP2210	NCTF_VSS#BE1 BE1
TPAD14-GP TP2211	NCTF_VSS#BE49 BE49
TPAD14-GP TP2212	NCTF_VSS#BF1 BF1
	NCTF_VSS#BF49 BF49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49 BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48 D1,D49,E1,E49,F1,F49

SB_0811
SHR_V1.5

	NCTF_VSS#BG2 BG2
	NCTF_VSS#BG48 BG48
	NCTF_VSS#BH3 BH3
TP2207	NCTF_VSS#BH47 BH47
TPAD14-GP	NCTF_VSS#BJ4 BJ4
	NCTF_VSS#BJ44 BJ44
	NCTF_VSS#BJ45 BJ45
TP2208 TPAD14-GP	NCTF_VSS#BJ46 BJ46
	NCTF_VSS#BJ5 BJ5
	NCTF_VSS#BJ6 BJ6
	NCTF_VSS#C2 C2
	NCTF_VSS#C48 C48
	NCTF_VSS#D1 D1
	NCTF_VSS#D49 D49
	NCTF_VSS#E1 E1
	NCTF_VSS#E49 E49
	NCTF_VSS#F1 F1
	NCTF_VSS#F49 F49

	TACH4/GPIO68 C40 — SATA_ODD_PWRGT 56
	TACH5/GPIO69 B41 — UMA_DIS# 20
	TACH6/GPIO70 C41 — VRAM_SIZE1
	TACH7/GPIO71 A40 — VRAM_SIZE2
	A20GATE P4 — H_A20GATE 27
H_PECI R — DY R2203 0R2J-2-GP	PECI AU16 — H_PECI 5,27
	RCIN# P5 — H_RCIN# 27
	PROCPWRGD AY11 — H_CPUPWRGD 5,11,36,97
PCH_THERMTRIP_R R2204 390R2J-1-GP	THRMTRIP# AY10 — H_THERMTRIP# 5,36
TP2201 TPAD14-GP	INIT3_3V# T14 — INIT3_3V#
	TS_VSS1 AH8
	TS_VSS2 AK11
	TS_VSS3 AH10
TS_VSS R2219 0R0402-PAD	TS_VSS4 AK10
	NC_1 P37

3D3V_S0 — DY R2205 10KR2J-3-GP — GFX_CRB_DET — R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 — 1D05V_VTT — DY 56R2J-4-GP

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG
R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG
R2210 10KR2J-3-GP

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2214 10KR2J-3-GP (2G) — R2216 10KR2J-3-GP (1G)
R2215 10KR2J-3-GP (1G_512M) — R2217 10KR2J-3-GP (2G_512M)
VRAM_SIZE1
VRAM_SIZE2

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY — R2212 1KR2J-1-GP

<Core Design>

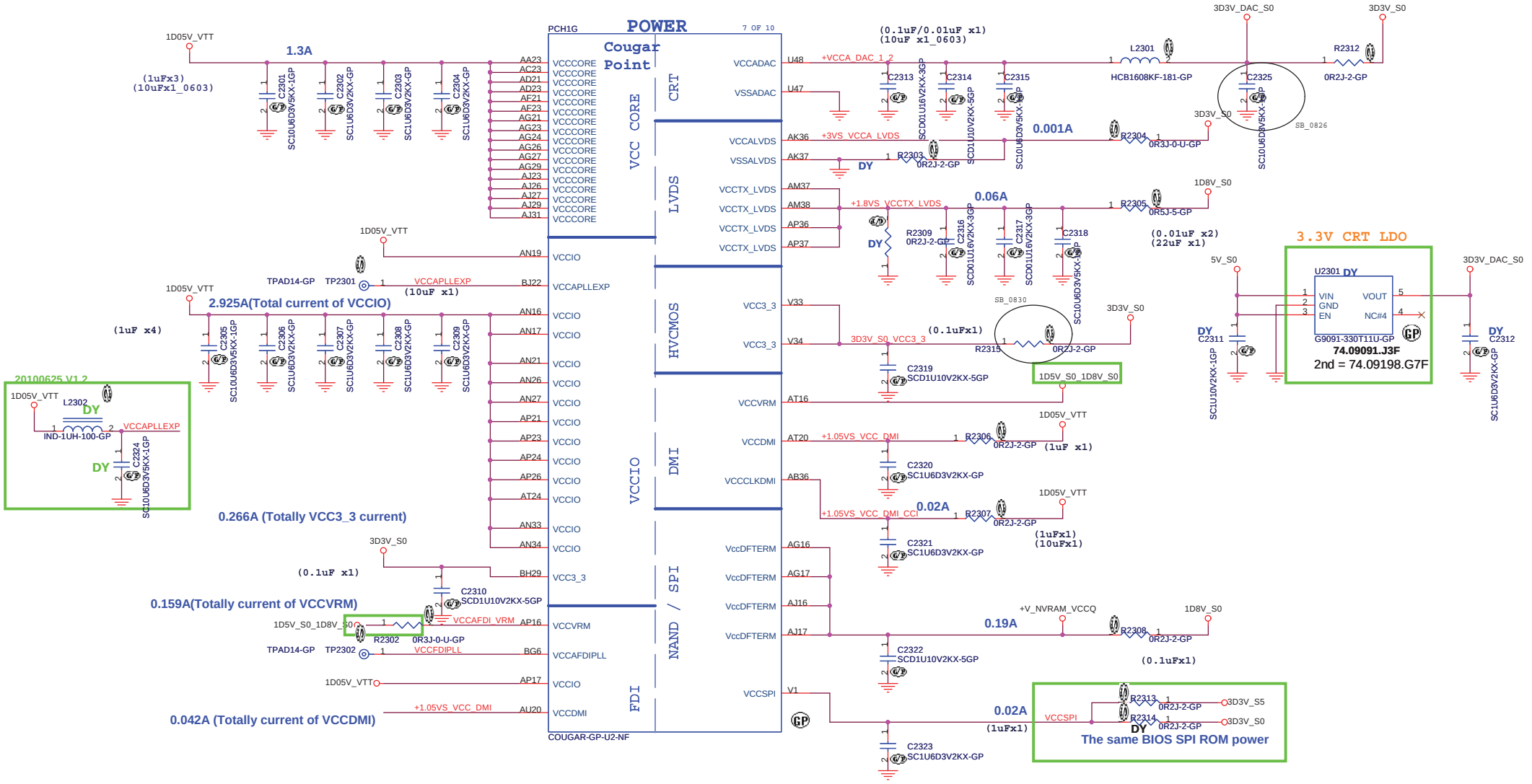
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 — Sheet 22 of 103

SSID = PCH 6A



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (POWER1)		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 23 of 103	

SSID = PCH

POWER

Cougar Point

PCH(1 OF 10)

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.08A

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.01A

6uA

<Core Design>

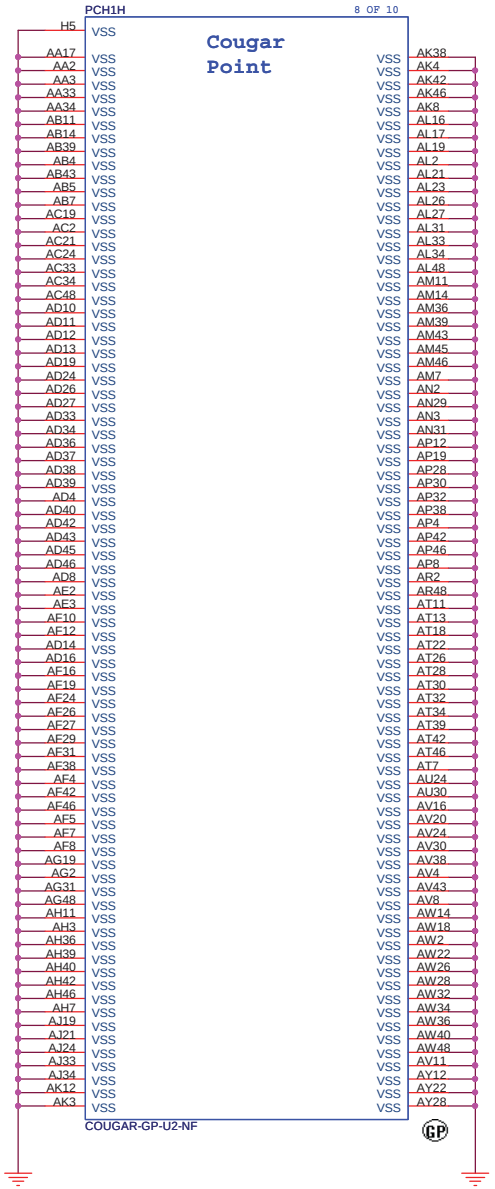
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

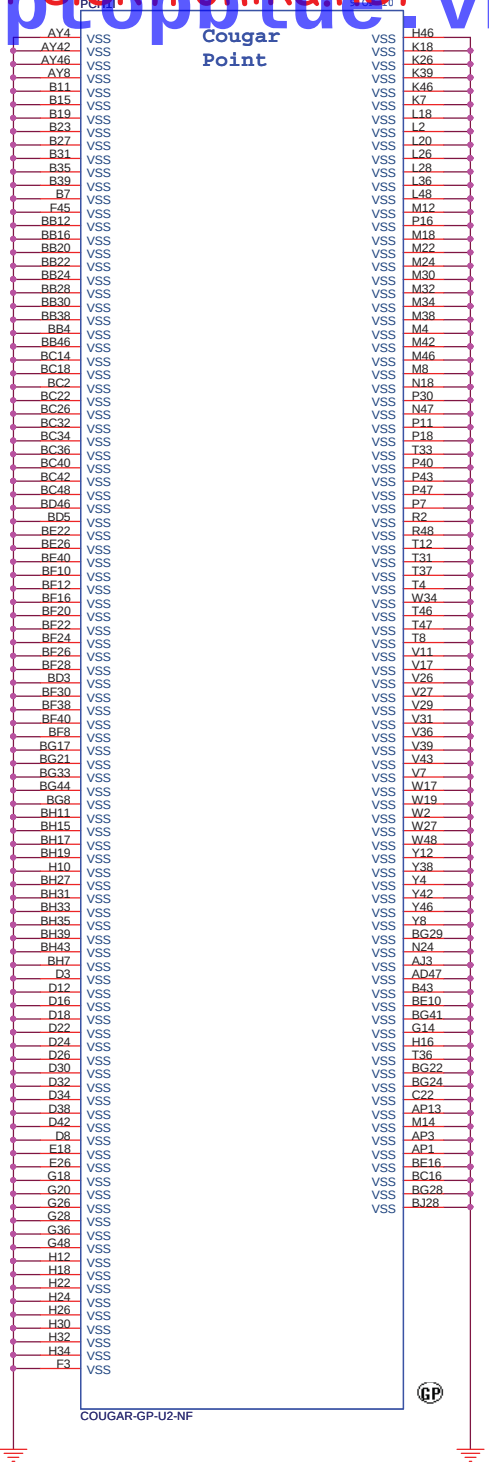
Title: PCH (POWER2)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 24 of 103

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 25 of 103

(Blanking)

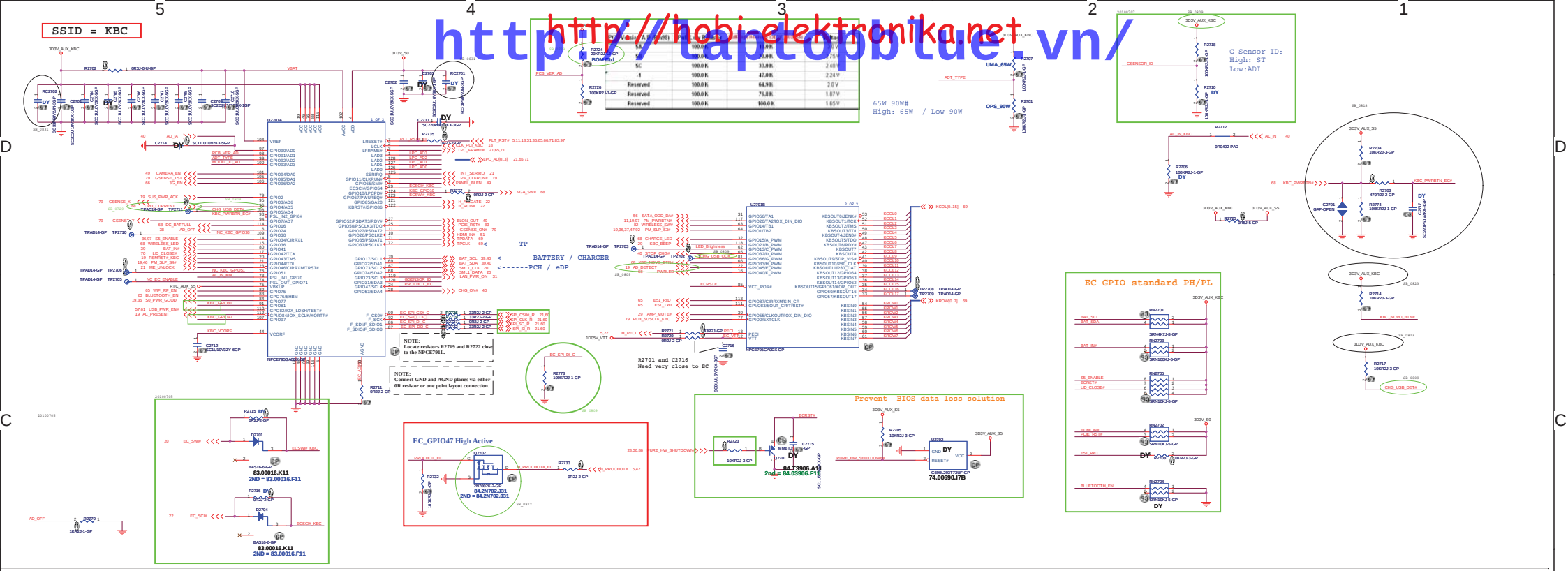
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

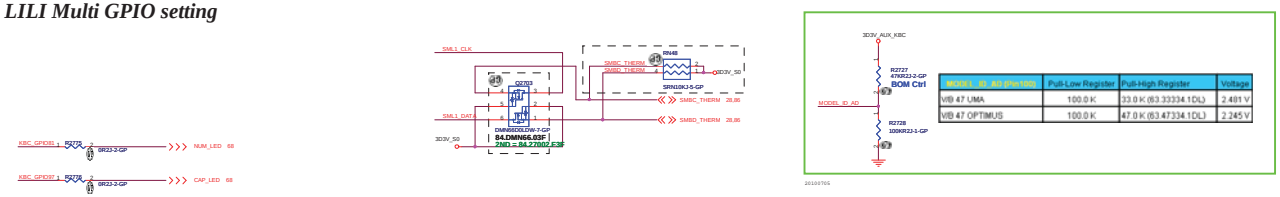
Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 26 of 103



LILI Multi GPIO setting



Wistron Corporation		
Title: KBC Nuvoton NPCE795		
Size: A1	Document Number: LA470	Rev: SB
Date: Monday, September 07, 2009	Sheet 27 of 53	

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA_0905 change to 390p

3
Q6
MMBT3904WT1G-GP
C183
SC390P50V2KX-GP

2
Q42
MMBT3904WT1G-GP
C434
SC390P50V2KX-GP
DY

2200p close to smsc2103 chip
REMOTE2-
REMOTE2+
C569
SC2200P50V2KX-2GP

between CPU, VGA and DIMM on bottom side

T8

1
Q9
MMBT3904WT1G-GP

2200p close to smsc2103 chip
H_THERMDA
H_THERMDC
C389
SC2200P50V2KX-2GP

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

SA_0905

5V_S0

D2801
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY

C39
C4D7U6D3V3KX-GP

R2801
0R3J-0-U-GP

R426
10KR2J-3-GP

SB_0819

FAN_TACH
FAN_PWM
5V_S0_FAN
FAN_PWM_C

R427
0R0402-PAD

EC2801
EC2802
DY
SCI.KP50V2KX-1GP

20100707_EMI

FAN1
ACES-CON4-4-GP
20.F0765.004
2nd = 20.F1808.004

3D3V_S0

R280
6K8R2J-GP

SHDN_SEL

SHDN --> 2N3904 ON External diode

R260
68R2-GP

C388
SCD1U10V2KX-4GP
2103_VDD

U31
EMC2103-2-AP-GP

VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
GPIO1
GPIO2
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-

SC 1203

THERM_SCI#
THERM_SYS_SHDN#
THERM_SCI#_R

TP66
TPAD14-GP

R272
0R0402-PAD

27,86 SMBC_THERM
27,86 SMBD_THERM

2103_4
2103_5

TP65 TPAD14-GP
TP67 TPAD14-GP

TRIP_SET_R276
SHDN_SEL
2K05R2F-GP

T8 = 105

RN49
SRN10KJ-5-GP

D2802
CH551H-30PT-GP
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
83.R5003.C8F

FAN_TACH
FAN_PWM

AFTP2803
AFTP2802
AFTP2801

SB_0825

pin6, ALERT# OD
pin7, SYS_SHDN# OD

3D3V_AUX_S5

D2803
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY

27,36,86 PURE_HW_SHUTDOWN#

R2812
10KR2J-3-GP
DY

C2811
SCD1U10V2KX-4GP
DY

Q2802
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

SB_0812

THERM_SYS_SHDN#

R2809
100KR2J-1-GP

R2810
0R2J-2-GP
DY

R2811
0R2J-2-GP

IMVP_PWRGD 36,42

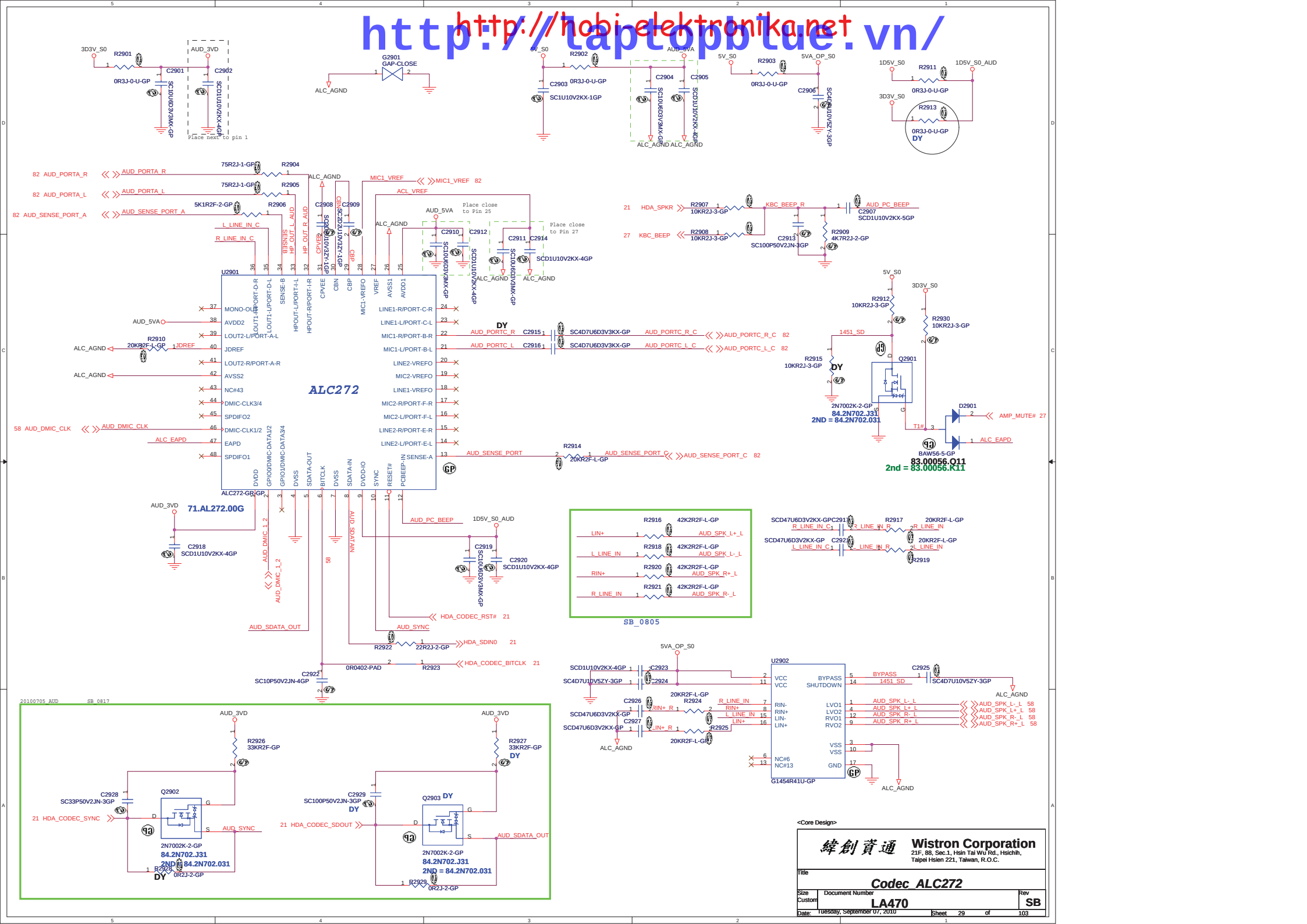
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 28 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 30 of 103

25MHz XTAL

LAN_XTAL0
LAN_XTAL1
X2
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
3rd = 82.30020.A31
R3130 1M1R2J-GP
SB_0824
C3103 C3148
25C12P50V2JN-3GP

3D3V_LAN_S5 1D05V_LAN_S5 1D05V_LAN_S5 3D3V_LAN_S5
R3123 2K49R2F-GP
LAN_RSET
LAN_ACT_LED# 59
LAN_EESK R3127 0R0402-PAD SPEED_100# 59

3D3V_S0 main pwr if have no ASF
R3136 1KR2J-1-GP
RTL_ISOLATE#
R3119 15KR2J-1-GP

U3101
GND
RTL8111E-VB-GR-GP

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33

REGOUT 1D05V_LAN_REGOUT
VDDREG VDDREG ENSWREG LAN_ENSWREG
EEDI/SDA LAN_EEDI
LED3/EEDO LAN_EEDO TP3102 TPAD14-GP
EECS/SCL LAN_EECS
DVDD10 1D05V_LAN_S5
LANWAKE# PCIE_WAKE# 19,65,66
DVDD33 3D3V_LAN_S5
ISOLATE# RTL_ISOLATE#
PERST# PLT_RST# 5,11,19,27,36,65,66,71,83,97

3D3V_LAN_VDDSREG
R3125 3D3V_LAN_S5
R3102 0ohm Res For Enable Switch Regulator.
R3103 0ohm Res For Disable Switch Regulator.
R3124 0R2J-2-GP

High:Link up
Low:Link down
GPO R3120 1KR2J-1-GP
LAN_EECS R3122 10KR2J-3-GP
LAN_EEDI R3126 10KR2J-3-GP
SMB_LAN_DATA R3128 10KR2J-3-GP
The SM DATA with 10K ohm pull GND.

R3132 DY 0R2J-2-GP
20 LAN_XI LAN_XTAL1

Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.

Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1#connected to 10K resistor pull high close to PCH side

1D05V_LAN_S5
SMB_LAN_DATA
R3121 0R2J-2-GP LAN_CLKREQ#
SB_0728
20 PCIE_CLK_LAN_REQ#
20 PCIE_TXP4
20 PCIE_TXN4
20 CLK_PCIE_LAN
20 CLK_PCIE_LAN#
1D05V_LAN_EVDD10
20 PCIE_RXP4 PCIE_RXP4_C C3145 SCD1U10V2KX-4GP
20 PCIE_RXN4 PCIE_RXN4_C C3147 SCD1U10V2KX-4GP

3D3V_S5
R3135 DY 0R3J-0-U-GP
Q3103 AO3419L-GP
C3151 SCD1U10V2KX-4GP
C3152 SCD1U16V2ZY-2GP
R3133 100KR2J-1-GP
LAN_PWR_ON_T
C3150 SC1U10V2KX-1GP
Q3104 2N7002K-1-GP
27 LAN_PWR_ON
84.2N702.031
2nd = 84.2N702.J31

SB_0812
20100705_Standard
vendor advice change
L3102 IND-4D7UH-159-GP
1D05V_LAN_REGOUT
1D05V_LAN_S5
C3146 SC4D7U6D3V3KX-GP
C3129 SCD1U10V2KX-4GP
L3101 adopt spec.
C3104 change to 4.7uF X5R type capacitor

Layout Note: Close to U3101 pin C3106 ~ C3112
C3130 C3131 C3132 C3133 C3134 C3138 C3139 SCD1U16V2ZY-2GP

R3131 0R0603-PAD
1D05V_LAN_EVDD10
C3128 SC1U10V2KX-1GP
C3149 SCD1U16V2ZY-2GP
Layout Note: Close to U3101 pin C3113&C3114
C3113 value modify to 1uF capacitor

3D3V_LAN_S5
3D3V_LAN_VDDSREG
R3134 0R0603-PAD
C3135 C3140 C3141 C3142 C3143 C3144 SCD1U16V2ZY-2GP
C3136 SC4D7U6D3V3KX-GP
C3137
C3122 change to 4.7uF X5R type capacitor
Layout Note: Close to U3101 pin C3115 ~ C3120

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E
Size: A3
Document Number: LA470
Rev: SB
Date: Tuesday, September 07, 2010
Sheet 31 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5159 (CARD READER)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

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<Core Design>

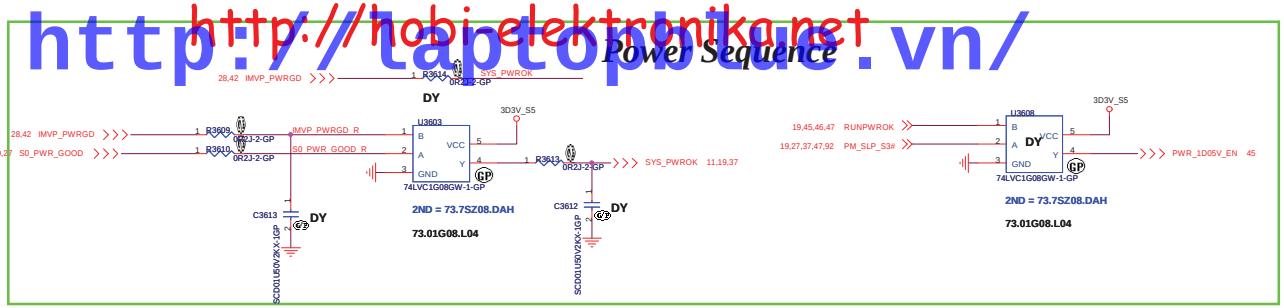
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Controller

Size	Document Number	Rev
A3	LA470	SB

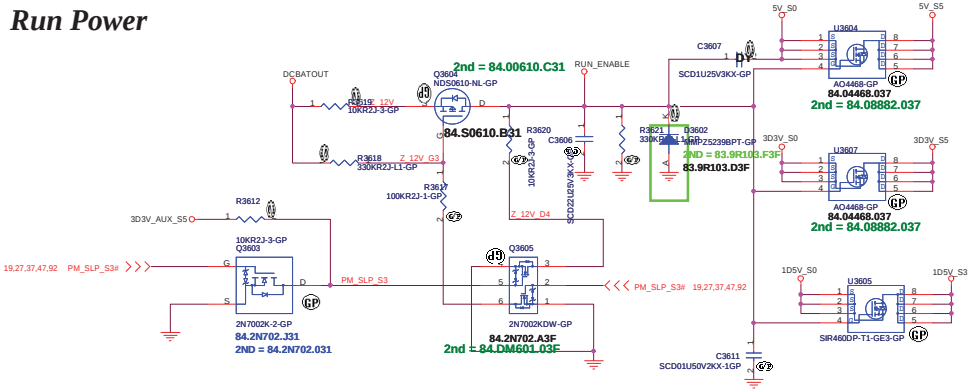
Date: Tuesday, September 07, 2010 Sheet 35 of 103

Power Sequence



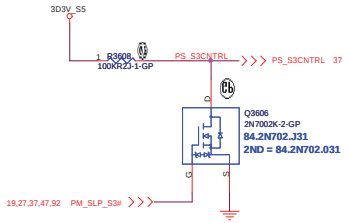
SSID = Reset.Suspend

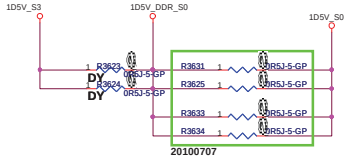
Run Power

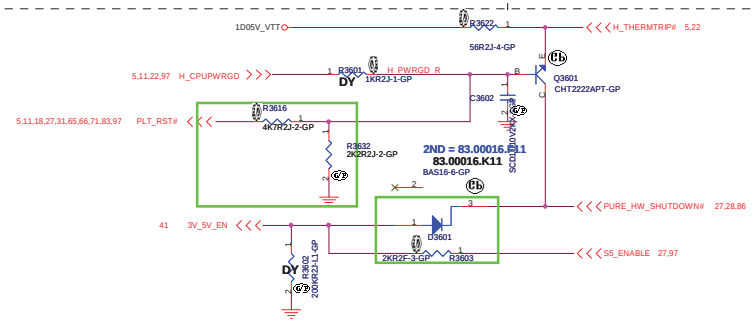


1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A







<Core Design>

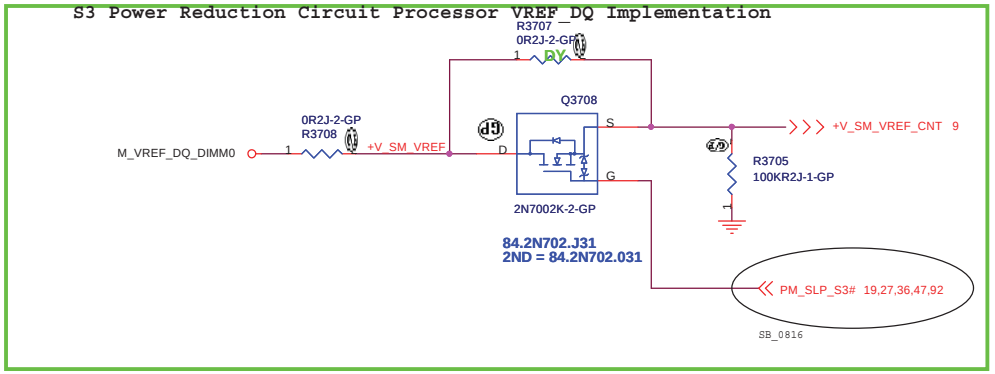
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

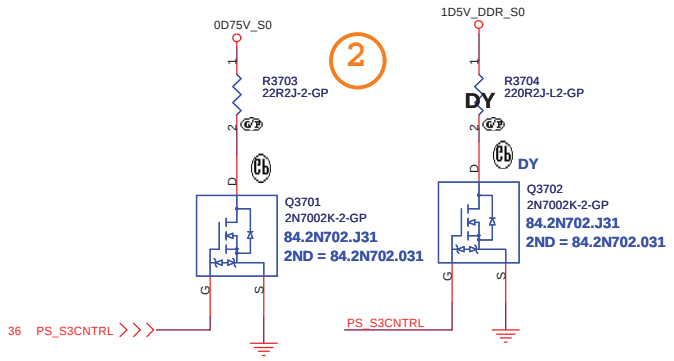
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 36 of 103

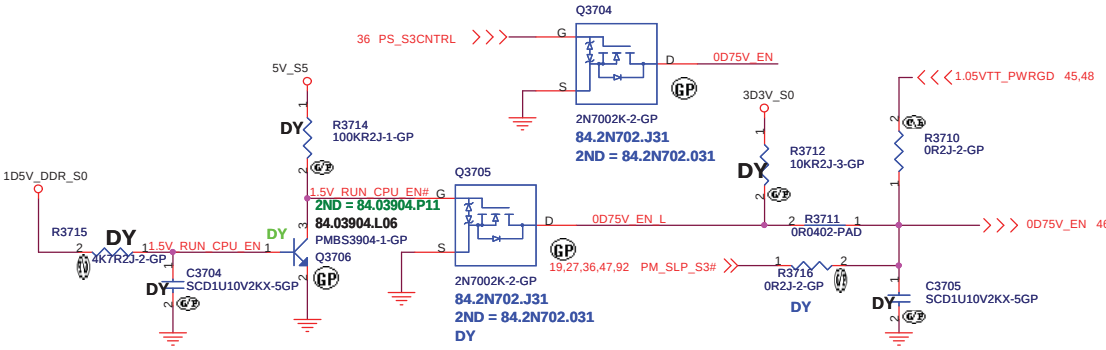
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



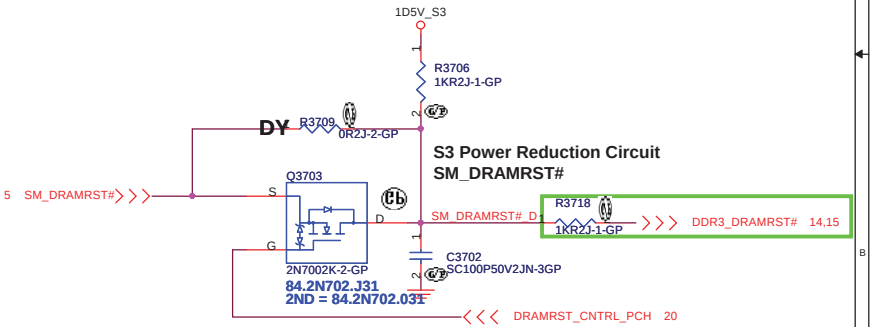
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

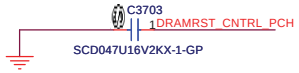


5 S3 Power Reduction X01 20091111

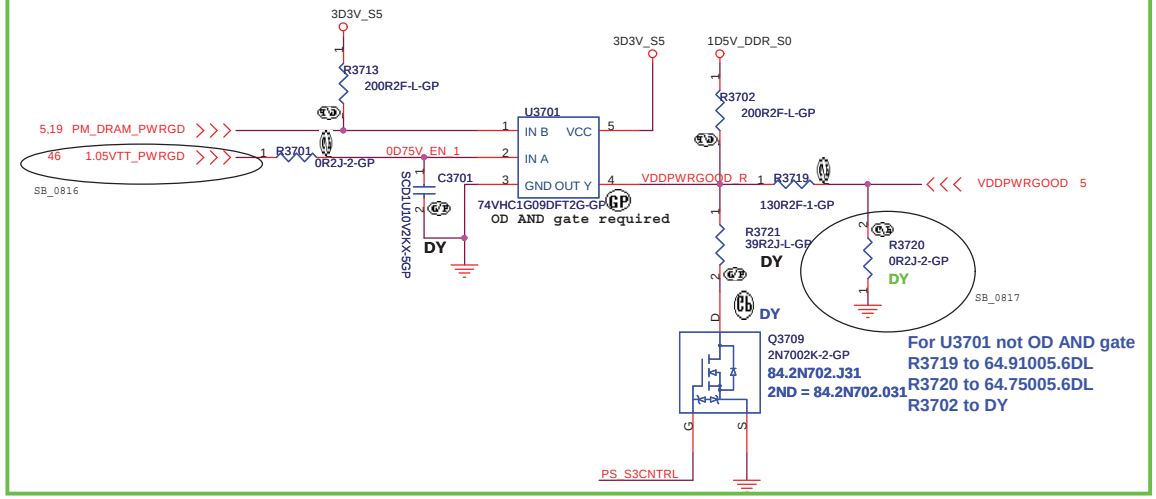


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



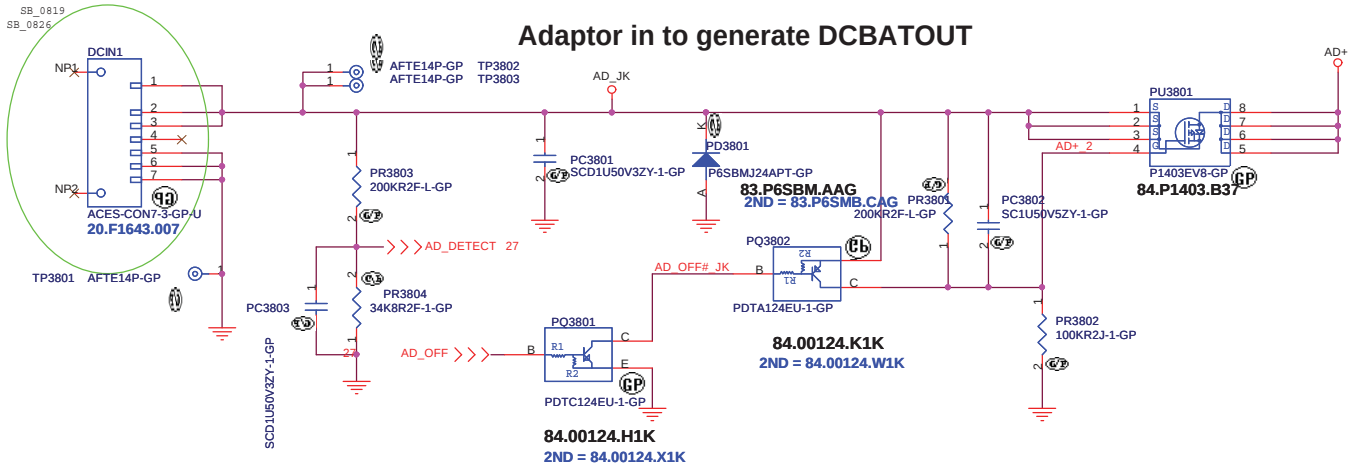
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
A3	LA470	SB

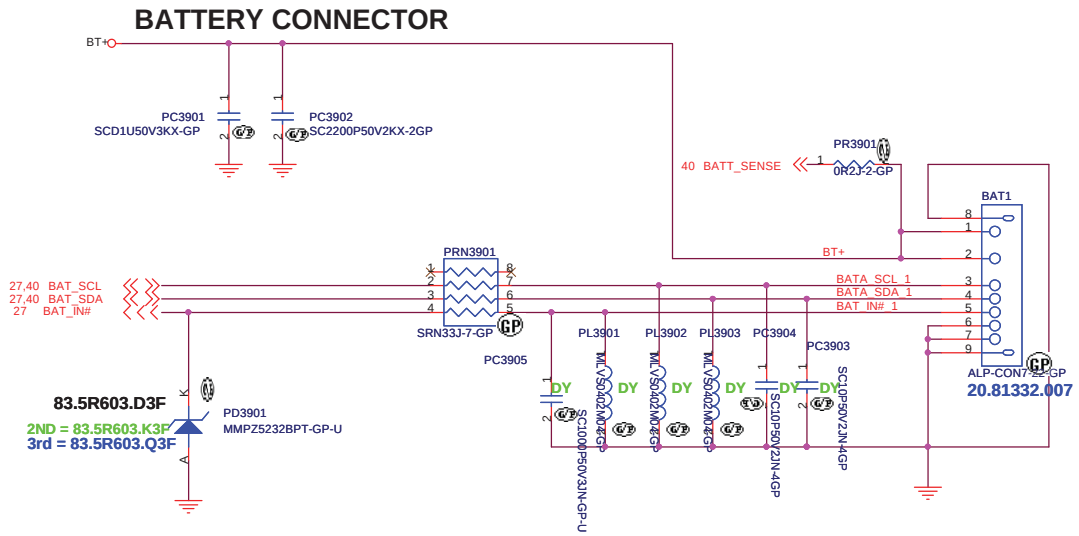
Date: Tuesday, September 07, 2010 Sheet 37 of 103

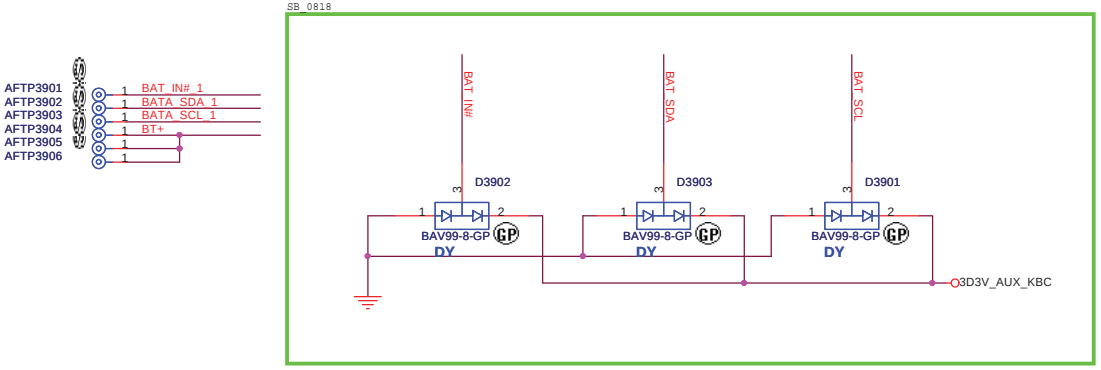


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DCIN_JACK***
Size	Document Number **LA470** Rev **SB**
Date: Tuesday, September 07, 2010	Sheet 38 of 103

BATTERY CONNECTOR





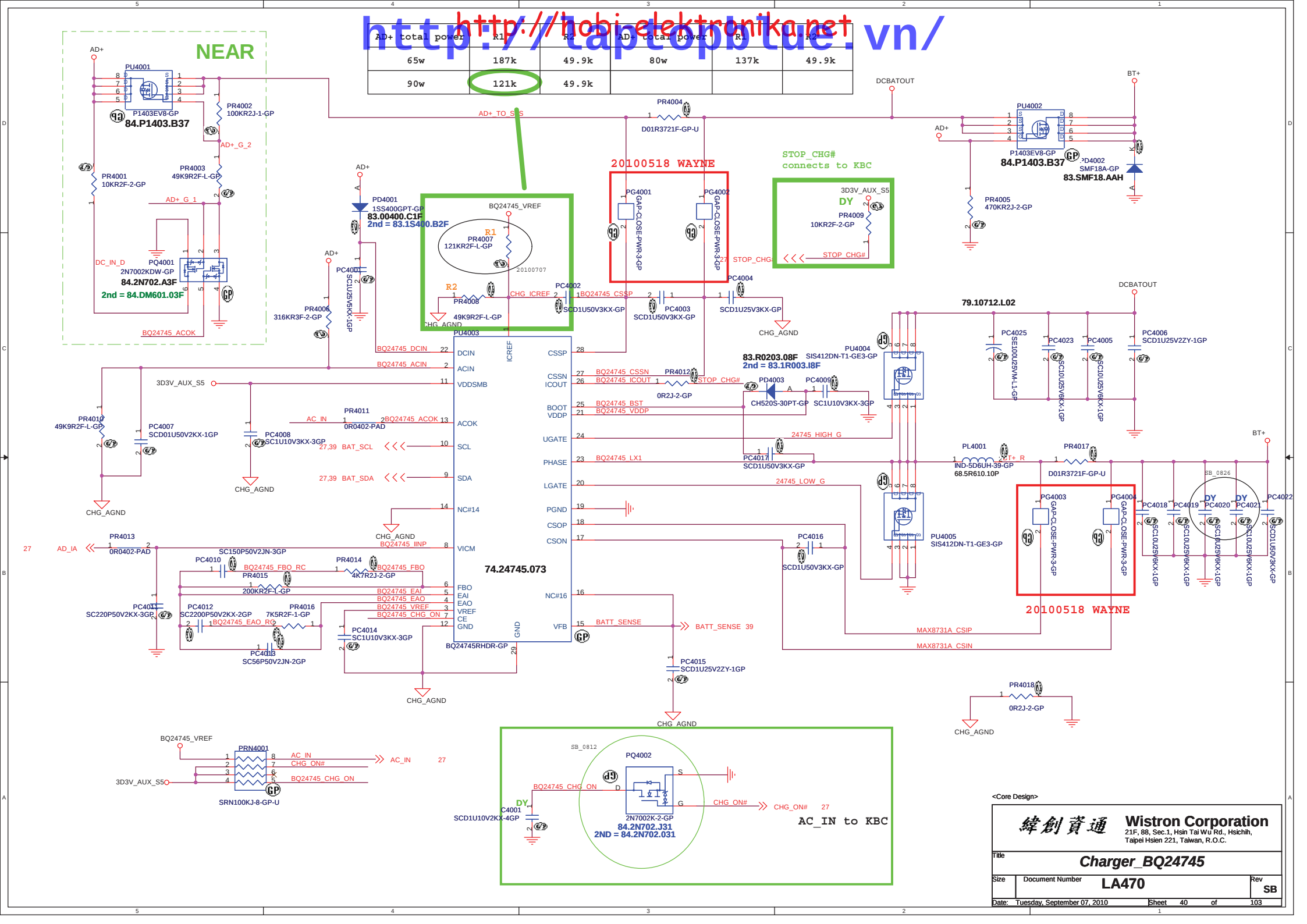
DY ???

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 39 of 103	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

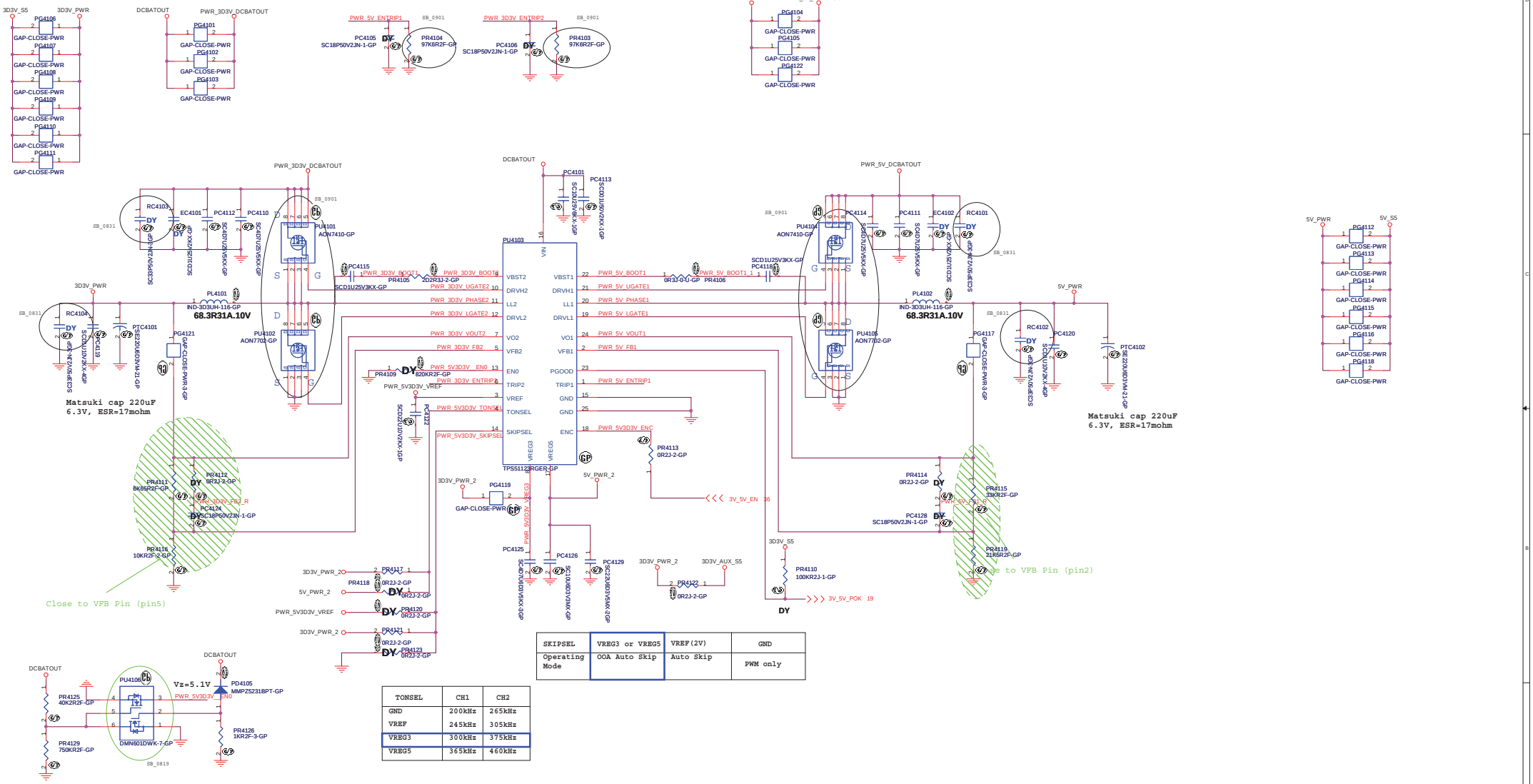


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Charger_BQ24745	
Size	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 40 of 103	

SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

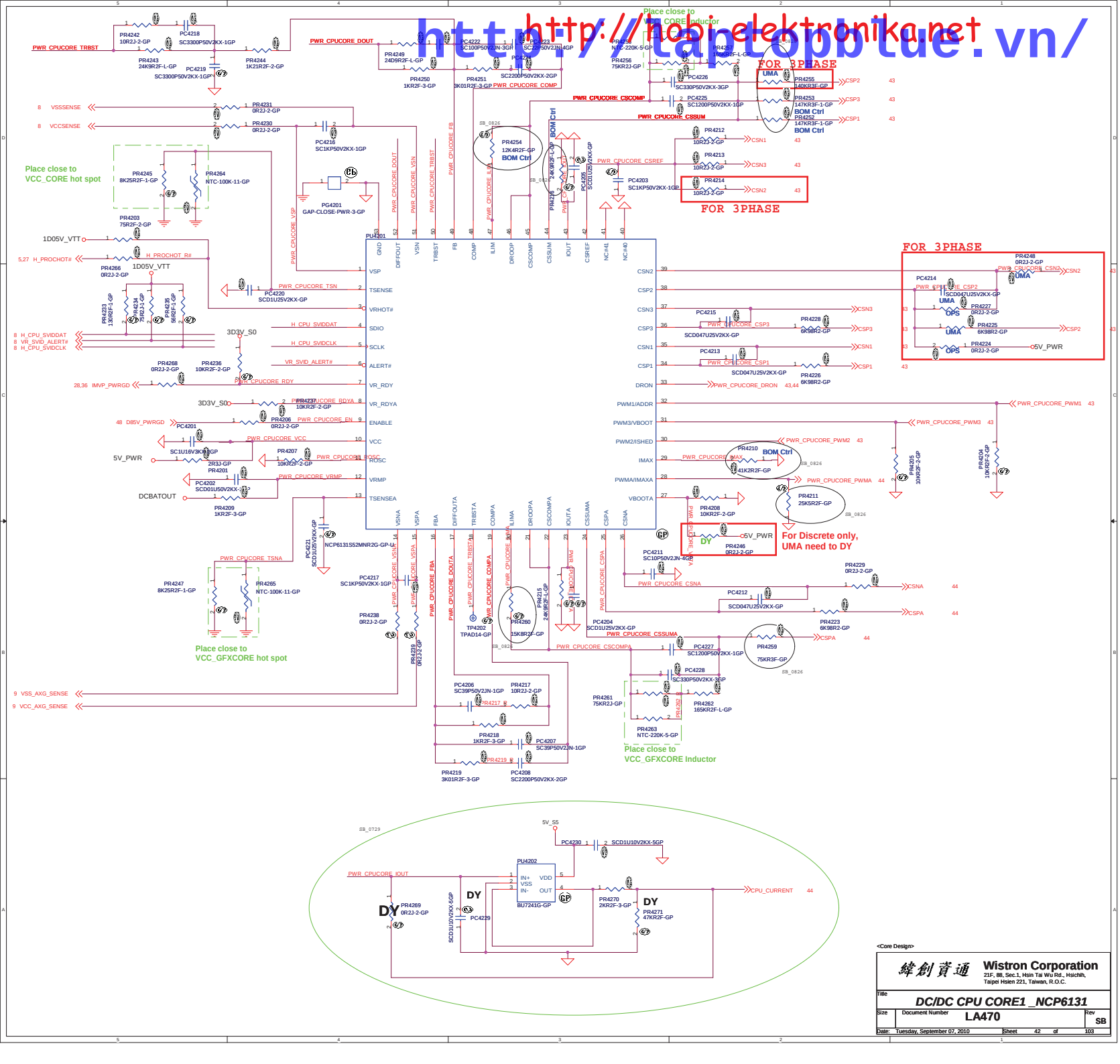
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size: | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 41 of 103



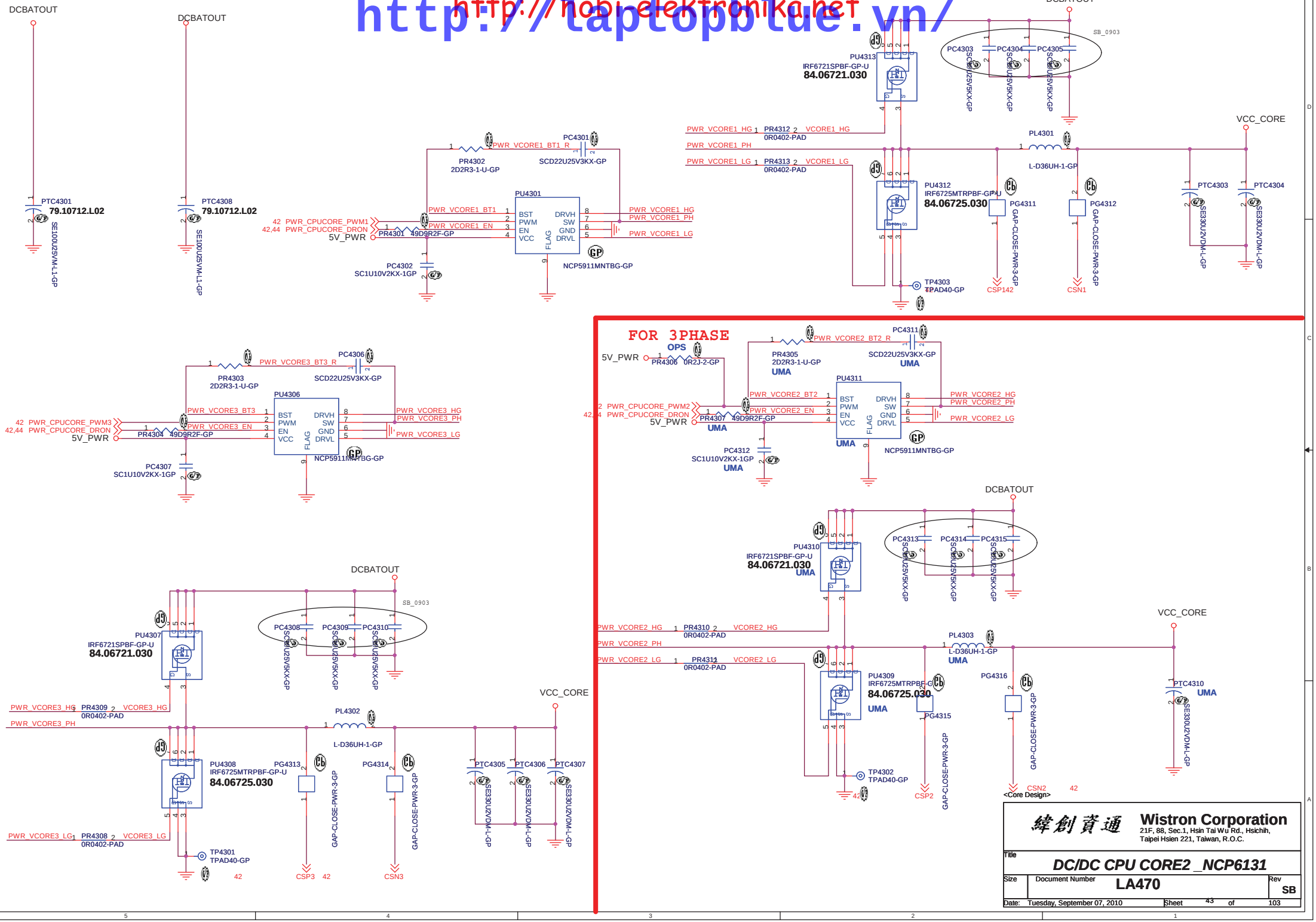
<Core Design>

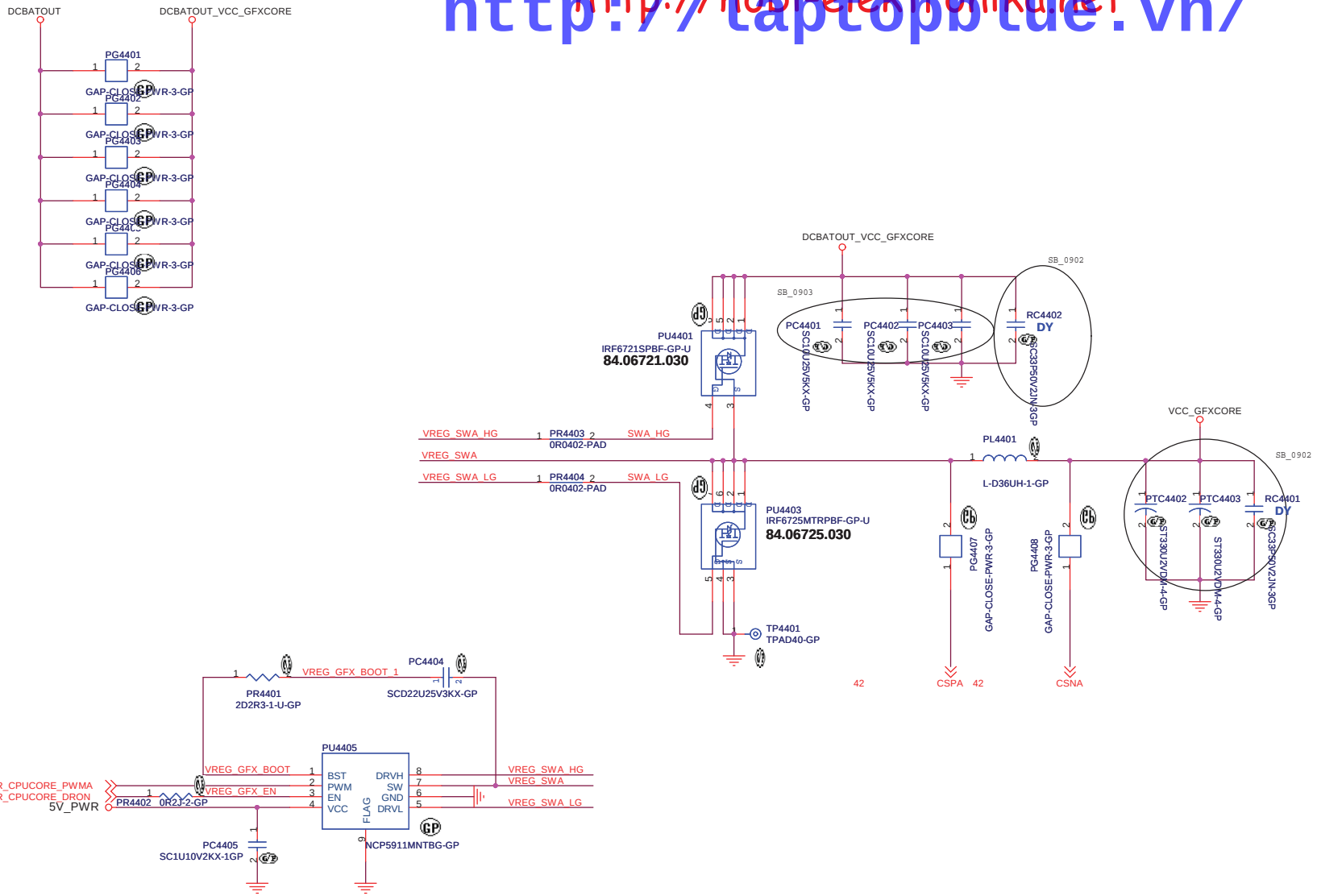
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC CPU CORE1 _NCP6131

Size	Document Number	Rev
	LA470	SB

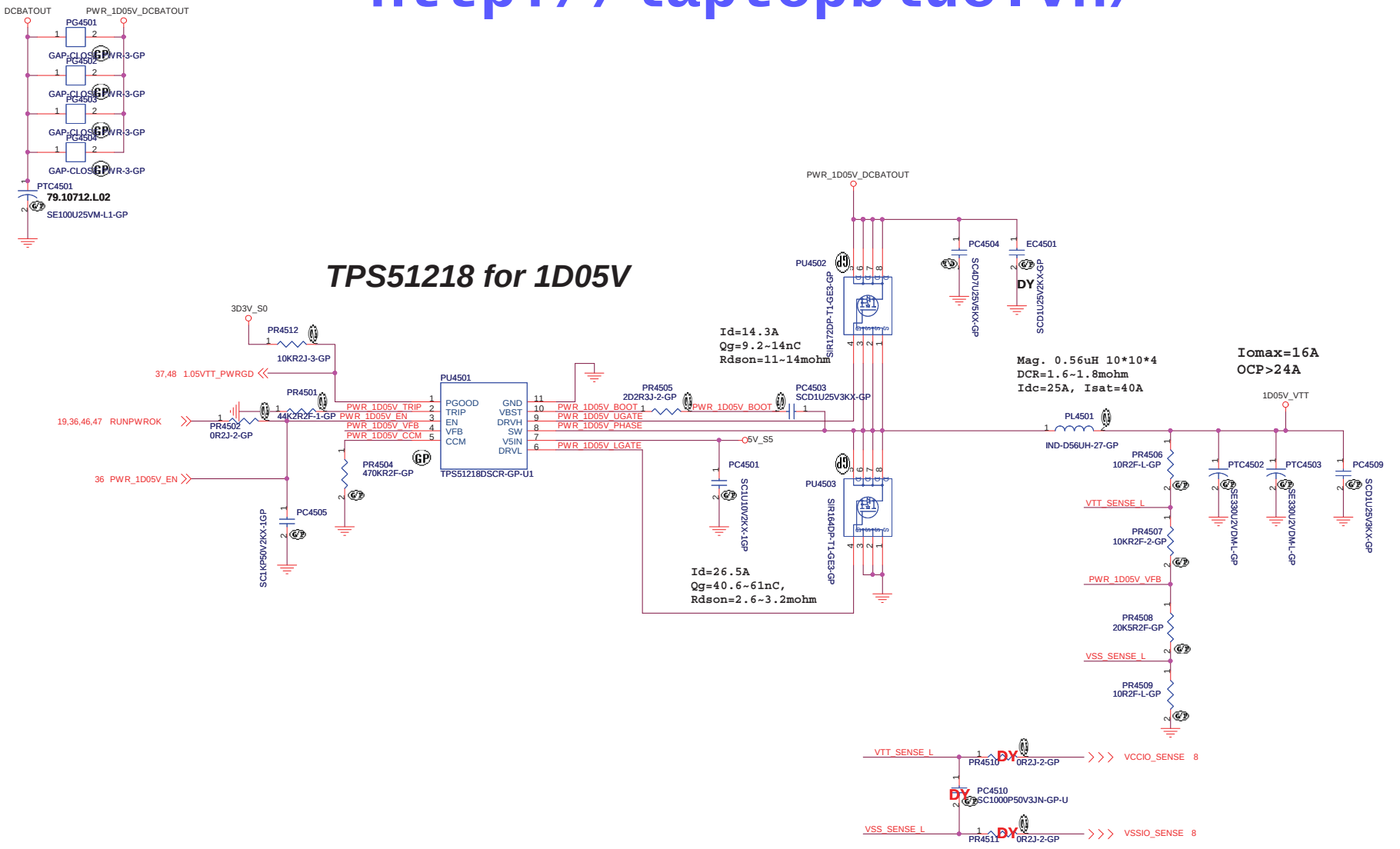
Date: Tuesday, September 07, 2010 Sheet 42 of 103





<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DC/DC CPU CORE3 _NCP6131***
Size / Document Number	**LA470**
Rev	**SB**
Date: Tuesday, September 07, 2010	Sheet 44 of 103

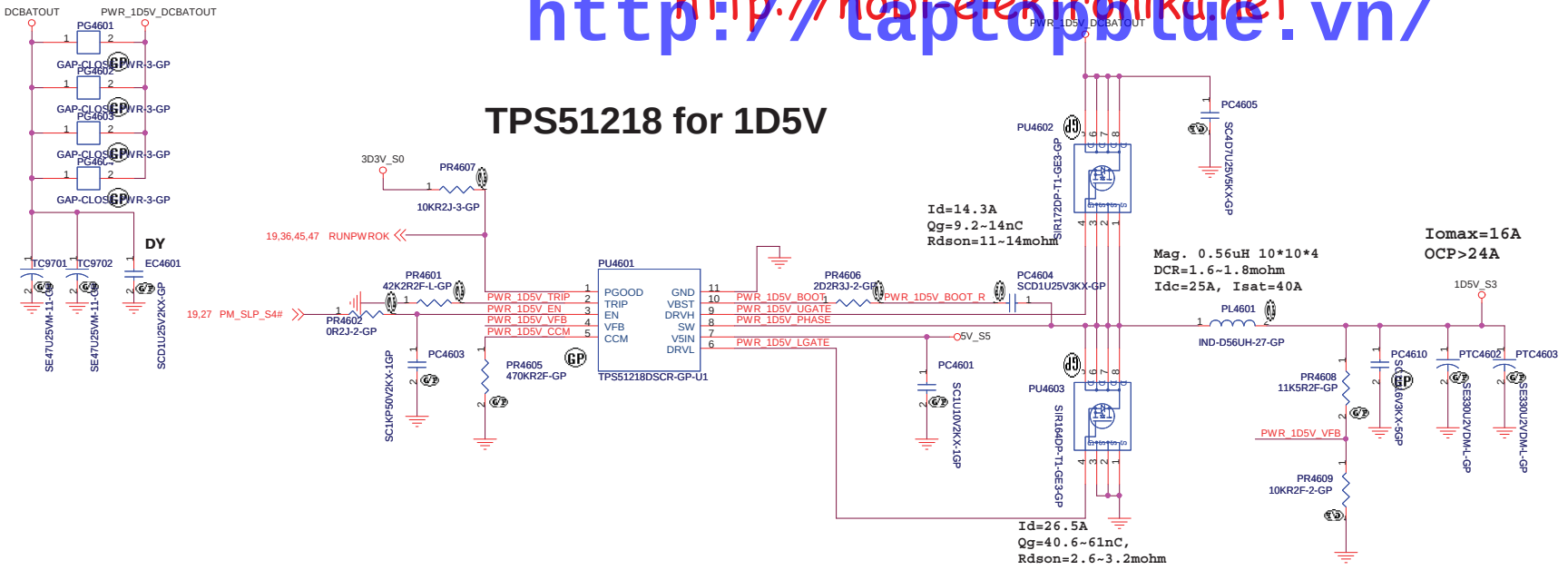


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

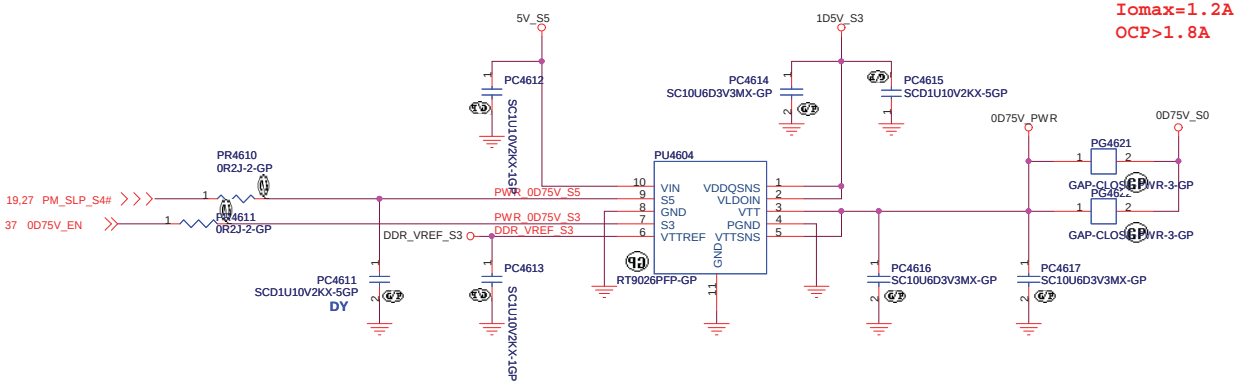
Title	TPS51218_1D05V	
Size	Document Number	Rev SB
Date: Tuesday, September 07, 2010	Sheet 45 of 103	

TPS51218 for 1D5V



Vout=0.704V*(R1+R2)/R2

RT9026 for 0D75V_S3



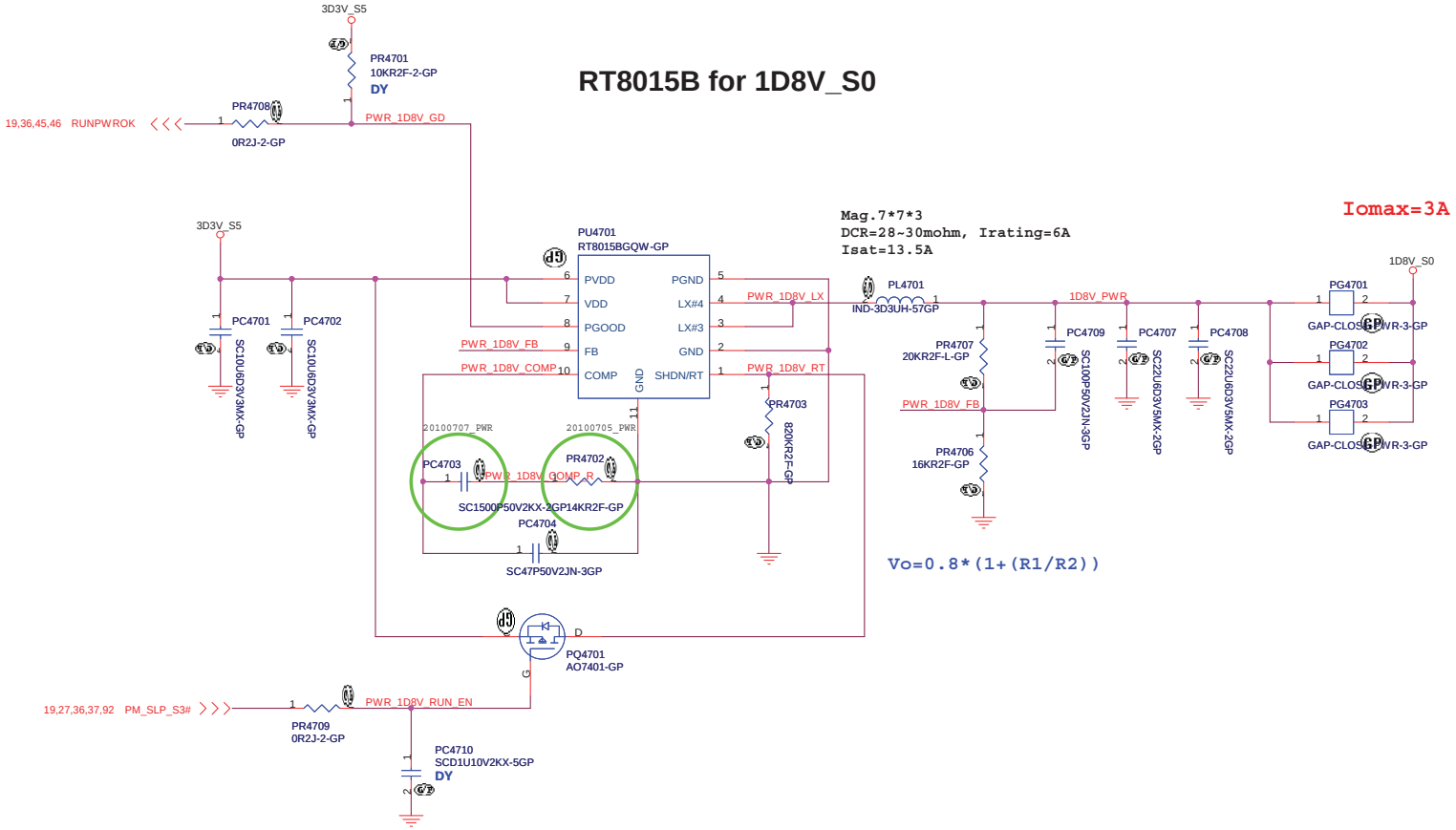
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SB

Date: Tuesday, September 07, 2010 Sheet 46 of 103

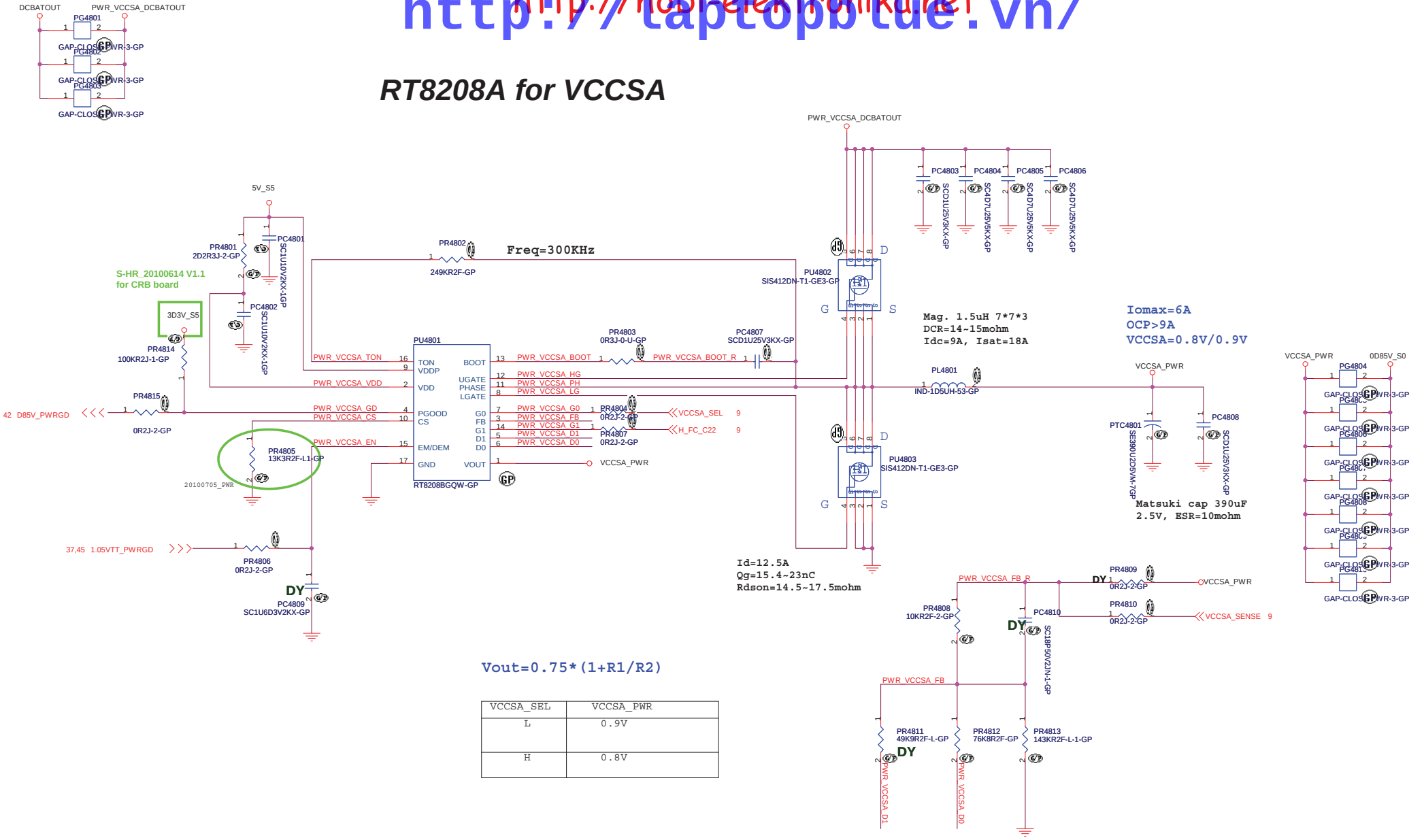


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT8015B	
Size	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 47 of 103	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

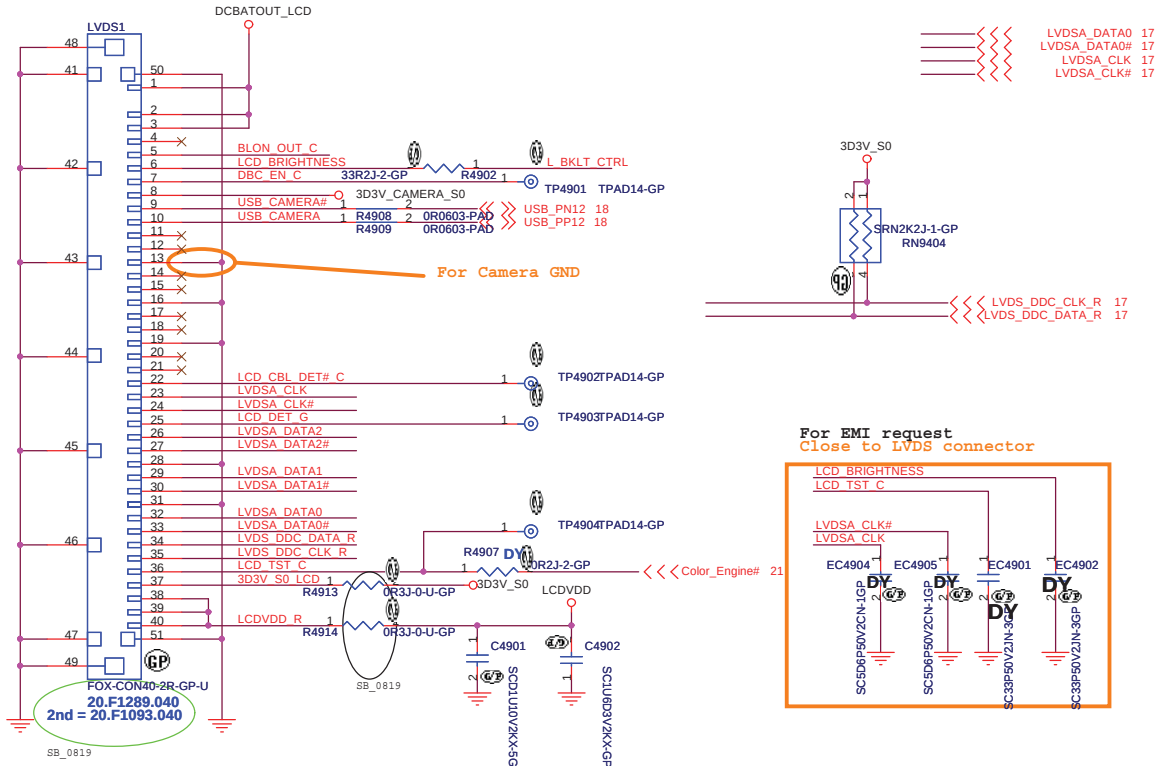
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

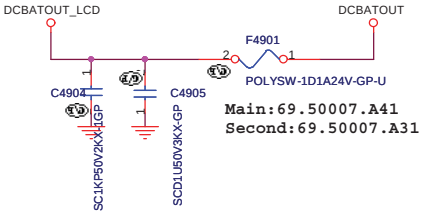
Title	RT8208B_VCCSA	
Size	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 48 of 103	

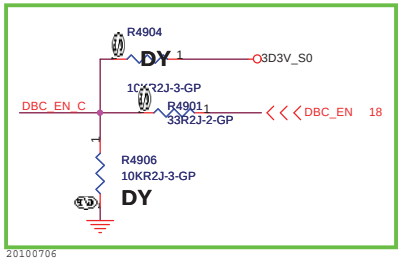
SSID = VIDEO

LVDS CONNECTOR

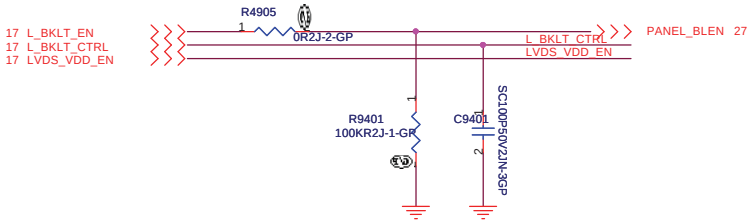


For EMI request
Close to LVDS connector

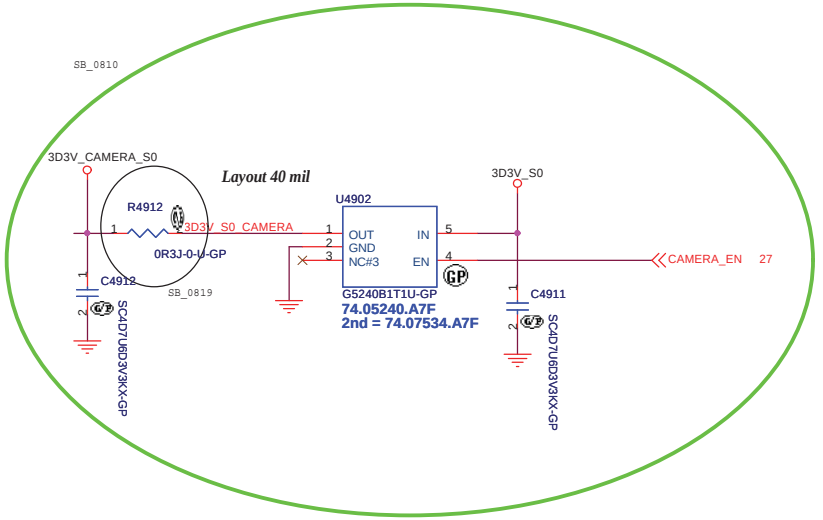




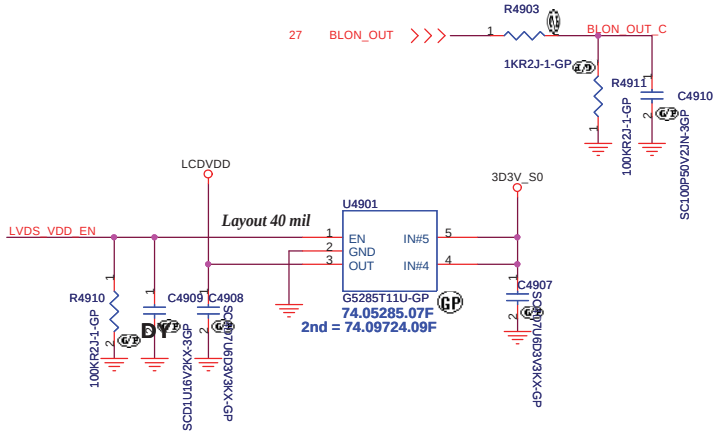
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



<Core Design>

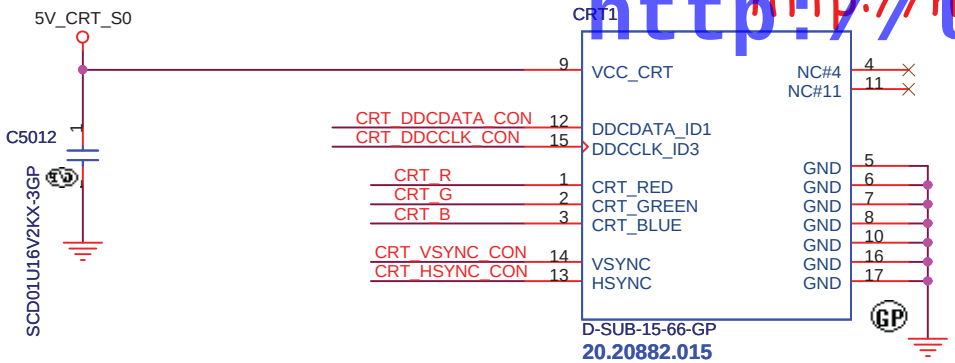
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

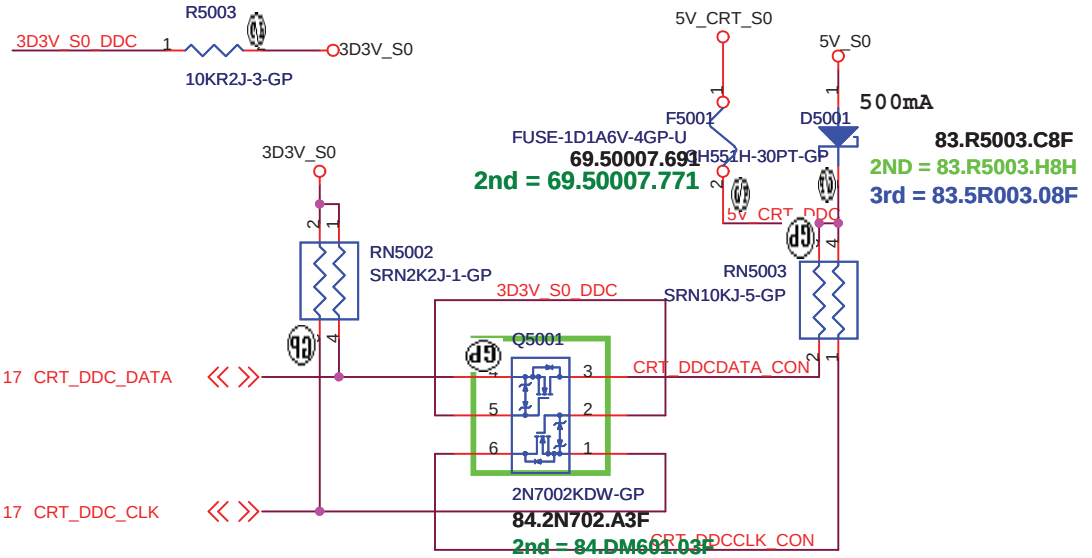
Title: LCD Connector

Size	Document Number	Rev
A3	LA470	SB

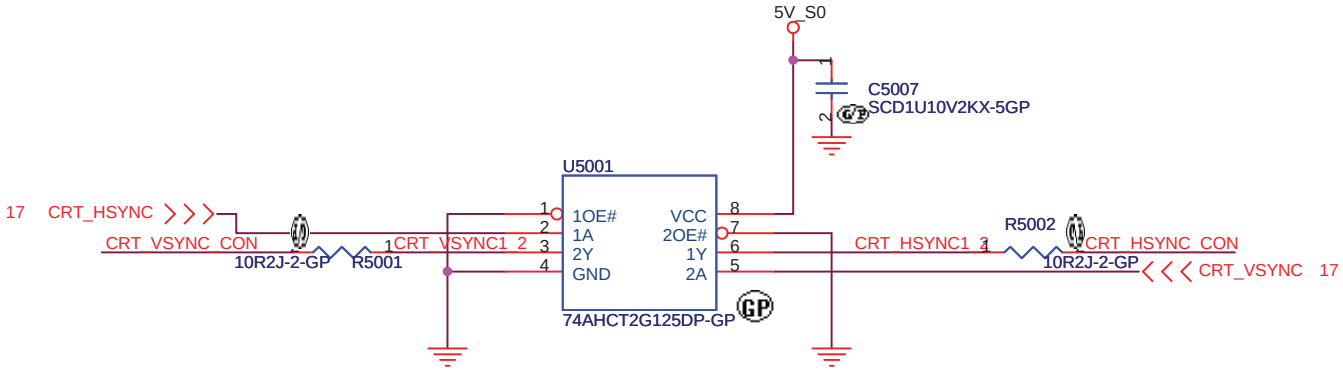
Date: Tuesday, September 07, 2010 Sheet 49 of 103

CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board

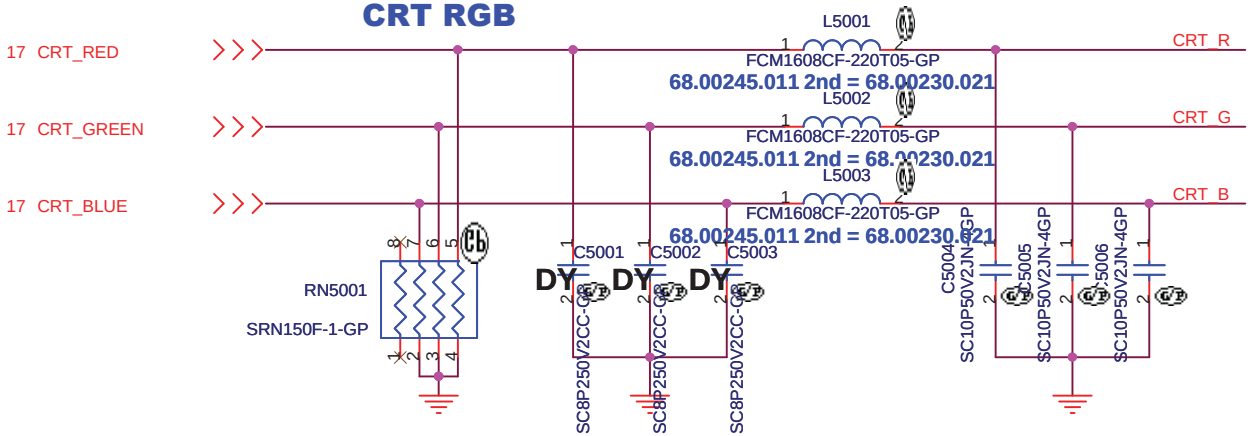


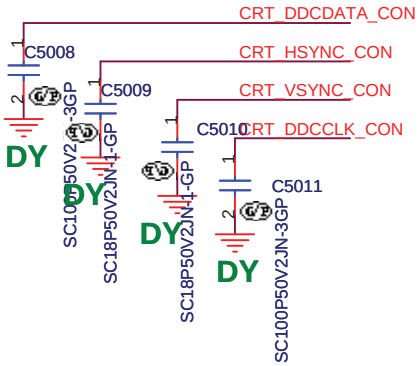


CRT Hsync & Vsync level shift



CRT RGB





<Core Design>

綽創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 50 of 103

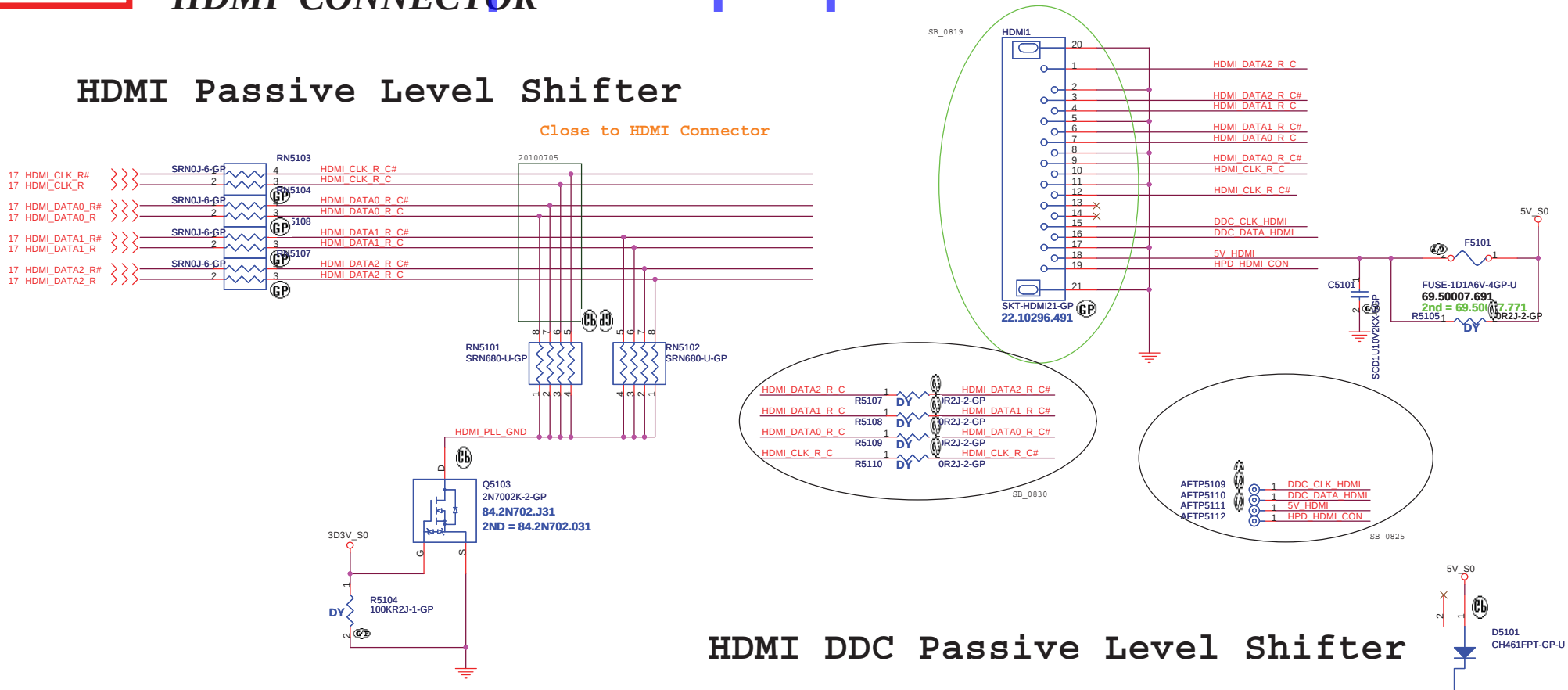
SSID = VIDEO

HDMI CONNECTOR

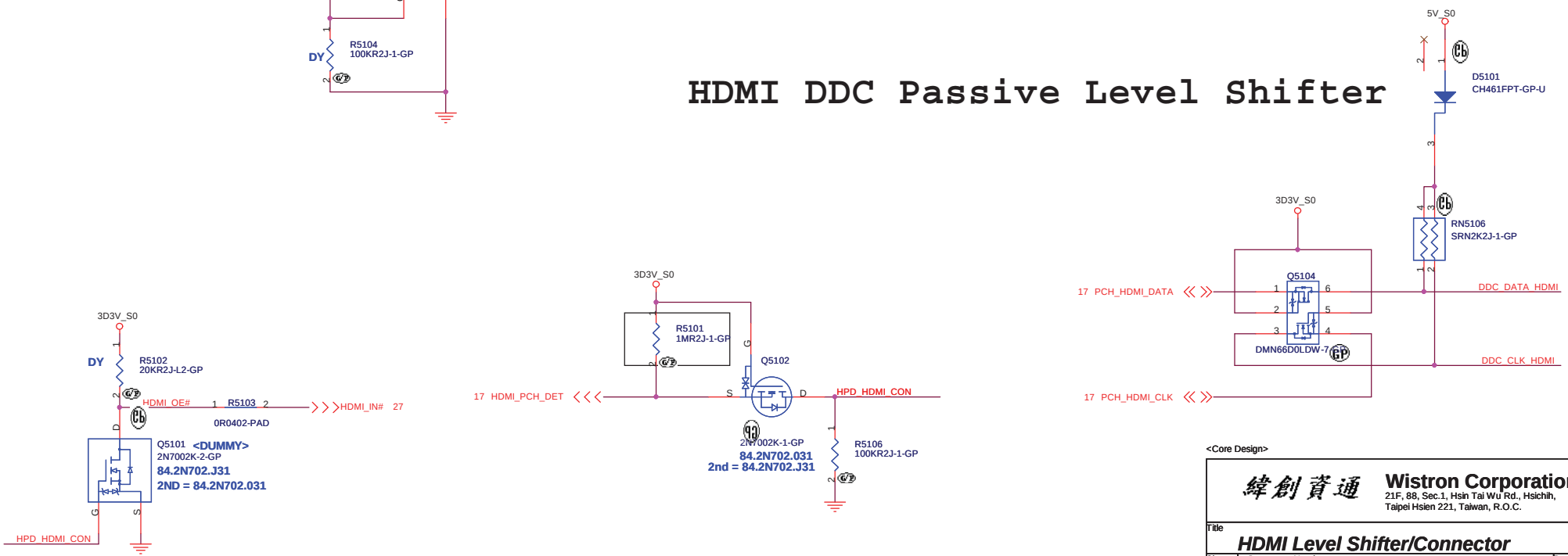
HDMI_CONN

HDMI Passive Level Shifter

Close to HDMI Connector



HDMI DDC Passive Level Shifter



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI Level Shifter/Connector		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 51 of 103	

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 52 of 103	

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***		
Size: A4	Document Number: **LA470**	Rev: **SB**
Date: Tuesday, September 07, 2010	Sheet 53 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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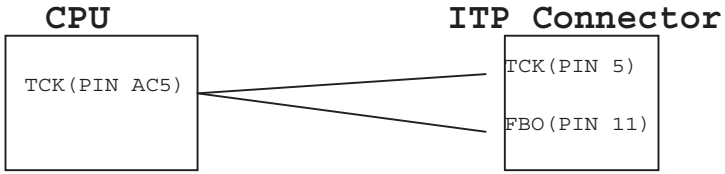
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



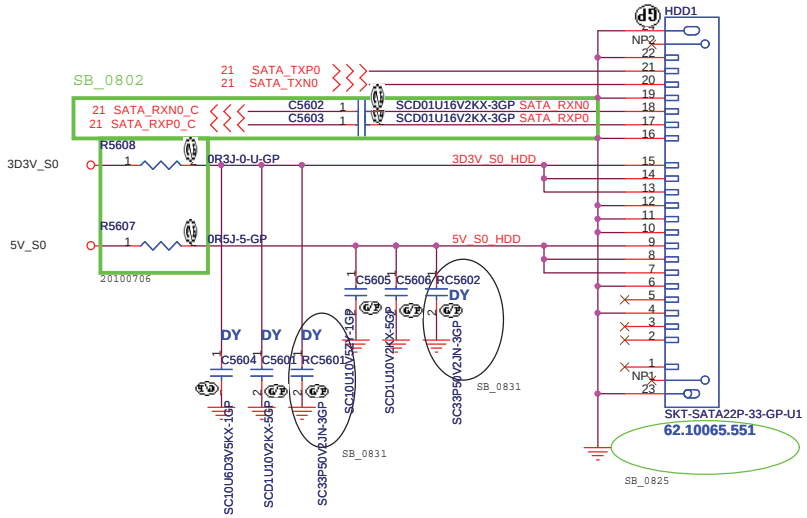
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

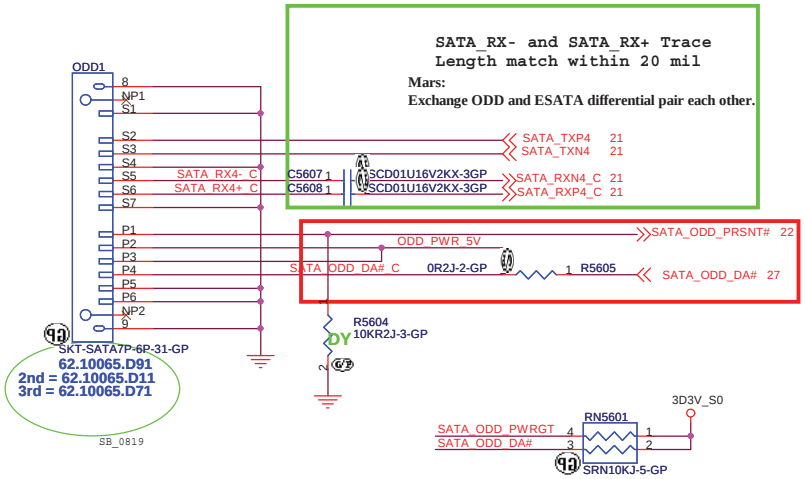
Title: ITP		
Size: A4	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 55 of 103	

SSID = SATA

SATA HDD Connector

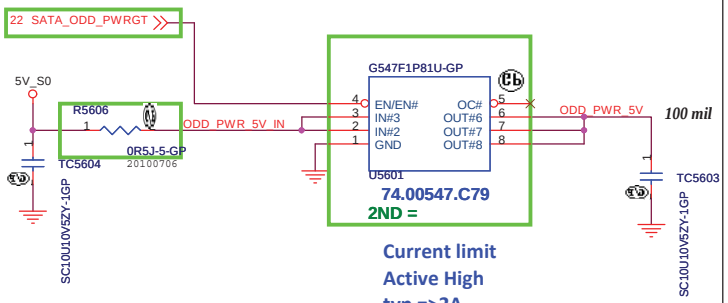


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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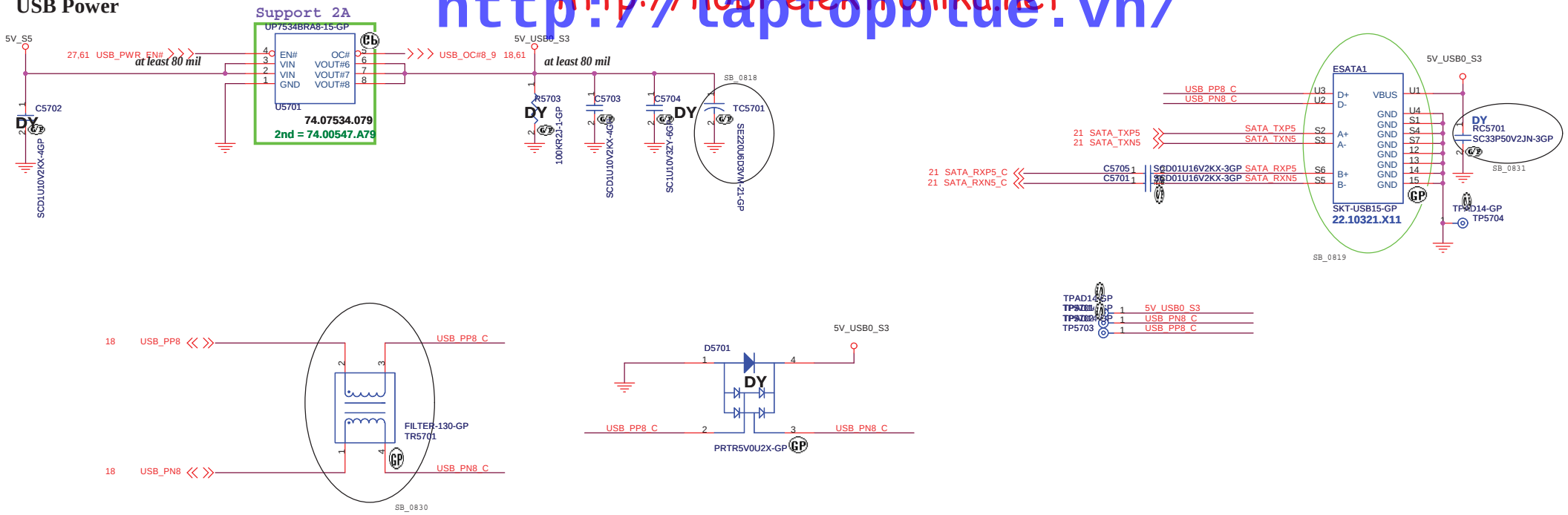
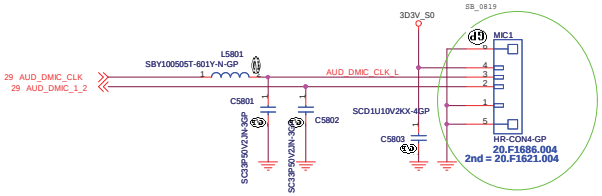
USB Power

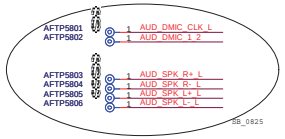


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

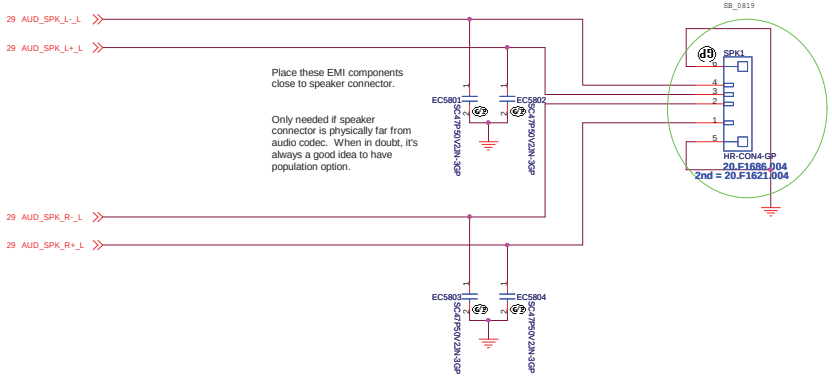
Title	E-SATA	
Size A3	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 57 of 103	





INTERNAL STEREO SPEAKERS

Port G



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
A2	LA470	SB

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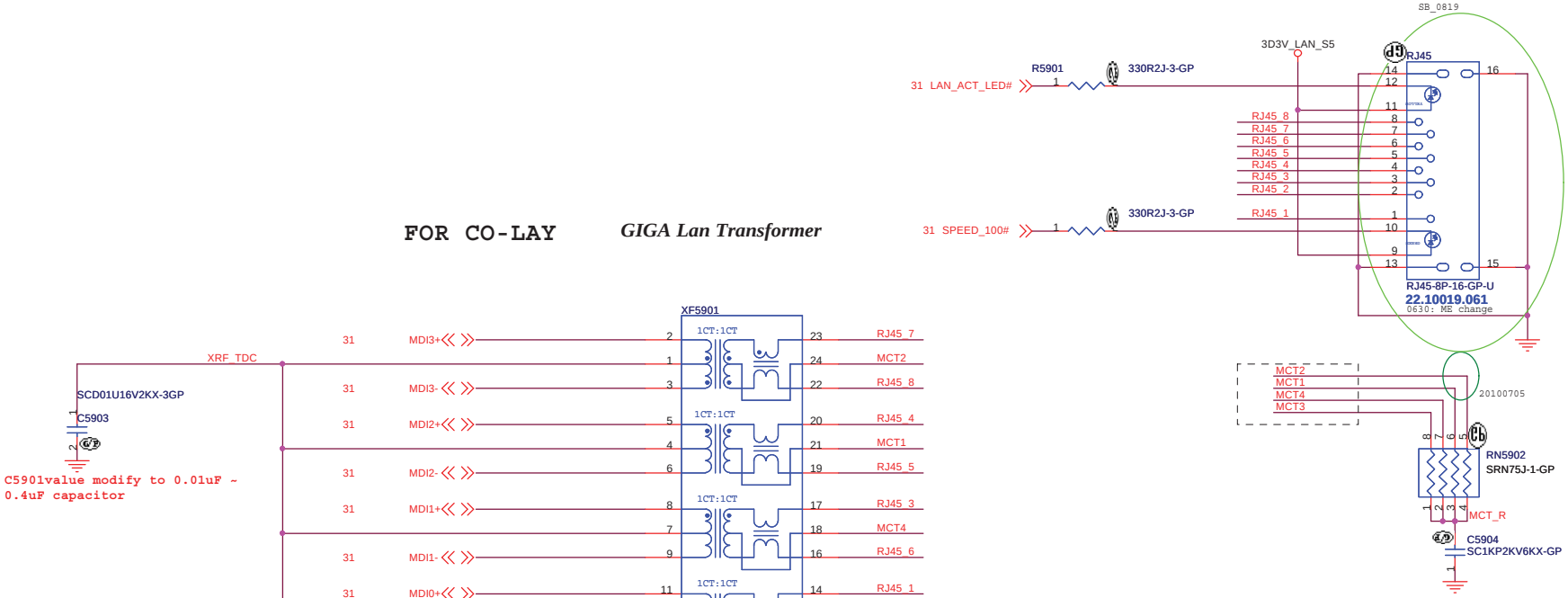
LAN Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45 / Transformer		
Size: A3	Document Number: LA470	Rev: SB
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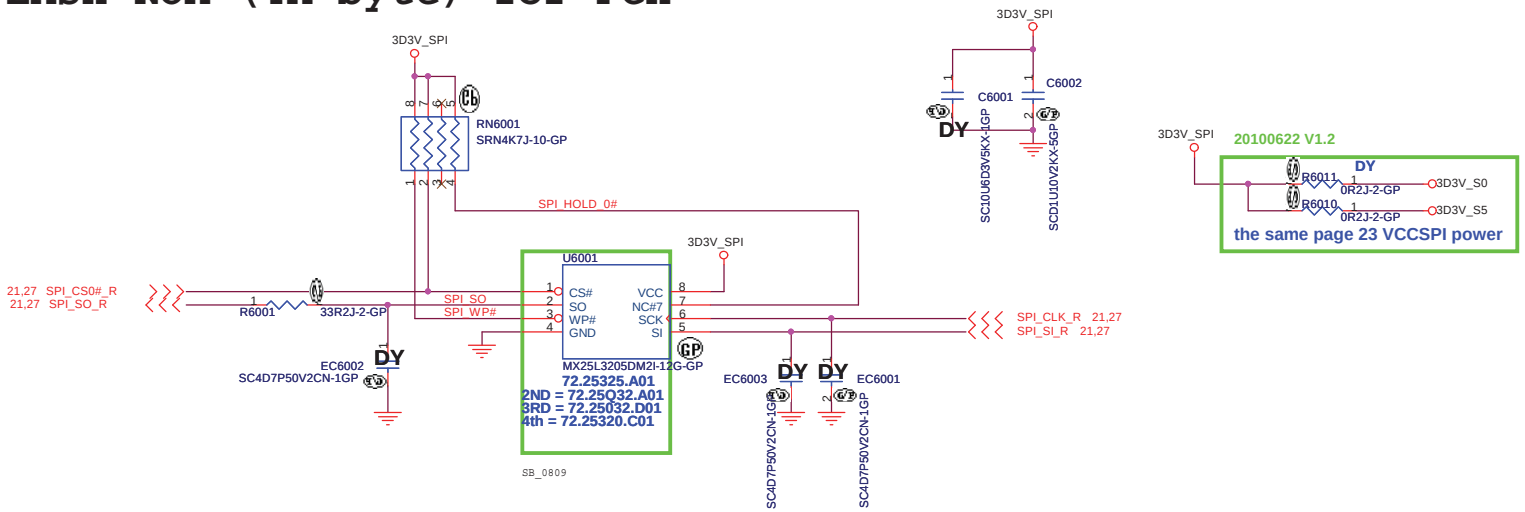
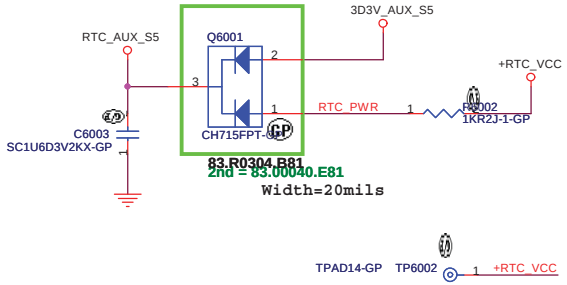
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
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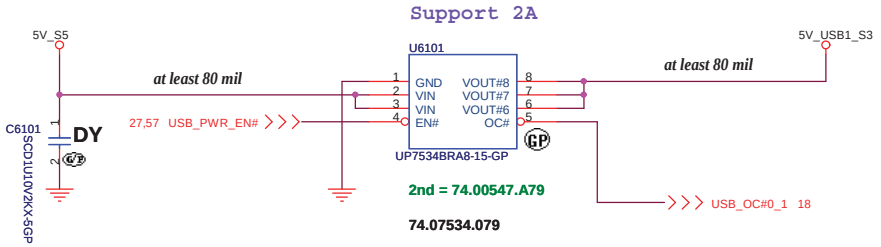
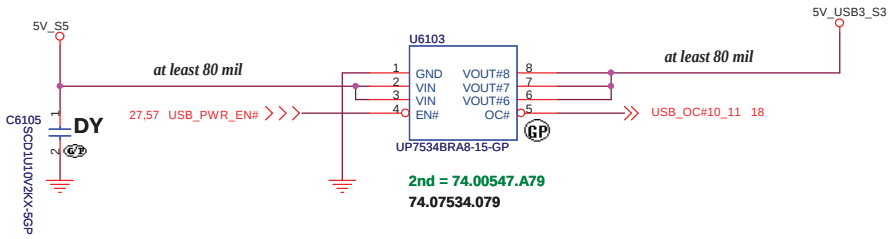
SSID = USB

IO Board USB Power



Sub-USB Board Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size	Document Number	Rev
A3	LA470	SB

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB 3.0 Port

Size	Document Number	Rev
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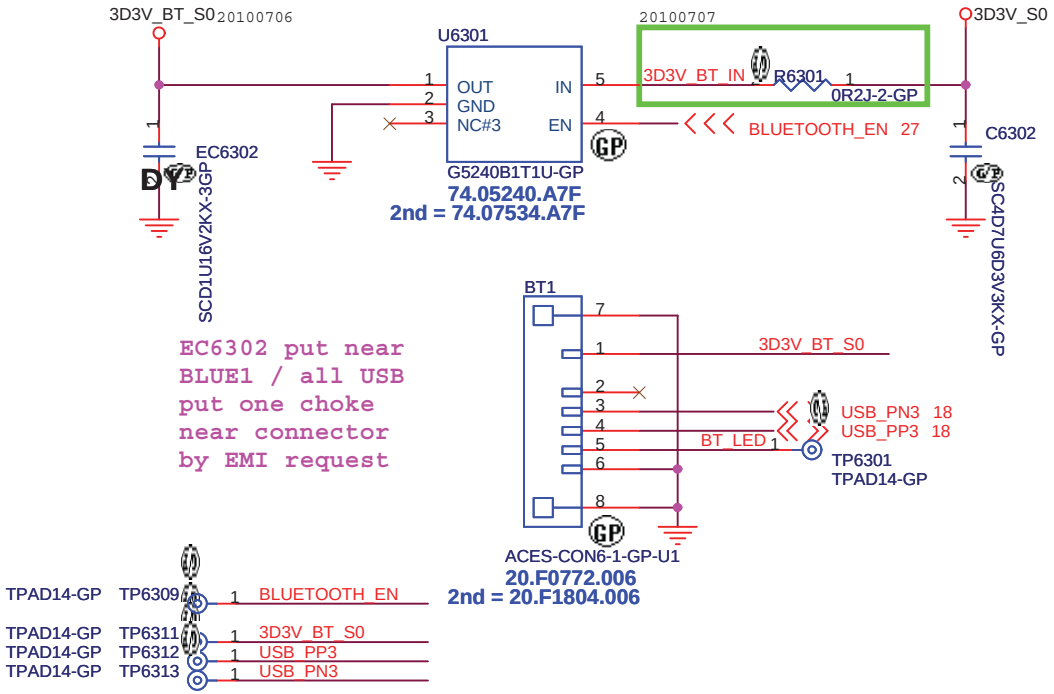
Date: Tuesday, September 07, 2010 Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

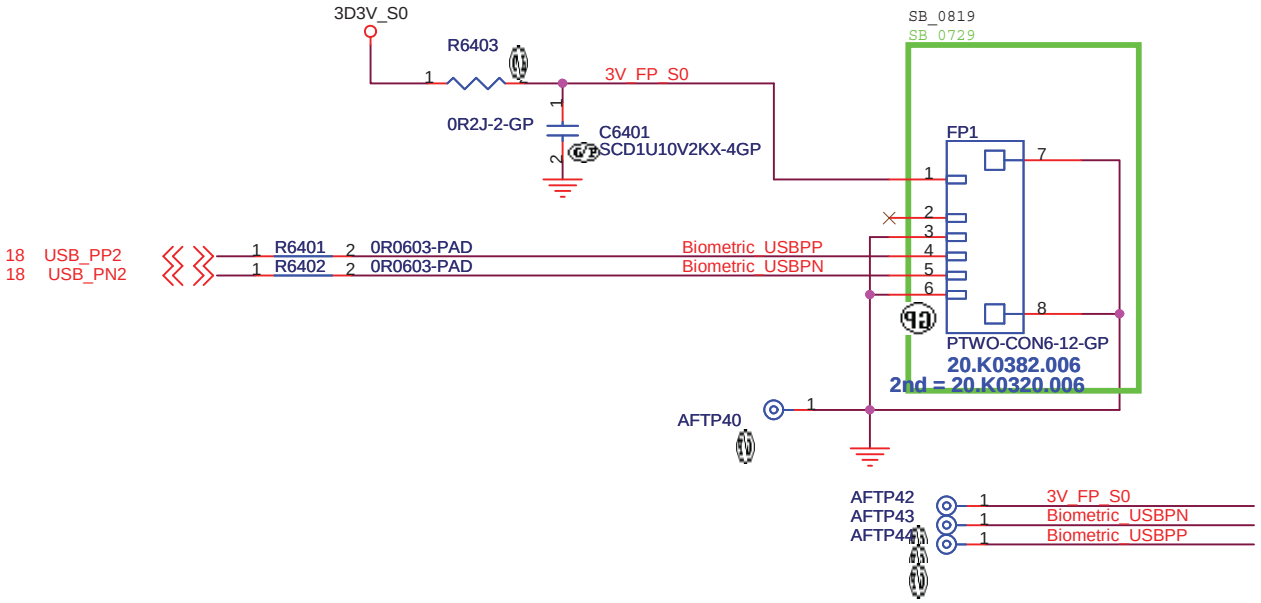
Bluetooth Module



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Bluetooth		
Size: A4	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 63 of 103	

Finger Printer Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

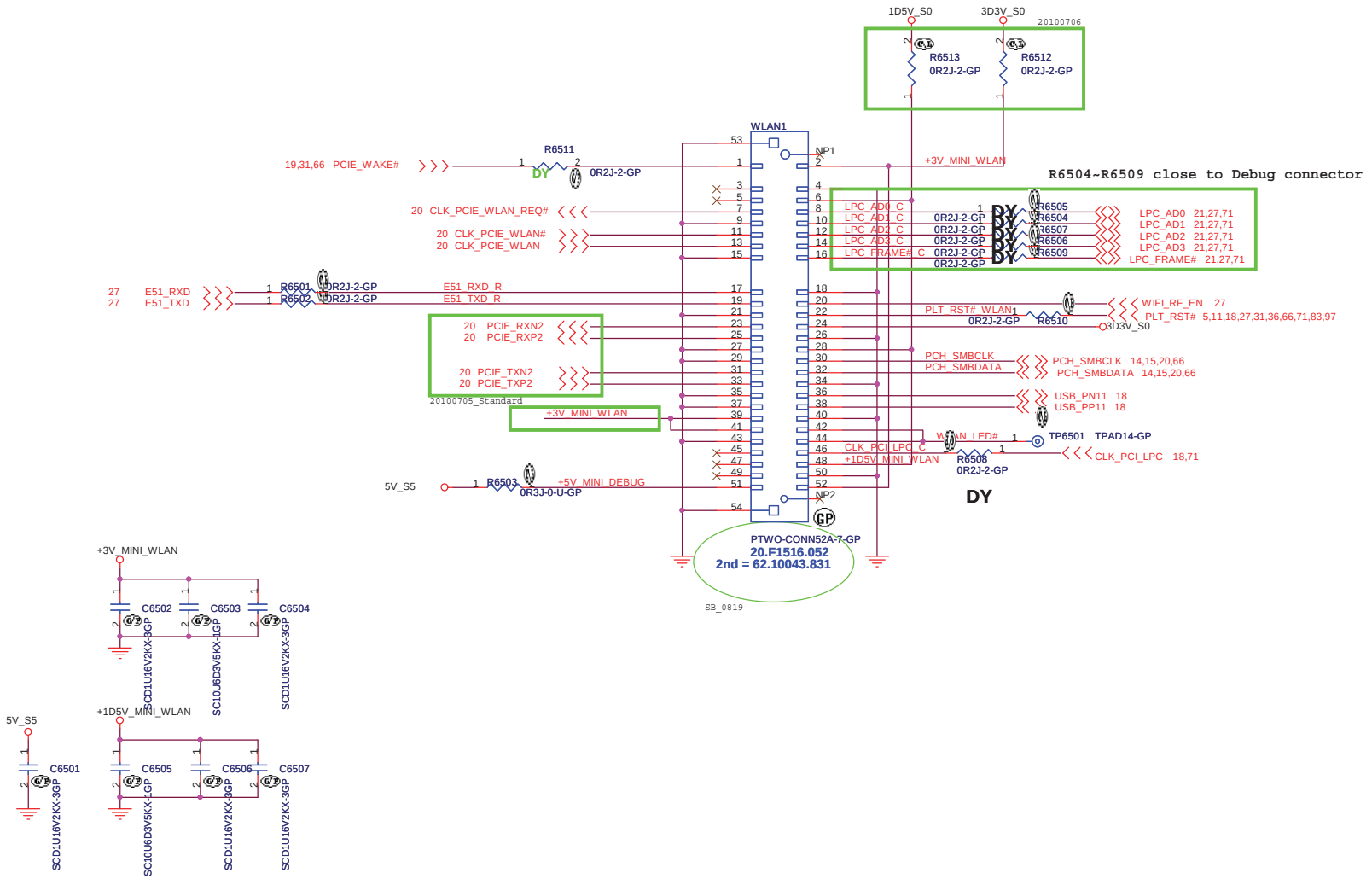
Title: **RESERVED**

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

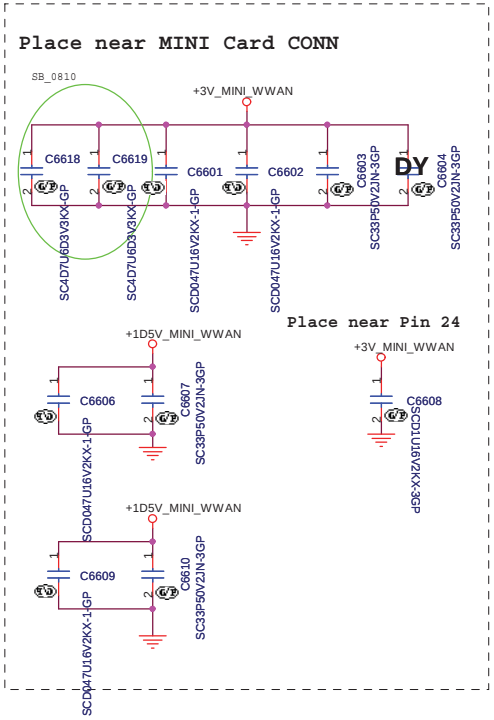


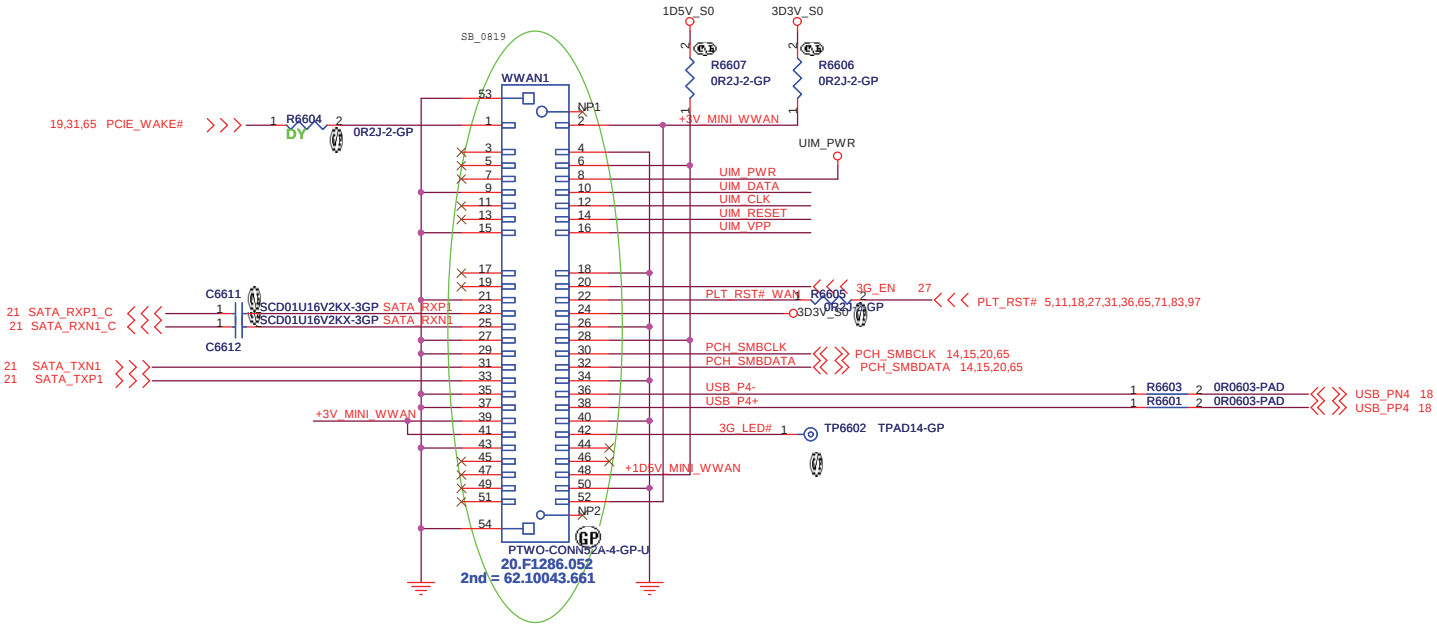
<Core Design>

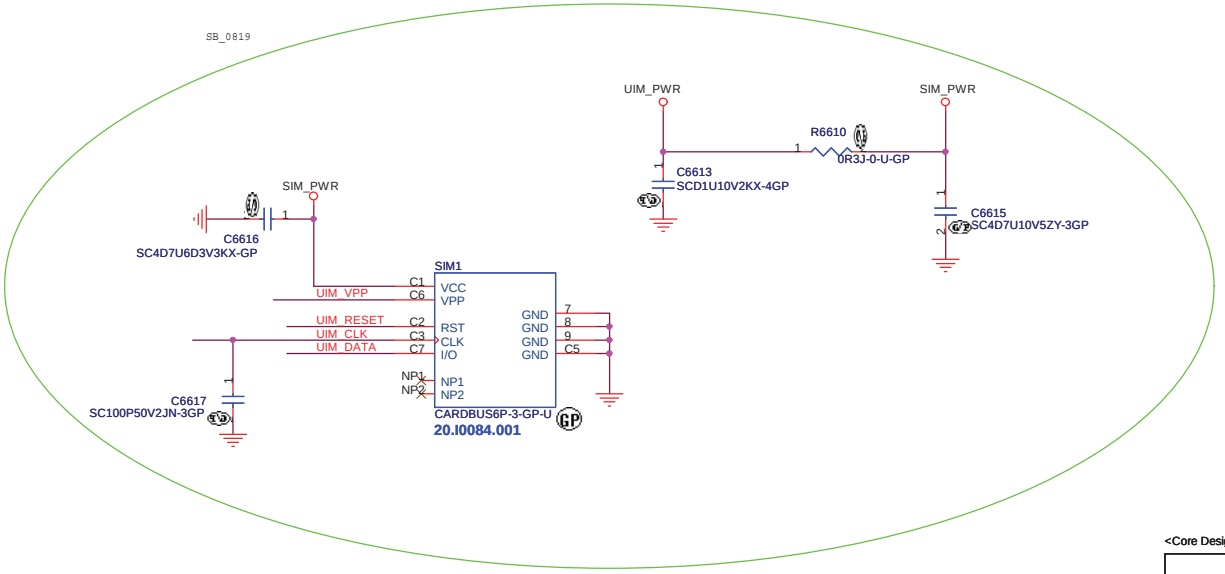
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MINICARD(WLAN)/ITP CONN
Size A3 / Document Number	LA470
Rev	SB
Date: Tuesday, September 07, 2010	Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
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Date: Tuesday, September 07, 2010 Sheet 66 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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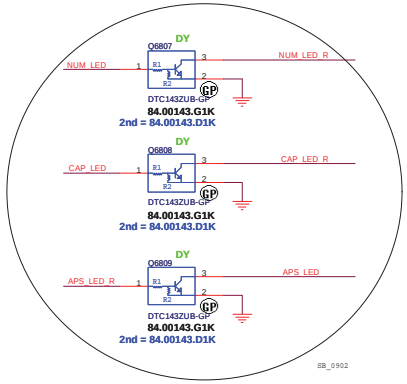
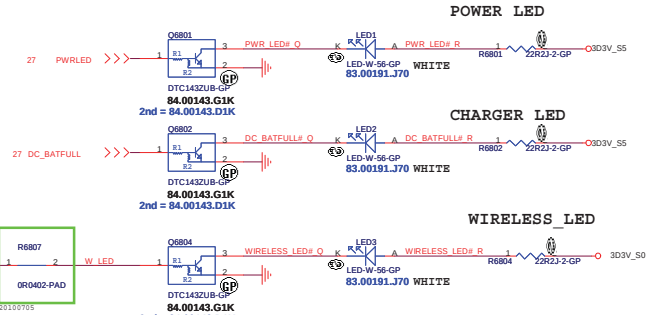
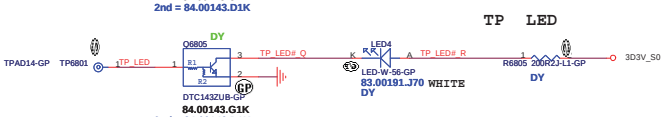
Date: Tuesday, September 07, 2010 Sheet 67 of 103

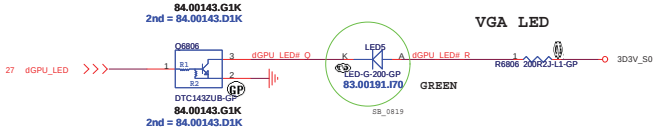
SSID = User.Interface

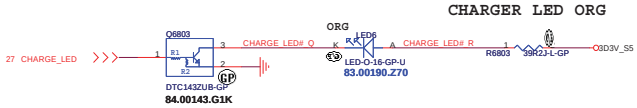
Power button LED



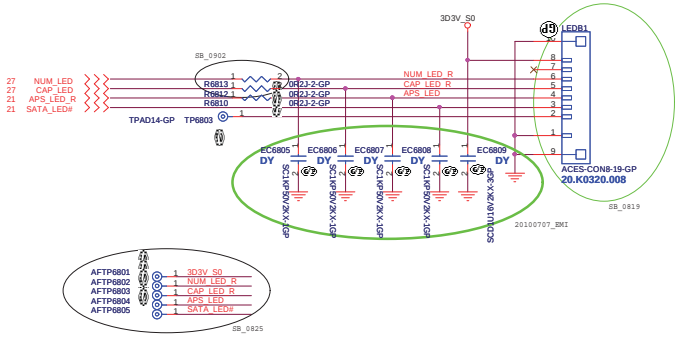


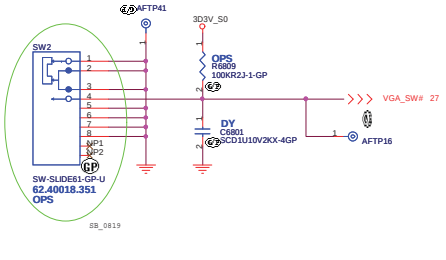


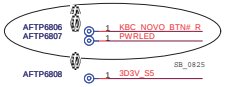




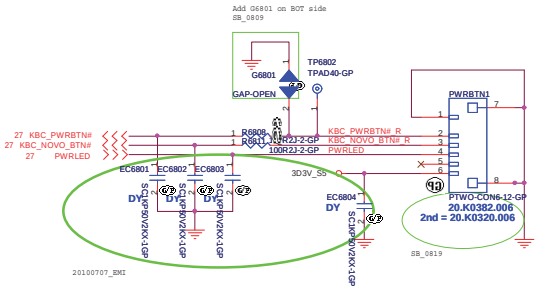
LED Bord CONN.







Power button LED(White)



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size: A2 | Document Number: LA470 | Rev: SB

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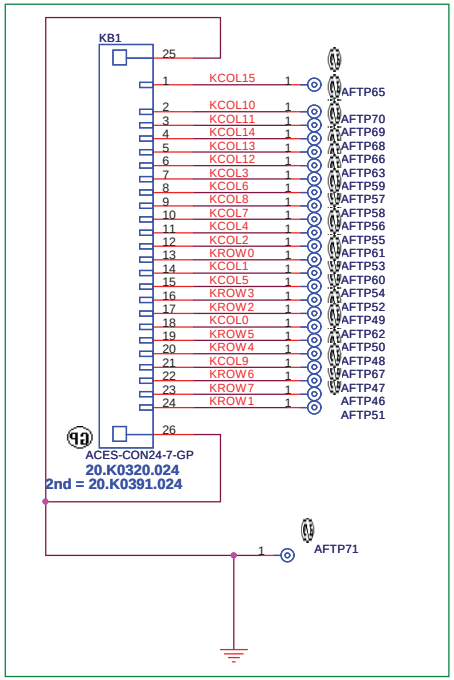
SSID = KBC

SSID = TouchPad

Internal KeyBoard Connector



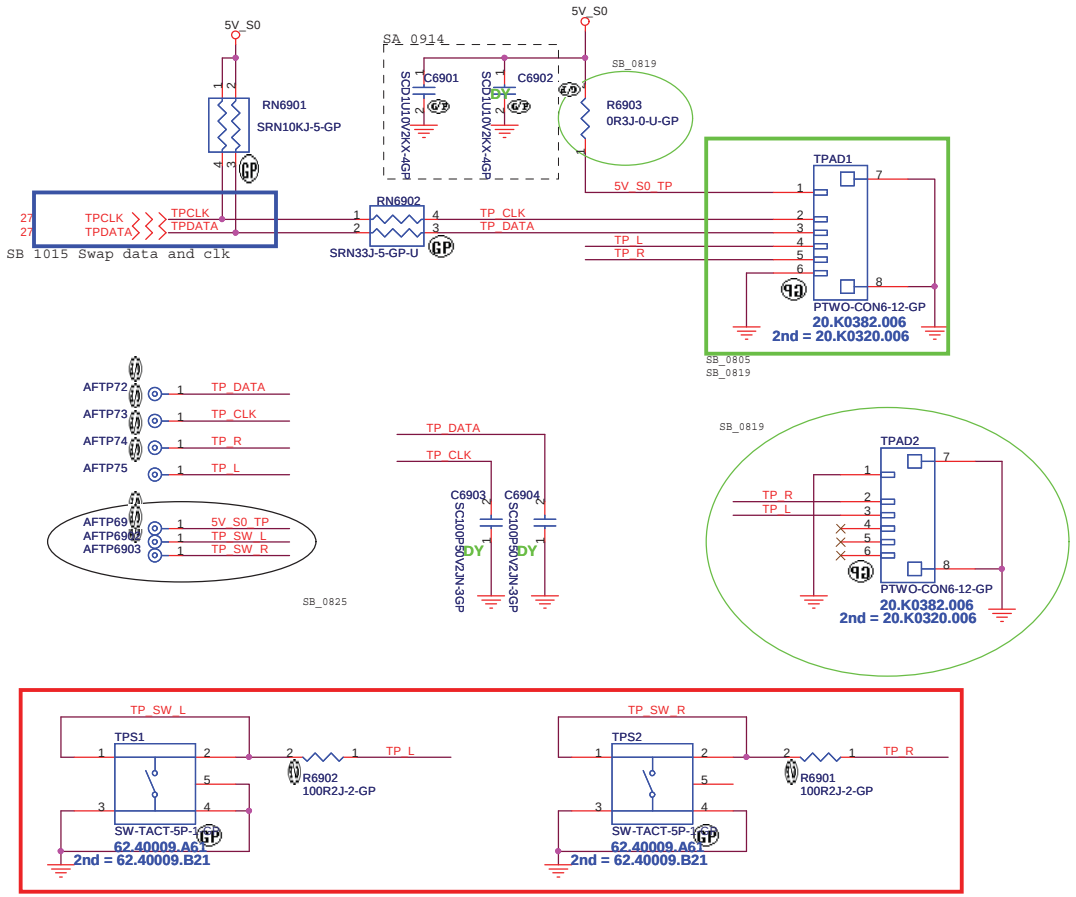
KROW[0..7] 27

KCOL[0..15] 27

20100705

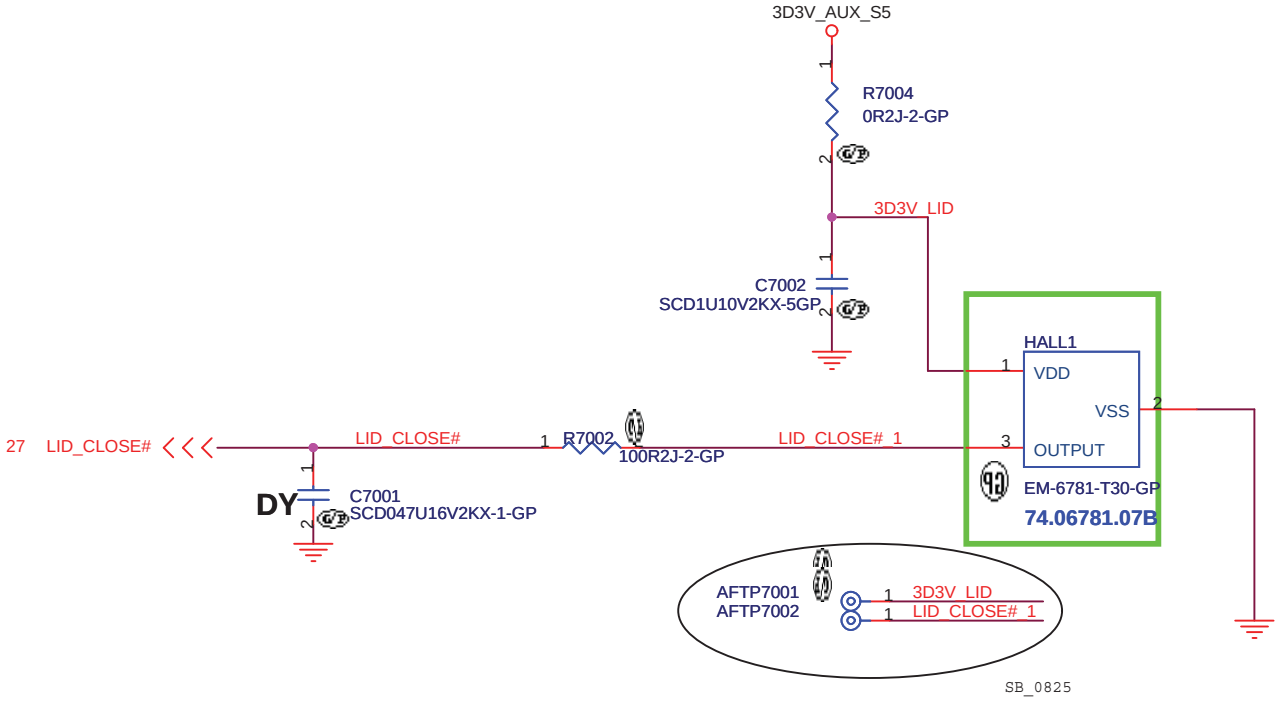
* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8



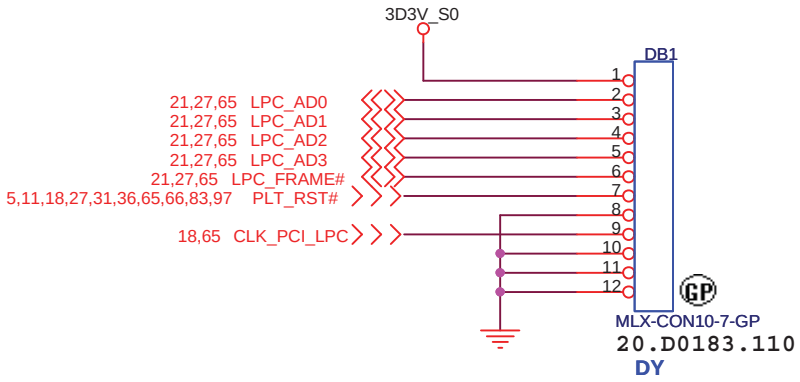
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Key Board/Touch Pad***
Size A3	Document Number **LA470** Rev **SB**
Date: Tuesday, September 07, 2010	Sheet 69 of 103



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *Hall Sensor*	
Size: A4	Document Number: LA470 — Rev: SB
Date: Tuesday, September 07, 2010	Sheet 70 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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A4	LA470	SB

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<Core Design>

緯創資通 Wistron Corporation
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Title: *Reserved*

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Title: CARD Reader CONN

Size	Document Number	Rev
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<Core Design>

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Title: New Card		
Size: A3	Document Number: LA470	Rev: SB
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Title: ***Reserved***

Size	Document Number	Rev
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Title: ***Reserved***

Size	Document Number	Rev
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Title: ***Reserved***

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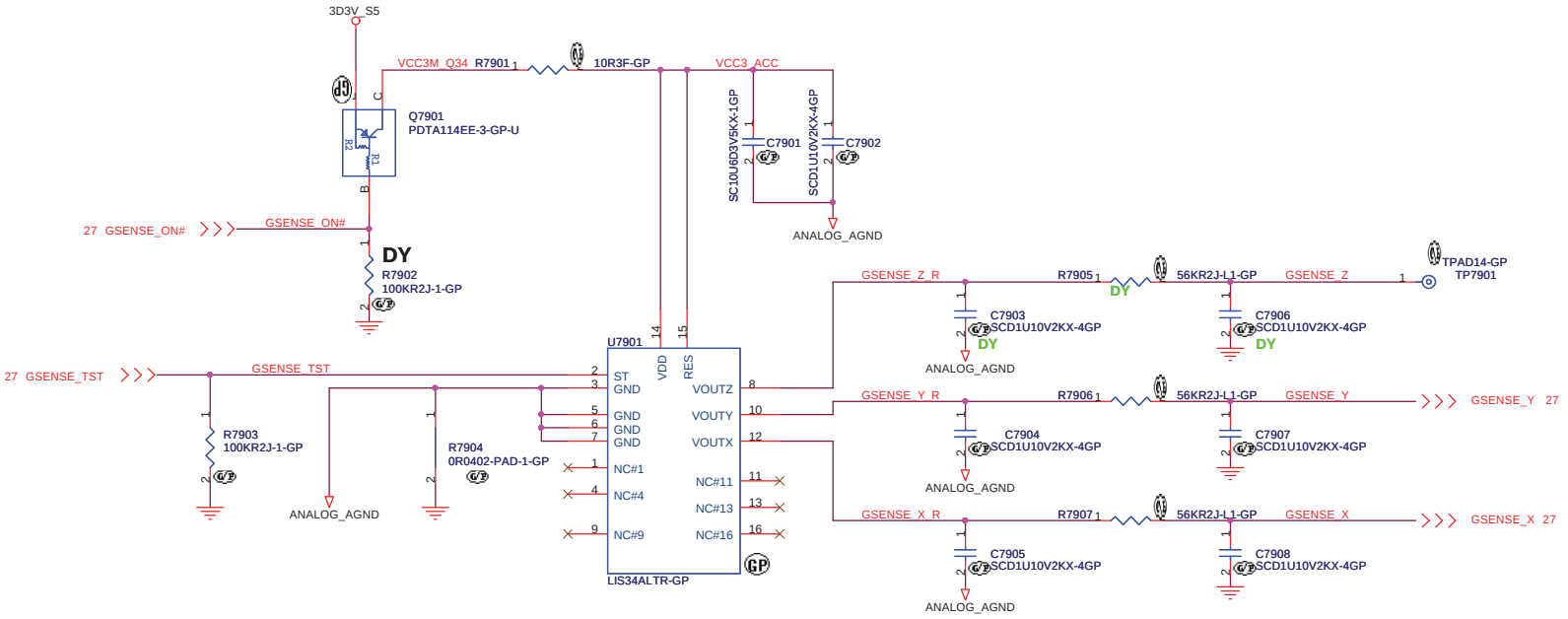
G-Sensor



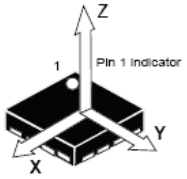
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Core Design>

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Title: **G-Sensor**

Size: Custom | Document Number: **LA470** | Rev: **SB**

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Title: ***Reserved***

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Title: ***Reserved***

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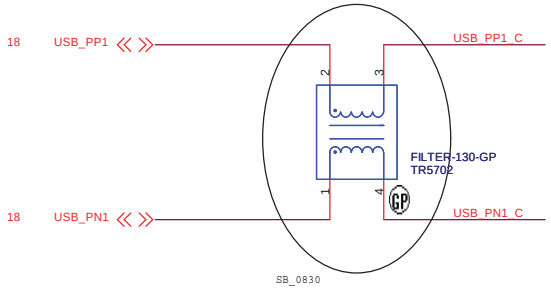
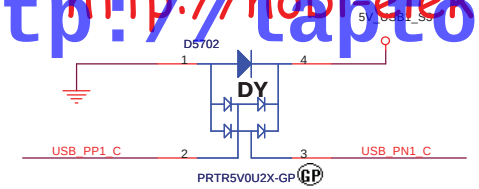
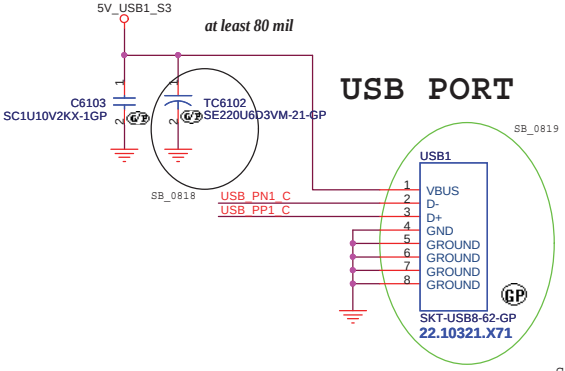
IO Board CONN 80 pin

USB1



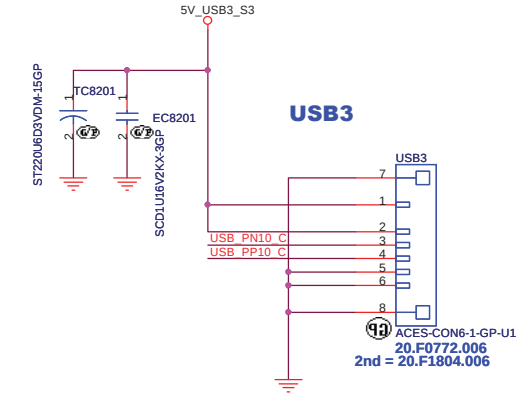


USB PORT

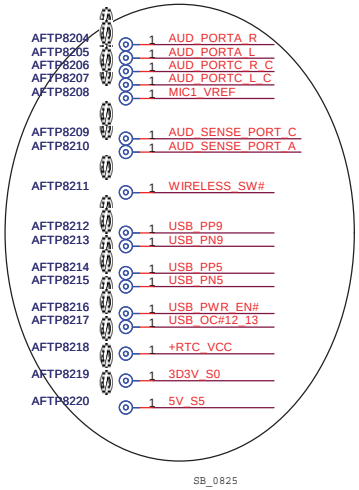


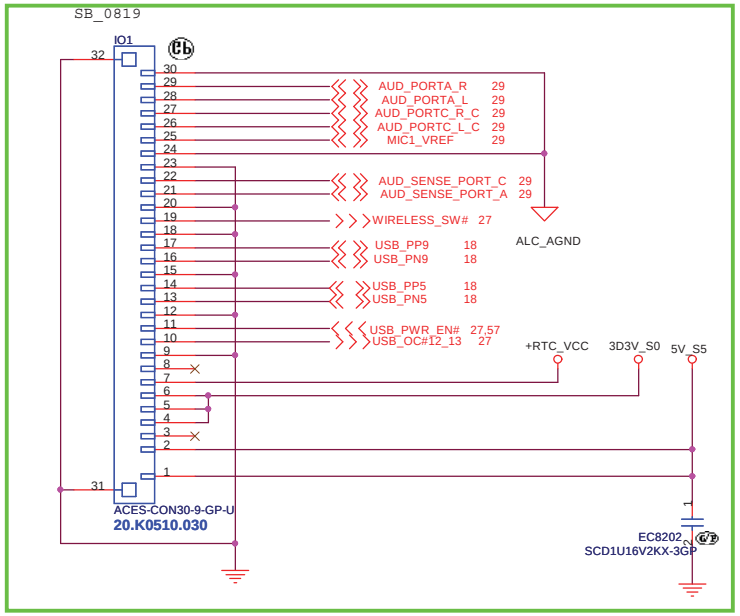
Mars:
Exchange ODD and ESATA differential pair each other.

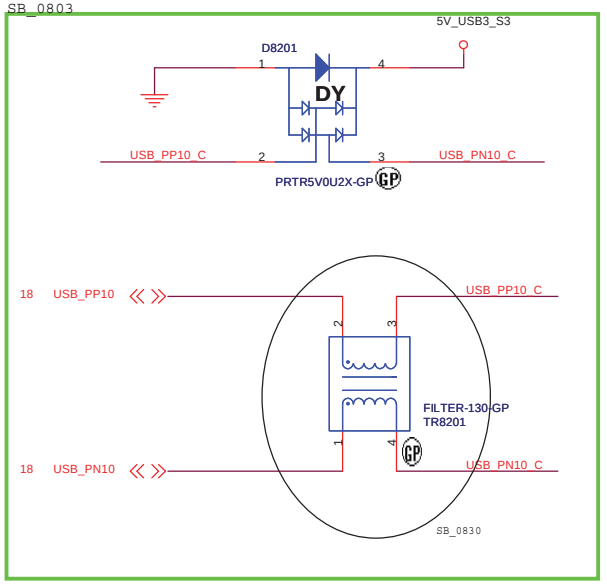
USB Board CONN.

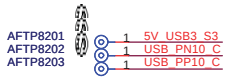


I/O Board CONN.









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Title: IO Board Connector		
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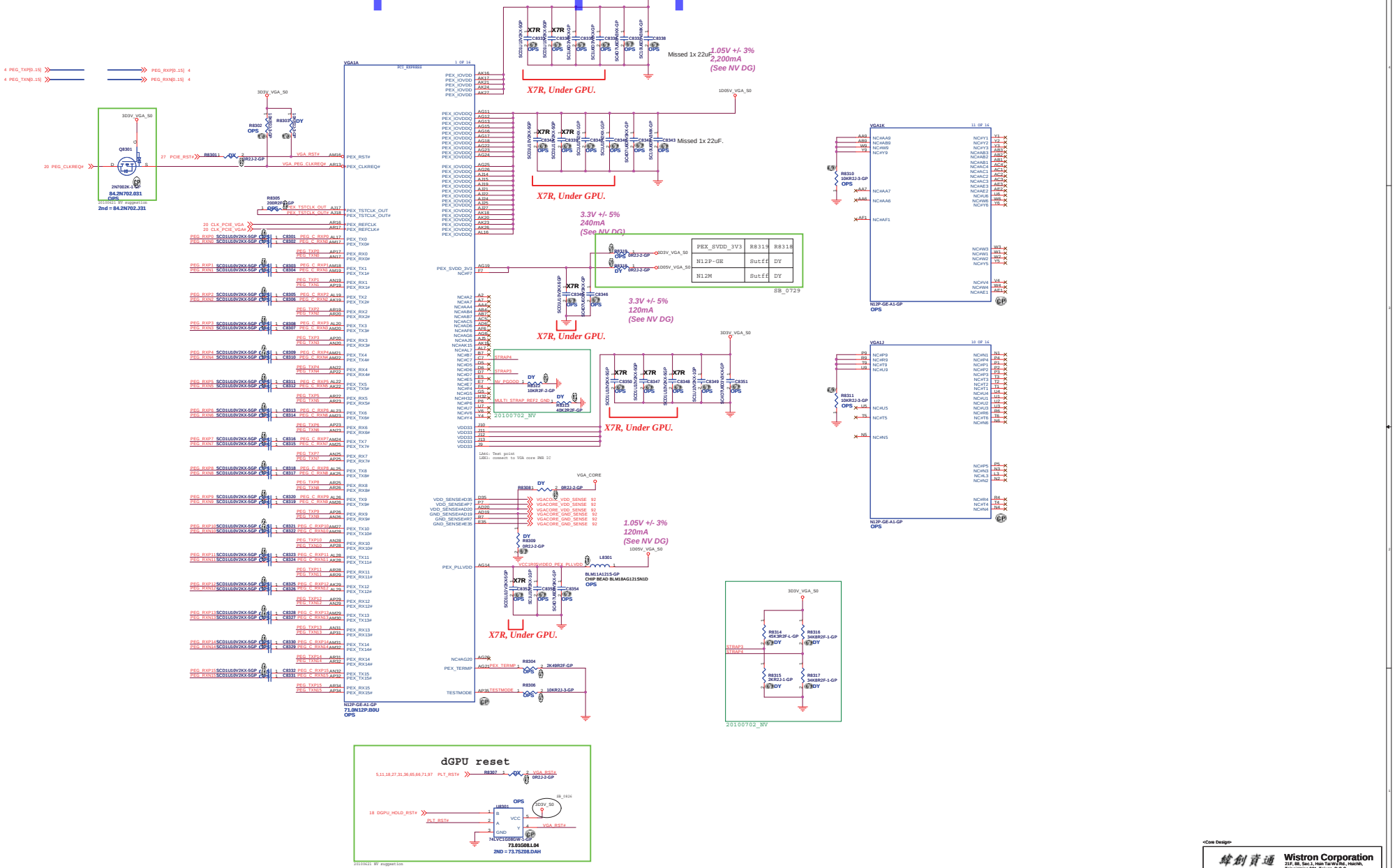

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Title: N12P-GE(1/6): PEG I/F

Size	Document Number	Rev
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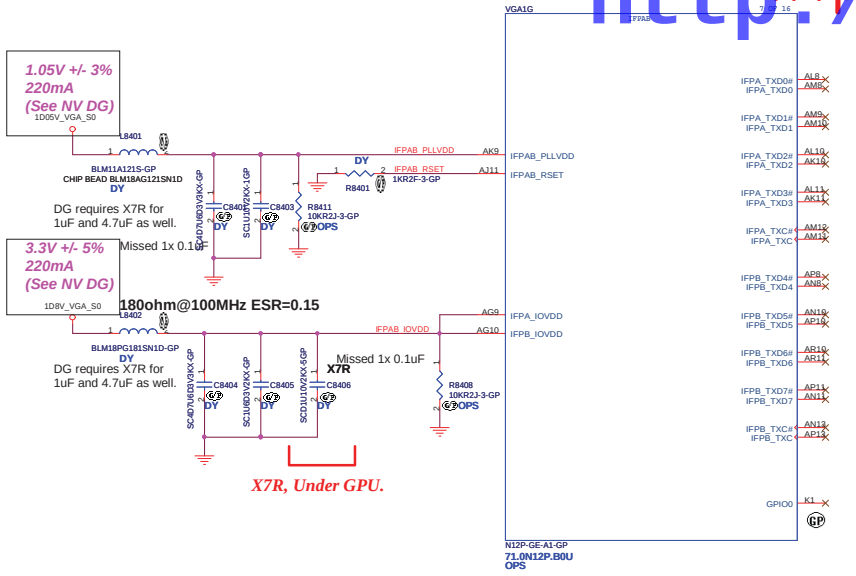
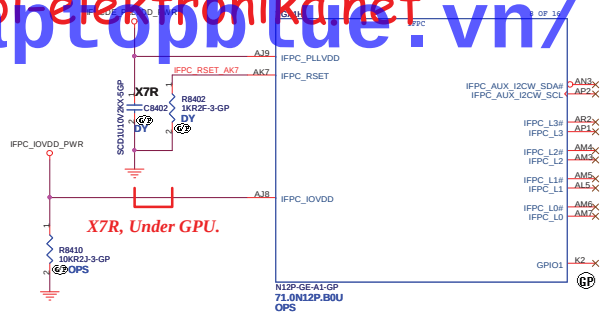
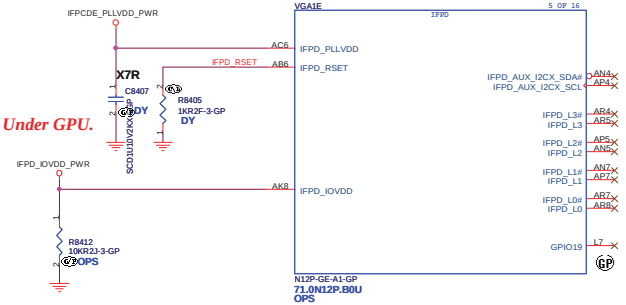
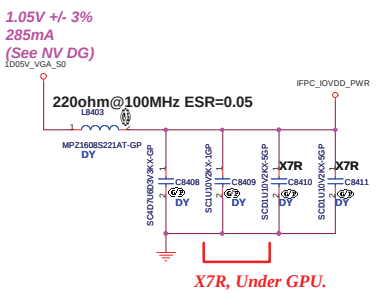
LVDS Interface

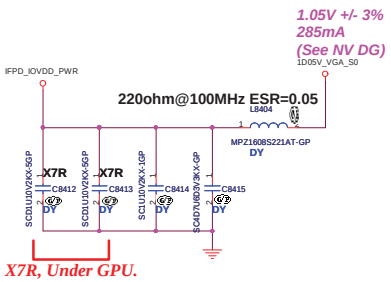


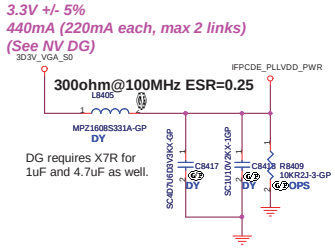
HDMI Interface

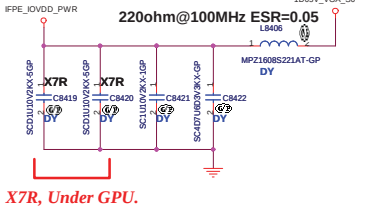


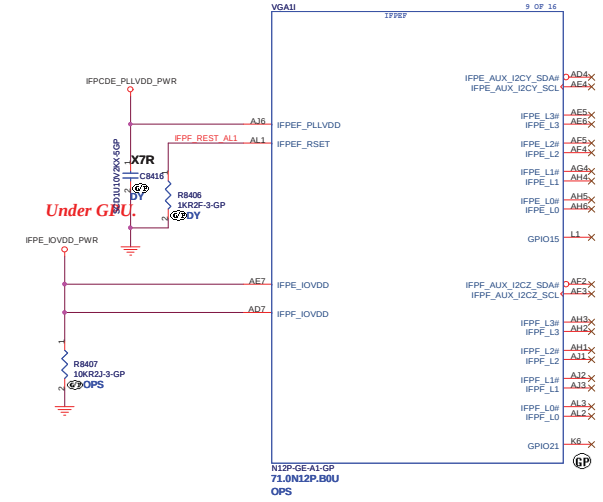












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Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

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EMI 10%
AC tolerance +/- 75mV < 50MHz
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

20100702_Change to Mode E

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination	R8504-R8507
N12P	Stuff 162 ohm 64.1620S.GIL
N12M	Stuff 243 ohm 64.2430S.GIL

FBCLK Termination place on VRAM side

Title: N12P-Q1/Q3 (3/6): VRAM I/F

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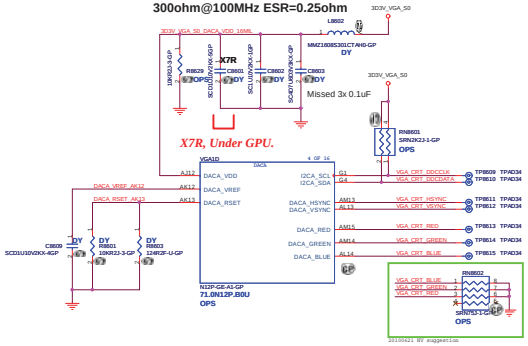
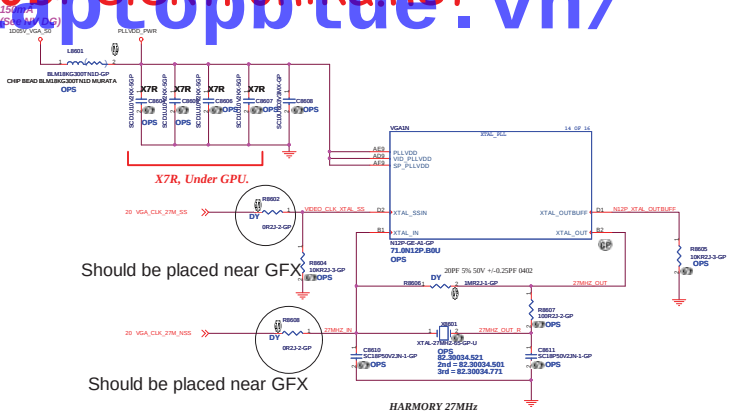
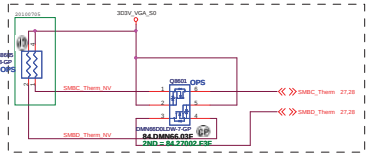
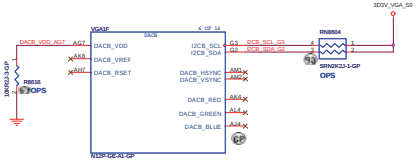
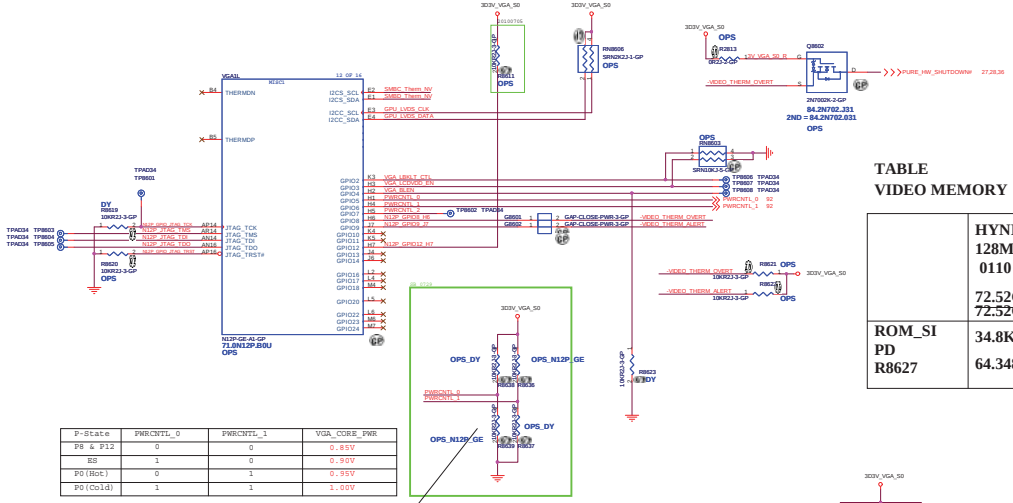










I2CA=>CRT, I2CC=>LVDS.

TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
	72.52G63.00U ~~72.52G63.A0U~~	72.42164.C0U ~~72.42164.D0U~~	72.51G63.C0U	72.41164.H0U
ROM_SIPD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

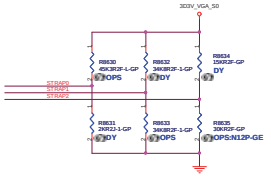
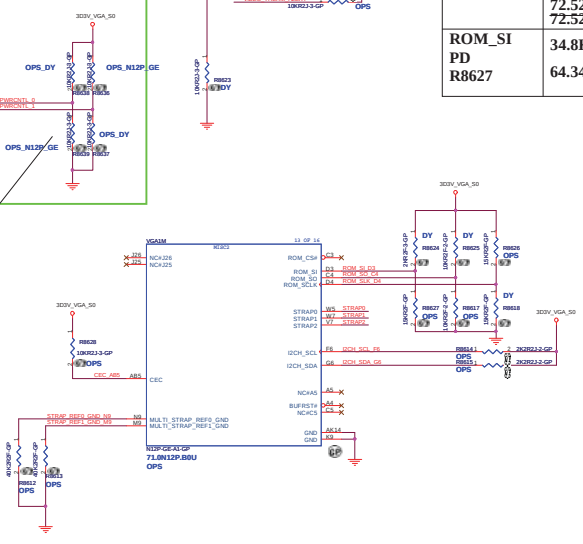


TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV1 DEV ID: 0x0DF7	N12M-GE DEV ID: 0xA7A 1010
STRAP2	PD R8635 30Kohm 64.30025.6DL	PD R8635 45Kohm 64.45325.6DL	PU R8634 15Kohm 64.15025.6DL

P-State	PWRCNTL_0	PWRCNTL_1	VGA_CORE_PWR
P8 & P12	0	0	0.85V
ES	1	0	0.90V
P0(Hot)	0	1	0.95V
P0(Cold)	1	1	1.00V

P-State	N12P-GE	N12P-GV1	N12M-GE	N12P-GV
NVVDD Boot Voltage	0.95V	0.90V	0.85V	TBD



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Title: N12P-Q1/Q3 (4/6): GPIO
Size: A1 | Document Number: LA470 | Rev: SB
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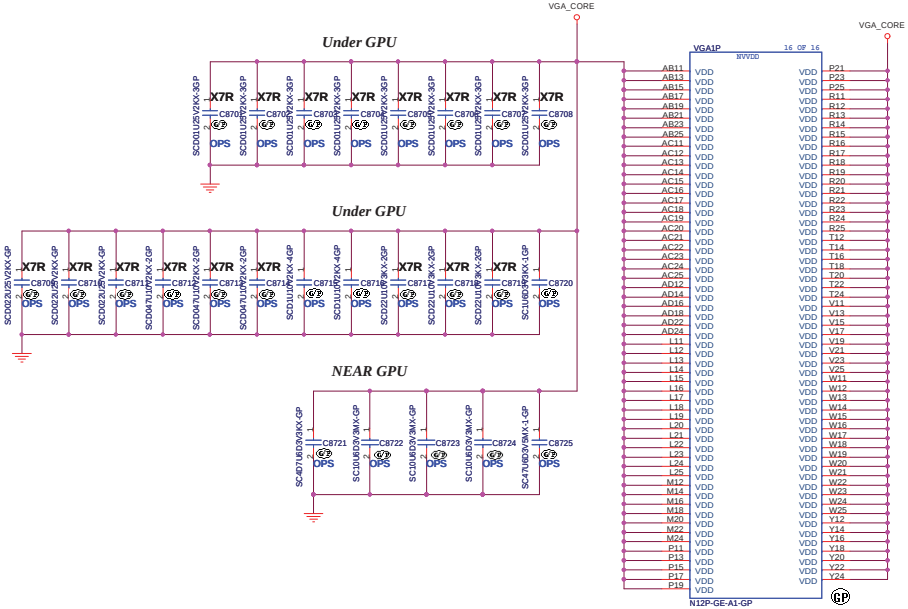

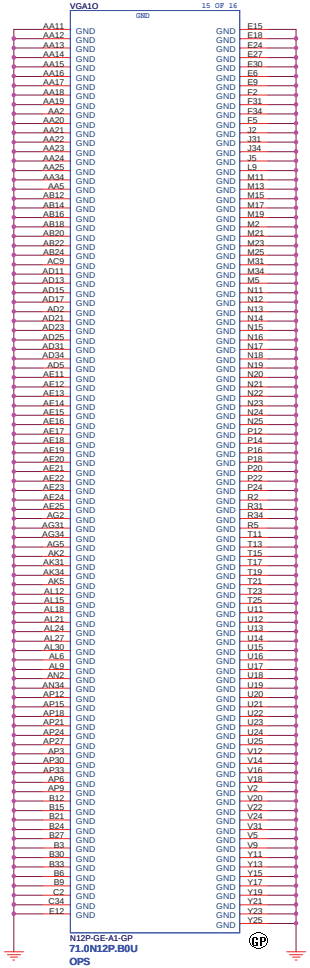

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Title: N12P-Q1/Q3 (5/6): POWER

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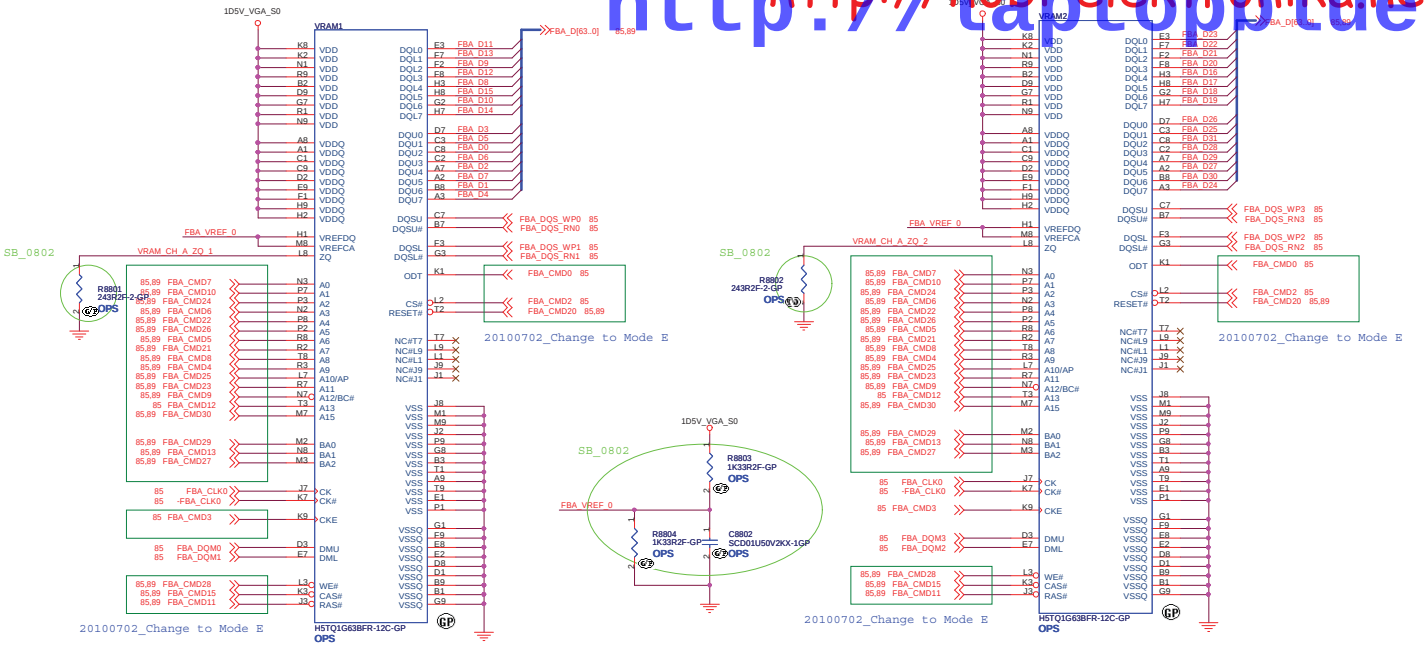
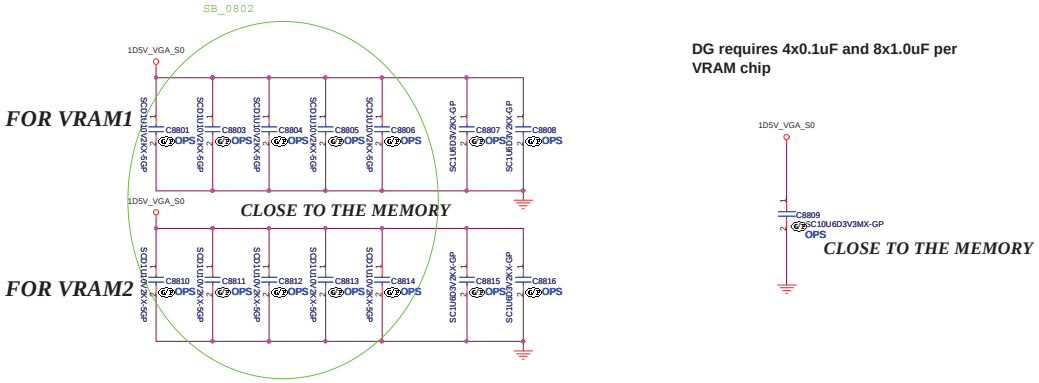


FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

VIDEO FRAME BUFFER PORT A

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM CHANNEL-A		
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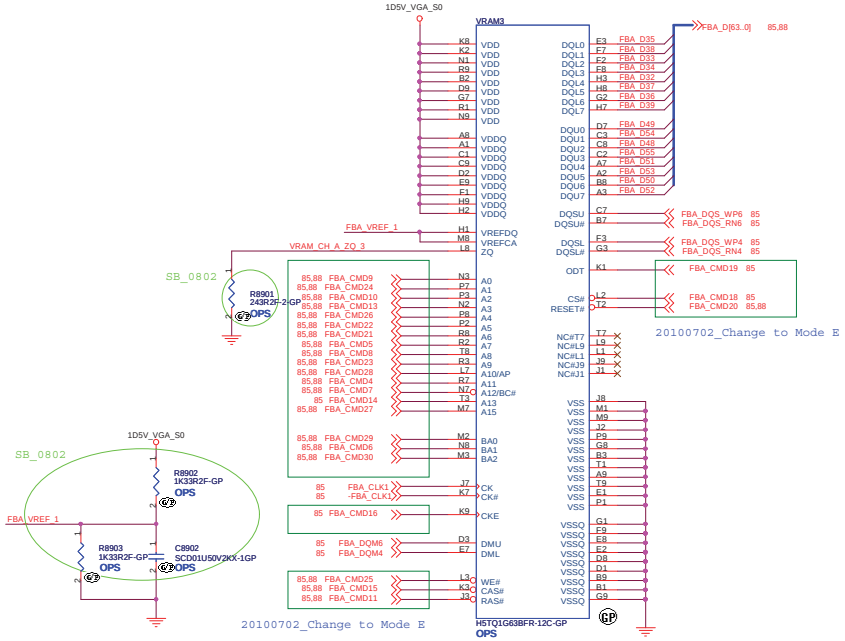
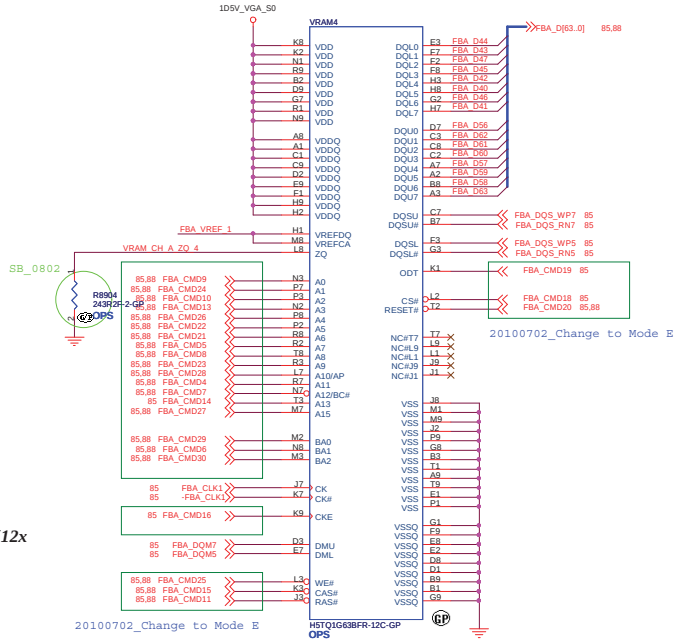
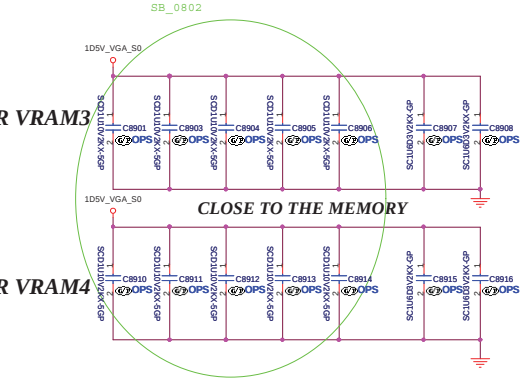


FB CMD mapping Mode D-N12x

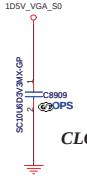




FOR VRAM3

CLOSE TO THE MEMORY

FOR VRAM4



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

<Core Design>

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Title	VRAM CHANNEL-A	
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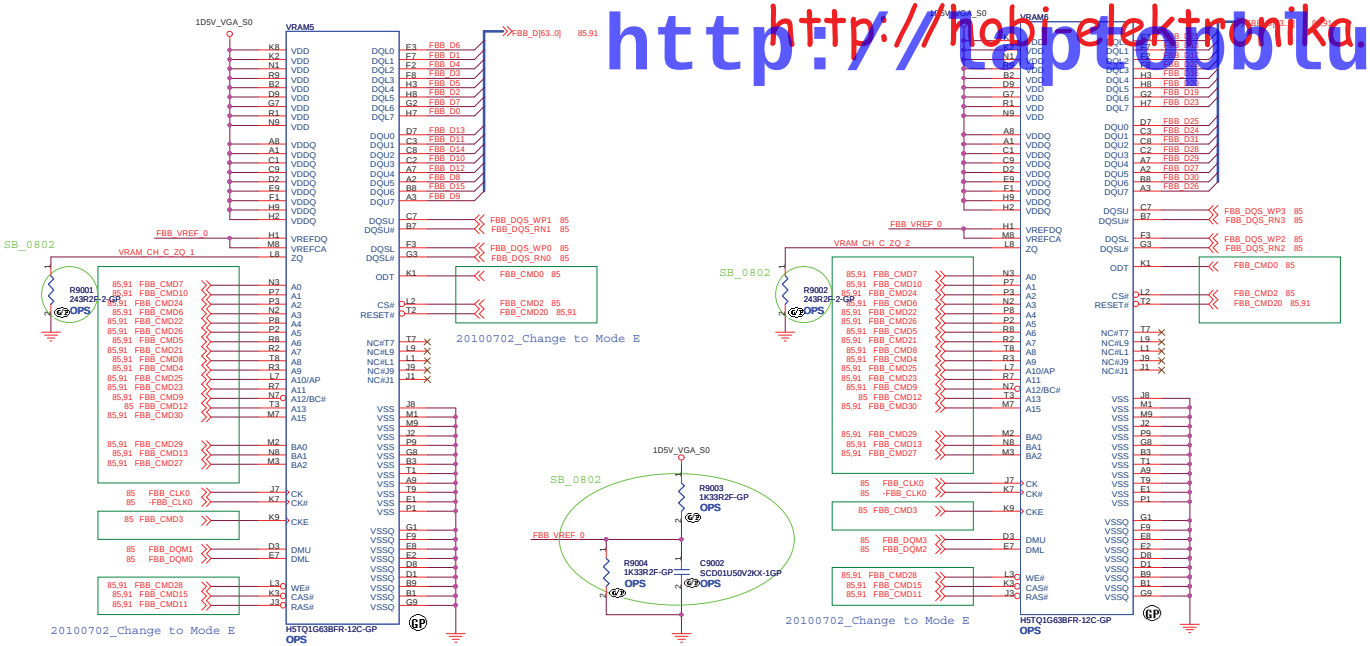
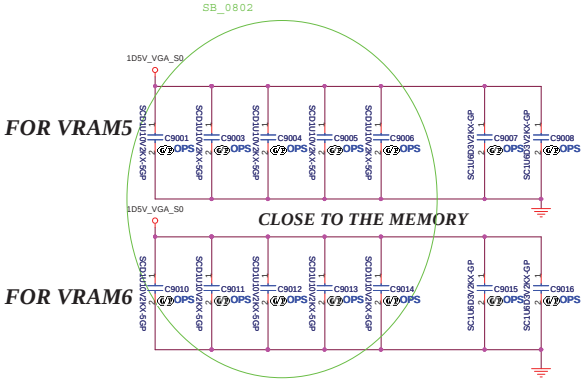
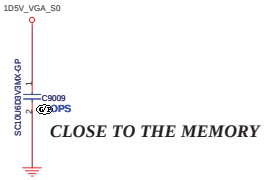




DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

<Core Design>

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Title: VRAM CHANNEL-C

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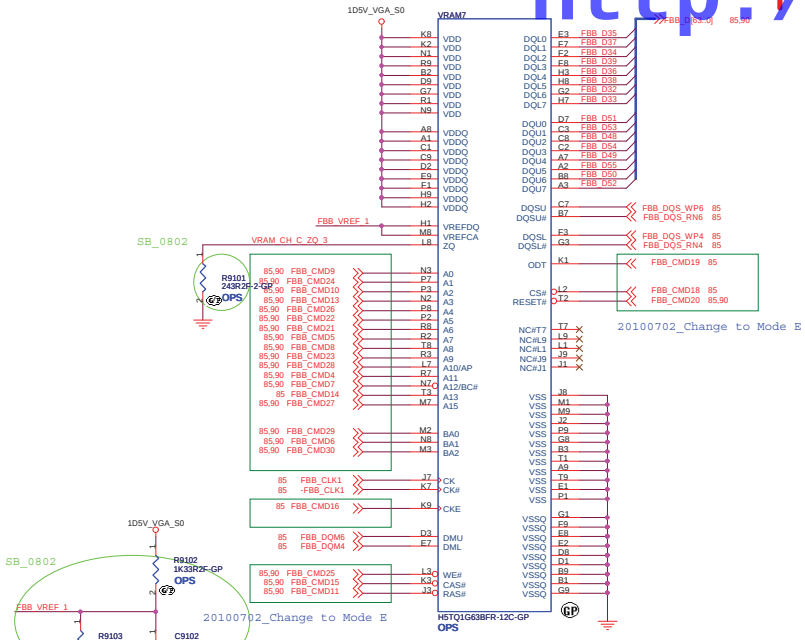

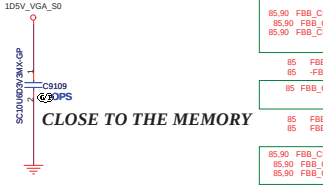

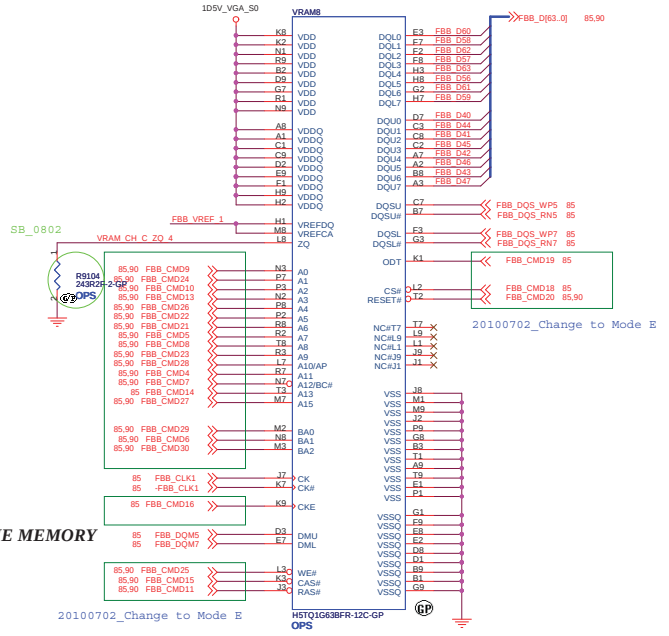

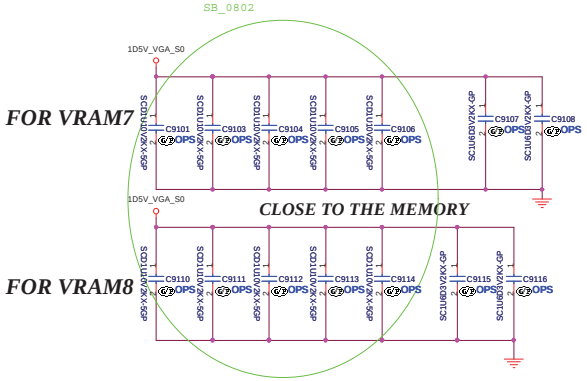

VIDEO FRAME BUFFER PORT C

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-C**

Size	Document Number	Rev
A2	LA470	SB

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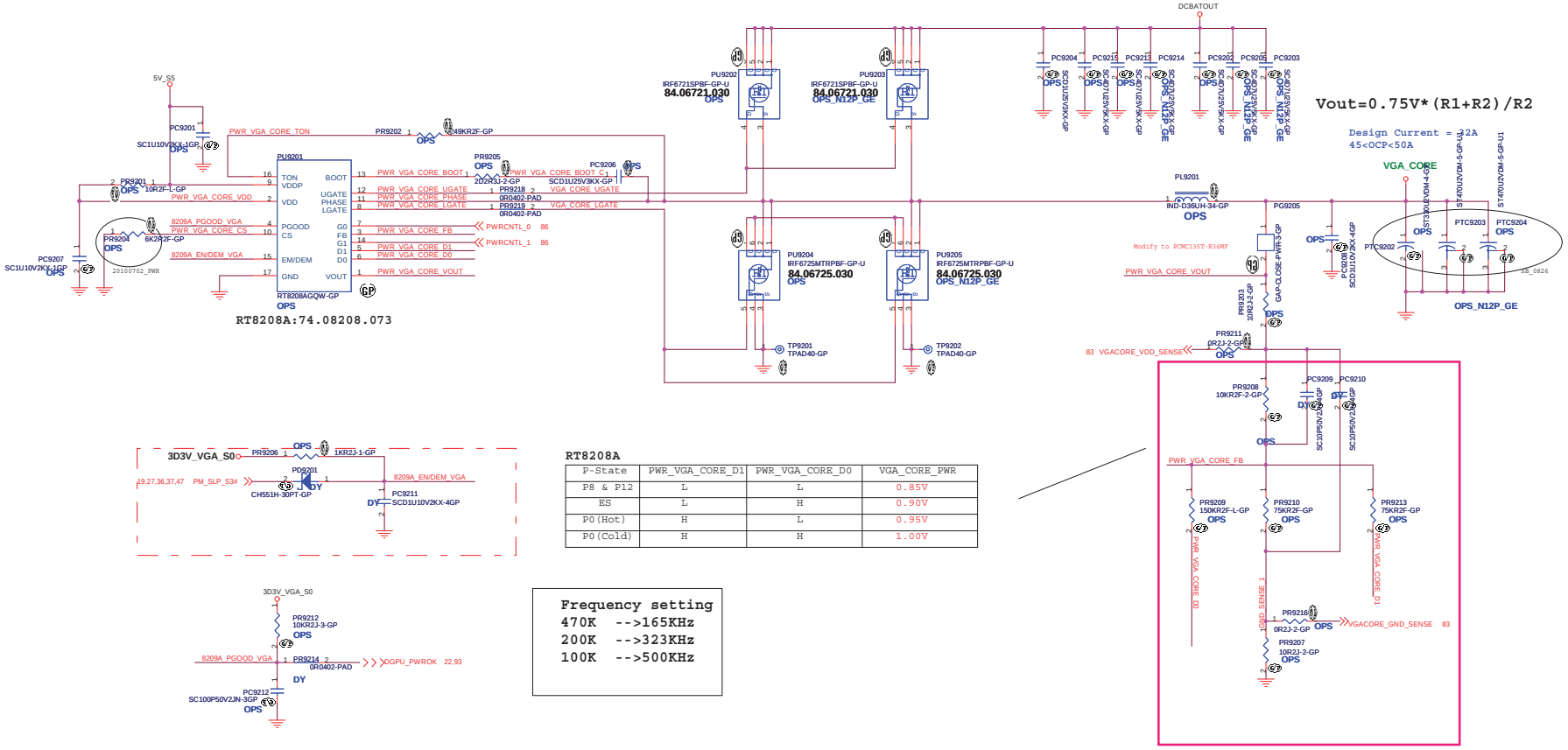

RT8208A

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 & P12	L	L	0.85V
ES	L	H	0.90V
P0(Hot)	H	L	0.95V
P0(Cold)	H	H	1.00V

Frequency setting
470K --->165KHz
200K --->323KHz
100K --->500KHz

<Core Design>

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Title	DC/DC_VGA CORE_RT8208A	
Size	Document Number LA47	Rev SB
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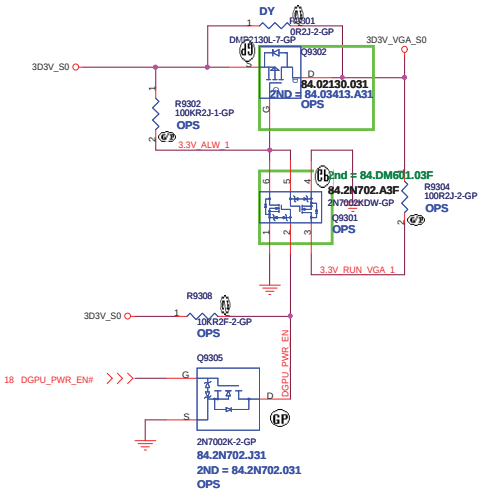
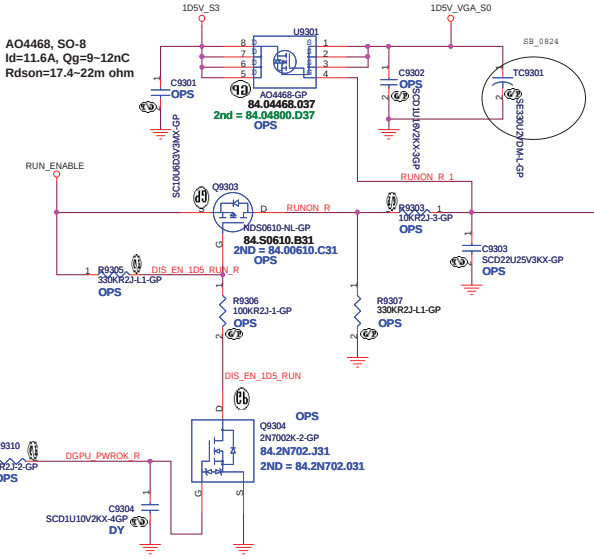
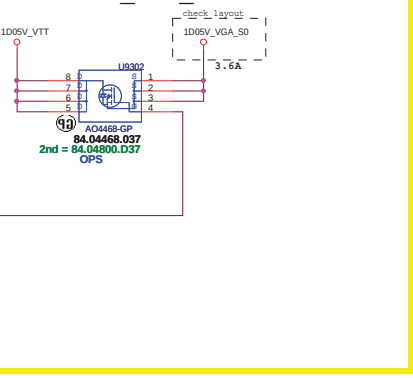
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

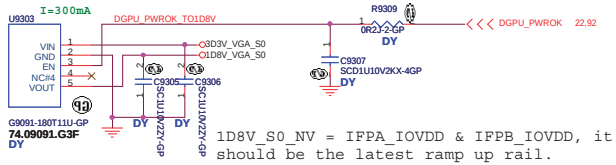


1.05V to 1.05V_VGA_S0 Transfer



20100707

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

<Core Design>

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Title	DISCRETE VGA POWER		
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<Core Design>

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Title: LVDS Switch

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<Core Design>

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Title
CRT_Switch

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<Core Design>

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Title
TOUCH PANEL

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CPU Plate

H1 HOLE276R178-GP — ZZ.00PAD.N11
H2 HOLE276R178-GP — ZZ.00PAD.N11
H3 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

Structure boss

H7 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H8 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H9 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H10 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H11 HOLE315X315R91-S1-GP — ZZ.00PAD.581
H12 HOLE256R115-GP — ZZ.00PAD.D11
H13 HOLE256R115-GP — ZZ.00PAD.D11
H15 HOLE256R115-GP — ZZ.00PAD.D11

MiniPCI Std-Off

H14 STF237R113H115-GP — 34.4V802.101

Check test point

5,11,18,27,31,36,65,66,71,83 PLT_RST# — AFTP1
3D3V_S0 — AFTP7
3D3V_AUX_S5 — AFTP8
3D3V_S5 — AFTP9
5V_S5 — AFTP10
11,19,27 PM_PWRBTN# — AFTP11
5,11,22,36 H_CPUPWRGD — AFTP12
27,36 S5_ENABLE — AFTP13

Test Point放在Dimm Door打開可量測處

AD+

EC9702 DY SCD1U25V2KX-GP
EC9703 DY SCD1U25V2KX-GP
EC9704 DY SCD1U25V2KX-GP

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Title: UNUSED PARTS/EMI Capacitors
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Title: *Change History*

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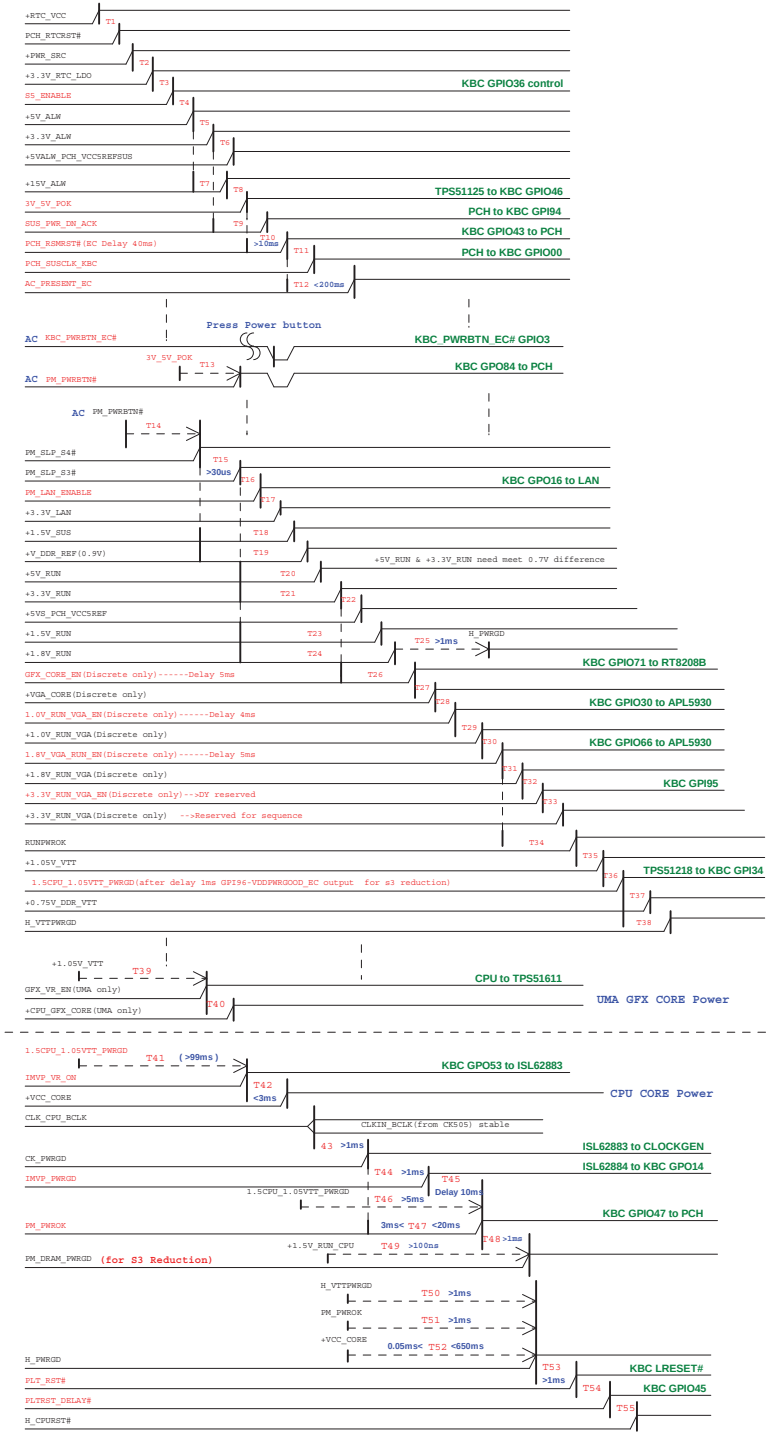
Intel-Power Up Sequence

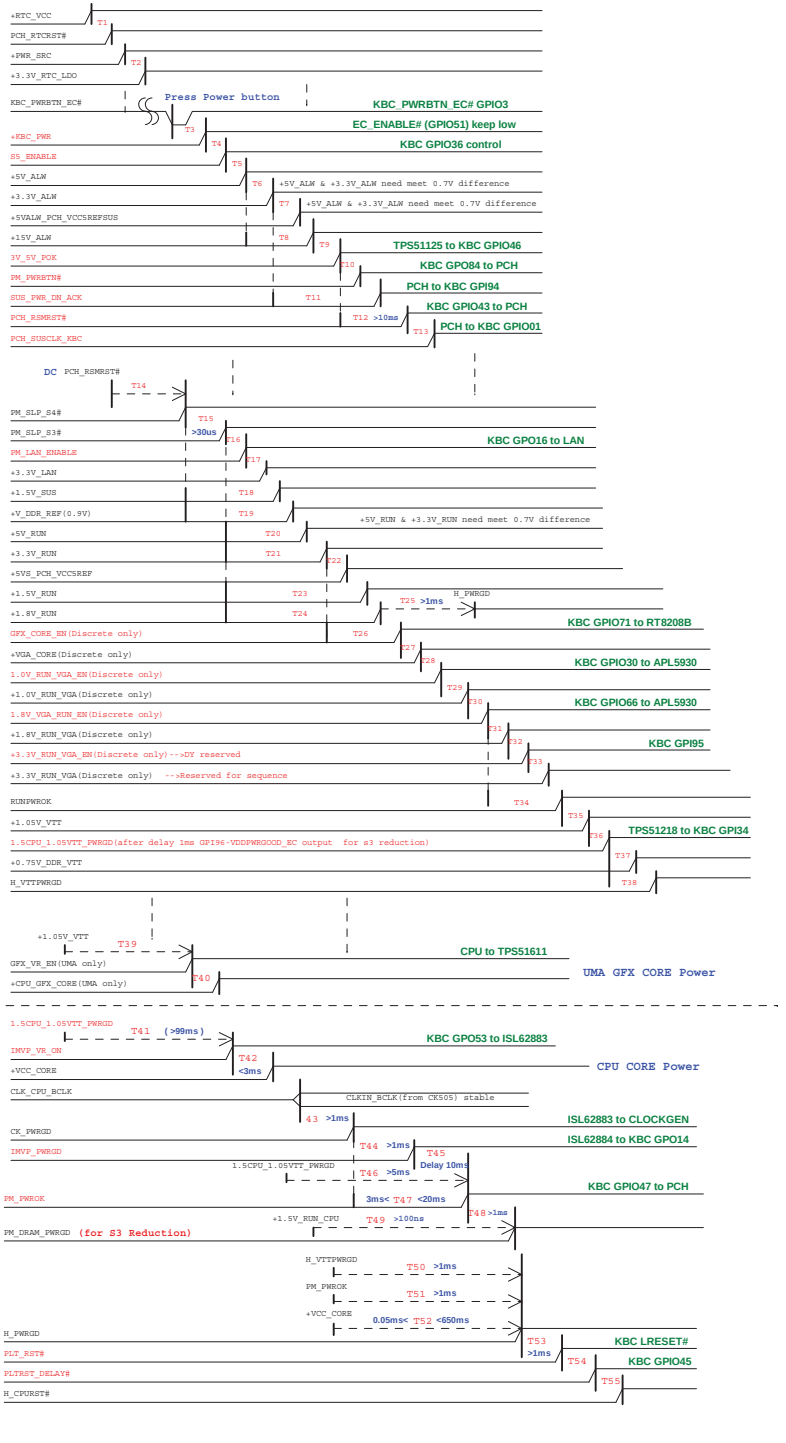
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence
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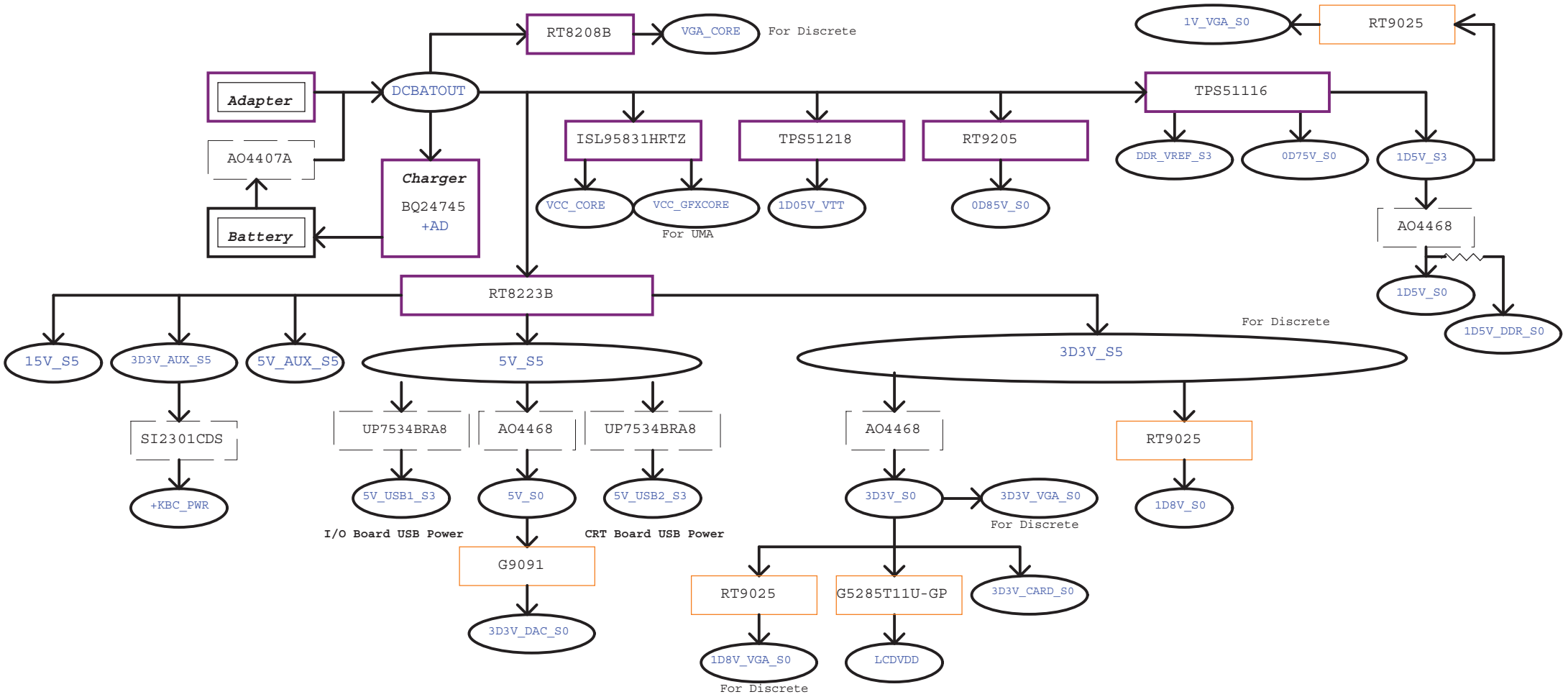

Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

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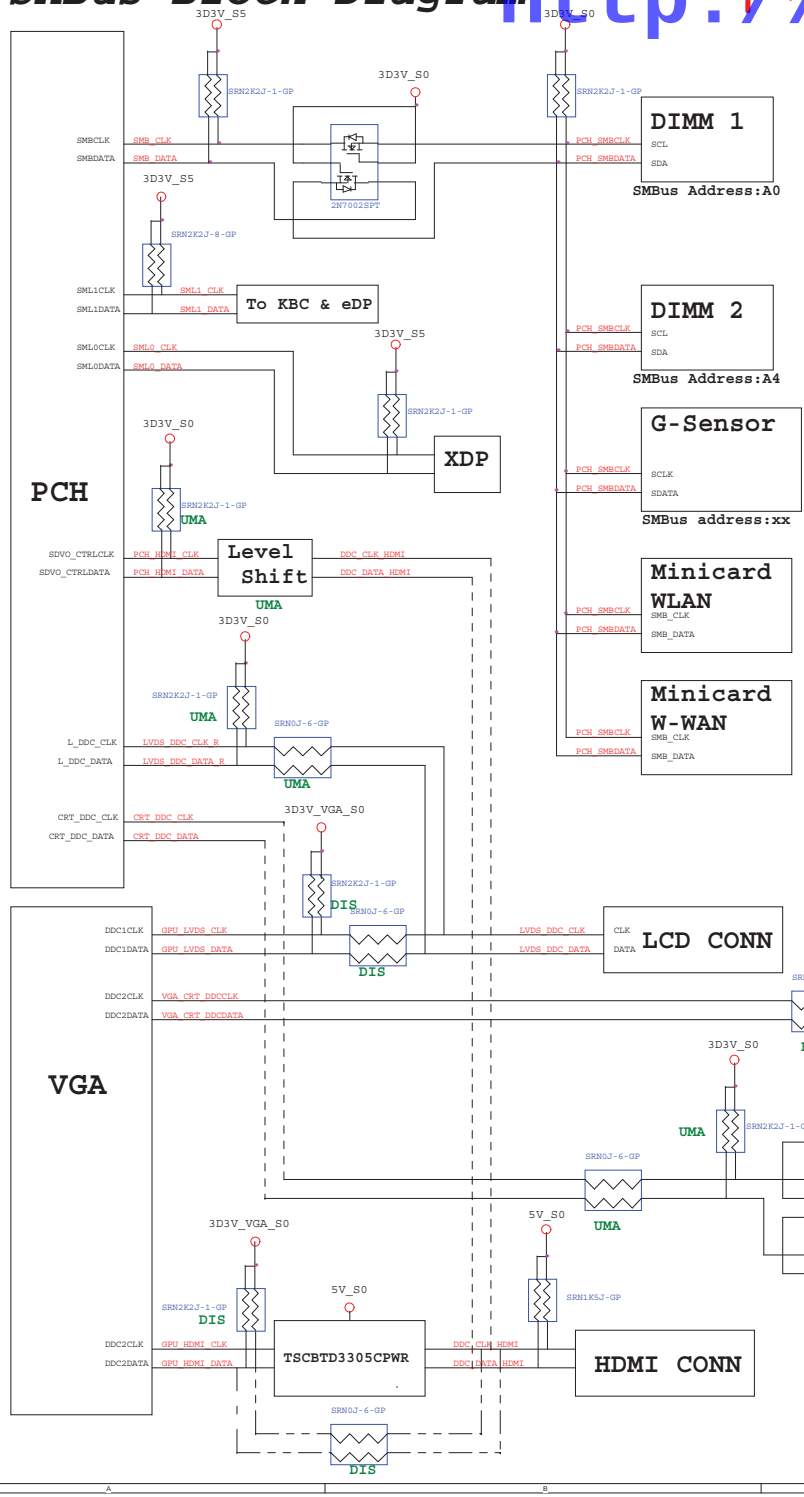
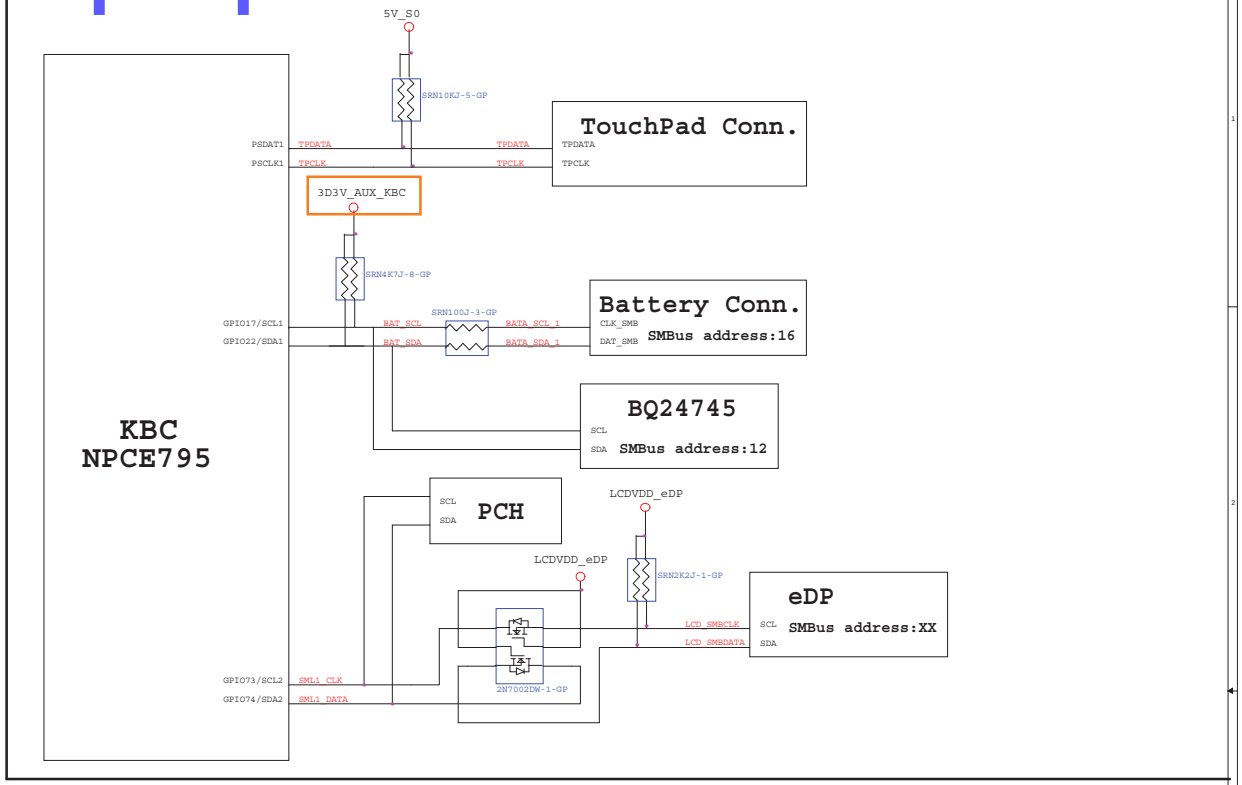
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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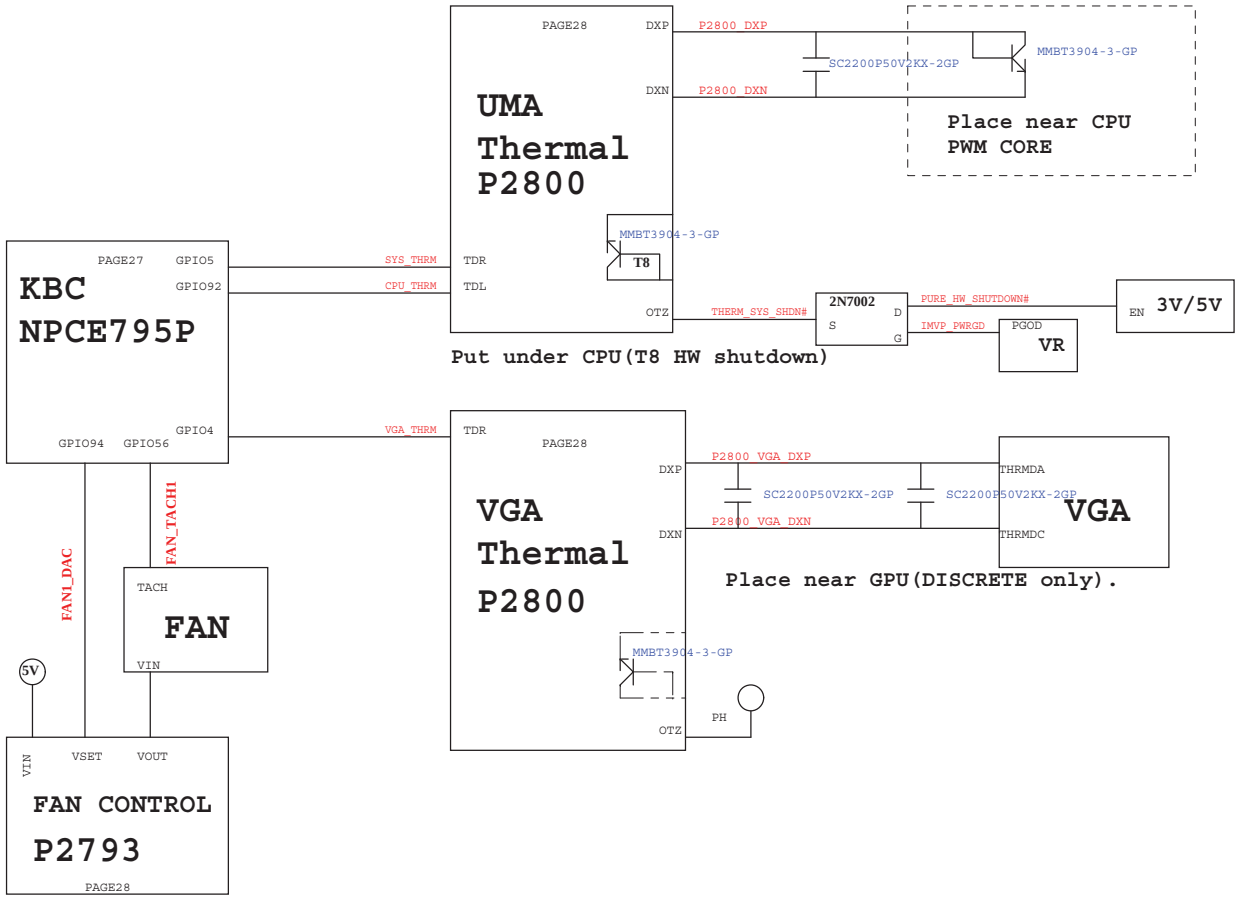
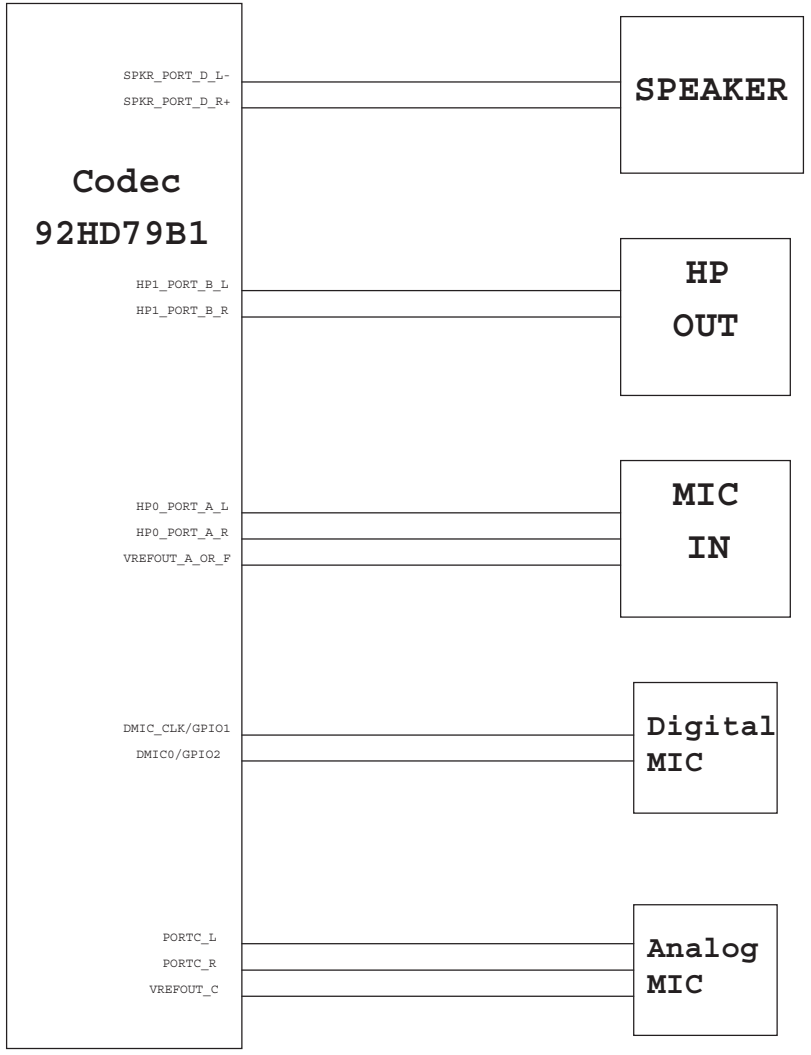
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title: *Change History*

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