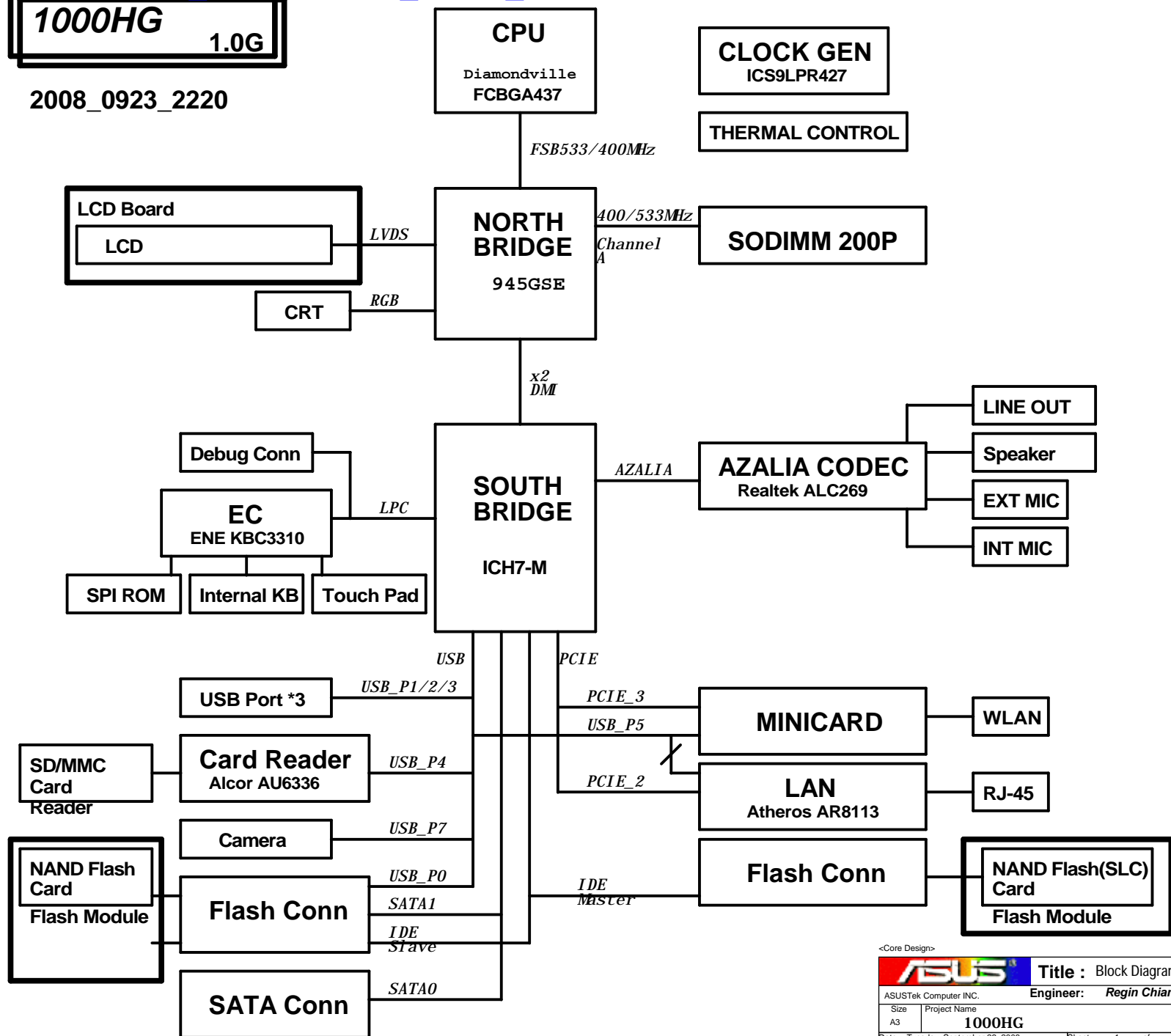


**1000HG**  
1.0G

2008\_0923\_2220

01\_Block Diagram  
02\_System Setting  
03\_Power Sequence  
04\_Clock Gen\_ICS9LPR426  
05\_Diamondville\_BUS  
06\_Diamondville\_PWR  
07\_NB-945GMS(HOST)  
08\_NB-945GMS(DMI)  
09\_NB-945GMS(GRAPHIC)  
10\_NB-945GMS(DDR2)  
11\_NB-945GMS(PWR)  
12\_NB-945GMS(PWR2)  
13\_NB-945GMS(GND)  
14\_SB-ICH7M(PWR)  
15\_SB-ICH7M(1)  
16\_SB-ICH7M(2)  
17\_SB-ICH7M(3)  
18\_DDR2 SODIMM  
19\_DDR2 Termination  
20\_Onboard VGA  
21\_LCD Conn\_LID  
22\_PCIE 3.5G & Ext. Antenna  
23\_Mini WIFI+ BT  
24\_LAN\_Atheros AR8113  
25\_MDC\_RJ11\_RJ45  
26\_Flash Conn  
27\_SATA Hdd  
28\_USB Port  
29\_Camera Conn  
30\_Card Reader\_AU6336C52  
31\_Codec\_ALC269  
32\_Audio\_AMP\_Jack  
33\_EC\_ENE KB3310  
34\_EC\_UART controller  
35\_Switch\_SPI ROM\_Debug Conn  
36\_Thermal Sensor\_FAN  
37\_KB\_Touch Pad  
38\_LED\_THERMTRIP  
39\_Discharge  
40\_PWR Jack  
41\_Srew Hole  
42\_EMI  
43\_POWER FLOW  
44\_Vcore  
45\_Power System  
46\_Power\_+1.8V & VTTDDR  
47\_Power\_VCCP  
48\_Power\_+1.5VS & +2.5VS  
49\_Power\_Charger  
50\_EC Pin Define  
51\_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

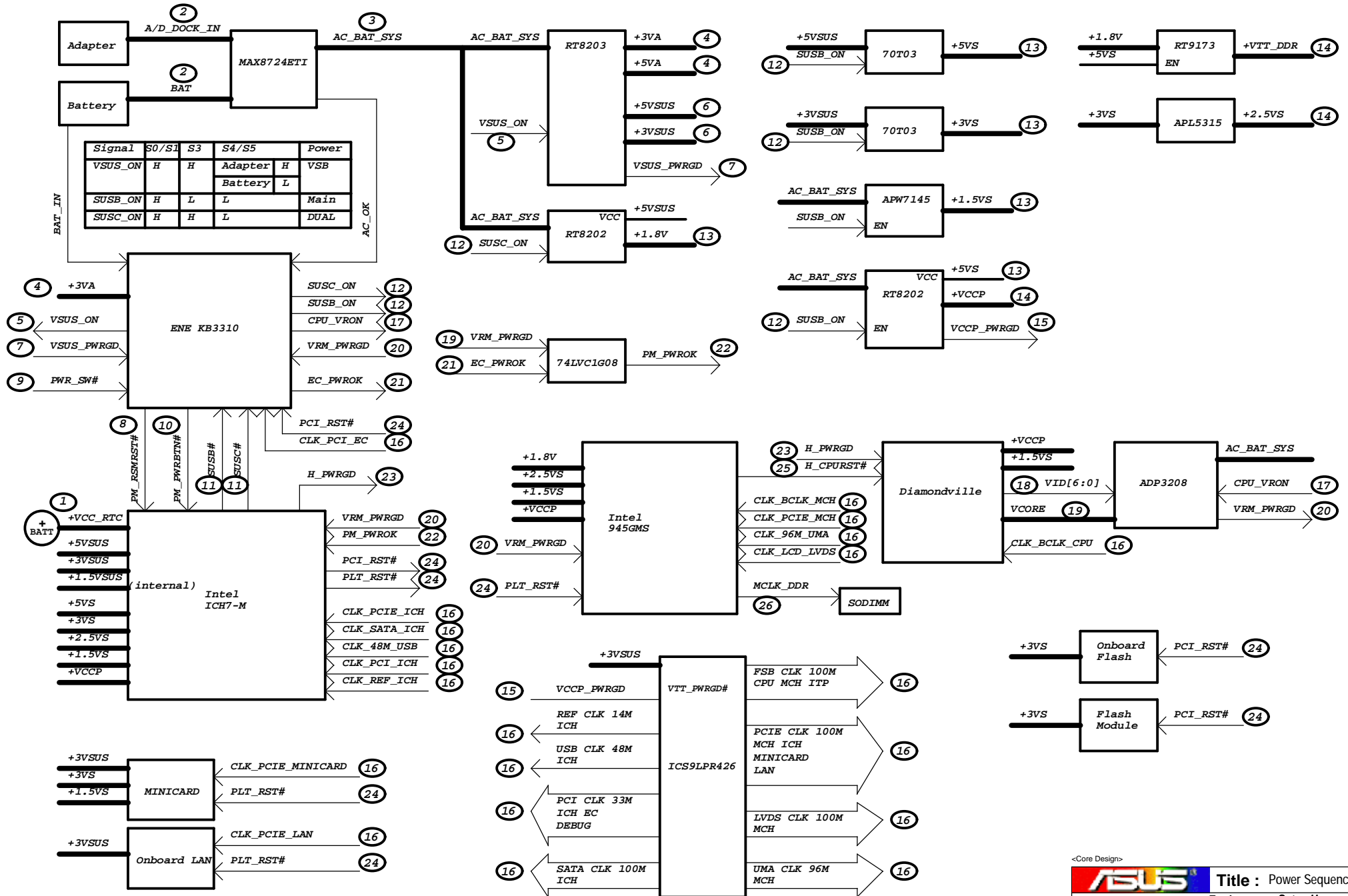
PCIE

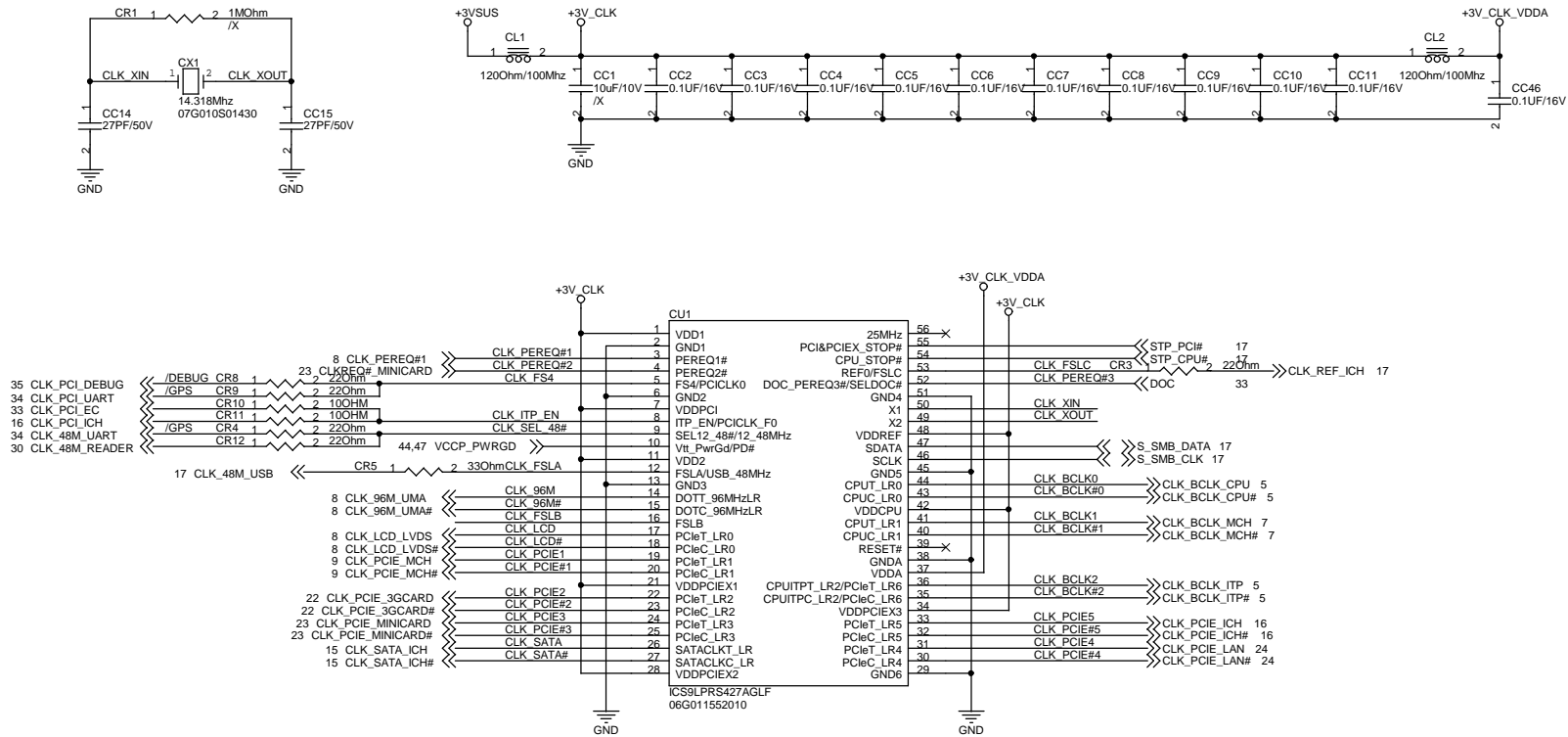
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM
ACZ_SDIN2	NC

<Core Design>

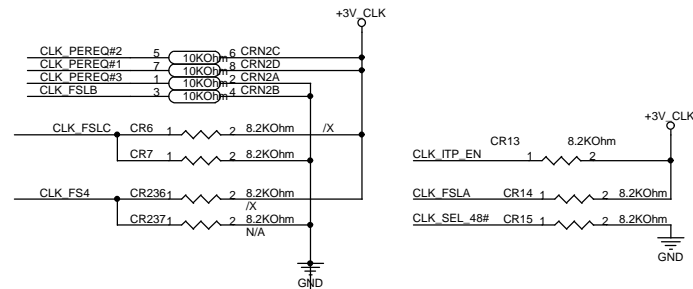




```
1:Disable
0:Enable
```

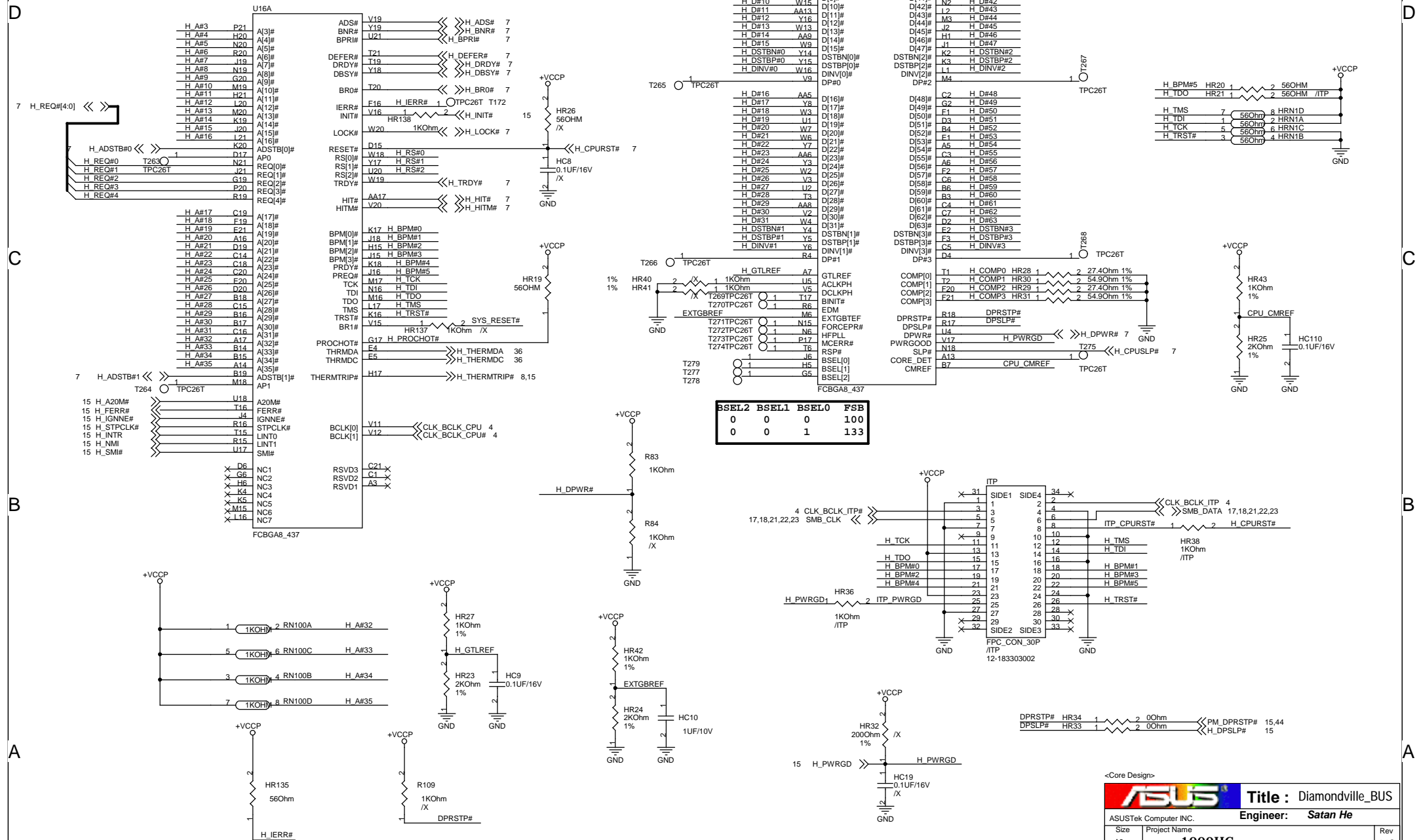
```
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6
```

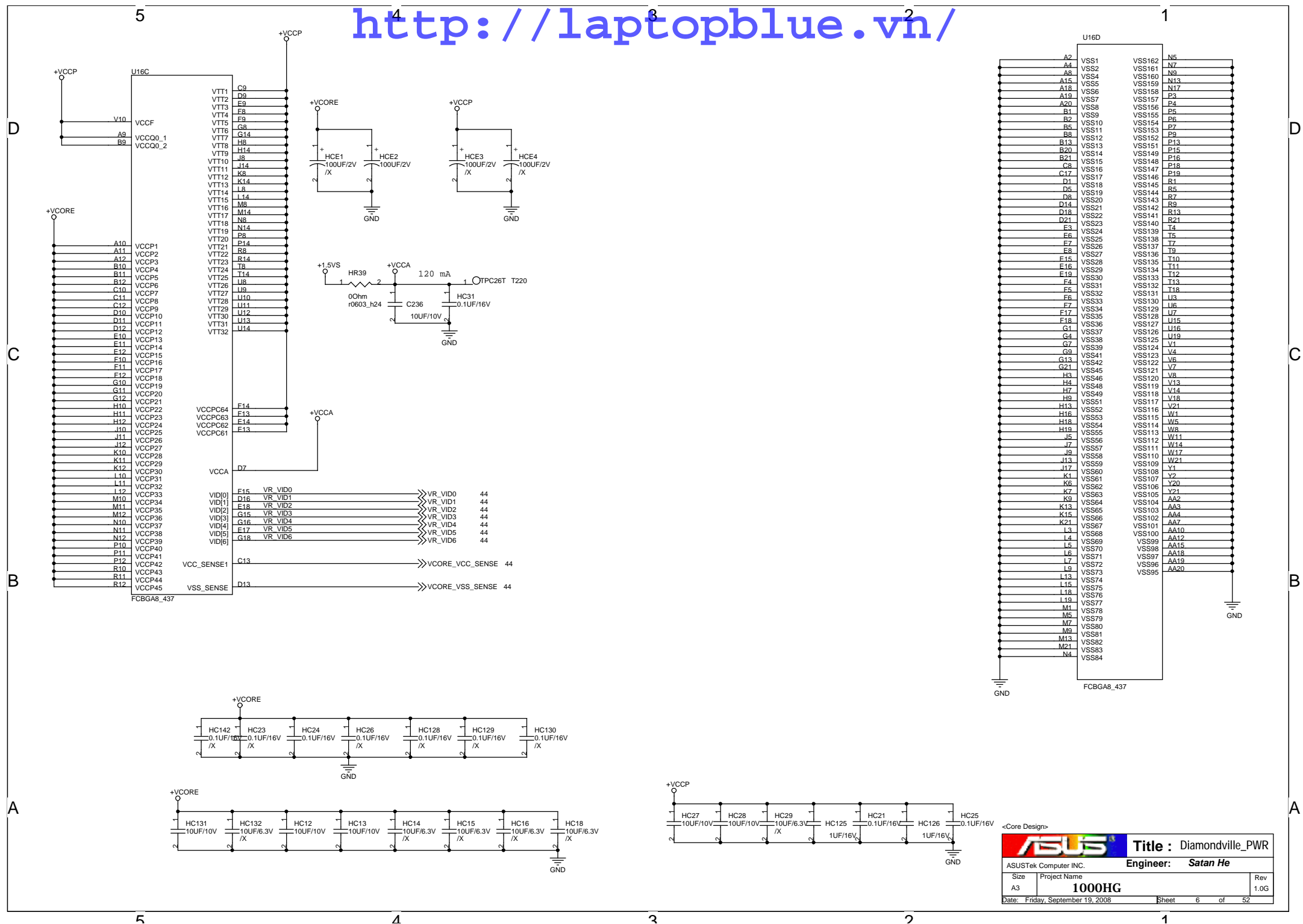
FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100



S SMB DATA	CC12	2	1	10PF/50V
				/X
S SMB CLK	CC13	2	1	10PF/50V
				/X
STP PCI#	CC103	2	1	10PF/50V
				/X
STP CPU#	CC104	2	1	10PF/50V
				/X

CLK_ITP_EN	CC37	2	1	10PF/50V
CLK_FSLC	CC39	2	1	22PF/50V
CLK_FSLA	CC40	2	1	10PF/50V
CLK_48M_UART	CC41	2	1	10PF/50V
CLK_FS4	CC42	2	1	22PF/50V
CLK_48M_READER	CC45	2	1	10PF/50V
CLK_PCIE_LAN	CC101	2	1	10PF/50V
CLK_PCIE_LAN#	CC102	2	1	10PF/50V
CLK_SATA_ICH	CC105	2	1	5PF/50V
CLK_SATA_ICH#	CC106	2	1	5PF/50V

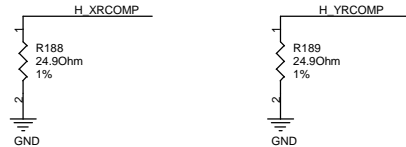




**Power :  
+VCCP**

### RCOMP

For Calibrating the FSB I/O Buffer



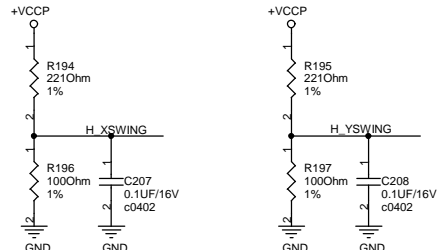
### SCOMP

For Slew Rate Compensation on the FSB

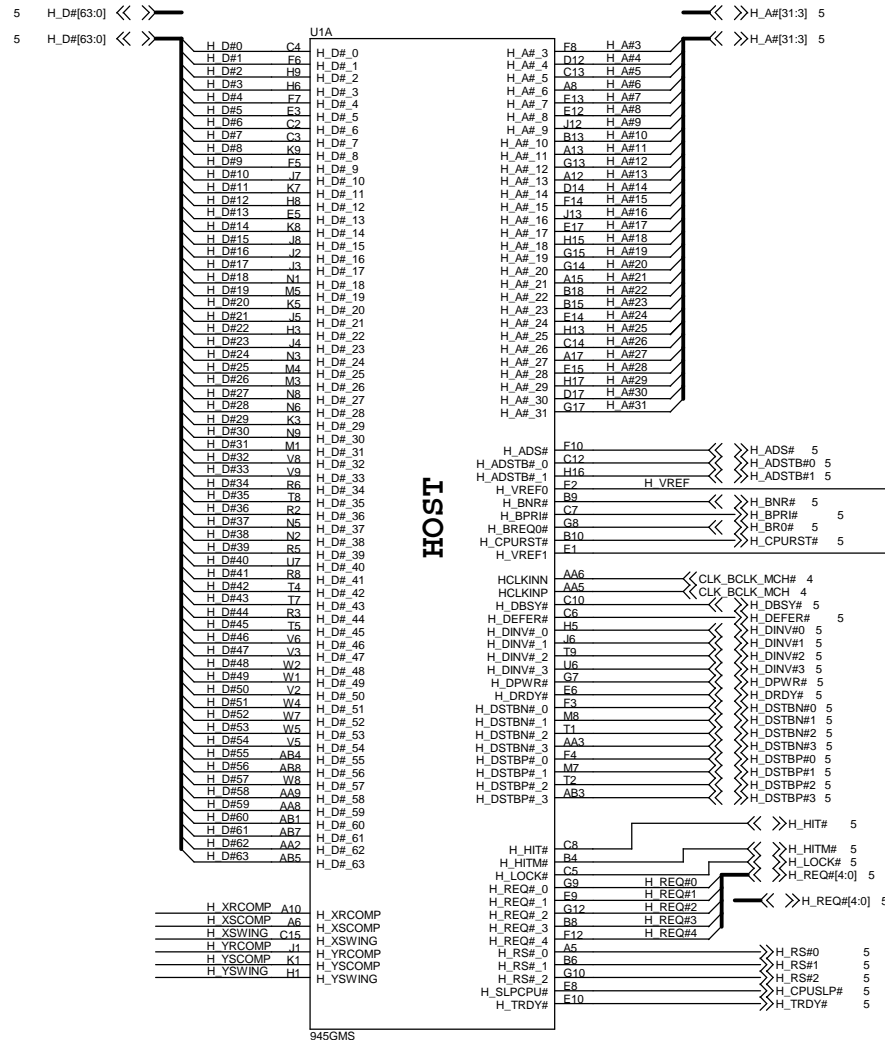


### Voltage Swing

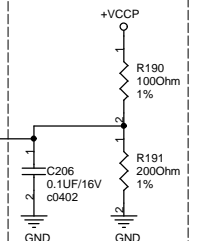
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =  
0.3125\*VCCP  
Trace should be 10 mil wide  
with 20 mil spacing



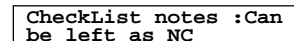
### AGTL+ I/O Voltage Reference



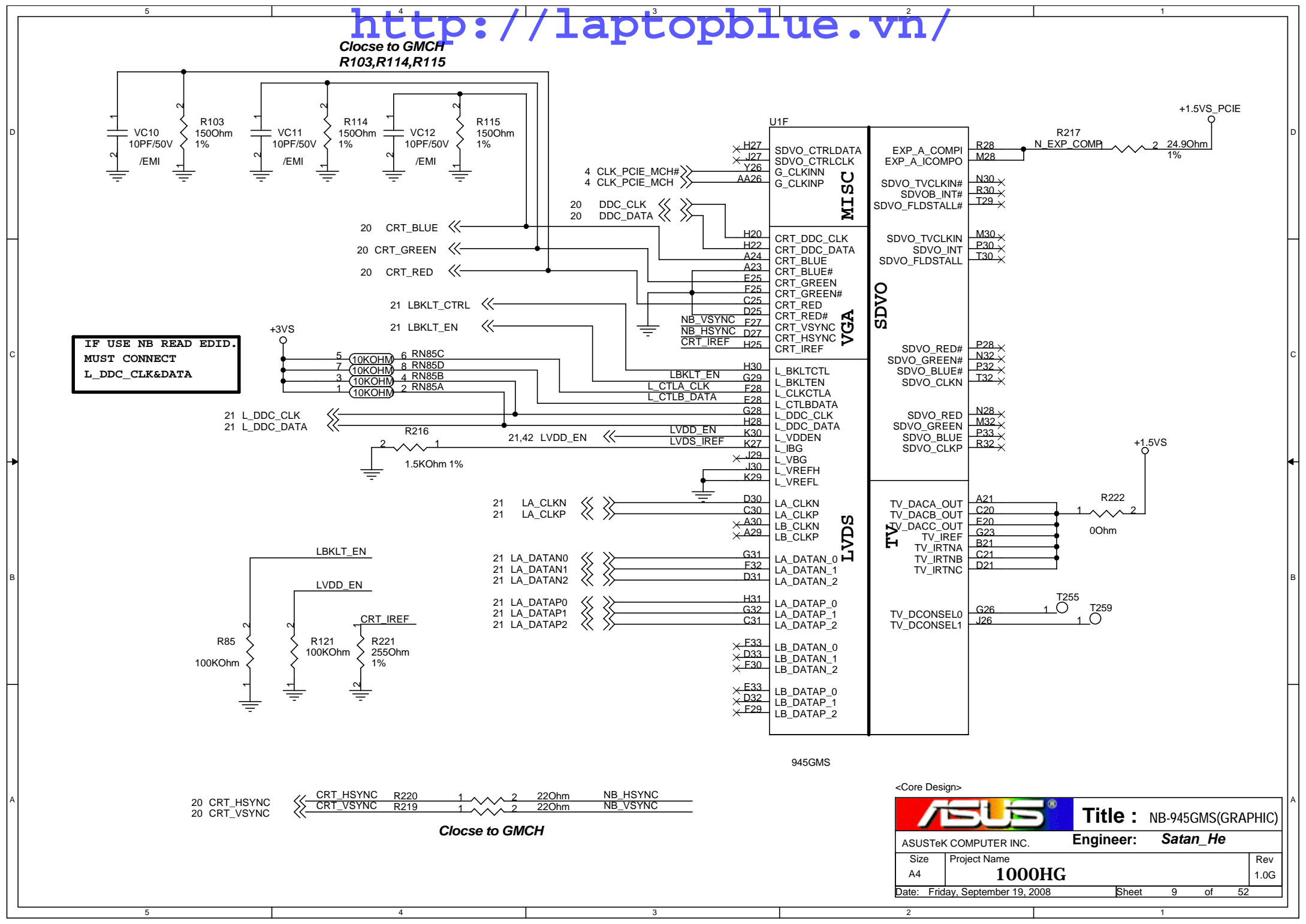
Layout Note:  
0.1uF should be placed 100mils or less from GMCH pin.

<Core Design>

<b>ASUS</b>		<b>Title : NB-945GMS(HOST)</b>	
ASUSTek COMPUTER INC.		Engineer: <b>Satan He</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 7 of 52	



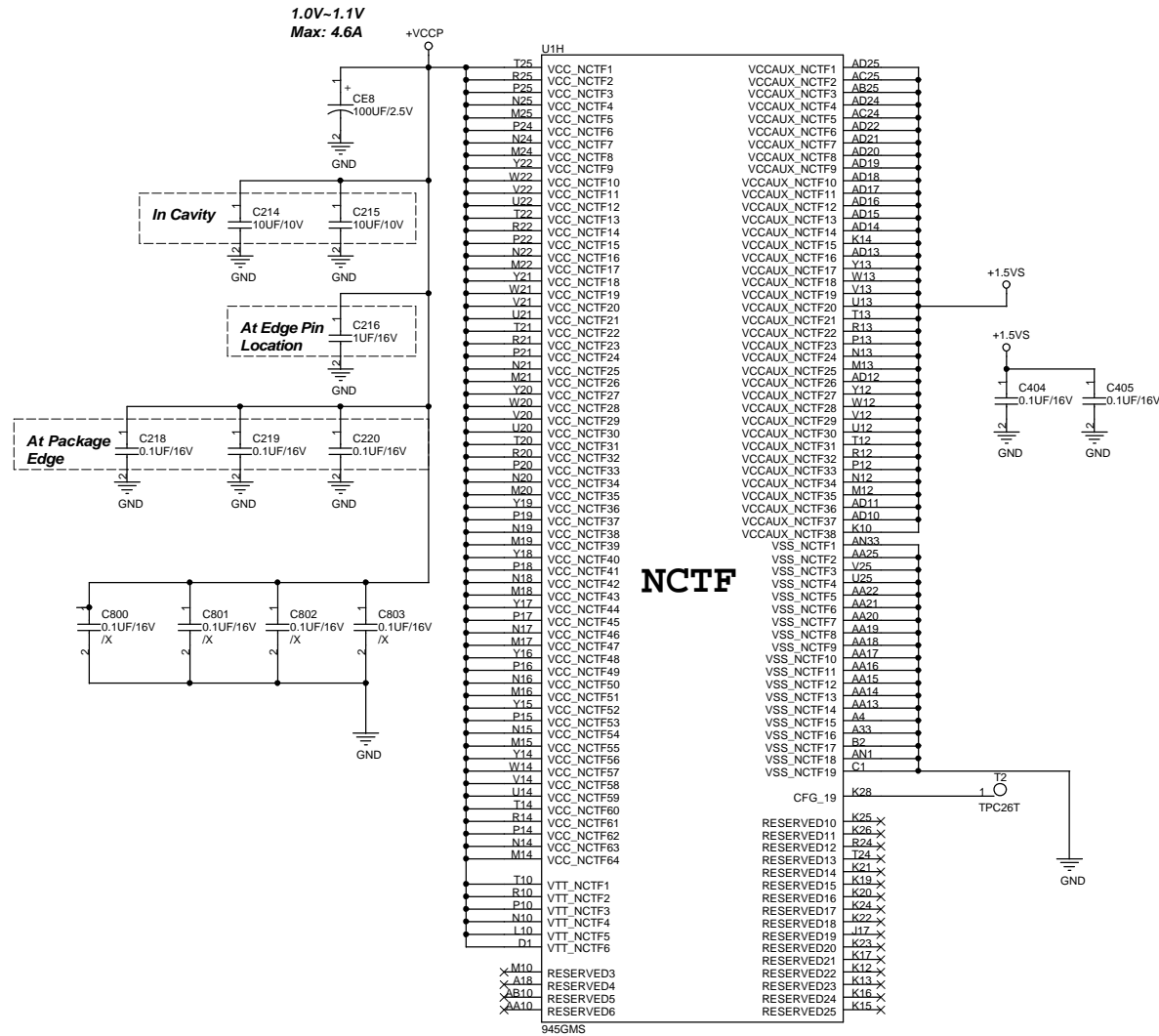




<Core Design>

		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: <b>Satan_He</b>	
Size A4	Project Name <b>1000HG</b>		Rev 1.0G
Date: Friday, September 19, 2008		Sheet 9	of 52





CFG\_19(K28) Strapping :

DMI LANE Reversal:

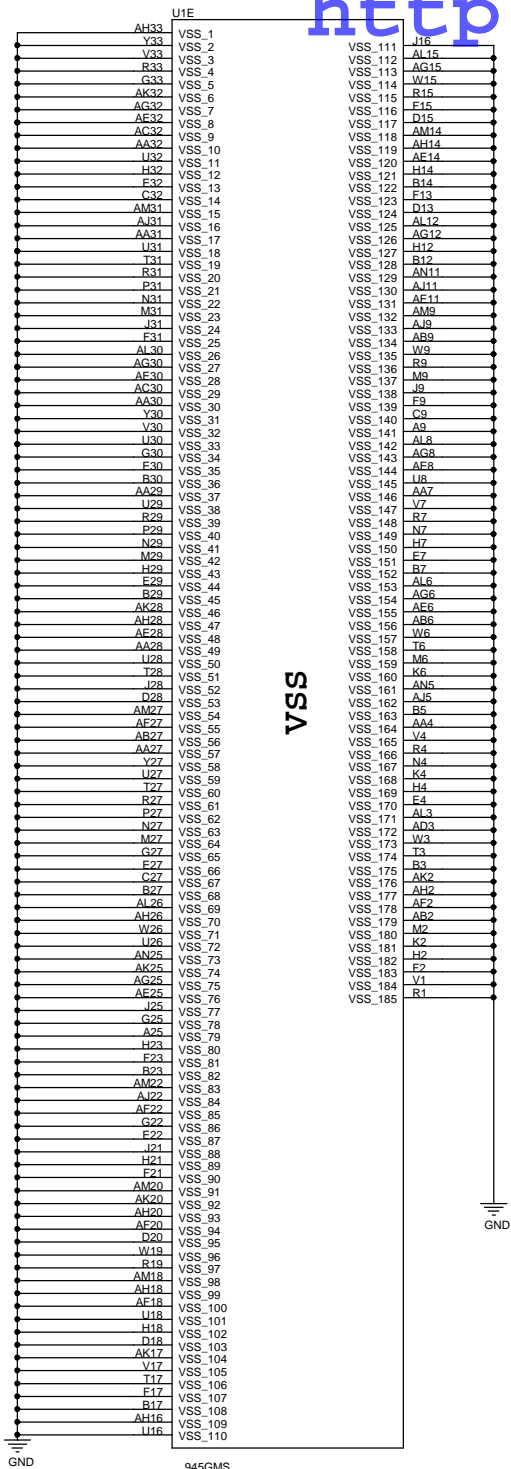
0:Normal Operation (Default)

1.:Reversal Lanes, 3->0,2->1..etc

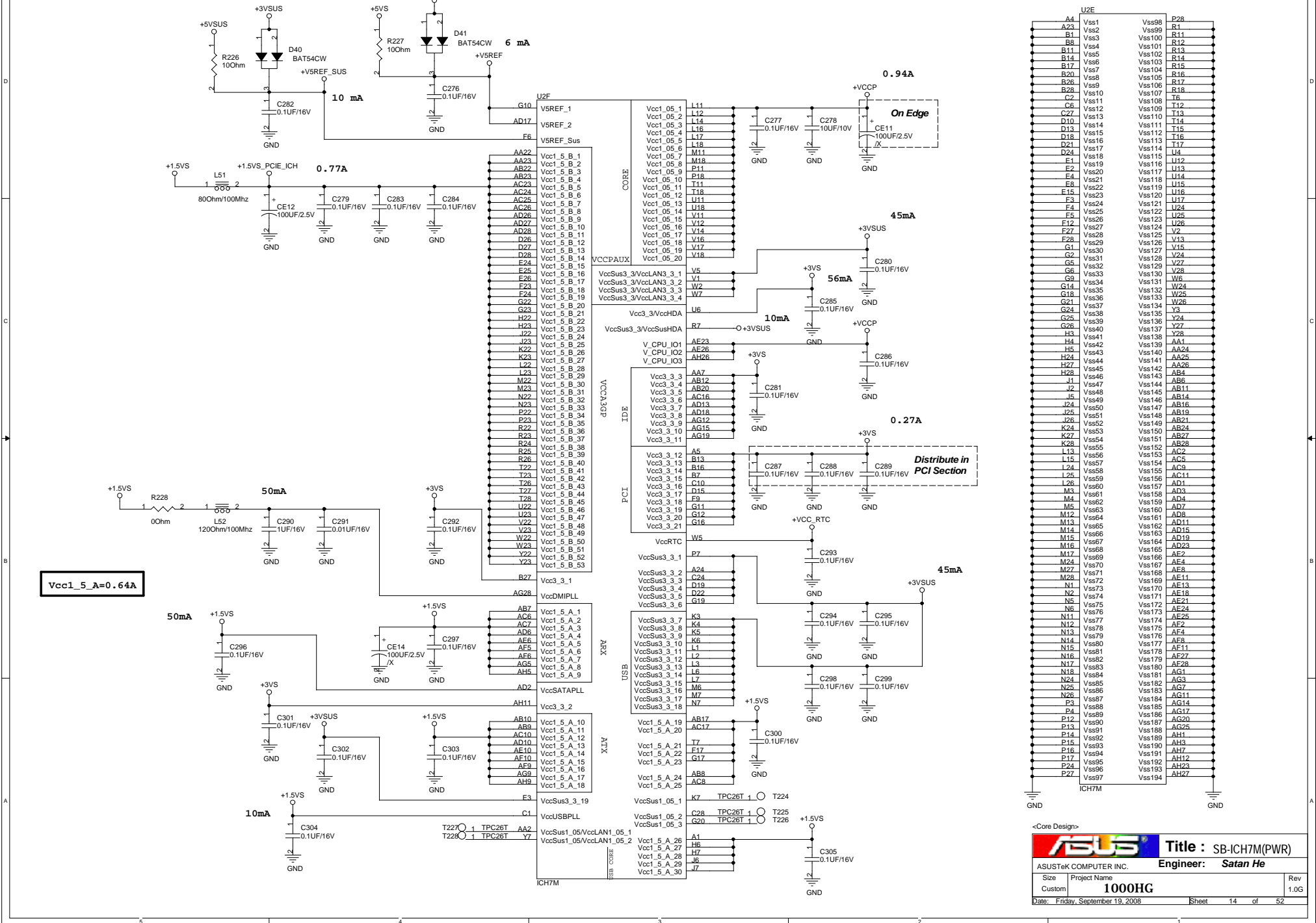
Note:945GMS doesn't support DMI Lane Reversal



<http://laptopblue.vn/>

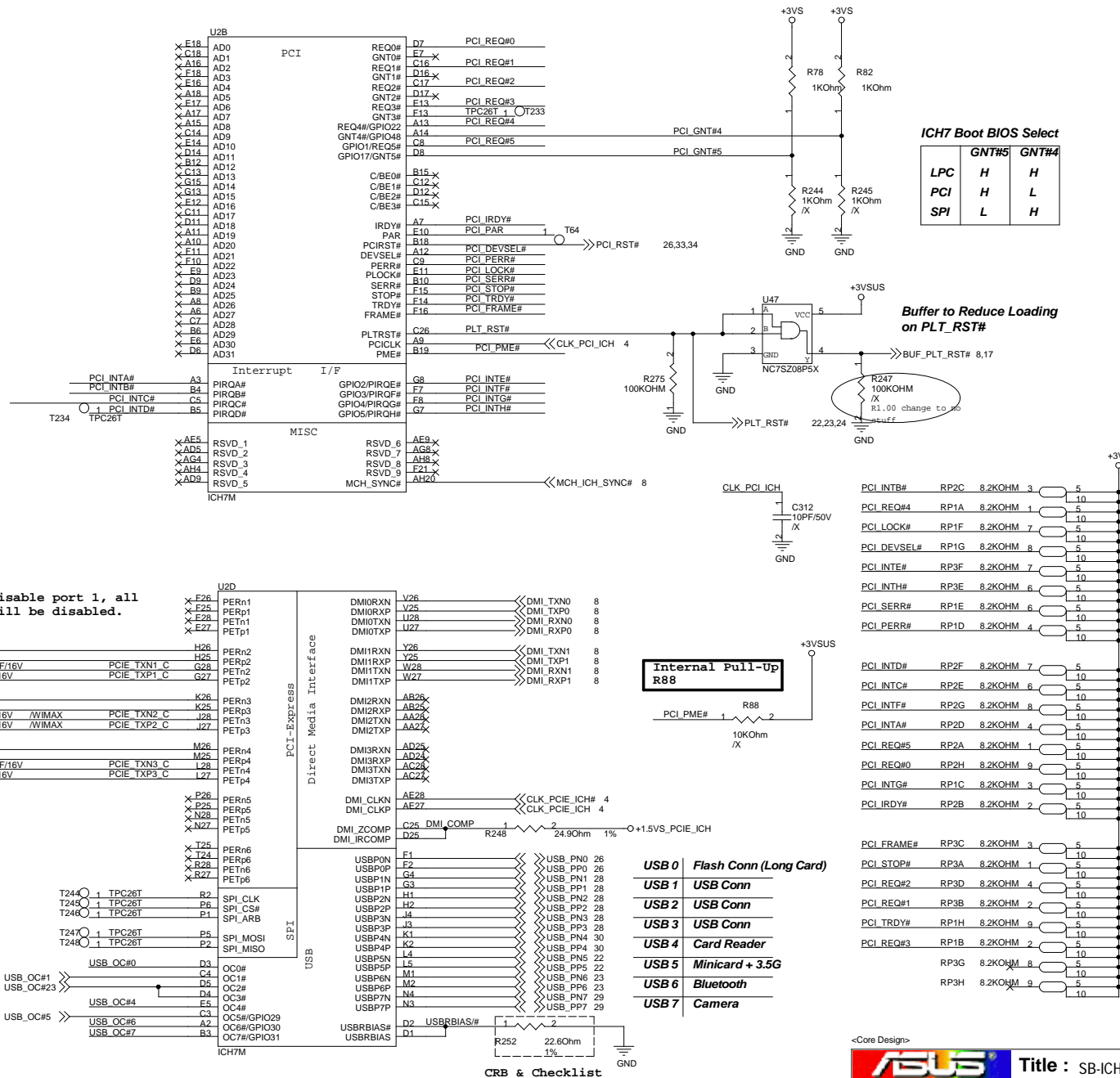


http://laptopblue.vn/



[illegible]





&lt;Core Design&gt;



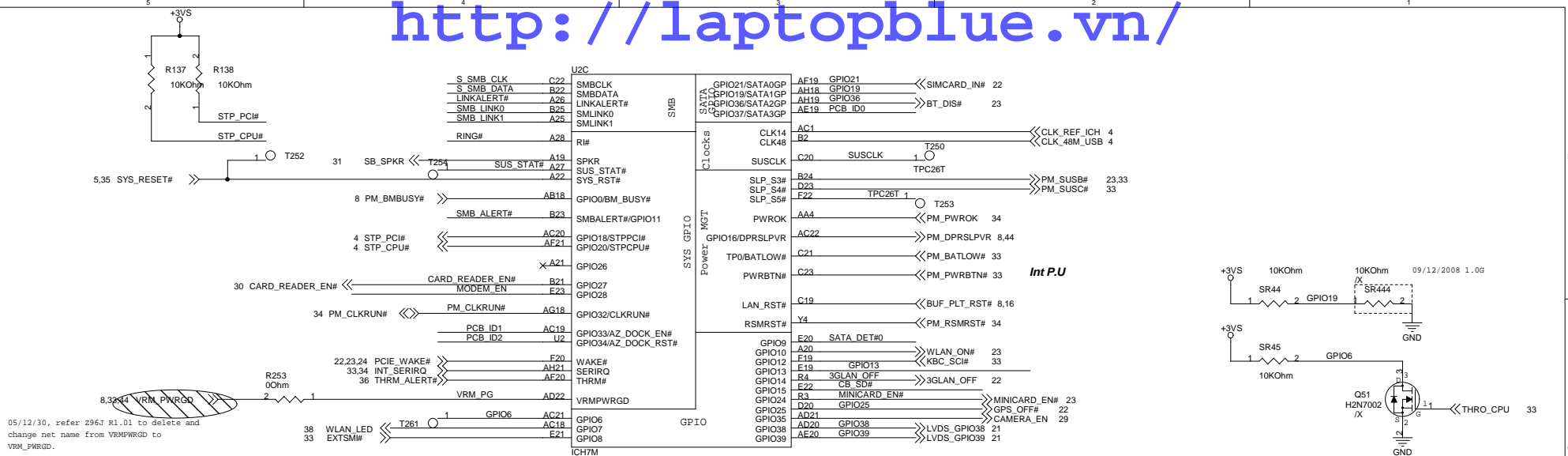
**Title :** SB-ICH7M(2)

ASUSTeK COMPUTER INC.

Engineer: *Satan He*

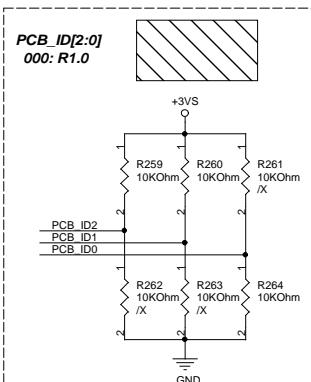
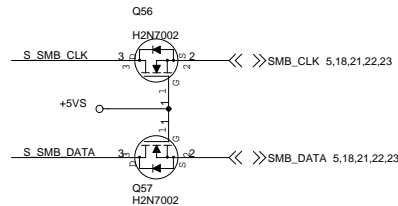
Size Custom	Project Name <b>1000HG</b>	Rev 1.0G
Date: Friday, September 19, 2008		Sheet 16 of 52





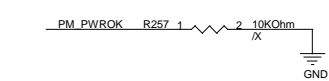
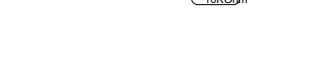
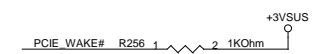
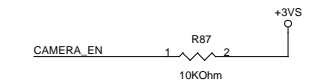
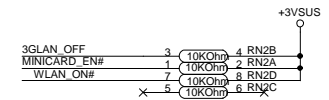
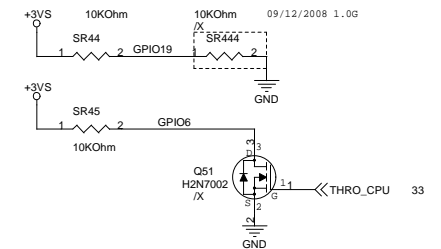
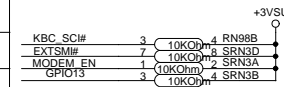
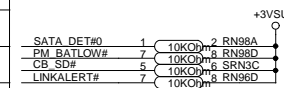
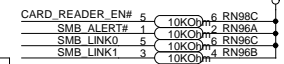
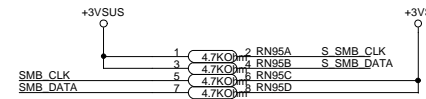
05/12/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM\_PWRGD.

S SMB\_CLK <<> S SMB\_CLK 4  
S SMB\_DATA <<> S SMB\_DATA 4



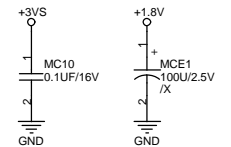
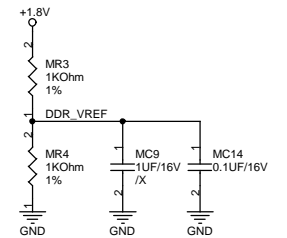
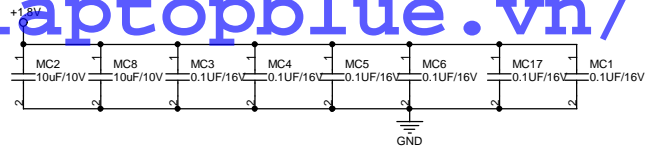
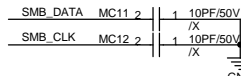
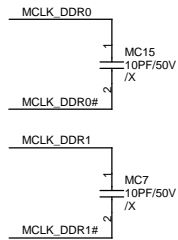
PCB\_VID3: PROJECT CODE

	WLAN_LED	WLAN	BT
High	v	v	v
High	v	x	x
High	x	v	v
Low	x	x	x



<Core Design>

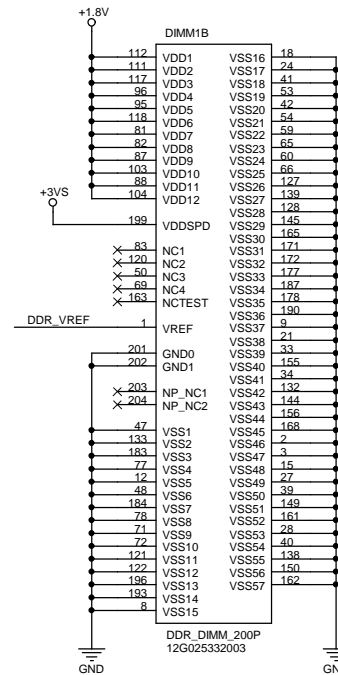
<b>ASUS</b>		Title : SB-ICH7M(3)	
ASUSTeK COMPUTER INC		Engineer: Satan He	
Size	Project Name	Rev	1.0G
Custom	1000HG	Date: Friday, September 19, 2008	Sheet 17 of 52



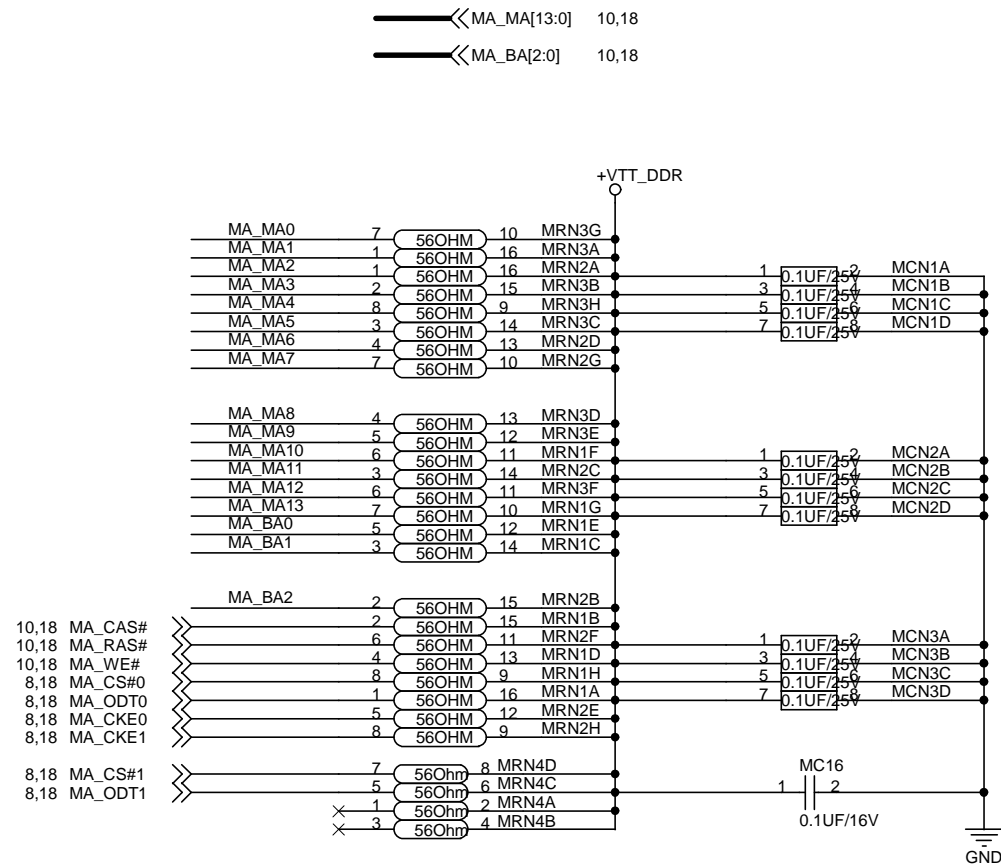
# STD Type

DIMM1A									
MA_MA0	102	A0	DO0	5	MA_DQ0				
MA_MA1	101	A1	DO1	7	MA_DQ1				
MA_MA2	100	A2	DO2	17	MA_DQ2				
MA_MA3	99	A3	DO3	19	MA_DQ3				
MA_MA4	98	A4	DO4	4	MA_DQ4				
MA_MA5	97	A5	DO5	6	MA_DQ5				
MA_MA6	94	A6	DO6	14	MA_DQ6				
MA_MA7	92	A7	DO7	16	MA_DQ7				
MA_MA8	93	A8	DO8	23	MA_DQ8				
MA_MA9	91	A9	DO9	25	MA_DQ9				
MA_MA10	105	A10/AP	DO10	35	MA_DQ10				
MA_MA11	90	A11	DO11	37	MA_DQ11				
MA_MA12	89	A12	DO12	20	MA_DQ12				
MA_MA13	116	A13	DO13	36	MA_DQ13				
	86	A14	DO14	38	MA_DQ14				
	X 84	A15	DO15	43	MA_DQ15				
	X 85	A16/BA2	DO16	45	MA_DQ16				
MA_BA0	107	BA0	DO17	45	MA_DQ17				
MA_BA1	106	BA1	DO18	55	MA_DQ18				
	110	SO#	DO19	44	MA_DQ19				
8,19 MA_CS#0		CK0	DO20	46	MA_DQ20				
8,19 MA_CS#1		CK1	DO21	56	MA_DQ21				
8 MCLK_DDR0		CK0#	DO22	58	MA_DQ22				
8 MCLK_DDR0#		CK1#	DO23	61	MA_DQ23				
8 MCLK_DDR1		CKE0	DO24	63	MA_DQ24				
8 MCLK_DDR1#		CKE1	DO25	73	MA_DQ25				
8,19 MA_CKE#		CAS#	DO26	75	MA_DQ26				
8,19 MA_CKE1		RAS#	DO27	62	MA_DQ27				
10,19 MA_CAS#		WE#	DO28	64	MA_DQ28				
10,19 MA_RAS#		SA0	DO29	74	MA_DQ29				
10,19 MA_WE#		SA1	DO30	76	MA_DQ30				
		SCL	DO31	123	MA_DQ31				
		SDA	DO32	125	MA_DQ32				
5,17,21,22,23 SMB_CLK		DO33	DO33	135	MA_DQ33				
5,17,21,22,23 SMB_DATA		DO34	DO34	137	MA_DQ34				
		DO35	DO35	124	MA_DQ35				
8,19 MA_ODT0		DO36	DO36	126	MA_DQ36				
8,19 MA_ODT1		DO37	DO37	134	MA_DQ37				
		DO38	DO38	136	MA_DQ38				
		DM0	DO39	141	MA_DQ39				
		DM1	DO40	143	MA_DQ40				
		DM2	DO41	151	MA_DQ41				
		DM3	DO42	153	MA_DQ42				
		DM4	DO43	140	MA_DQ43				
		DM5	DO44	142	MA_DQ44				
		DM6	DO45	152	MA_DQ45				
		DM7	DO46	154	MA_DQ46				
		DQS0	DO47	157	MA_DQ47				
		DQS1	DO48	159	MA_DQ48				
		DQS2	DO49	123	MA_DQ49				
		DQS3	DO50	175	MA_DQ50				
		DQS4	DO51	158	MA_DQ51				
		DQS5	DO52	160	MA_DQ52				
		DQS6	DO53	174	MA_DQ53				
		DQS7	DO54	176	MA_DQ54				
		DQS#0	DO55	179	MA_DQ55				
		DQS#1	DO56	181	MA_DQ56				
		DQS#2	DO57	189	MA_DQ57				
		DQS#3	DO58	191	MA_DQ58				
		DQS#4	DO59	180	MA_DQ59				
		DQS#5	DO60	182	MA_DQ60				
		DQS#6	DO61	192	MA_DQ61				
		DQS#7	DO62	194	MA_DQ62				
			DO63		MA_DQ63				

GROUP1  
GROUP2  
SWAP

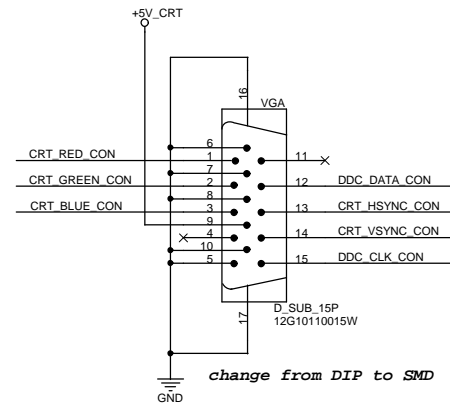
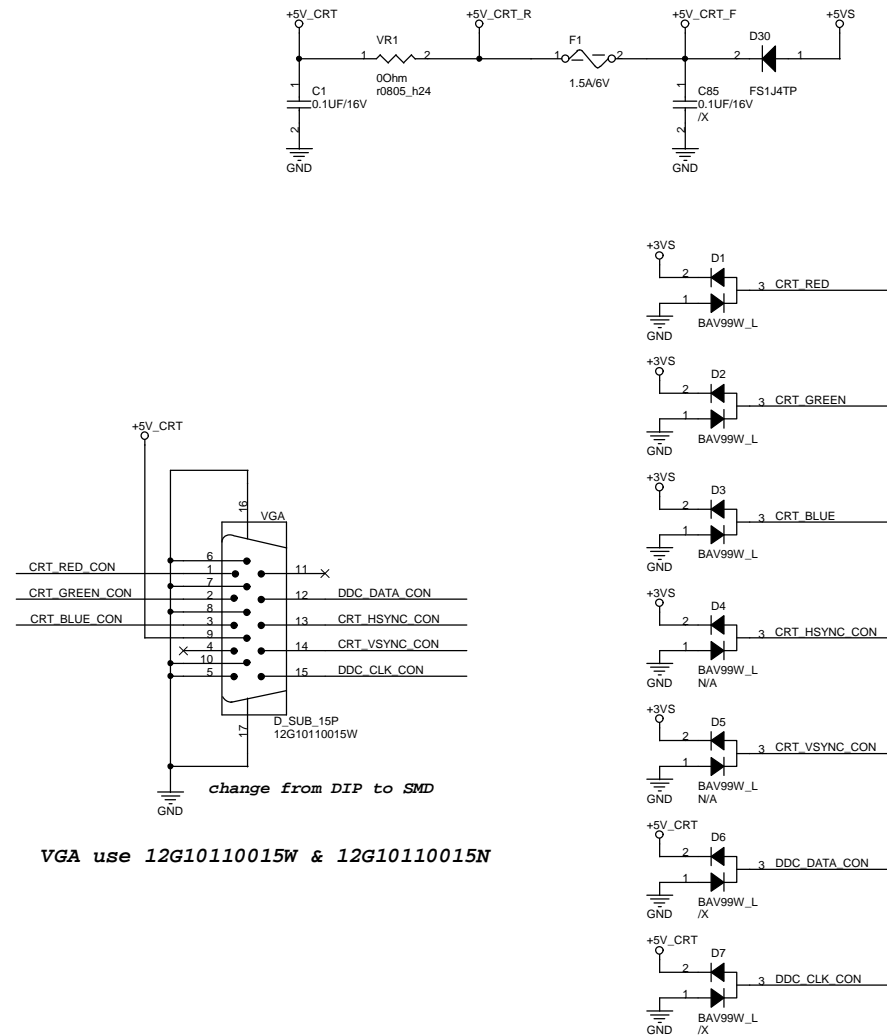
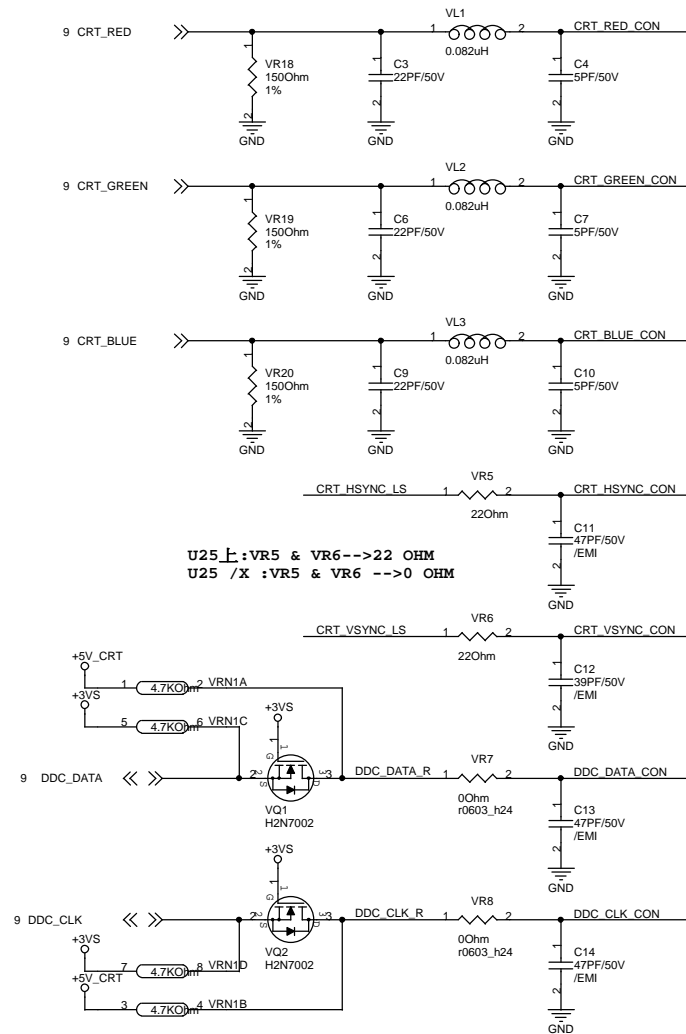


<Core Design>

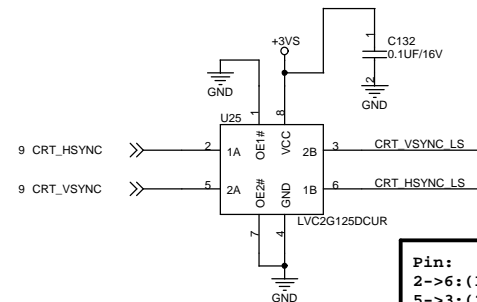


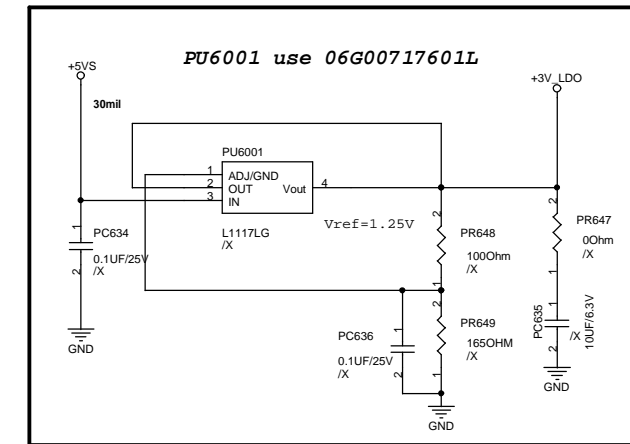
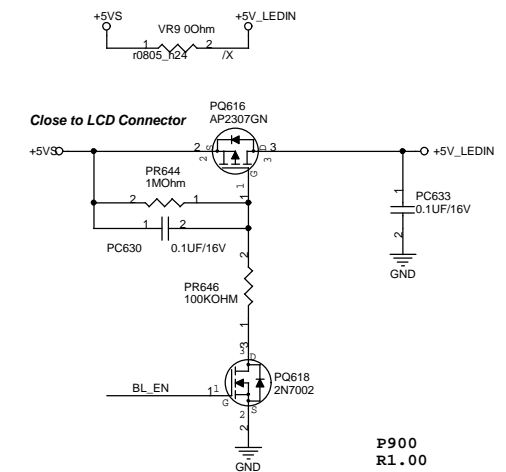
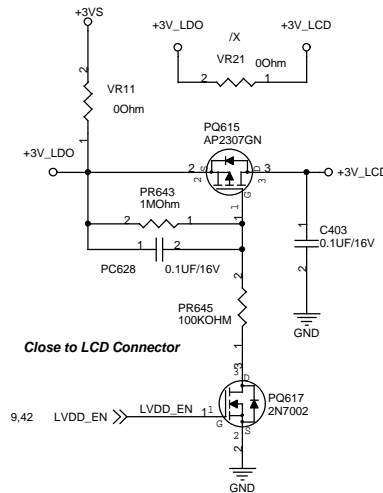
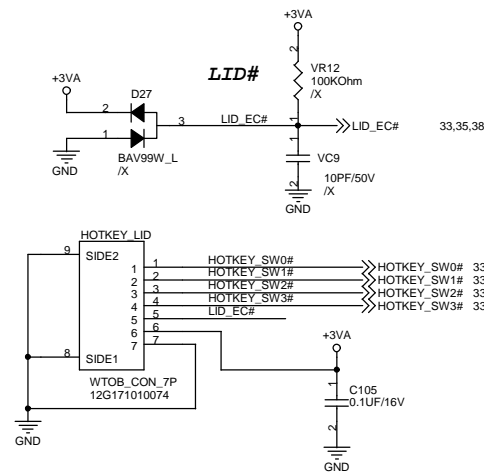
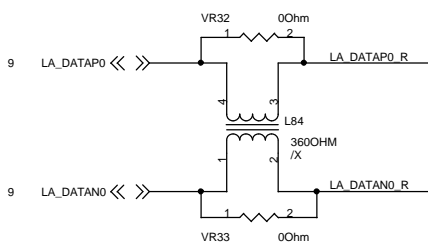
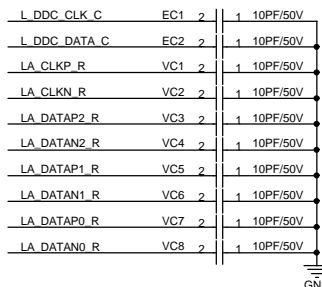
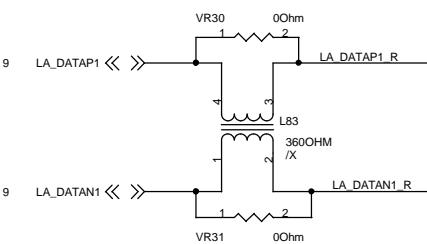
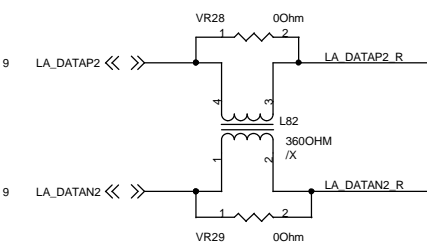
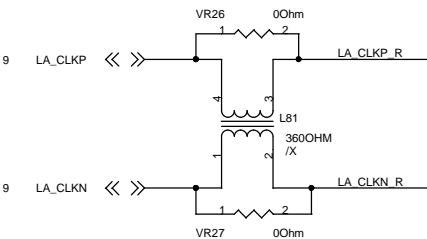
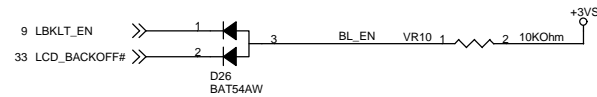
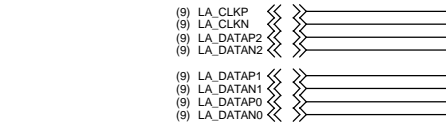
<Core Design>

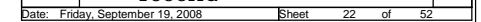
		<b>Title :</b> DDR2_Termination	
ASUSTek Computer INC.		<b>Engineer:</b> Kell_Huang	
Size A4	Project Name <b>1000HG</b>		Rev 1.0G
Date: Friday, September 19, 2008		Sheet	19 of 52

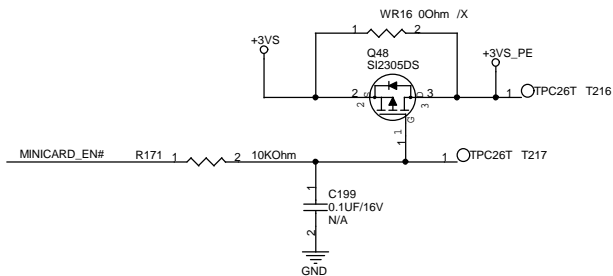


VGA use 12G10110015W & 12G10110015N

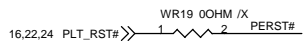
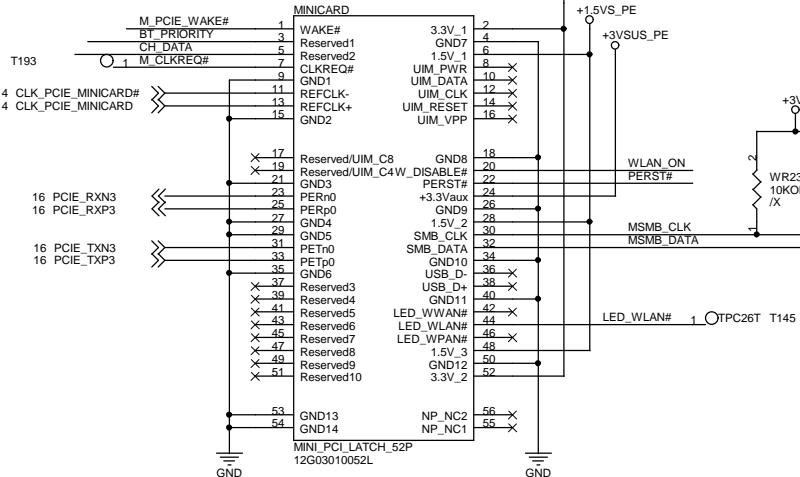




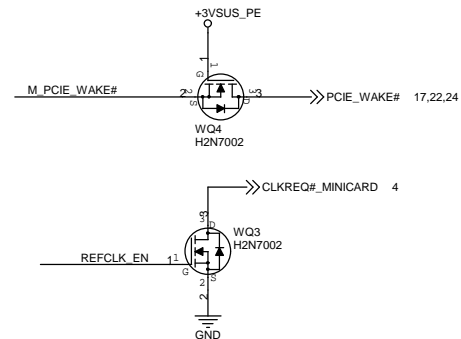
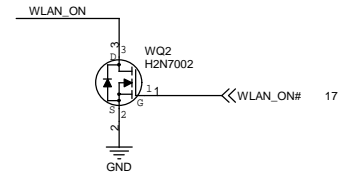
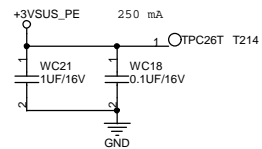
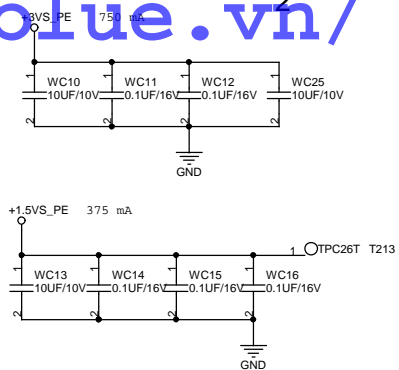
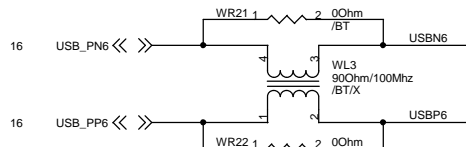
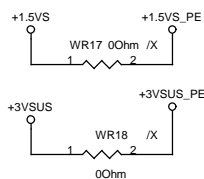
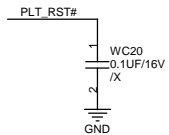
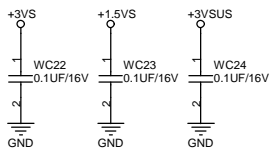
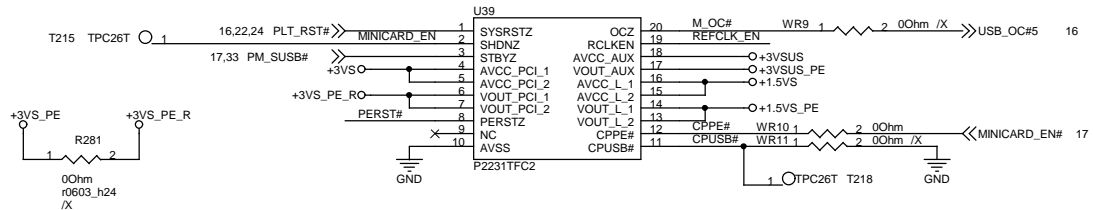




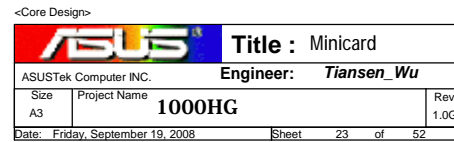
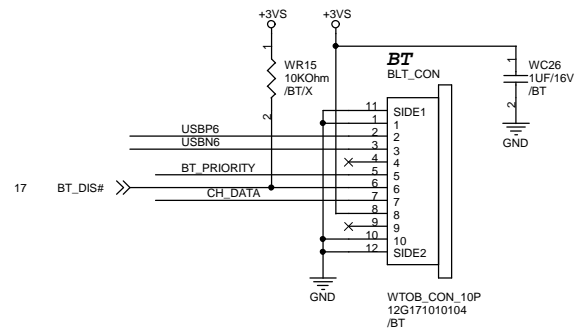
MINICARD use 12G03010052Q

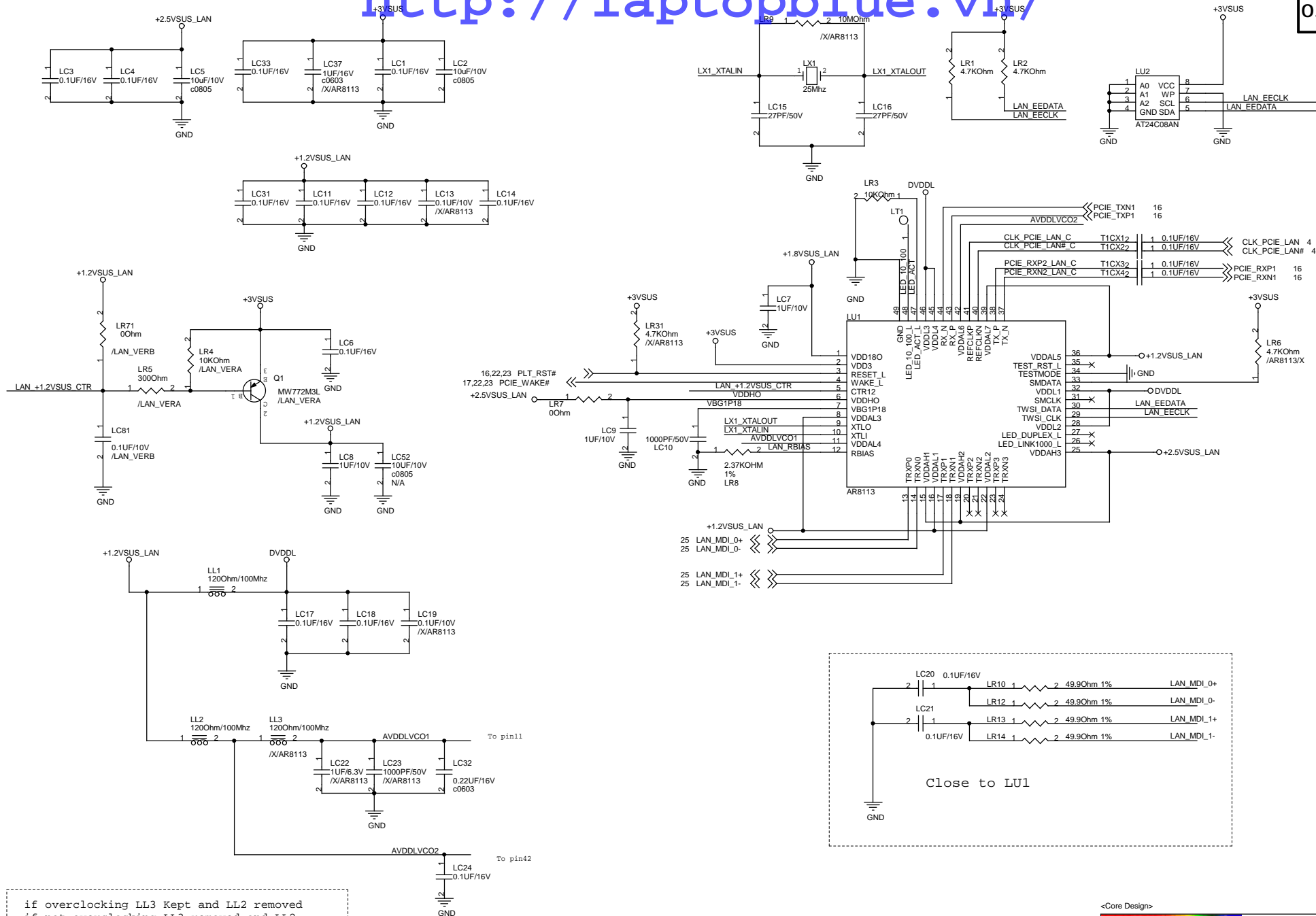


U39 use 06G030057011



## BlueTooth

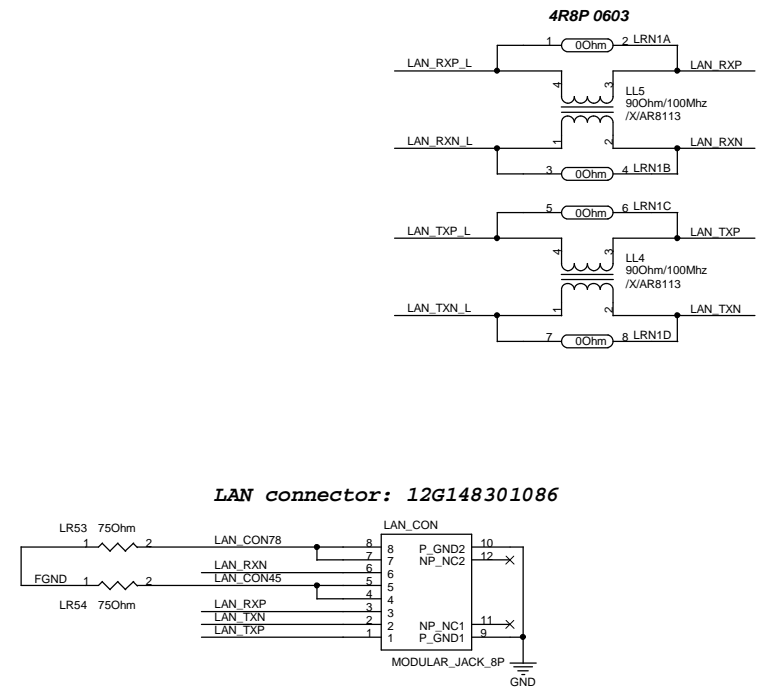
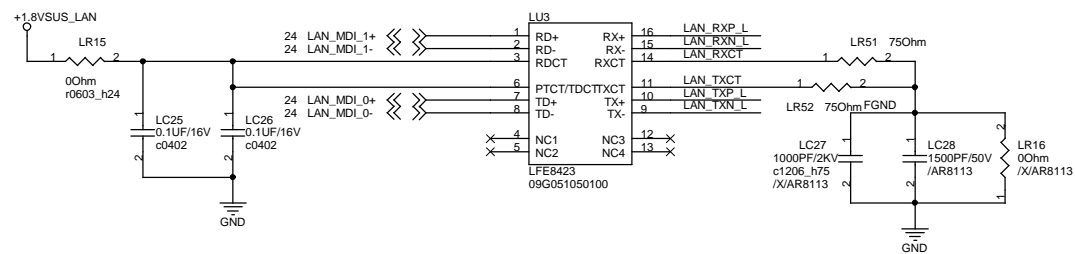




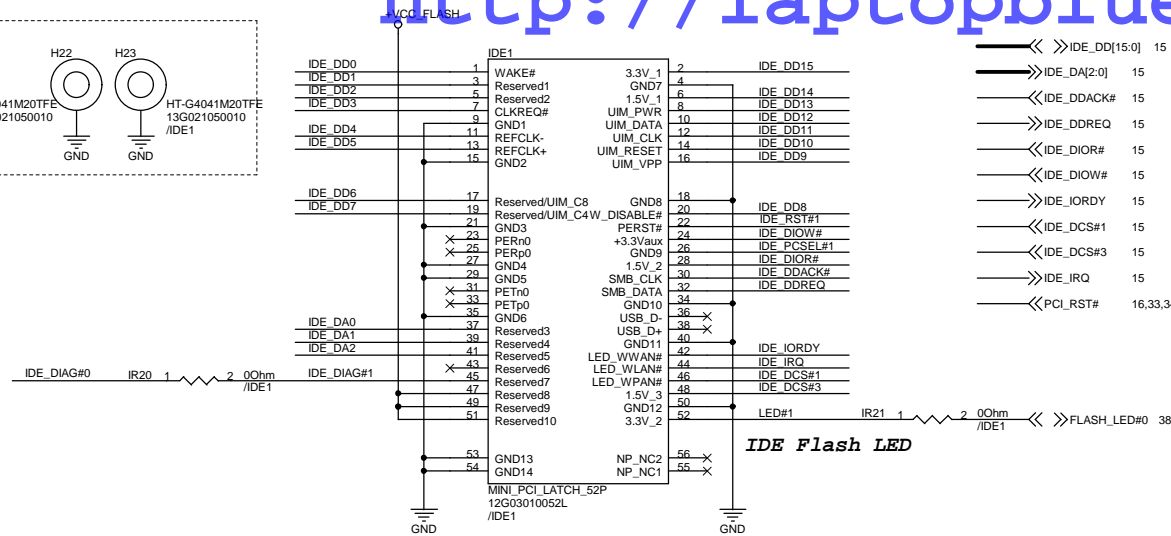
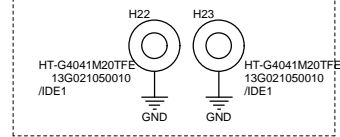
if overclocking LL3 Kept and LL2 removed  
if not overclocking LL3 removed and LL2 Kept

<Core Design>

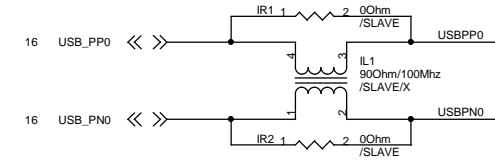
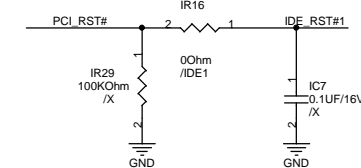
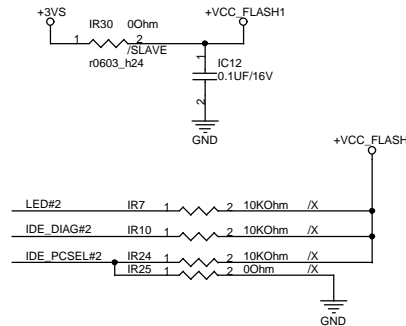
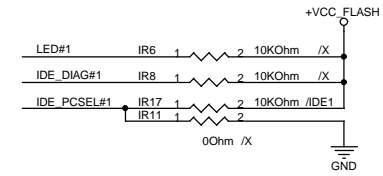
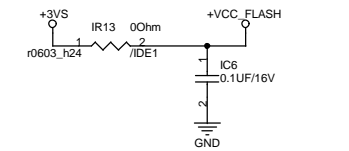
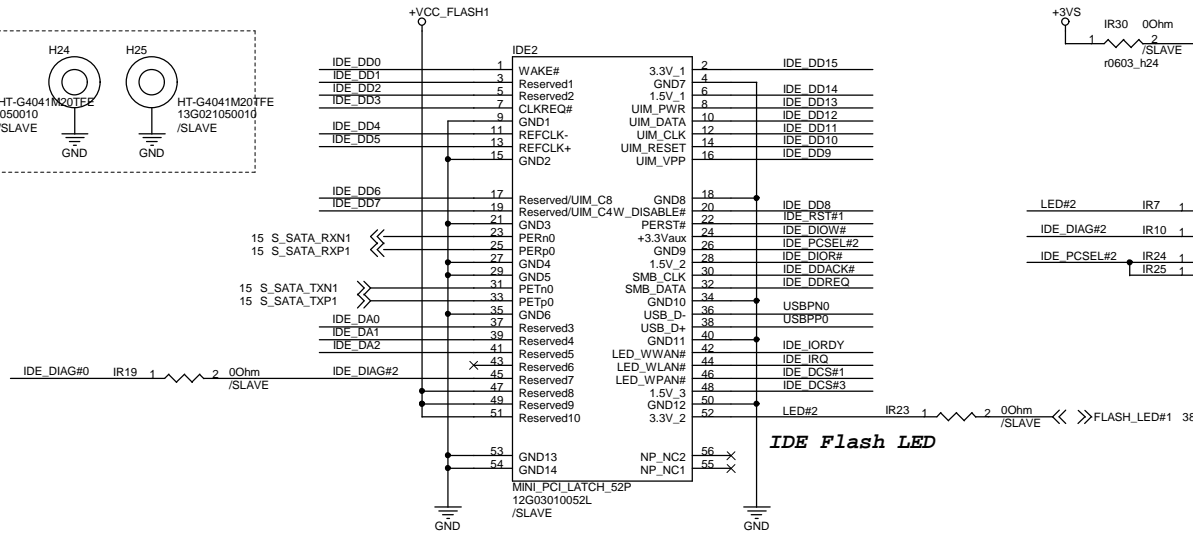
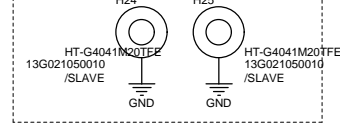




短卡



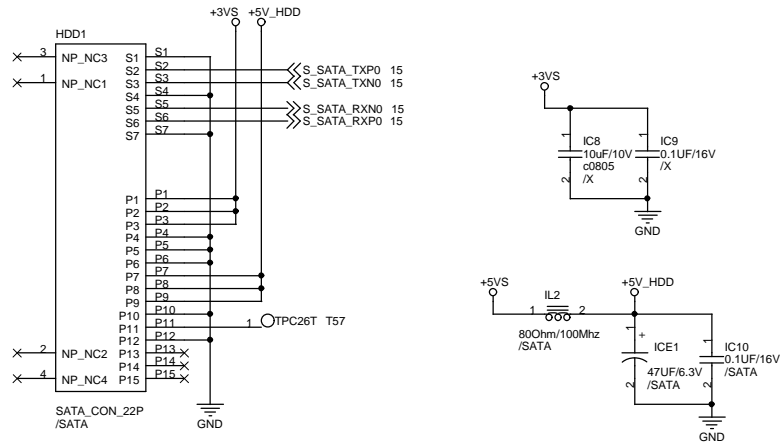
長卡




**Naming Rule:**  
IC: IU?  
R: IR?  
C: IC?  
L: IL?

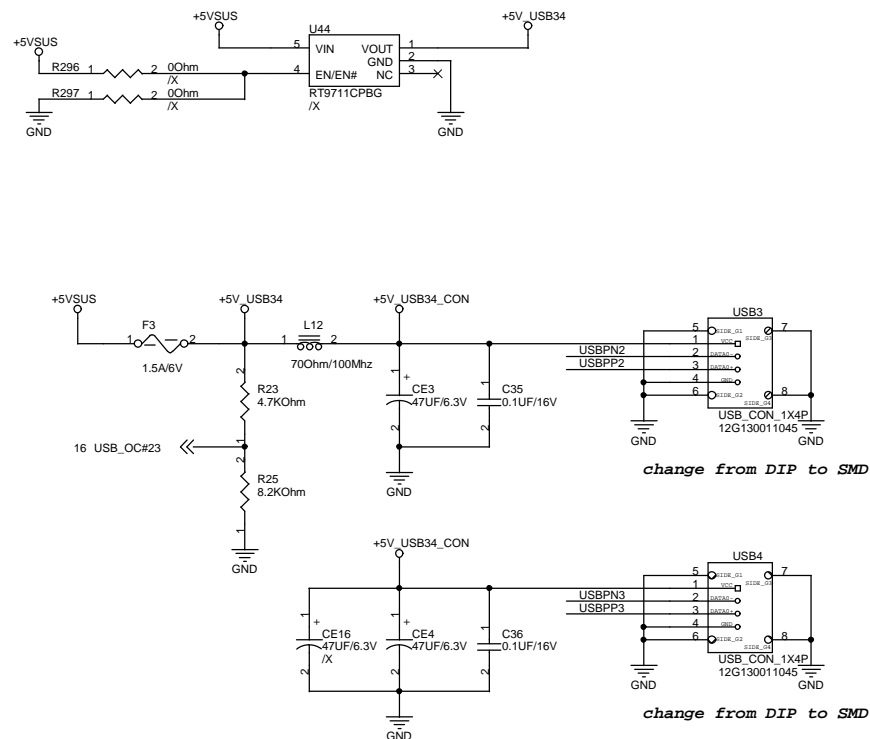
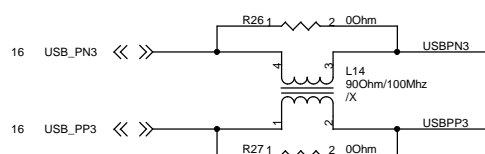
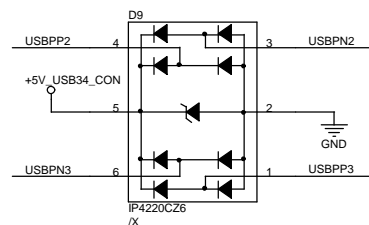
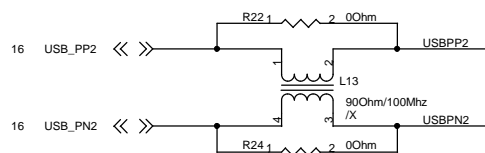
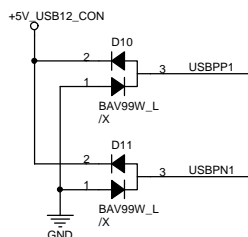
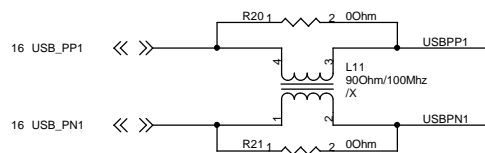
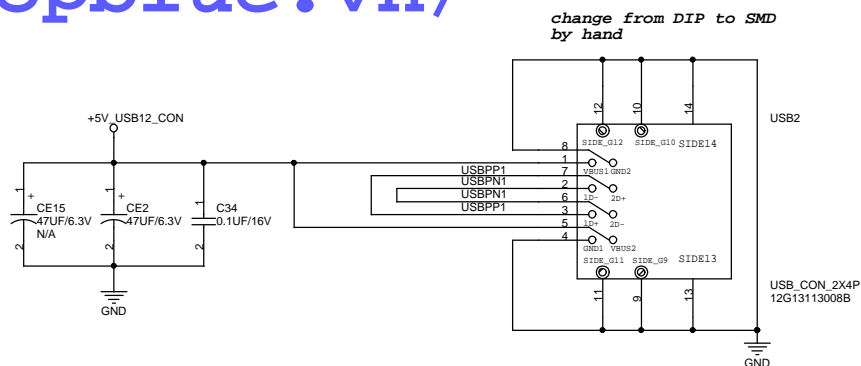
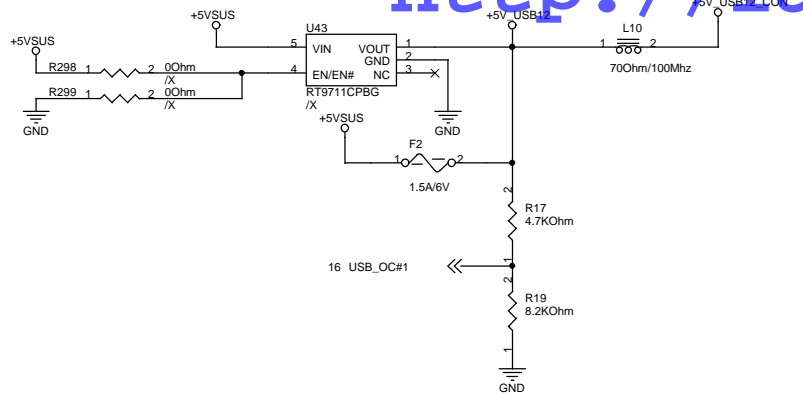
Change ODD to  
SATA IF

## SATA HDD Connector



<Core Design>

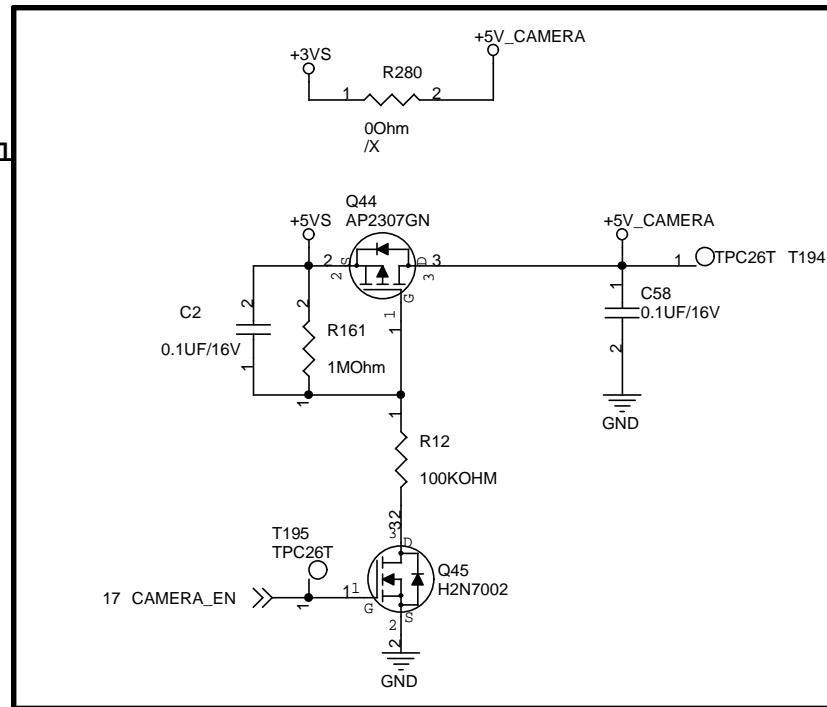
		<b>Title :</b> SATA HDD	
ASUSTek Computer INC.		<b>Engineer:</b> <i>KingCa_Jin</i>	
Size A3	Project Name <b>1000HG</b>		Rev 1.0G
Date: Friday, September 19, 2008		Sheet 27 of 52	



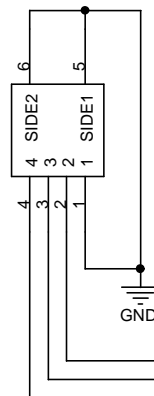
<Core Design>

<b>ASUS</b>		<b>Title : USB Port</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 28 of 52	

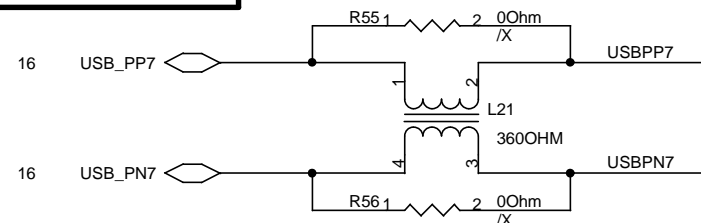
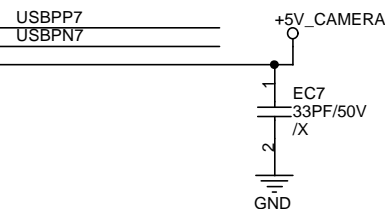
## Power Control



CAMERA  
WtoB\_CON\_4P



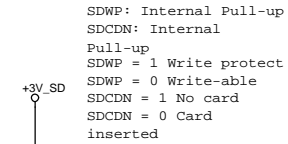
## CAMERA USB Interface



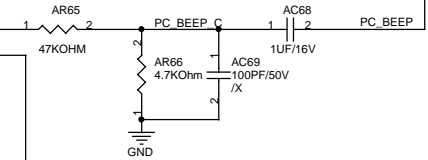
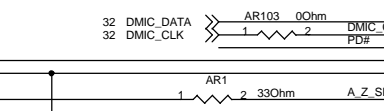
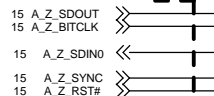
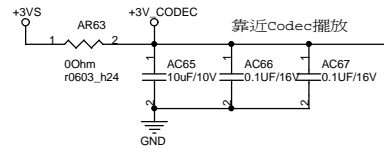
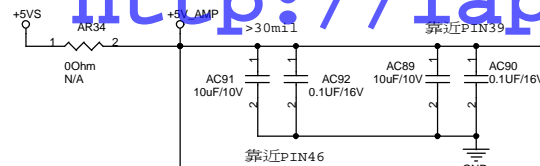
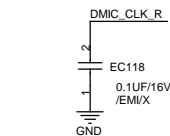
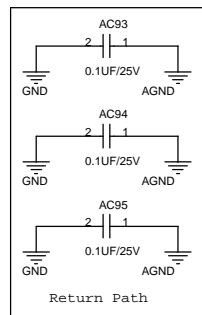
<Core Design>

<b>ASUS</b>		<b>Title : Camera Power</b>	
ASUSTek Computer INC.		<b>Engineer: Kell_Huang</b>	
Size A4	Project Name <b>1000HG</b>		Rev 1.0G
Date: Friday, September 19, 2008		Sheet	29 of 52

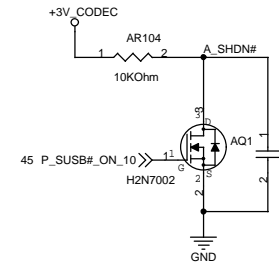
CLKSEL:		CRR10
B52: Internal pull-down		10KOhm
C52: Internal pull-up		/C52/X



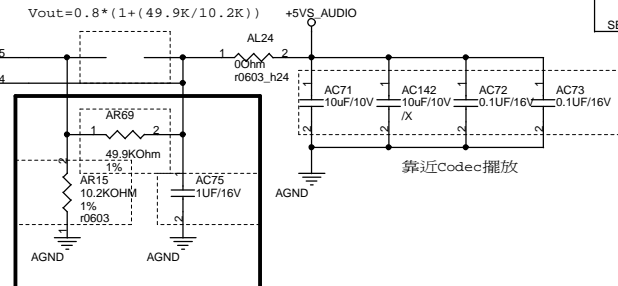
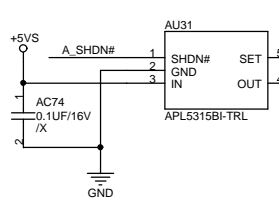
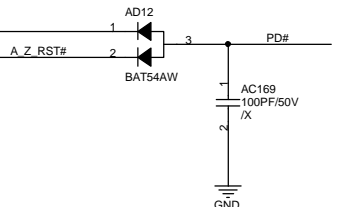
```
Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.
```



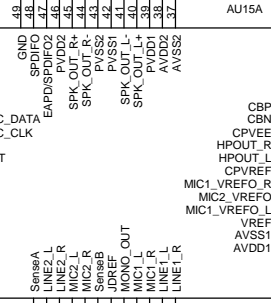
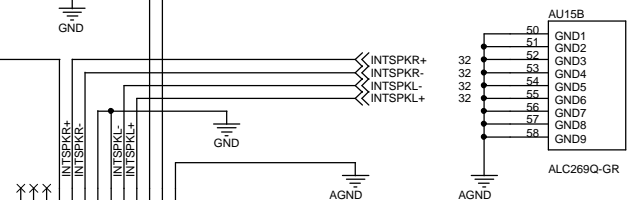
OP\_SD#: Controlled by EC to power down Class-D speaker amp.



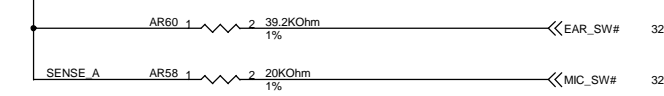
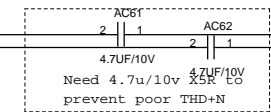
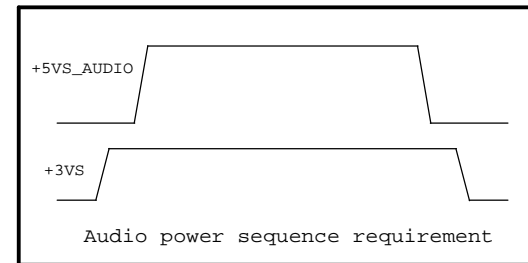
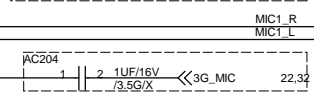
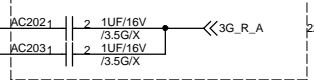
PD#: Internal Pull-up 50K to +3V



For Audio Noise Issue

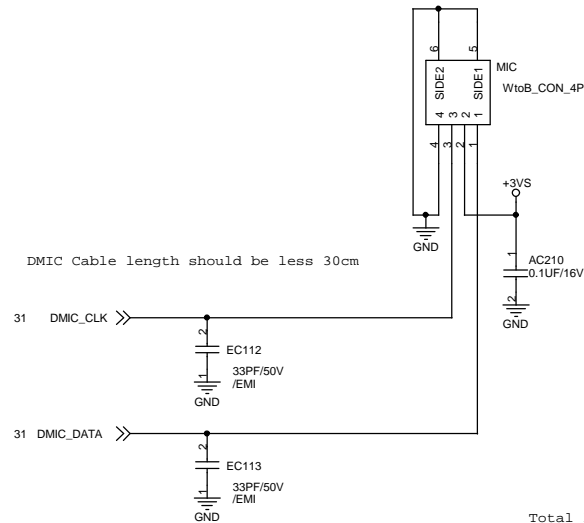


Analogs: Pin.13~Pin.38  
Digital: Pin.1~Pin.12 and Pin.39~Pin.48

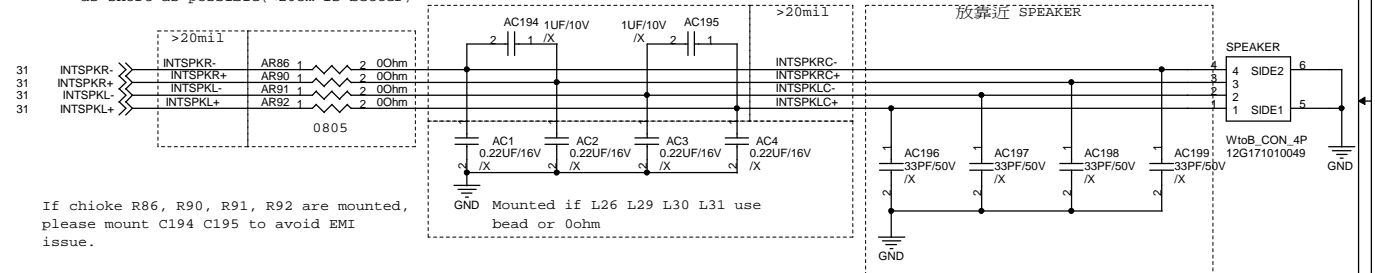


<Core Design>

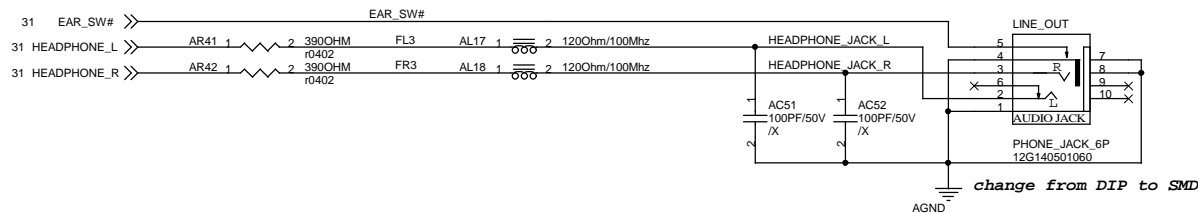
<b>ASUS</b>		<b>Title : ALC269-1</b>	
ASUSTek Computer Inc.		Engineer: Mick	
Size A3	Project Name 1000HG	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 31 of 52	



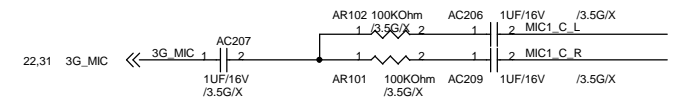
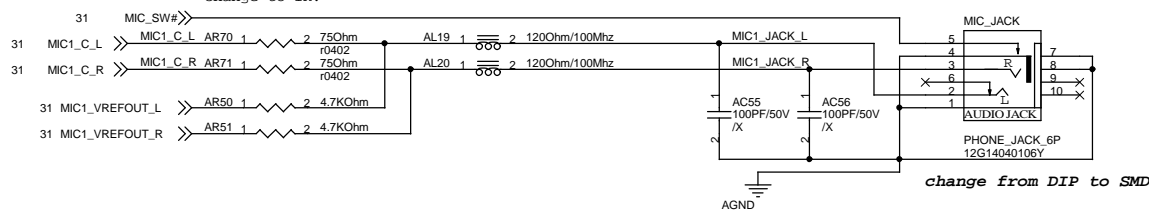
Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)



#### LINE\_OUT use 12G140501060



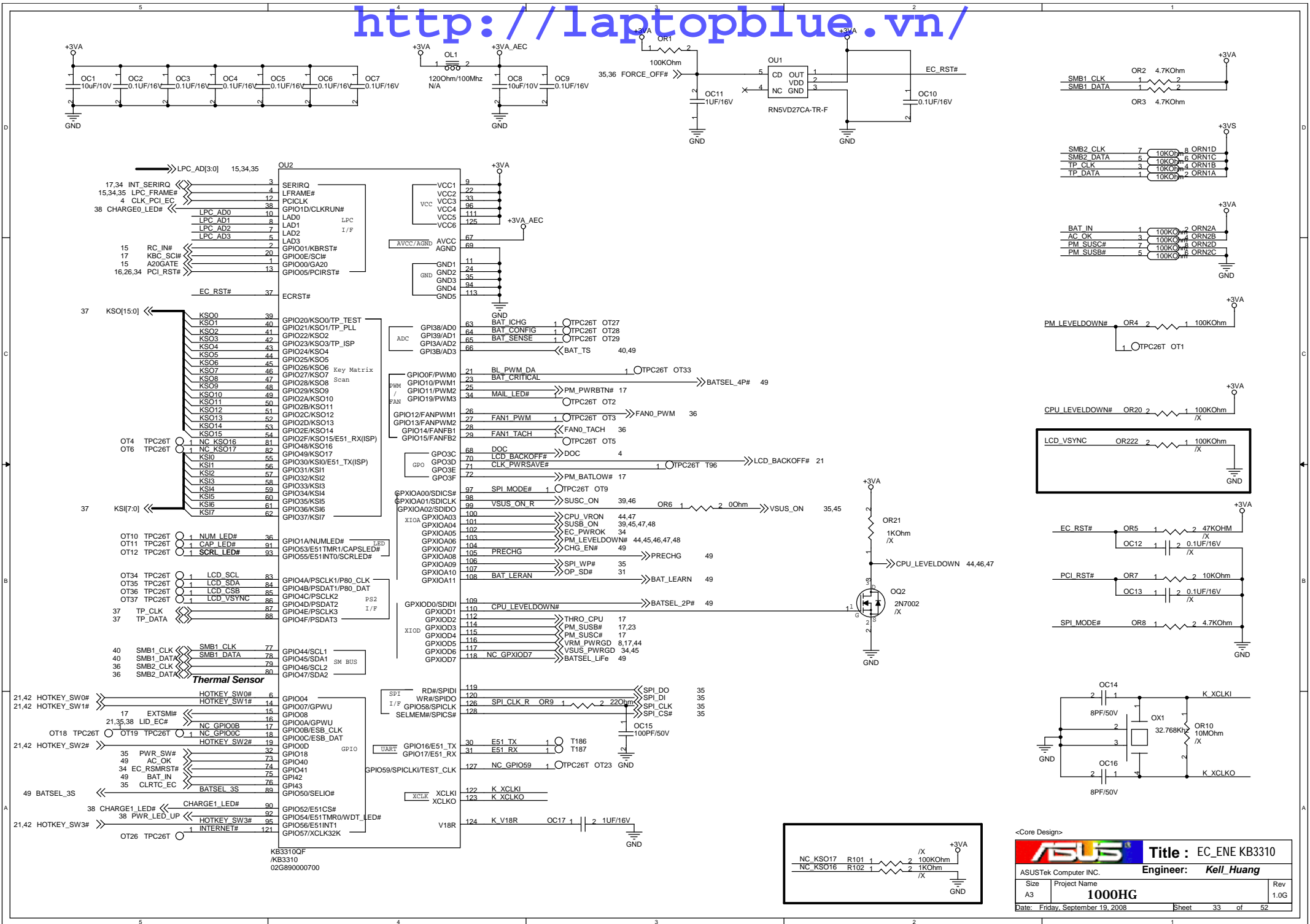
#### MIC\_JACK use 12G14040106Y

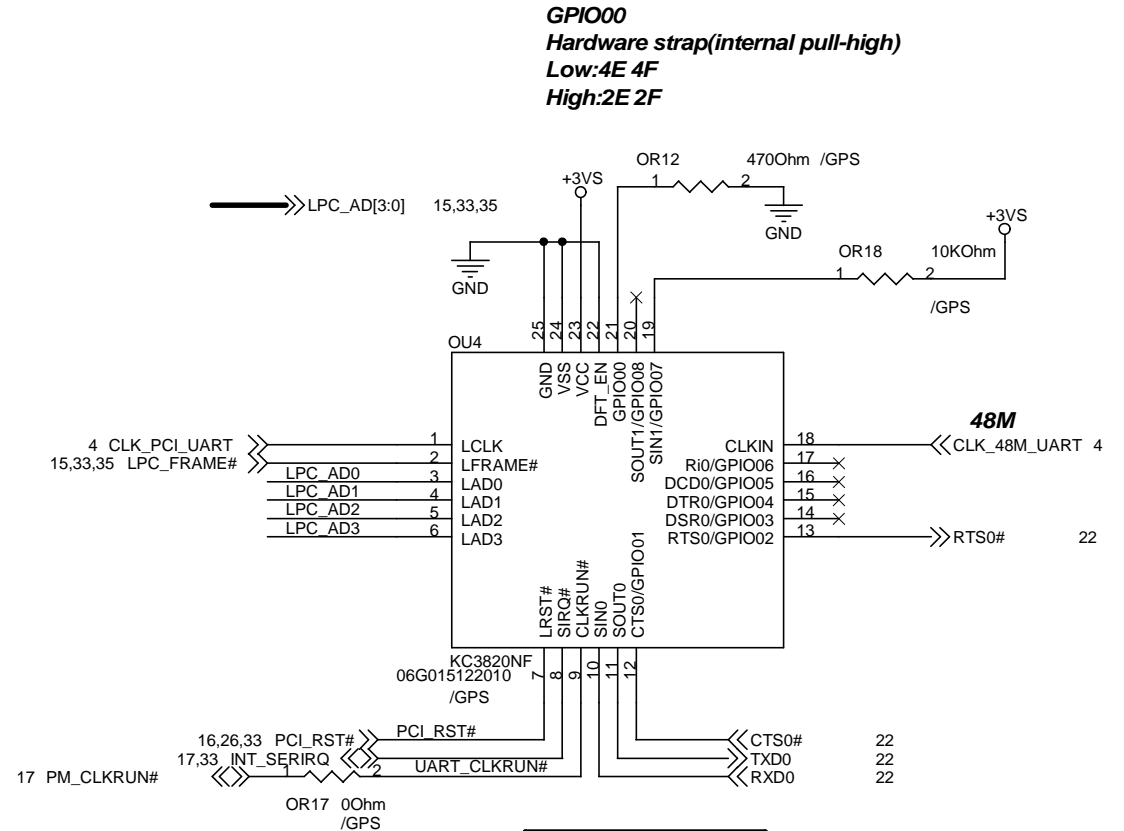
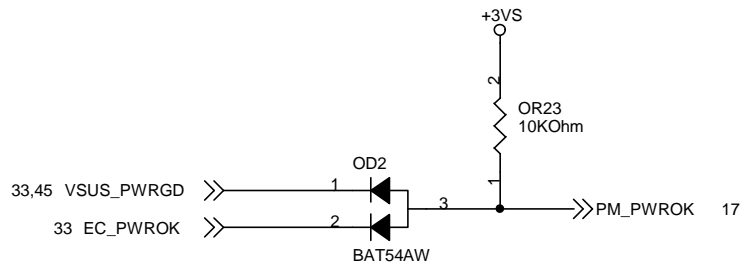
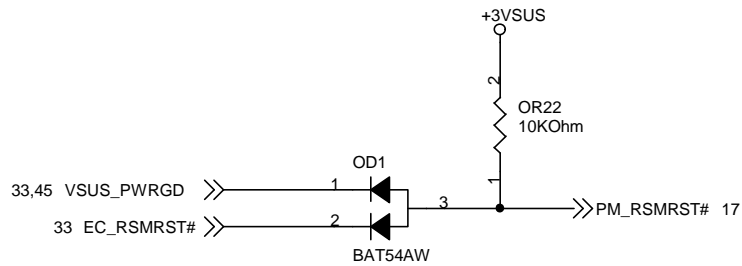


<Core Design>

<b>ASUS</b>		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name 1000HG	Rev 1.0G	
Date: Friday, September 19, 2008	Sheet	32	of 52



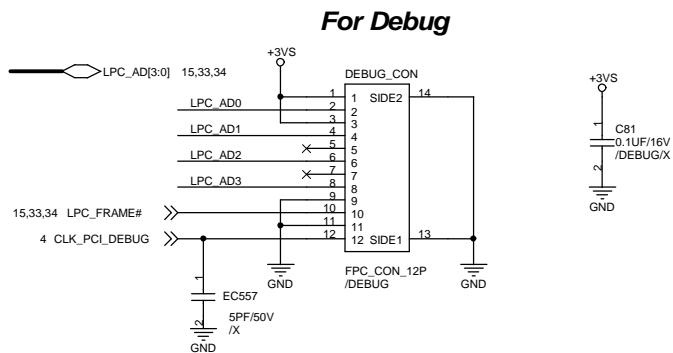
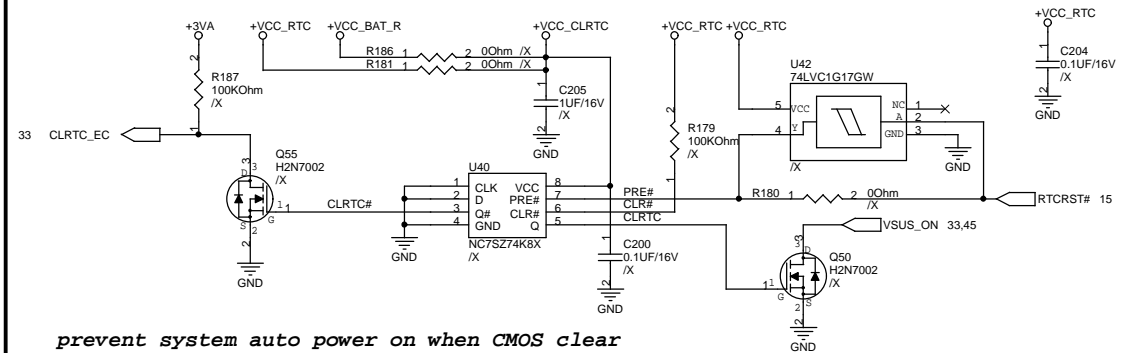
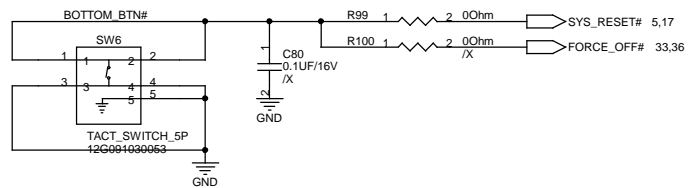
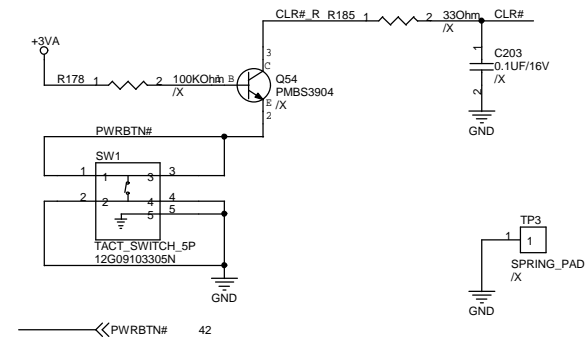
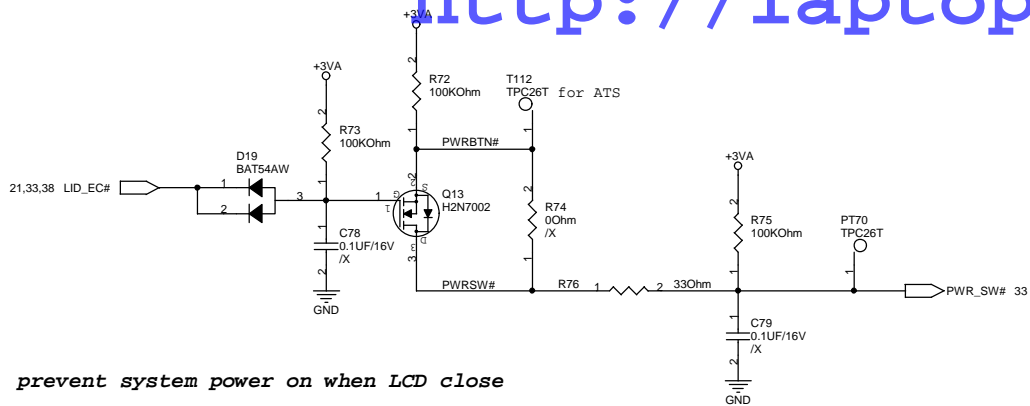




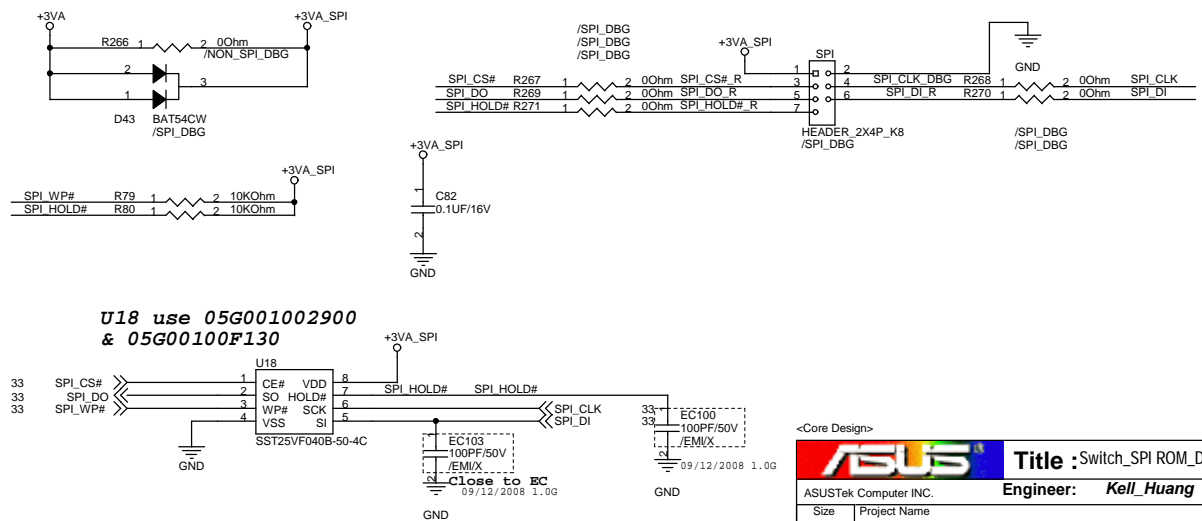
UART Control  
IC for using  
GPS module due  
to no UART on  
ENE EC

<Core Design>

http://laptopblue.vn/



```
Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125
```

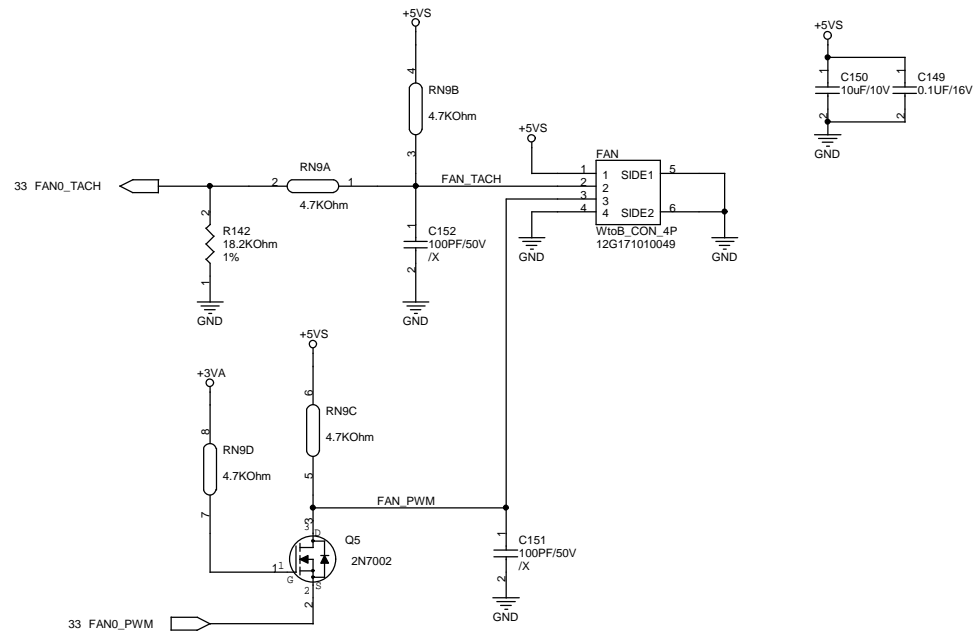
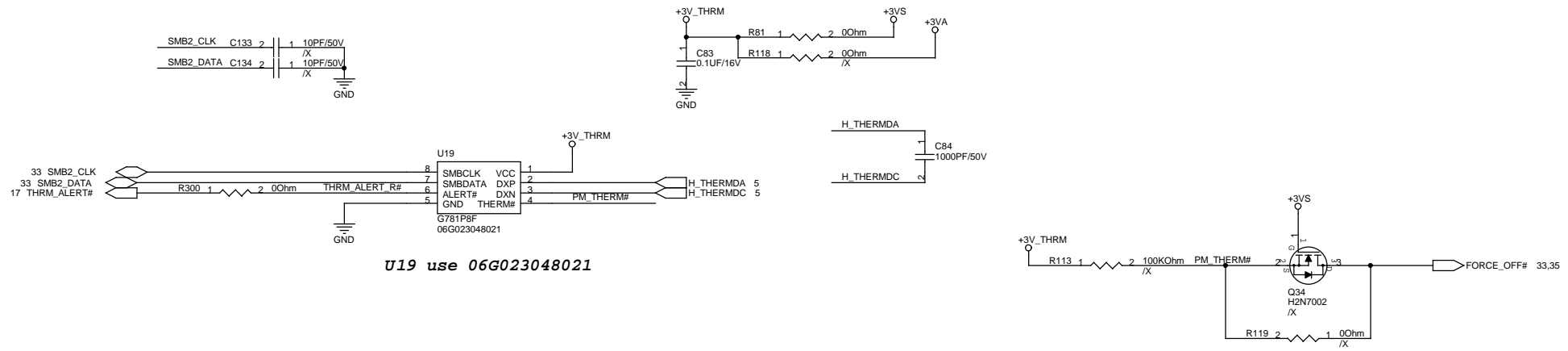


&lt;Core Design&gt;



**Title :** Switch\_SPI ROM\_Debug

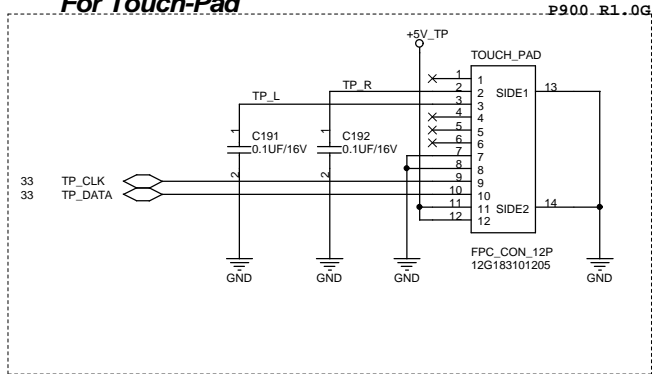
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 35 of 52	



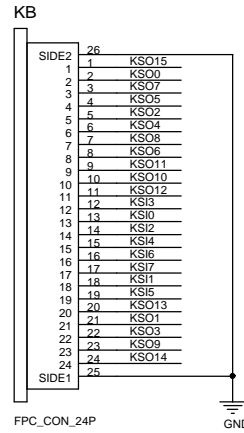
<Core Design>

ASUS		Title : Thermal Sensor_FAN	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	1000HG	1.0G	
Date: Friday, September 19, 2008		Sheet	36 of 52

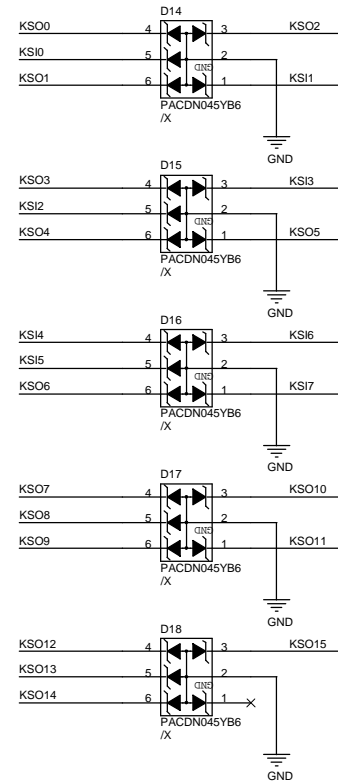
### For Touch-Pad



### For Keyboard Connector

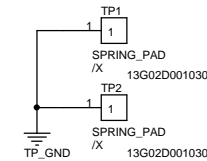
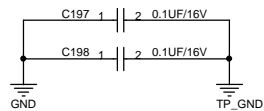
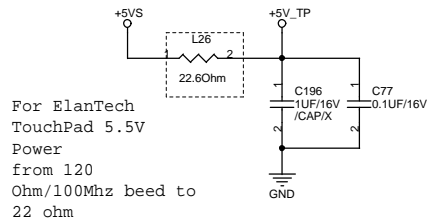
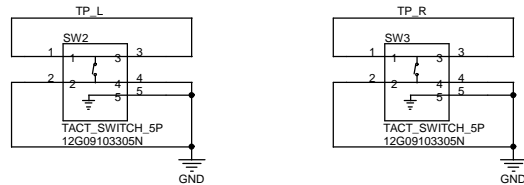


KSO[15:0] 33  
KSI[7:0] 33



KSI0	EC10	1	2	33PF/50V
KSI1	EC11	1	2	33PF/50V
KSI2	EC12	1	2	33PF/50V
KSI3	EC13	1	2	33PF/50V
KSI4	EC14	1	2	33PF/50V
KSI5	EC15	1	2	33PF/50V
KSI6	EC16	1	2	33PF/50V
KSI7	EC17	1	2	33PF/50V
KSO0	EC18	1	2	33PF/50V
KSO1	EC19	1	2	33PF/50V
KSO2	EC20	1	2	33PF/50V
KSO3	EC21	1	2	33PF/50V
KSO4	EC22	1	2	33PF/50V
KSO5	EC23	1	2	33PF/50V
KSO6	EC24	1	2	33PF/50V
KSO7	EC25	1	2	33PF/50V
KSO8	EC26	1	2	33PF/50V
KSO9	EC27	1	2	33PF/50V
KSO10	EC28	1	2	33PF/50V
KSO11	EC29	1	2	33PF/50V
KSO12	EC30	1	2	33PF/50V
KSO13	EC31	1	2	33PF/50V
KSO14	EC32	1	2	33PF/50V
KSO15	EC33	1	2	33PF/50V

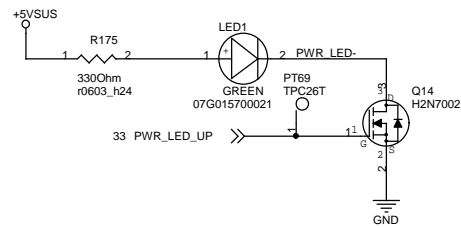
**SW2, SW3 use 12G09103305N**



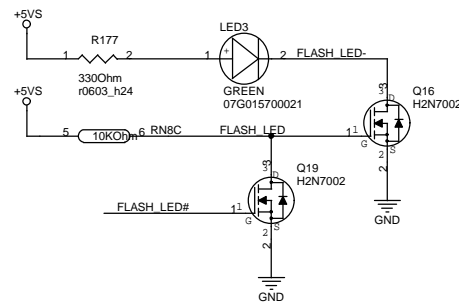
<Core Design>

<b>ASUS</b>		<b>Title : KB_Touch Pad</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 37 of 52	

### for POWER LED

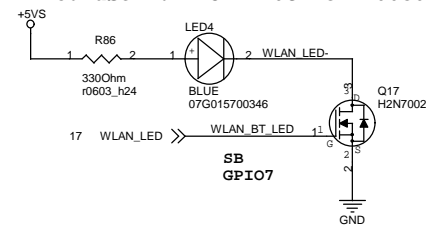


### for FLASH LED

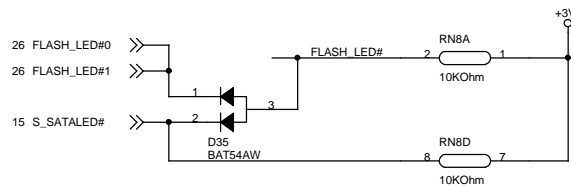
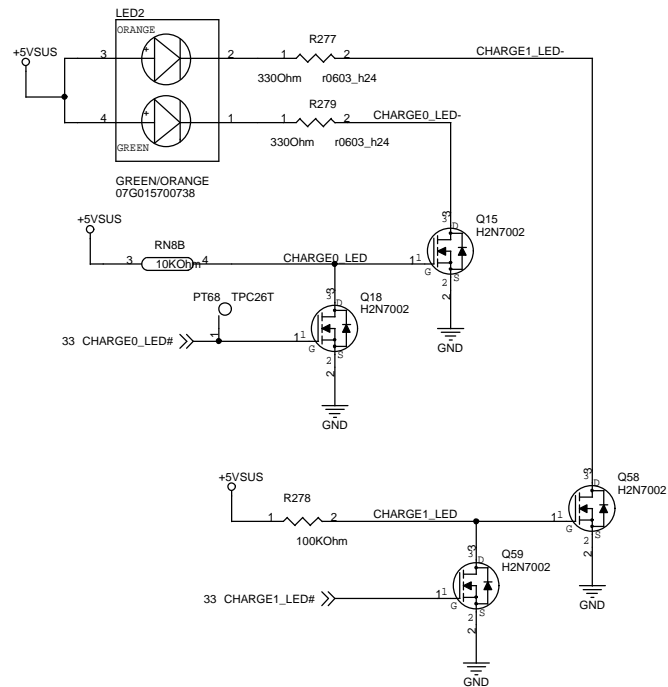


### for WLAN/BlueTooth LED

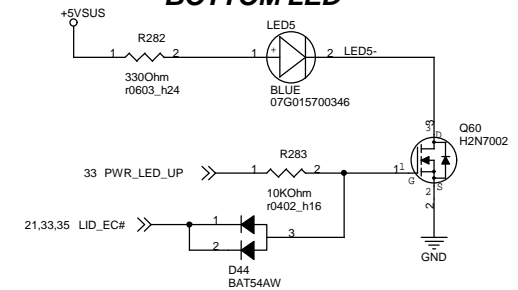
R86 use 4.7K OHm 10G213472003030



### for CHARGE LED

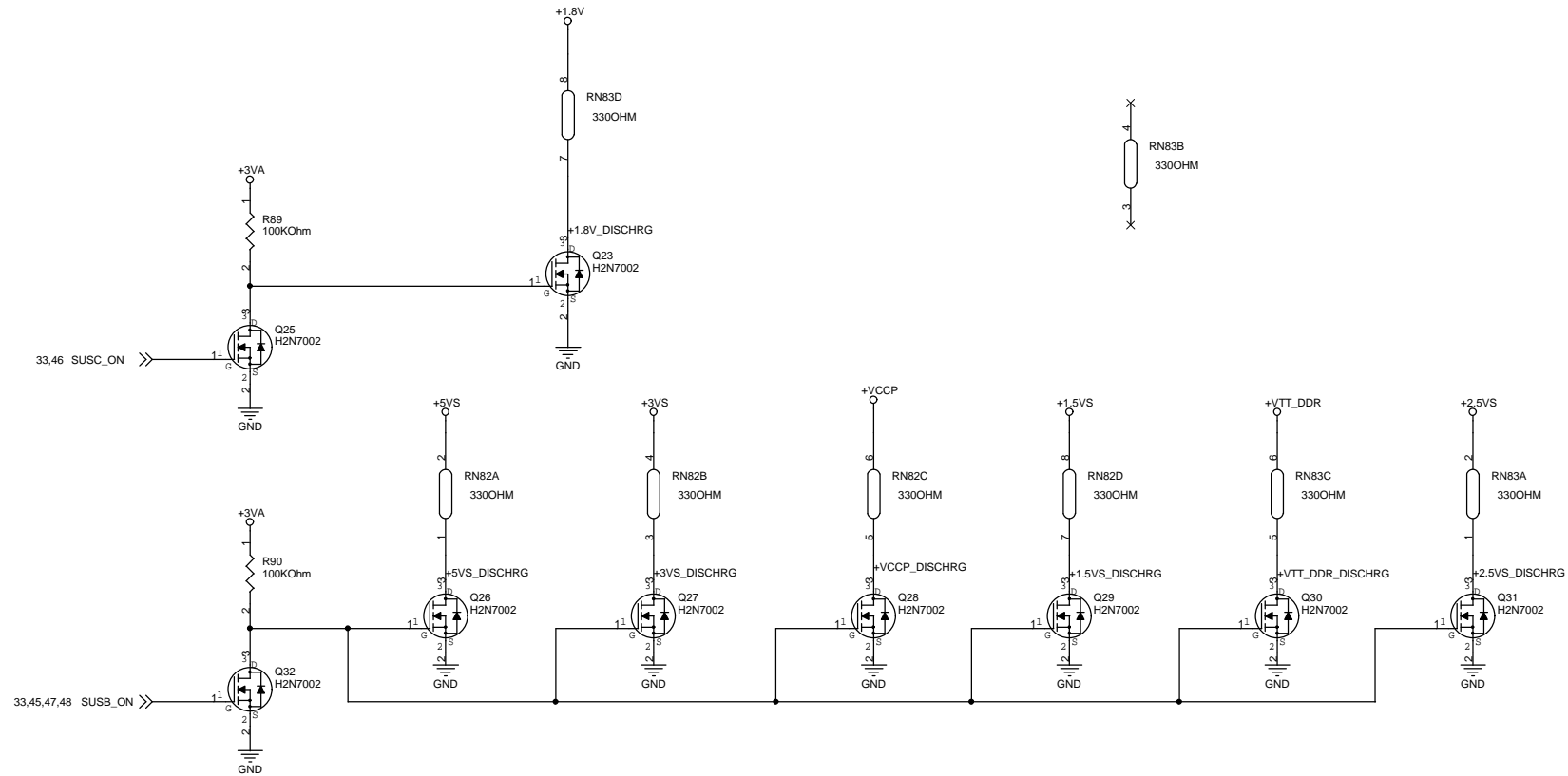


### for POWER BOTTOM LED



<Core Design>

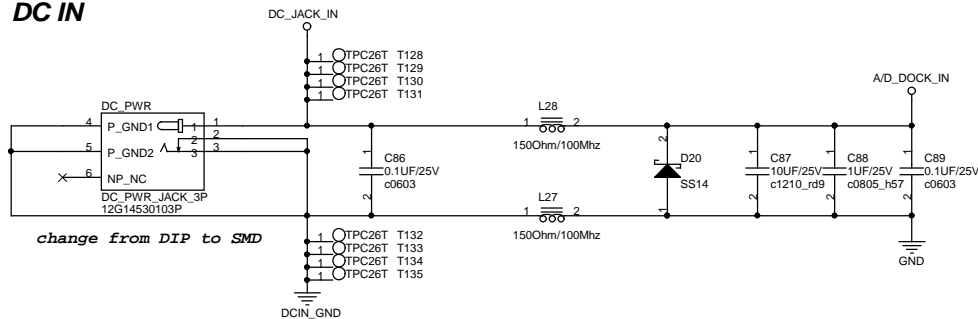
<b>ASUS</b>		<b>Title : LED</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet 38 of 52	



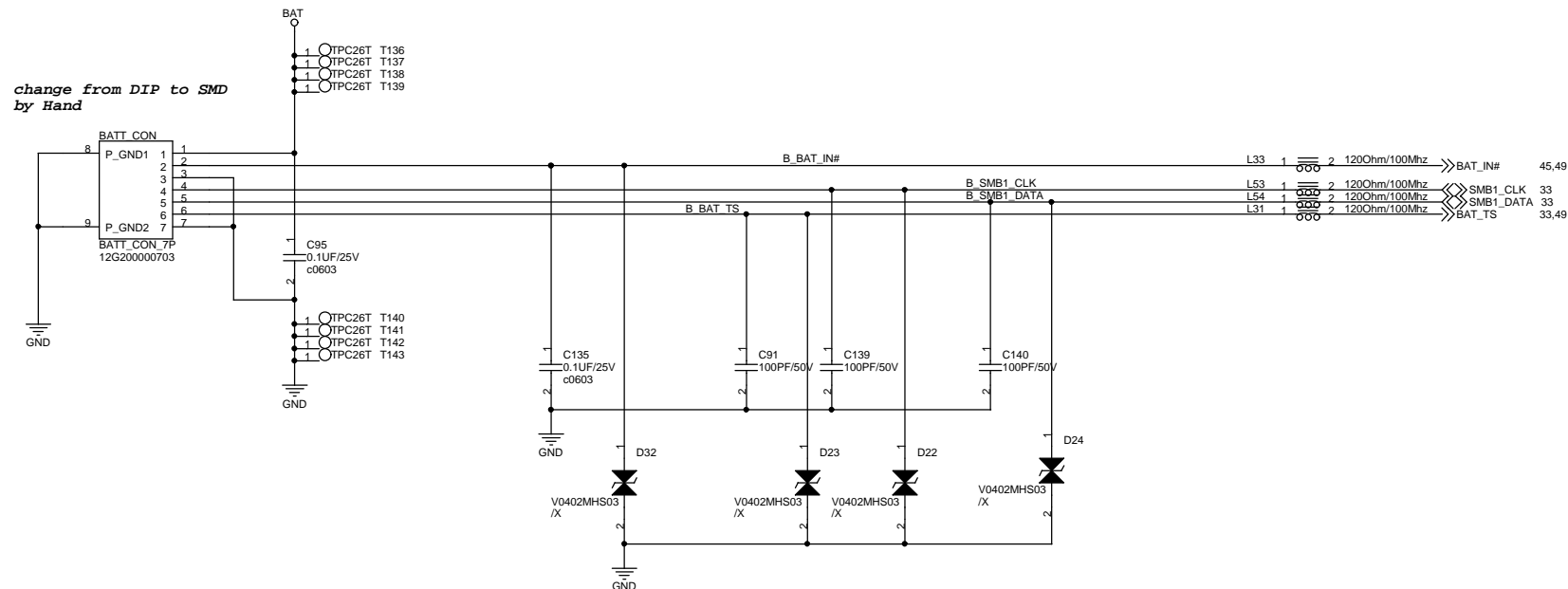
<Core Design>

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet	39 of 52

## DC IN



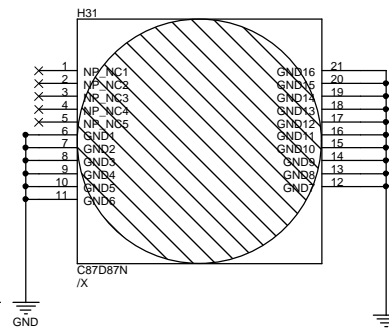
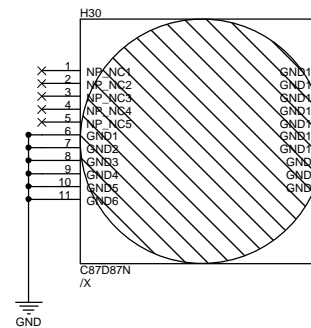
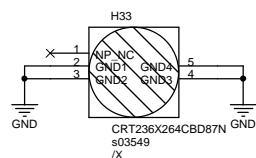
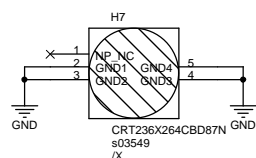
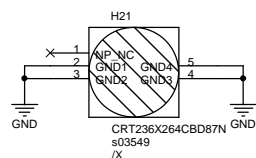
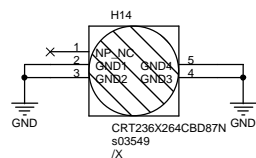
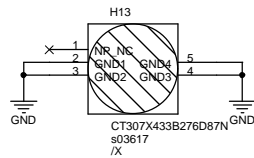
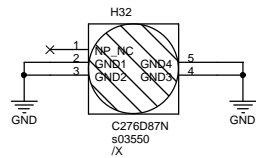
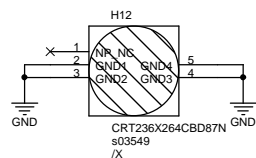
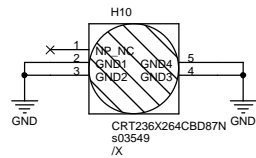
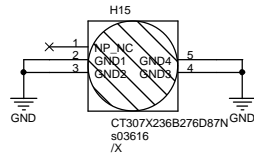
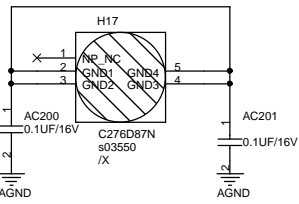
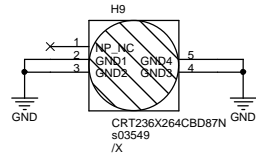
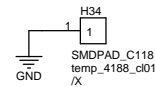
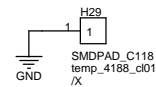
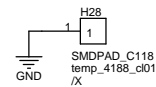
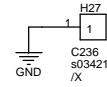
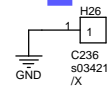
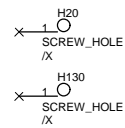
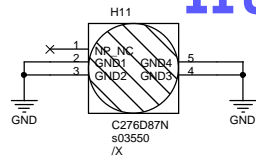
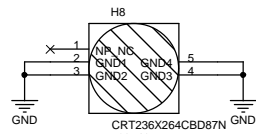
## BAT IN



<Core Design>

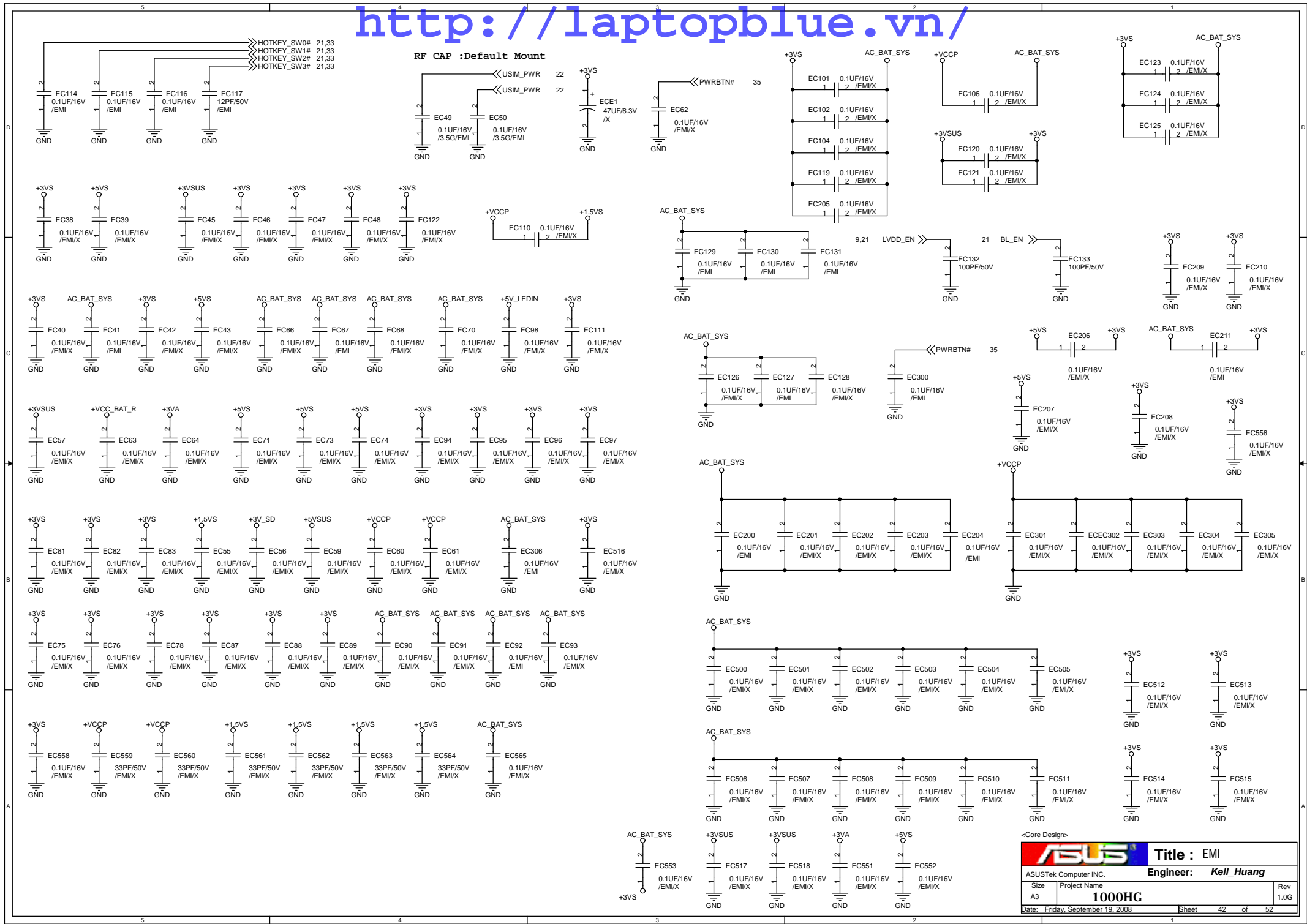
<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size	Project Name	Rev	
A3	1000HG	1.0G	
Date: Friday, September 19, 2008		Sheet	40 of 52

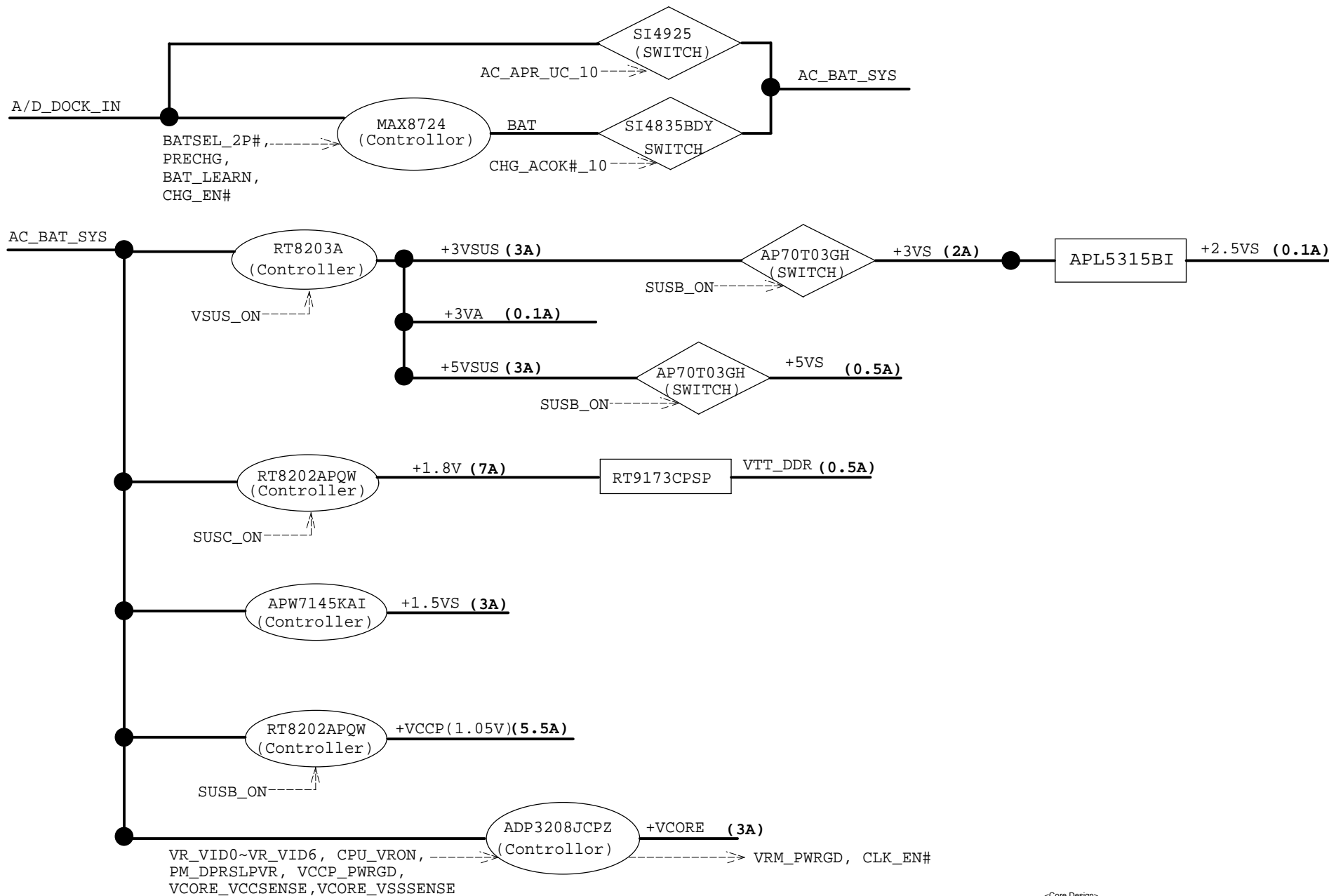




<Core Design>

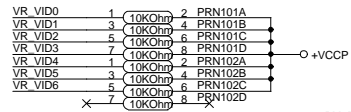
<b>ASUS</b>		<b>Title : Srew Hole</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008	Sheet 41	of 52	





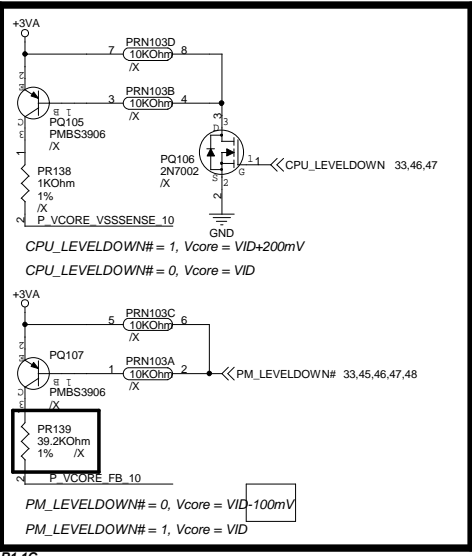
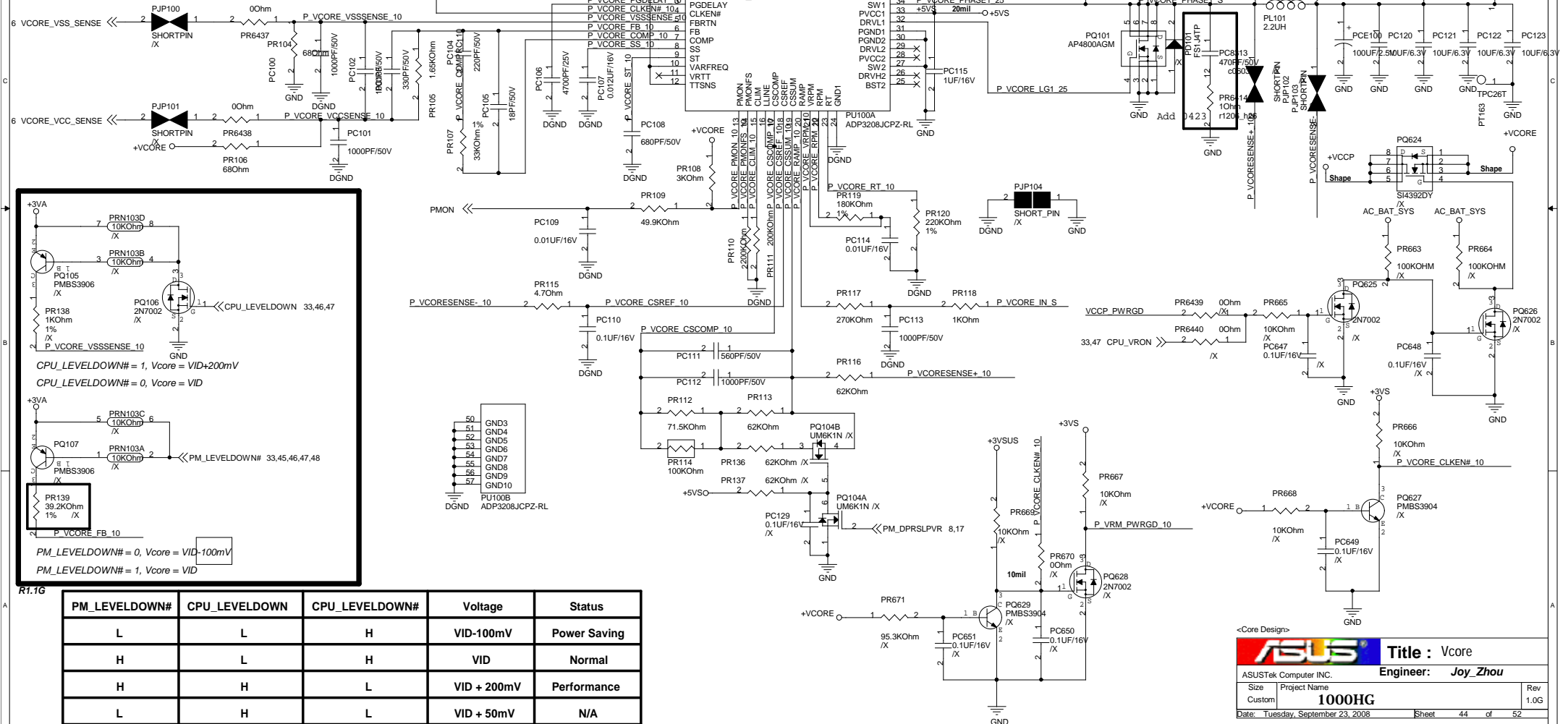
<Core Design>

		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 1000HG		Rev 1.0G
Date: Friday, September 19, 2008		Sheet	43 of 52

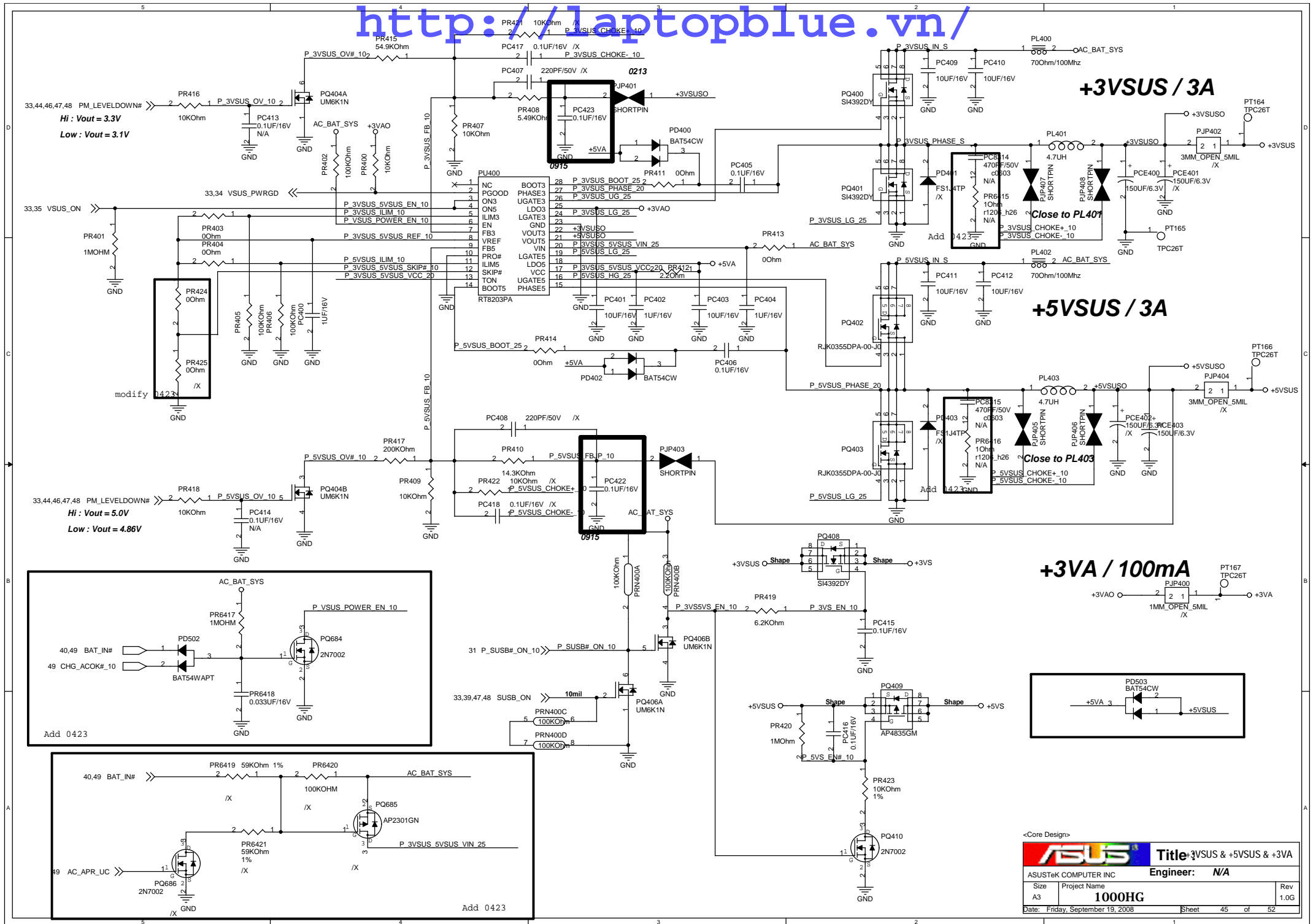


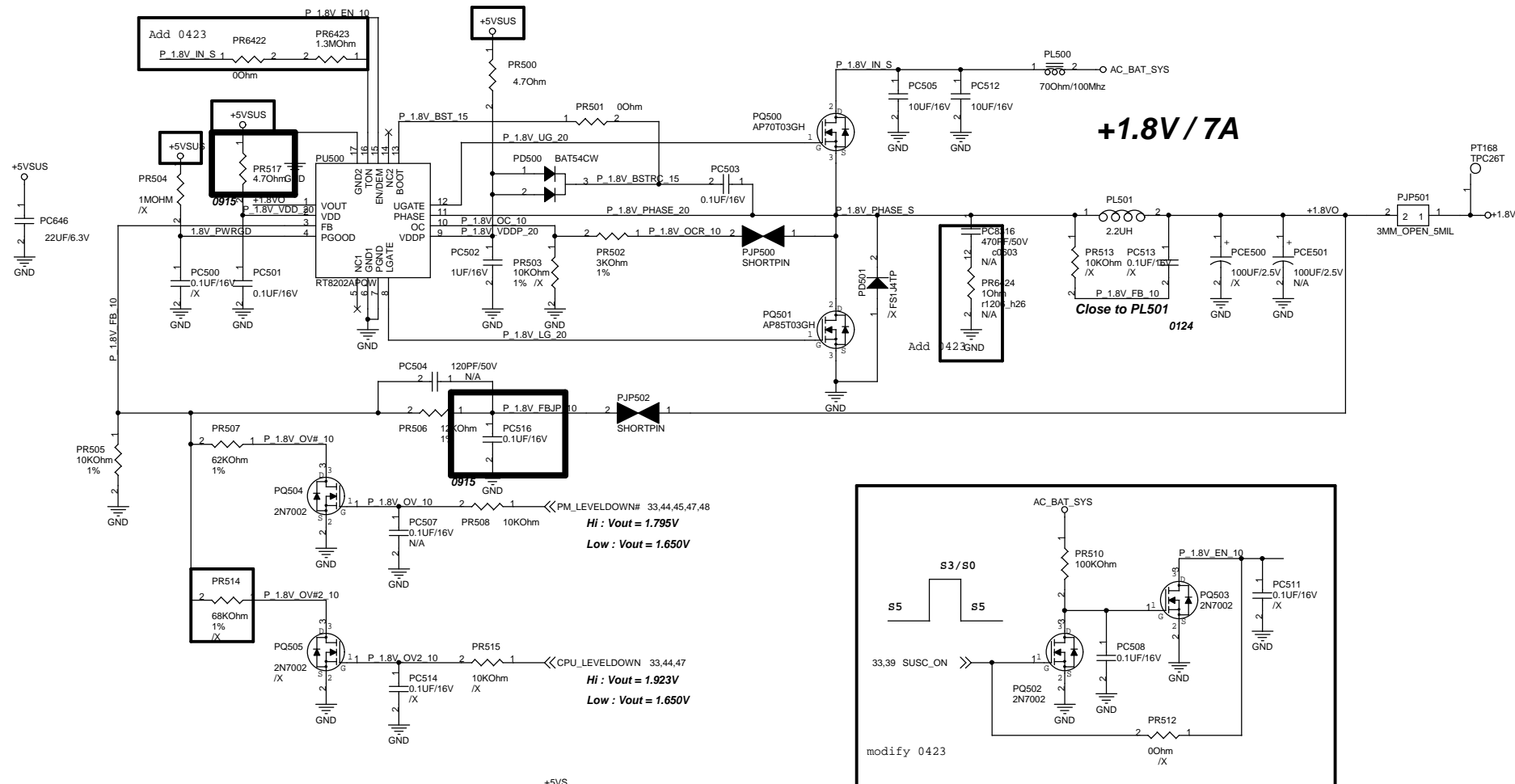
5,15 PM\_DPRSTP# >>>  
**STP\_CPU# = 0, CPU is in Deep Sleep Mode**  
 8,17 PM\_DPRSLPVR >>>  
**PM\_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled**  
 33,47 CPU\_VRON >>>  
**CPU\_VRON = 1, Vcore Regulator Enabled**  
 4,47 VCCP\_PWRGD >>>  
**VCCP\_PWRGD = 1, Vcore Regulator Enabled**  
 8,17,33 VRM\_PWRGD <<<  
**VRM\_PWRGD = 1, Vcore Power OK**

CLK\_EN# <<<  
**CLK\_EN# = 0, Clock is enabled**

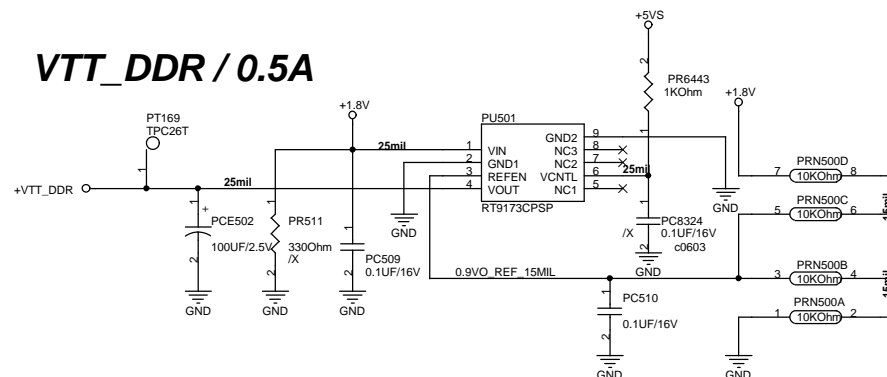


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

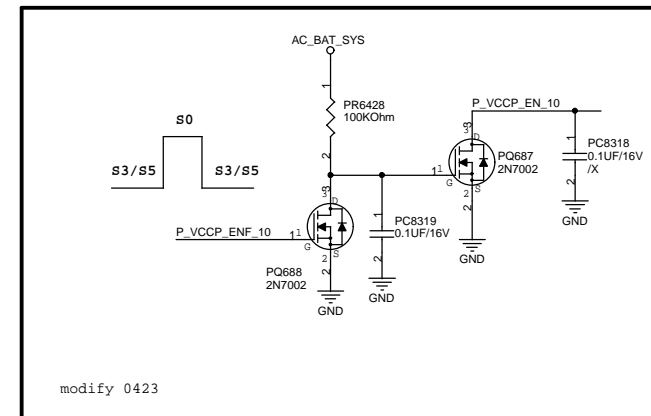
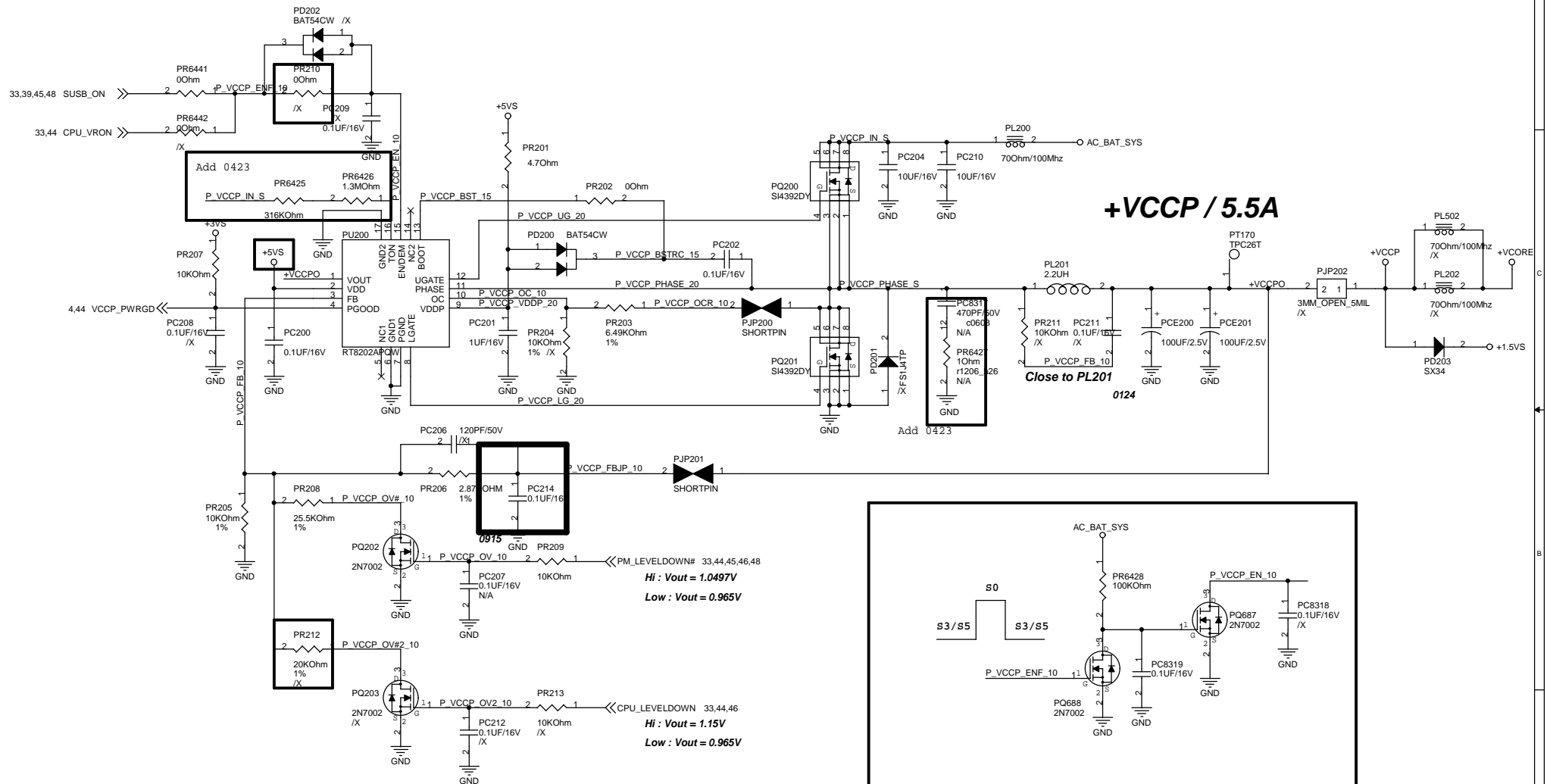




***VTT\_DDR / 0.5A***



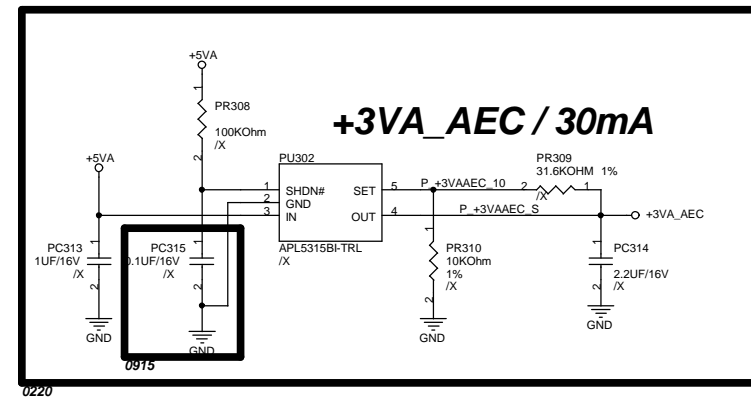
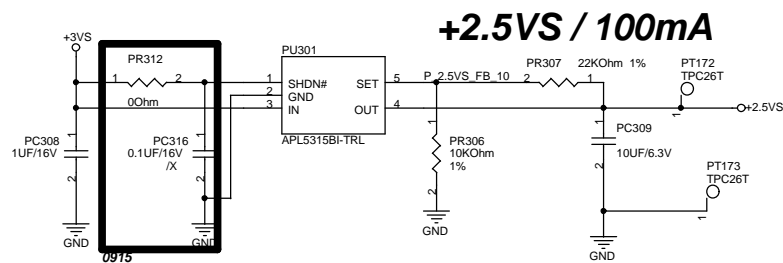
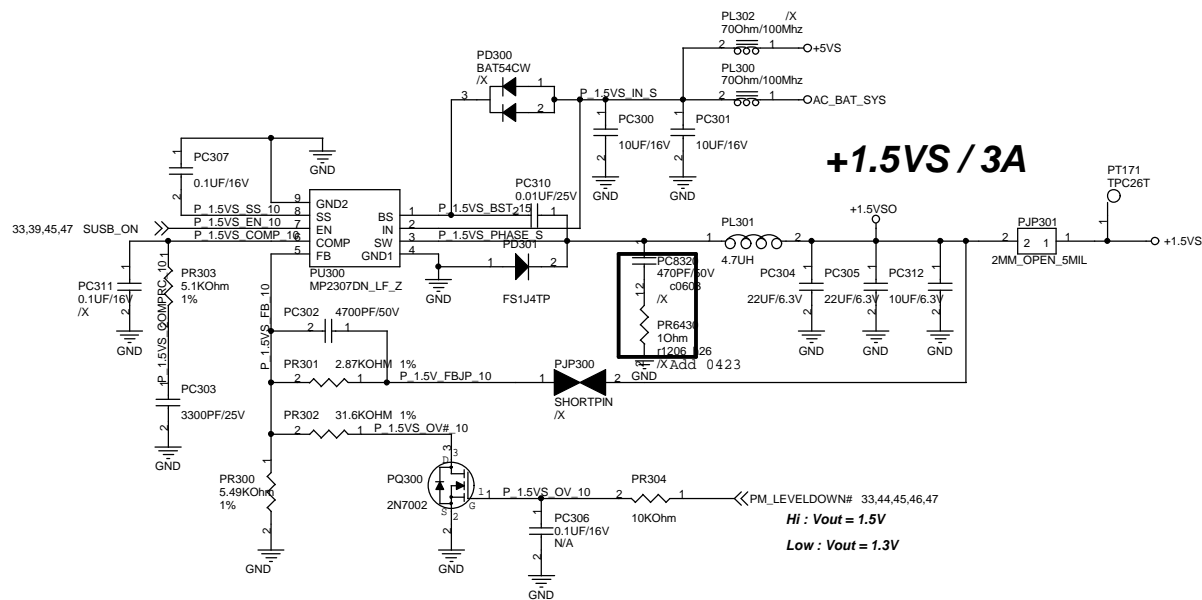
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<Core Design>

<b>ASUS</b>		<b>Title : VCCP</b>	
ASUSTek Computer INC.		Engineer: <b>Joy_Zhou</b>	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet	47 of 52



<Core Design>



<b>Charging Current :</b>		
<b>4P#</b>	<b>2P#</b>	<b>Icharge</b>
1	0	1.506A
0	1	2.502A
0	0	3.589A

<Core Design>



**Title :** Charger

ASUSTek Computer INC.

Engineer: *Joy Zhou*

Size
------

1000HG

Sheet 49 of 52

Date: Fri

## EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

## EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Core Design>

		<b>Title :</b> EC Pin Define	
ASUSTek Computer INC.		<b>Engineer:</b> Satan He	
Size A3	Project Name <b>1000HG</b>	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet	50 of 52

From 1000 2008.3.21.0100 circuit

1.Remove IDE3 CONN

2.Add SATA HDD1 conn

1000H Power 載腔踢璃:

part reference	埠腔踢?	政妻腔踢?
PD301	07G004072020	07G004019410

咳靖腔踢璃:

part reference	part number	component name
PQ624	07G005360110	N-MOSFET SI4392DY-T1-E3 SO-8
PR664	10G212100314050	RES 100K OHM 1/16W (0402) 1%
PQ626	07G005000730	N-MOSFET 2N7002-7-F SOT-23
PR663	10G212100314050	RES 100K OHM 1/16W (0402) 1%
PC648	11G233110411030	MLCC 0.1UF/16V (0603)X7R 10%
PQ625	07G005000730	N-MOSFET 2N7002-7-F SOT-23
PC647	11G233110411030	MLCC 0.1UF/16V (0603)X7R 10%
PR665	10G212100214010	RES 10K OHM 1/16W(0402)1%
PR666	10G212100214010	RES 10K OHM 1/16W(0402)1%
PQ627	07G003000120	TRASIS. PMBS3904 SOT-23
PC649	11G232110411320	MLCC 0.1UF/16V (0402) X7R 10%
PR668	10G212100214010	RES 10K OHM 1/16W(0402)1%
PR667	10G212100214010	RES 10K OHM 1/16W(0402)1%
PQ628	07G005000730	N-MOSFET 2N7002-7-F SOT-23
PC650	11G232110411320	MLCC 0.1UF/16V (0402) X7R 10%
PR670	10G212000004030	RES 0 OHM 1/16W(0402)JUMP
PR669	10G212100214010	RES 10K OHM 1/16W(0402)1%
PQ629	07G003000120	TRASIS. PMBS3904 SOT-23
PC651	11G232110411320	MLCC 0.1UF/16V (0402) X7R 10%
PR671	10G212100214010	RES 10K OHM 1/16W(0402)1%

<Core Design>

		Title : History	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size A3	Project Name 1000HG	Rev 1.0G	
Date: Friday, September 19, 2008		Sheet	51 of 52

http://laptopblue.vn/

From 1000 2008\_0412\_1600 circuit

For costdown

Change C315, C316 from "/DTV\_/GPS" to "/WIMAX"  
Change WR44 } WR28 } WR29 } WR34 } WR35 } WR37 } WR39 from "/DTV\_/GPS" to "/WIMAX"  
Change WR25 } WR26 from "/3.5G" to "/3.5G/WIMAX"  
Change WR43 from "/3.5G" to "/3.5G/WIMAX/GPS"  
For 3.5G/WIMAX: 0ohm  
For GPS: 100Kohm  
Change EC6 from "/3.5G" to "/3.5G/X"  
Change WR33 from "/DTV\_/GPS" to "/GPS/WIMAX"  
Change WR27 from "/DTV\_/GPS" to "/WIMAX/X"  
Change WR30 from "/3.5G" to "/3.5G/X"  
Change AC202 } AC203 from "/3.5G" to "/3.5G/X"  
Change AC207 } AR102 } AR101 } AC206 } AC209 from "/3.5G" to "/3.5G/X"

For Power change


1, PR413 change to 0 ohm, PN: 10G213000003030.  
2, PC504 change to N/A.  
3, PCE403 change to 150uF, PN: 11G08D415750 ↗ N/A.  
4, PCE500 change to /X, PCE501 change to N/A.  
5 ↗ PR412 change to 2.2ohm ↗ 10G2132R2003010 (   
6 ↗ PR1111 ↗ PR1112 ↗ PR1113 change to 100K ohm ↗ 10G212104004030  
  
7 ↗ Change PR423 from 68K to 10K (10G212100214010).  
8 ↗ Set PC414, PC413, PC507, PC207, PC306 Stuff.  
9 ↗ Set OL1 stuff (   
10 ↗ Set PR308, PC313, PU302, PR309, PR310, PC314 not stuff  
11 ↗ Change PR207 from 1M to 10K (10G212103004010).  
12 ↗ Change PR400 from 1M to 10K (10G212103004010).

13 ↗ PC108 change to 680PF/50V ↗ 11G232168114030

For Ea audio MIC test

AL24 from 120OHM BEED change to 0ohm

<Core Design>

		Title : History	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name		Rev
A3	1000HG		1.0G
Date: Friday, September 19, 2008		Sheet	52 of 52