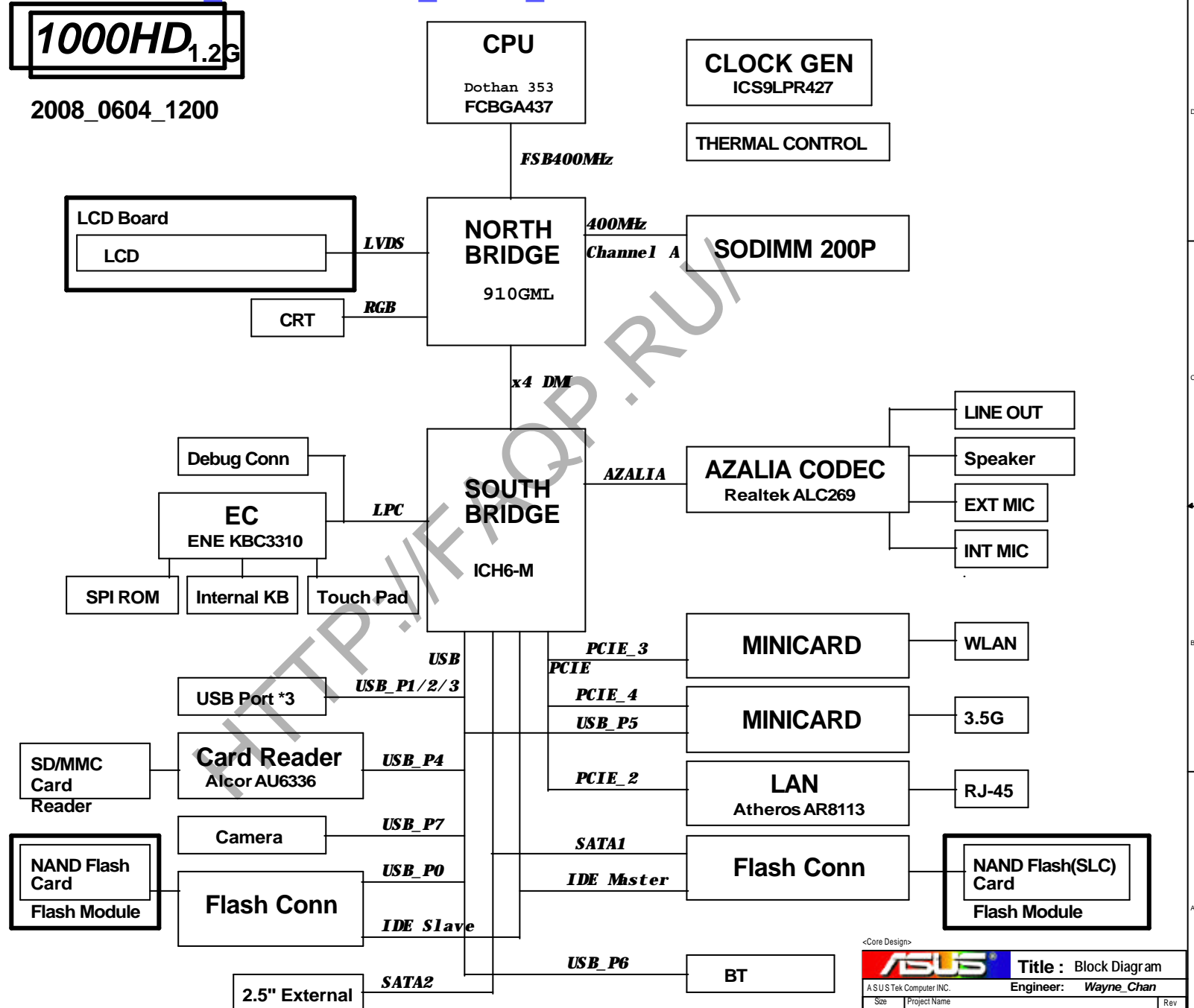


01\_Block Diagram  
02\_System Setting  
03\_Power Sequence  
04\_EC Pin Define  
05\_History  
06\_\*  
07\_Clock Gen\_ICS9LPR427  
08\_Dothan\_HOST  
09\_Dothan\_PWR\_GND  
10\_NB-910GML\_HOST\_DMI  
11\_NB-910GML\_DRAM  
12\_NB-910GML\_VGA\_LVDS\_TV  
13\_NB-910GML\_PWR  
14\_NB-910GML\_GND  
15\_SB-ICH6-M\_Azalia\_GPIO\_PCI\_LAN  
16\_SB-ICH6-M\_USB\_PCIE\_DMI\_IDE\_SATA  
17\_SB-ICH6-M\_PWR\_GND  
18\_DDR2 SODIMM  
19\_DDR2 Termination  
20\_Onboard VGA  
21\_LCD Conn\_LID  
22\_PCIEx 3.5G & Ext. Antenna  
23\_Mini WIFI+ BT  
24\_LAN\_Atheros AR8113  
25\_MDC\_RJ45  
26\_Flash Conn  
27\_SATA HDD  
28\_USB Port  
29\_Camera Power  
30\_Card Reader\_AU6336C52  
31\_Codec\_ALC269  
32\_Audio\_AMP\_Jack  
33\_EC\_ENE KB3310  
34\_EC\_UART controller  
35\_Switch\_SPI ROM\_Debug Conn  
36\_Thermal Sensor\_FAN  
37\_KB\_Touch Pad  
38\_LED  
39\_Discharge  
40\_PWR Jack  
41\_Srew Hole  
42\_EMI  
43\_POWER FLOW  
44\_Vcore  
45\_Power System  
46\_Power\_+1.8V & VTTDDR  
47\_Power\_VCCP  
48\_Power\_+1.5VS & +2.5VS  
49\_Power\_Charger



EEE PC 1000HD PCB version

GPI29	GPI31	PCB version
0	0	1.0G
0	1	
1	0	
1	1	

USB

USB0	Flash Conn
USB1	USB Conn
USB2	USB Conn
USB3	USB Conn
USB4	Card Reader
USB5	Minicard
USB6	BT
USB7	Camera


PCIE

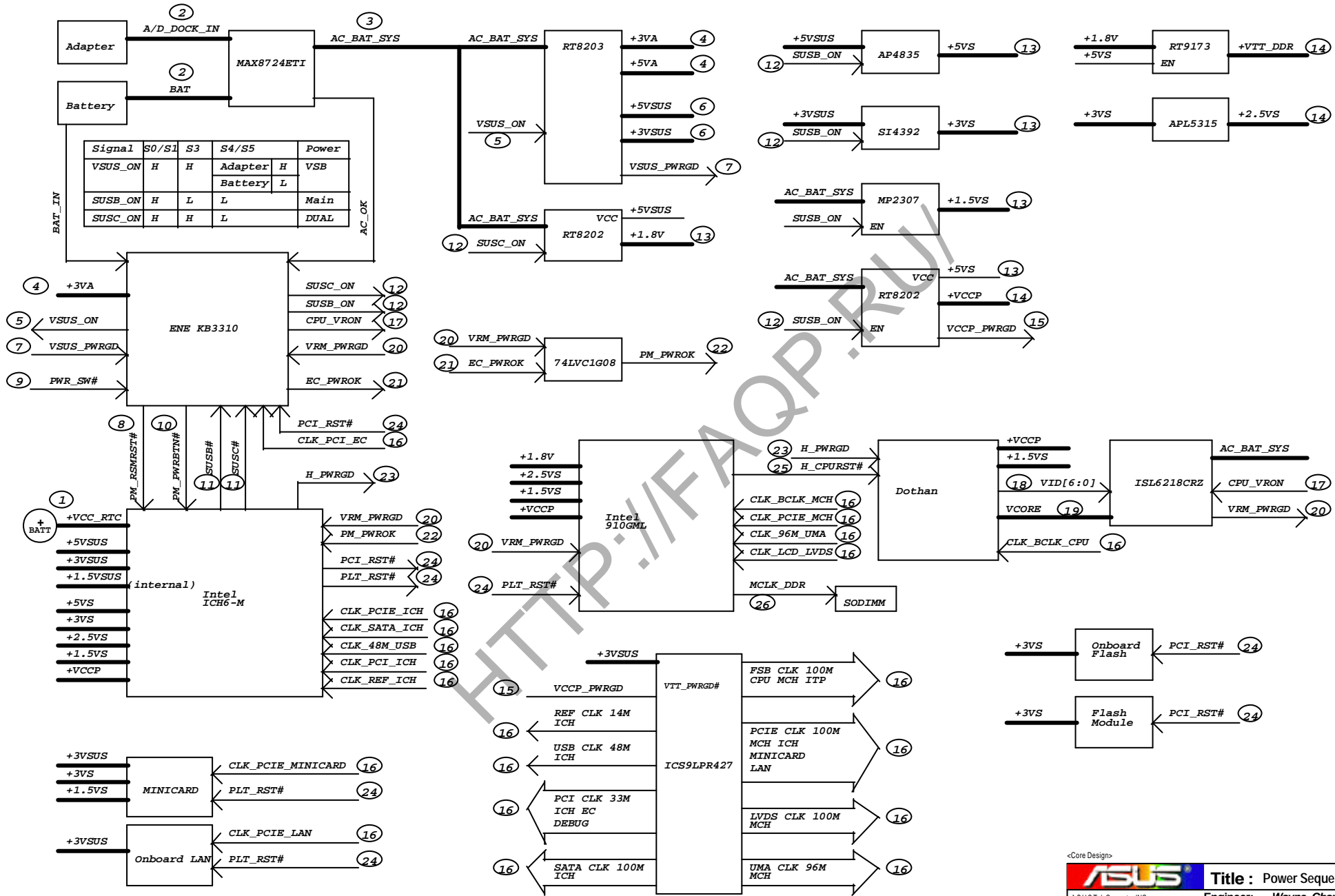
PCIE1	NC
PCIE2	LAN
PCIE3	Minicard
PCIE4	Minicard

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Core Design>

		Title : System Setting	
ASUS Tek Computer INC.		Engineer: Wayne_Chan	
Size A3	Project Name 1000HD	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 2 of 49	



## EC KB3310 GPIO SETTING


Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pullhigh
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Internal pullhigh
15	GPIO08	EXTSM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	LidOff, 1-LidOn. Internal Pull Up
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	HOTKEY_SW2#	I	Internal pullhigh
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL_4P#	I	battery charging current setting
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debugport
31	GPIO17/E51_RX	E51_RX	I	RS232 debugport
32	GPIO18	PWR_SW#	I	power button, intel mp4p
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	CHG_LED_GREEN#	O	Green LED for charging
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_FLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pullhigh
56	GPIO31/KSI1	KSI1	I	Internal pullhigh
57	GPIO32/KSI2	KSI2	I	Internal pullhigh
58	GPIO33/KSI3	KSI3	I	Internal pullhigh
59	GPIO34/KSI4	KSI4	I	Internal pullhigh
60	GPIO35/KSI5	KSI5	I	Internal pullhigh
61	GPIO36/KSI6	KSI6	I	Internal pullhigh
62	GPIO37/KSI7	KSI7	I	Internal pullhigh
63	GPIO38/AD0	BAT_I_CHG	I	
64	GPIO39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

## EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery LowLow
73	GPIO40	AC_OK	I	AC Adaptor PlugIn
74	GPIO41	EC_RSMRST#	O	10K pull down to GND
75	GP42	BAT_IN	I	
76	GP43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	NC	I	for KB type detection
82	GPIO49/KSO17	NC	I	for KB type detection
83	GPIO4A/PSCLK1	NC	O	LCD_SCL
84	GPIO4B/PSDAT1	NC	O	LCD_SDA
85	GPIO4C/PSCLK2	NC	O	LCD_CSB
86	GPIO4D/PSDAT2	NC	O	LCD_VSYNC
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLD	SCRL_LED#	O	
95	GPIO56	HOTKEY_SW3#	I	Internal pullhigh
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	EC_PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P, 3P
110	GPXID1	CPU_LEVELDOWN#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SUSB#	I	100K pull down to GND
115	GPXID4	PM_SUSCH#	I	100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	VSUS_PWRGD	I	
118	GPXID7	BATSEL_LIFe	O	
121	GPIO57	INTERNET#	I	Internal pullhigh
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	Internal pullhigh

<Core Design>

		<b>Title : EC Pin Define</b>	
ASUS Tek Computer INC.		Engineer: Wayne Chan	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 4 of 49	

## 1.0G From 1000H 2008.3.31.2030 circuit

- 1.Change CPU to Dothan
- 2.Change NB to 910GML
- 3.Change SB to ICH6-M
- 4.VCORE control change to ISL6218CRZ

### 1.1G


- 1.Change Project name to 1000D
- 2.Support LiFe Battery
- 3.Add speaker connect

### 1.2G

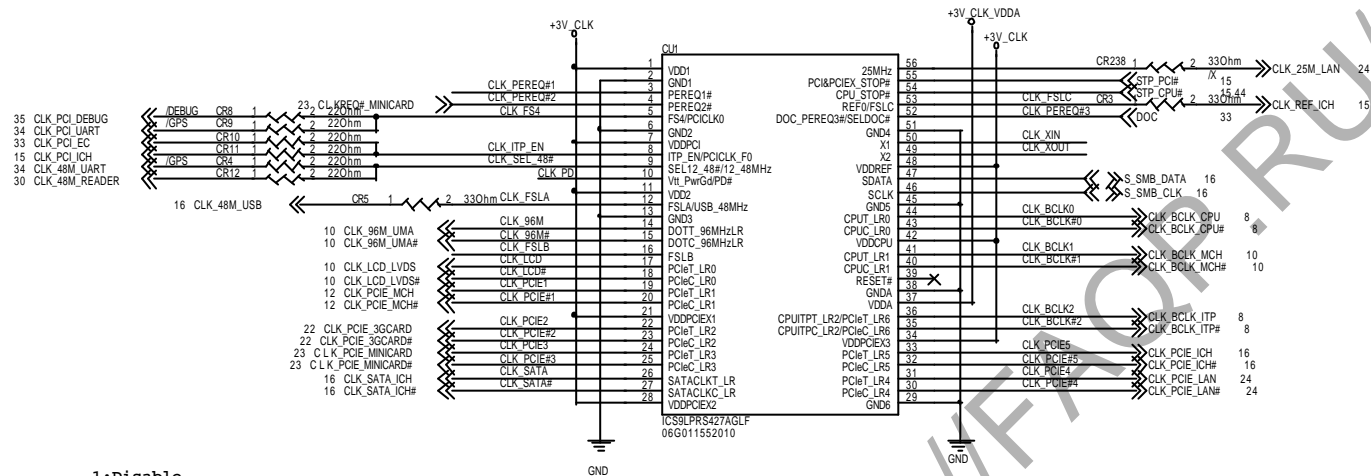
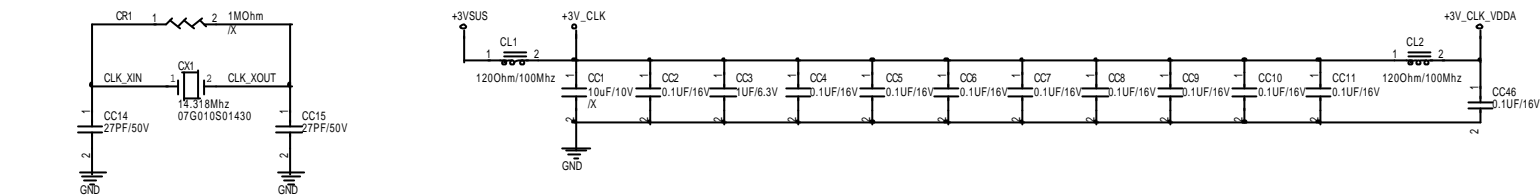
- 1.Change Project name to 1000HD
- 2.Modify page 45.
- 3.Add and reserved CE1 CE5 CE6 for USB port
- 4.Modify schematic of LED
- 5.Remove Capacitor of Microphone from clock and data signal
- 6.Add page33 Hotkey de-bounced related schematic
- 7.Add page23 PERST#pull down 1M ohm

HTTP://FAQP.RU/

<Core Design>

		Title : History	
ASUS Tek Computer INC.		Engineer: Wayne Chan	
Size A3	Project Name 1000HD	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 5 of 49	

[HTTP://FAQP.RU/](http://FAQP.RU/)



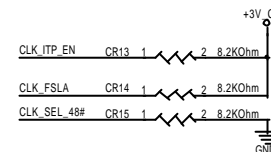
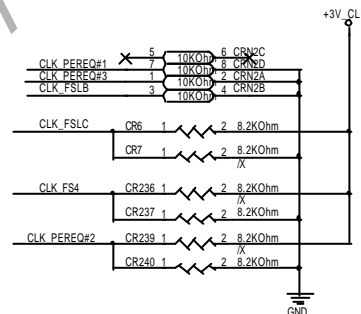
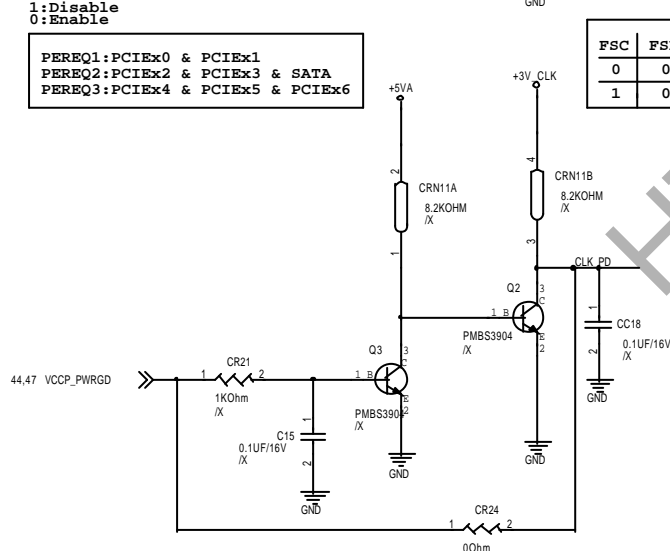
S_SMB_DATA	CC12	2	1	10PF/50V
S_SMB_CLK	CC13	2	1	10PF/50V

CLK_PCI_ICH	CC36	2	1	10PF/50V
CLK_PCI_EC	CC37	2	1	10PF/50V
CLK_PCI_DEBUG	CC38	2	1	10PF/50V
CLK_REF_ICH	CC39	2	1	10PF/50V
CLK_48M_USB	CC40	2	1	10PF/50V
CLK_48M_UART	CC41	2	1	10PF/50V
CLK_PCI_UART	CC42	2	1	10PF/50V
CLK_48M_READER	CC45	2	1	10PF/50V

1:Disable  
0:Enable

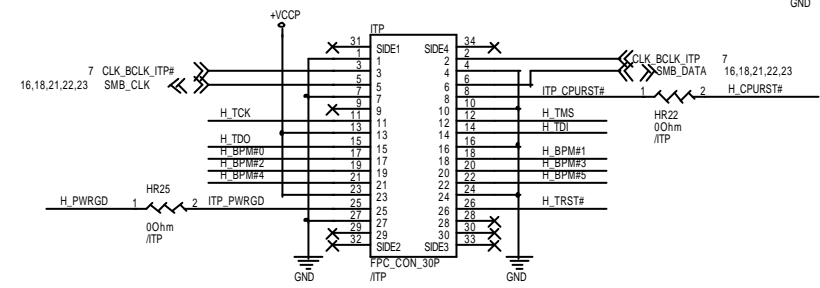
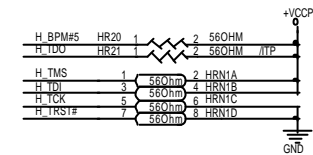
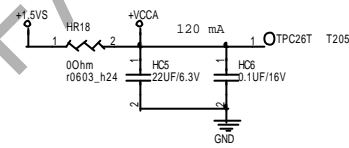
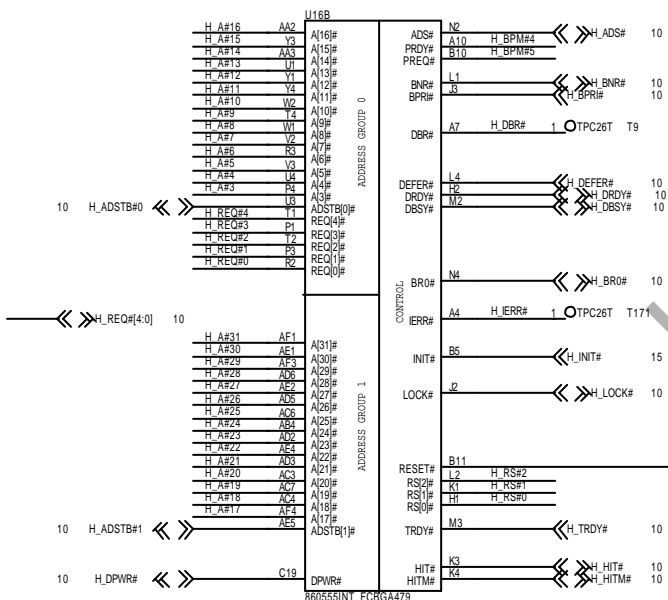
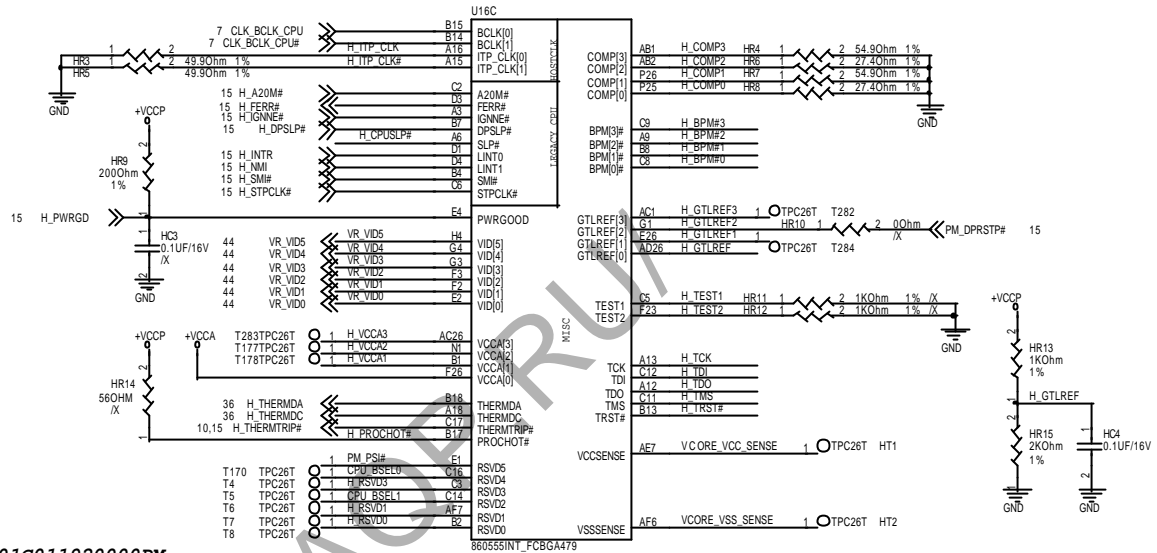
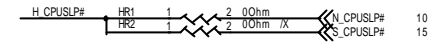
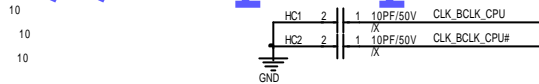
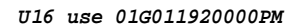
PEREQ1:PCIEx0 & PCIEx1  
PEREQ2:PCIEx2 & PCIEx3 & SATA  
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100

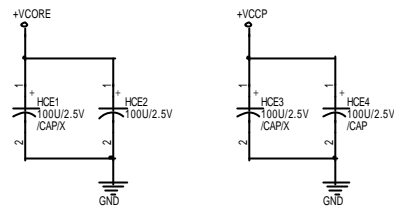
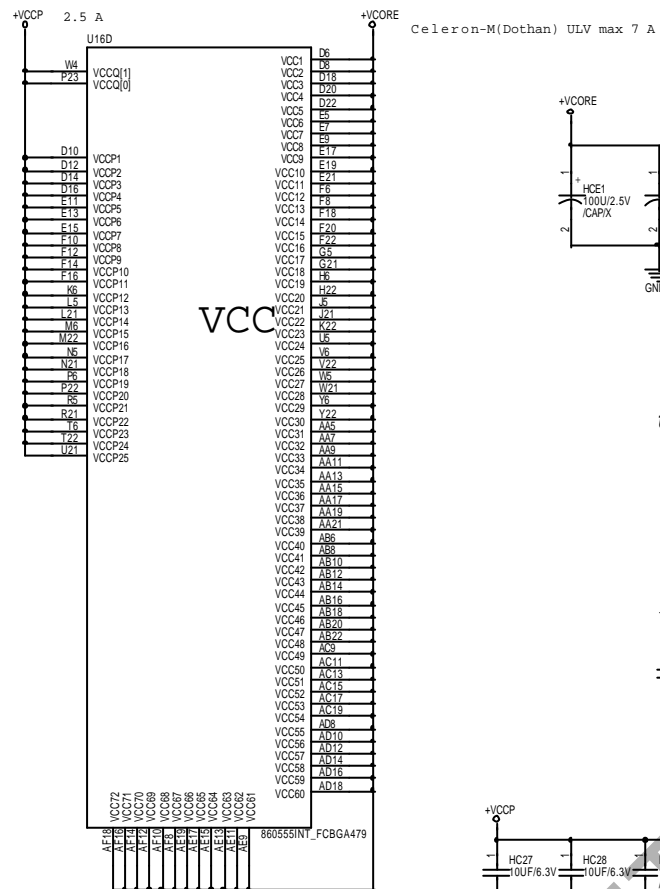


<Core Design>

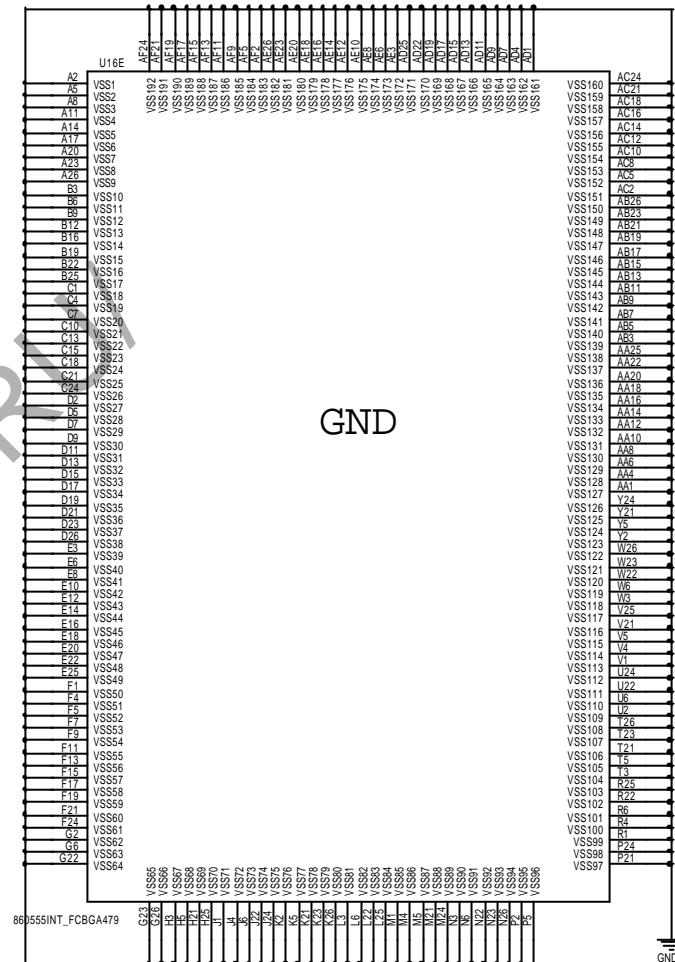
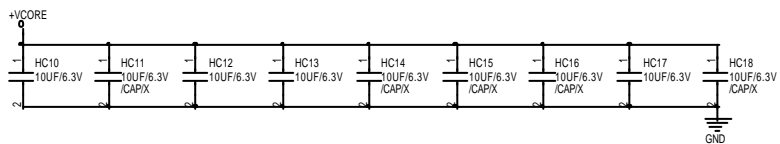
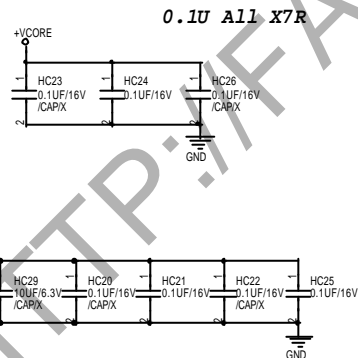
<b>ASUS</b>		<b>Title : C10 ck Gen_ICS9LPRS427</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 7 of 49	

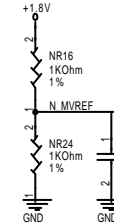
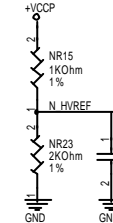
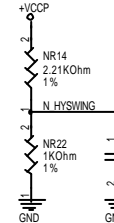
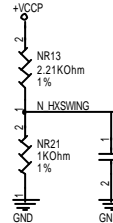
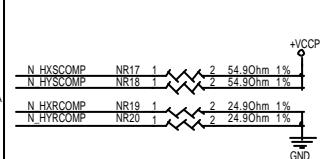
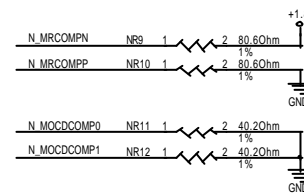
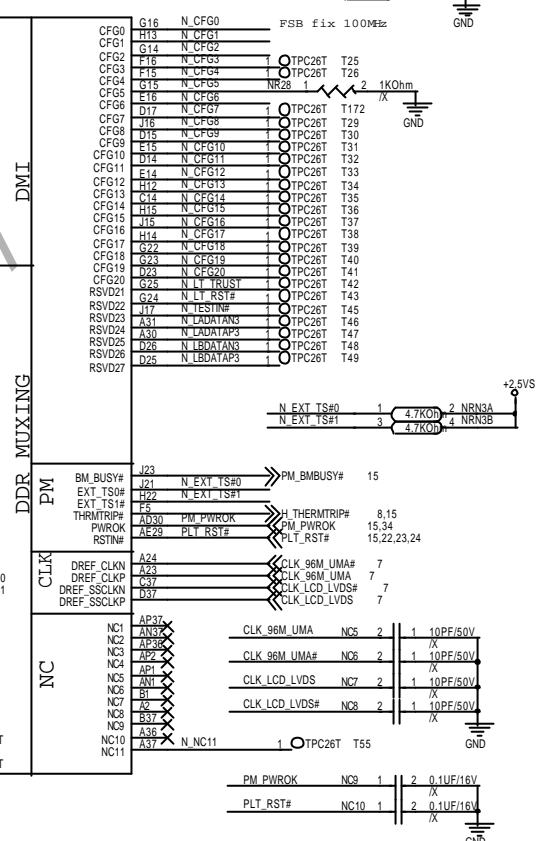
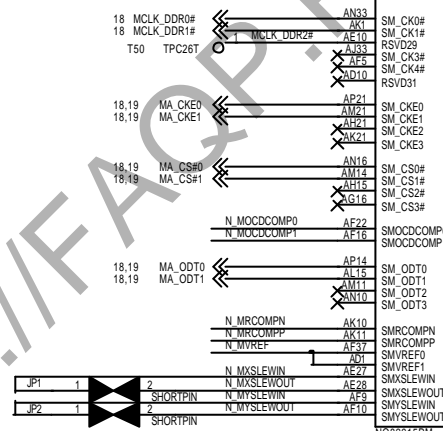
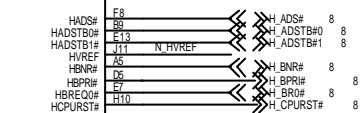
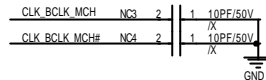
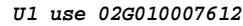
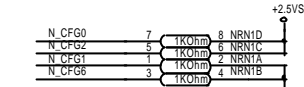


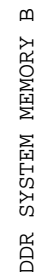




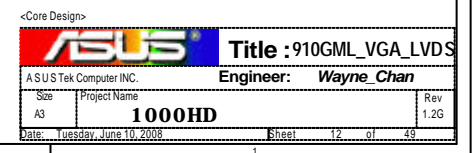
U16 use 01G011920000PM

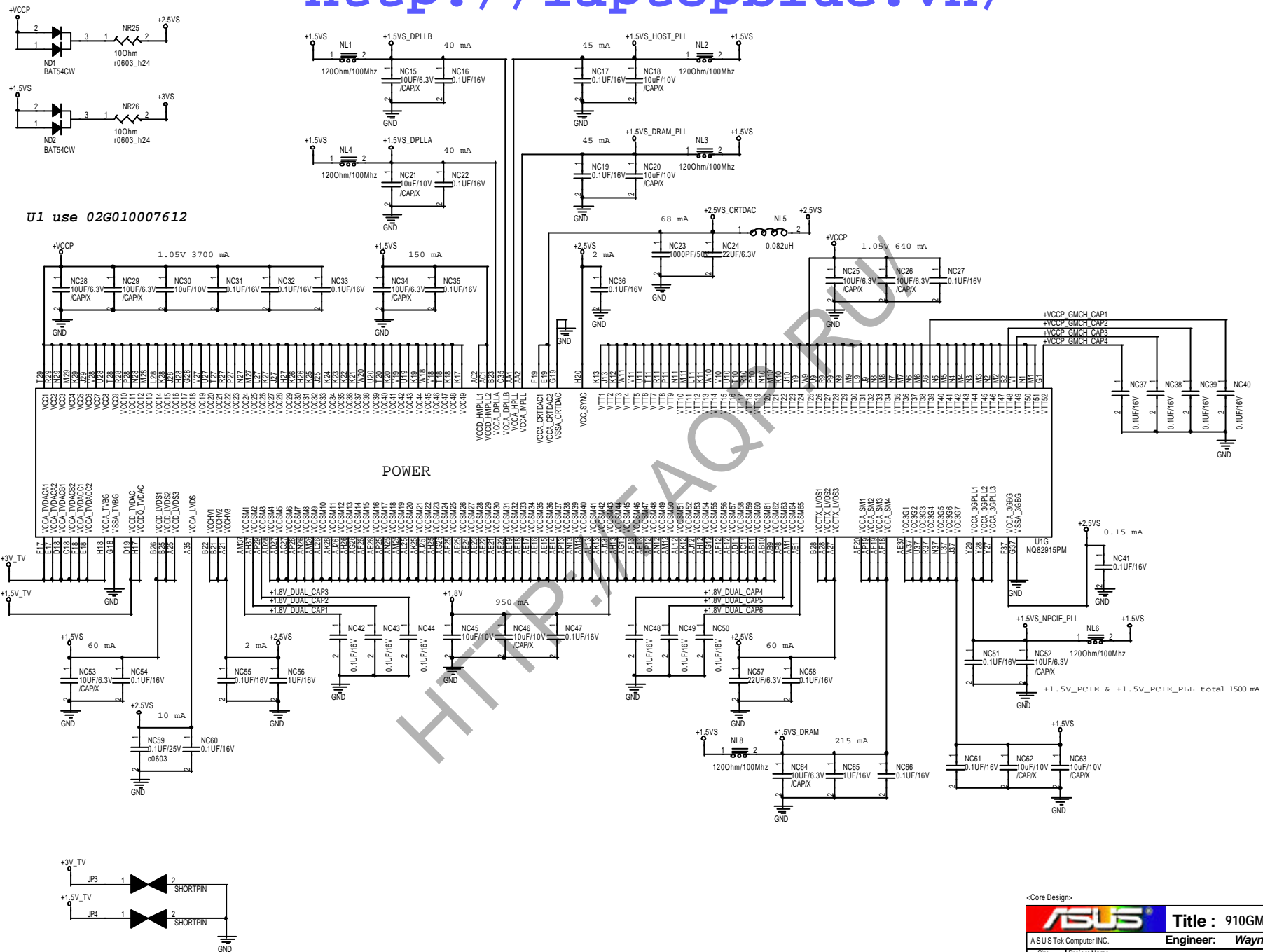


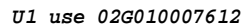




PCI-E signals can be left NC, If unused.

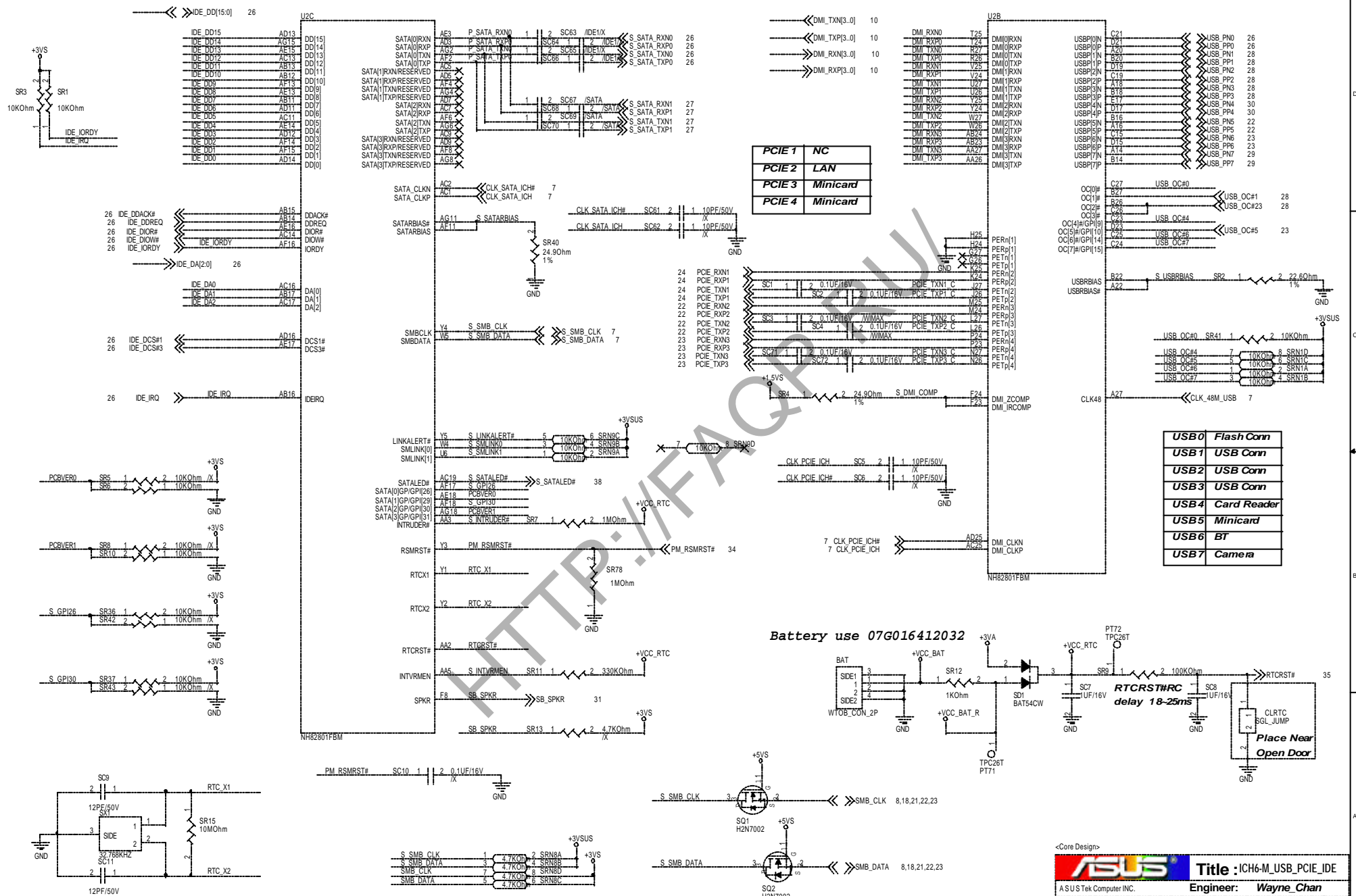




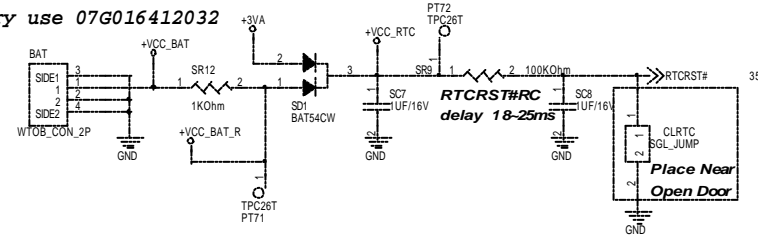








Battery use 07G016412032



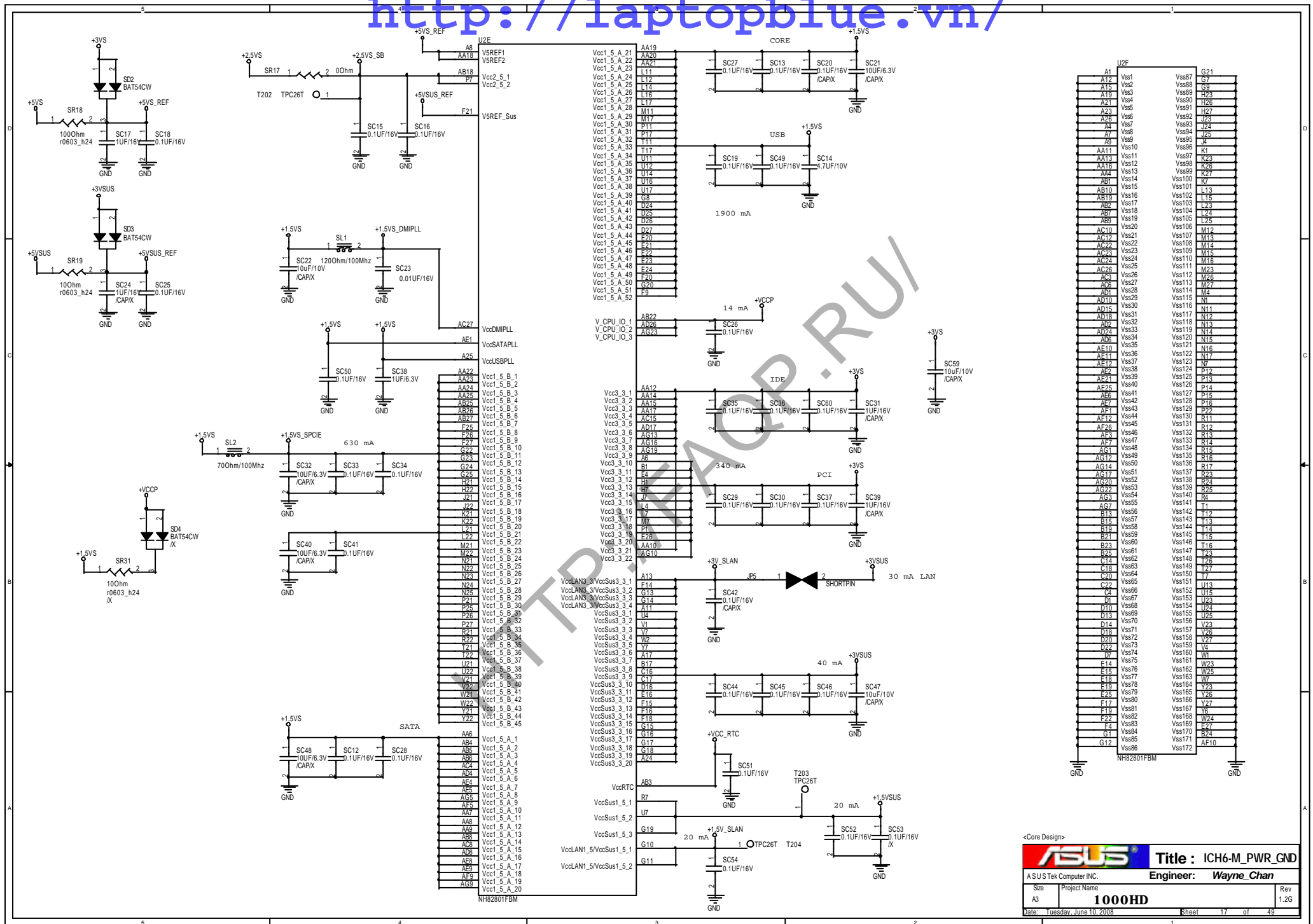
&lt;Core Design&gt;

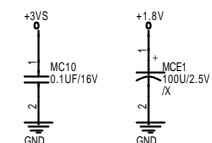
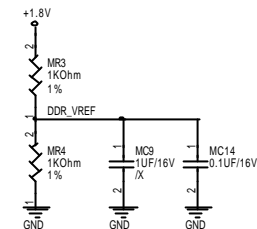
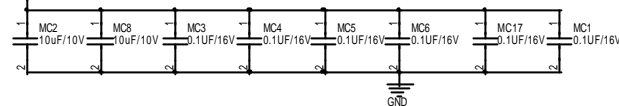
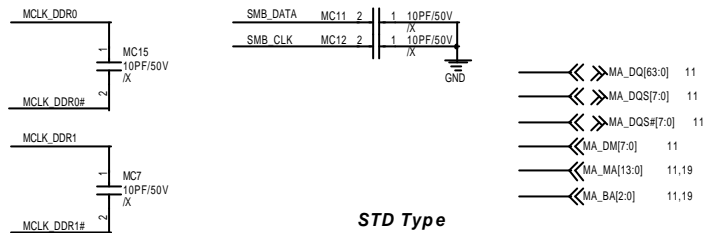


Title : ICH6-M\_USB\_PCIE\_IDE

ASUSTek Computer INC.		Engineer: <u>Wayne Chan</u>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: <u>Tuesday, June 10, 2008</u>		Sheet <u>16</u> of <u>49</u>	



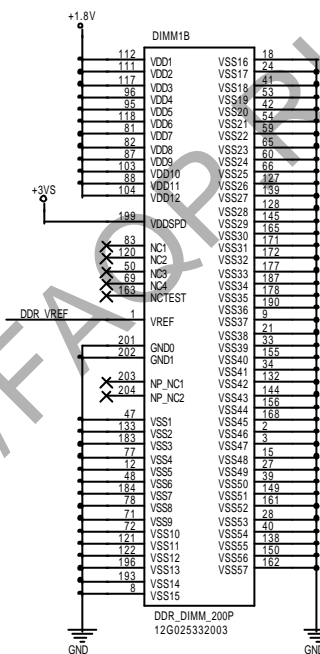




DIMM1A			DIMM1B		
MA_MA0	102	A0	MA_DQ0	5	MA_DQ0
MA_MA1	101	A1	MA_DQ1	7	MA_DQ1
MA_MA2	100	A2	MA_DQ2	17	MA_DQ2
MA_MA3	99	A3	MA_DQ3	19	MA_DQ3
MA_MA4	98	A4	MA_DQ4	4	MA_DQ4
MA_MA5	97	A5	MA_DQ5	6	MA_DQ5
MA_MA6	94	A6	MA_DQ6	14	MA_DQ6
MA_MA7	92	A7	MA_DQ7	16	MA_DQ7
MA_MA8	91	A8	MA_DQ8	23	MA_DQ8
MA_MA9	81	A9	MA_DQ9	25	MA_DQ9
MA_MA10	105	A10AP	MA_DQ10	35	MA_DQ10
MA_MA11	90	A11	MA_DQ11	37	MA_DQ11
MA_MA12	89	A12	MA_DQ12	20	MA_DQ12
MA_MA13	116	A13	MA_DQ13	22	MA_DQ13
MA_BA2	86	A14	MA_DQ14	36	MA_DQ14
MA_BA1	84	A15	MA_DQ15	38	MA_DQ15
MA_BA0	107	BA0	MA_DQ16	43	MA_DQ16
MA_BA1	106	BA1	MA_DQ17	45	MA_DQ17
MA_CS#0	110	S#0	MA_DQ18	56	MA_DQ18
MA_CS#1	115	S#1	MA_DQ19	57	MA_DQ19
MCLK_DDR0	30	CK0	MA_DQ20	44	MA_DQ20
MCLK_DDR0#	164	CK0#	MA_DQ21	46	MA_DQ21
MCLK_DDR1	166	CK1	MA_DQ22	58	MA_DQ22
MCLK_DDR1#	79	CK1#	MA_DQ23	61	MA_DQ23
MA_CKE0	80	CKE0	MA_DQ24	63	MA_DQ24
MA_CKE1	113	CKE1	MA_DQ25	61	MA_DQ25
MA_CAS#	108	CAS#	MA_DQ26	73	MA_DQ26
MA_RAS#	109	RAS#	MA_DQ27	75	MA_DQ27
MA_WE#	139	WE#	MA_DQ28	62	MA_DQ28
SMB_CLK	200	SA0	MA_DQ29	64	MA_DQ29
SMB_DATA	197	SA1	MA_DQ30	74	MA_DQ30
MA_ODT0	114	ODT0	MA_DQ31	76	MA_DQ31
MA_ODT1	119	ODT1	MA_DQ32	123	MA_DQ32
MA_DM0	10	DM0	MA_DQ33	125	MA_DQ33
MA_DM1	26	DM1	MA_DQ34	135	MA_DQ34
MA_DM2	52	DM2	MA_DQ35	137	MA_DQ35
MA_DM3	67	DM3	MA_DQ36	124	MA_DQ36
MA_DM4	130	DM4	MA_DQ37	126	MA_DQ37
MA_DM5	147	DM5	MA_DQ38	134	MA_DQ38
MA_DM6	170	DM6	MA_DQ39	136	MA_DQ39
MA_DM7	185	DM7	MA_DQ40	141	MA_DQ40
MA_DQ80	13	DQ80	MA_DQ41	143	MA_DQ41
MA_DQ81	31	DQ81	MA_DQ42	151	MA_DQ42
MA_DQ82	51	DQ82	MA_DQ43	153	MA_DQ43
MA_DQ83	70	DQ83	MA_DQ44	140	MA_DQ44
MA_DQ84	131	DQ84	MA_DQ45	142	MA_DQ45
MA_DQ85	148	DQ85	MA_DQ46	152	MA_DQ46
MA_DQ86	169	DQ86	MA_DQ47	164	MA_DQ47
MA_DQ87	188	DQ87	MA_DQ48	157	MA_DQ48
MA_DQS#0	11	DQS#0	MA_DQ49	159	MA_DQ49
MA_DQS#1	29	DQS#1	MA_DQ50	173	MA_DQ50
MA_DQS#2	49	DQS#2	MA_DQ51	175	MA_DQ51
MA_DQS#3	68	DQS#3	MA_DQ52	168	MA_DQ52
MA_DQS#4	129	DQS#4	MA_DQ53	160	MA_DQ53
MA_DQS#5	146	DQS#5	MA_DQ54	174	MA_DQ54
MA_DQS#6	167	DQS#6	MA_DQ55	176	MA_DQ55
MA_DQS#7	186	DQS#7	MA_DQ56	179	MA_DQ56
			MA_DQ57	181	MA_DQ57
			MA_DQ58	189	MA_DQ58
			MA_DQ59	191	MA_DQ59
			MA_DQ60	180	MA_DQ60
			MA_DQ61	182	MA_DQ61
			MA_DQ62	192	MA_DQ62
			MA_DQ63	184	MA_DQ63

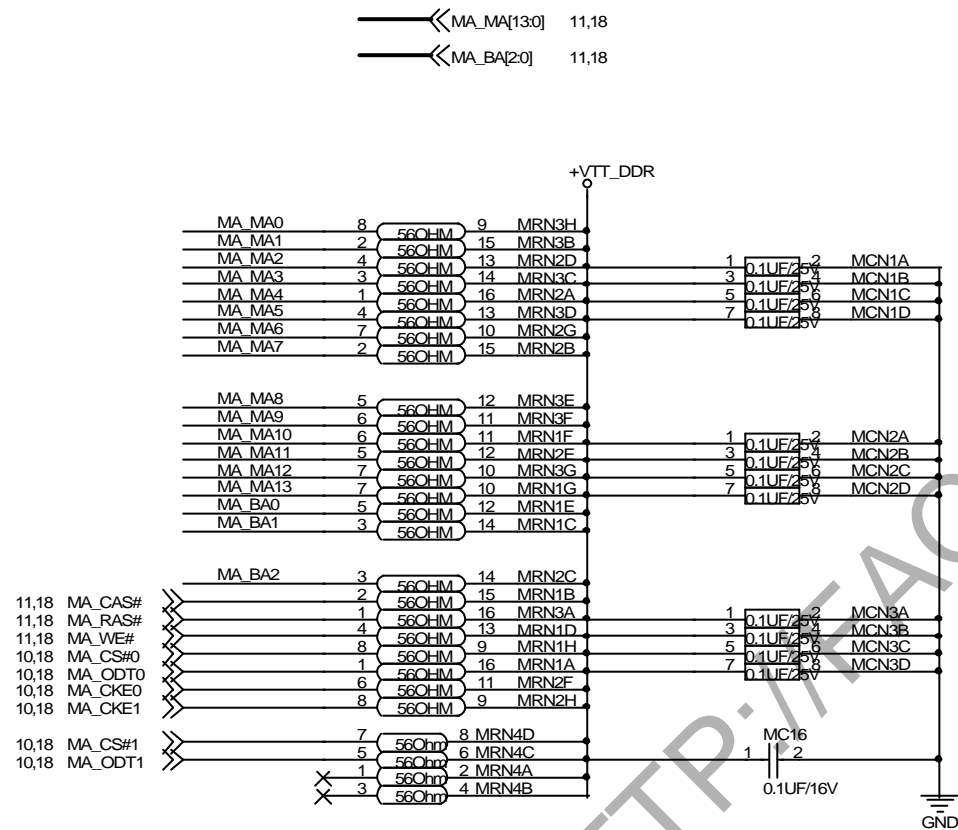
DDR\_DIMM\_200P  
12G025332003

GROUP1  
GROUP2  
SWAP




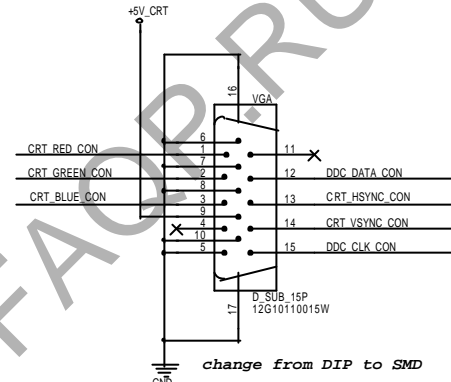
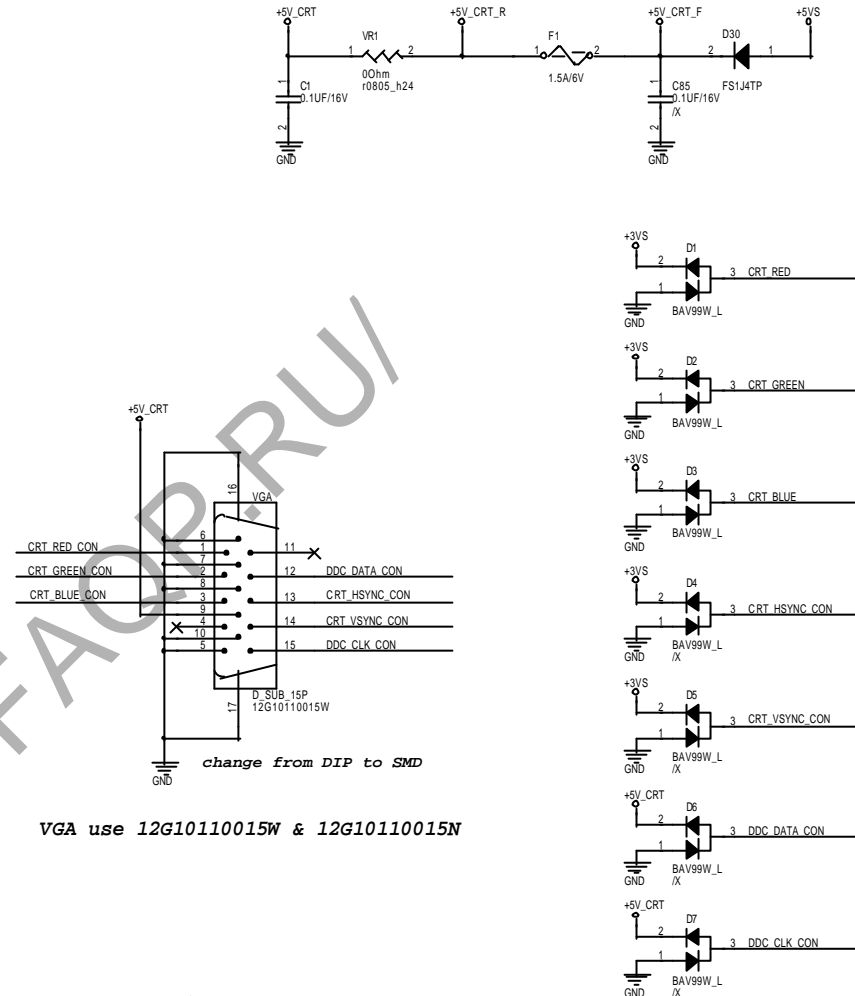
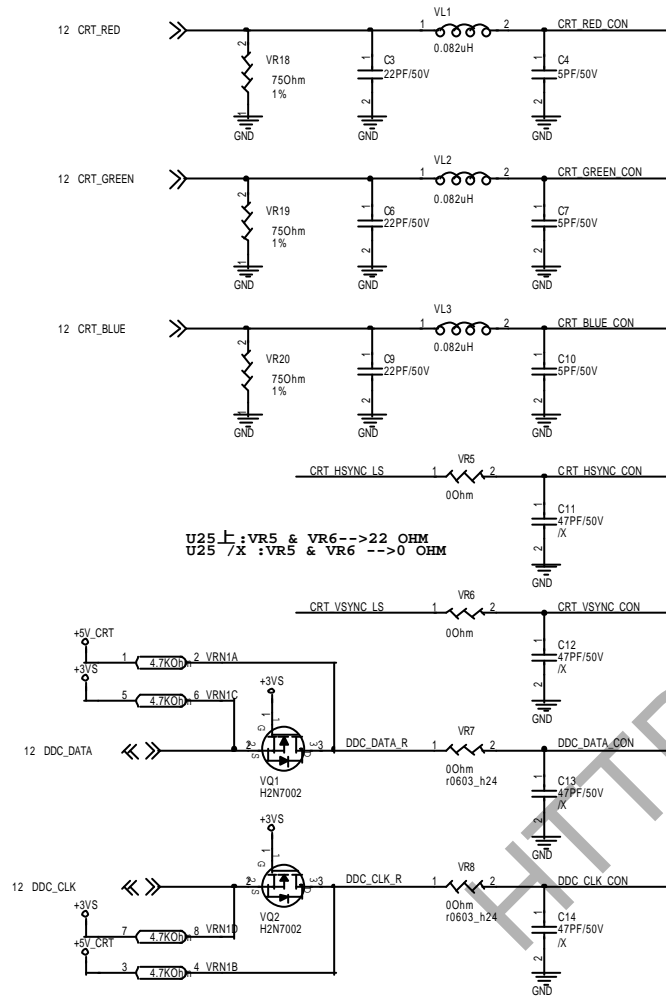
<Core Design>

ASUS		Title : DDR2 SODIMM	
ASUS Tek Computer INC.		Engineer: Wayne_Chan	
Size A3	Project Name 1000HD	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 18 of 49	

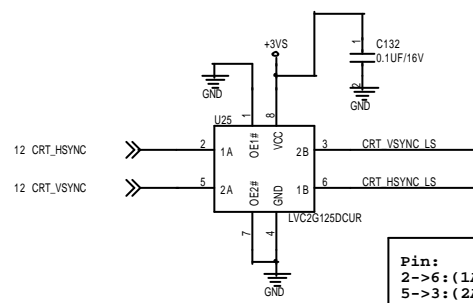


<Core Design>

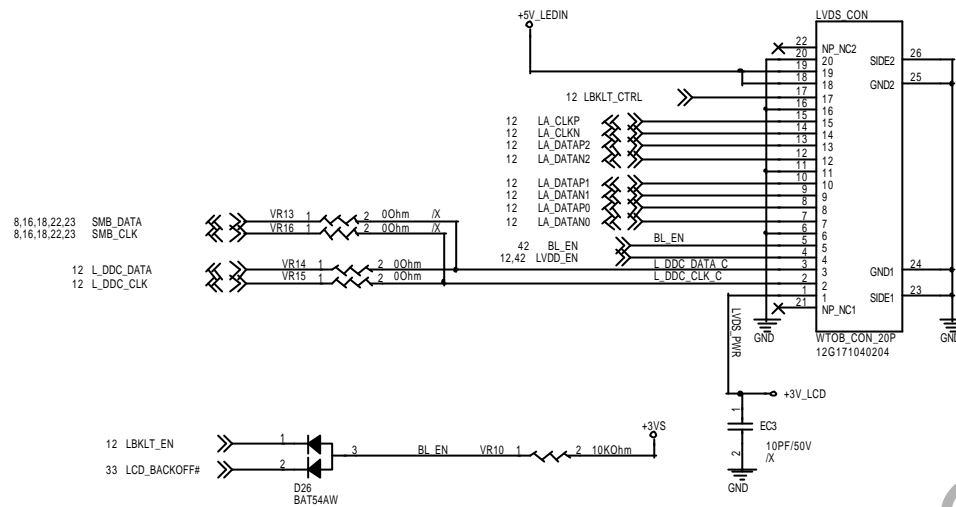
		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: Wayne_Chan	
Size A4	Project Name 1000HD	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 19 of 49	



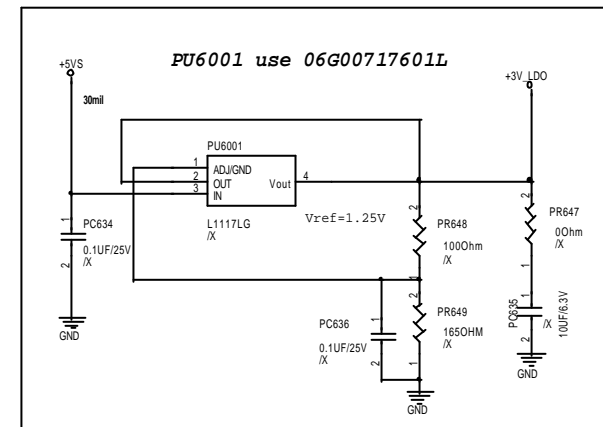
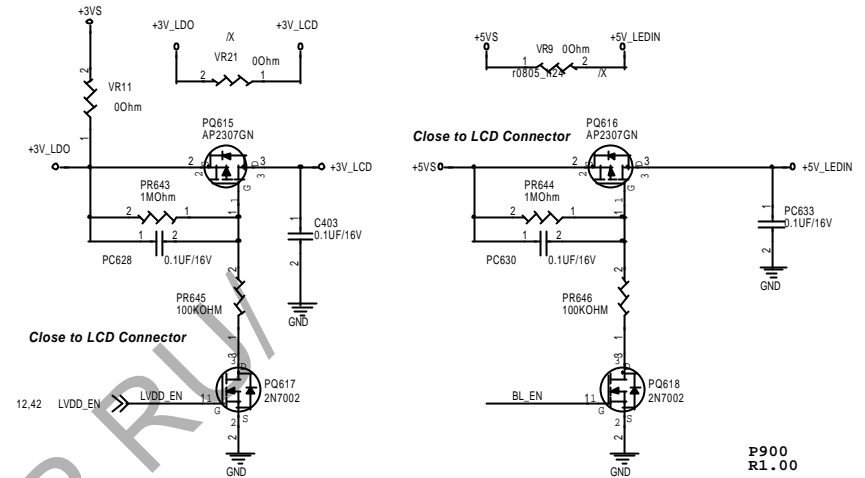
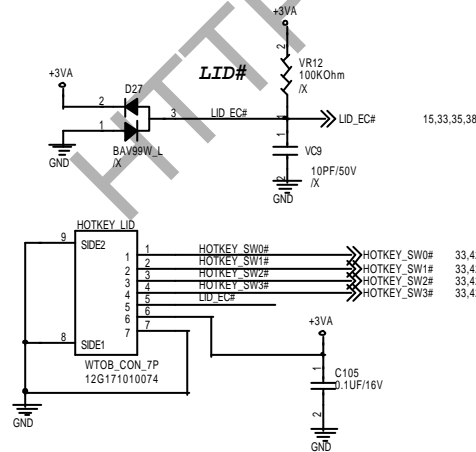
VGA use 12G10110015W & 12G10110015N



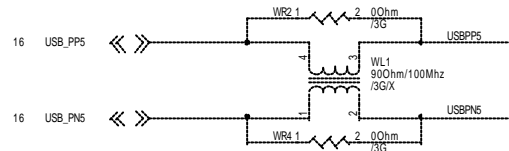
Pin:  
2->6: (1A->1B)  
5->3: (2A->2B)



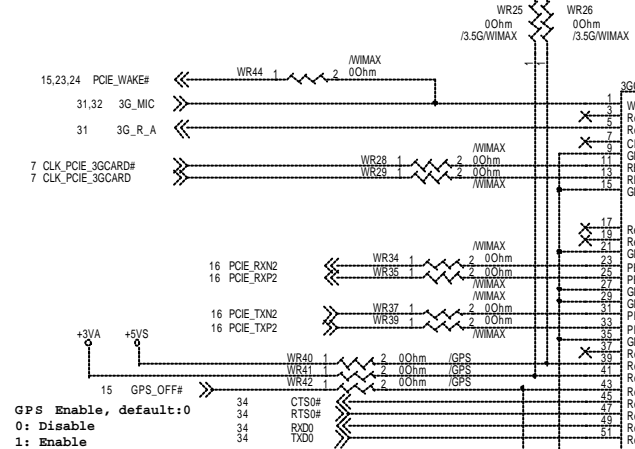
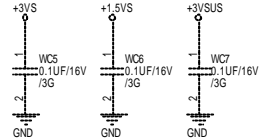
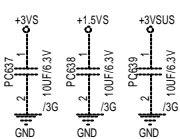
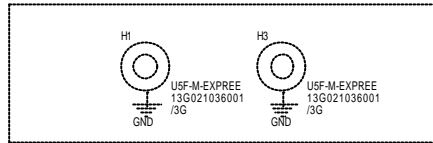
L_DDC_CLK_C	EC1	2	1	10PF/50V
L_DDC_DATA_C	EC2	2	1	10PF/50V
LA_CLKP	VC1	2	1	10PF/50V
LA_CLKN	VC2	2	1	10PF/50V
LA_DATA2	VC3	2	1	10PF/50V
LA_DATA2	VC4	2	1	10PF/50V
LA_DATA1	VC5	2	1	10PF/50V
LA_DATA1	VC6	2	1	10PF/50V
LA_DATA0	VC7	2	1	10PF/50V
LA_DATA0	VC8	2	1	10PF/50V



<Core Design>



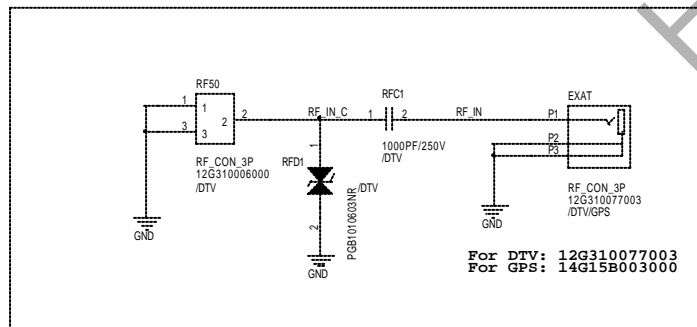
/GPS: AW GPS-M09  
/DTV: ASUS MC3100U  
/3.5G: SIERRA 8780  
/WIMAX: INTEL5050



GPS Enable, default:0  
0: Disable  
1: Enable

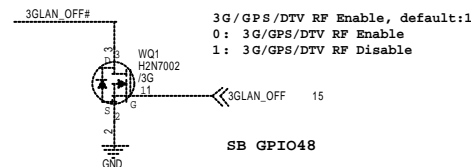
WR43:  
For 3.5G/WIMAX: 0ohm  
For GPS: 100Kohm

#### External Antenna

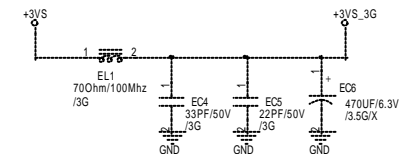


For DTV: 12G310077003  
For GPS: 14G15B003000

MINICARD use 12G03010052K



SB GPIO48



3G/GPS/DTV RF Enable, default:1  
0: 3G/GPS/DTV RF Enable  
1: 3G/GPS/DTV RF Disable

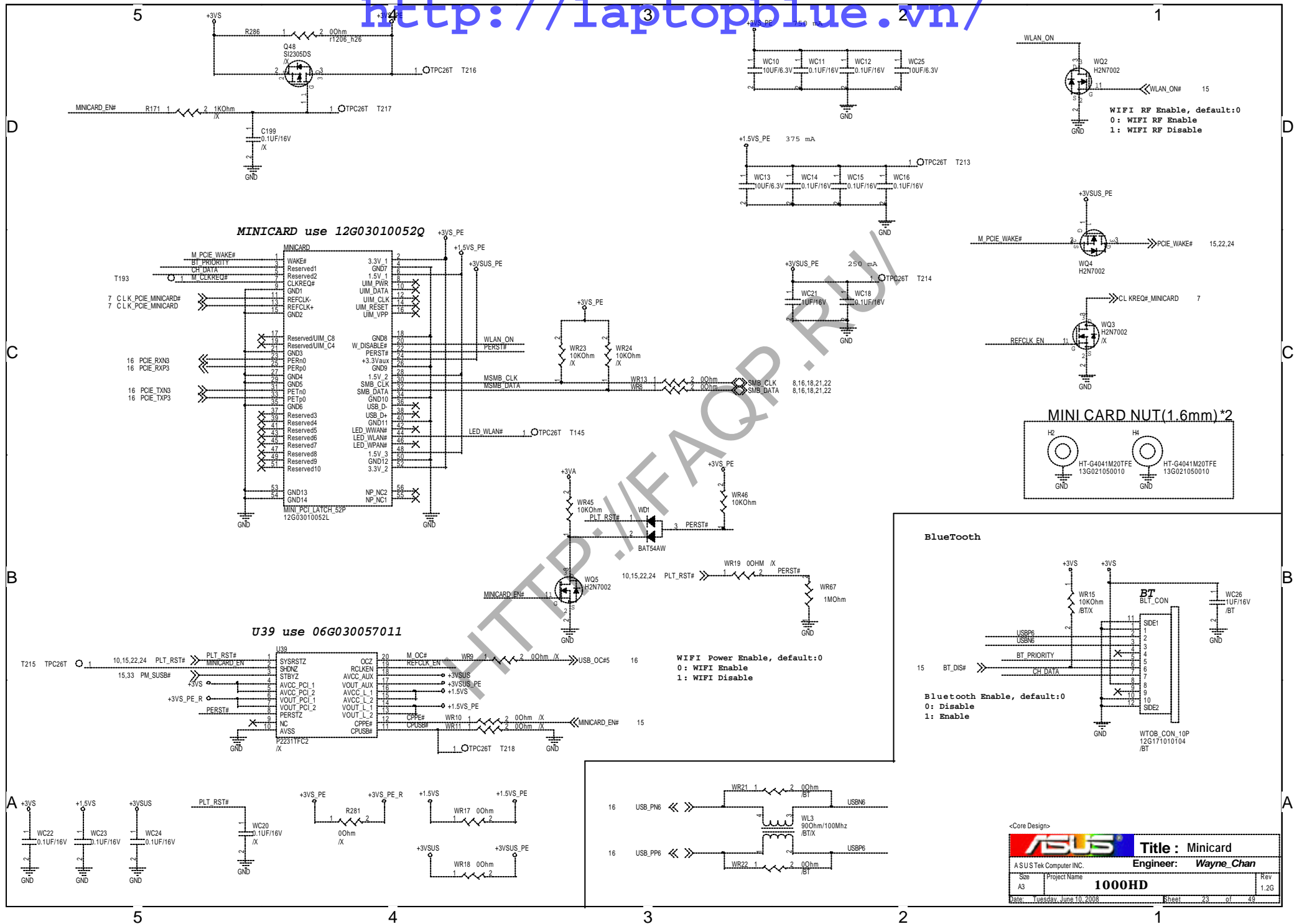
<Core Design>

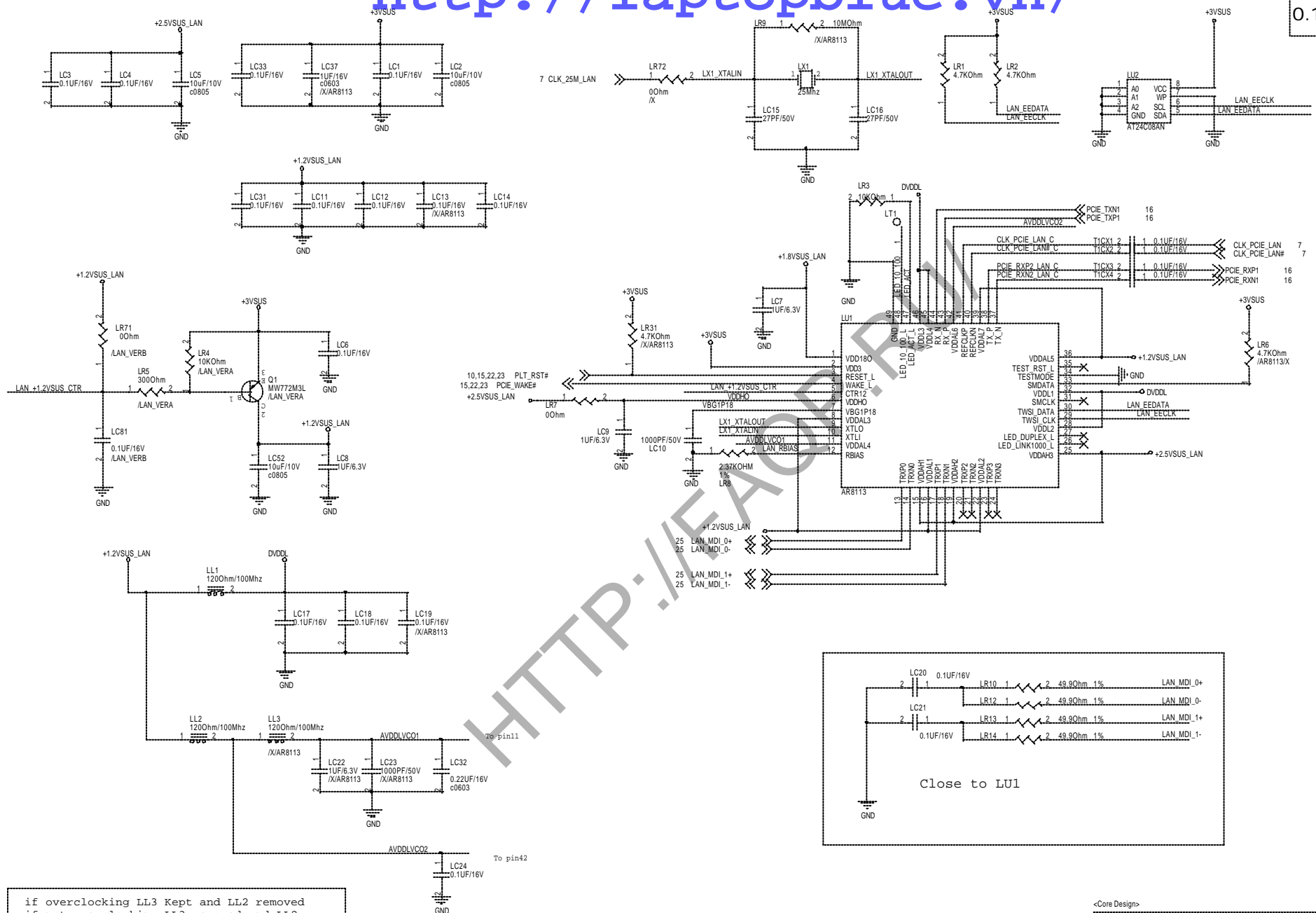


3.5G Module & External Antenna

Title :

ASUS Tek Computer INC.	Engineer: Wayne Chan
Size: A3	Project Name: 1000HD
Date: Tuesday, June 10, 2008	Sheet: 22 of 49

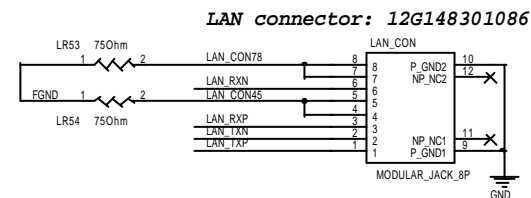
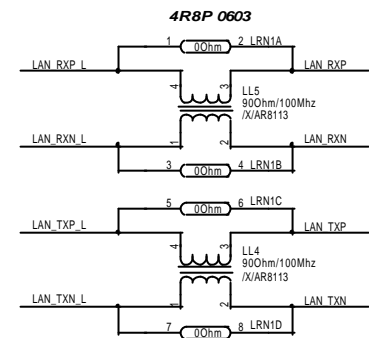
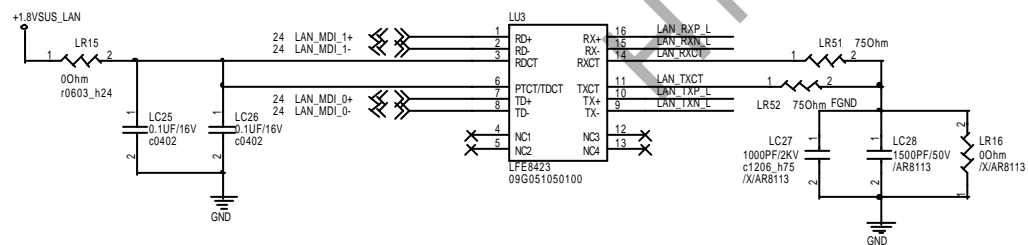




<Core Design>

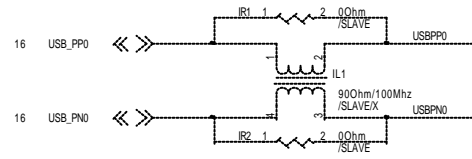
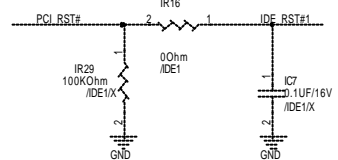
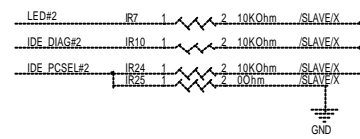
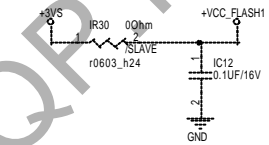
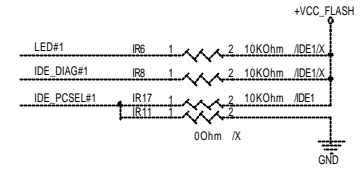
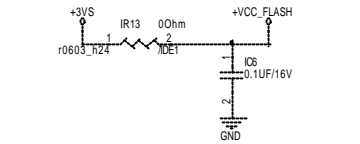
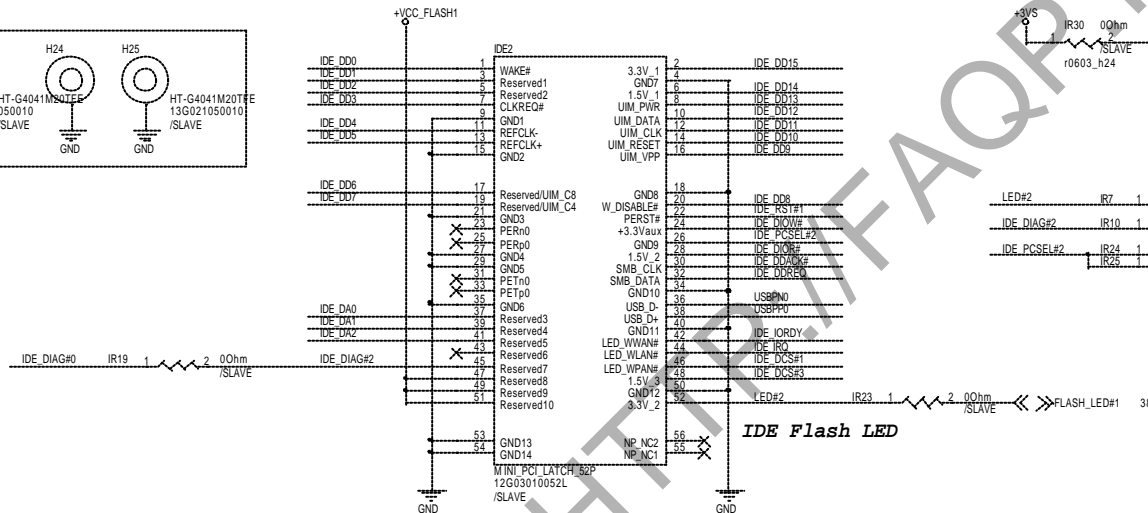
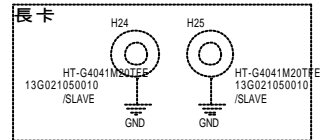
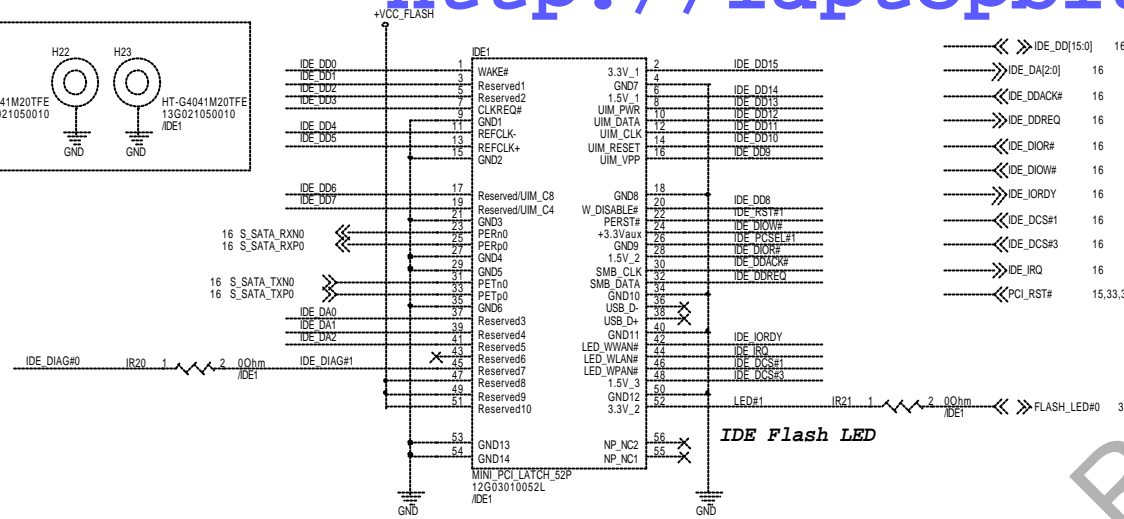
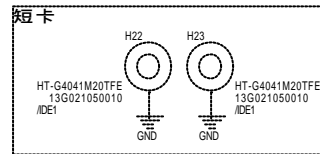
<b>ASUS</b>		<b>Title : AR8113</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne Chan</b>	
Size	Project Name	1000HD	Rev
A3			1.2G
Date: Tuesday, June 10, 2008		Sheet	24 of 49





<Core Design>

		Title : MDC_RJ45	
ASUS Tek Computer INC.		Engineer: Wayne_Chan	
Size A3	Project Name 1000HD	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 25 of 49	

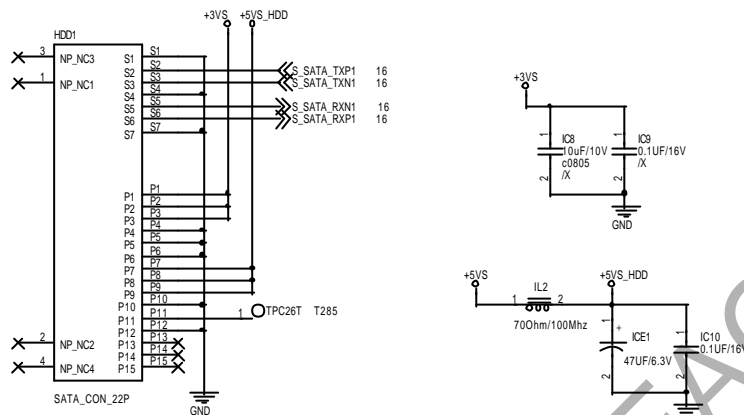


Naming Rule:  
IC: IU?  
R: IR?  
C: IC?  
L: IL?

<Core Design>

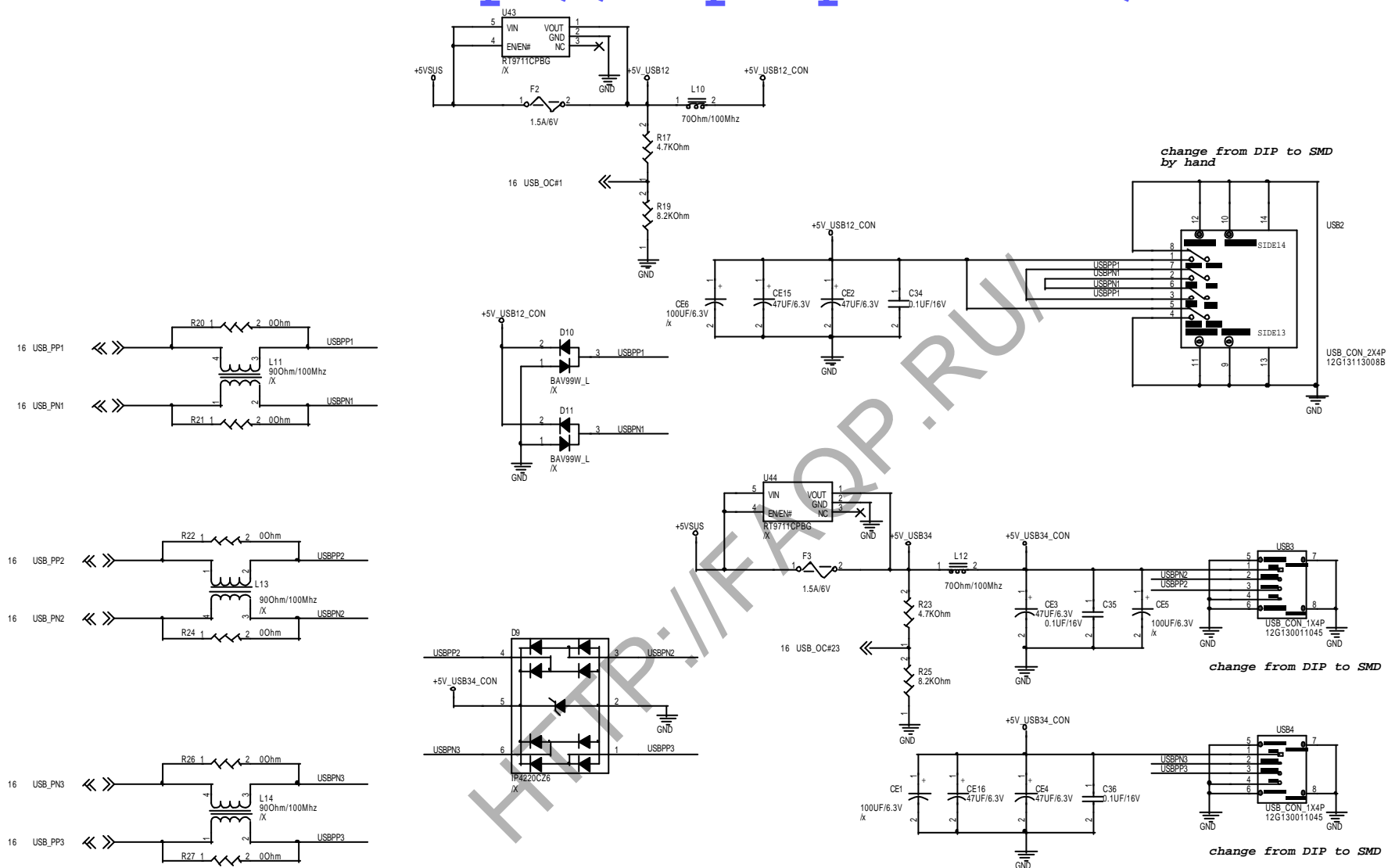
Change\_ODD to  
SATA IF

## SATA HDD Connector

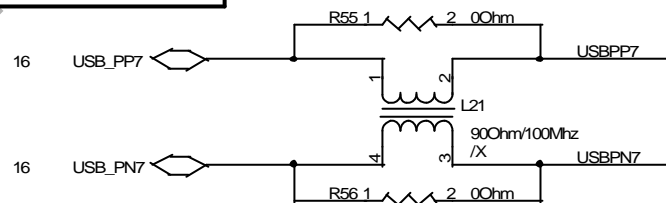
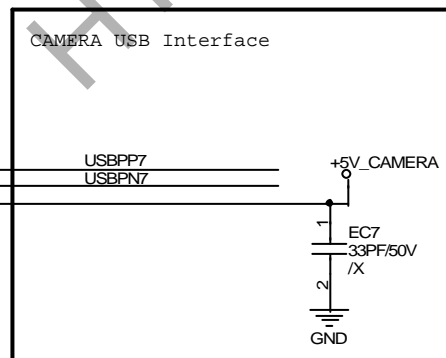
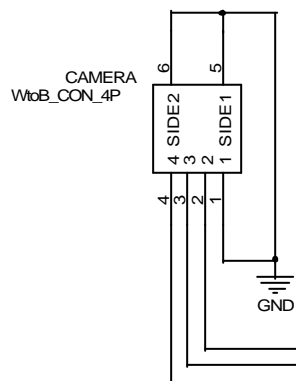
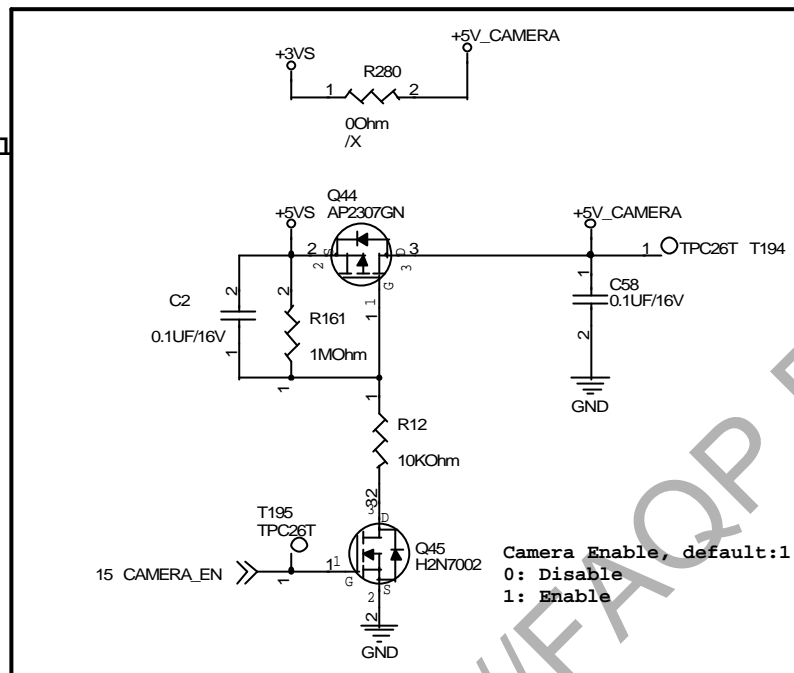


<Core Design>

<b>ASUS</b>		<b>Title : HD + Flash Conn</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne_Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet 27 of 49	



## Power Control



<Core Design>



**Title :** Camera Power

ASUSTek Computer INC.

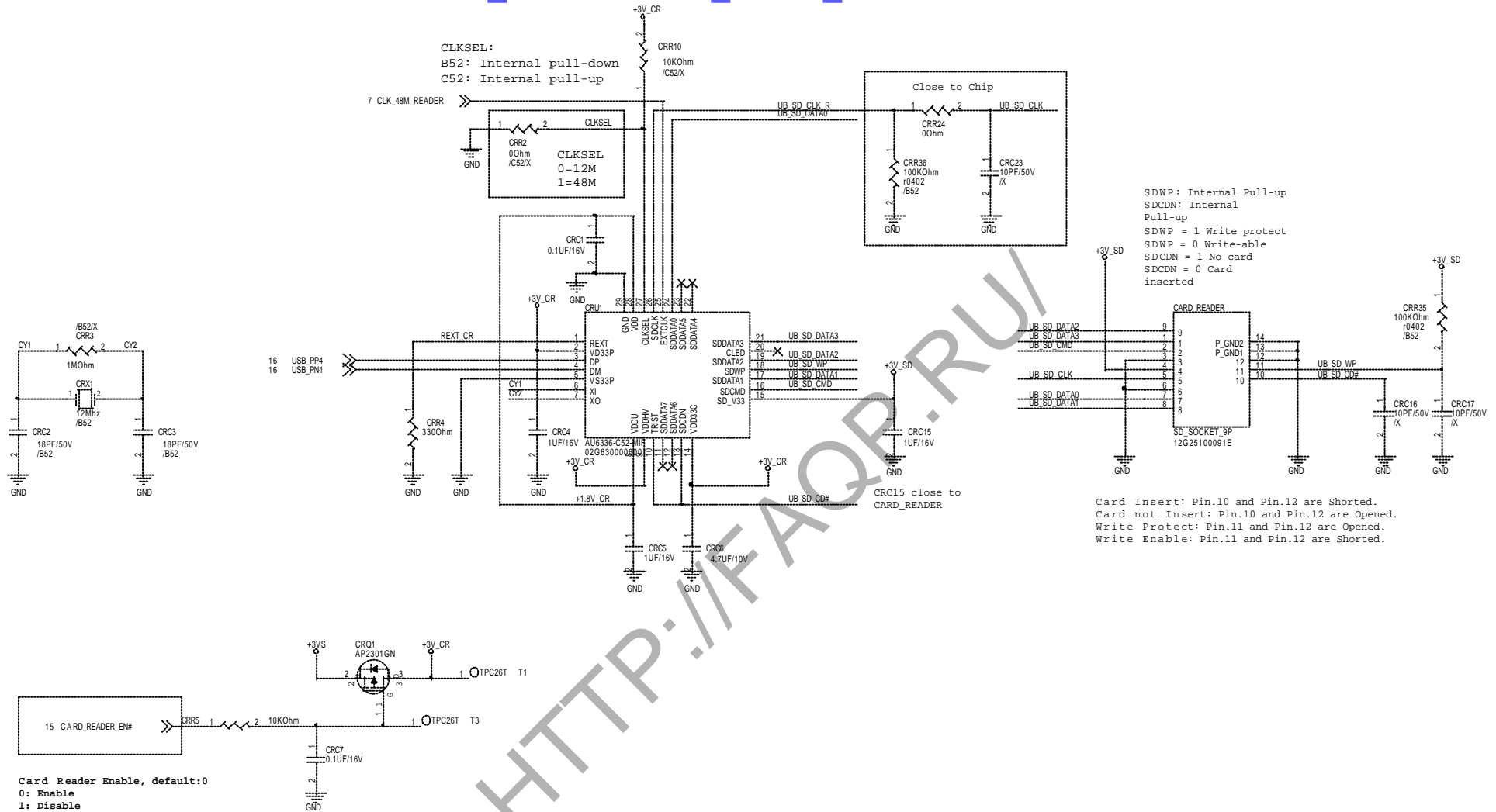
Engineer: *Wayne\_Chan*

Size	Project Name
A4	<b>1000HD</b>

Rev	1.2G
-----	------

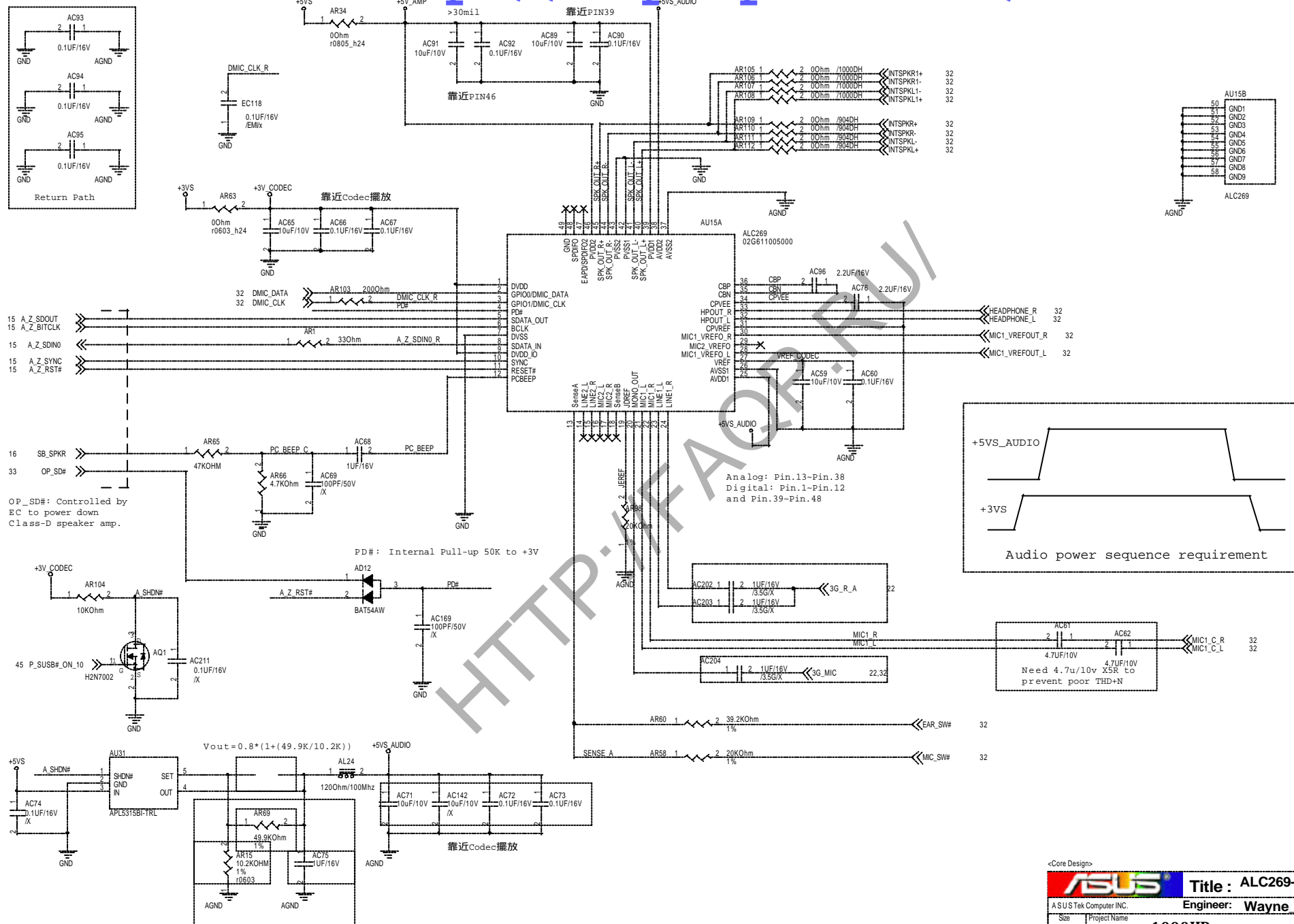
Date: Tuesday, June 10, 2008.

Sheet 29 of 49



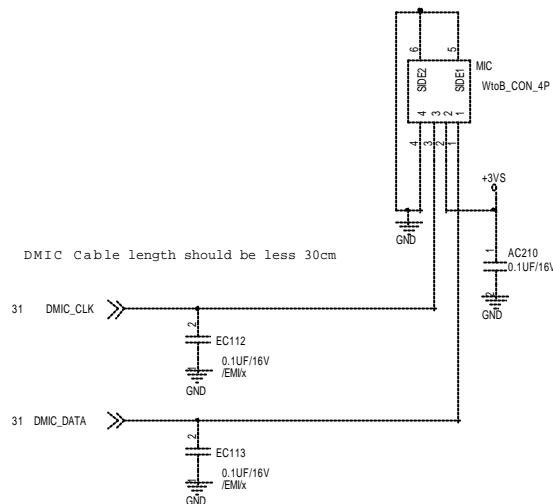
<Core Design>

<b>ASUS</b>		<b>Title : AU6336-C52</b>	
ASUS Tek Computer INC.		<b>Engineer: Wayne Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet: 30 of 49	

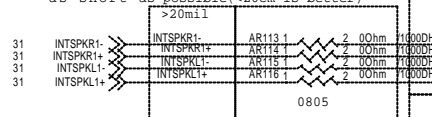


<Core Design>

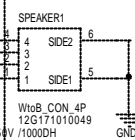
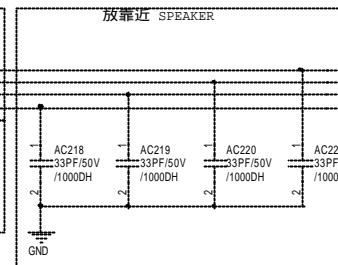
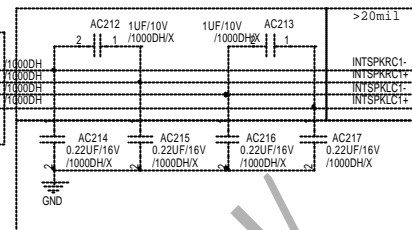
<b>ASUS</b>		<b>Title : ALC269-1</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet	34 of 49



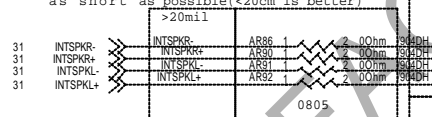
Total length from speakerR+ L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)



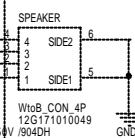
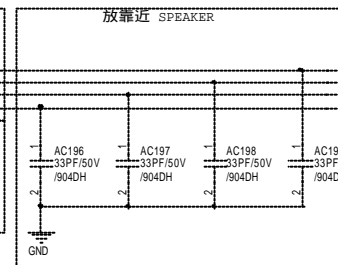
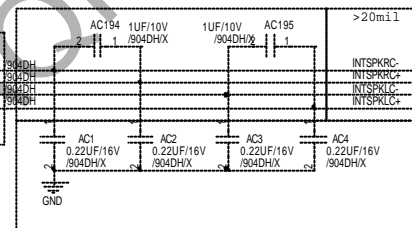
If choke AR113, AR114, AR115, AR116 are mounted, please mount AC212 AC213 to avoid EMI issue.



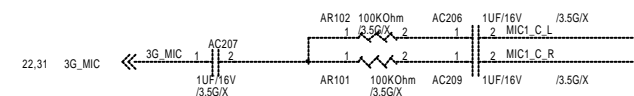
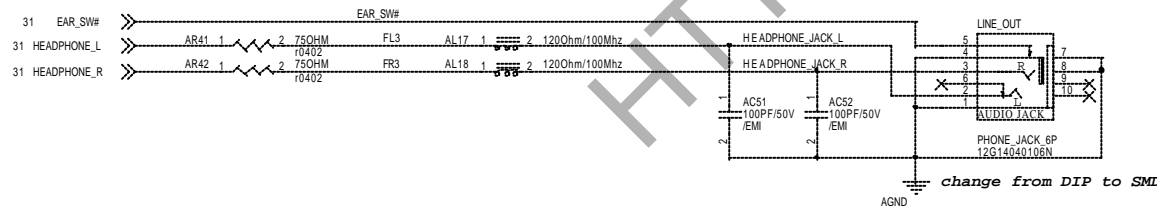
Total length from speakerR+ L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)



If choke AR86, AR90, AR91, AR92 are mounted, please mount AC194 AC195 to avoid EMI issue.

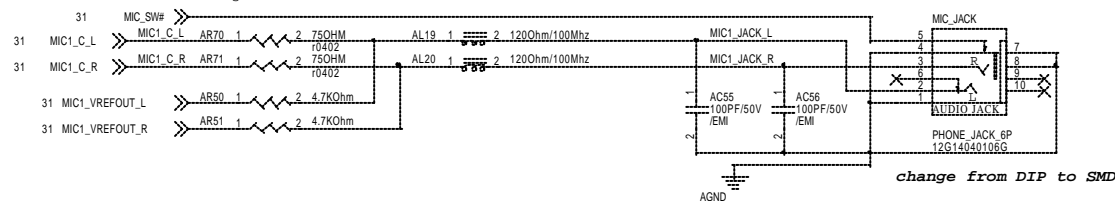


LINE\_OUT use 12G140501060



R70 and R71: If don't need retasking function, change to 1K.

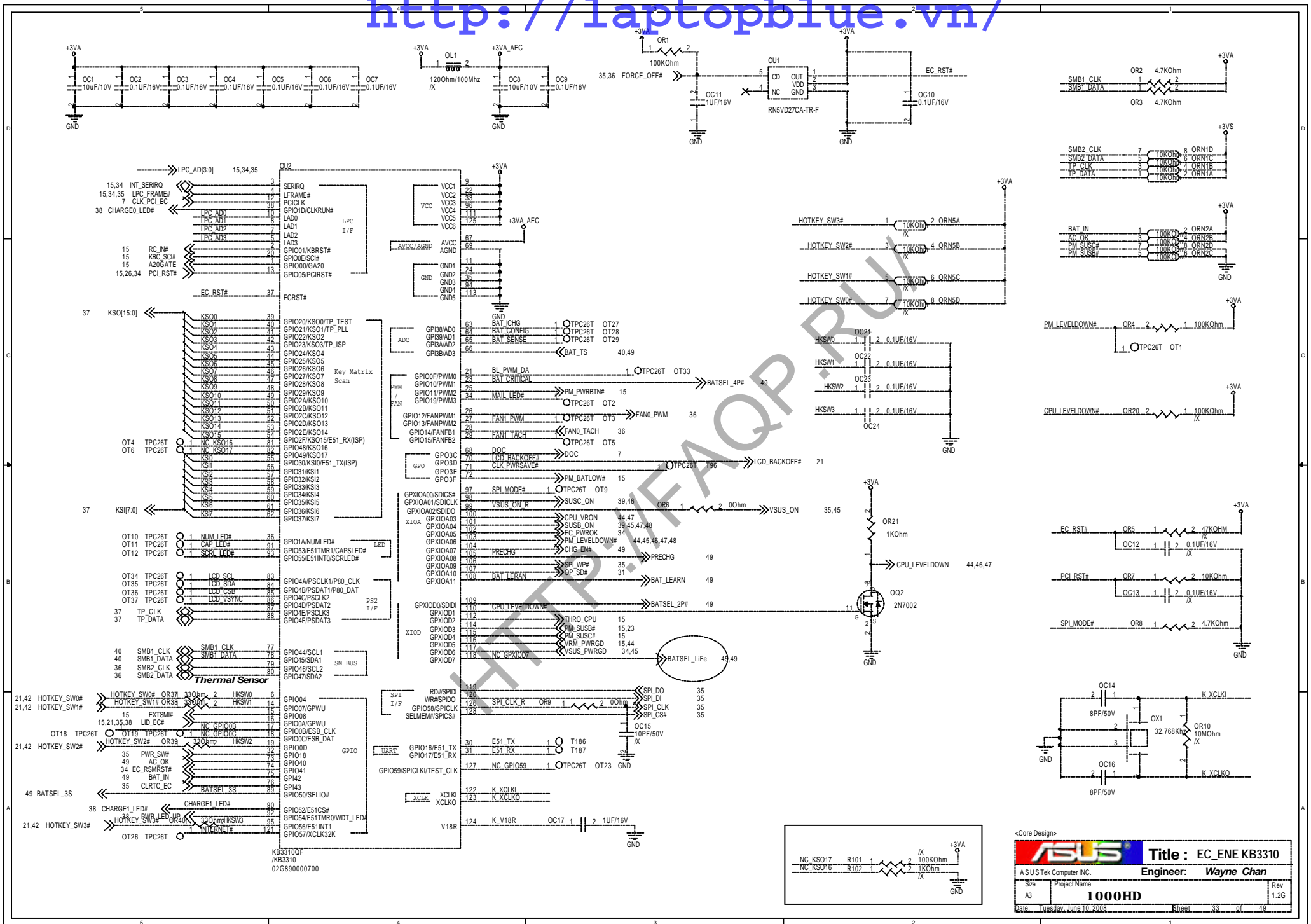
MIC JACK use 12G14040106Y

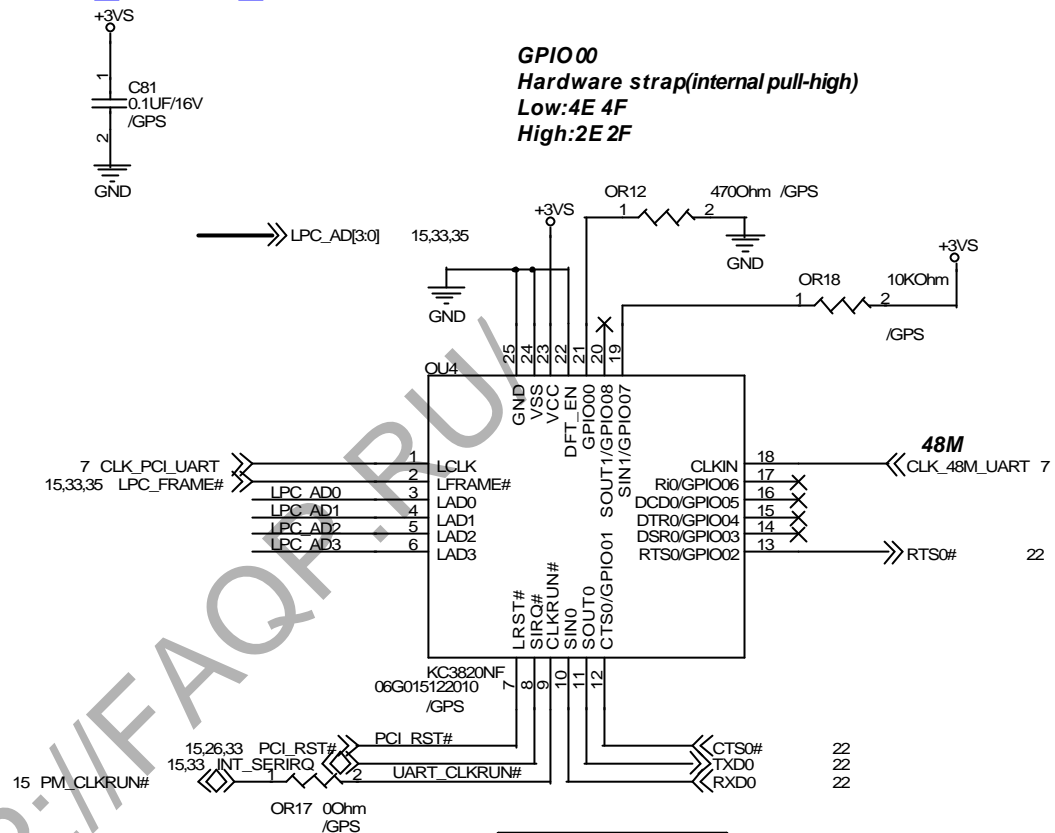
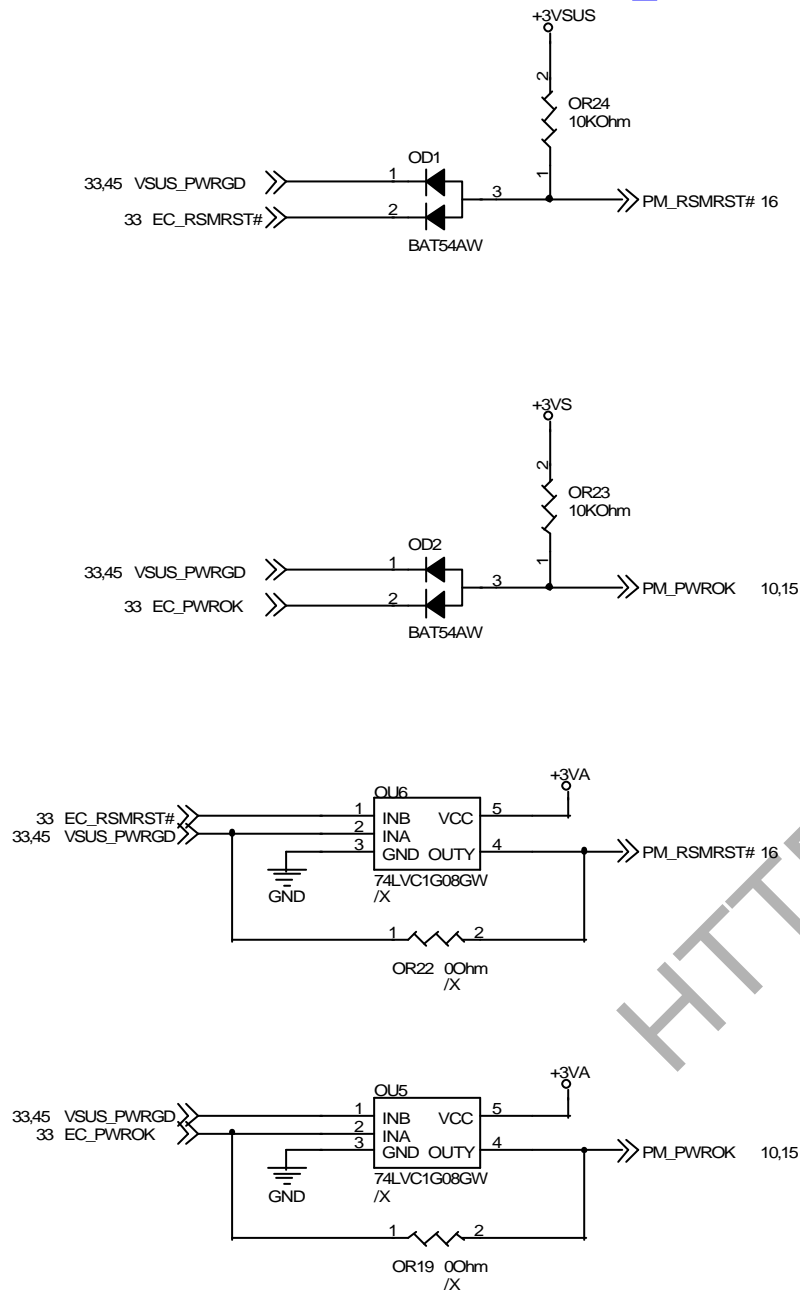


<Core Design>

<b>ASUS</b>		Title : ALC269-2	
ASUS Tek Computer INC.		Engineer: Wayne Chan	
Size	Project Name	1000HD	Rev
A3			1.2G
Date: Tuesday, June 10, 2008		Sheet	32 of 48







UART Control  
IC for using  
GPS module due  
to no UART on  
ENE EC

<Core Design>

ASUS		Title : EC_UART_KC3820	
ASUSTek Computer INC.		Engineer: Wayne_Chan	
Size A4	Project Name 1000HD		Rev 1.2G
Date: Tuesday, June 10, 2008		Sheet	34 of 49

```
prevent system auto power on when CMOS clear
```

***For Debug***

Debug Card cable use Z96 Touch Pad cable, P/N:  
14G124110126, 14G124110120, 14G124110121  
14G124110124, 14G124110125

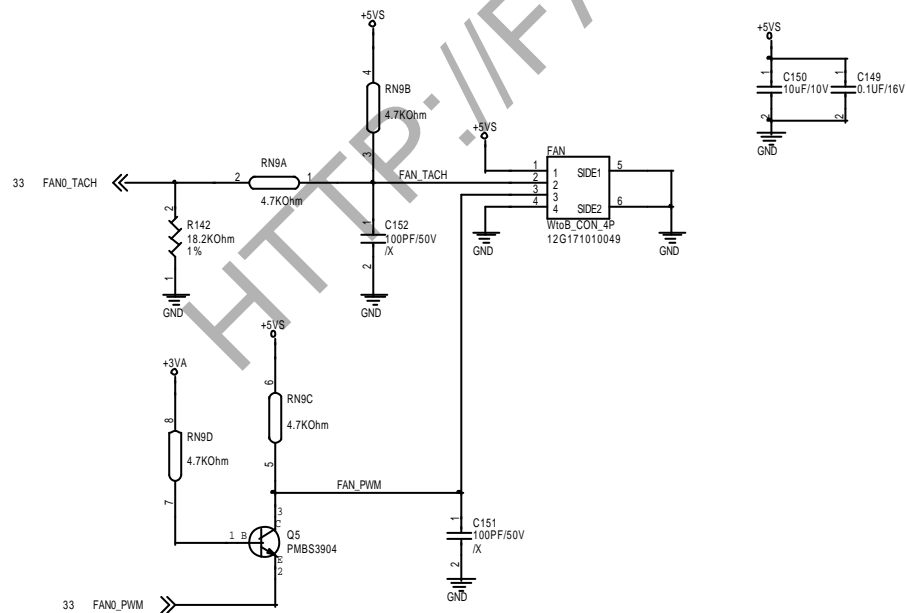
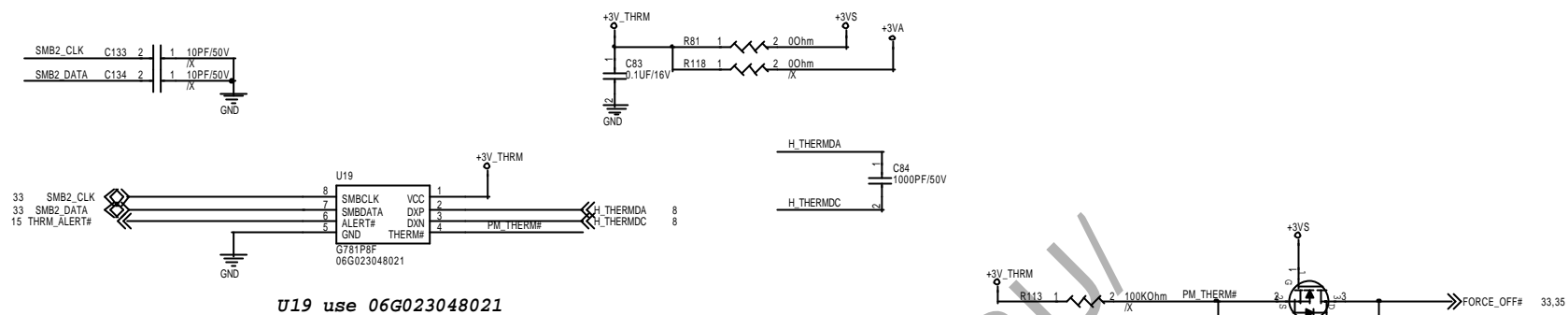
```
prevent system auto power on when CMOS clear
```

&lt;Core Design&gt;



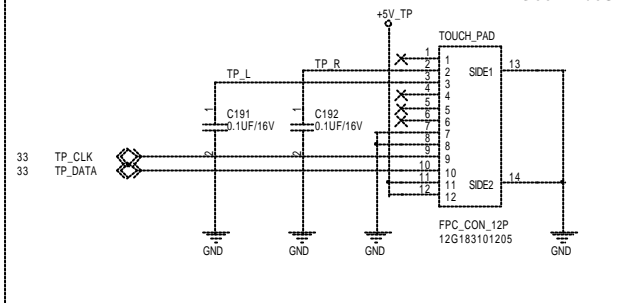
**Title :** Switch\_SPI ROM\_Debug

ASUS Tek Computer INC.		Engineer: <b>Wayne_Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2C	
Date: <b>Tuesday, June 10, 2008</b>		Sheet <b>35</b> of <b>49</b>	

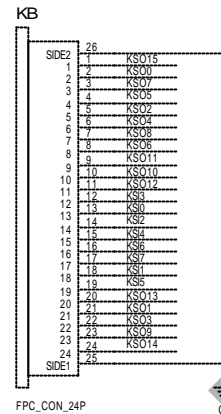


***For Touch-Pad***

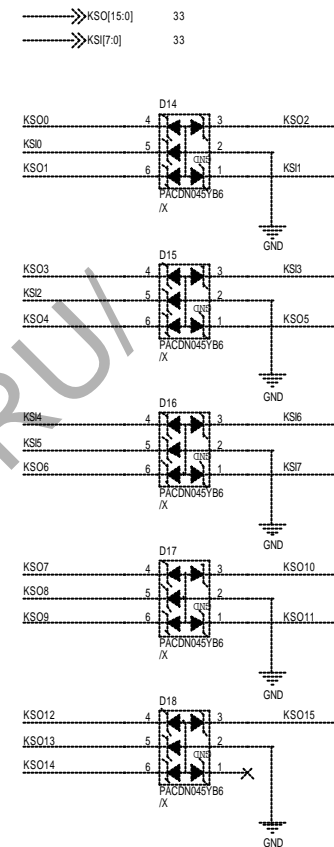
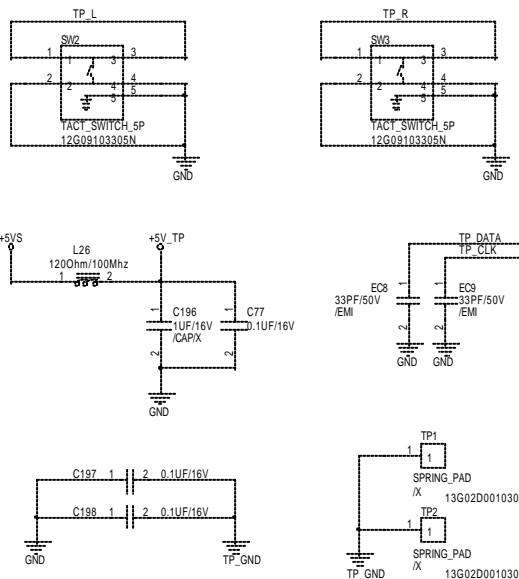
P900 R1.0G



***For Keyboard Connector***

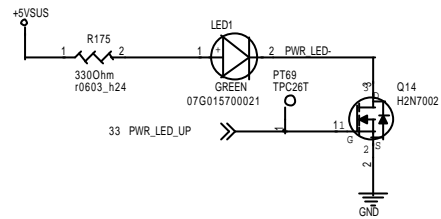


SW2, SW3 use 12G09103305N

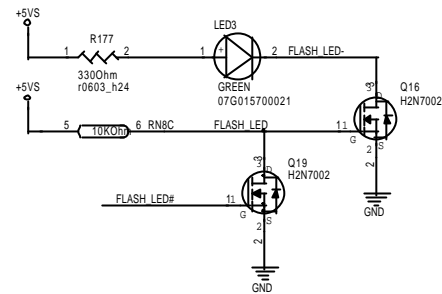


KS10	EC10	1	2	33PF/50V
KS11	EC11	1	2	33PF/50V
KS12	EC12	1	2	33PF/50V
KS13	EC13	1	2	33PF/50V
KS14	EC14	1	2	33PF/50V
KS15	EC15	1	2	33PF/50V
KS16	EC16	1	2	33PF/50V
KS17	EC17	1	2	33PF/50V
KS00	EC18	1	2	33PF/50V
KS01	EC19	1	2	33PF/50V
KS02	EC20	1	2	33PF/50V
KS03	EC21	1	2	33PF/50V
KS04	EC22	1	2	33PF/50V
KS05	EC23	1	2	33PF/50V
KS06	EC24	1	2	33PF/50V
KS07	EC25	1	2	33PF/50V
KS08	EC26	1	2	33PF/50V
KS09	EC27	1	2	33PF/50V
KS010	EC28	1	2	33PF/50V
KS011	EC29	1	2	33PF/50V
KS012	EC30	1	2	33PF/50V
KS013	EC31	1	2	33PF/50V
KS014	EC32	1	2	33PF/50V
KS015	EC33	1	2	33PF/50V

### for POWER LED

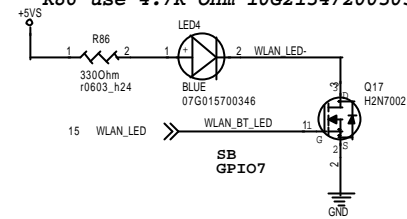


### for FLASH LED



### for WLAN/BlueTooth LED

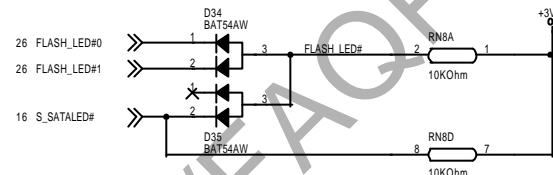
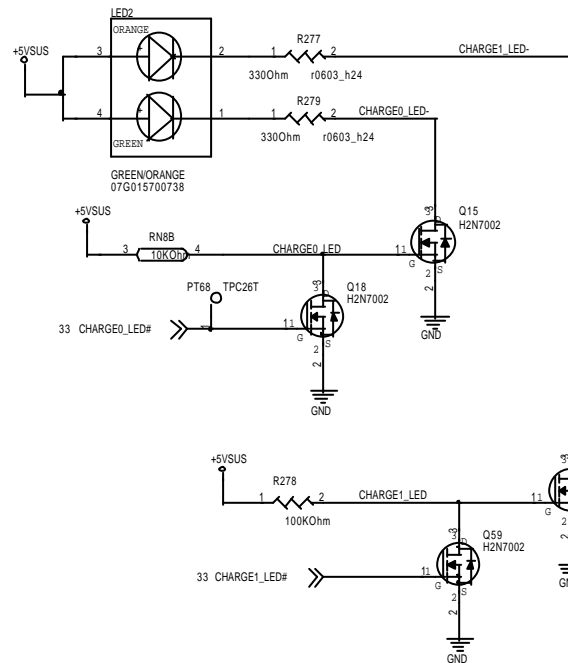
R86 use 4.7K OHm 10G213472003030



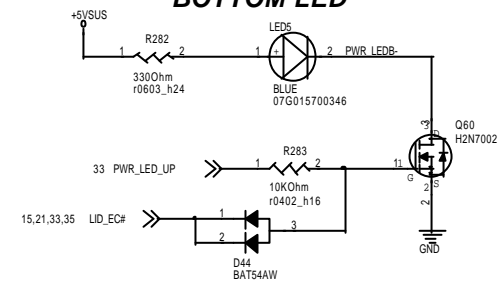
SB  
GPIO7

WIFI/BT LED Enable,default:1  
0: WIFI and BT are both disabled  
1: one of WIFI and BT is Enable or both are Enable

### for CHARGE LED

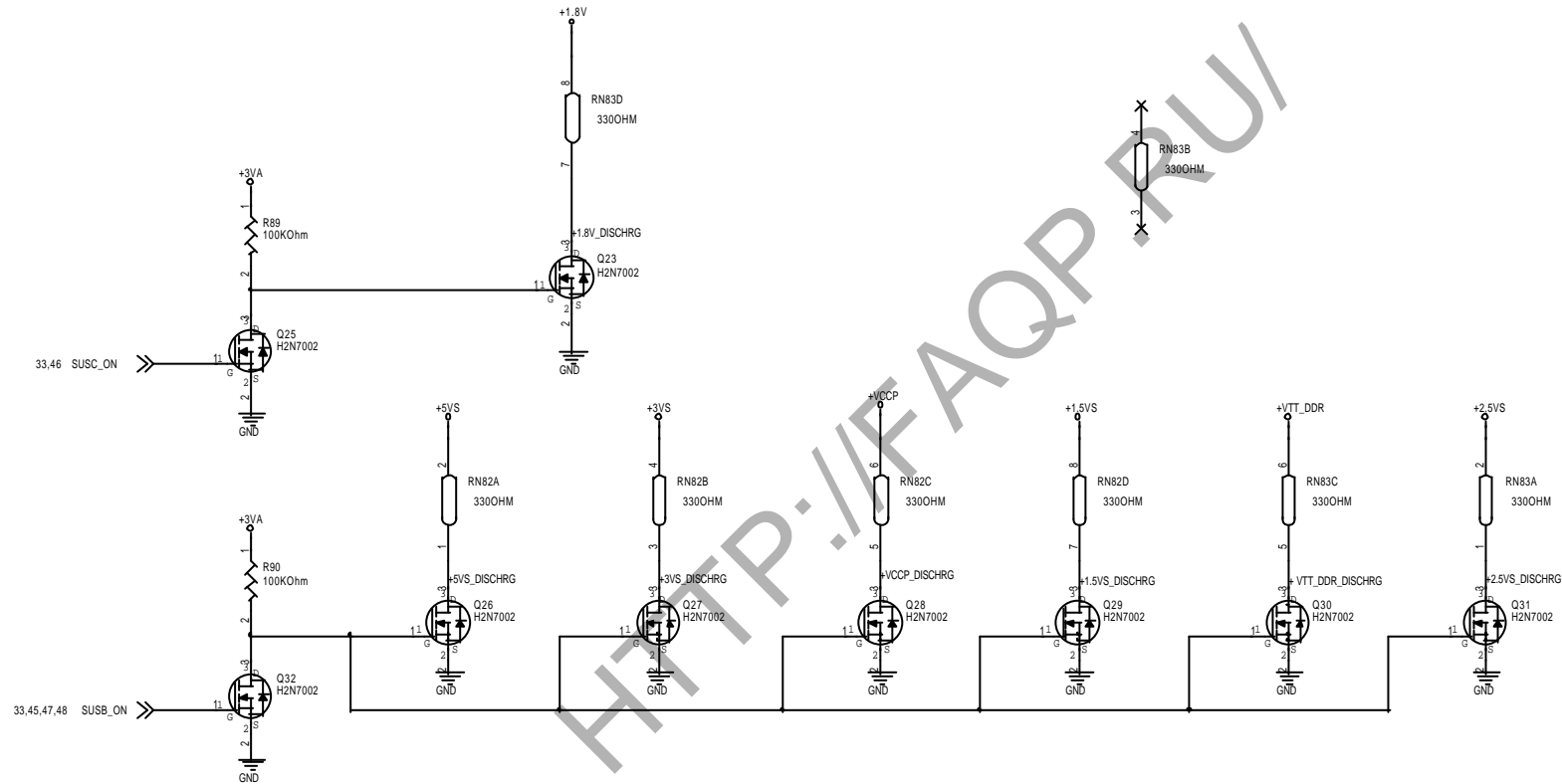


### for POWER BOTTOM LED



<Core Design>

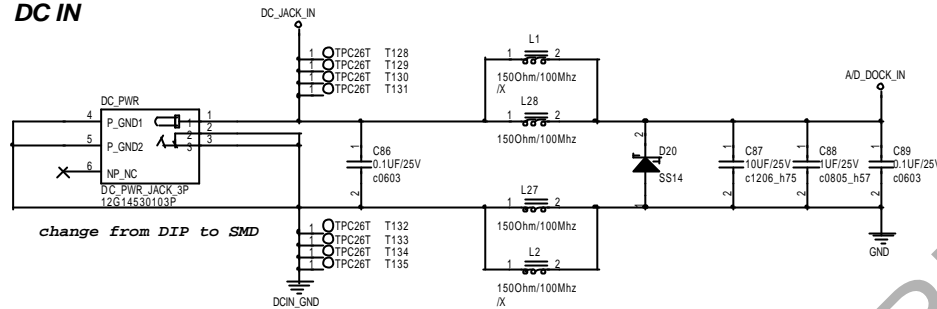
<b>ASUS</b>		<b>Title : LED</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne_Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: <b>Tuesday, June 10, 2008</b>		Sheet <b>38</b> of <b>48</b>	



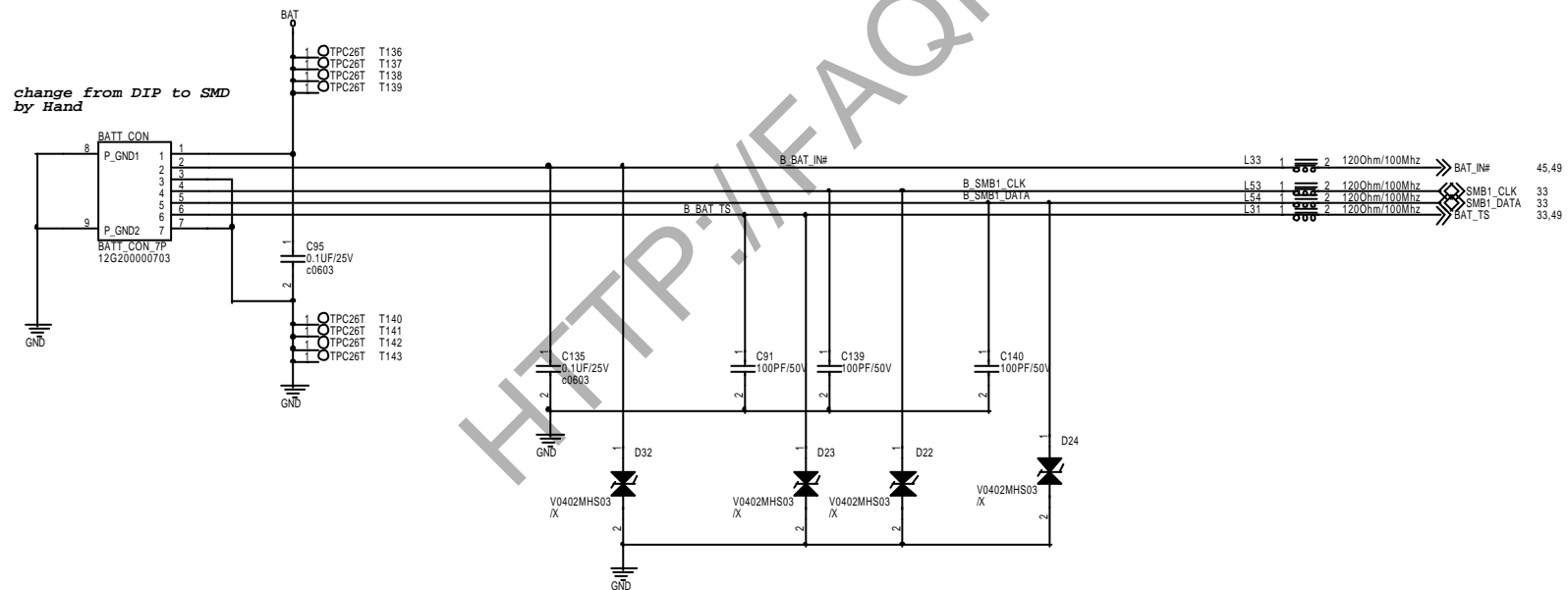
<Core Design>

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet	39 of 49

### DC IN



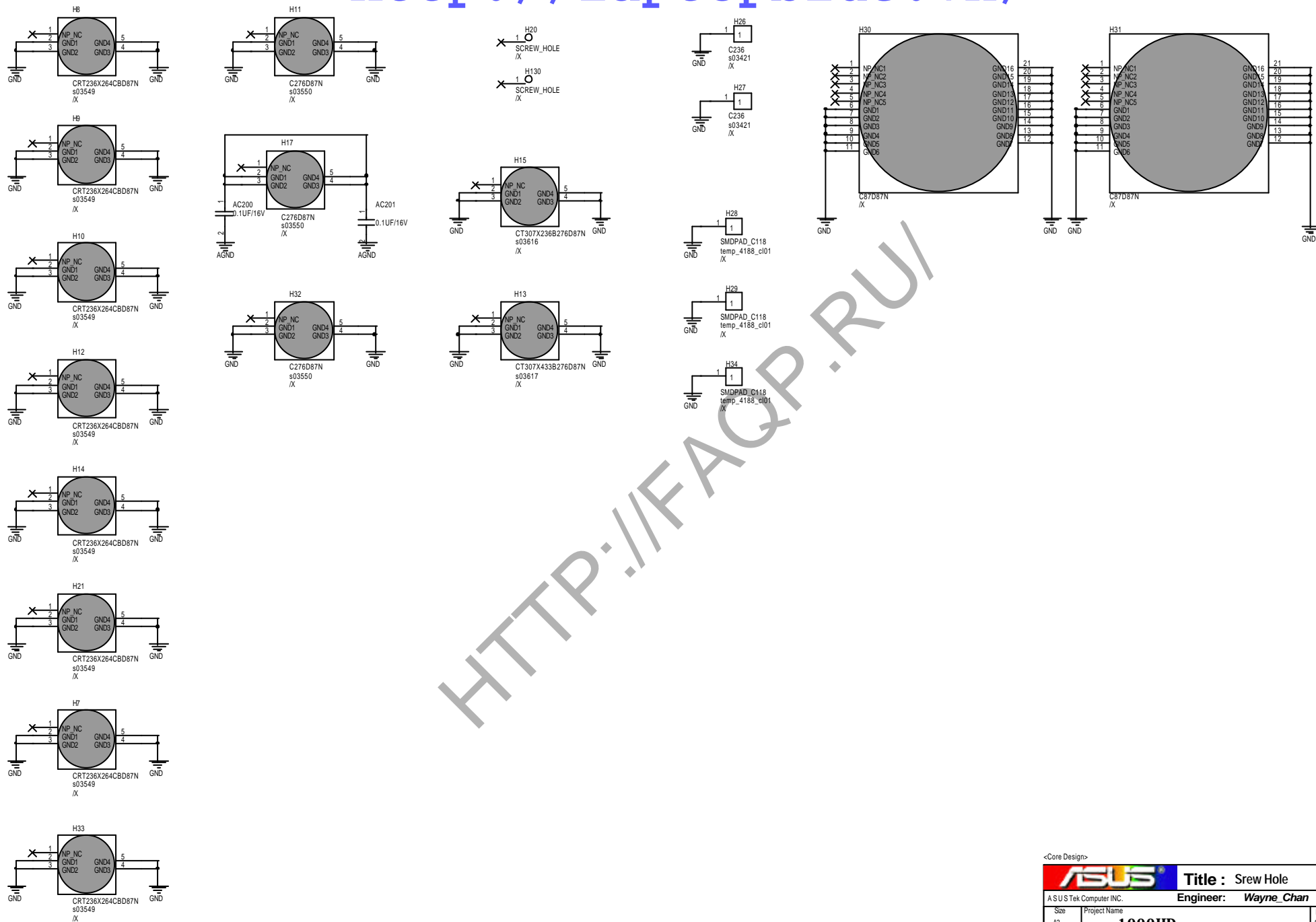
### BAT IN



<Core Design>

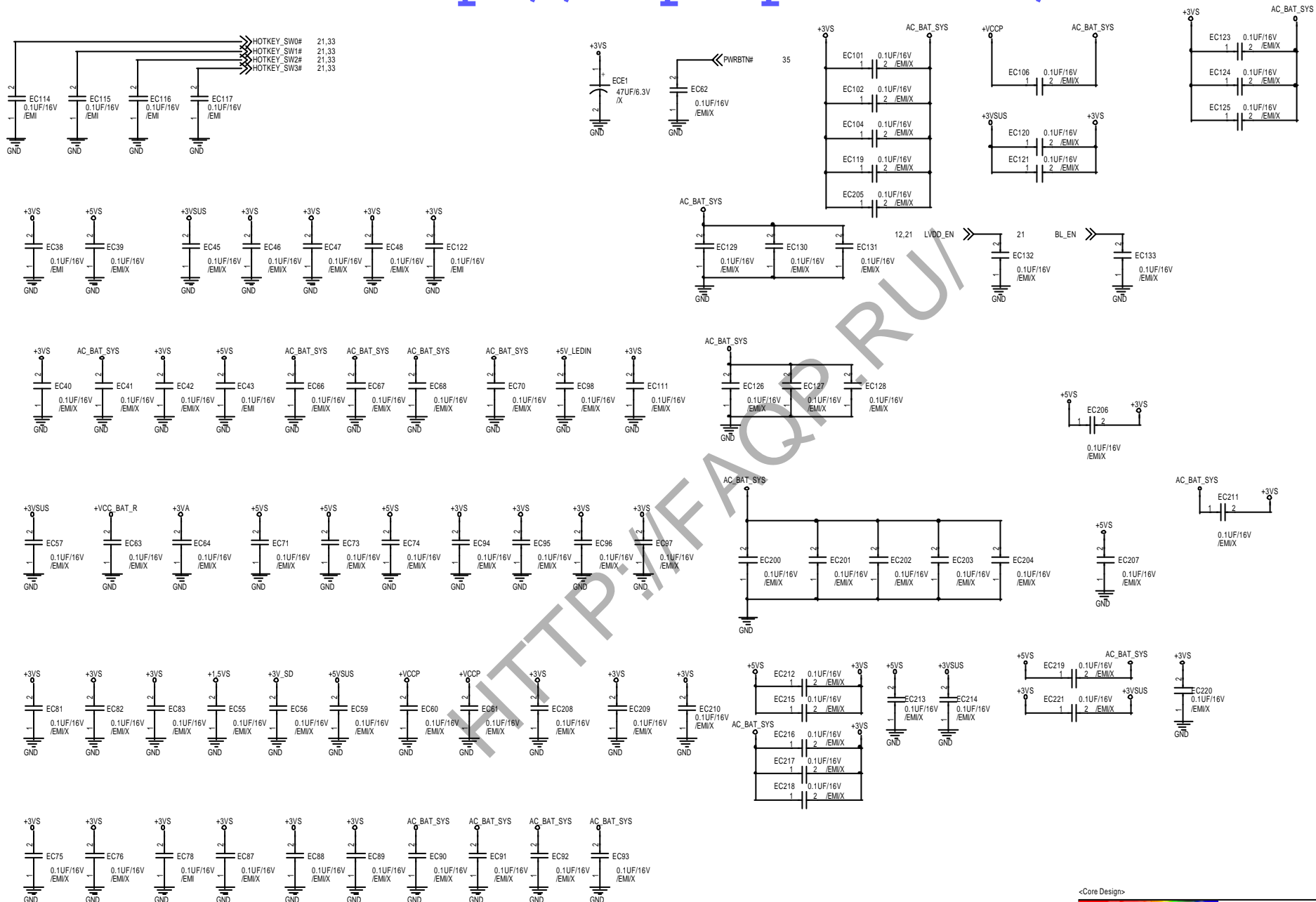
<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne Chan</b>	
Size A3	Project Name <b>1000HD</b>	Rev 1.2G	
Date: Tuesday, June 10, 2008		Sheet	40 of 49

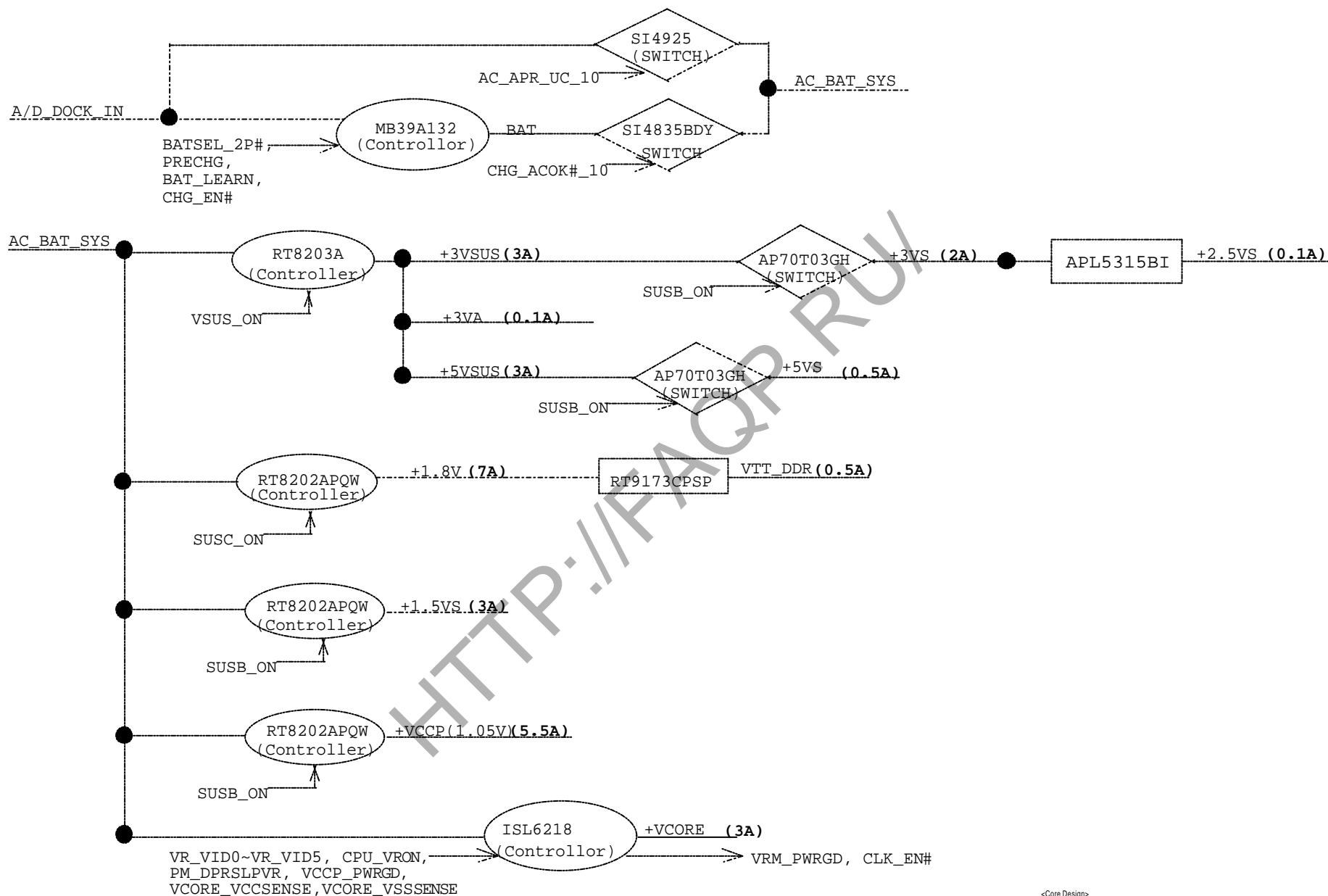


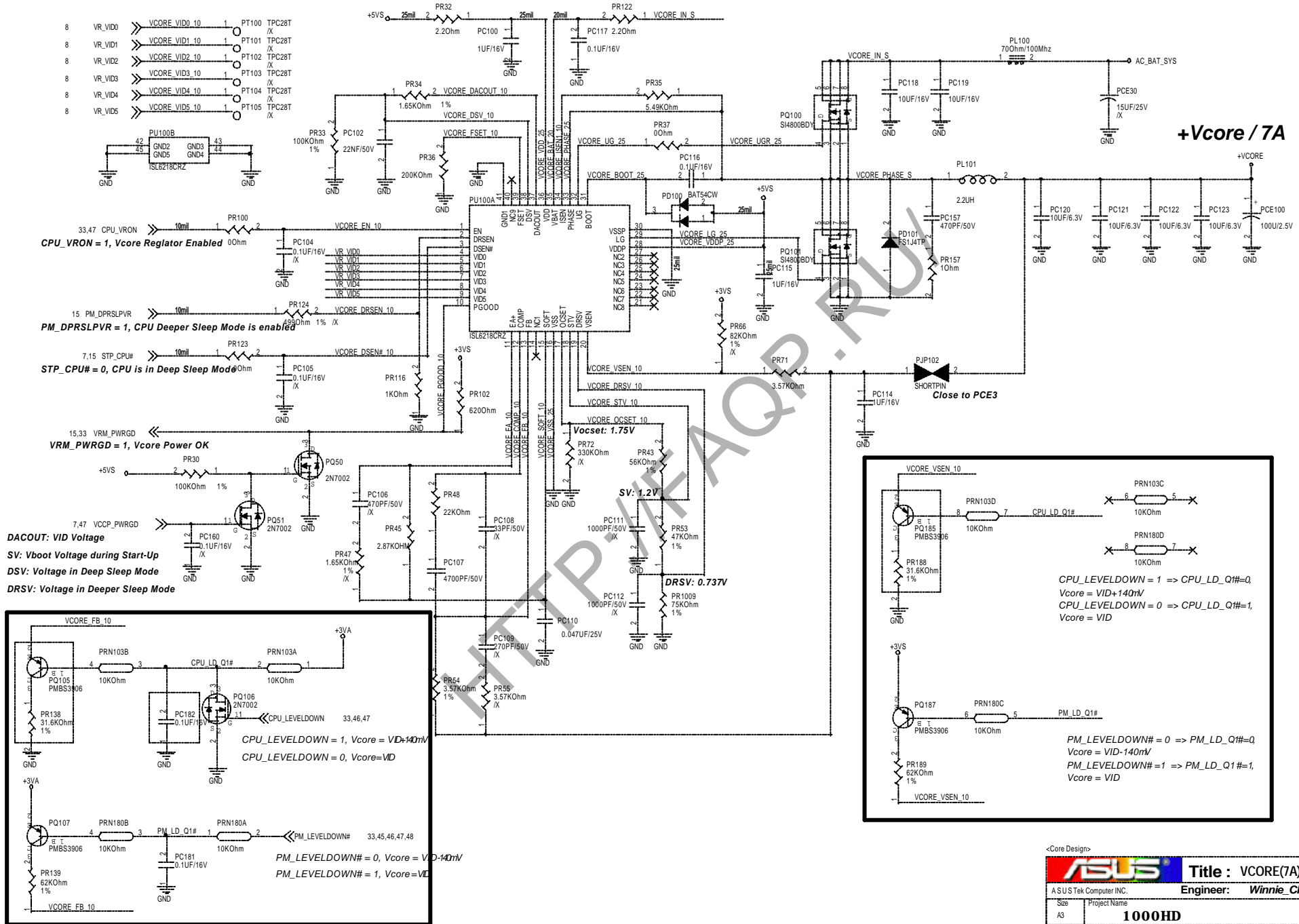


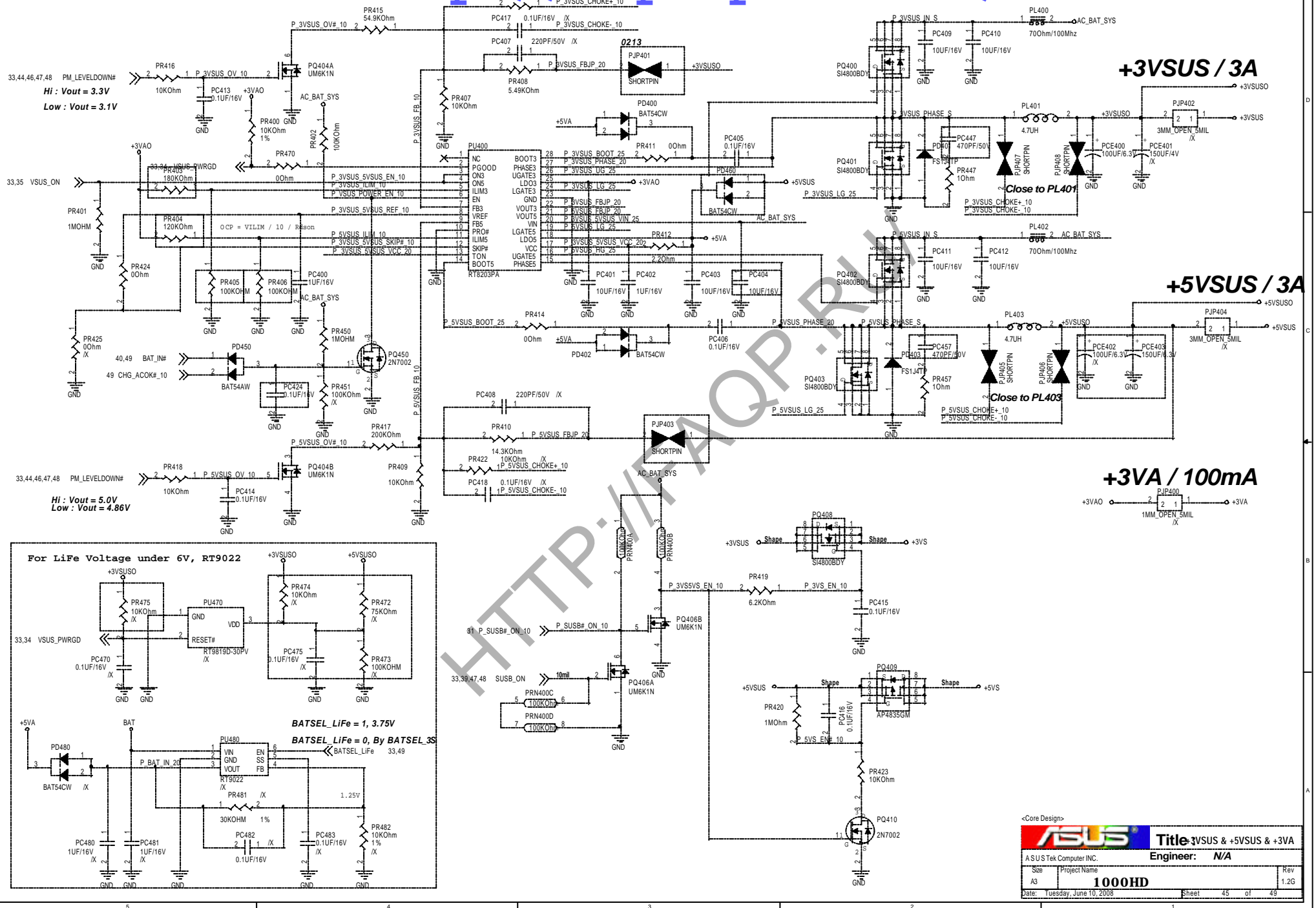
<Core Design>

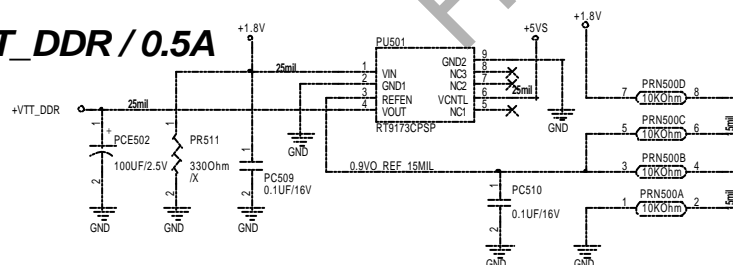
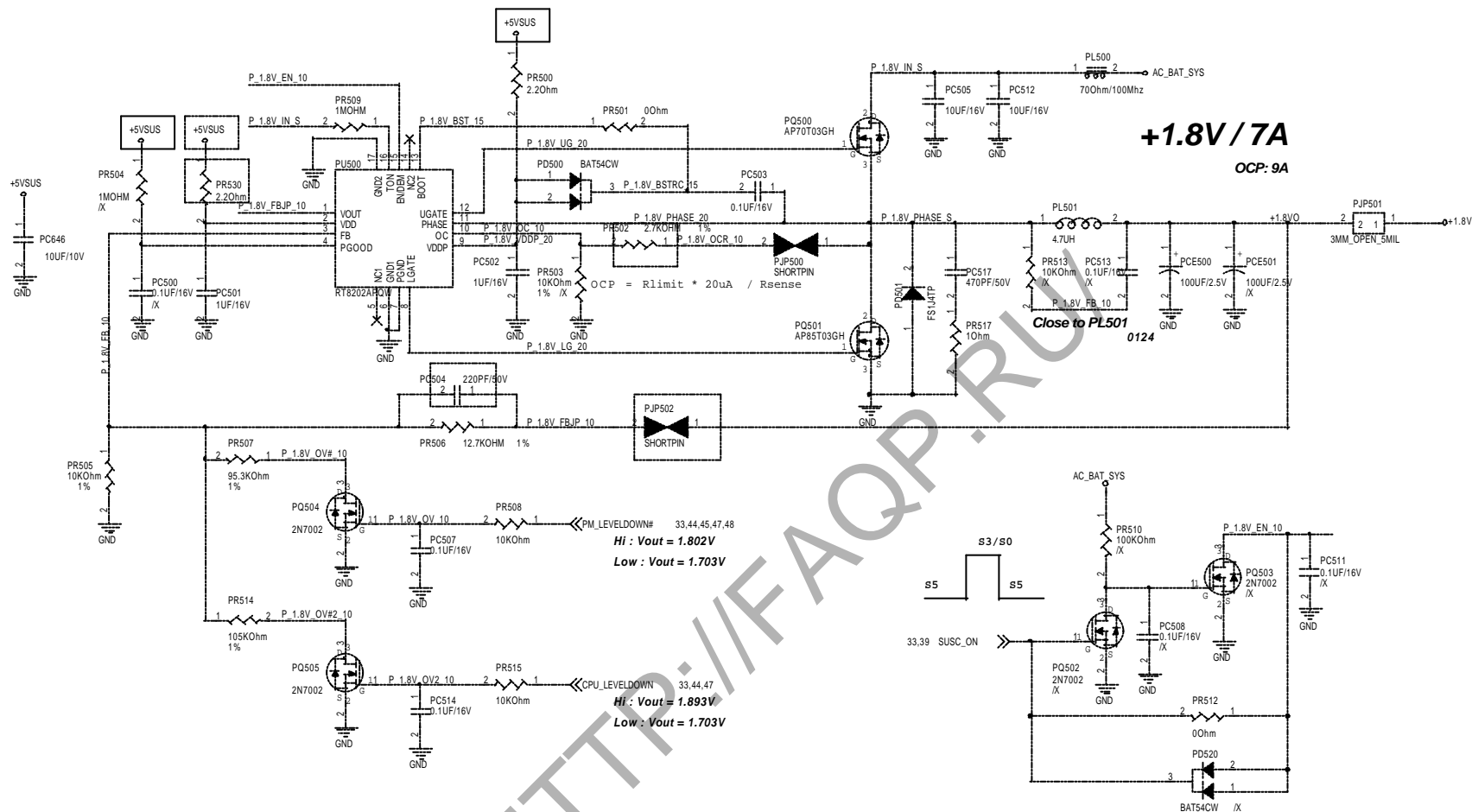
<b>ASUS</b>		<b>Title : Srew Hole</b>	
ASUS Tek Computer INC.		Engineer: <b>Wayne_Chan</b>	
Size	Project Name		Rev
A3	<b>1000HD</b>		1.2G
Date: <b>Tuesday, June 10, 2008</b>		Sheet	41 of 49





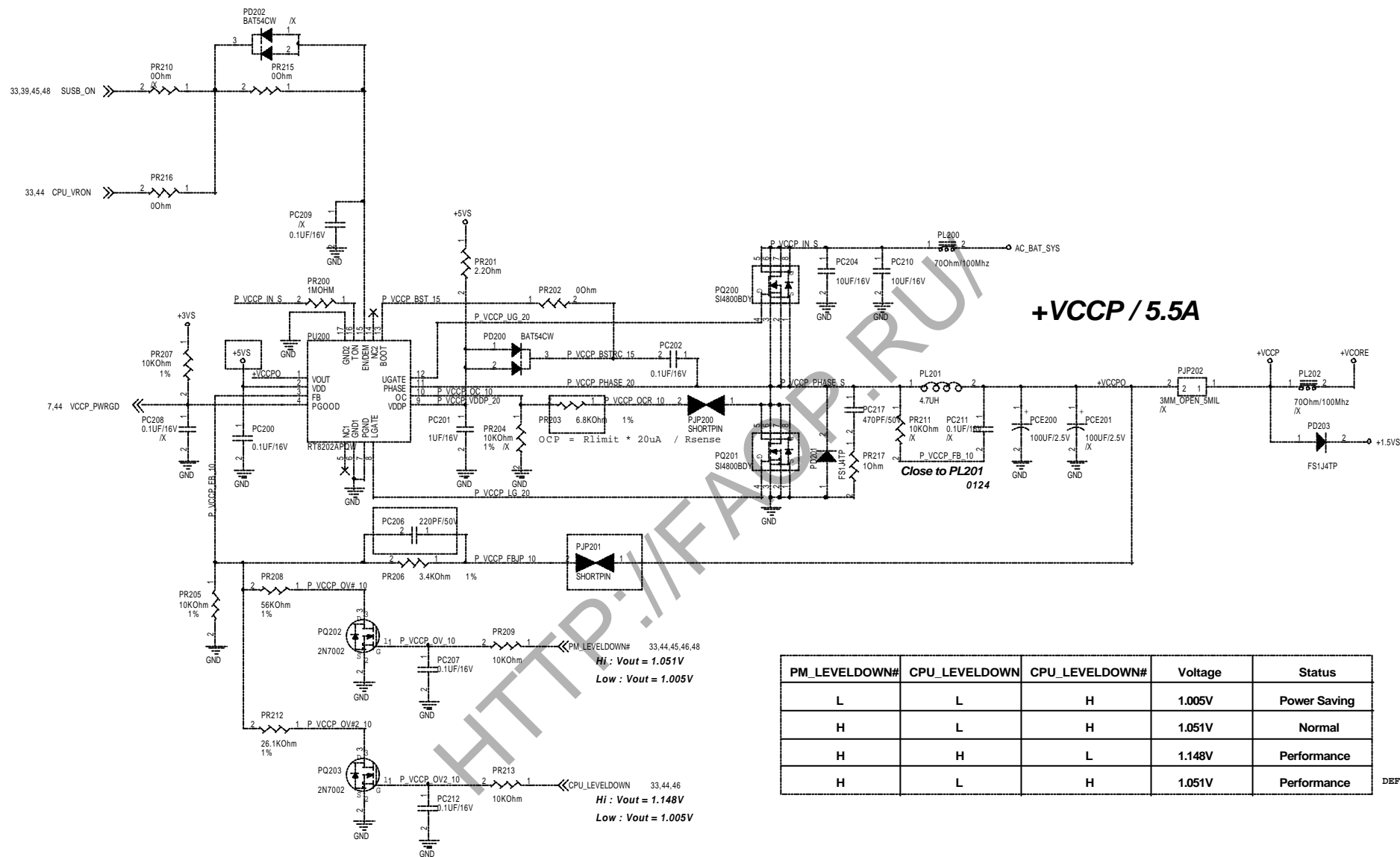






PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.703V	Power Saving
H	L	H	1.802V	Normal
H	H	L	1.893V	Performance
H	L	H	1.802V	Performance

DEFAULT



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.005V	Power Saving
H	L	H	1.051V	Normal
H	H	L	1.148V	Performance
H	L	H	1.051V	Performance

DEFAULT

&lt;Core Design&gt;



**Title :** VCCP

ASUSTek Computer INC.

Engineer: Joy\_Zhou

Size
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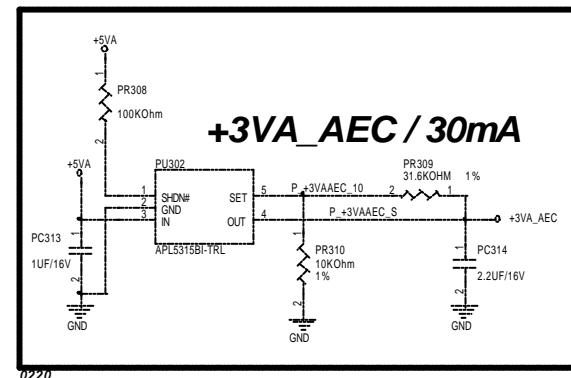
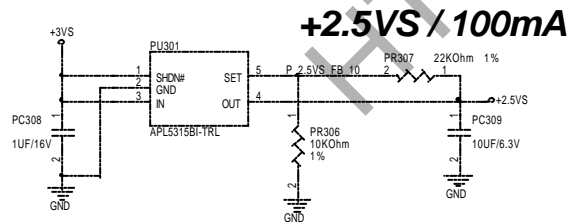
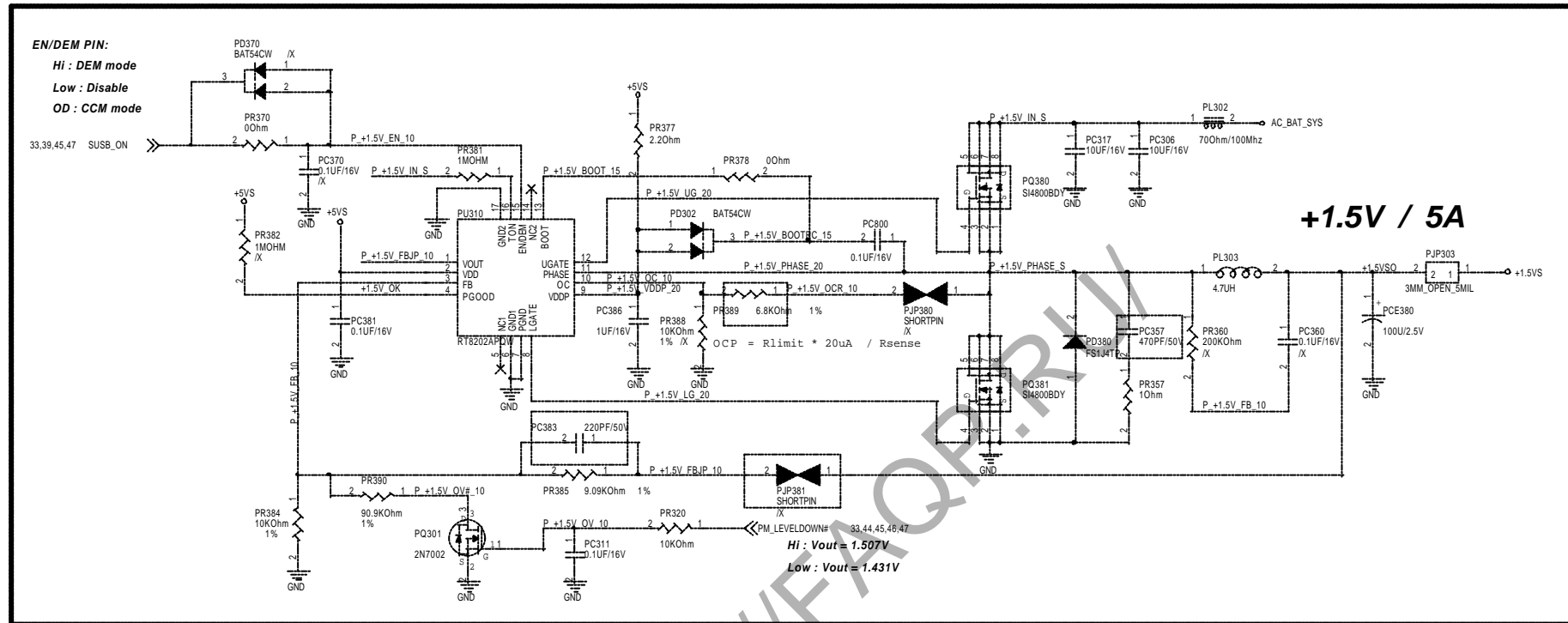
Project Name	
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**1000HD**

Rev  
1.2G

Date: Tuesday, June 10, 2008

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<Core Design>

<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUS Tek Computer INC.		Engineer: <b>Joy Zhou</b>	
Size	Project Name	Rev	
A3	<b>1000HD</b>	1.2G	
Date: Tuesday, June 10, 2008		Sheet	48 of 49



