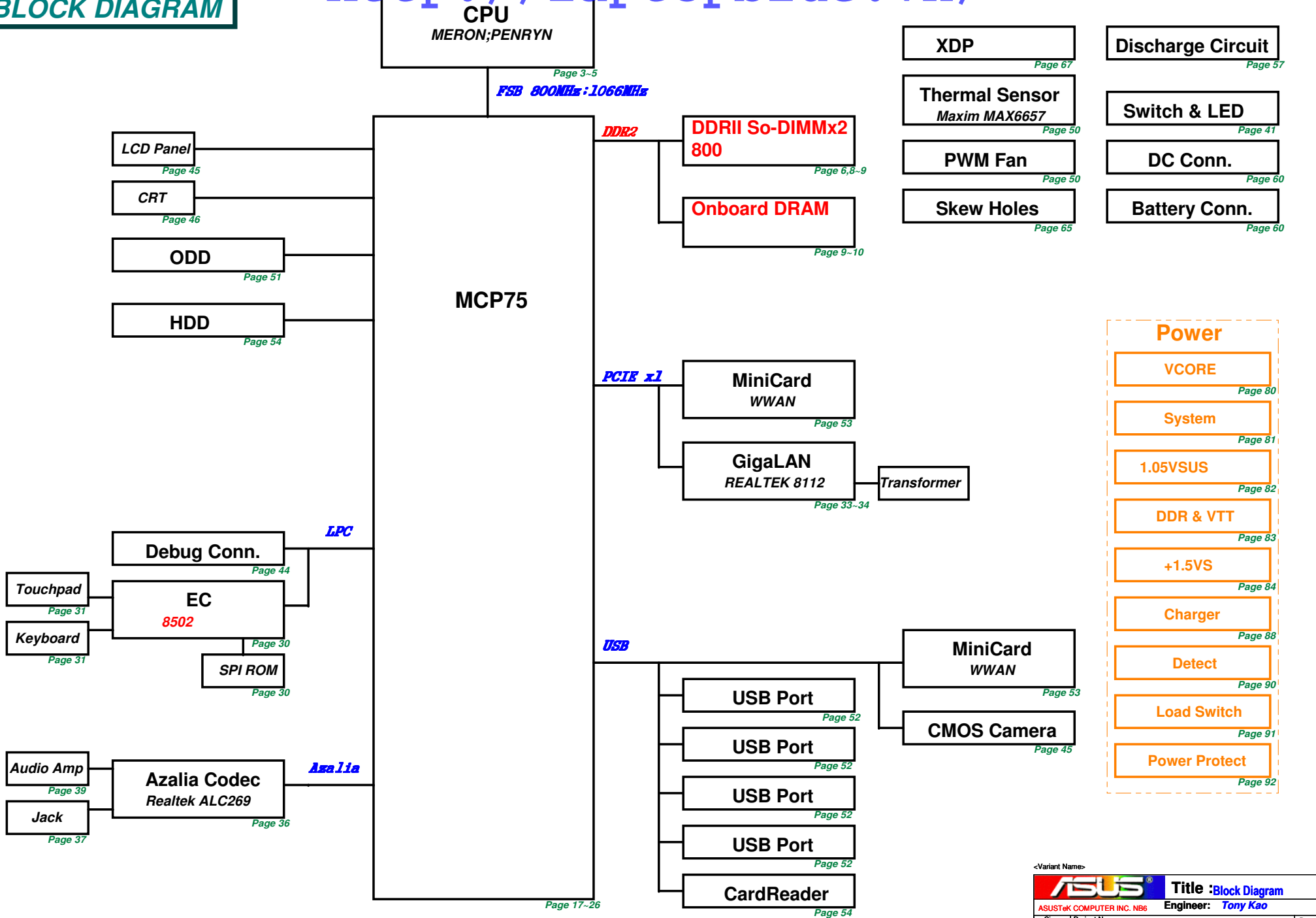


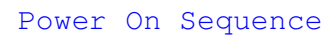
# K40IN BLOCK DIAGRAM

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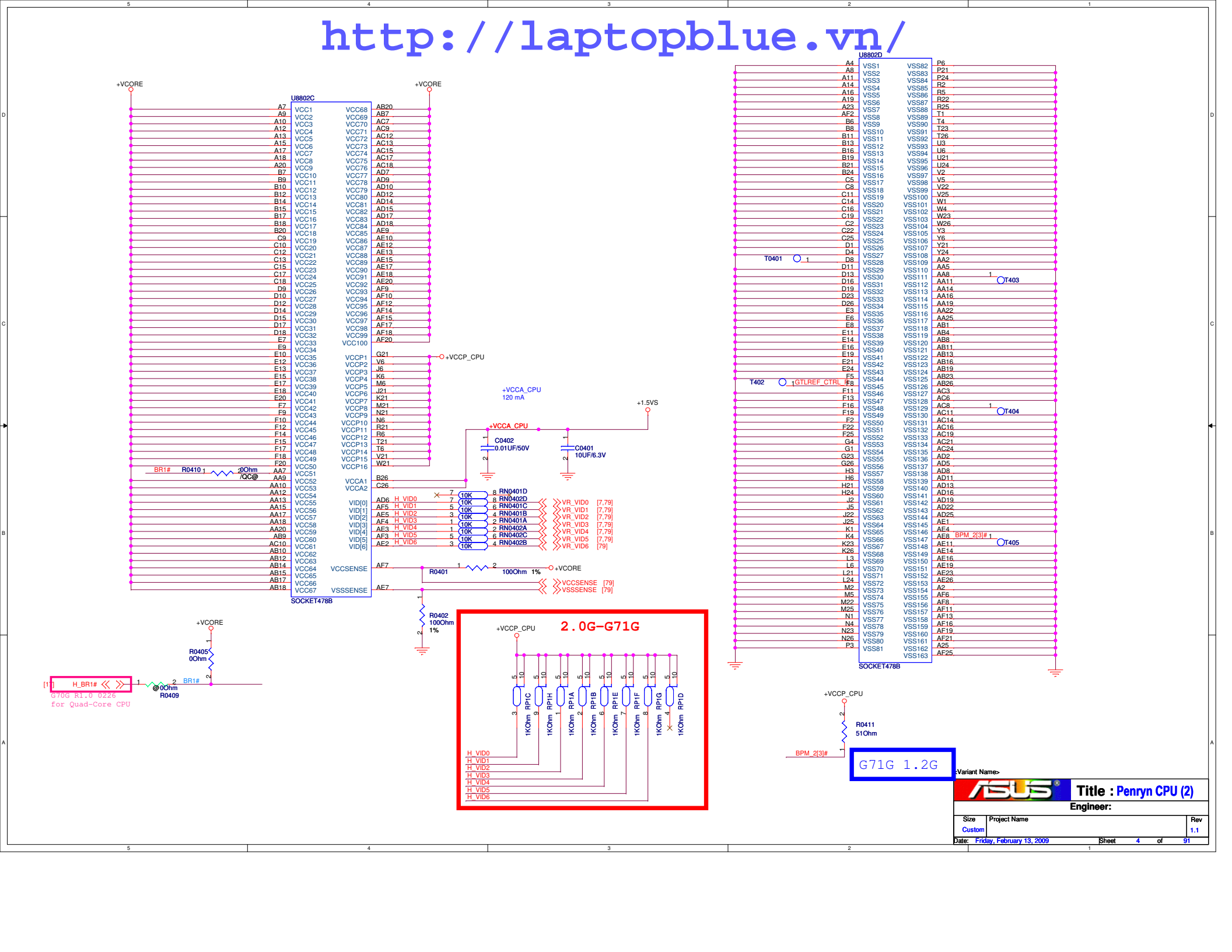
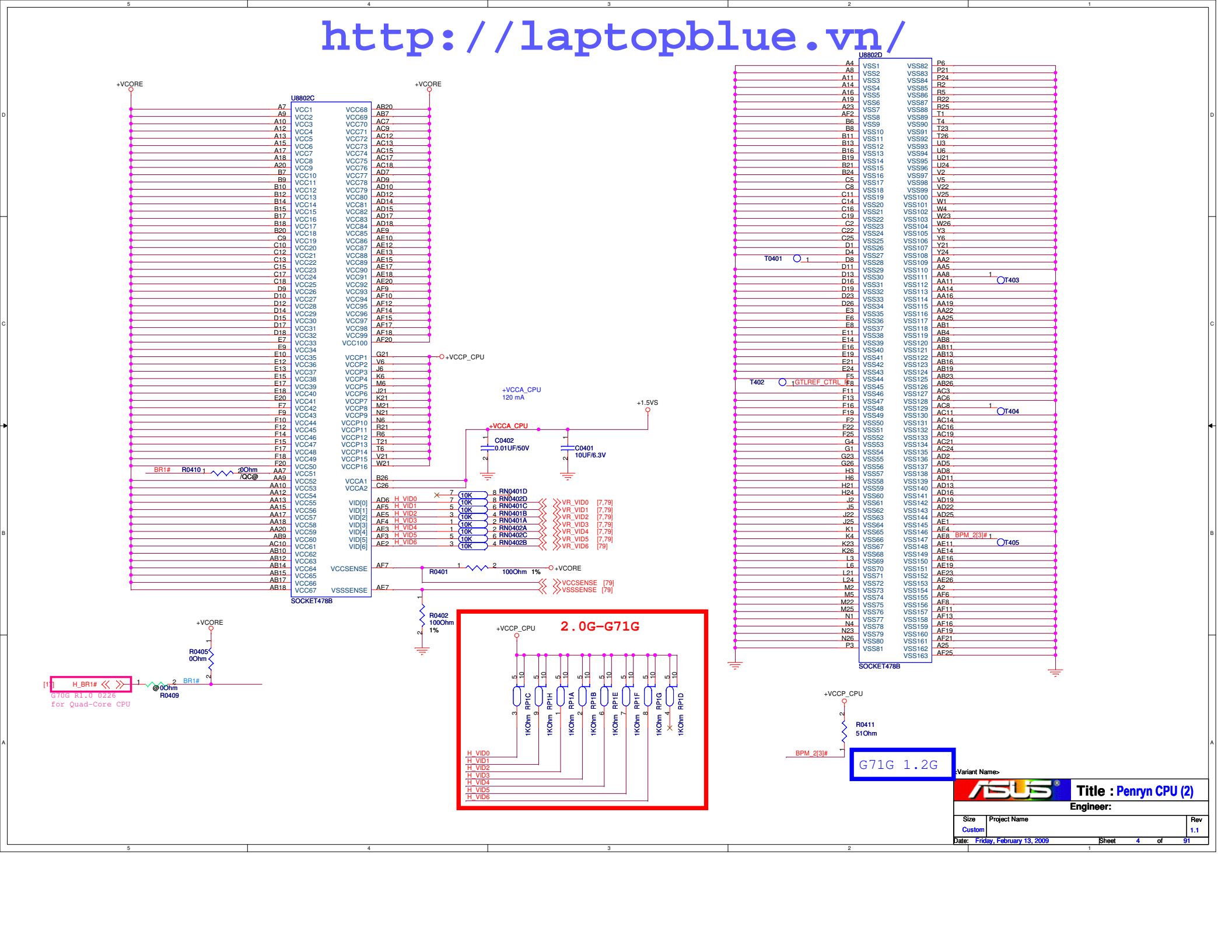
<Variant Name>

		<b>Title :</b> Block Diagram	
ASUSTeK COMPUTER INC. NBS		<b>Engineer:</b> <i>Tony Kao</i>	
Size Custom	Project Name <b>G71G</b>		Rev 1.0
Date: Friday, February 13, 2009		Sheet	1 of 91

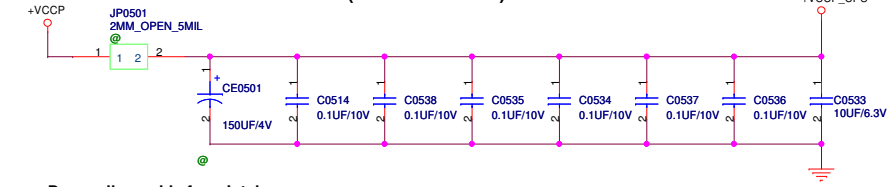
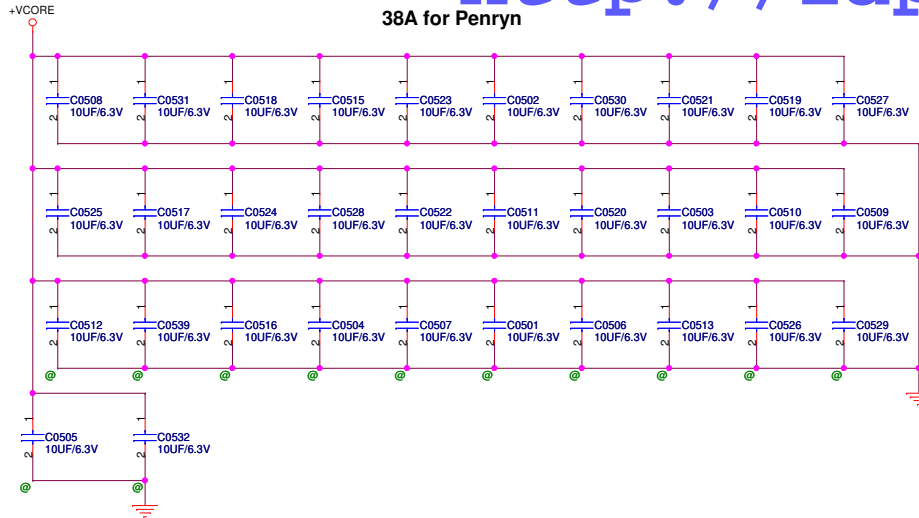


① → ②②





## 38A for Penryn



### Decoupling guide from Intel

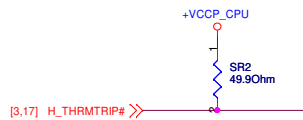
VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

### +V CORE Mid-Frequency Capacitor

Intel: 22uF \*32  
F3S: 10uF \*16  
A7S: 10uF \*10 ....11/17  
V1V: ?

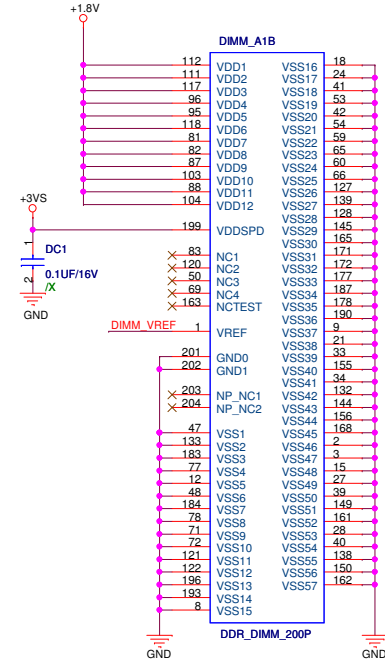
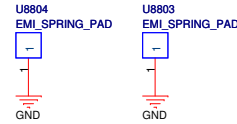
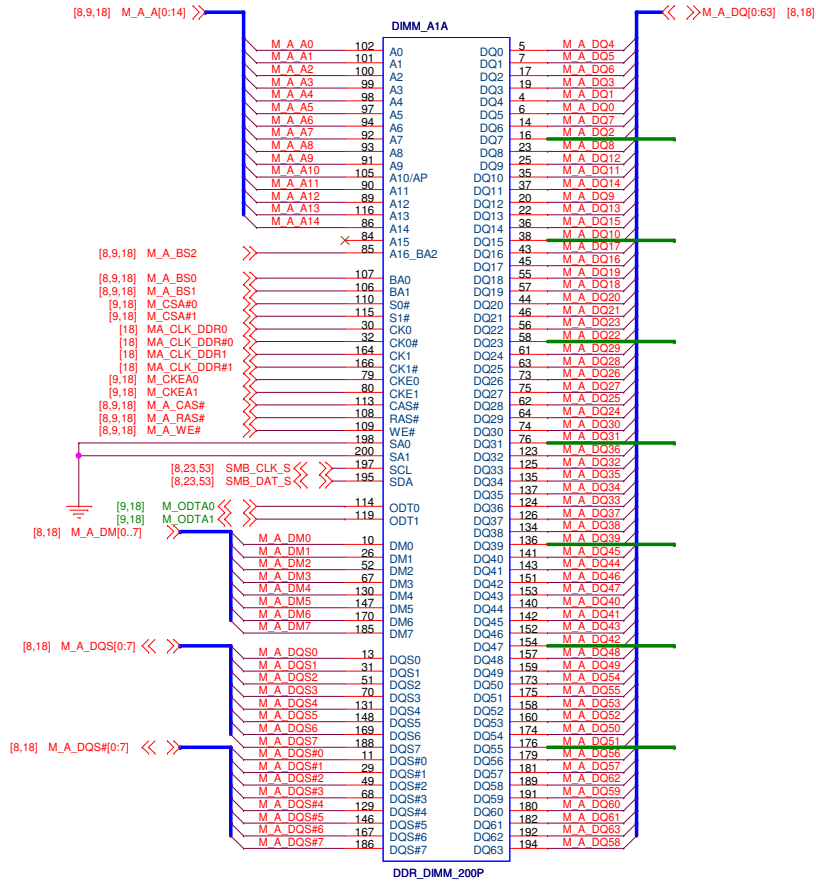
### +VCCP Decoupling Capacitor

Intel: 270uF \*1, 0.1uF \*6  
F3S: 100uF \*1, 0.1uF \*4  
V1V: ?

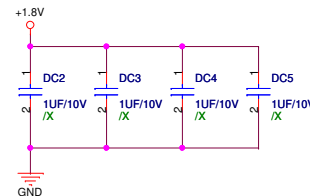


<Variant Name>

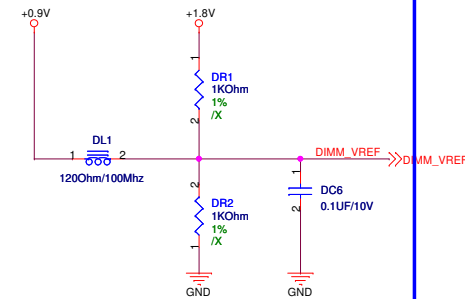
<b>ASUS</b>		<b>Title : CPU CAPS</b>	
		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009	Sheet	5	of 91



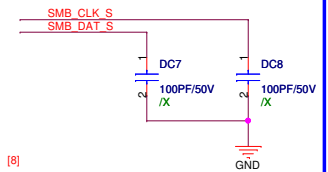
Power Cap Close to DIMM



DIMM\_VREF Close to DIMM



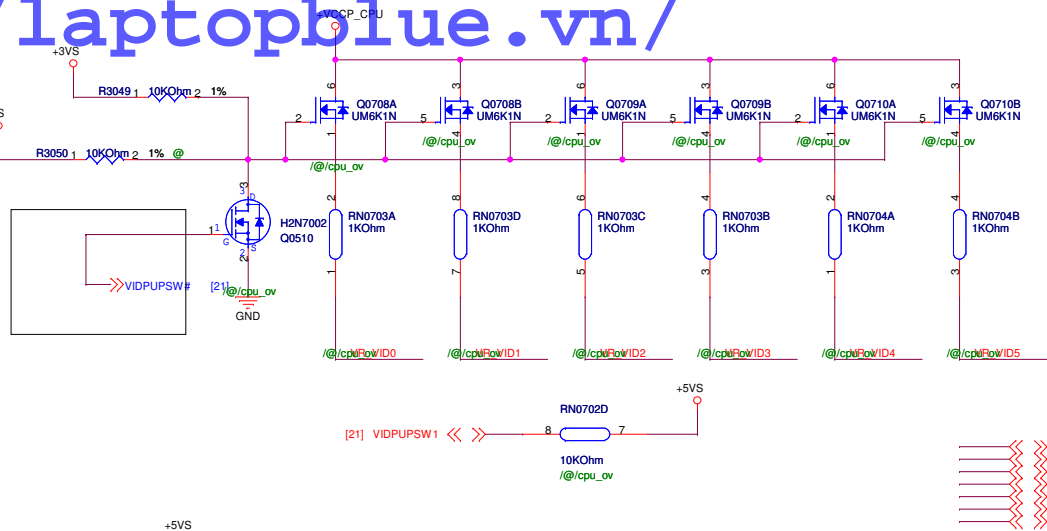
Close to DIMM



<Variant Name>

<b>ASUS</b>		<b>Title :</b>
ASUSTek COMPUTER INC. NB6		<b>Engineer:</b>
Size A3	Project Name	Rev 1.0
Date: Friday, February 13, 2009	Sheet 6	of 91

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		<b>Title</b> <u>DDR3 SO-DIMM_0</u>	
<b>ASUSTek COMPUTER INC. N86</b>		<b>Engineer:</b> <u>Vincent Chung</u>	
<b>Size</b> Custom	<b>Project Name</b> <u>G71V</u>		<b>Rev</b> 1.0
<b>Date:</b> <u>Friday, February 13, 2009</u>		<b>Sheet</b> <u>7</u>	<b>of</b> <u>91</u>

10

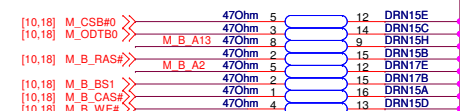
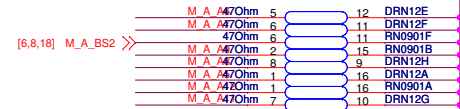
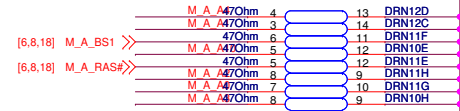
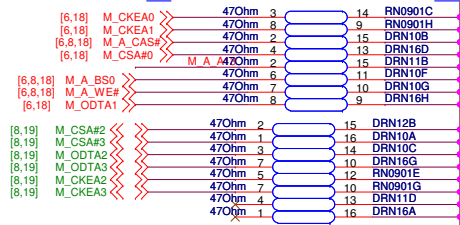




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—<< >>M\_A\_A[0:14] [6,8,18]

—<< >>M\_B\_A[0:14] [10,18]



DC14  
0.1UF/10V

DC16  
0.1UF/10V

DC11  
0.1UF/10V

DC12  
0.1UF/10V

DC13  
0.1UF/10V

DC15  
0.1UF/10V

DC17  
0.1UF/10V

DC18  
0.1UF/10V

GND


<Variant Name>

<b>ASUS</b>		<b>Title DDR3 termination</b>	
ASUSTek COMPUTER INC. NB6		Engineer: <b>Vincent Chung</b>	
Size Custom	Project Name <b>G71V</b>	Rev 1.0	
Date: Monday, February 16, 2009		Sheet 9	of 91



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<Variant Name>

		<b>Title :</b> Cantiga-DDR3/PEG(2)	
<b>Engineer:</b>			
Size	Project Name		Rev
C			1.0
Date: Friday, February 13, 2009		Sheet	11 of 91

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<Variant Name>			
		Title : Cantiga-POWER(5)	
Engineer:			
Size	Project Name		Rev
Custom			1.0
Date: Friday, February 13, 2009	Sheet	14	of 91

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<Variant Name>



Title : Cantiga-GND

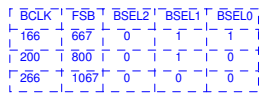
Engineer:

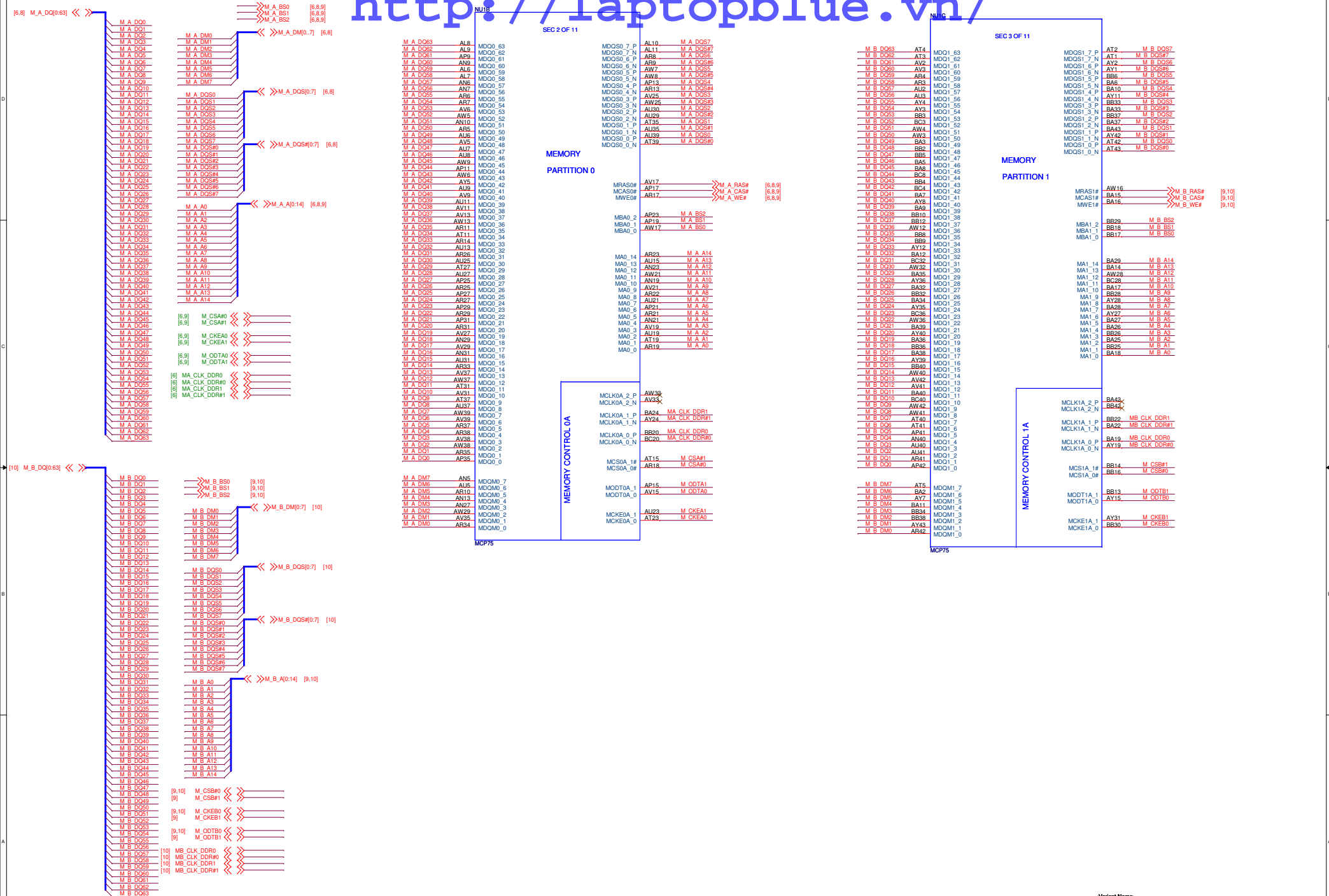
Size B	Project Name	Rev 1.0
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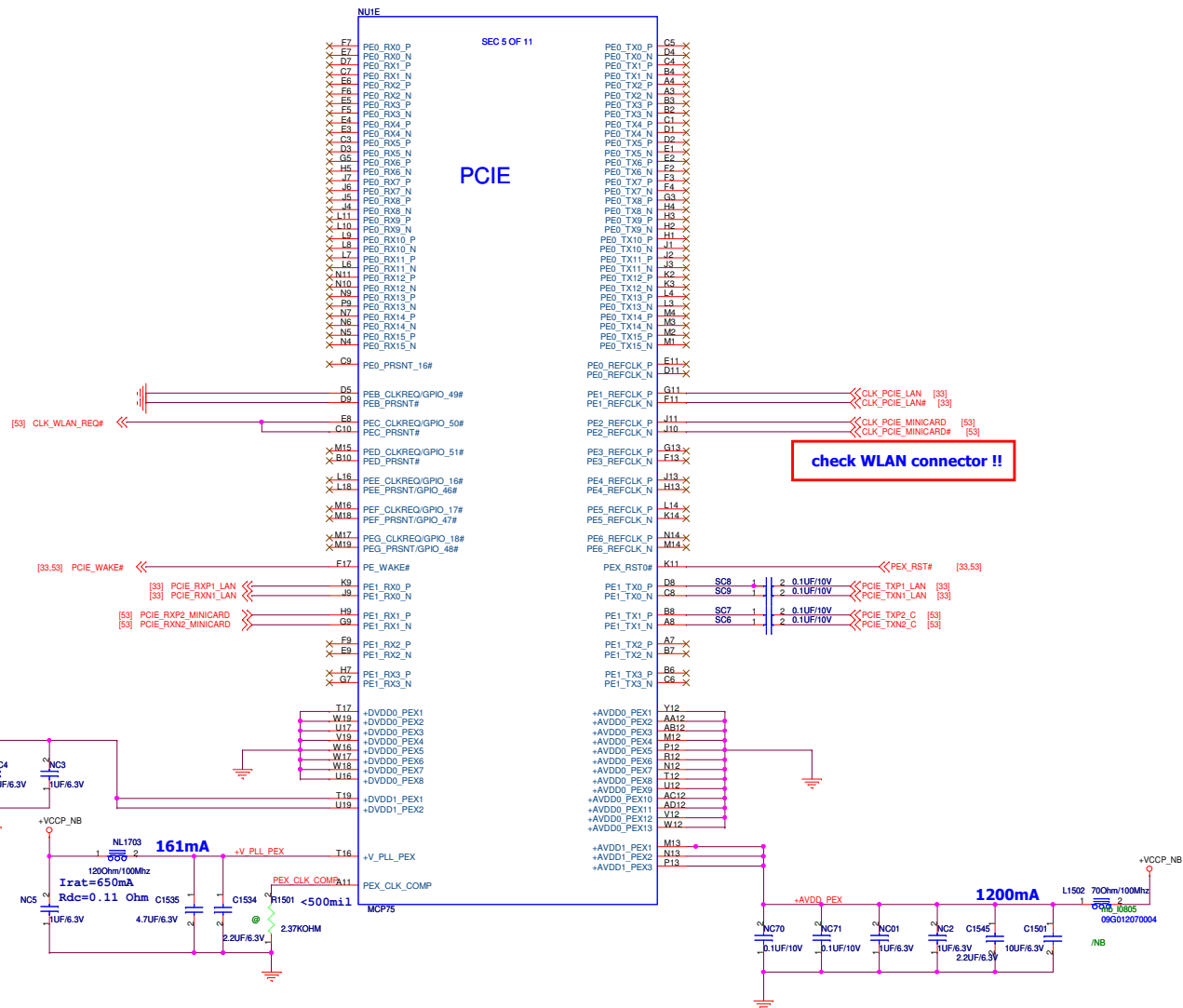
http://laptopblue.vn/

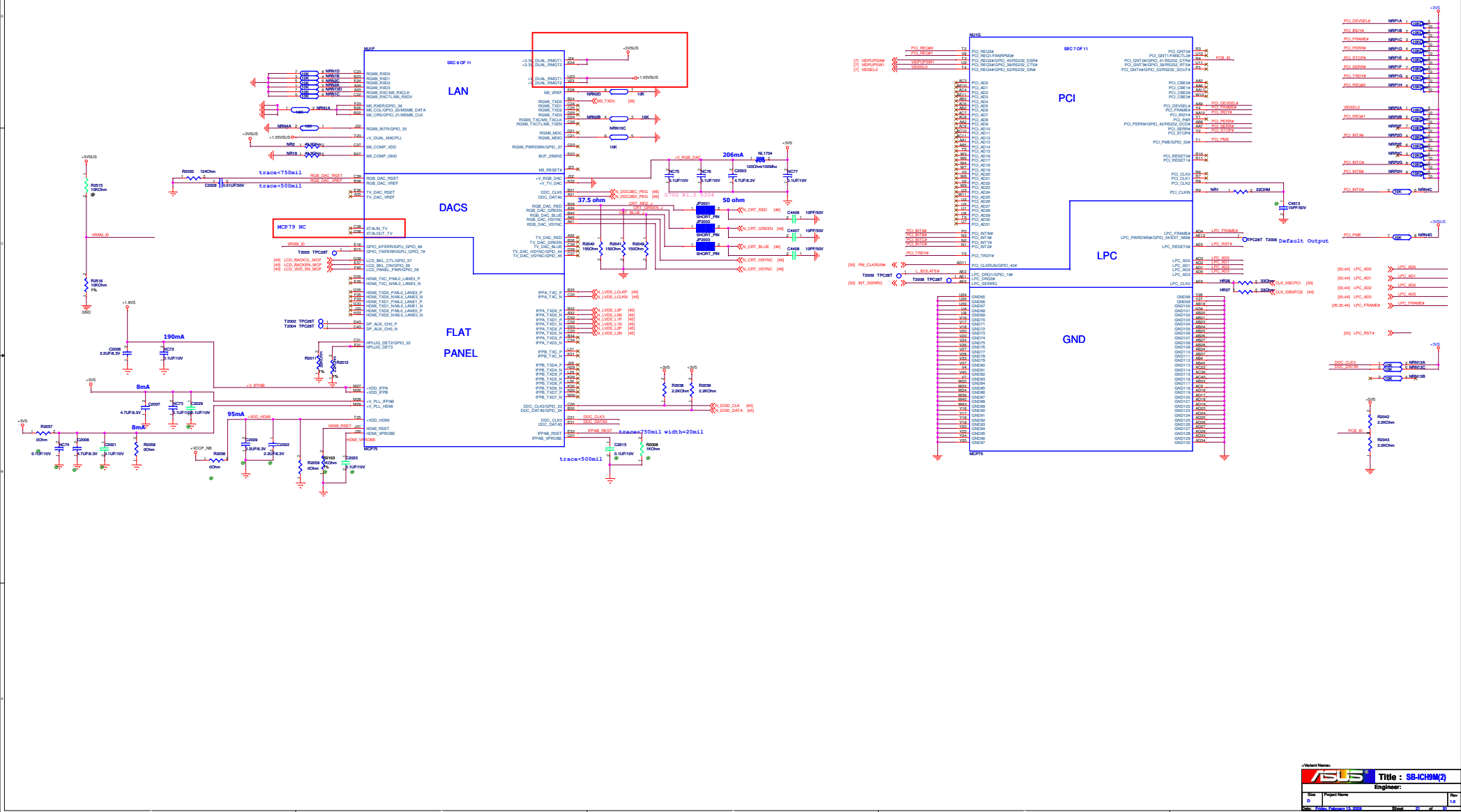




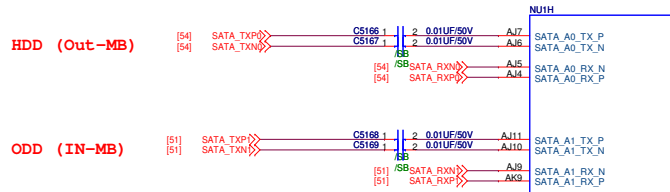


		<b>Title :</b>	
<b>Engineer:</b>			
<b>Size</b> C	<b>Project Name</b>		<b>Rev</b> 1.0
<b>Date:</b> Friday, February 13, 2009		<b>Sheet</b> 19	<b>of</b> 91





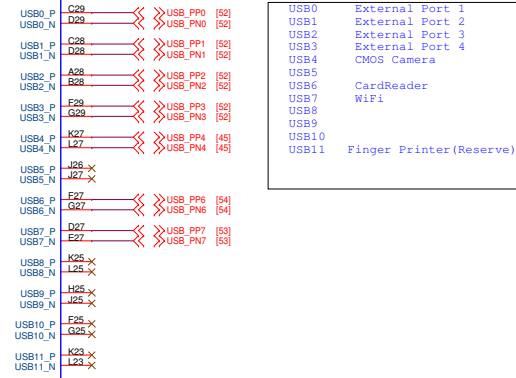
Check connector pin definition !!



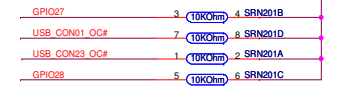
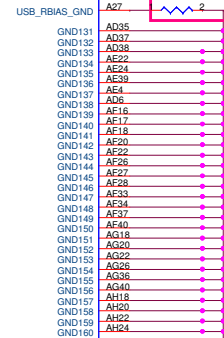
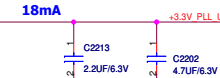
SATA

USB

Check connector pin definition !!



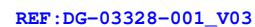
USB\_OC2/GPIO\_25# <--> L21 <--> USB\_CON01\_OC# [52]  
USB\_OC1/GPIO\_26# <--> K21 <--> USB\_CON01\_OC# [52]  
USB\_OC2/GPIO\_27/MG3PIC# <--> J21 <--> GPIO27  
USB\_OC3/GPIO\_28/MG3PIC# <--> H21 <--> GPIO28



<Variant Name>



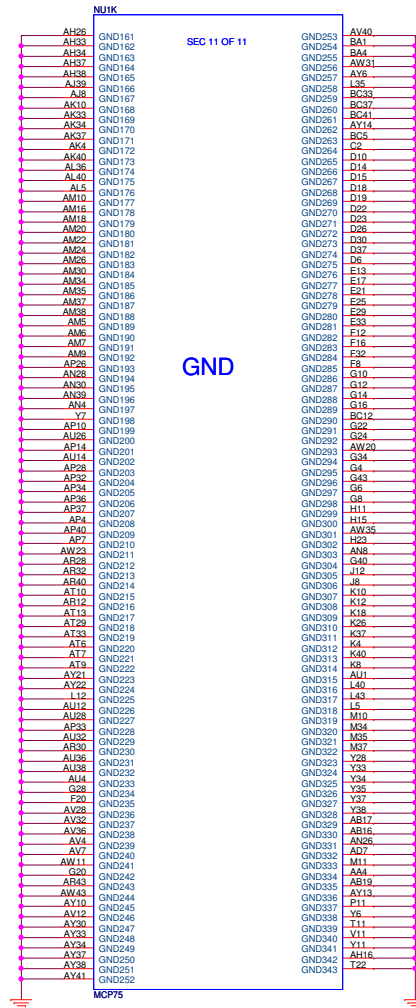
NU1J



<b>+MCP_VDD_VID[2:0]</b>	<b>Core Voltage</b>
<b>001</b>	<b>1</b>
<b>010</b>	<b>0.95</b>
<b>011</b>	<b>0.9</b>



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<Variant Name>

		<b>Title : SPI ROM</b>	
<b>Engineer:</b>			
Size	Project Name	Rev	
C		1.0	
Date: Friday, February 13, 2009		Sheet	25 of 91

[6.8,23.53] SCL\_3A << >> SMB\_CLK\_S [6.8,23.53]

[6.8,23.53] SDA\_3A << >> SMB\_DAT\_S [6.8,23.53]

Onboard DRAM ID

GPIO_6	GPIO_11	Vendor
0	0	Qimonda HYB18T512161B2F-25
0	1	Samsung K4N51163Q2-NC25
1	0	Hynix HY5PS121621CFP-25

HDA\_SYNC STRAP (BUF\_SIO\_CLK)

0	14.318MHz (default)
1	24MHz

RGMII\_TXD0

0	MII
1	RGMII

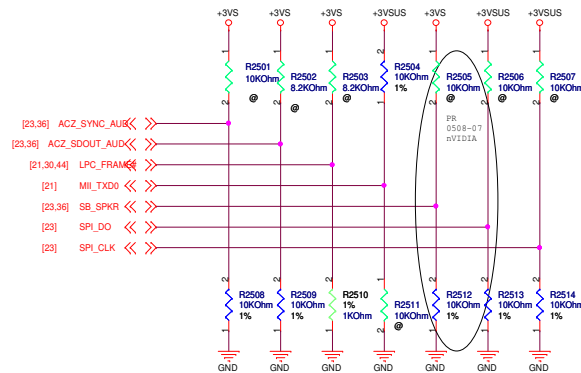
SPKR

0	User mode boot Init table
1	Safe mode boot Init table

Base on EC

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz



<Variant Name>

ASUS		Title :
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Monday, February 16, 2009		Sheet 26 of 31

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<Variant Name>



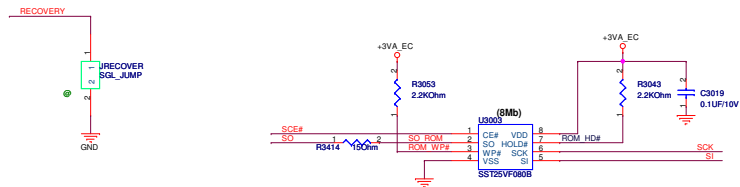
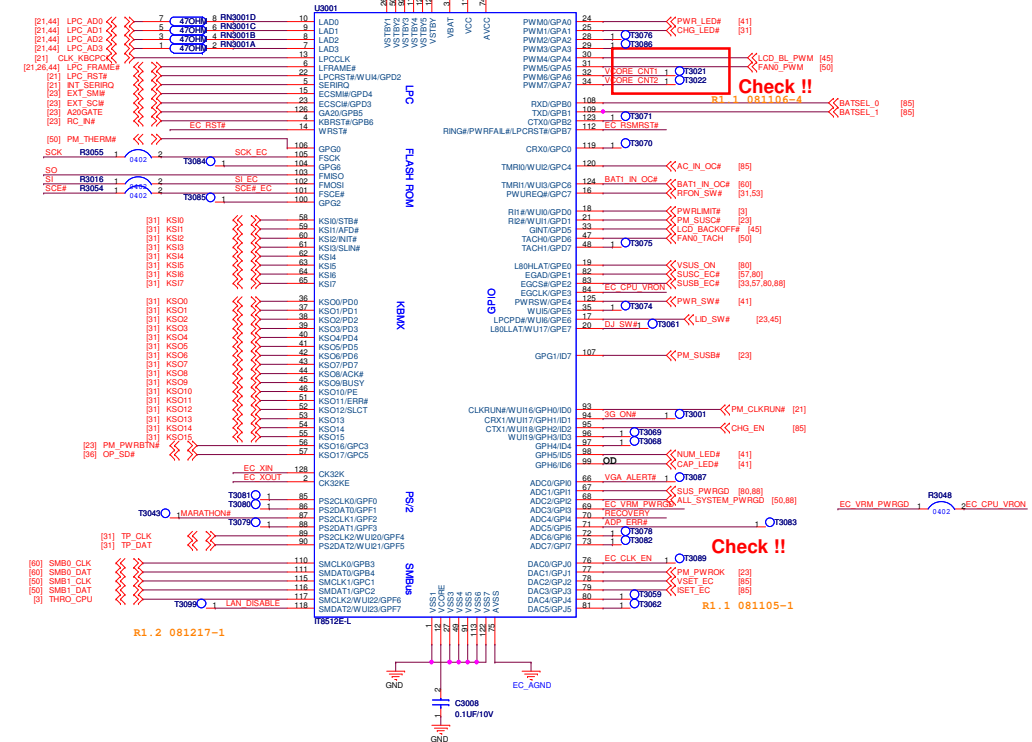
**Title :** Main Clock-2

ASUSTek Computer Inc.

**Engineer:** Tony Kao

Size	Project Name	Rev
A2	C90P	1.00

Date: Friday, February 13, 2009 Sheet 29 of 91



The schematic diagram illustrates the power supply circuit. It features a +3VA input connected to a 1.3001 1200MHz/100Mhz oscillator and a 500 resistor. The output is +3VA EC. A JP3001 connector is connected to ground (EC\_AGND). A +3V input is connected to a JP3002 connector, which is also connected to a +3VACC output. Various capacitors (C3003, C3004, C3005, C3006, C3007, C3002, C3001) are connected to ground (EC\_AGND).

**+3V<sub>A</sub> EC**

R3002 1 4 2 4.7KOhm SMB0\_CLK  
R3006 1 4 2 4.7KOhm SMB0\_DAT

R3020 1 X0P06 2 1% AC\_B1\_OCF  
R3021 1 X0P06 2 1% BAT1\_IN\_OCF  
R3027 1 X0P06 2 1% LID\_SW#  
R3029 1 X0P06 2 1% PWR\_SW#

**+5VUS**

R3051 1 2 2 10KOhm PM\_PWRNRN#  
R3052 1 X0P06 2 1% EXT\_SWR#

**+5VS**

R3035 1 X0P06 2 1% V<sub>REG</sub>  
R3036 1 X0P06 2 1% V<sub>REG</sub>

R3004 1 4 2 4.7KOhm SMB1\_CLK  
R3008 1 4 2 4.7KOhm SMB1\_DAT  
R3008 1 4 2 4.7KOhm PM\_CLK#  
R3002 1 X0P06 2 1% PM\_CLKR#

Note: Close to EC

R1.1 081028-1

+3VA\_EC

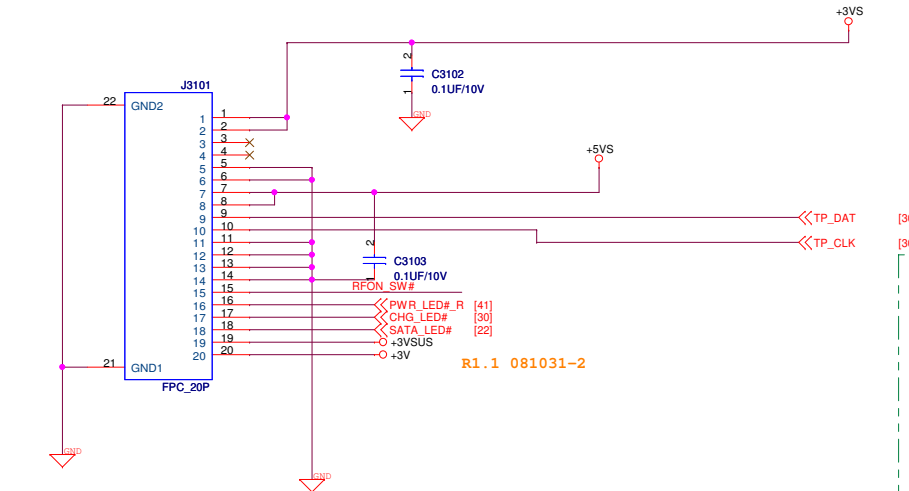
R3039 : 10K Ohm 2 100W RATHON

**I/O Base Address**  
Note: It can be programmable by EC firmware

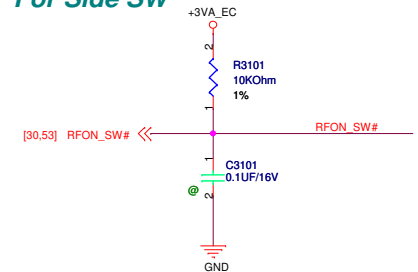
**Share Memory**  
Note: It can be programmable by EC firmware.

**PP Enable**  
Note: Default Int. Pull-Low

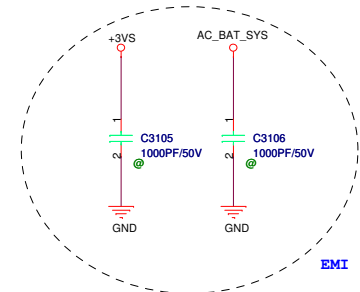
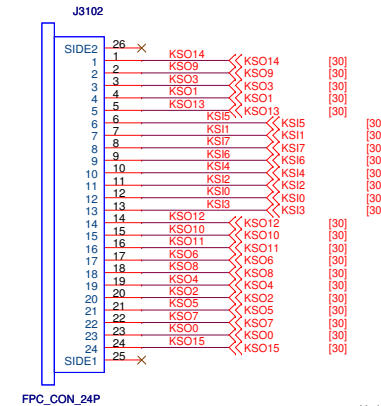
```
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
```



## For Side SW



## Keyboard Connector



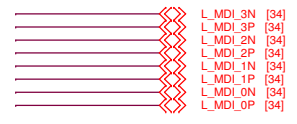
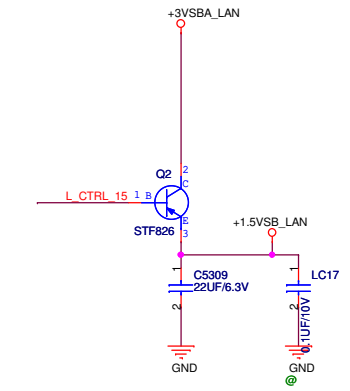
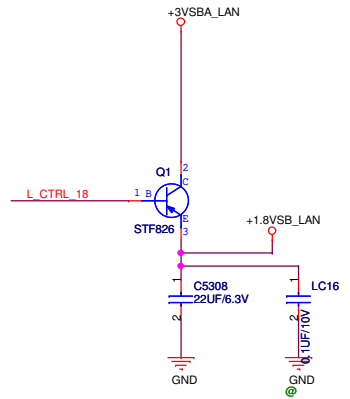
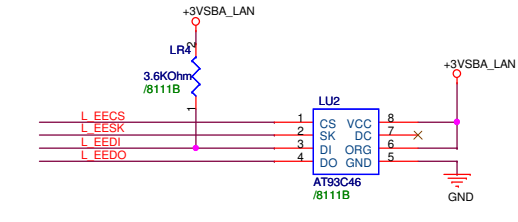
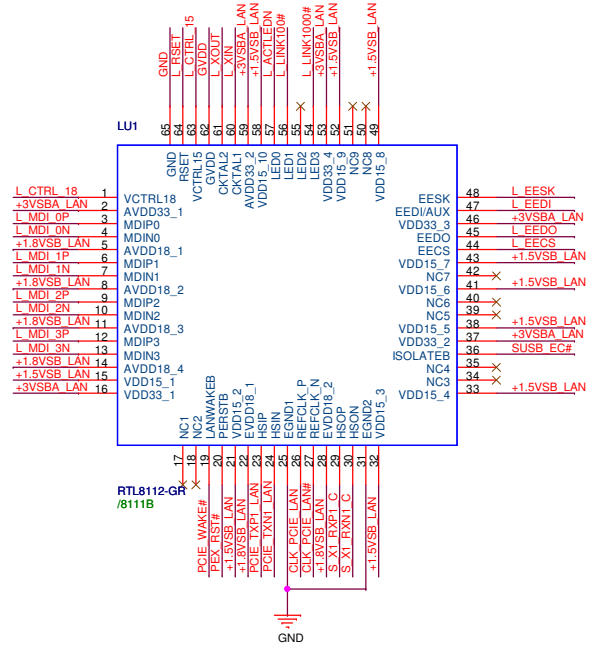
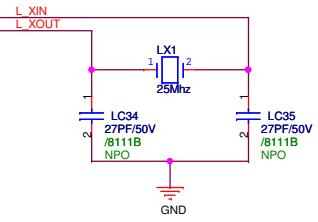
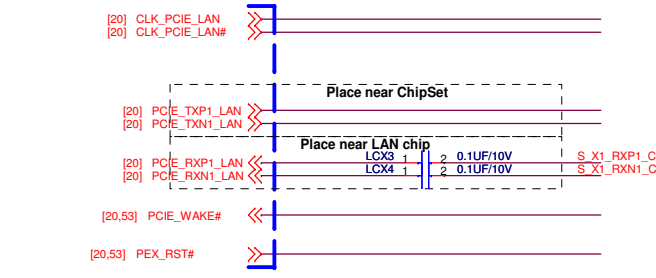
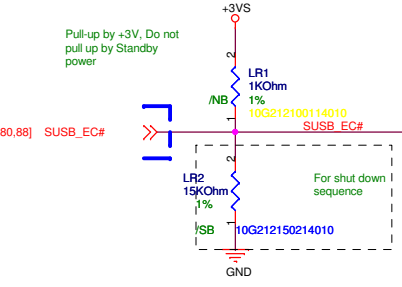
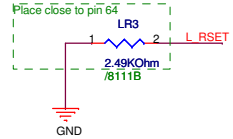
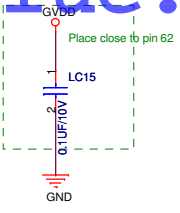
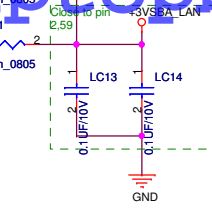
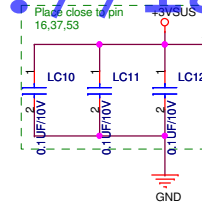
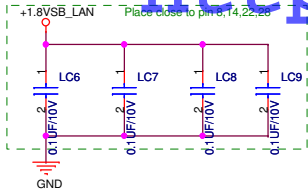
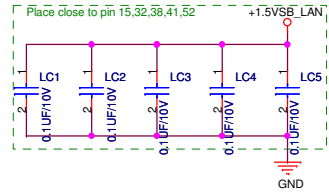
## For Thermal Control Method

Remove redundant components



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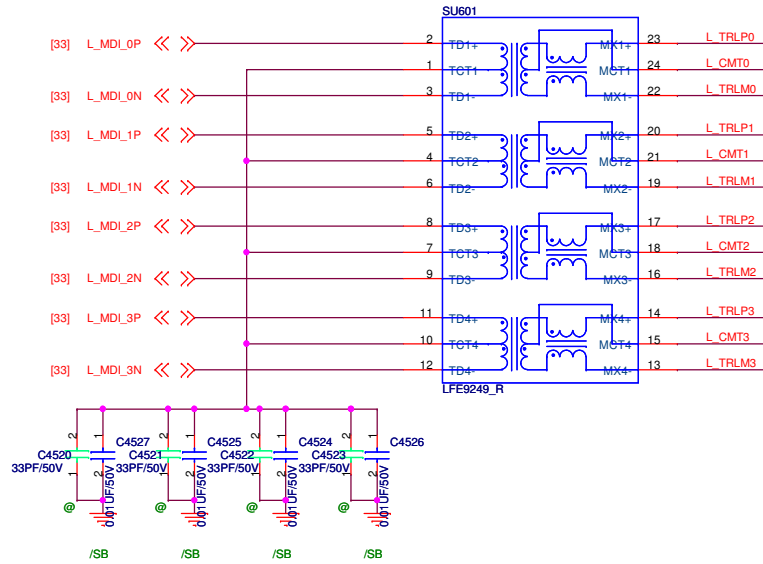
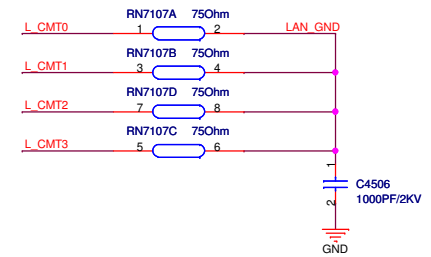




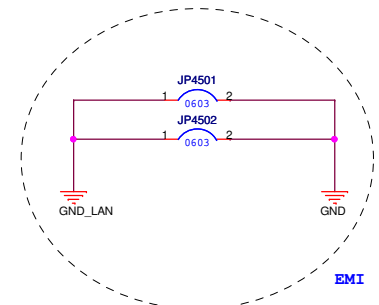
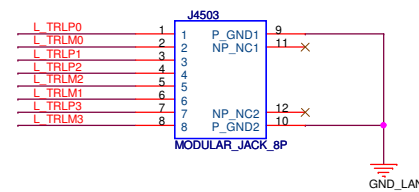
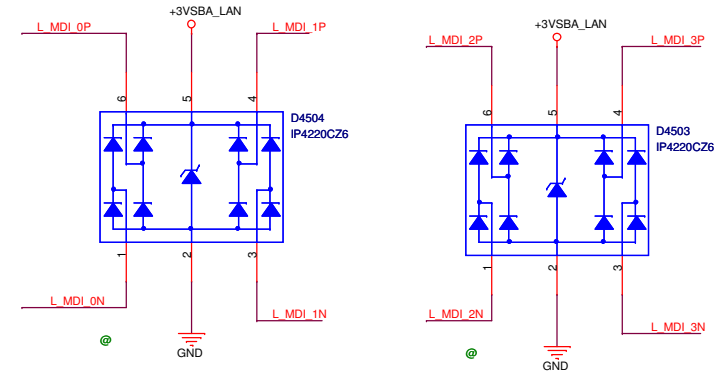
<Variant Name>

<b>ASUS</b>		<b>Title : RST_Reset Circuit</b>	
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung	
Size	Project Name	Rev	
Custom	G71V	1.0	
Date: Friday, February 13, 2009		Sheet	33 of 91

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LAN CONN.




<Variant Name>

<b>ASUS</b>		Title : 10	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009		Sheet	34 of 91

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<Variant Name>



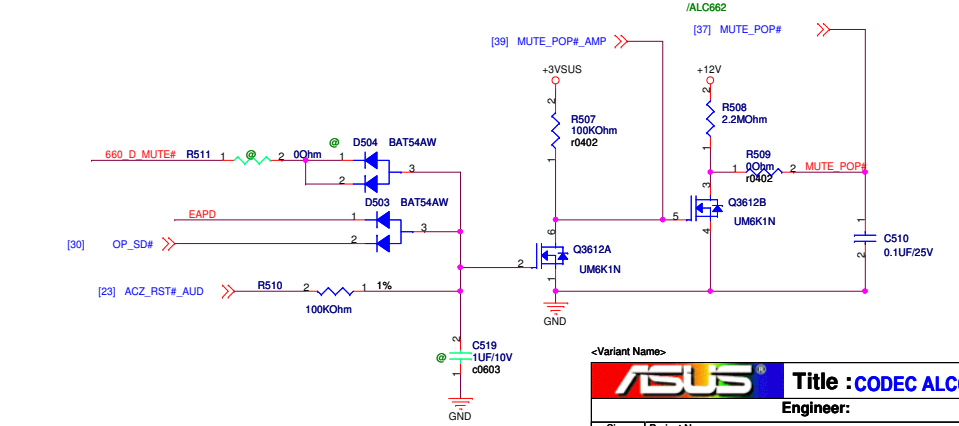
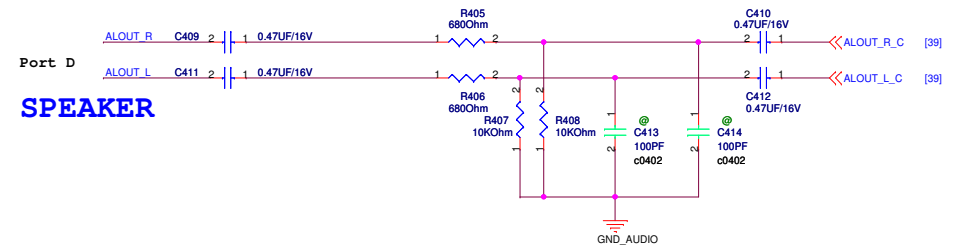
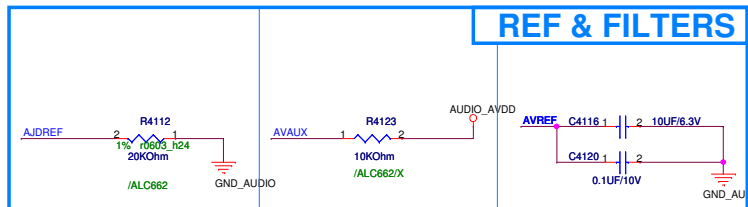
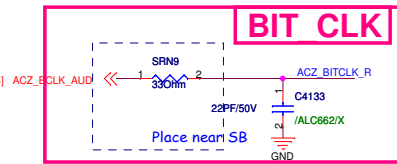
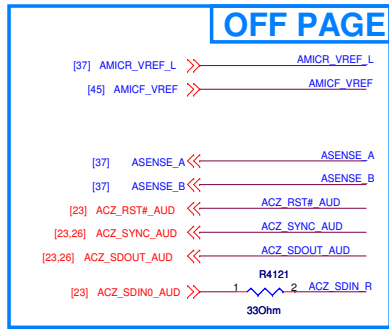
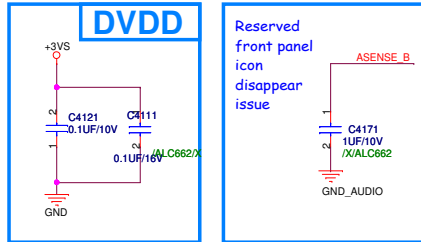
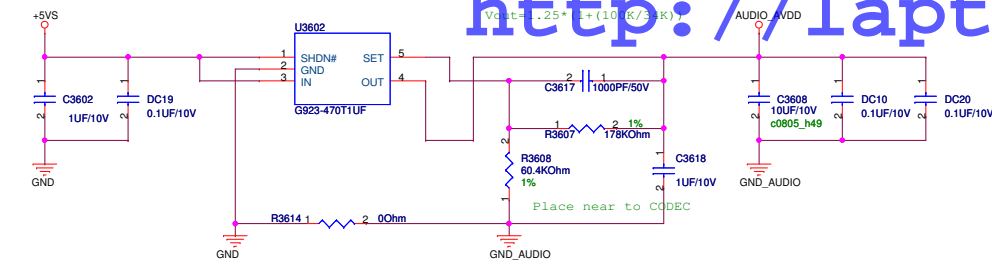
Title : **MDC**

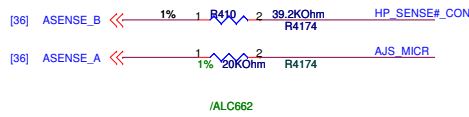
ASUSTeK COMPUTER INC

Engineer: *Vincent Chung*

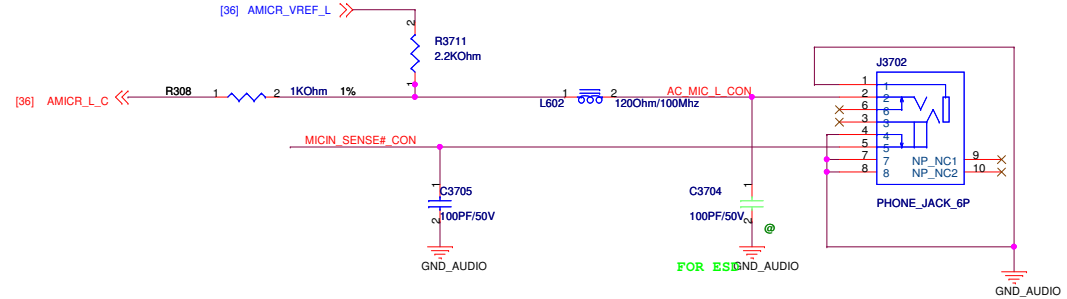
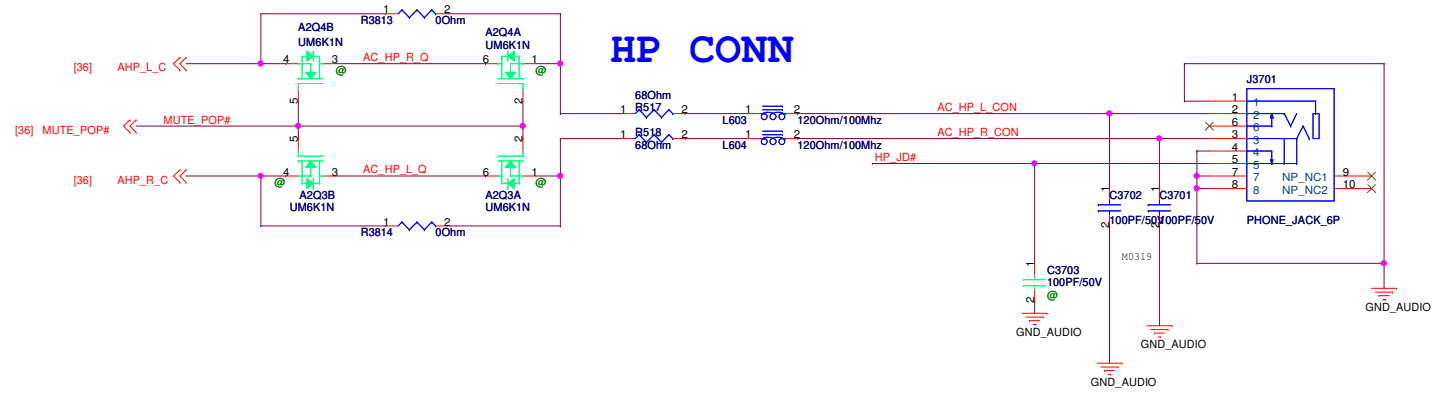
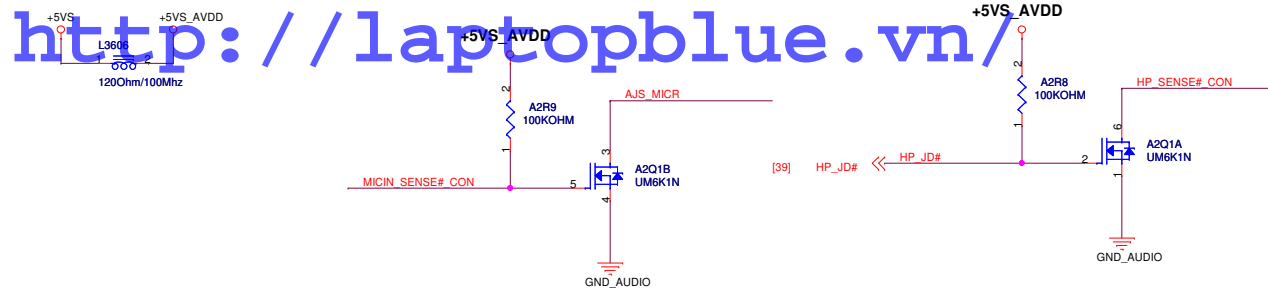
Size	Project Name	Rev
Custom	<b>G71V</b>	1.0

Date: *Friday, February 13, 2009*Sheet 35 of 91





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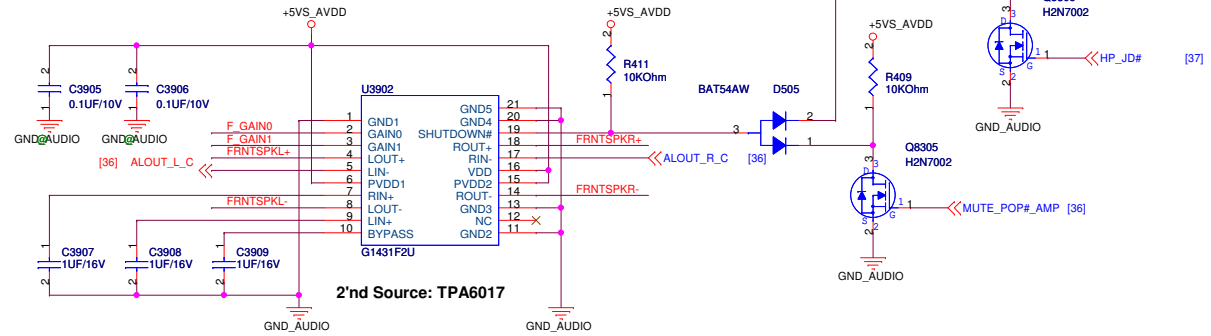
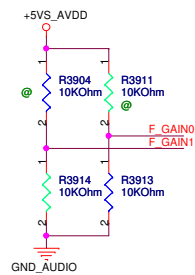
## External MIC CONN

ASUS			Title : AUD_Amp & Jack	
			Engineer:	
Size	Project Name		Rev	
Custom			1.0	
Date:	Friday, February 13, 2009		Sheet	37 of 91

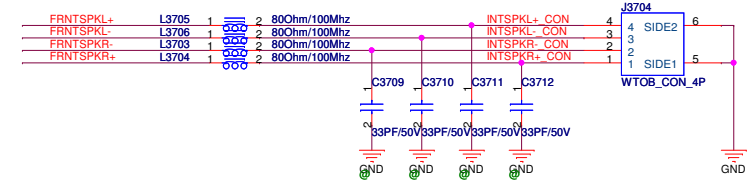
<http://laptopblue.vn/>

<Variant Name>

		Title : <b>AUD_FM2010</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>John Hung</b>	
Size Custom	Project Name <b>N2Sv</b>		Rev 1.0
Date: <b>Friday, February 13, 2009</b>		Sheet	38 of 91

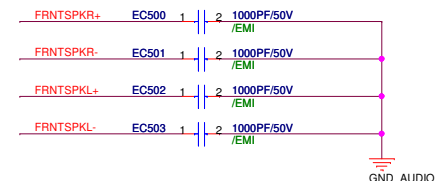


## SPEAKER CONNECTOR (2W)



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

## 2.0G-G71G-EMI



<Variant Name>

<b>ASUS</b>		<b>Title : AUD_Woofr &amp; Front</b>
Size		Engineer:
Custom	Project Name	Rev 1.0
Date: Friday, February 13, 2009	Sheet 39 of 91	

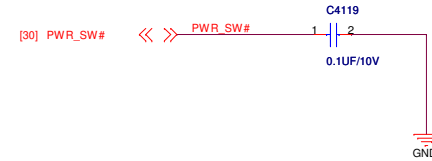
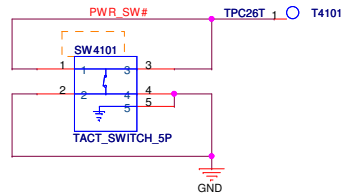
<http://laptopblue.vn/>

<Variant Name>

		Title : CB_R5C833	
Engineer:			
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009			
Sheet 40 of 91			

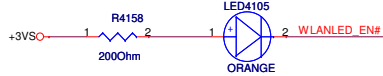


## SWITCH BUTTON

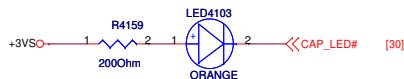


## LED

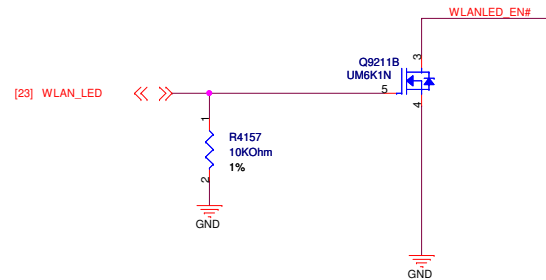
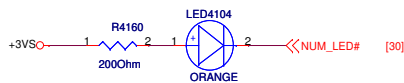
### For WireLess LED



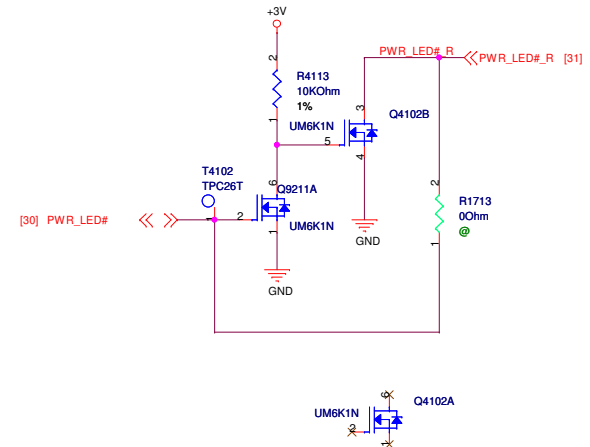
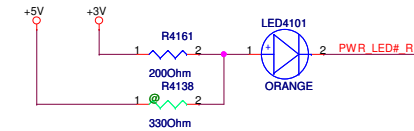
### for Cap. Lock



### for Num Lock



### For POWER LED



<Variant Name>

<b>ASUS</b>		Title : CB_R5C833	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009	Sheet	41	of 91


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<Variant Name>

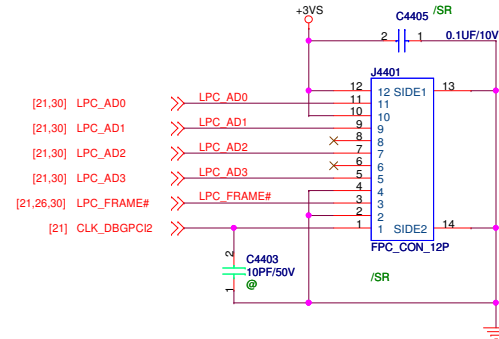
		<b>Title :</b> CB_4in1 CardReader	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b>	
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009		Sheet	42 of 91

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<Variant Name>

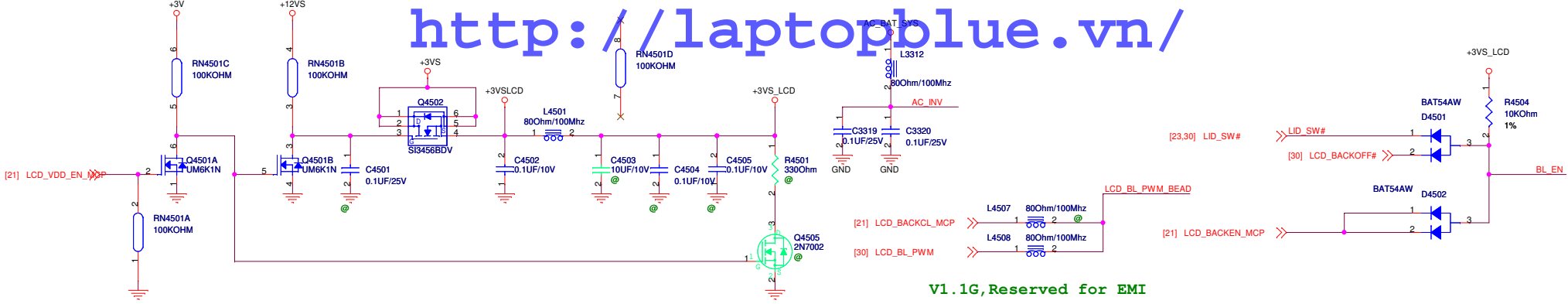
		Title : NEW CARD	
Engineer:			
Size	Project Name	Rev	
Custom		1.1	
Date: Friday, February 13, 2009		Sheet	43 of 91

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<Variant Name>

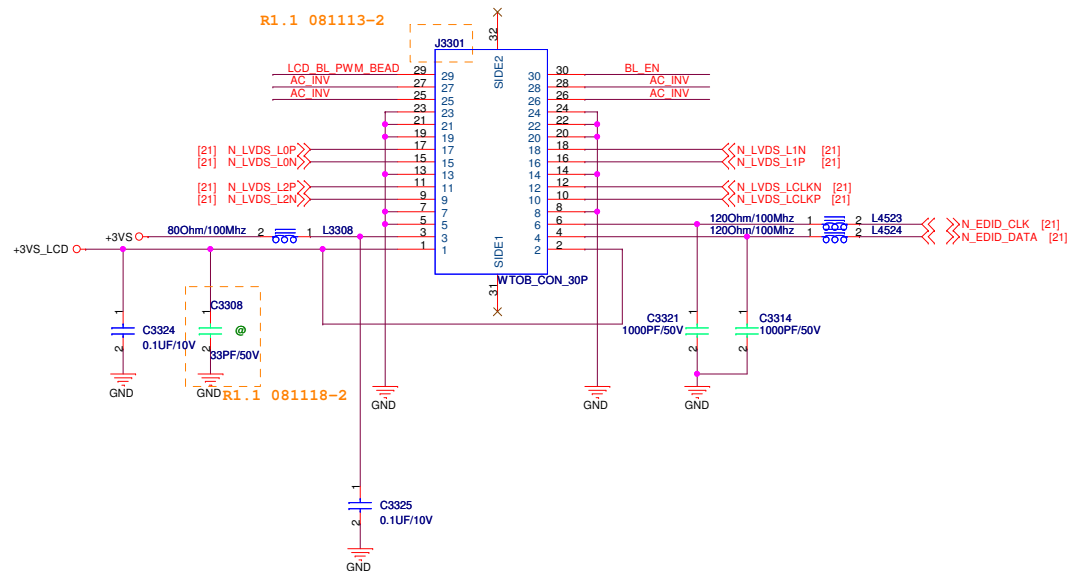
		Title : <b>DEBUG</b>	
Engineer:			
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009		Sheet 44 of 91	



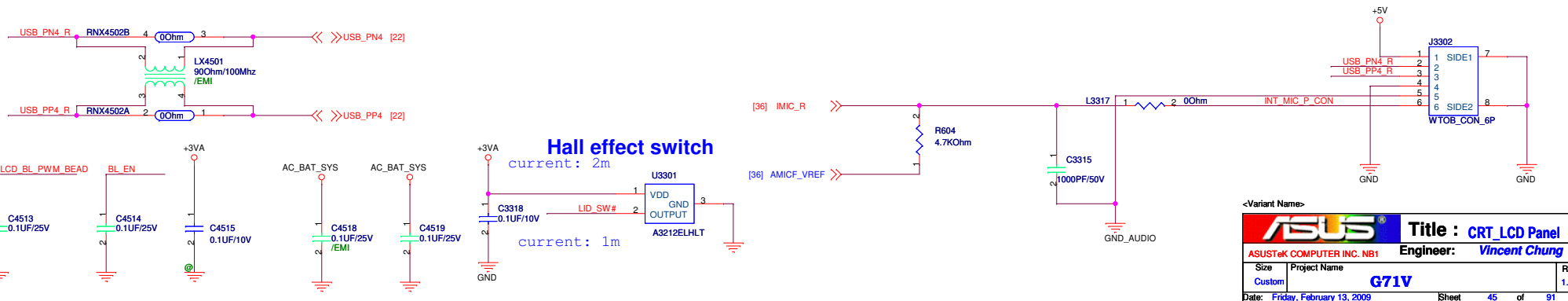
## LED PANEL LVDS Interface

R1.1 081113-2

R1.2 081202-1



## CAMERA & MIC

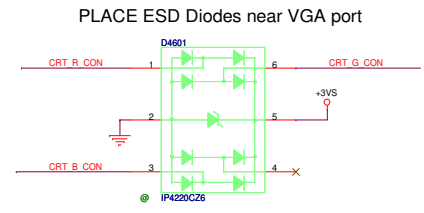
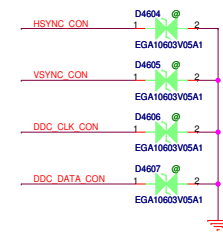
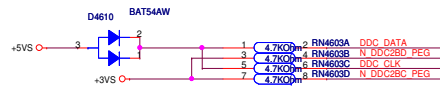
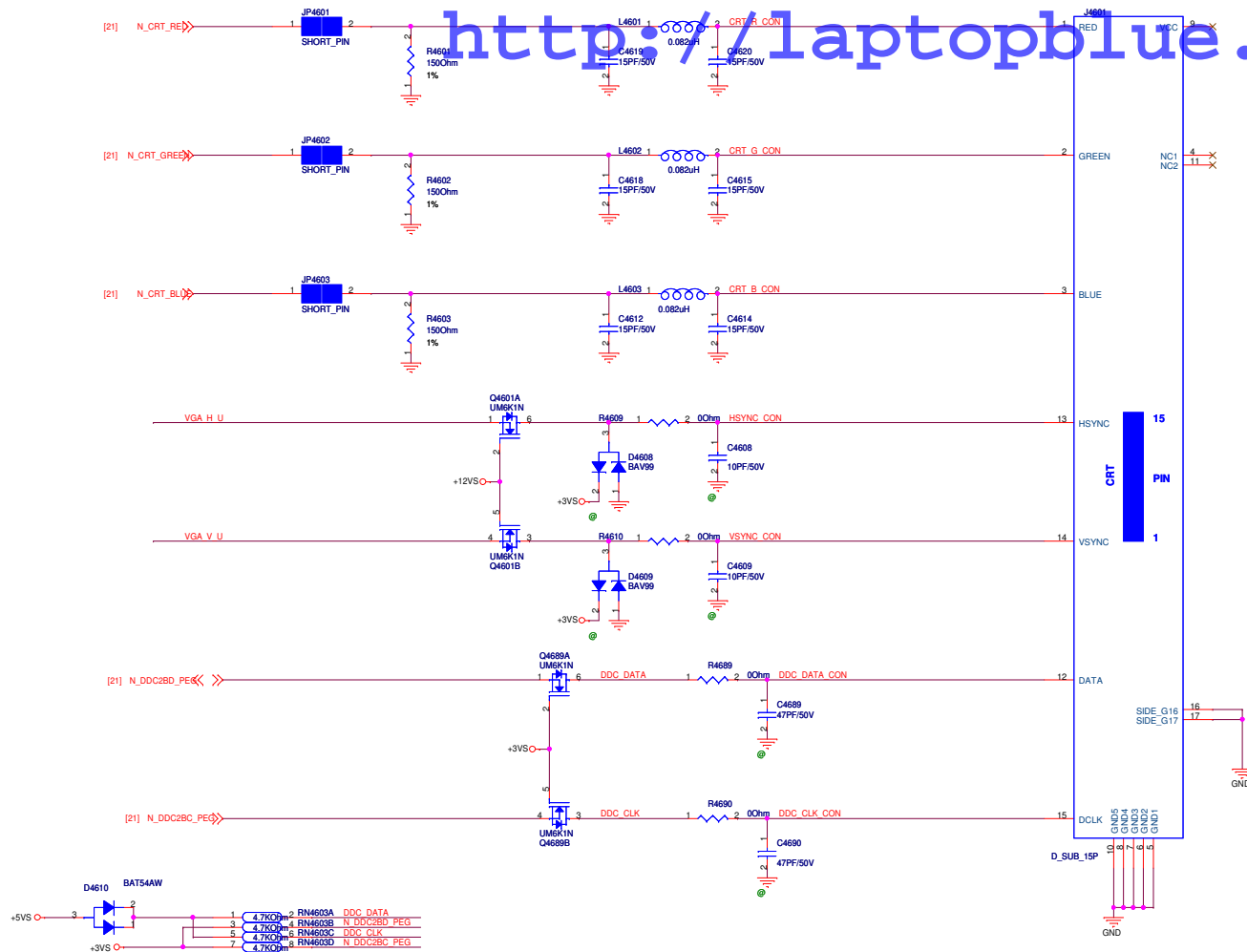


## Hall effect switch


current: 2m

current: 1m


ASUS		Title : CRT_LCD Panel	
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung	
Size	Project Name	Rev	
Custom	G71V	1.0	
Date: Friday, February 13, 2009	Sheet	45	of 91



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<Variant Name>			
		Title : TPM	
Engineer:			
Size	Project Name		Rev
Custom			1.0
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<Variant Name>		
		Title LVDS & Inverter CON
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date: Friday, February 13, 2009		Sheet 48 of 91



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<Variant Name>



**Title :**

**Engineer:**

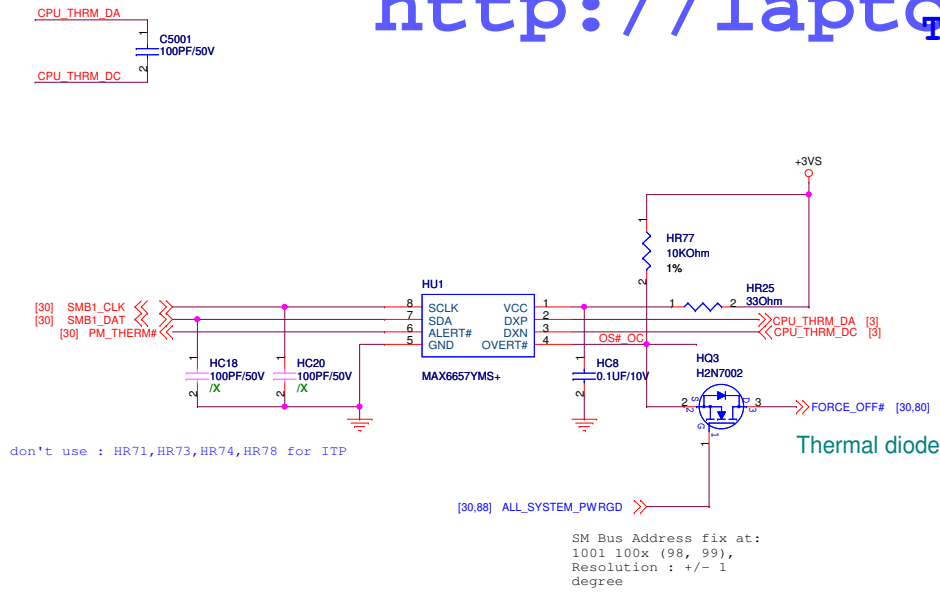
Size  
**A**

Project Name

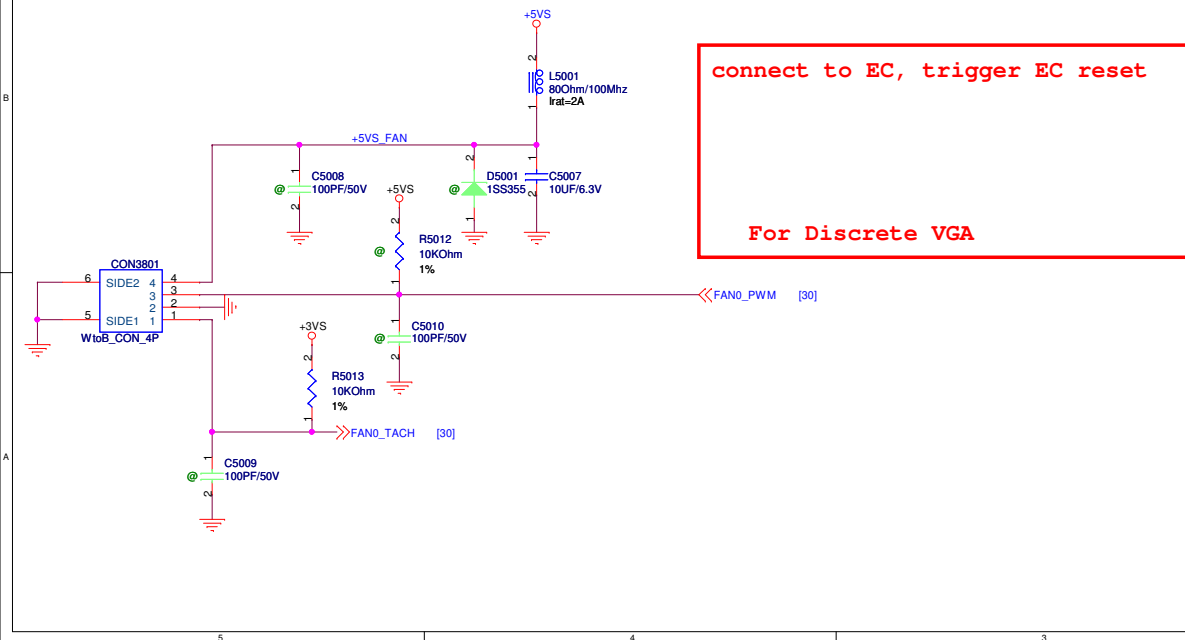
Rev  
**1.0**

Date: **Friday, February 13, 2009**

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## DC FAN Control

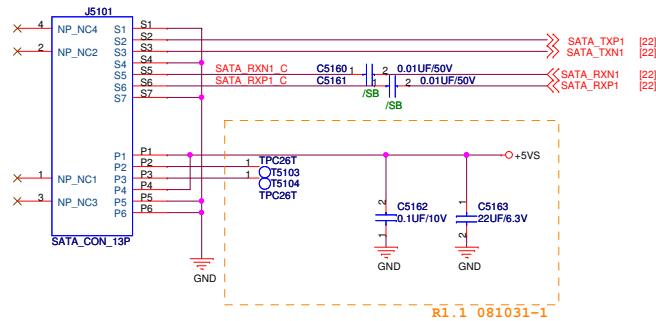


<Variant Name>

<b>ASUS</b>		<b>Title : Thermal &amp; Fan</b>	
Engineer:		Rev	
Size	Project Name	Rev	
Custom		1.1	
Date: Friday, February 13, 2009	Sheet	50	of 91

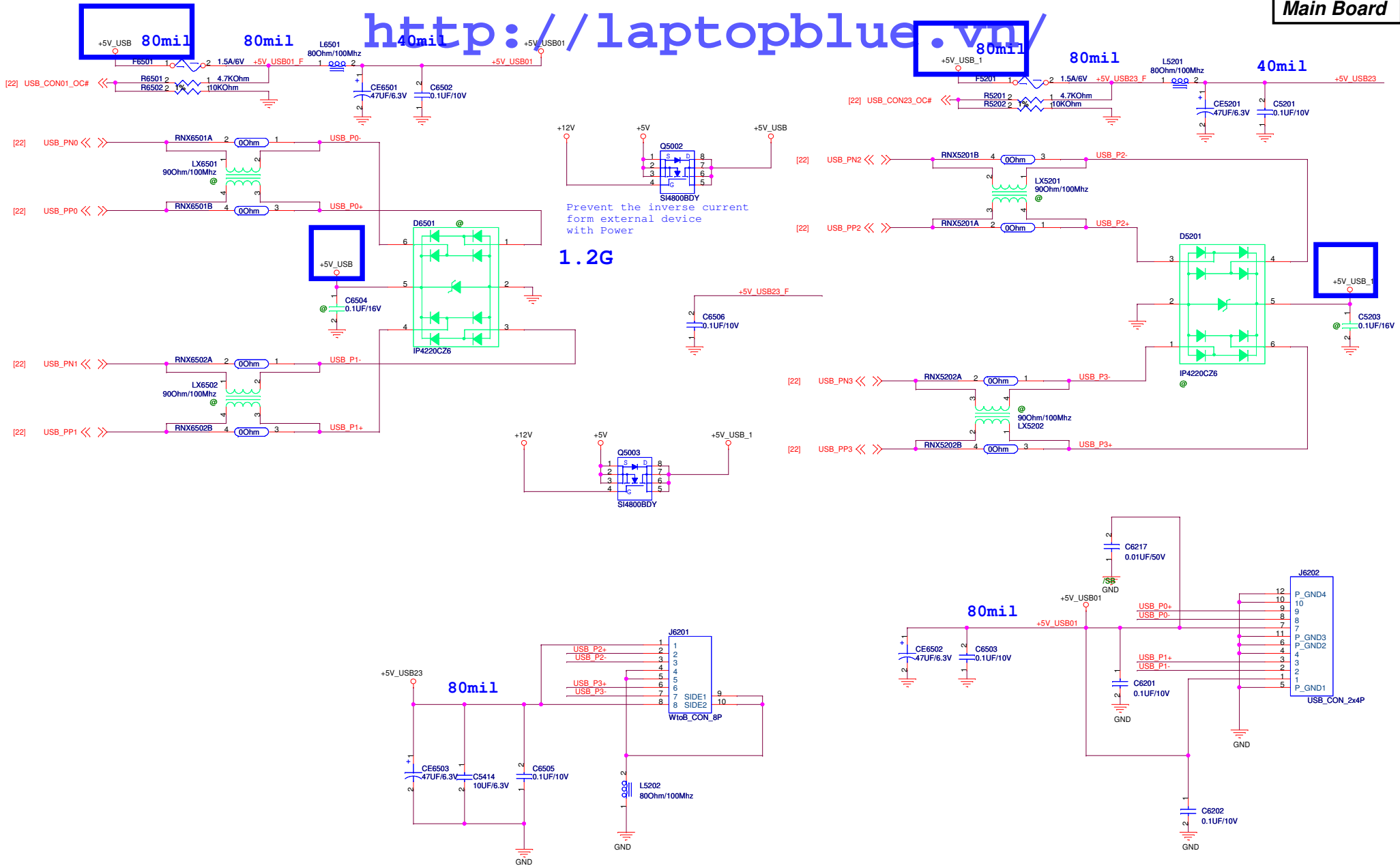
<http://laptopblue.vn/>

ODD



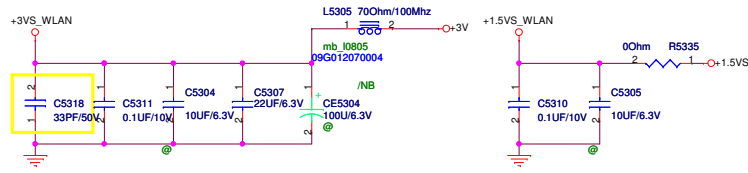
<Variant Name>

<b>ASUS</b>		<b>Title</b> Sata HDD & Swap Bay	
		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009		Sheet	51 of 91

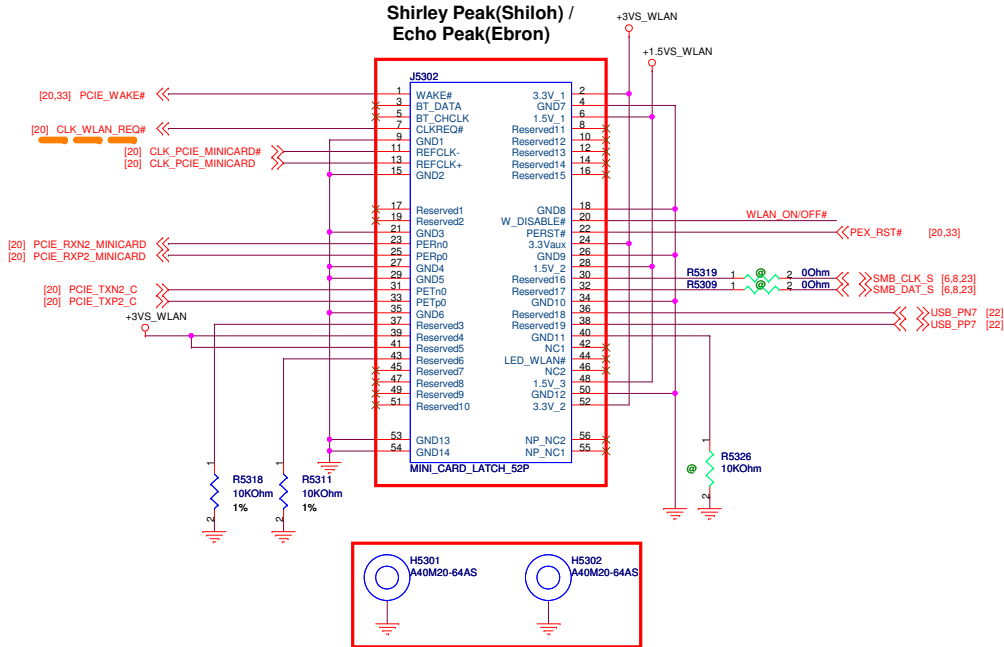
<http://laptopblue.vn/>


&lt;Variant Name&gt;

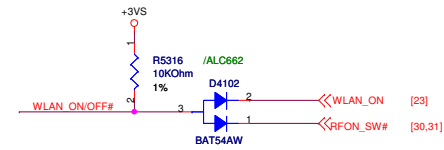
<b>ASUS</b>		<b>Title : USB_USB Ports</b>	
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung	
Size	Project Name	Rev	
Custom	G71V	1.0	
Date: Friday, February 13, 2009		Sheet	52 of 91



## Shirley Peak(Shiloh) / Echo Peak(Ebron)



N2



<Variant Name>

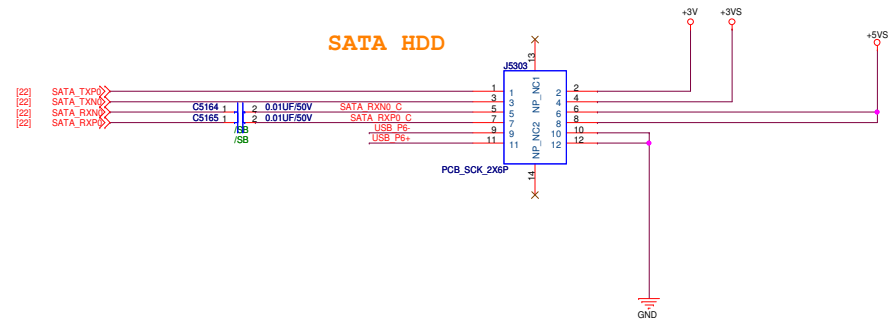
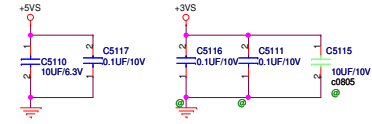
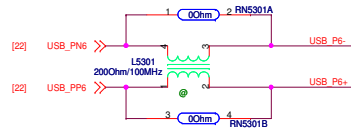
**ASUS** Title :Minicard card & Nut  
Engineer:

Size	Project Name	Rev
Custom		1.0

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### USB Cardreader



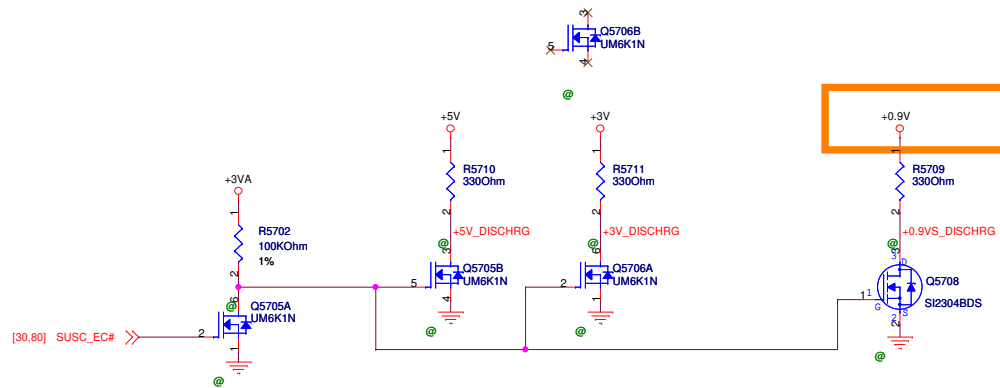
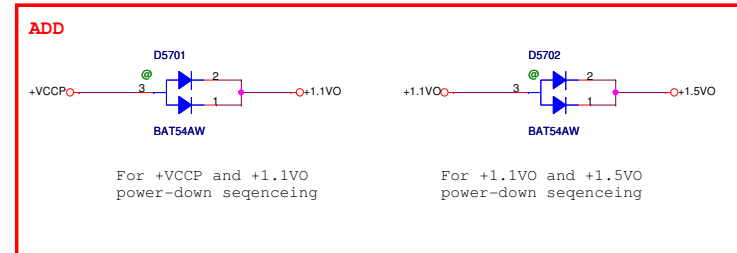
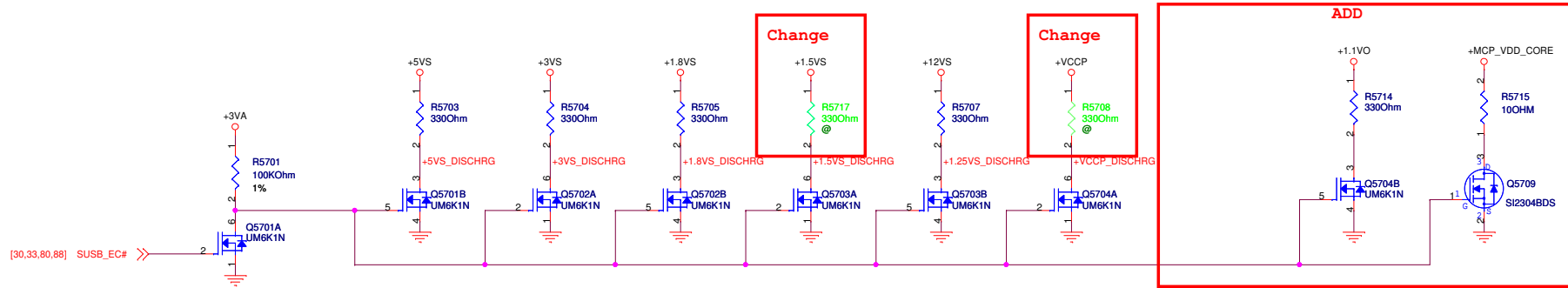
<http://laptopblue.vn/>

<Variant Name>

		<b>Title :</b>
<b>Engineer:</b>		
Size <b>A</b>	Project Name	Rev <b>1.0</b>
Date: <b>Friday, February 13, 2009</b>		Sheet <b>55</b> of <b>91</b>

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<Variant Name>

<b>ASUS</b>		<b>Title : DSG_Discharge</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>G71G</b>	1.0	
Date: Friday, February 13, 2009		Sheet	57 of 91


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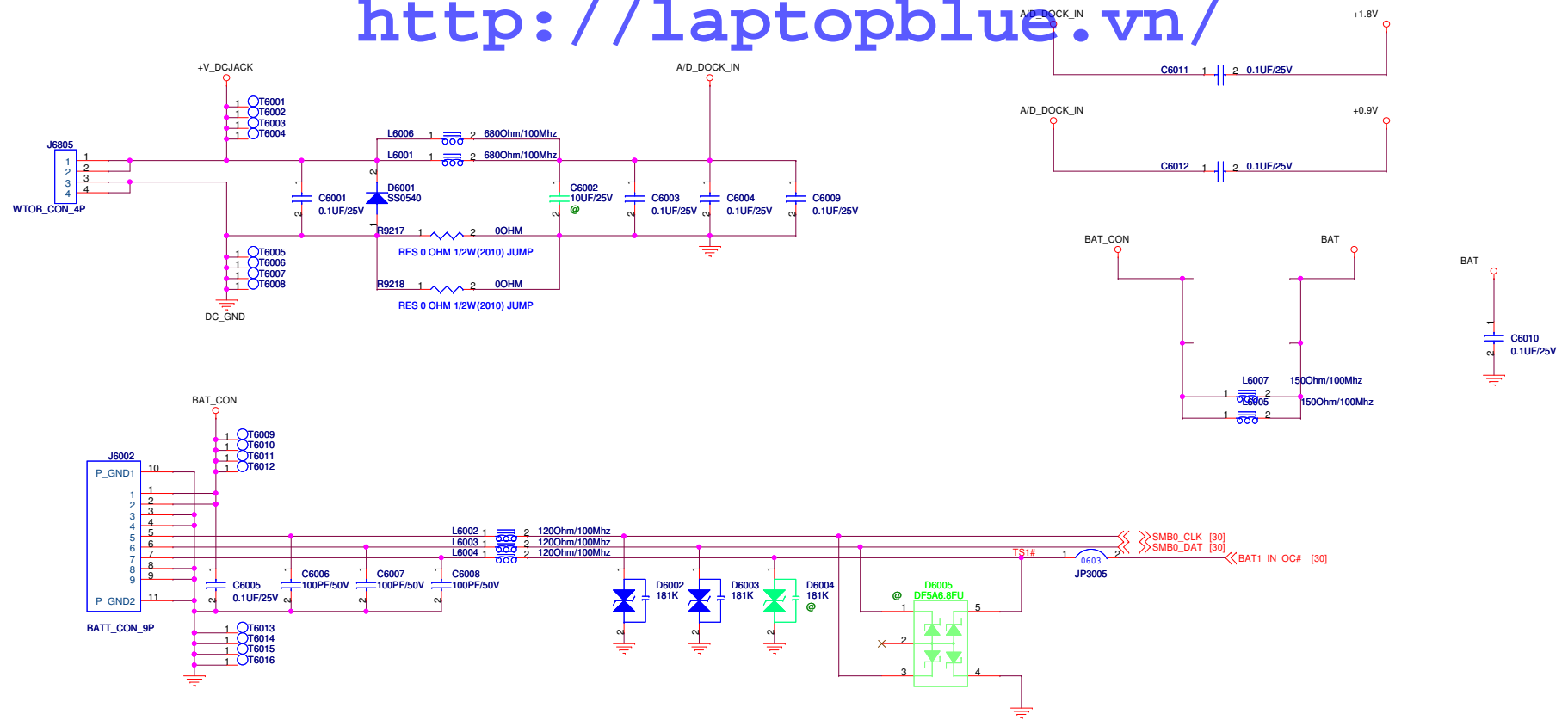
<Variant Name>

		<b>Title :</b>	
		<b>Engineer:</b>	
Size	Project Name		Rev
Custom			1.0
Date: Friday, February 13, 2009		Sheet	58 of 91

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<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC. NB6		<b>Engineer:</b>
Size A	Project Name	
Date: <a href="#">Friday, February 13, 2009</a>		Sheet <a href="#">59</a> of <a href="#">91</a>
Rev <a href="#">1.0</a>		



<Variant Name>

<b>ASUS</b>		<b>Title :DC_DC &amp; BAT Conn.</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Vincent Chung</b>	
Size	Project Name	Rev	
Custom	<b>G71V</b>	1.0	
Date: Friday, February 13, 2009		Sheet	60 of 91

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<http://laptopblue.vn/>

<Variant Name>

		Title : <b>FP_Fingerprint Conn.</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Vincent Chung</b>	
Size Custom	Project Name <b>G71V</b>		Rev 1.0
Date: <b>Friday, February 13, 2009</b>		Sheet <b>63</b> of <b>91</b>	

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<Variant Name>

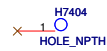
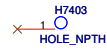
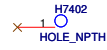
		Title : <b>TUN_TV Tuner</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>John Hung</b>	
Size Custom	Project Name <b>N2Sv</b>		Rev 1.0
Date: <b>Friday, February 13, 2009</b>		Sheet	64 of 91



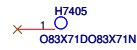
## Hole-A



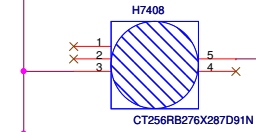
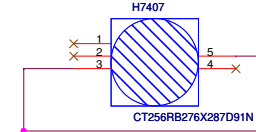
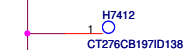
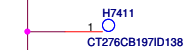
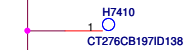
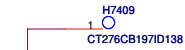
## Hole-B



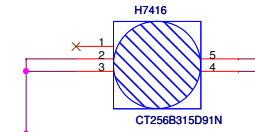
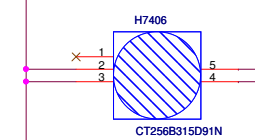
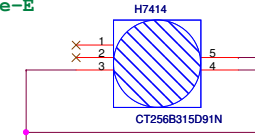
## Hole-C



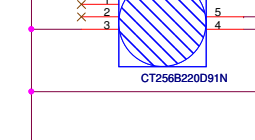
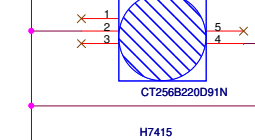
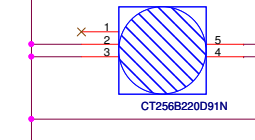
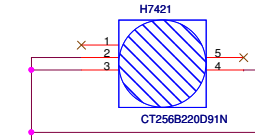
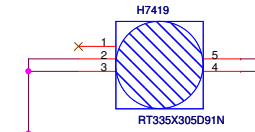
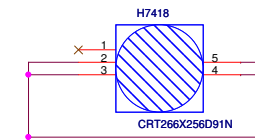
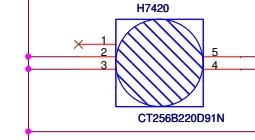
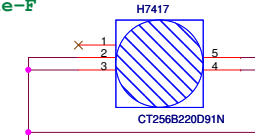
## Hole-D



## Hole-E



## Hole-F




<Variant Name>

<b>ASUS</b>		<b>Title :ME_Conn &amp; Screw Holes</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Vincent Chung</b>	
Size	Project Name	Rev	
Custom	<b>G71V</b>	1.0	
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<Variant Name>

		Title : E-SATA	
Engineer:			
Size	Project Name		Rev
Custom			1.0
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## Place Beside CPU



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<Variant Name>

		Title :	
		Engineer:	
Size	Project Name		Rev
Custom			1.0
Date: Friday, February 13, 2009		Sheet	68 of 91

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		Title : <b>N10M-GE1_PCIE</b>	
ASUSTeK COMPUTER INC		Engineer: <b>ENGINEER</b>	
Size Custom	Project Name <b>N10JG</b>		Rev 1.0
Date: <b>Friday, February 13, 2009</b>			
Sheet		69 of 91	

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<http://laptopblue.vn/>

		Title : <b>N10M-GE1 VRAM</b>	
ASUSTeK COMPUTER INC		Engineer: <b>ENGINEER</b>	
Size	Project Name		Rev
Custom	<b>N10JG</b>		1.0
Date: <b>Friday, February 13, 2009</b>		Sheet	71 of 91

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		Title : <b>N10M-GE1_DISPLAY</b>	
ASUSTeK COMPUTER INC		Engineer: <b>ENGINEER</b>	
Size	Project Name		Rev
Custom	<b>N10JG</b>		1.0
Date: <b>Friday, February 13, 2009</b>		Sheet	72 of 91



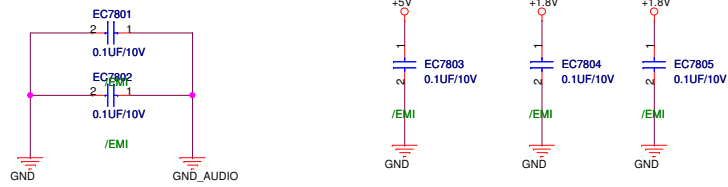
<http://laptopblue.vn/>

		Title : <b>N10M-GE1_XTAL</b>	
ASUSTeK COMPUTER INC		Engineer: <b>ENGINEER</b>	
Size	Project Name		Rev
Custom	<b>N10JG</b>		1.0
Date: <b>Friday, February 13, 2009</b>		Sheet	73 of 91

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http://laptopblue.vn/

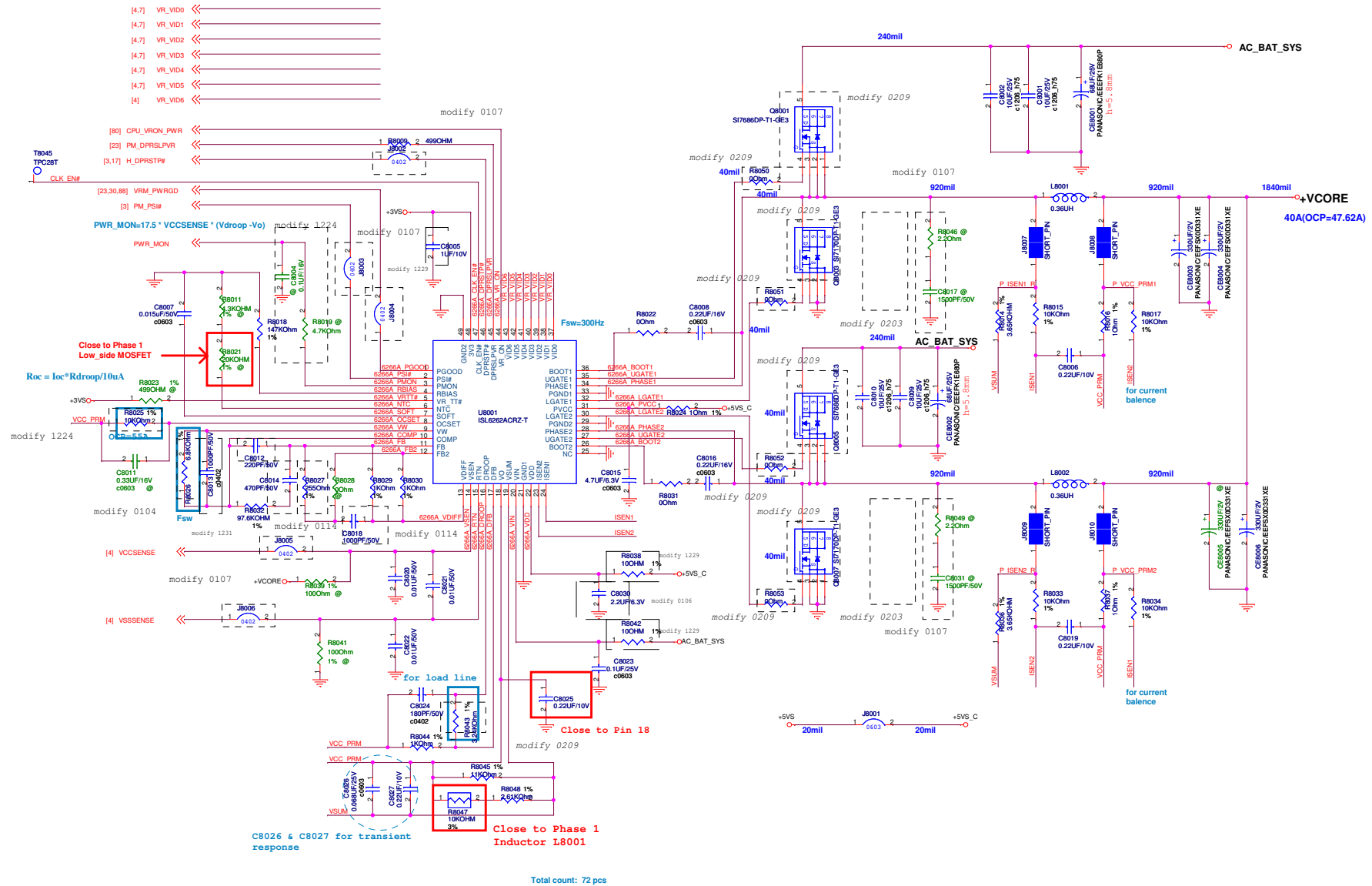


<Variant Name>

		Title :Fingerprint & Touchpad	
ASUSTeK COMPUTER INC. NB1		Engineer: Wenchi_Shen	
Size	Project Name	Rev	
Custom	M70Sv	1.1	
Date: Friday, February 13, 2009		Sheet	77 of 91

20080520	1.2G
Page 52	1. ADD USB+5V gate Q5002
Page 56	2. ADD R5626,R5609
Page 4	3. DEL R0412
Page 54	4. ADD C5402,C5403 5p for SMBus in GPIO controller ; GPRN10 change to 10K ohm
Page 84	5. Controlle +5V with SUSC#_PWR
Page 82	6. Change +VCCP to 1.2V default for CPU O.C. ability improve
20080701	2.0G
Page 56	1. TP-LED v.s. TP-disable LED reverse
Page 45	2. Inverter CN pin 19 reserve 0 phm to GND ,never stuff for single-lamp inverter
Page 46	3. Battery in P/H change to +3VA
Page 80	4. CPU load-line modify to 2.1 mini-ohm (R8036 由 10.5K改成 9.31K 1%)

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Total count: 72 pcs

<Variant Name>

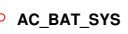


HS MOS Second source IRF8714  
LS MOS Second source IRF8736

```

modify 0106

```



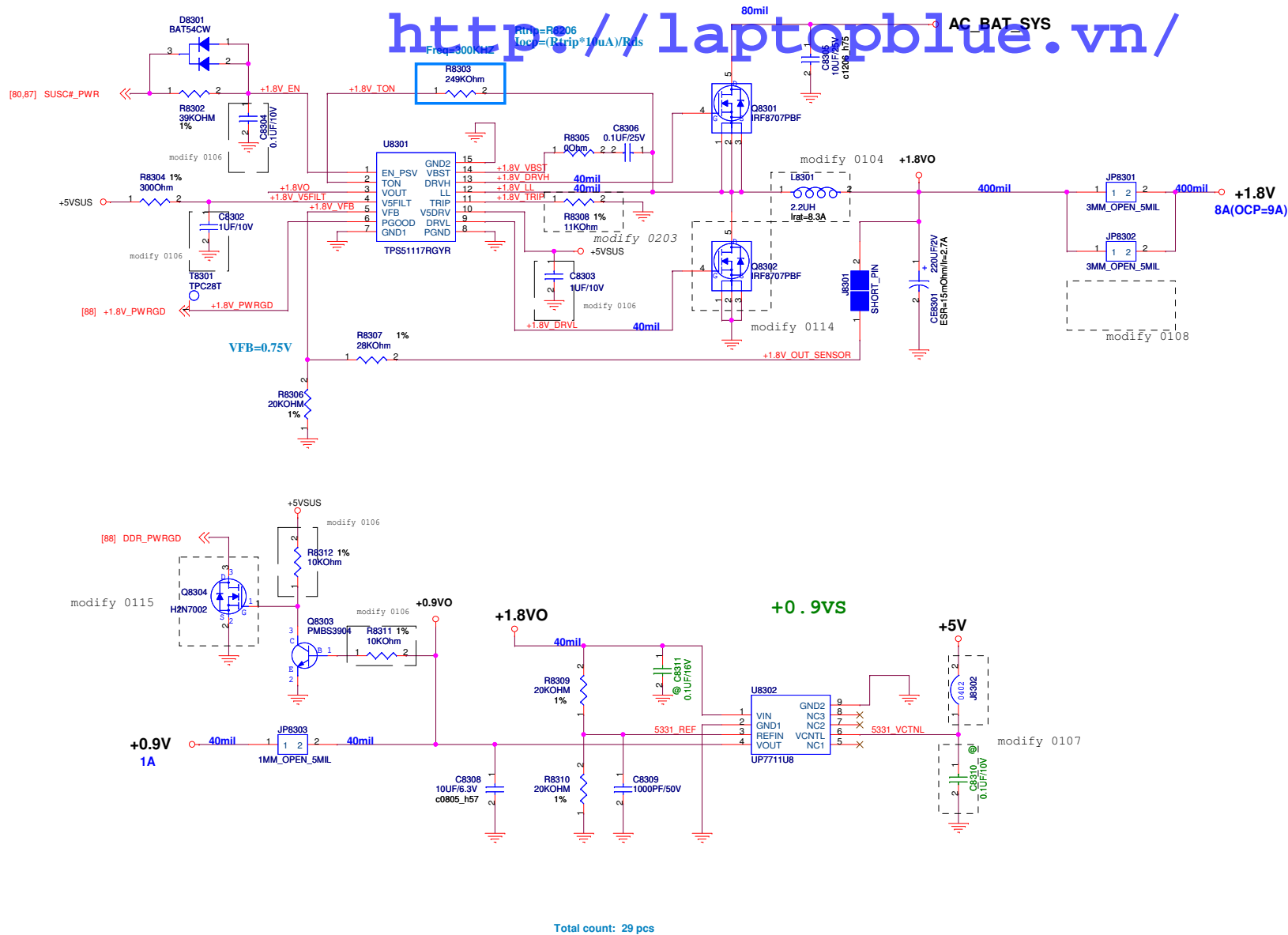
**<Variant Name>**





**<Variant Name>**





+1.5VS



		<b>Title :</b> INS29401694	
<b>ASUSTek COMPUTER INC. NB</b>		<b>Engineer:</b> Eason	
<b>Size</b> B	<b>Project Name</b>  <div style="text-align: center; font-size: 1.5em; font-weight: bold;">K50I</div>	<b>Rev</b> 1.0	
<b>Date:</b> Friday, February 13, 2009		<b>Sheet</b> 83	<b>of</b> 91

**Title :** INS29491694

Engineer: **Eason**

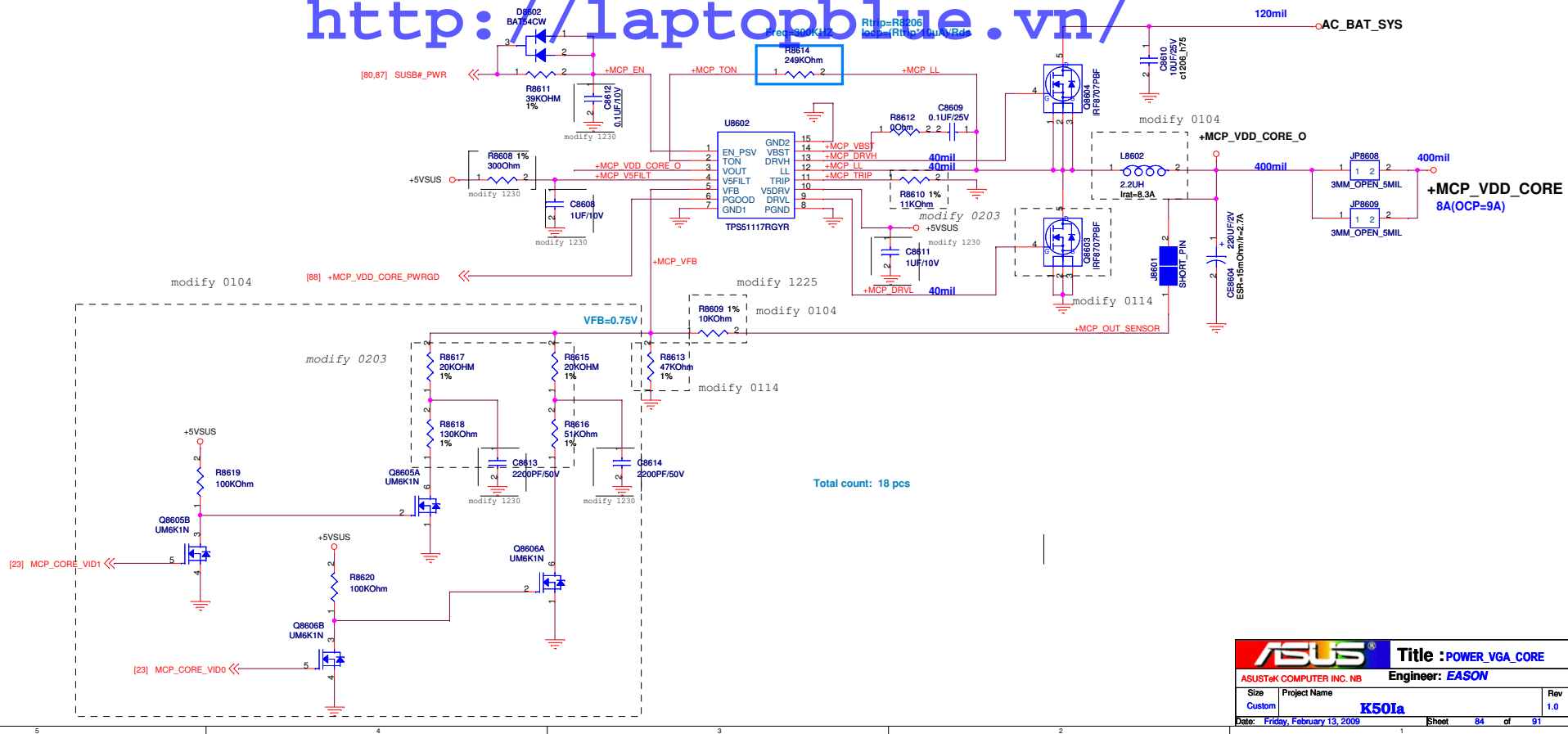
Size	Project Name
B	

**K50I**

Date: Friday, February 13, 2009

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[illegible][illegible]

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**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

TOTAL COUNT:56 PCS

Charger IC and EC Code correlation sheet :  
Charger MAX8725 => EC CODE : 200  
Charger MAX17015 => EC CODE : 201  
Charger MB39A132 => EC CODE : 202

ASUS® Title : POWER\_CHARGER\_202  
Engineer: Eason  
Date: Friday, February 13, 2009 Sheet 65 of 91

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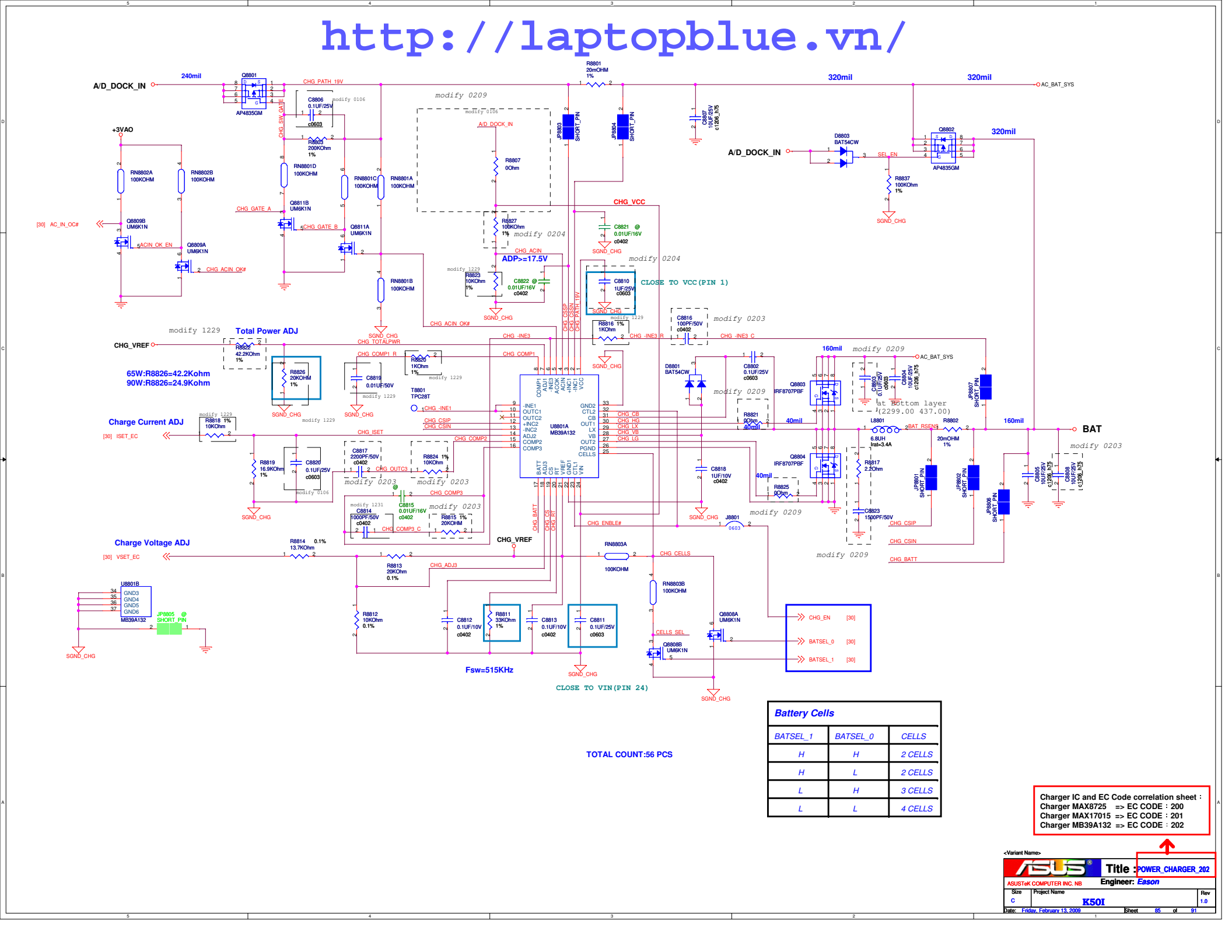
**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

TOTAL COUNT:56 PCS

Charger IC and EC Code correlation sheet :  
Charger MAX8725 => EC CODE : 200  
Charger MAX17015 => EC CODE : 201  
Charger MB39A132 => EC CODE : 202

ASUS  
ASTUTAK COMPUTER INC. NB  
Project Name: K50I  
Date: Friday, February 13, 2009  
Sheet: 65 of 91  
Title: POWER\_CHARGER\_202  
Engineer: Eason  
Rev: 1.0



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**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

TOTAL COUNT:56 PCS

Charger IC and EC Code correlation sheet :  
Charger MAX8725 => EC CODE : 200  
Charger MAX17015 => EC CODE : 201  
Charger MB39A132 => EC CODE : 202

ASUS® Title : POWER\_CHARGER\_202  
Engineer: Eason  
Date: Friday, February 13, 2009 Sheet 65 of 91

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**Charge Current ADJ**

65W: R8826=42.2Kohm  
90W: R8826=24.9Kohm

**Charge Voltage ADJ**

30 ISET\_EC

30 VSET\_EC

**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
H	L	2 CELLS
L	H	3 CELLS
L	L	4 CELLS

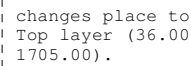
**Charger IC and EC Code correlation sheet :**  
 Charger MAX8725 => EC CODE : 200  
 Charger MAX17015 => EC CODE : 201  
 Charger MB39A132 => EC CODE : 202

**ASUS** Title: POWER\_CHARGER\_202  
 Engineer: Eason  
 Date: Friday, February 13, 2009  
 Sheet: 65 of 91

BATTERY IN DETECT

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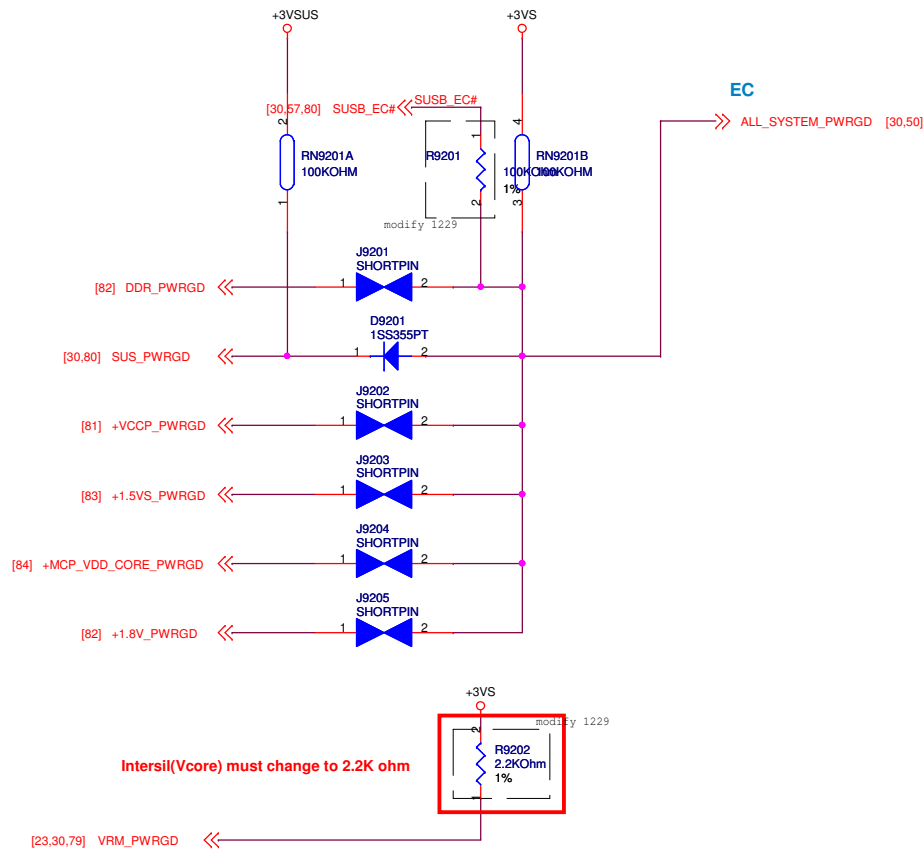
<http://laptopblue.vn/>



**<Variant Name>**



## POWER GOOD DETECTOR



Total count: 8 pcs

<Variant Name>

<b>ASUS</b>		Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size B	Project Name K50I		Rev 1.0
Date: Friday, February 13, 2009		Sheet 88 of 91	

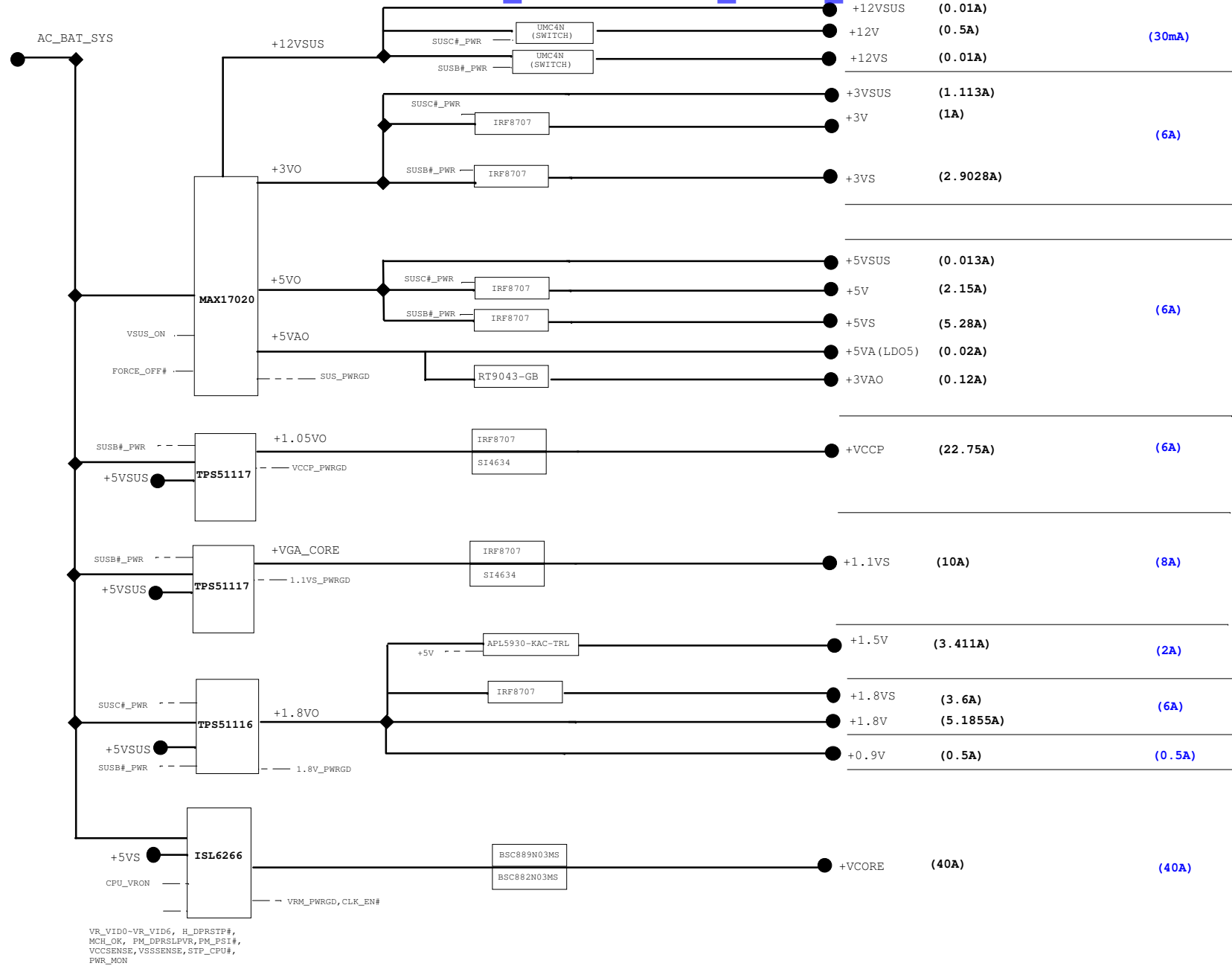


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<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size	Project Name		Rev
Custom	K50I		1.0
Date: Friday, February 13, 2009		Sheet	89 of 91



<Variant Name>

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