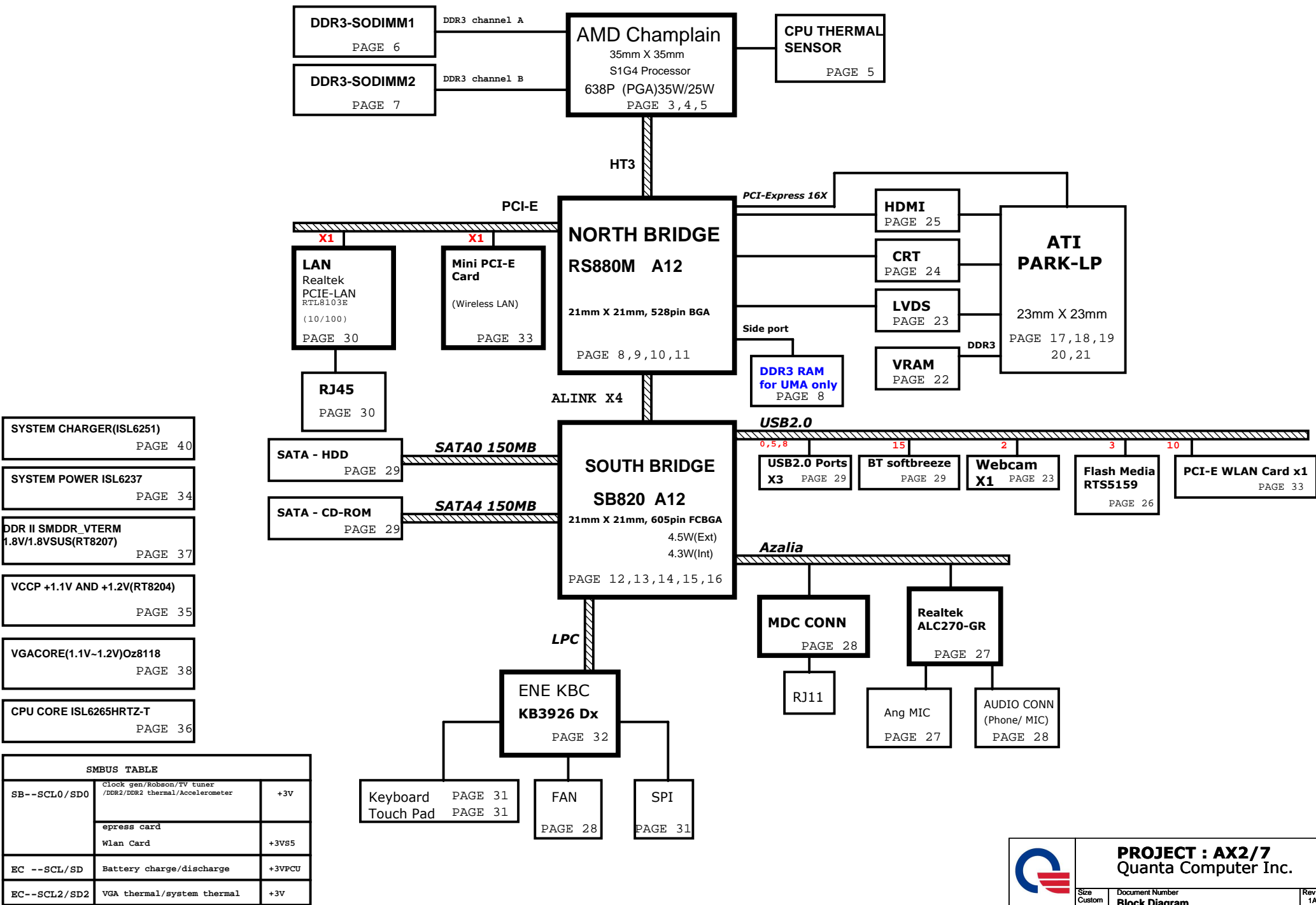


AX2/7 : SYSTEM DIAGRAM



01



PROJECT : AX2/7
Quanta Computer Inc.

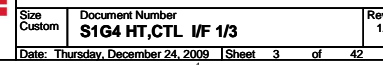
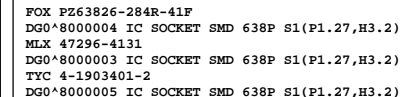
Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Thursday, December 24, 2009	Sheet 1	of 42

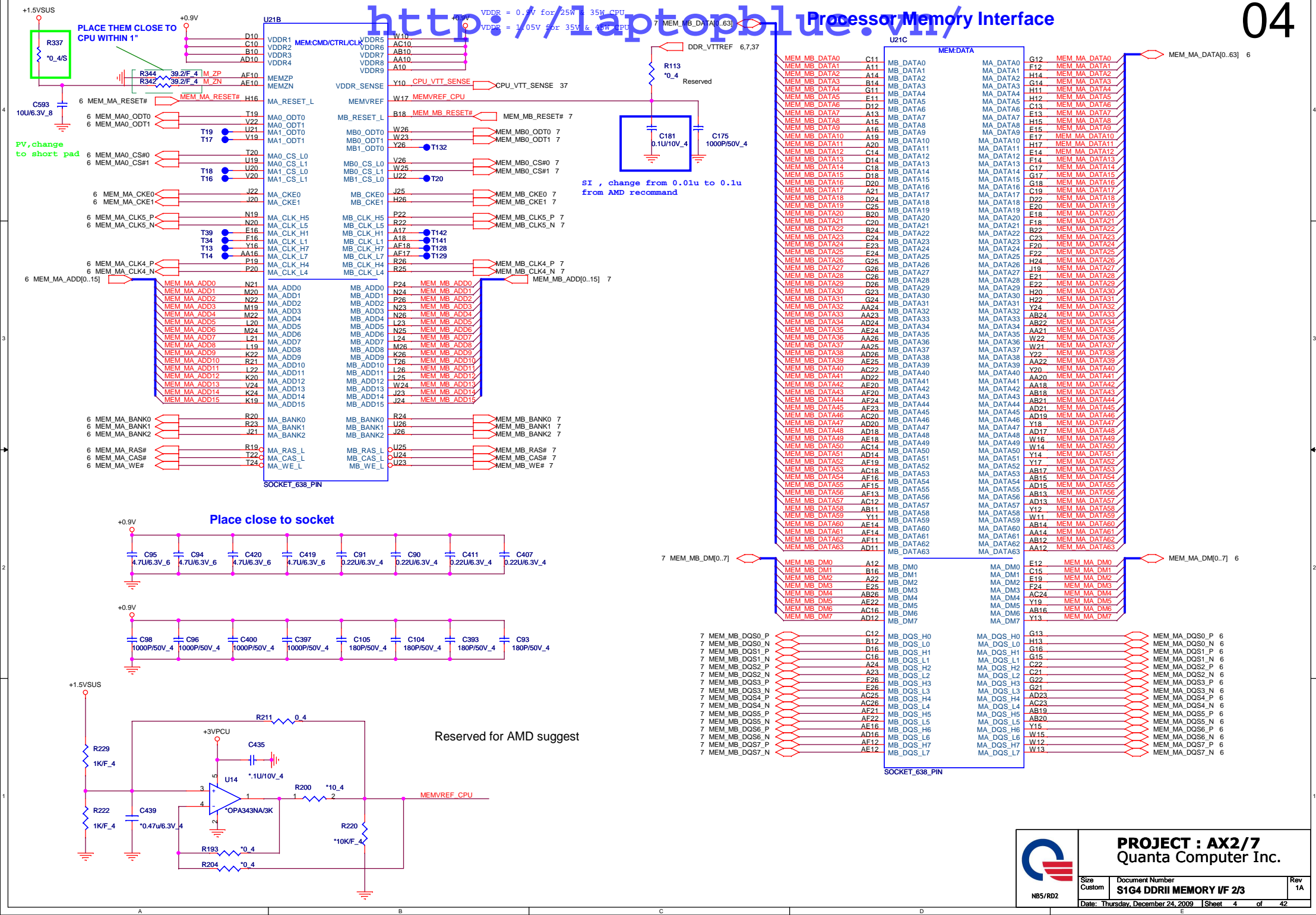
PV,delete all external clock GEN reserve material



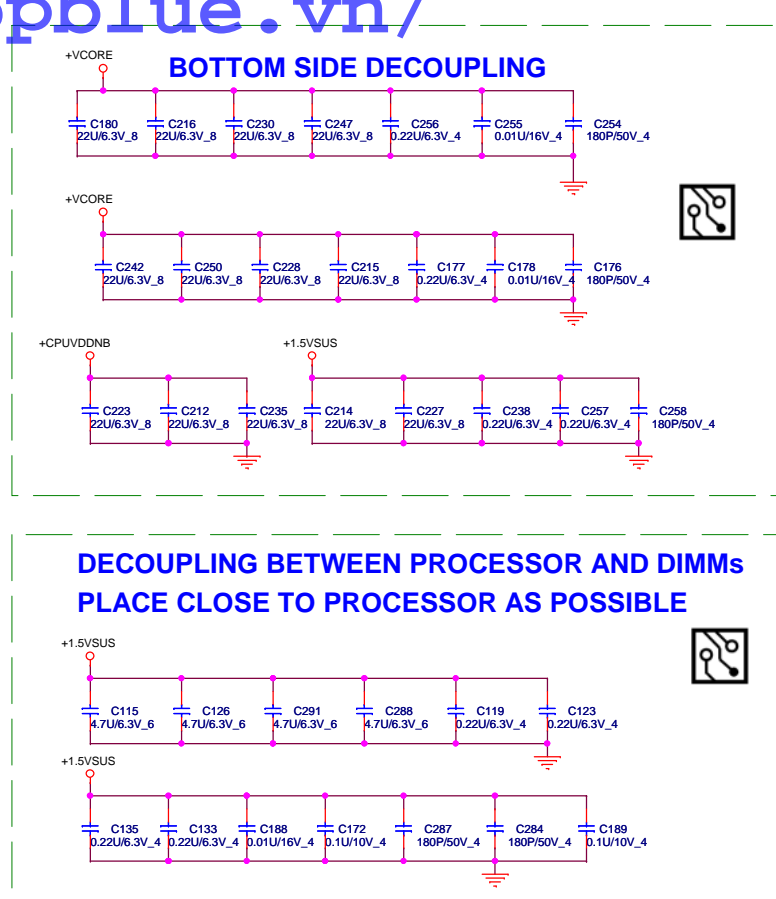
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number Clock Generator	Rev 1A
Date: Wednesday, December 23, 2009 Sheet 2 of 42		

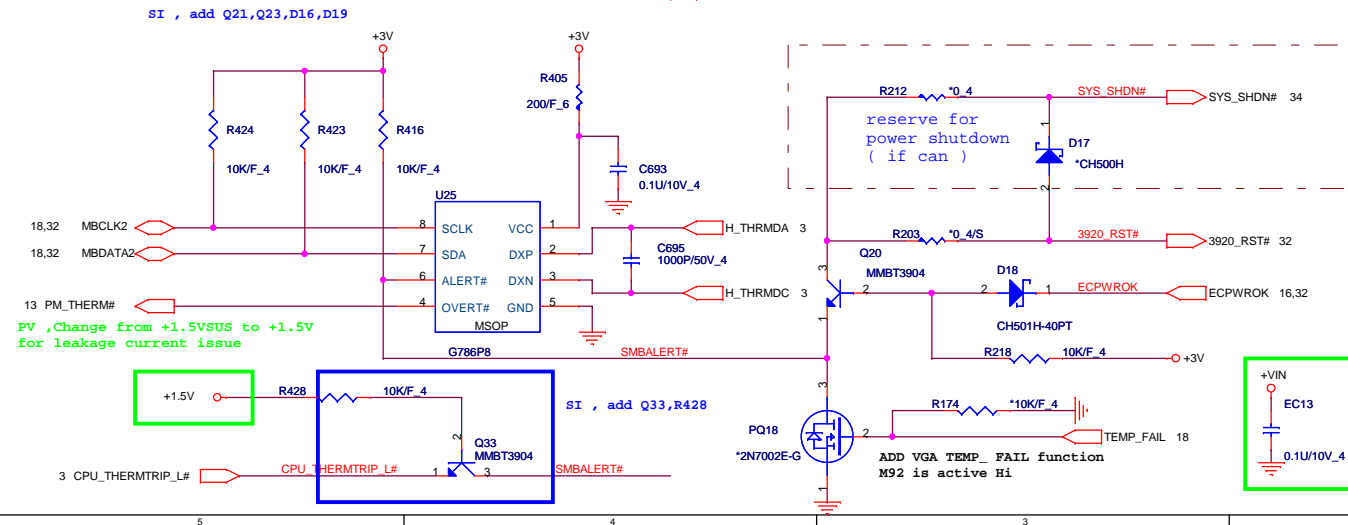


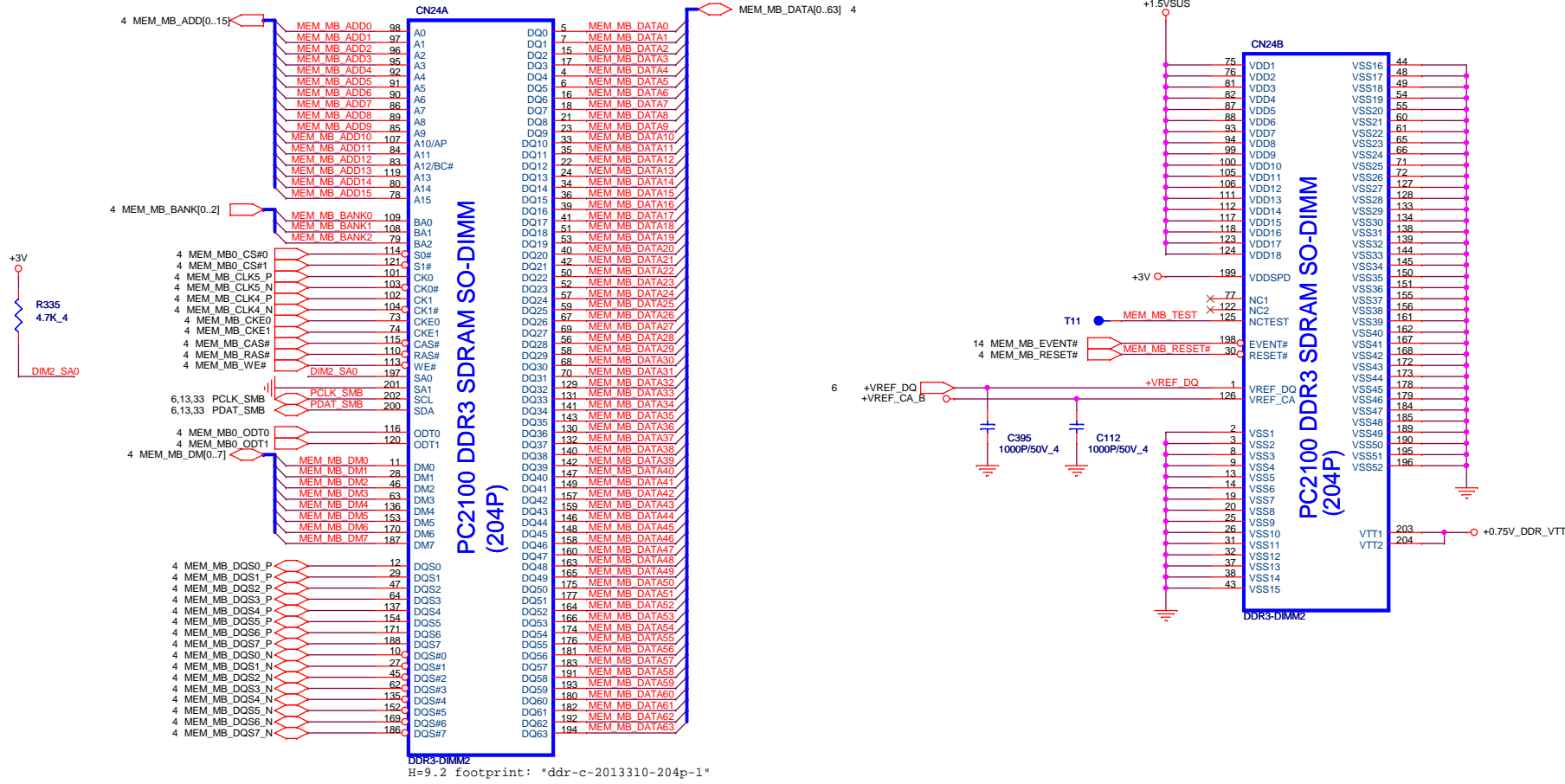


PROJECT : AX2/7
Quanta Computer Inc.



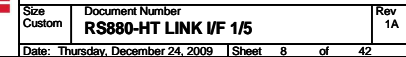
The diagram illustrates the connection of HyperTransport nets across plane splits. It is divided into two sections by a dashed line. The top section shows connections for nets EC1 through EC12, with labels like +1.5V_VGA, +1.8V_VGA, +VGA_CORE, +VIN, +5V, and +VGA_CORE on the left, and +3V, +3V, +3V, +3V, +3V, and +3V on the right. The bottom section shows connections for nets EC2 through EC11, with labels like +VGA_CORE on the left, and +3V, +3V, +3V, +3V, +3V, and +1.1V on the right. The diagram illustrates how these nets are connected across a plane split, with labels like EC10, EC12, EC8, EC7, EC1, EC2, EC9, EC11, EC15, and EC6 indicating specific connection points or components.

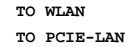




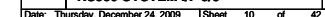
PROJECT : AX2/7
Quantia Computer Inc.

Size Custom	Document Number DDR3 SODIMMS TERMINATIONS	Rev 1A
Date: Thursday, December 24, 2009 Sheet 7 of 42		

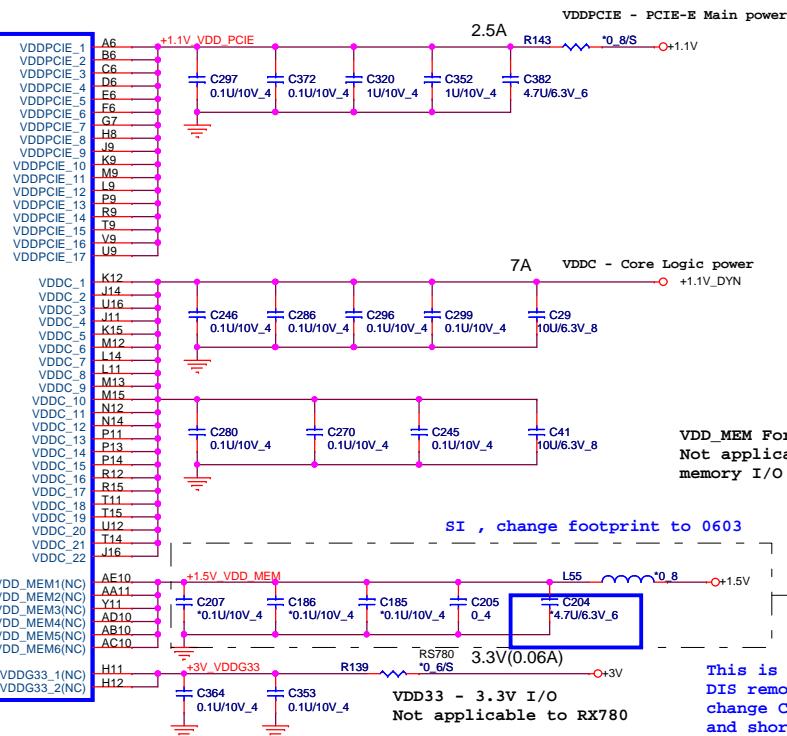
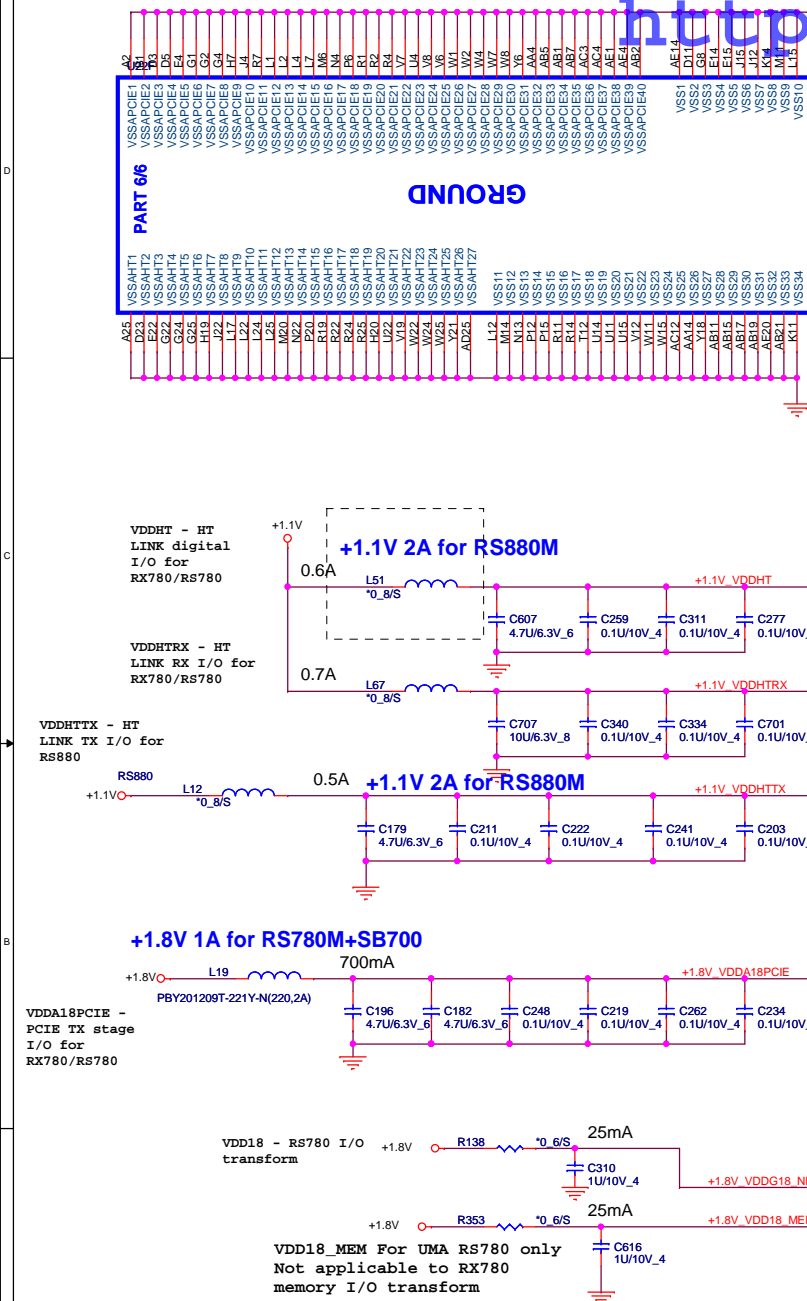




DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLT18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD18	+1.8V	VDDLT33	NC



VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

SI , change footprint to 0603

This is side port power
DIS remove L55 ,
change C205 to 0 ohm
and short to GND



NB5/RD2

Size	Custom
------	--------

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number RS880-POWER5/5
----------------	--

	Re
	1

Date: Tuesday, December 22, 2009 Sheet 11 of 42

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB

TO RS880

+1.1V_PCIE_VDDR

SI , C404 change to
reserve only

SI , add AND gate for the reset input
of PCIE devices from AMD recommend

Place within 0.5"
of SB

SI , remove R483,R286
from AMD recommend

SI , change pull high
from +3V_VGA to
+3V_DELAY

SI , change from
VGA_RSTA to A_RST#_R

SI , change to 27P

PV,change
to short pad

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

PCIE CLKs

PCIE CLKs

PCIE CLKs

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SATA ODD

```
XTLVDD_SATA-- SATA
crystal power
```

NOTE:

R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

+1.1V_AVDD_SATA

SI , change to reserve only

U30
TC7SH08

13

+1.

SB820M A12

SERIAL ATA

HW MONITOR

SB800
Part 2 of

Part 2 of 5

FLASH

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

IS NO IDE, TEST
FOR DEBUG BUS
ATORY

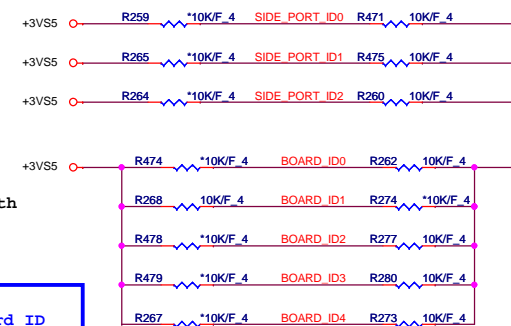
- PV, change to short pad

For blue tooth
23 & wireless
merge card

SI define board ID

PV define for M93

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port



ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF



PROJECT : AX2/7
Quanta Computer Inc.

Size	Custom
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Document Number
SB820-ACPI/GPIO/USB 2/4

	Rev 1A
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Date: Thursday, December 24, 2009 Sheet 14 of 42





internal have pull
Hi 10K, confirm AMD
ward this pull Hi
not need

13 ACZ_SDOUT

+VDDIO_AZ

R257
10K/F_4

12 PCI_CLK_TPM

R258
10K/F_4

R448
10K/F_4

12 PCI_CLK2

R447
10K/F_4

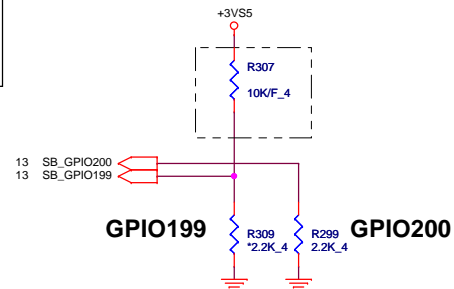
12 PCI_CLK3

R445
10K/F_4

PV, add it to force
PCIe of SB820 at Gen I

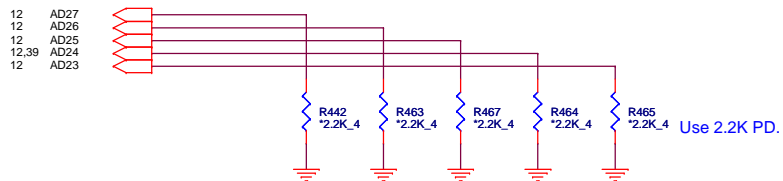
PV, add it to force
PCIE of SB820 at Gen I

It must ready
before RSMRST#



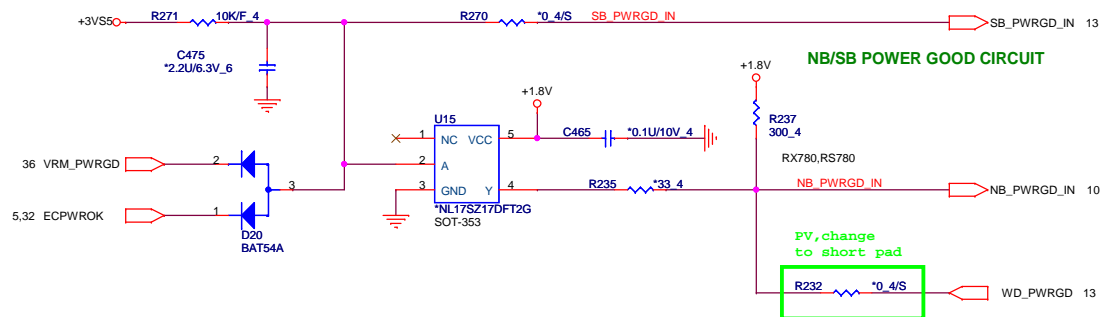
PULL HIGH	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



Use 2.2K PD.

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

PV, change
to short pad

PULL HIGH	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

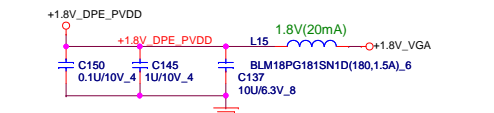
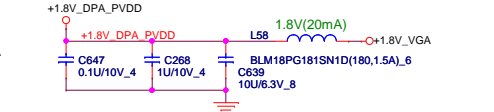
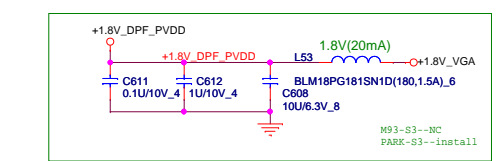
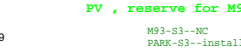
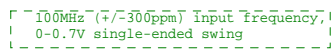


PROJECT : AX2/7
Quanta Computer Inc.

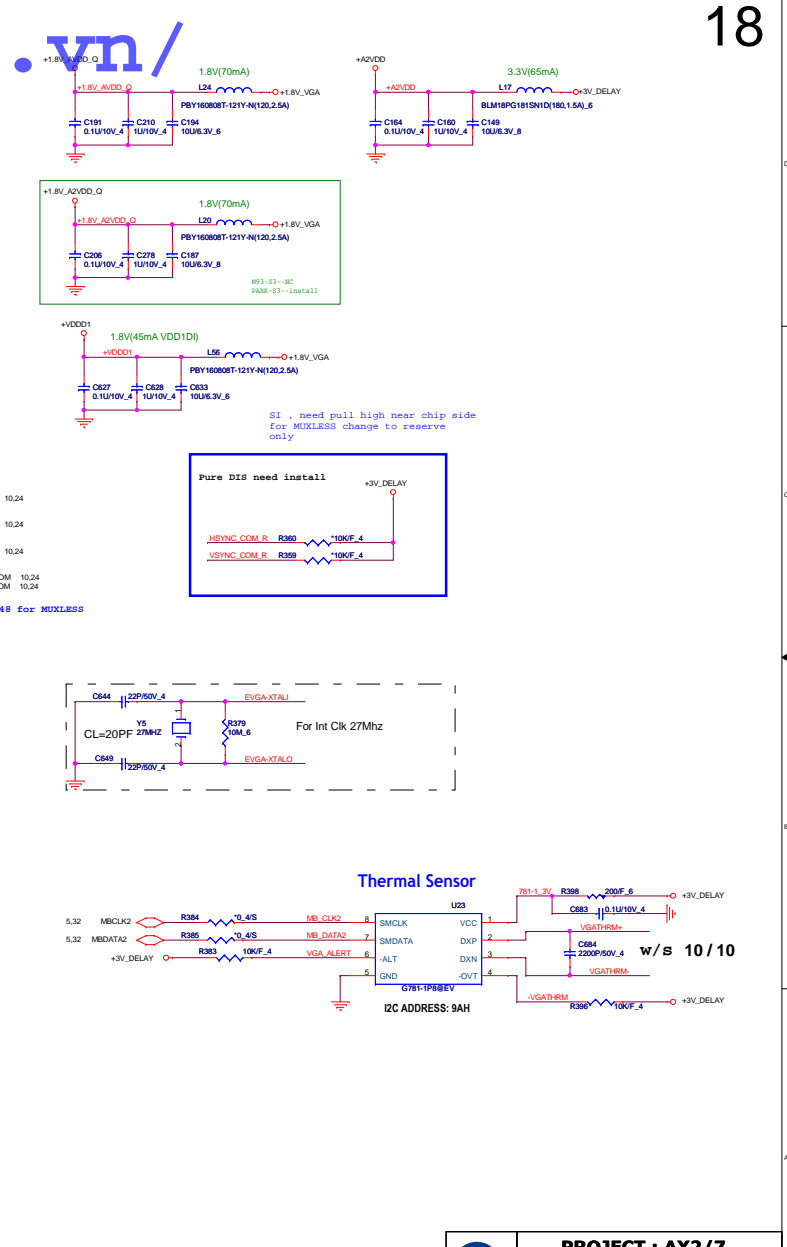
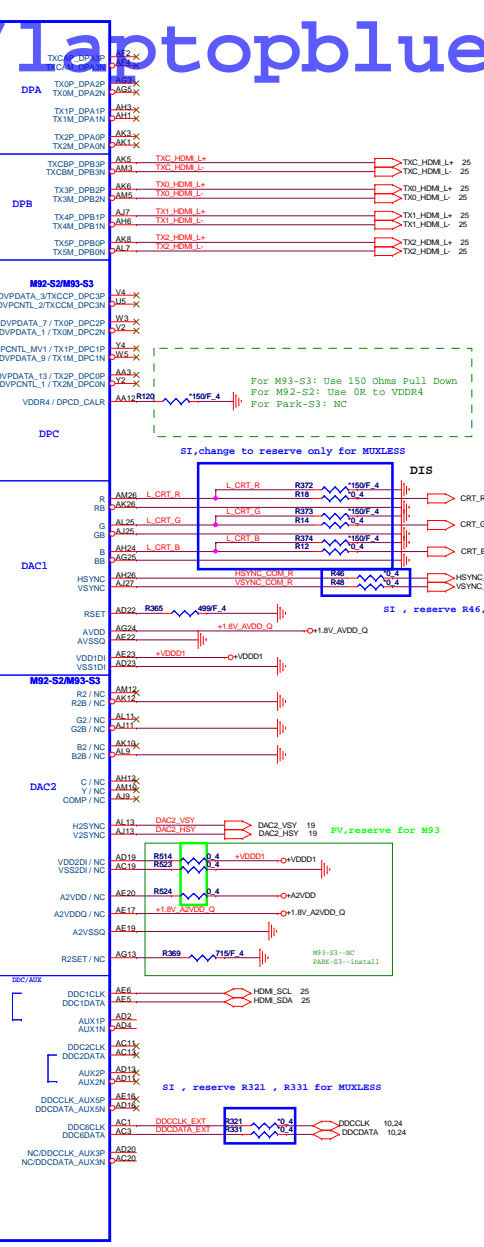
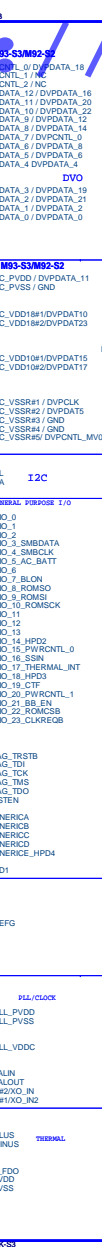
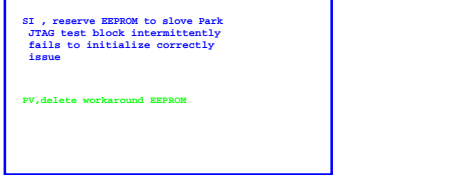
Size Custom	Document Number SB820-STRAPS
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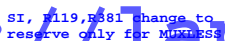
Rev	1A
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Date: Thursday, December 24, 2009 Sheet 16 of 42



	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V





RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

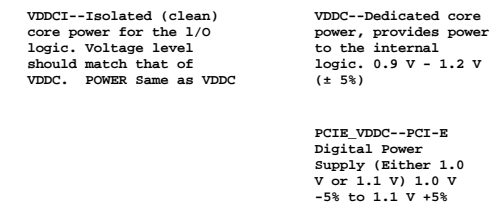


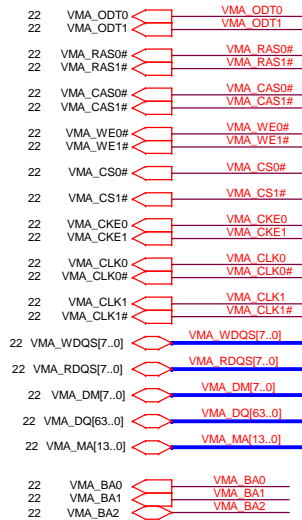
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.



PROJECT : AX2/7
Quanta Computer Inc.

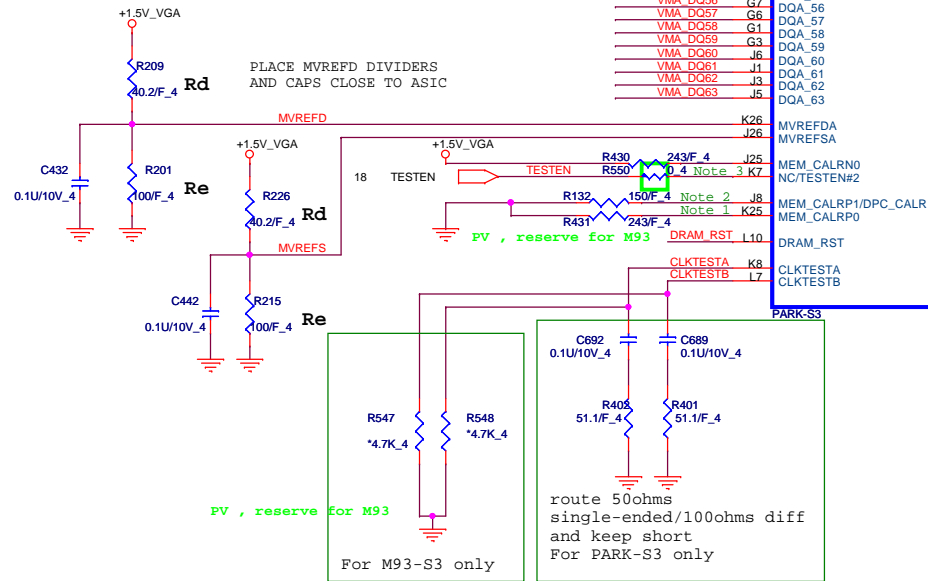
Size Custom	Document Number PARK_GND / LVDS/ Straps	Rev 1A
Date: Thursday, December 24, 2009	Sheet 19	of 42





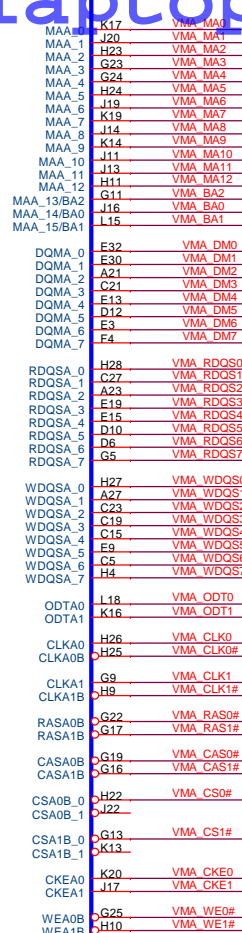
support 1gbt
VRAM (64M X 16)

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

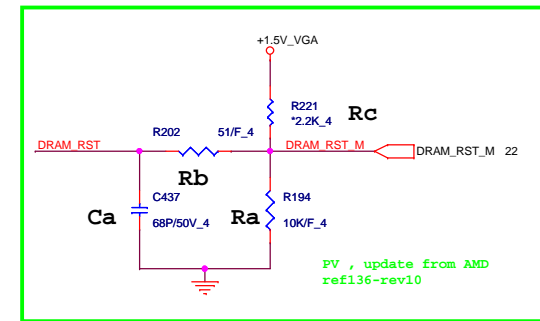


Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24

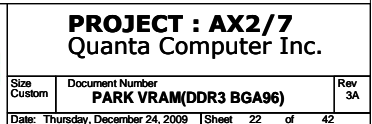
MEMORY INTERFACE

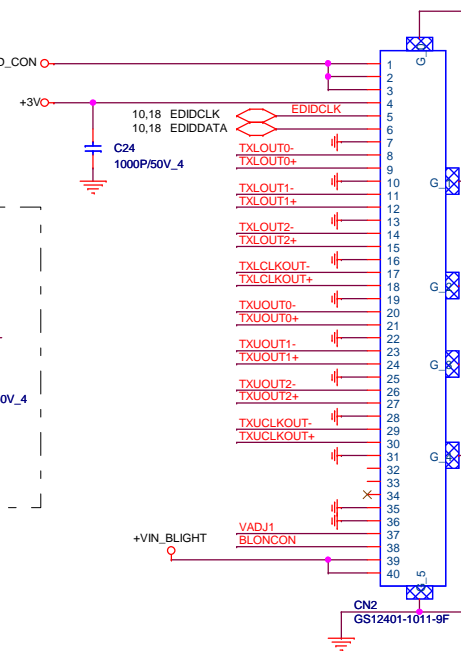
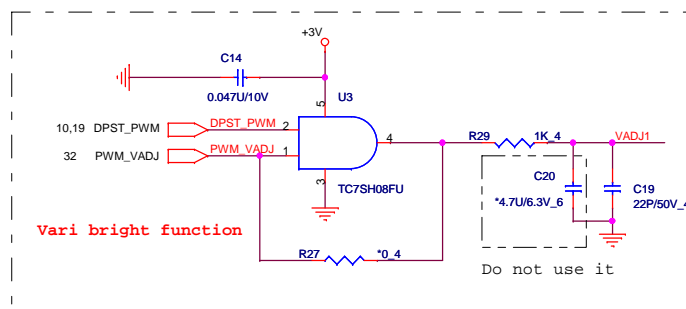
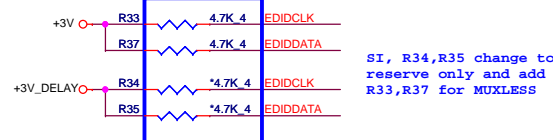
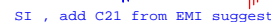


Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

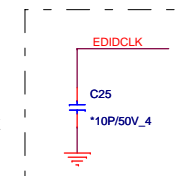
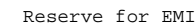


For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.

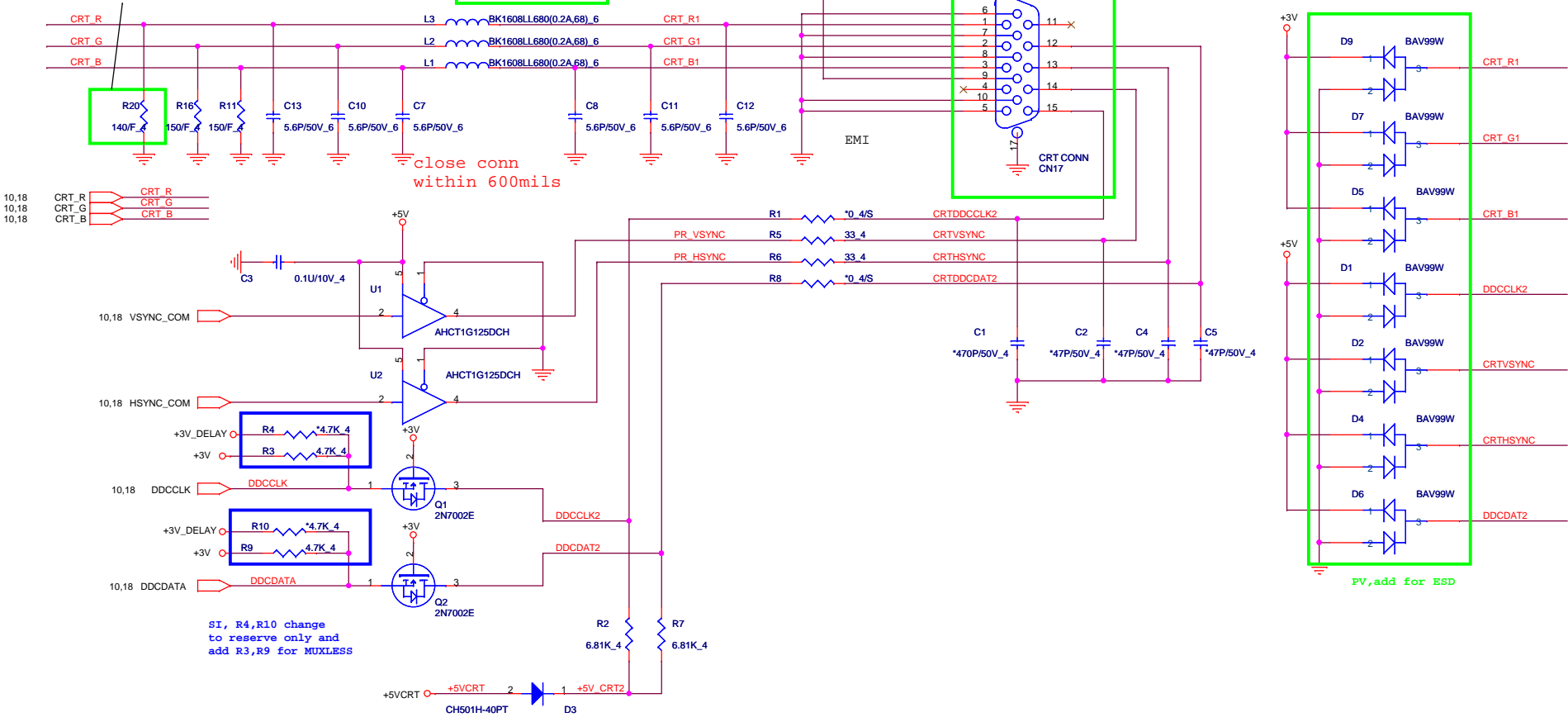




SI , update footprint
to 88266-05001-06-5P-L-SMT



R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)



10,18 CRT_R
10,18 CRT_G
10,18 CRT_B

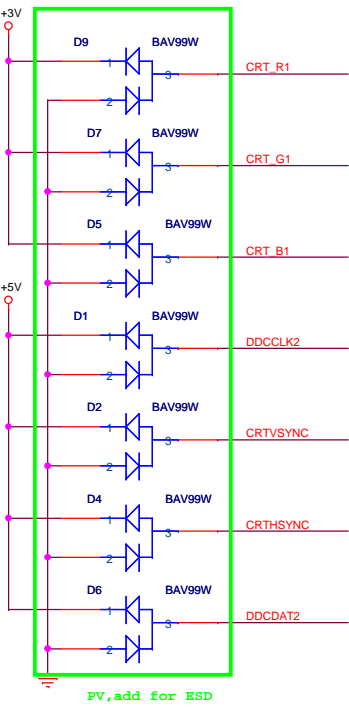
10,18 VSYNC_COM

10,18 HSYNC_COM

10,18 DDCCCLK

10,18 DDCCDATA





SI, R4,R10 change
to reserve only and
add R3,R9 for MUXLESS



PV,add for ESD

HDMI HPD SENSE

```
for Layout
concern
,placement close
HDMI conn
```

TX2 HDMI+L	3		4	0_4P2R_4	TX2 HDMI-
TX2 HDMI+L	2		2		TX2 HDMI+
RP11					
TX1 HDMI+L	3		4	0_4P2R_4	TX1 HDMI-
TX1 HDMI+L	2		2		TX1 HDMI+
RP10					
TX0 HDMI+L	3		4	0_4P2R_4	TX0 HDMI-
TX0 HDMI+L	2		2		TX0 HDMI+
L46					
TXC HDMI+L	4		3	WCM2012-90	TXC HDMI-
TXC HDMI+L	1		2		TXC HDMI+

PV, add for EMI

SI, change to reserve only for MUXLESS

for Layout concern, placement close HDMI conn

TXC HDMI-
TXC HDMI+

Close to HDMI Connector

PV , change footprint
to F3_2X1_65-2_8

Pin	Signal	Function
1	TX2 HDMI-	D2+ D2- D1+ D1- D0+ D0-
3	TX2 HDMI-	
4	TX1 HDMI+	
6	TX1 HDMI-	
7	TX0 HDMI-	
9	TX0 HDMI-	
10	TXC HDMI+	D2 Shield D1 Shield D0 Shield CK Shield GND
12	TXC HDMI-	
15	HDMI SCLK	DDC CLK CE Remote DDC DATA NC
16	HDMI SDATA	
18	+5V_HDMVCC	+5V
19	HDMI_DET	HP DET

18 EXT_TMDS_HPD

10 INT_TMDS_HPD 

Pure DIS : Add R85 , Q12

UMA / MUXLESS : Add R64 , R59 , Q11

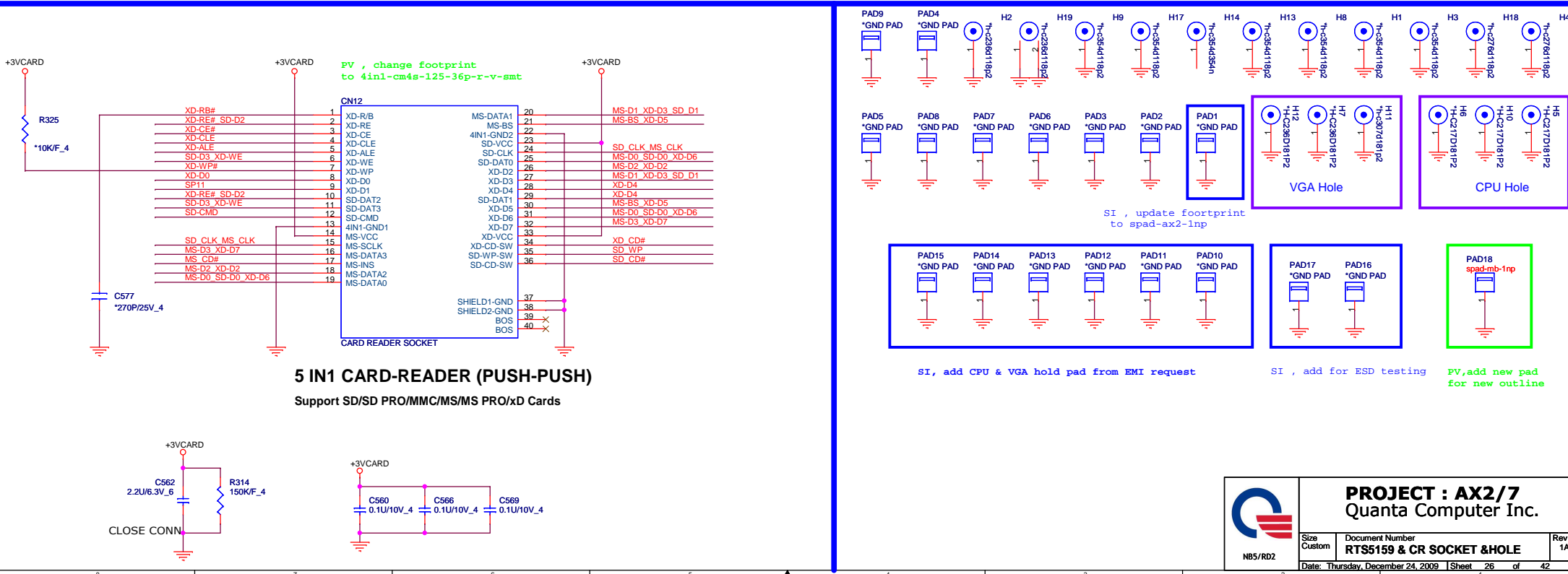
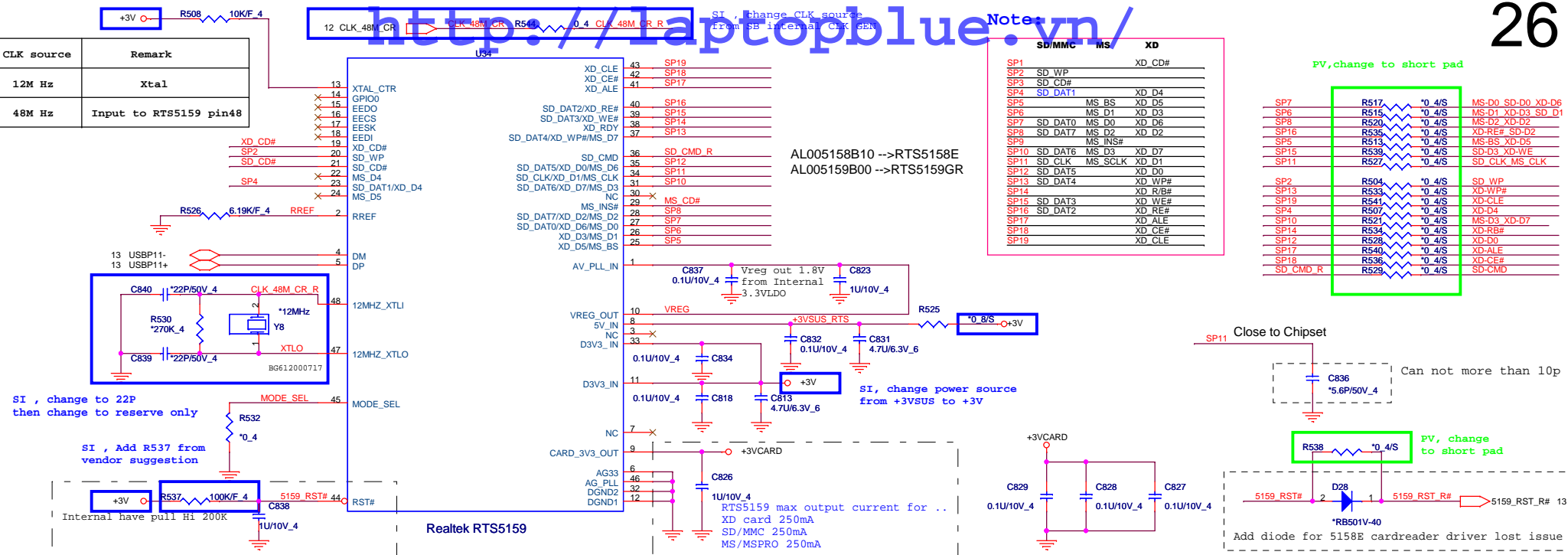
```
SI , add R64,R59,Q11
for MUXLESS
```

SI , change power source
to +5V HDMVCC

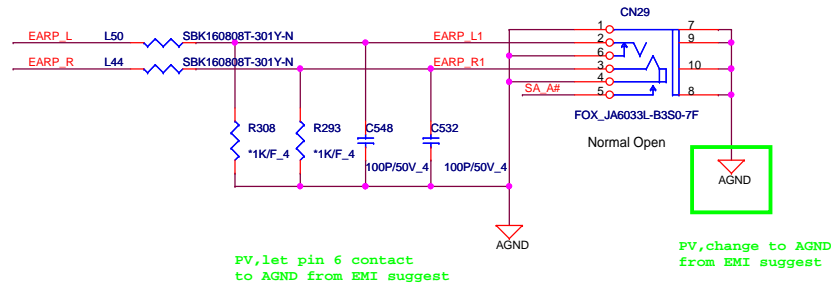
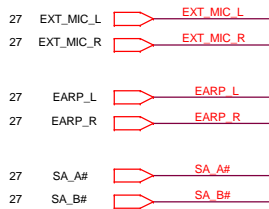
UMA DDC4 is 5V
tolerance , the MOSFET
level shifter no need
Discrete DDC is 3V
tolerance, the MOSFET
level shifter is need

SI, remove R93 , R350 . Add RP30
R94,R351,Q14,Q15 change to
reserve only for MUXLESS

PIN 13	CLK source	Remark
Floating	12M Hz	Xtal
Pull high	48M Hz	Input to RTS5159 pin48

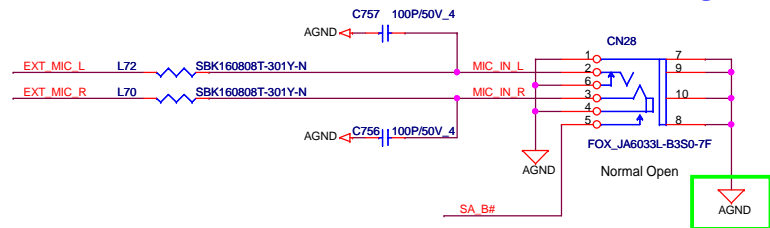




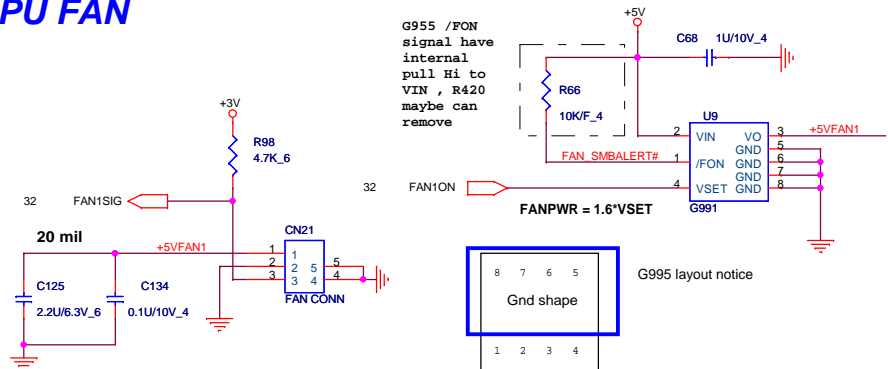


SA_A# -->EXT Ear Phone

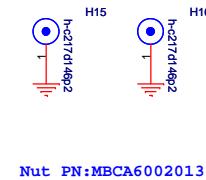
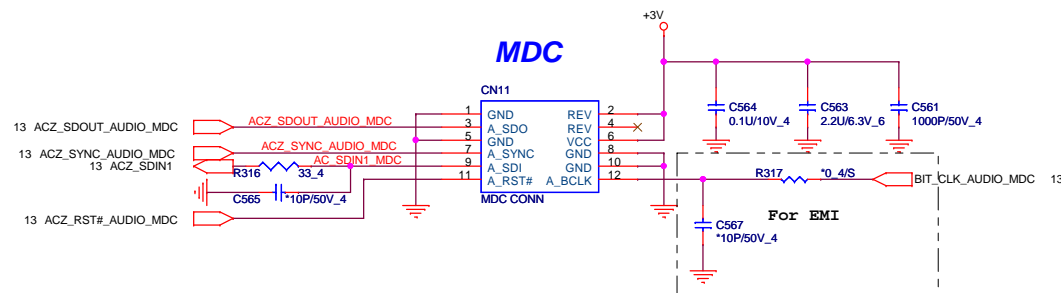
SA_B# -->EXT MIC



CPU FAN



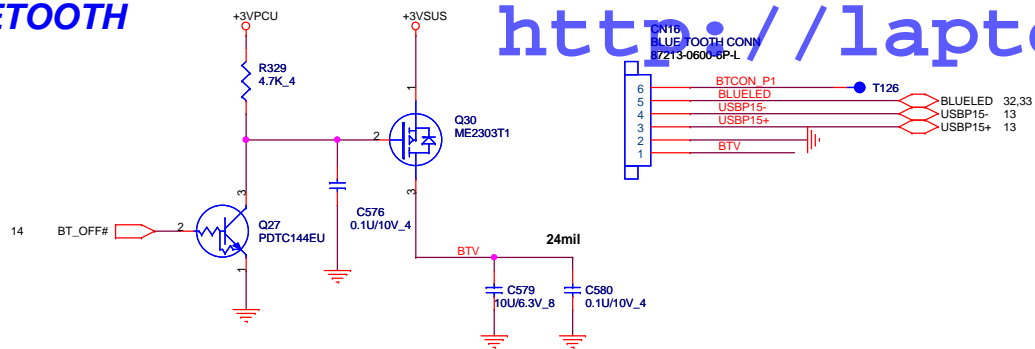
Modem CONN



PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/MDC1.5/CPU FAN	1A
Date: Thursday, December 24, 2009	Sheet 28	of 42

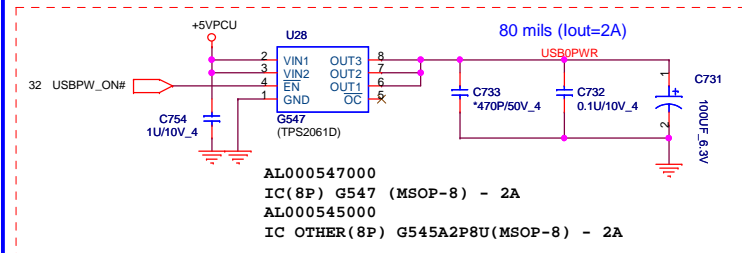
BLUETOOTH



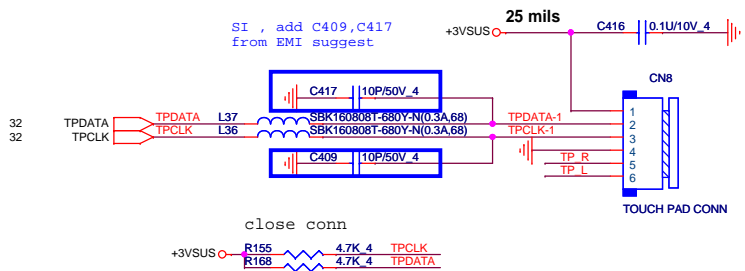
<http://laptopblue.vn/>

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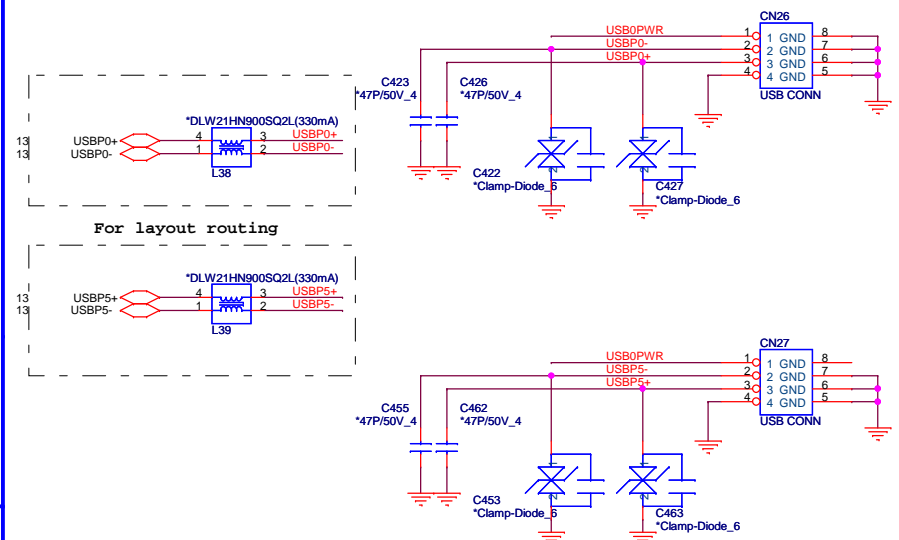
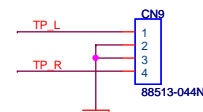
LEFT SIDE USBX2



TOUCH PAD CONN



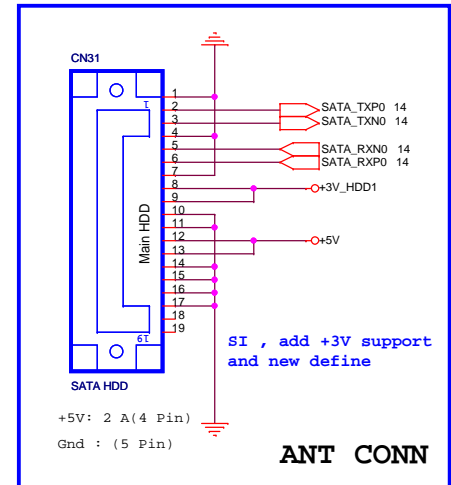
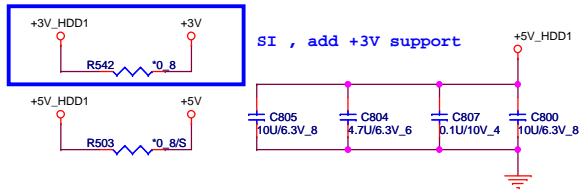
To TOUCH PAD SW board



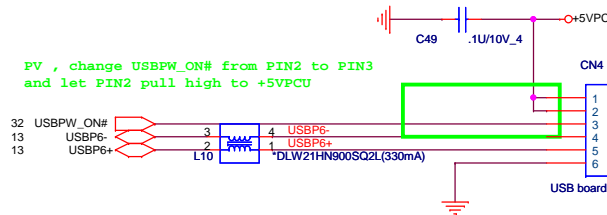
SATA HDD CONNECTOR

SI , update P/N : DFHS13FS019

SI , delete CN30 change to ANT CONN

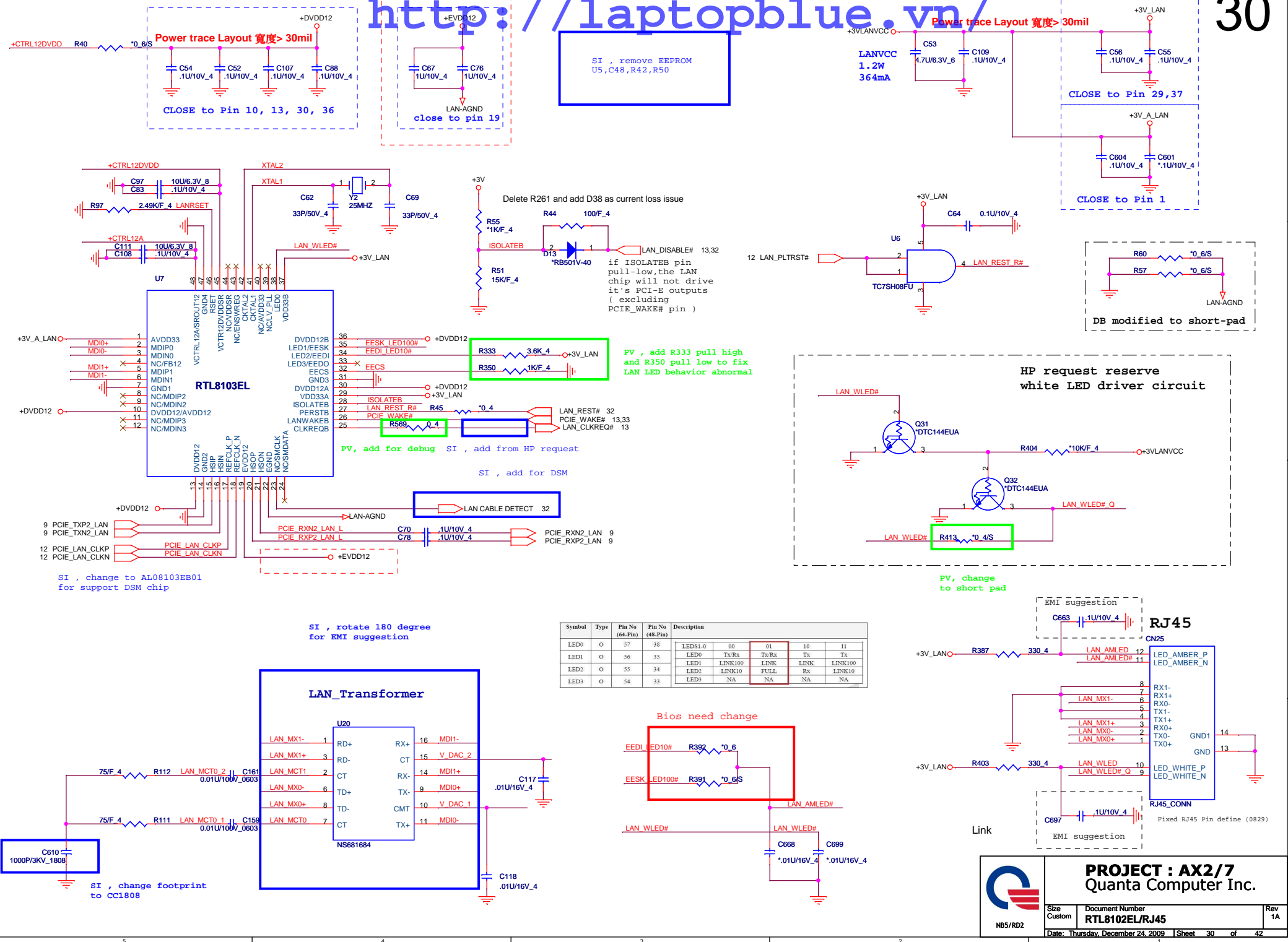


Right SIDE USBX1



PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A
Date: Thursday, December 24, 2009 Sheet 29 of 42		

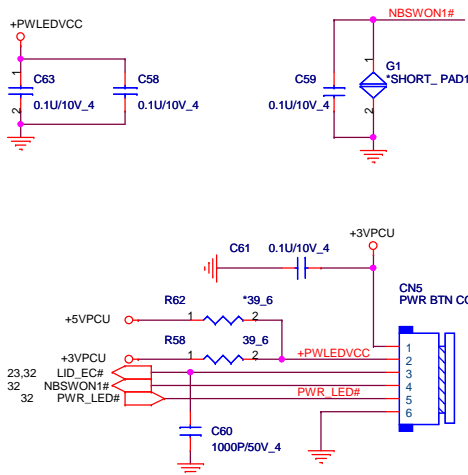


POWER BUTTON CONNECTOR

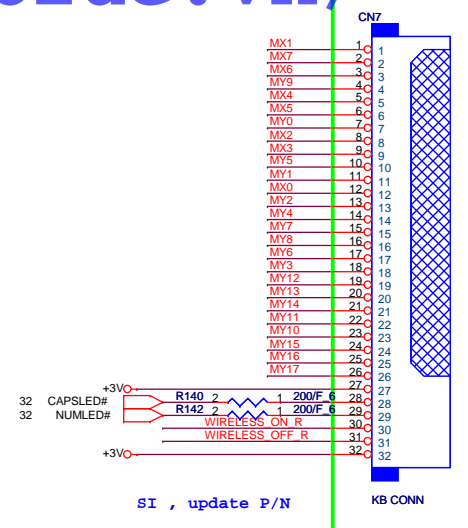
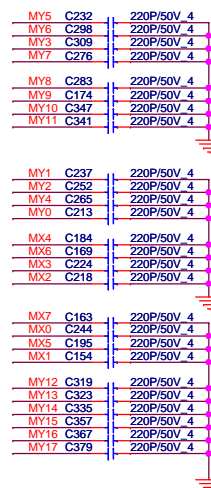
KEYBOARD CONN

PV, update footprint to b1135h-32r1a-tand-32p-1-sm

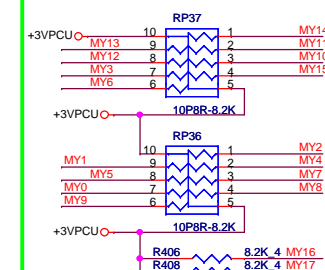
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1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWLED#
6. GND

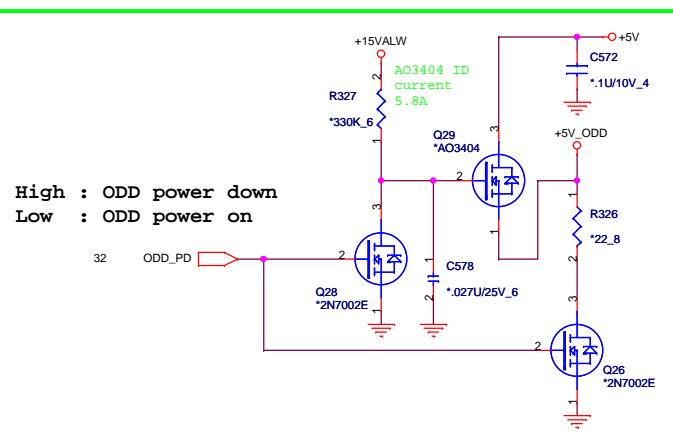
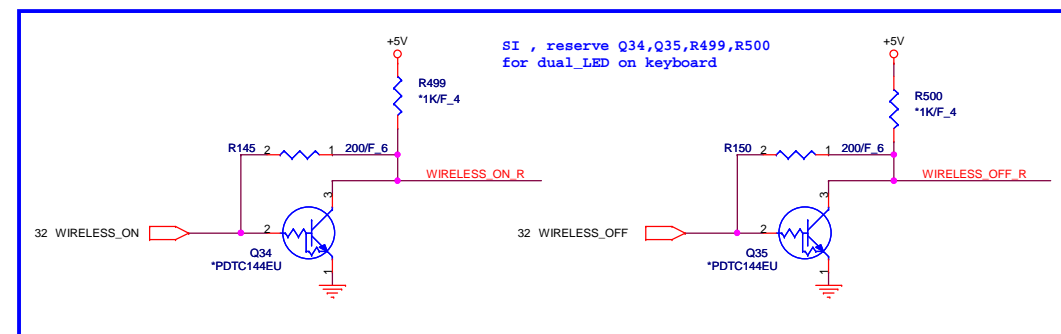
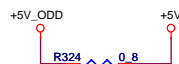
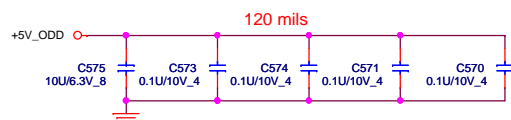
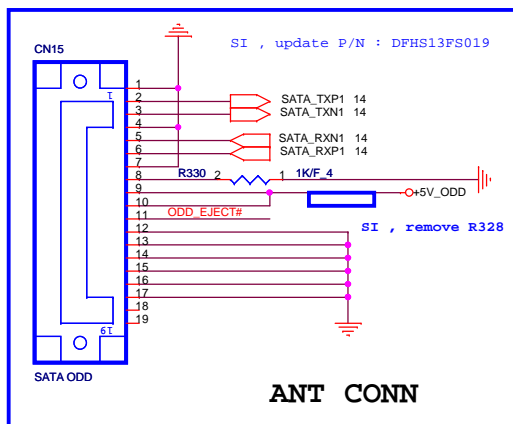


KEYBOARD PULL-UP

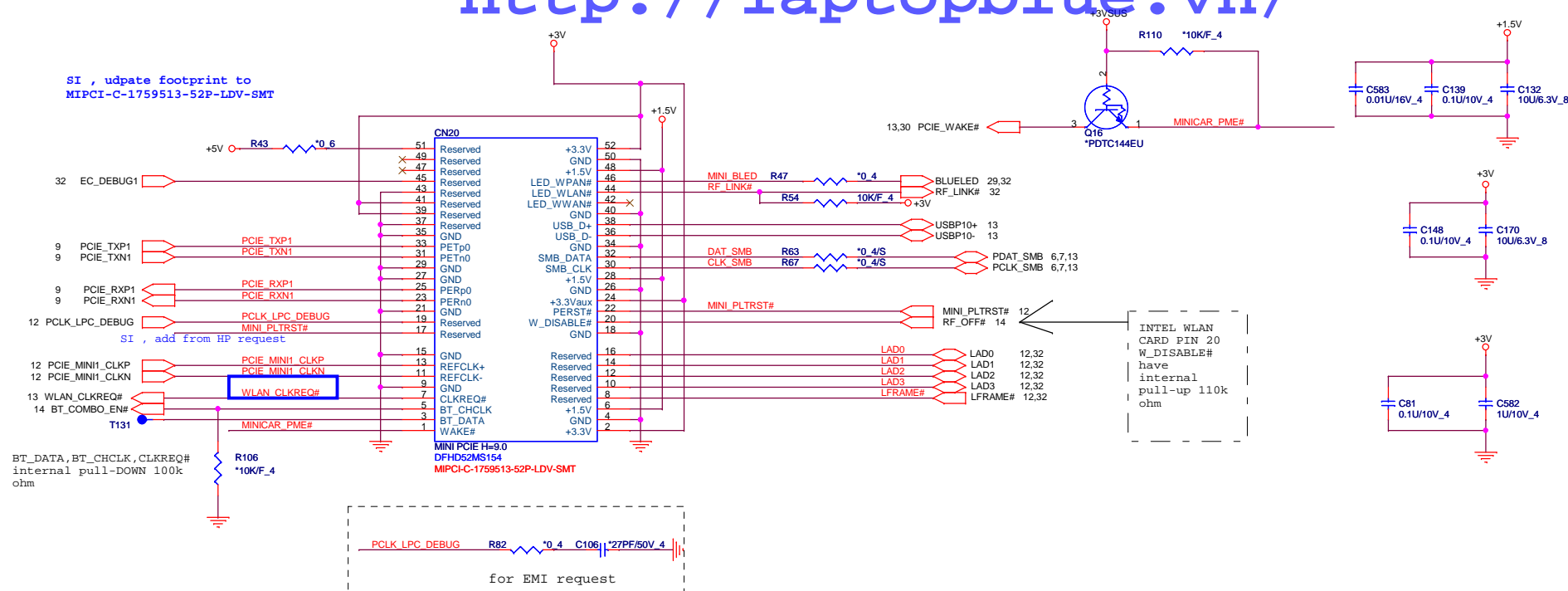


SATA CD-ROM

SI , delete CN13 change to ANT CONN



PV, change to reserve only



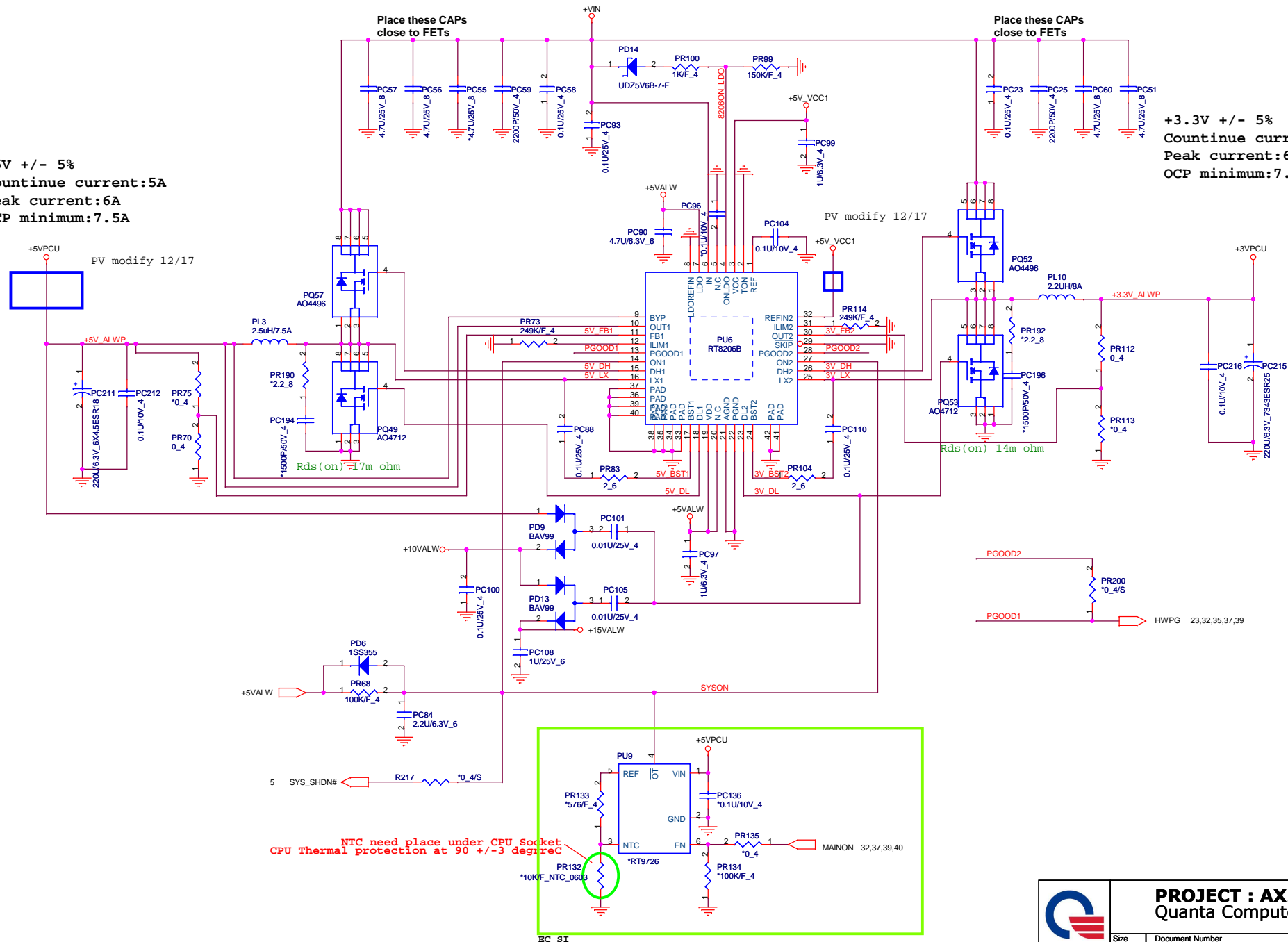
INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm



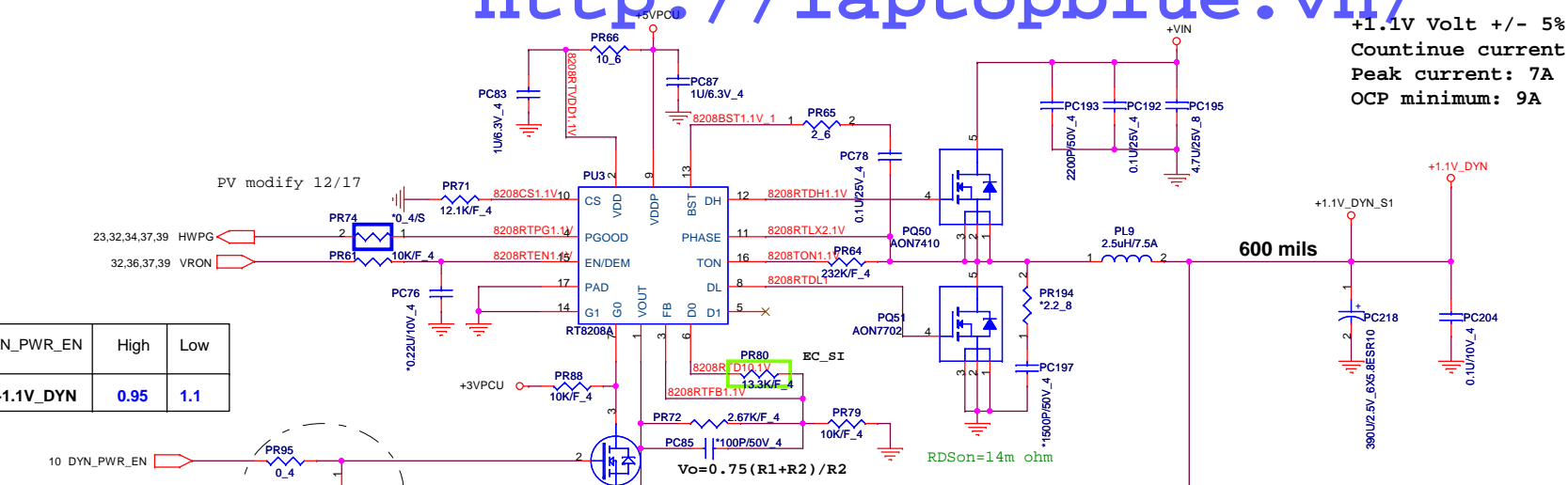
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number Mini CARD/LED	Rev 1A
Date: Thursday, December 24, 2009	Sheet 33	of 42

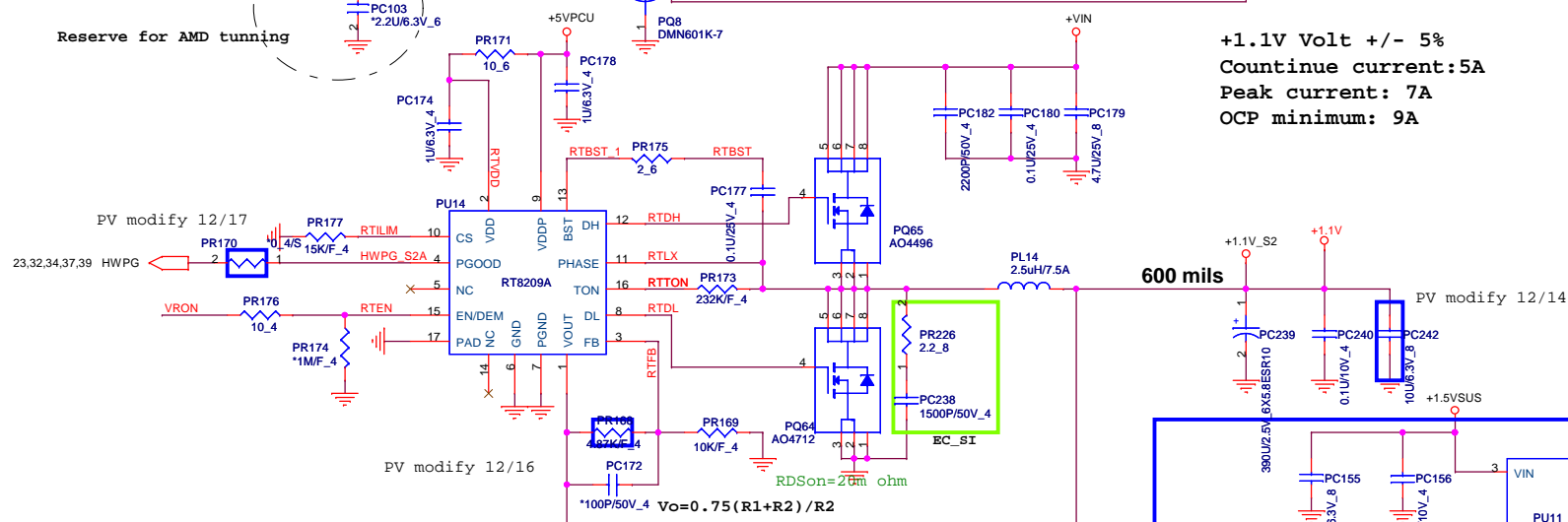
+3.3V +/- 5%
Continue current:5A
Peak current:6A
OCP minimum:7.5A



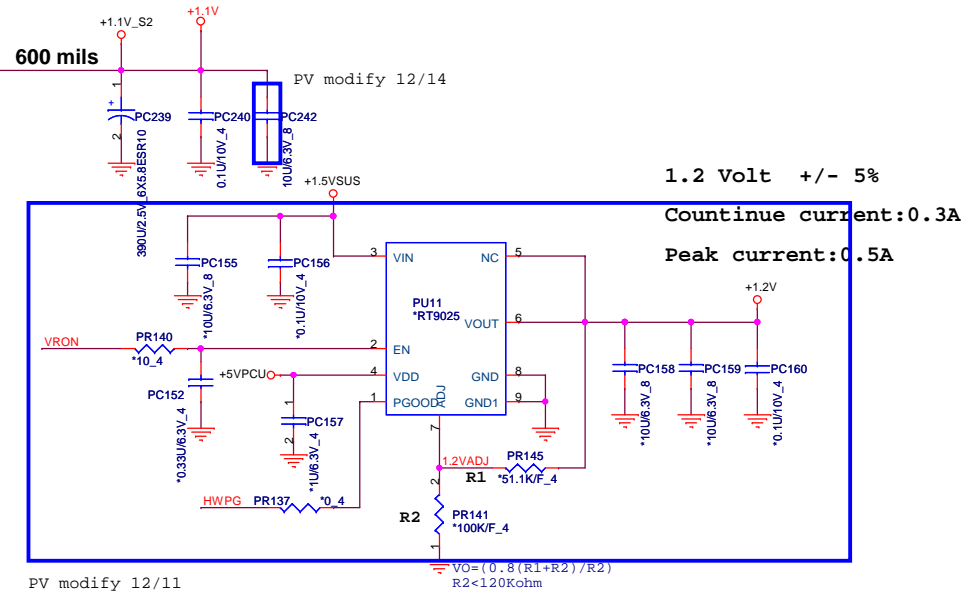
DYN_PWR_EN	High	Low
+1.1V_DYN	0.95	1.1



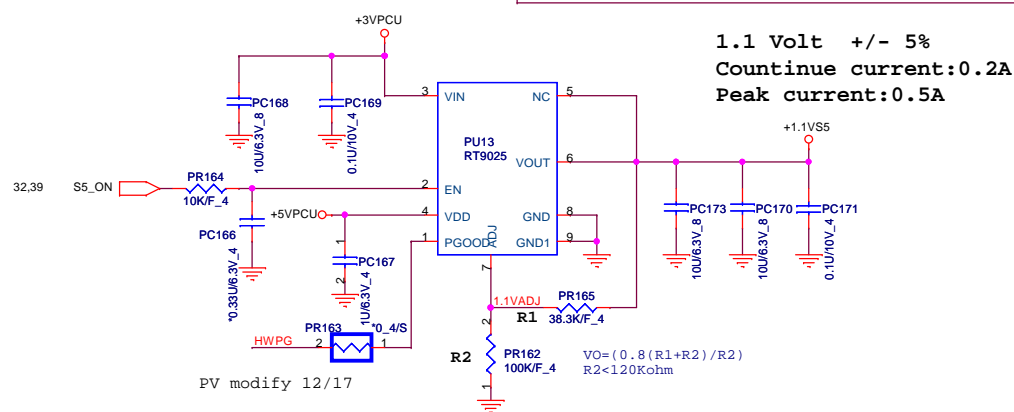
+1.1V Volt +/- 5%
Continue current: 5A
Peak current: 7A
OCP minimum: 9A



+1.1V Volt +/- 5%
Continue current: 5A
Peak current: 7A
OCP minimum: 9A



```
1.2 Volt +/- 5%
Continue current:0.3A
Peak current:0.5A
```

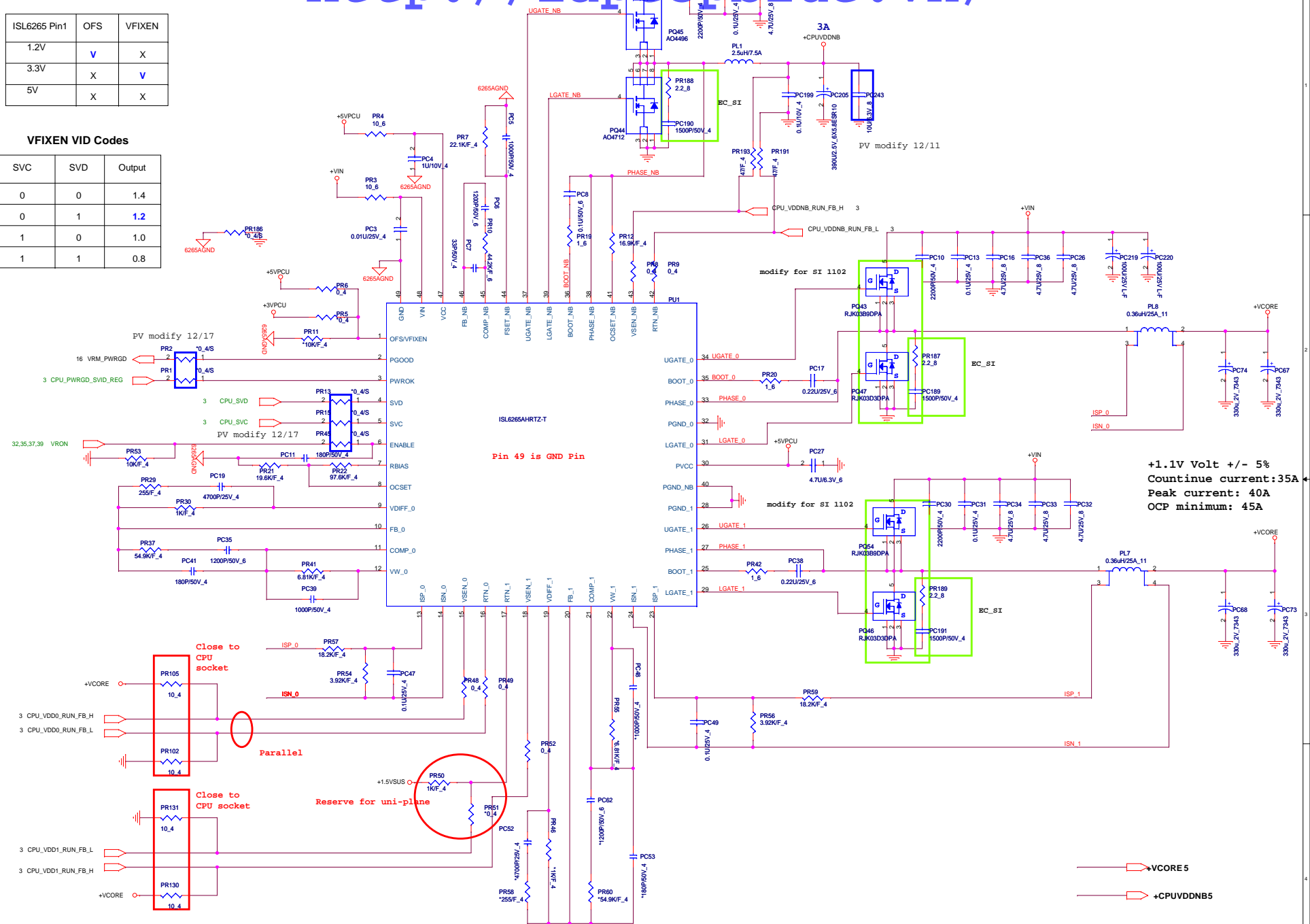


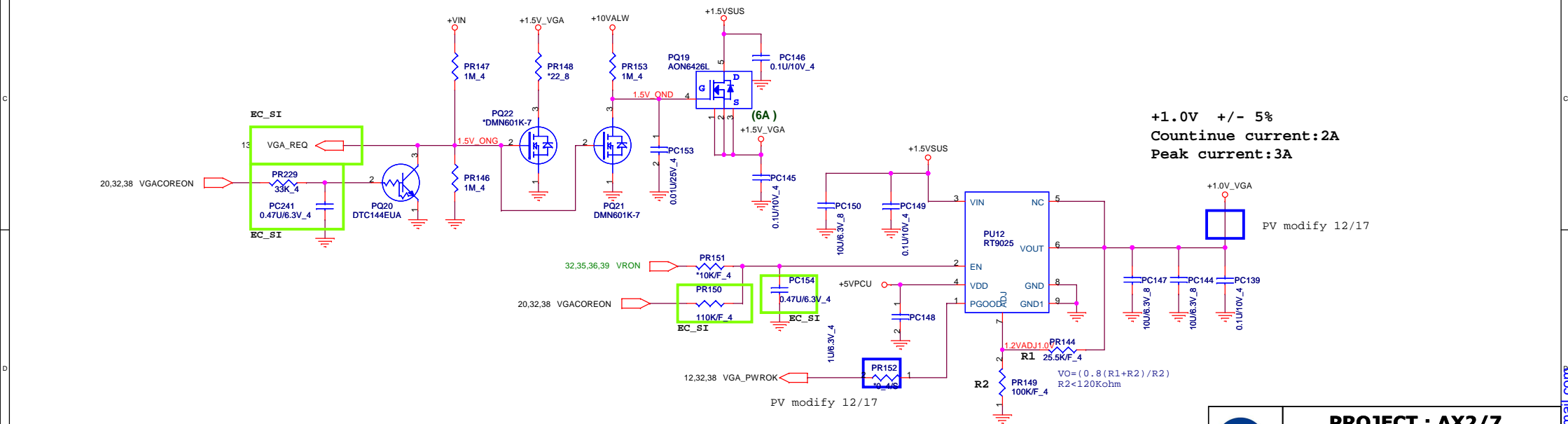
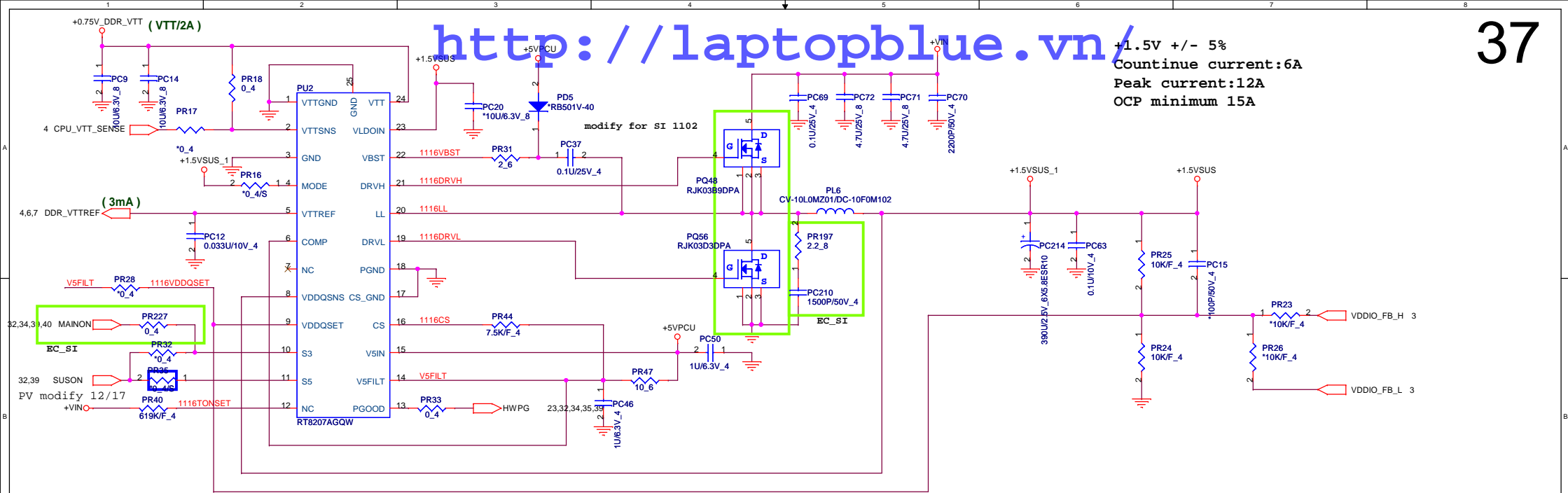
1.1 Volt +/- 5%
Continue current:0.2A
Peak current:0.5A

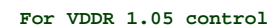
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

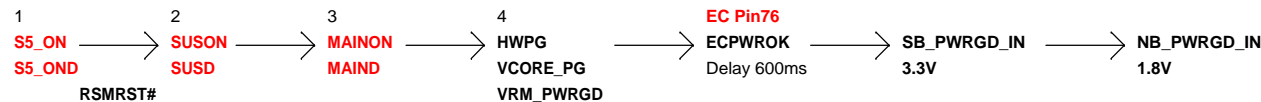
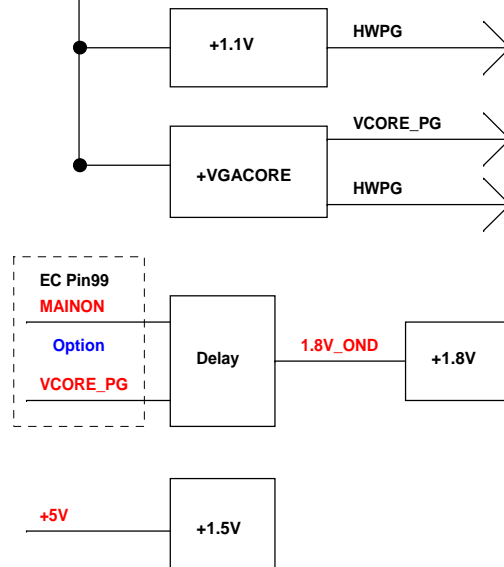
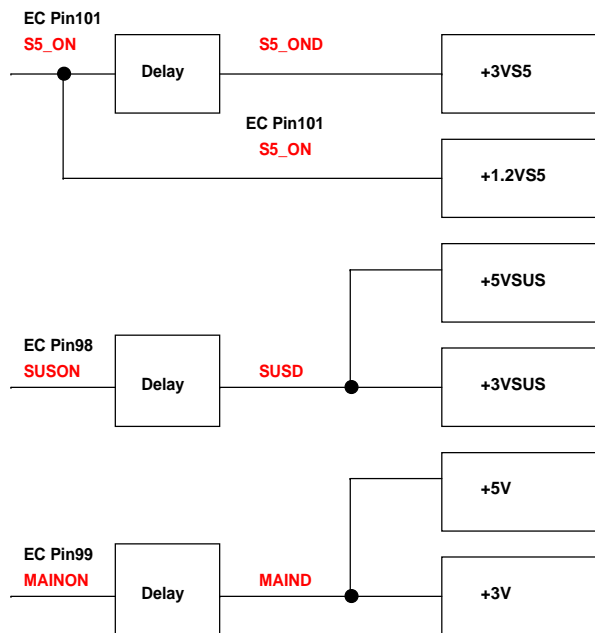
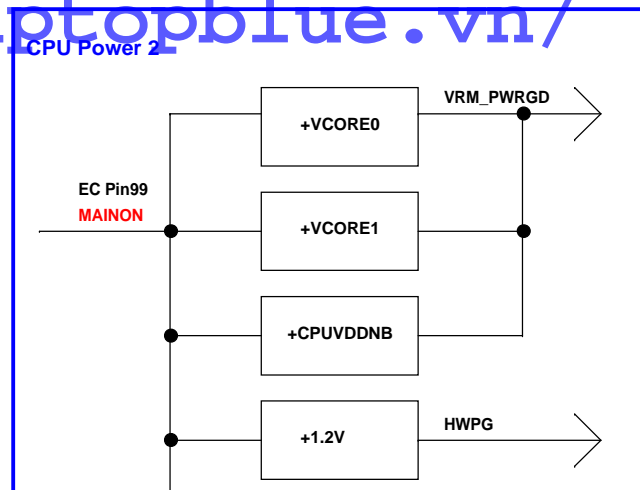
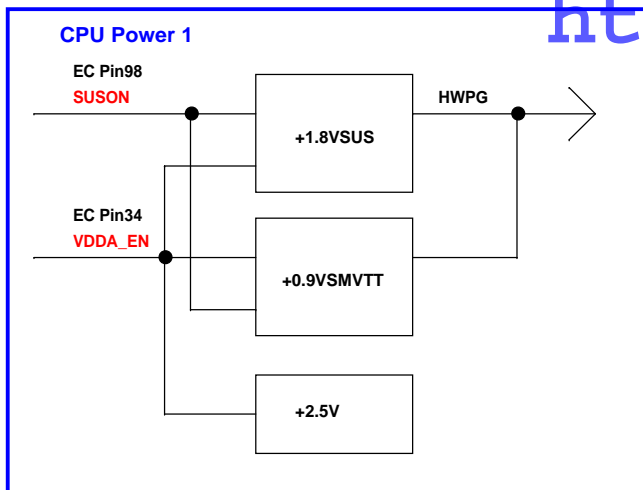
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8











Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

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SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT