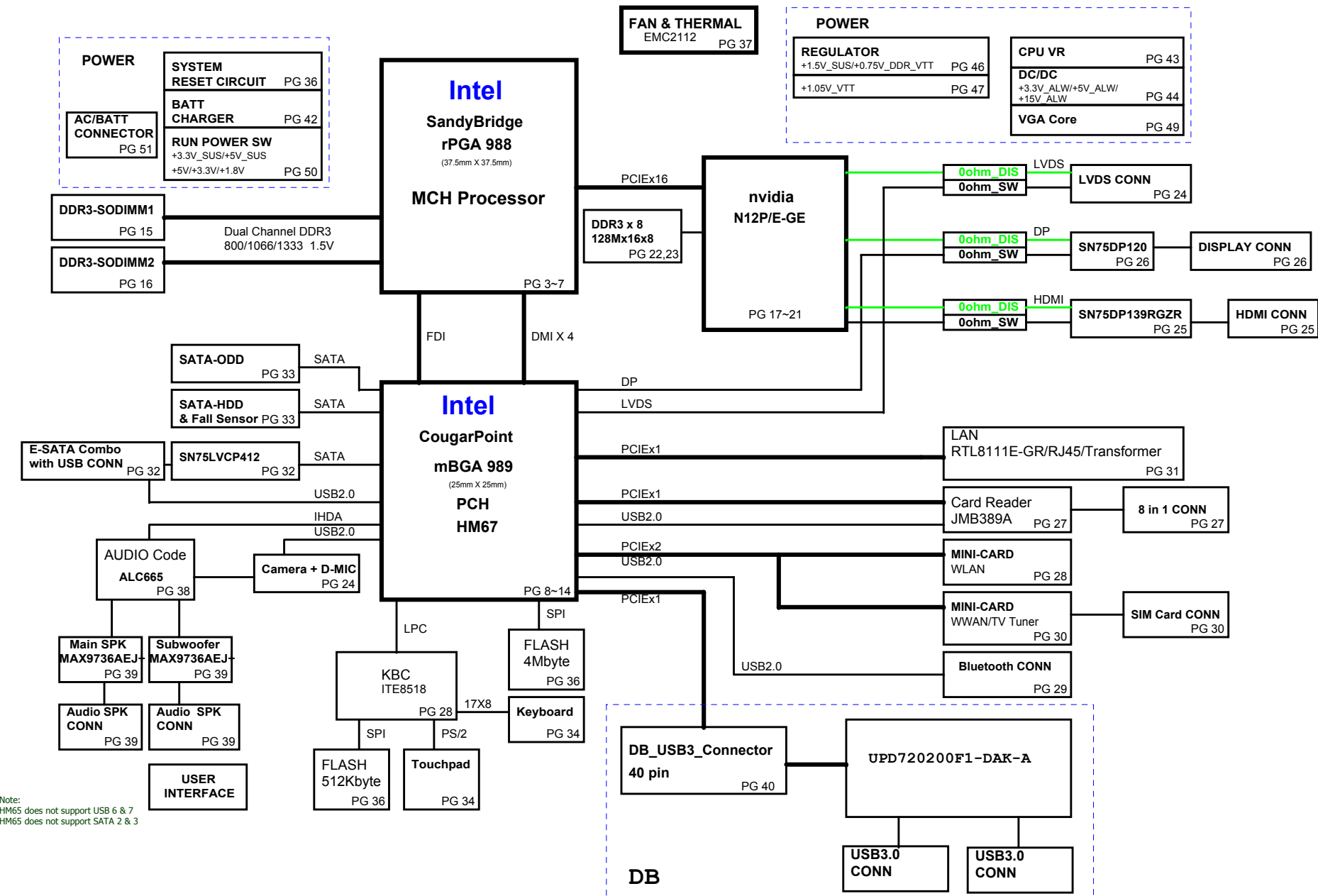


GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:

_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only




Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Table of Contents

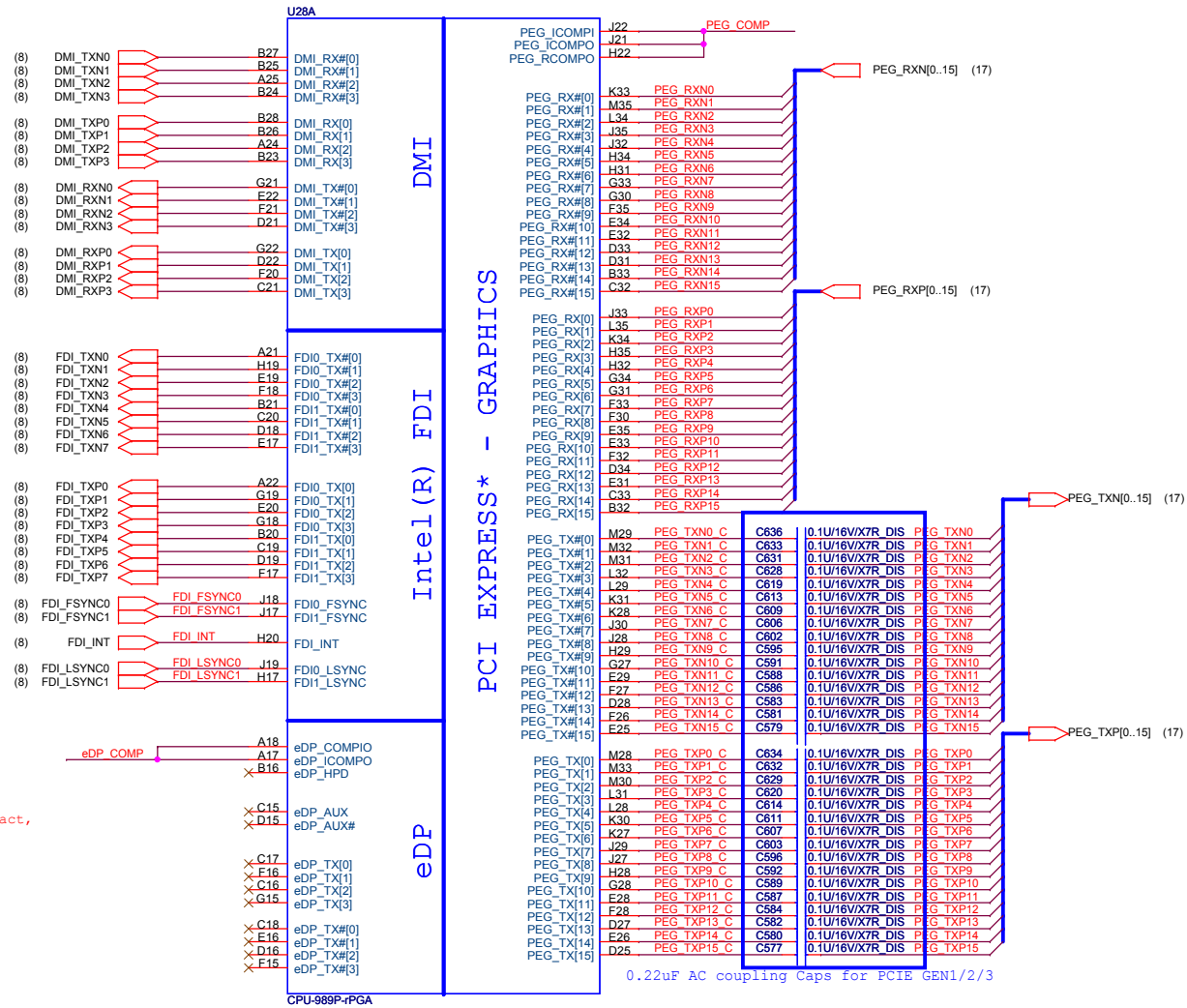
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-7	Sandy Bridge
8-14	PCH
15-16	DDRIII SO-DIMM(204P)
17-21	N12P-GE/N12P-GT
22-23	VRAM
24	LCD CONN
25	HDMI CONN
26	MINI DP CONN
27	Card Reader (JMB389)
28	SIO (ITE8502)
29	MINI-Card (WLAN/WPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
32	Right USB/ESATA
33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FLASH / RTC/ RESET CIRCUIT
37	FAN / THERMAL
38	AUDIO CODEC
39	AUDIO AMP
40	Left USB/MMB CONN
41	BLANK
42	Charger (ISL88731)
43	CPU CORE(NCP6131S)
44	3V/5V (TPS51427A)
45	1.8V_RUN(RT8015DGQW)
46	1.5_DDR/0.75(RT8207A)
47	1.05V_VTT(VT358)
48	VCCSA(TPS51461)
49	VGA_N12x-dGFX(NCP3218MNR)
50	Run Power Switch
51	DCin & Batt
52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	power sequence(DIS)
58	power sequence(UMA)
59	power sequence(OPTIMUS)

Power States

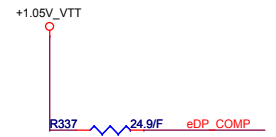
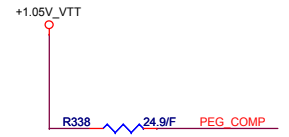
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation



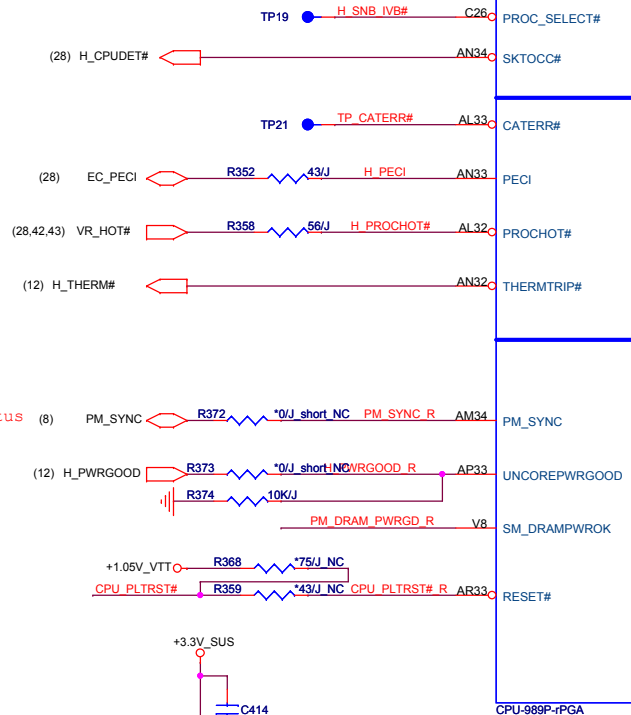
0.22uF AC coupling Caps for PCIe GEN1/2/3



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

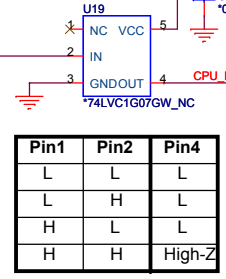


shut down when asserted
Over 130 degree C will
drive low

provide power management status
(form PCH to CPU)

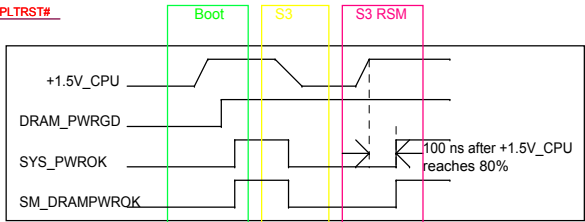
IN	OUT
L	L
H	High-Z

(11,17,27,28,29,30,31,40) PLTRST#

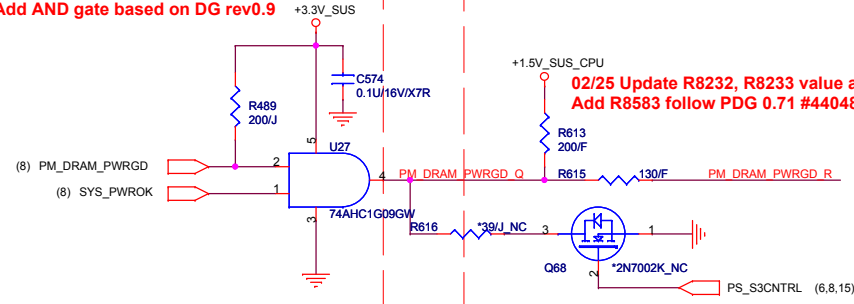


Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z

level shift for reset pin(07/12)



3/16 Change topology;
Add AND gate based on DG rev.0.9



02/25 Update R8232, R8233 value and routing,
Add R8583 follow PDG 0.71 #440484

PS_S3CNTRL (6,8,15)

MISC

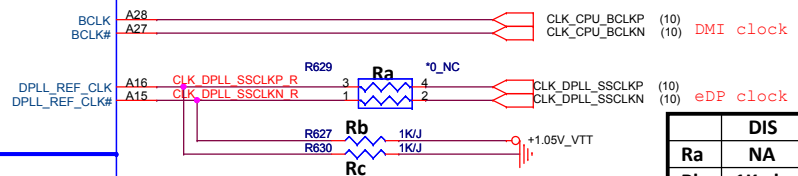
THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM



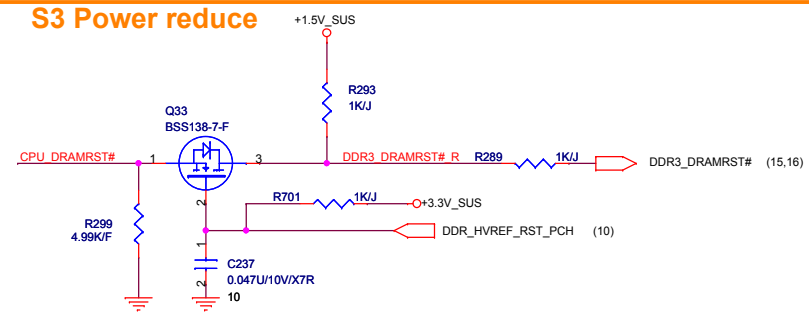
	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

26.1 change to 25 ohm

S3 Power reduce

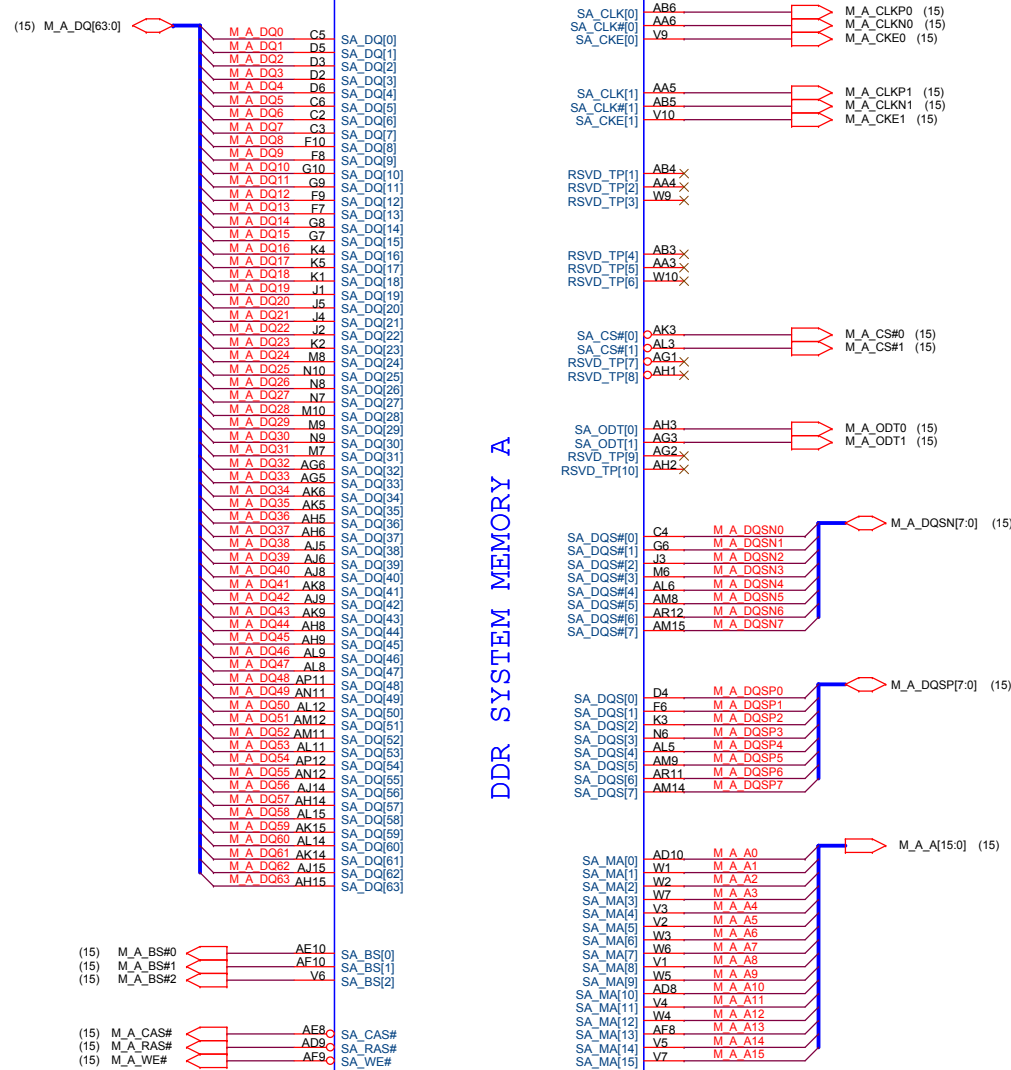
+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3
(Because can't reset DRAM when into S3)

S3 Power reduce



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

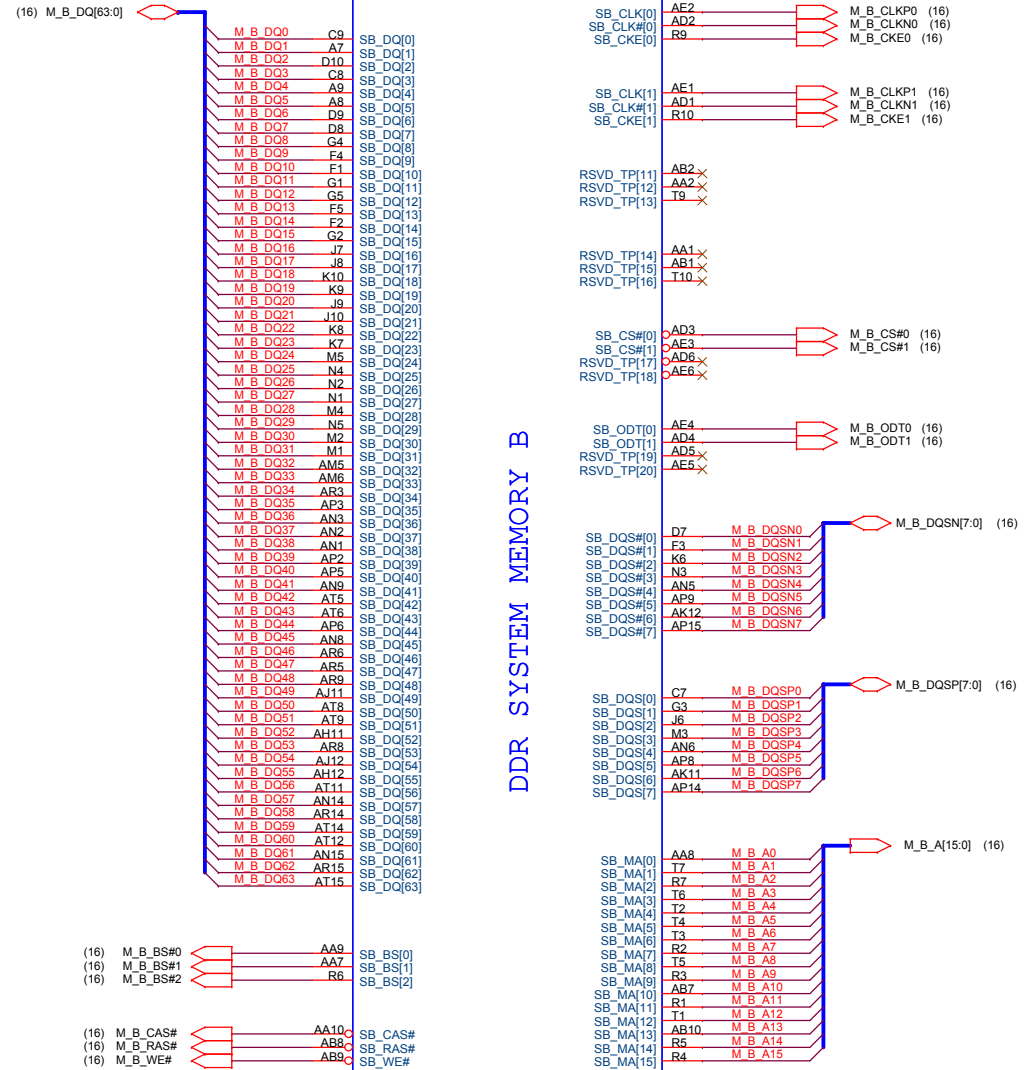
U28C



CPU-989P-IPGA

DDR SYSTEM MEMORY A

U28D



CPU-989P-IPGA

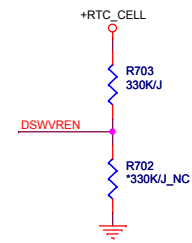
DDR SYSTEM MEMORY B



Quanta Computer Inc.

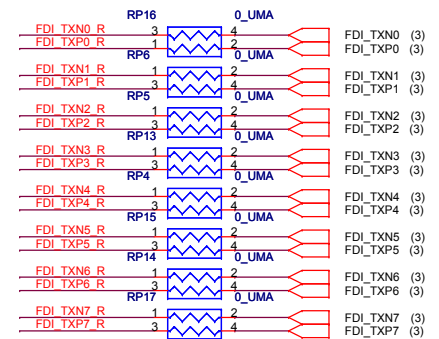
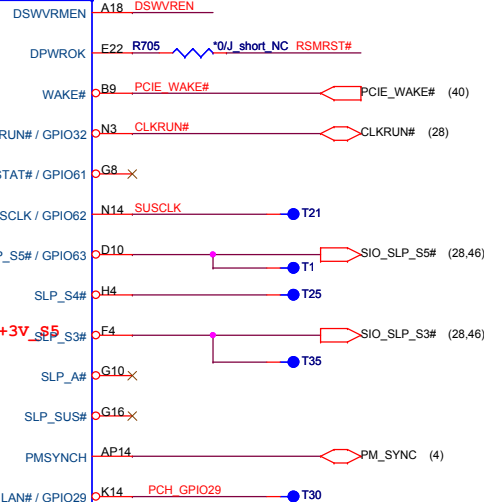
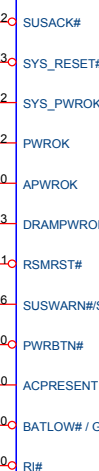
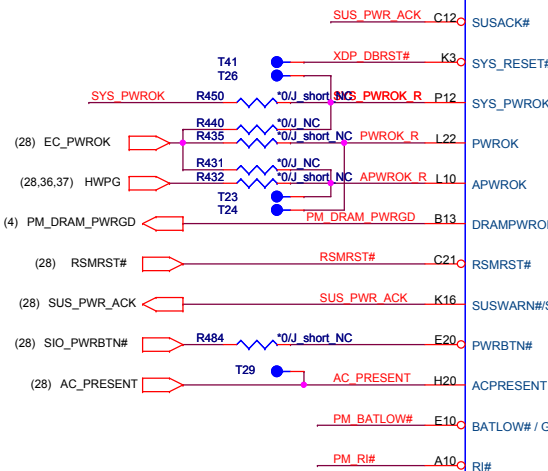
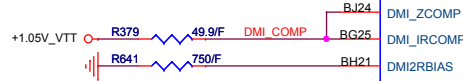
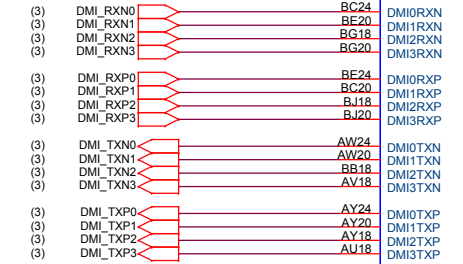
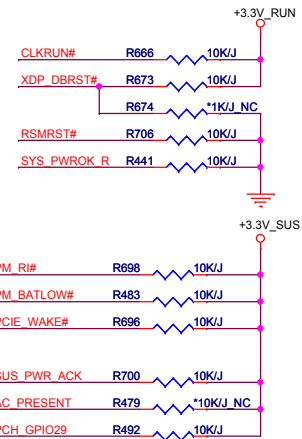
PROJECT : GM6C MLK DIS

Cougar Point (DMI, FDI, PM)

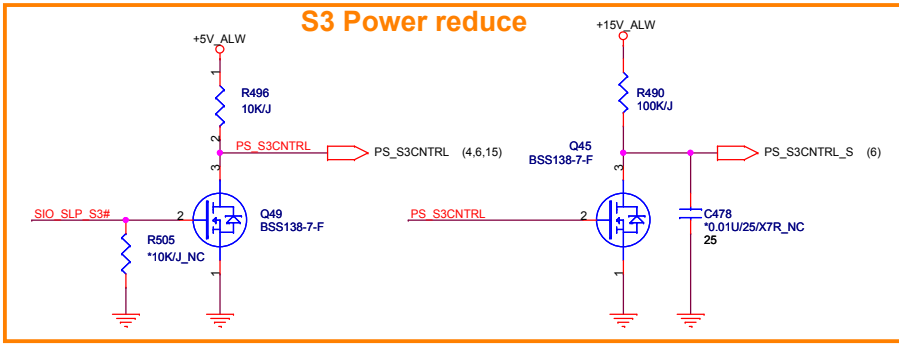


On Die DSW VR Enable
High = Enable (Default)
Low = Disable

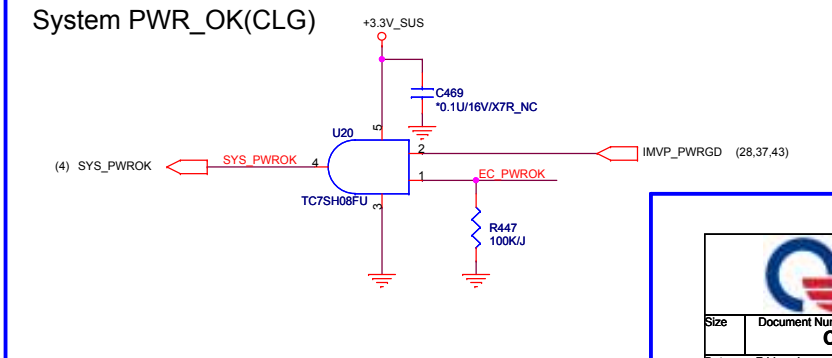
PCH Pull-high/low(CLG)



S3 Power reduce




System PWR_OK(CLG)

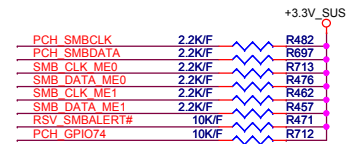
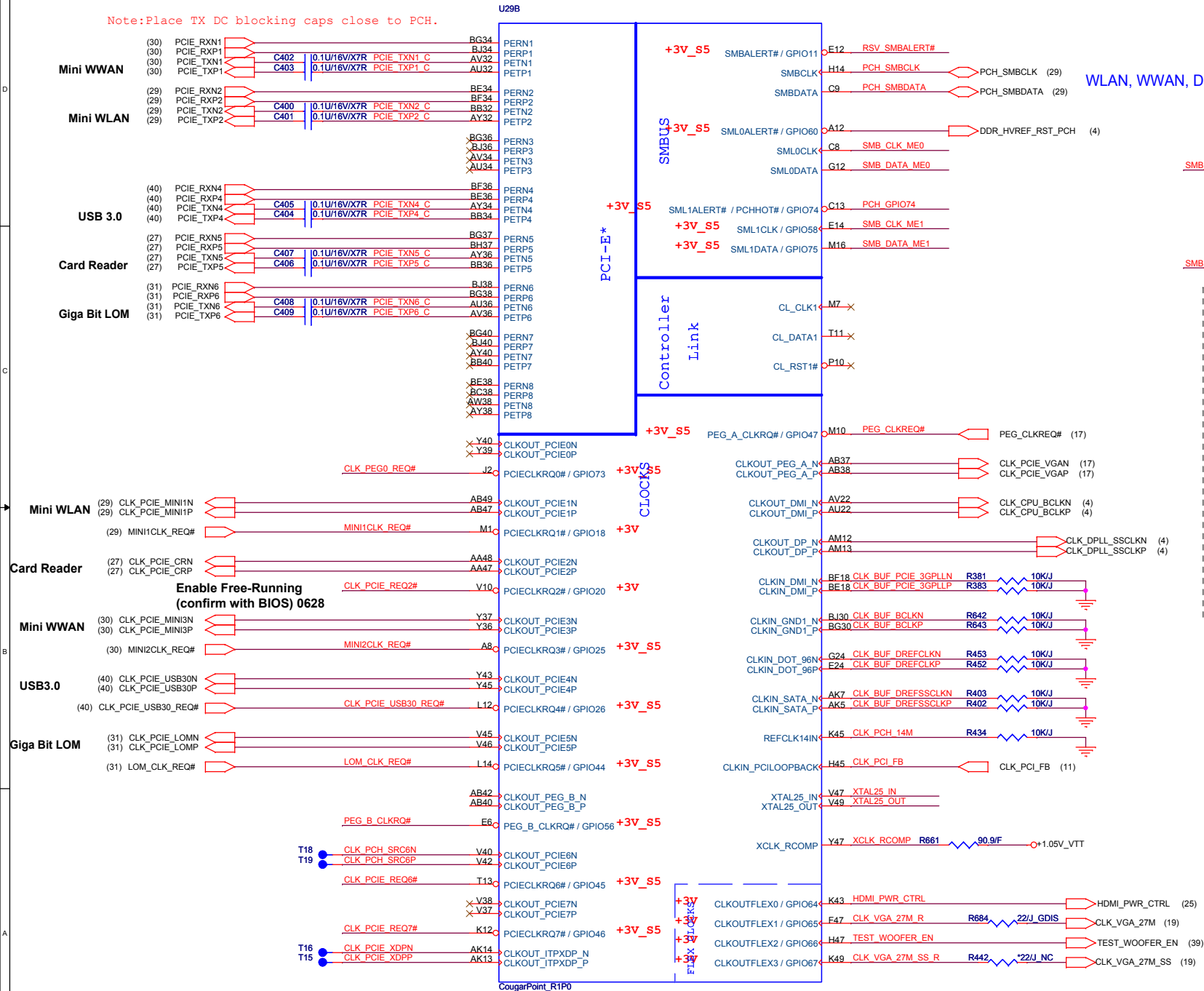




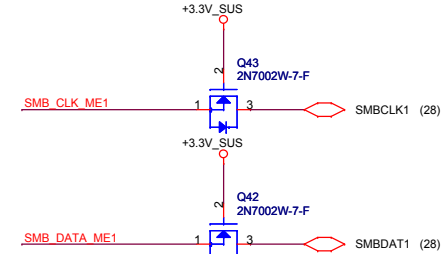
PCH Strap Table

 Quanta Computer Inc. PROJECT : GM6C MLK DIS	
Size	Document Number
Cougar Point 2/7	
Date: Friday, January 07, 2011	Sheet 9 of 59

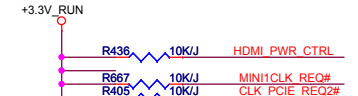
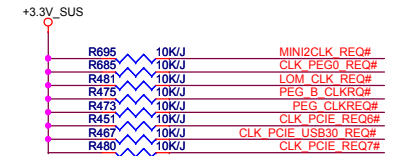
Note: Place TX DC blocking caps close to PCH.



WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor



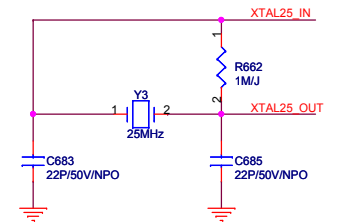
PCIe Clock Request

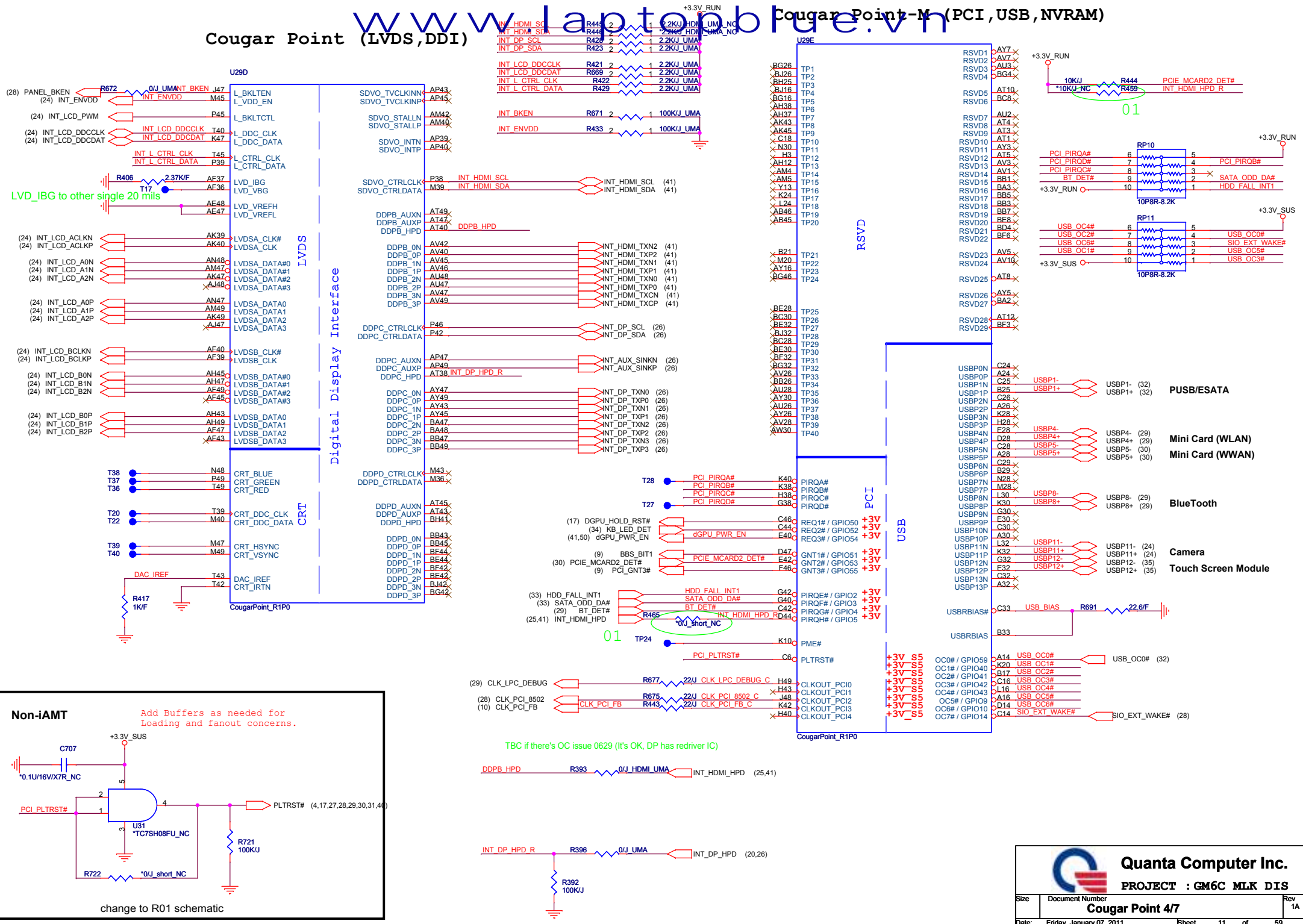


PCIeCLKRQ[0,3,4,5,6,7]# should have a 10K pull-up to +V3.3A. PCIeCLKRQ[1,2] should have a 10K pull-up to +3.3S

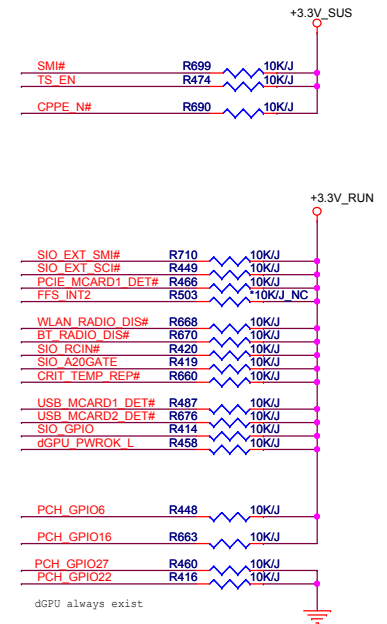
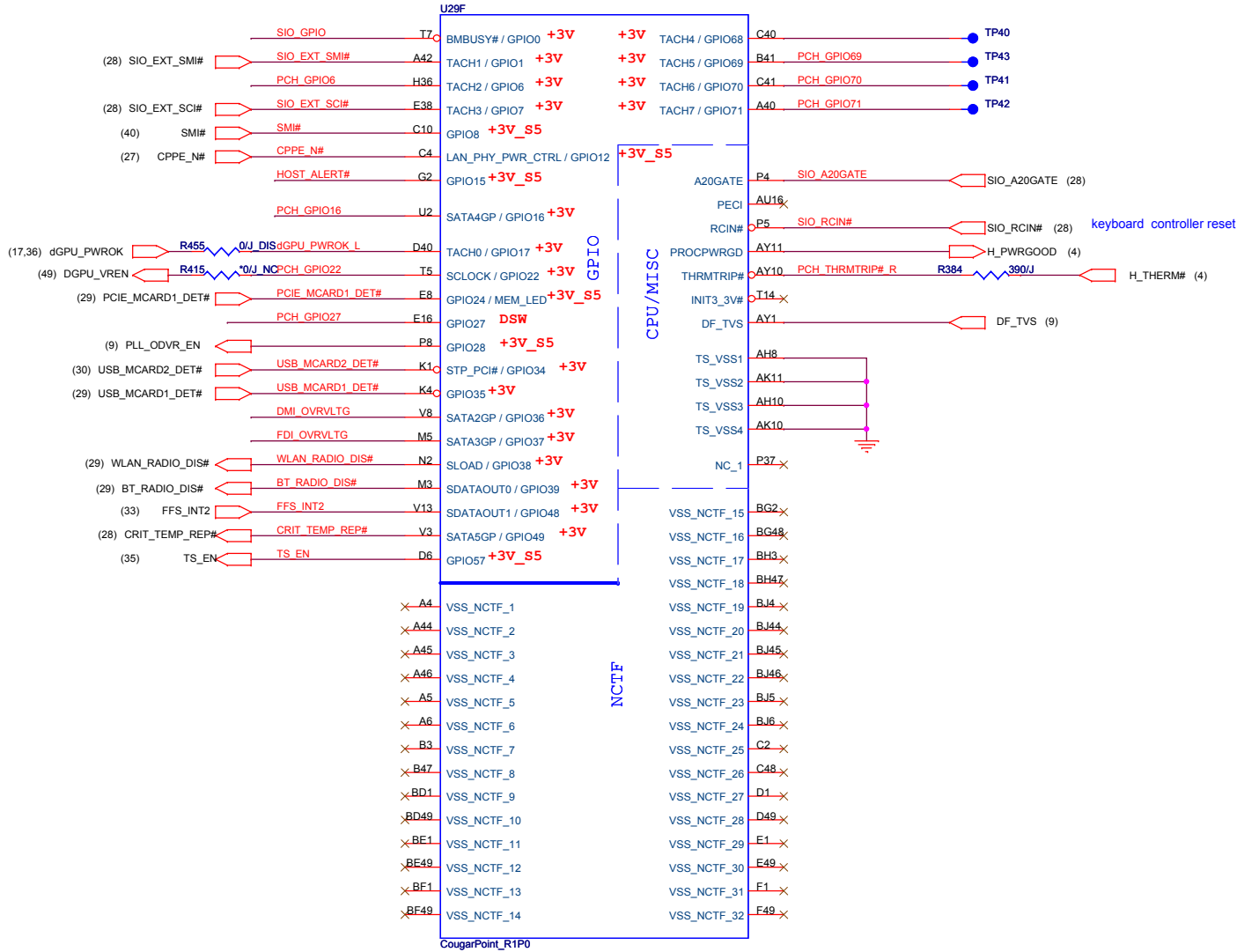
Change as big package (UM9)

25MHz Clock for DCI Function





Cougar Point (GPIO,VSS_NCTF,RSVD)



FDI TERMINATION VOLTAGE OVERRIDE

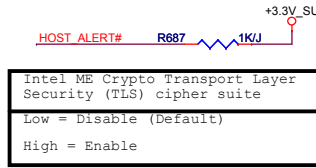
LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)



Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

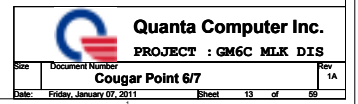
High = Enable



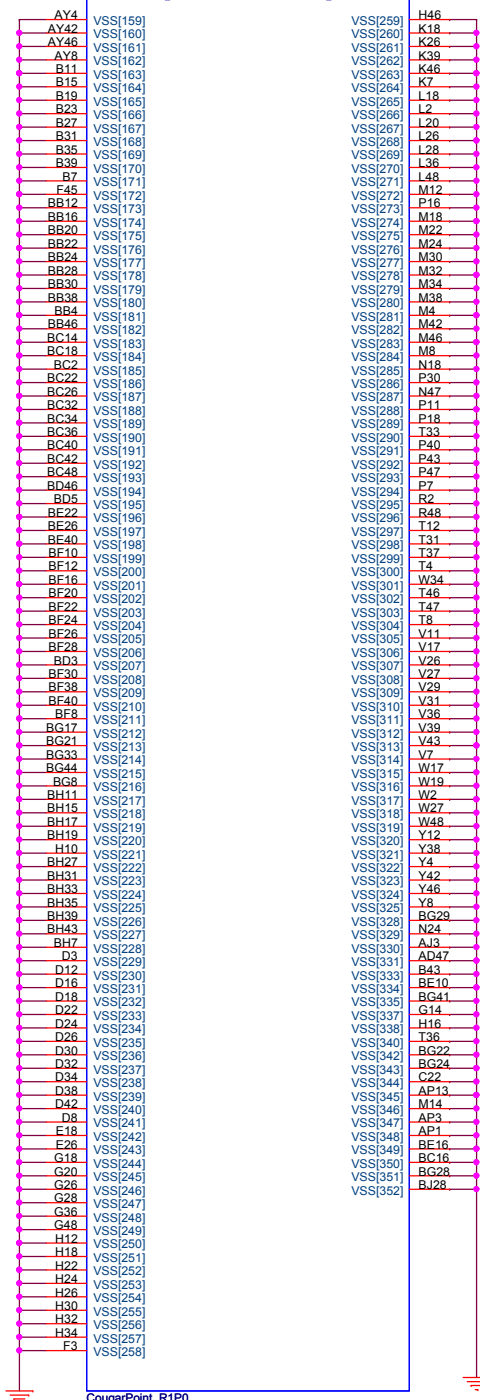
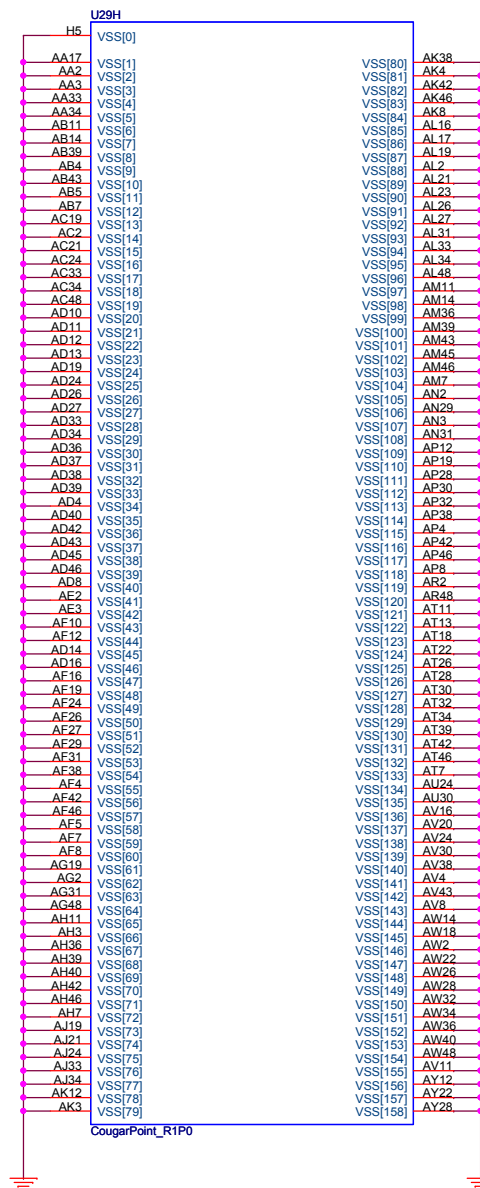
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Cougar Point-M (POWER)

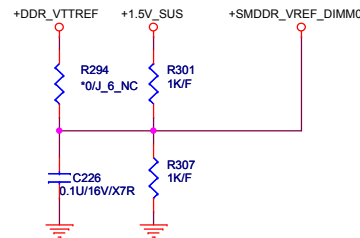
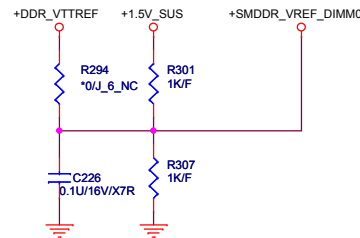


IBEX PEAK-M (GND)

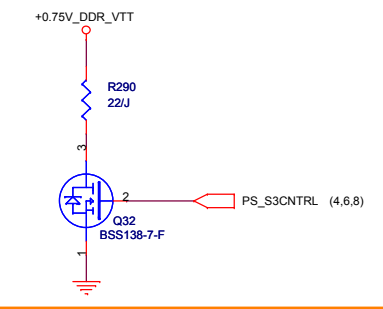


Quanta Computer Inc.

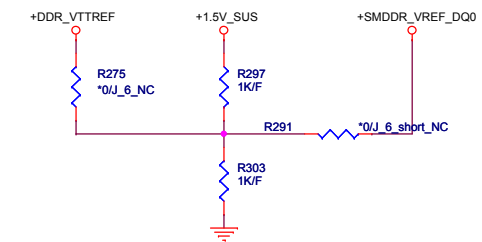
PROJECT : GM6C MLK DIS

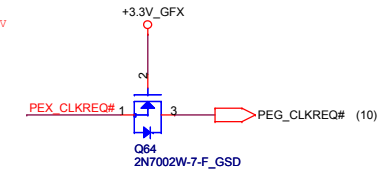


S3 Power reduce



+DDR_VTTREF +1.5V_SUS +SMDDR_VREF_DQ0



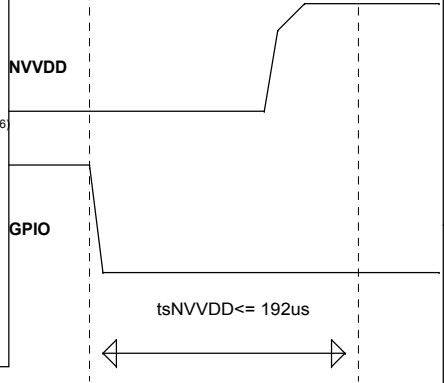


I/O 3.3V

PEX_RST

$T_{rise} \geq 1\mu s$

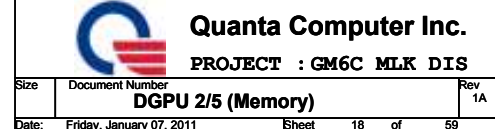
$T_{fall} \leq 500ns$

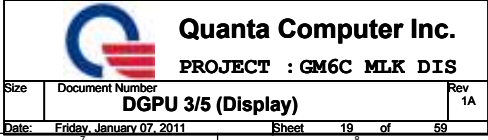


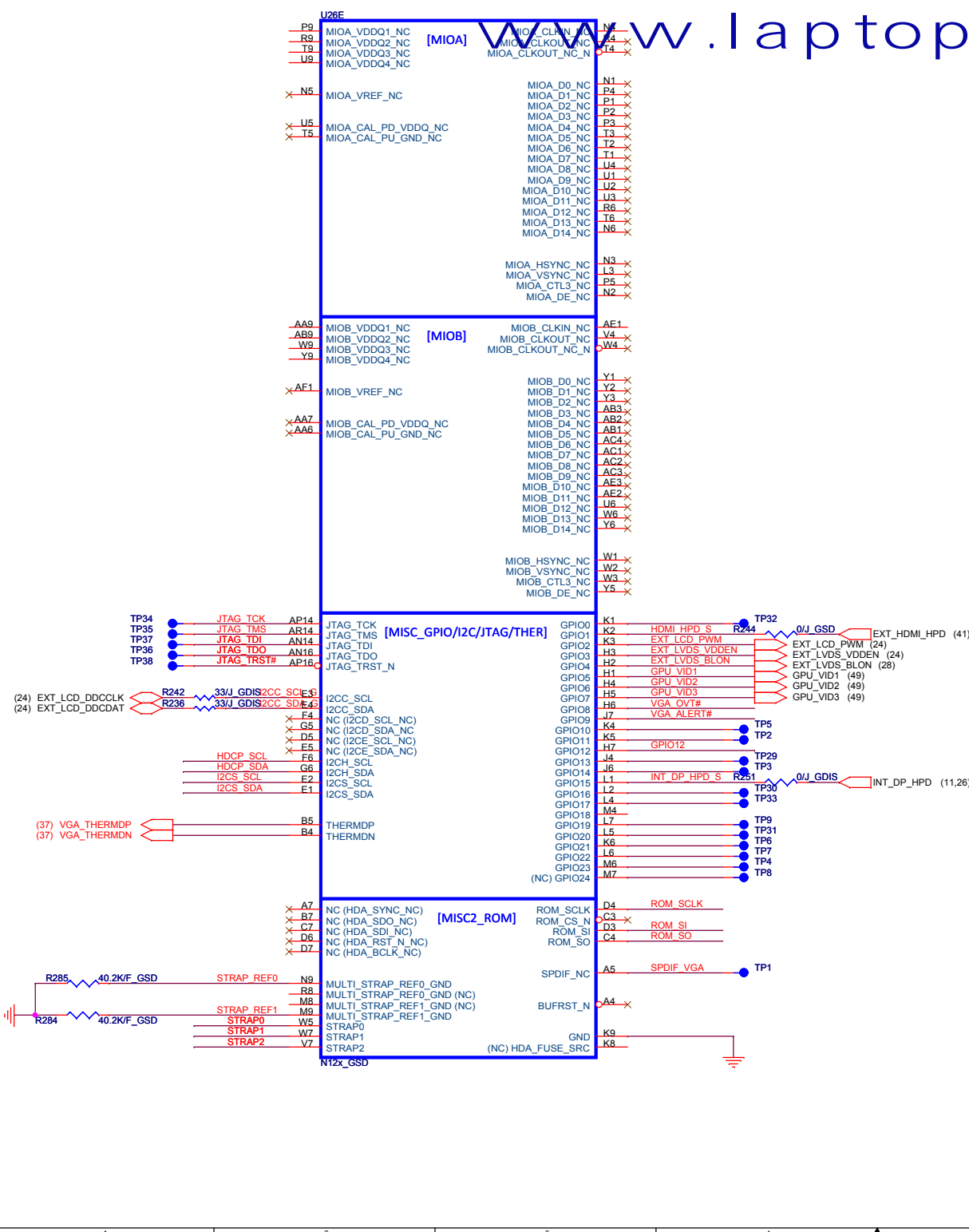
FB_CAL_PD_VDDQ/FB_CAL_PU_GND
DG-05093-001_V02:Page 94

FB_CAL_TERM_GND
DG-05093-001_V02:Page 94

40.2/F or 60.4/F dependent on GPU SKU





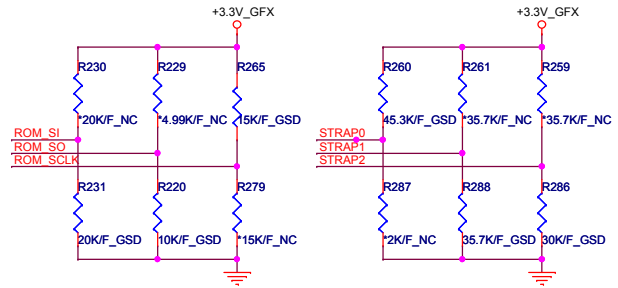


		Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table				
RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

ROM_SI Strap Bit for RAM Mapping

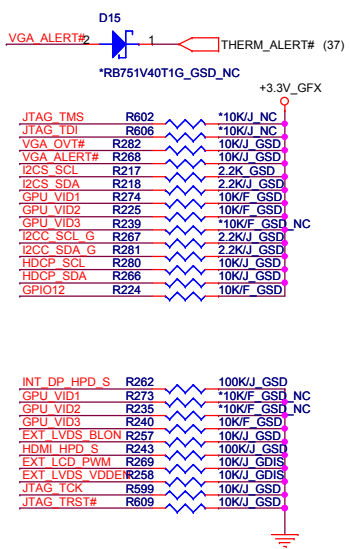
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



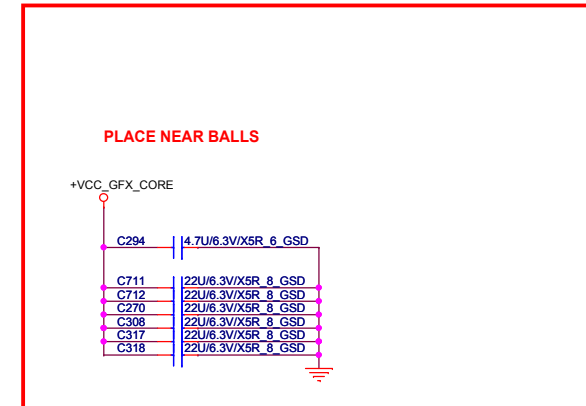
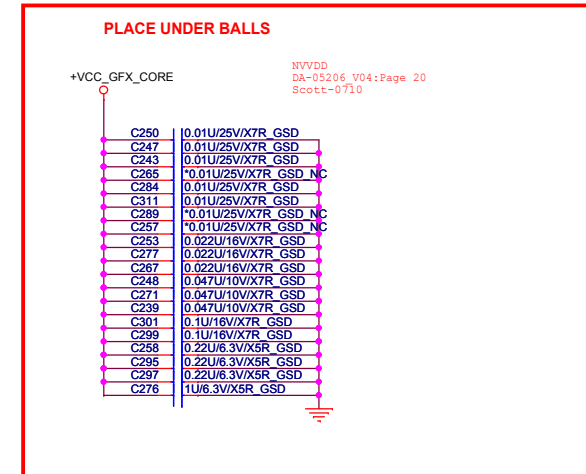
STRAP2 ROM_SCLK				
N12P-GE (AJON12P0T02)	PD 30K	PU 15K	0xDF5	
N12P-GT (AJON12P0T03)	PD 35K	PU 15K	0xDF6	
N12P-GS (AJON12P0T04)	PD 25K	PU 15K	0xDF4	

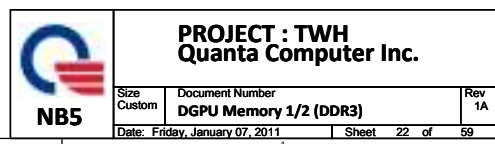
GPIO ASSIGNMENTS

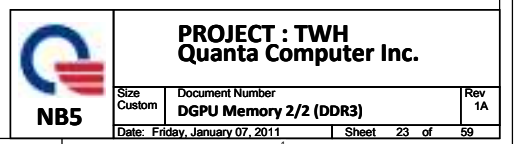
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD0 VID0
6	OUT	N/A	NVVD1 VID1
7	OUT	N/A	NVVD2 VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

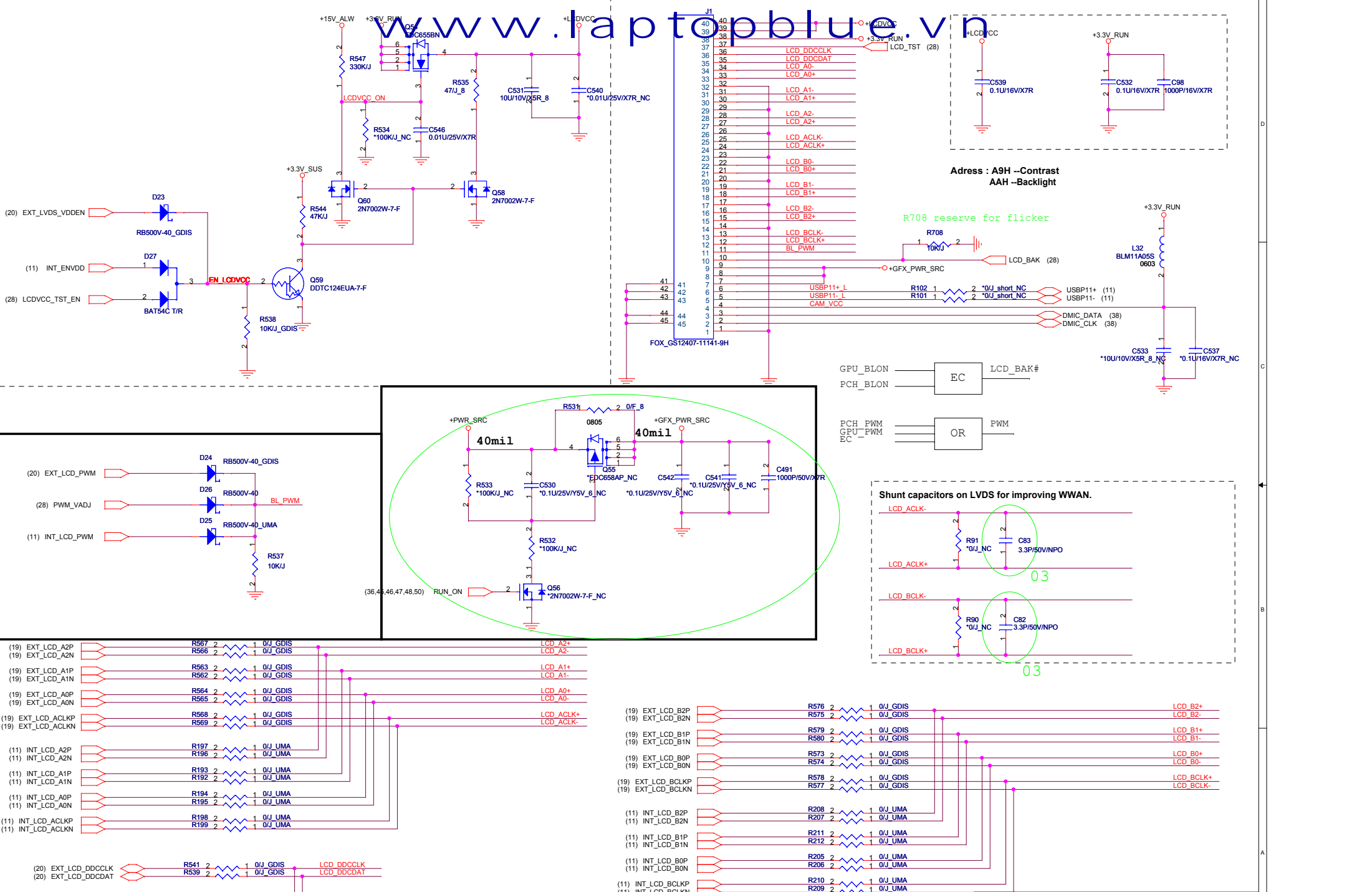


31.56A



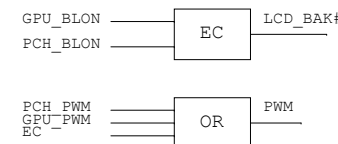




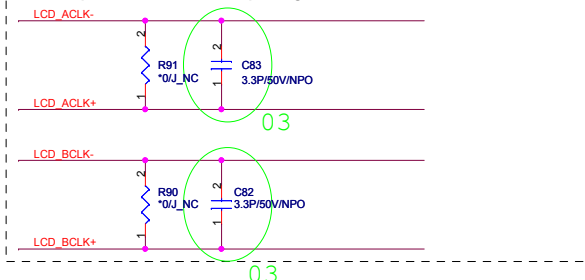


Address : A9H --Contrast
AAH --Backlight

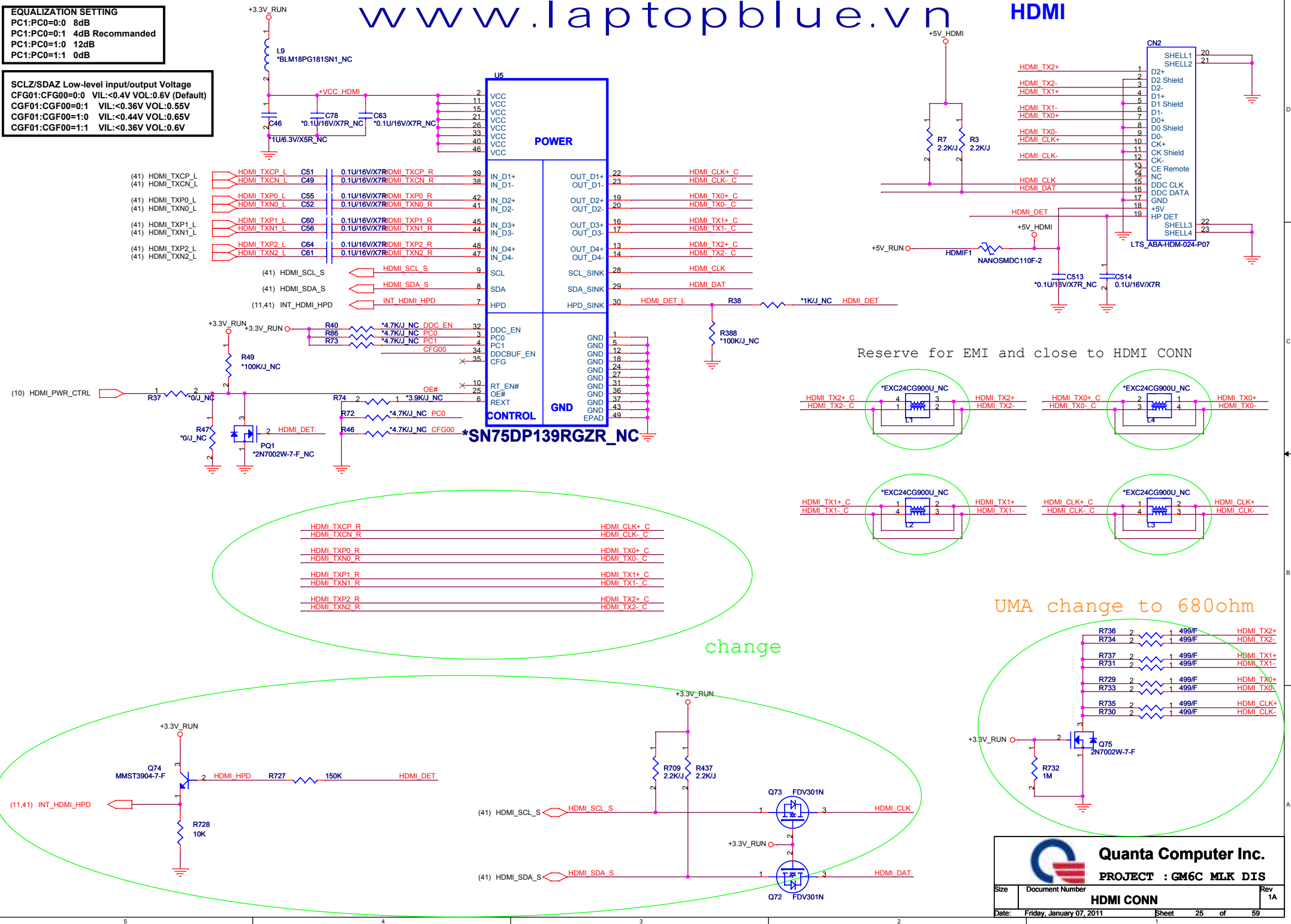
R708 reserve for flicker



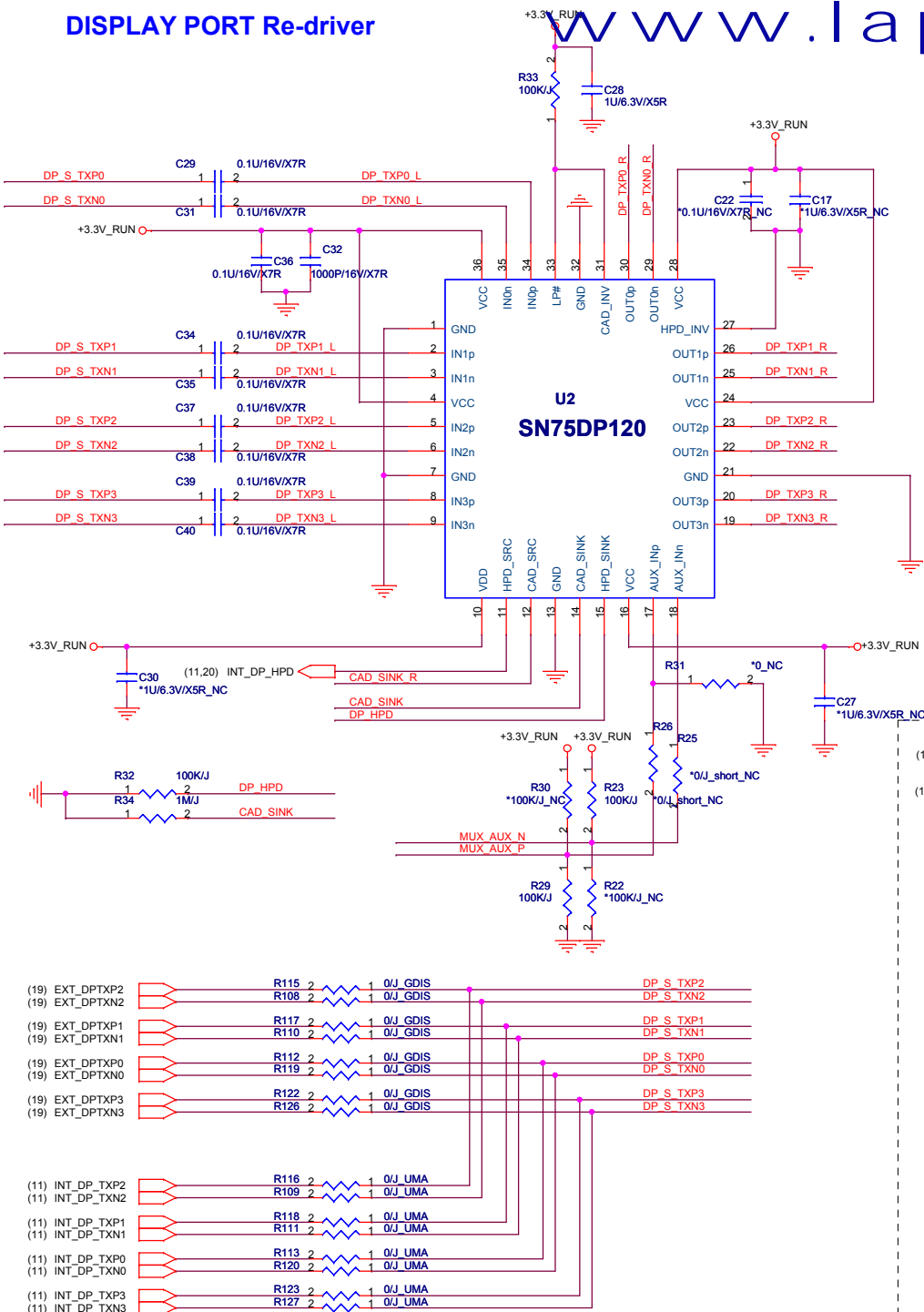
Shunt capacitors on LVDS for improving WWAN.



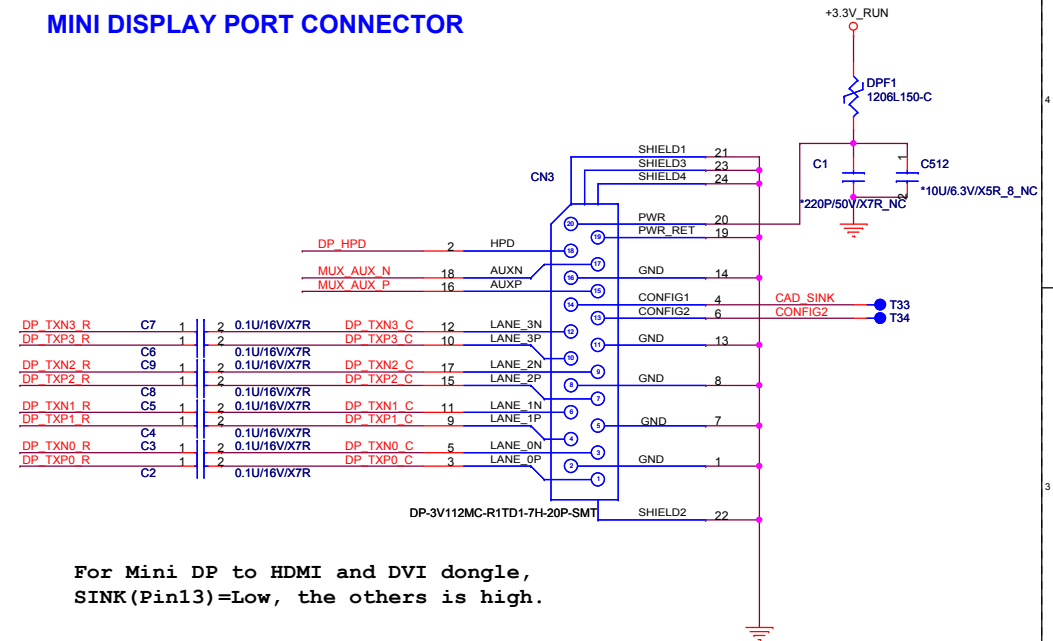
SCLZ/SDA2 Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V



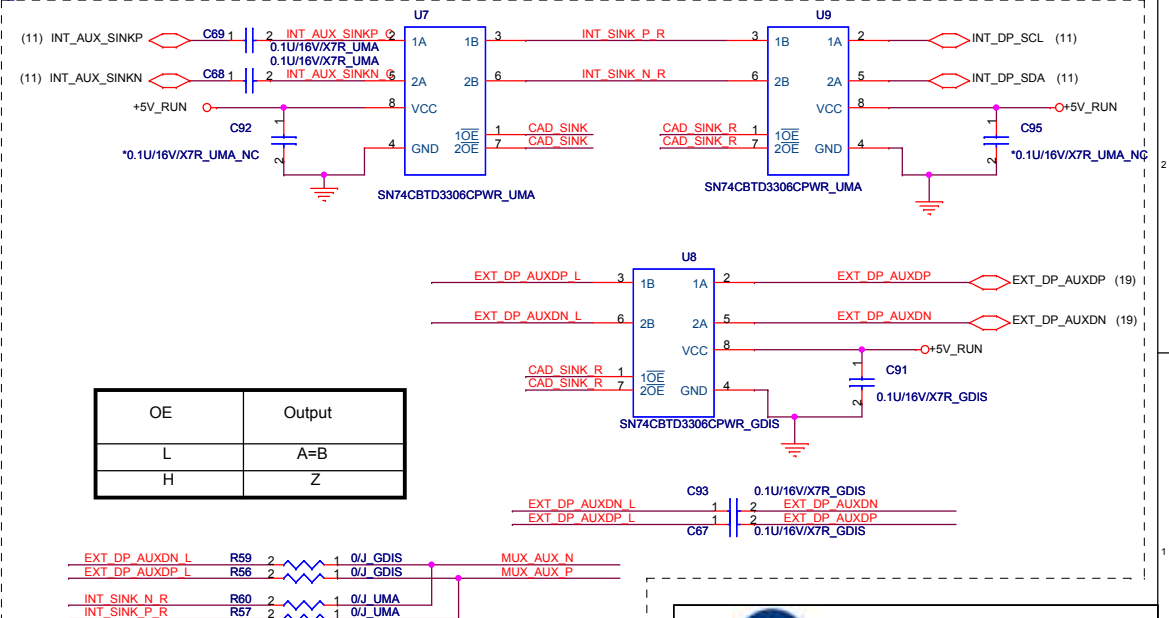
DISPLAY PORT Re-driver



MINI DISPLAY PORT CONNECTOR

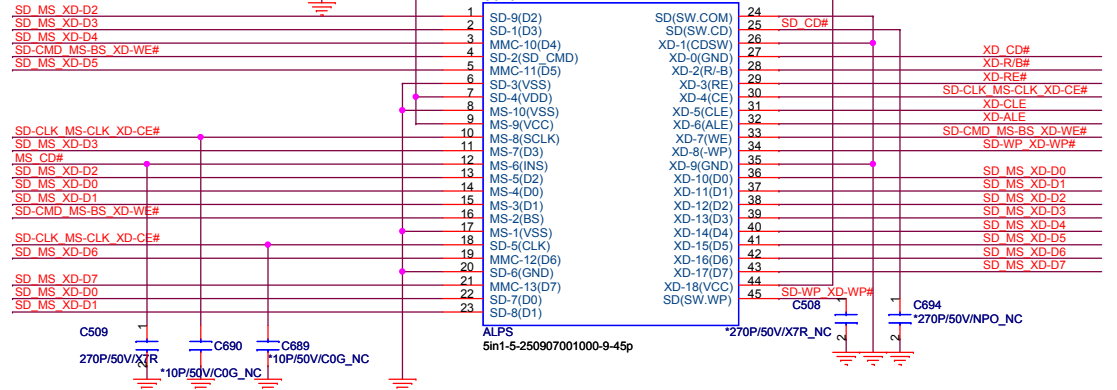


For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.



OE	Output
L	A=B
H	Z

2.2uF cap is no more than 250mils away from the power pin and have a min trace width of 40mils.



MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3.Application

Layout Note:
Place this cap close to pin 18

For AMD Platform only, Intel doesn't need
to connect to PCH(Vendor)

Card Reader interface signal mapping

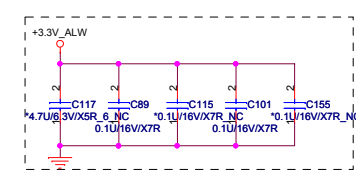
Pin	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xd	SD D0	MS D0	XD D0
MDIO01		SD D1	MS D1	XD D1
MDIO02		SD D2	MS D2	XD D2
MDIO03		SD D3	MS D3	XD D3
MDIO04		SD CMD	MS BS	XD WE#
MDIO05		SD CLK	MS CLK	XD CE#
MDIO06		SD WP		XD WP#
MDIO07				XD CLE
MDIO08		MMC D4	MS D4	XD D4
MDIO09		MMC D5	MS D5	XD D5
MDIO10		MMC D6	MS D6	XD D6
MDIO11		MMC D7	MS D7	XD D7
MDIO12				XD RE#
MDIO13				XD R/B#
MDIO14				XD ALE
CR1 LEDN		SD LED#	MS LED#	XD LED#
CR1 PCTLN		SD PWR#	MS PWR#	XD PWR#
CR1 CD0		SD CD#	MS CD#	XD CD#
CR1 CD1				
CR1 CD2				



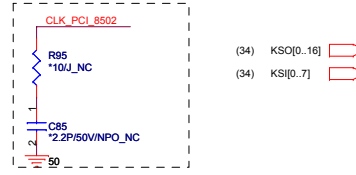
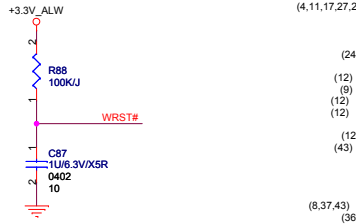
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

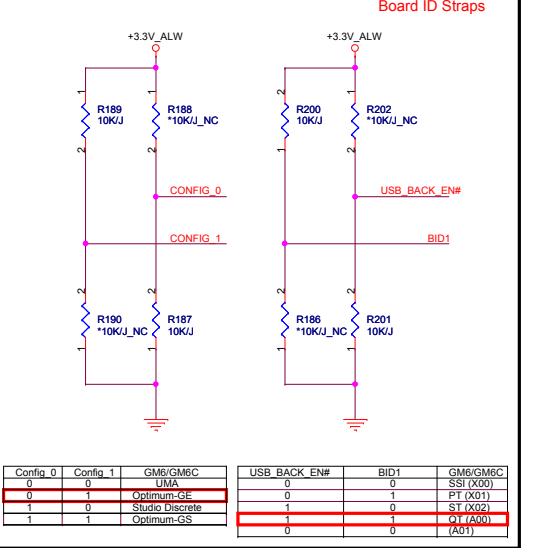
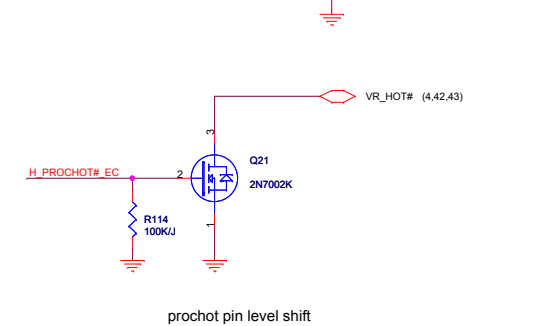
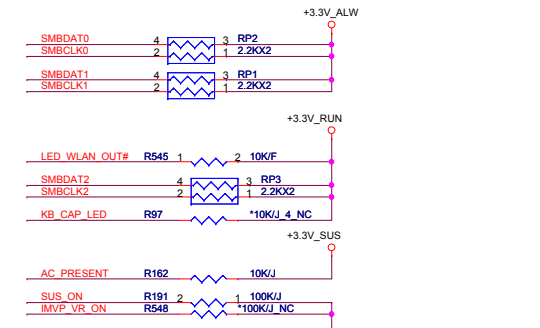
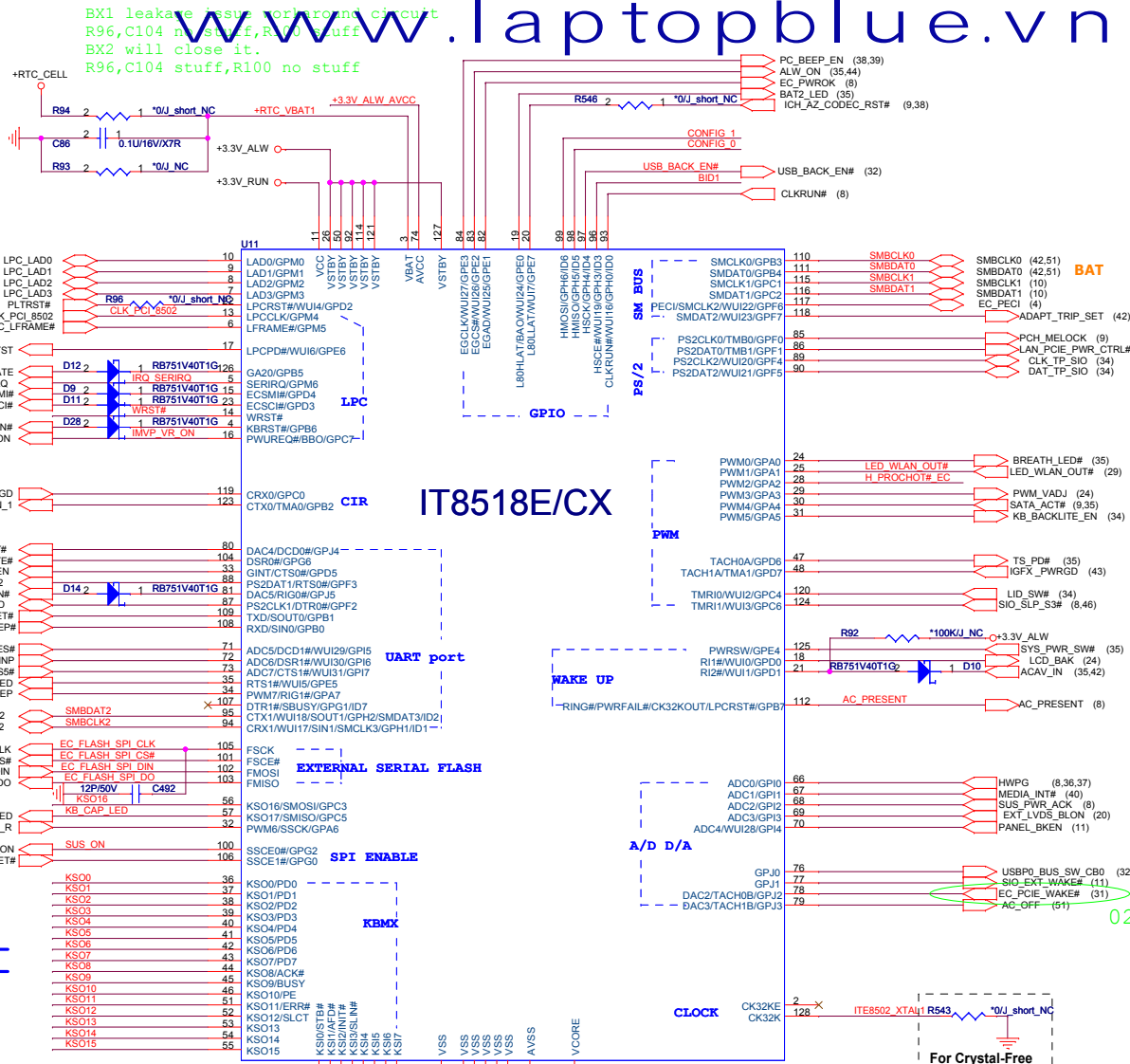
Card Reader (JMB389)



Layout Note: Place these caps close to ITE8502



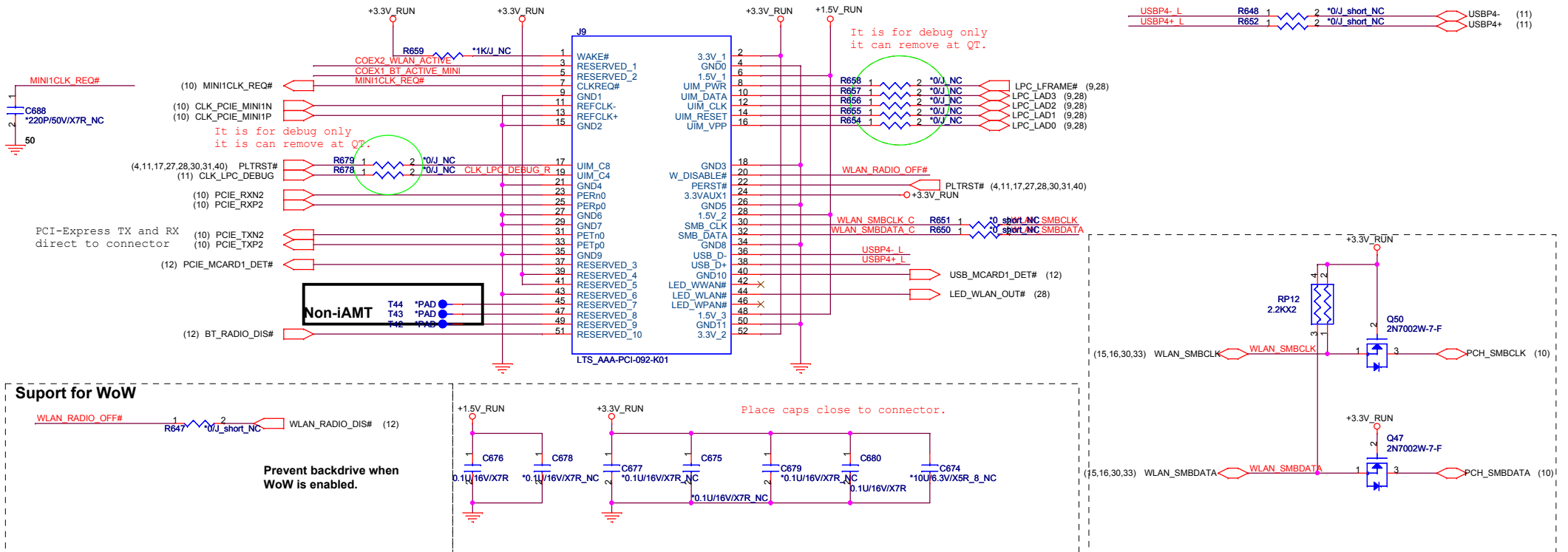
Layout Note: Place PC169 close to ITE8502



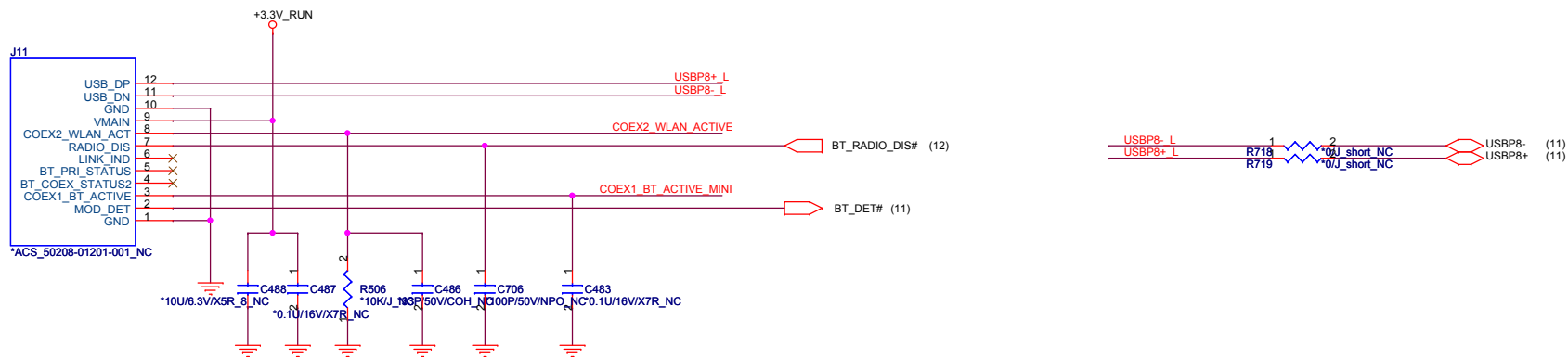
Config_0	Config_1	GM6/GM6C	UMA	USB_BACK_EN#	BID1	GM6/GM6C
0	0	Optimum-GS	0	0	0	SS1 (X00)
0	1	Optimum-GS	0	0	1	PT (X01)
1	0	Optimum-GS	0	0	0	ST (X02)
1	1	Optimum-GS	0	0	1	Q1 (A00)
1	1	Optimum-GS	0	0	0	A01

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MiniCard WLAN connector



Support Dell BT375 (Little Stone) module (XPS) W TO B

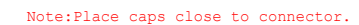
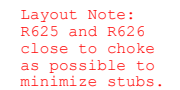


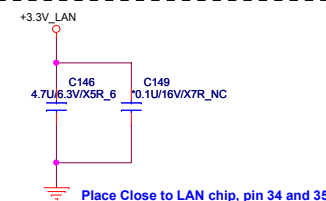
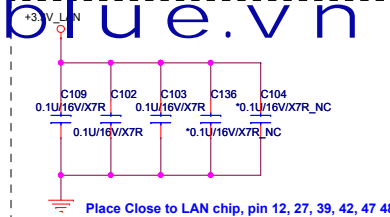
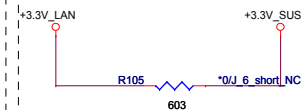
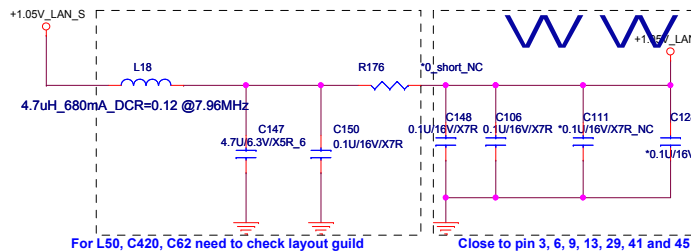
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

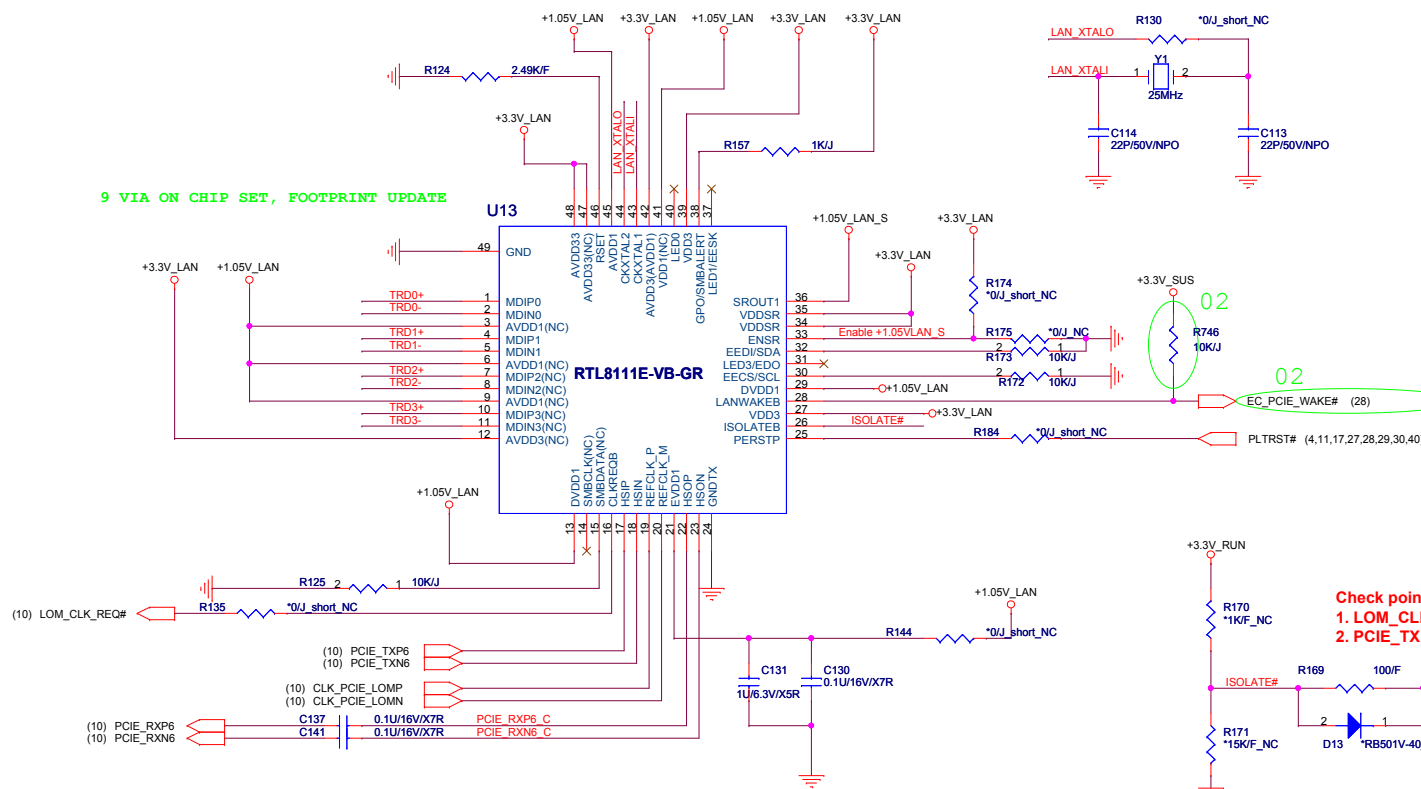
Size	Document Number	Rev
	MINI-Card (WLAN/WPAN)	1A
Date:	Friday, January 07, 2011	Sheet 29 of 59

Quanta Computer Inc.

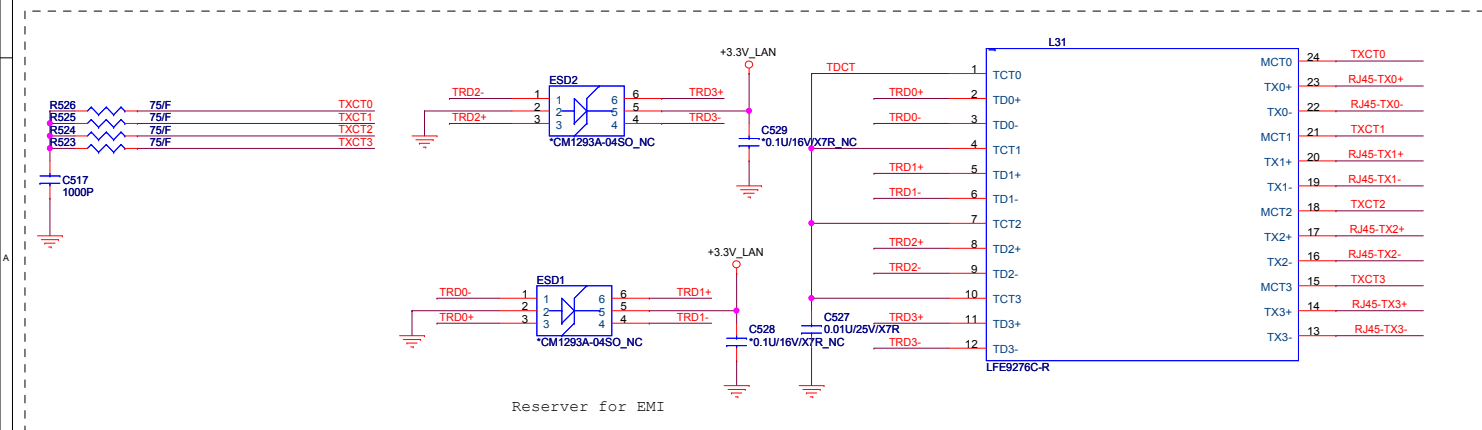
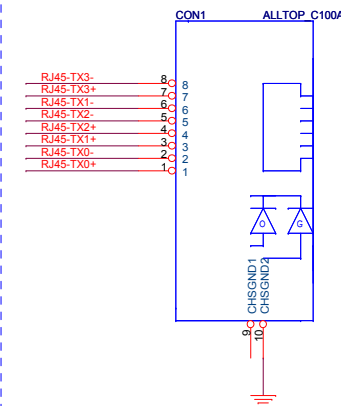




9 VIA ON CHIP SET, FOOTPRINT UPDATE

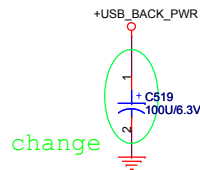


RJ-45 Connector



Continuous 1.5A
Pulse 2.3A(max)

OUT3 8
OUT2 7
OUT1 6



change

USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R
USBP1+ R
USBP1- R

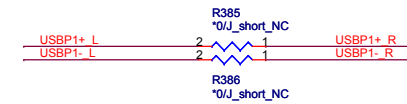
ESATA RXP4 R
ESATA RXN4 R
ESATA TXP4 R
ESATA TXN4 R
ESATA RXP4 C
ESATA RXN4 C
ESATA TXP4 C
ESATA TXN4 C
ESATA RXP4 R
ESATA RXN4 R
ESATA TXP4 R
ESATA TXN4 R
ESATA RXP4 C
ESATA RXN4 C
ESATA TXP4 C
ESATA TXN4 C

C524
C521
C523
C525

FOX_3Q38131-R33C1B-8H

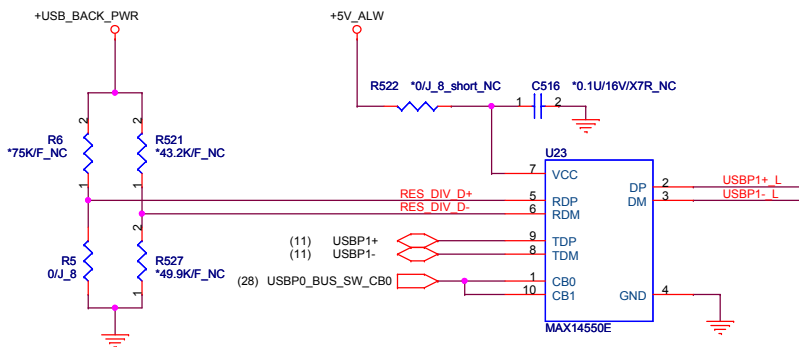
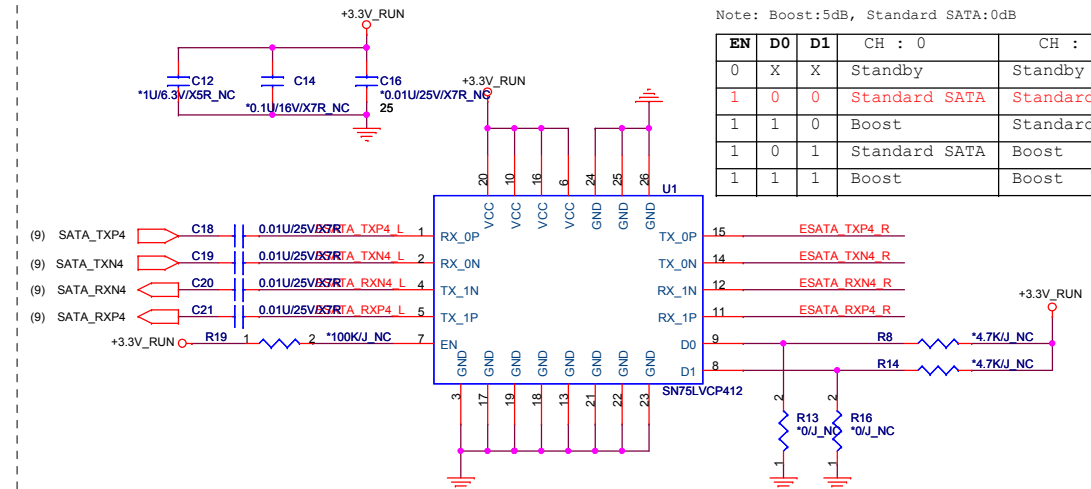
CN4

USB_CHG_DET# (35)



Layout Note: Please put those on the same side of MB PCB

EN	DO	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

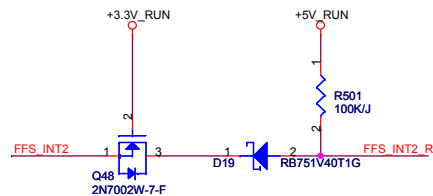
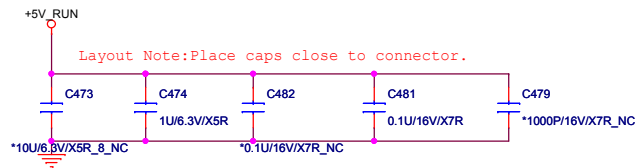
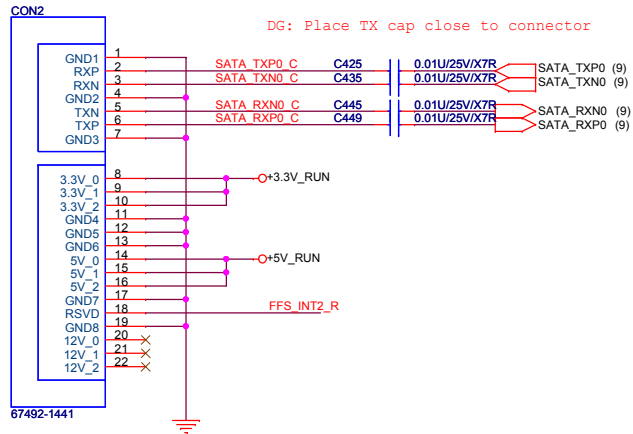


R15 needs to be 49.9K_F if we use external resistors.

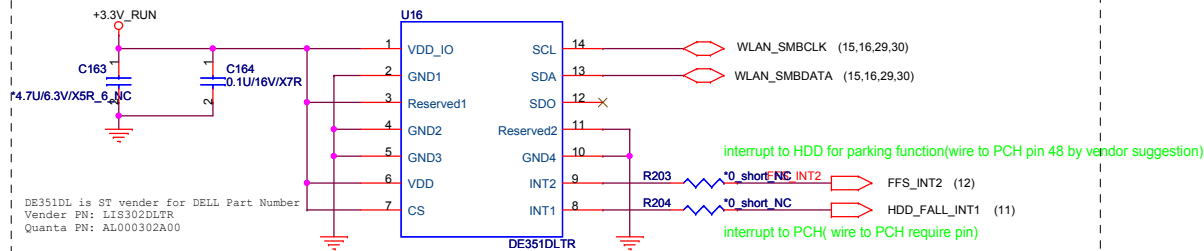
CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
 (5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

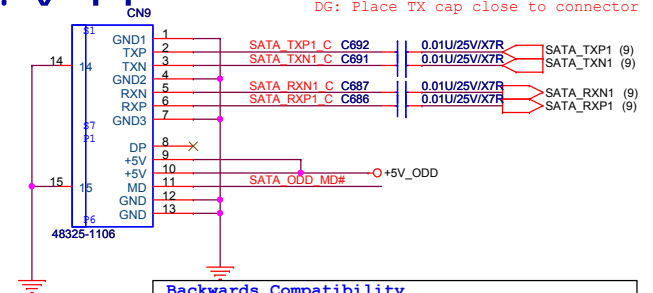
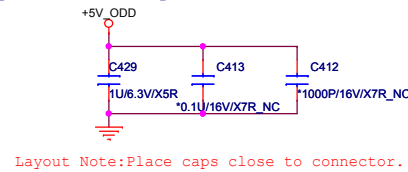
SATA Connector.



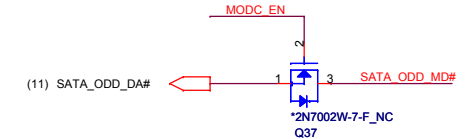
3-axis Fall Sensor (HDD data protector)



DDD Connector



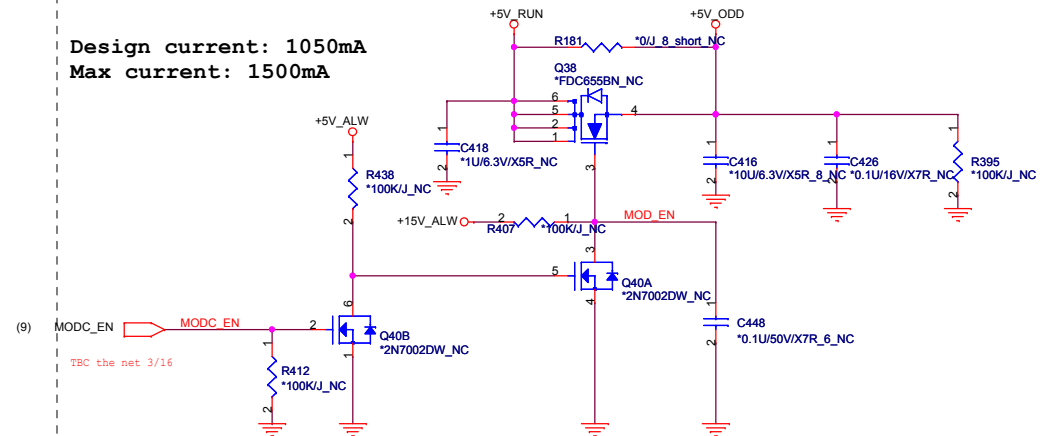
Backwards Compatibility



Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA
Max current: 1500mA

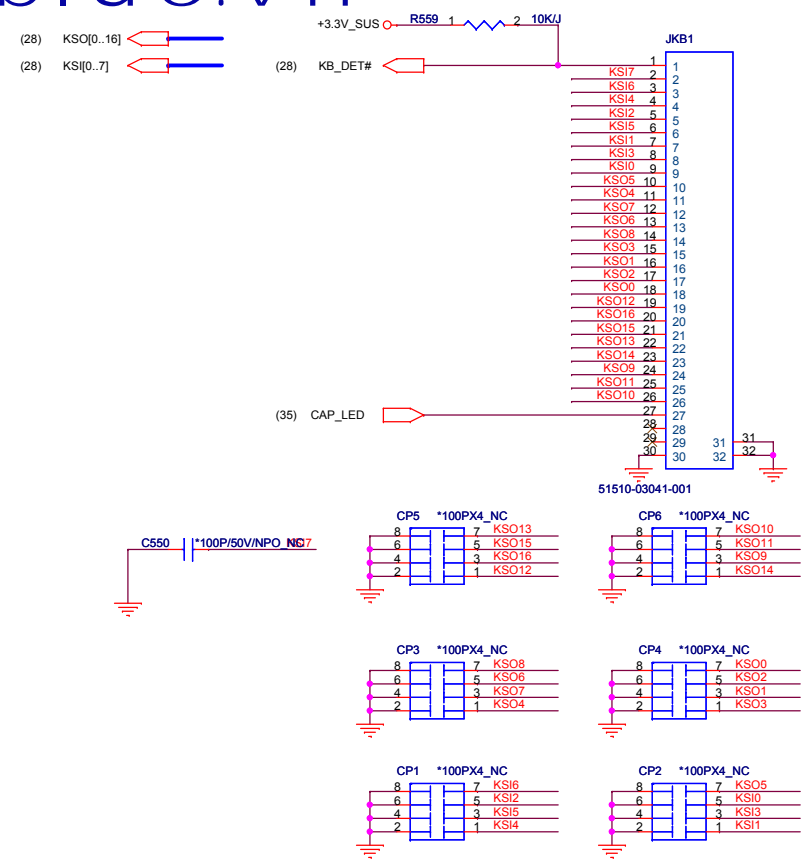


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PROJECT : GM6C MLK DIS

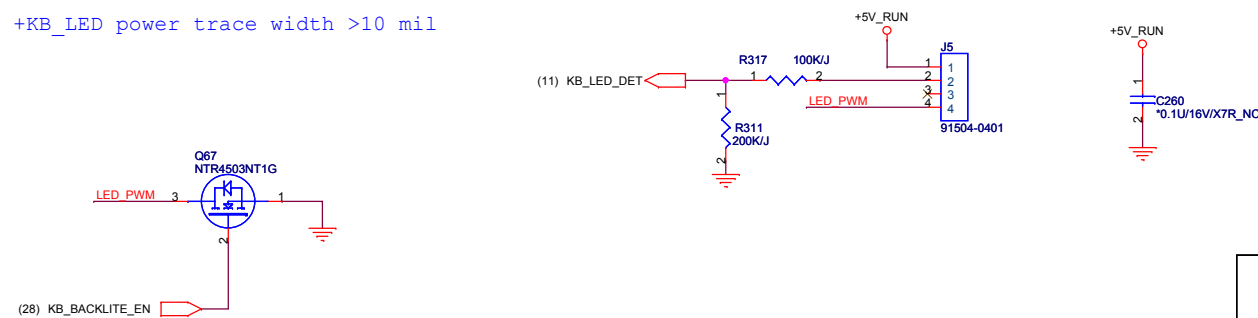
SATA (HDD&ODD)

KEYBOARD CONNECTOR



Layout Note: 100P CAPS CLOSE TO JKB3

```
+KB_LED power trace width >10 mil
```

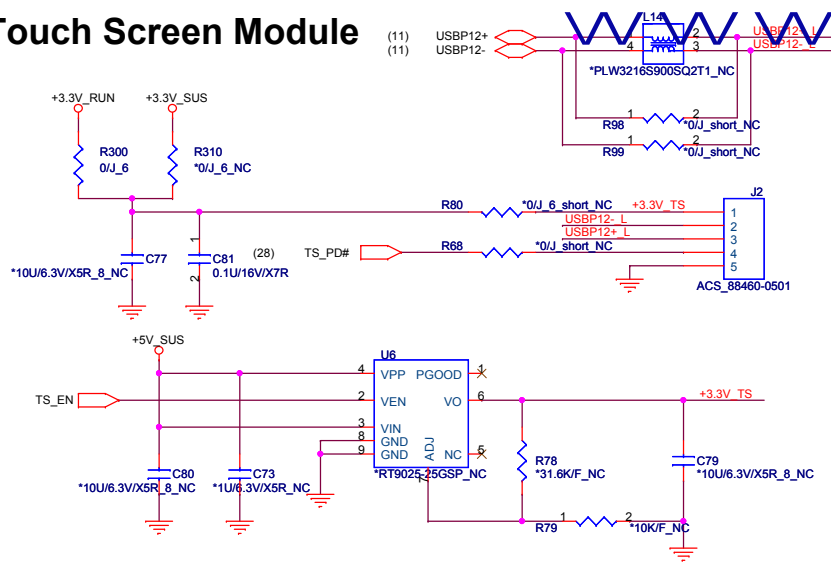


PROJECT : GM6C MLK DIS

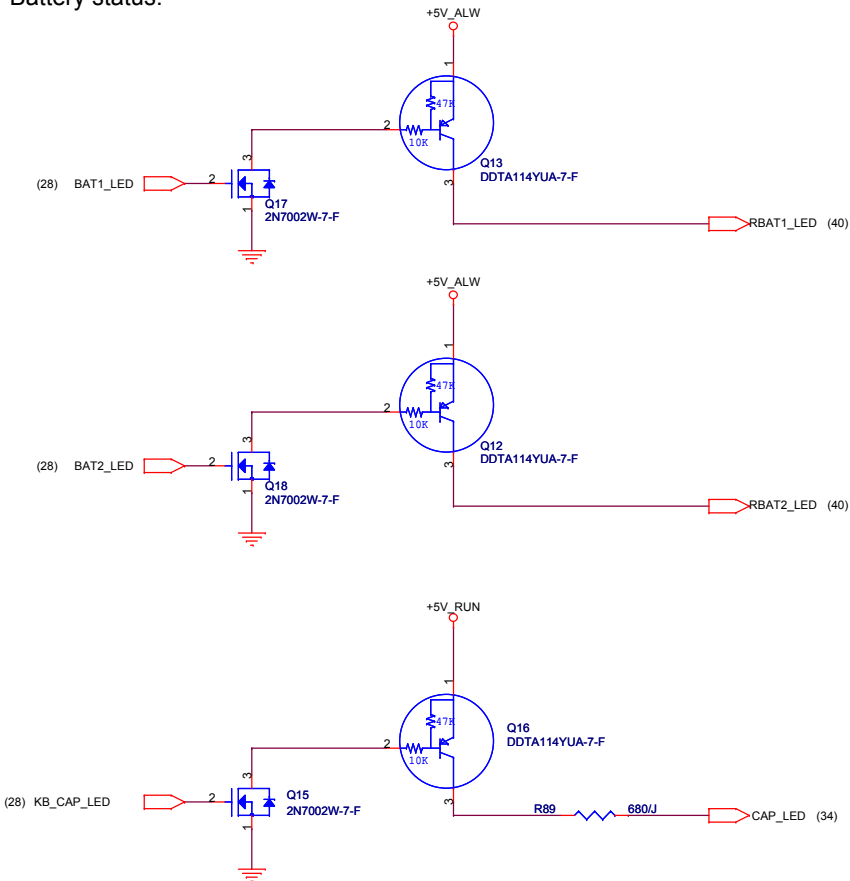
Rev
1A

Sheet 34 of 59

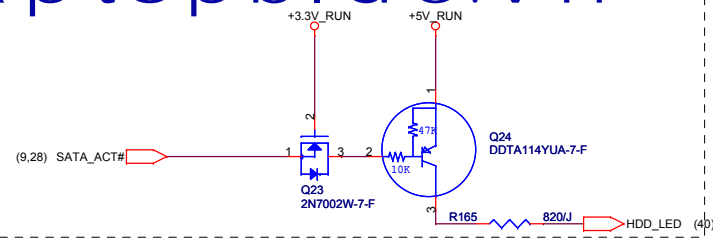
Touch Screen Module



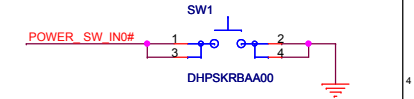
Battery status.



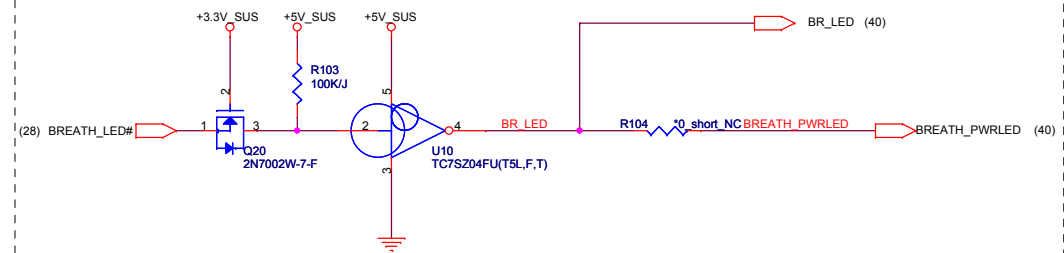
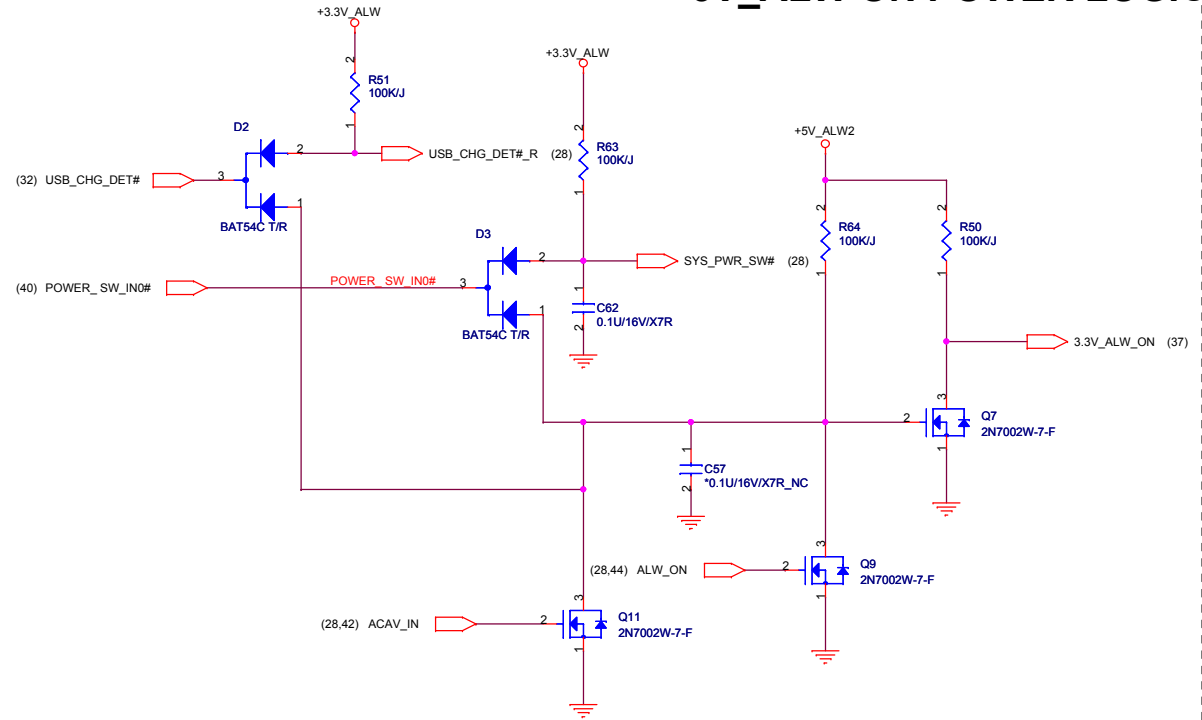
HDD activity LED.



Power button for Engineer



3V_ALW ON POWER LOGIC

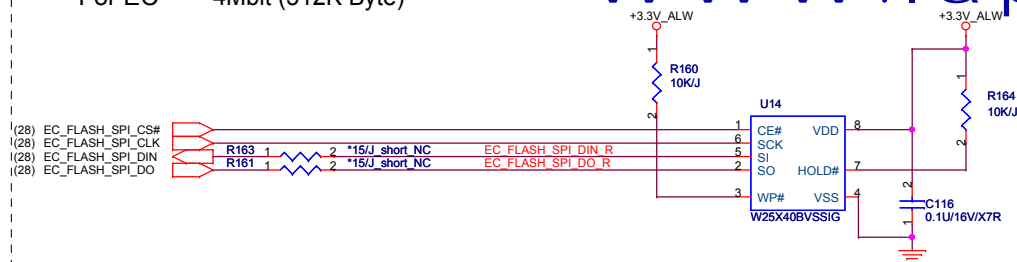


Quanta Computer Inc.

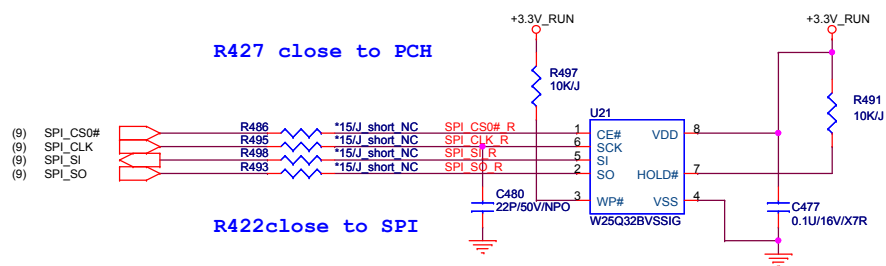
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SWITCH/LED/T-Screen	1A
Date:	Friday, January 07, 2011	Sheet 35 of 59

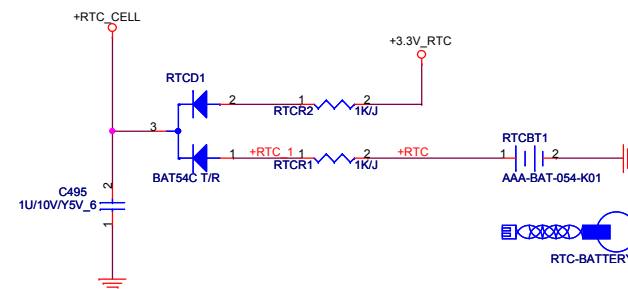
For EC 4Mbit (512K Byte)



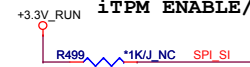
For PCH 32Mbit (4M Byte)



RTC BATTERY



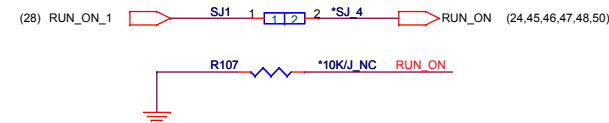
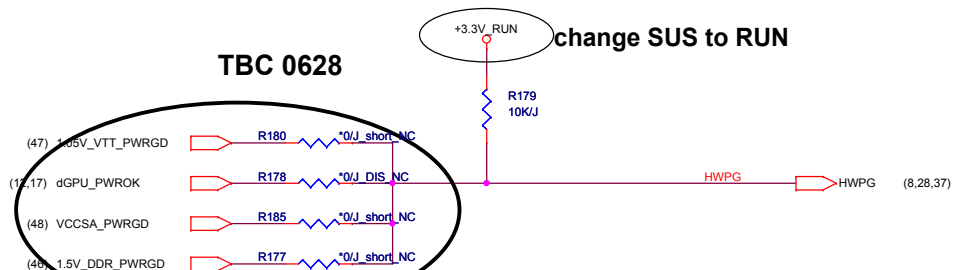
iTPM ENABLE/DISABLE



TPM Function	R428
Enable	Mount
Disable	NC (Default)

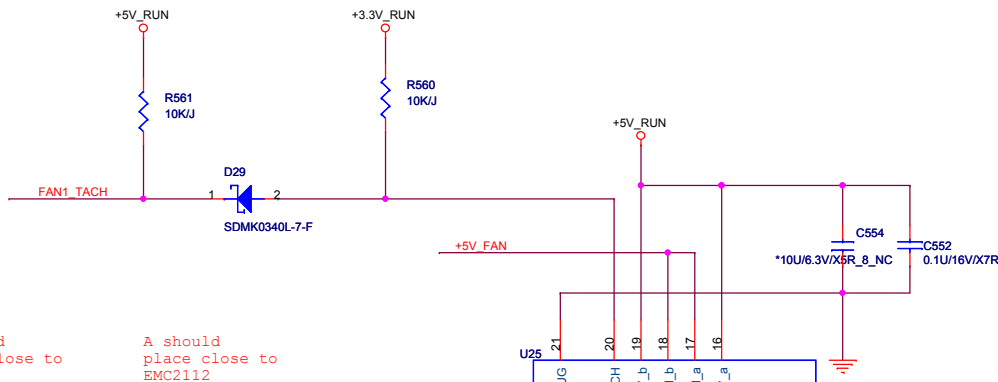
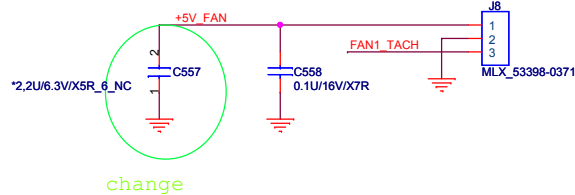
RESET CIRCUIT

TBC 0628



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PROJECT : GM6C MLK DIS



Need to check with BIOS

ADDR_SEL

HIGH: 0101 110xb

OPN: 0111 101xb

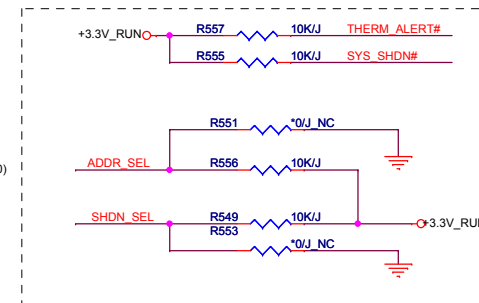
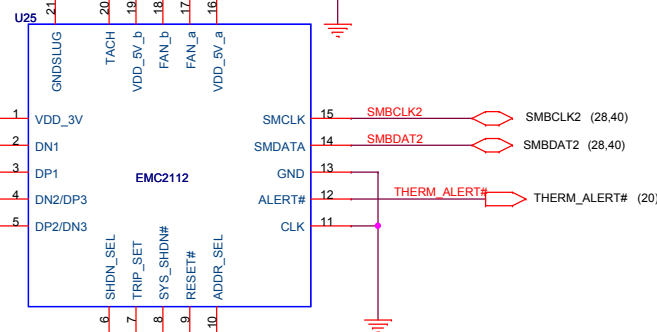
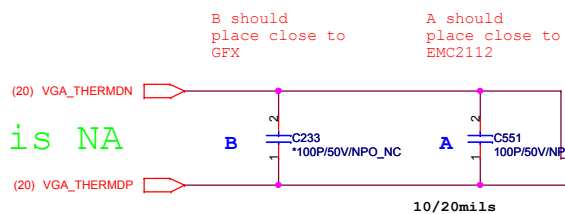
GND: 0101 111xb

SHDN_SEL

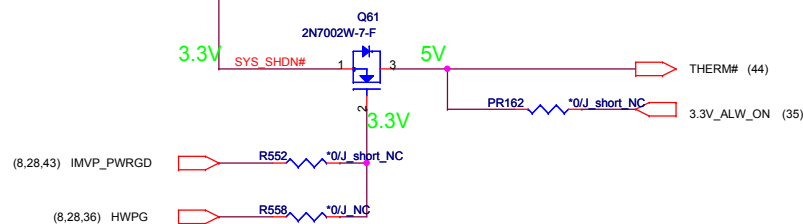
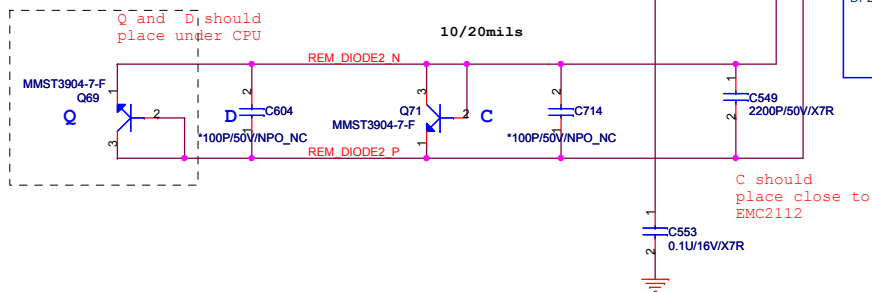
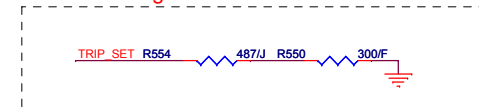
HIGH: External Diode 2 Mode

OPN: AMD CPU/Diode Mode

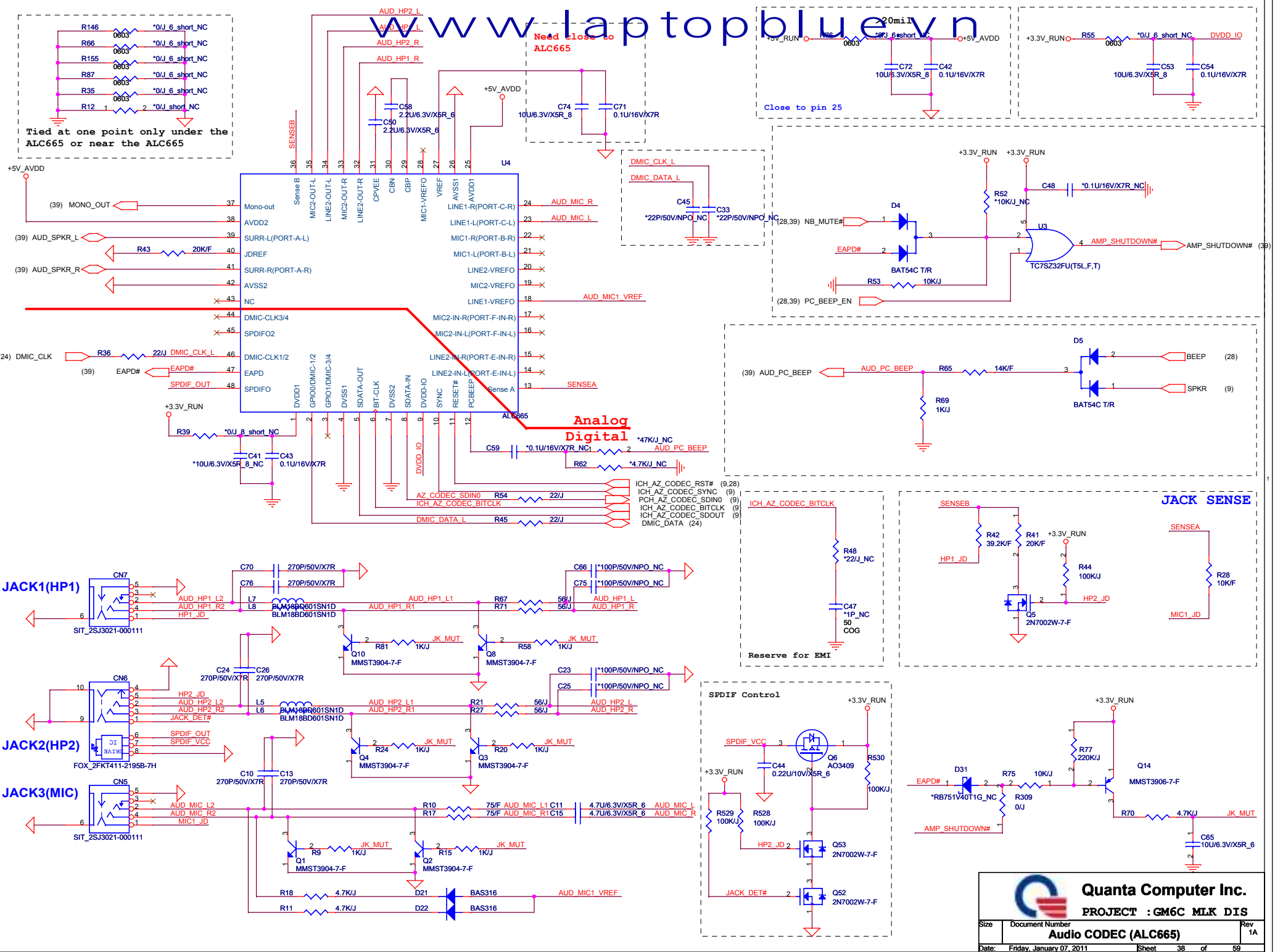
GND: Intel Transistor Mode



OTP 85 degree C

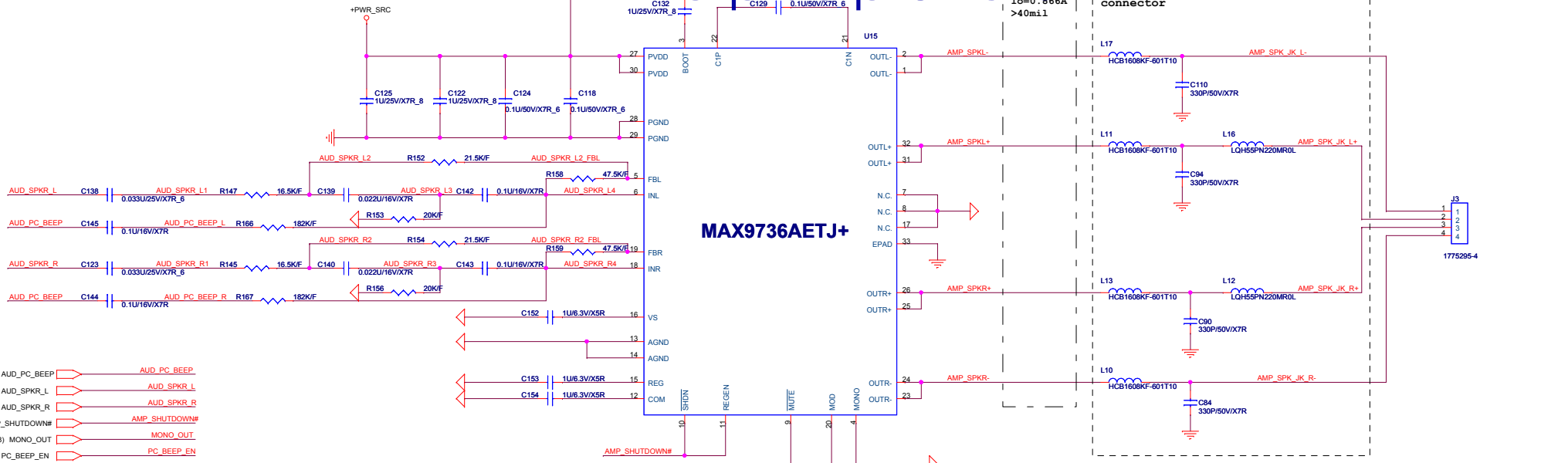


reserve HWPG only HW control (07/12)

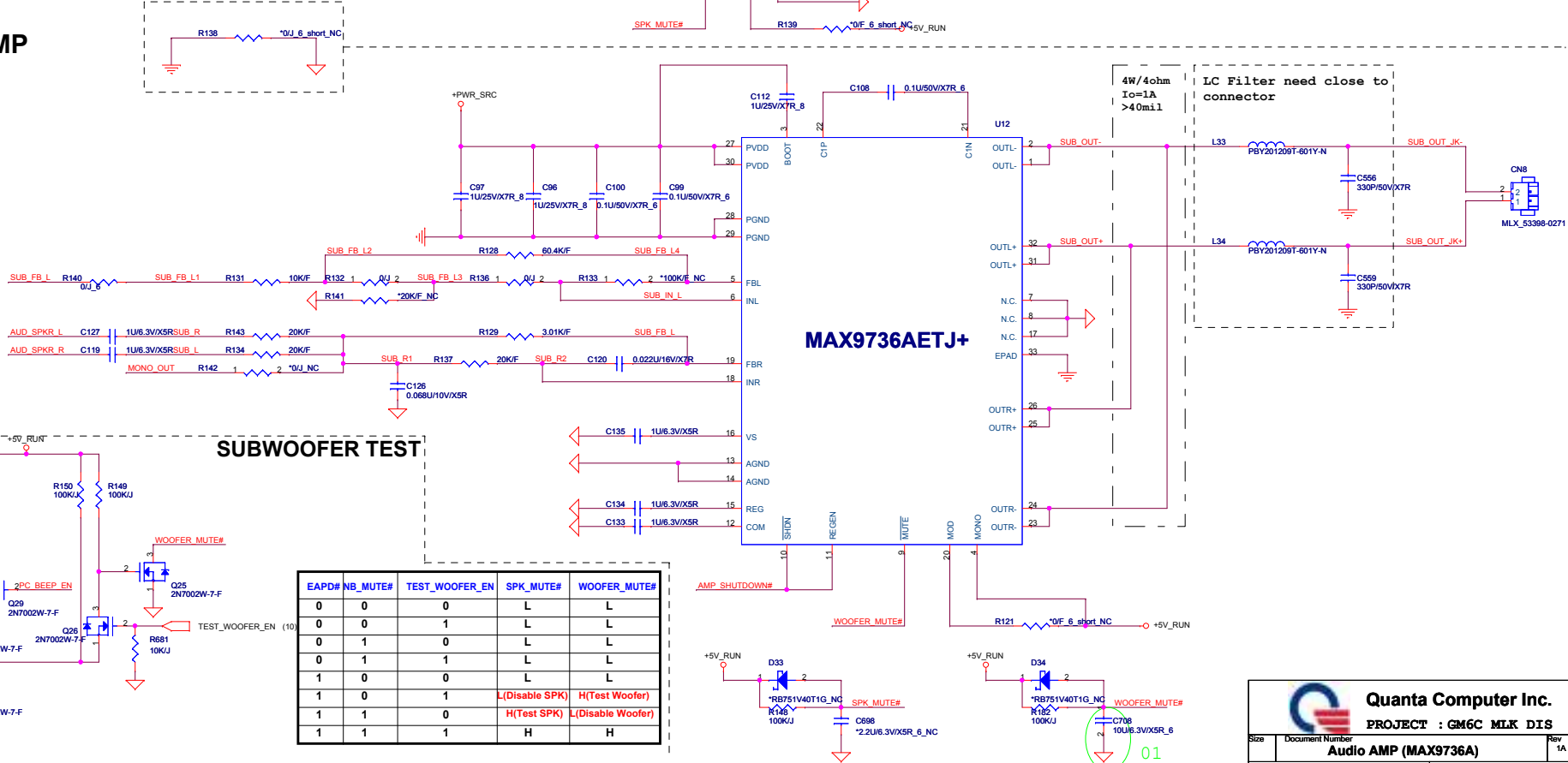


Main Speaker AMP

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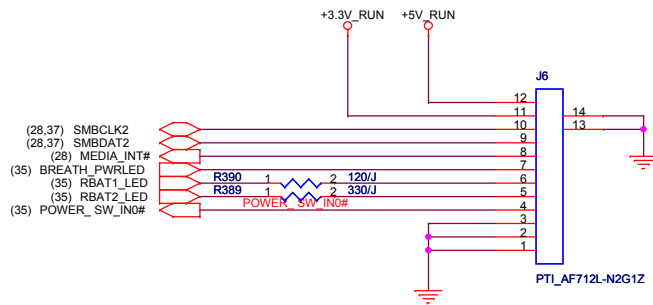
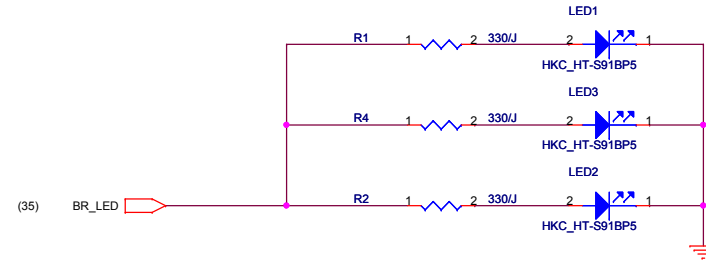
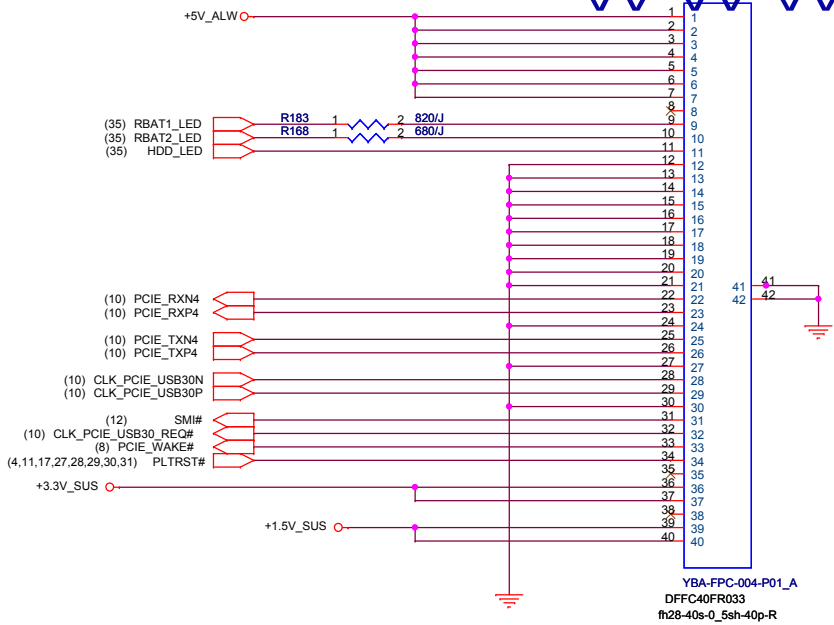


SUBWOOFER AMP



SUBWOOFER TEST

EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H



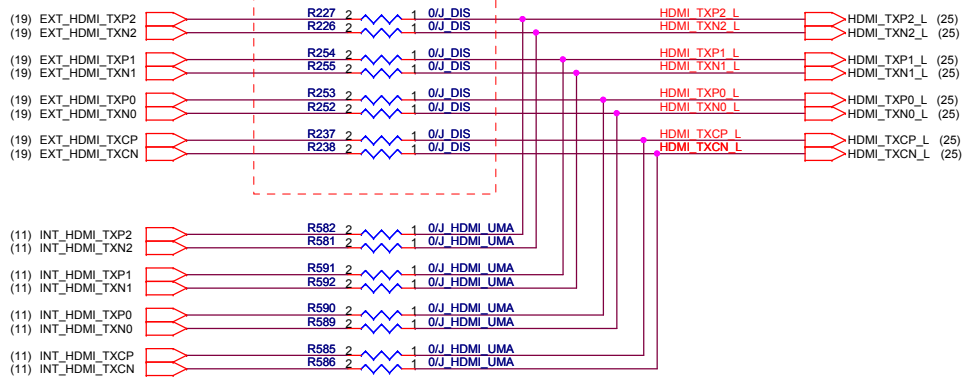
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

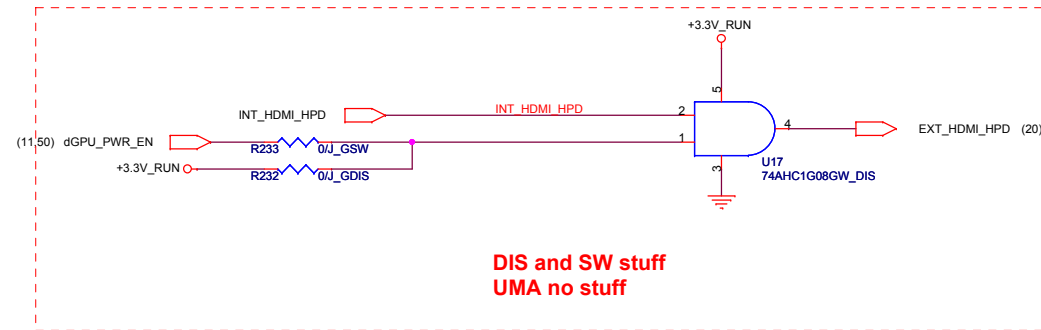
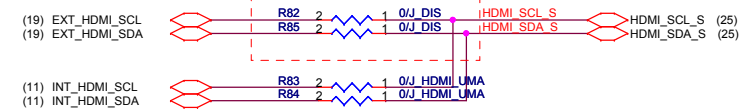
Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date:	Friday, January 07, 2011	Sheet 40 of 59

HDMI Switch

DIS and SW stuff
UMA no stuff



DIS and SW stuff
UMA no stuff

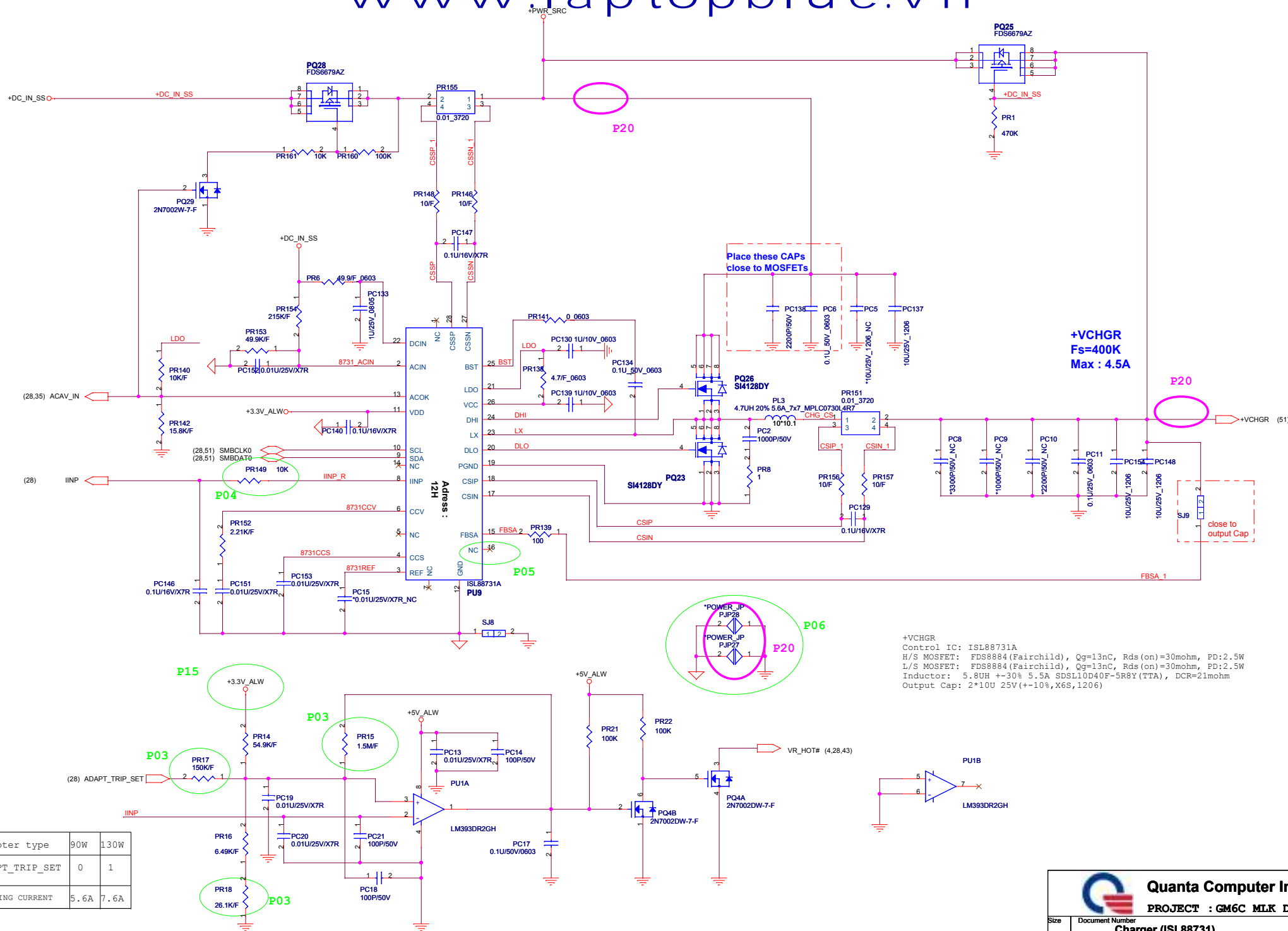


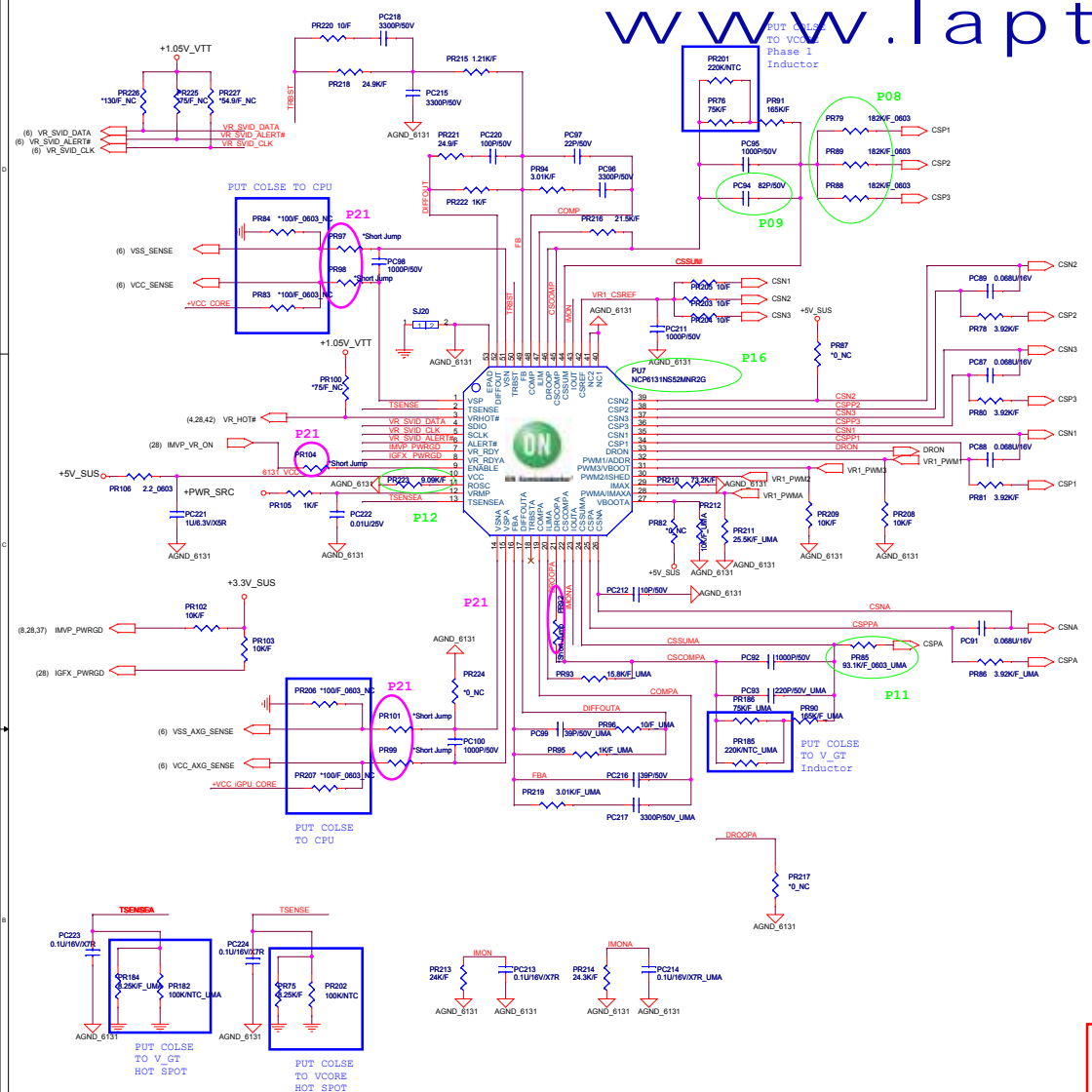
DIS and SW stuff
UMA no stuff



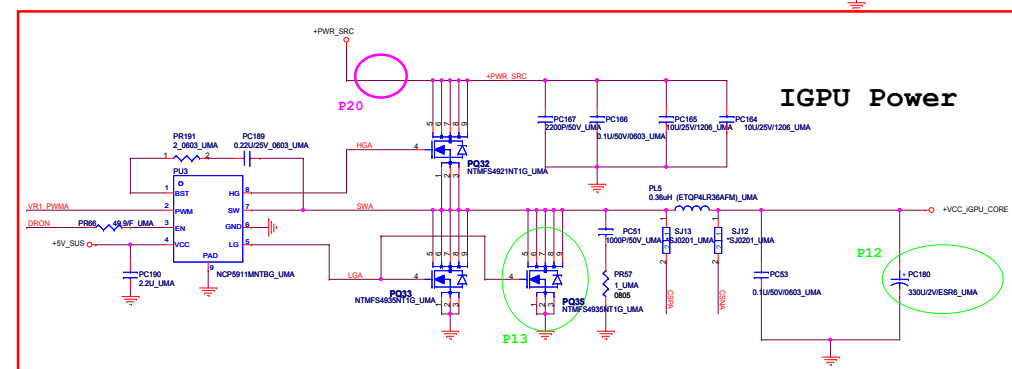
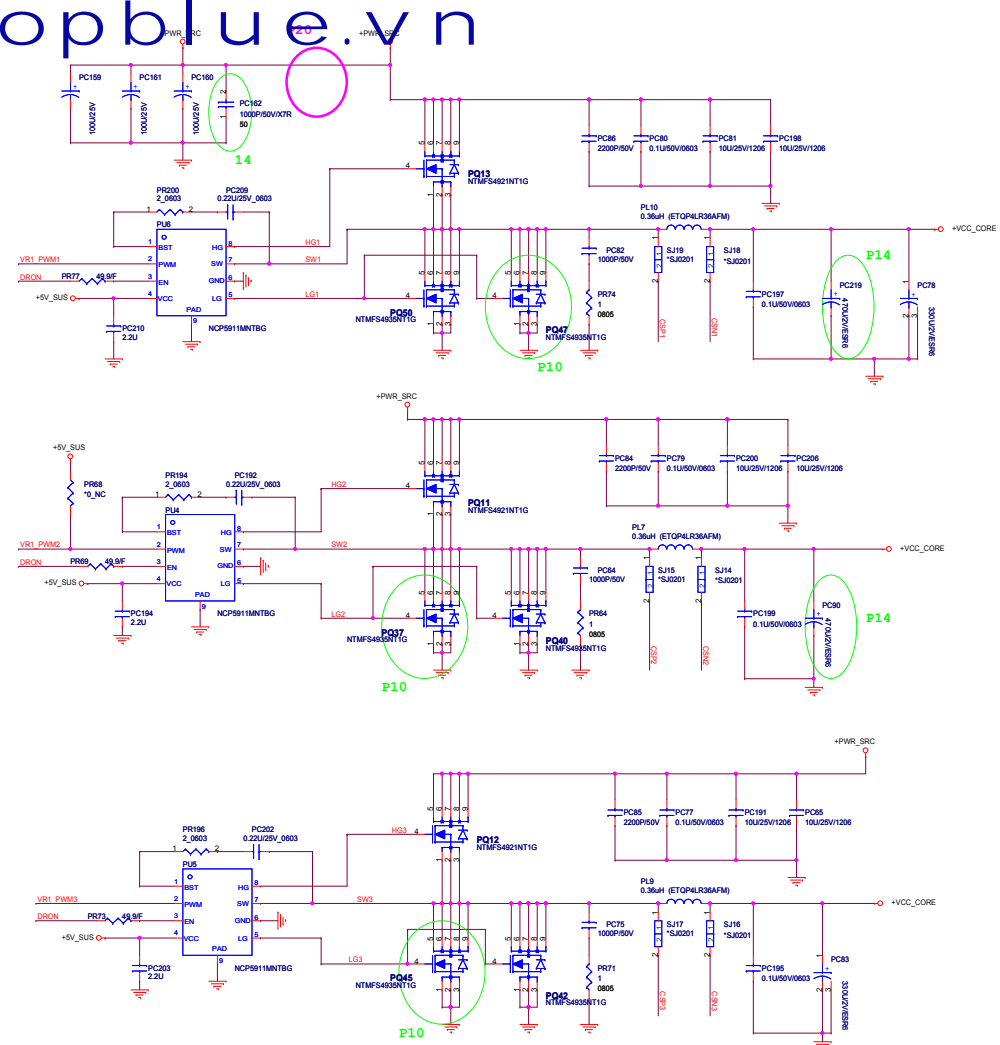
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

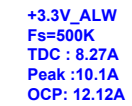


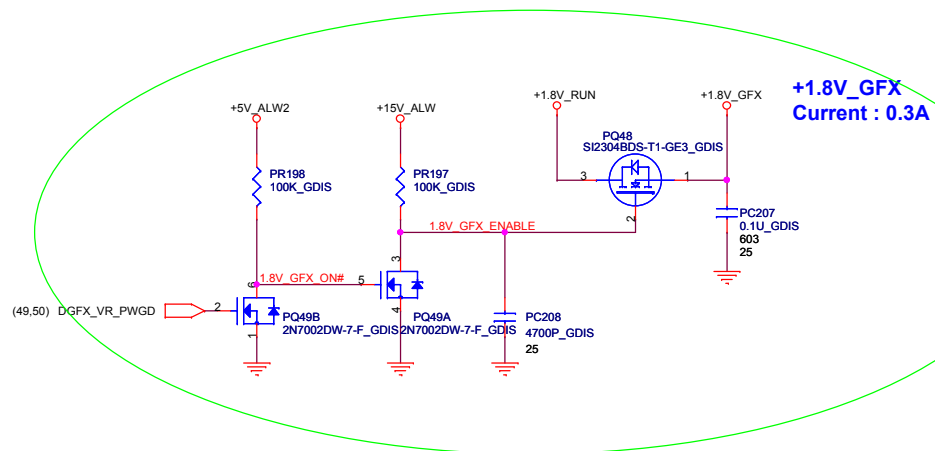
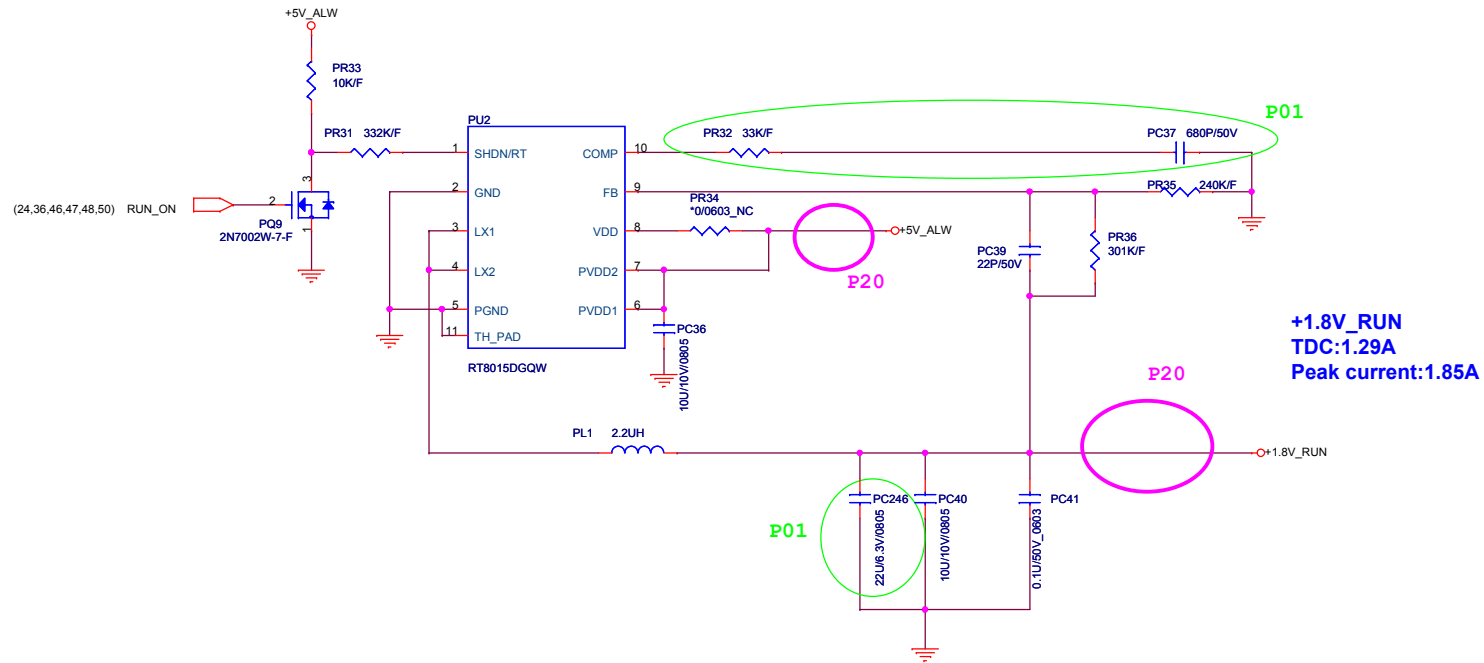


Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)



	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831

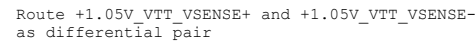


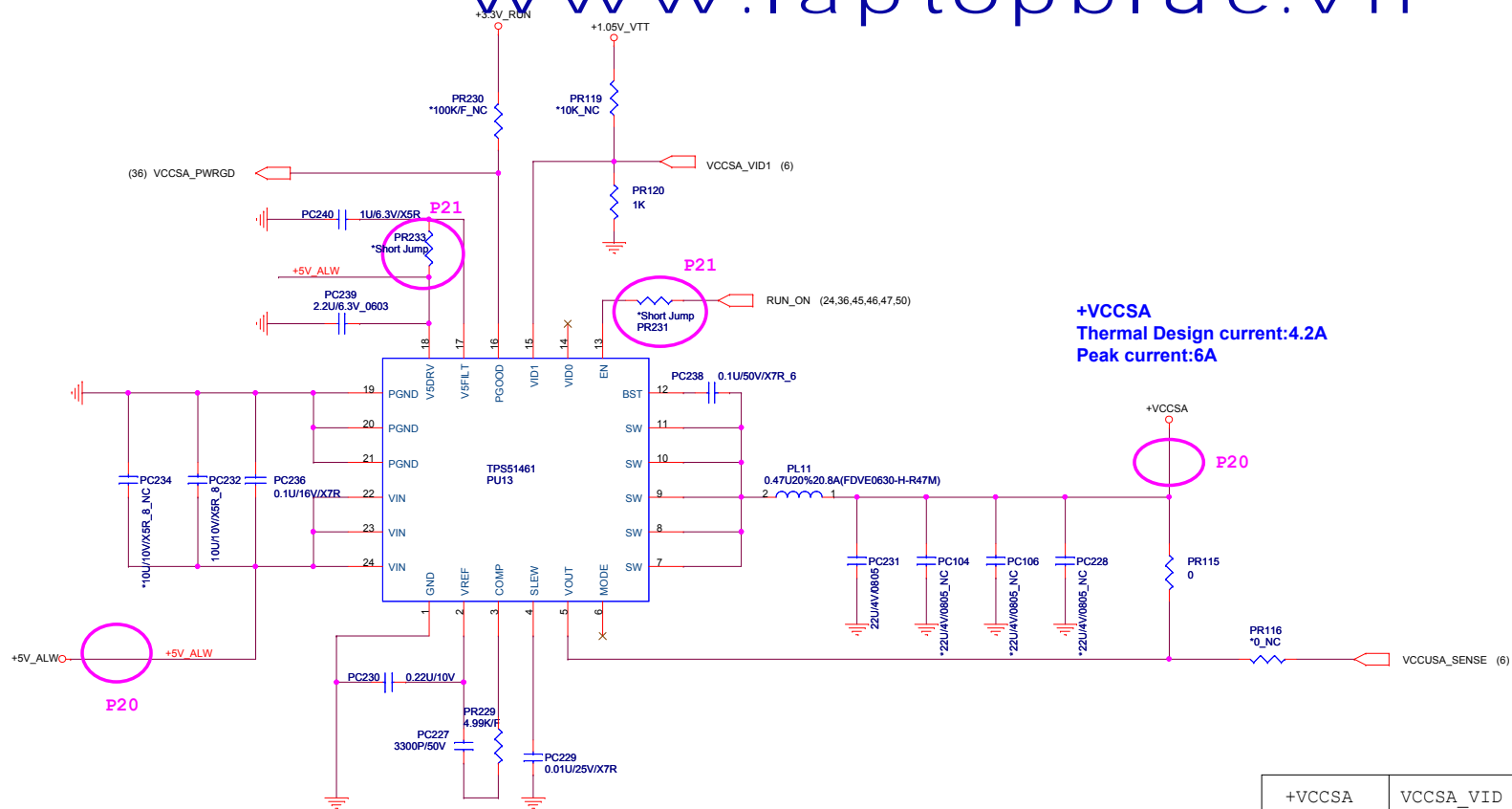


MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

N12P-GE:

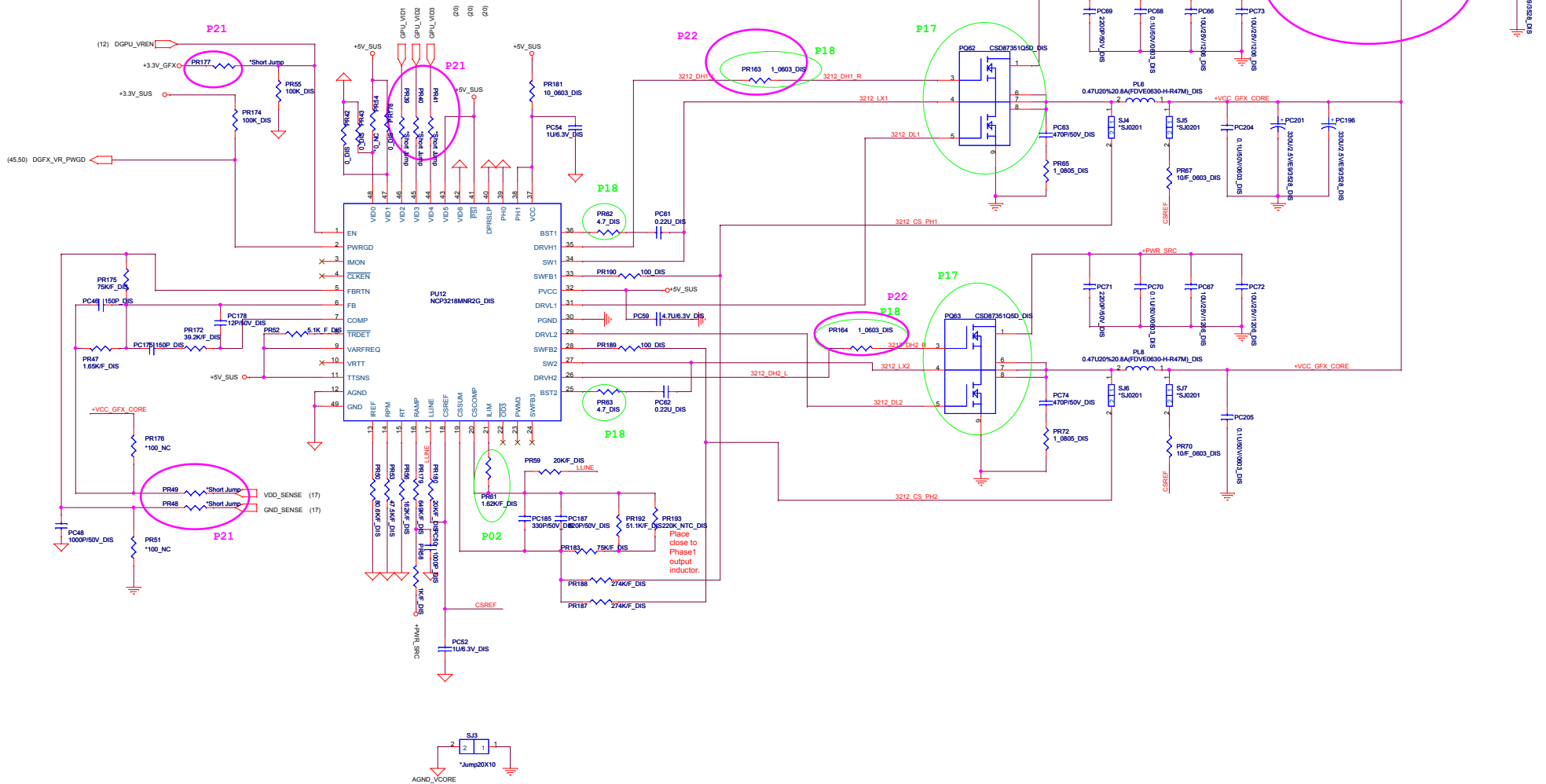
GPU VID3	GPU VID2	GPU VID1
0.85V	1	0
0.95V	0	1
1.0V	0	1

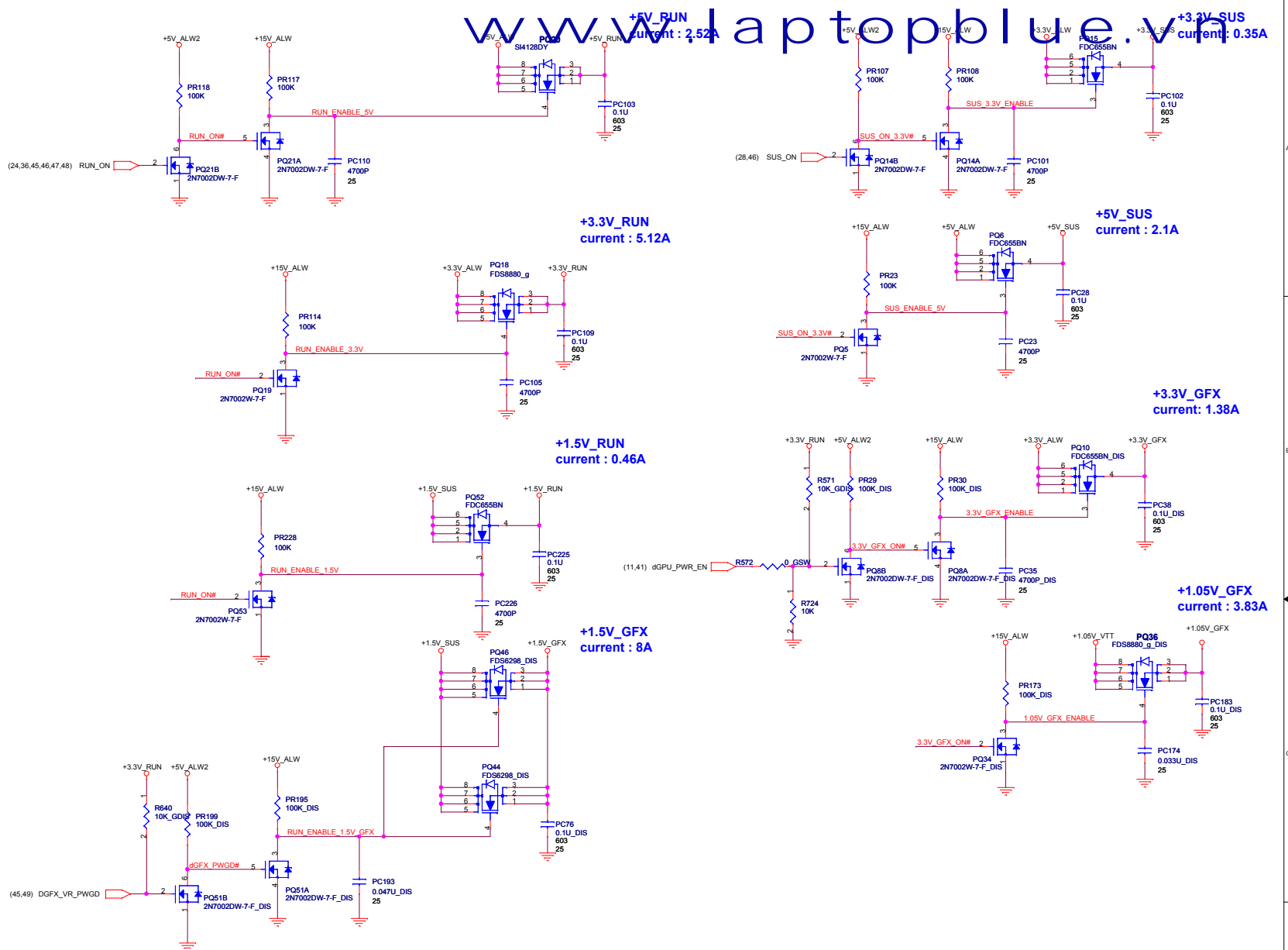
N12P-GS:

GPU VID3	GPU VID2	GPU VID1
0.825V	1	0
0.975V	0	1
1.0V	0	1

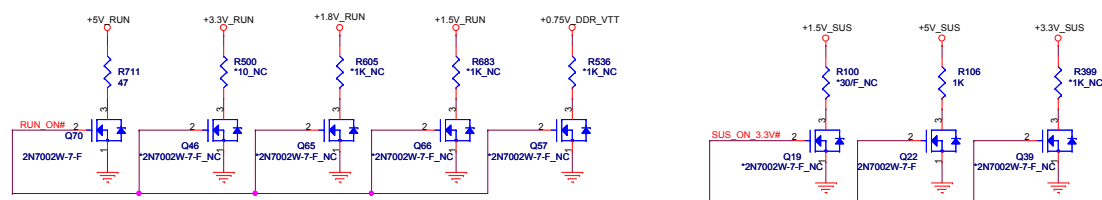
	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

+VCC_GFX_CORE
F_s=300K
Current:21.81A
OCP:52A





Reserve discharge path

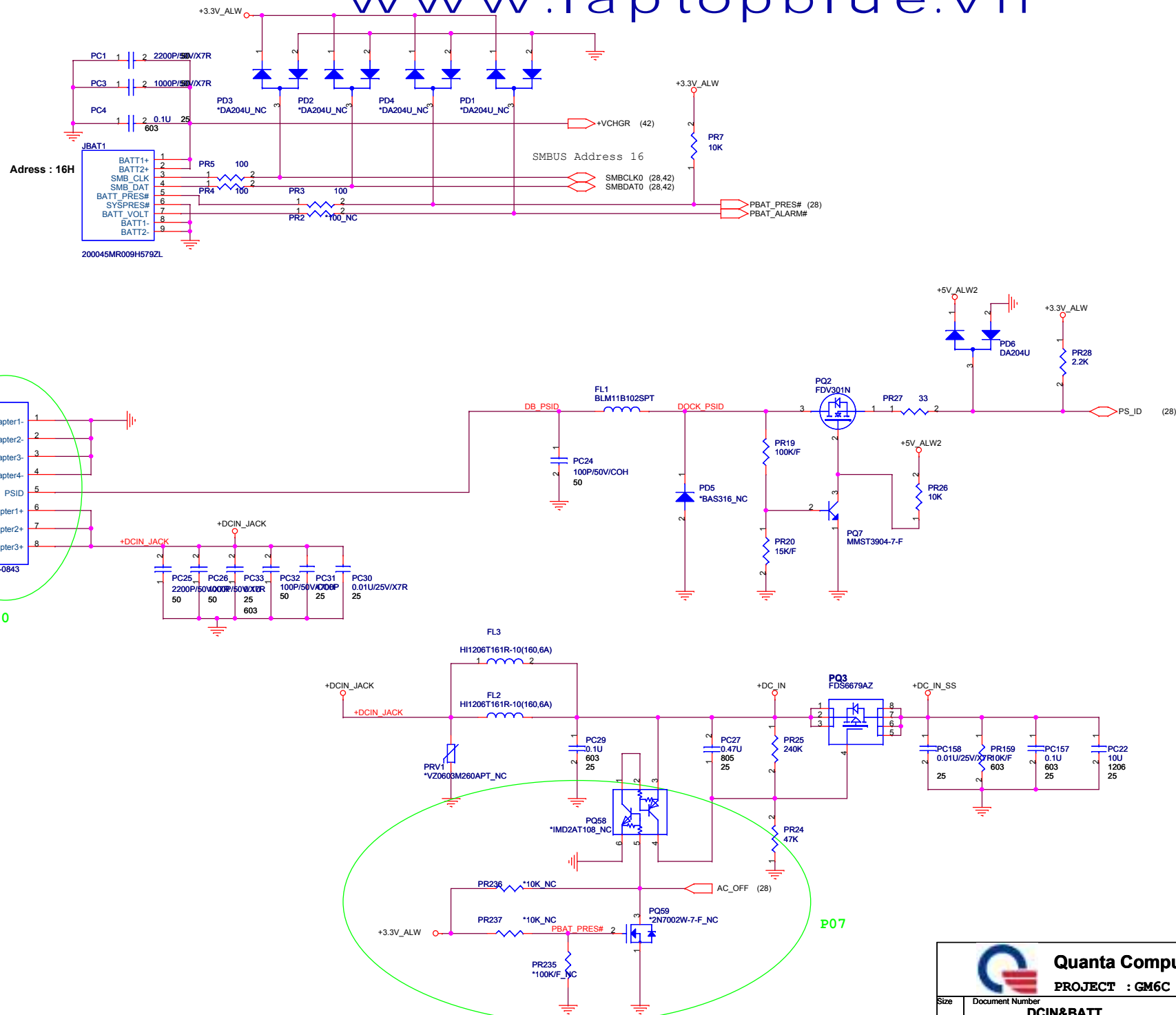
**Quanta Computer Inc.**

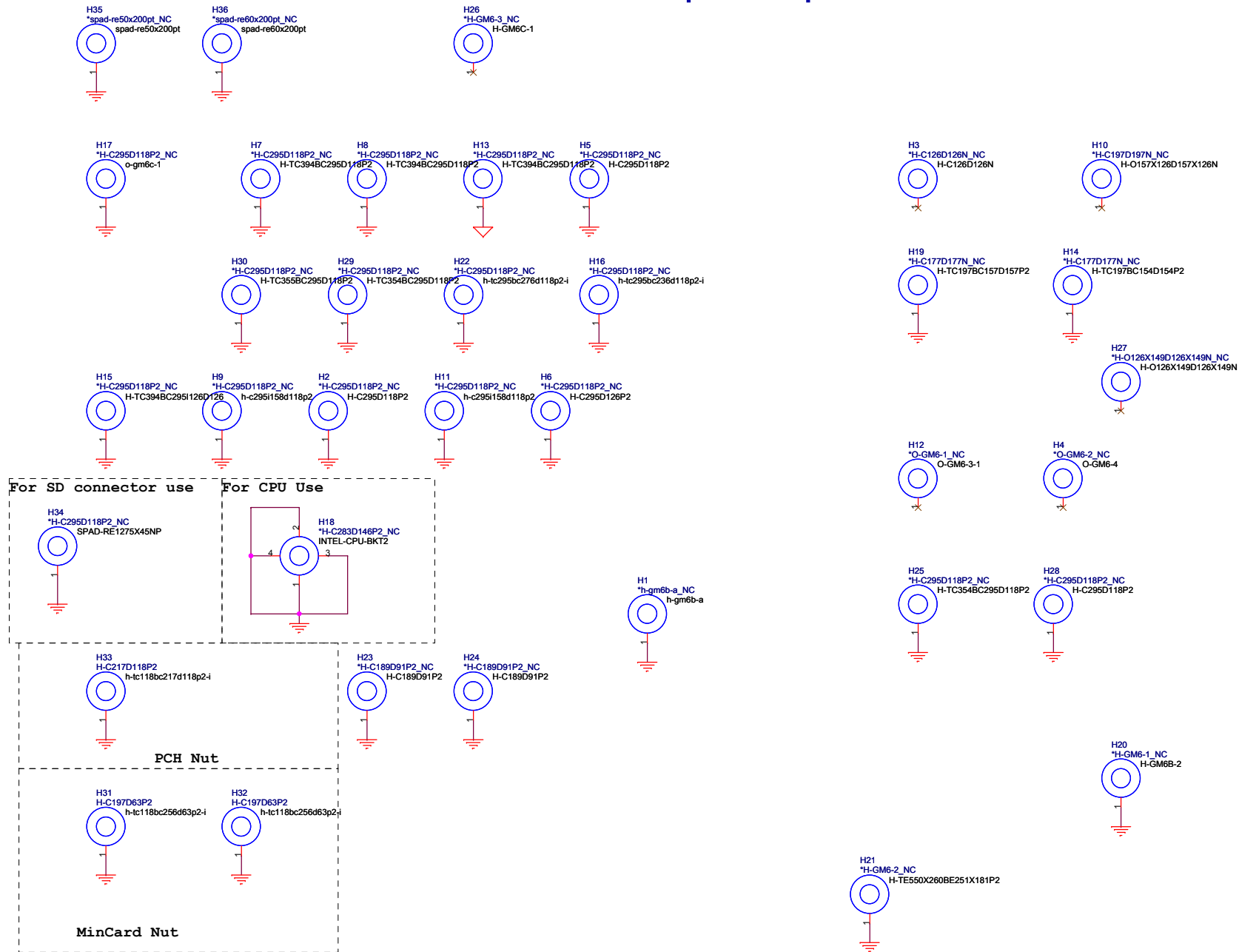
PROJECT : GM6C MLK DIS

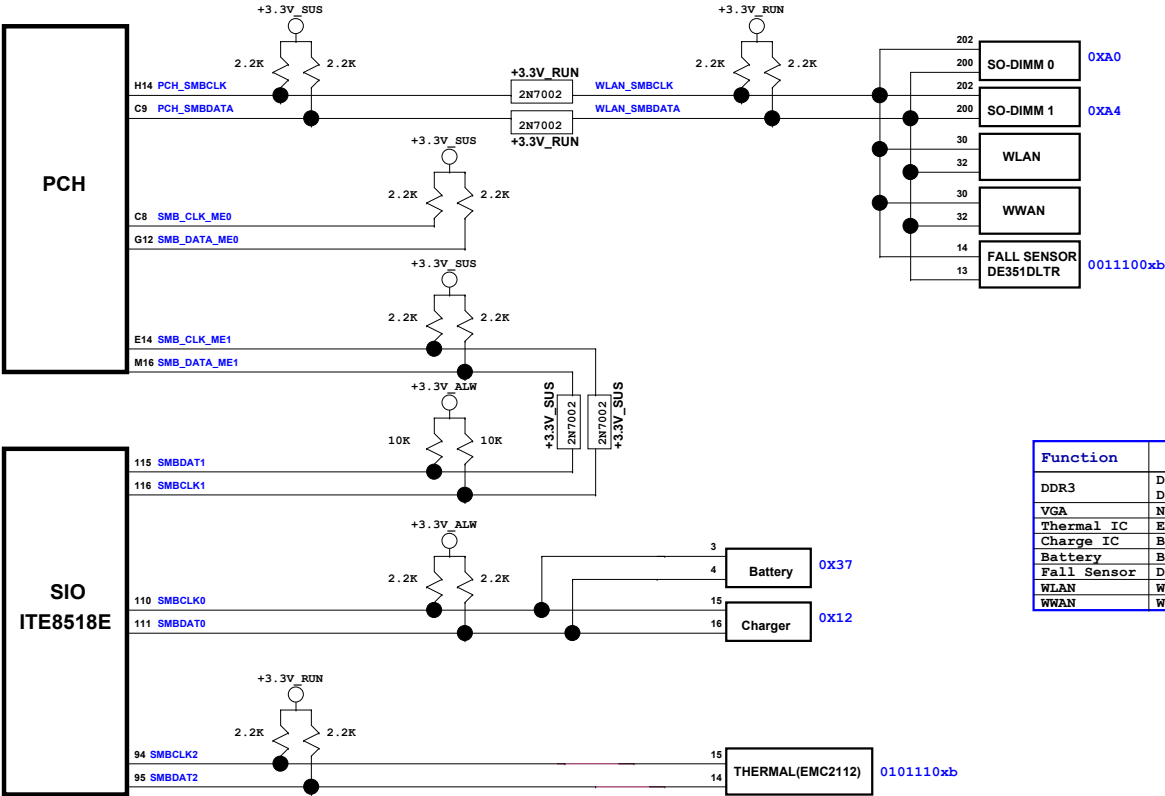
Run Power Switch

Size	Document Number	Rev
	Run Power Switch	1A
Date:	Friday, January 07, 2011	Sheet 50 of 59

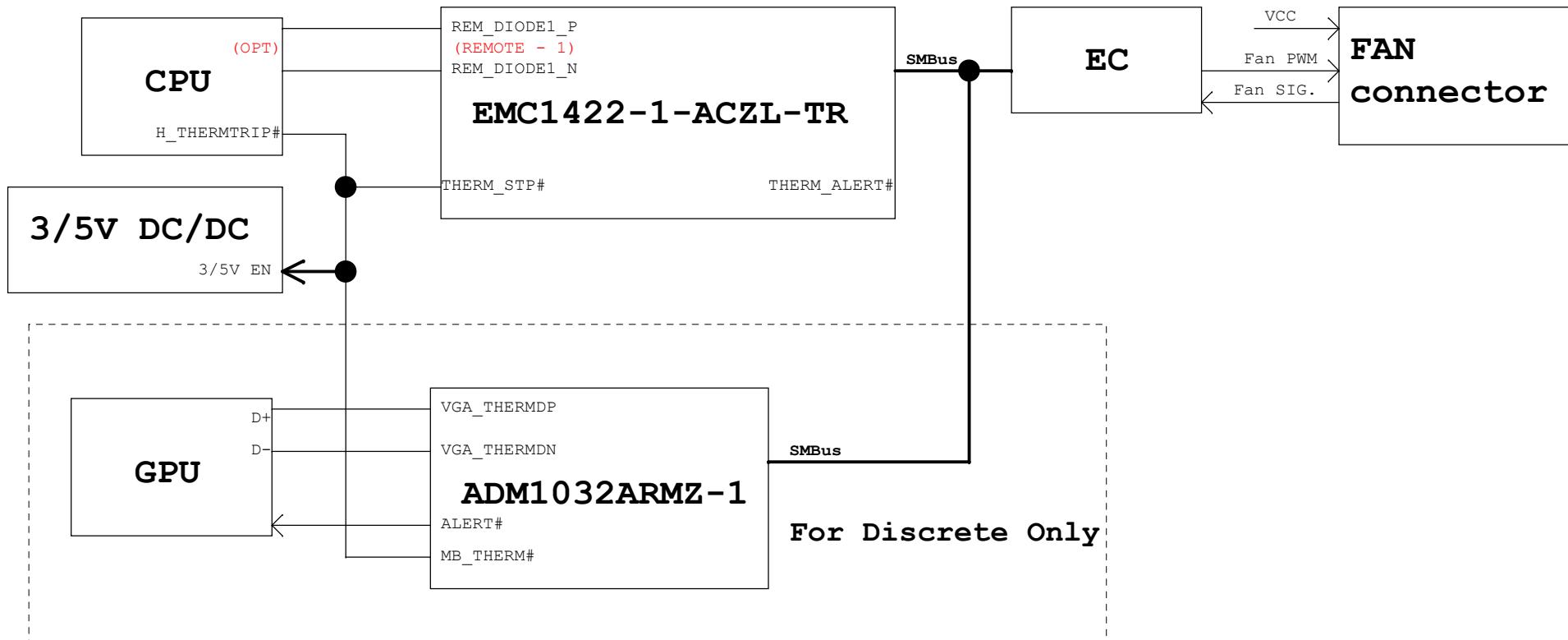
Rev

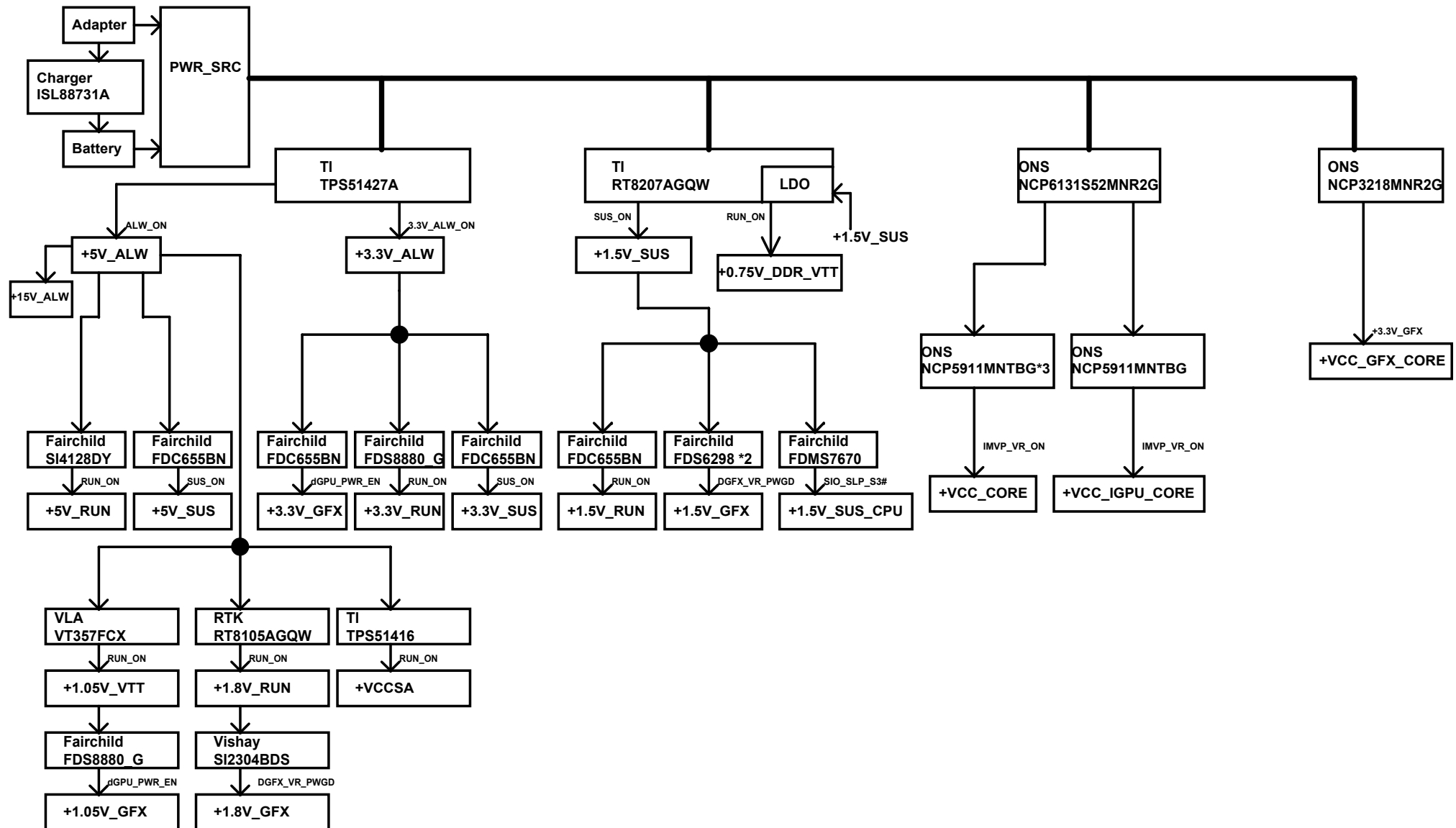




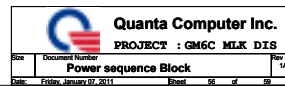


Function	IC	SMBus Address
DDR3	DIMM0	A0
	DIMM1	A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X



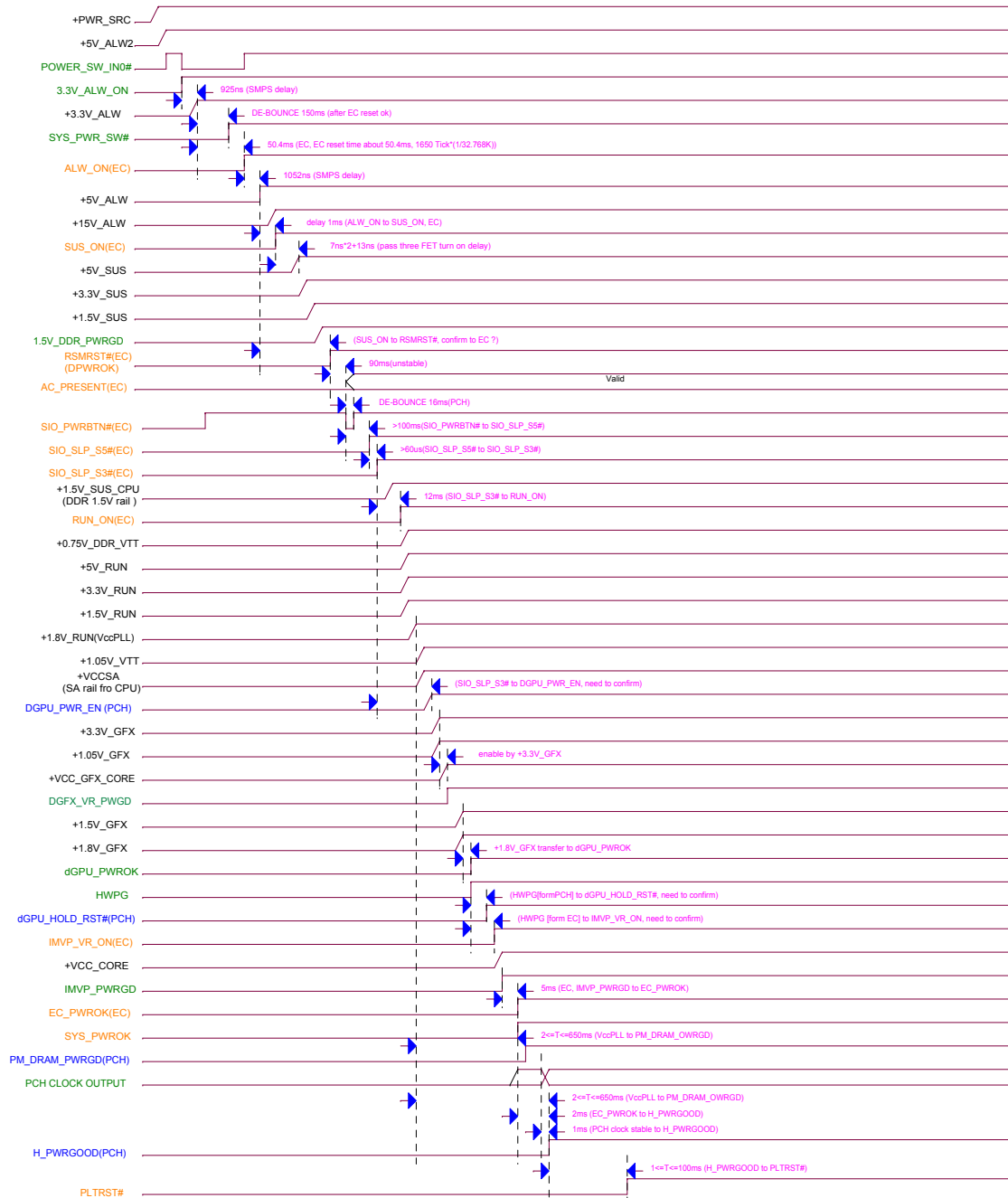


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