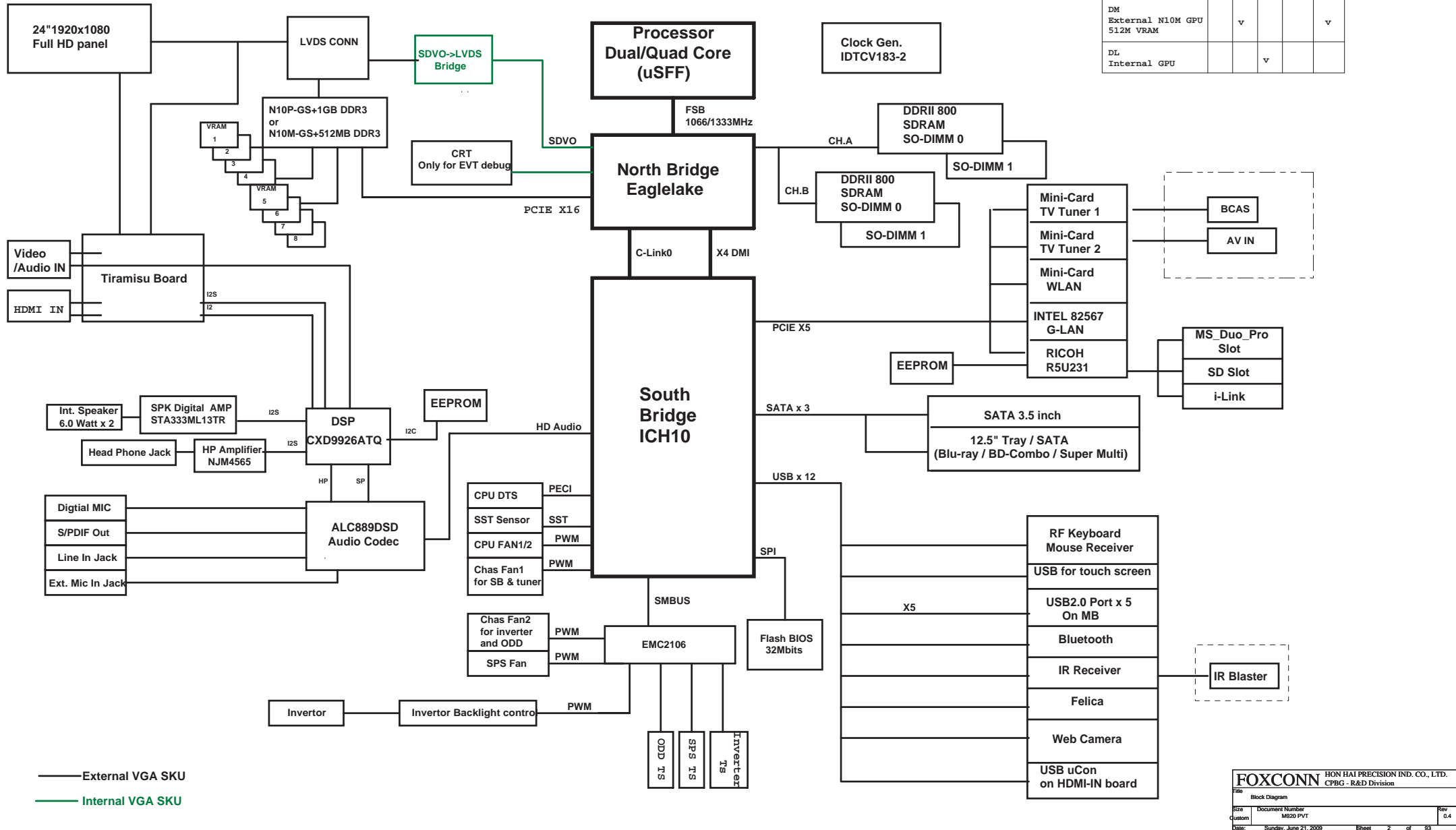
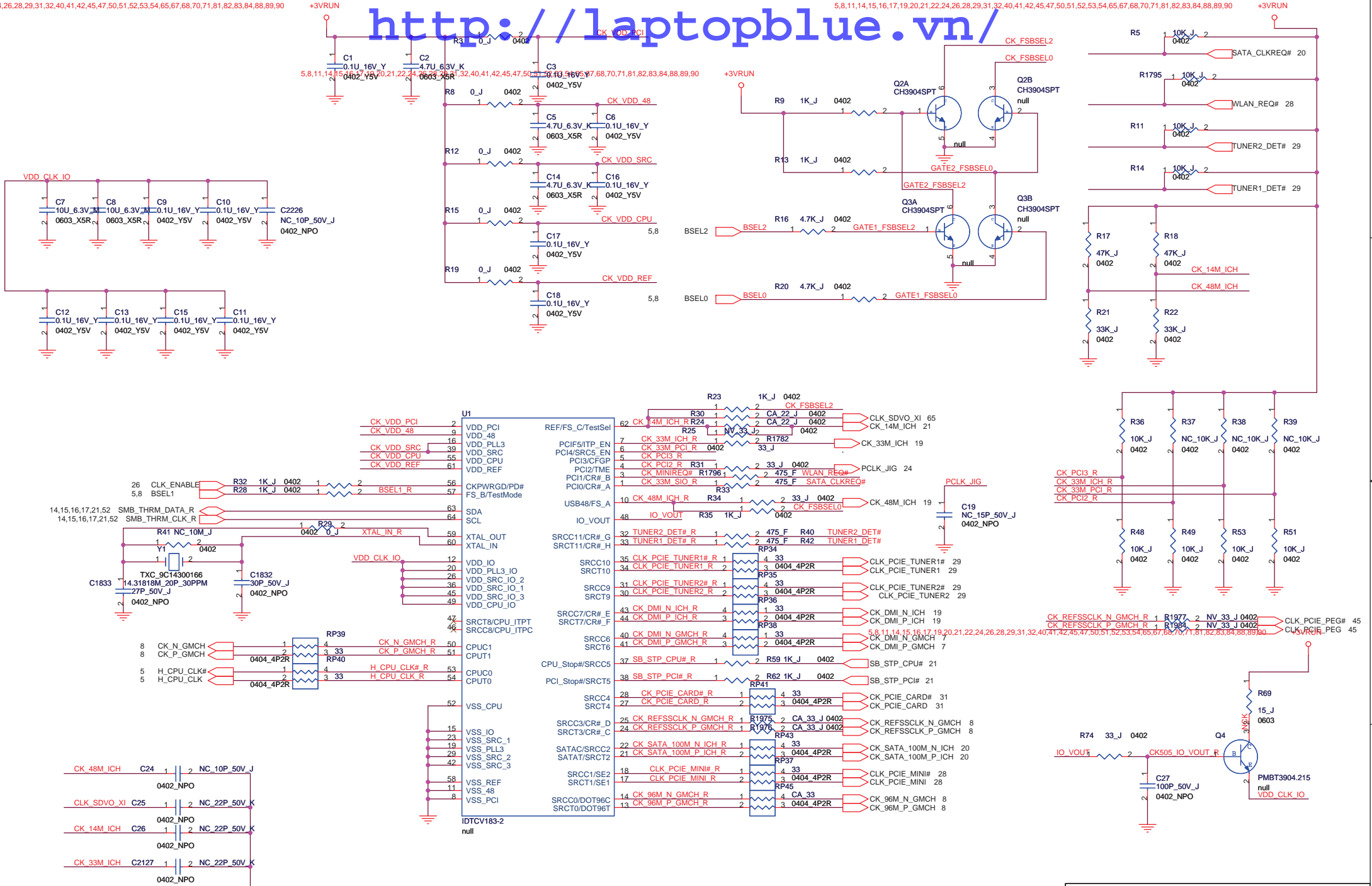


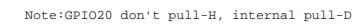
## Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Index Page			53	VGA (CRYSTAL)		
02	Block Diagram(Syatem)			54	VGA (SSC)		
03	CLOCK GEN			55	VGA (Change History)		
04	CPU HOST 1/3			56	VGA (PWR&GND)		
05	CPU THERMAL 2/3			57	VGA (RF solution)		
06	CPU POWER 3/3			58	VGA (VRAM DDR3) 1/4		
07	Eaglelake HOST/PCI-E 1/7			59	VGA (VRAM DDR3) 2/4		
08	Eaglelake VGA/MISC 2/7			60	VGA (VRAM DDR3) 3/4		
09	Eaglelake DDRII CH A 3/7			61	VGA (VRAM DDR3) 4/4		
10	Eaglelake DDRII CH B 4/7			62	VGA (VRAM BYPASS)		
11	Eaglelake POWER 5/7			63	VGA (VRAM BYPASS)		
12	Eaglelake POWER 6/7			64	VGA (HIDEMI CONN)		
13	Eaglelake GND 7/7			65	VGA (SDVO To LVDS)		
14	DDRII(CHA DIMM0) 1/4			66	VGA (INVERTER)		
15	DDRII(CHA DIMM1) 2/4			67	VGA (LVDS OUTPUT)		
16	DDRII(CHB DIMM0) 3/4			68	VGA (CRT for DEBUG)		
17	DDRII(CHB DIMM1) 4/4			69	AUDIO Block Diagram		
18	DDRII Termination			70	AUDIO(CODEC & POWER)		
19	ICH10(PCIe/USB/PCI) 1/5			71	AUDIO DSP		
20	ICH10(HOST/SATA)2/5			72	AUDIO(SPK AMP)		
21	ICH10(PM/LAN/HDA)3/5			73	AUDIO( HP&Vedio IN )		
22	ICH10(Power)4/5			74	AUDIO( EXTMIC)		
23	ICH10(Ground)5/5			75	AUDIO( LINE IN)		
24	Flash ROM&Debug			76	AUDIO (MUTE)		
25	Power Squence 1/2			77	Power Block Diagram		
26	Power Squence 2/2			78	DCIN		
27	INTEL GLAN Boazman			79	SYSPWR(+3V/+5V)		
28	PCIe WLAN			80	DDR2PWR(+1_8V/+0_9V)		
29	TV-TUNER			81	SYSPWR(+1_1V)		
30	AVIN/IR DB CONN			82	SYSPWR(+1_2V)		
31	PCIE BUS1/2			83	SYSPWR(+1_5V)		
32	PCIE BUS2/2			84	VGAPWR		
33	SATA HDD/ODD			85	VHCORE (1) -- ISL6334A		
34	Side USB Ports			86	VHCORE (2) -- ISL6208		
35	Felica			87	HDD PWR+12V		
36	CIR&BT			88	OVP Portect		
37	RF KB			89	Others PWR Plane		
38	Camera			90	HOLE&BOSS&EMI&RF		
39	Tarte			91	Change History		
40	Thermal&BL			92			
41	FAN			93			
42	LED			94			
43	DB CONN			95			
44	VGA Block Diagram			96			
45	VGA (PCI-E)			97			
46	VGA (PCI-E TX)			98			
47	VGA (PCIE RX&STRAP)			99			
48	VGA (FBA_DDR3)						
49	VGA (FBC_DDR3)						
50	VGA (DACAB)						
51	VGA (IFP_ABCDEF)						
52	VGA (GPIO)						

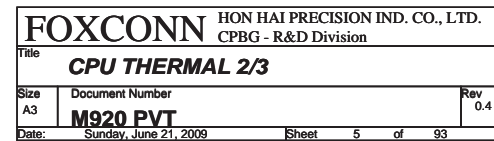
# M920 Block Diagram (24" Wide Screen)

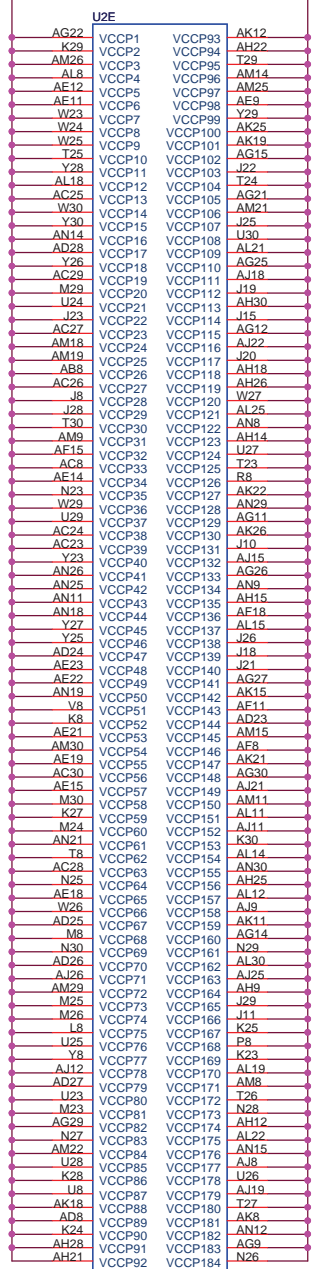




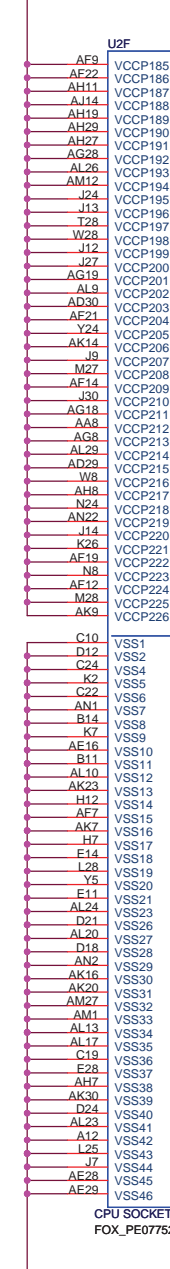


<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title		<b>CPU HOST 1/3</b>	
Size A3	Document Number <b>M920 PVT</b>		Rev 0.4
Date:	June 21, 2009	Sheet	4 of 93





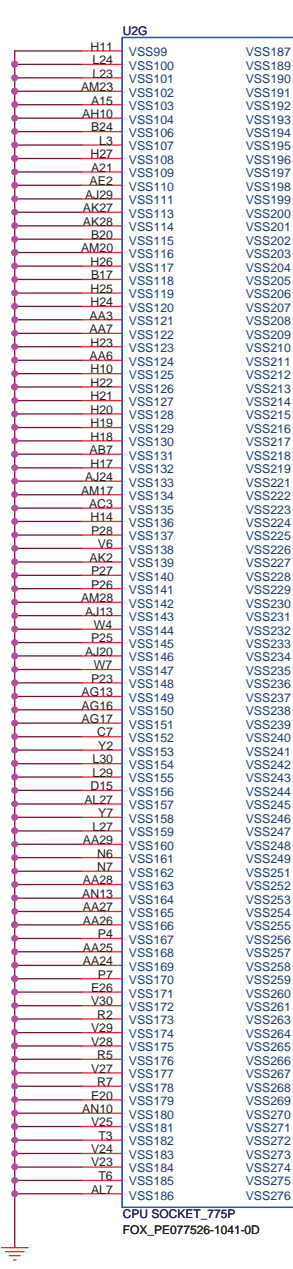
CPU SOCKET\_775P  
FOX\_PE077526-1041-0D



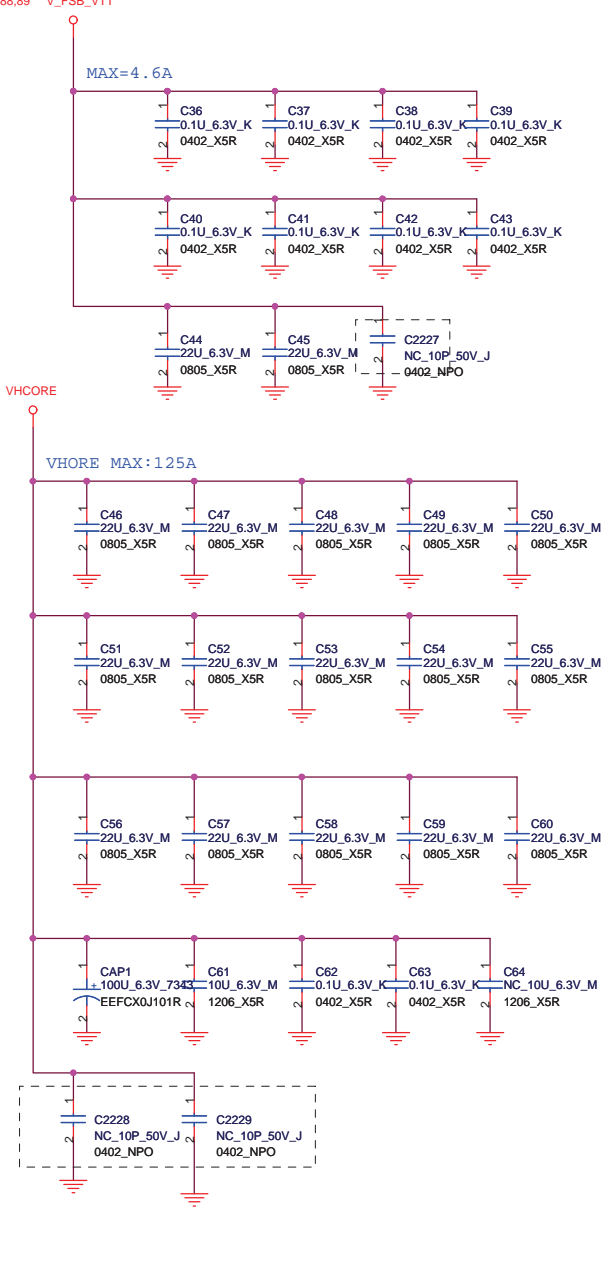
VTT



CPU SOCKET\_775P  
FOX\_PE077526-1041-0D



CPU SOCKET\_775P  
FOX\_PE077526-1041-0D

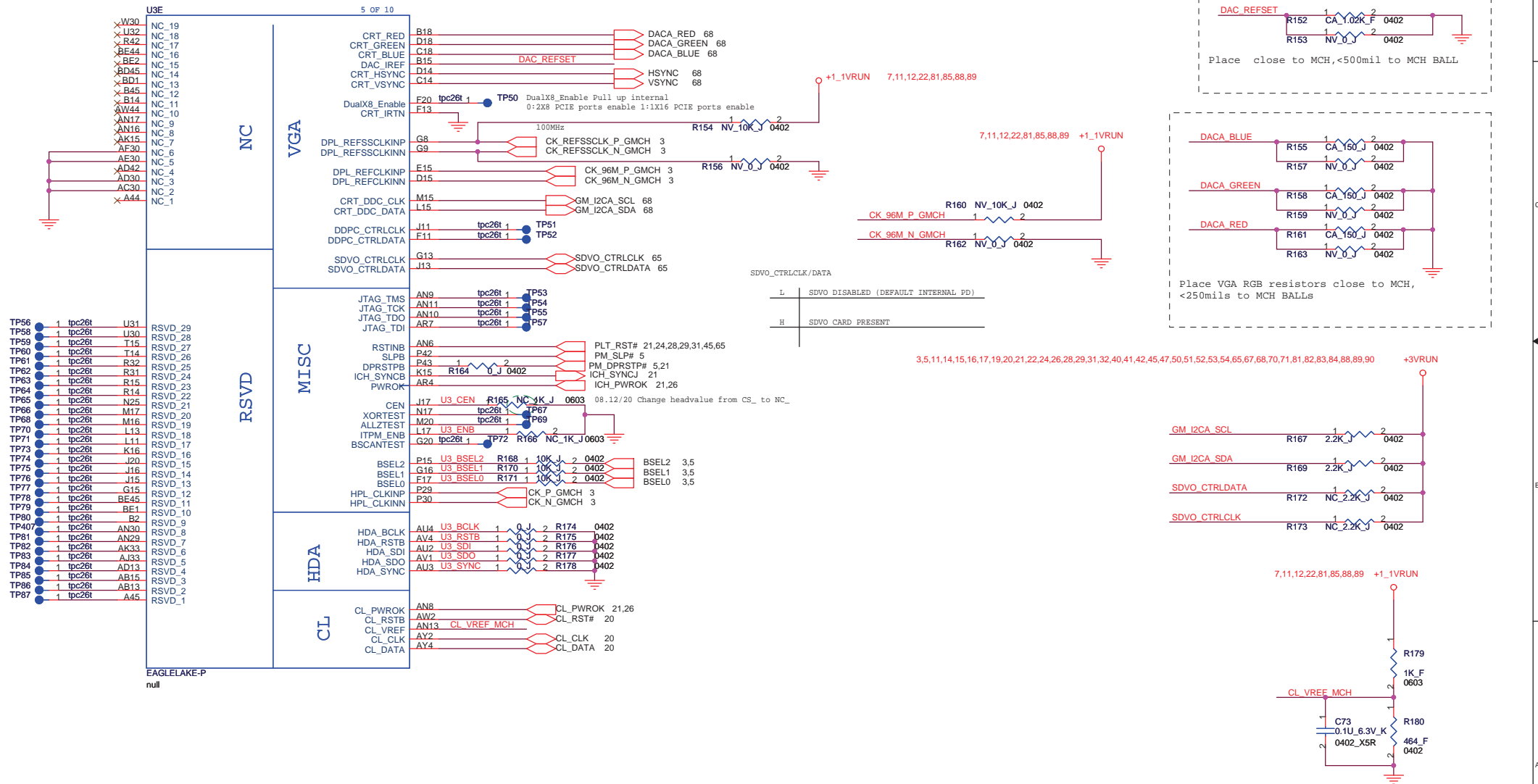


CPU SOCKET\_775P  
FOX\_PE077526-1041-0D

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
CPU POWER 3/3		CPBG - R&D Division	
File	M920 PVT		
Size	Document Number	Rev 0.4	
A3	M920 PVT		
Date:	Sunday, June 21, 2009	Sheet	6 of 93







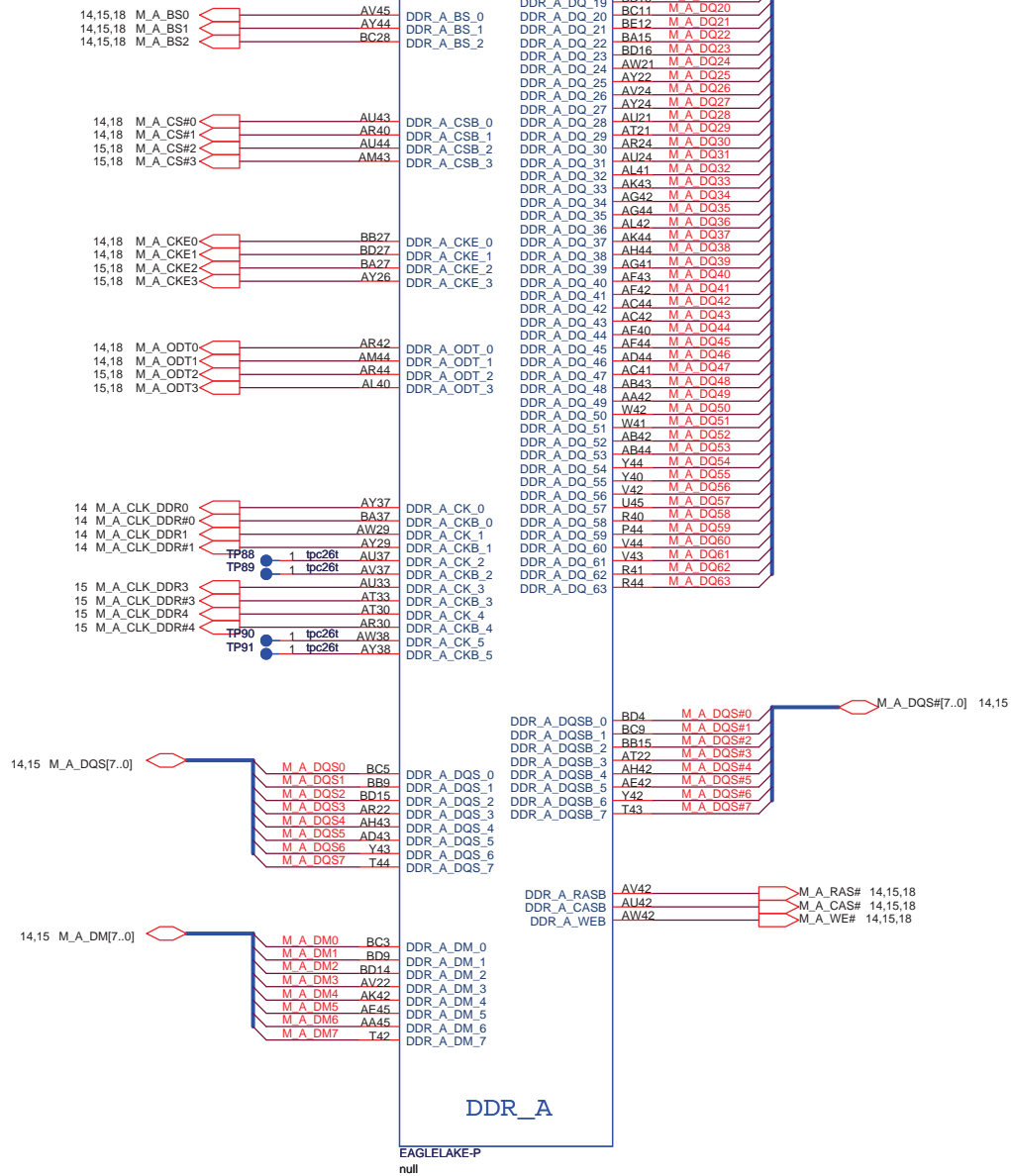


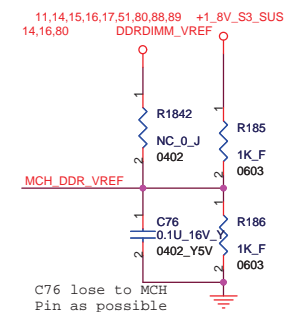
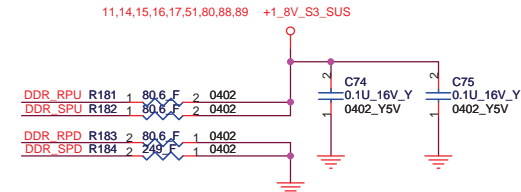
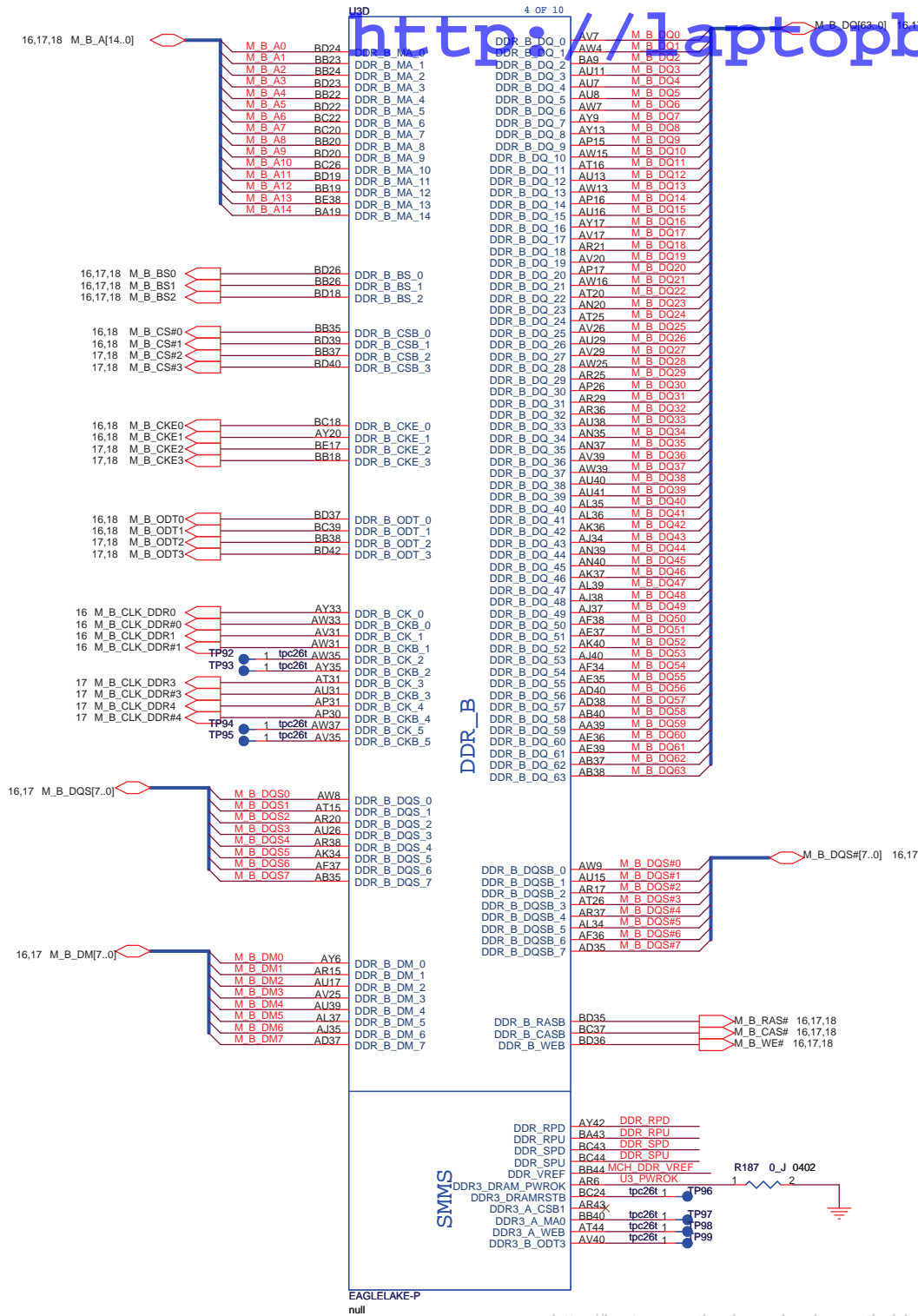
The screenshot shows a network packet capture analysis tool. The main display area shows a large blue packet with the URL 'http://laptopblue.v.'. The packet details pane on the right shows the Ethernet II frame structure, including MAC addresses and frame length.

Frame	Length	Source	Destination	Ethernet II Type
14,15,18	1500	08:00:27:00:00:00	08:00:27:00:00:00	0x0000

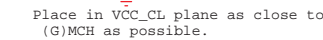
Packet Details:

- Ethernet II, Src: M\_A\_00 (08:00:27:00:00:00), Dst: M\_A\_DQ (63.01:14:15), Type: M\_A\_00 (08:00:27:00:00:00)
- Internet Protocol Version 4, Src: 192.168.1.1, Dst: 192.168.1.1
- TCP, Src Port: 80, Dst Port: 80
- HTTP, GET / HTTP/1.1





```
external Gfx:2.08A(max)
internal Gfx:1.31A(max)
```



```
external Gfx:0.9229A(max)
internal Gfx:2.0597A(max)
```

10,14,15,16,17,51,80,88,89 +1\_8V\_S3\_SUS

```
external Gfx:0.9229A(max)
internal Gfx:2.0597A(max)
```

10,14,15,16,17,51,80,88,89 +1\_8V\_S3\_SUS

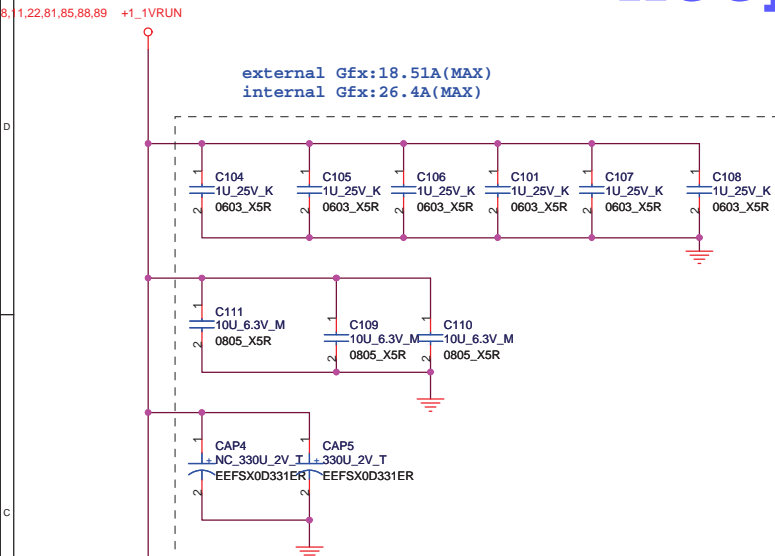
7,8,12,22,81,85,88,89 +1\_1VRUN

262.6mA

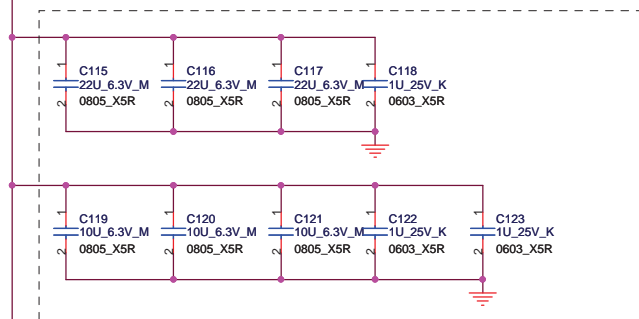
Place this parts close to  
VCC\_SMCLK ballout in MCH backside

7,8,12,22,81,85,88,89 +1\_1VRUN

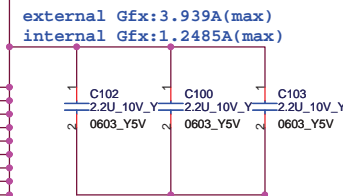
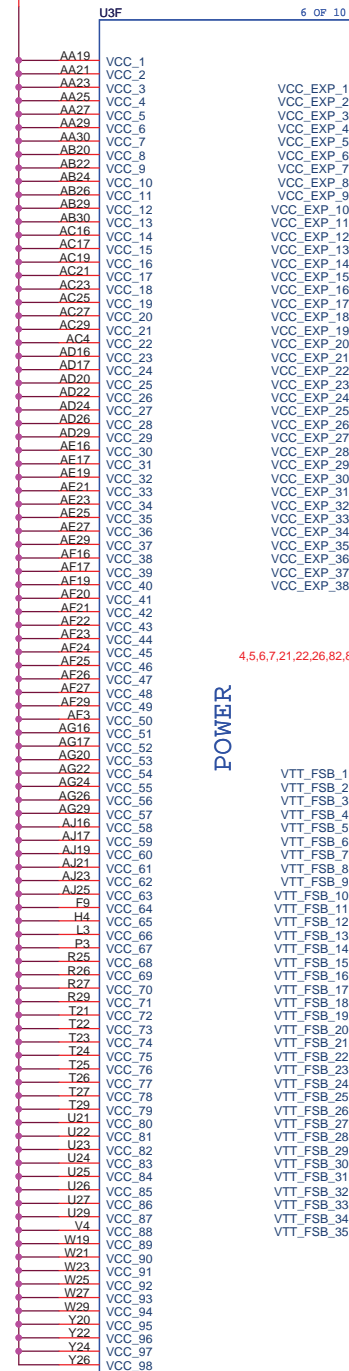
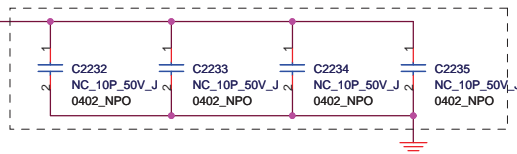
R194 0\_J 0402



Backside cap sites, placed directly underneath the VCC\_Core center-array pins, with sufficient via connections



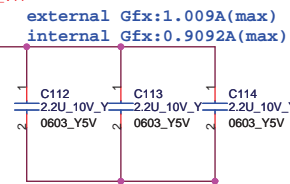
Top-side caps. Place along the (G)MCH edge.



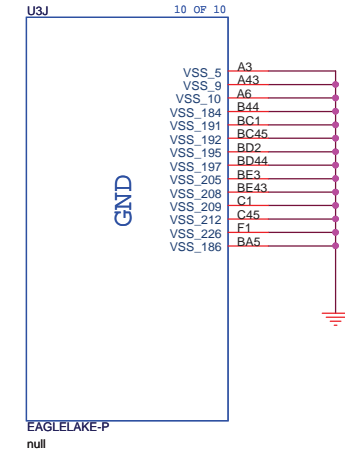
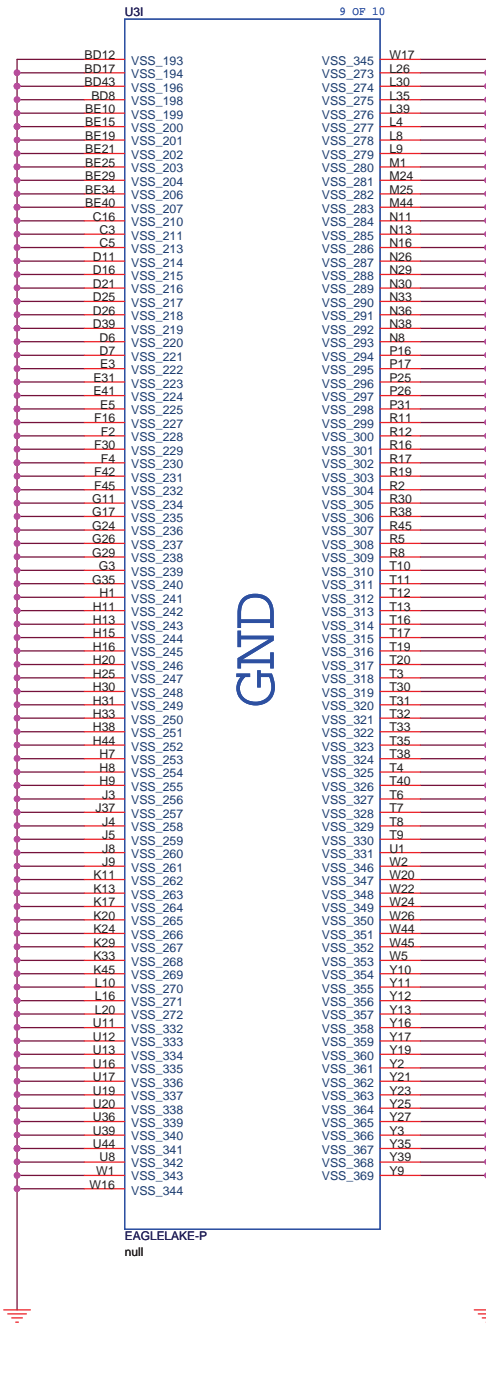
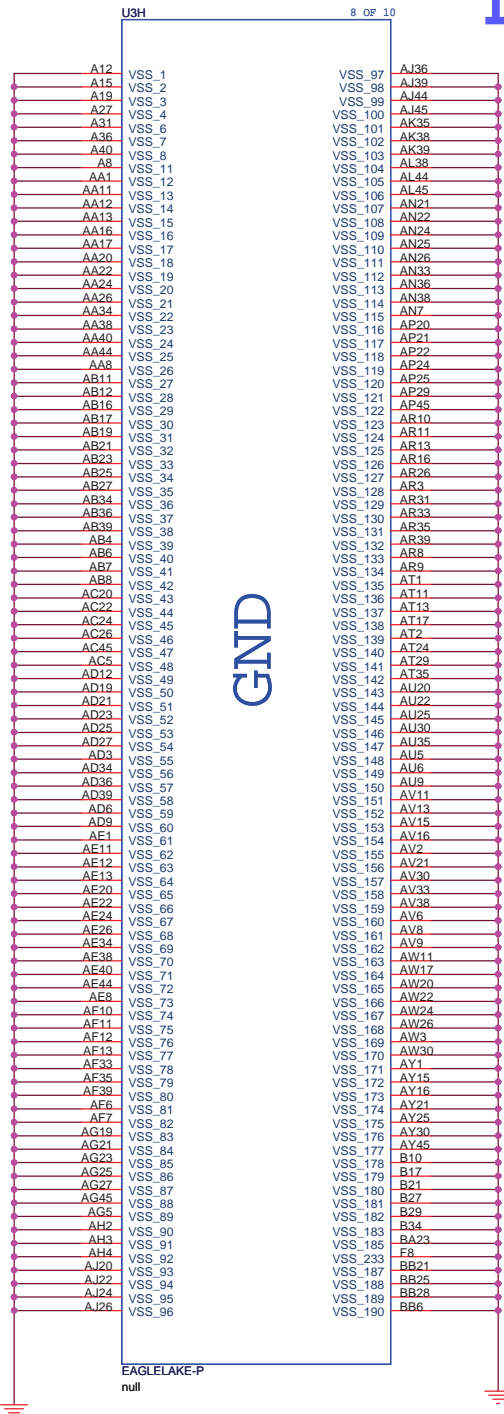
Place in the VCC\_EXP plane as close the (G)MCH as possible

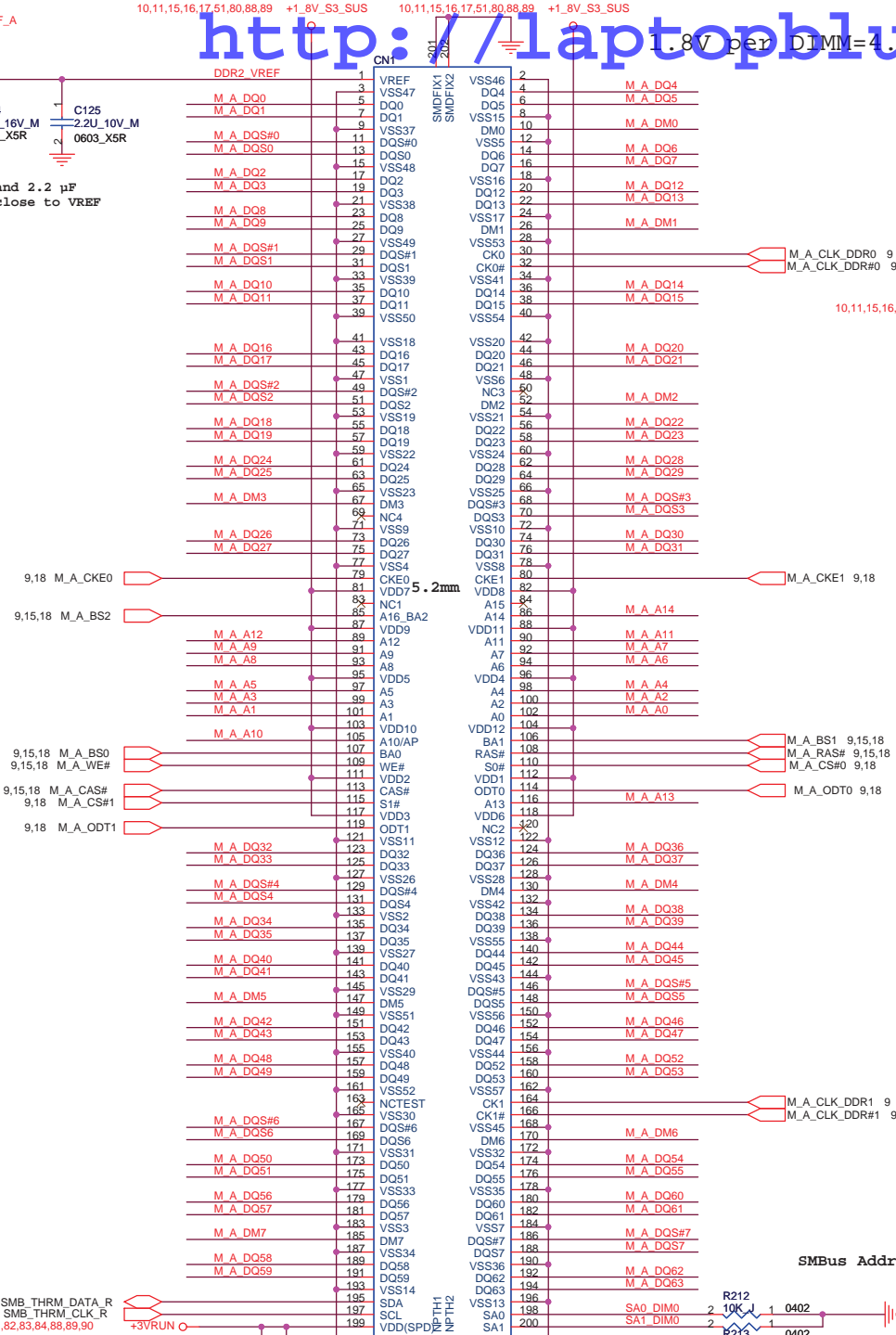
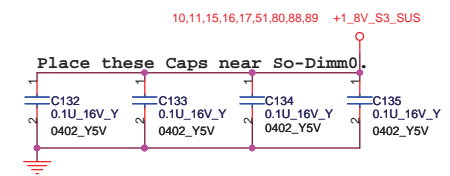
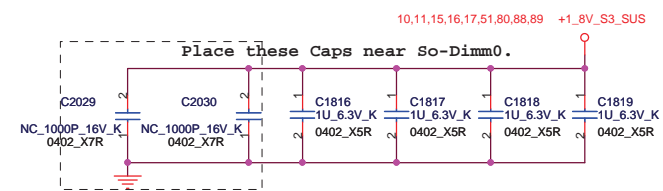
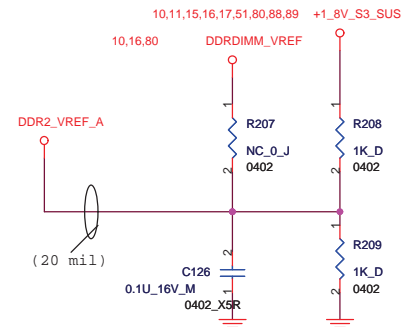
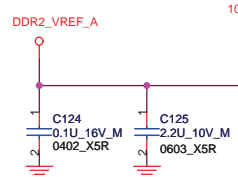
4,5,6,7,21,22,26,82,85,88,89 V\_FSB\_VTT

POWER



Place in the FSB\_VTT plane as close the (G)MCH as possible

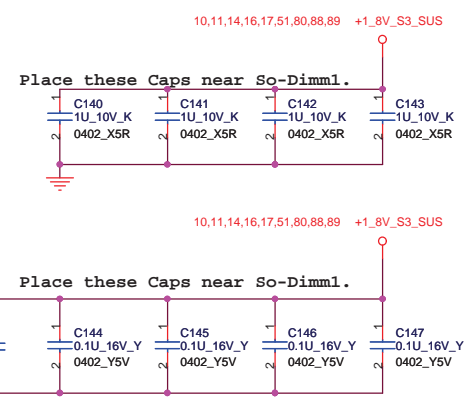
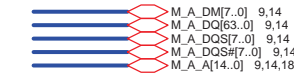
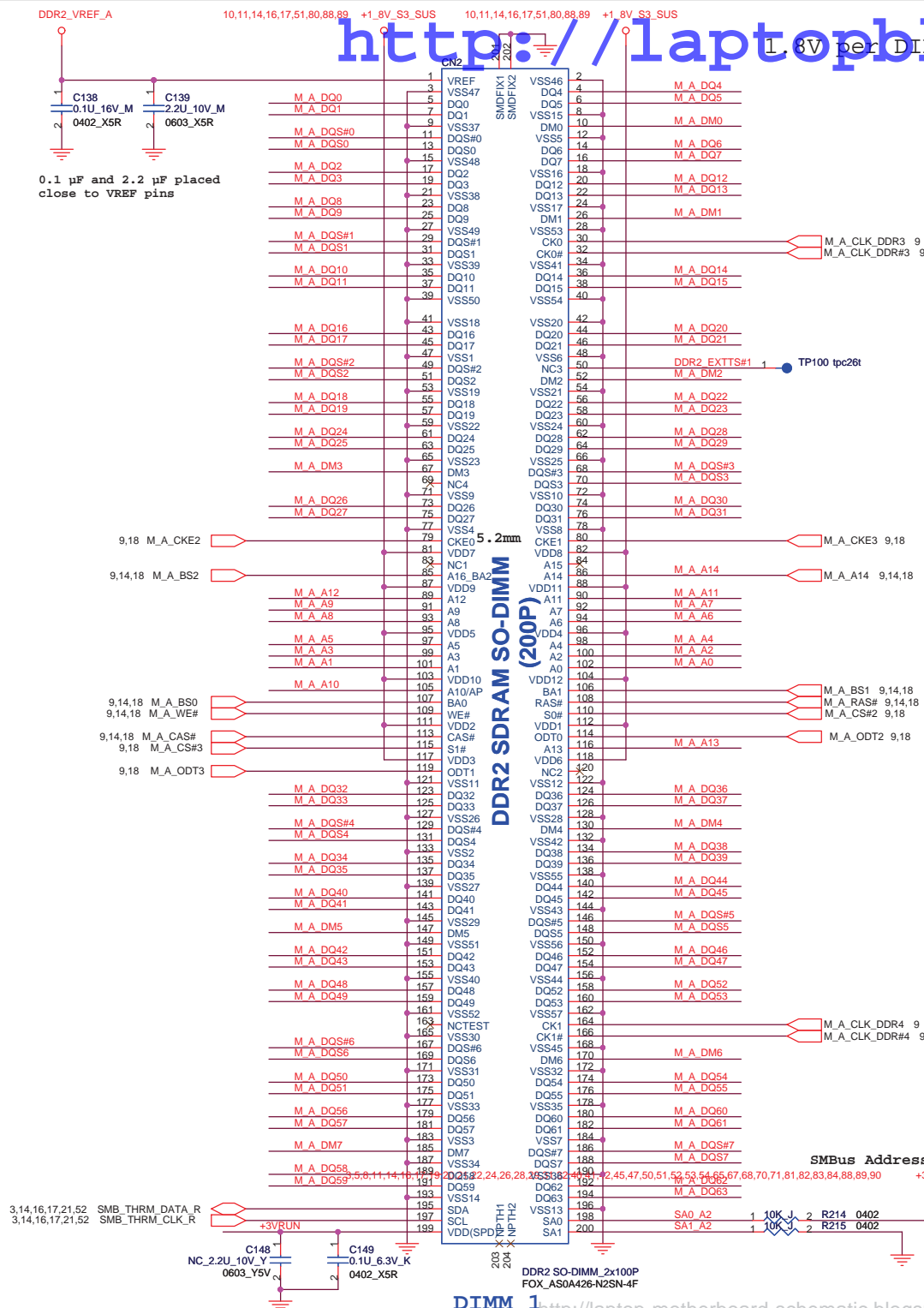




SMBus Address: A0(W)/A1(R)

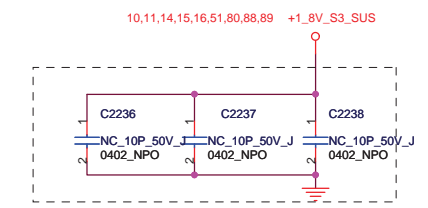
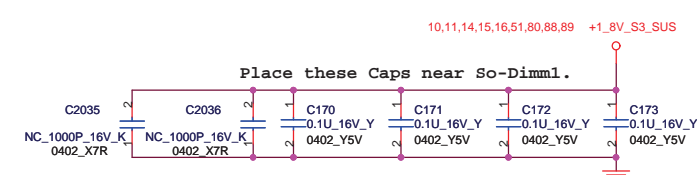
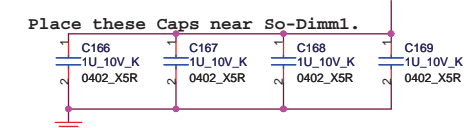
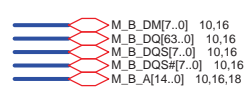
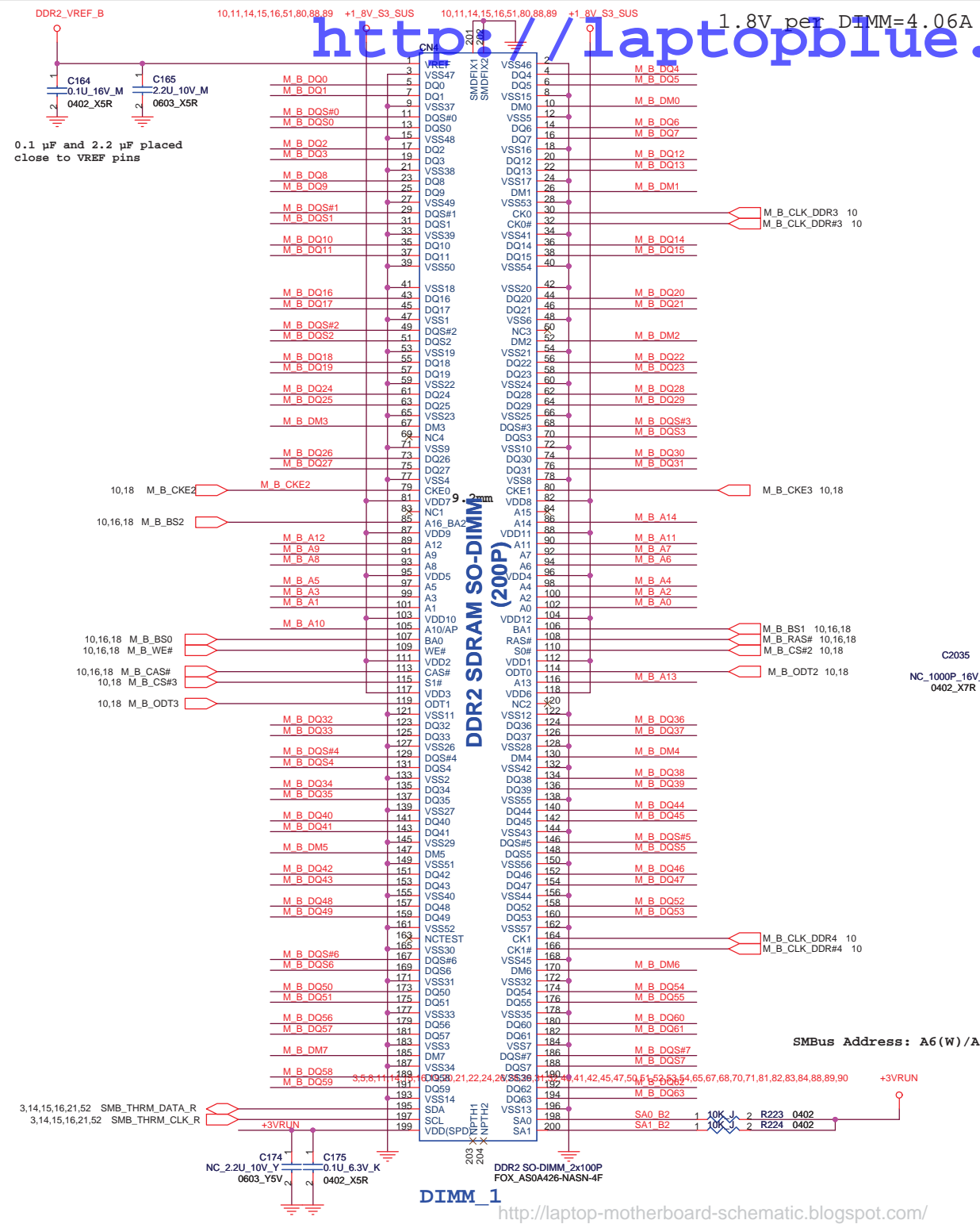
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division			
File <b>DDRII(CHA DIMM0) 1/4</b>			
Size A3	Document Number <b>M920 PVT</b>	Rev 0.4	
Date: Sunday, June 21, 2009	Sheet 14	of 93	







<http://laptopblue.vn/>

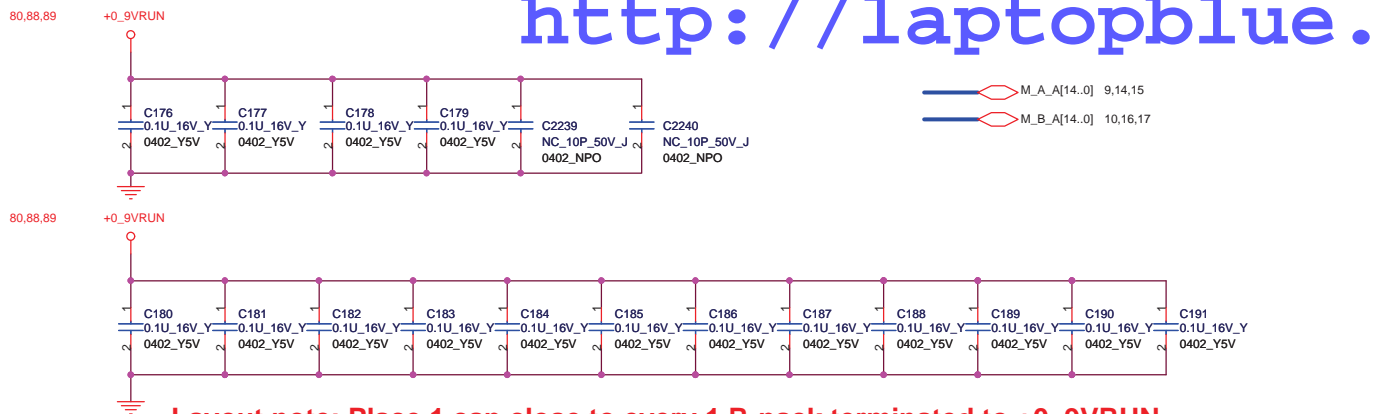


SMBus Address: A6(W)/A7(R)

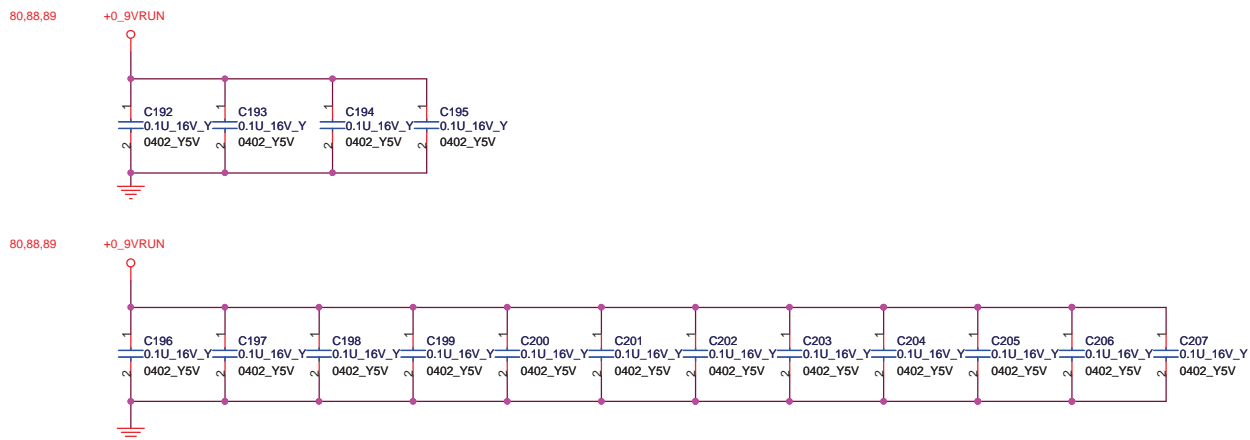
<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
File <b>DDRII(CHB DIMM1) 4/4</b>		
Size A3	Document Number <b>M920 PVT</b>	Rev 0.4
Date: Sunday, June 21, 2009	Sheet 17	of 93

<http://laptop-motherboard-schematic.blogspot.com/>

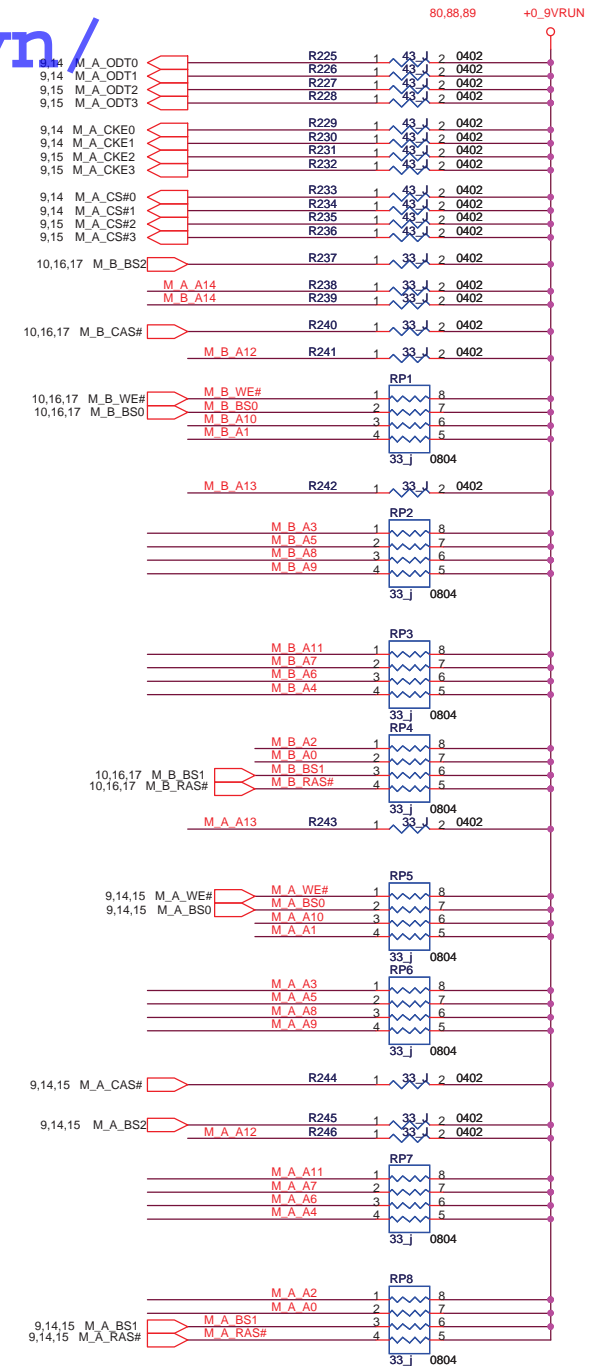
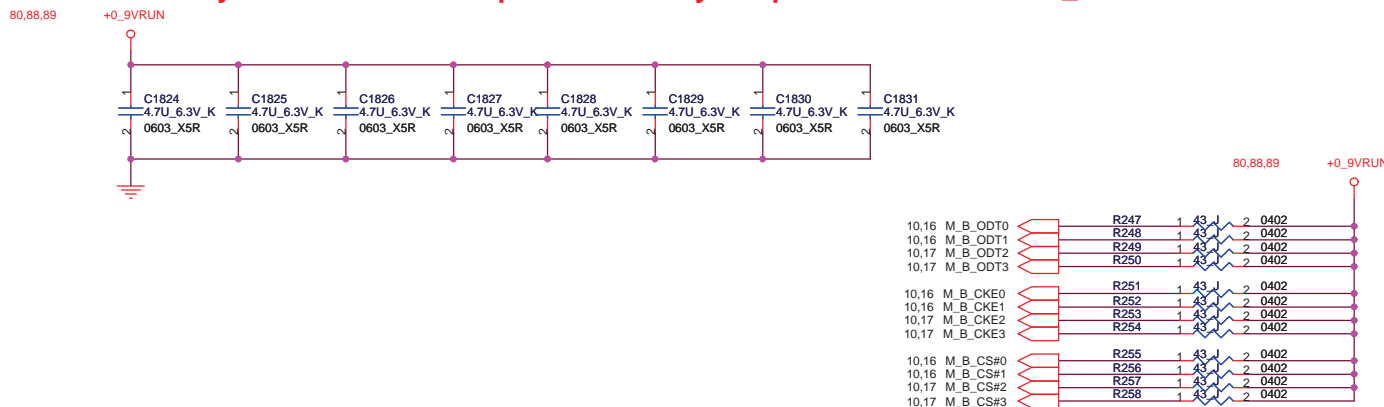
<http://laptopblue.vn/>

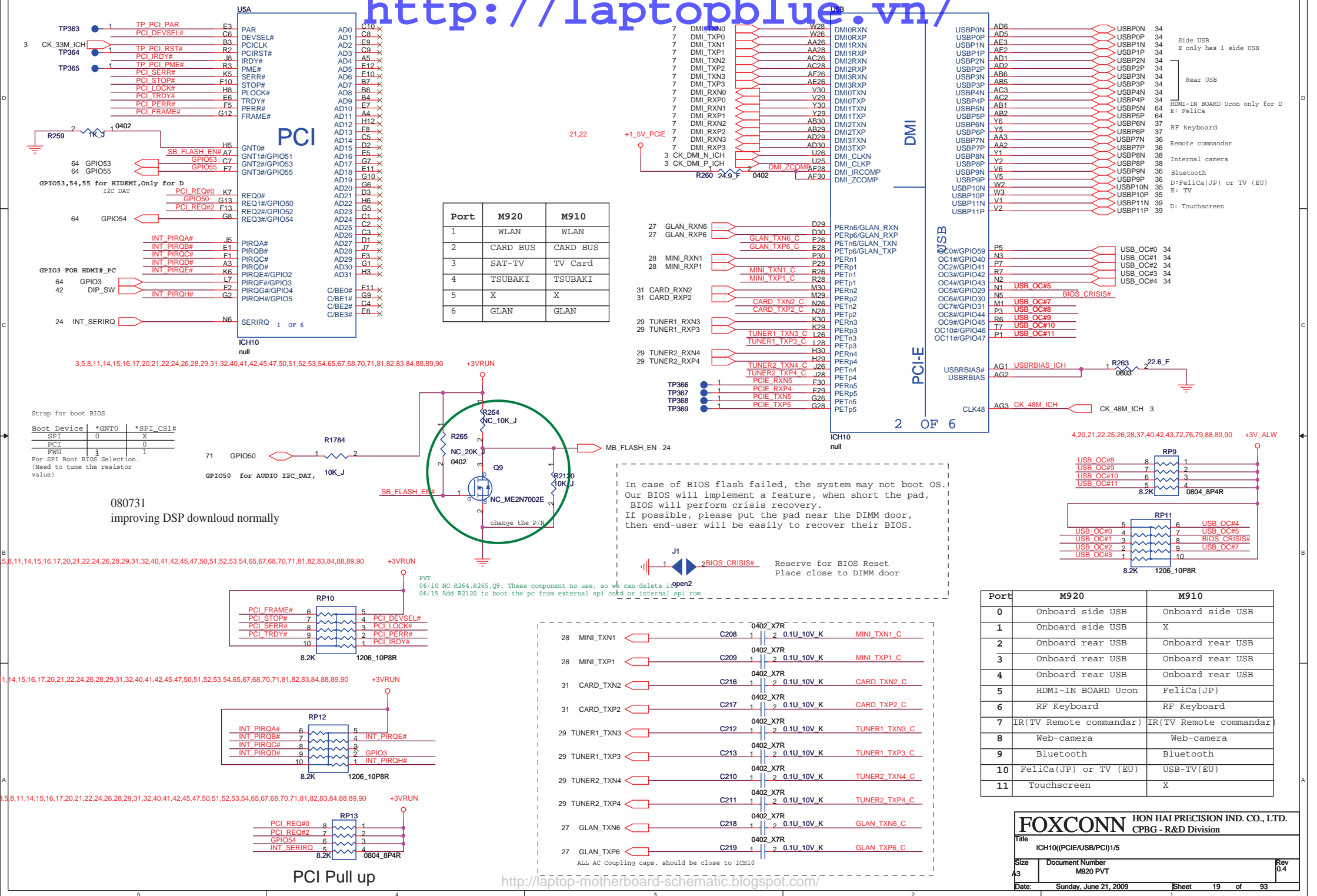


Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VRUN

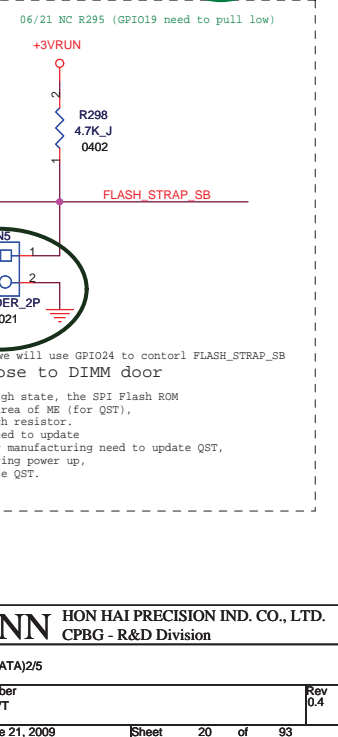
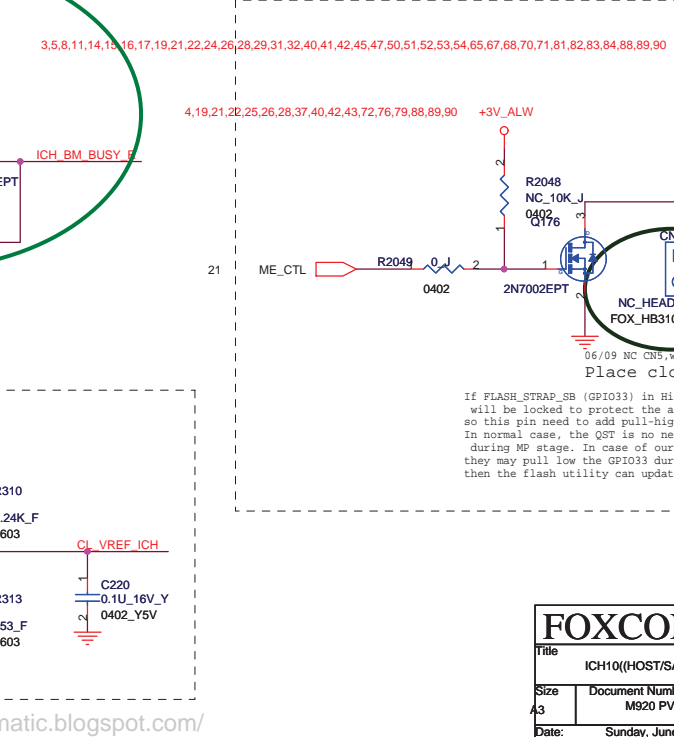
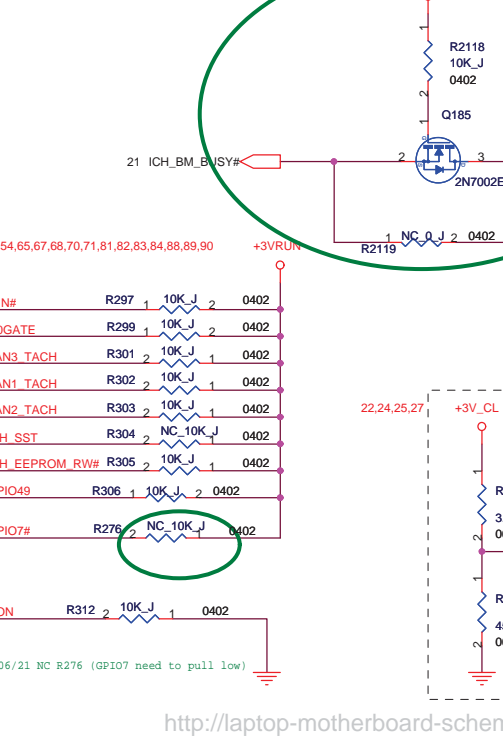
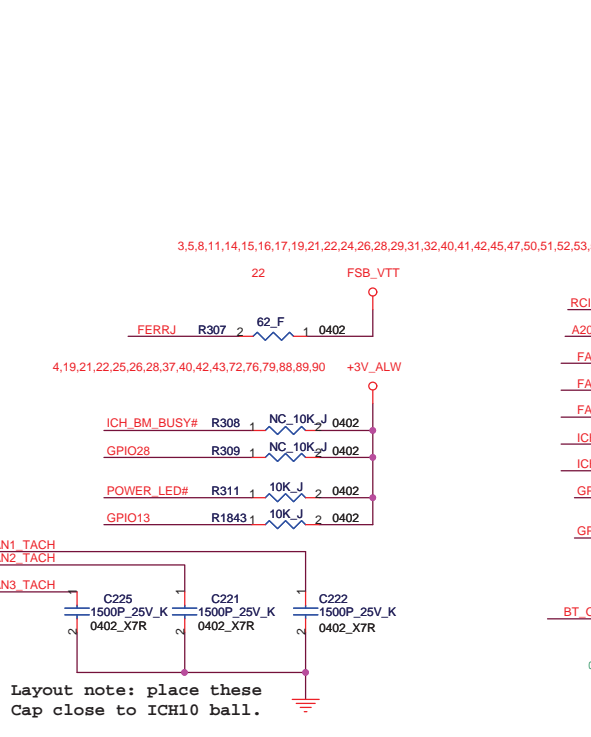
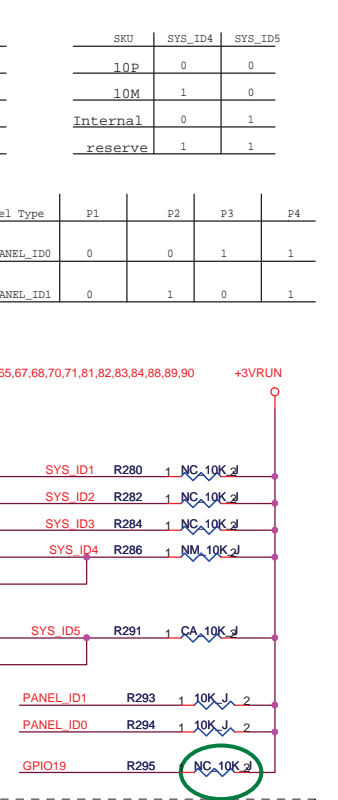
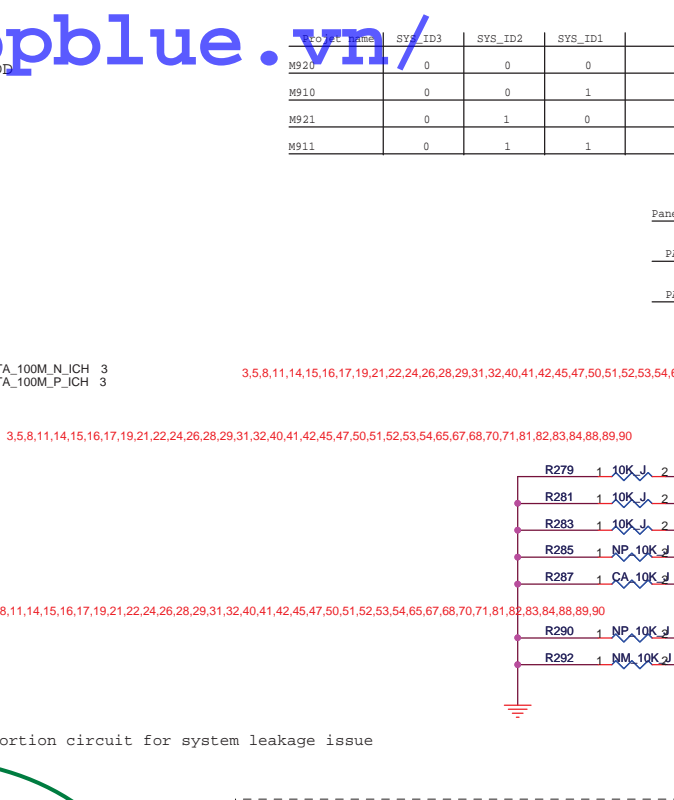
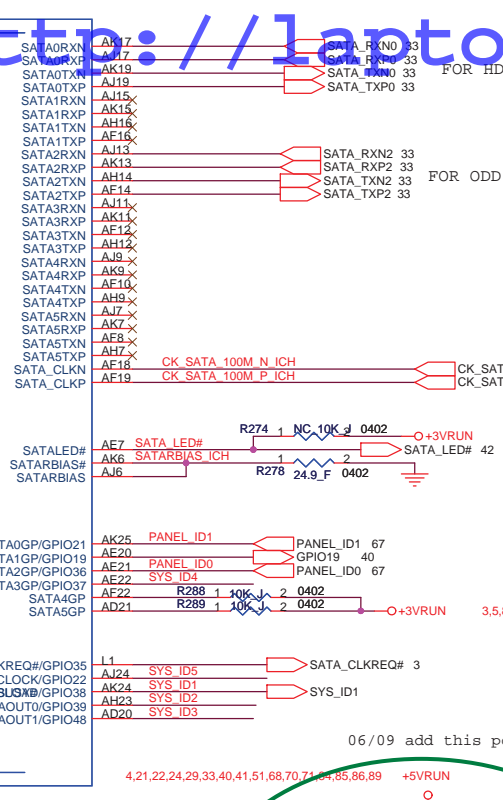
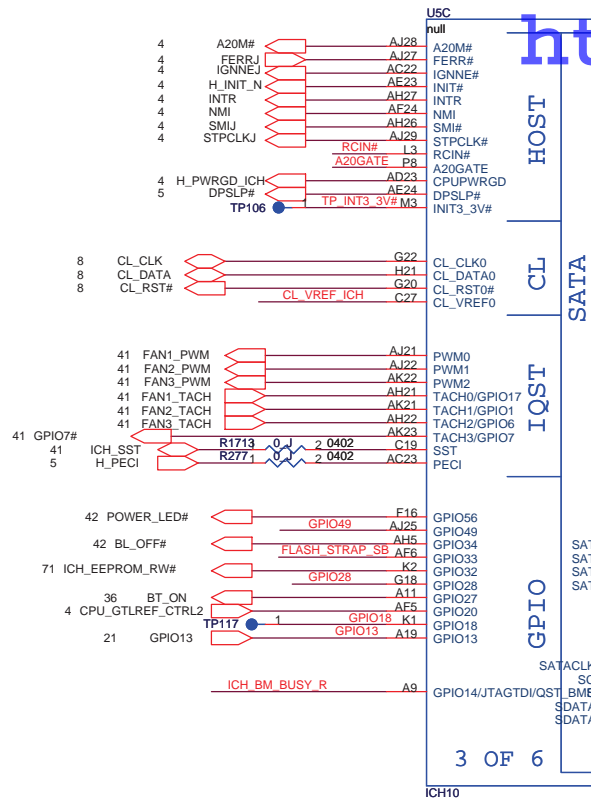


Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VRUN

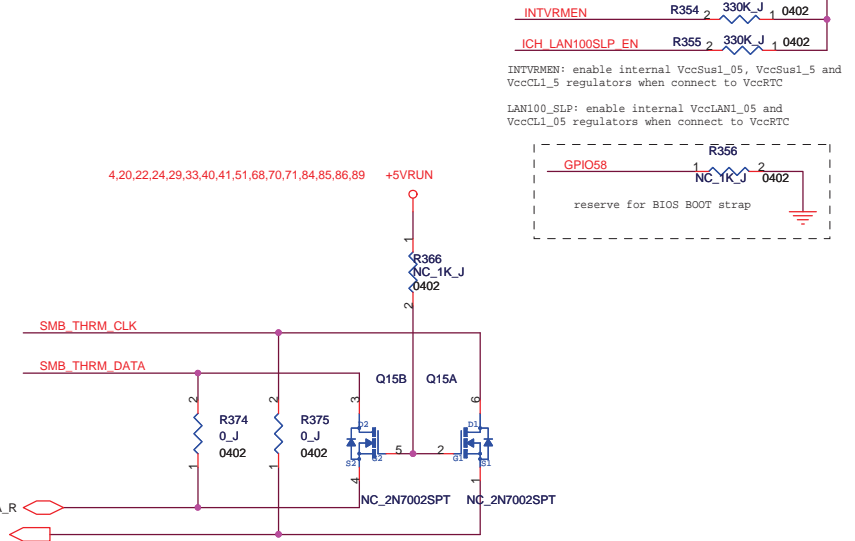
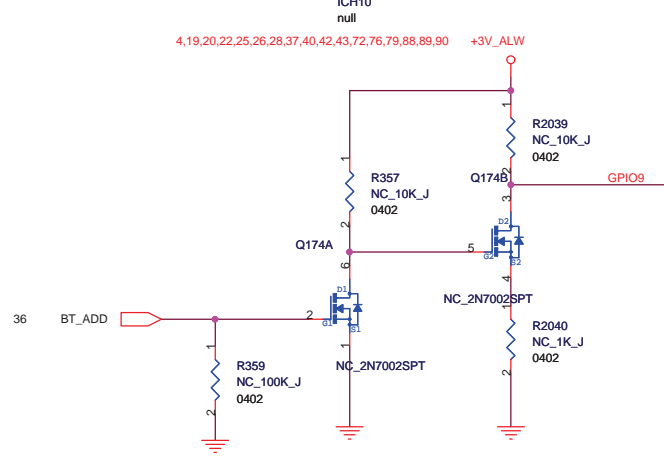
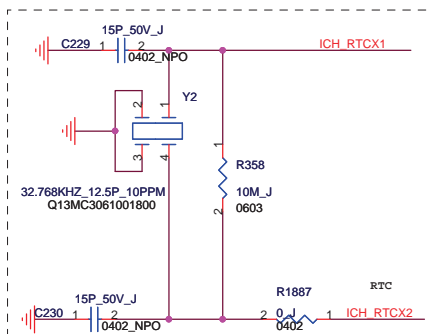
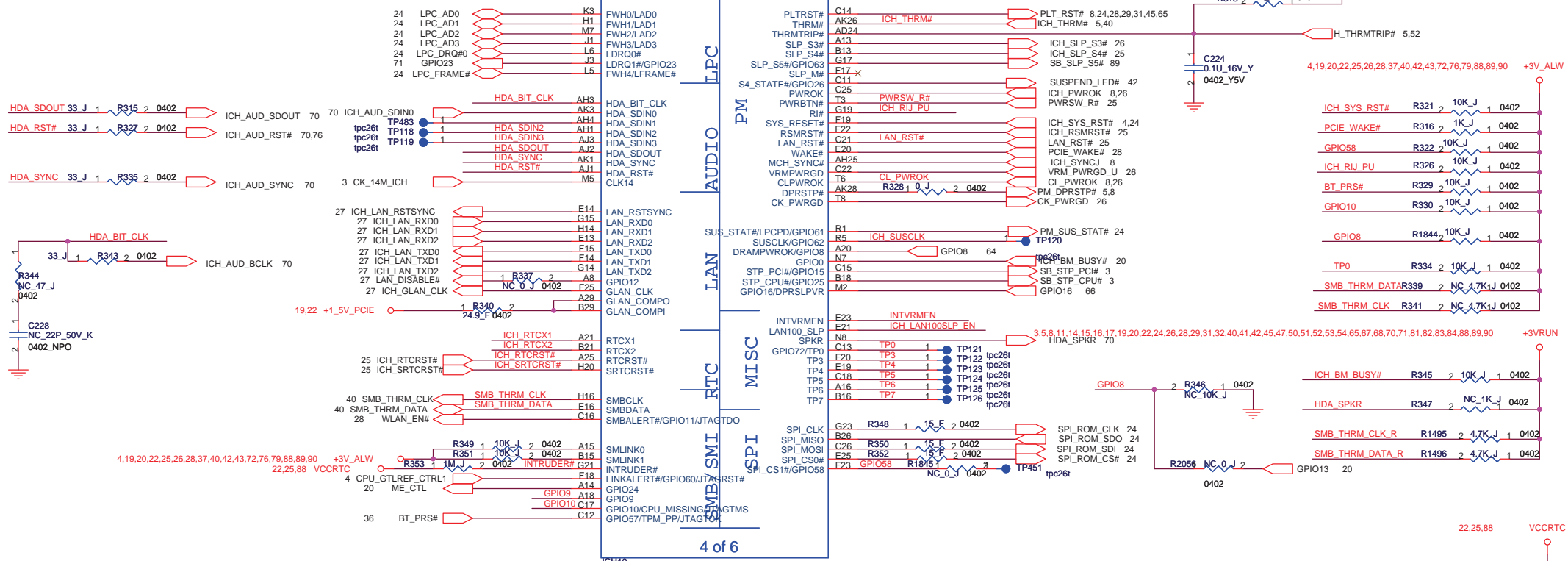


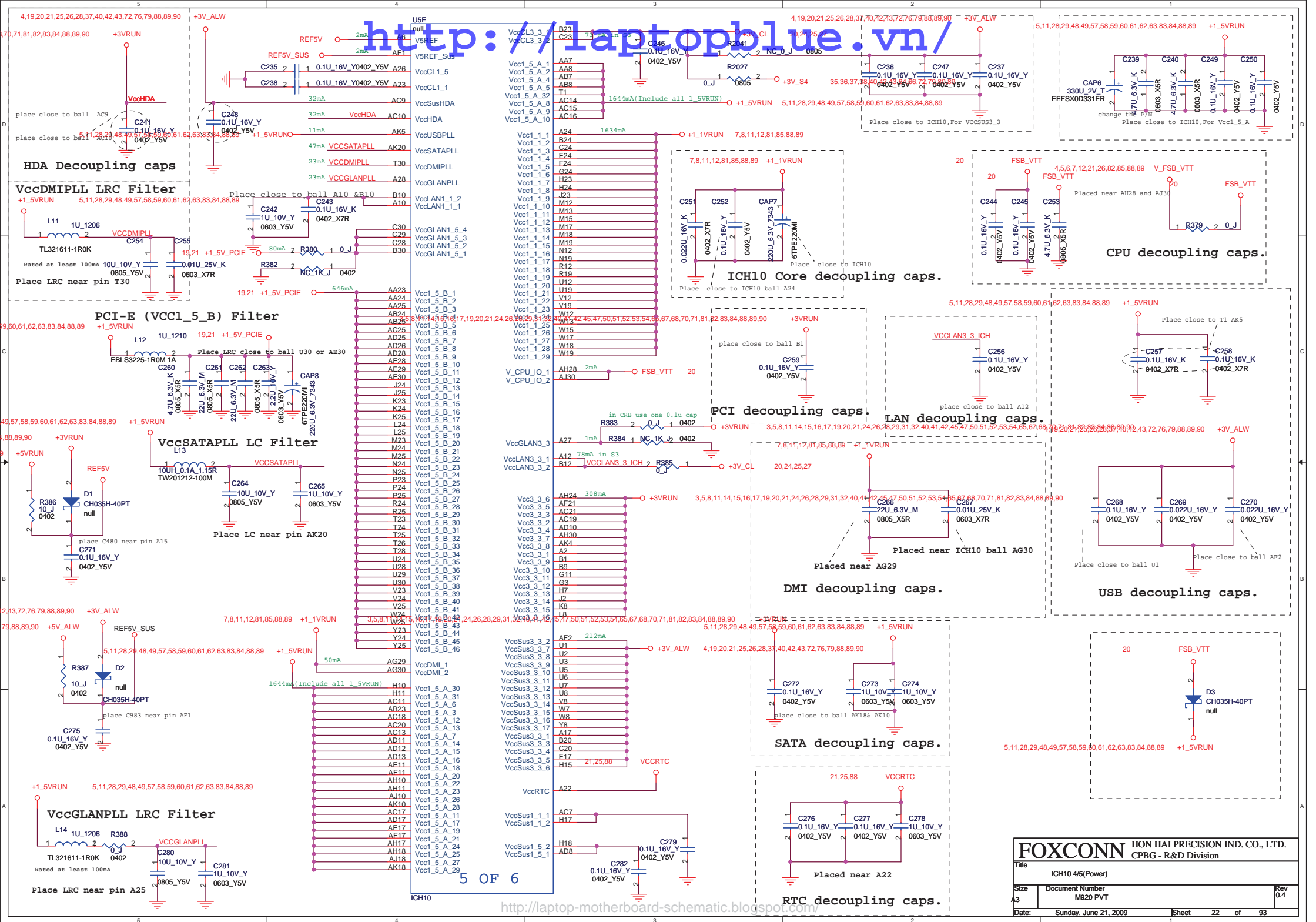


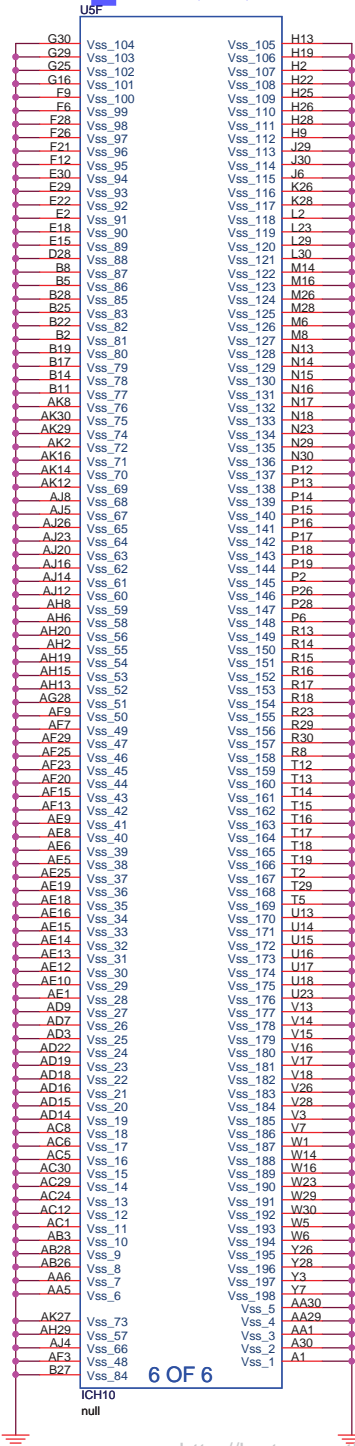


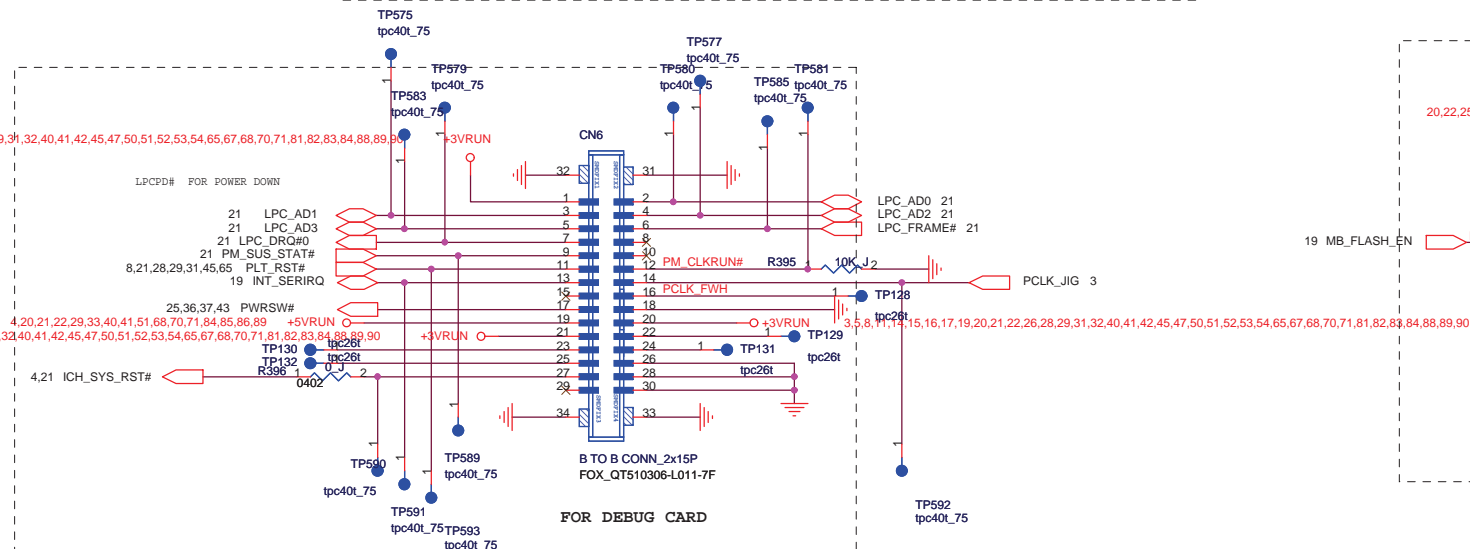
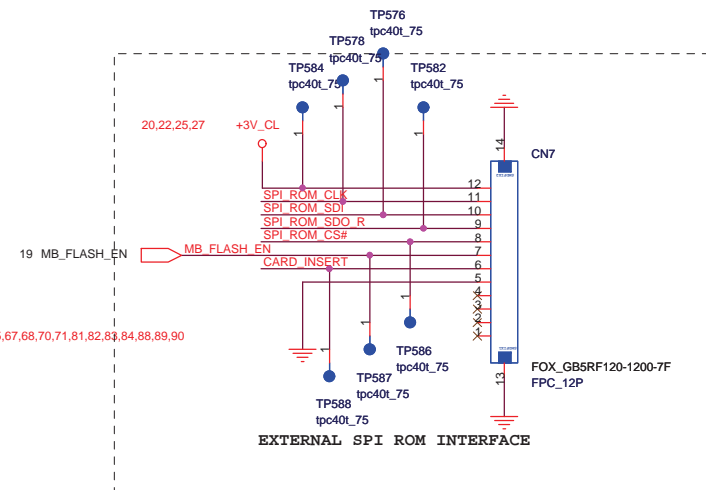
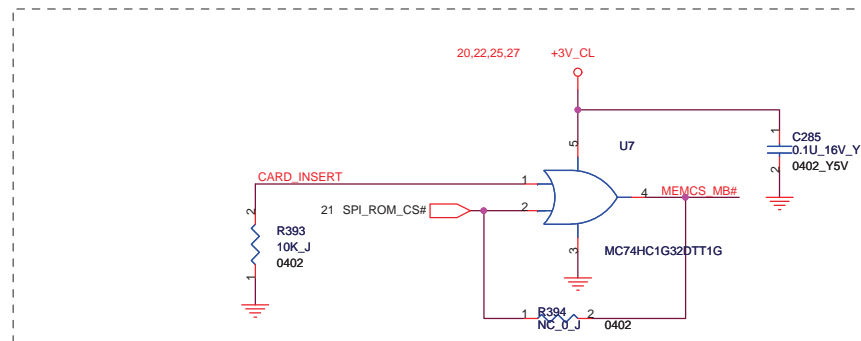




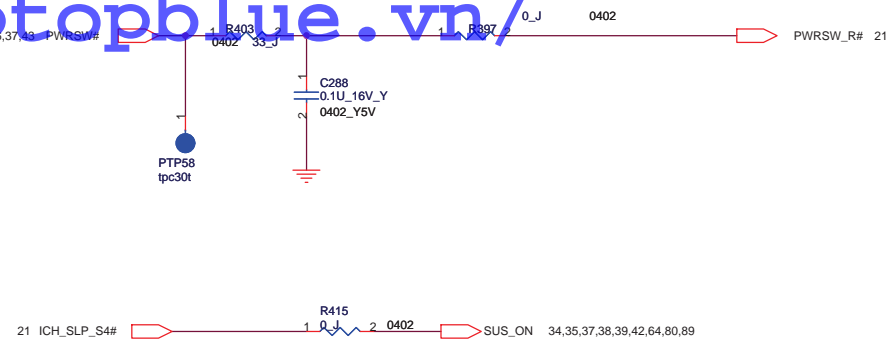
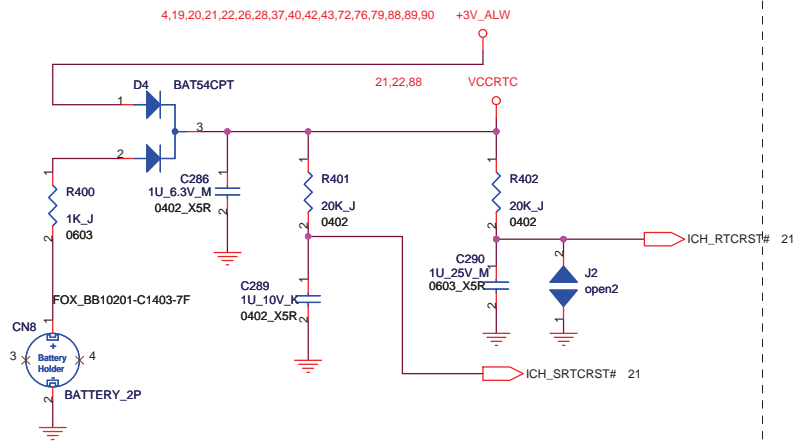






[illegible]

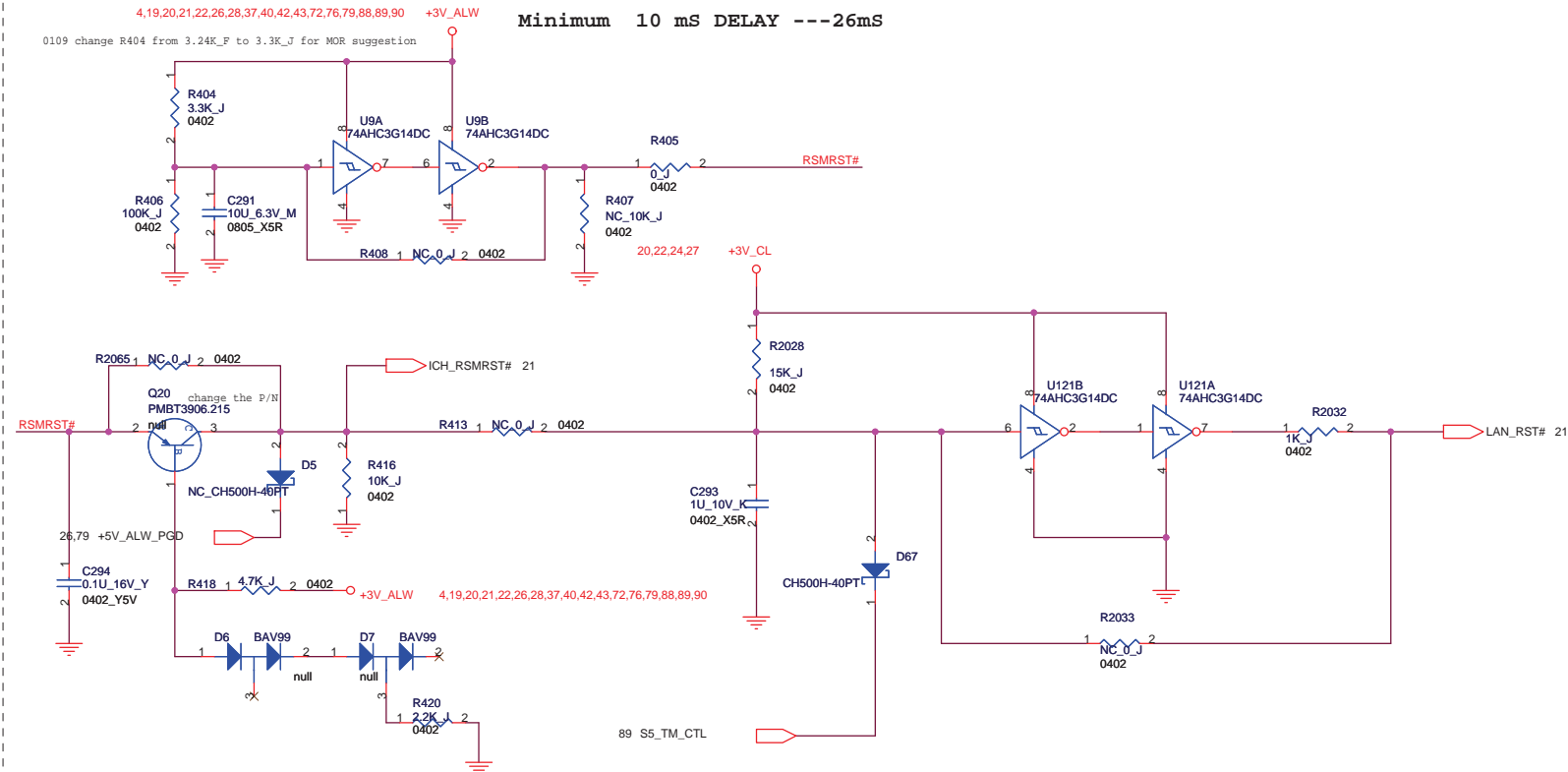
Delay time from VCCRTC high to RTCRST# inactive 18-25ms



Delay time from +3v\_alw high to RSMRST# inactive

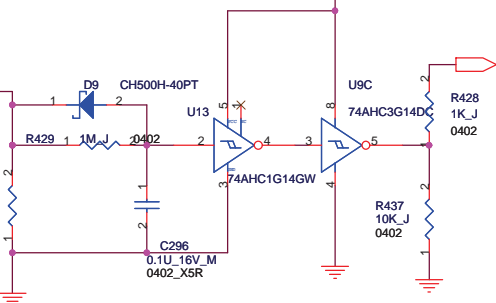
Minimum 10 ms DELAY ---26ms

0109 change R404 from 3.24K\_F to 3.3K\_J for MOR suggestion



ICH\_SLP\_S3# inactive to RUN\_ON active(3/5VRUN ) delay  
Minimum 20ms -- 80ms

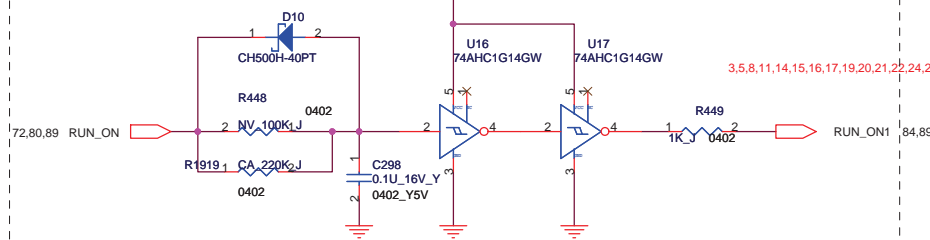
4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V\_ALW



NV\_VDD POWER LOGIC

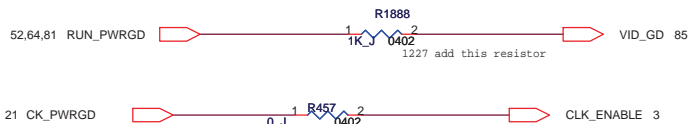
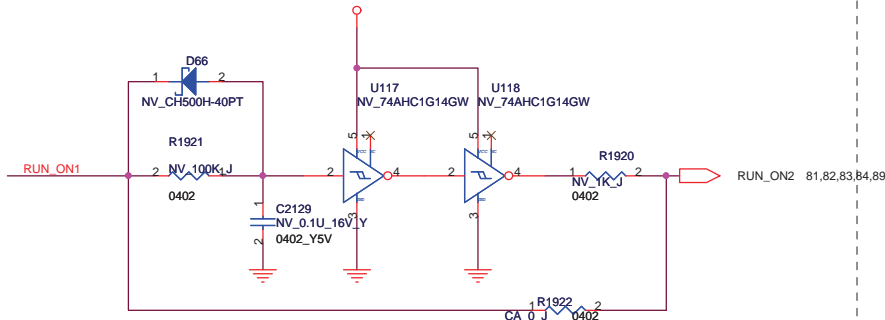
Minimum 5ms DELAY -- 10ms

4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V\_ALW



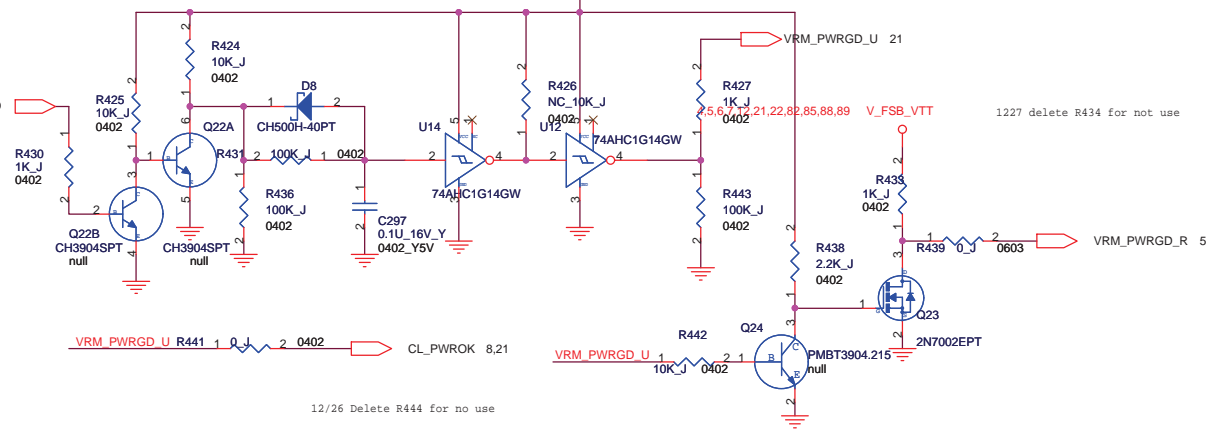
+1\_5VRUN/+1\_1VRUN/V\_FSB\_VTT/PEX\_VDD  
Minimum 5ms DELAY -- 10ms

4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V\_ALW



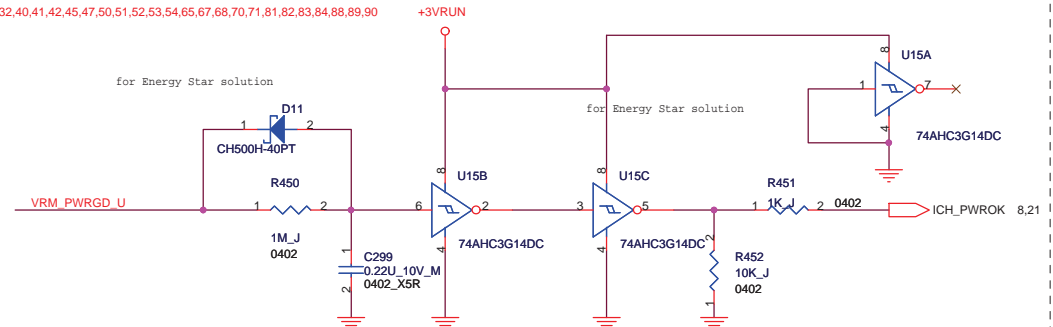
VRM\_PWRGD Delay time and level shift

for Energy Star solution



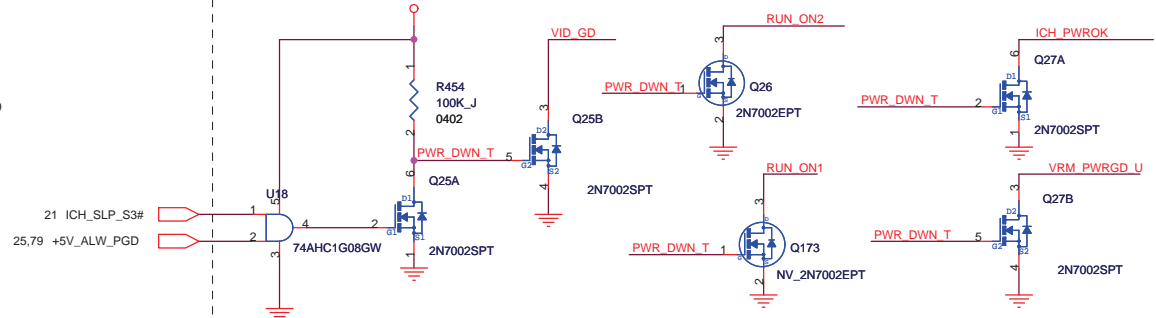
ICH\_VRM\_PWRGD DELAY 99ms to ICH\_PWROK Minimum 99ms DELAY

for Energy Star solution



POWER DOWN TIMING

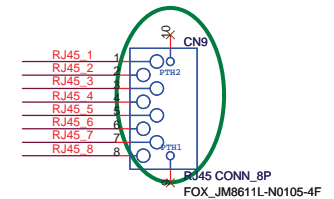
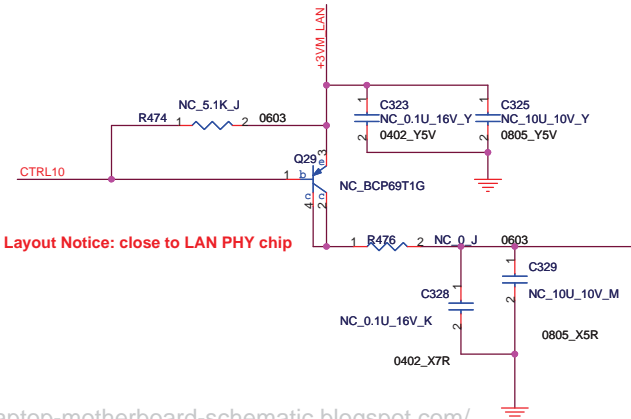
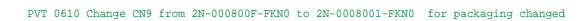
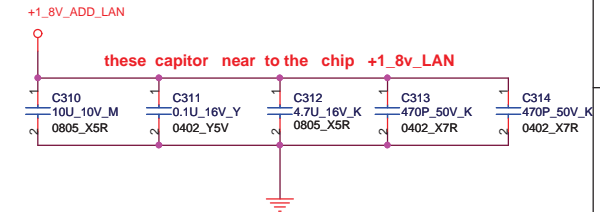
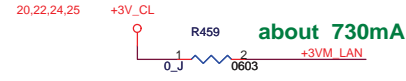
4,19,20,21,22,25,28,37,40,42,43,72,76,79,88,89,90 +3V\_ALW



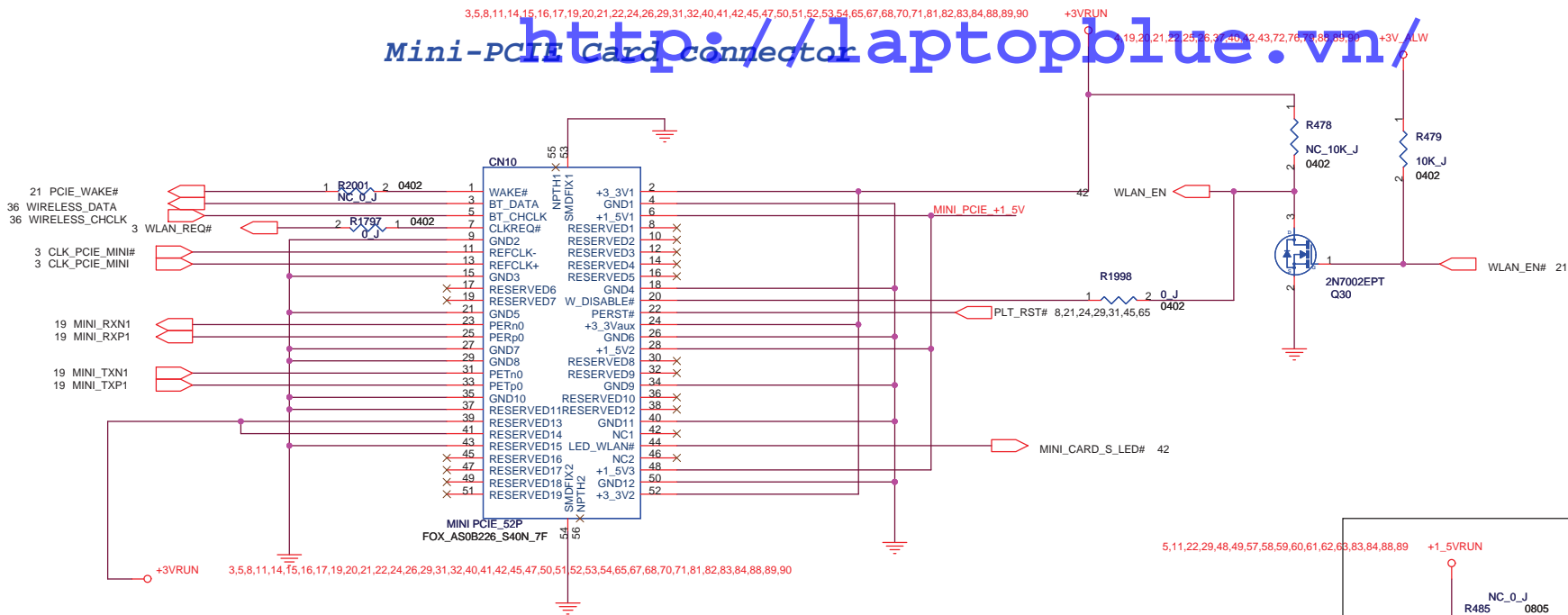
FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	Power Sequence 2/2		
Size	Document Number	Rev	
A3	M920 PVT	0.4	
Date:	Sunday, June 21, 2009	Sheet	26 of 93



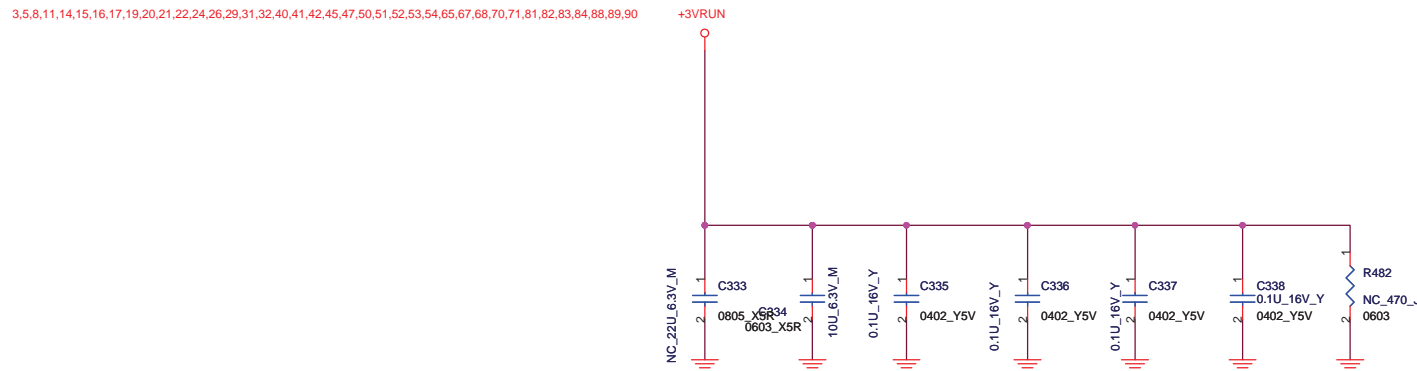
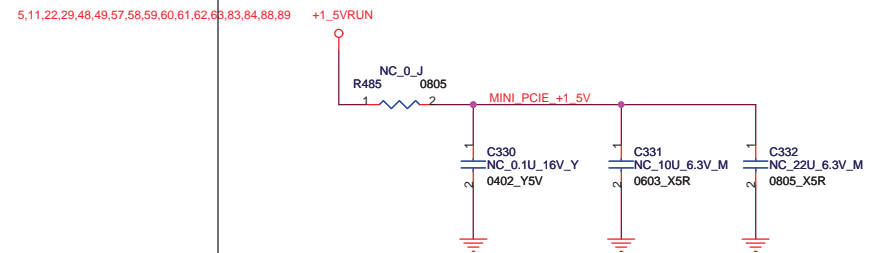
http://laptopblue.vn/



<http://laptop-motherboard-schematic.blogspot.com/>



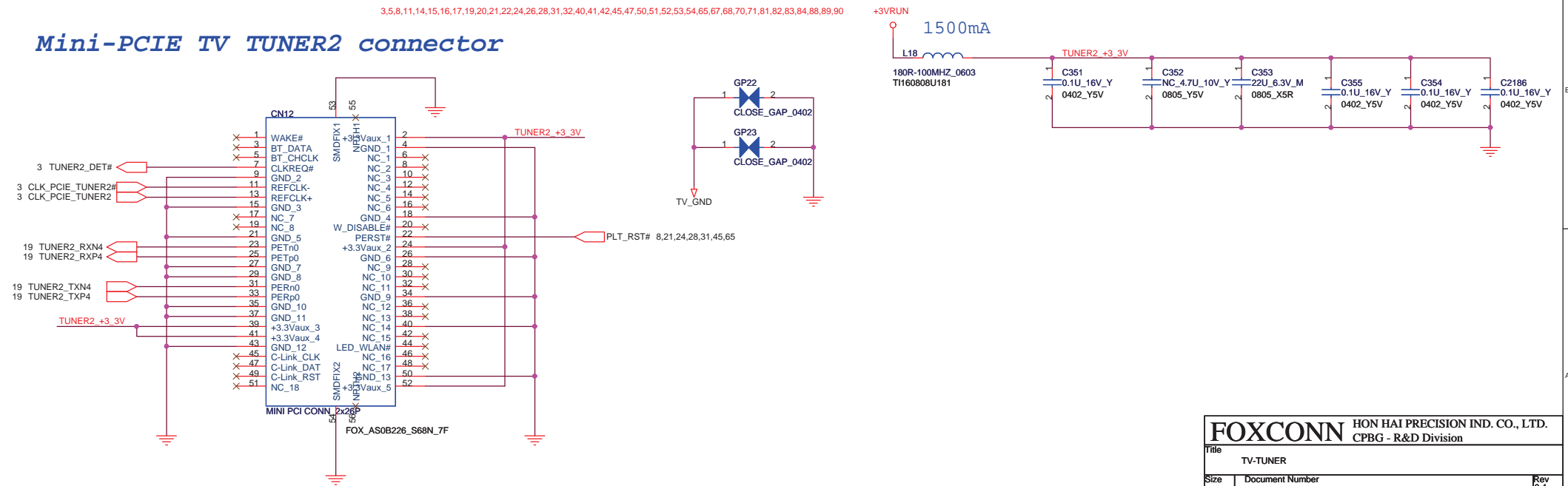
PCIe 3.3V spec.(Normal 750mA)(MAX 1100mA)



Mini-PCIE TV TUNER1 connector  
//laptopblue.vn/ 2500mA



## Mini-PCIE TV TUNER2 connector



<b>FOXCONN</b>		<b>HON HAI PRECISION IND. CO., LTD.</b>	
		<b>CPBG - R&amp;D Division</b>	
Title <b>TV-TUNER</b>			
Size A3	Document Number <b>M920 PVT</b>		Rev 0.4
Date: <b>Sunday, June 21, 2009</b>		Sheet <b>29 of 93</b>	

54321

Blank

http://laptopblue.vn/

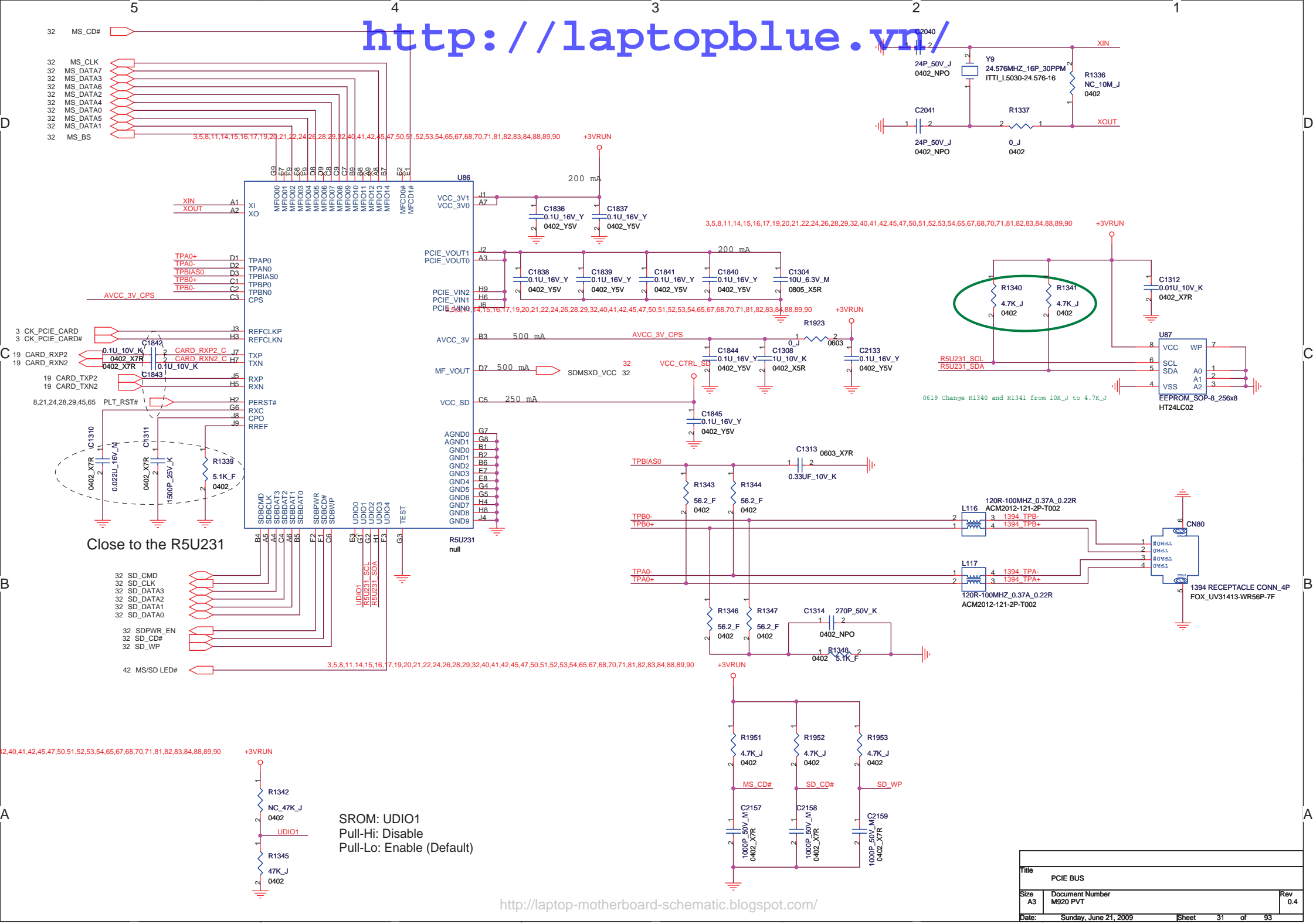
D

DVT  
04/14 Delete all AV\_IN function for MOR request  
(Delete CN14,C368,C2131,C2132,C2130,C2039,TP486,TP485,TP484,TP487,TP489,TP491,TP487,TP490 and TP488)

A

FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title AV/IR DB CONN			
Size A3	Document Number M920 PVT		Rev 0.4
Date:	Sunday, June 21, 2009	Sheet	30 of 93

http://laptopblue.vn/

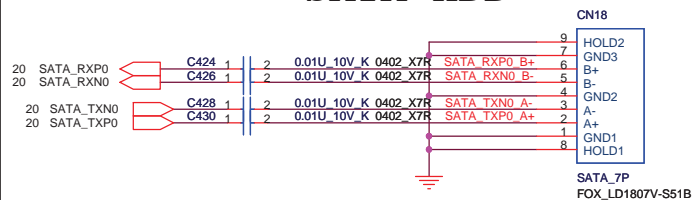


Title			
PCIE BUS			
Size A3	Document Number M920 PVT		Rev 0.4
Date:	Sunday, June 21, 2009	Sheet	31 of 93



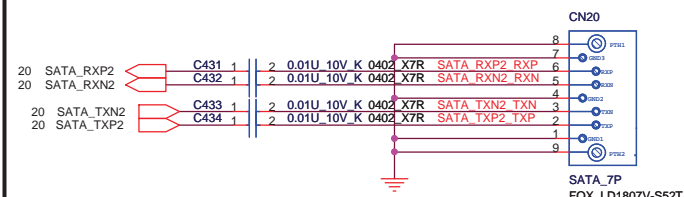


## SATA HDD



PLACE SHESE CAPS CLOSE TO CN18

## SATA ODD

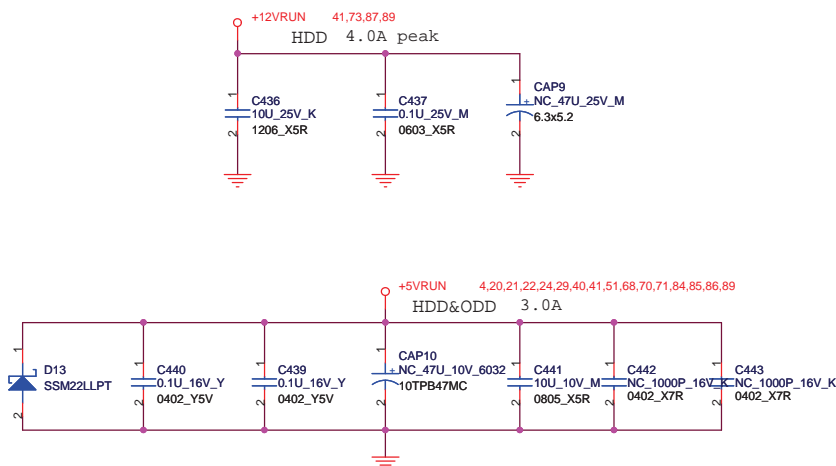
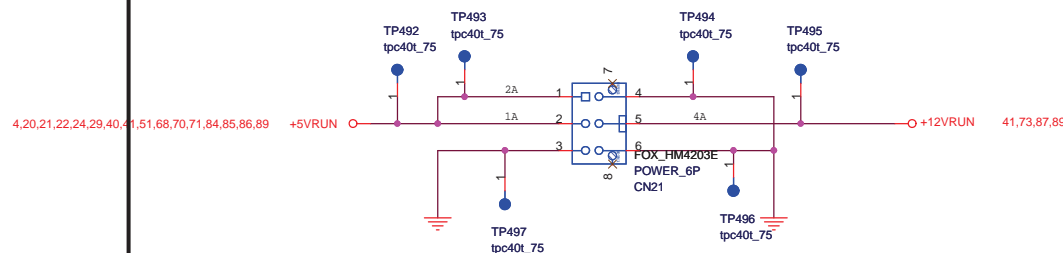


PLACE SHESE CAPS CLOSE TO CN20

## HDD&ODD POWER

5V: 3A (HDD 0.8A+ODD 2A)

12V: 4A peak, 4 seconds(HDD 4A)



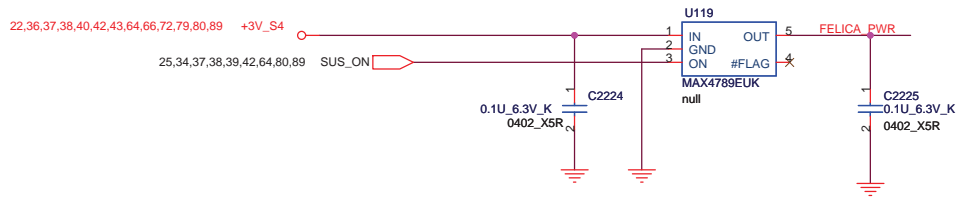
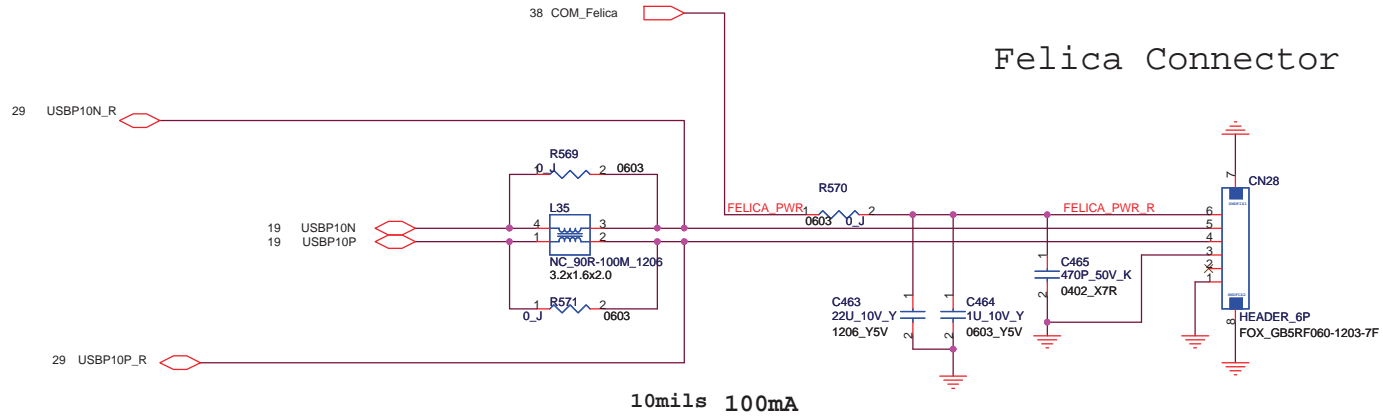
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

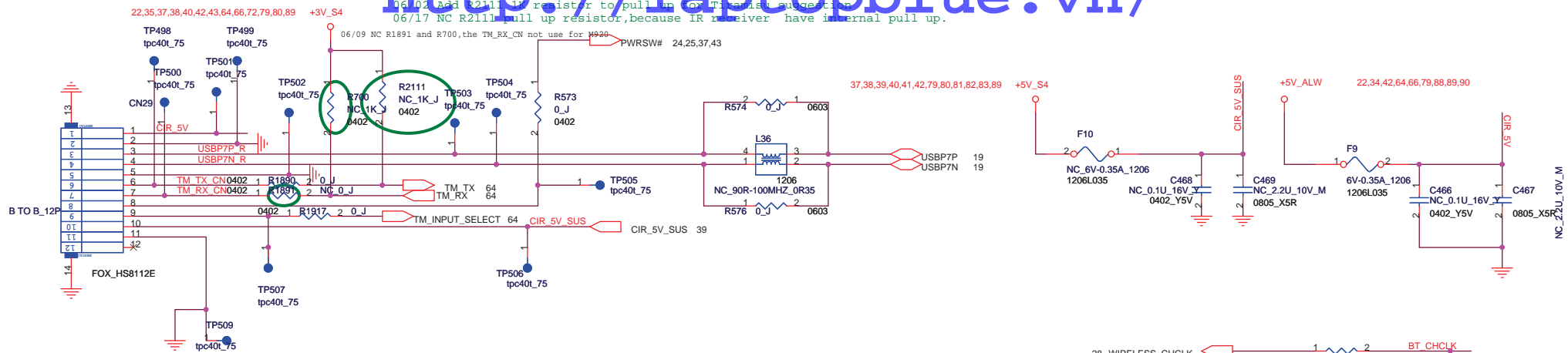
Title: SATA HDD/ODD

Size: Document Number M920 PVT

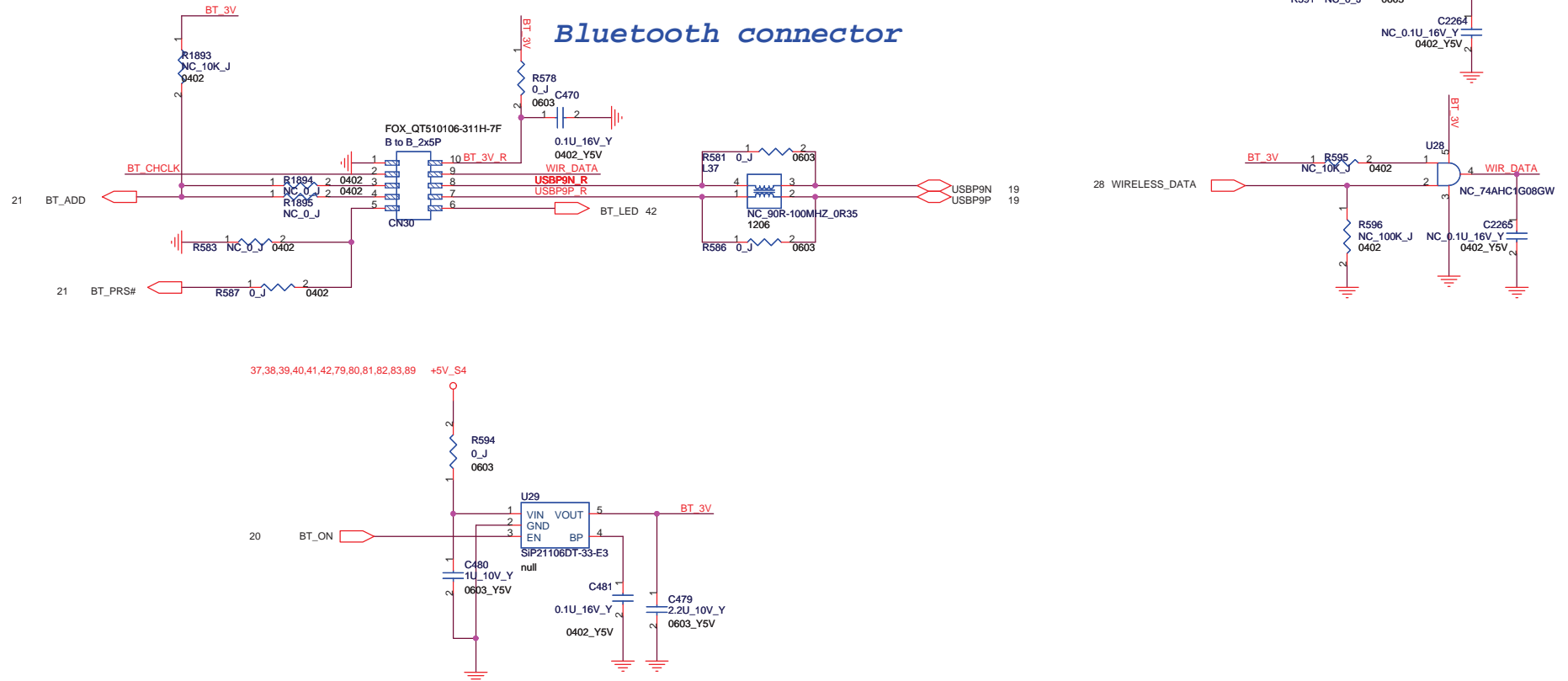
Date: Sunday, June 21, 2009 Sheet 33 of 93

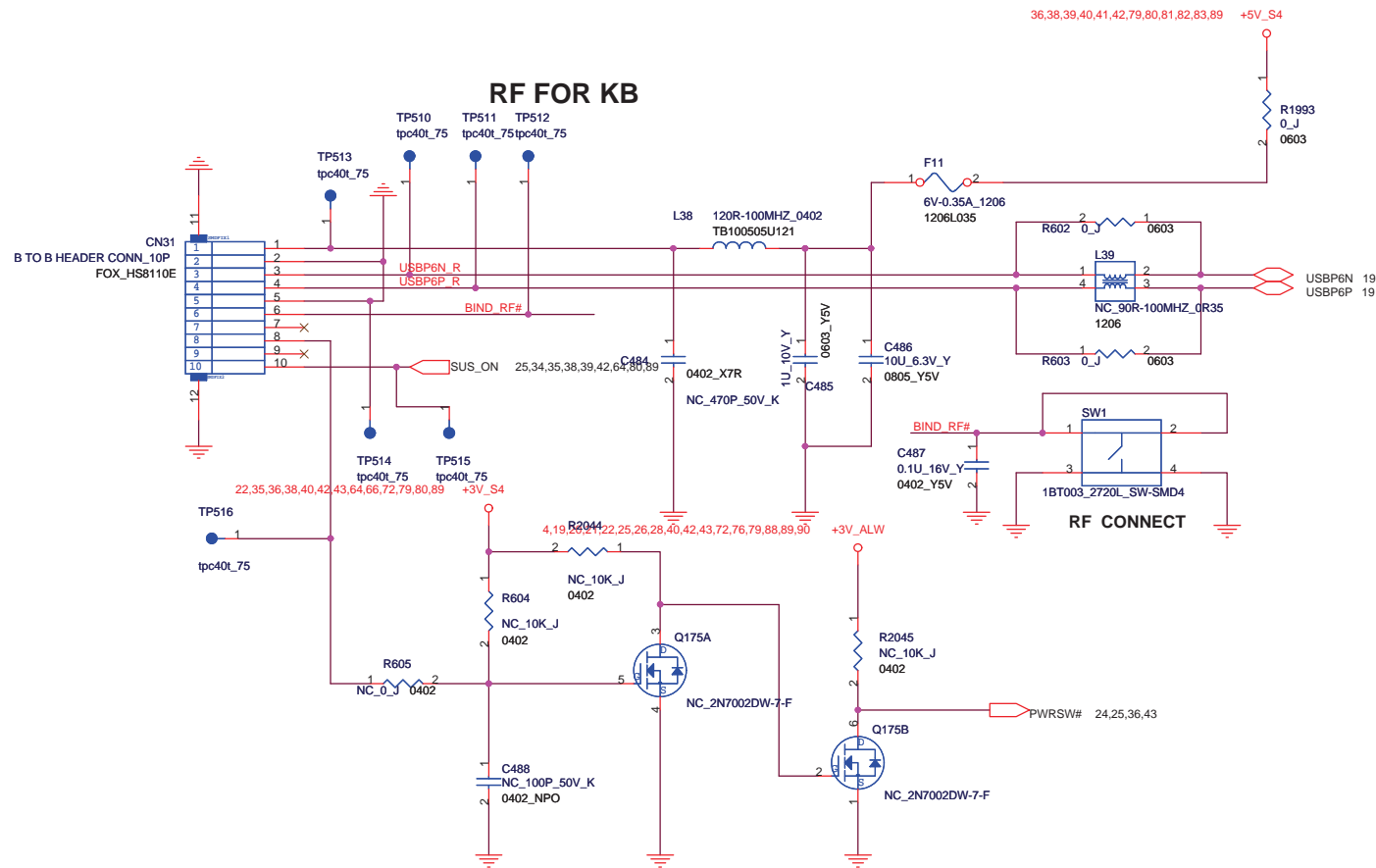




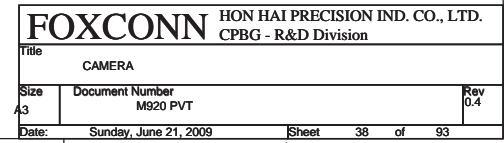


## Bluetooth connector



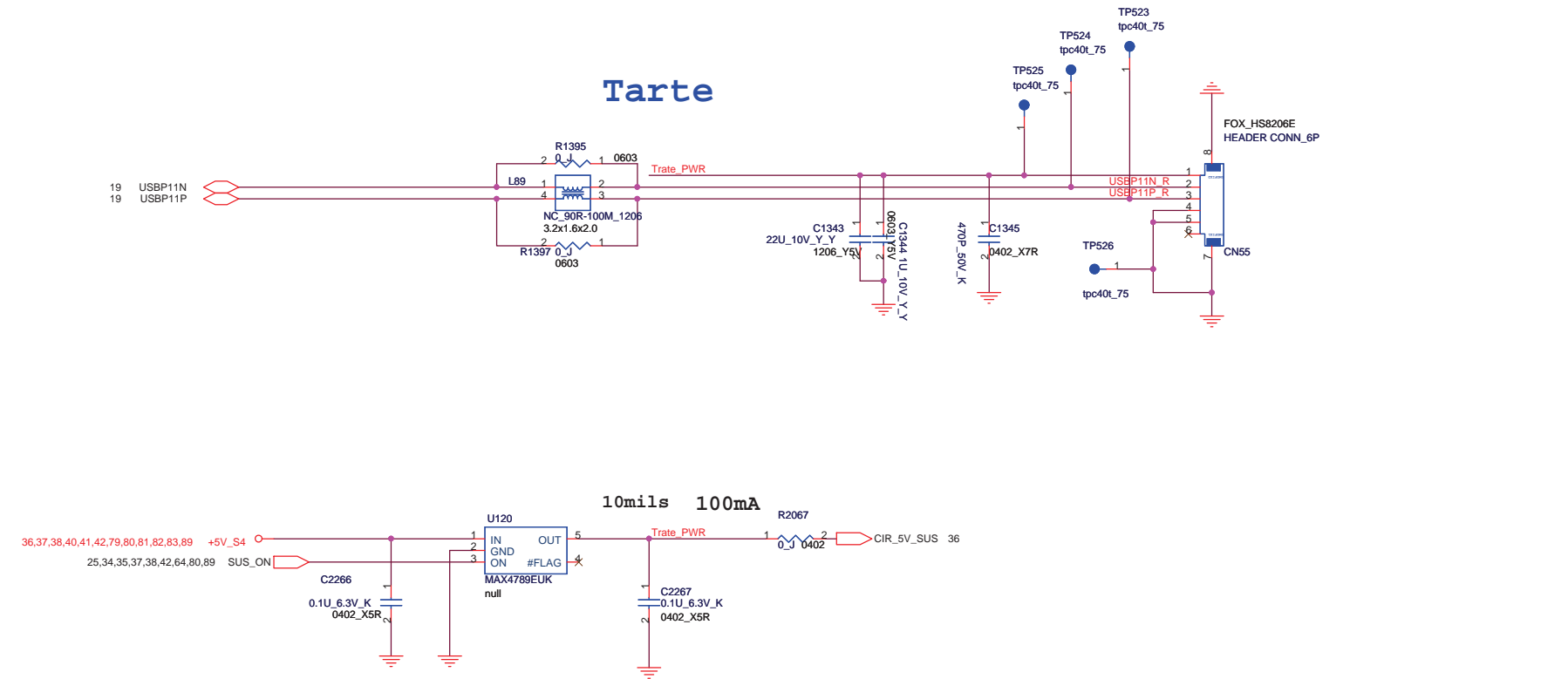


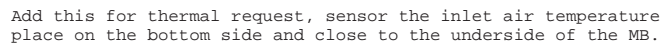
AX4789EUK NC\_0\_J 0603 CAMERA





5	4	3	2	1
---	---	---	---	---





**SPS FAN (Include 2 FANs)**

36,37,38,39,41,42,79,80,81,82,83,89 +5V\_S4

+12V\_FAN

TP531

tpc40t\_75

D27 CH035H-40PT

TP532 tpc40t\_75

R646 NC\_10K\_J 0402

D53 CH035H-40PT

FAN4 TACH\_HM

FAN4 PWM\_HM

CN38 HEADER\_4P FOX\_HS8104E

36,37,38,39,41,42,79,80,81,82,83,89 +5V\_S4

+5VRUN

R1798 NC\_10K\_J 0402

TM\_FAN\_CTL

Q157 2N7002EPT

C520 10U\_25V\_K 1206\_X5R

R1900

TP533 tpc40t\_75

36,37,38,39,41,42,79,80,81,82,83,89

GPIO19

R2050

0402

R1799 NC\_10K\_J 0402

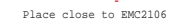
Q158 2N7002EPT

R1800 1M\_J 0402

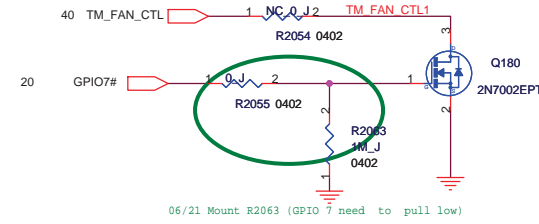
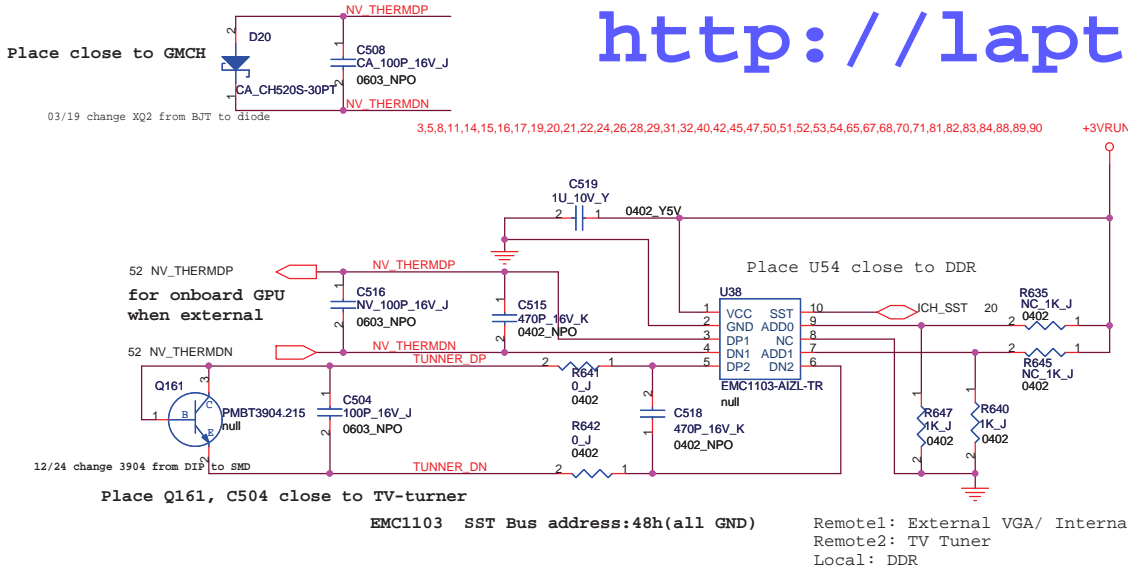
06/20 Mount R1800 (GPIO 19 need to pull low)

<http://laptop-mo>

Place close CN41

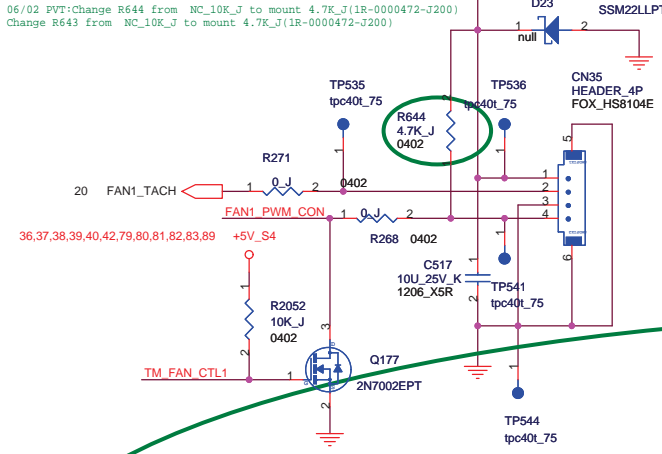


Date: Sunday, June 21, 2009 Sheet 40 of 93



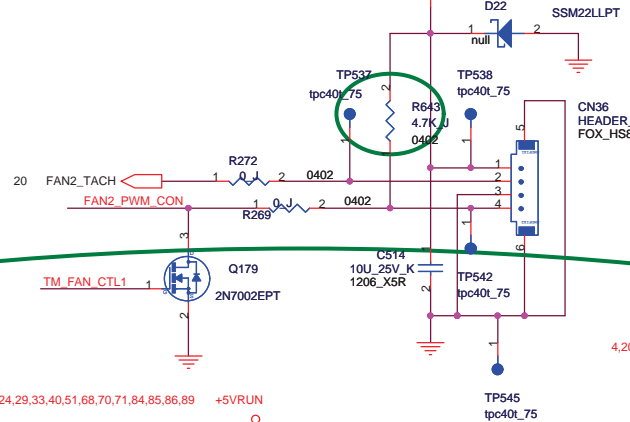
## CPU FAN1

4,20,21,22,24,29,33,40,51,68,70,71,84,85,86,89



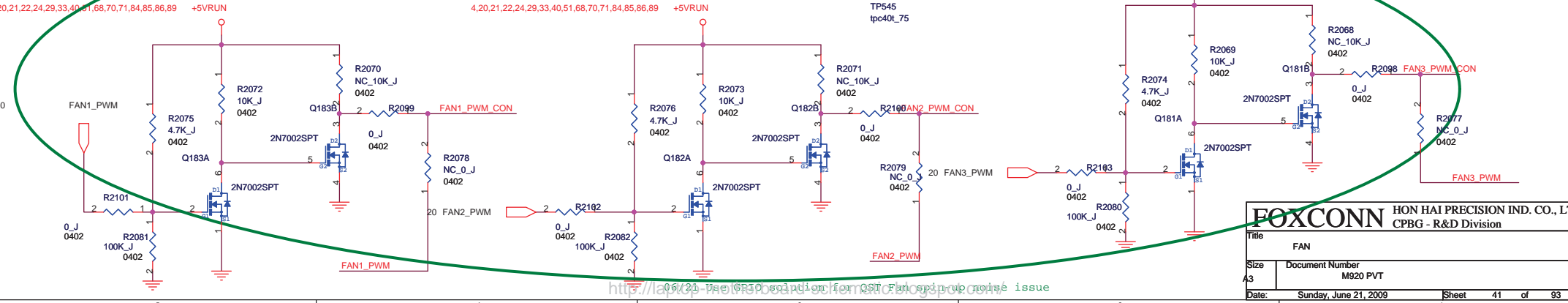
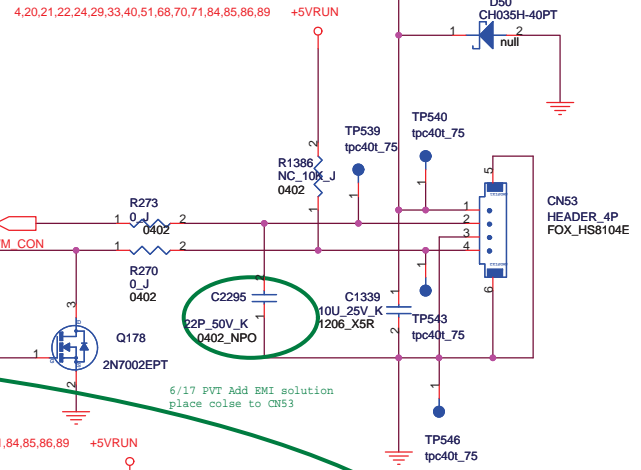
## CPU FAN2

4,20,21,22,24,29,33,40,51,68,70,71,84,85,86,89



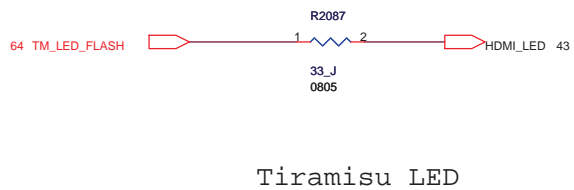
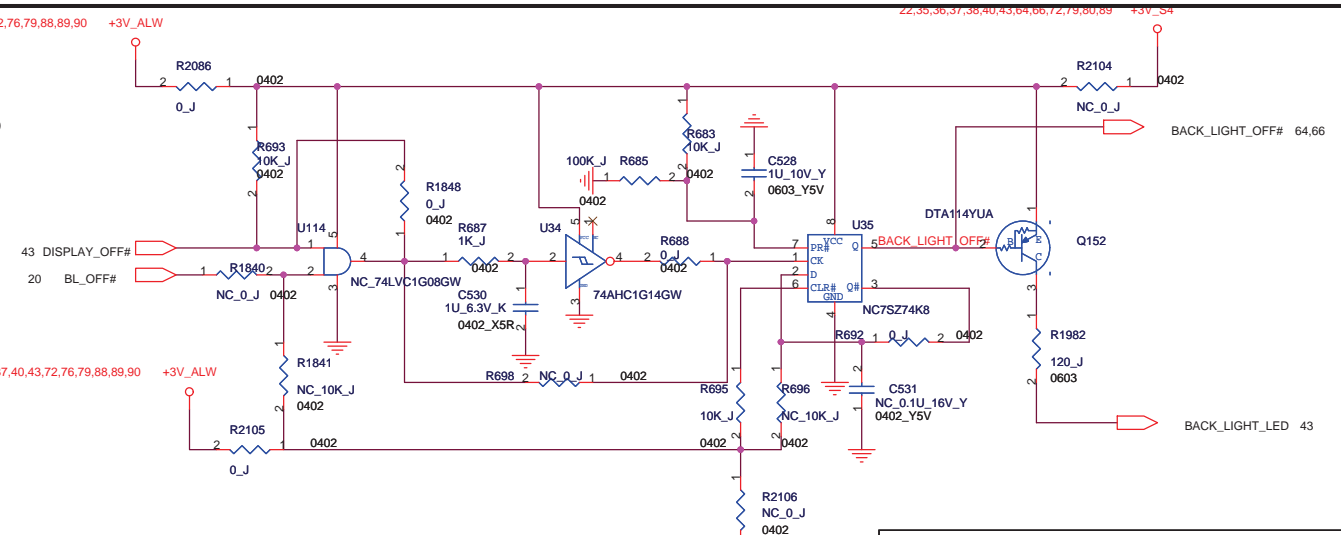
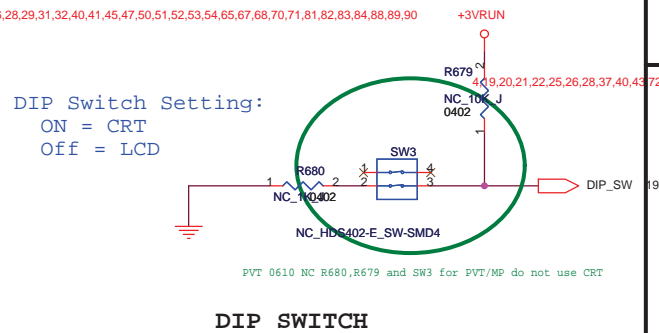
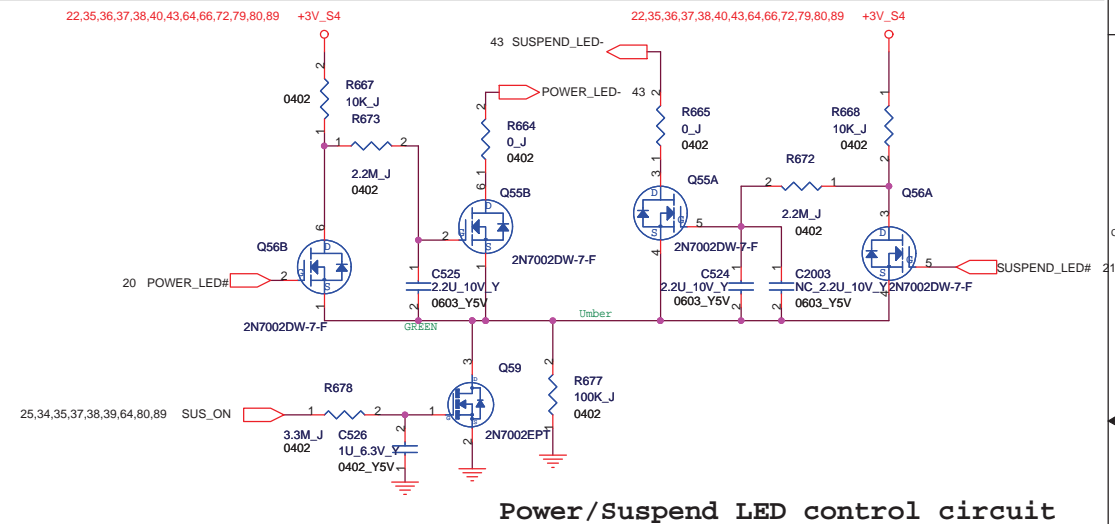
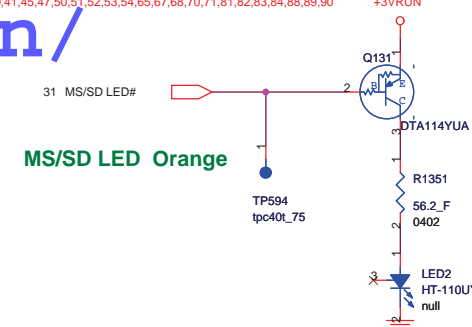
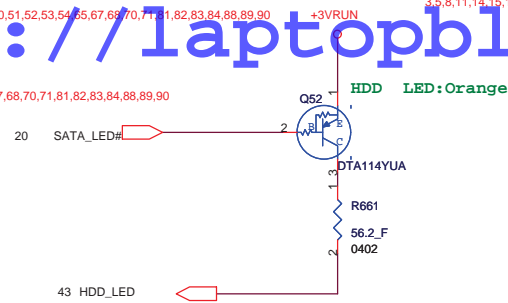
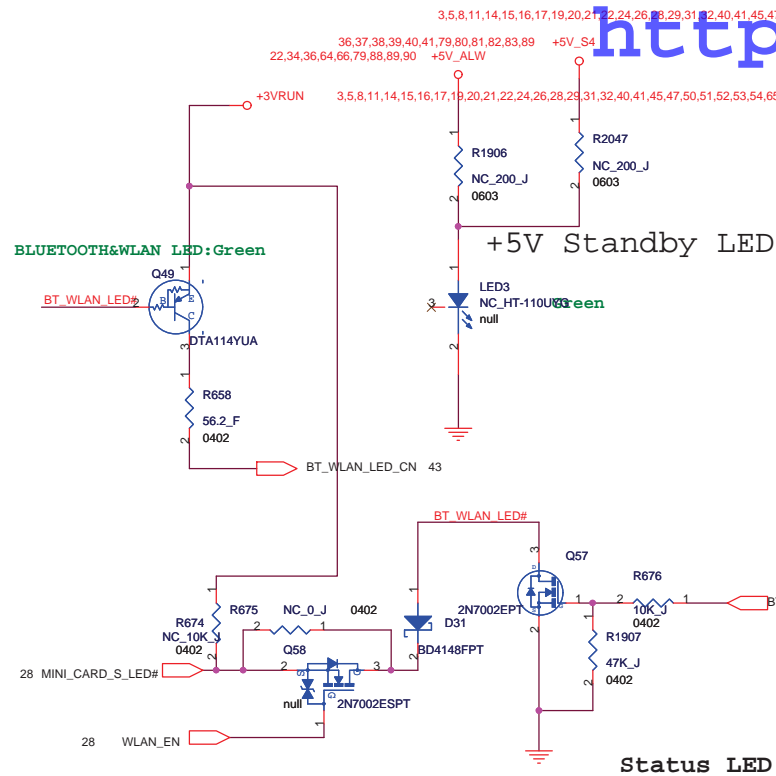
## CHASSIS FAN

0109 delete D65 for no use

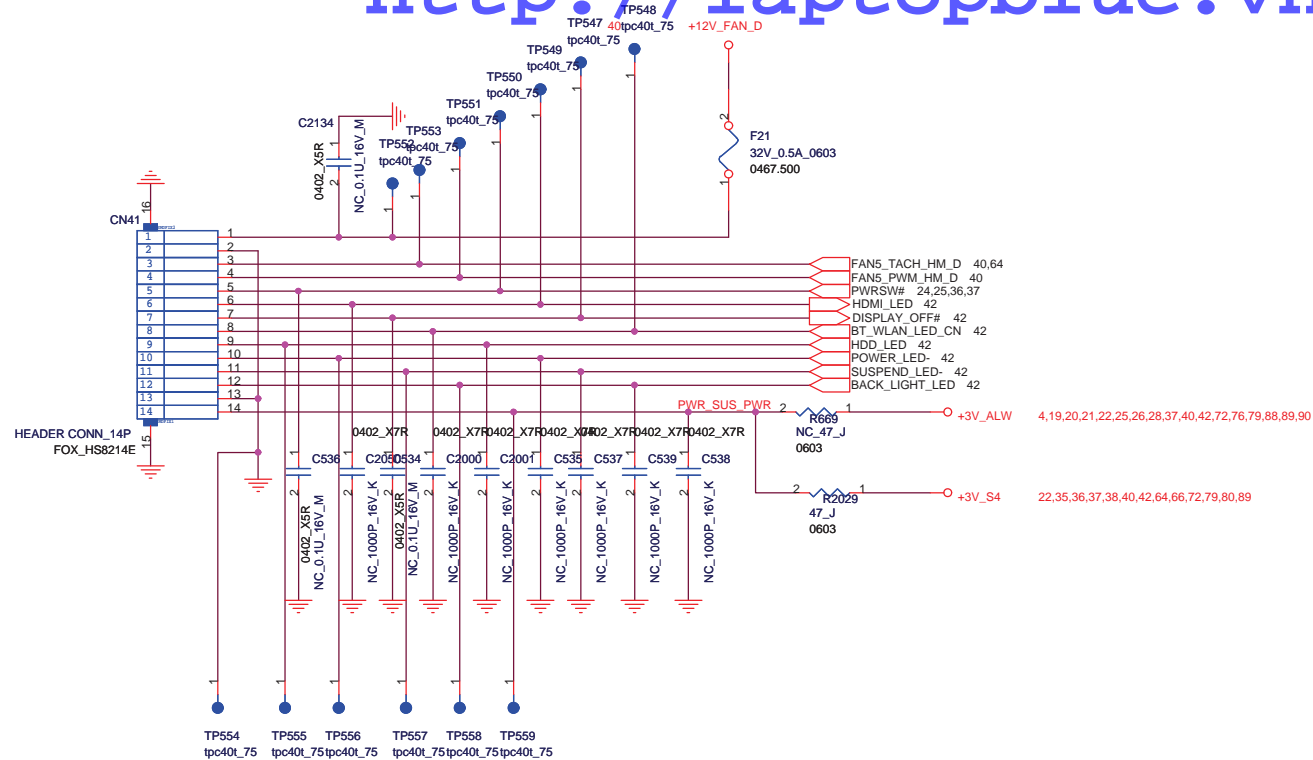


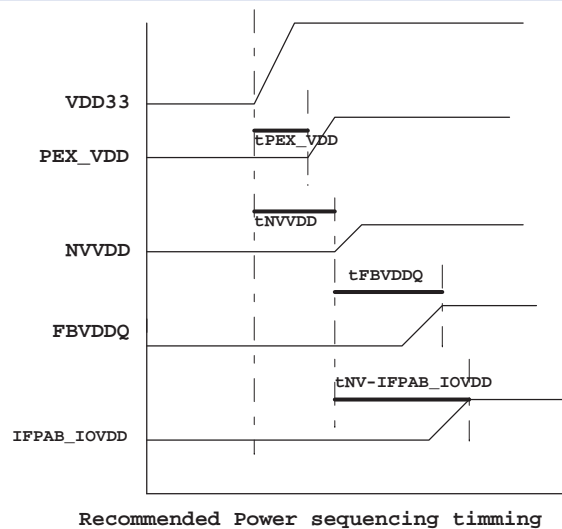
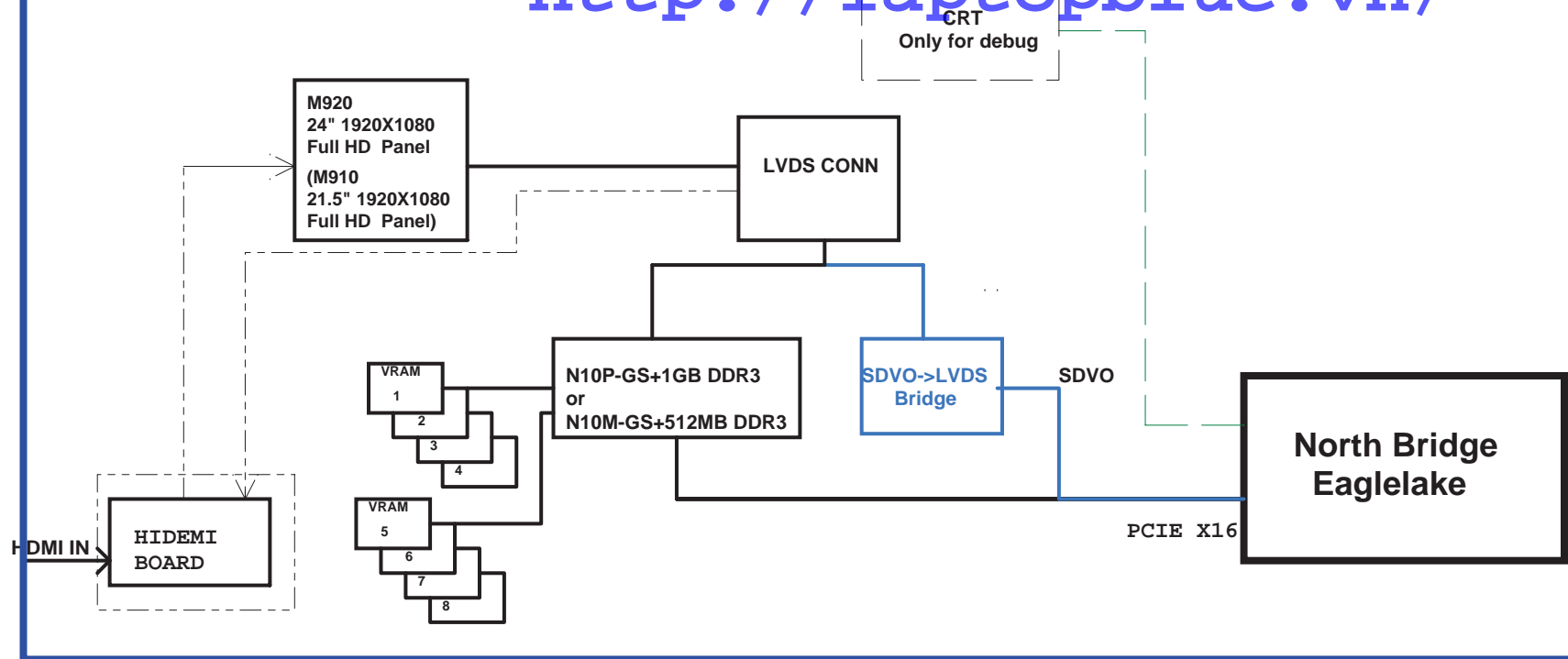
FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	FAN		
Size	Document Number	Rev	
A3	M920 PVT	0.4	
Date:	Sunday, June 21, 2009	Sheet	41 of 93

3,5,8,11,14,15,16,17,19,20,21,22,24,26,28,29,31,32,40,41,45,47,50,51,52,53,54,55,67,68,70,71,81,82,83,84,88,89,90  
36,37,38,39,40,41,79,80,81,82,83,89 +5V\_S4  
22,34,36,64,66,79,88,89,90 +5V\_ALW



Display off LED





note:  
VDD33 =+3VRUN  
NVVDD=NV\_VDD  
FBVDDQ=FBVDD=+1\_5VRUN

tNVVDD>=0  
tFBVDDQ>=0  
tNV-IFPAB\_IOVDD>0  
tPEX\_VDD>0 NV suggestion

The ramp time for any rail must be more than 40 us

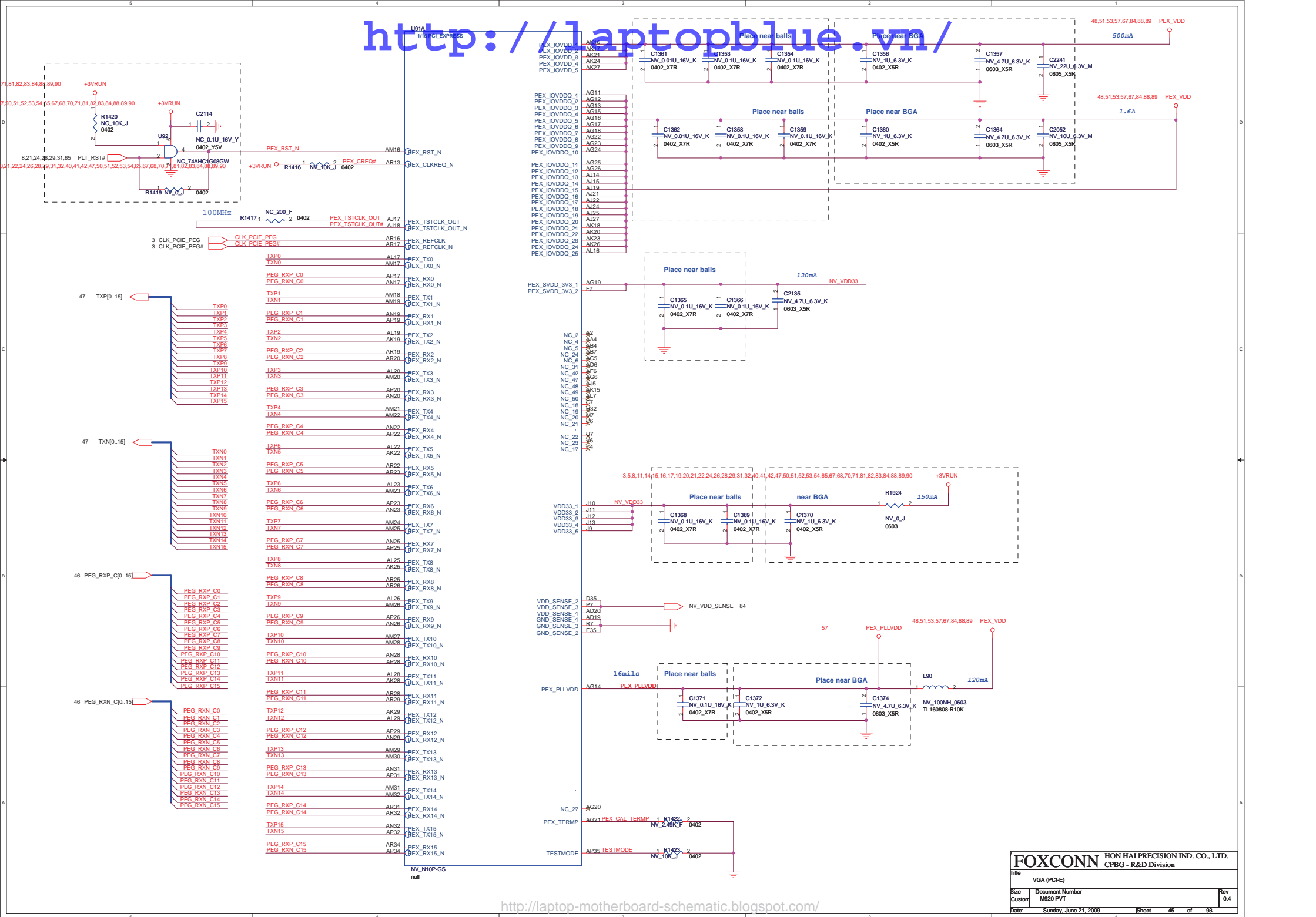
At any time  
NVVDD<=VDD33+0.5V  
FBVDDQ<=VDD33+0.5V

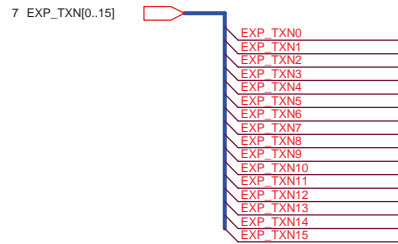
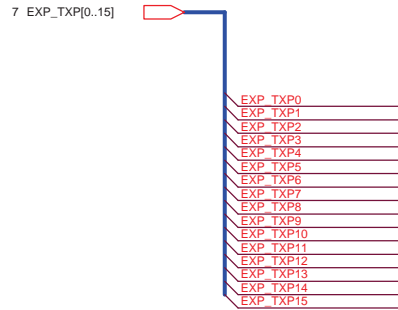
#### NOTE:

##### Head value table

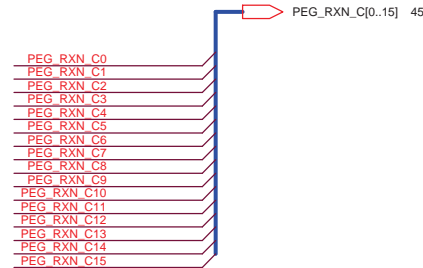
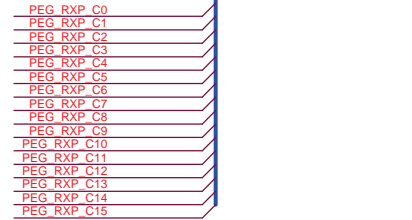
M920 H	NV_,NP_,
M920 M	NV_,
M920 L	CA_,
M920 MST	NV_,NP_, TM_,







EXP_TXP0	C1420	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C0
EXP_TXN0	C1421	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C0
EXP_TXP1	C1422	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C1
EXP_TXN1	C1423	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C1
EXP_TXP2	C1424	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C2
EXP_TXN2	C1425	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C2
EXP_TXP3	C1426	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C3
EXP_TXN3	C1427	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C3
EXP_TXP4	C1428	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C4
EXP_TXN4	C1429	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C4
EXP_TXP5	C1430	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C5
EXP_TXN5	C1431	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C5
EXP_TXP6	C1432	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C6
EXP_TXN6	C1433	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C6
EXP_TXP7	C1434	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C7
EXP_TXN7	C1435	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C7
EXP_TXP8	C1436	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C8
EXP_TXN8	C1437	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C8
EXP_TXP9	C1438	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C9
EXP_TXN9	C1439	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C9
EXP_TXP10	C1440	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C10
EXP_TXN10	C1441	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C10
EXP_TXP11	C1442	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C11
EXP_TXN11	C1443	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C11
EXP_TXP12	C1444	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C12
EXP_TXN12	C1445	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C12
EXP_TXP13	C1446	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C13
EXP_TXN13	C1447	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C13
EXP_TXP14	C1448	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C14
EXP_TXN14	C1449	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C14
EXP_TXP15	C1450	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXP_C15
EXP_TXN15	C1451	0402_X7R	2	1	NV_0.1U_16V_K	PEG_RXN_C15

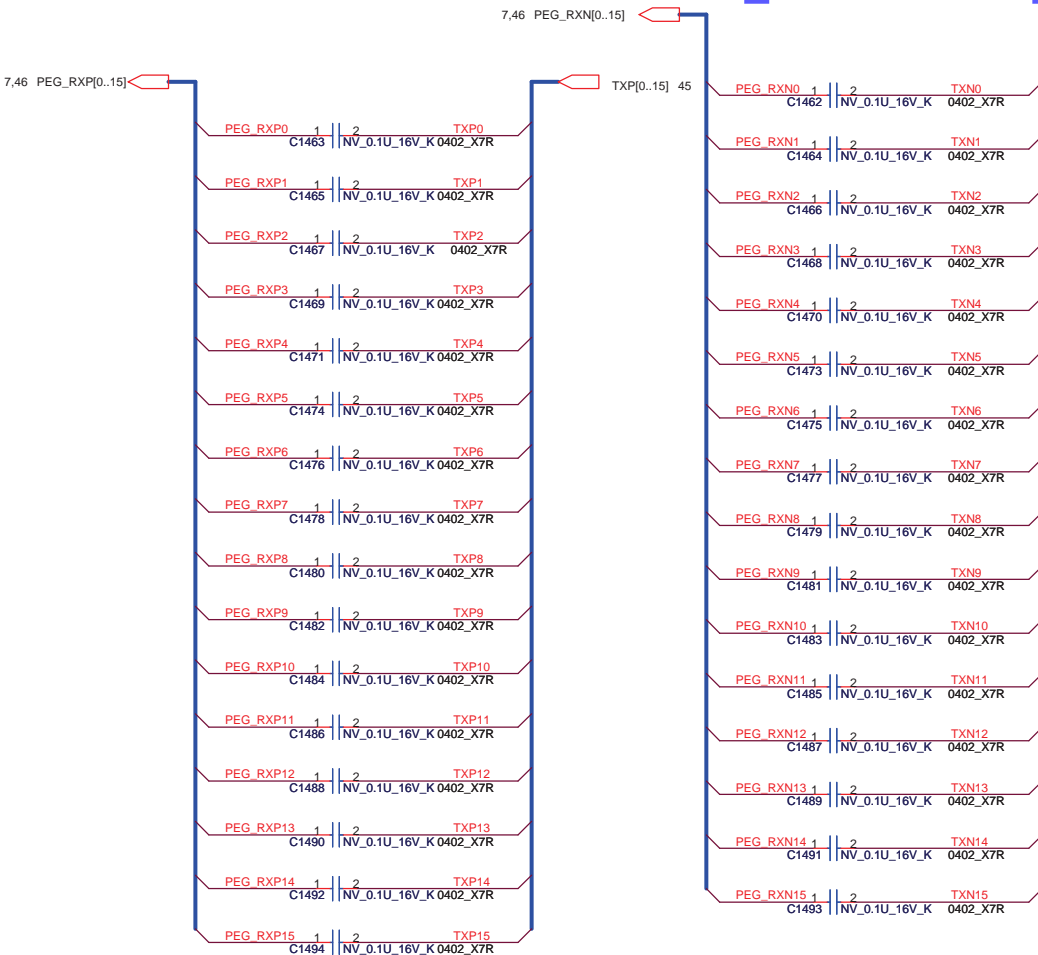


close to NB

EXP_TXP0	0402_X7R	2	1	CA_0.1U_16V_K	C1452	SDVOB_RED+	SDVOB_RED+	65
EXP_TXN0	0402_X7R	2	1	CA_0.1U_16V_K	C1453	SDVOB_RED-	SDVOB_RED-	65
EXP_TXP1	0402_X7R	2	1	CA_0.1U_16V_K	C1454	SDVOB_GREEN+	SDVOB_GREEN+	65
EXP_TXN1	0402_X7R	2	1	CA_0.1U_16V_K	C1455	SDVOB_GREEN-	SDVOB_GREEN-	65
EXP_TXP2	0402_X7R	2	1	CA_0.1U_16V_K	C1456	SDVOB_BLUE+	SDVOB_BLUE+	65
EXP_TXN2	0402_X7R	2	1	CA_0.1U_16V_K	C1457	SDVOB_BLUE-	SDVOB_BLUE-	65
EXP_TXP3	0402_X7R	2	1	CA_0.1U_16V_K	C1458	SDVOB_CLK+	SDVOB_CLK+	65
EXP_TXN3	0402_X7R	2	1	CA_0.1U_16V_K	C1459	SDVOB_CLK-	SDVOB_CLK-	65

close to NB

7.47	PEG_RXN2	0402_X7R	2	1	CA_0.1U_16V_K	C1460	STALL-	STALL-	65
7.47	PEG_RXP2	0402_X7R	2	1	CA_0.1U_16V_K	C1461	STALL+	STALL+	65



XCLK\_417: 0  
 1 (Reserved) (270MHz Default)  
 FB\_0\_BAR\_SIZE 0 256MB(Default)  
 ROM\_SO (0001)  
 SMB\_ALT\_ADDR: 0(0X9E)  
 VGA\_DEVICE: 1(VGA Device)

PCI\_DEVID[4]: 1 ROM\_SCLK (1010)  
 SUB\_VENDOR: 0

0 (No video BIOS ROM)  
 1 (BIOS ROM is present)

SLOT\_CLK\_CFG: 1

0 (GPU and MCH not share a common reference clk)  
 1 (GPU and MCH share a common reference clk)

PEX\_PLL\_EN\_TERM: 0  
 0 Disable(Default)  
 1 Enable

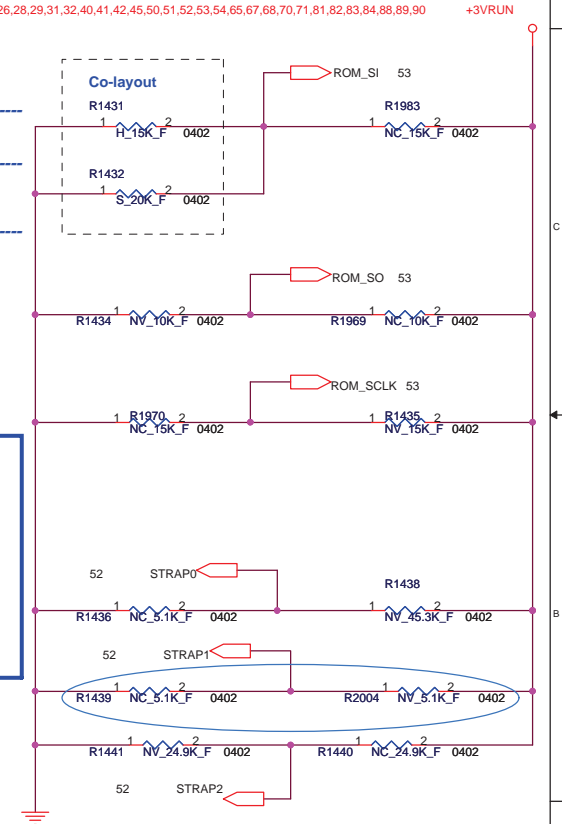
USER[3:0]: 1111 STRAP0 (1111)

N10\_3GIO\_PADCFG[3:0] STRAP1 (1000)  
 1000 Desktop(normal swing)

NB9X\_PCI\_DEVID[4:0]:PUN STRAP2 (0100)  
 N10P-GS 0X0A34 (0100)  
 N10M-GS 0X0A74 (0100)

#### ROM\_SI:

0010 64Mx16 DDR3 - 96 ball - monolithic 64-bit Hynix  
 0011 64Mx16 DDR3 - 96 ball - monolithic 64-bit Samsung



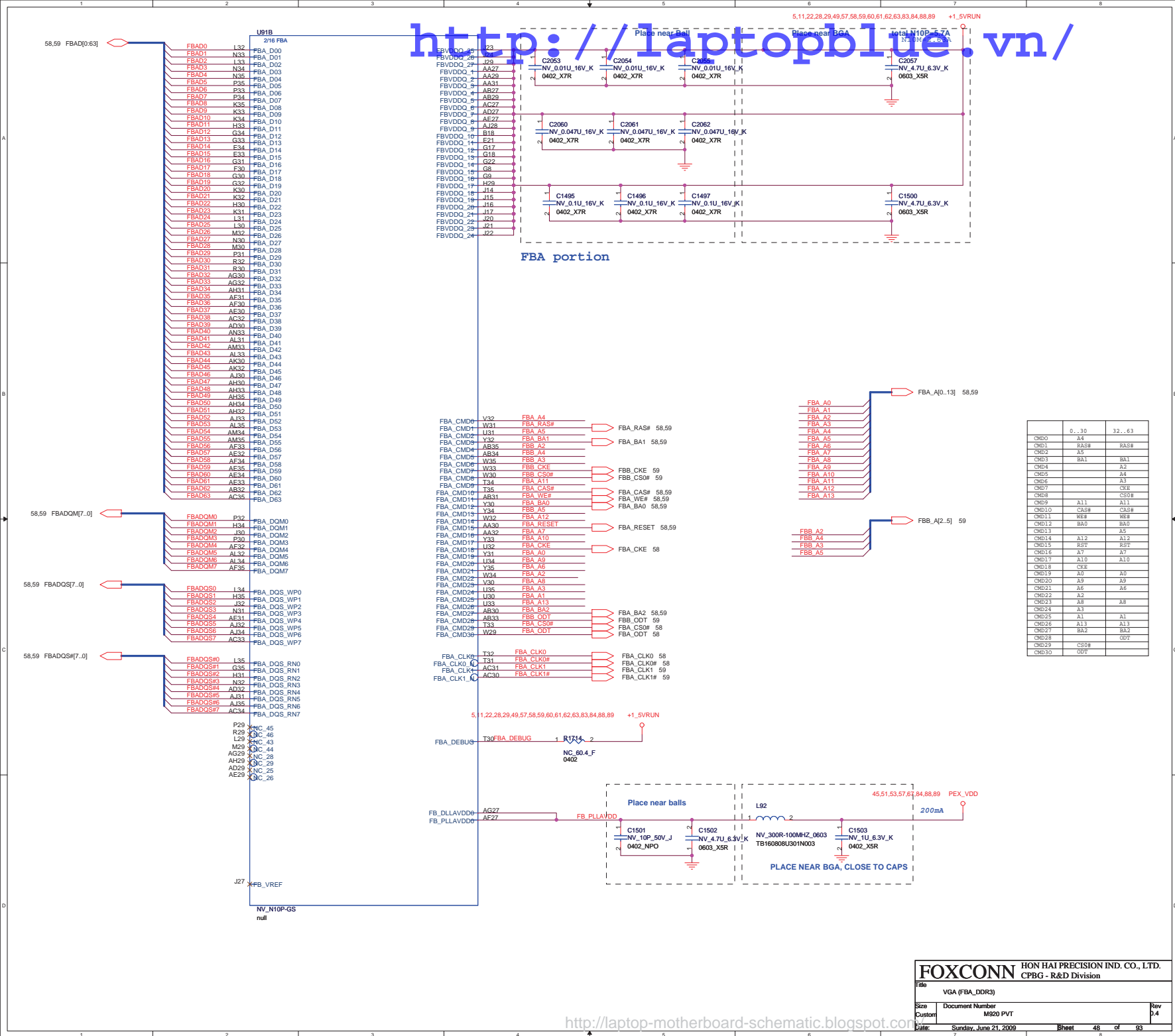
#### Logical Strap bit Mapping

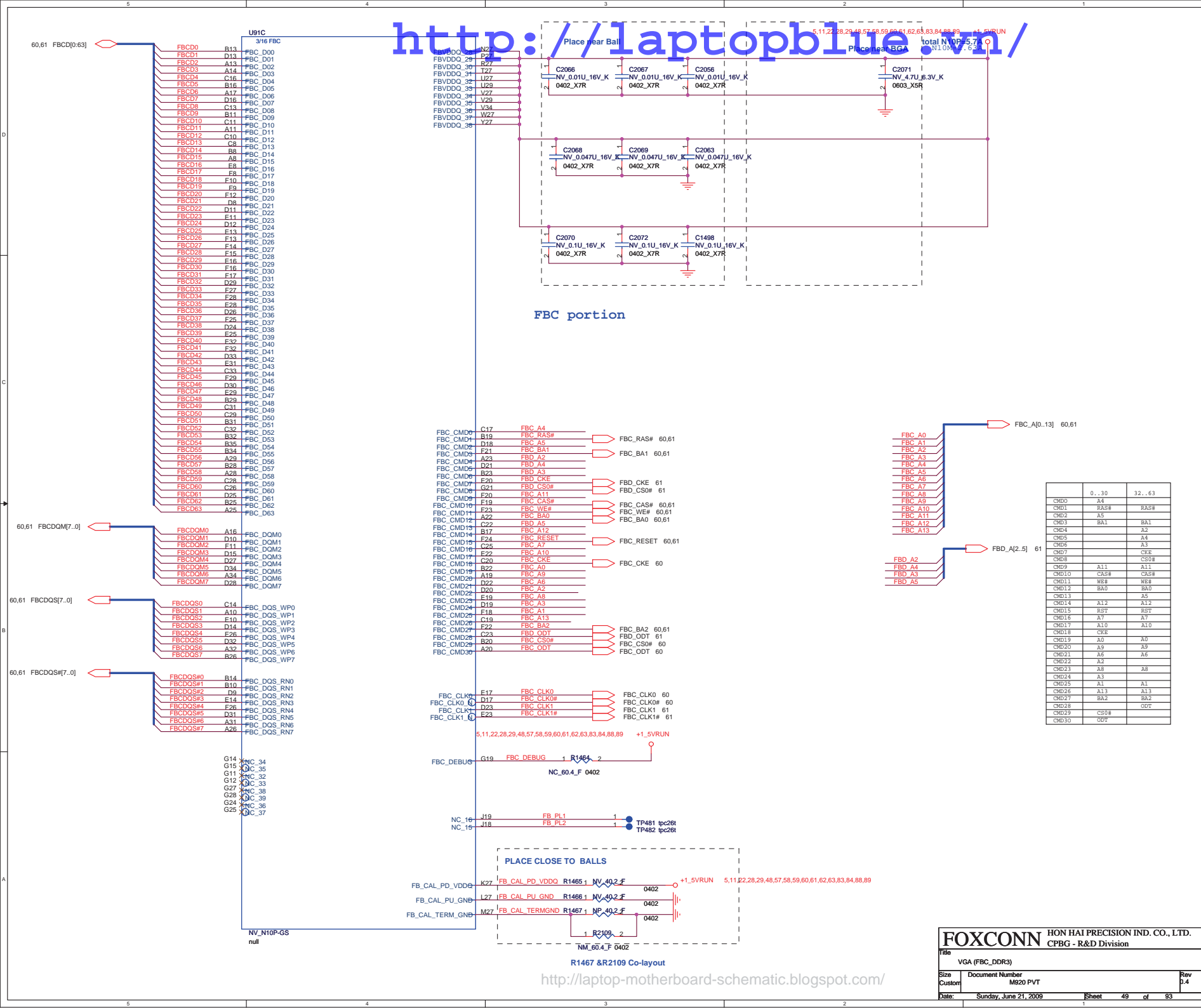
Resistor values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

#### Strap Options

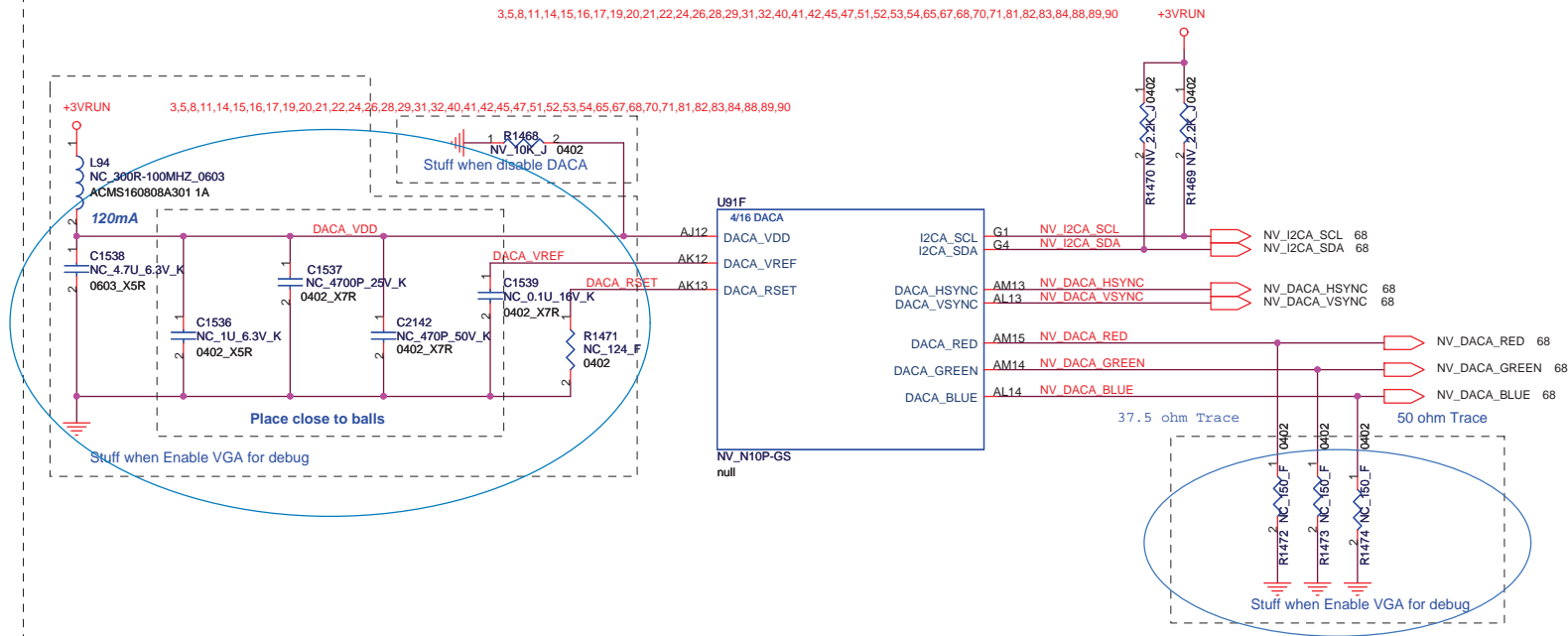
Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04202-001\_v02\_secured>

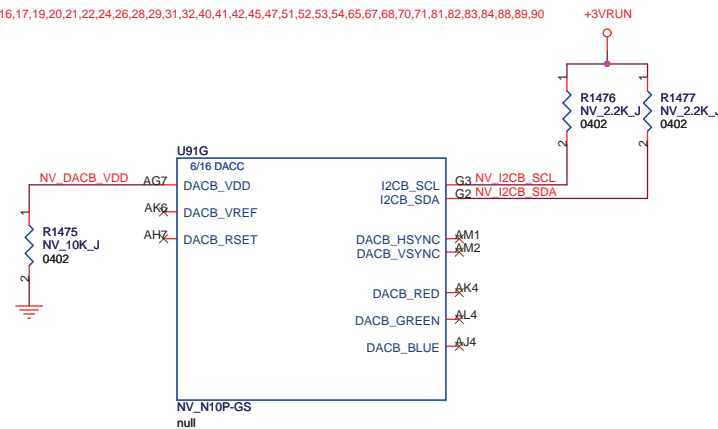




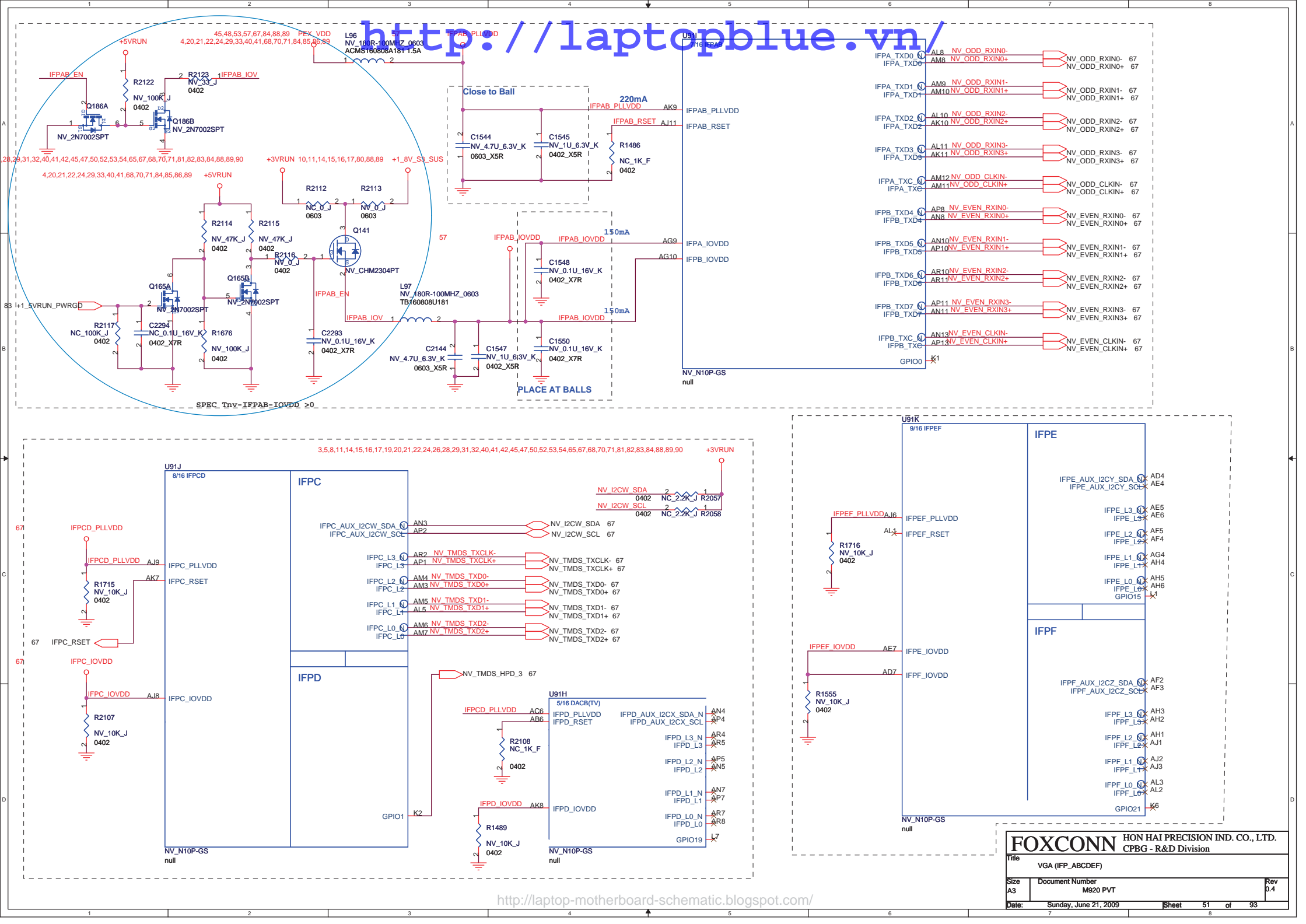
3,5,8,11,14,15,16,17,19,20,21,22,24,26,28,29,31,32,40,41,42,45,47,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90



3,5,8,11,14,15,16,17,19,20,21,22,24,26,28,29,31,32,40,41,42,45,47,51,52,53,54,65,67,68,70,71,81,82,83,84,88,89,90

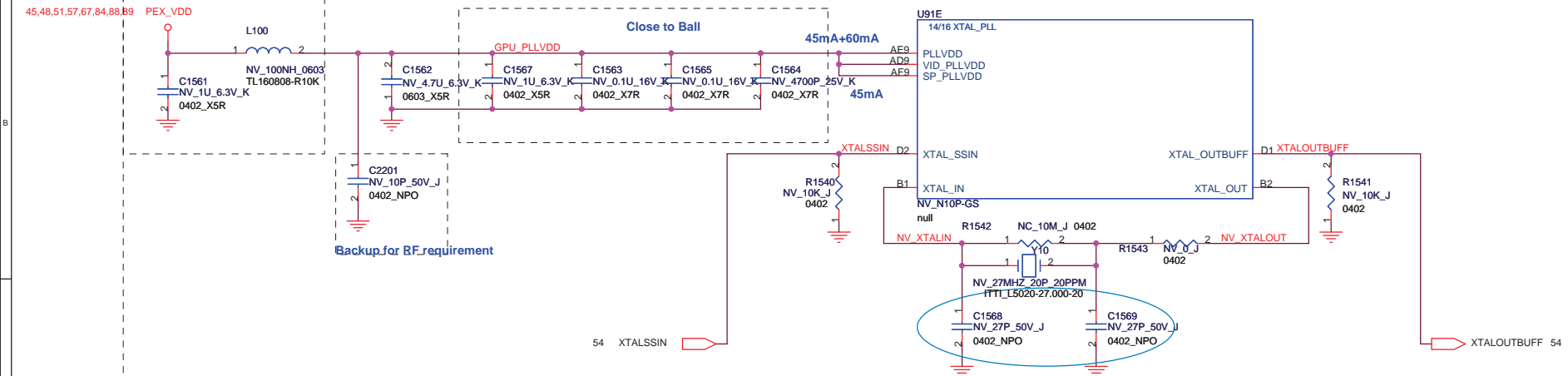
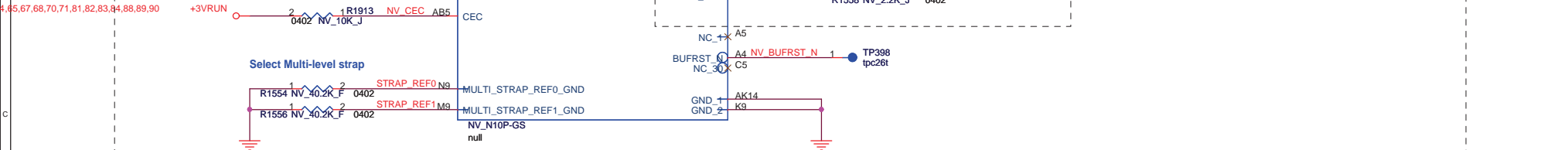




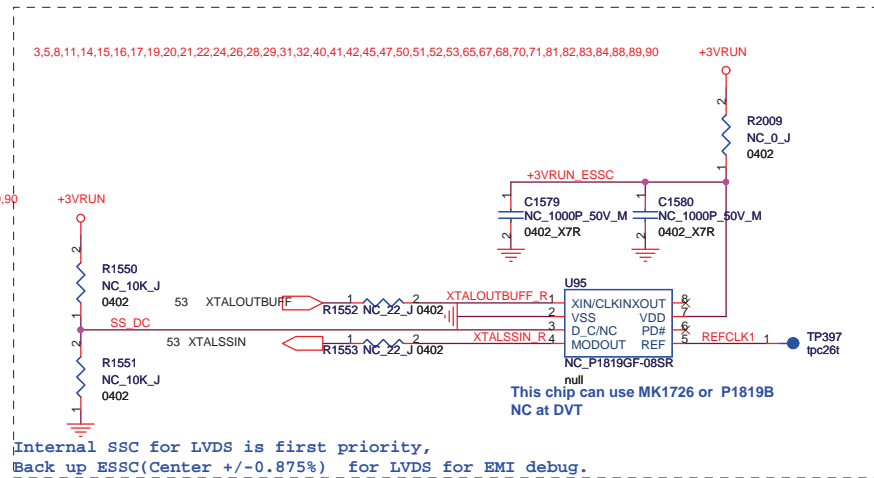




<http://laptopblue.vn/>



<http://laptopblue.vn/>



FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
VGA (SSC)			
Size	Document Number	Rev	
43	M920 PVT	0.4	
Date:	Sunday, June 21, 2009	Sheet	54 of 93

M920 Change History

- 11/18 Initial release with NB9X v01
- 12/03 Rough for RFQ V02
- 12/04 Rough for RFQ V03
- 12/09 Rough for netin v04
- 12/15 Rough for netin v05
- 12/30
- 1.cancel PCIE lane reverse
- 2.NC R1417 for PEX\_CLK test
- 3.NC AND gate U92 which for PEX\_RST
- 4.Correct GPU\_VDD\_SENSE reverse
- 5.Change ROM\_SO PD 10K
- 6.Change ROM\_SCLK 5K PU
- 7.Del FB\_CKE &CS0#&ODT 0ohm
- 8.Del FB\_CKE&ODT PD 10K
- 9.Del GPU\_Vref mizer funtion to fix Vref =0.5X
- 10.Change FB\_CAL\_TERM\_GND PD 40.2ohm to TP
- "11.Share none use IFPC\_PLLVDD&IFPD\_PLLVDD, IFPC\_IOVDD&IFPD\_IOVDD,IFPE\_IOVDD&IFPF\_IOVDD with a common resistor 10K PD"
- 12.PU GPIO\_NV\_THERM\_ALERT# 10K
- 13.camcel GPIO10 to TP
- 14.Stuff R1508 JTAG\_TRST\_N
- 15.PU I2CH 10K
- 16.PU CEC 10K
- 17.NC\_ESS
- 18.Change VRAM\_CLK term R to 73.2ohm\_F
- 19.Del VRAM\_Vref\_Mizer
- 20.Add 0.1u cap for Term resistor array
- 21.update VRAM symbol
- 22.Update Headvalue to NPd
- 23.Change TIRAMISU\_CONN to 50 PIN
- 24.Change U106 from G546A to G546B
- 25.Change INVERTOR\_CONNECTOR to 8PIN
- 26.Change SW\_U105 &U101 Sel signal TIRAMISU\_EXIST\_SEL
- 27.Camcel BL\_OFF# function on VGA page
- 28 add a cap for U102
- 29.Change LVDS connector to 1N-0040000-FWG0
- 30.I2C add 10pF
- 31.GPU Power add 22pF
- 32.FB\_DATA\_SWAP
- 33.FBVDDQ =+1\_5VRAN
- 34.Change Power decoupling follow DG
- 35 Change L94 Form 240R to 220R follow DG
- 01/03
- 1.Add a 0.1uF cap for u92 NC.
- 2.Change R1417 200\_Ω to 200\_F consist with M910
- 3.Add a 4.7uF cap for PEX\_SVDD
- 4.Add a 0ohm Resistor for VDD33 backup for debug
- 5.Revise PCIE\_TX Off-Page name .
- 6.Revise SDVO\_AC coupling capacitance headvalue
- 7.Revise DACA decoupling cap.
- 8.Revise IFPAB\_IOCDD latch.
- 9.Del GPU\_GPIO3&4 duplicate PD 10K
- 10.Revise PLLVDD\_SP\_PLLVDD decoupling capacitance.
- 11.Del TM\_Exist\_SEL duplicate PU.
- 01/07
- 1.reassign the TIRAMISU\_50Pin connector pin assignment.
- 2.Mirror LVDS\_RP horizontally for layout requirement.
- 3.Change GPU strap Pin,re define VRAM head value as Q\_H\_S\_.
- 4.Change LVDS connectoer pin assignment.
- 01/08
- 1.Change FBA\_CMD term R assignment fro layout requirement.
- 2.chang I2CH PD 10K to 2.2K,
- 3.Change CN57 inverter connector to 10pin 1N-0010000-M1T0.
- 4.Change CN57 Pin assignment.
- 5.Change R1416 from 0 to 10K for PEX\_CLKREQ#
- 6,add NC\_PU resistor for GPU strap.
- 7,PD\_FB\_CAL\_TERM\_GND\_NC\_40.2ohm
- 8,Delete C1786&L105 for CH7308B\_LVDD,change L106 to 0603 size.

- 01/09
- 1.Del Ch7308 none use NC part R1662,R1651&R1652&R1658,
- 2.Add c71 c72 for SDVO\_Ctrl BUS
- 4,Revise FB\_CAL\_TERM\_GND PD 40.2ohm from NV to NC\_
- 5.TIRAMISU\_Vedio\_IN change to A\_GND\_T
- 01/13
- Add two cap for PEX\_VDD
- change L97 from 30R to 22R
- change PEX\_SVDD
- 01/14
- Change GPU strap pin
- Change Rom\_SCLK from 15K PD to 15K PU
- Change strap 2 from 10K PU to 25K PD
- Add a 0ohm NC resistor for ESSC\_VCC
- 01/14
- Change INV\_CONN pin assignment
- Backup 3v3Run for IFPAB\_IOVDD
- 01/19
- Back roll from 01/17 to 01/14
- Change Q147 part
- Add ICH\_GPIO8 connect to TM\_EXIST\_SEL\_NC back up
- 01/21
- 1.Change R1721 to NC.
- 2.Change
- FBCAL\_PU\_GND R1466 40.2 -> 40.2ohm
- FBCAL\_PD\_VDDQ R1465 60.4 -> 40.2ohm
- FBCAL\_TERM\_GND R1465 NC -> 40.2ohm
- FBCLK Termination = R1568,R1581 73.2 -> 242ohm
- 3.Change ODT Term &CKE term
- EVT2
- 02/23
- 1.del VRAM Termination resistor.
- 2.del excrement capacitance based on layout to cost down.
- 3.NC\_CH7308B reserve pin and Bscan pin
- 02/25
- 1.Change +3V\_ALW power to +3V\_S4 for Tiramisu portion circuit.
- 2.Add TM\_HWS#
- 02/25
- 1.add a RC for LCDVCC\_EN
- 03/02
- 1.Change Headvalue\_NPD\_ to NP\_;
- 2.Stuff R1721 for NV thermal alert.
- 03/03
- 1.Modified by Chen QianKun,add TMDs output solution.
- 03/09
- 1.update the power filter Cap&Bead&Inductor based on DG\_v04.
- NV\_VDD two caps 0.01u change to 4700p
- PEX\_VDD two 0.1u chage to 0.01u
- L90 change from 10nH to 100nH
- L100 change from 120R/100MHz to 100nH
- L92 change from 220R/100MHz to 300R/100MHz
- L94 change from 220R/100MHz to 300R/100MHz
- L96 change from 120R to 180R
- L97 change from 220R to 180R
- 2.Rivise TMDs output circuit I2CW for DCC
- 3.del unused NC part R1574,R2015,R1588,R2088,R1602,R2019,R1616 and R2021
- 4.Del extra caps for VRAM bypass to cost down.

- 03/12
- 1.change TMDs\_DDC resistor to RP
- 2.change net name HDMI\_IN\_DETECT to TM\_SOURCE\_IN\_DETECT
- 3.Change net name HDMI\_PC#\_SELECT to TM\_PC#\_SELECT
- 5.change Q154 latch signal from +3VRUN to RUN\_PWRGD
- 4,Add 0.1u between GND and A\_GND

- 03/16
1. change tiramisu\_conn pin define
2. change C2108 from 0.1uf to 0.01uf
3. change D68? from 16-RSB12JS-2000 to 16-PESD5V2-S200

- 03/16\_2
1. Change TM\_SUS\_ON# circuit
2. NC\_CAP33 and change C1793 from 4.7u to 10u.
3. Change r2025 from 0ohm to 10Kohm
4. NC\_RF solution caps
5. NC\_ESSC

- 03/16\_2
1. PD\_IFPCD power
2. PD\_IFPCD RSET

DVT

- 04/08
1. P49, Change FB\_CAL\_TERM\_GND resistor for 10M\_SKU
2. P53, Change the CRYSTAL caps C1568,C1569 from 1C-2N20270-J000 to 1C-2N20200-J600

- 04/14
- 1.P51/P67, NC tiramisu\_MST solution parts : R2057,R2058,R2108,R2034,L118,L119, C2276,C2277,C2278,C2282,C2283,C2284,RP95,RP96,RP97,RP98,RP99,D68,D70, R2038,C2269,C2270,C2271,C2272,C2273,C2274,C2279
- 2.P66, Del C1795,R2025 change to 1K, CAP33 change to 330uF , add discharge circuit
- 3.P47, Del Qimonda strap\_resistor R1433
- 4.P51, Del IFPAB-IOVDD\_backup +3VRUN\_circuit R2011

- 04/15
- 1.P48/P49/P58/P59/P60/P61,change net name FBA(C)WDQS[7..0] to FBA(C)DQS[7..0], change FBA(C)RDQS[7..0] to FBA(C)DQS#[7..0].
- 2,P67,Change RP95,RP96,RP97,RP98,RP99 from 1R-1010000-JP00 to 1R-1010000-JX00.

- 04/17
- 1.P64, Change CN56\_PIN 1 to +5V\_ALW\_PIN 5 to DC\_OUT,Change F18 from 1M-F6V0A25-F000 to 1M-F6V0A75-0000.
- 2.P66,Change C1793 from 1C-2B70106-M100 to 1C-33R0157-M101.
- Change R1669 from 1R-0000471-J300 to 1R-0000101-J300 and stuff it.
- 3.P51, Change IFPAB-IOVDD from +1\_8V\_S3\_SUS to +3VRUN

- 04/18
- 1.P64, Change C2120,C2122 from 1C-2B20471-K000 to 1C-2N20221-K000 and stuff it as audio request.
- 2.P66, Change R1669 from 1R-0000101-J300 to 1R-0000101-J600 .

- 04/20
- 1.P66, Add a 10uF cap C ? .

PVT

- 06/02
- 1.Page 51 Change IFPAB\_ABIOVDD power latch circuit (Q141).
- 2.Page 47 Change strap 1 from PD\_5K to PU\_5K according to Nvidia N10x\_GPU qualification.
- 3.Nc CRT function for H&M\_SKU.
- 4,NC\_R1508

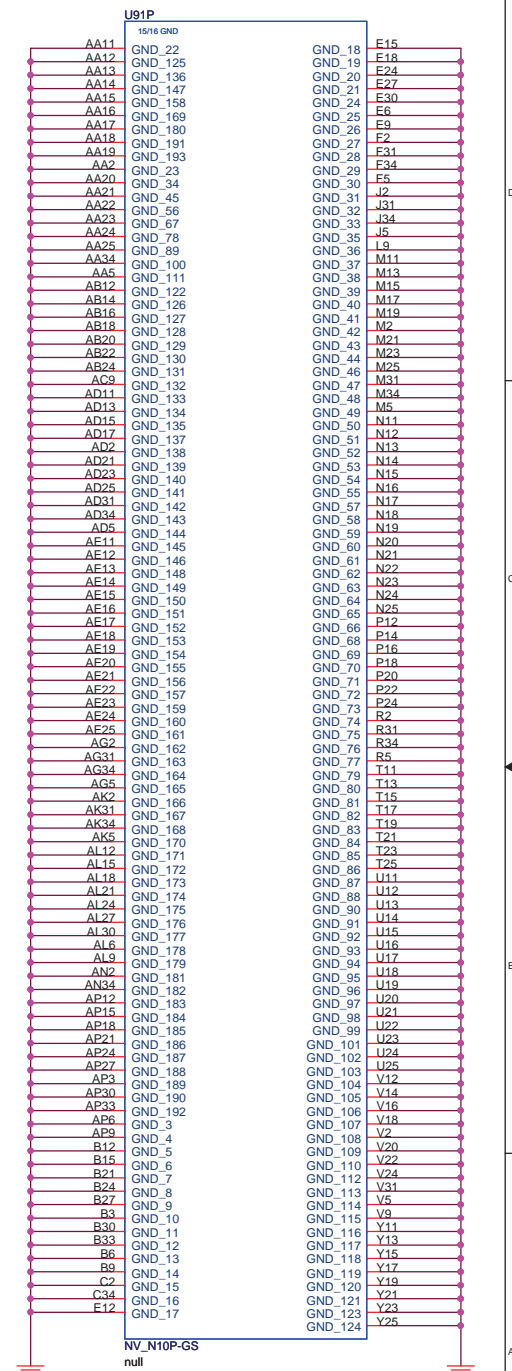
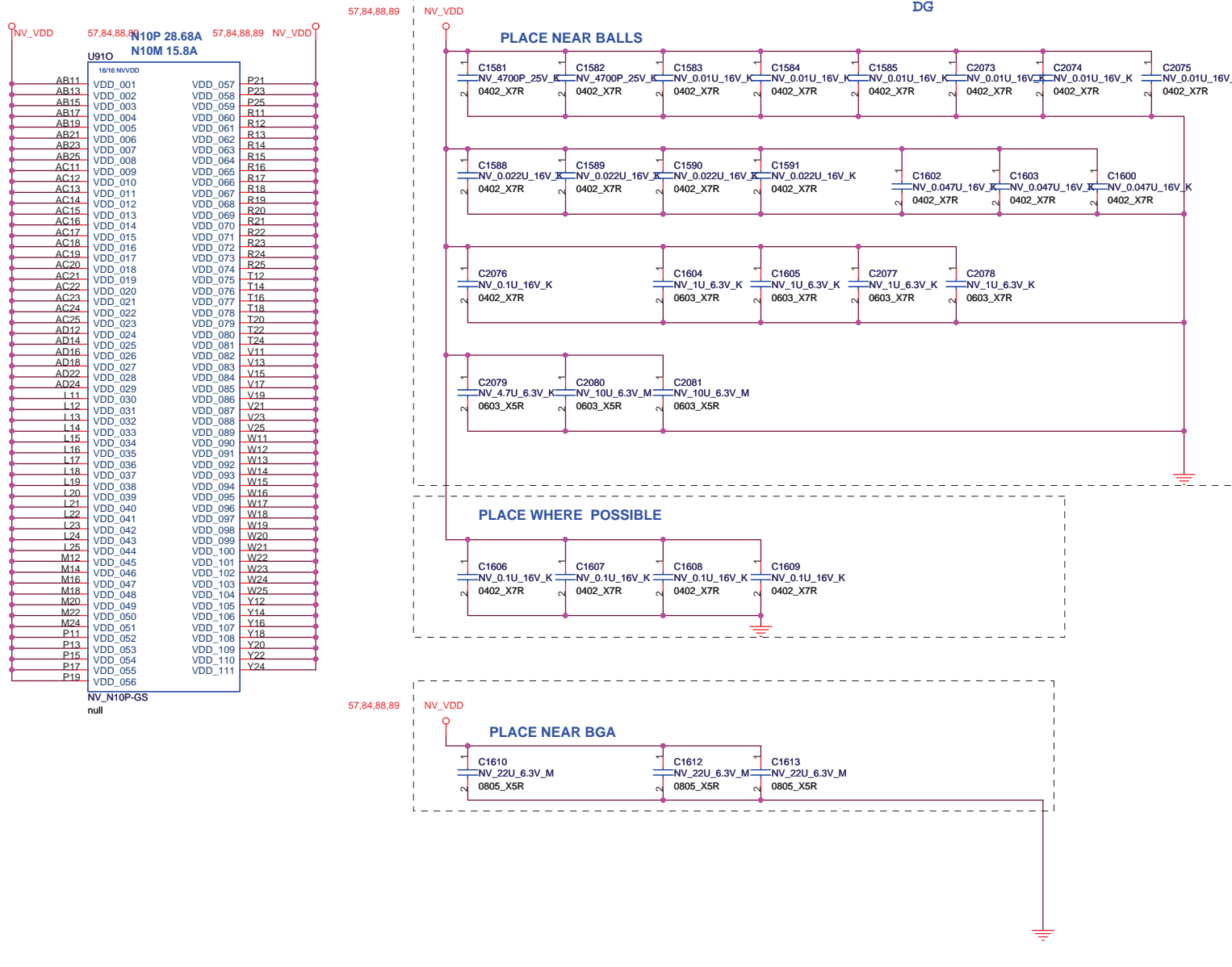
- 06/15
- 1.Change CN56\_Pin1 from +5V\_ALW to DC\_OUT.Change F18 from 1M-F6V0A75-0000 to 1M-F6V0A25-F000.

- 06/18
- 1.P67 Change IFPCD\_PLLVDD power rail from PEX\_VDD to +3VRUN.
- 2.P53 Change C1568 and C1569 from 1C-2N20200-J600 to 1C-2N20270-J000.

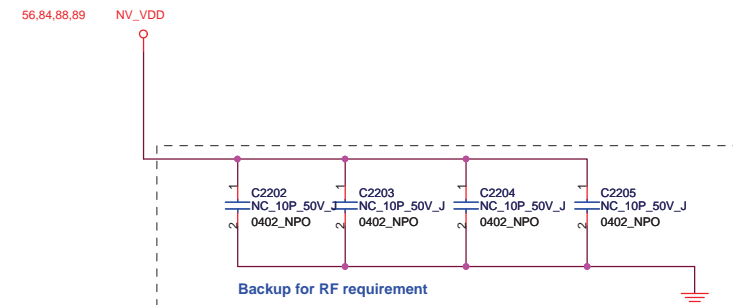
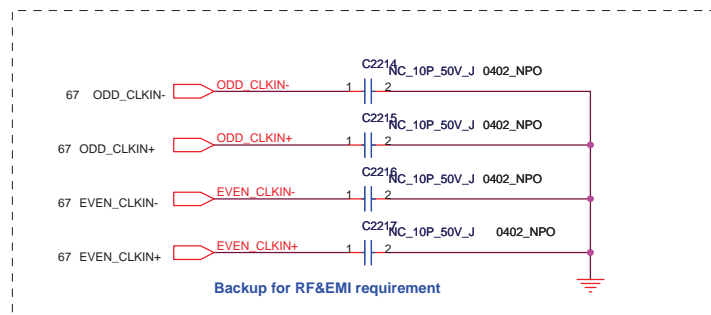
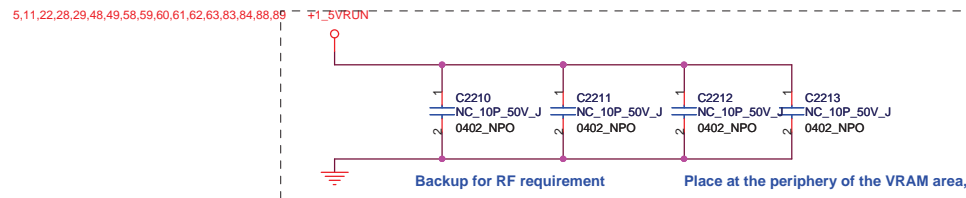
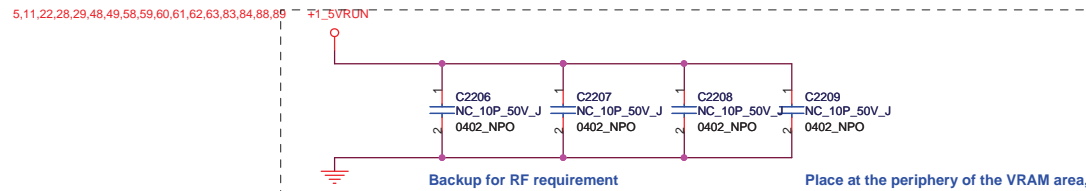
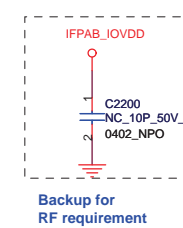
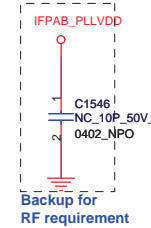
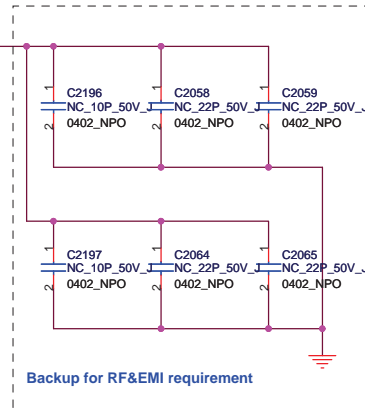
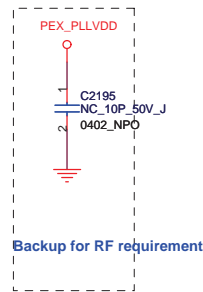
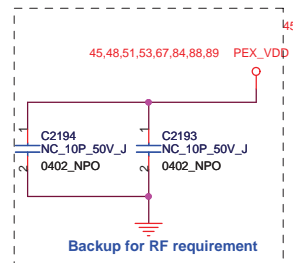
- 06/19
- 1.P64 Add one fuse F? between DC\_OUT and CN56.

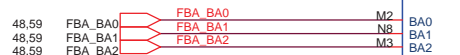
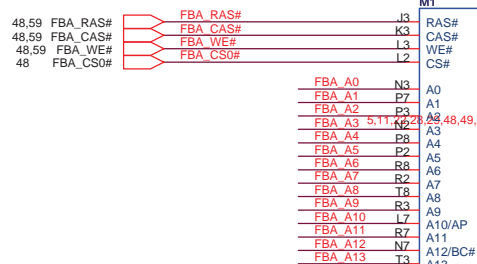
- 06/20
- 1.Add discharge\_circuit for IFPAB\_IOVDD

FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	VGA (PWR&GND)		
Size A3	Document Number M920 PVT	Rev 0.4	
Date:	Sunday, June 21, 2009	Sheet 55 of 93	1

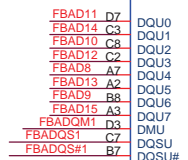
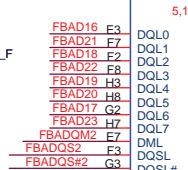




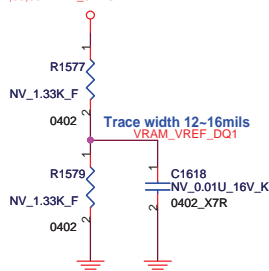




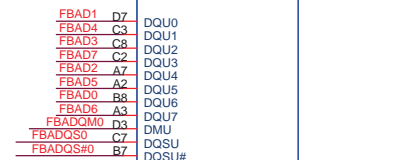
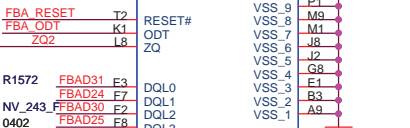
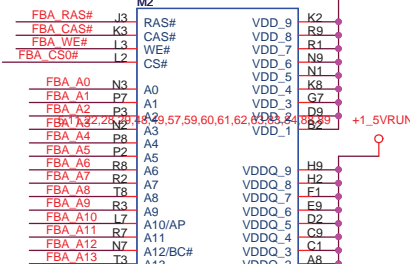
1 R1568 NV\_243\_F 0402



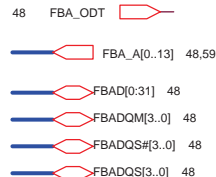
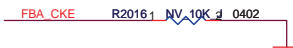
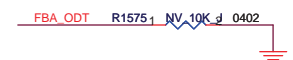
NV\_SDRAM\_FBGA-96P\_1GB  
H5TQ1G63BFR-12C

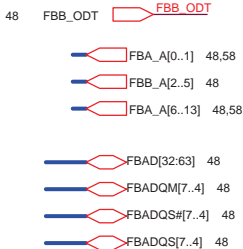


	0..30	32..63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	A2
CMD4	A2	A4
CMD5	A4	A3
CMD6	A3	CKE
CMD7	CKE	CS0#
CMD8	CS0#	A11
CMD9	A11	CAS#
CMD10	CAS#	WE#
CMD11	WE#	BA0
CMD12	BA0	A5
CMD13	A5	A12
CMD14	A12	RST
CMD15	RST	A7
CMD16	A7	A10
CMD17	A10	CKE
CMD18	CKE	A0
CMD19	A0	A9
CMD20	A9	A6
CMD21	A6	A8
CMD22	A8	A3
CMD23	A3	A1
CMD24	A1	BA2
CMD25	BA2	ODT
CMD26	ODT	CS0#
CMD27	CS0#	ODT
CMD28	ODT	
CMD29		
CMD30		



NV\_SDRAM\_FBGA-96P\_1GB  
H5TQ1G63BFR-12C

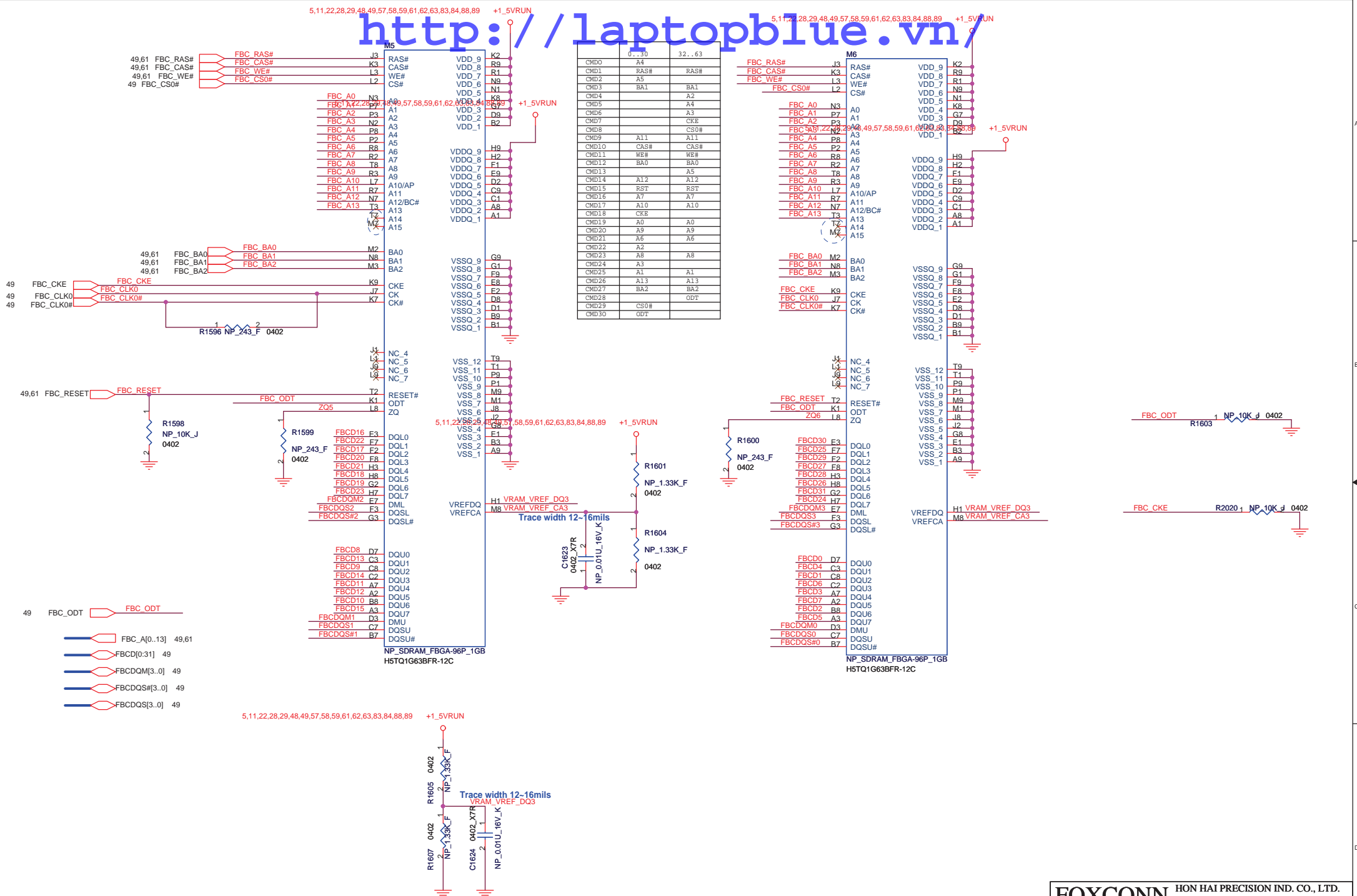


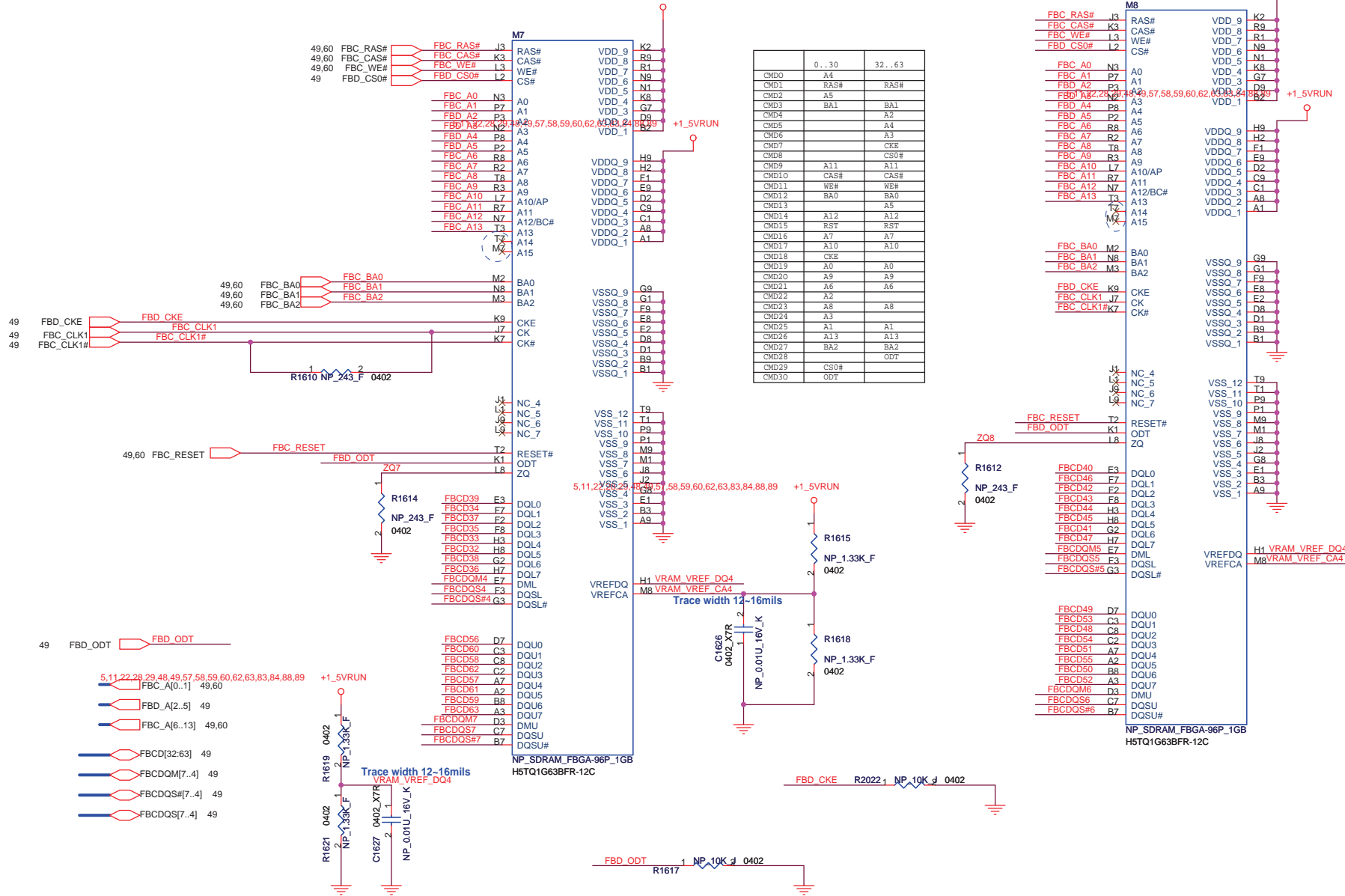


49,49,57,58,59,61,62,63,83,84,88,89 +1\_5VRUN

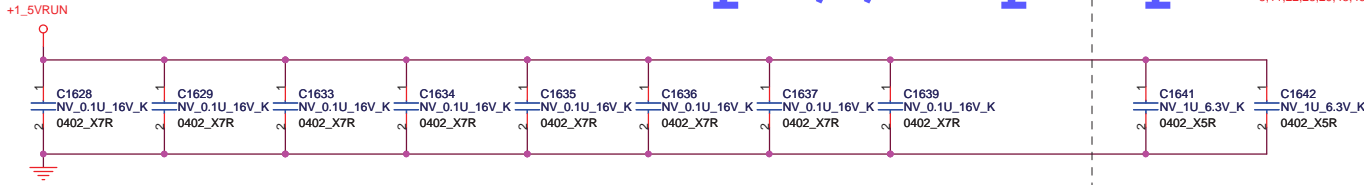
5,11,21,28,29,48,49,57,58,59,61,62,63,83,84,88,89 +1\_5V

http://laptopblue.vn/

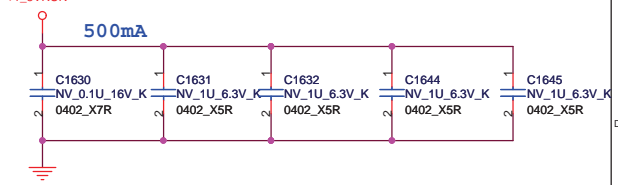




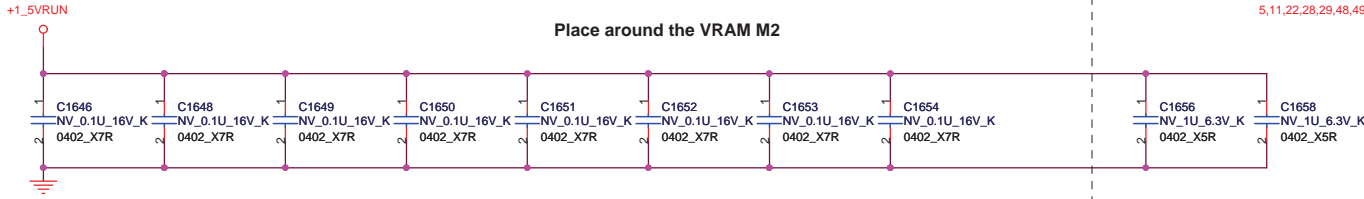
Place around the VRAM M1



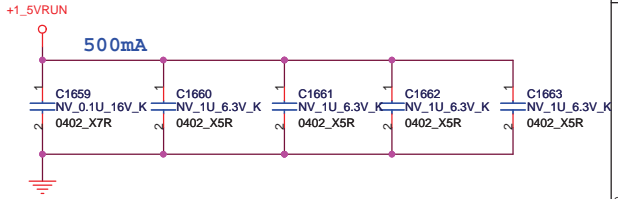
Place around the VRAM M1



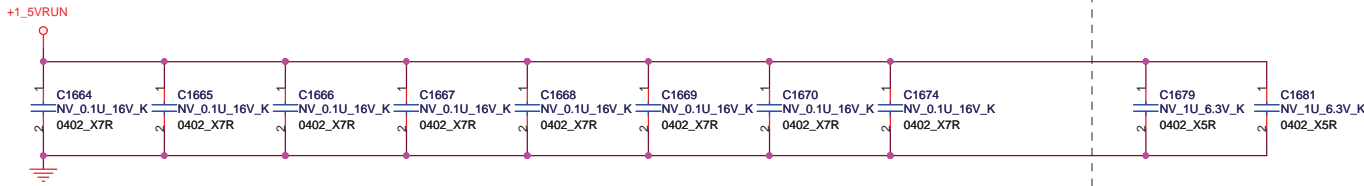
Place around the VRAM M2



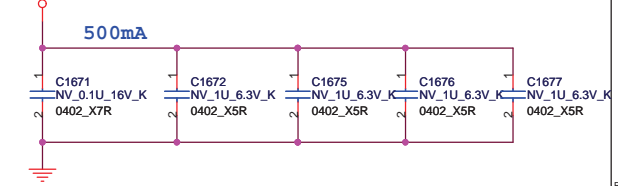
Place around the VRAM M2



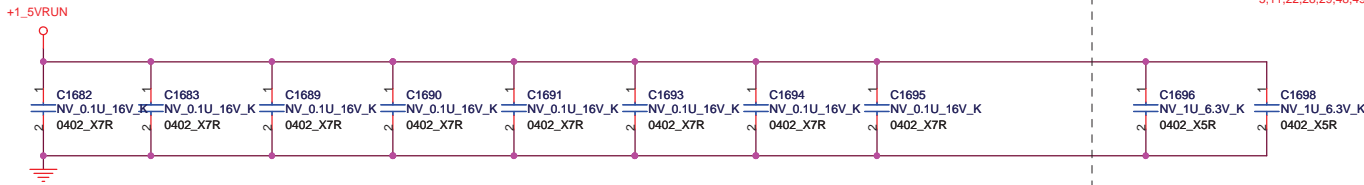
Place around the VRAM M3



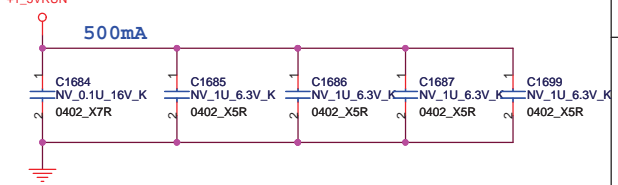
Place around the VRAM M3



Place around the VRAM M4



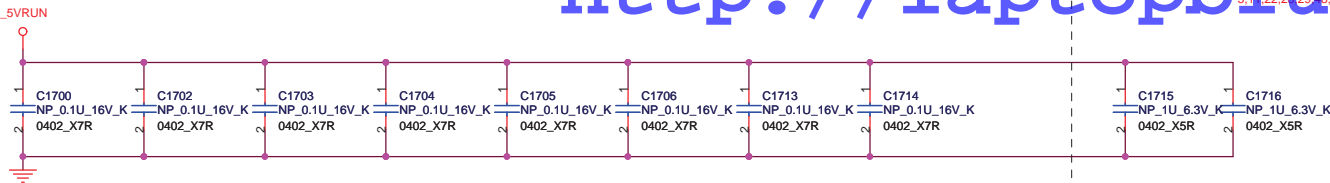
Place around the VRAM M4



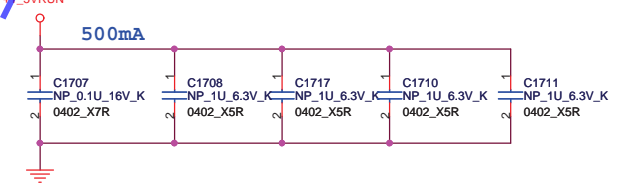
PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

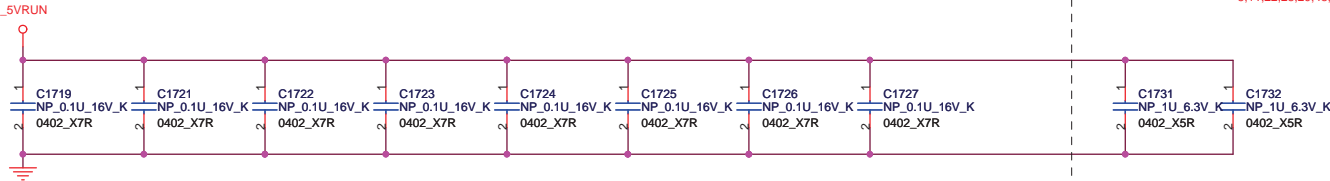
Place around the VRAM M5



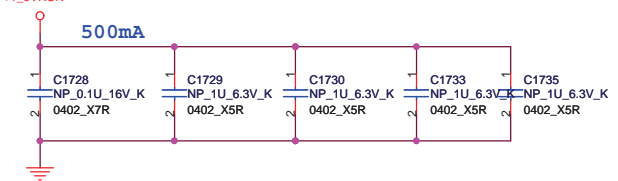
Place around the VRAM M5



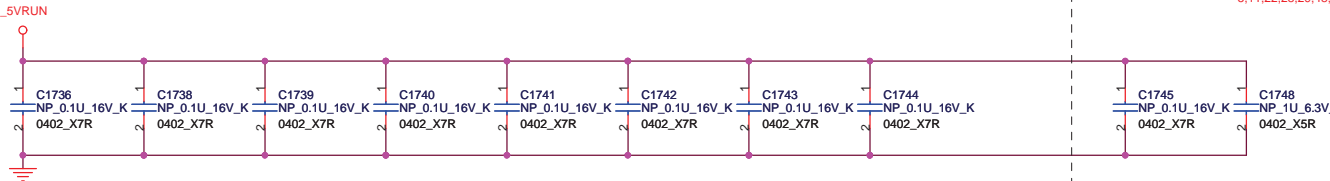
Place around the VRAM M6



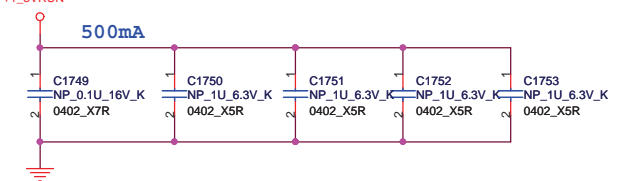
Place around the VRAM M6



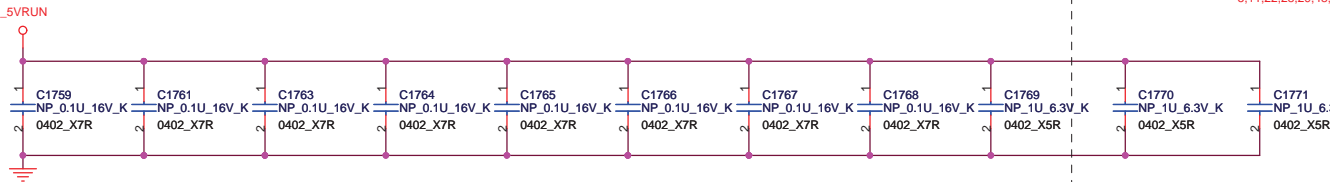
Place around the VRAM M7



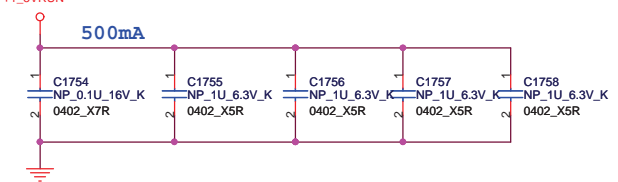
Place around the VRAM M7



Place around the VRAM M8



Place around the VRAM M8

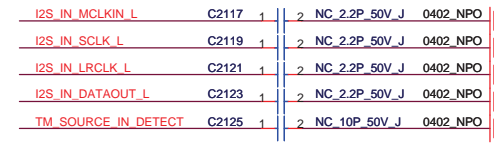
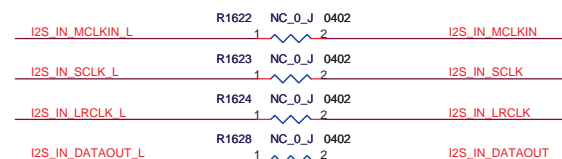
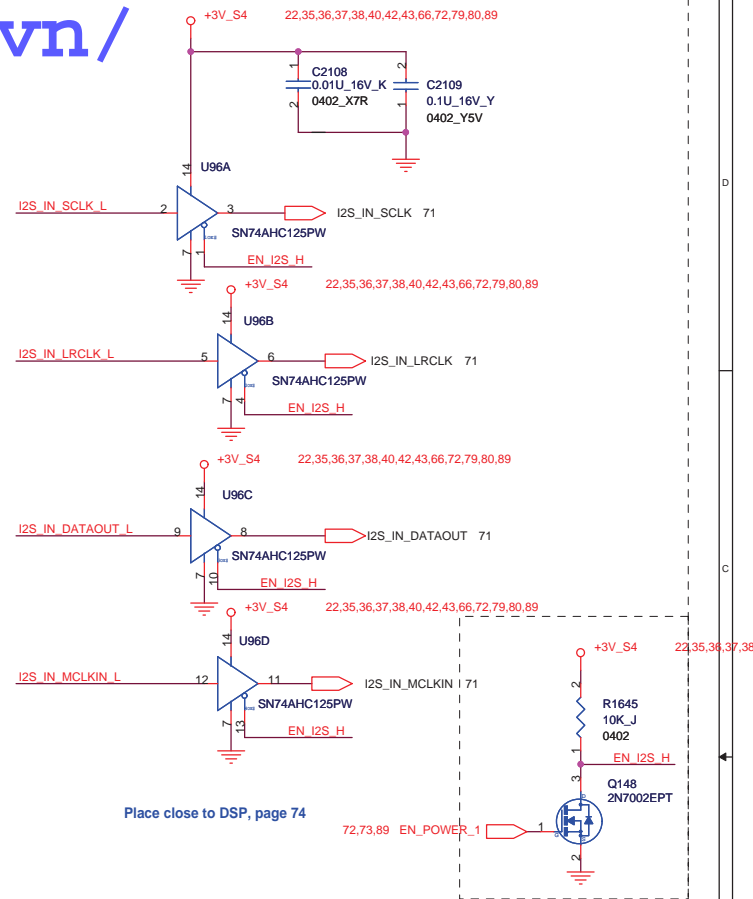
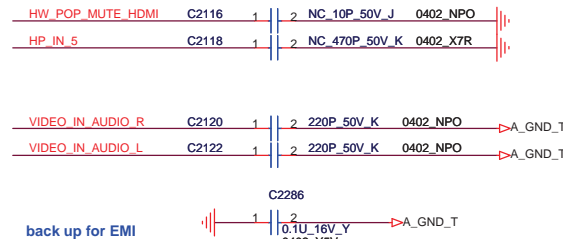
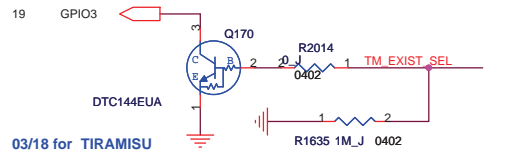
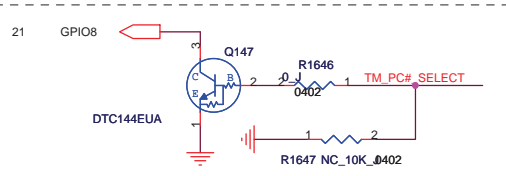
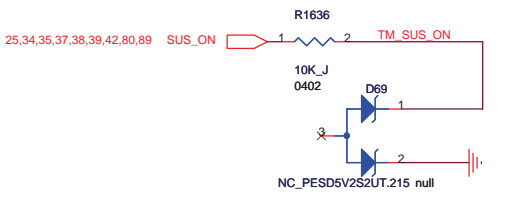
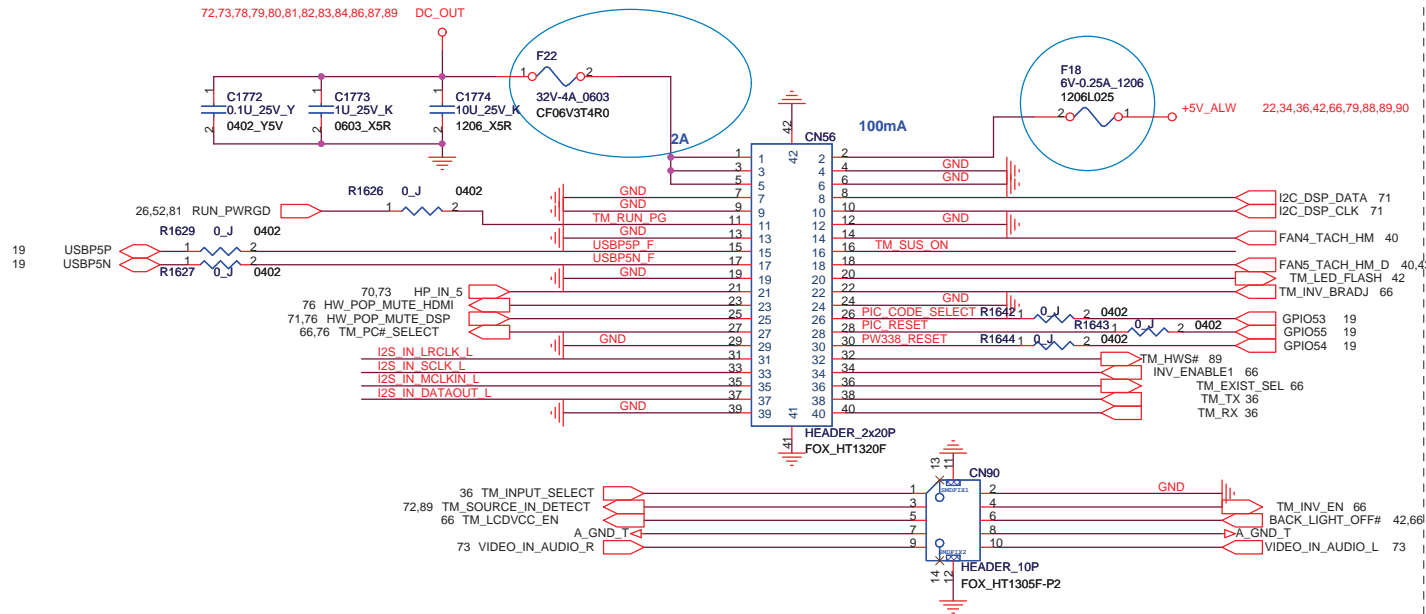


PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.

PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title		
VGA (VRAM BYPASS) 2/2		
Size	Document Number	Rev
A3	M920 PVT	0.4
Date:	Sunday, June 21, 2009	Sheet 63 of 93

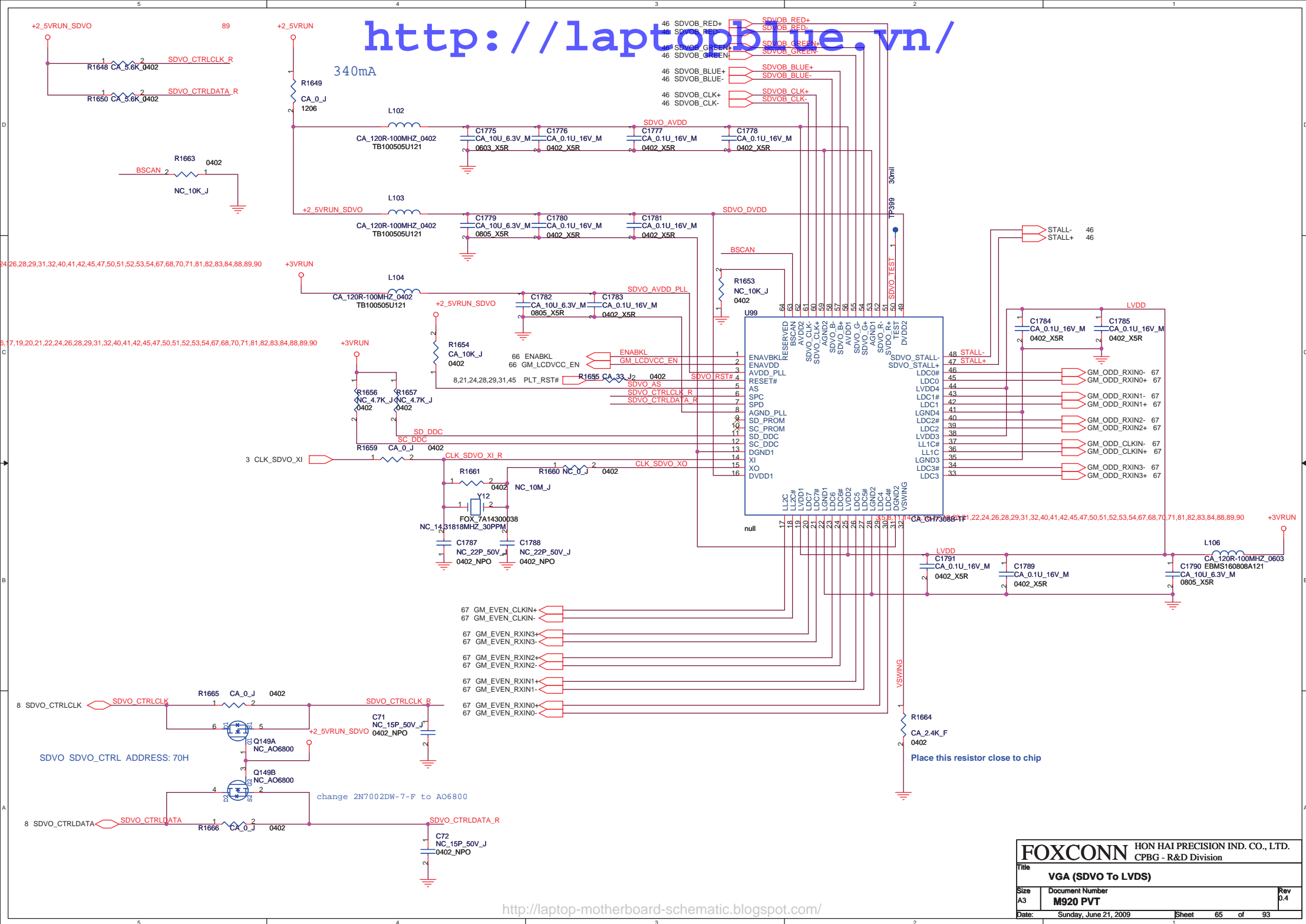




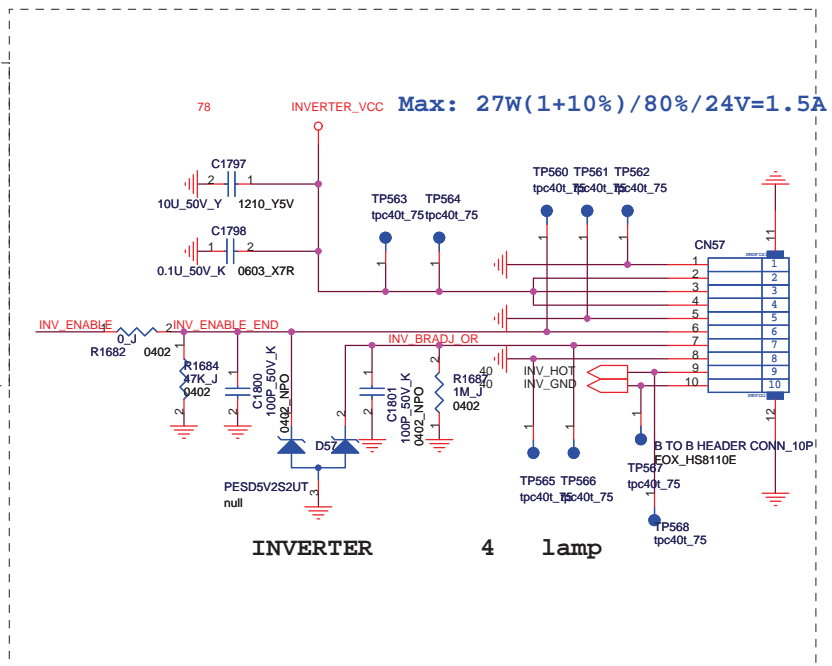
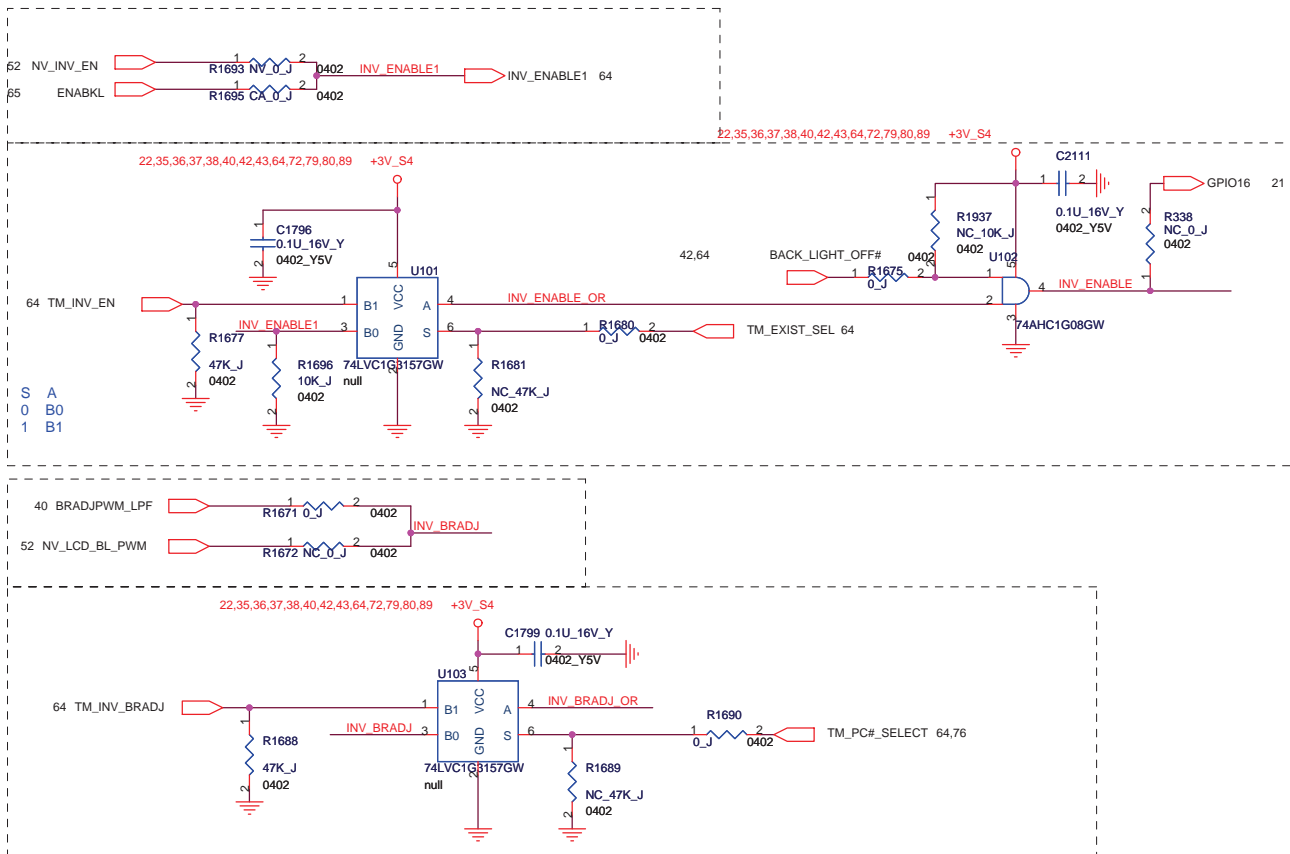
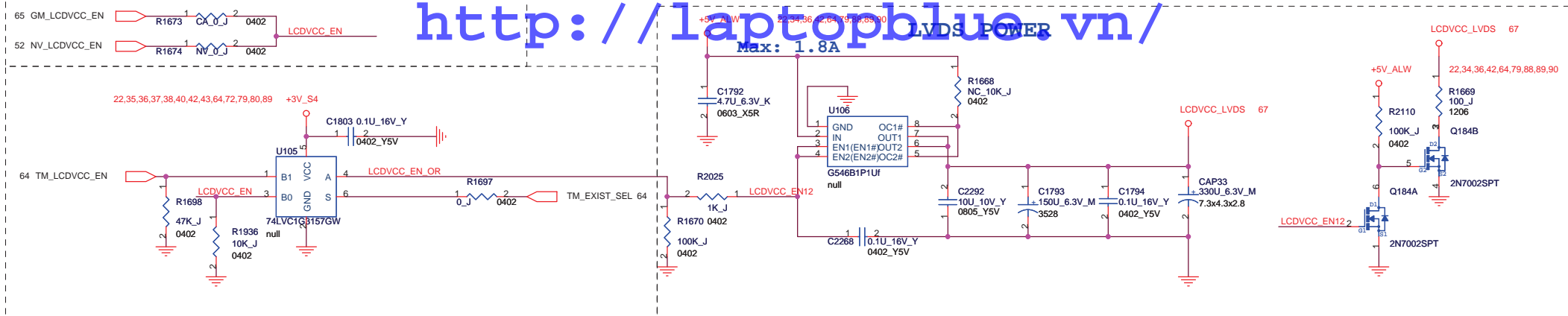
46 SDVOB\_RED+  
46 SDVOB\_RED-  
46 SDVOB\_GREEN+  
46 SDVOB\_GREEN-

SDVOB\_RED+  
SDVOB\_RED-  
SDVOB\_GREEN+  
SDVOB\_GREEN-

http://laptopblue.vn/



http://laptopblue.vn/



**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title	VGA (INVERTER)
-------	----------------

Size A3	Document Number <b>M920 PVT</b>
------------	------------------------------------

Date: Sunday, June 21, 2009

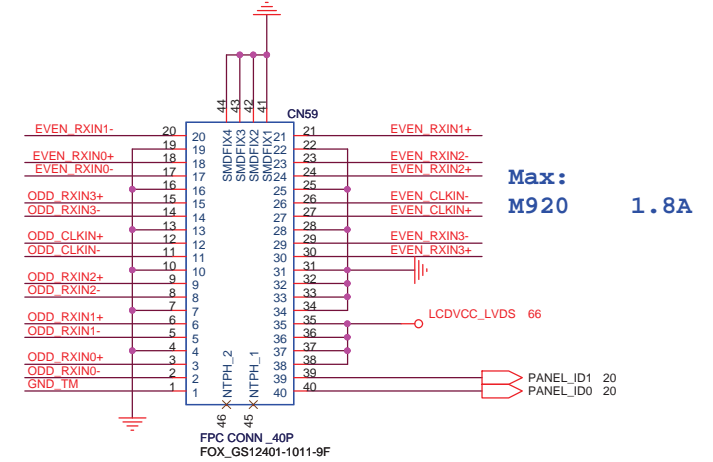
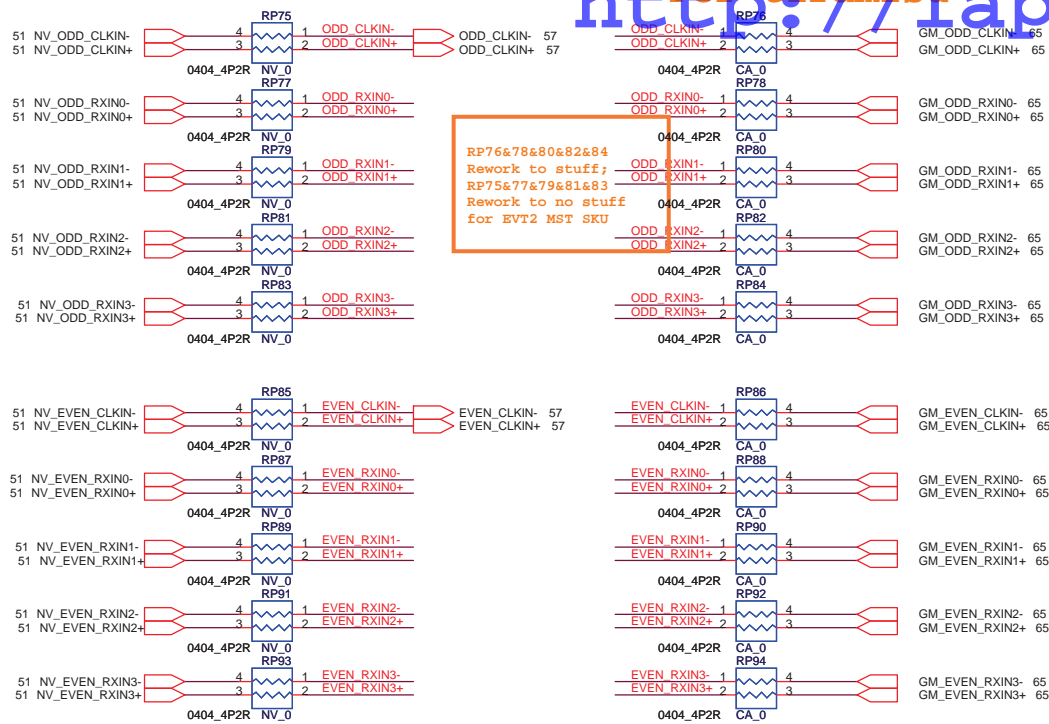
Sheet 66 of 93

Rev	0.4
-----	-----

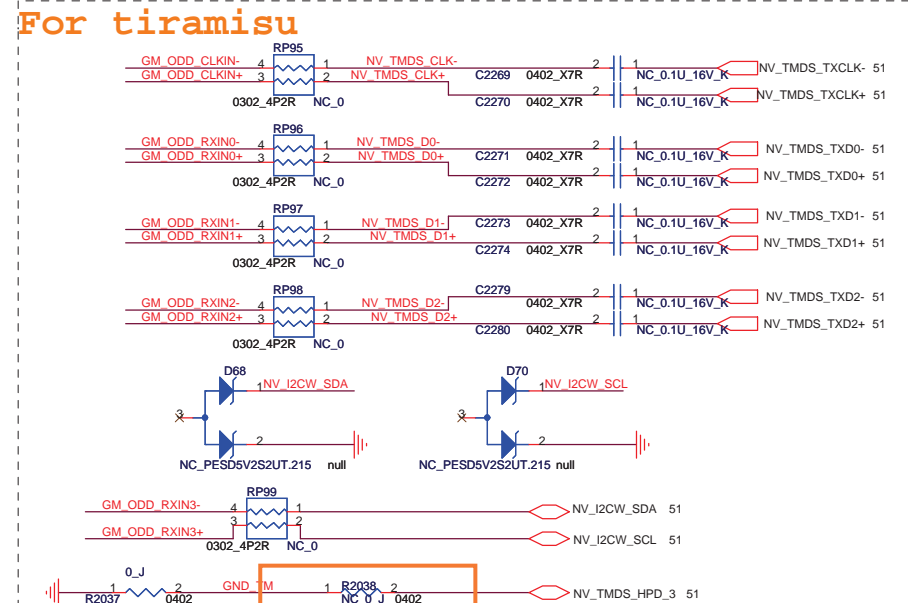
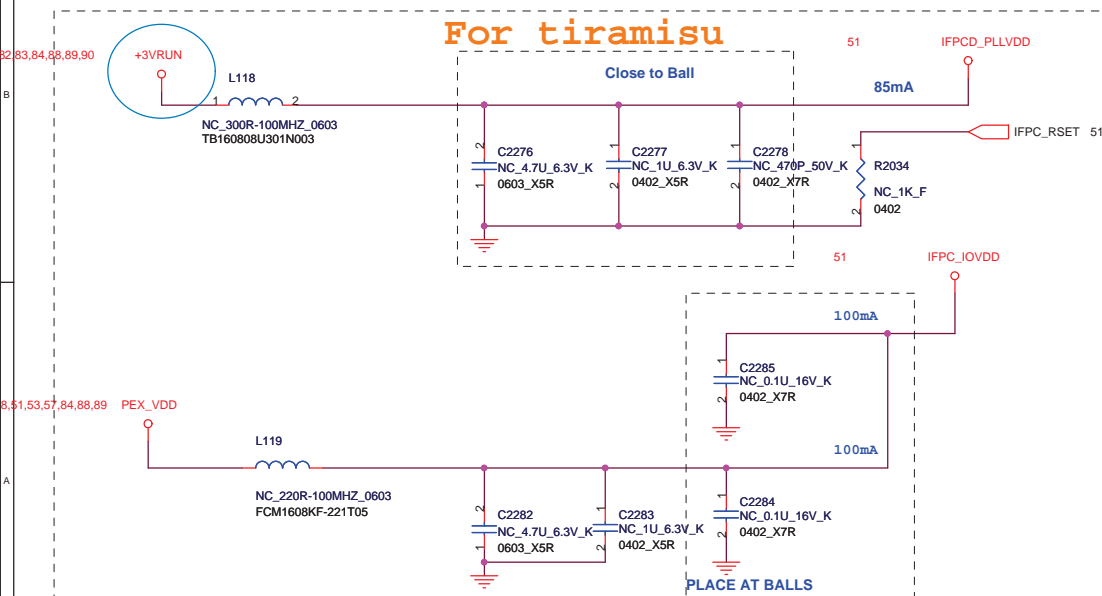
<http://laptop-motherboard-schematic.blogspot.com/>

For tiramisu

<http://laptopblue.vn/>



Panel ID		
00	AUO 24" 1920*1080 M240HW01 V0	

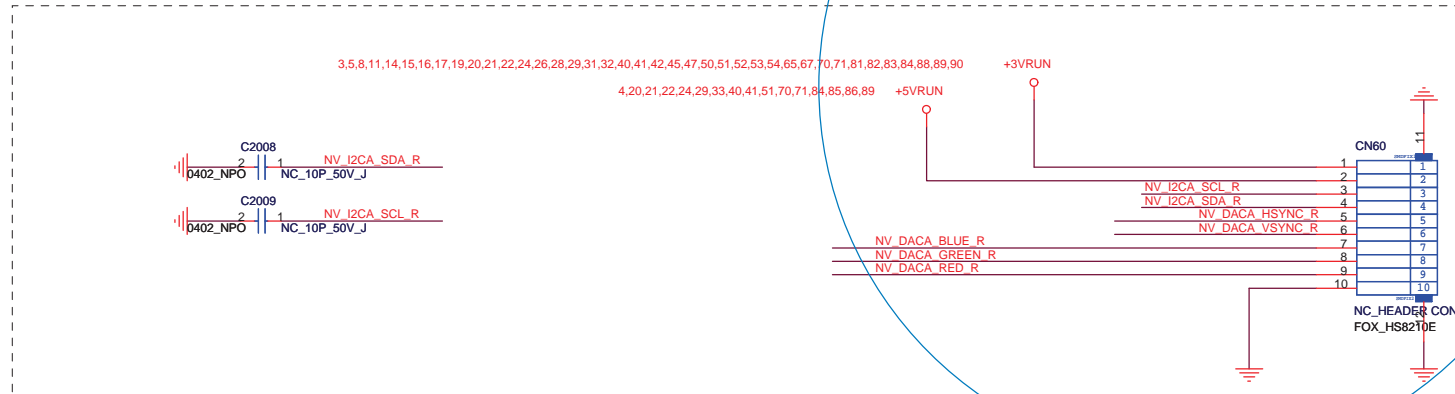
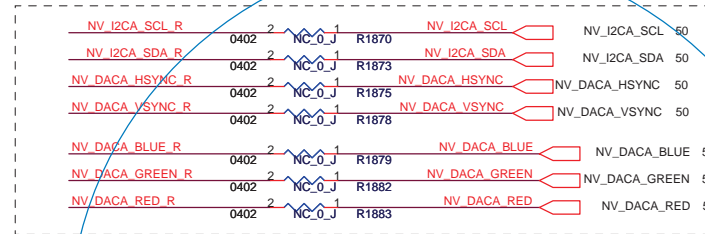
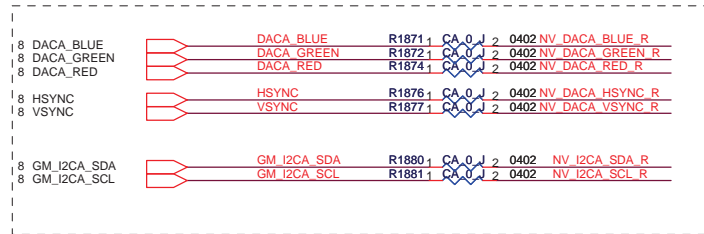


<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title <b>VGA (LVDS OUTPUT)</b>			
Size A3	Document Number <b>M920 PVT</b>		Rev 0.4
Date:	Sunday, June 21, 2009	Sheet	67 of 93

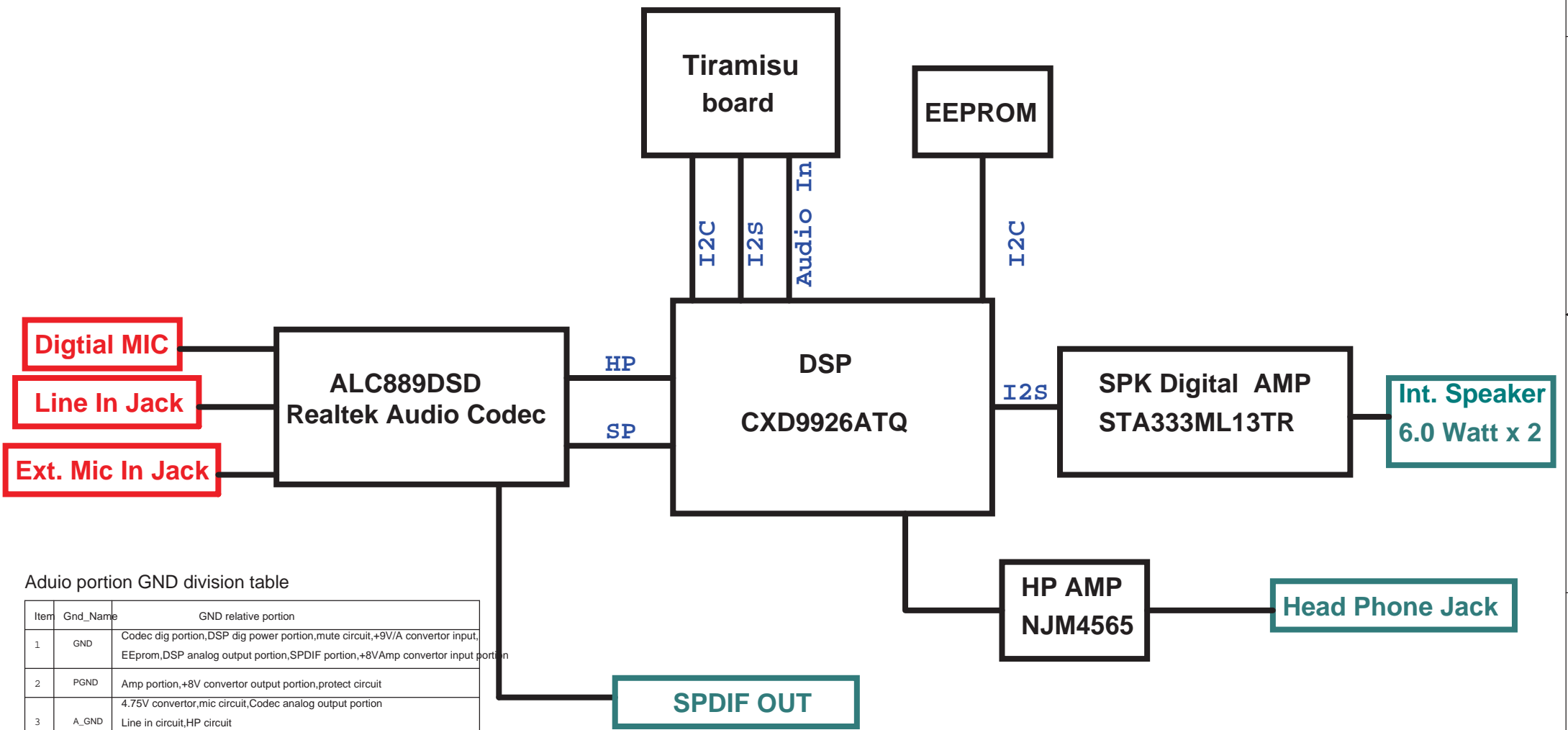
Head value TM\_ : Just for EVT2 MST SKU

<http://laptop-motherboard-schematic.blogspot.com/>

<http://laptopblue.vn/>



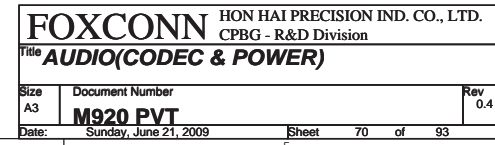
# M920 Audio Board Block Diagram



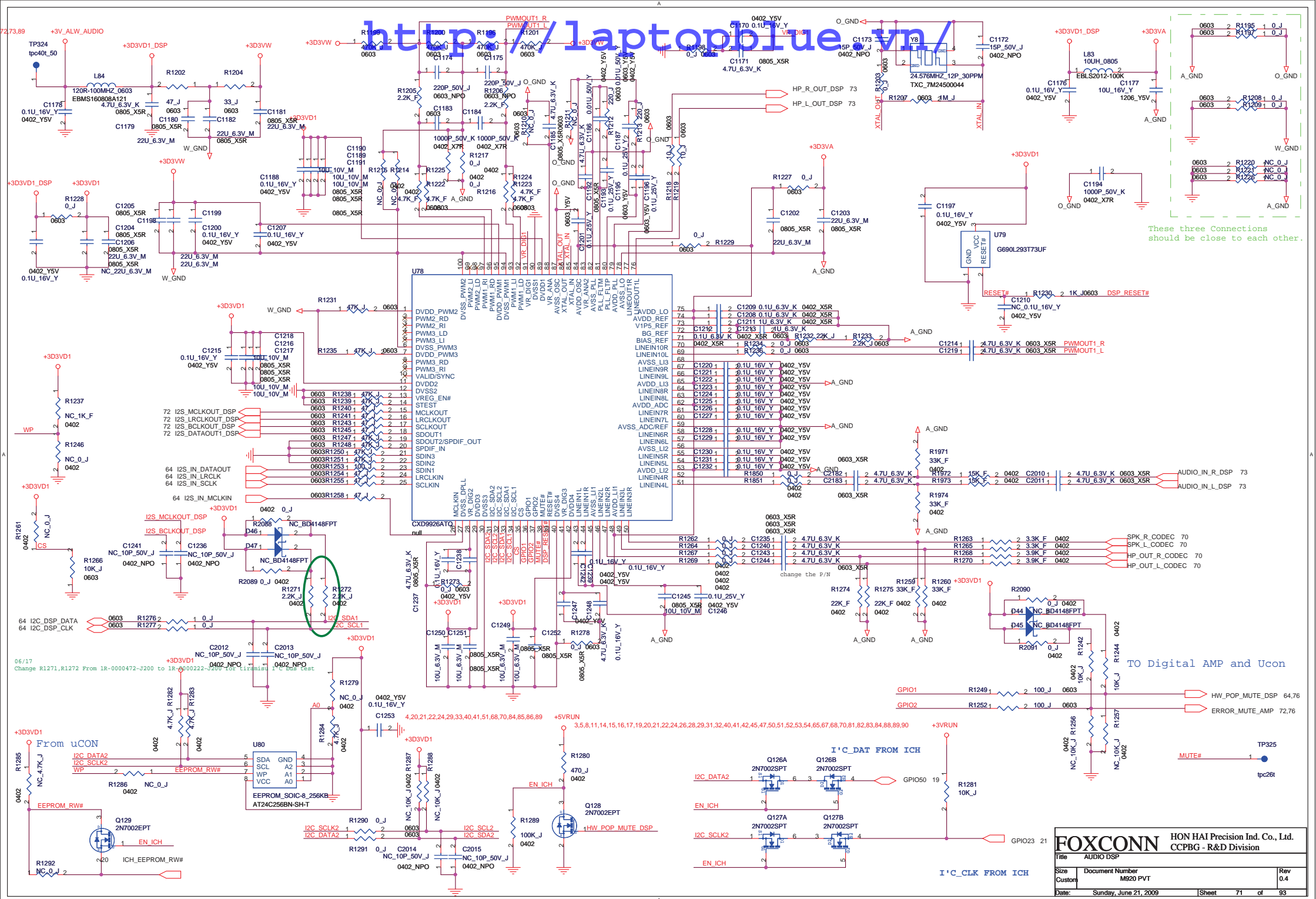
Aduio portion GND division table

Item	Gnd_Name	GND relative portion
1	GND	Codec dig portion,DSP dig power portion,mute circuit,+9V/A convertor input,EEprom,DSP analog output portion,SPDIF portion,+8VAmp convertor input portion
2	PGND	Amp portion,+8V convertor output portion,protect circuit
3	A_GND	4.75V convertor,mic circuit,Codec analog output portion Line in circuit,HP circuit
4	O_GND	DSP osc portion
5	W_GND	DSP PWM power portion

<http://laptop-motherboard-schematic.blogspot.com/>

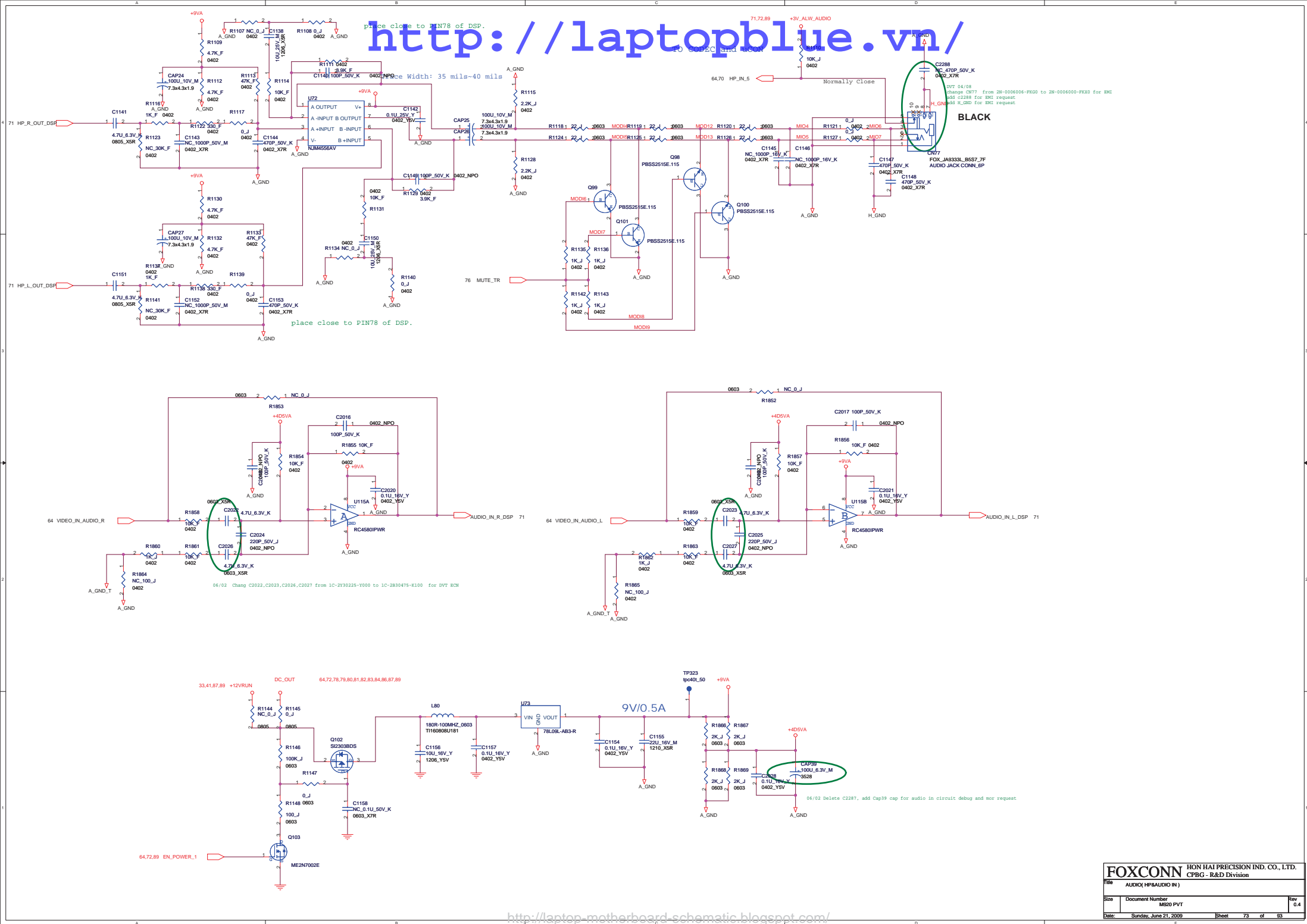


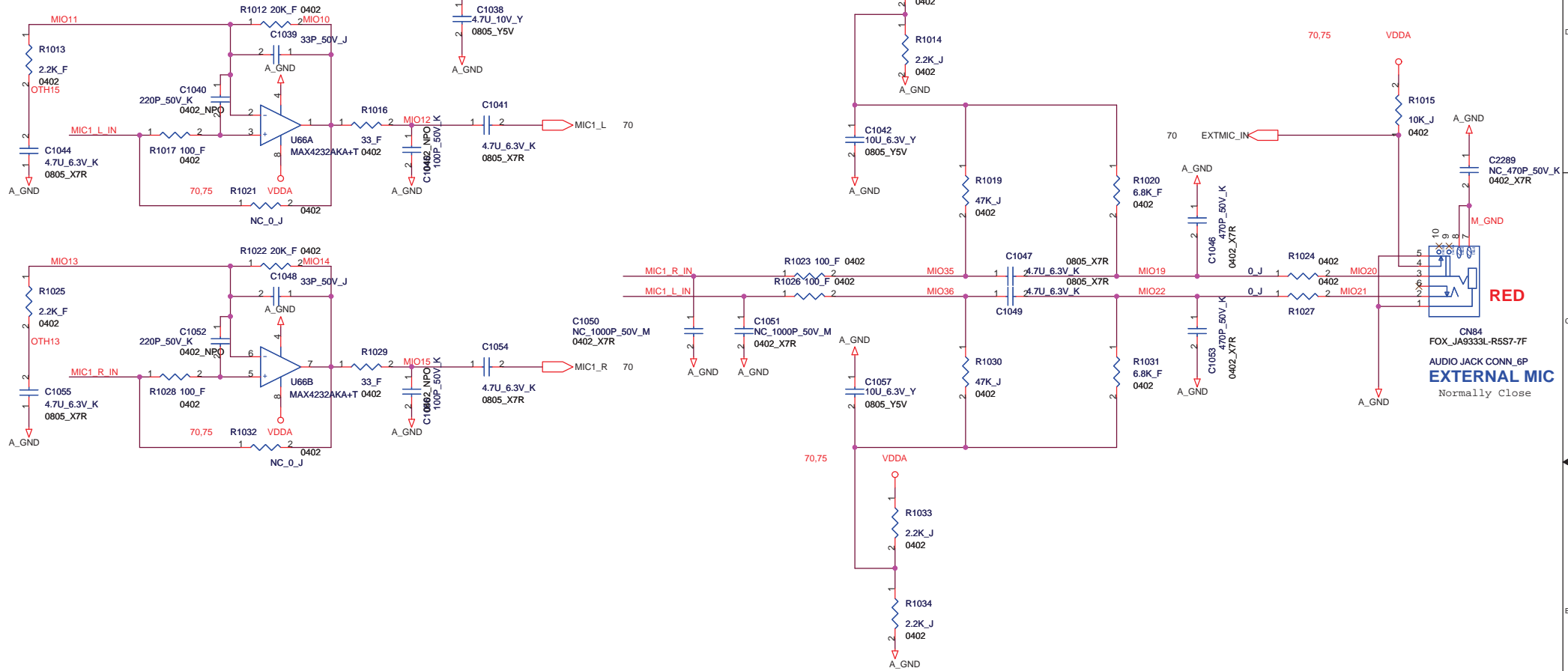


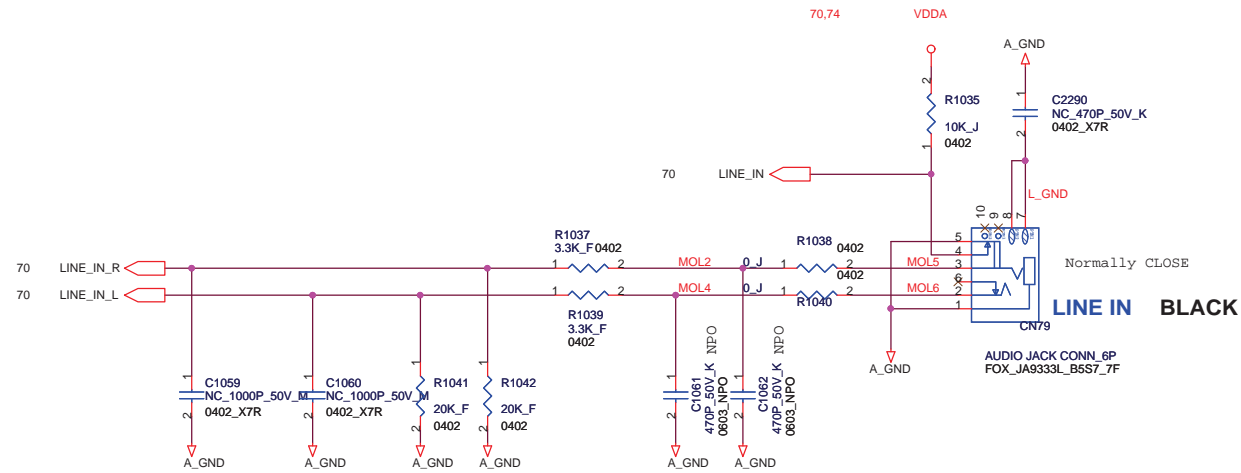




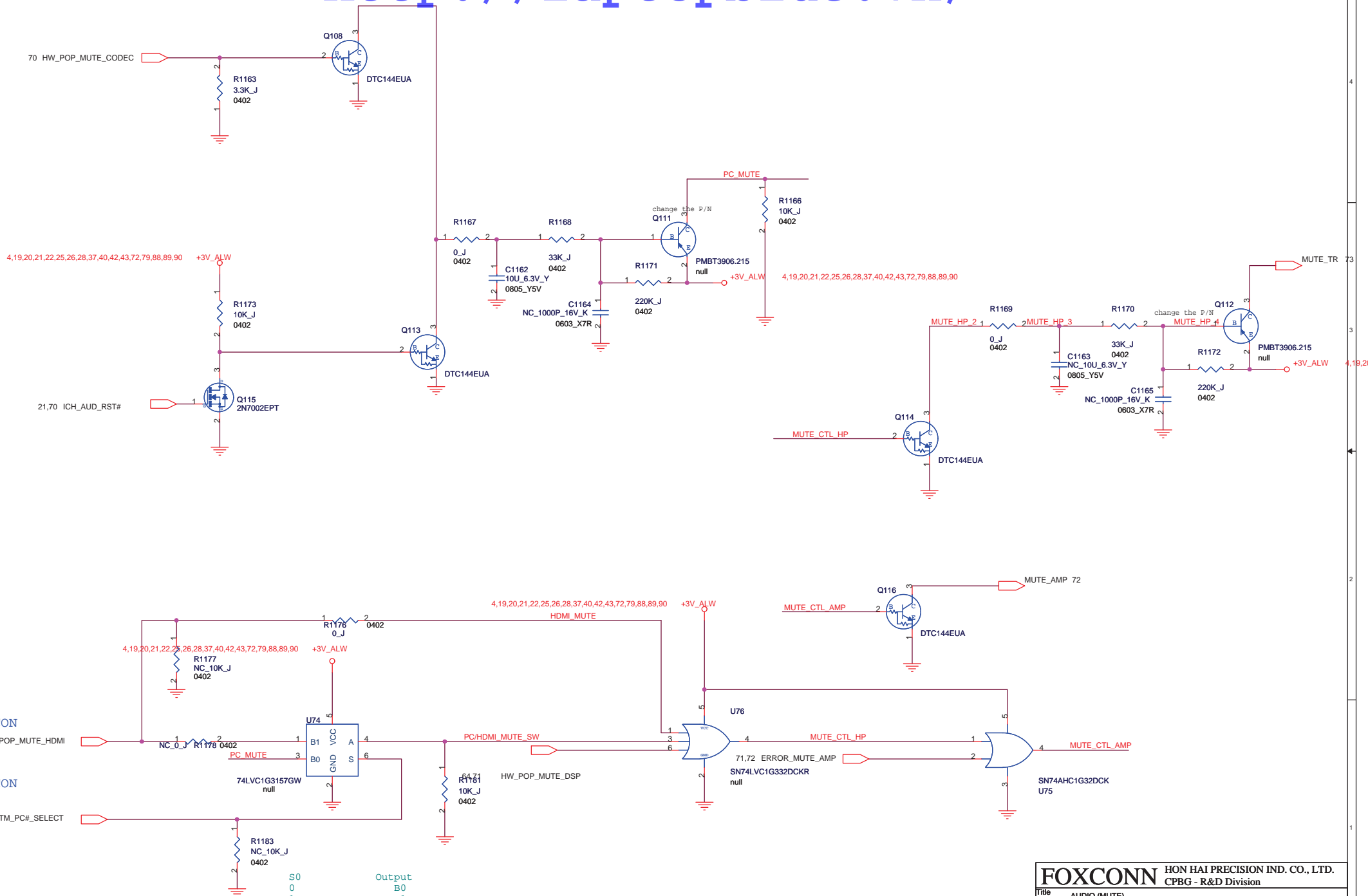
<http://laptopblue.vn/>







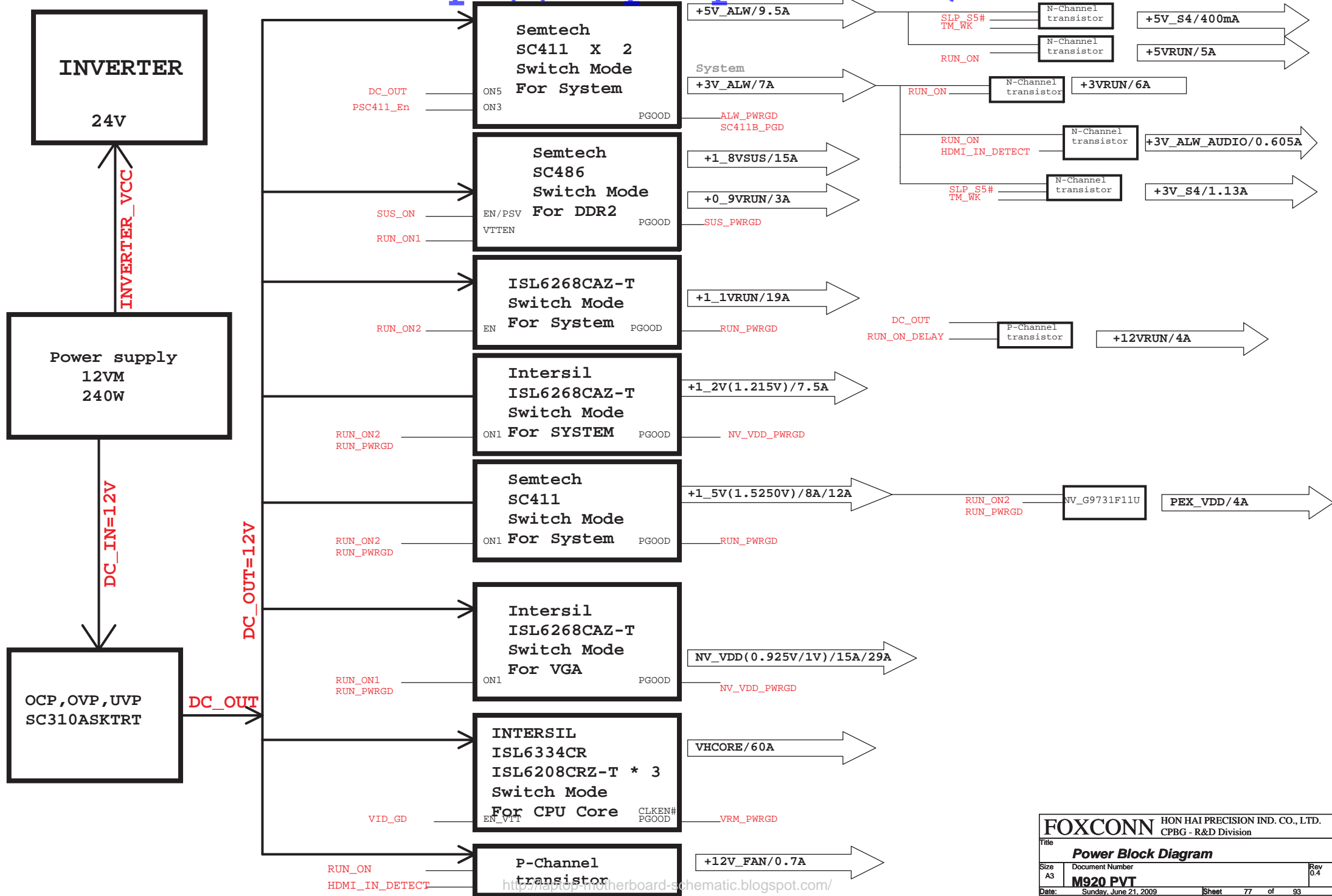
<http://laptopblue.vn/>



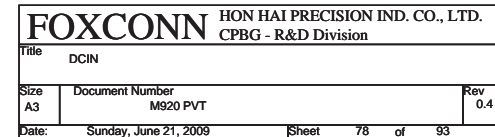
Output  
B0  
B1  
When HIDEIMI Mode ,HDMI/PC\_Select pin is " 1"  
When PC Mode , HDMI/PC\_Select pin is "0"

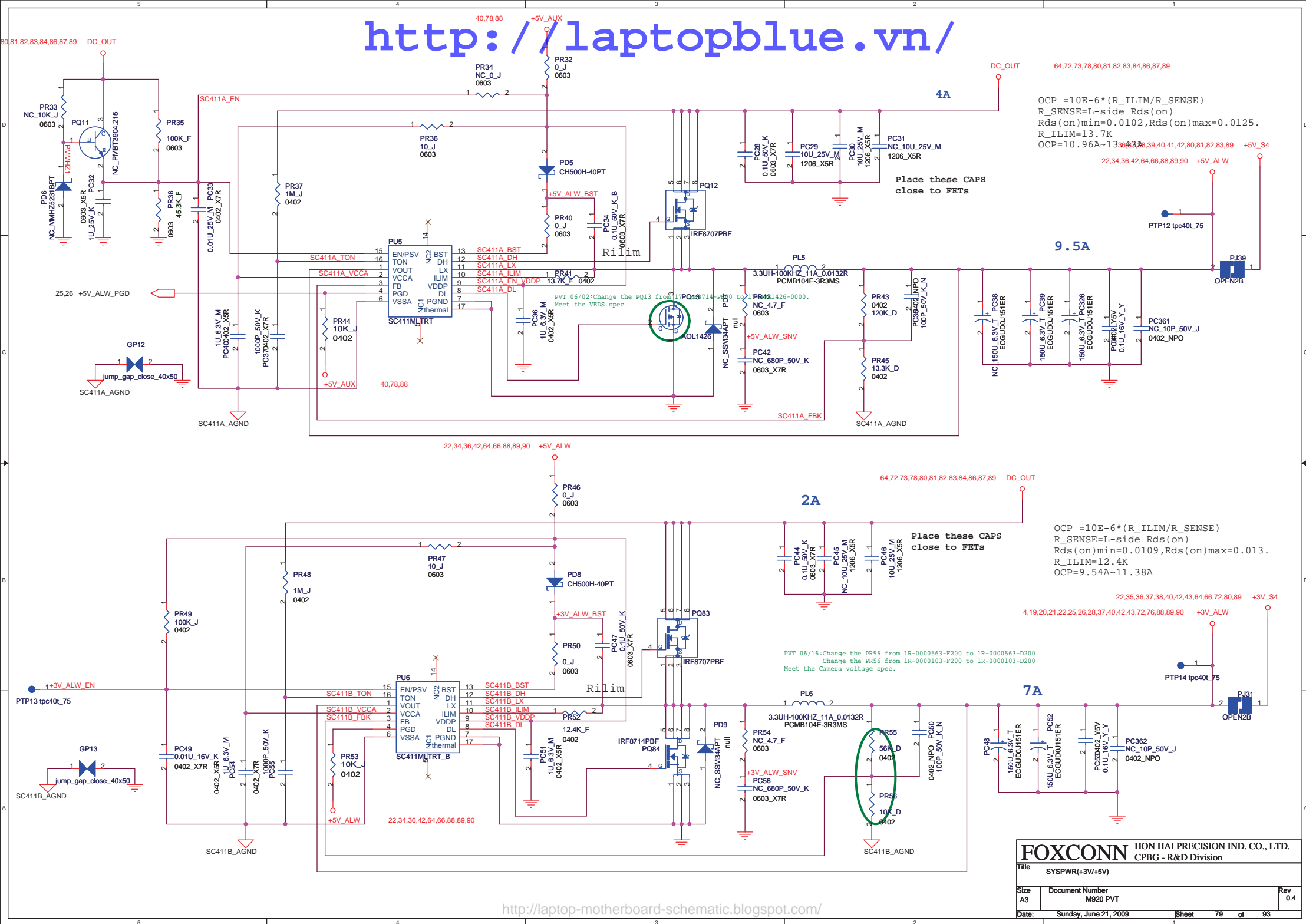
<http://laptop-motherboard-schematic.blogspot.com/>

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	AUDIO (MUTE)	
Size	Document Number	Rev
A3	M920 PVT	0.4
Date:	Sunday, June 21, 2009	Sheet 76 of 93



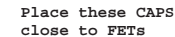






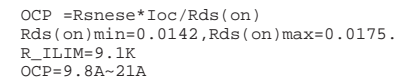


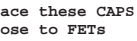
64,72,73,78,79,80,82,83,84,86,87,89 DC\_OUT 36,37,38,39,40,41,42,79,80,82,83,89 +5V S4



$OCP = R_{snes} \cdot I_{oc} / R_{ds(on)}$   
 $R_{ds(on)min} = 0.0038, R_{ds(on)max} = 0.0046.$   
 $R_{ILIM} = 4.7K$   
 $OCP = 19.4A \sim 40.8A$

```
06/19
change PQ18 from 17-A0L1426-0000 to 17-A0L1412-0000 and NC it
change PQ19 from 17-A0L1426-0000 to 17-A0L1412-0000
change PR77 from 1R-0007871-F200 to 1R-0000472-F200
```





## 10P OCP

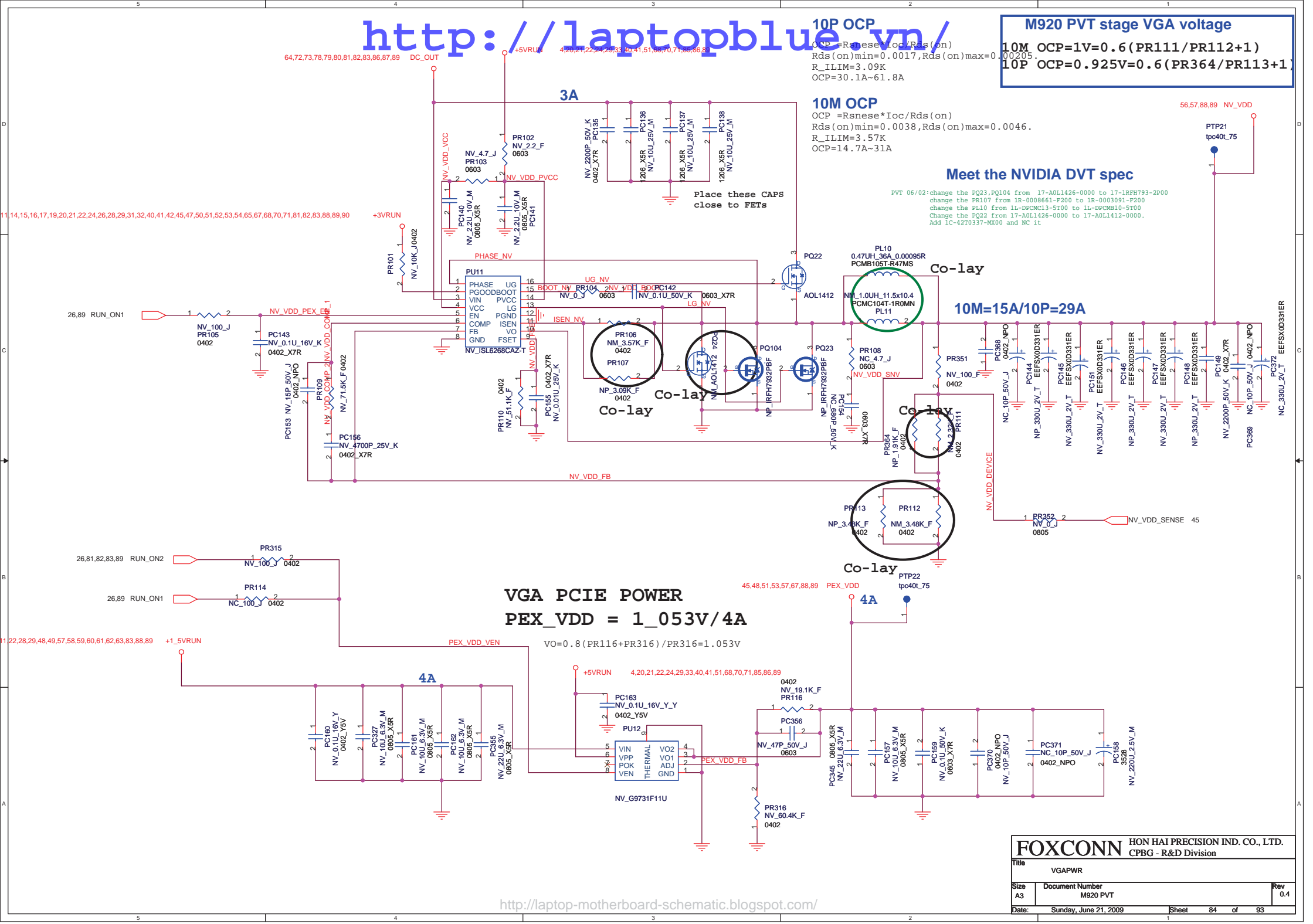
```
OCP = 10E-6*(R_ILIM/R_SENSE)
R_SENSE=L-side Rds(on)
Rds(on)min=0.0038,Rds(on)max=0.0046.
R_ILIM=6.81K
OCP=14.8A~17.9A
```

10M OCP

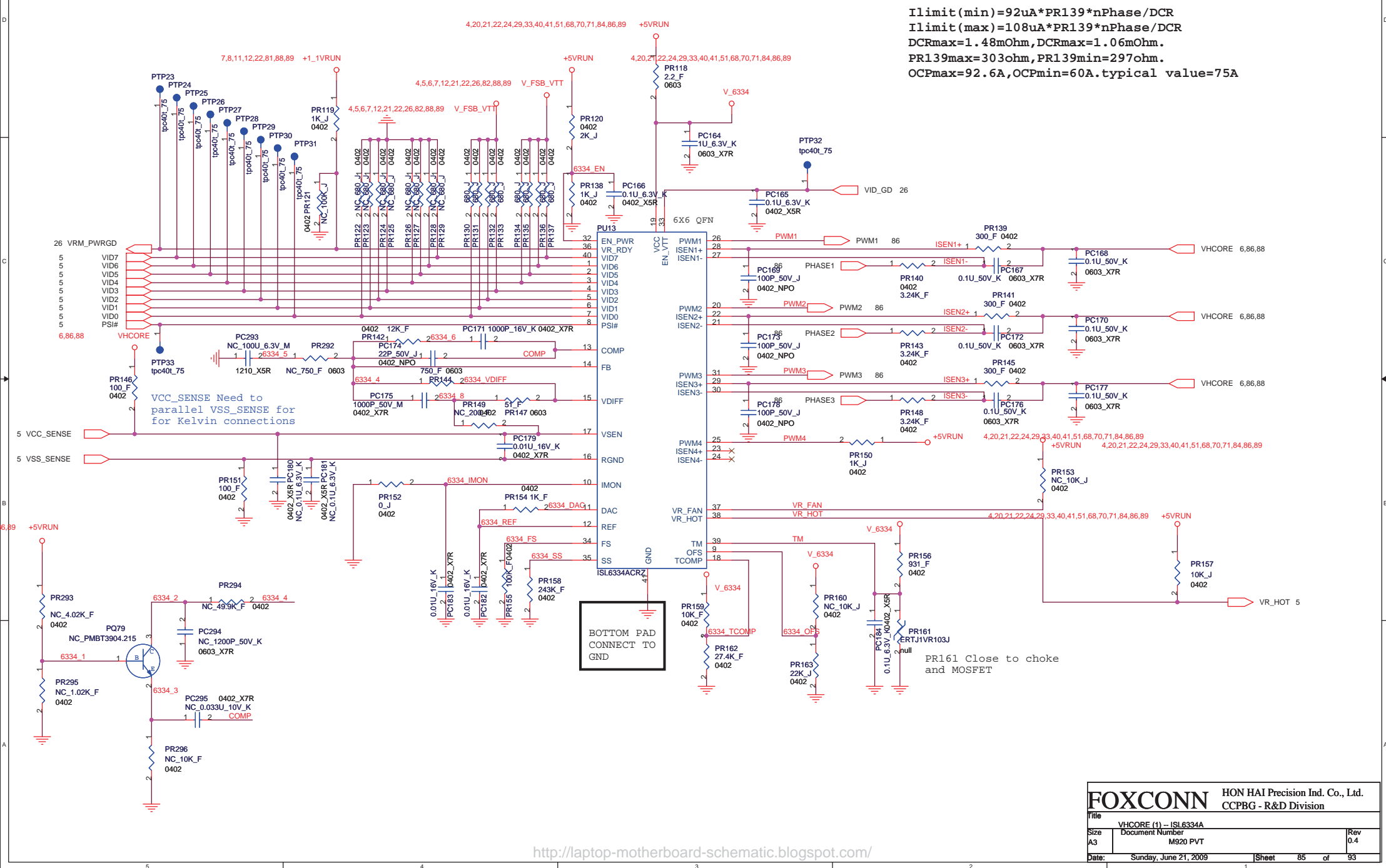
```
OCP = 10E-6*(R_ILIM/R_SENSE)
R_SENSE=L-side Rds(on)
Rds(on)min=0.0038,Rds(on)max=0.0046.
R_ILIM=4.3K
OCP=9.35A~11.32A
```

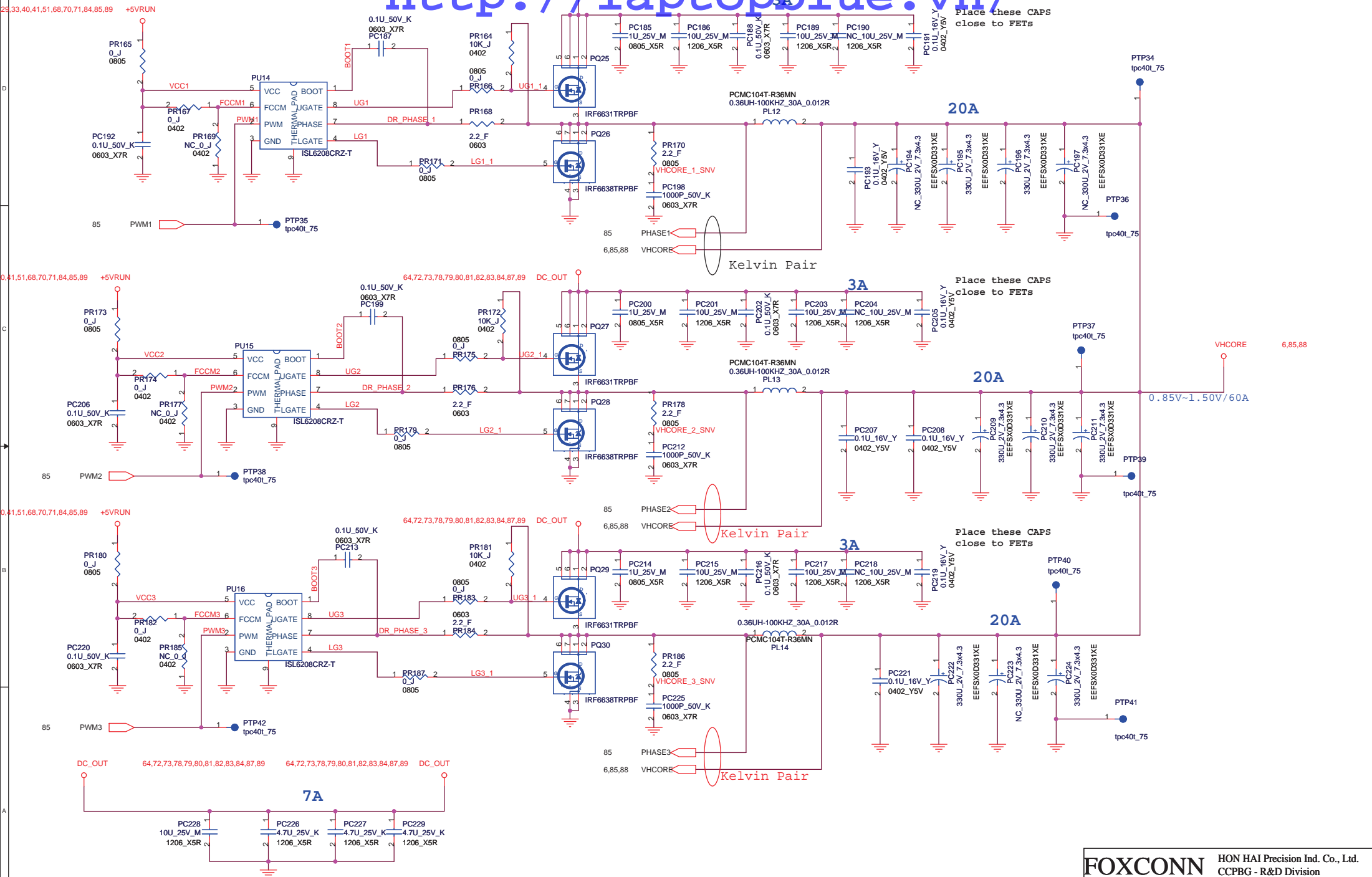
10M OCP=1V=0.6(PR111/PR112+1)  
10P OCP=0.925V=0.6(PR364/PR113+1)

<h1 style="margin: 0;">FOXCONN</h1>		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title <span style="float: right;">VGAPWR</span>			
Size	Document Number	Rev	
A3	M920 PVT		0.4
Date: Sunday, June 21, 2009		Sheet 84 of 93	

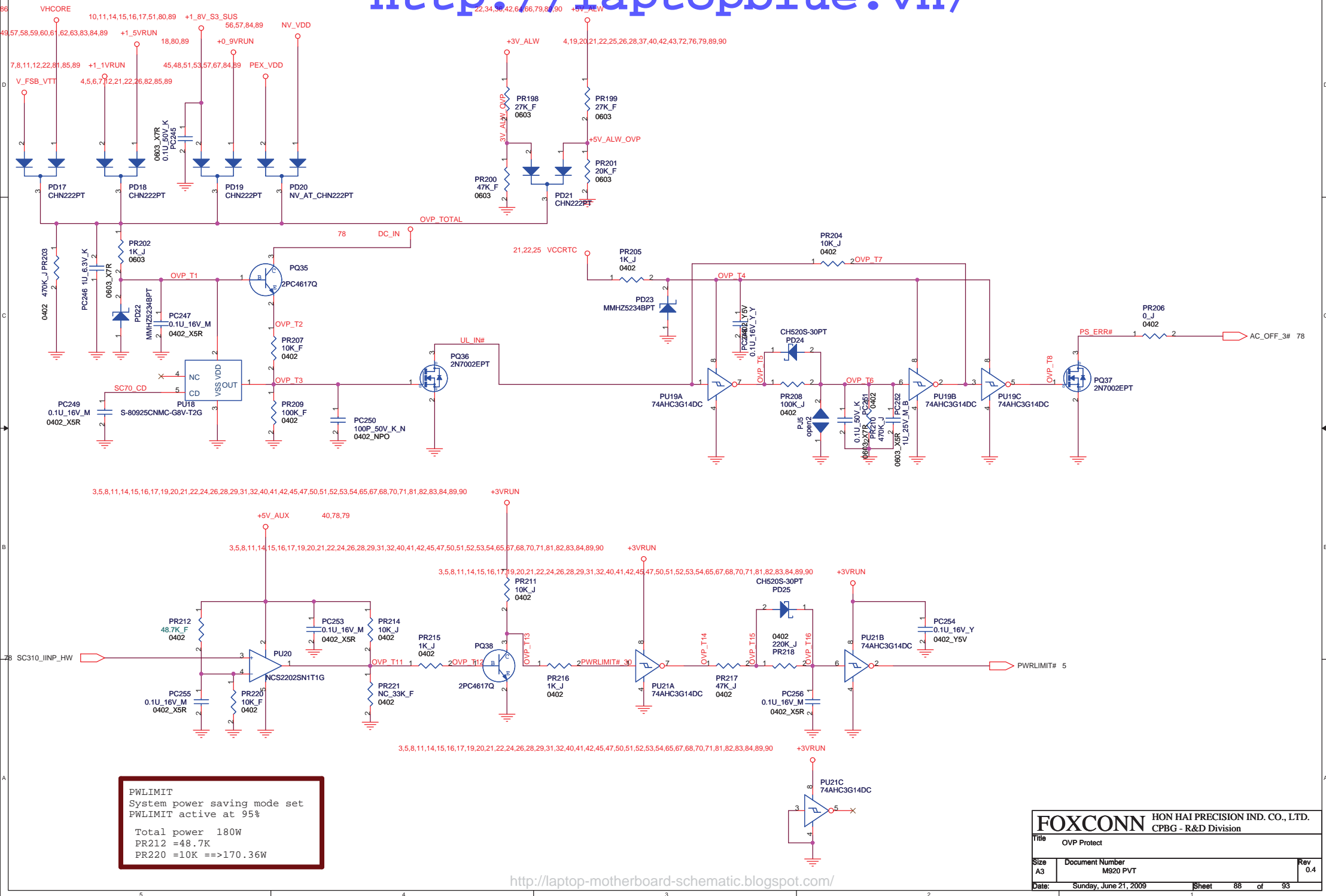


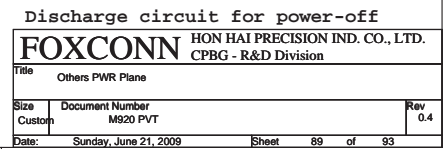




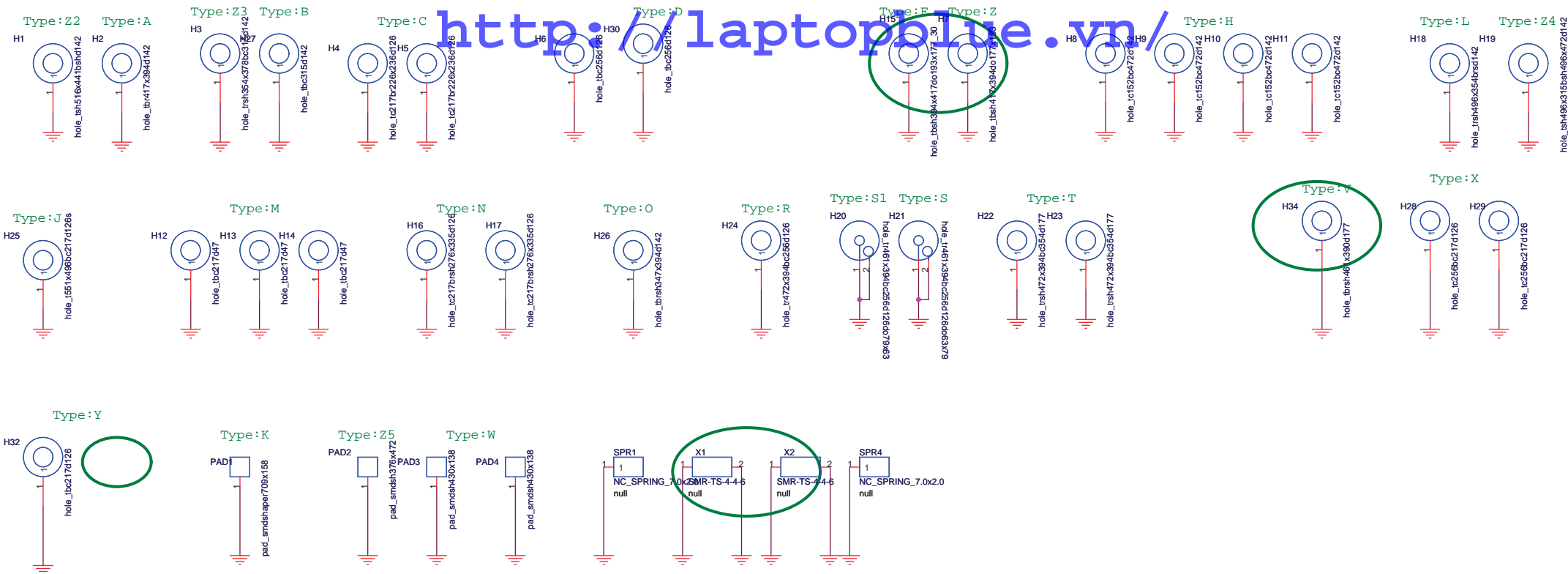




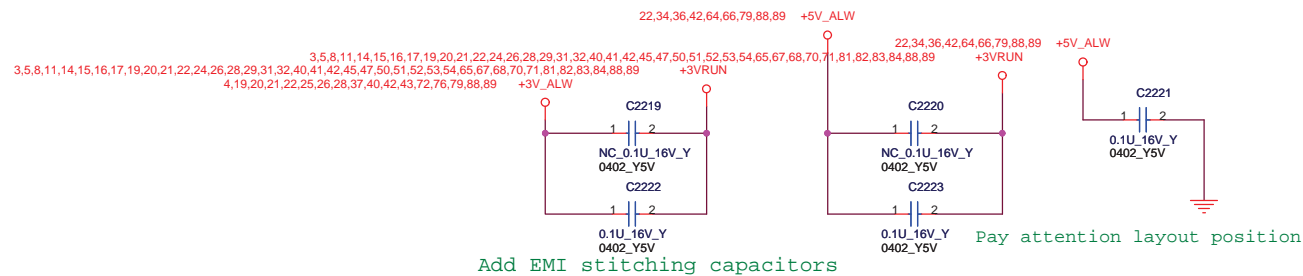




http://laptopblue.vn/



```
06/17 Change H15,H34 and H7 PAD Type for ME request
      ADD X1,X2 and Delete SPR2 and SPR3 for EMI and ME Request
06/20 Delete H35 for ME Request.
```



Blank Please

M920 Change History  
DVT stage

04/08  
EE Portion:  
Page 3, Change C1832 from 27pf to 30pf according to crystall match test  
Page 19, Stuff external SPI BIOS MB\_FLASH\_EN circuit for MOR request, this circuit will delete from PVT stage.  
Page 25, Change RSMRST# timing circuit the same as EVT1 circuit for MOR suggest.  
Page 29 Delete Debug component R492,R1994,C356,C357,C358,C359,C360,C361,C1342,  
Page 26, Change VRMPWVRGD delay circuit ,change net ' ICH\_VRMPWRGD' to ' VRM\_PWRGD\_U' for EVT2 schematic mistake  
Audio Portion:  
Page 72 Change cap21,cap22 from 1000u to 470u, Add CAP37,CAP38 470u at Power +8vAMP , Del NC\_R1057,NC\_R1058  
and connected net  
Page 73 and Page 75 change CN77 and CN79 from 2N-0006006-FKG0 to 2N-0006000-FKX0  
Page 74 change CN84 from 2N-0006002-FRG0 to 2N-0006000-FRX0  
Page 73&74&75 Add H\_GND,M\_GND and L\_GND for EMI request  
Page 73&74&75 Add C2288,C2289,C2290 470p CAP between H\_GND and A\_GND,M\_GND and A\_GND,L\_GND and A\_GND  
for EMI request  
Power Portion:  
Page 81 change the PQ17 from 17-A044680-0000 to 17-A0L1426-0000. for costdown failure item.  
Page 84 change the PQ22 from 17-A044680-0000 to 17-A0L1426-0000. for costdown failure item.  
Page 79 change the PR41 from 1R-0001432-F200 to 1R-0001372-F200. Meet the VEDS spec.

04/13  
EE Portion:  
Page 39 Delete R1396  
Page 34 ME request change USB connector CN26,CN27 color from gary to black,change PN  
from 2N-0004009-FEG0 to 2N-0004008-FEG0  
Page 90 For EMI Request,Mount SPR2 and SPR3  
Page 29 For EMI Request add GP22,GP23 between TV\_GND and GND

Audio Portion:  
Page 76 Delete NC\_R1175 for no use  
Page 72 Add 1 pcs 0.1U cap and mount C1088,C1079 cap for EMI request.

04/15  
EE Portion:  
Page 14 Change R209,R208 from 1R-0000102-F200 to 1R-0000102-D200 for improve the VREF margin  
Page 16 Change R217,R218 from 1R-0000102-F200 to 1R-0000102-D200 for improve the VREF margin  
Page 42 NC R2047,LED3 For MOR request

04/16  
Power Portion:  
Page 81 Change the PR77 from 1R-0000822-F200 to 1R-0007871-F200  
Page 84 Change the PR112 from 1R-0004641-F200 to 1R-0003481-F200  
Change the PR113 from 1R-0004641-F200 to 1R-0003481-F200  
Change the PR364 from 1R-0002321-F200 to 1R-0001911-F200  
Change the PR106 from 1R-0003091-F200 to 1R-0003571-F200

Page 85 For Vcore intel spec change as below:  
Change the PR144 from 1R-0008250-F300 to 1R-0000751-F300  
Change the PR140,PR143,PR148 from 1R-0000472-F200 to 1R-0003241-F201  
Change the PR142 from 1R-0000203-F200 to 1R-0000123-F200  
Change the PC175 from 1C-2B20681-K000 to 1C-2N20102-J600  
Change the PR147 from 1R-0000201-F200 to 1R-0000510-F300

Page 86 Change the PC194 from 1C-42T0337-MX02 to NC  
Change the PC197 from 1C-42T0337-MX02 to NC  
Change the PC223 from 1C-42T0337-MX02 to NC  
Change the PR182 from NC to 1R-0000000-J200  
Change the PR185 from 1R-0000000-J200 to NC  
Change the PR174 from NC to 1R-0000000-J200  
Change the PR177 from 1R-0000000-J200 to NC  
Change the PR167 from NC to 1R-0000000-J200  
Change the PR169 from 1R-0000000-J200 to NC

04/17  
EE Portion:  
Page 20 Stuff for MOR request ,it will be NC at PVT stage.  
Page 35 Delete CN89,R2061,R2062 ,2042,2043for desgin change.This connector and resister is no use .  
Page 36 Delete R577,C2128,IR\_BLAster for MOR reconment.  
Page 29 Delete R2092 ,R2093 and net VIDEO\_COMP1 because AV IN board be canceled  
Page 30 Delete all AV\_IN function for MOR request  
Page 42 Add TP594 For L6 TEST

Audio Portion:  
Page 72 change C1100,C1101,C2291 from 0.1U cap to 0.01u cap for MOR request.  
change C1088,C1079 ,C1089,C1099 to 470p cap for mor request, and mount C1089,C1099.

http://laptopblue.vn/

04/18  
EE Portion:  
Page 42 Stuff R2086 and R2105 ,NC R2104 and R2106 for MOR request

04/19  
Power Portion:  
Page 83 change the PQ86 from 17-1RF8714-PB00 to 17-A0L1412-0000  
change the PR341 from 1R-0000183-F200 to 1R-0006811-F200  
change the pr350 from 1R-0001372-F200 to 1R-0000432-F200

Page 84.change the pc144 from NC to stuff  
change the pc146 from NC to stuff

Page 89 add the 12V\_fan discharge circuit.

04/20  
EE Portion:  
Page 29 Change AV\_IN\_GND TO TV\_GND due to AV\_IN/IR Function have been canceled.  
Page 40 NC CN37,C523,C497 for thermal suggest

PVT stage

06/02  
Power Portion:  
Page 79 Change the PQ13 from 17-1RF8714-PB00 to 17-A0L1426-0000. Meet the VEDS spec.  
Page 83. Stuff the PR343 (1R-0000103-F200)in PVT stage.for VGA requirement  
Page 84 Change the PQ23,PQ104 from 17-A0L1426-0000 to 17-1RFH793-2P00  
Change the PR107 from 1R-0008661-F200 to 1R-0003091-F200  
Change the PL10 from 1L-DPCMC13-5T00 to 1L-DPCMB10-5T00  
Change the PQ22 from 17-A0L1426-0000 to 17-A0L1412-0000.  
Add 1C-42T0337-MX00 and NC it .for NVIDIA requirement in PVT stage.

EE Portion:  
Page 32 Change CN50 From 1N-1014000-0000 to 1N-1014002-0000 For vendor change material.  
Page 36 Add R2111 1K to pull up for Tiramisu suggestion  
Page 29 Delete CN69,R1847,R1957,R1958,R1959,R1960,R1961.

Audio Portion:  
Page 73 Delete C2287, add Cap39 The cap for audio in circuit debug and mor request  
Chang C2022,C2023,C2026,C2027 from 1C-2Y30225-Y000 to 1C-2B30475-K100 for DVT ECN

06/10  
EE Portion: Page 20 Add R2118,R2119 and Q185 this portion circuit for system leakgea issue  
Page 36 NC R1891 and R700,the TM\_RX\_CN not use  
Page 20 NC CN5,we will use GPIO24 to contorl FLASH\_STRAP\_SB  
Page 19 NC R264,R265,Q9 Confirmed with our SW members, we don't use this function, so we can delete it.  
Page 42 NC R680,R679 and SW3 for PVT/MP do not use CRT  
Page 29 Change L17 from 1L-BT11608-0800 to 1L-BACMS16-080A for power consumption  
Page 27 Change CN9 from 2N-000800F-FKN0 to 2N-0008001-FKN0 for package changed

06/15  
EE Portion: Page 19 Add R2120 to boot the pc from external spi card or internal spi rom  
Page 27 Change C2161 From 1C-2B20104-K000 to 1C-2N20050-D000 for EMI Request

06/17  
Audio Portion: Page 71 Change R1271,R1272 From 1R-0000472-J200 to 1R-0000222-J200 for tiramisu I'C bus test  
Power Portion:  
1.Page 79. Change the PR55 from 1R-0000563-F200 to 1R-0000563-D200  
Change the PR56 from 1R-0000103-F200 to 1R-0000103-D200 Meet the Camera voltage spec.  
2.Page 81 and Page 84,change the power budget value.

EE Portion: Page 40 Add +3VALW as another power source for SMSC VCC  
Page 41 Add C2295 on Fan3 Tach for EMI request.  
Page 36 NC R2111 pull up resistor,because IR receiver have internal pull up.  
Page 90 Change H15,H34 and H7 PAD Type for ME request  
Page 90 ADD X1,X2 and Delete SPR2 and SPR3 for EMI and ME Request

06/19  
Power Portion:  
Page 81. change PQ18 from 17-A0L1426-0000 to 17-A0L1412-0000 and NC it  
change PQ19 from 17-A0L1426-0000 to 17-A0L1412-0000  
change PR77 from 1R-0007871-F200 to 1R-0000472-F200

EE Portion: Page 27 Change C315 and C316 from 1C-2N20150-J000 to 1C-2N20330-J000 for crystal test result  
Page 31 Change R1340 and R1341 from 10K\_J to 4.7K\_J for Vendor suggestion

06/21  
EE Portion:  
Page 41 Use GPIO solution for QST Fan spin-up noise issue(Mount Q177,Q178,Q179,R2101,R2081,R2099,  
R2102,R2082,R2100,R2103,R2080,R2098, NC R2070,R2078,R2071,R2079,R2104)  
Page 41 Mount R2063 (GPIO 7 need to pull low)  
Page 40 Mount R1800 (GPIO 19 need to pull low)  
Page 20 NC R295,R276 (GPIO19 ,GPIO7 need to pull low)

Power Portion: Page 79. Reserve PC373,PC374,PC375,PC376,PC377,PC378,PC379

FOXCONN

HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title <b>Change History</b>		
Size 43	Document Number <b>M920_PVT_Noise</b>	Rev <b>0.4</b>
Date Sunday, June 21, 2009	Sheet 91	of 93

http://laptop-motherboard