

Compal confidential

Schematics Document

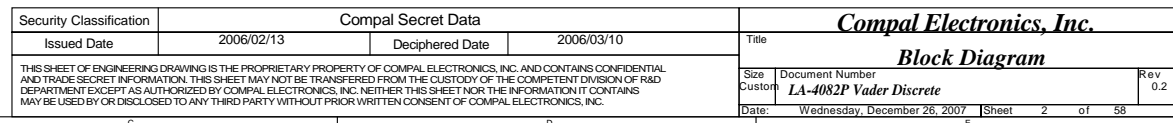
Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

LA-4082P Vader Discrete (NB9P-GS,NB9M-GE)

2007-12-26 Rev 0.4



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	Cover Sheet	
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power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB assignment:
USB-0 Right side
USB-1 Right side
USB-2 Left side(with ESATA)
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express
USB-10 X
USB-11 X

PCIe assignment:
PCIe-1 TV tuner/WWAN/Robeson
PCIe-2 X
PCIe-3 WLAN
PCIe-4 New Card
PCIe-5 Card
PCIe-6 GLAN (Marvell)

Symbol Note :
 : means Digital Ground
 : means Analog Ground
@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

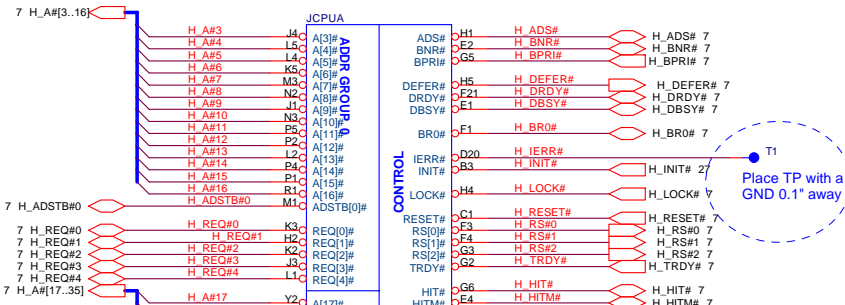
EC SM Bus1 address			EC SM Bus2 address		
Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD – Cypress	38H				
CAP BOARD – ST	b0H				

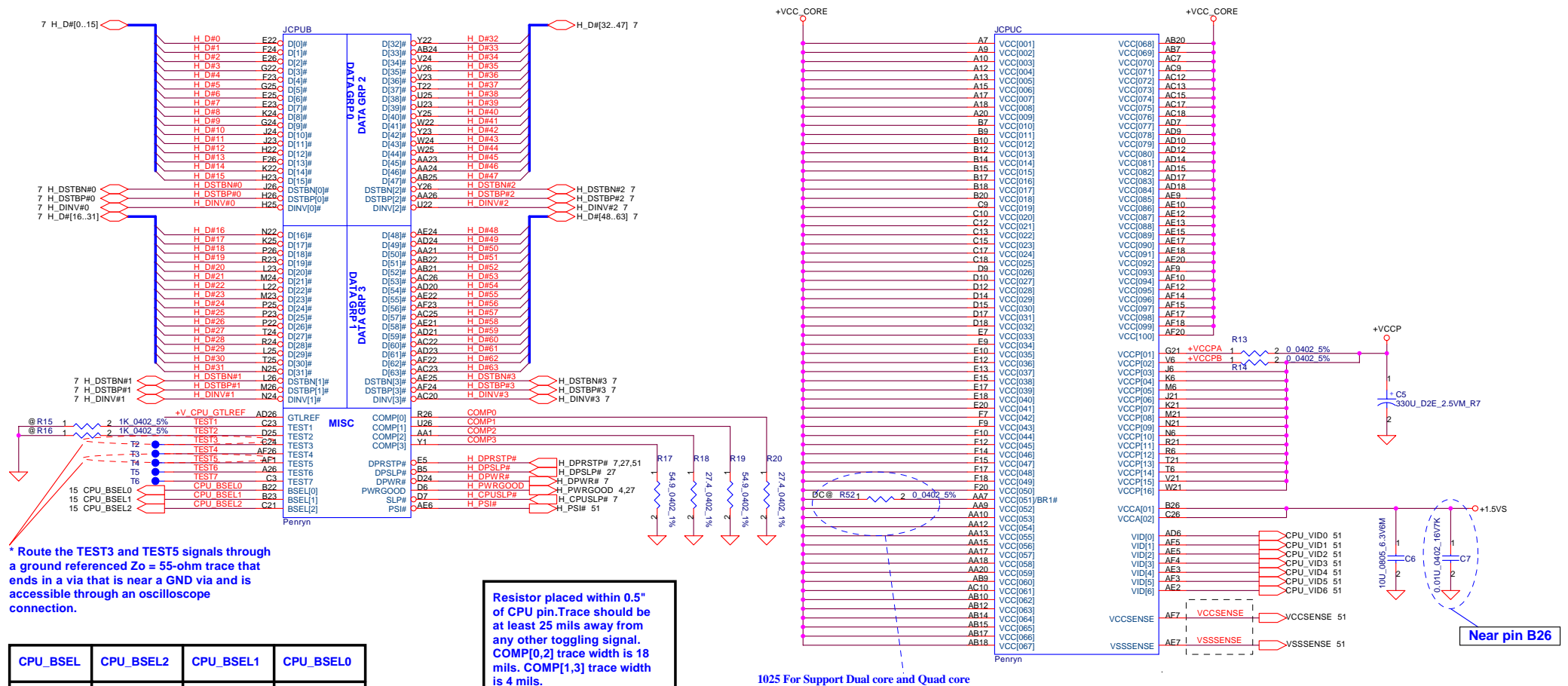
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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ITP-XDP Connector

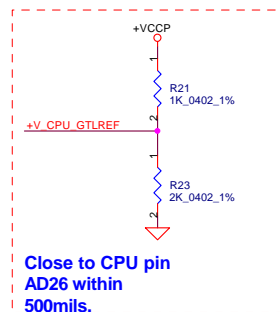




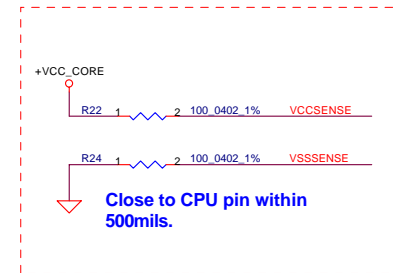
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

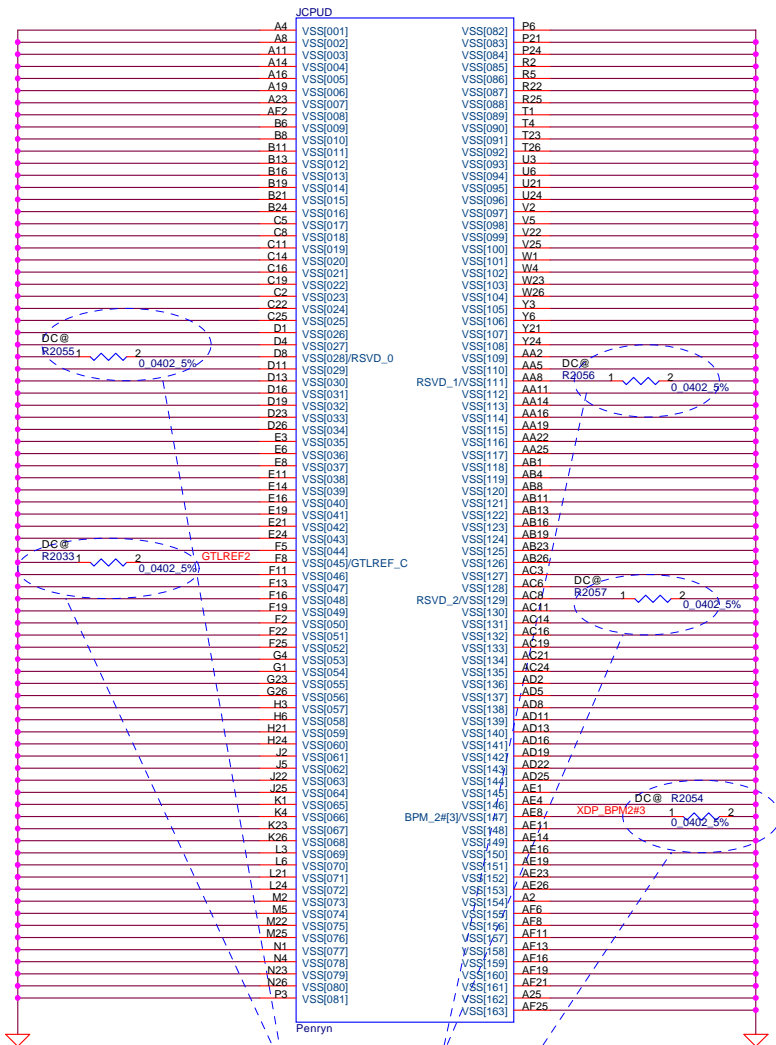
1025 For Support Dual core and Quad core



Length match within 25 mils.
The trace width/space/other
is 20/7/25.

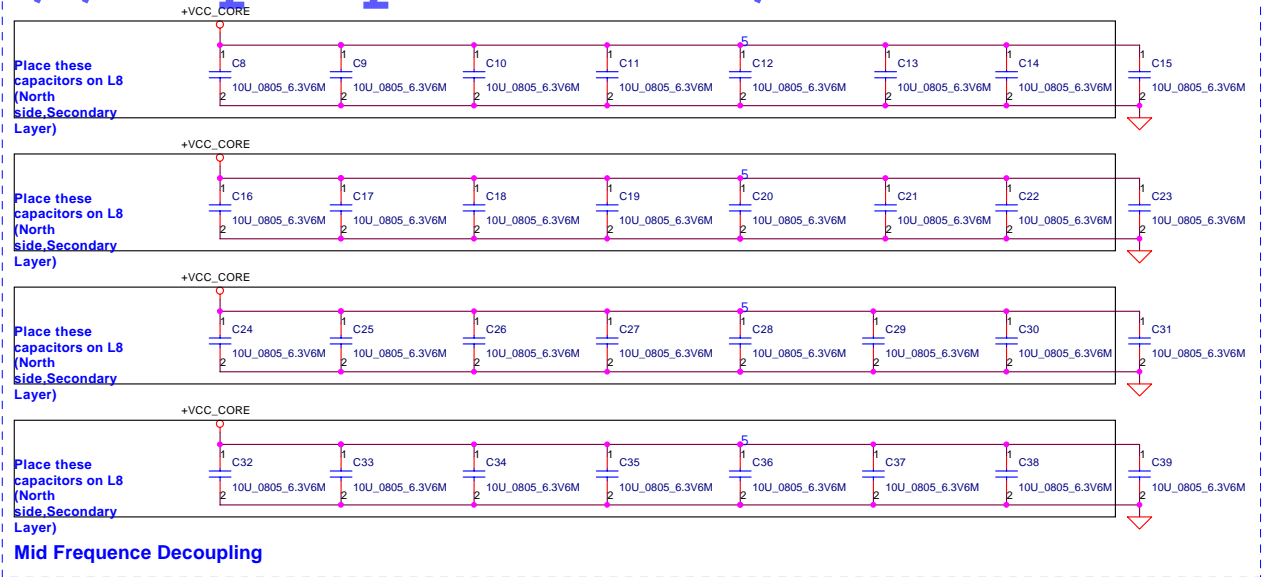


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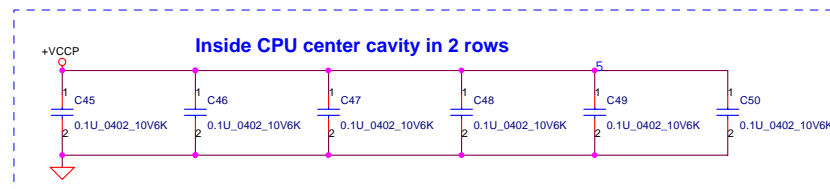
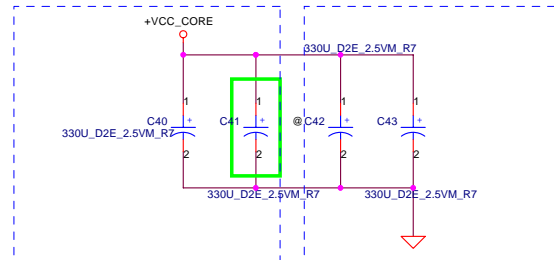
1025 For Support Dual core and Quad core

GTLREF2 → GTLREF2 4
XDP_BPM2#3 → XDP_BPM2#3 4

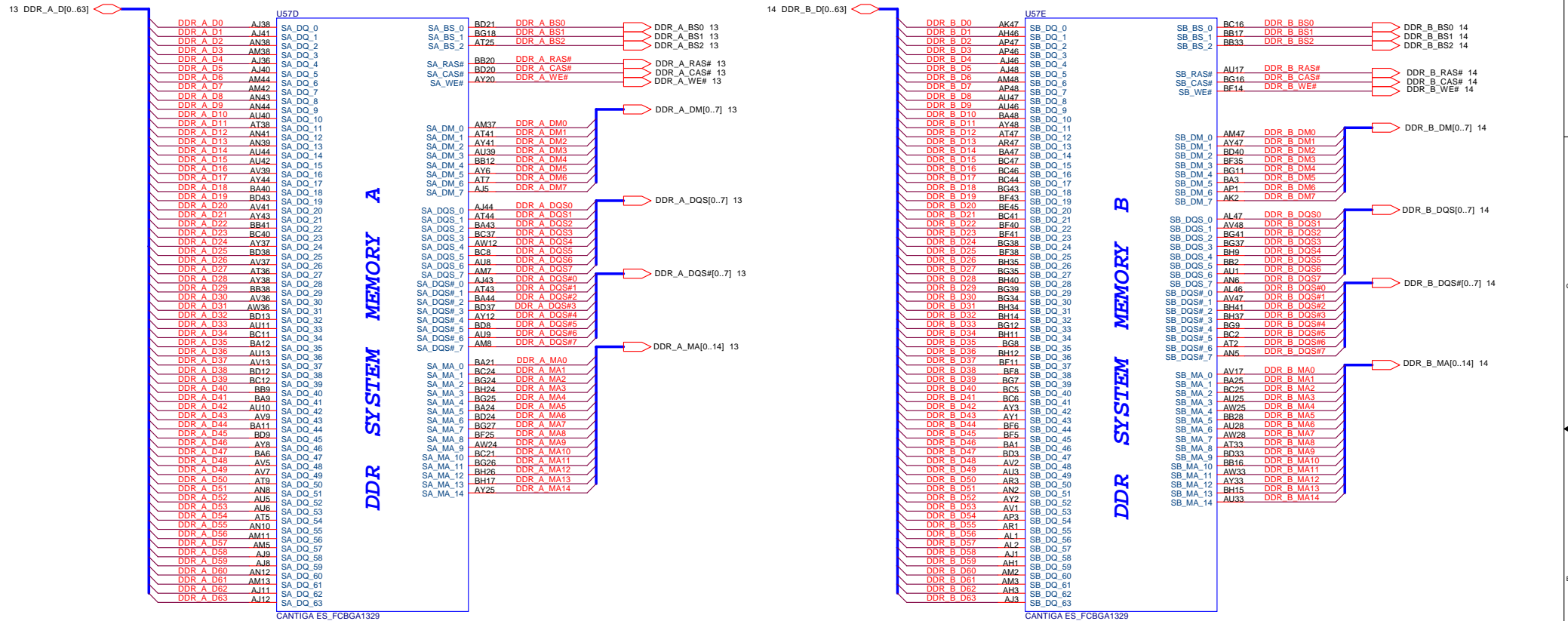


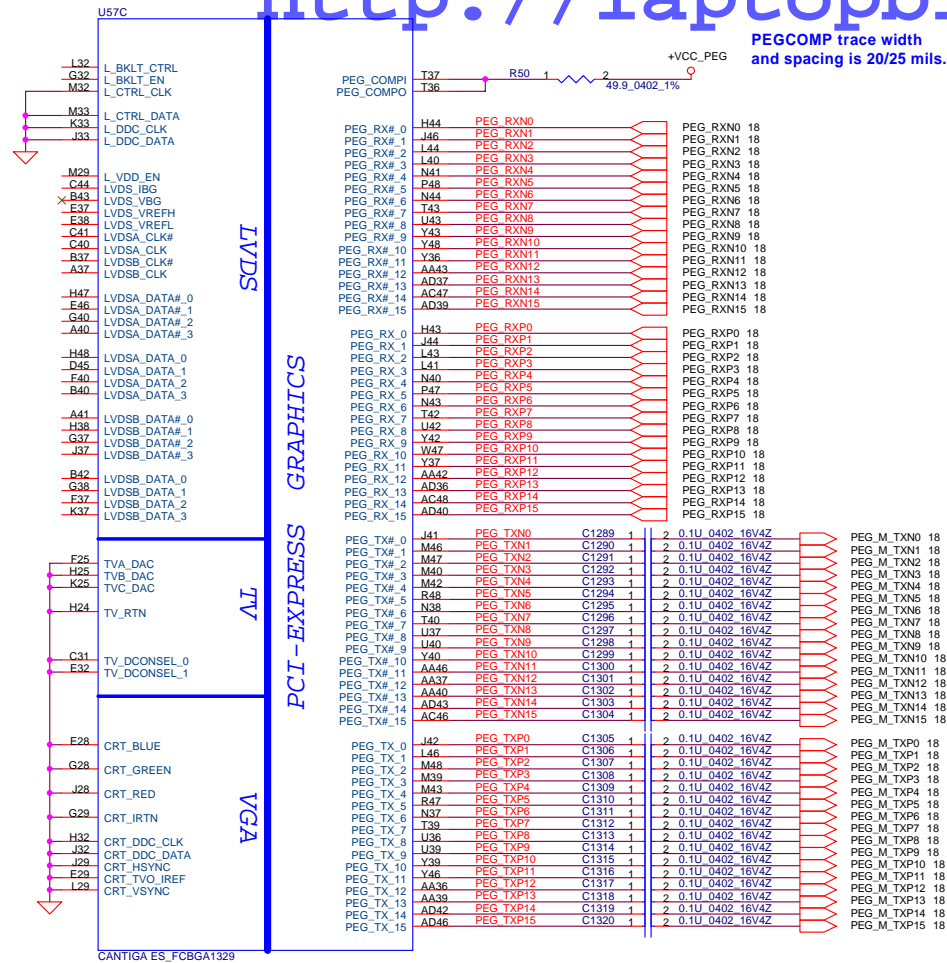
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



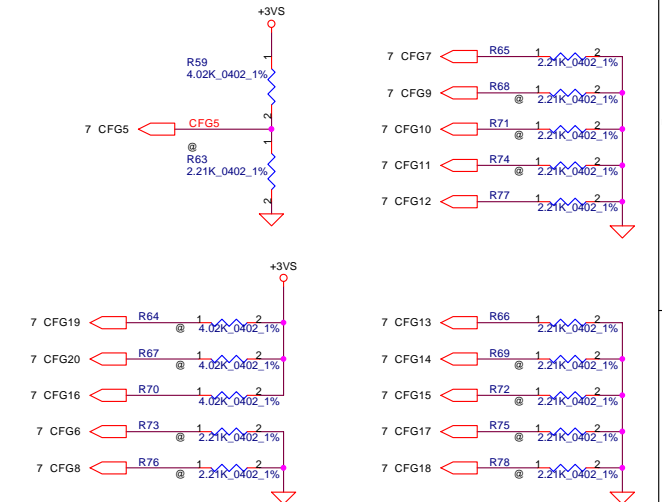
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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *

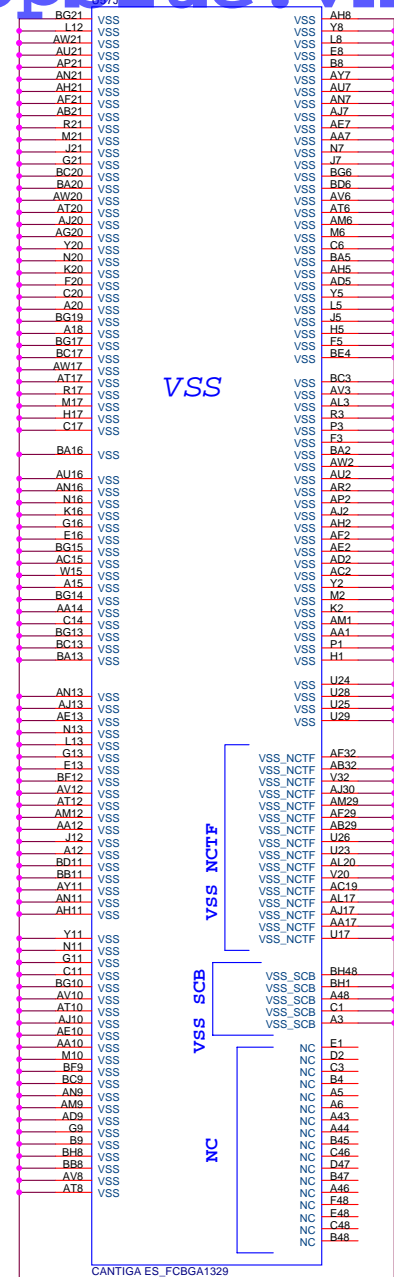
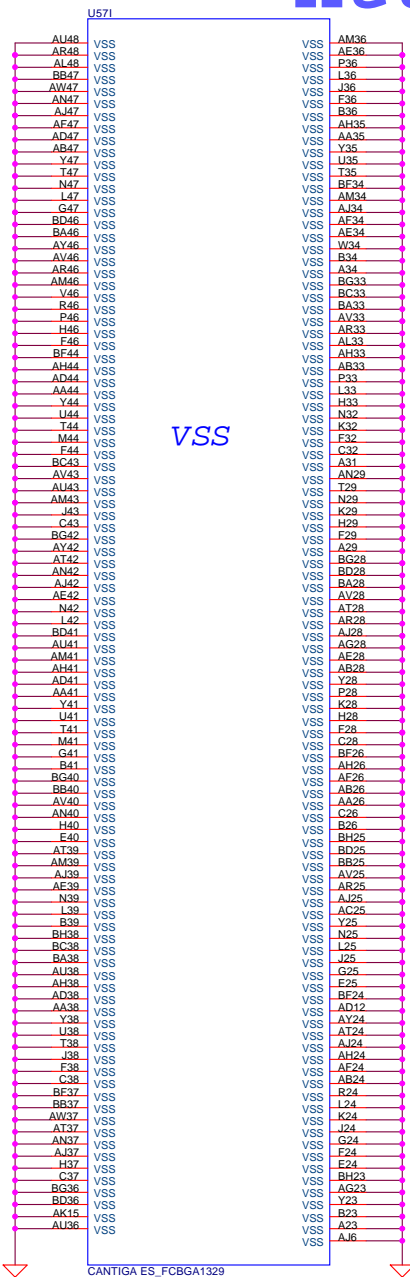


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Extl Graphic: 1210.34mA
integrated Graphic: 1930.4mA

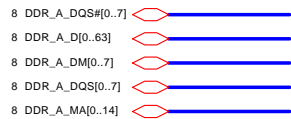


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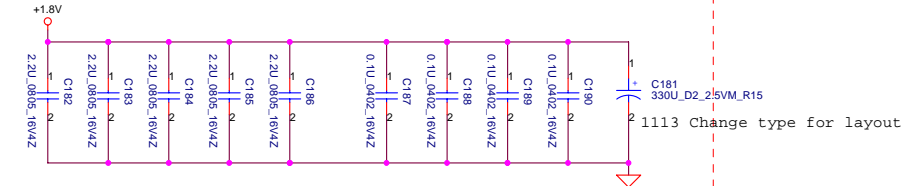


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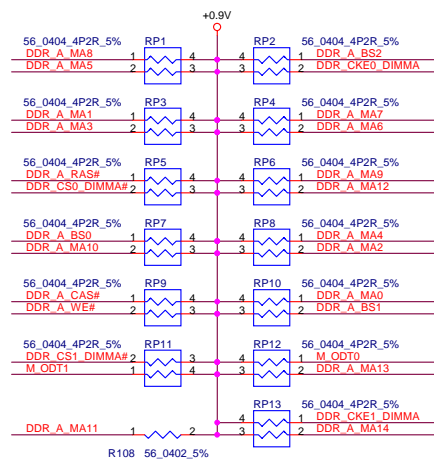
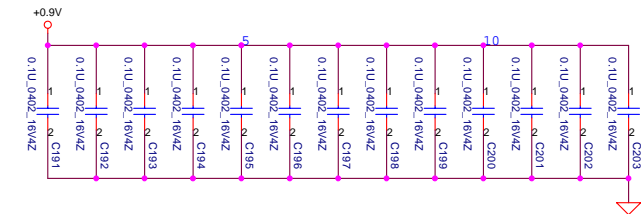
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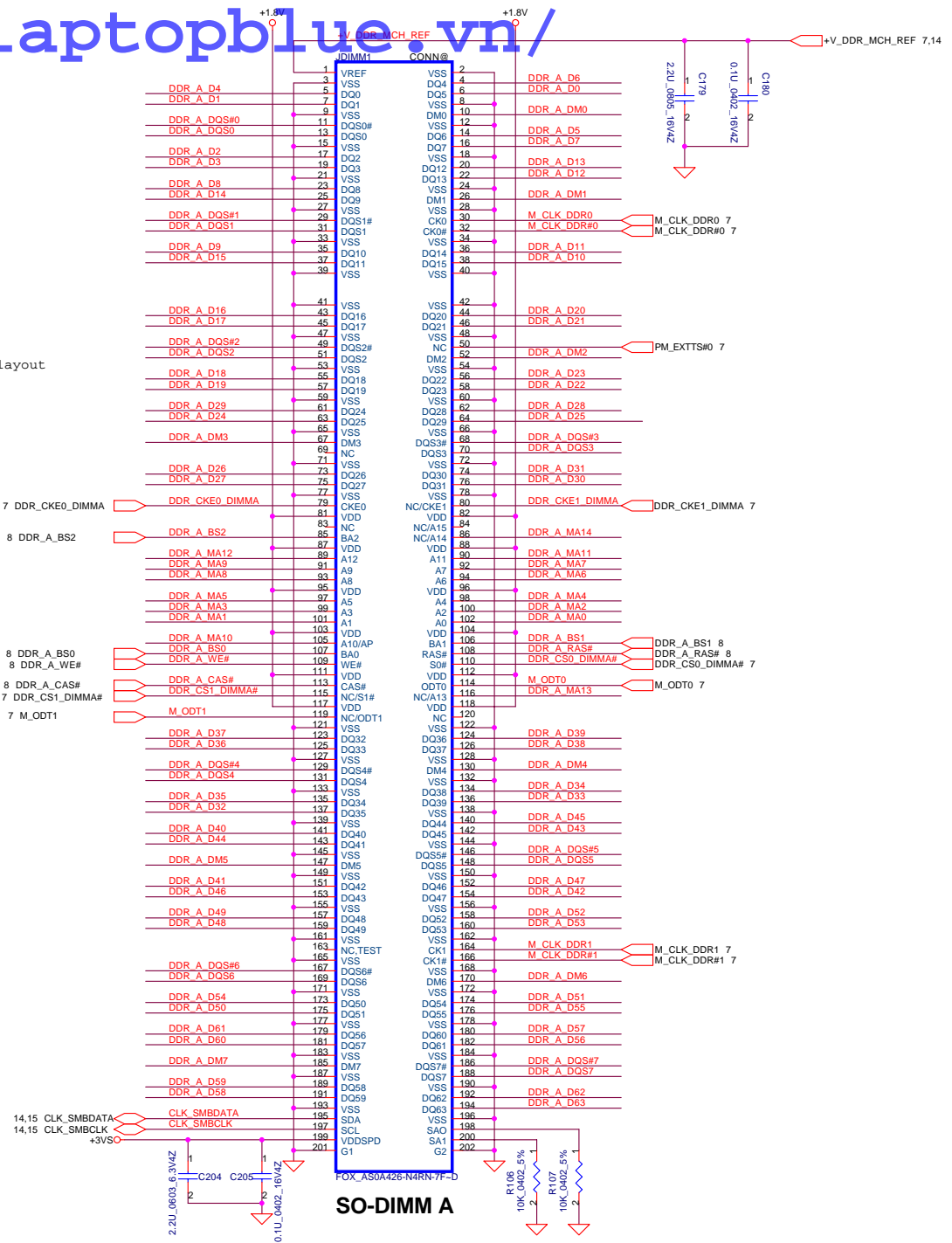
Layout Note:
Place near
JP3



Layout Note:
Place one cap close to every
2 pullup
resistors terminated to +0.9VS

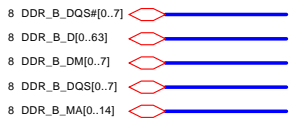


Layout Note:
Place these resistor
closely JP3,all
trace length Max=1.5"

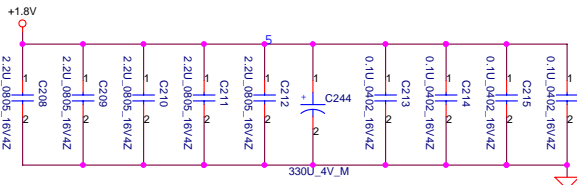


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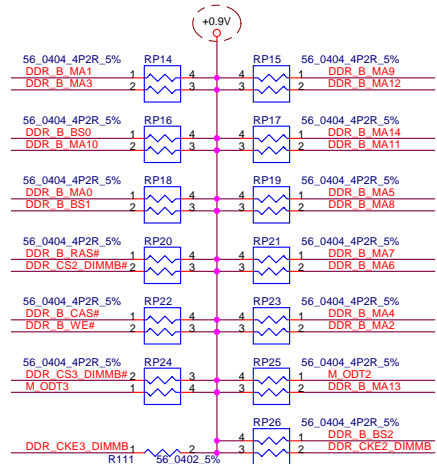
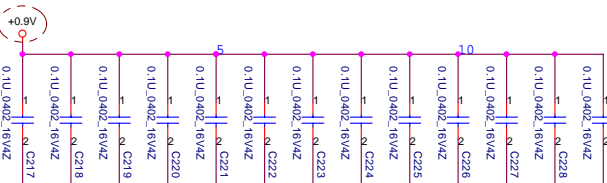
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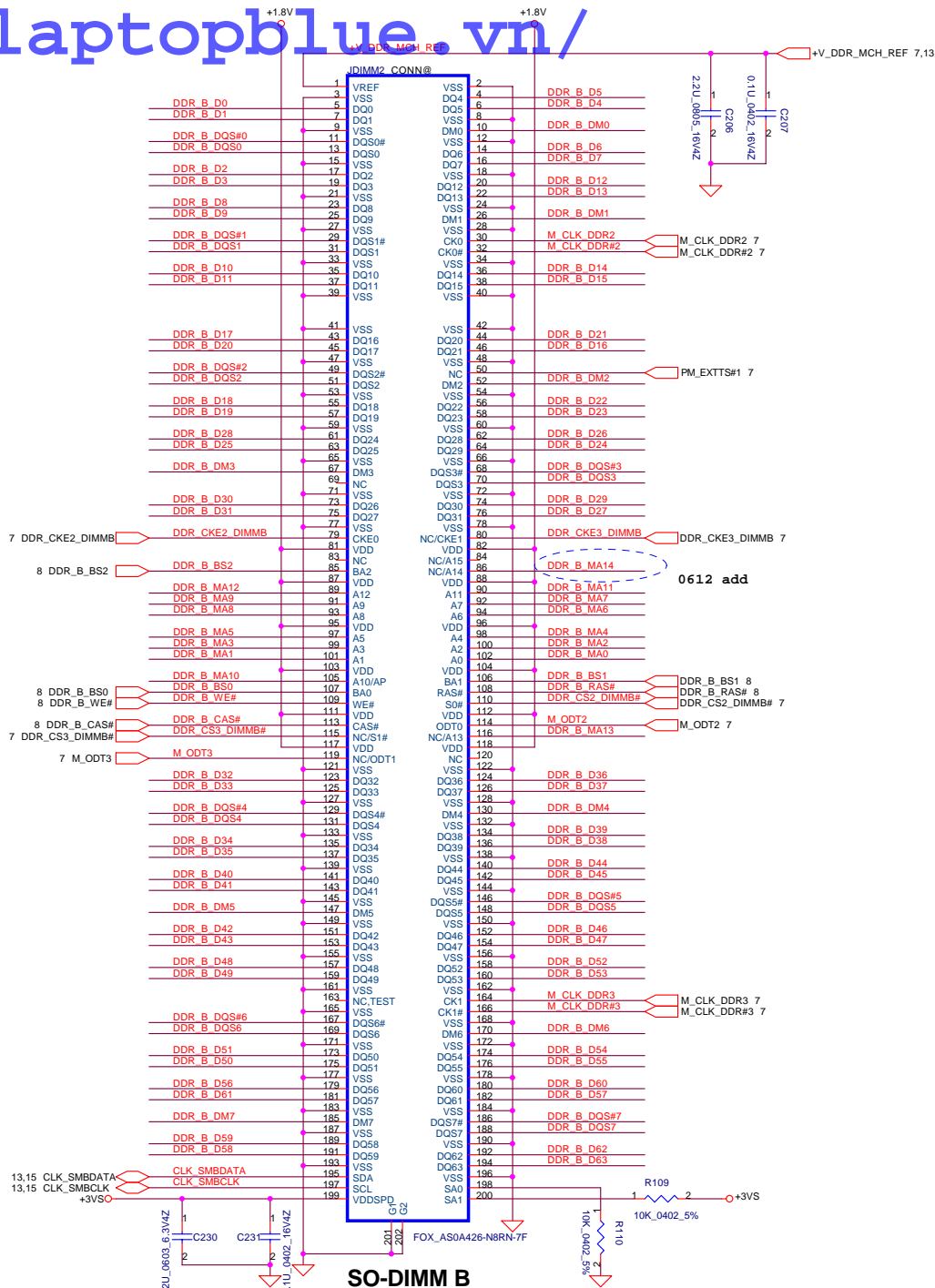
Layout Note:
Place near
JP10



Layout Note:
Place one cap close to every
2 pullup
resistors terminated to +0.9VS



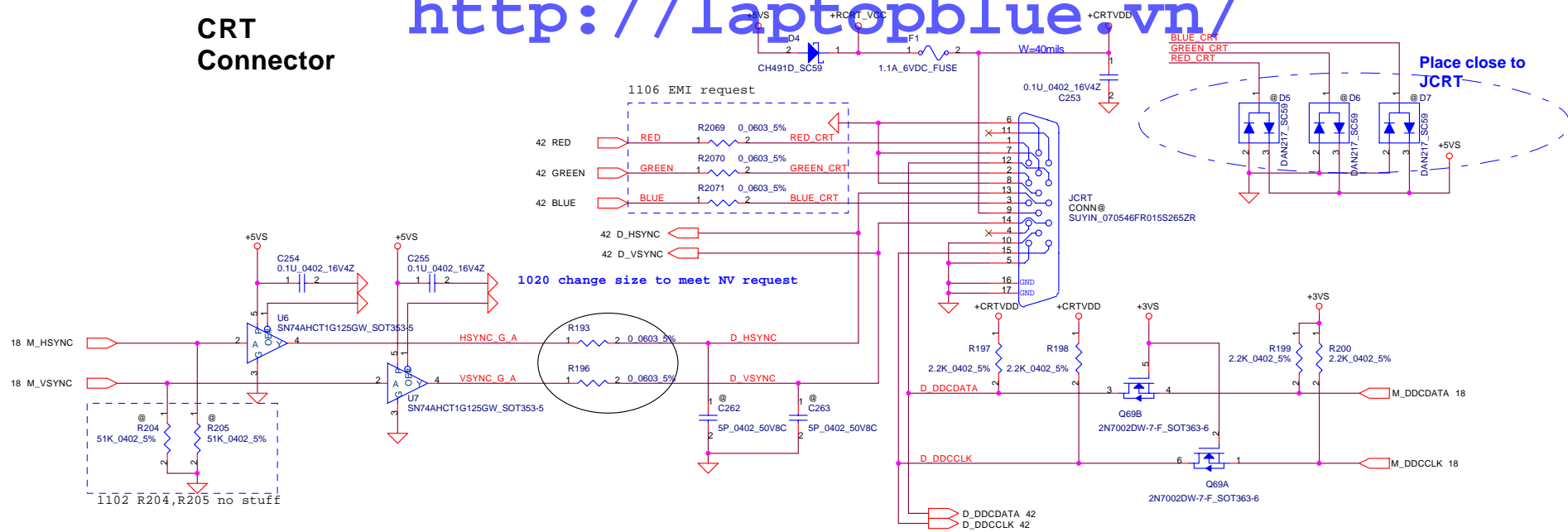
Layout Note:
Place series resistor
closely JP3, all
trace length Max=1.5"



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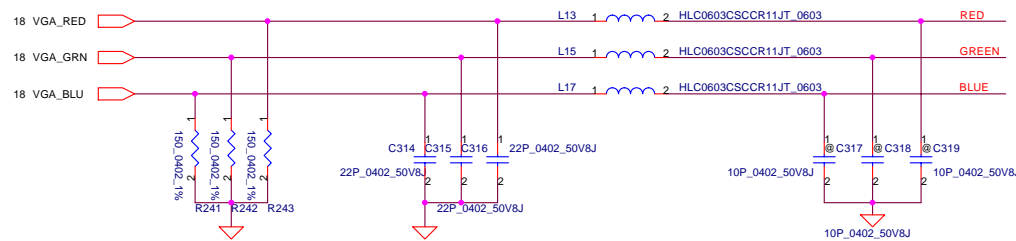
CRT Connector

<http://laptopblue.vn/>

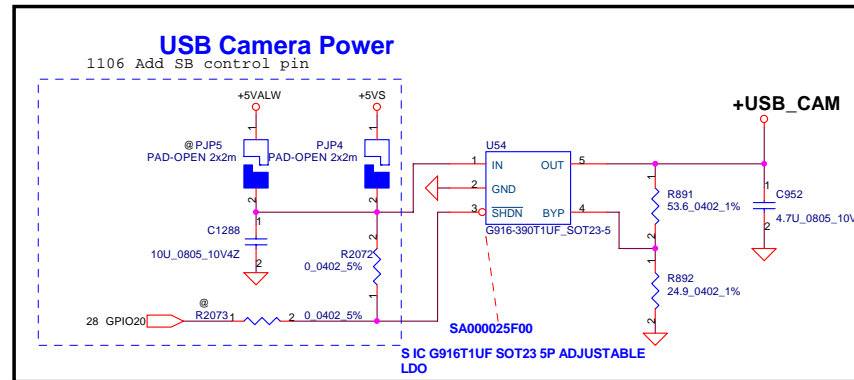
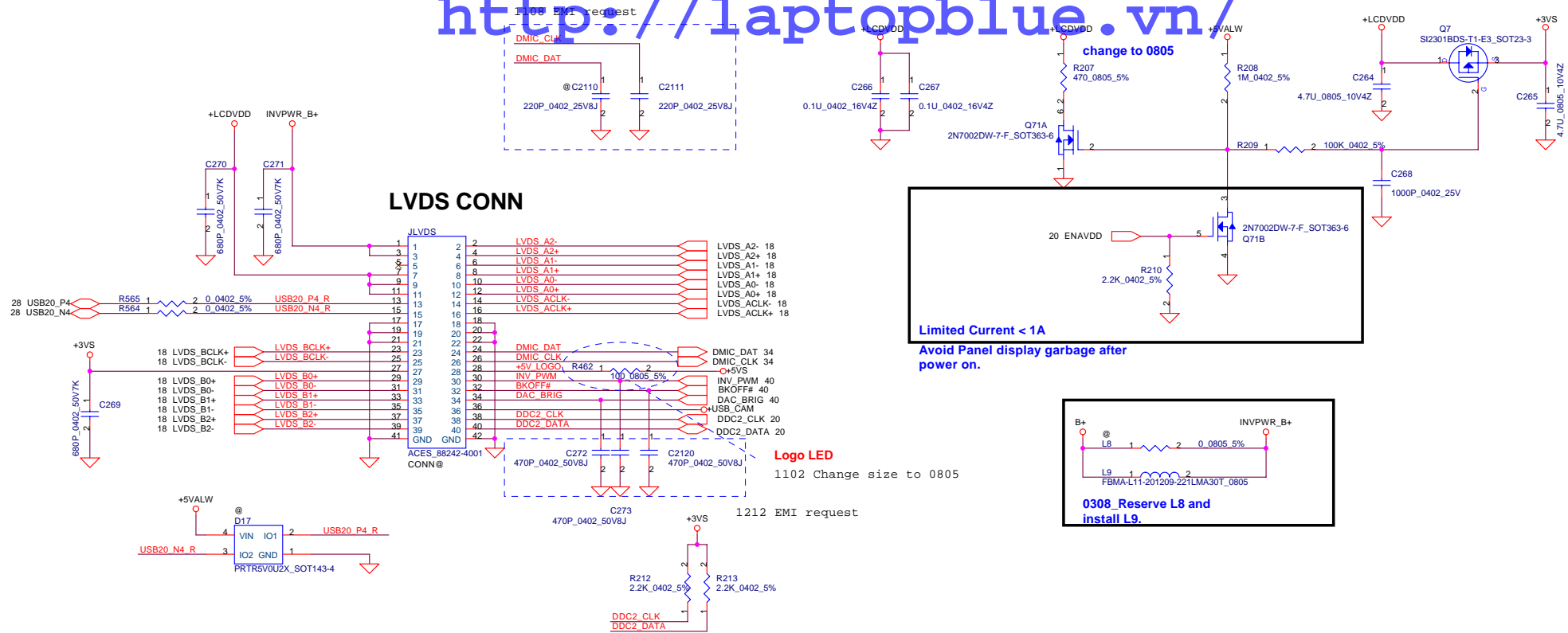


CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.



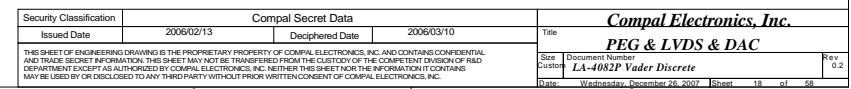
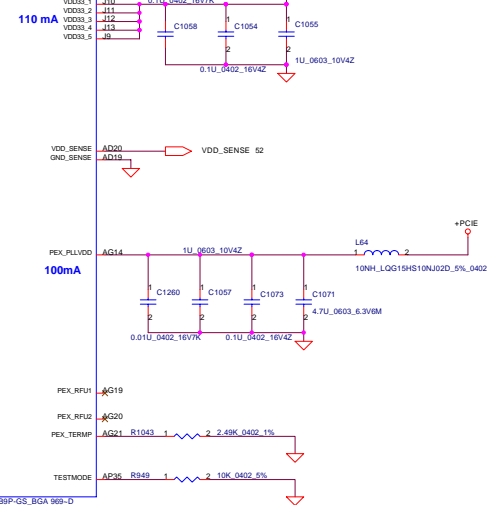
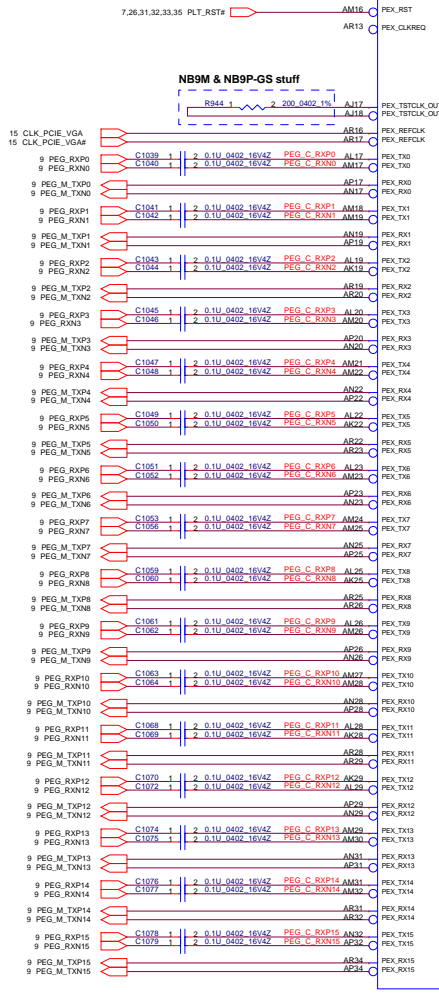
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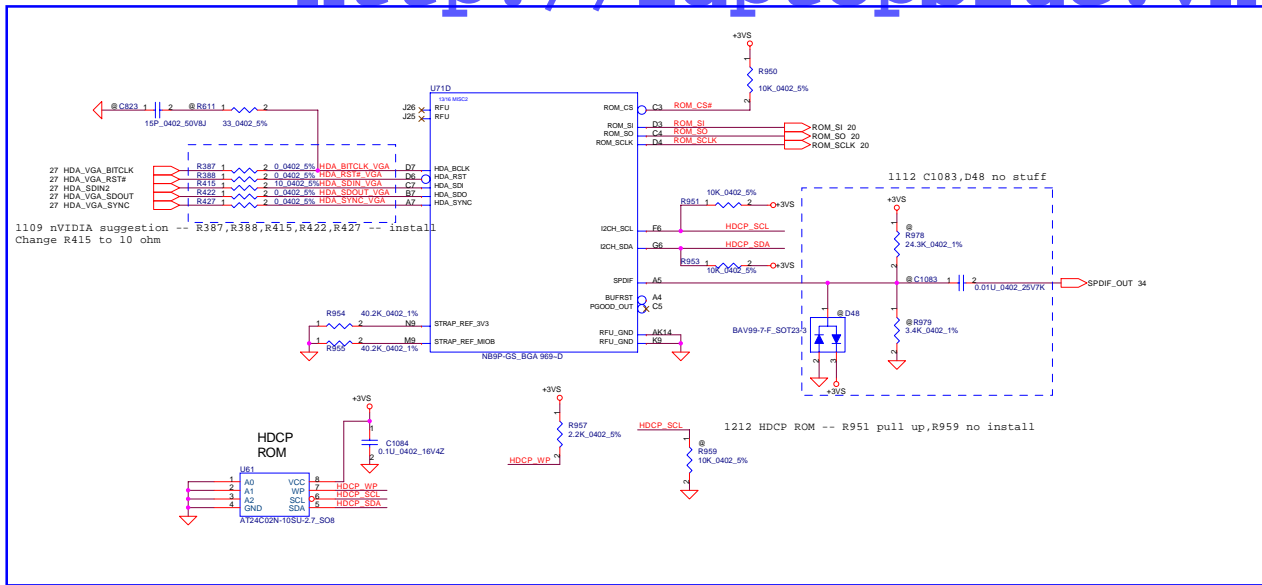


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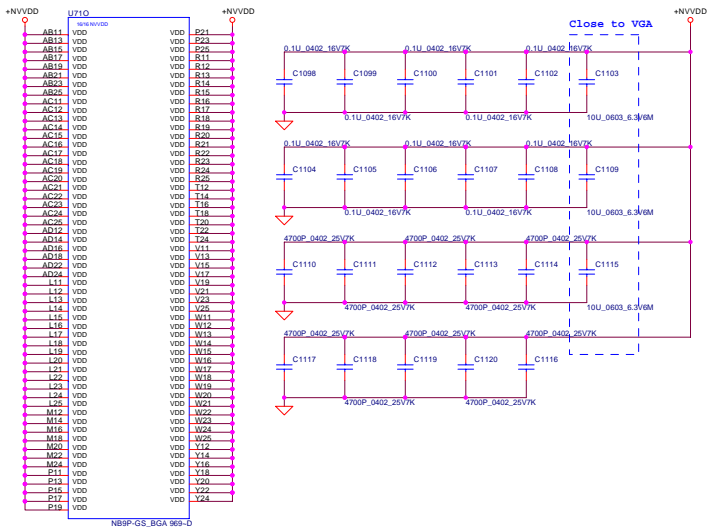
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500 mA



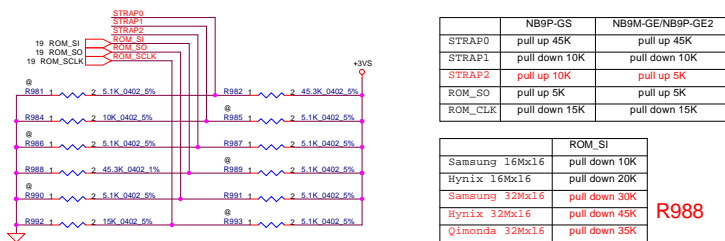


VGA Core power

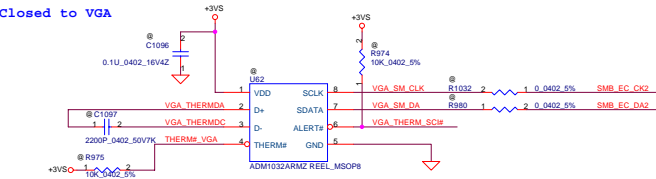


MULTI LEVEL STRAPS For NB9M-Gx (64bit)

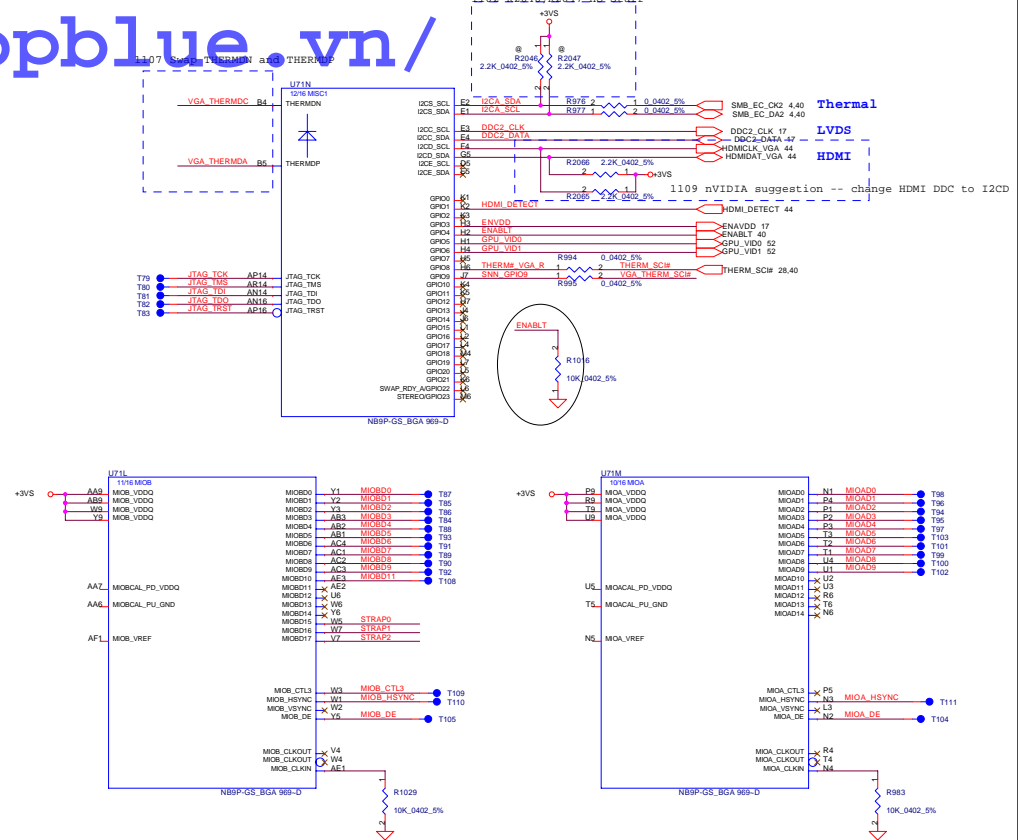
NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B



VGA Thermal Sensor ADM1032ARMZ

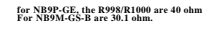


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



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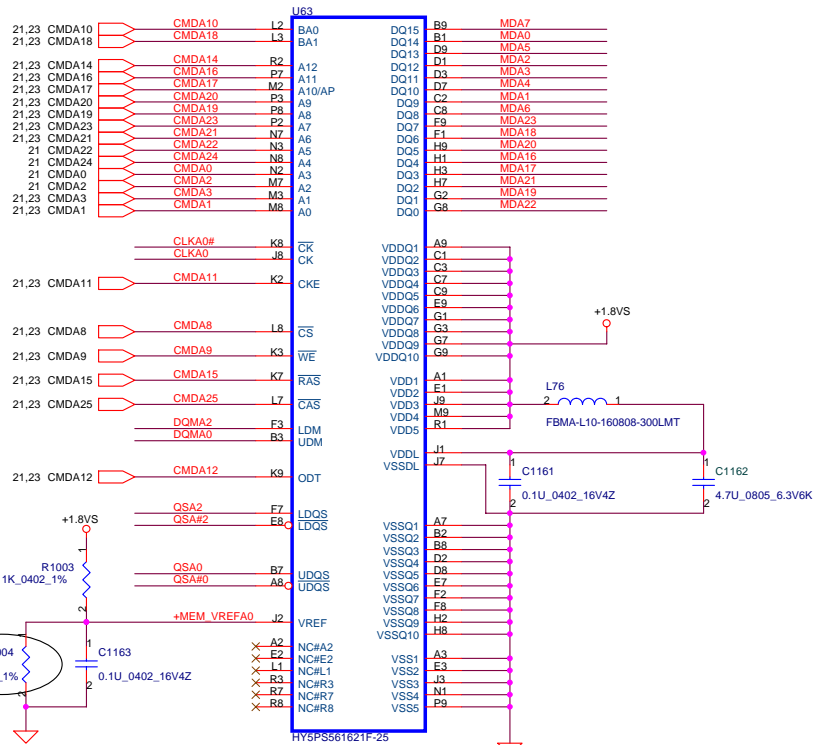
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

32Mx16 DDR2 400MHz *4==>256MB

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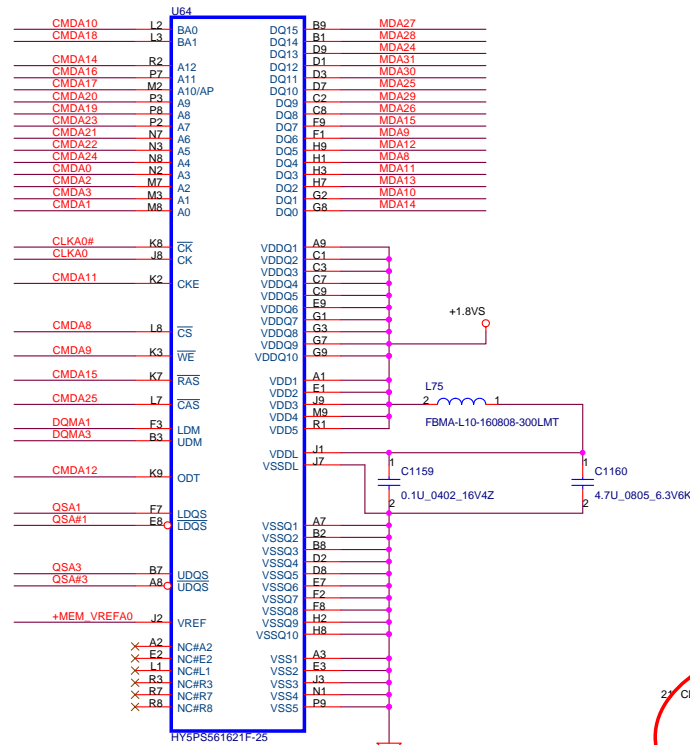
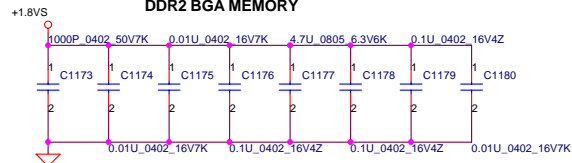
21.23 QSA[7..0] QSA[7..0]
21.23 QSA# [7..0] QSA# [7..0]
21.23 DQMA[7..0] DQMA[7..0]
21.23 MDA[63..0] MDA[63..0]



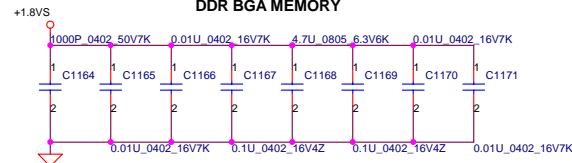
Vref= 0.5* 1.8V for NB9M, R1004=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1004=1K ohm

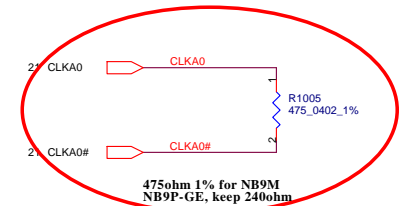
DDR2 BGA MEMORY



DDR BGA MEMORY



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD28		
CMD29		
CMD30		

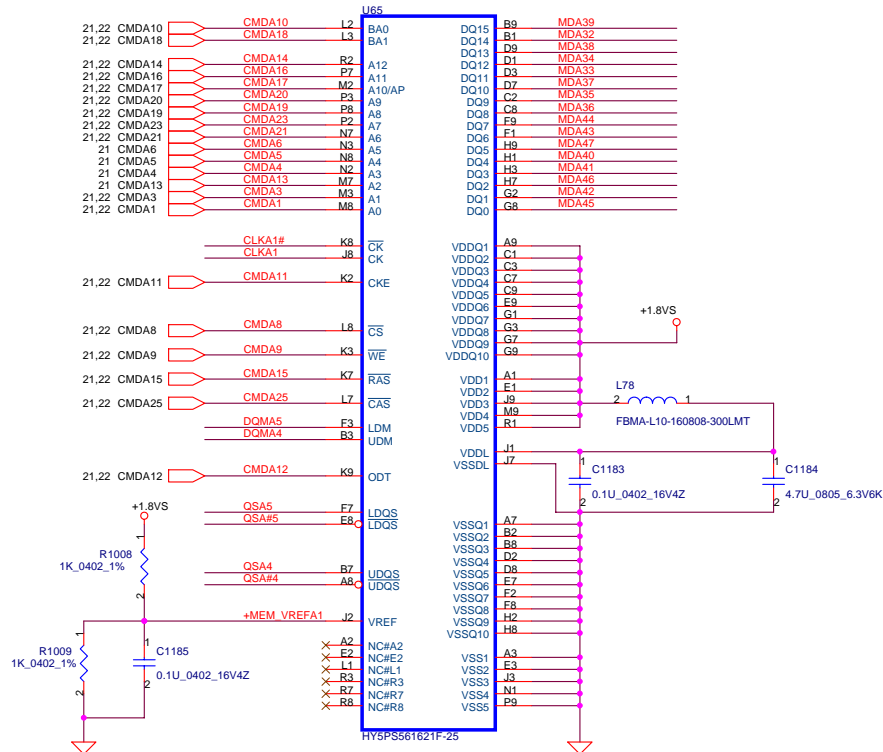
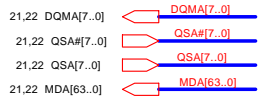


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						Size		Document Number		Rev	
						Date		LA-4082P Vader Discrete		0.2	
						Wednesday, December 26, 2007		Sheet 22 of 58			

VRAM DDR2 chips (256MB & 512MB)

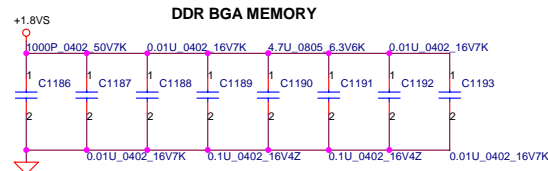
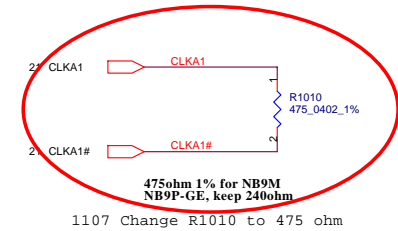
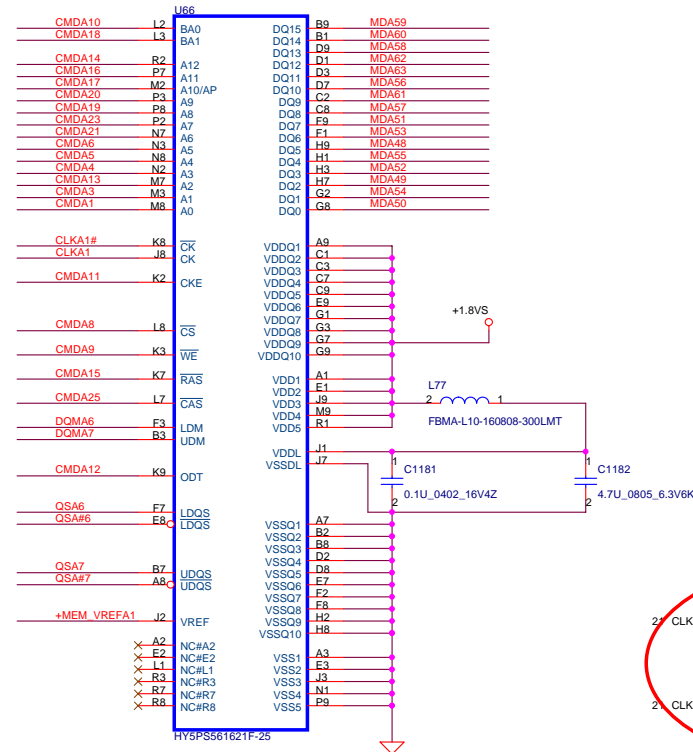
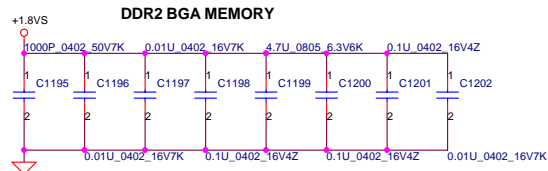
32Mx16 DDR2 400MHz *8==>512MB

32Mx16 DDR2 400MHz *4==>256MB



Vref= 0.5* 1.8V for NB9M, R1009=1K ohm

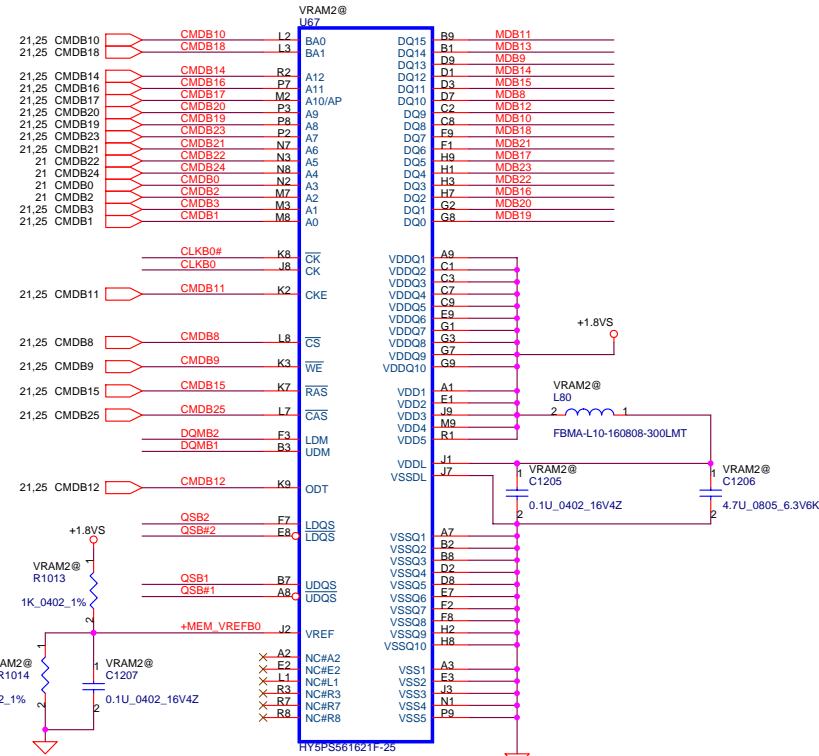
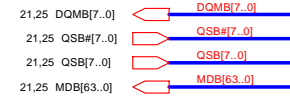
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm



Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

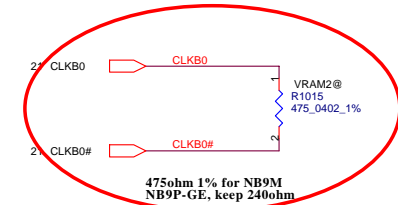
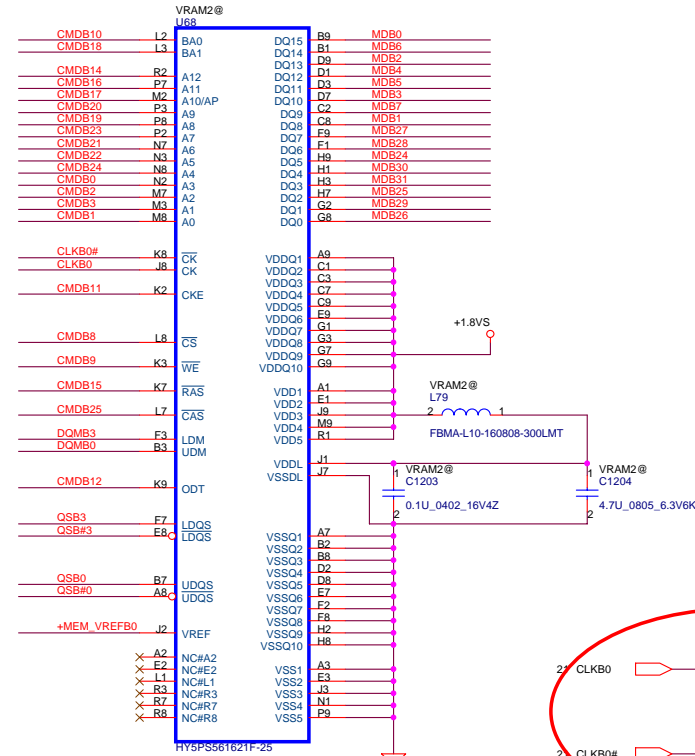
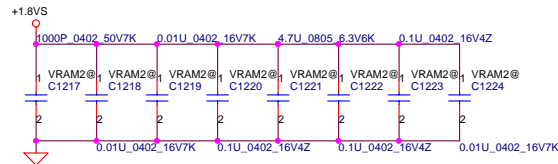
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB



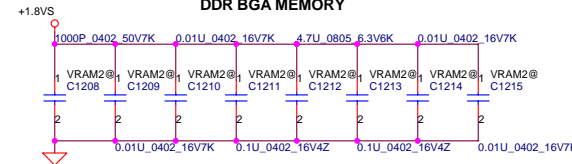
Vref= 0.5* 1.8V for NB9M, R1014=1K ohm
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm

DDR2 BGA MEMORY



1107 Change R1015 to 475 ohm

DDR2 BGA MEMORY

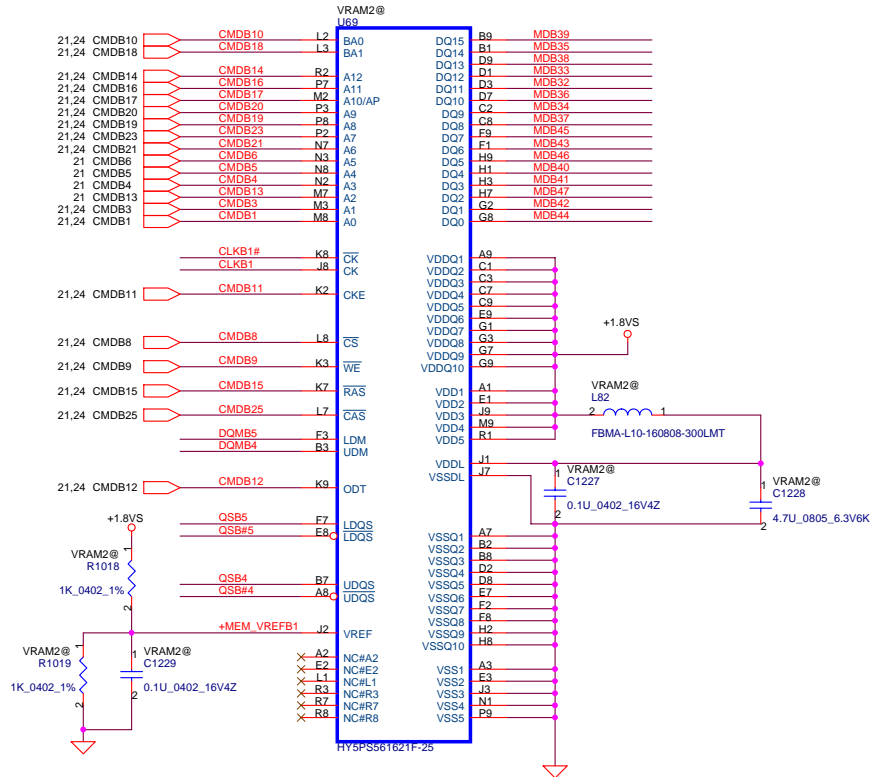


Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

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				CHANNEL B EXT. 256M 1			
				Size			
Document Number		LA-4082P		Vader Discrete		Rev 0.2	
Date:		Wednesday, December 26, 2007		Sheet 24		of 58	

VRAM DDR2 chips (256MB & 512MB)

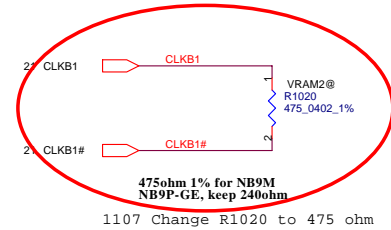
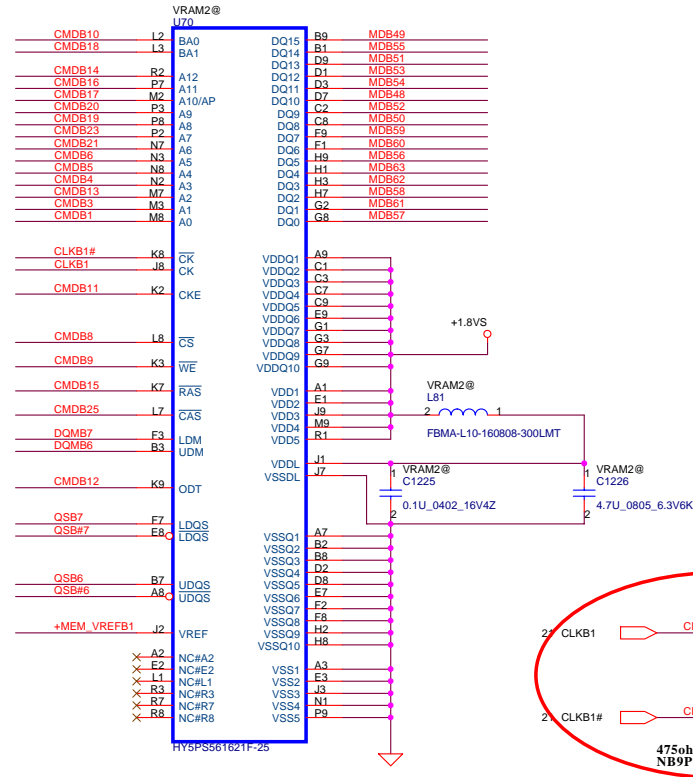
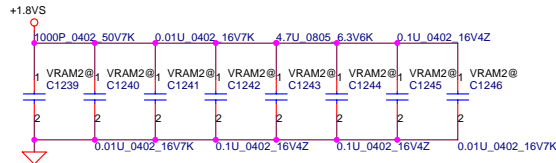
32Mx16 DDR2 400MHz *8==>512MB



Vref= 0.5* 1.8V for NB9M, R1019=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm

DDR2 BGA MEMORY



Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

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					Size	Document Number		Rev	
					Customer	LA-4082P		Vader Discrete	
					Date:	Wednesday, December 26, 2007		Sheet	25 of 58

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Interrupt 1/F


PCI	PIRQA#	J5	PIRQA#	PIRQE#/GPIO2	H4	PCI_PIRQE#
PCI	PIRQB# <td>E1</td> <td>PIRQB#<td>PIRQF#/GPIO2<td>K6</td><td>PCI_PIRQF#</td></td></td>	E1	PIRQB# <td>PIRQF#/GPIO2<td>K6</td><td>PCI_PIRQF#</td></td>	PIRQF#/GPIO2 <td>K6</td> <td>PCI_PIRQF#</td>	K6	PCI_PIRQF#
PCI	PIRQC# <td>J6</td> <td>PIRQC#<td>PIRQG#/GPIO4<td>F2</td><td>PCI_PIRQG#</td></td></td>	J6	PIRQC# <td>PIRQG#/GPIO4<td>F2</td><td>PCI_PIRQG#</td></td>	PIRQG#/GPIO4 <td>F2</td> <td>PCI_PIRQG#</td>	F2	PCI_PIRQG#
PCI	PIRQD# <td>C4</td> <td>PIRQD#<td>PIRQH#/GPIO5<td>G2</td><td>PCI_PIRQH#</td></td></td>	C4	PIRQD# <td>PIRQH#/GPIO5<td>G2</td><td>PCI_PIRQH#</td></td>	PIRQH#/GPIO5 <td>G2</td> <td>PCI_PIRQH#</td>	G2	PCI_PIRQH#

PCI_PIRQH# 39

A schematic diagram showing a resistor labeled "1K_0402_5%" connected to a signal line labeled "PCI_GNT3#". The resistor is represented by a blue zigzag line with terminals "1" and "2". Terminal "1" is connected to the "PCI_GNT3#" line, and terminal "2" is connected to ground, indicated by a red triangle symbol. The resistor is labeled "@ R354" above it.

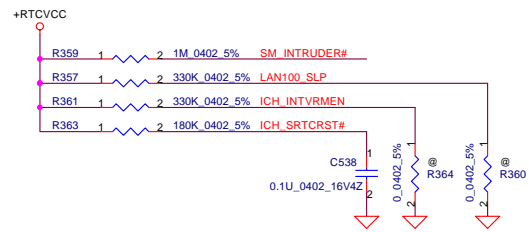
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

28 SPI_CS1#_R  SPI_CS1#_R @R356 1 2 1K_0402_5% +3VALW

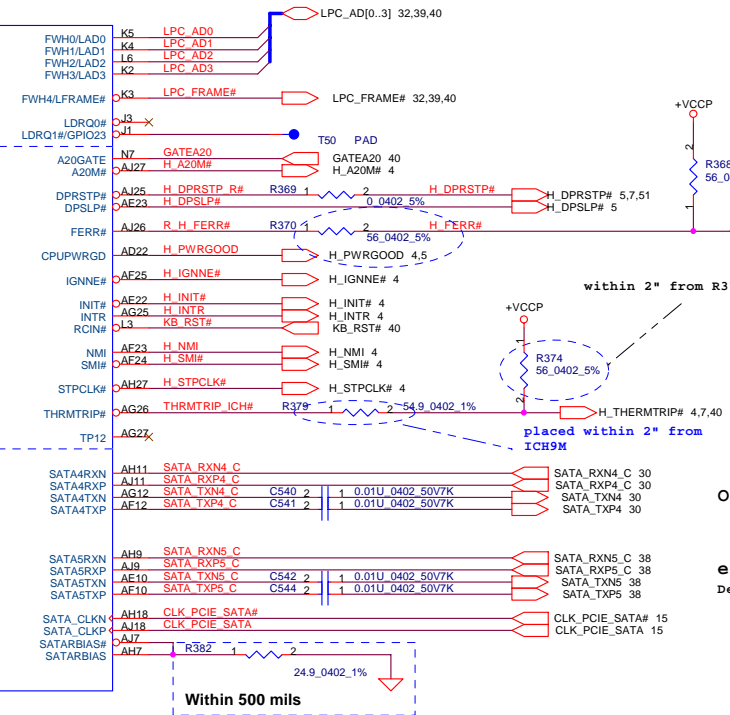
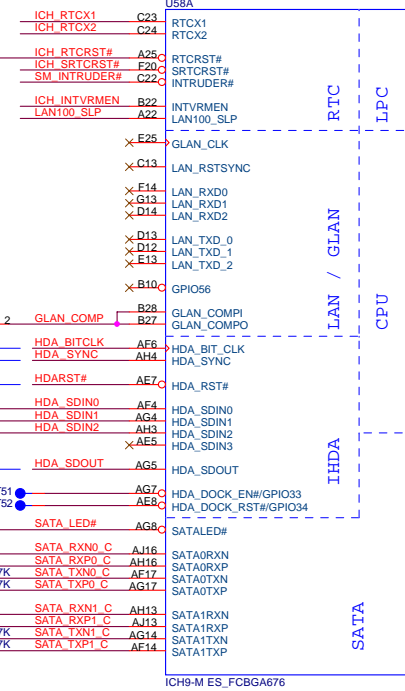
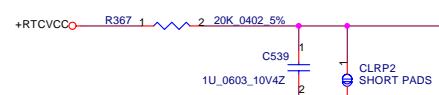
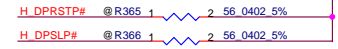
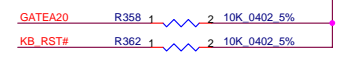
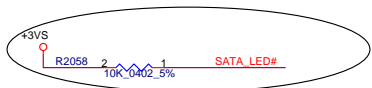
PCI_GNT0#  PCI_GNT0# @R355 1 2 1K_0402_5%

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				ICH9(1/4)-PCI/INT			
				Size	Document Number		
				LA-4082P Vader Discrete			0.2
Date:				Wednesday, December 26, 2007		Sheet	26 of 58

ICH9M Internal VR Enable Strap (Internal VR for VccBus1.05, VccSys1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



1015 add pull up to meet Intel design

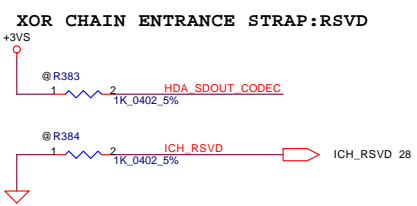


ODD

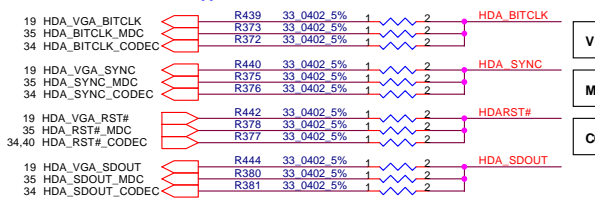
e-SATA
De-feature disable

P- HDD
S- HDD

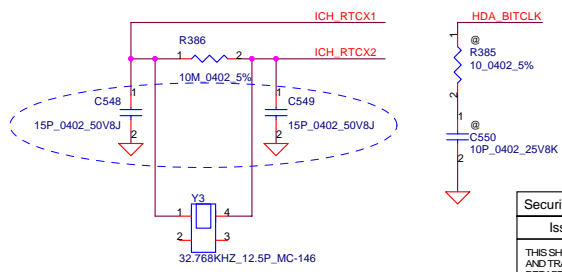
1212 Swap SATA1 and SATA4



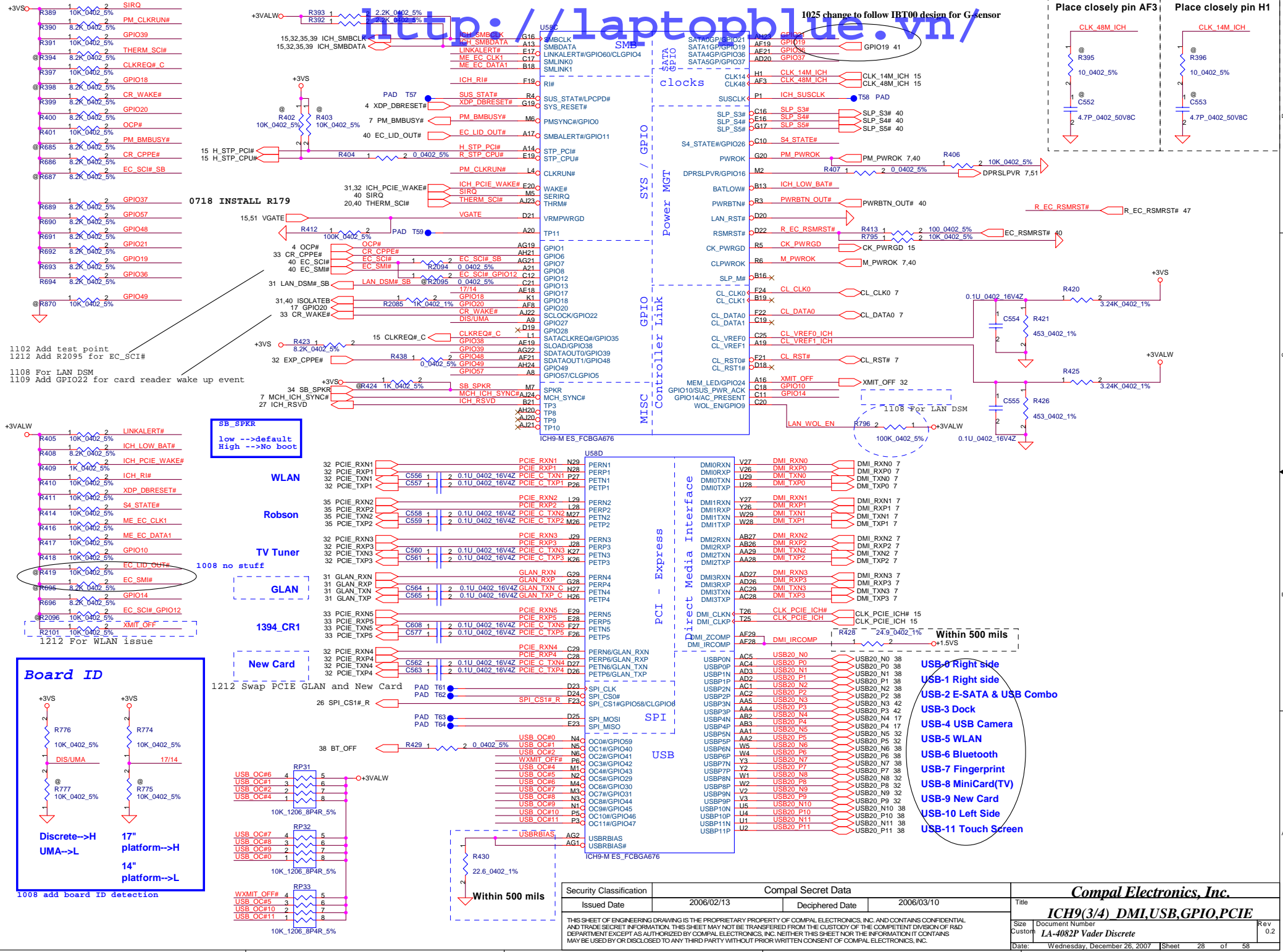
1008 add them for Intel suggestion



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	



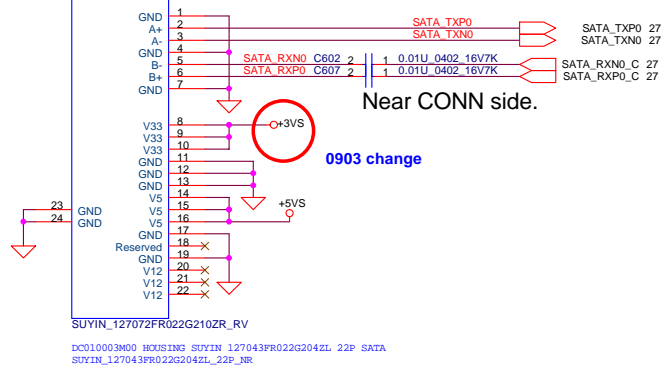
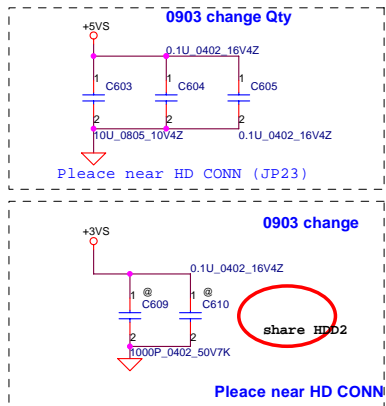
http://laptopblue.vn/



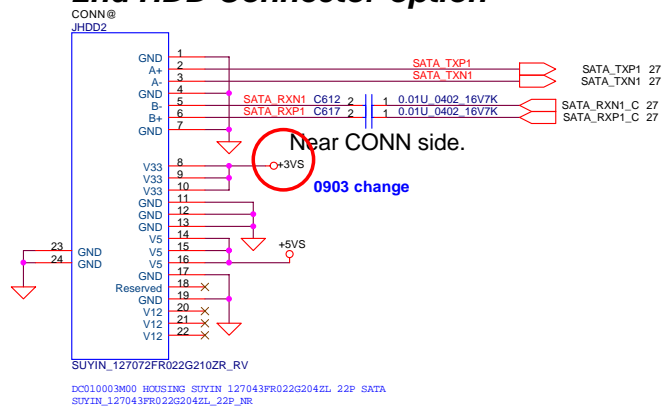
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
				ICh9(3/4) DMI,USB,GPIO,PCIE	
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		Custom		LA-4082P Vader Discrete	0.2
		Date		Wednesday, December 26, 2007	Sheet 28 of 58

US8E			
A26	VSS[001]	VSS[107]	H5
A27	VSS[002]	VSS[108]	J23
A3	VSS[003]	VSS[109]	J26
A6	VSS[004]	VSS[110]	J27
AB1	VSS[005]	VSS[111]	AC22
A23	VSS[006]	VSS[112]	K28
AB28	VSS[007]	VSS[113]	K28
AB2	VSS[008]	VSS[114]	L13
AB4	VSS[009]	VSS[115]	L19
AB5	VSS[010]	VSS[116]	L2
AC17	VSS[011]	VSS[117]	L26
AC26	VSS[012]	VSS[118]	L27
AC27	VSS[013]	VSS[119]	L5
AC3	VSS[014]	VSS[120]	L7
AD1	VSS[015]	VSS[121]	M12
AD10	VSS[016]	VSS[122]	M13
AD11	VSS[017]	VSS[123]	M14
AD13	VSS[018]	VSS[124]	M15
AD14	VSS[019]	VSS[125]	M16
AD17	VSS[020]	VSS[126]	M17
AD18	VSS[021]	VSS[127]	M23
AD21	VSS[022]	VSS[128]	M28
AD28	VSS[023]	VSS[129]	M28
AD29	VSS[024]	VSS[130]	N11
AD4	VSS[025]	VSS[131]	N12
AD5	VSS[026]	VSS[132]	N13
AD6	VSS[027]	VSS[133]	N14
AD7	VSS[028]	VSS[134]	N15
AD9	VSS[029]	VSS[135]	N16
AE12	VSS[030]	VSS[136]	N17
AE13	VSS[031]	VSS[137]	N18
AE14	VSS[032]	VSS[138]	N26
AE16	VSS[033]	VSS[139]	N27
AE17	VSS[034]	VSS[140]	P12
AE2	VSS[035]	VSS[141]	P13
AE24	VSS[036]	VSS[142]	P15
AE3	VSS[037]	VSS[143]	P16
AE4	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P21
AE9	VSS[041]	VSS[147]	P22
AF13	VSS[042]	VSS[148]	P28
AF16	VSS[043]	VSS[149]	P29
AF18	VSS[044]	VSS[150]	P4
AF22	VSS[045]	VSS[151]	R1
AH26	VSS[046]	VSS[152]	R11
AF26	VSS[047]	VSS[153]	R12
AF5	VSS[048]	VSS[154]	R13
AF7	VSS[049]	VSS[155]	R14
AF9	VSS[050]	VSS[156]	R15
AG13	VSS[051]	VSS[157]	R17
AG16	VSS[052]	VSS[158]	R18
AG18	VSS[053]	VSS[159]	R28
AG19	VSS[054]	VSS[160]	R28
AG20	VSS[055]	VSS[161]	T12
AG3	VSS[056]	VSS[162]	T13
AG6	VSS[057]	VSS[163]	T14
AG8	VSS[058]	VSS[164]	T15
AG9	VSS[059]	VSS[165]	T16
AH12	VSS[060]	VSS[166]	T17
AH14	VSS[061]	VSS[167]	T23
AH17	VSS[062]	VSS[168]	B26
AH19	VSS[063]	VSS[169]	U12
AH2	VSS[064]	VSS[170]	U13
AH25	VSS[065]	VSS[171]	U14
AH26	VSS[066]	VSS[172]	U15
AH28	VSS[067]	VSS[173]	U16
AH5	VSS[068]	VSS[174]	U17
AH8	VSS[069]	VSS[175]	AD23
AJ12	VSS[070]	VSS[176]	U26
AJ14	VSS[071]	VSS[177]	U27
AJ17	VSS[072]	VSS[178]	U3
AJ8	VSS[073]	VSS[179]	Y1
B11	VSS[074]	VSS[180]	Y13
B14	VSS[075]	VSS[181]	Y15
B17	VSS[076]	VSS[182]	Y23
B2	VSS[077]	VSS[183]	Y28
B20	VSS[078]	VSS[184]	V28
B23	VSS[079]	VSS[185]	V4
B5	VSS[080]	VSS[186]	V5
C6	VSS[081]	VSS[187]	W26
C26	VSS[082]	VSS[188]	W27
C27	VSS[083]	VSS[189]	W3
E11	VSS[084]	VSS[190]	Y1
E14	VSS[085]	VSS[191]	Y28
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y4
E21	VSS[088]	VSS[194]	Y6
E5	VSS[089]	VSS[195]	AG28
E8	VSS[090]	VSS[196]	AH6
F8	VSS[091]	VSS[197]	AF2
F16	VSS[092]	VSS[198]	B25
F28	VSS[093]		
F29	VSS[094]		
G12	VSS[095]		
G14	VSS[096]	VSS_NCTFF[01]	A1
G18	VSS[097]	VSS_NCTFF[02]	A2
G21	VSS[098]	VSS_NCTFF[03]	A28
G24	VSS[099]	VSS_NCTFF[04]	A29
G26	VSS[100]	VSS_NCTFF[05]	AH1
G27	VSS[101]	VSS_NCTFF[06]	AH29
G8	VSS[102]	VSS_NCTFF[07]	AJ1
H2	VSS[103]	VSS_NCTFF[08]	AJ2
H23	VSS[104]		

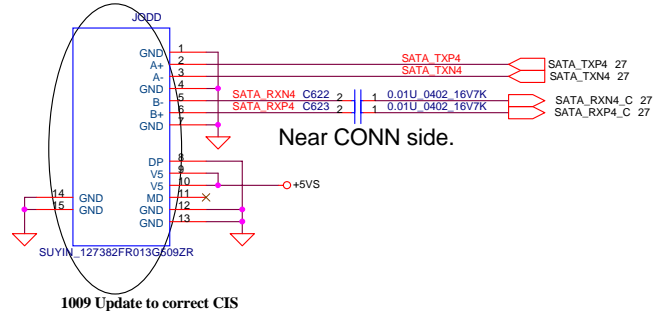
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> <i>ICH9(4/4) POWER&GND</i>		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title		
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				Date: Wednesday, December 26, 2007	Sheet 29	of 58



2nd HDD Connector-option

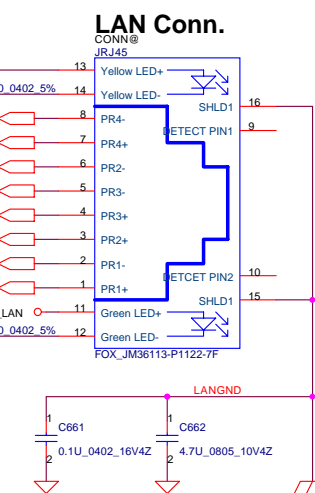
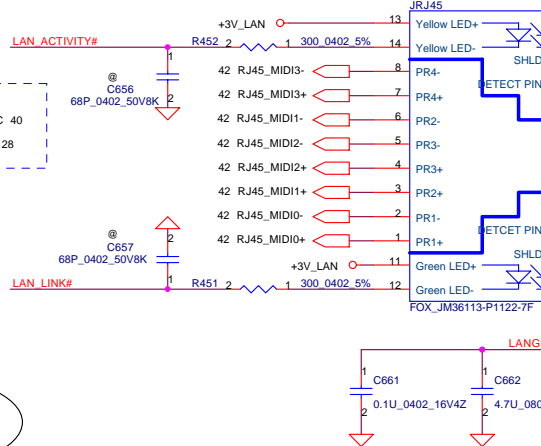
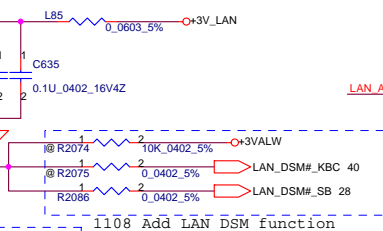
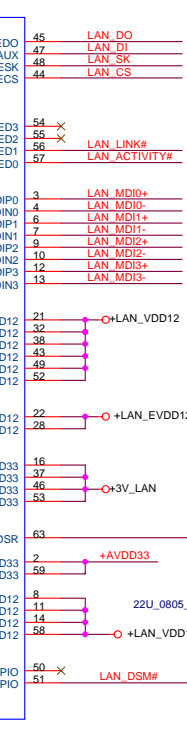
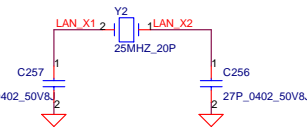
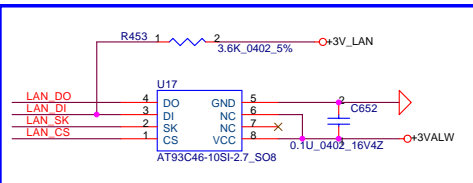
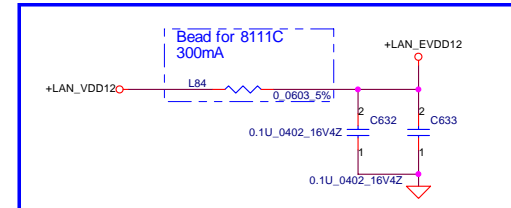
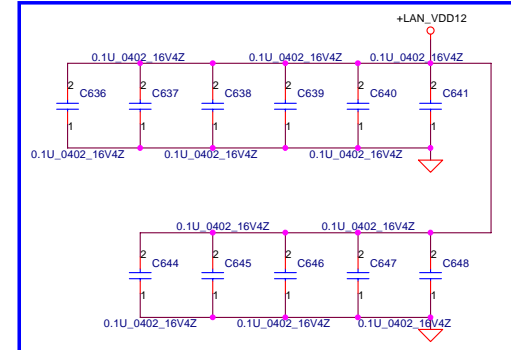
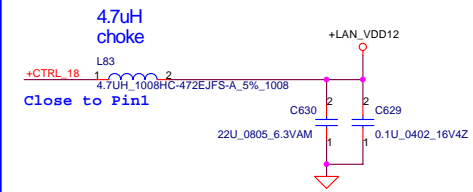
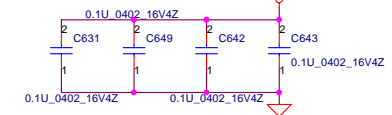
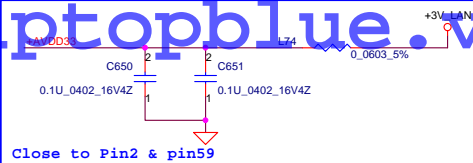


CD-ROM Connector



ZZZ1
LA-4082P

Security Classification	Compal Secret Data			Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	HDD & CDROM	
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Place these components
colsed to LAN chip

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Issued Date	2006/02/13	Deciphered Date	2006/03/10			
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				8111C GLAN		
				Size	Document Number	Rev
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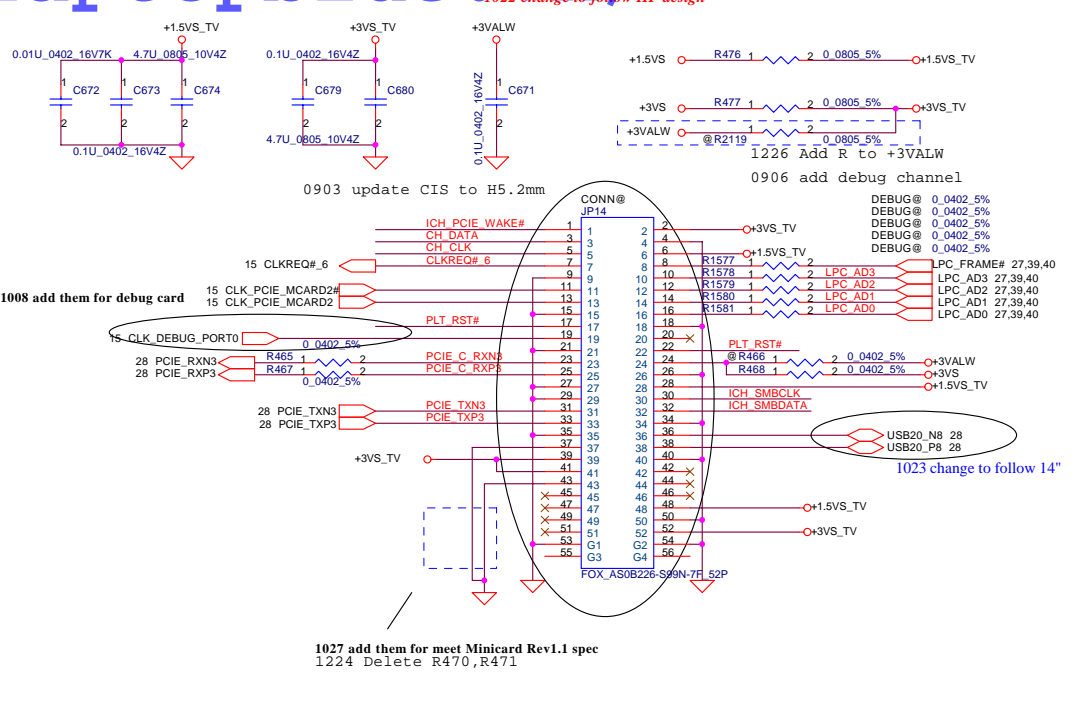
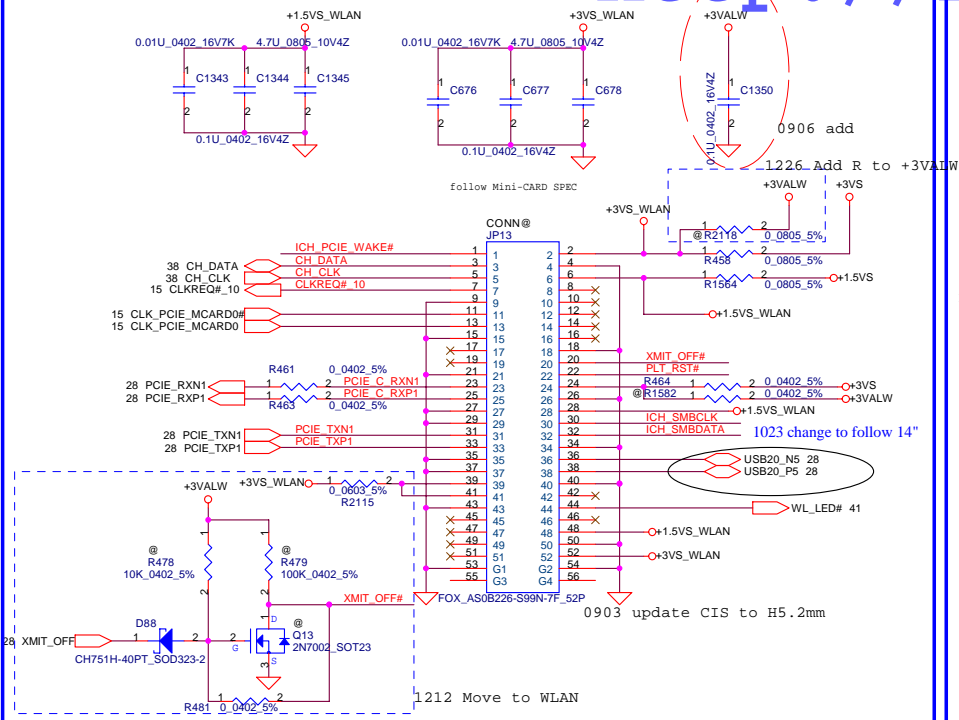
Mini Card 0--WLAN

1022 change to follow HP design

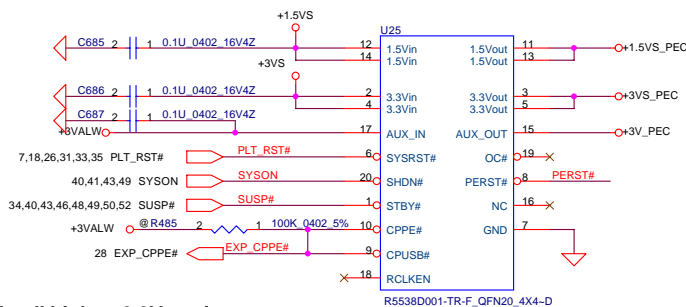
http://laptopblue.vn/

Mini Card 2--TV tuner

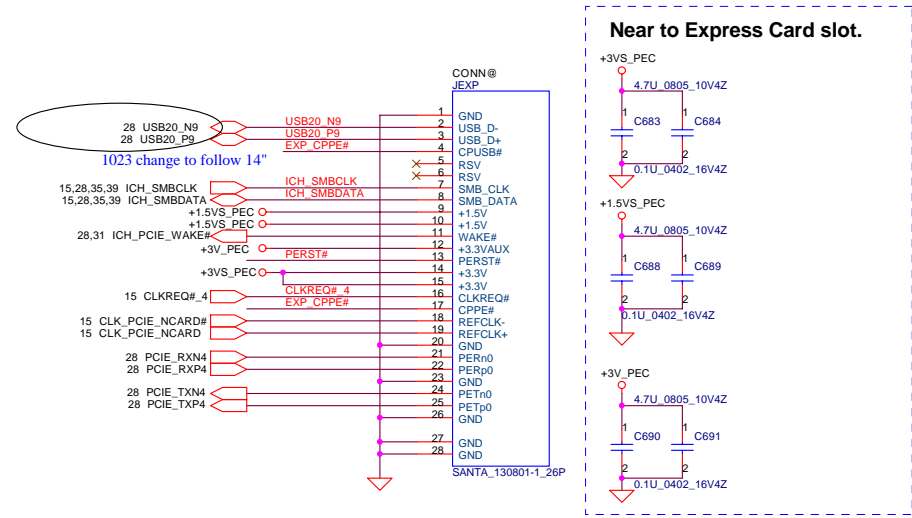
1022 change to follow HP design



New Card



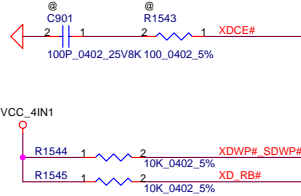
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



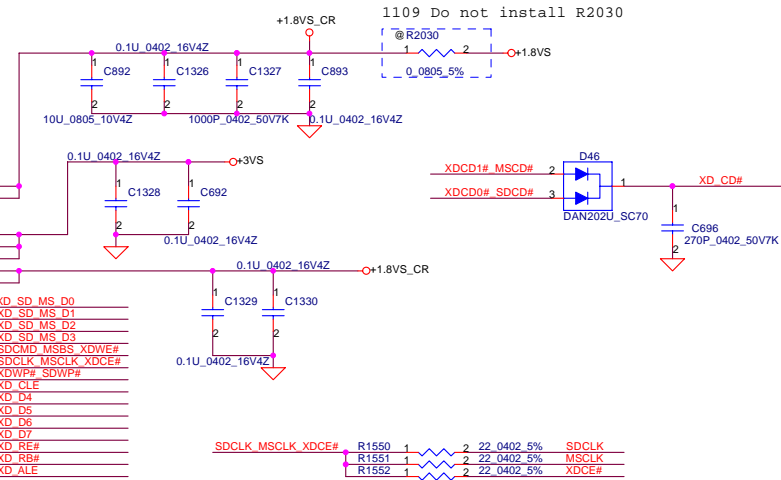
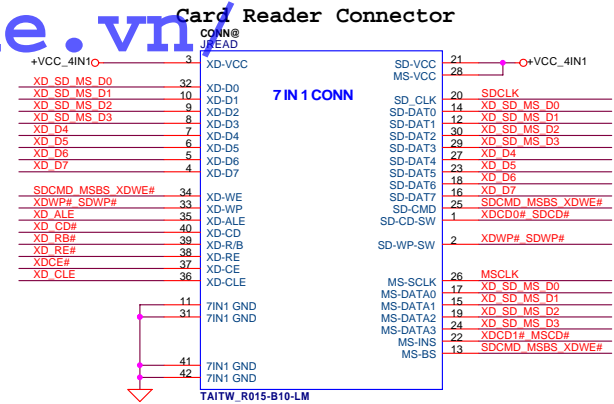
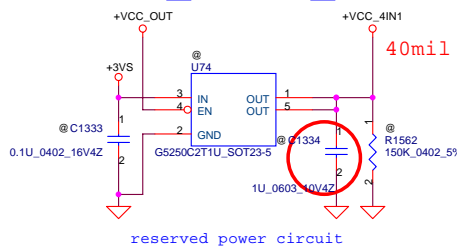
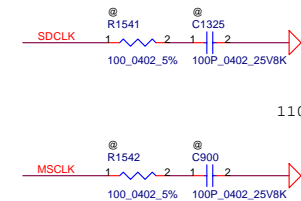
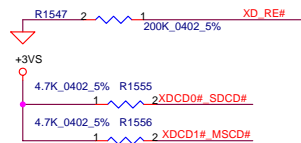
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	WLAN, WWAN, New Card	
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need change to low active switch

1102 Install R1553



1212 Change XD_ALE to +3VS



1023 JMicro suggest to change

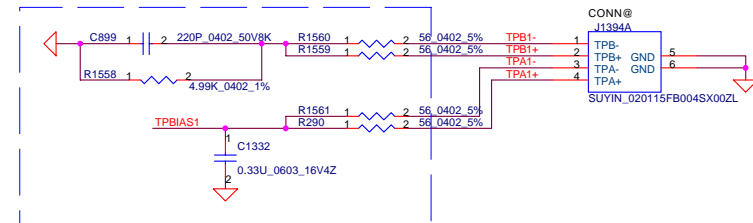
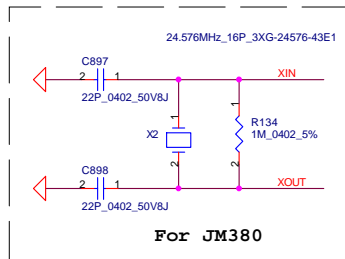
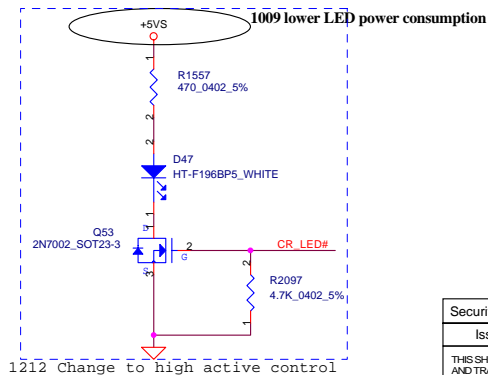
1109 Add D86 for card reader wake up

use for PWR EN#
8mA sink current

JMB380

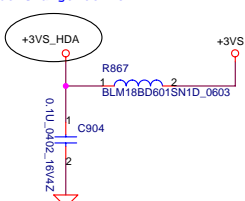
JMB380-QGAZ0A QFN48 7X7

White LED: $V_F=3V$, $I_F = 5mA$, $R_{es} = 56\Omega$



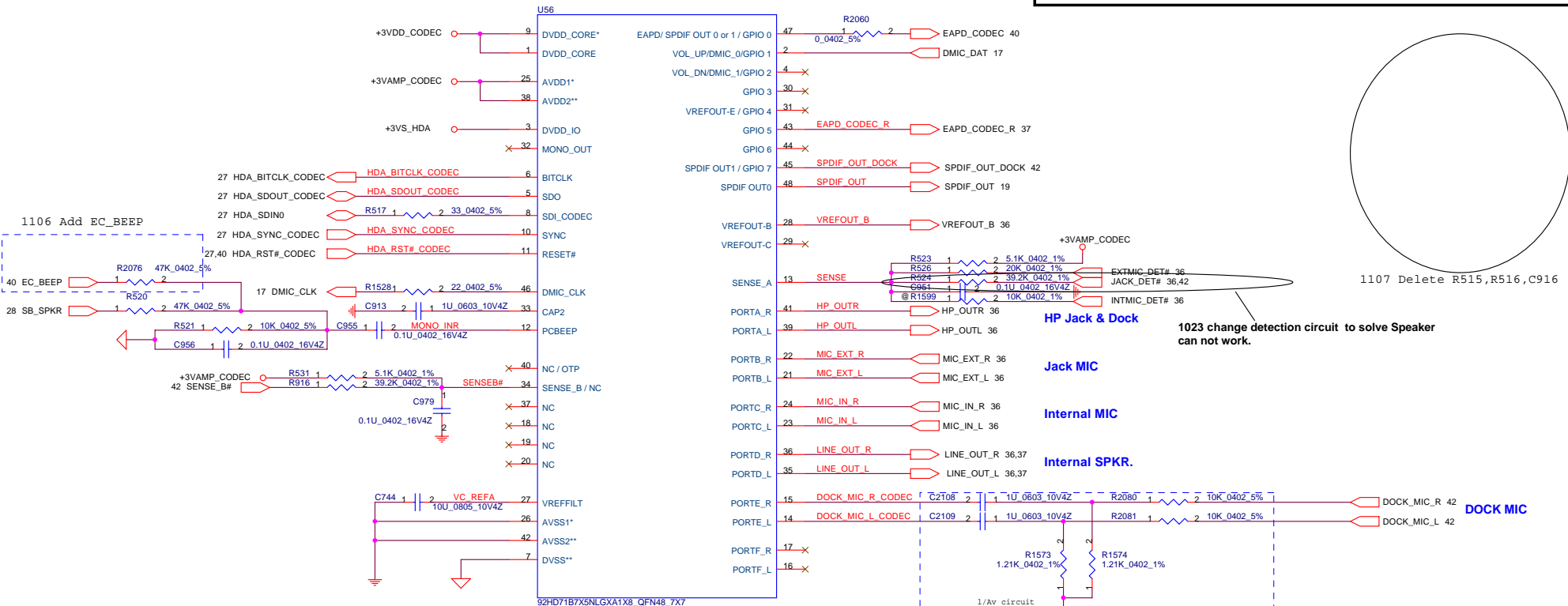
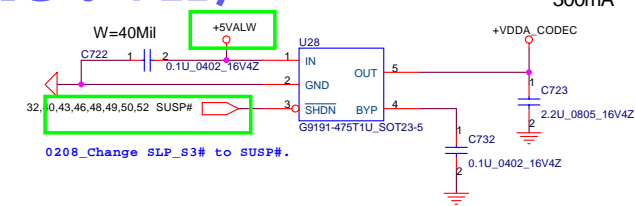
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Issued Date		2006/02/13	Deciphered Date		2006/03/10	Title			
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						Size	Document Number		Rev
						Cust	LA-4082P Vader Discrete		0.2
Date:		Wednesday, December 26, 2007		Sheet	33	of 58			

1008 Change to +3V



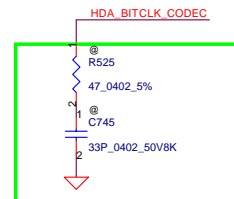
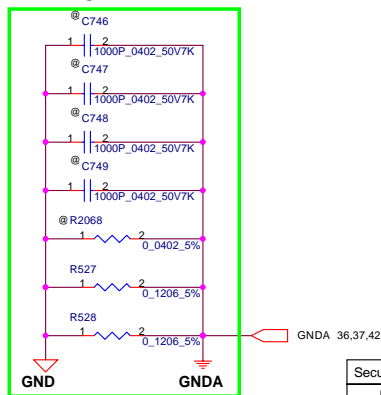
<http://laptopblue.vn/>

CODEC POWER (4.75V) 300mA



1106 Change C746,C747,C748,C749 to 1000PF

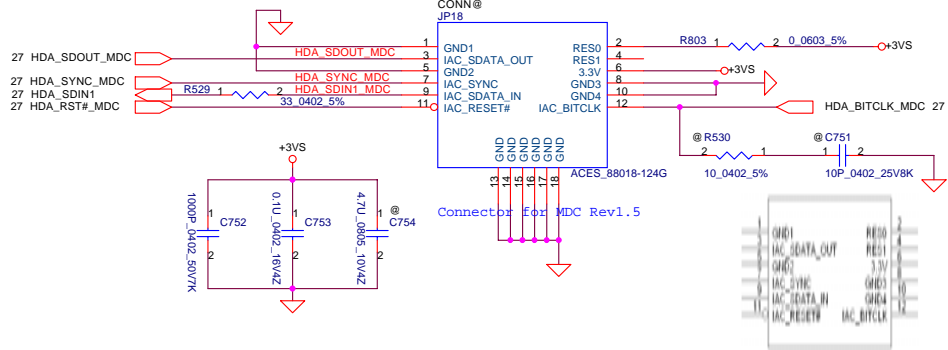
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



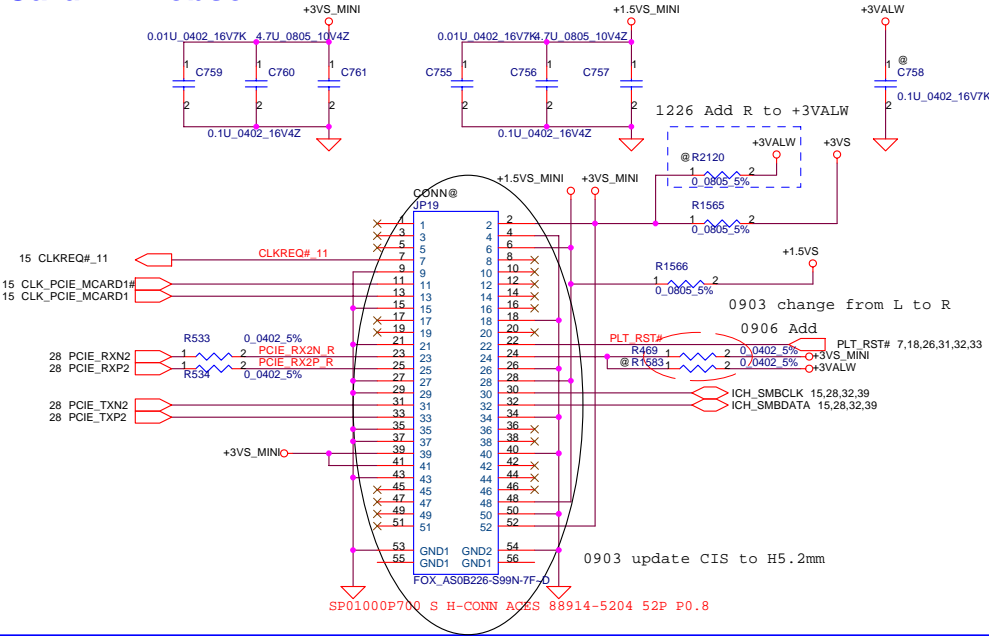
Security Classification		Compal Secret Data	
Issued Date	2006/02/13	Deciphered Date	2006/03/10
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Size		Codec IDT9271B7	
Document Number		LA-4082P Vader Discrete	
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MDC 1.5 Conn.

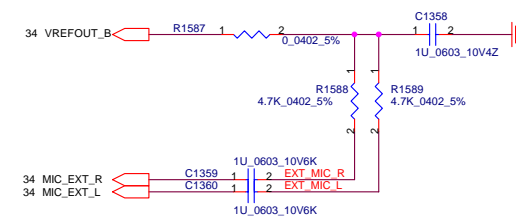
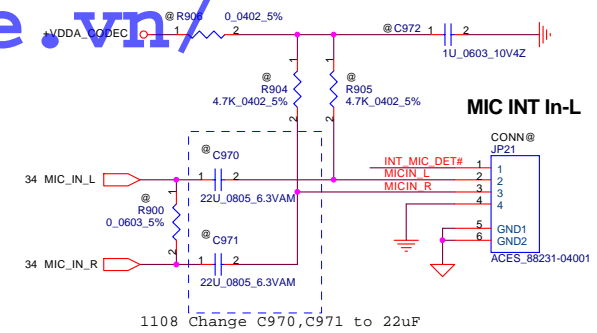
Change type 4/25



Mini Card 1---Robson

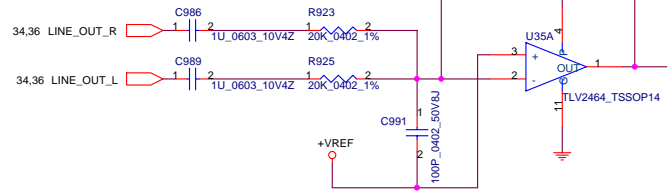


0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002

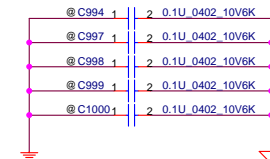
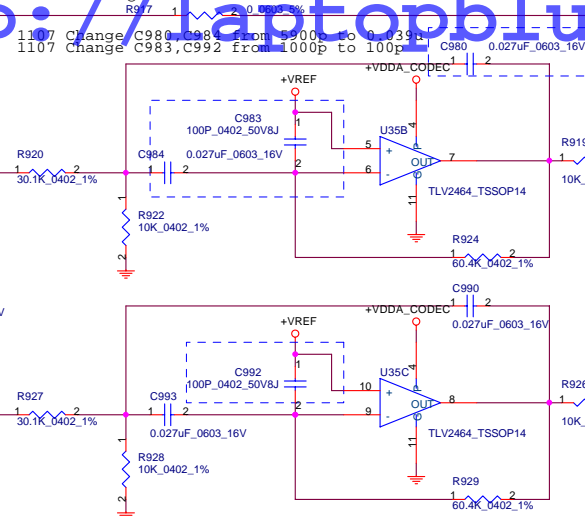
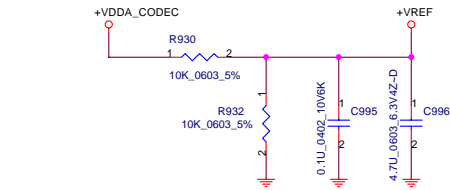


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	AMP & Audio Jack		
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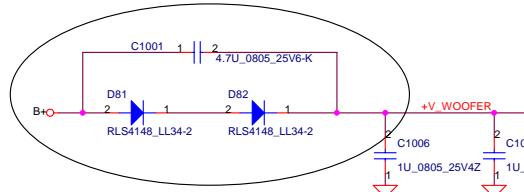
1107 Change C982 from 5900p to 0.039u



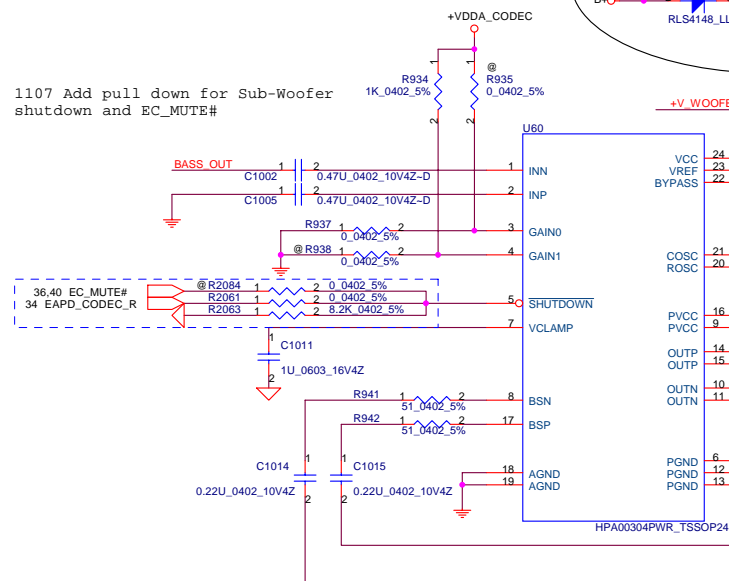
1224 C987 change from 0.47u to 0.056uF
Change C984, C980, C993, C990 to 0.027uF



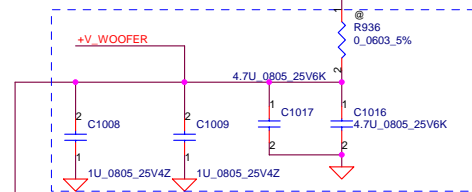
1009 change Subwoofer power circuit



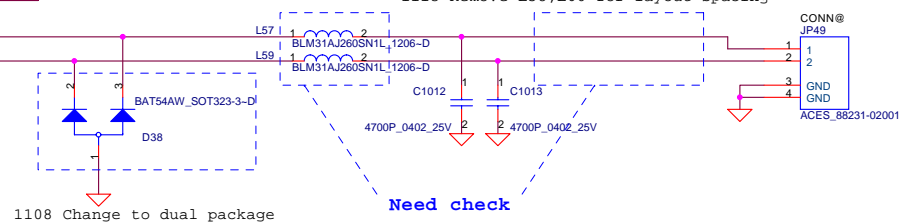
1107 Add pull down for Sub-Woofers shutdown and EC_MUTE#



1107 Change C1008, C1009 to 1uF and no install R936



1113 Remove L58, L60 for layout spacing



1108 Change to dual package

Need check

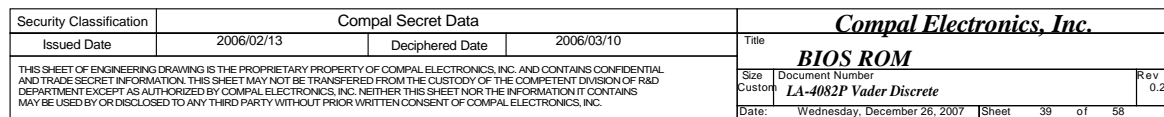
Sub-woofer Connector

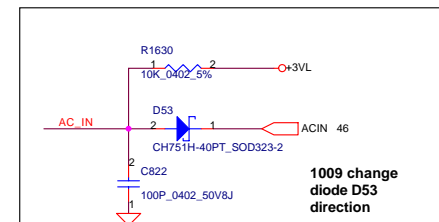
Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	EQ & Sub Woofer	
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				Custom	LA-4082P Vader Discrete
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http://laptopblue.esata/usb.com

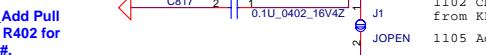


Security Classification	Compal Secret Data			Compal Electronics, Inc. USB, BT, eSATA		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title		
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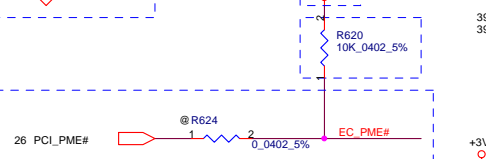




1009 change
diode D53
direction

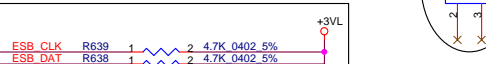


1102 Change R615 to 8.2k ohm add pull down on SYSON

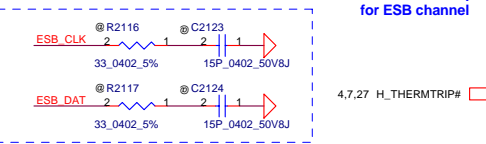


0214_Add Pull high resistor for LID_SW# and WL_BTN#.

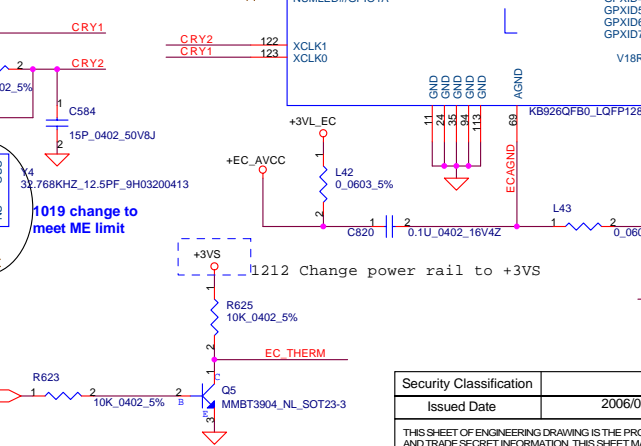
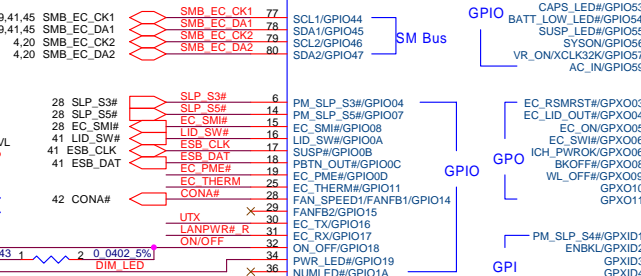
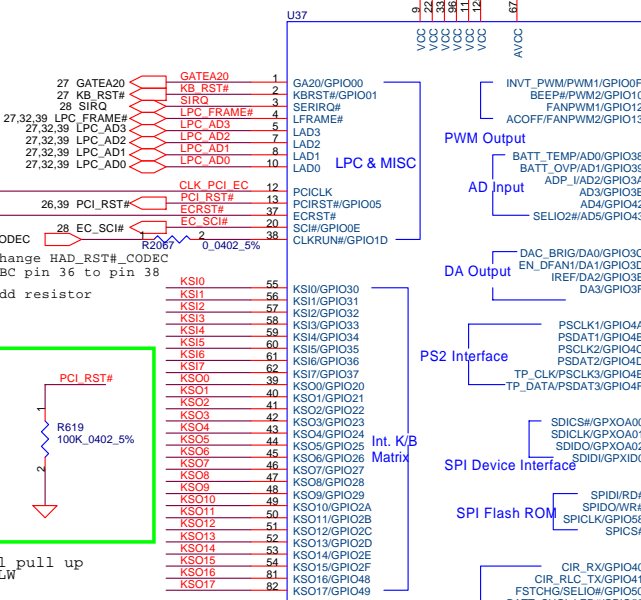
```
1114 R620 no stuff, SB internal pull up
1212 Change power rail to +3VALW
```



1025 Add Pull up
for ESB channel

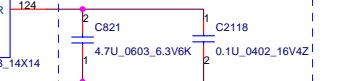
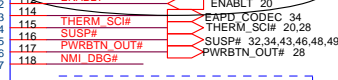
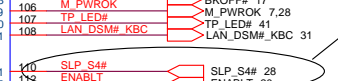
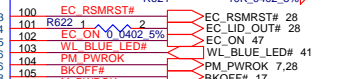
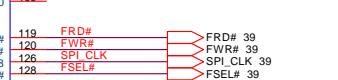
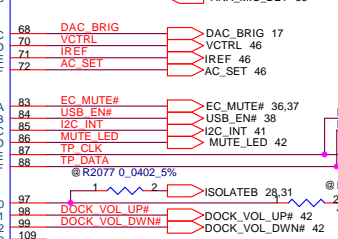
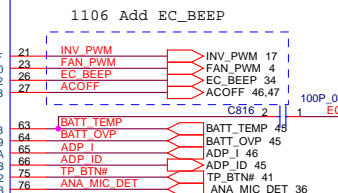


1225 Add R,C for EMI

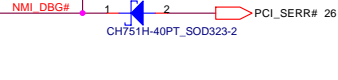
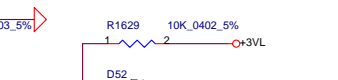
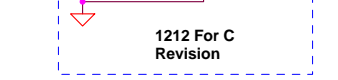


1019 change to

```
1212 Change power rail to +3VS
```

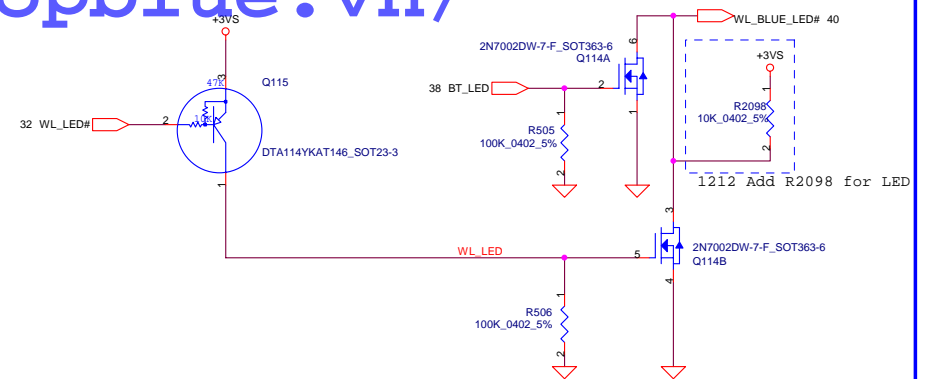


121

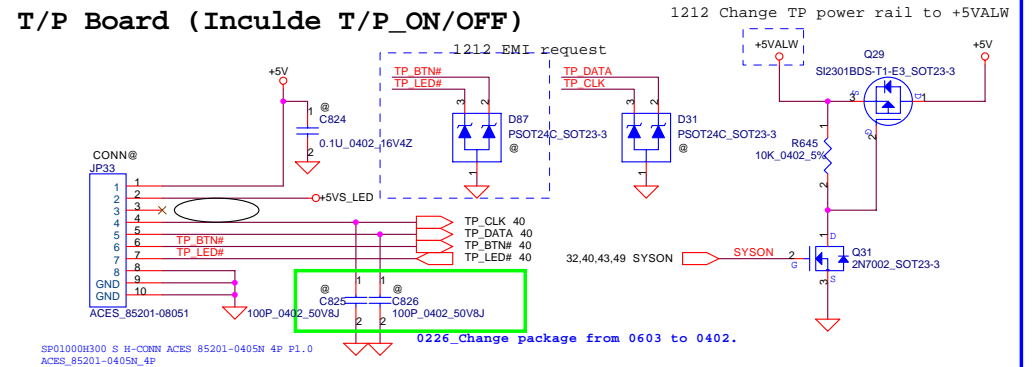
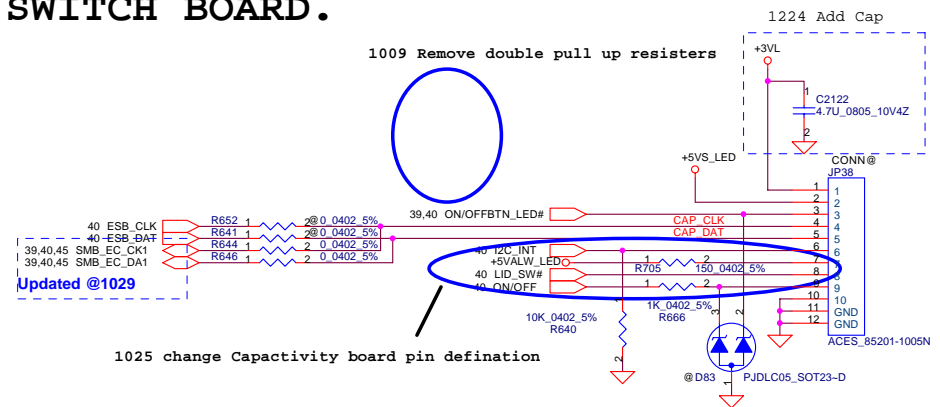


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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				Custom	0.1
Date: Wednesday, December 26, 2007 12:58 PM				Sheet	40 of 58

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```
1212 Delete SW5,SW6
```



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					Custom	LA-4082P Vader Discrete	0.1
					Date:	Wednesday, December 26, 2007	Sheet

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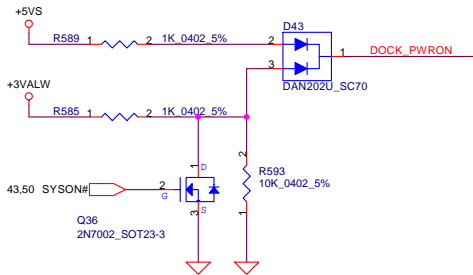
Atlas/ Saturn Dock

DOCK_PWR_ON Spec

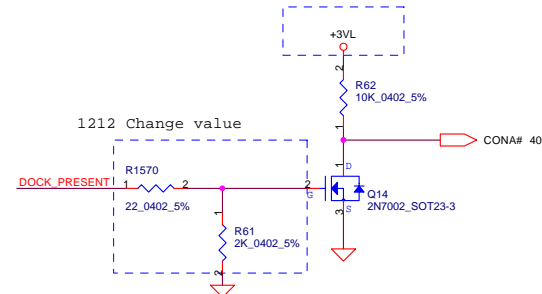
0V = Notebook S4/S5, Dock off

2.5V = Notebook S3, Dock on

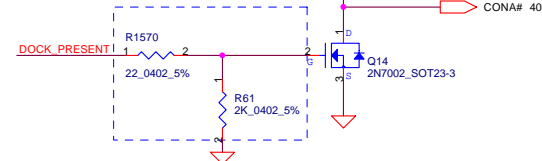
4V = Notebook S0, Dock on



1112 Change power rail from +3VALW to +3VL



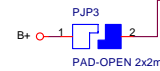
1212 Change value



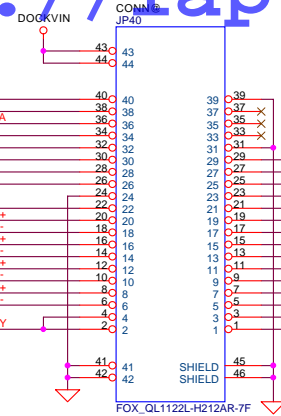
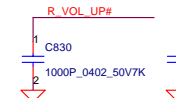
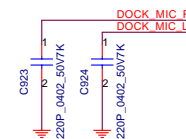
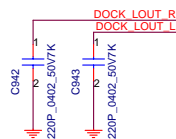
1009 Remove TV components

16 GREEN
16 RED
16 D_DDCDATA
16 BLUE
16 D_HSYNC
16 D_DDCCLK
28 USB20_N3
16 D_VSYNC
28 USB20_P3
31 RJ45_MIDI3+
31 RJ45_MIDI3-
31 RJ45_MIDI2+
31 RJ45_MIDI2-
31 RJ45_MIDI1+
31 RJ45_MIDI1-
31 RJ45_MIDI0+
31 RJ45_MIDI0-

GREEN
RED
D_DDCDATA
BLUE
D_HSYNC
D_DDCCLK
D_VSYNC
RJ45_MIDI3+
RJ45_MIDI3-
RJ45_MIDI2+
RJ45_MIDI2-
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RJ45_MIDI0+
RJ45_MIDI0-
+V BATTERY

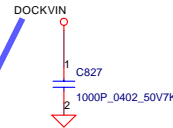


need change to reverse type connector

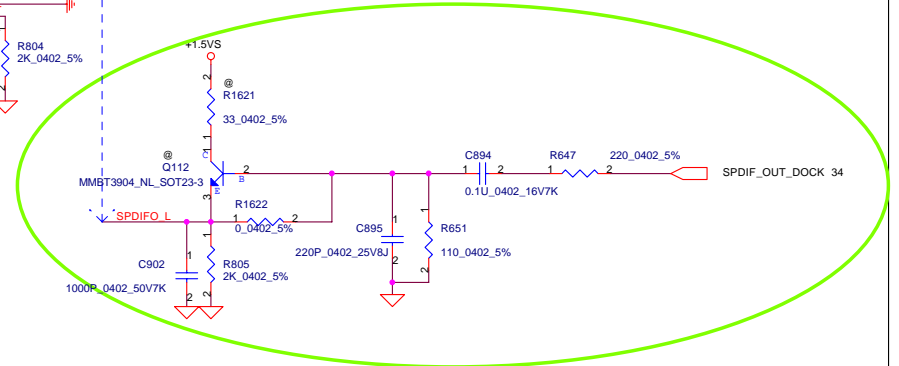


CIR_IN 36,40
MUTE_LED 40
DOKK_SLP_BTN# 40
JACK_DET# 34,36
R_VOL_UP# 2 200_0402_5%
R_VOL_DWN# 2 200_0402_5%
SPDIFO_L
AUDIO_OGND
DOKK_LOUT_R 36
DOKK_LOUT_L 36
DOKK_MIC_R_C
DOKK_MIC_L_C
AUDIO_ICND
DOKK_PRESENT

JACK_DET# 34,36
DOKK_VOL_UP# 40
DOKK_VOL_DWN# 40

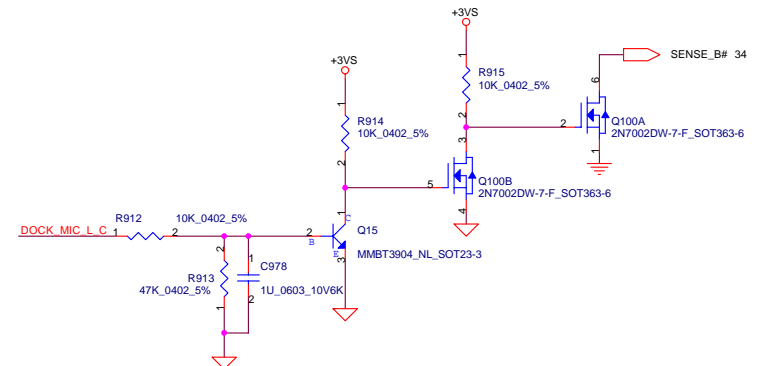
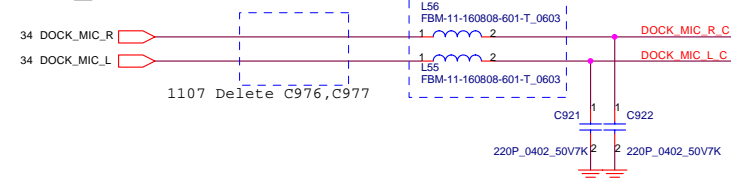


1009 Add pull up



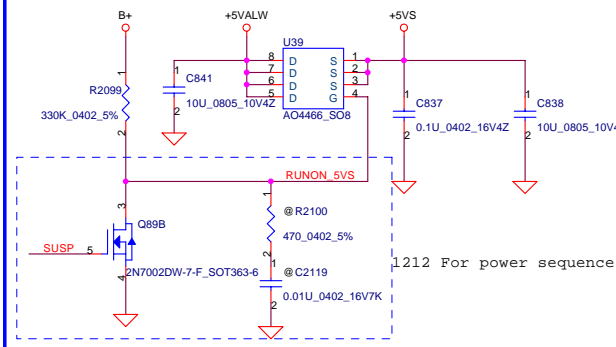
MIC_Dock

Need 600 Ohm 500 mA

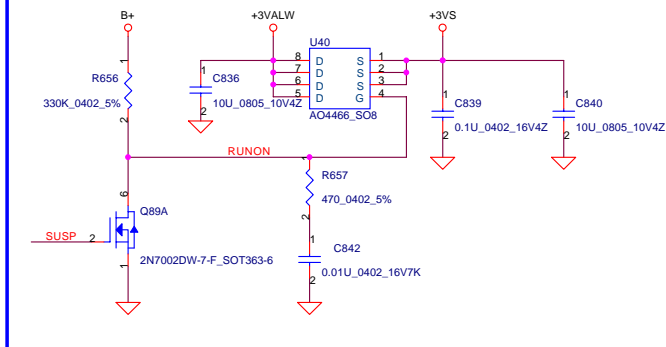


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				Custom	LA-4082P Vader Discrete
				Date	Wednesday, December 26, 2007
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				Rev	0.1

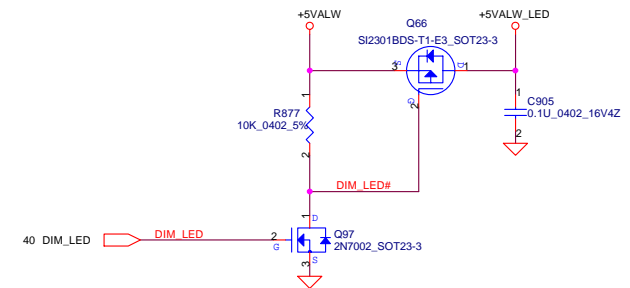
+5VALW to +5VS Transfer



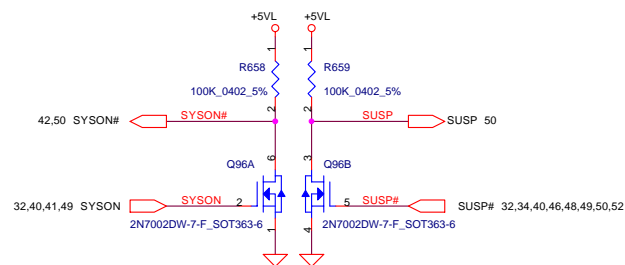
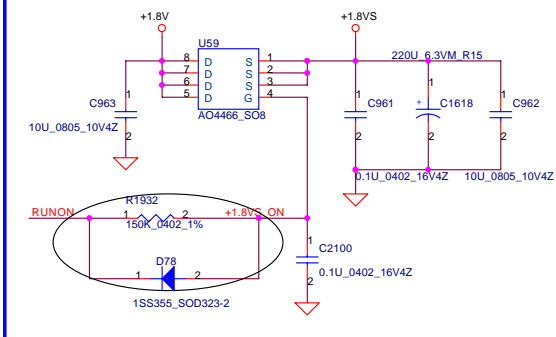
+3VALW to +3VS Transfer



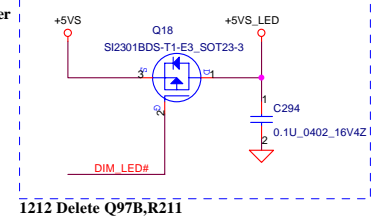
DIMM LED



+1.8V to +1.8VS Transfer



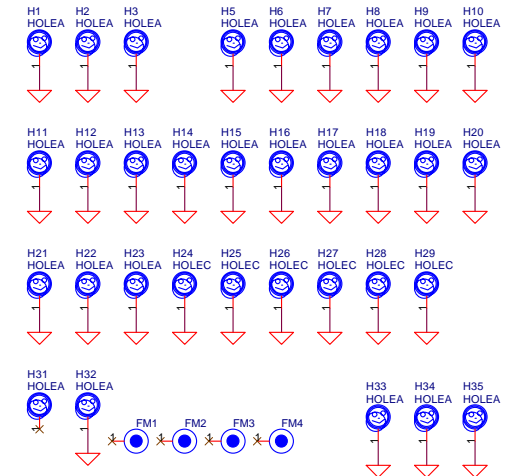
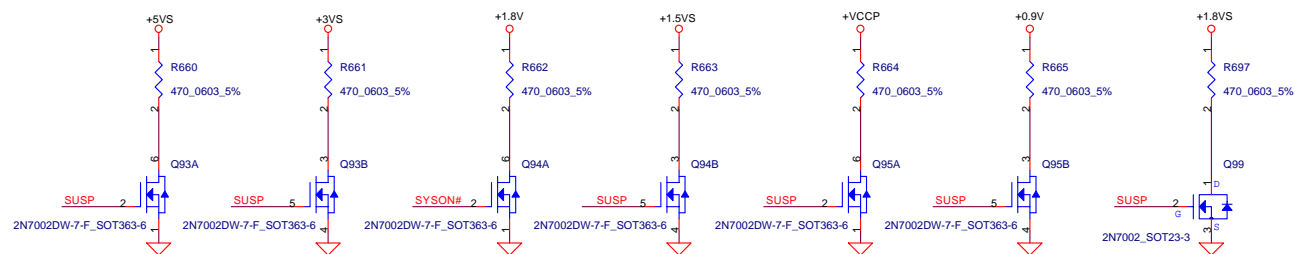
1009 Add for LED power



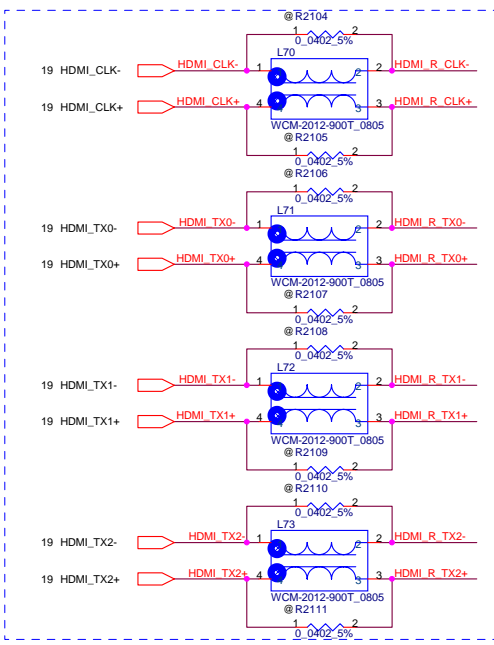
1212 Delete Q97B,R211

1212 Outline modify

Discharge circuit

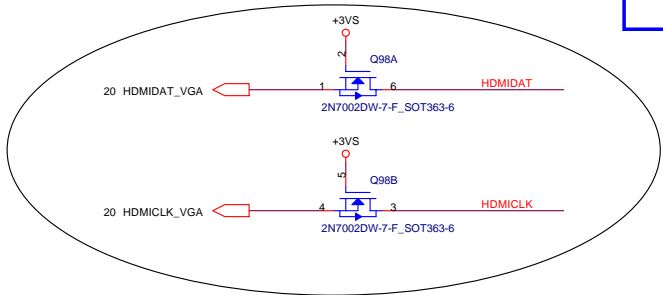
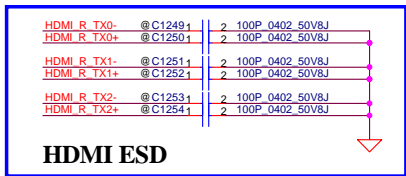
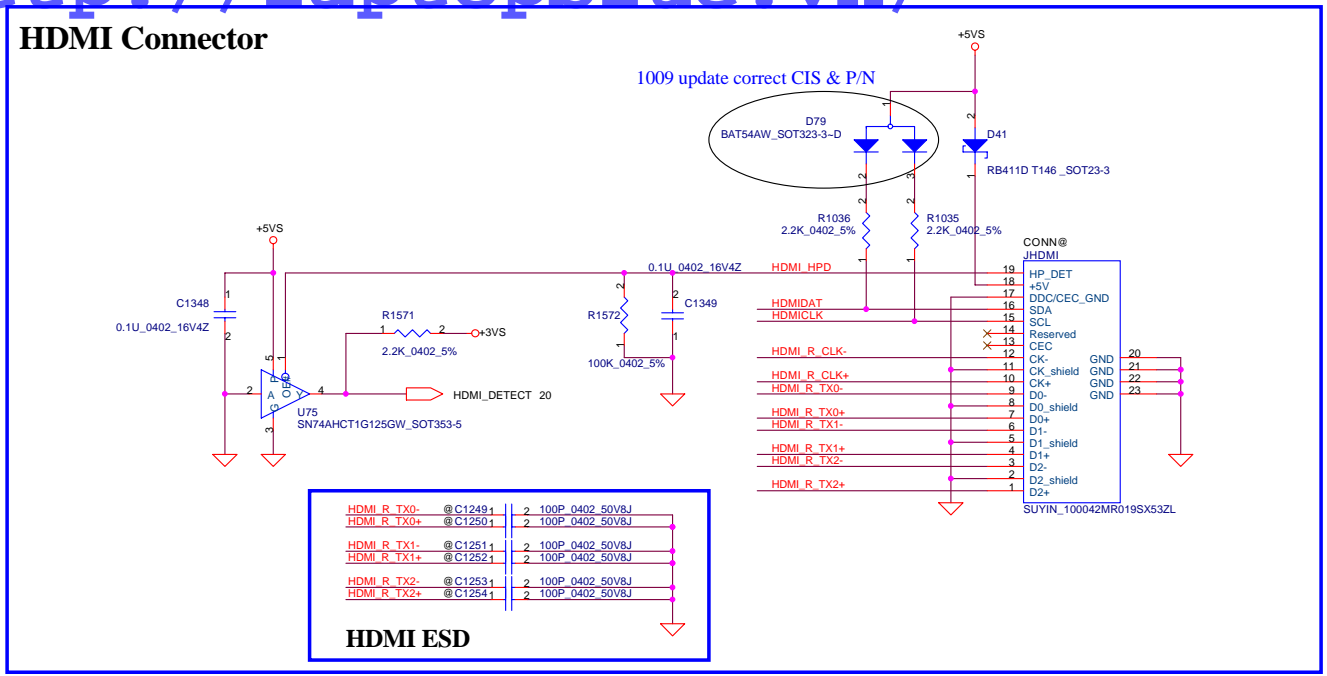


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				Custmr	LA-4082P Vader Discrete	0.1
				Date:	Wednesday, December 26, 2007	Sheet 43 of 58

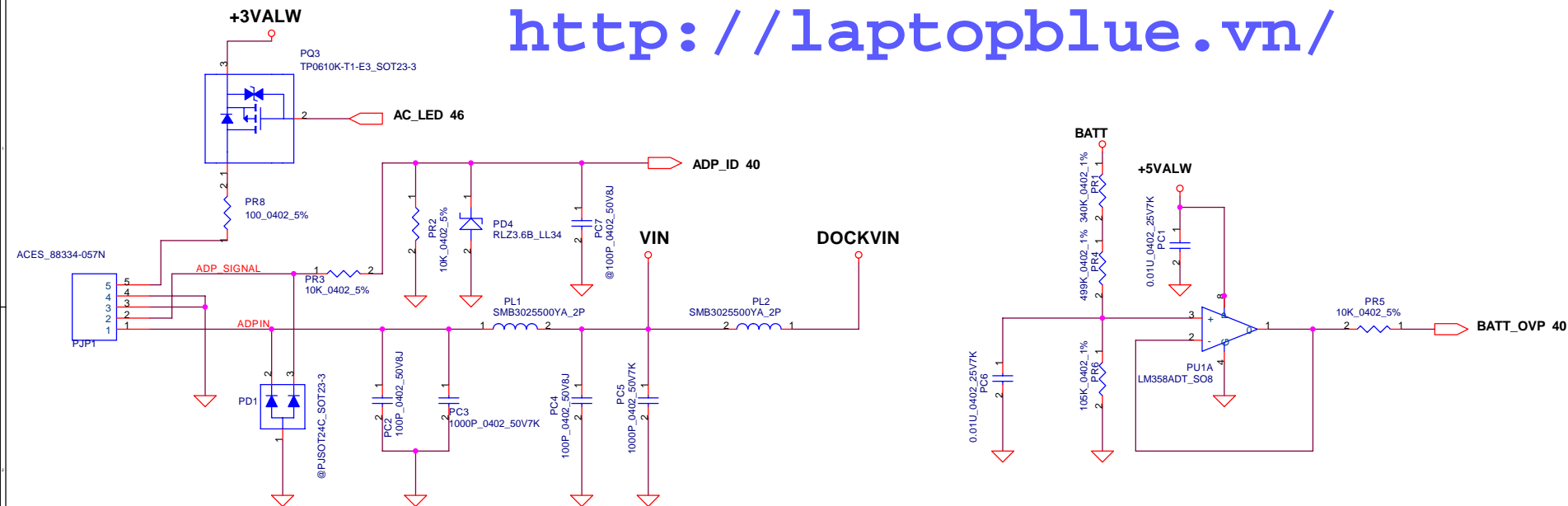


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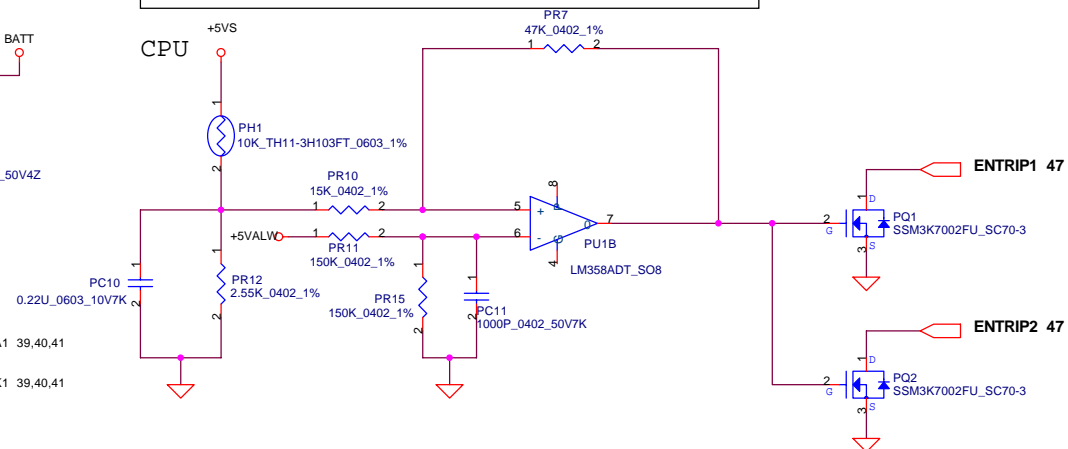
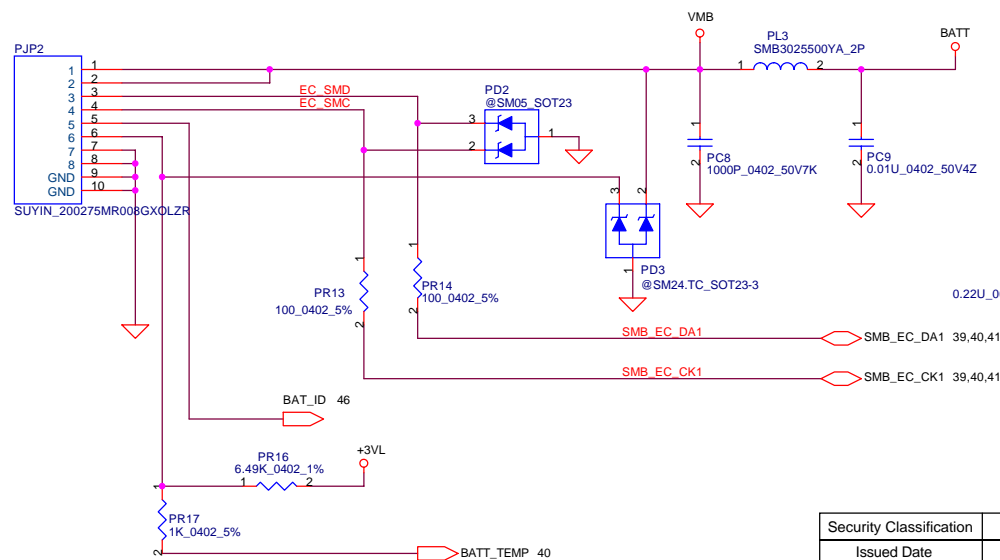
HDMI Connector



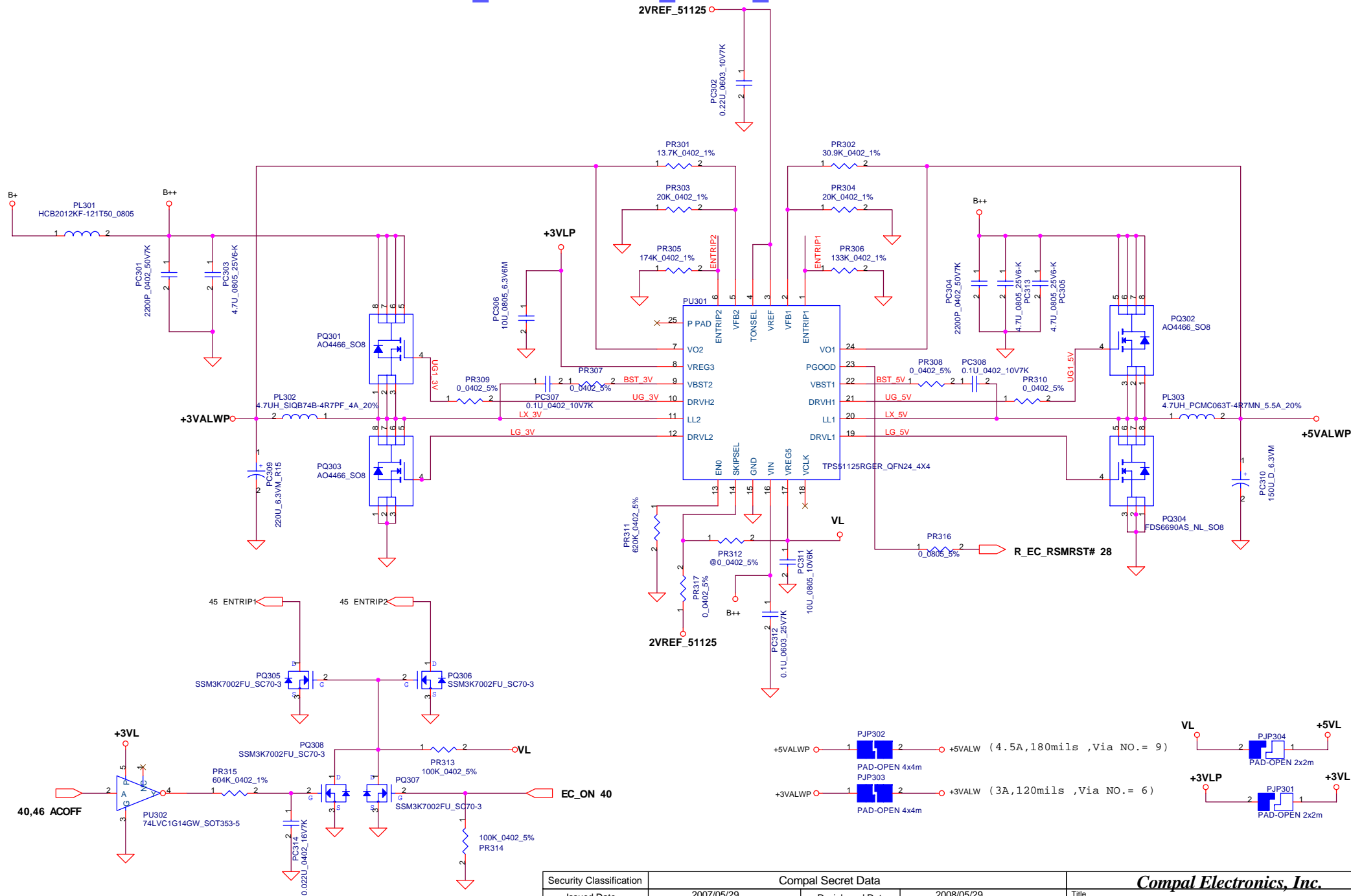
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				Custom	LA-4082P Vader Discrete
Date: Wednesday, December 26, 2007				Sheet	44 of 58
				Rev	0.1



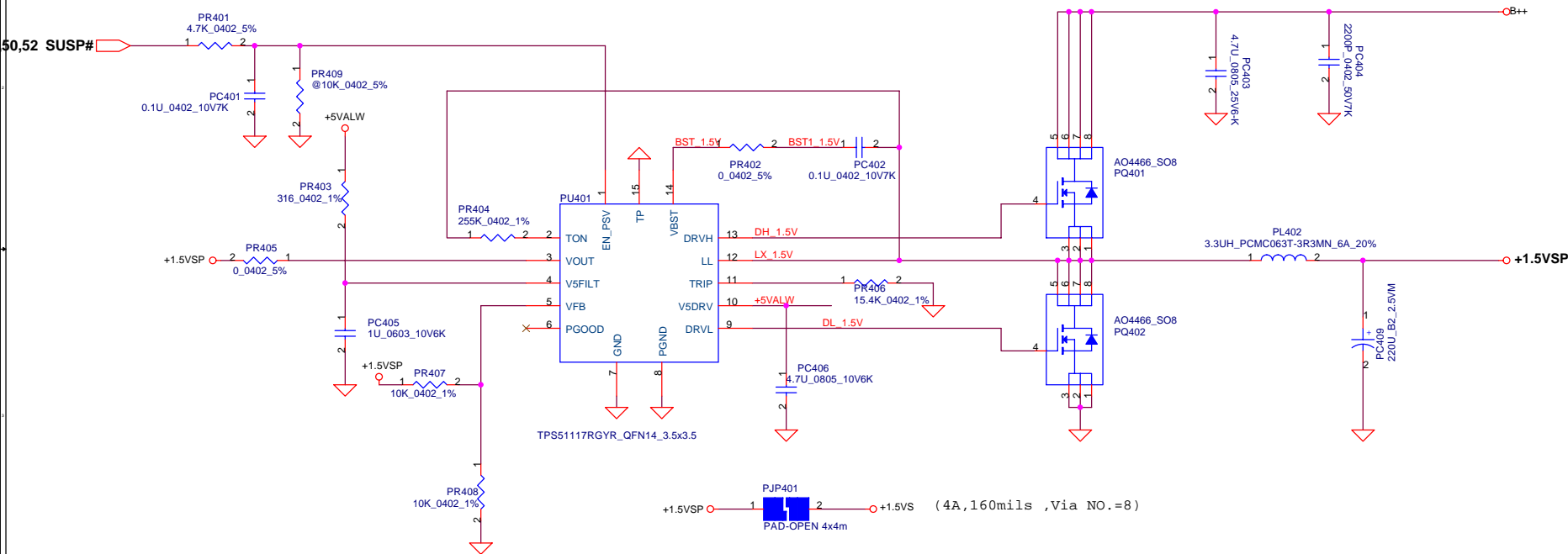
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



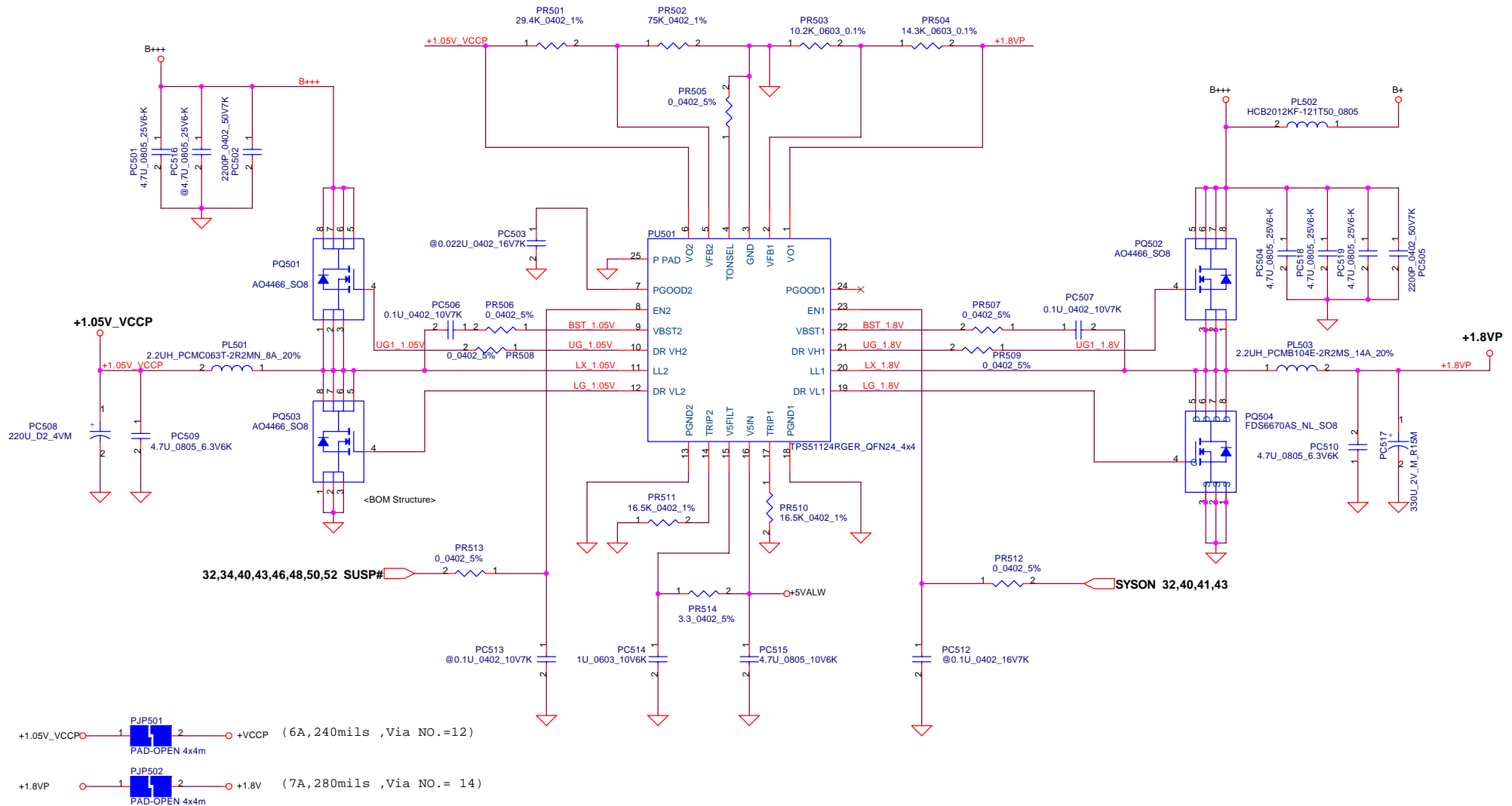
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/05/29	Deciphered Date	2008/05/29	DC Connector/CPU OTP Montevina Consumer Discrete		
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				Size	Document Number	Rev 0.1
				Date:	Wednesday, December 26, 2007	Sheet 45 of 58



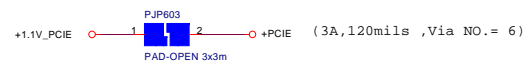
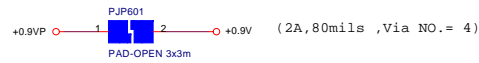
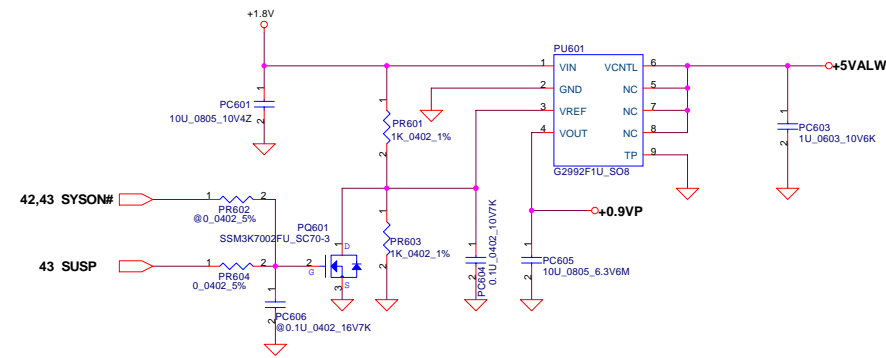
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				Montevina Consumer Discrete	
				Date	Wednesday, December 26, 2007
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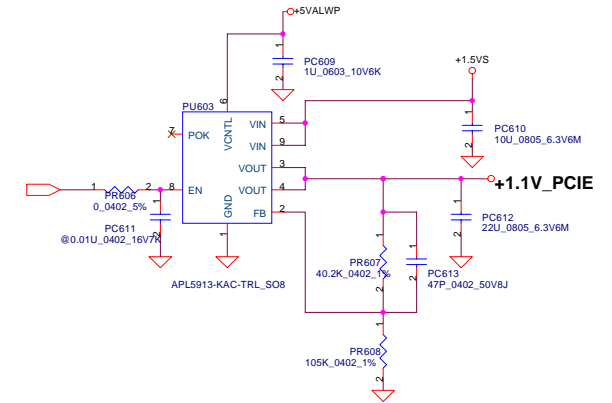
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	
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Size	Document Number	Montevina Consumer Discrete			Rev 0.1
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Size	Document Number	Montevina Consumer Discrete		Rev	0.1
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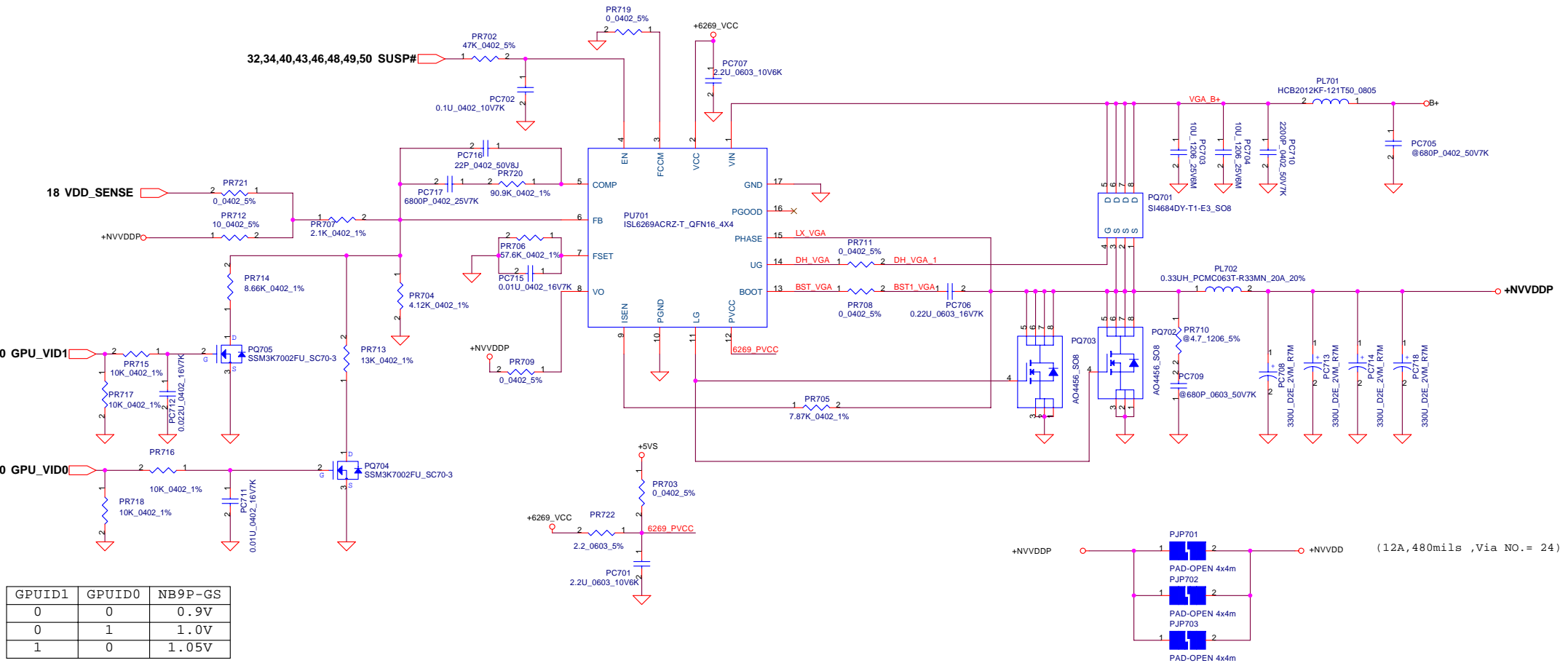


32,34,40,43,46,48,49,52 SUSP#



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Issued Date	2006/11/23	Deciphered Date	2007/11/23	Title		
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Size		Document Number		Montevina Consumer Discrete		
Date		Wednesday, December 26, 2007		Sheet	50	of 58

Security Classification	Compal Secret Data			Compal Electronics, Inc. CPU CORE		
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title		
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GPUID1	GPUID0	NB9P-GS
0	0	0.9V
0	1	1.0V
1	0	1.05V

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title VGA CORE		
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Date:				Wednesday, December 26, 2007	ISheet	52 of 58

Version Change List (P. I. R. List) for Power Circuit

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as luf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

<2007.10.08>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1	Fix Audio disappear	follow Intel SB design suggestion to separate HDA Bus	27	Add R439, R440, R442, R444	0.2
2		Add to determine board type and project	28	Add R777, R776, R774, R775	0.2
		Meet EC request	28	non-stuff R419, R695	
3	Fix Audio disappear	follow Intel SB design suggestion	29	Change power rail from +1.5v to +3v	0.2
4		meet SW debug request	32	Add Debug CLK and PLT_RST#	0.2
5	Fix Audio disappear	follow Intel HDA bus design for Discrete platform	34	Change codec power rail from +1.5v to +3v	0.2
6	Fix can not power on issue	Meet EC and SPI access sequence	39	change SPI power rail from+3valw to +3VL	0.2
7		Follow Intel design guide	7	Change R30 value	0.2
<2007.10.09> 1	Fix HDMI can not detect	follow Nvidia design request	18	change HDMI I2C channel to I2C B channel	0.2
2		Meet HP request to remove TV	18	Remove TV all components at VGA side	0.2
3		update ODD footprint	30	update JODD footprint	0.2
4	Fix ODD wrong pins	lower system power consumption	33	change Card Reader LED power rail	0.2
5		Meet Sub-woofer pwoer request	37	change D81, D82	0.2
6	Solve EC always damage	Solve EC always damage	40	change D53 direction	0.2
7		Double pull up and pwoer rail is different	41	Remove pull up resistors	0.2
8		lower system power consumption	41	change Cap-lock, HDD LED power rail	0.2
9		Meet HP request to remove TV	42	Remove TV all components at Dock side	0.2
10		lower system power consumption and meet LED status	43	Add +5VS_LED (Inculde DIM function)	0.2
11		solve HDMI pull up	44	update D79 footprint	0.2
<2007.10.19> 1		Meet ME limit area at KBC	27	Change Y4 material	0.2
2		Follow IDT suuggestion	35	change R886 to 1206	0.2
3		Follow Nvidia suggestion	25	Change R193, R196 size to 0603	0.2
<2007.10.20> 1		follow correct power rail	38	change Touch screen power rail	0.2
2		Meet HP request	39	Change ST G-sensor P/N & package	0.2
3		Meet HP request for WLAN &TV slot swap	32	Swapped WLAN and TV all support components	0.2
<2007.10.22> 1		Change LAN chip to meet Energy star spec	31	change LAN brand to Realtek	0.2
2					

<2007.10.23>

<2007.10.25>

<2007.10.31>

<2007.11.02>

Item	Fixed Issue	Reason for Change	PAGE	Modify List	M.B. Ver.
1	Fix USB loading of SB	follow 14" Blade USB channel design	28 17 32 38 38 42	Chnage all USB channel Change USB channel of Camera Change USB channel of WLAN & TV Tuner & New card Change USB channel of Left side, Right side, E-SATA Change USB channel of Touch screen, Finger print Change USB channel of Dock	0.2
2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2
3		Solve Speak no sound issue	36 36 34	add pullup at HP_DET# Change Q203 to N-channel FET Change R524 pin2 connect to JACK_DET#	0.2
1		Meet HP request for QC and DC co-lay	4 5 6	add GTLREF and XDP circuits	0.2
2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2
3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2
4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2
1			34	Use Audio Codec GPIO5 to shutdown Sub-woofer	
2			40	Connect HDA_RST#_CODEC to EC	
3			34	Separate SPDIF out to VGA and Docking	
1		Common design	16	R204,R205 no stuff	0.3
2		Change +5VS_LOGO resistor size to 0805	17	R642 size to 0805	0.3
3		Double pull up	20	R2046,R2047 no stuff	0.3
4		For card reader power	33	install R1553	0.3
5		For KBC C0 version	40	R616 no stuff	0.3
6		Add pull down resistor for SUSP# and SYSON	40	Change R615 to 8.2k and add R2062	0.3
7		Change HAD_RST#_CODEC from KBC pin 36 to pin 38	40		0.3
8		Change GSENSOR LED control pin from SB to KBC	41	Install R668, no install R667	0.3
9		Add pull down for sub-woofer power-down	37	Add R2063	0.3

<2007.11.04>

<2007.11.05>

<2007.11.06>

<2007.11.07>

<2007.11.08>

<2007.11.09>

<2007.11.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Move resistor from LS4086P to MB	41	Add R2064	0.3
2		Change to dual type for layout space	16	Change Q69,Q70 to dual type	0.3
3		Only use LIS302DLTR	39	U77, R2025 no install	0.3
4		Change CIR_IN power rail	40	Connect R642.1 to +5VL	0.3
1		nVIDIA suggestion for NB9M-GS/GE	22	R1005 change to 475 ohm	0.3
2		nVIDIA suggestion -- add Pull up 2.2K on HDMIDAT_VGA and HDMICLK_VGA to +3VS. at VGA side	18	Add R2065,R2066	0.3
1	EMI request	CRT add resistor for EMI	16	Add R2069,R2070,R2071	0.3
2		HP suggestion	34	Change C746,C747,C748,C749 to 1000PF	0.3
3		USB camere power and add GPO pin for shutdown	17	Add PJP5,R2072,R2073	0.3
4		LAN DSM support	31	1. USB camera - SB GPIO20 2. ISOLATE - SB GPIO18 3. LAN OGPIO - SB GPIO14	0.3
5		EC_BEEP	34	Add R2076	0.3
6		G-sensor LED control by SB	41	Delete R668	0.3
1		Modify FPR connector pin assignment	38	Modify JP41 pin assignment	0.3
2		Modify Audio	34 36 37 42	1. Add C2108,C2109,R2080,R2081 2. Add R2082,R2083 3. Change C1008,C1009 to 1UF 4. Delete C976,C977 5. Delete R515,R516,C916 6. Change C982,C980,C984 from 5900p to 0.039u 7. Change C983,C992 from 1000p to 100p 8. Add EC_MUTE# to sub-woofer shutdown pin and R2084	0.3
3		nVIDIA suggestion	20	1. Delete strap pin 2. Change R1020, R1015, R1010 to 475 ohm 3. Swap THERMDN and THERMDP	0.3
1		EMI request	17	Add C2100,C2111	0.3
2		Audio	36 37	Change C970,C971 to 22uF, add C2112, change D38 to dual type	0.3
1		nVIDIA suggestion	19 20	Change HDMI DDC to I2CD R387,R388,R415,R422,R427 -- install Change R415 to 10 ohm and no install Delete R99, Change +IFPC_PLLVDD to +PCIE	0.3
2		JMicron suggestion	33	Do not install R2030 Add D86 for card reader wake up Add SB GPIO22 for wake up event	0.3
1		HP request	4	Add EMC1403 for Qaud core	0.3

<2007.12.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		MV DG for VDDC_QDAC	10	Chagne VCCD_QDAC to +1.5VS	0.4
2		WLAN issue	32	Change XMIT_OFF#,WL_LED# and component to WLAN connector	0.4
3		PCIE issue	28	Swap GLAN and NewCard PCIE port	0.4
4		Modify CardReader LED	33	Use 2N7002 to control LED	0.4
5		KBC	40	Change SMB_EC_DA1,SMB_EC_CK1 power rail from +5VL to +3VL Add C2118 for KBC pin124 Chagne EC_THERM power rail to +3VS	0.4
6		WL_BLUE_LED# issue	41	Add R2089 pull up for WL_BLUE_LED#	0.4
7		Power sequence	43	Add R2099,R2100,C2119 and Q89 change to dual type	0.4
8		DIM_LED	43	Delete Q97B,R211	0.4
9		EC_PME#	40	Change EC_PME# power rail to +3VALW	0.4
10		WLAN issue	28	Add R2101	0.4
11		Change TP power rail	41	Change TP power rail to +5VALW	0.4
12		G-sensor	41	G-sensor -- R2031 change to 470 ohm and pull up to +3VS	0.4
13		For Dock present	42	R1570 change to 22 ohm,R61 change to 2K ohm	0.4
14		Clock generator	15	Add series R2102,R2103 for 27M_SSC and 27M_CLK	0.4
15		HDCP ROM	19	R951 pull up,R959 no install	0.4
16		EMI request	17	C272,C273,C2120 -- 470pF C228,C798 -- 10pF C2111 -- 220pF Add D87	0.4
17		Modify BT/FPR circuit	38		0.4
1		HP request	36 37	Change value	0.4
1		For ENE cap board EMI issue	40	Add R and C	0.4

<2007.12.24>

<2007.12.25>

1	JAL50 power sequence AC mode			96.09.03.
2		Vin		
3		B+		
4		+3VL		
5		+5VALW/+3VALW		
6		RSMRST#	→ T1 ←	T1, >1ms, +3VALW to RSMRST#
8		ON/OFF#	→ T12 ←	T12, User define
10	PWRBTN_O UT→SB	PWRBTN_OUT#	→ T13 ← → T14 ←	T13, 150ms, T14, 100ms
11	SB→EC	SLP_S5#	→ T2 ←	T2, <110ms, RSMRST# to SLP_S5#
12	SB→EC	SLP_S4#	→ T3 ←	T3, 1~16 RTOCLK, SLP_S5# to SLP_S4#
14	EC→Power	SYSON	→ T4 ←	T4, 10ms, SLP_S3# to SYSON
15		+1.8V		
16	SB→EC	SLP_S3#	→ T5 ←	T5, 1~16 RTOCLK, SLP_S4# to SLP_S3#
18	EC→Power	SUSP#	→ T6 ←	T6, 20ms, SLP_S3# to SUSP#
19		+5VS/+3VS/+1.5VS/+VCCP		
20	EC→Power	VR_ON	→ T7 ←	T7, 30ms, SLP_S3# to VR_ON
21		+CPU_CORE		
22	Power→EC	VGATE(VRMPWRGD)		
24		(CLPWROK) M_PWROK	→ T8 ←	T8, 30ms, SLP_S3# to M_PWROK
25		CL_RST#	→ T9 ←	T9, >500us, M_PWROK to CL_RST#
26		CL_PWRGD	→ T10 ←	T10, 0~100ns, VRMPWRGD to CL_PWRGD
27		PM_PWROK (SB_PWROK)		
28		H_PWRGOOD		
29		PLT_RST#(PCI_RST#)		
30		H_RESET#	→ T11 ←	T11, >1ms, PLT_RST# to H_RESET#