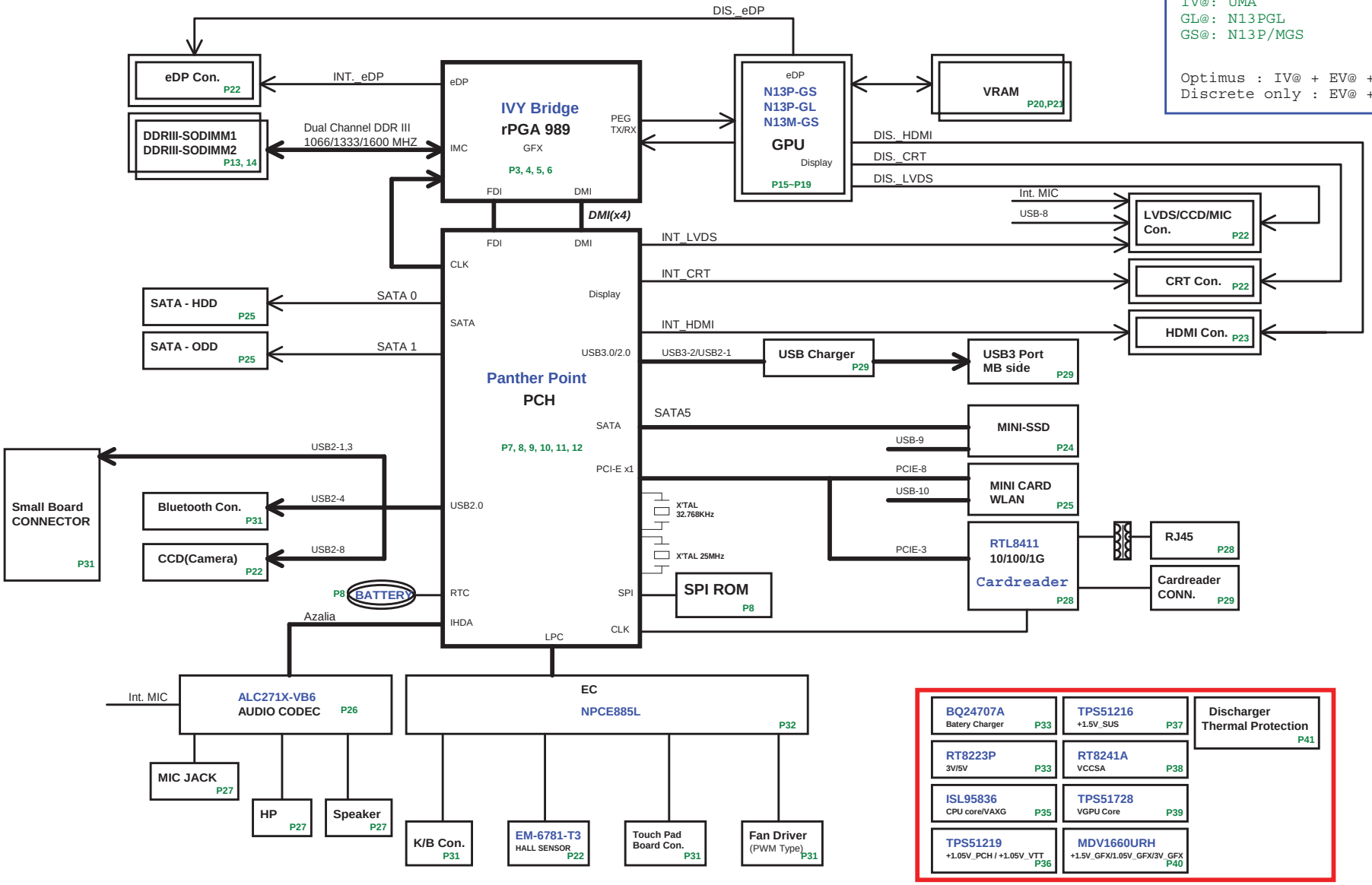
ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

BOM

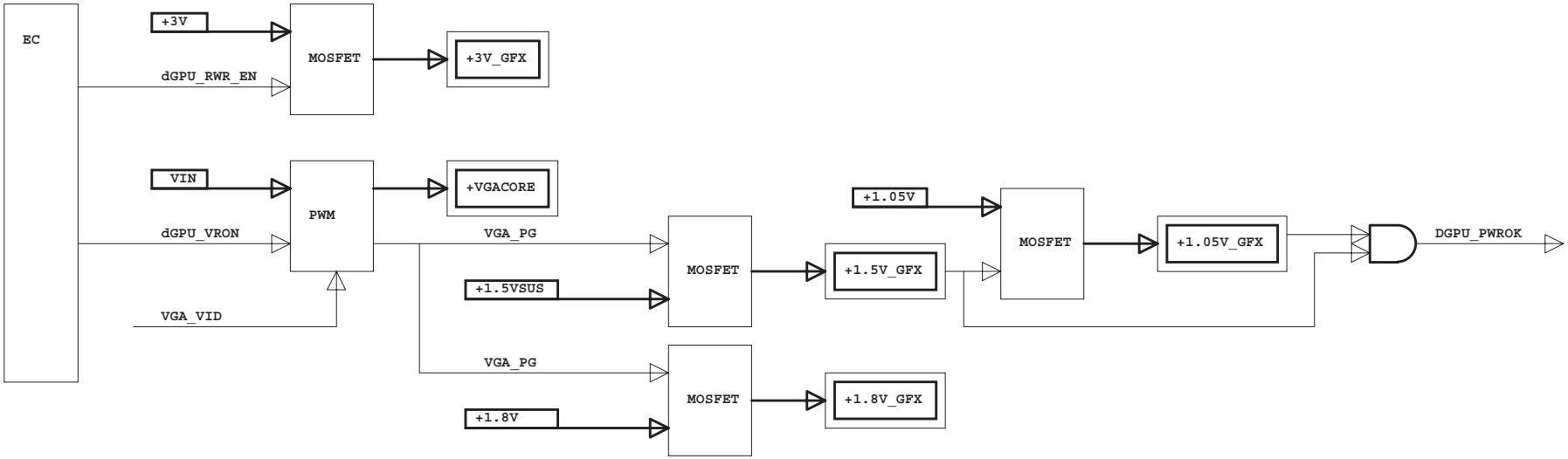
IV@ : iGPU
EV@ : dGPU
OP@ : Optimus
DO@ : Discrete only
SP@ : Special
SNP@: N13PGS/GL
IV@: UMA
GL@: N13PGL
GS@: N13P/MGS

Optimus : IV@ + EV@ + OP@
Discrete only : EV@ + DO@



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Block Diagram
Size | Document Number | Rev 1A
Date: Friday, November 11, 2011 | Sheet 1 of 44

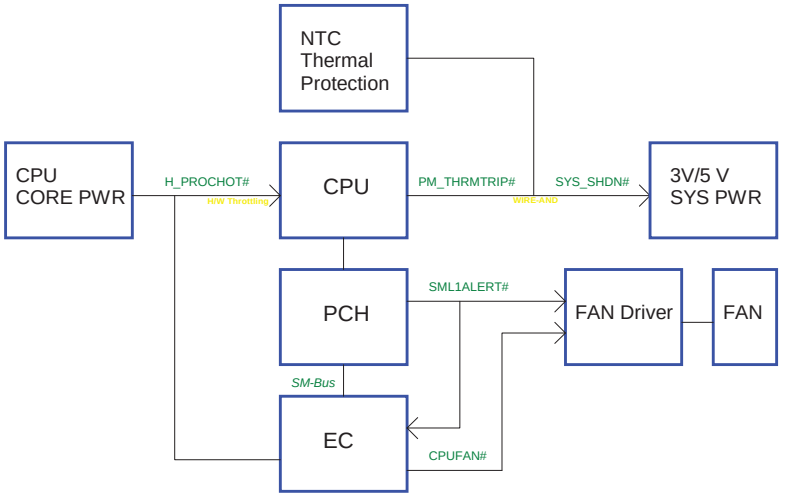
VGA power up sequence



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Friday, November 11, 2011 Sheet 2 of 44

IVY Bridge Processor (DMI,PEG,FDI)

U16A

DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 E20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

DMI

FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]
FDI_FSYNC0 J18 FDI0_FSYNC
FDI_FSYNC1 J17 FDI1_FSYNC
FDI_INT H20 FDI_INT
FDI_LSYNC0 J19 FDI0_LSYNC
FDI_LSYNC1 H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP A18 eDP_COMPIO
A17 eDP_ICOMPO
INT_eDP_HPD_Q B16 eDP_HPD
EDP-AUX+ C15 eDP_AUX
EDP-AUX- D15 eDP_AUX#
EDP-ML0+ C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
EDP-ML0- C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
E15 eDP_TX#[3]

TP59 TP58

eDP

PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0] K33 PEG_RX#0 [15]
PEG_RX#[1] M35 PEG_RX#1 [15]
PEG_RX#[2] L34 PEG_RX#2 [15]
PEG_RX#[3] J35 PEG_RX#3 [15]
PEG_RX#[4] J32 PEG_RX#4 [15]
PEG_RX#[5] H34 PEG_RX#5 [15]
PEG_RX#[6] H31 PEG_RX#6 [15]
PEG_RX#[7] G33 PEG_RX#7 [15]
PEG_RX#[8] G30 PEG_RX#8 [15]
PEG_RX#[9] F35 PEG_RX#9 [15]
PEG_RX#[10] E34 PEG_RX#10 [15]
PEG_RX#[11] E32 PEG_RX#11 [15]
PEG_RX#[12] D33 PEG_RX#12 [15]
PEG_RX#[13] D31 PEG_RX#13 [15]
PEG_RX#[14] B33 PEG_RX#14 [15]
PEG_RX#[15] C32 PEG_RX#15 [15]

PEG_RX[0] J33 PEG_RX0 [15]
PEG_RX[1] L35 PEG_RX1 [15]
PEG_RX[2] K34 PEG_RX2 [15]
PEG_RX[3] H35 PEG_RX3 [15]
PEG_RX[4] H32 PEG_RX4 [15]
PEG_RX[5] G34 PEG_RX5 [15]
PEG_RX[6] G31 PEG_RX6 [15]
PEG_RX[7] F33 PEG_RX7 [15]
PEG_RX[8] F30 PEG_RX8 [15]
PEG_RX[9] E35 PEG_RX9 [15]
PEG_RX[10] E33 PEG_RX10 [15]
PEG_RX[11] E32 PEG_RX11 [15]
PEG_RX[12] D34 PEG_RX12 [15]
PEG_RX[13] E31 PEG_RX13 [15]
PEG_RX[14] C33 PEG_RX14 [15]
PEG_RX[15] B32 PEG_RX15 [15]

PCI EXPRESS* - GRAPHICS

PEG_TX#[0] M29 R_PEG_TX#0 C395 EV@0.22u/6.3V_4 PEG_TX#0 [15]
PEG_TX#[1] M32 R_PEG_TX#1 C400 PEG_TX#1 [15]
PEG_TX#[2] M31 R_PEG_TX#2 C402 PEG_TX#2 [15]
PEG_TX#[3] L32 R_PEG_TX#3 C405 PEG_TX#3 [15]
PEG_TX#[4] L29 R_PEG_TX#4 C407 PEG_TX#4 [15]
PEG_TX#[5] K31 R_PEG_TX#5 C413 PEG_TX#5 [15]
PEG_TX#[6] K28 R_PEG_TX#6 C414 PEG_TX#6 [15]
PEG_TX#[7] J30 R_PEG_TX#7 C418 PEG_TX#7 [15]
PEG_TX#[8] J28 R_PEG_TX#8 C421 PEG_TX#8 [15]
PEG_TX#[9] H29 R_PEG_TX#9 C424 PEG_TX#9 [15]
PEG_TX#[10] G27 R_PEG_TX#10 C425 PEG_TX#10 [15]
PEG_TX#[11] E29 R_PEG_TX#11 C430 PEG_TX#11 [15]
PEG_TX#[12] F27 R_PEG_TX#12 C431 PEG_TX#12 [15]
PEG_TX#[13] D28 R_PEG_TX#13 C434 PEG_TX#13 [15]
PEG_TX#[14] F26 R_PEG_TX#14 C439 PEG_TX#14 [15]
PEG_TX#[15] E25 R_PEG_TX#15 C440 PEG_TX#15 [15]

PEG_TX[0] M28 R_PEG_TX0 C398 EV@0.22u/6.3V_4 PEG_TX0 [15]
PEG_TX[1] M33 R_PEG_TX1 C401 PEG_TX1 [15]
PEG_TX[2] M30 R_PEG_TX2 C404 PEG_TX2 [15]
PEG_TX[3] L31 R_PEG_TX3 C406 PEG_TX3 [15]
PEG_TX[4] L28 R_PEG_TX4 C408 PEG_TX4 [15]
PEG_TX[5] K30 R_PEG_TX5 C409 PEG_TX5 [15]
PEG_TX[6] K27 R_PEG_TX6 C417 PEG_TX6 [15]
PEG_TX[7] J29 R_PEG_TX7 C419 PEG_TX7 [15]
PEG_TX[8] J27 R_PEG_TX8 C420 PEG_TX8 [15]
PEG_TX[9] H28 R_PEG_TX9 C422 PEG_TX9 [15]
PEG_TX[10] G28 R_PEG_TX10 C427 PEG_TX10 [15]
PEG_TX[11] E28 R_PEG_TX11 C428 PEG_TX11 [15]
PEG_TX[12] F28 R_PEG_TX12 C433 PEG_TX12 [15]
PEG_TX[13] D27 R_PEG_TX13 C436 PEG_TX13 [15]
PEG_TX[14] E26 R_PEG_TX14 C437 PEG_TX14 [15]
PEG_TX[15] D25 R_PEG_TX15 C444 PEG_TX15 [15]

Ivy Bridge_rPGA_2DPC_Rev0p61

HPD disable

This signal can be left as no connect if entire eDP interface is disabled.

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

For Sandy Bridge processor only implementation:
PROC_SELECT can be left NC.

For IVY/Sandy processor compatibility:
Needs a pull-up resistor to PCH VccDFTERM rail (1.8V) through a 2.2 K±5% pull-up resistor.
Connect to the DF_TVS of PCH though a 1K±5% series resistor.

IVY Bridge Processor (CLK,MISC,JTAG)

wo eDP and dGPU
Connect DPLL_REF_SSCLK on Processor to GND through 1K ± 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K ± 5% resistor

U16B

[8] H_SNB_IVB# H_SNB_IVB# C26 PROC_SELECT#
TP45 SKTOCC# AN34 SKTOCC#

MISC

BCLK A28 CLK_CPU_BCLKP CLK_CPU_BCLKP [9]
BCLK# A27 CLK_CPU_BCLKN CLK_CPU_BCLKN [9]
DPLL_REF_CLK A16 CLK_DPLL_SSCLKP_R CLK_DPLL_SSCLKP [9]
DPLL_REF_CLK# A15 CLK_DPLL_SSCLKN_R CLK_DPLL_SSCLKN [9]

CLOCKS

TP11 TP_CATERR# AL33 CATERR#
[32] EC_PECI AN33 PECI
[32,35] H_PROCHOT# H_PROCHOT# R124 56_4 H_PROCHOT#_R AL32 PROCHOT#
[10] PM_THRMTRIP# PM_THRMTRIP# AN32 THERMTRIP#

THERMAL

SM_DRAMRST# R8 CPU_DRAMRST# CPU_DRAMRST# [4]
SM_RCOMP[0] AK1 SM_RCOMP_0 R173 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R458 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R460 200/F_4

DDR3 MISC

CRB 1.0 : SM_RCOMP[2..0] W:20mils, S:15mils, L 500mils

Ra R440 1V@0_4P2R
Rb R442 DO@1K_4 +1.05V
Rc R438 DO@1K_4

	EV	UMA/OPT.
Ra	NA	0 ohm
Rb	1K	NA
Rc	1K	NA

Intel recommended UNCOREPWRGOOD routing on one layer

[7] PM_SYNC PM_SYNC AM34 PM_SYNC
apply C5205 for nosie
C165 0.1u/10V_4
[10] H_PWRGOOD H_PWRGOOD AP33 UNCOREPWRGOOD
R116 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V R107 75_4 R113 43_4 CPU_PLTRST#_R AR33 RESET#
CPU_PLTRST#
R115 *750/F_4
[9] PCI_PLTRST# R114 *1.5K/F_4

PWR MANAGEMENT

Ivy Bridge_rPGA_2DPC_Rev0p61

PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCLK
TMS AR27 PCH_JTAG_TMS
TRST# AP30 XDP_TRST#
TDI AR28 PCH_JTAG_TDI
TDO AP26 PCH_JTAG_TDO
DBR# AL35 XDP_DBRST# [7]
BPM#[0] AT28 XDP_BPM0
BPM#[1] AP29 XDP_BPM1
BPM#[2] AR30 XDP_BPM2
BPM#[3] AT30 XDP_BPM3
BPM#[4] AP32 XDP_BPM4
BPM#[5] AR31 XDP_BPM5
BPM#[6] AT31 XDP_BPM6
BPM#[7] AR32 XDP_BPM7

TP53 TP18 TP20 TP19 TP12 TP56 TP54 TP55 TP51 TP52 TP49 TP47 TP50 TP46

For XDP

U3 NC VCC IN GNDOUT 74LVC1G07GW
+3V
C167 0.1u/10V_4
CRB 1.0 : change to +3V(S0)

+3V_S5
C516 0.1u/10V_4
U18 74AHC1G09
[7] SYS_PWROK
[7] PM_DRAM_PWRGD
PM_DRAM_PWRGD_Q
+1.5V_CPU
R461 200/F_4
R459 130/F_4 PM_DRAM_PWRGD_R
R462 *39_4
Q30 *2N7002K
MAINON_ON_G
MAINON_ON_G [5,41]

FDI Disabling (Discrete Only)

9/26 add

FDI_INT
R444 DO@0_4 FDI_FSYNC0
R446 DO@0_4 FDI_FSYNC1
R443 DO@0_4 FDI_LSYNC0
FDI_LSYNC1
R441 DO@1K/F_4
R447 DO@1K/F_4

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation

+1.05V
Routed within 25 mils
R433 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V
Routed within 500 mils
R439 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)

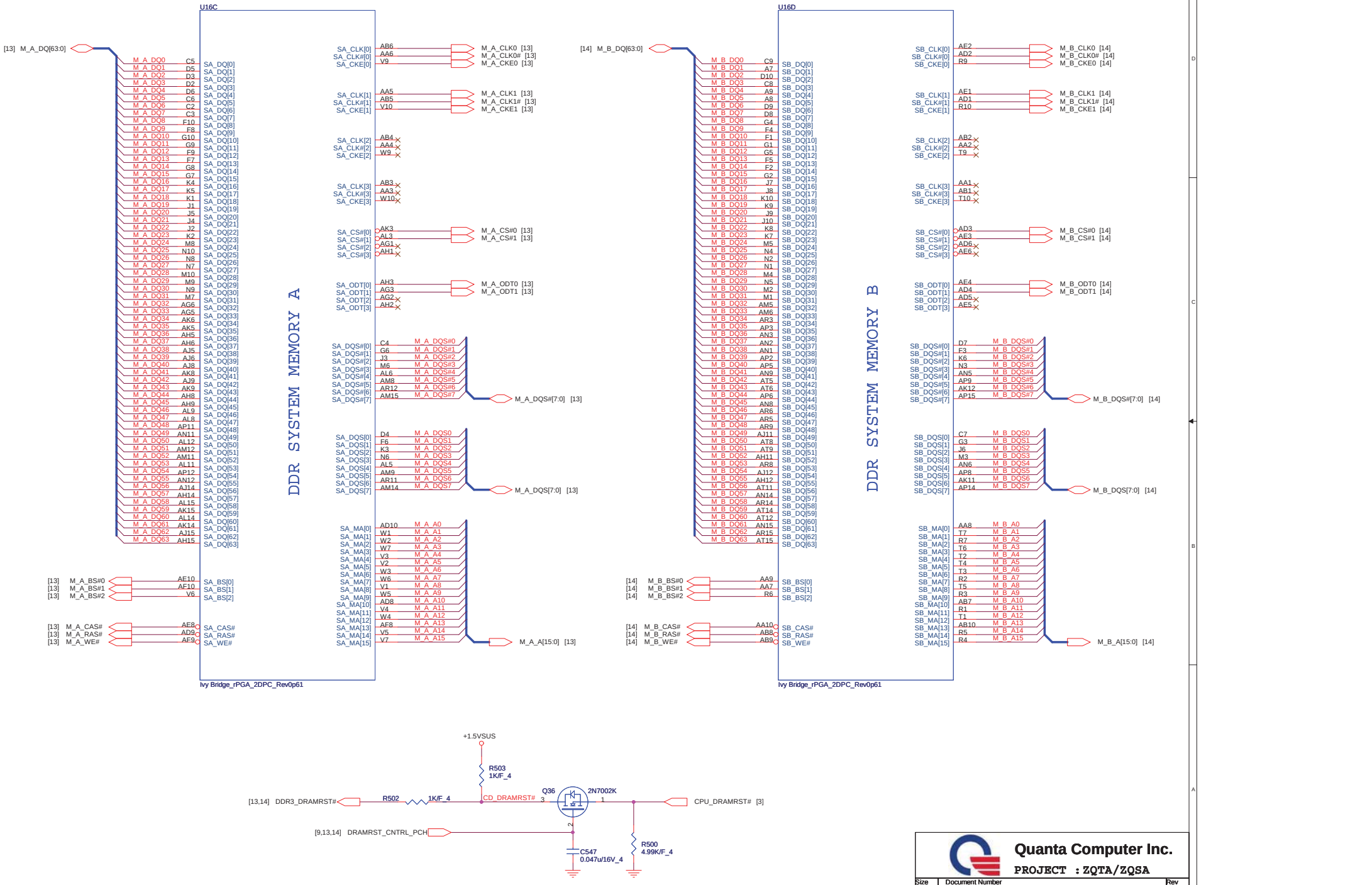
+1.05V
H_PROCHOT# R122 62_4
PCH_JTAG_TDO R134 51_4
PCH_JTAG_TMS R135 51_4
PCH_JTAG_TDI R430 51_4
XDP_PREQ# R132 *51_4
XDP_TCLK R137 51_4
XDP_TRST# R128 51_4
9/27 modify

[7,35] IMVP_PWRGD
Q4 FDV301N
R86 1K_4
PM_THRMTRIP#
Q5 MMBT3904
SYS_SHDN# [34,41]

[5,7,8,9,11,22,32,35,36,40,41] +1.05V
[7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size: Document Number: IVY Bridge 1/4 Rev: 1A
Date: Friday, November 11, 2011 Sheet 3 of 44

IVY Bridge Processor (DDR3)



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: IVY Bridge 2/4	Rev: 1A
Date: Friday, November 11, 2011	Sheet 4 of 44	

IVY Processor (POWER)

IVY Bridge Processor (GRAPHIC POWER)

CPU Core Power
IVY 45W:TDC 52A
IVY SPEC
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
total : 10uF x 10 , RSVD x 1
total : 22uF x 16 , RSVD x 3
tatal : 470u x 4, RSVD x2

SNB : Spec	Cose down
470uF/4mohm x 4	330uF x2
22uF x 16	22uF x 4
10uF x 10	10uF x 20 reserved x 5

CPU VTT
IVY 45W:1.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF x1
22uF x 12	22uF x 2
22uF x 7 (Non-stuff)	10uF x 10 reserved x 4

CPU VTT
IVY 45W:TDC 38A

Spec	Cose down	IVY SPEC
470uF/4mohm x 2	330uF x1	22uF_8 x2 Socket TOP cavity
22uF x 12	10uF x 10	22uF_8 x2 Socket BOT cavity
		22uF_8 x4 Socket TOP edge
		22uF_8 x4 Socket BOT edge
		470uF_7343 x2

POWER

0929 change value by CRB

U16F

CORE SUPPLY | PEG AND DDR | SVID | SENSE LINES

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

	DIS. VGA	UMA/ Optimus
Ra	0 ohm	NA

U16G

GRAPHICS | DDR3 - 1.5V RAILS | SA RAIL | 1.8V RAIL | MISC | SENSE LINES | VREF

IVY SPEC
330uF x1, 10uF_8 x6 Socket BOT edge.

For M3 solution need Rb4, Rd1 W/O M3 then NC ball B4 and D1

10 mil

Ivy Bridge_rPGA_2DPC_Rev0p61

CPU VCCPL
IVY 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

10uF (Reserved)

Voltage selection for VCCIO:
this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Trace Route to Power IC area.

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Remove PU resistor 54.9/F, stuff at IMVP7 page

Place PU resistor close to CPU

SVID DATA
Remove PU resistor 130/F, stuff at IMVP7 page

Place PU resistor close to CPU

SVID ALERT

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU SA
IVY 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

CPU MCH
IVY 45W: 5A

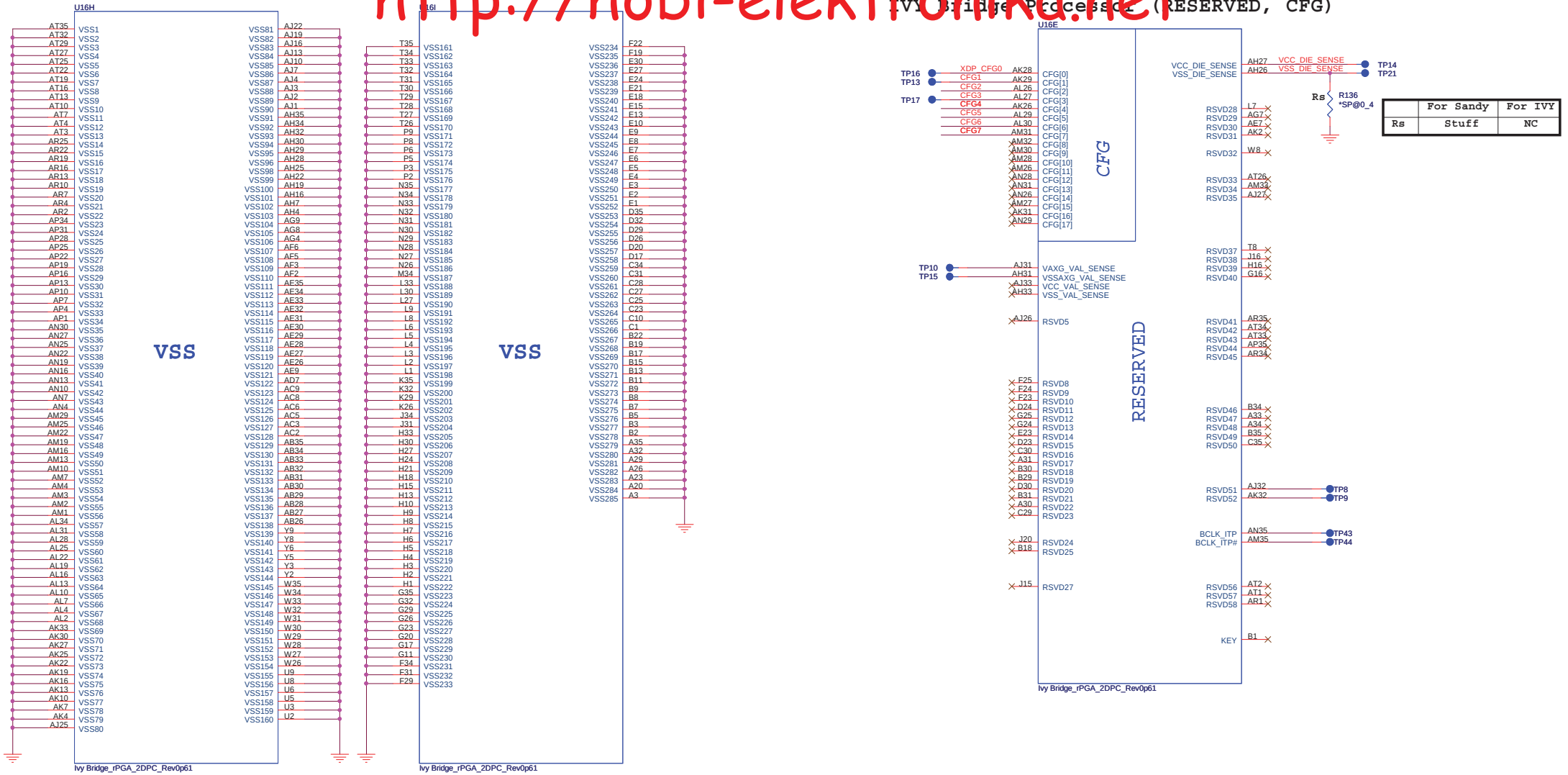
Spec	Real
330uF/6mohm x 1	10uF x 8
10uF x 6	

4.5A

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size: | Document Number: IVY Bridge 3/4 | Rev: 1A
Date: Friday, November 11, 2011 | Sheet 5 of 44

IVY Bridge Processor (VSS)

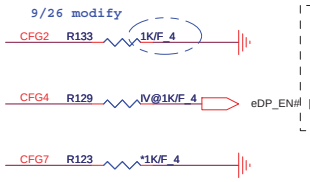
IVY Bridge Processor (RESERVED, CFG)

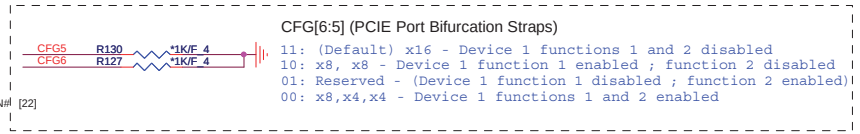


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training





Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	IVY Bridge 4/4	1A

Date: Friday, November 11, 2011 Sheet 6 of 44

[3,5,8,9,11,22,32,35,36,40,41] +1.05V
[3,8,9,10,11,15,28,30,31,34,35,36,41,42] +3V_S5
[3,5,8,9,11,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

CPT/PPT (DMI,FDI,PM)

U20C

DMI_RXN0 [3] BC24 DMI0RXN
DMI_RXN1 [3] BE20 DMI1RXN
DMI_RXN2 [3] BG18 DMI2RXN
DMI_RXN3 [3] BG20 DMI3RXN
DMI_RXP0 [3] BE24 DMI0RXP
DMI_RXP1 [3] BC20 DMI1RXP
DMI_RXP2 [3] BJ18 DMI2RXP
DMI_RXP3 [3] BJ20 DMI3RXP
DMI_TXN0 [3] AW24 DMI0TXN
DMI_TXN1 [3] AW20 DMI1TXN
DMI_TXN2 [3] BB18 DMI2TXN
DMI_TXN3 [3] AV18 DMI3TXN
DMI_TXP0 [3] AY24 DMI0TXP
DMI_TXP1 [3] AY20 DMI1TXP
DMI_TXP2 [3] AY18 DMI2TXP
DMI_TXP3 [3] AU18 DMI3TXP
DMI_ZCOMP BJ24
+1.05V R521 49.9/F_4 DMI_COMP BG25 DMI_IRCOMP
R527 750/F_4 BH21 DMI2RBIAS

DMI

FDI_RXN0 BJ14 FDI_TXN0 [3]
FDI_RXN1 AY14 FDI_TXN1 [3]
FDI_RXN2 BE14 FDI_TXN2 [3]
FDI_RXN3 BH13 FDI_TXN3 [3]
FDI_RXN4 BC12 FDI_TXN4 [3]
FDI_RXN5 BJ12 FDI_TXN5 [3]
FDI_RXN6 BG10 FDI_TXN6 [3]
FDI_RXN7 BG9 FDI_TXN7 [3]
FDI_RXP0 BG14 FDI_TXP0 [3]
FDI_RXP1 BB14 FDI_TXP1 [3]
FDI_RXP2 BF14 FDI_TXP2 [3]
FDI_RXP3 BG13 FDI_TXP3 [3]
FDI_RXP4 BE12 FDI_TXP4 [3]
FDI_RXP5 BG12 FDI_TXP5 [3]
FDI_RXP6 BJ10 FDI_TXP6 [3]
FDI_RXP7 BH9 FDI_TXP7 [3]
FDI_INT AW16 FDI_INT [3]
FDI_FSYNC0 AV12 FDI_FSYNC0 [3]
FDI_FSYNC1 BC10 FDI_FSYNC1 [3]
FDI_LSYNC0 AV14 FDI_LSYNC0 [3]
FDI_LSYNC1 BB10 FDI_LSYNC1 [3]

FDI

System Power Management

SUS_PWR_ACK R539 *0_4 SUSACK# C12 SUSACK#
[3] XDP_DBRST# XDP_DBRST# K3 SYS_RESET#
C607 *1u/10V_4
SYS_PWROK P12 SYS_PWROK
R583 *0_4 L22 PWROK +3V_S5
PWROK_EC L10 APWROK +3V_S5
[3] PM_DRAM_PWRGD PM_DRAM_PWRGD B13 DRAMPWROK +3V_S5
[32] PCH_RSMRST# PCH_RSMRST# C21 RSMRST#
SUS_PWR_ACK K16 SUSWARN#/SUSPWRDNACK/GPIO30 +3V_S5
[32] DNBSWON# E20 PWRBTN#
AC_PRESENT H20 ACPRESENT / GPIO31 DSW
PM_BATLOW# E10 BATLOW# / GPIO72 +3V_S5
PM_R# A10 R# +3V_S5

DSWVRMEN A18 DSWVREN [8]
DPWROK F22 PCH_RSMRST#
WAKE# B9 PCIE_WAKE# PCIE_WAKE# [28]
+3V CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# [32]
SUS_STAT# / GPIO61 G8 SUS_STAT# T15
SUSCLK / GPIO62 N14 PCH_SUSCLK T12
SLP_S5# / GPIO63 D10 PCH_SLP_S5# T14
SLP_S4# H4 SUSC# [32]
+3V_S5
SLP_S3# F4 SUSB# [32]
SLP_A# G10 SLP_A# SLP_A# [32]
10/31 modify
SLP_SUS# G16 SLP_SUS# T10
PMSYNCH AP14 PM_SYNC [3]
SLP_LAN# / GPIO29 K14 SLP_LAN#

PANTHER POINT

CRT,DPT (LVDS,DDI)

U20D

[22] INT_LVDS_BLON J47 L_BKLTEN
[22] INT_LVDS_DIGON M45 L_VDD_EN
[22] INT_LVDS_BRIGHT P45 L_BKLTCTL
[22] INT_LVDS_EDIDCLK T40 L_DDC_CLK
[22] INT_LVDS_EDIDDATA K47 L_DDC_DATA
+3V R164 2.2K_4 R188 2.2K_4 T45 L_CTRL_CLK P39 L_CTRL_DATA
R186 2.37K/F_4 T7 AF37 LVD_IBG AF36 LVD_VBG
AE48 LVD_VREFH AE47 LVD_VREFL

LVDS

[22] INT_TXLCLKOUT- AK39 LVDSA_CLK#
[22] INT_TXLCLKOUT+ AK40 LVDSA_CLK
[22] INT_TXLOUT0- AN48 LVDSA_DATA#0
[22] INT_TXLOUT1- AM47 LVDSA_DATA#1
[22] INT_TXLOUT2- AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
[22] INT_TXLOUT0+ AN47 LVDSA_DATA0
[22] INT_TXLOUT1+ AM49 LVDSA_DATA1
[22] INT_TXLOUT2+ AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 HDMI_DDCCLK_SW [23]
SDVO_CTRLDATA M39 HDMI_DDCDATA_SW [23]
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 HDMI_HP [23]
DDPB_0N AV42 INT_HDMITX2N_R RP18 3 IV@0_4P2R INT_HDMITX2N [23]
DDPB_0P AV40 INT_HDMITX2P_R 2 1 INT_HDMITX2P [23]
DDPB_1N AV45 INT_HDMITX1N_R RP19 3 IV@0_4P2R INT_HDMITX1N [23]
DDPB_1P AV46 INT_HDMITX1P_R 2 1 INT_HDMITX1P [23]
DDPB_2N AU48 INT_HDMITX0N_R RP20 3 IV@0_4P2R INT_HDMITX0N [23]
DDPB_2P AU47 INT_HDMITX0P_R 2 1 INT_HDMITX0P [23]
DDPB_3N AV47 INT_HDMICLK-_R RP21 3 IV@0_4P2R INT_HDMICLK- [23]
DDPB_3P AV49 INT_HDMICLK+_R 2 1 INT_HDMICLK+ [23]

INT. HDMI

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42 DDPC_HPD_PU
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT36
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

DDPC_HPD_PU R169 *2.2K_4
DDPD_HPD_PU R197 *2.2K_4
0 : Port not detected

Digital Display Interface

[22] INT_CRT_BLU N48 CRT_BLUE
[22] INT_CRT_GRN P49 CRT_GREEN
[22] INT_CRT_RED T49 CRT_RED
[22] INT_CRT_DDCCLK T39 CRT_DDC_CLK
[22] INT_CRT_DDCDAT M40 CRT_DDC_DATA

CRT

[22] INT_HSYNC R126 IV@33_4 INT_CRT_HSYNC_R M47 CRT_HSYNC
[22] INT_VSYNC R125 IV@33_4 INT_CRT_VSYNC_R M49 CRT_VSYNC
DAC_IREF T43 DAC_IREF
T42 CRT_IRTN
R187 1K/F_4

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36 DDPD_HPD_PU
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

PANTHER POINT

The required series-resistors are:
• Direct Connect - 33 Ω
• Docking Topology - 20 Ω

R place close to PCH
R483 IV@150/F_4 INT_CRT_BLU
R482 IV@150/F_4 INT_CRT_GRN
R484 IV@150/F_4 INT_CRT_RED

PCH Pull-high/low(CLG)

+3V
CLKRUN# R584 8.2K_4
XDP_DBRST# R567 4.99K/F_4
R554 *1K_4
PCH_RSMRST# R219 10K_4
SYS_PWROK R601 *10K_4

+3V_S5
CRB 1.0 change R8315 to 1K
PM_R# R545 10K_4
PM_BATLOW# R282 8.2K_4
PCIE_WAKE# R261 10K_4
SLP_LAN# R230 *10K_4
SUS_PWR_ACK R538 10K_4
AC_PRESENT R220 10K_4
PM_DRAM_PWRGD R232 200/F_4
wo S3 leakage, remove R

System PWR_OK(CLG)

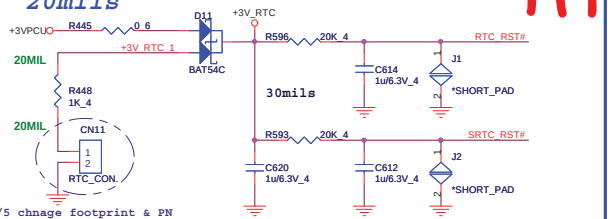
IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again

+3V_S5
C629 *0.1u/10V_4
to PCH Pin12, XDP and EE debug
[3] SYS_PWROK SYS_PWROK
U24 TC7SH08FU
IMVP_PWRGD [3,35]
PWROK_EC [32]
R594 100K_4

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
Panther Point 1/6
Rev 1A
Date: Friday, November 11, 2011
Sheet 7 of 44

RTC Circuitry(RTC)

20mils

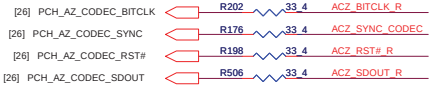


10/5 chnage footprint & PN

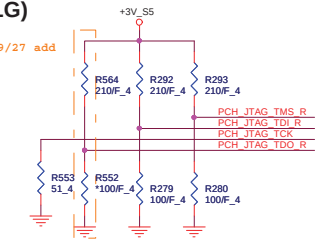
CN13 DFWF02MS118

battery AHL03003022 AHL03003024

HDA Bus(CLG)

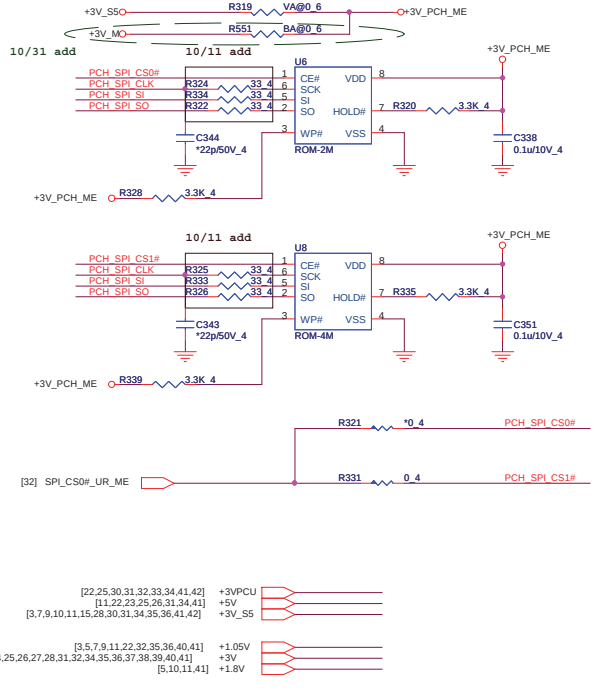


PCH JTAG Debug (CLG)

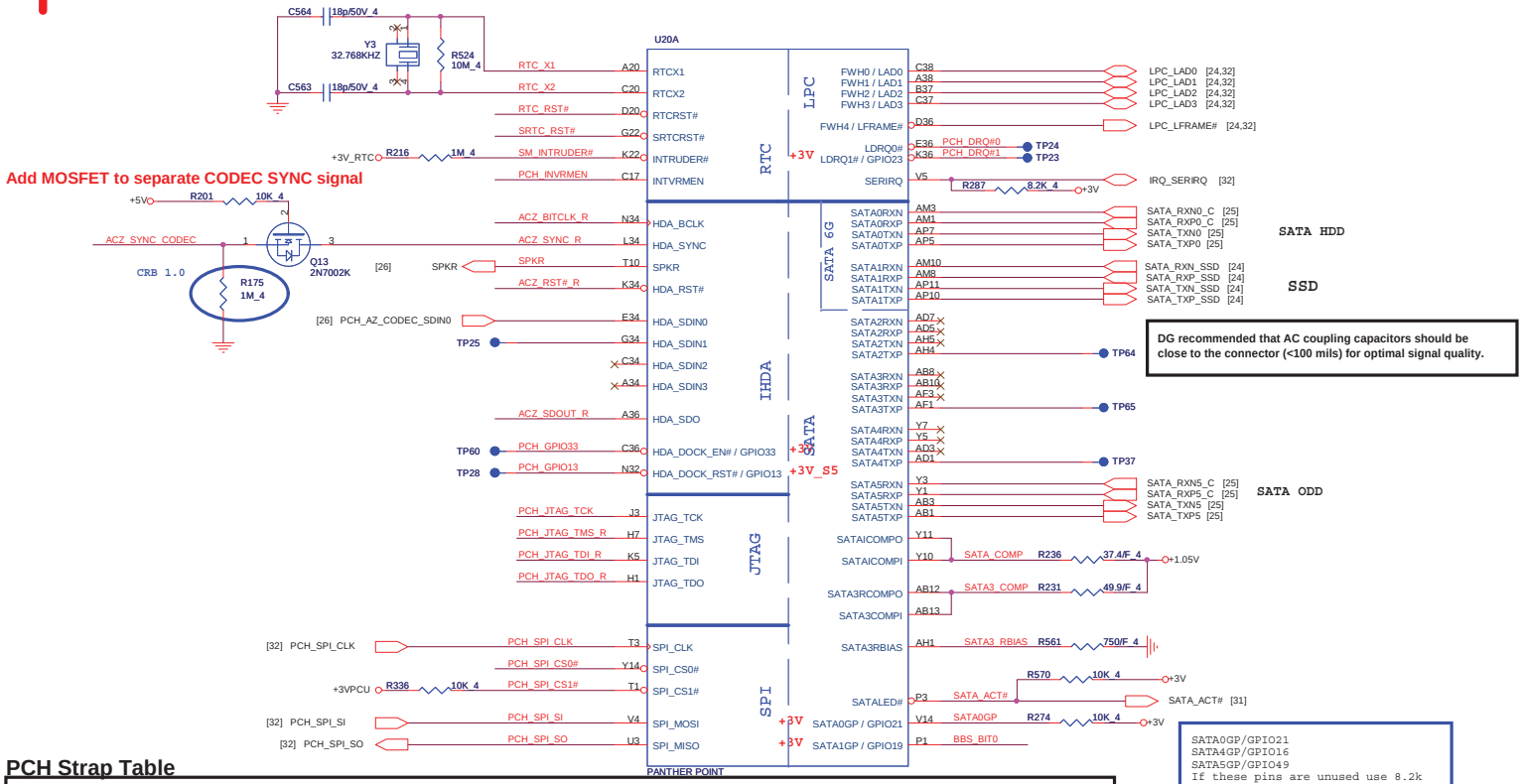


PCH Dual SPI (CLG) (Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01------>2MB
for BA W25Q64BVSSIG / AKE3EFP0N00------>8MB



PCH2 (CLG) CPT/PPT (HDA,JTAG,SATA)

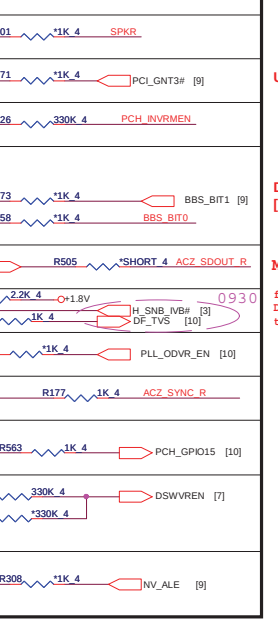


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

SATA0GP/GPIO21
SATA4GP/GPIO16
SATA5GP/GPIO49
If these pins are unused use 8.2k to 10k pull-up to +Vcc3_3 or 8.2k to 10k pull-down to ground

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

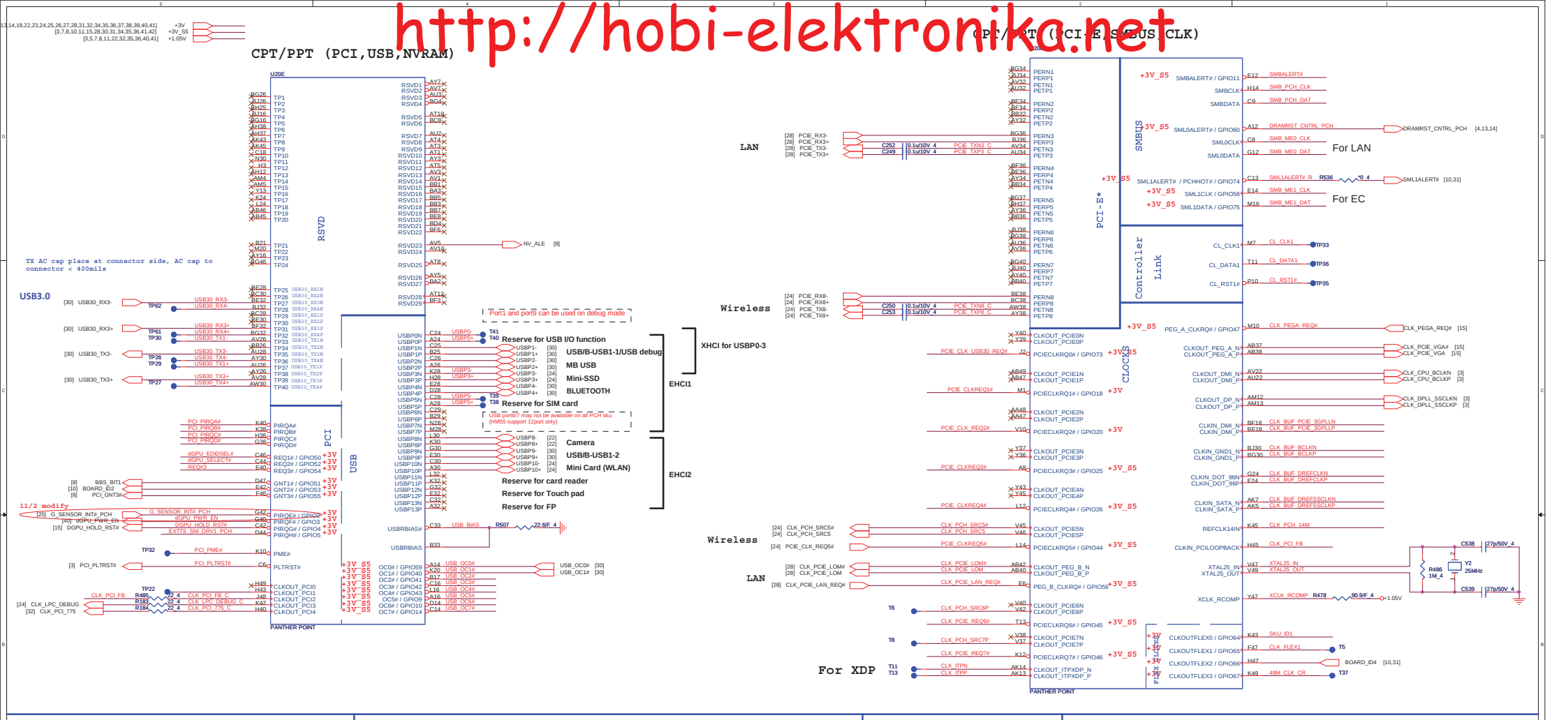
ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

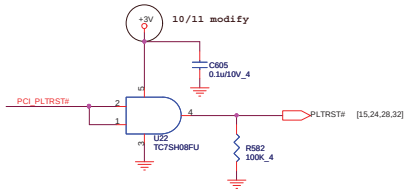
Needs to be pulled High for Huron River platform. chklist 1.2

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

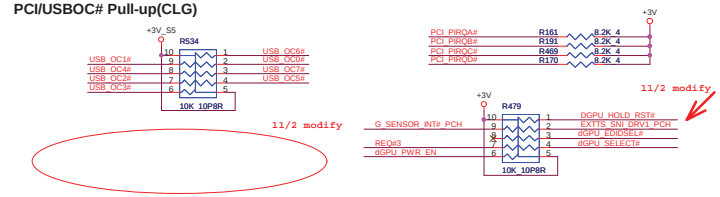
Size	Document Number	Rev
	Panther Point 2/6	1A
Date: Friday, November 11, 2011	Sheet 8 of 44	

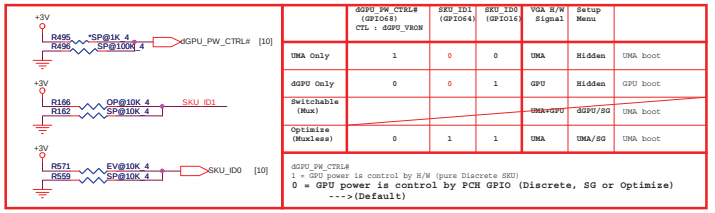


PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)

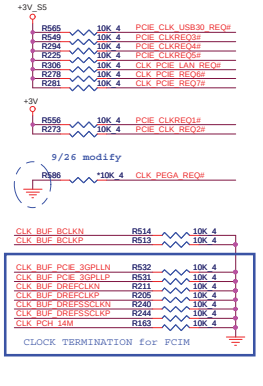




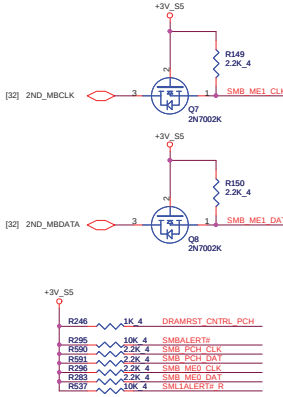
	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO54)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0	0	1	GPU	Hidden	GPU boot
Switchable (Mux)				UMA+dGPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
--->(Default)

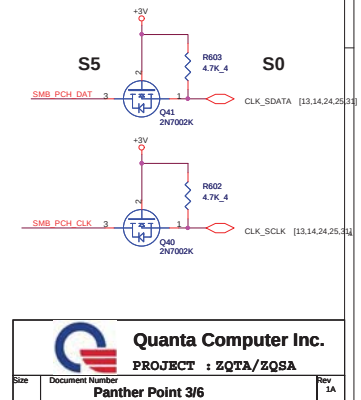
CLK_REQ/Strap Pin(CLG)



SMBus(EC)



SMBus(PCH)



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	Panther Point 3/6	1A

Date: Friday, November 11, 2011 Sheet 9 of 44

CPT/PPT (GPIO,VSS_NCTF,RSVD)

[9,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[3,7,8,9,11,15,28,30,31,34,35,36,41,42] +3V_S5

U20F

S_GPIO R276 100_4 T7 BMBUSY# / GPIO0 +3V
[32] SIO_EXT_SMI# A42 TACH1 / GPIO1 +3V
BOARD_ID1 H36 TACH2 / GPIO6 +3V
[32] SIO_EXT_SCI# E38 TACH3 / GPIO7 +3V
TP63 C10 GPIO8 +3V_S5
TP66 GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
[8] PCH_GPIO15 G2 GPIO15 +3V_S5
[9] SKU_ID0 U2 SATA4GP / GPIO16 +3V
[15,19] DGPU_PWROK D40 TACH0 / GPIO17 +3V
G_SENSOR_ID T5 SCLOCK / GPIO22 +3V
11/2 modify
PCH_GPIO24 E8 GPIO24 / MEM_LED +3V_S5
PCH_GPIO27 E16 GPIO27 DSW
[8] PLL_ODVR_EN P8 GPIO28 +3V_S5
STP_PCI# K1 STP_PCI# / GPIO34 +3V
[39,40] dGPU_VRON K4 GPIO35 +3V
DMI_OVRVLTG V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG M5 SATA3GP / GPIO37 +3V
MFG_MODE N2 SLOAD / GPIO38 +3V
BOARD_ID0 M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP V13 SDATAOUT1 / GPIO48 +3V
[9,31] SML1ALERT# R572 *SHORT_4 CRIT_TEMP_REP# V3 SATA5GP / GPIO49 +3V
TP34 SV_DET_NC D6 GPIO57 +3V_S5
R266 100K_4
10/11 modify

GPIO

TACH4 / GPIO68 +3V C40 dGPU_PW_CTRL# [9]
TACH5 / GPIO69 +3V B41 CABLE_ID [22]
TACH6 / GPIO70 +3V C41 BOARD_ID3
TACH7 / GPIO71 +3V A40 R491 10K_4 +3V

CPU/MISC

A20GATE P4 SIO_A20GATE SIO_A20GATE [32]
PECI AU16 PCH_PECI TP31
RCIN# P5 SIO_RCIN# SIO_RCIN# [32]
PROCPWRGD AY11 H_PWRGOOD [3]
THRMTRIP# AY10 PCH_THRMTRIP# R249 390_4 PM_THRMTRIP# [3]
INIT3_3V# T14
DF_TVS AY1 DF_TVS DF_TVS [8]
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

PANTHER POINT

SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

GPIO Pull-up/Pull-down(CLG)

+3V_S5
PCH_GPIO24 R307 *10K_4
PLL_ODVR_EN R303 10K_4
10/31 modify
+3V
SIO_EXT_SMI# R148 10K_4
SIO_EXT_SCI# R145 10K_4
STP_PCI# R566 *10K_4
SIO_A20GATE R290 10K_4
SIO_RCIN# R304 10K_4
CRIT_TEMP_REP# R560 10K_4
+1.8V
DF_TVS R550 *1K_4
Follow the Emerald Lake 2 CRB
PCH_GPIO27 R223 10K_4

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

SV_SET_UP
High = Strong (Default)
+3V
TEST_SET_UP R272 10K_4
R285 *1K_4

Reserve for future

+3V
R555 10K_4 BOARD_ID0 R568 *10K_4
R471 10K_4 BOARD_ID1 R467 *10K_4
R490 *10K_4 BOARD_ID3 R487 10K_4
R472 *10K_4 BOARD_ID4 R468 10K_4
BOARD_ID3 [31]
BOARD_ID4 [9,31]

SGPIO

+3V
S_GPIO R302 1K_4
R289 *1K_4

BOARD_ID2

8 Layer ------->High *
6 Layer ------->Low

+3V
R167 *10K_4
R172 10K_4
BOARD_ID2 [9]

+3V
R305 100K_4 FDI_OVRVLTG R291 *1K_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
DMI_OVRVLTG R286 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
G_SENSOR_ID R288 SP@10K_4
R275 SP@1K_4

BIOS RECOVERY	High = W/O G_SENSOR Low = W G_SENSOR

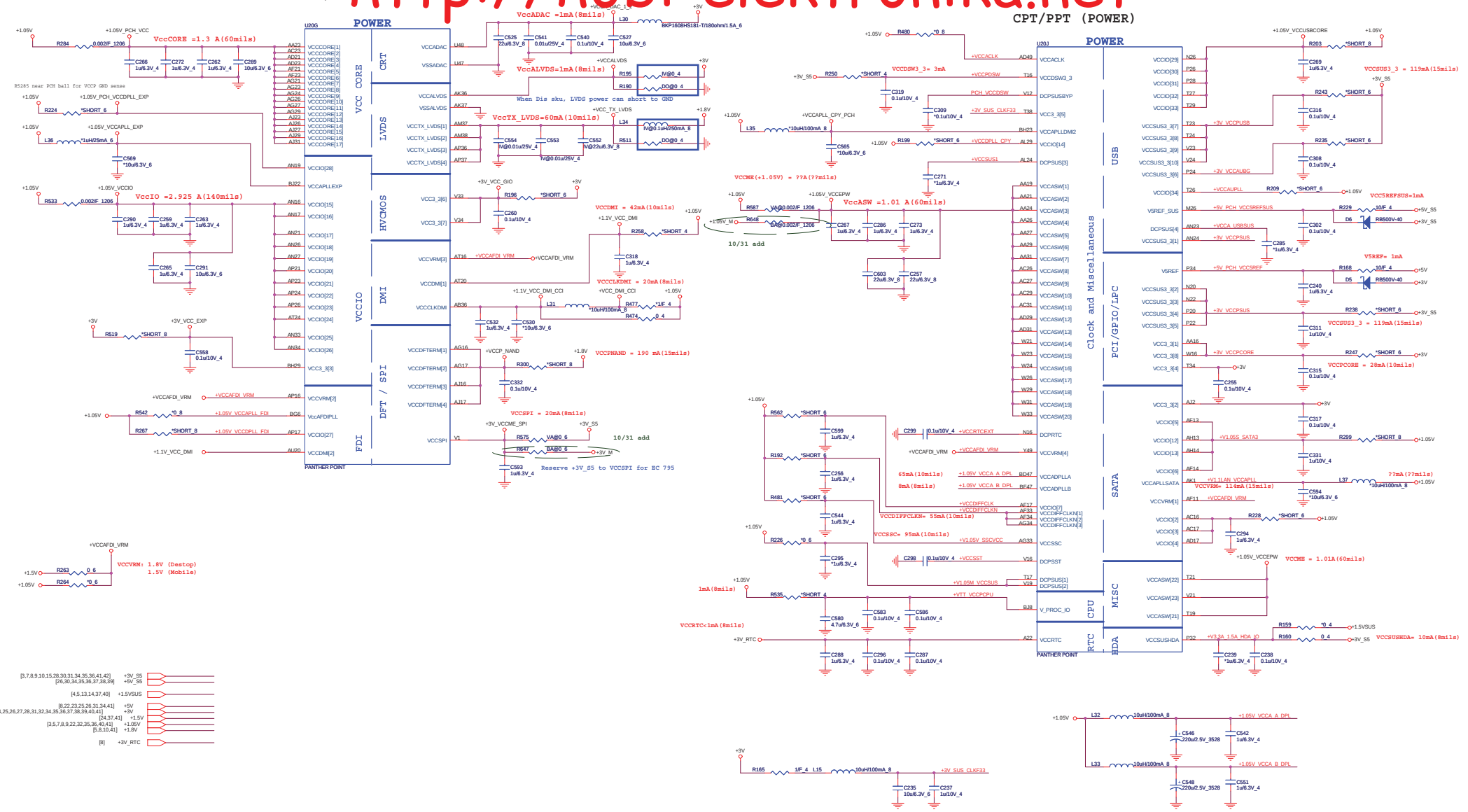
MFG-TEST

+3V
MFG_MODE R569 10K_4
R557 *1K_4

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	Panther Point 4/6	1A
Date: Friday, November 11, 2011	Sheet 10 of 44	

CPT/PPT (POWER)

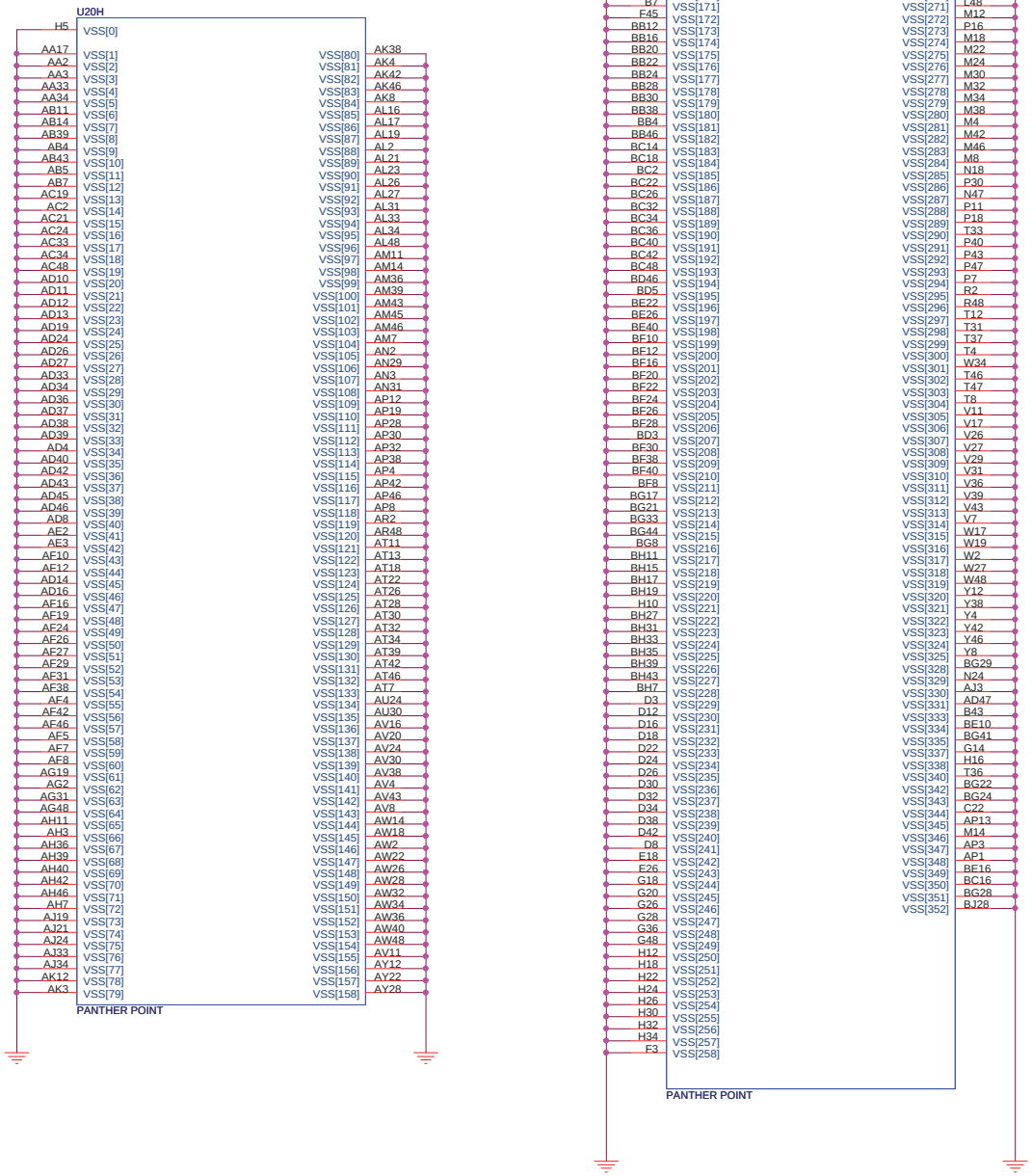


Quanta Computer Inc.

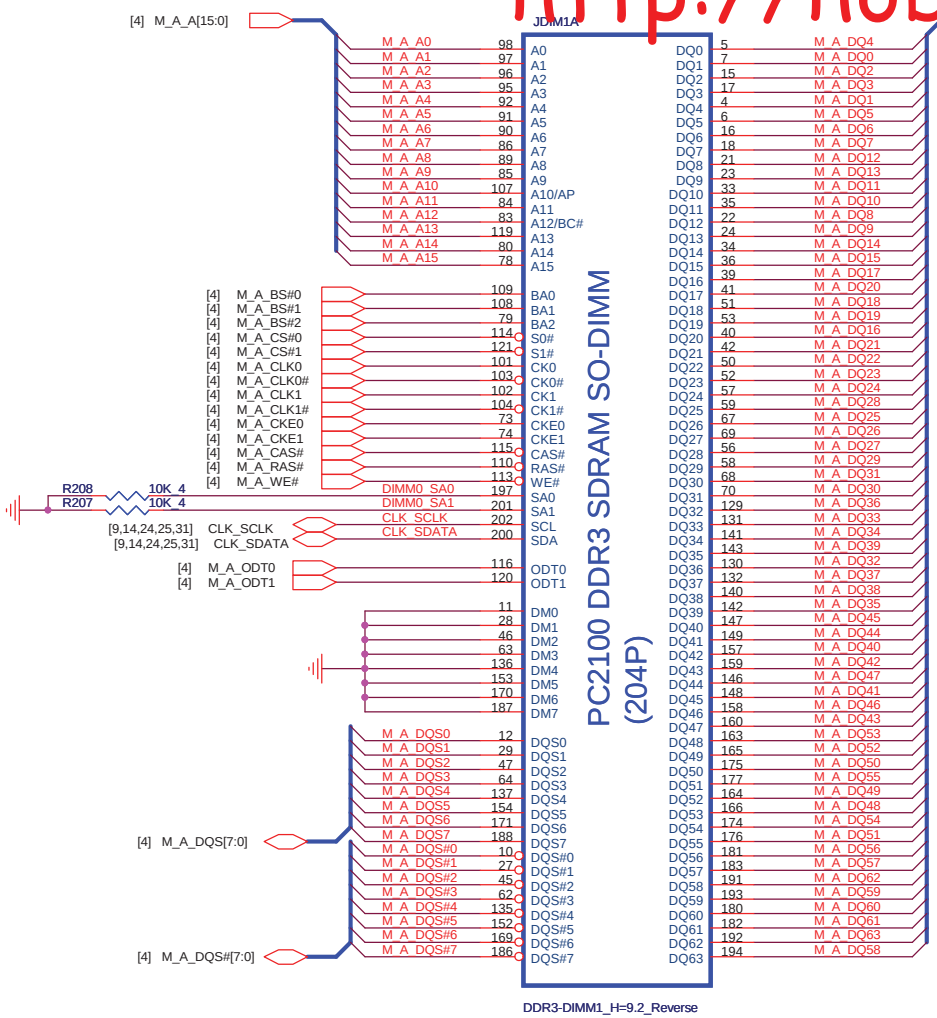
PROJECT : ZQTA/ZQSA

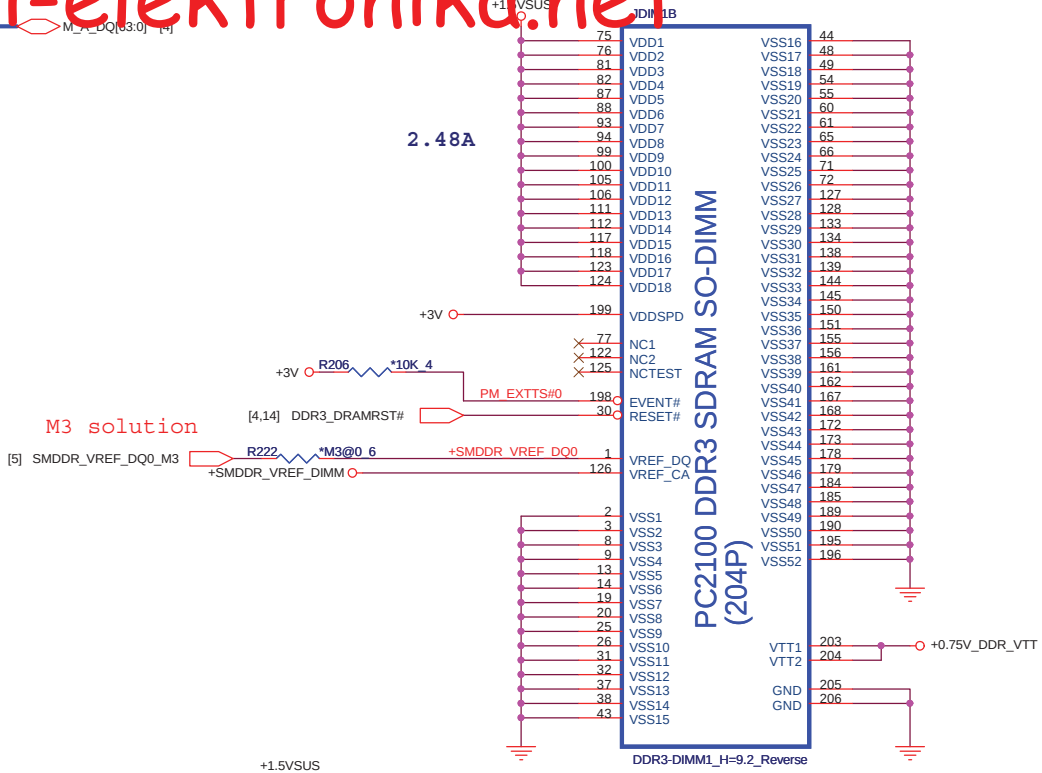
Size	Document Number	Rev
	Panther Point 5/6	1A
Date: Friday, November 11, 2011	Sheet 11 of 44	

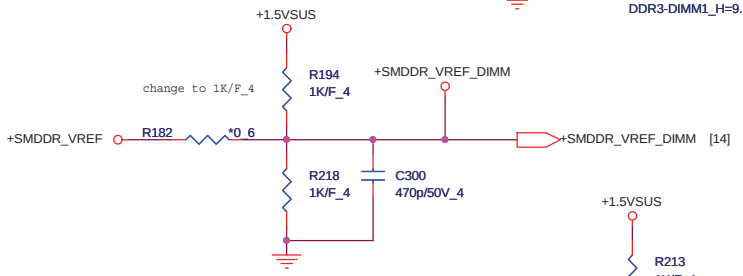
IBEX PEAK-M (GND)

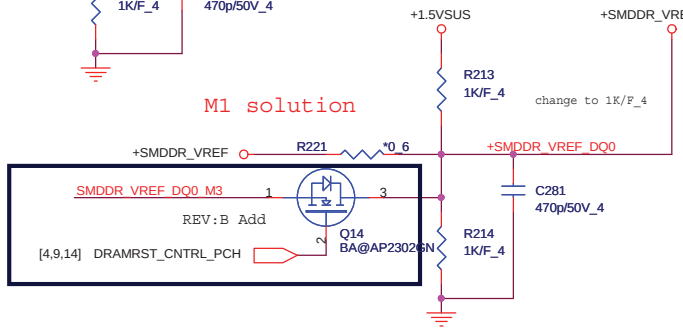


Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: Panther Point 6/6	Rev: 1A
Date: Friday, November 11, 2011	Sheet 12 of 44	

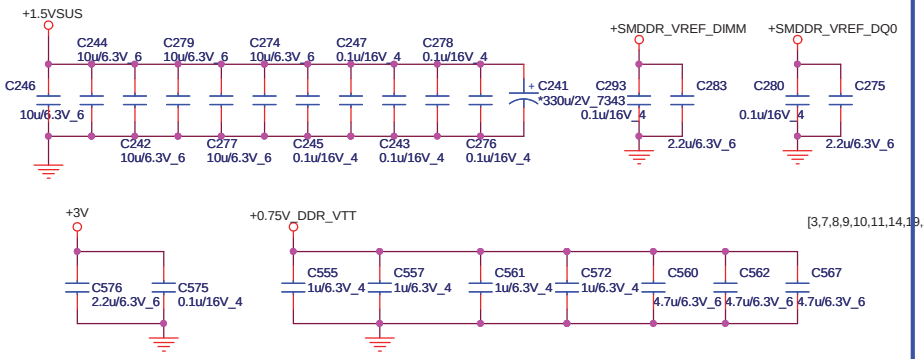






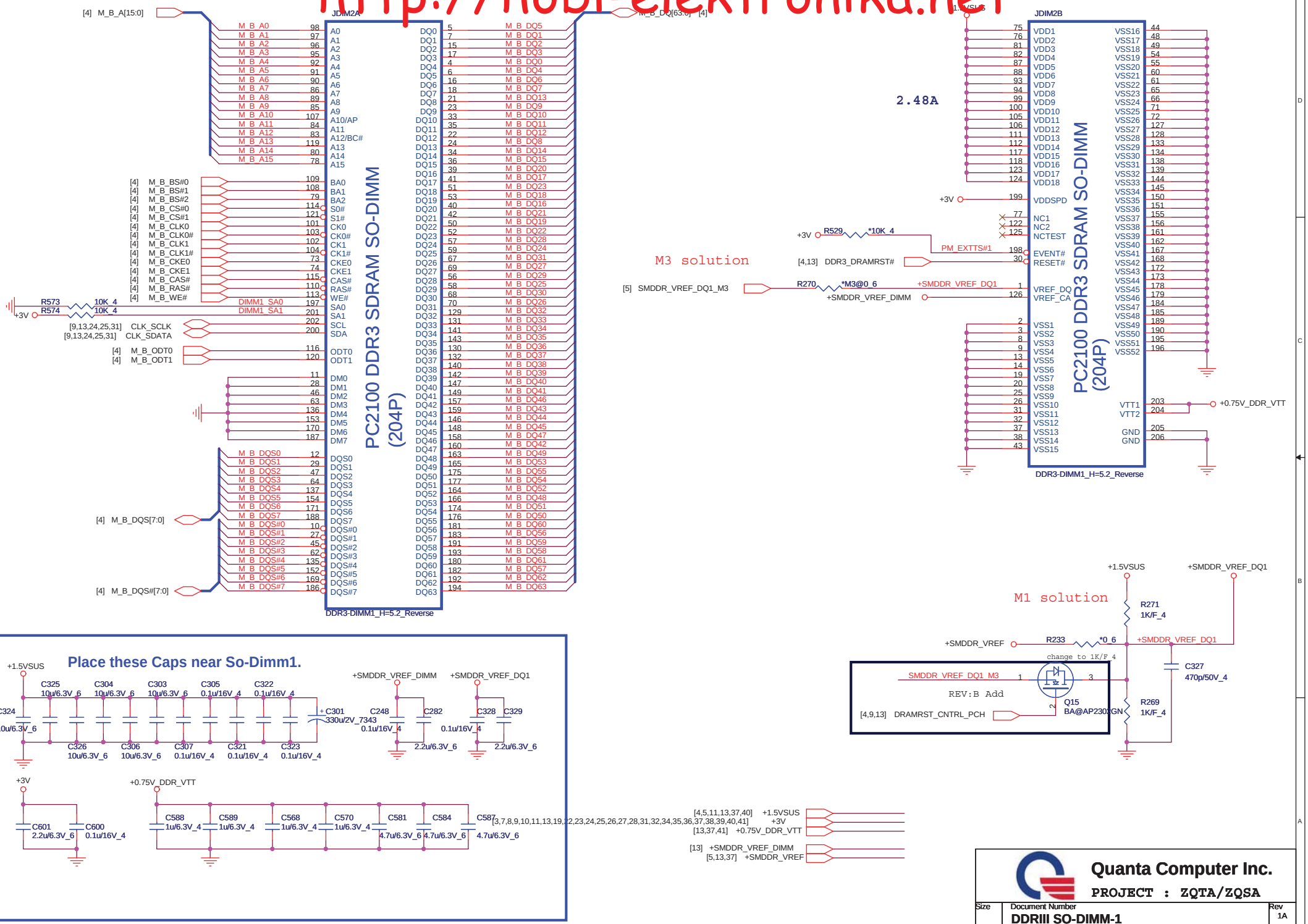


Place these Caps near So-Dimm0.



[4,5,11,14,37,40] +1.5VSUS
[3,7,8,9,10,11,14,19,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[14,37,41] +0.75V_DDR_VTT
[5,14,37] +SMDDR_VREF

Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Friday, November 11, 2011	Sheet 13 of 44	



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1A
Date: Friday, November 11, 2011	Sheet 14 of 44	

N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

1000mA
2500mA
[PEG Interface]
U15A
EV@N13x
N13P

for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R
Reserve -->L	Stuff--> L

10/31 modify
10/11 chnage type
10/5 modify
10/11 change to 1k
12~16 mils width

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

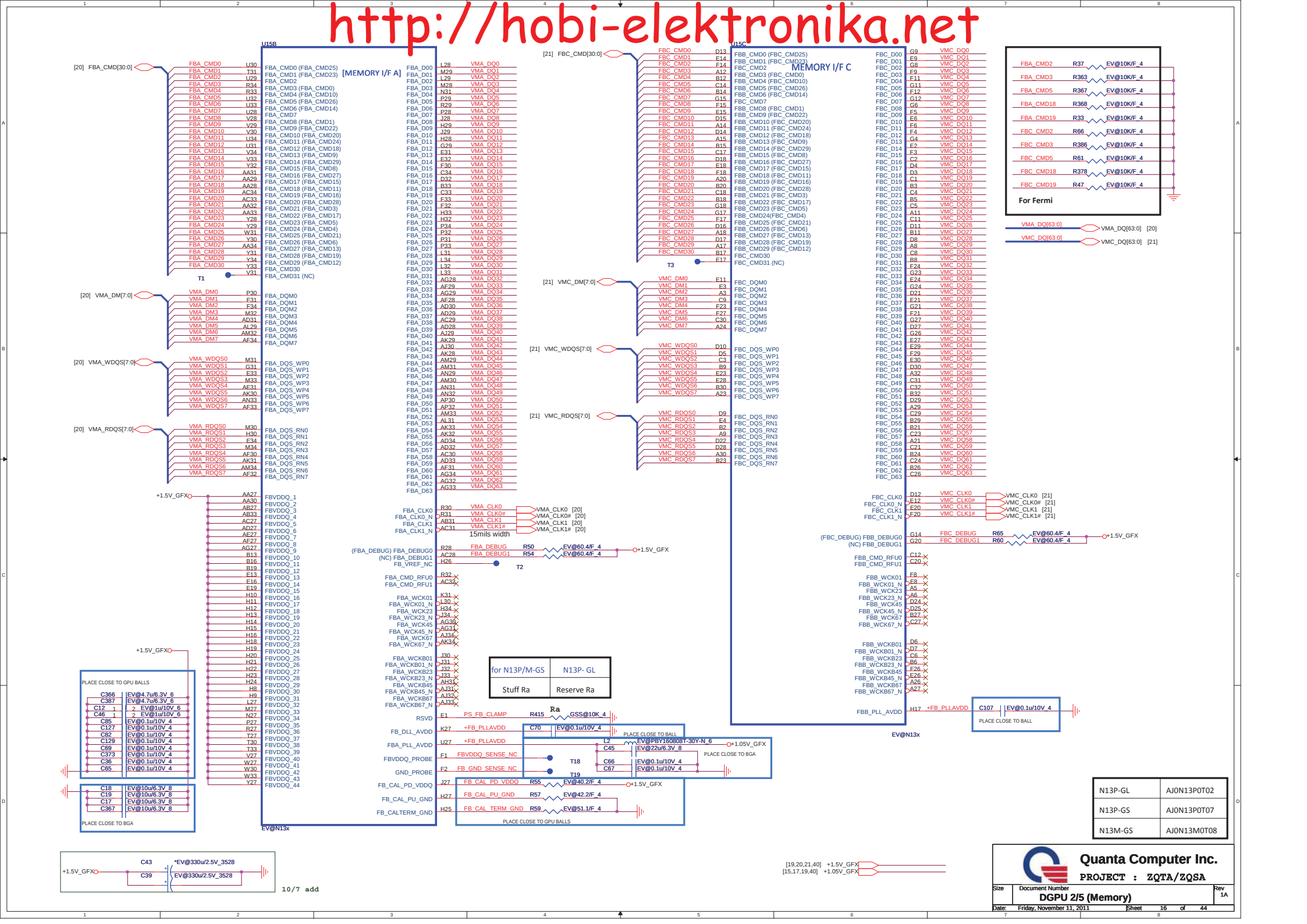
Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

PEX_RST timing

I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A
Date: Friday, November 11, 2011	Sheet 15 of 44	



N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A
Date: Friday, November 11, 2011	Sheet 16 of 44	

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

10/6 modify

50 mA
320 mA
220 mA
285 mA
120 mA
10/7 add
(1.05V +/- 3%)

U15D

[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]

EV@N13x

PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 3/5 (Display)	1A

Date: Friday, November 11, 2011 Sheet 17 of 44

[15,17,19,39,40] +3V_GFX

STRAP2
N13P-GL (1001) ---> 10k PU
N13P-GS (1011) ---> 20K PU

STRAP1
N13P-GL (0111) ---> 45.3k PD
N13P-GS (0110) ---> 34.8K PD

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

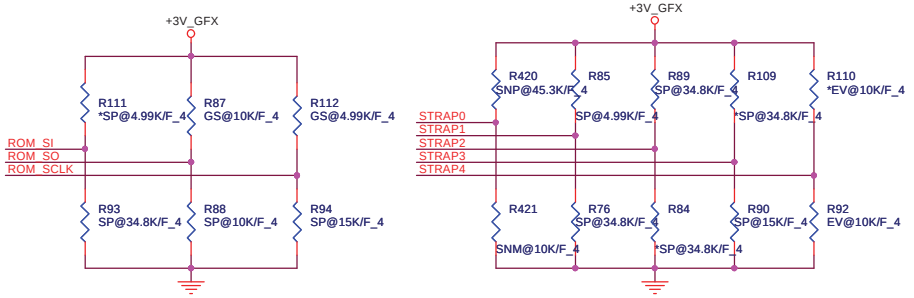
Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
34.8K---> CS33482FB22
45.3K ---> CS34532FB18

Logical Strap Bit Mapping

PU/VDD	PD	
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00



N13P-GS/-GL Straping table

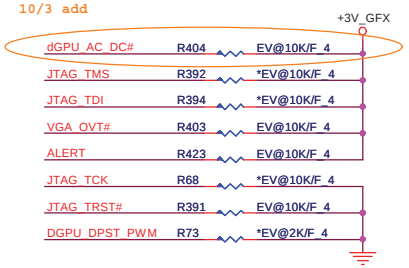
ROM_SI	ROM_SO	ROM_SCLK
1G Hynix 64Mx16 -->15K PD	N13P-GL --> 10K PD	N13P-GL (0010) ---> 15k PD
1G Micron 64Mx16 -->20K PD	N13P-GS --> 10K PU	N13P-GS (1000) ---> 4.99K PU
2G Hynix 128Mx16 -->35K PD (Default)		
2G Micron 128Mx16 -->45K PD		

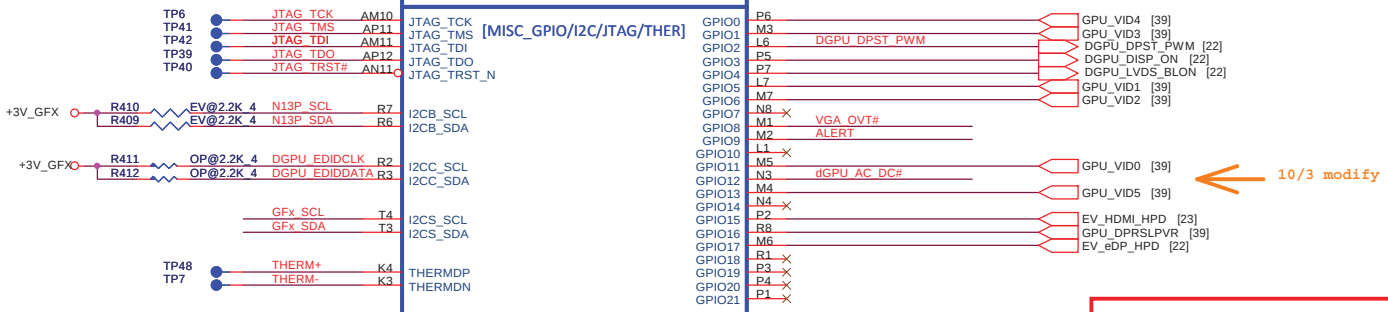
U15E

[MIOA]

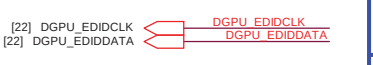
[MIOB]

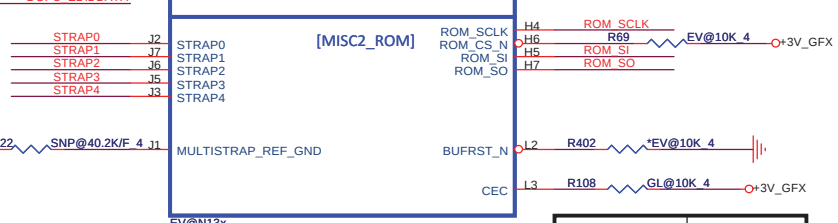
10/3 add





10/3 modify

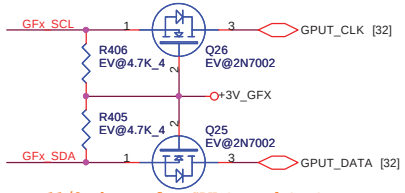




R422	
N13P-GS/GL	40.2K
N13M-GS	NC

for N13P/M-GS	for N13P- GL
Reserve R108	Stuff R108

GFx SMBus Isolation * *

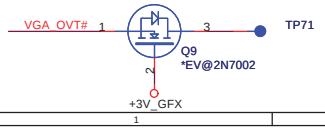


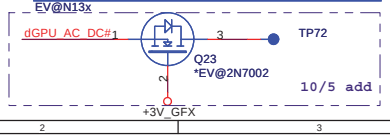
11/8 change for GPU temp detect

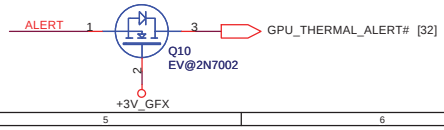
N13M-GS Straping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

Remark :
0 -> 10K PD
1 -> 10K PU



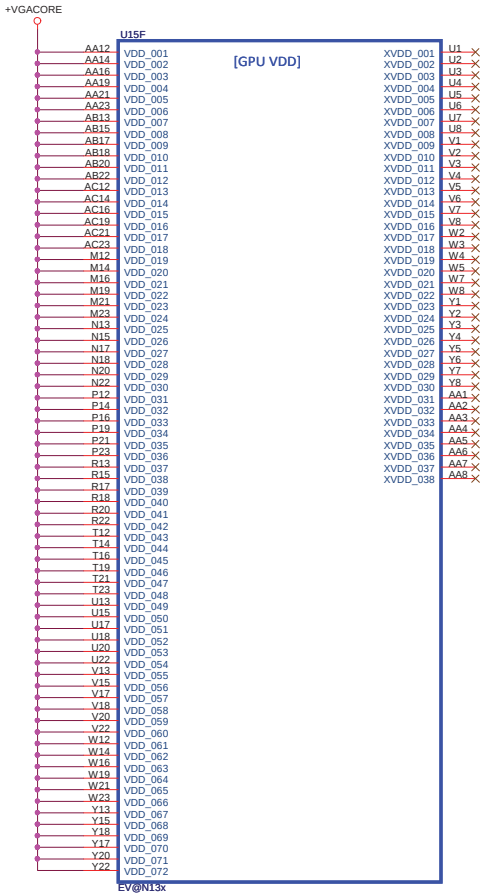


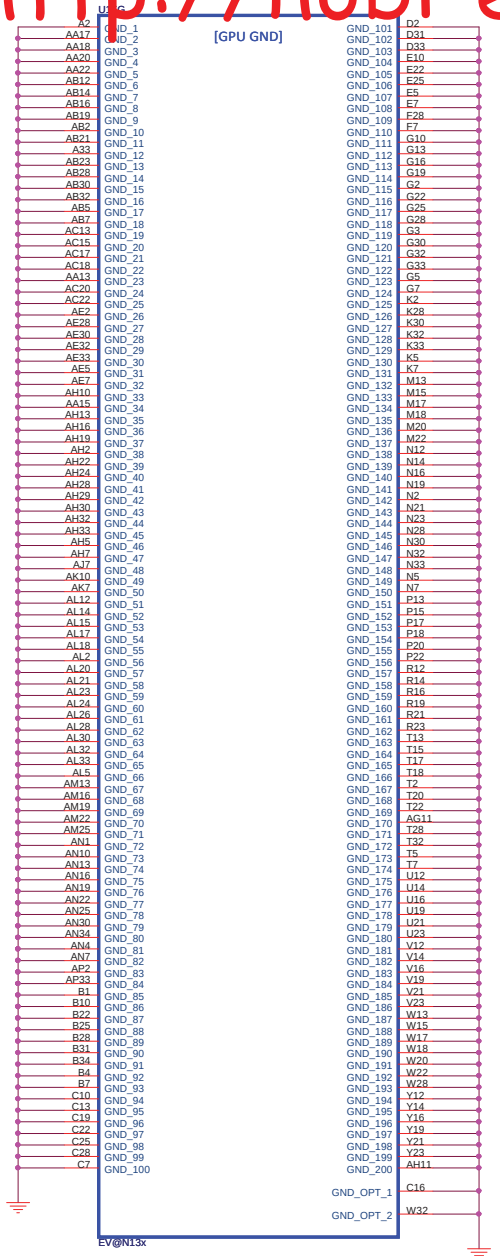


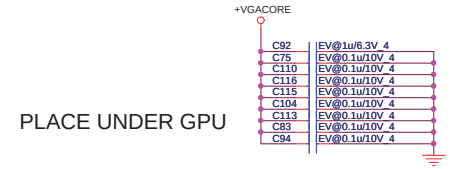
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

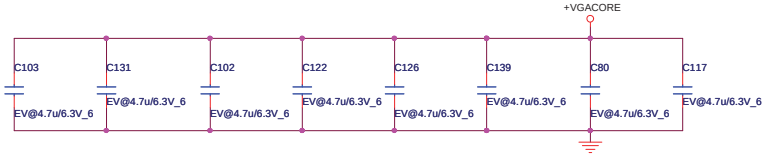
Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A
Date: Friday, November 11, 2011	Sheet 18 of 44	

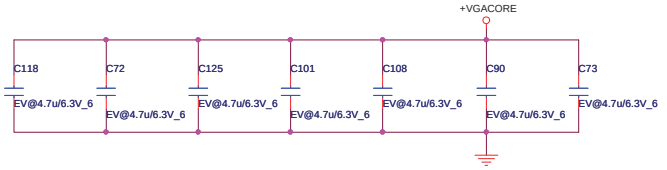
N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

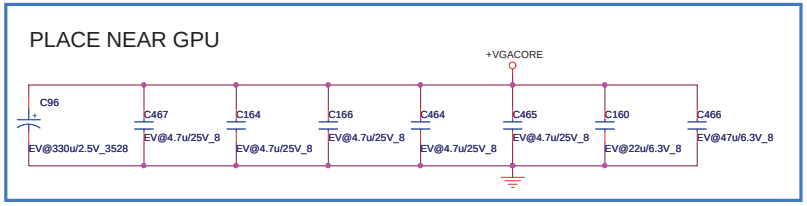


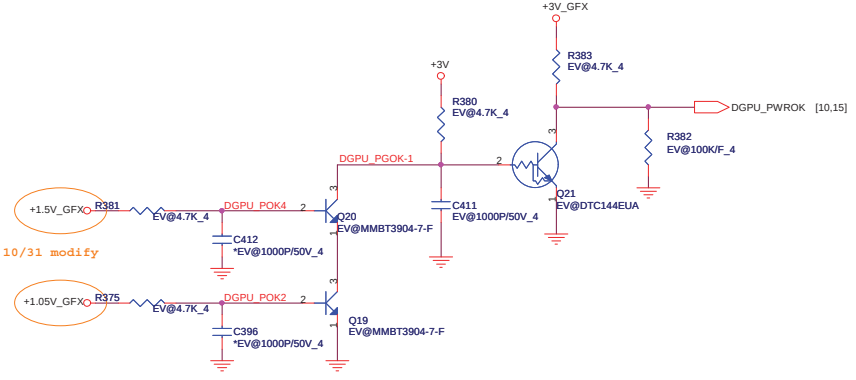


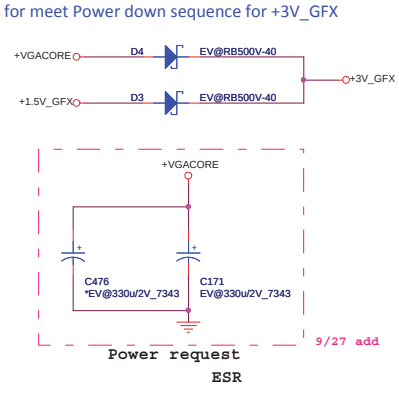












[31,39] +VGACORE
[15,16,17,40] +1.05V_GFX
[16,20,21,40] +1.5V_GFX
[15,17,18,39,40] +3V_GFX
[3,7,8,9,10,11,13,14,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A
Date: Friday, November 11, 2011	Sheet 19 of 44	

HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

VRAM2 / VRAM5 / VRAM1 / VRAM6

96-BALL SDRAM DDR3
EV@VRAM_DDR3

10/12 SWAP Pin

Should be 240 Ohms +-1%

R43 EV@243/F_4
R364 EV@243/F_4
R34 EV@243/F_4
R373 EV@243/F_4

+1.5V_GFX

[16] FBA_CMD17 — FBA_CMD17 — TP1
[16] FBA_CMD1 — FBA_CMD1 — TP2
10/14 modify

VMA_CLK0 — R371 EV@162/F_4 — VMA_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1 — R41 EV@162/F_4 — VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R366 EV@1.33K/F_4 — VREFC_VMA1 — R365 EV@1.33K/F_4 — C376 EV@0.1u/10V_4
R39 EV@1.33K/F_4 — VREFD_VMA1 — R38 EV@1.33K/F_4 — C34 EV@0.1u/10V_4
R36 EV@1.33K/F_4 — VREFC_VMA3 — R35 EV@1.33K/F_4 — C24 EV@0.1u/10V_4
R370 EV@1.33K/F_4 — VREFD_VMA3 — R369 EV@1.33K/F_4 — C380 EV@0.1u/10V_4

+1.5V_GFX

C30 EV@1u/10V_4
C27 EV@1u/10V_4
C374 EV@1u/10V_4
C25 EV@1u/10V_4

C369 EV@10u/6.3V_8
C379 EV@1u/10V_4
C382 EV@1u/10V_4
C23 EV@1u/10V_4
C29 EV@1u/10V_4
C32 EV@1u/10V_4

C416 EV@10u/6.3V_8
C26 EV@1u/10V_4
C375 EV@1u/10V_4
C28 EV@1u/10V_4
C37 EV@1u/10V_4
C33 EV@1u/10V_4
C31 EV@1u/10V_4
C371 EV@1u/10V_4

C386 EV@10u/6.3V_8
C368 EV@10u/6.3V_8
C381 EV@0.1u/10V_4
C35 EV@0.1u/10V_4
C377 EV@0.1u/10V_4
C378 EV@0.1u/10V_4
C370 EV@0.1u/10V_4

C44 EV@10u/6.3V_8
C88 EV@10u/6.3V_8
C372 EV@0.1u/10V_4
C385 EV@0.1u/10V_4
C383 EV@0.1u/10V_4

[16,19,21,40] +1.5V_GFX

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU Memory 1/2 (DDR3)	1A
Date: Friday, November 11, 2011	Sheet 20 of 44	

HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

CHANNEL B: 256MB/512MB DDR3

[3] VMC_DQ[3..0]
[16] VMC_DM[7..0]
[16] VMC_WDQS[7..0]
[16] VMC_RDQS[7..0]

VRAM8 / VRAM4 / VRAM3 / VRAM7 — 96-BALL SDRAM DDR3 — SNP@VRAM _DDR3

10/12 SWAP Pin

Should be 240 Ohms +-1%

R385 SNP@243/F_4 — VMC_ZQ1
R64 SNP@243/F_4 — VMC_ZQ2
R52 SNP@243/F_4 — VMC_ZQ3
R379 SNP@243/F_4 — VMC_ZQ4

+1.5V_GFX

R388 SNP@162/F_4 — VMC_CLK0 / VMC_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R62 SNP@1.33K/F_4 — VREFC_VMC1
R63 SNP@1.33K/F_4
C121 SNP@0.1u/10V_4
R74 SNP@1.33K/F_4 — VREFD_VMC1
R70 SNP@1.33K/F_4
C148 SNP@0.1u/10V_4

R49 SNP@162/F_4 — VMC_CLK1 / VMC_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R56 SNP@1.33K/F_4 — VREFC_VMC3
R58 SNP@1.33K/F_4
C79 SNP@0.1u/10V_4
R376 SNP@1.33K/F_4 — VREFD_VMC3
R377 SNP@1.33K/F_4
C403 SNP@0.1u/10V_4

C137 C384 C68 C423 SNP@1u/10V_4
C152 C448 C446 C394 C58 C429 SNP@10u/6.3V_8 / SNP@1u/10V_4
C21 C445 C132 C393 C397 C399 C442 C50 SNP@0.1u/10V_4
C53 C410 C51 C22 C97 C426 C391 C389 SNP@1u/10V_4

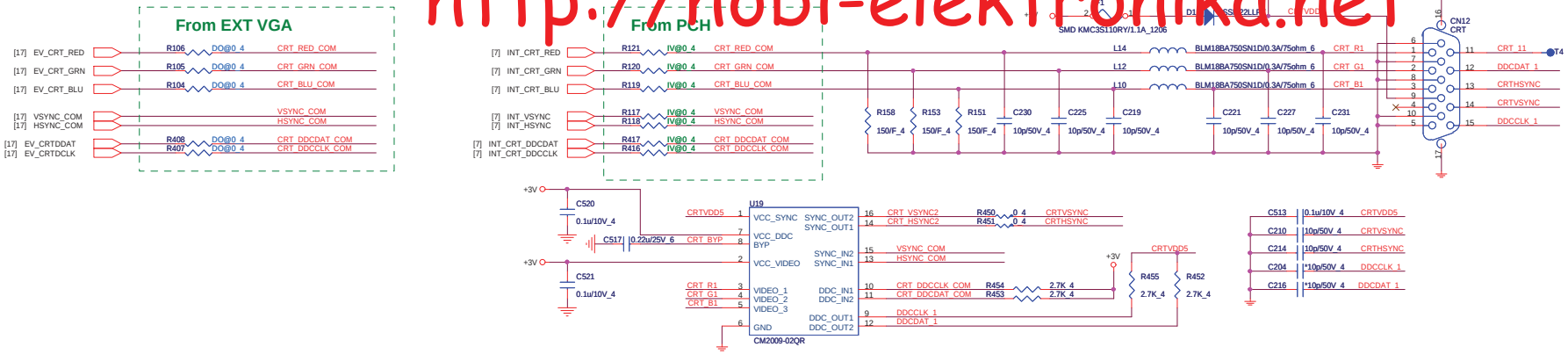
[16] FBC_CMD17 — FBC_CMD17 — TP3
[16] FBC_CMD1 — FBC_CMD1 — TP4

[16,19,20,40] +1.5V_GFX

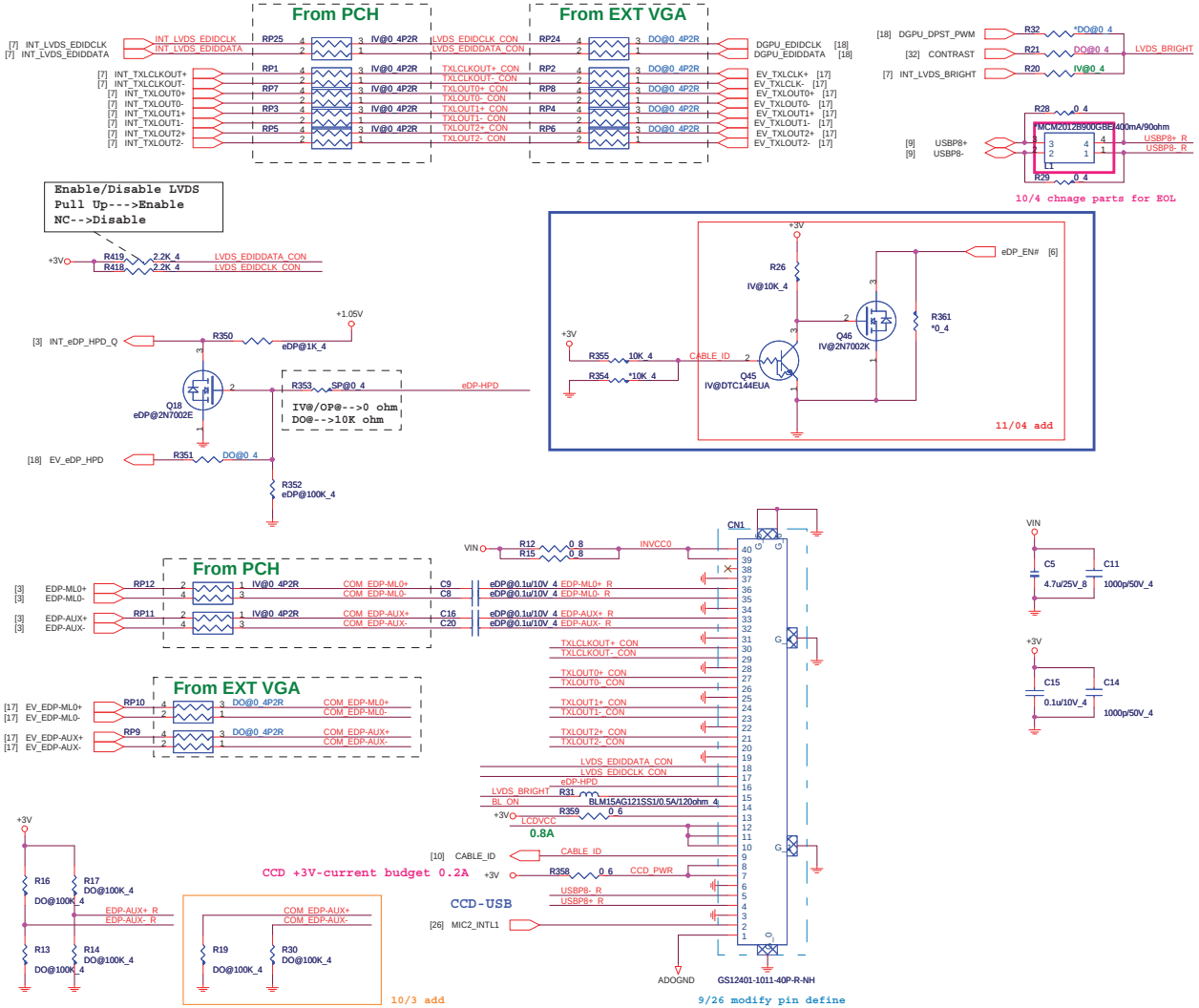
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, November 11, 2011	Sheet 21 of 44	

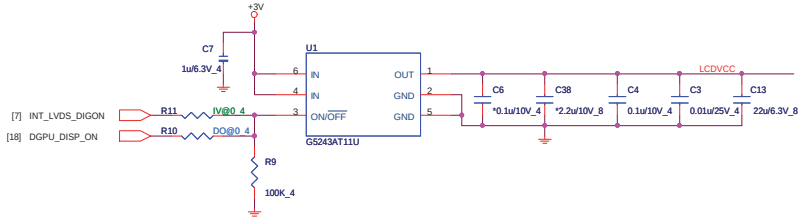
CRT



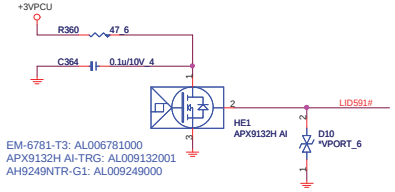
LVDS & eDP



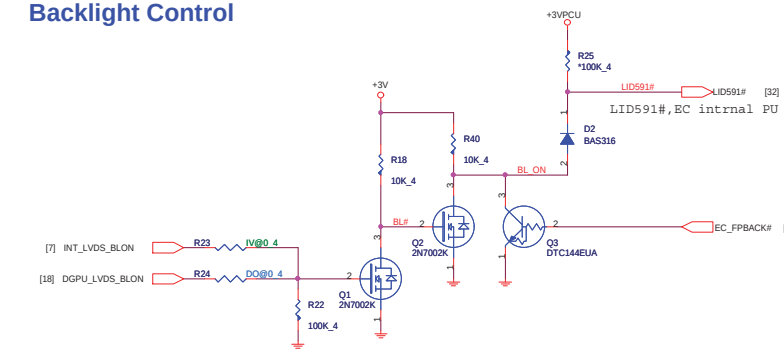
LCD Power



Lid Switch (Hall sensor)



Backlight Control



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size | Document Number | Rev 1A
CRT/LVDS/CAMERA/LID
Date: Friday, November 11, 2011 | Sheet 22 of 44

HDMI

From PCH

[7] INT_HDMITX2N
[7] INT_HDMITX2P
C270 0.1u/10V_4
C284 0.1u/10V_4
INT_HDMITX2N_C
INT_HDMITX2P_C

[7] INT_HDMITX1N
[7] INT_HDMITX1P
C258 0.1u/10V_4
C261 0.1u/10V_4
INT_HDMITX1N_C
INT_HDMITX1P_C

[7] INT_HDMITX0N
[7] INT_HDMITX0P
C264 0.1u/10V_4
C268 0.1u/10V_4
INT_HDMITX0N_C
INT_HDMITX0P_C

[7] INT_HDMICLK+
[7] INT_HDMICLK-
C254 0.1u/10V_4
C251 0.1u/10V_4
INT_HDMICLK+_C
INT_HDMICLK-_C

DO@--->499 ohm
P/N:CS14992FB24
IV@/OP@--->680 ohm
P/N:CS16802JB27

R512 SP@680_4
R515 SP@680_4
R522 SP@680_4
R520 SP@680_4
R518 SP@680_4
R516 SP@680_4
R525 SP@680_4
R523 SP@680_4

+5V
R517 *100K/F_4
Q38 2N7002E

From EXT VGA

[17] EV_HDMITX2N
[17] EV_HDMITX2P
RP14 DO@0_4P2R
INT_HDMITX2N
INT_HDMITX2P

[17] EV_HDMITX1N
[17] EV_HDMITX1P
RP15 DO@0_4P2R
INT_HDMITX1N
INT_HDMITX1P

[17] EV_HDMITX0N
[17] EV_HDMITX0P
RP16 DO@0_4P2R
INT_HDMITX0N
INT_HDMITX0P

[17] EV_HDMICLK-
[17] EV_HDMICLK+
RP17 DO@0_4P2R
INT_HDMICLK-
INT_HDMICLK+

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

HDMI connector

CN13 HDMI CONN
SHELL1 20
SHELL2 21
1 D2+
2 D2 Shield
3 D2-
4 D1+
5 D1 Shield
6 D1-
7 D0+
8 D0 Shield
9 D0-
10 CK+
11 CK Shield
12 CK-
13 CE Remote
14 NC
15 DDC CLK
16 DDC DATA
17 GND
18 +5V
19 HP DET

INT_HDMITX2P_C
INT_HDMITX2N_C
INT_HDMITX1P_C
INT_HDMITX1N_C
INT_HDMITX0P_C
INT_HDMITX0N_C
INT_HDMICLK+_C
INT_HDMICLK-_C
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HP
0_4_HP_DET_CN

+5V
SMD KMC3S110RY/1.1A_1206 F2
D19 SSM22LLPT
C545 470p/50V_4
R178 0_4
R179 100K_4

9/22 change parts

HDMI-detect

+3V
R174 10K_4
R181 10K_4
R185 IV@0_4 HDMI_HP [7]
R189 DO@0_4 EV_HDMI_HPD [18]
[32] HDMI_HPD_EC#
+5V
R180 *10K_4
HDMI_MB_HP
Q12 2N7002E
Q11 2N7002E

I2C

UMA	R239 R245	CS22202JB18
DIS	R239 R245	CS24702JB38

From EXT VGA

[17] EV_HDMI_DDCCK_C
[17] EV_HDMI_DDCDAT_C
R493 DO@0_4 HDMI_DDCCLK_COM
R508 DO@0_4 HDMI_DDCDATA_COM

From PCH

[7] HDMI_DDCCLK_SW
[7] HDMI_DDCDATA_SW
R501 IV@0_4 HDMI_DDCCLK_COM
R504 IV@0_4 HDMI_DDCDATA_COM

+5V
+3V
R489 SP@2.2K_4
Q35 BSN20
D20 RB501V-40
R494 2.2K_4
HDMI_DDCCLK_MB
R510 SP@2.2K_4
Q37 BSN20
D21 RB501V-40
R509 2.2K_4
HDMI_DDCDATA_MB

EMI

INT_HDMITX2P_C
R212 *100/F_4
INT_HDMITX2N_C
INT_HDMITX1P_C
R200 *100/F_4
INT_HDMITX1N_C
INT_HDMITX0P_C
R204 *100/F_4
INT_HDMITX0N_C
INT_HDMICLK+_C
R193 *100/F_4
INT_HDMICLK-_C

[3,7,8,9,10,11,13,14,19,22,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[8,11,22,25,26,31,34,41] +5V

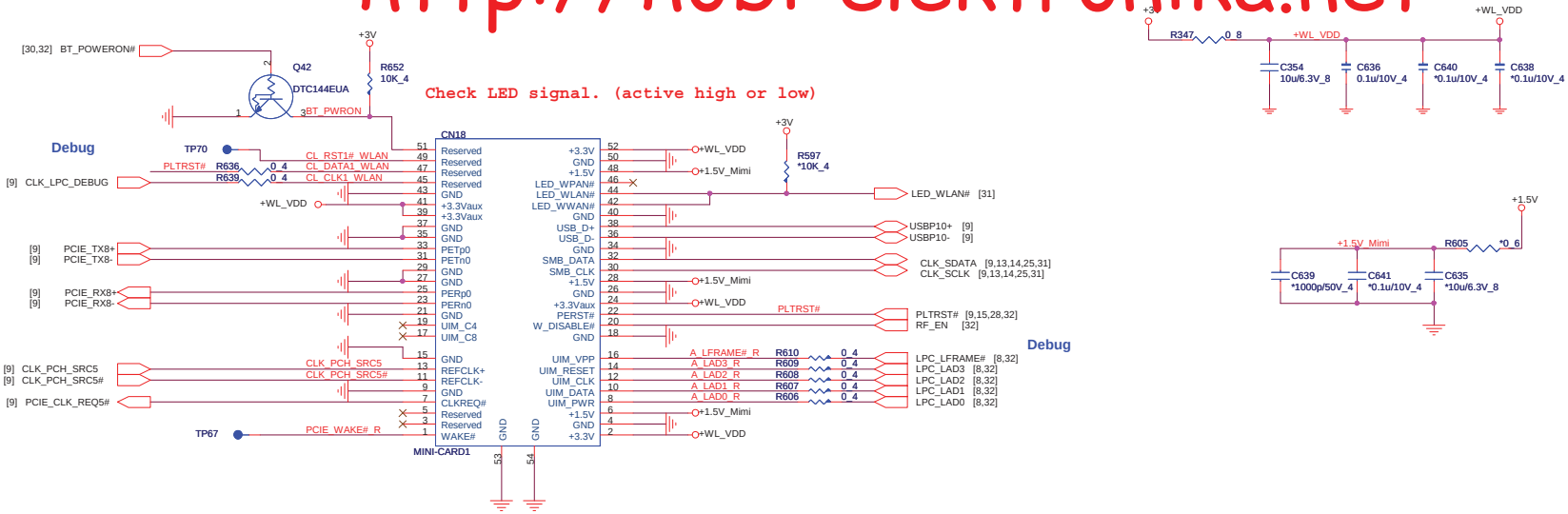
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	HDMI (PS8101)	1A

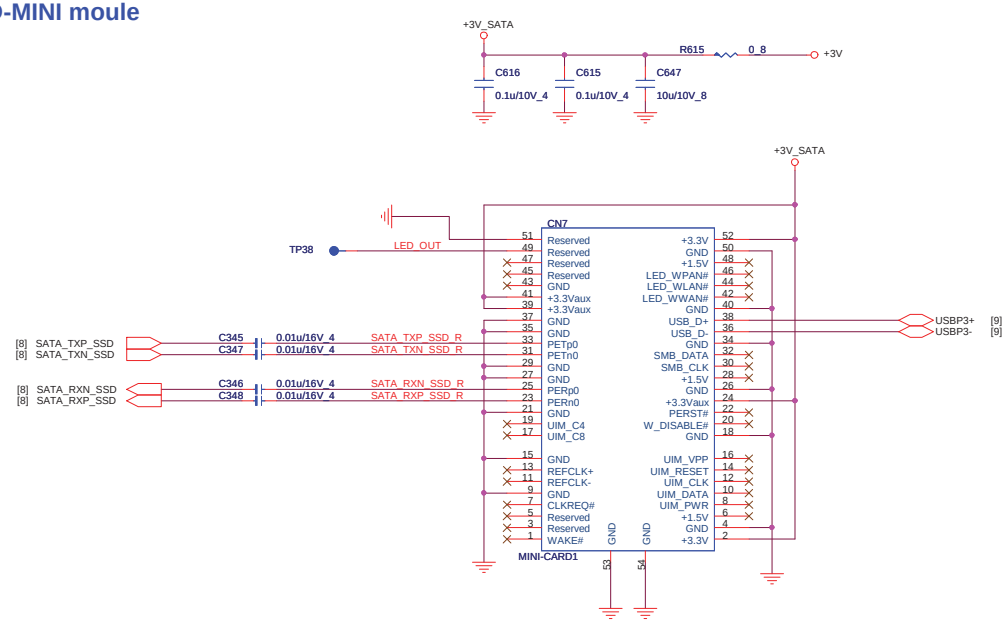
Date: Friday, November 11, 2011 Sheet 23 of 44

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

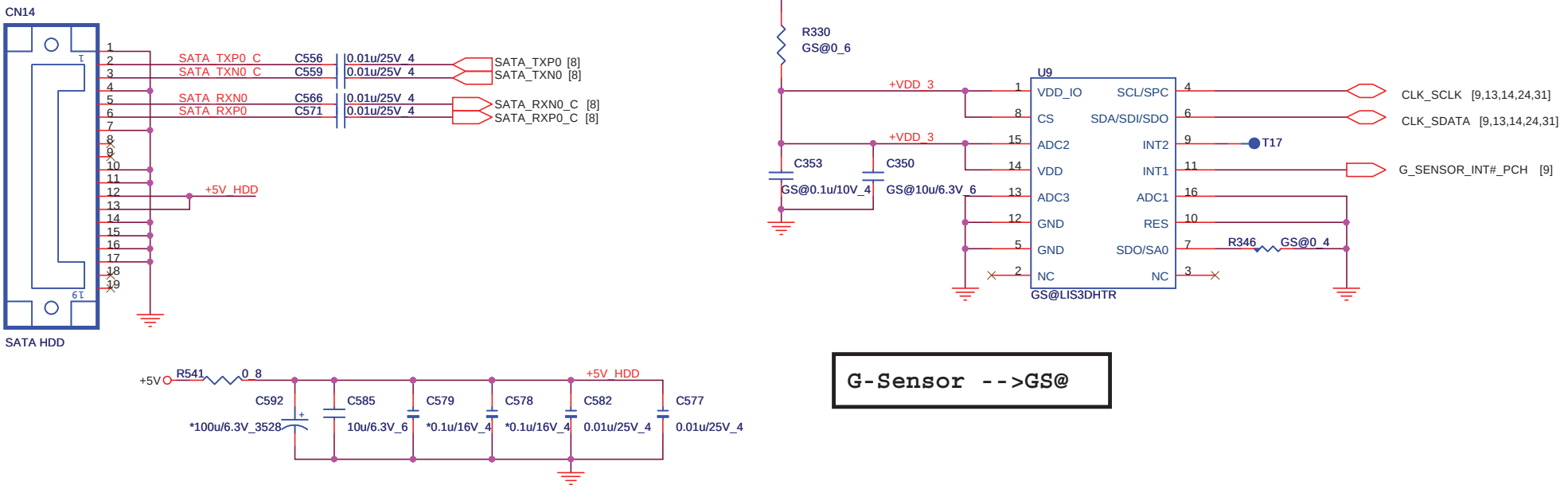


SSD-MINI moule



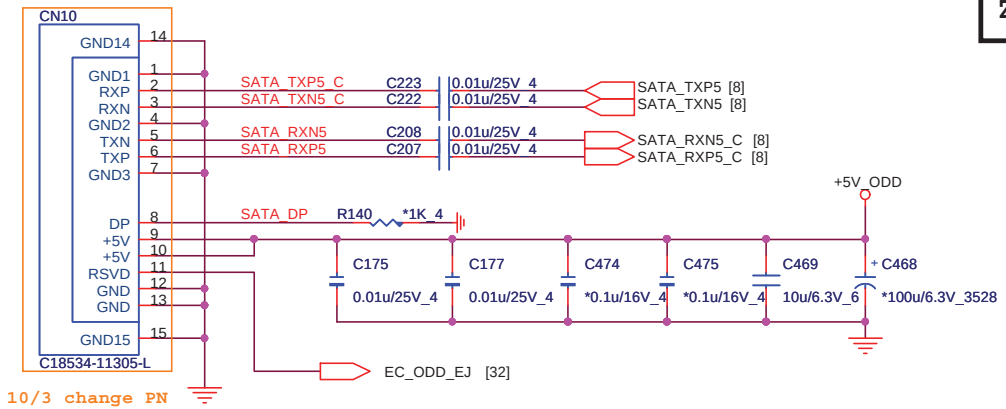
Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: MINI PCI-E / SSD	Rev: 1A
Date: Friday, November 11, 2011	Sheet 24 of 44	

MAIN SATA HDD(HDD)



G-Sensor -->GS@

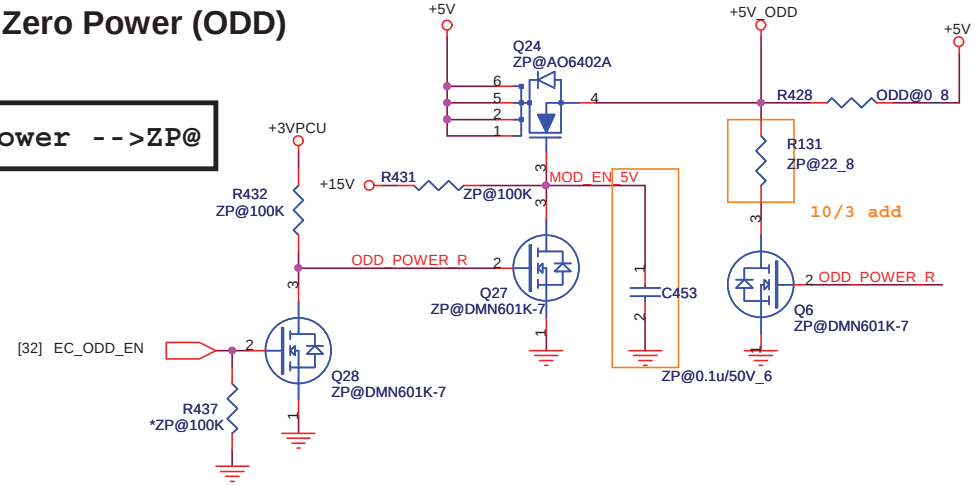
ODD (ODD)



10/3 change PN

Zero Power (ODD)

Zero Power -->ZP@



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: SATA-HDD/ODD/G Sensor	Rev 1A
Date: Friday, November 11, 2011	Sheet 25 of 44	

Codec(ADO)

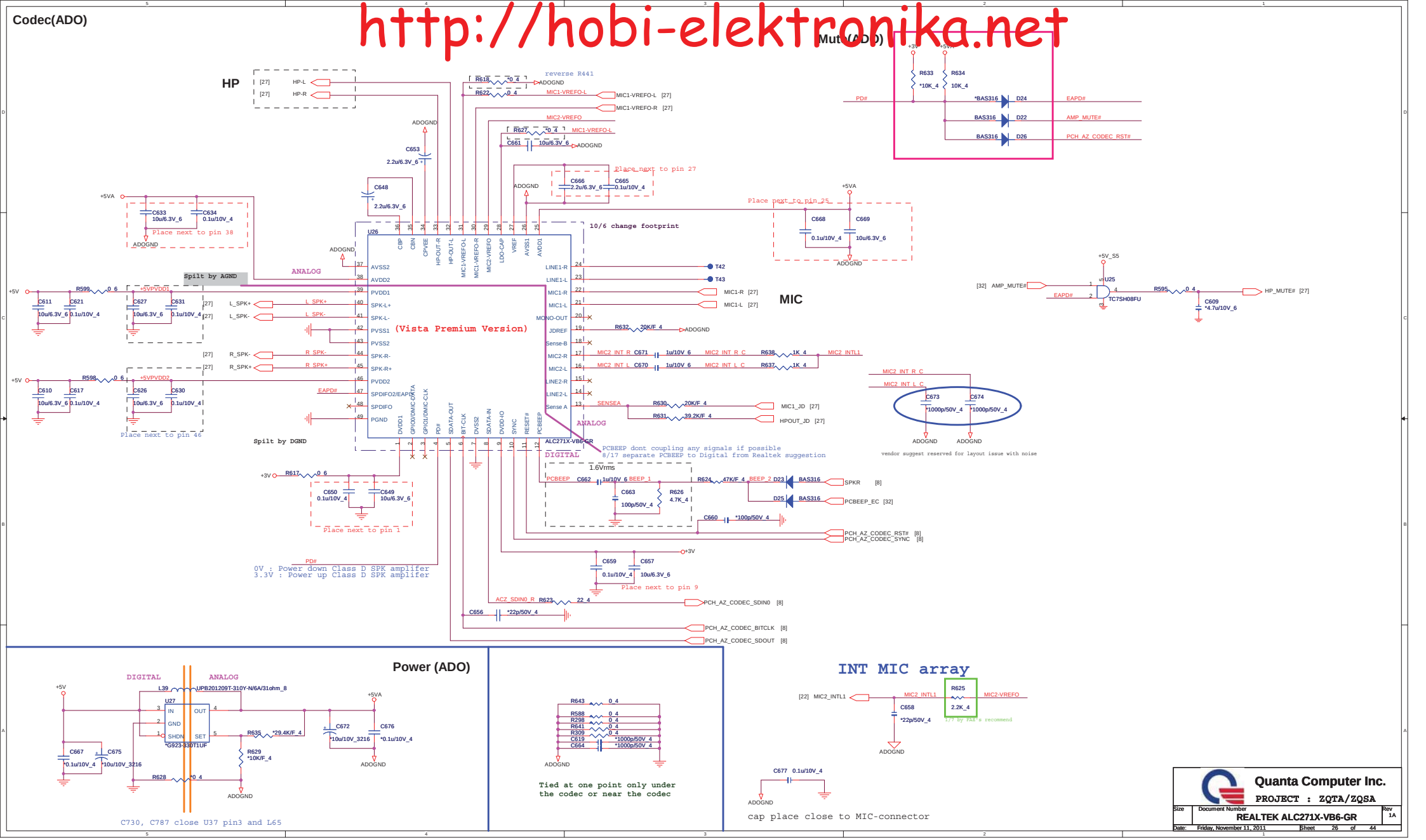
HP

Mute(ADO)

MIC

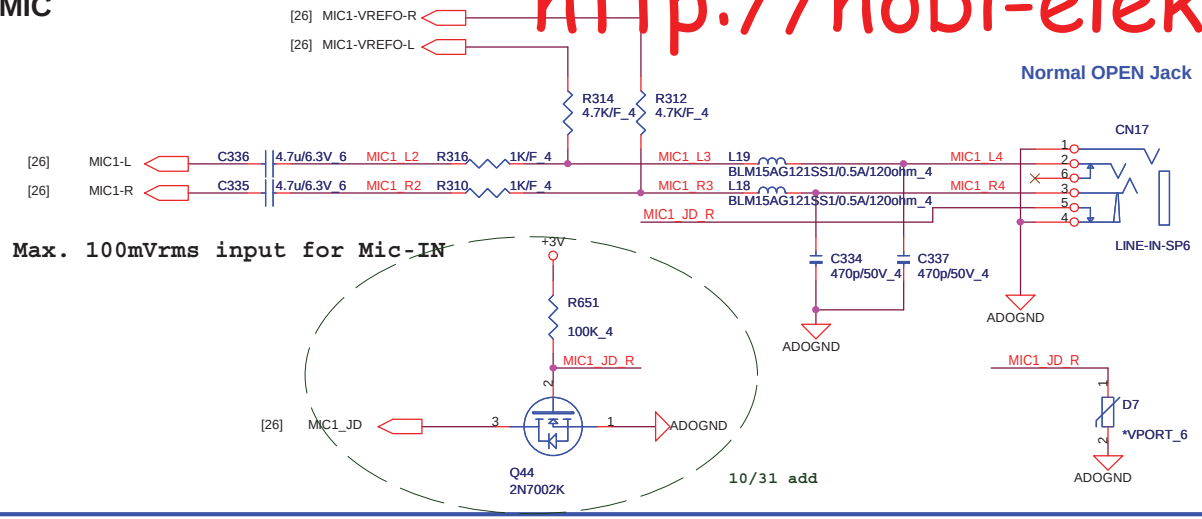
Power (ADO)

INT MIC array

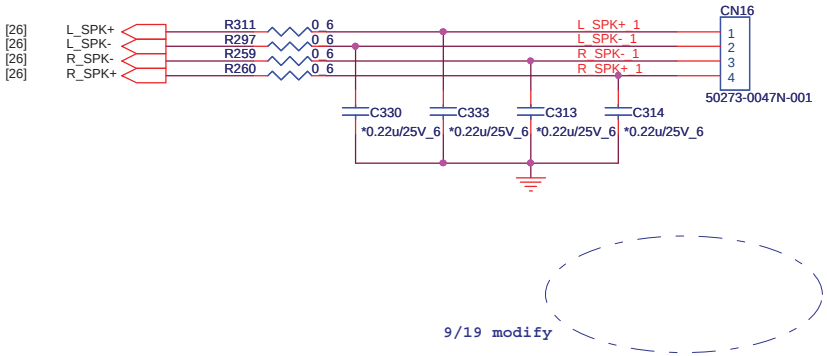


Quanta Computer Inc.			
PROJECT : ZQTA/ZQSA			
Size	Document Number		Rev
	REALTEK ALC271X-VB6-GR		1A
Date: Friday, November 11, 2011	Sheet 26 of 44		

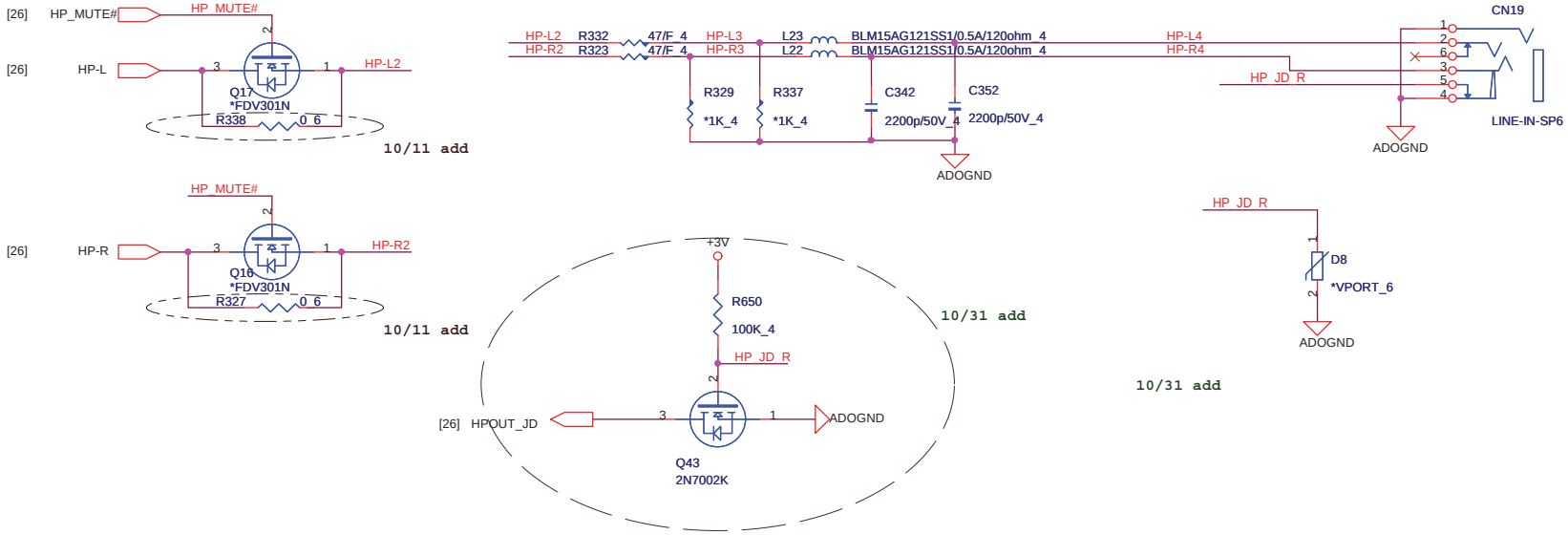
MIC



Internal Speaker

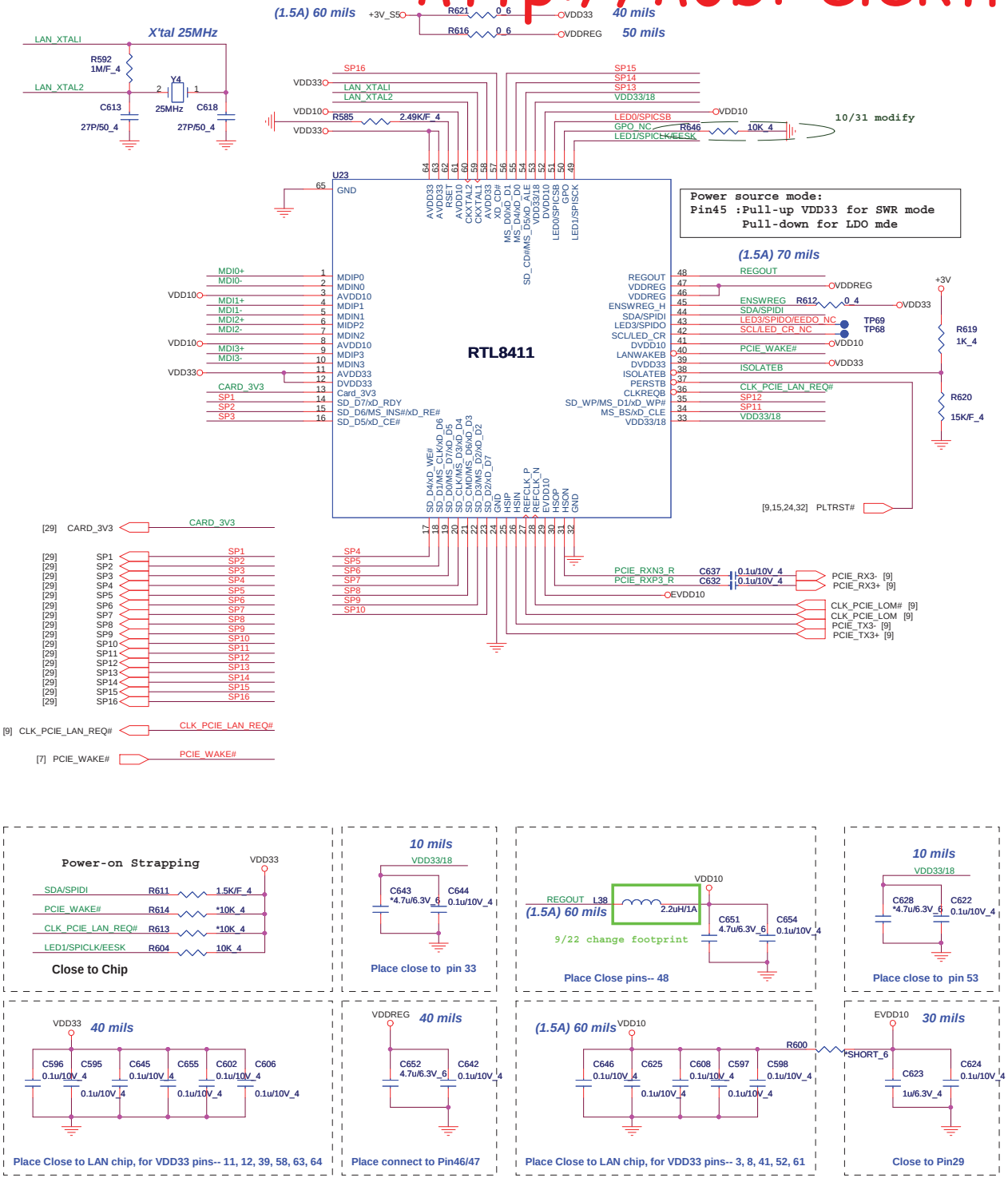


HP

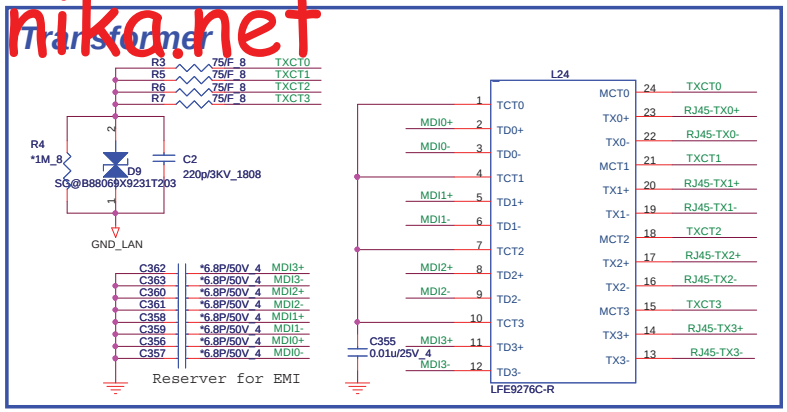


Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: AUDIO JACK CONN	Rev 1A
Date: Friday, November 11, 2011	Sheet 27 of 44	

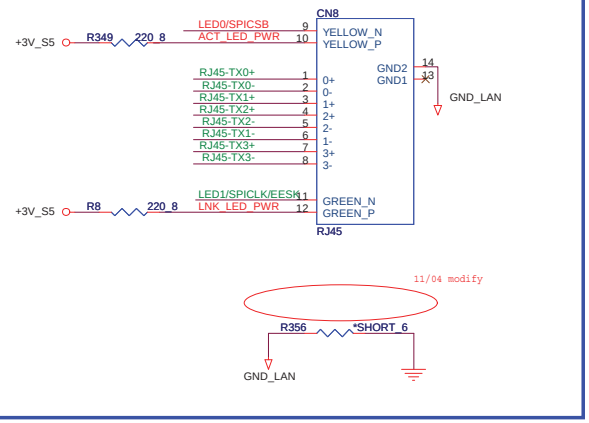
LAN/Card reader



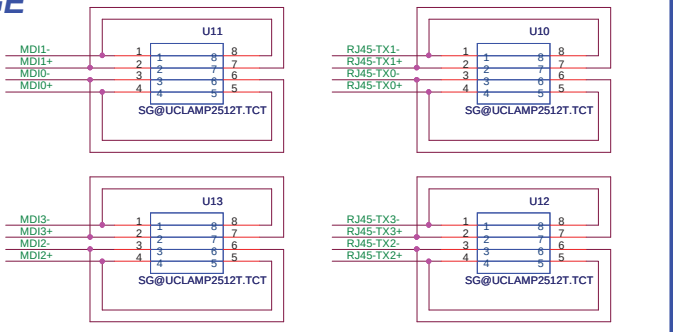
Transformer



RJ45



SURGE



[3,7,8,9,10,11,15,30,31,34,35,36,41,42] +3V_S5

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

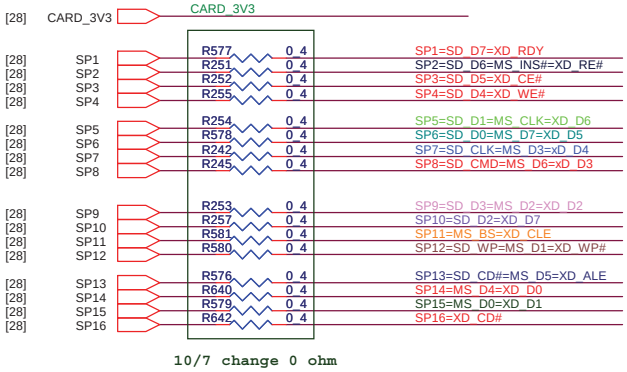
Size	Document Number	Rev
	LAN-RTL8411/CARD READER	1A
Date: Friday, November 11, 2011	Sheet 28 of 44	

CARD READER CONNECTOR

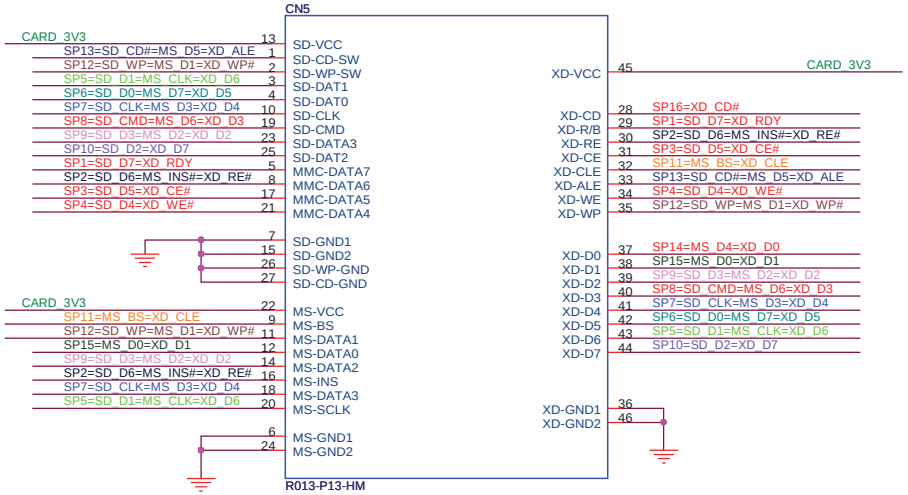
XD,MMC 4.2/SD,MS/MSP
7 IN1 CARD READER

Share Pin

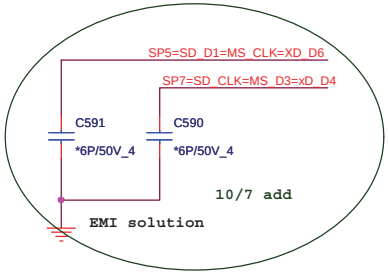
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

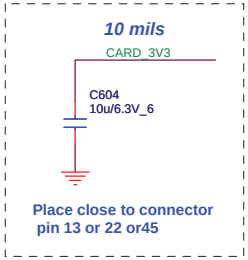


10/7 change 0 ohm



1 : DFHS44FR012
2 : :DFHS44FR014



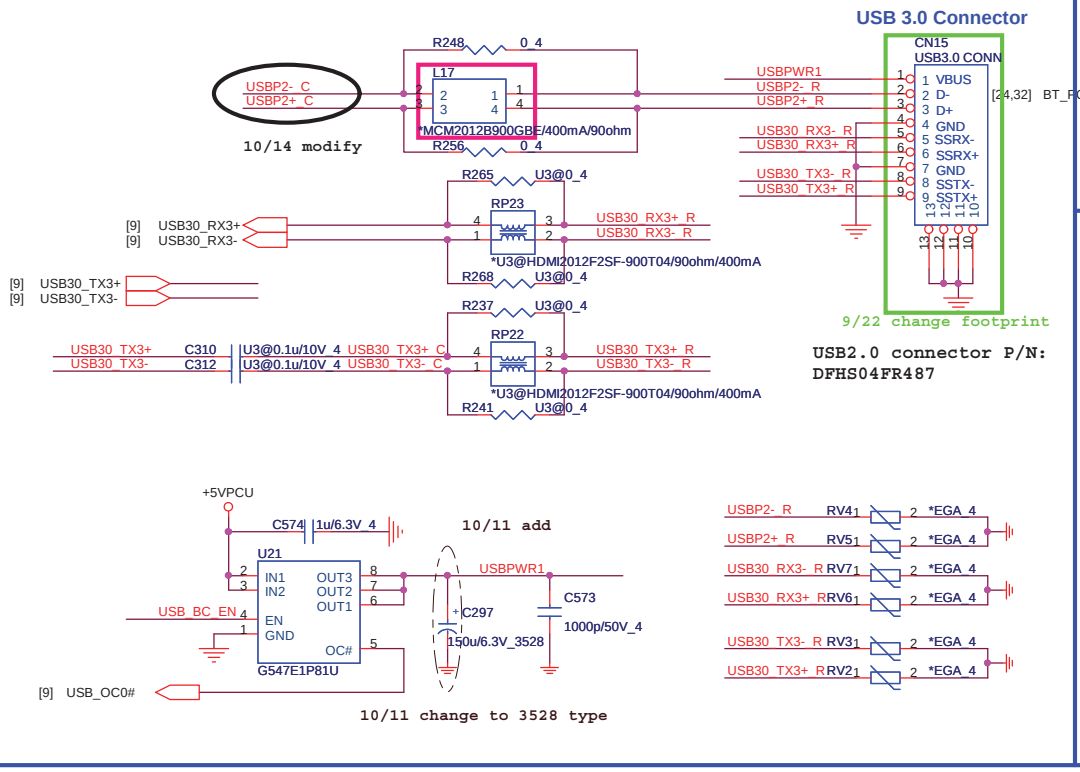


Quanta Computer Inc.

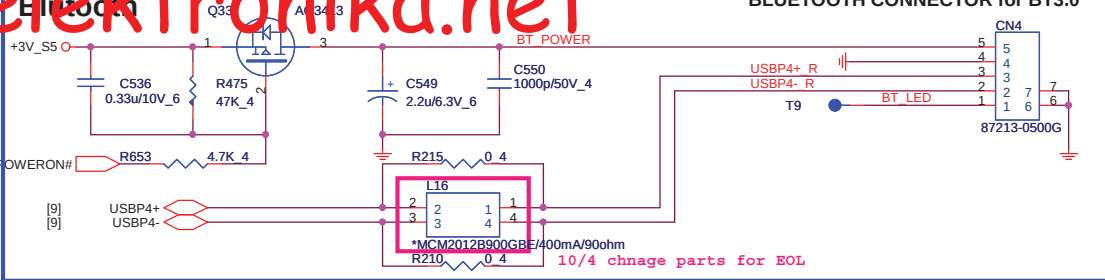
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	CARD READER CONNECTOR	1A
Date: Friday, November 11, 2011	Sheet 29 of 44	

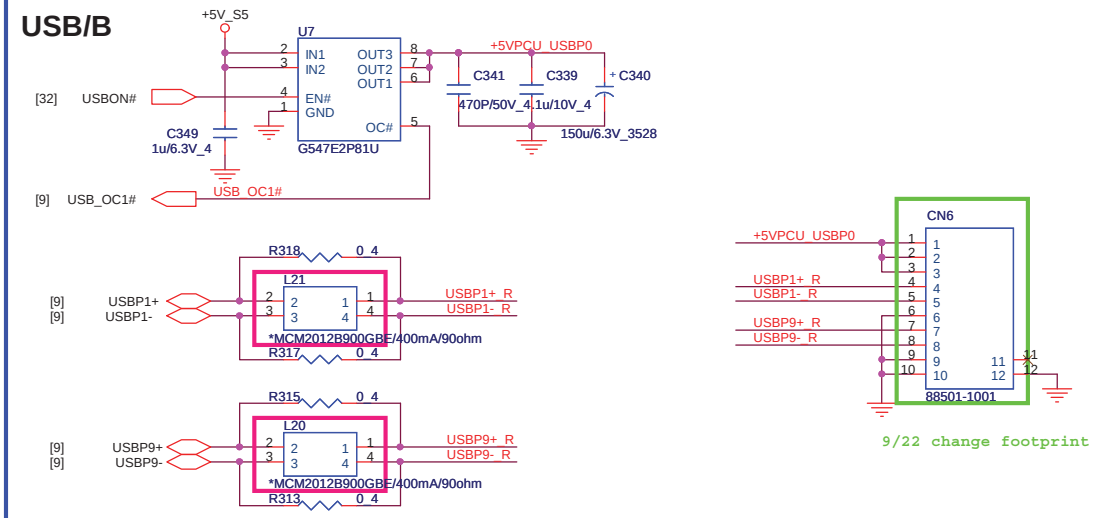
USB3.0/2.0



BLUETOOTH CONNECTOR for BT3.0



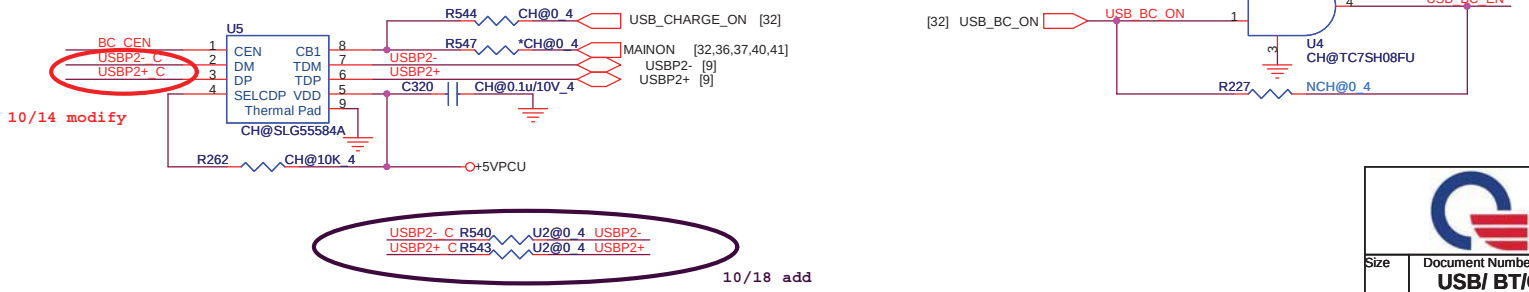
USB/B



USB Charger to 3.0

USB Charger -->CH@
None Charger--> NCH@

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



Quanta Computer Inc.			
PROJECT : ZQTA/ZQSA			
Size	Document Number		Rev
	USB/ BT/CHARGER		1A
Date: Friday, November 11, 2011		Sheet 30 of 44	

K/B

9/14 modify

KB CONN

10/11 modify

+VGACORE

RP13 10K_10P8R

CPU FAN

10/5 add

FANPWR = 1.6*VSET

G995P1U

FAN_CONN.
53398-0310-3P-L
DFHD03MR026

TOUCHPAD & Switch CONN.

Model EA/EG/BA---->SW3,SW4
VA/VG--------->SW5,SW6

50mil

10/5 modify

11/1 modify pin define

11/04 modify

LED

Power

Power Botton

Blue

Battery

HDD

Blue

WLAN

AMBER

LED_AMBER/BLUE

HDD_LED

WLAN_LED

For BA WLAN function

BA@SWITCH

*BA@EGA-0402

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	KB/FAN/TP+FP/LED	1A
Date: Friday, November 11, 2011	Sheet 31 of 44	

EC(KBC)

L13 PBY160808T-250Y-N/3A/25ohm_6 — +3VPCU — 30mil — 0.03A(30mils)

+3VPCU — R156 2.2_6 — +3VPCU_EC

C224 4.7u/6.3V_6 | C220 0.1u/10V_4 | C203 *0.1u/16V_4 | C217 0.1u/10V_4 | C206 *0.1u/16V_4 | C483 0.1u/10V_4

C228 0.1u/10V_4 | C226 10u/6.3V_6 — E775AGND

3V — D13 RB500V-40 — C522 4.7u/6.3V_6 | C523 0.1u/10V_4

U17 WPCE885

VCC1 VCC2 VCC3 VCC4 VCC5 AVCC VDD

CLK_PCI_775 — R152 *22_4 — C218 *10p/50V_4

LPC

[8,24] LPC_LFRAME#	3	LFRAME
[8,24] LPC_LAD0	126	LAD0
[8,24] LPC_LAD1	127	LAD1
[8,24] LPC_LAD2	128	LAD2
[8,24] LPC_LAD3	1	LAD3
[9] CLK_PCI_775	2	LCLK
[7] CLKRUN#	8	GPIO11/CLKRUN
[10] SIO_A20GATE	121	GPIO85/GA20
[10] SIO_RCIN#	122	KBRST/GPIO86
[10] SIO_EXT_SCI#	29	ECSCI/GPIO54
[22] EC_FPBACK#	6	GPIO24/LDRQ
[26] AMP_MUTE#	124	GPIO10/LPCPD
[9,15,24,28] PLTRST#	7	LRESET (PLTRST#)
[24] RF_EN	123	GPIO67/PWUREQ
[8] IRQ_SERIRQ	125	SERIRQ
[10] SIO_EXT_SMI#	9	GPIO65/SMI

KB

[31] MX0	54	KBSIN0
[31] MX1	55	KBSIN1
[31] MX2	56	KBSIN2
[31] MX3	57	KBSIN3
[31] MX4	58	KBSIN4
[31] MX5	59	KBSIN5
[31] MX6	60	KBSIN6
[31] MX7	61	KBSIN7
[31] MY0	53	KBSOUT0/JENK
[31] MY1	52	KBSOUT1/TCK
[31] MY2	51	KBSOUT2/TMS
[31] MY3	50	KBSOUT3/TDI
[31] MY4	49	KBSOUT4/JEN0
[31] MY5	48	KBSOUT5/TDO
[31] MY6	47	KBSOUT6/RDY
[31] MY7	43	KBSOUT7
[31] MY8	42	KBSOUT8
[31] MY9	41	KBSOUT9/SDP_VIS
[31] MY10	40	KBSOUT10/P80_CLK
[31] MY11	39	KBSOUT11/P80_DAT
[31] MY12	38	KBSOUT12/GPIO64
[31] MY13	37	KBSOUT13/GPIO63
[31] MY14	36	KBSOUT14/GPIO62
[31] MY15	35	KBSOUT15/GPIO61/XOR_OUT
[31] MY16	34	GPIO60/KBSOUT16
[31] MY17	33	GPIO57/KBSOUT17

SMB

[33] MBCLK	70	GPIO17/SCL1
[33] MBDATA	69	GPIO22/SDA1
[9] 2ND_MBCLK	67	GPIO73/SCL2
[9] 2ND_MBDATA	68	GPIO74/SDA2
[18] GPUT_CLK	119	GPIO23/SCL3
[18] GPUT_DATA	120	GPIO31/SDA3

PS/2

[31] TPCLK	72	GPIO37/PSCLK1
[31] TPDATA	71	GPIO35/PSDAT1
[8] ME_WR	10	GPIO26/PSCLK2
[24,30] BT_POWERON#	11	GPIO27/PSDAT2
[25] EC_ODD_EN	77	GPIO00/32KCLKIN

Reserve for writing ME ROM

[3] EC_PECI — +1.05V — R147 0_4 — R142 43_4 — +1.05V_VTT_EC — EC_PECR_R

VTT - the power supply for the PECI signal
PECI - the PECI 3.0 data bus, bidirectional signal.

DG0.9 and chklist 0.9 apply one series 43ohm near EC side

VTT 12 — PECI 13

GND1 5 | GND2 18 | GND3 45 | GND4 78 | GND5 89 | GND6 116 | AGND 103 | VCORF 44

L11 PBY160808T-250Y-N/3A/25ohm_6 — E775AGND — C478 1u/6.3V_4 — VCORF_UR_44

A/D

GPIO90/AD0	97	TEMP_MBAT [33]
GPIO91/AD1	98	T46
GPIO92/AD2	99	T32
GPIO93/AD3	100	ICM [33]

D/A

GPIO94/DA0	101	T33
GPI95/DA1	105	CPUFAN#_DAC [31]
GPI96/DA2	106	T35

E775AGND — C519 10u/6.3V_8 ICM — C518 0.01u/25V_4

GPIO

GPIO01/TB2	64	ACIN [33]
GPIO02	79	T26
GPIO03	95	NBSWON#
GPIO04	96	RF_SW# [31] — 11/9 modify
GPIO05	108	T36
GPIO06/IOX_DOUT/RTS1	93	LID591# [22]
GPIO07	94	M_PON_R — R644 *SHORT_4 — M_PON [42]
GPIO16	114	SLP_A#_R — R645 *SHORT_4 — SLP_A# [7] — 10/31modify
GPIO30	109	T31
GPIO36/CTS1	15	T28
GPIO41	80	VRON [35]
GPIO42/SCL3B/TCK	17	HWPG
GPIO43/SDA3B/TMS	20	VGA_THERM#_R — R449 *SHORT_4 — GPU_THERMAL_ALERT# [18]
GPIO44/TDI	21	SUSB# [7]
GPO47/SCL4	24	T21
GPIO50/PSCLK3/TDO	25	D/C# [33]
GPIO51	26	S5_ON — S5_ON [34,41]
GPIO52/PSDAT3/RDY	27	HDMI_HPD_EC# [23]
GPIO53/SDA4	28	T22
GPIO70	73	SUSC# [7]
GPIO71	74	PWROK_EC [7]
GPIO72	75	PCH_RSMRST# [7]
GPIO75/SPI_SCK	82	MAINON [30,36,37,40,41]
GPO76/SHBM	83	T29
GPIO77	84	EC_ODD_EJ [25]
GPIO81	91	DNBSWON# [7]
GPO82/IOX_LDSH/TEST	110	Do not use it — T34
GPO84/IOX_SCLK/XORTR	112	USBON# [30]
GPIO97	107	USB_CHARGE_ON [30]

TIMER

GPIO56/TA1	31	T20
GPIO20/TA2/IOX_DIN_DIO	117	SUSON [37]
GPIO14/TB1	63	FANSIG [31]
GPIO15/A_PWM	32	CONTRAST [22]
GPIO21/B_PWM	118	PCBEEP_EC [26]
GPIO13/C_PWM	62	PWRLED# [31]
GPIO32/D_PWM	65	BATLEDD# [31]
GPIO45/E_PWM	22	T25
GPIO40/F_PWM/RI1	16	SUSLED# — SUSLED# [31]
GPIO66/G_PWM	81	T27
GPIO33/H_PWM/SOUT1	66	BATLED1# [31]

IR

GPIO87/CIRRXM/SIN_CR	113	USB_BC_ON [30]
GPIO34/SIN1/CIRRXL	14	+0.75V_ON [37]
GPIO46/CIRRXM/TRST	23	T24
GPO83/SOUT_CR/TRIST	111	PROCHOT_EC

FIU

F_SDI/F_SDIO1	86	PCH_SPI_SO [8]
F_SDO/F_SDIO0	87	PCH_SPI_SI [8]
F_CS0	90	SPI_CS0#_UR_ME [8]
F_SCK	92	PCH_SPI_CLK [8]
GPIO55/CLKOUT/IOX_DIN_DIO	30	T23
VCC_POR	85	VCC_POR# — R146 47K/F_4 — +3VPCU
VREF	104	+A3VPCU

pin14 +VCC_GFX — pin13 GFX_PWRGD
pin22 +3V_D for ATI — pin21 dGPU_VRON
pin24 +1V for ATI — pin23 +VGPU_CORE
pin26 +1.8V_GPU for ATI — pin25 +1.5V_GPU
pin28 GPU_RST# — pin27 dGPU_PWROK

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

Power on bottom

+3VPCU — R1 10K_4 — NBSWON# — C1 0.1u/10V_4 — D1 *VPORT_6 — SW2 SWITCH — 11/04 modify

SM BUS PU(KBC)

+3VPCU

MBCLK	R434	10K_4
MBDATA	R435	10K_4
GPUT_CLK	R155	10K_4
GPUT_DATA	R154	10K_4
2ND_MBCLK	R143	10K_4
2ND_MBDATA	R144	10K_4

10/11 add

PROCHOT_EC — R465 100K_4 — Q31 2N7002K — H_PROCHOT# [3,35]

HWPG(KBC)

+3V — R463 10K_4 — HWPG

[38] HWPG_VCCSA	D14	BAS316
[41] HWPG_1.8V	D17	BAS316
[36,38] HWPG_VTT	D15	*BAS316
[37] HWPG_VDDR	D16	BAS316
[34] SYS_HWPG	D18	BAS316

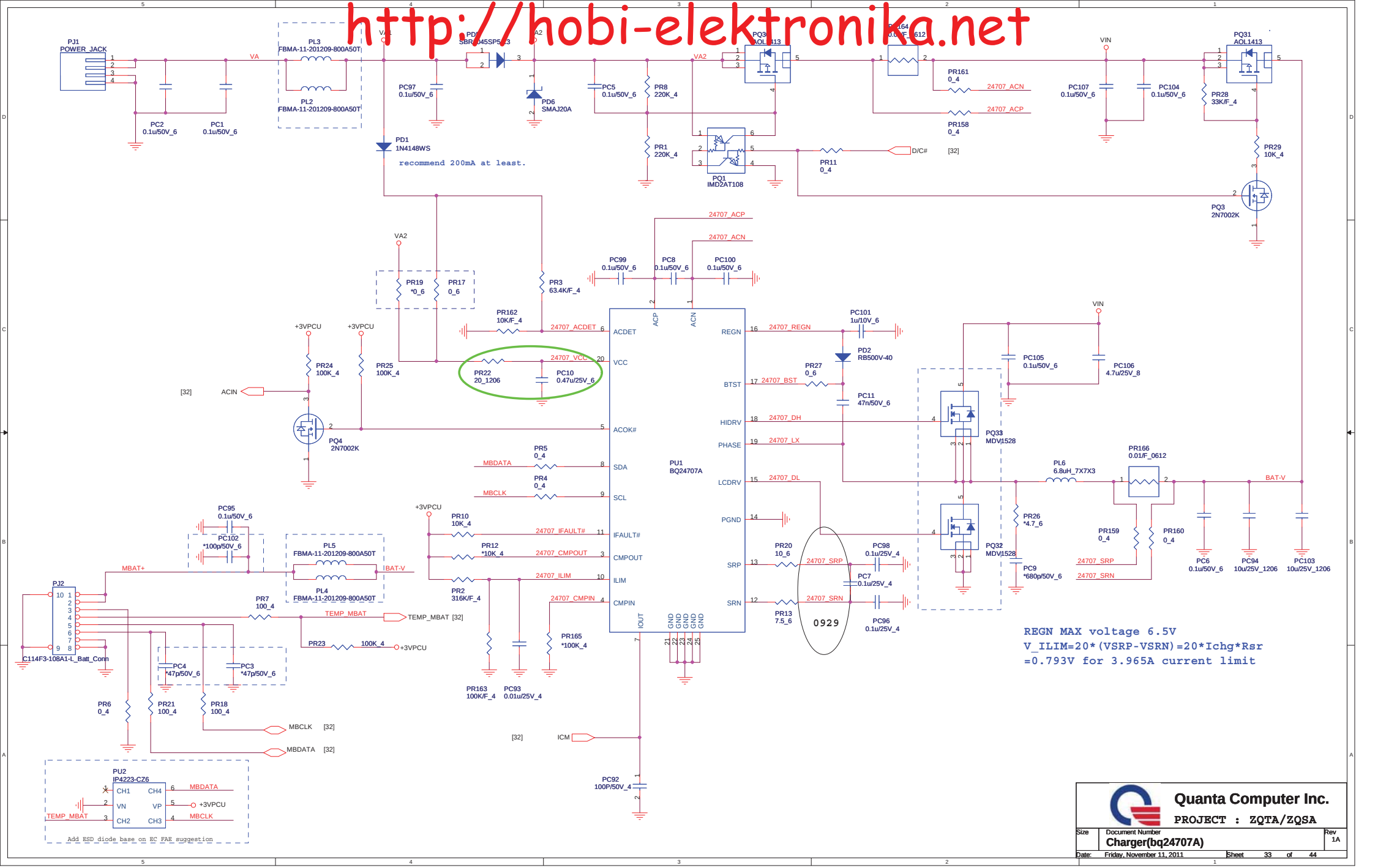
+3VPCU — S5_ON — R141 VA@10K_4 — M_PON — R654 BA@10K_4

11/2 modify

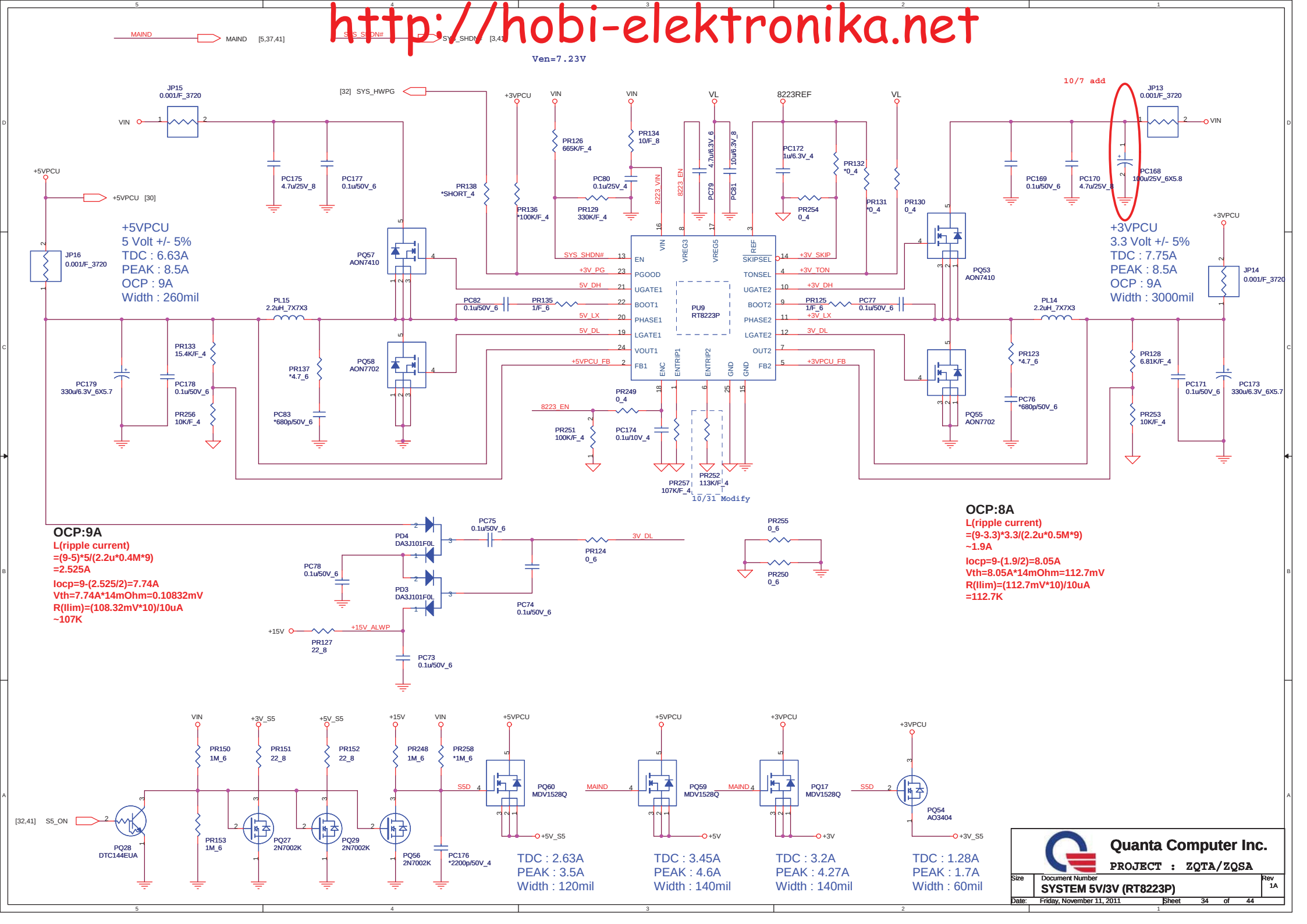
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

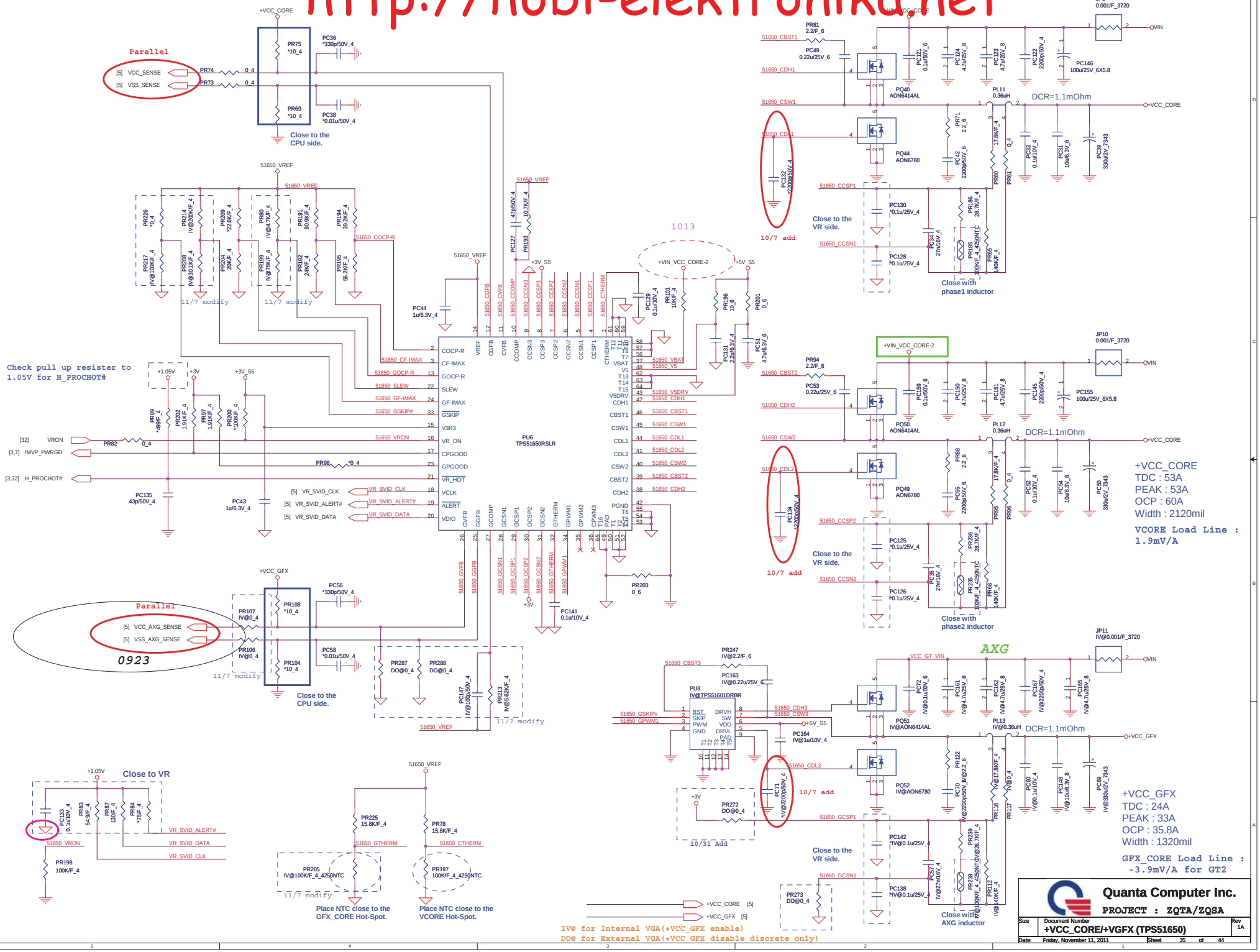
Size	Document Number	Rev
	WPCE885 & FLASH	1A

Date: Friday, November 11, 2011 — Sheet 32 of 44

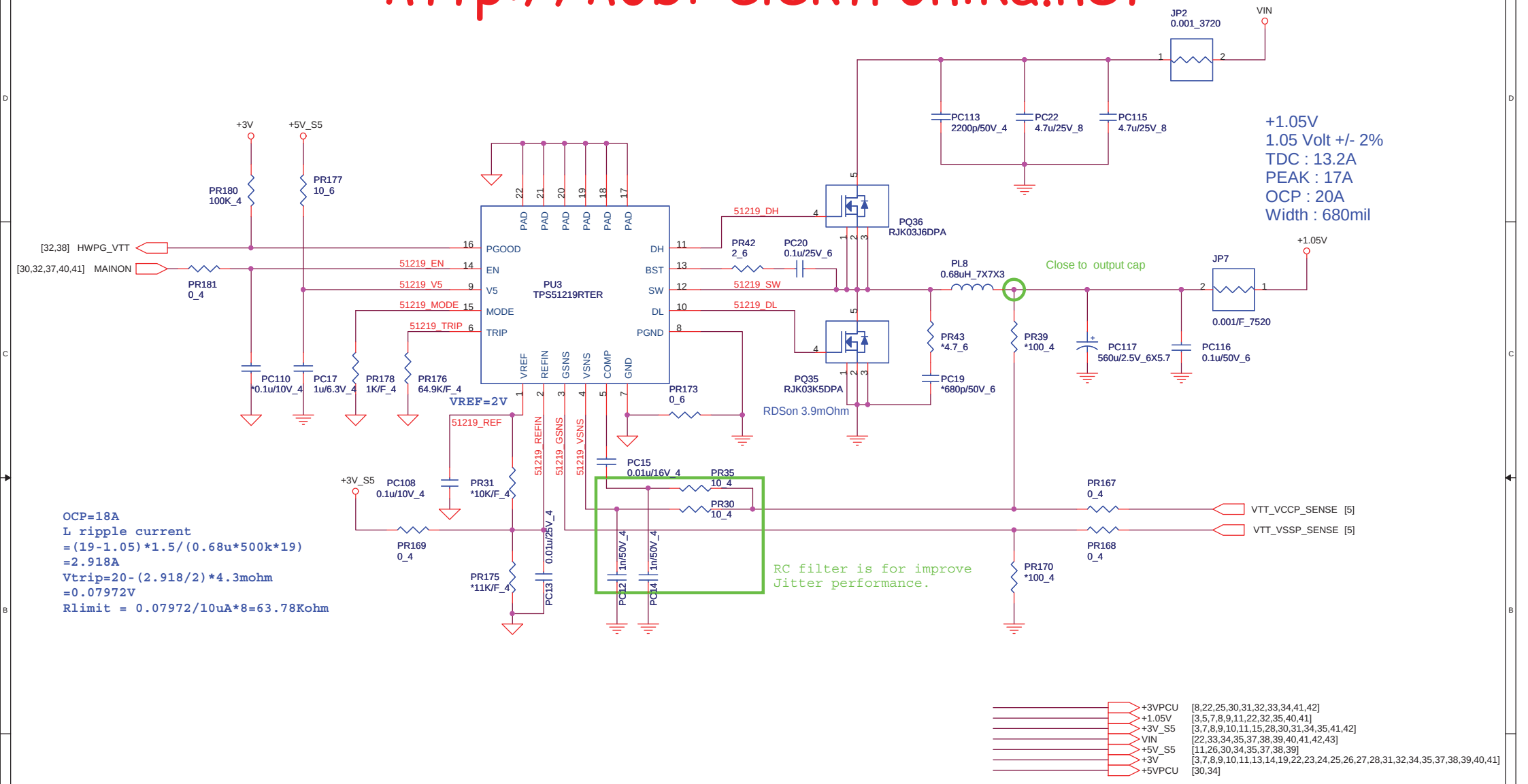


Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: Charger(bq24707A)	Rev: 1A
Date: Friday, November 11, 2011	Sheet 33 of 44	





Quanta Computer Inc.	PROJECT : ZQTA/ZQSA	
Size	Document Number: +VCC_CORE/+VGFX (TPS51650)	Rev 1A
Date: Friday, November 11, 2011	Sheet 35 of 44	

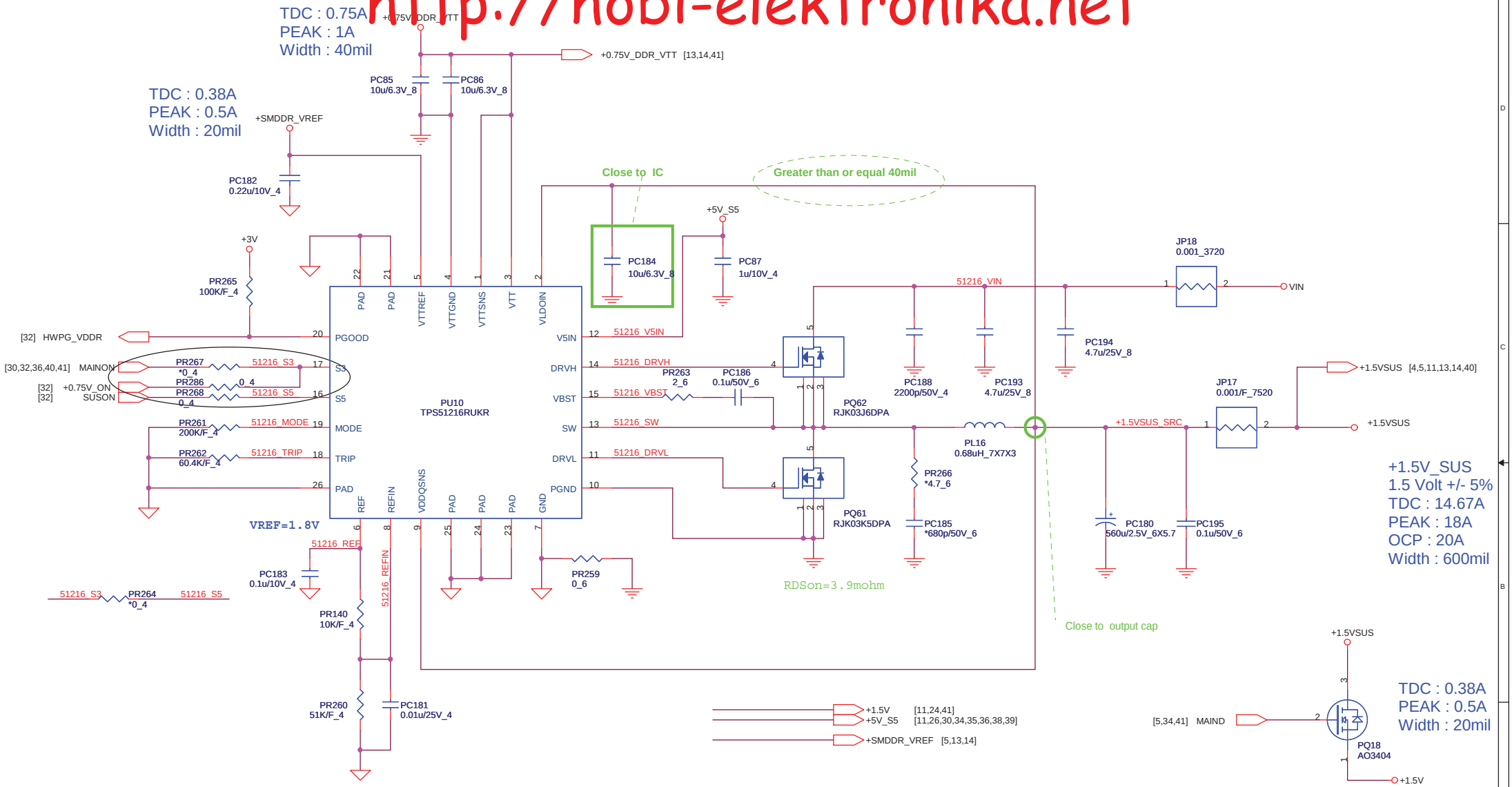


+3VPCU	[8,22,25,30,31,32,33,34,41,42]
+1.05V	[3,5,7,8,9,11,22,32,35,40,41]
+3V_S5	[3,7,8,9,10,11,15,28,30,31,34,35,41,42]
VIN	[22,33,34,35,37,38,39,40,41,42,43]
+5V_S5	[11,26,30,34,35,37,38,39]
+3V	[3,7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41]
+5VPCU	[30,34]

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V (TPS51219)	1A
Date: Friday, November 11, 2011	Sheet 36 of 44	



OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*4.3mohm
=0.07508V
Rlimit=0.07508/10uA*8=60.063Kohm

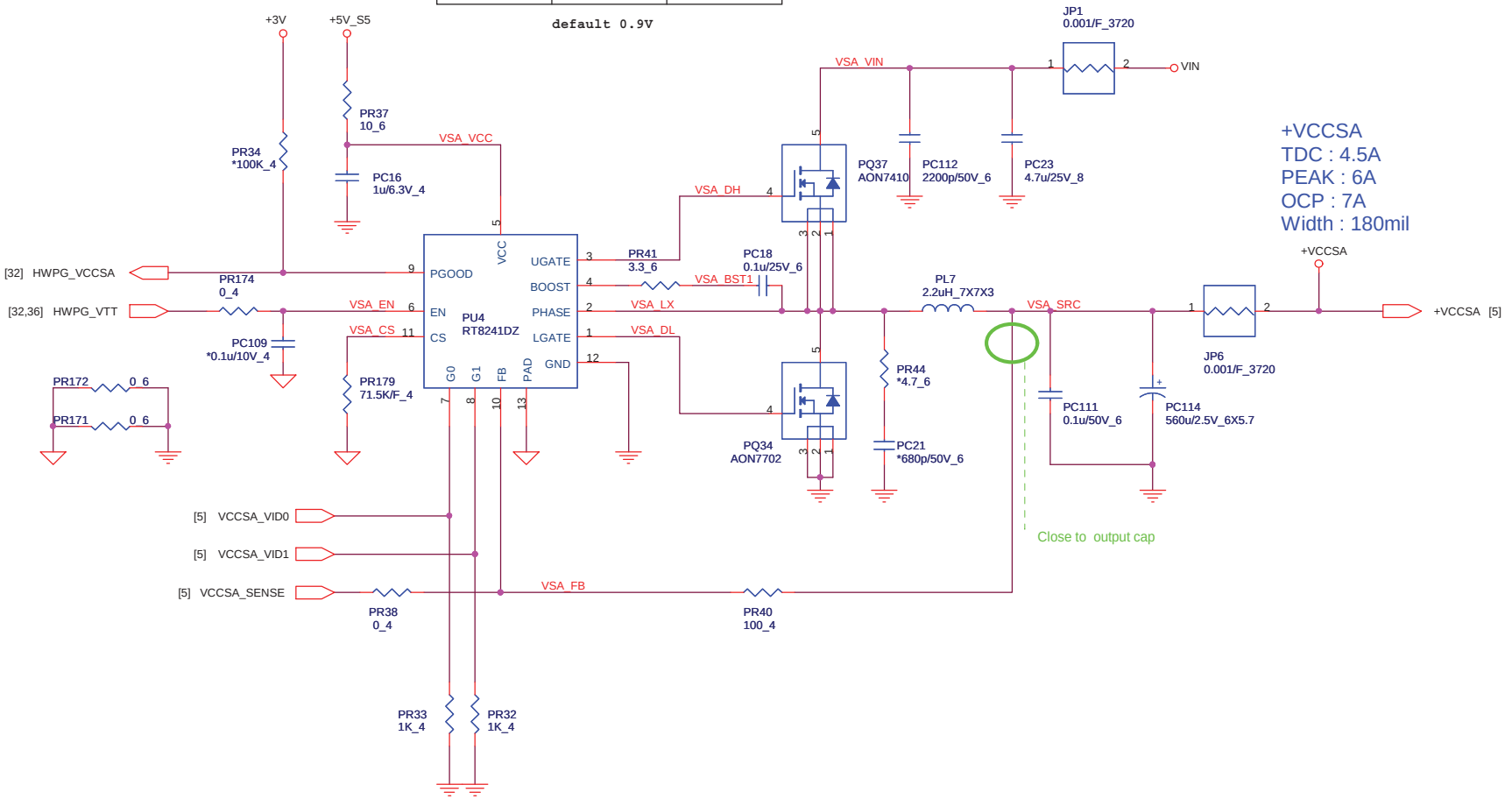
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
Date: Friday, November 11, 2011	Sheet 37 of 44	

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

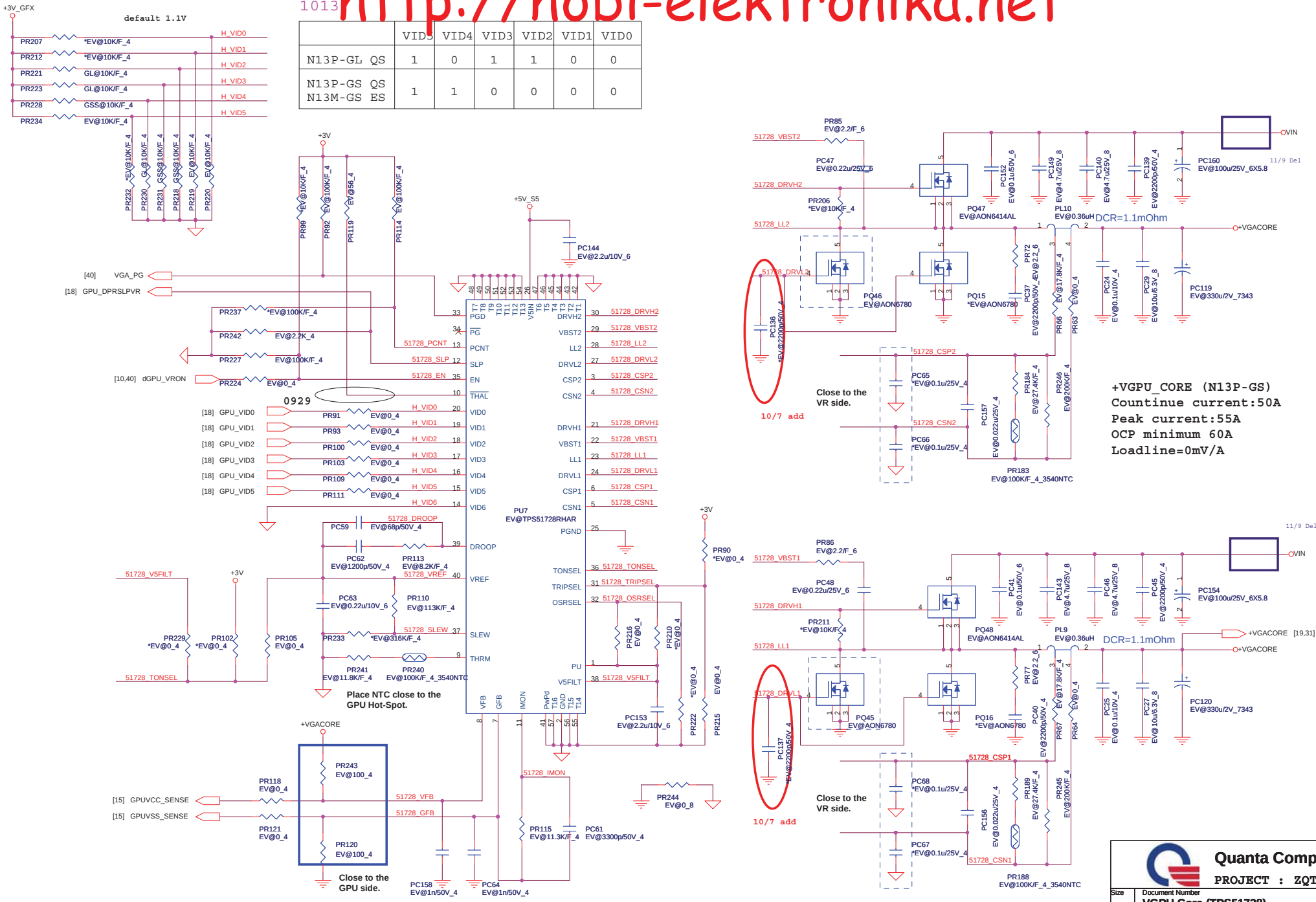


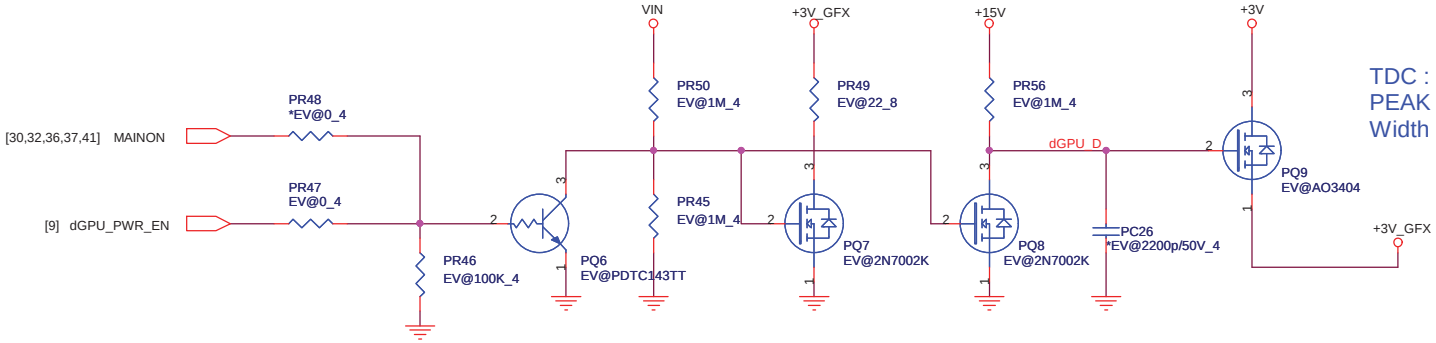
OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

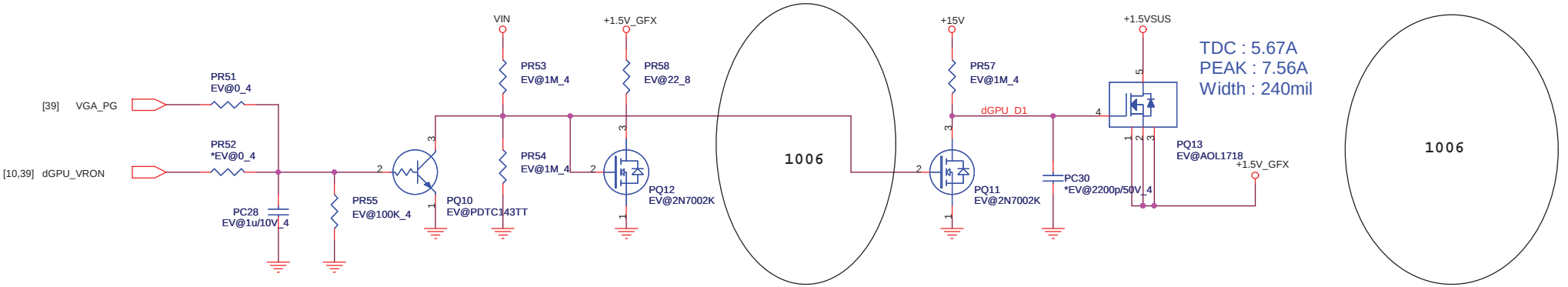
Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: VCCSA(RT8241DZ)	Rev: 1A
Date: Friday, November 11, 2011	Sheet 38 of 44	

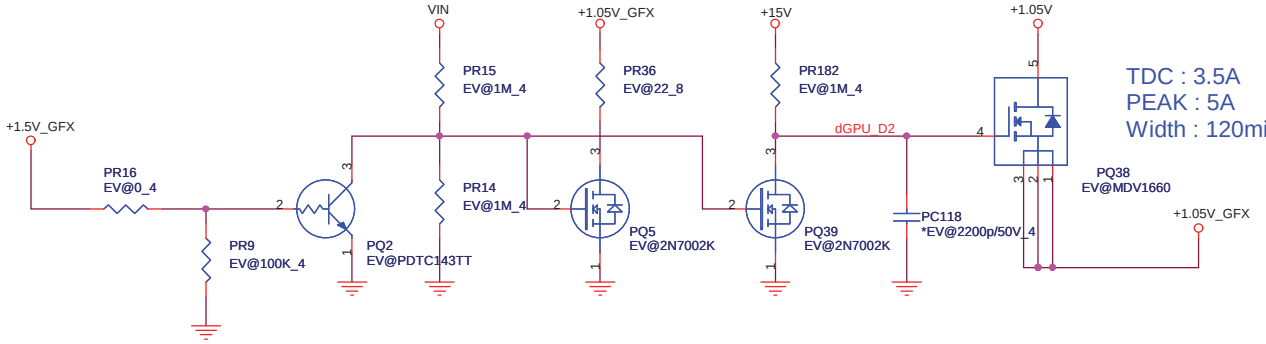
1013

	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS N13M-GS ES	1	1	0	0	0	0









Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	GPU_PWR	1A

Date: Friday, November 11, 2011 Sheet 40 of 44

+1.8V
1.8 Volt +/- 5%
TDC : 1.61A
PEAK : 2A
Width : 60mil

+3VPCU
PC187 10u/6.3V_8
PC190 0.1u/25V_4
PU11 TPS54318RTER
VIN PH BOOT PWRGD GND GND AGND VSNS COMP RT/CLK SS EN PAD
[30,32,36,37,40] MAINON
PR154 *100K/F_4
PC89 1000p/50V_4
54418-1_VFB
PR271 10K/F_4
PR270 121K/F_4
PC192 *100p/50V_4
PC196 1200p/50V_4
PC191 0.01u/25V_4
PR269 0_6
PC189 0.1u/50V_6
PL1 1uH_7X7X3
HWPG_1.8V [32]
PR155 *100K/F_4
+3V_S5
+1.8V
JP5 0.001/F_3720
R1 PR157 100K/F_4
R2 PR156 78.7K/F_4
PC88 0.1u/25V_4
PC90 10u/6.3V_8
PC91 10u/6.3V_8
V0=0.8*(R1+R2)/R2

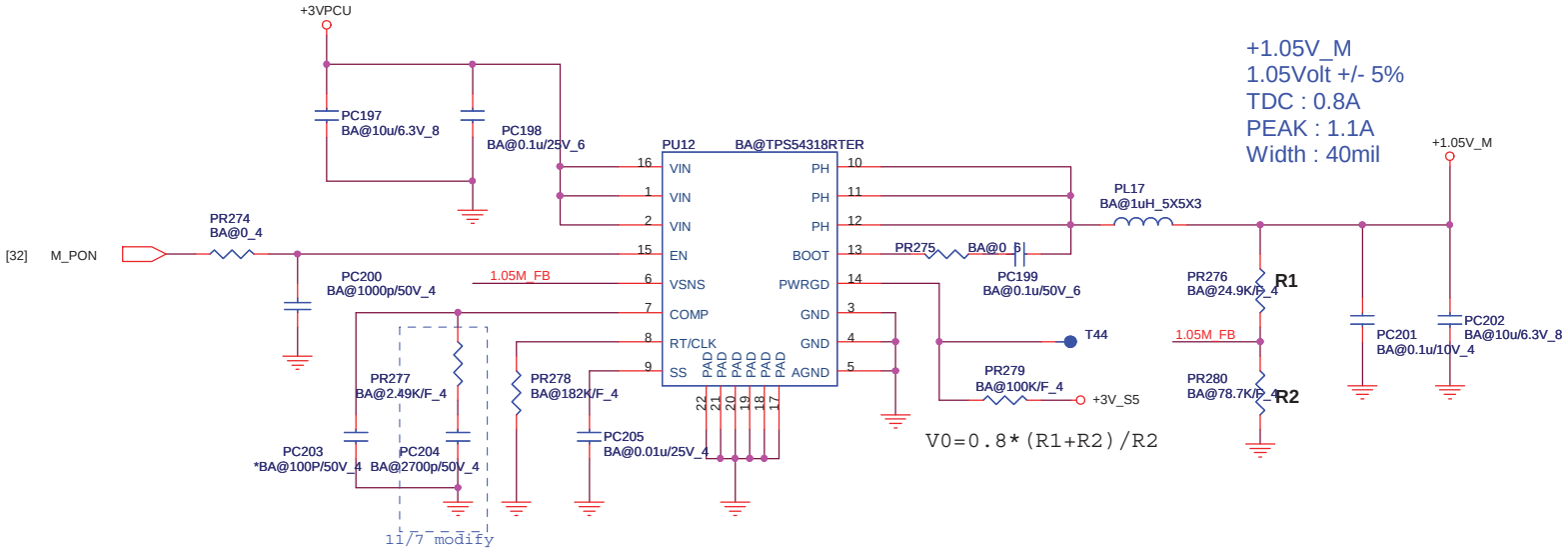
Thermal protection

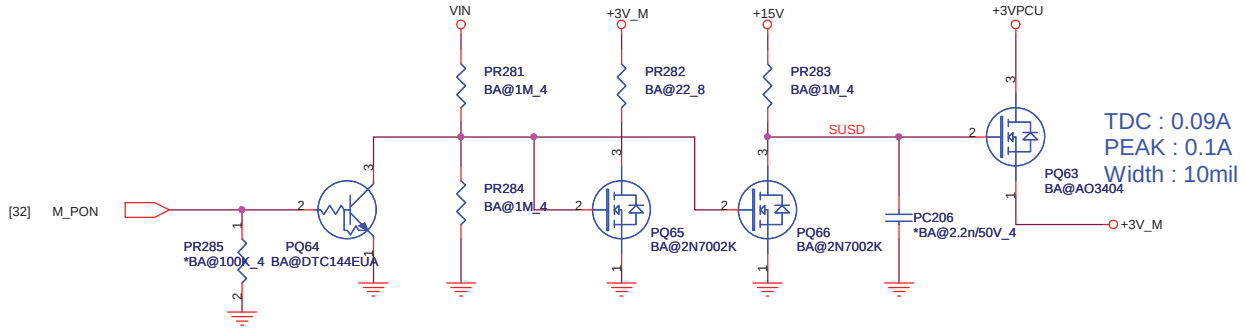
VIN
PD7 DA2J10100L
PR190 1M_6
PQ41 AO3409
[32,34] S5_ON
PQ42 DTC144EUA
PR59 0_6
VL
PR70 1.74K/F_4
PR76 200K/F_4
PR187 10K_6_NTC
2.469V
PR79 200K/F_4
PC166 0.1u/50V_6
PR62 200K_6
PU5A BA10393F
PC33 0.1u/50V_6
PQ43 2N7002K
PU5B BA10393F
SYS_SHDN# [3,34]
PQ14 2N7002K

[3,5] MAINON_ON_G
MAINON
PQ19 DTC144EUA
PR141 *100K/F_6
PR142 1M_4
PR143 1M_4
PR146 22_8
PR145 22_8
PR148 22_8
PR147 22_8
PR144 22_8
PR149 22_8
PR139 1M_4
+3V +5V +0.75V_DDR_VTT +1.5V +1.05V +1.8V +15V
PQ22 2N7002K
PQ21 2N7002K
PQ25 2N7002K
PQ24 2N7002K
PQ20 2N7002K
PQ26 2N7002K
PQ23 2N7002K
MAIND
MAIND [5,34,37]
PC84 *2200p/50V_4
[13,14,37] +0.75V_DDR_VTT

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size | Document Number +1.8V/Discharge/Thermal | Rev 1A
Date: Friday, November 11, 2011 | Sheet 41 of 44



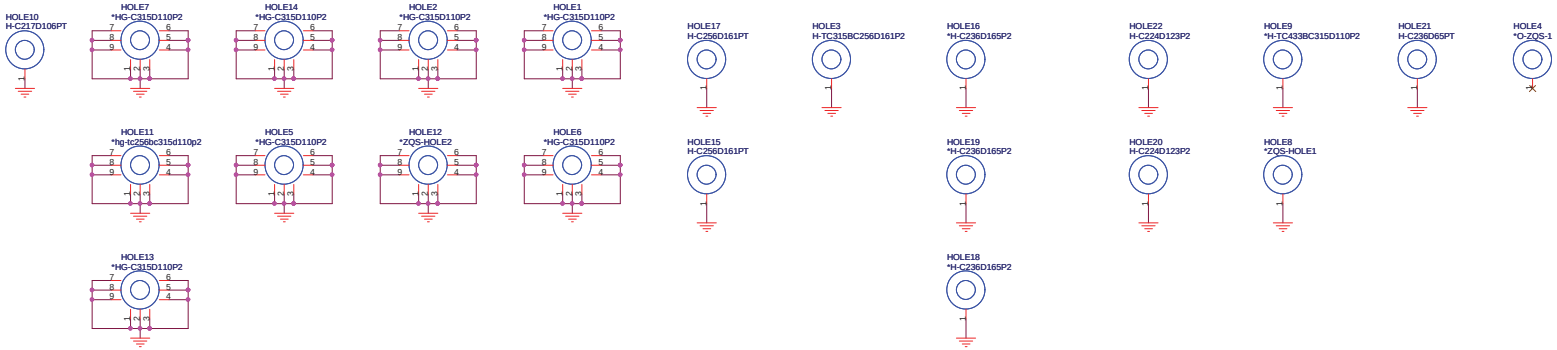


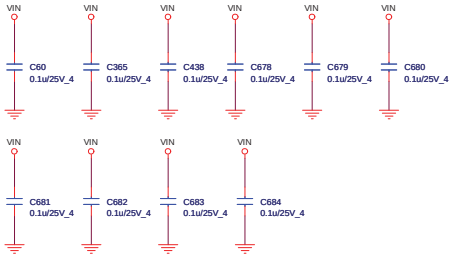
Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V_M/+3V_M	1A
Date: Friday, November 11, 2011	Sheet 42 of 44	

Hole





Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	Hole	1A

Date: Friday, November 11, 2011 Sheet 43 of 44

CHANGE LIST

Model	date	
ZASA/ZSQTA	9/26	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	9/27	Update power circuit Page19 : add C3777,C3778
	9/30	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	10/3	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	10/4	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	10/5	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	10/6	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	10/7	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	10/11	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	10/14	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581

Quanta Computer Inc. PROJECT : ZQTA/ZQSA Size: Document Number: Change list; Rev: 1A Date: Friday, November 11, 2011; Sheet 44 of 44	DOC NO.	PROJECT MODEL :	ZQTA/ZQSA	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON: