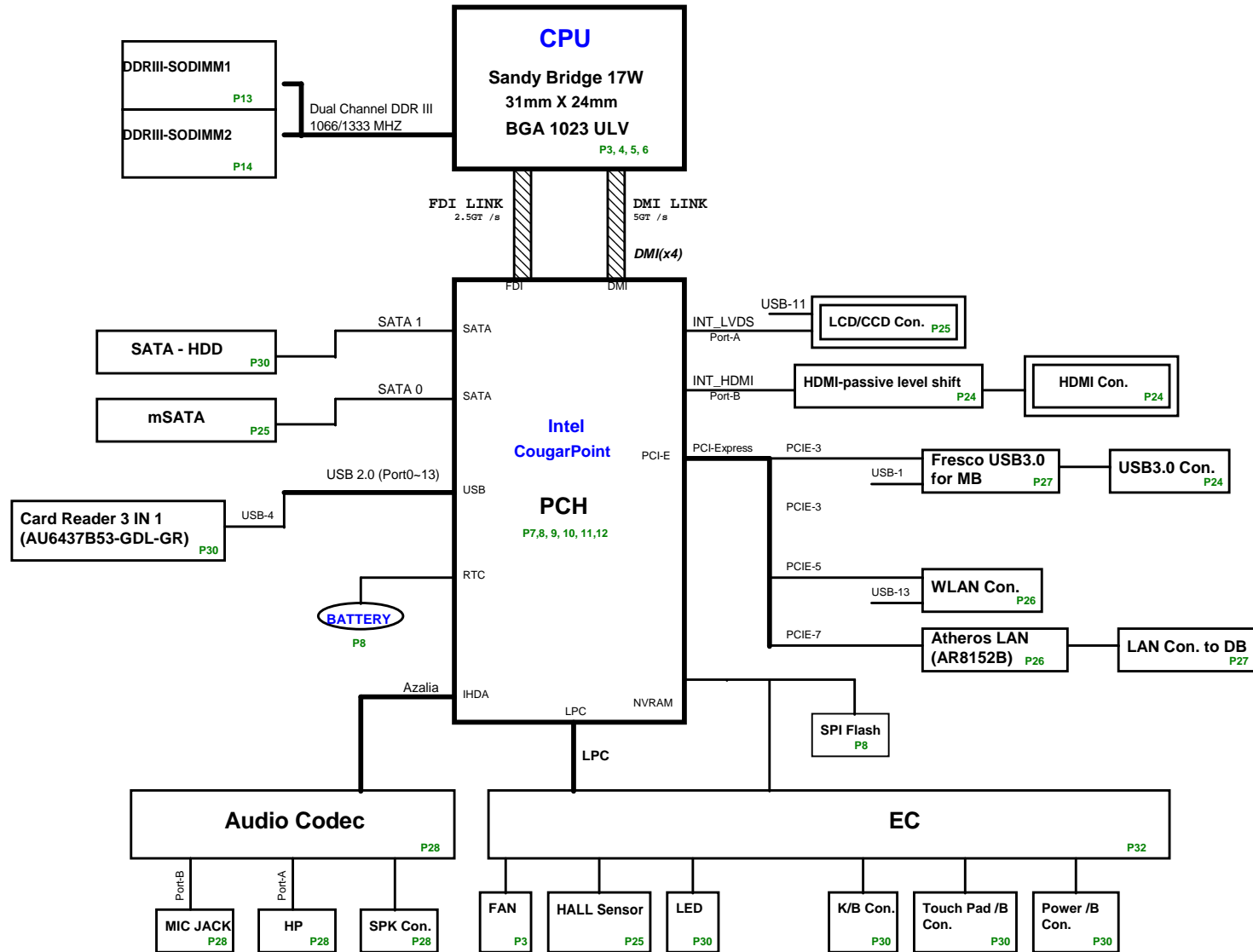


## PCB HDI Stackups

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : SGND  
 LAYER 5 : SVCC  
 LAYER 6 : IN2  
 LAYER 7 : GND  
 LAYER 8 : BOT



**POWER SYSTEM**

ISL88731CHRTZ-T	P33
TPS51123	P34
TPS51216RUKR	P35
OZ80116	P36
TPS51461RGER	P37
ISL95837HRZ-T	P38
G9661-25ADJF12U	P39

+VCC\_CORE

+1.5V  
+1.5VSUS+VTT  
+1.05V

+1.8V

+1.5V\_S5  
 +3VPCU  
 +3V\_S5  
 +3V  
 +5VPCU  
 +5V\_S5  
 +5V  
 +SMDDR\_VTERM  
 +SMDDR\_VREF  
 +VCCSA



Quanta Computer Inc.

PROJECT : BY1

Size Document Number  
Block Diagram

Date: Wednesday, November 09, 2011 Sheet 1 of 40 Rev 1A

Table of Contents

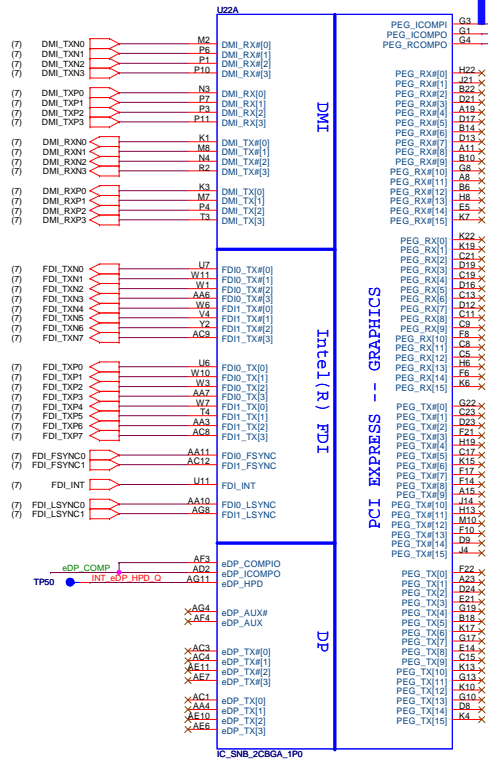
PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3-6	Processor	CPU
7-12	PCH	CLG
13-14	DDRIII SO-DIMM	DDR
15	S3 Power reduction	
16-23	Blank	Blank
24	HDMI	HDMI
25	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
	LVDS	LCD
	mSATA	SSD
26	Wireless Lan/BT	RF
27	USB 3.0	USB
28	Codec CX20671-21Z	ADO
29	Atheros LAN	LAN
30	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP connector	TPD
	Power Button	PB
	USB Board/HDD Connector	USB/HDD
31	Cut RTC Battery Power SW	SW
32	EC NPCE795LA0DX	EC
33	Charger (ISL88731C)	PWM
34	System 5V/3V Power	PWM
35	DDR Power	PWM
	+1.05VSUS	LDO
	+1.5V	LDO
36	+1.05V/VTT	PWM
37	+VCCAS	PWM
38	+VCC_Core	PWM
39	+1.8V	LDO
	Discharge(3V/5V/+1.5V)	LDO
40	EE Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V--+19V		S0-S5
+VCCRTC	+3.0V--+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V--+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

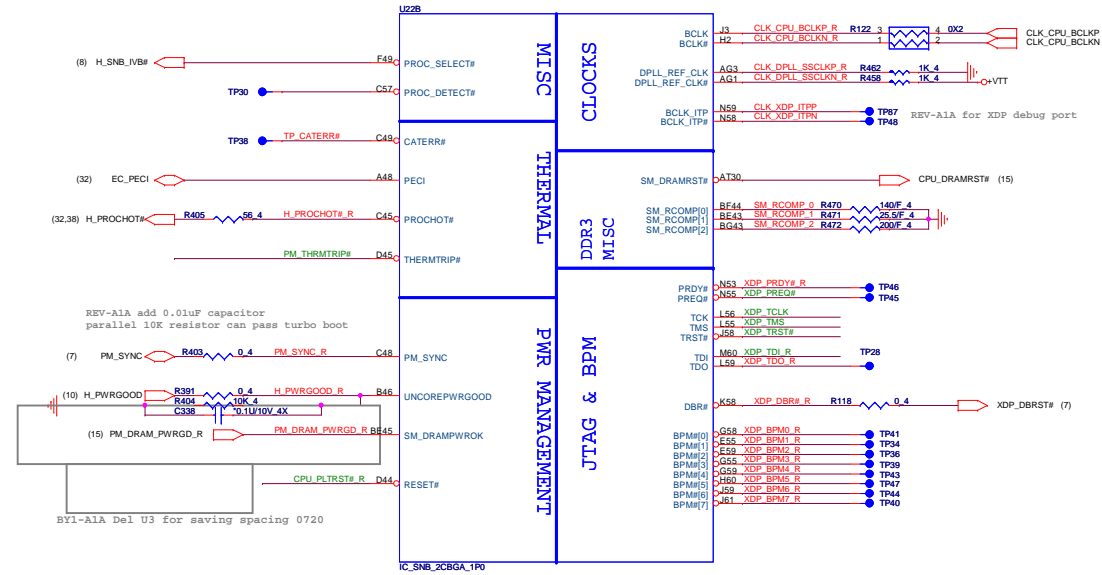
GND PLANE	PAGE
AGND_DC/DC	34
ADOGND	All
GND	28

ITEM	Value Code	FUNCTIONS
1	IVB@	Ivy Bridge
2	SNB@	Sandy Bridge
3	IV@	UMA
4	U3@	USB 3.0
5	IU3@	USB 2.0 and Chief River (colay W USB 3.0)
6	HM@	HDMI
7	IHM@	Internal HDMI
8	C@	Cost issue

## Sandy Bridge Processor (DM, PEG, FDI)


<http://laptopblue.vn/>

## Sandy Bridge Processor (CLK, MISC, JTAG)



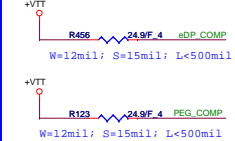
## FDI Disabling (Discrete Only)

&lt;CPU&gt;



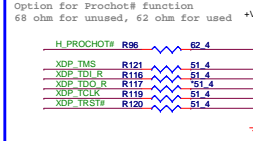
## DP &amp; PEG Compensation

&lt;CPU&gt;



## Processor pull-up &lt;CPU&gt;

&lt;CPU&gt;

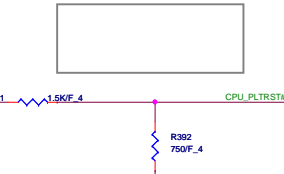


## Level Shift &lt;CPU&gt;

&lt;CPU&gt;

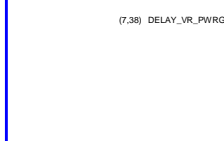


BY1-A1A Del U3 for saving spacing 0720



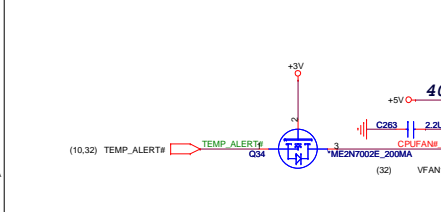
## Thermal Trip &lt;CPU&gt;

&lt;CPU&gt;



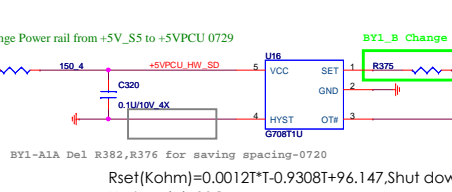
## FAN Control--&gt;For one FAN solution &lt;THC&gt;

&lt;THC&gt;

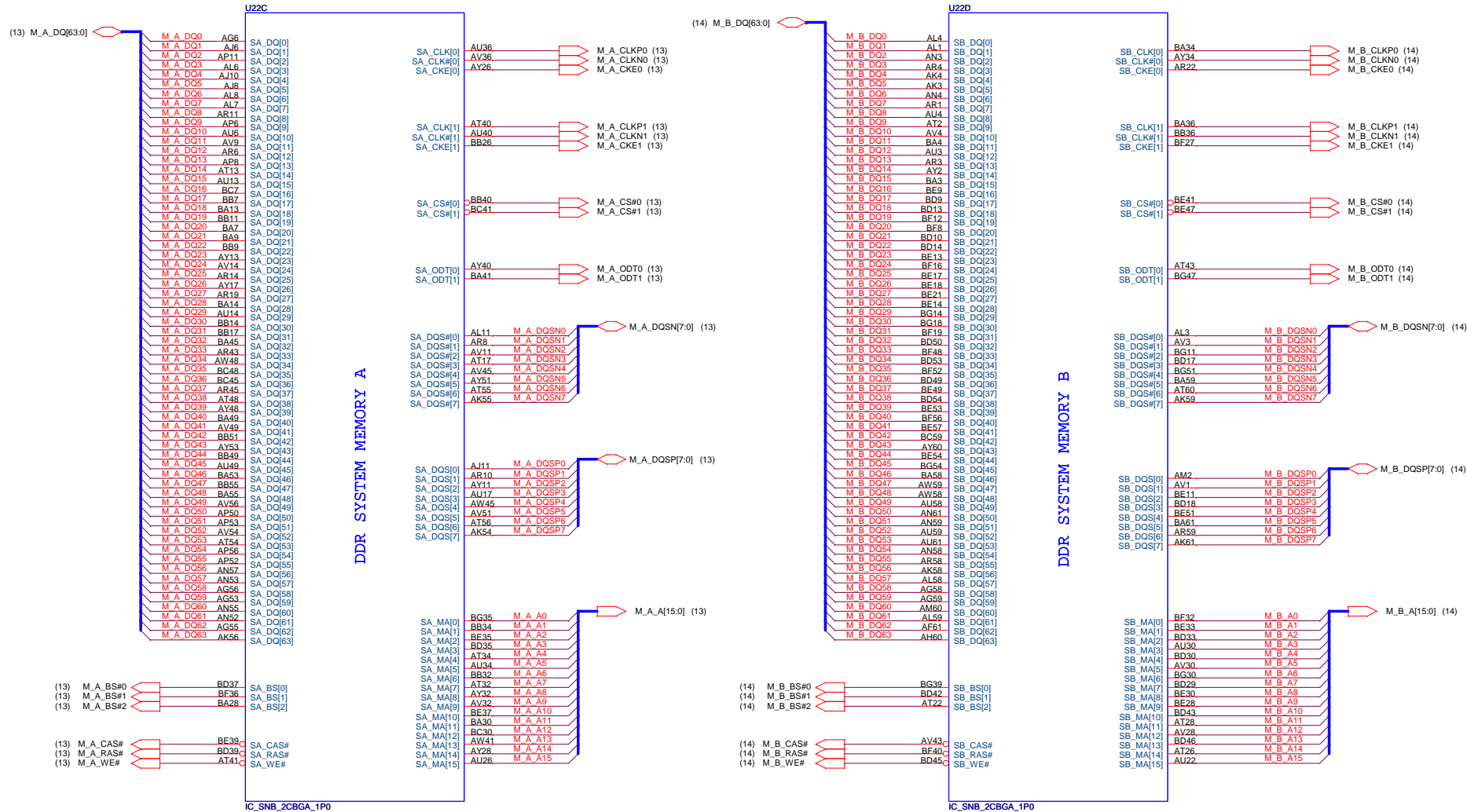


## CPU Thermal sensor / MB Local TEMP &lt;THC&gt;

&lt;THC&gt;

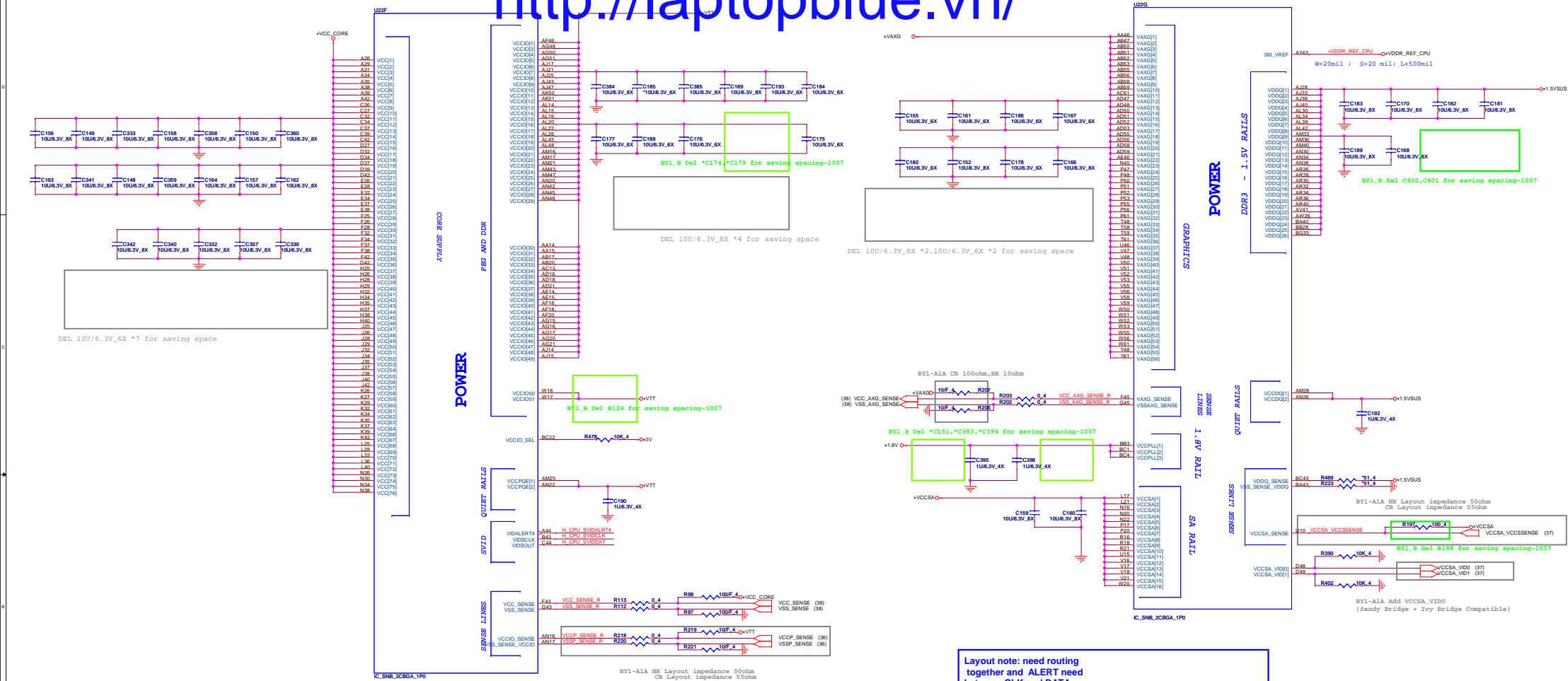


REV-C3A Change VCC PINS of U3 from +3VPCU to VL  
Add R496, R497, R499  
Reverse R14, R498, R31, R24, Q3

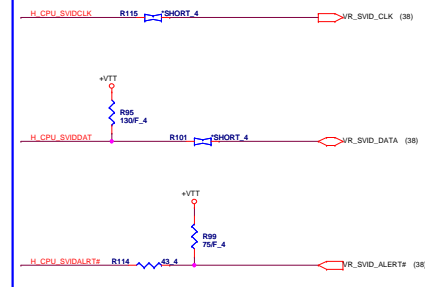


ssor (POWER)

<http://laptopblue.vn/>



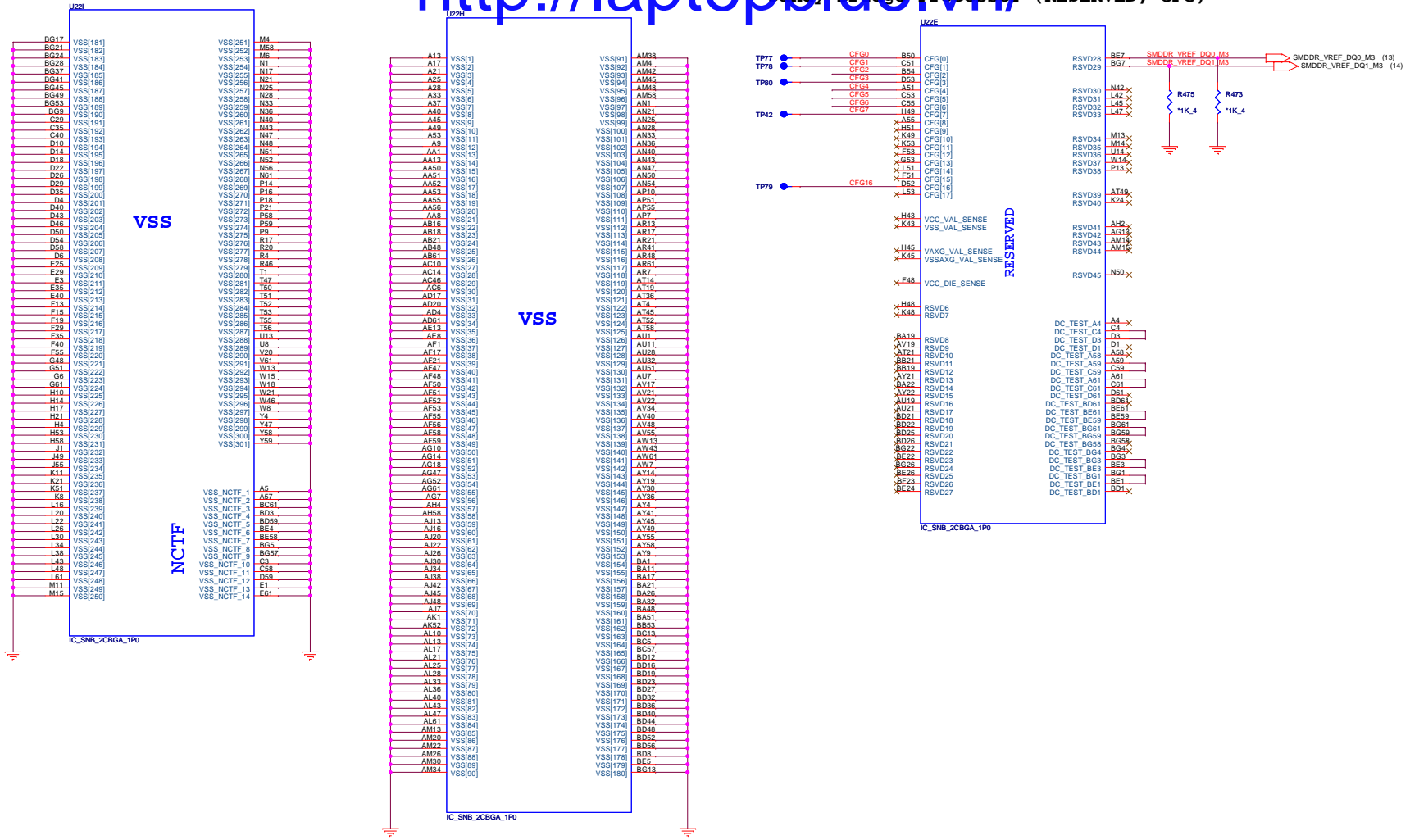
Layout note: need routing together and ALERT need between CLK and DATA



Sandy Bridge Processor (CPU)

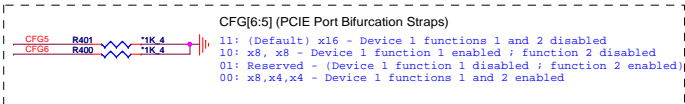
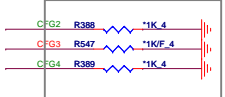
Sandy Bridge Processor (RESERVED, CFG)

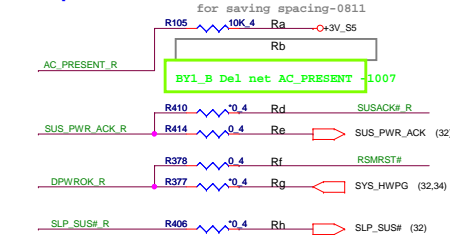
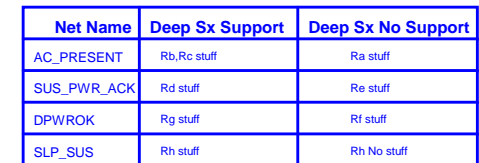
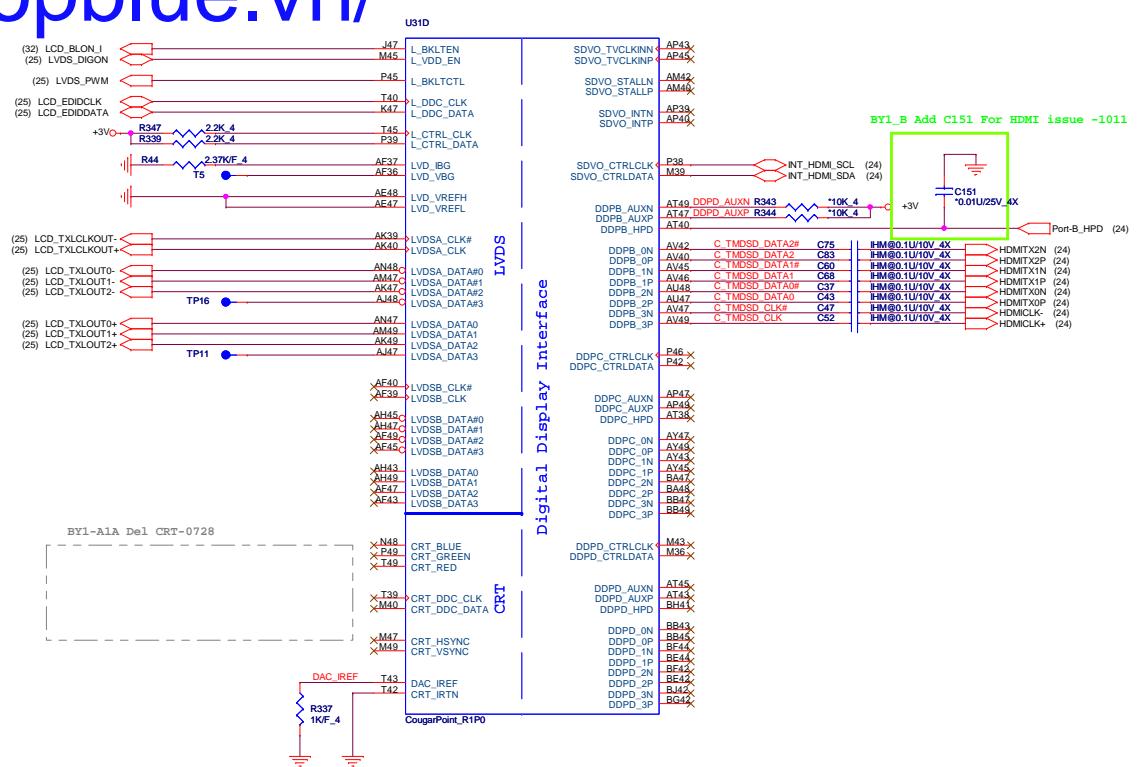
http://laptopblue.vn/



Processor Strapping

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



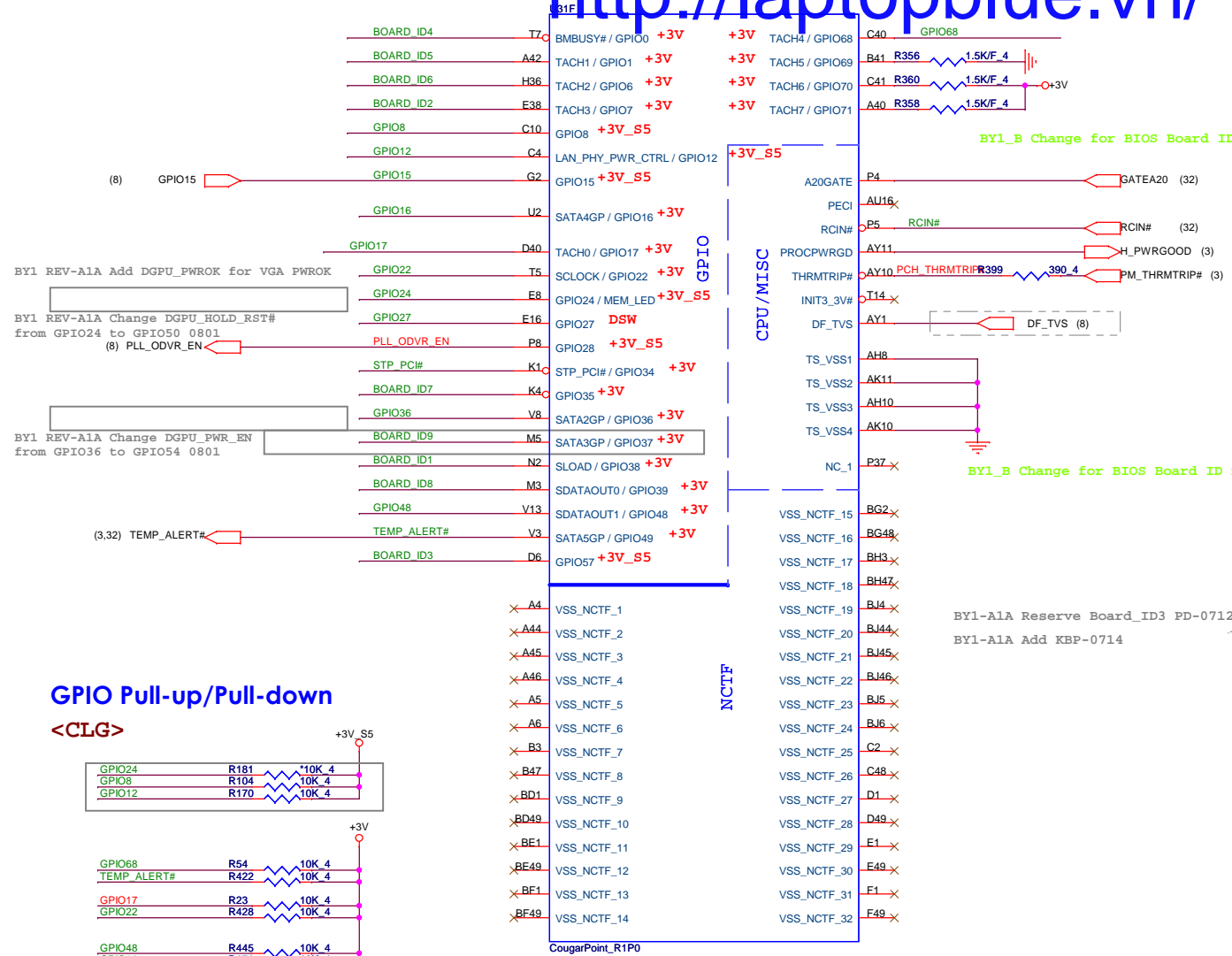




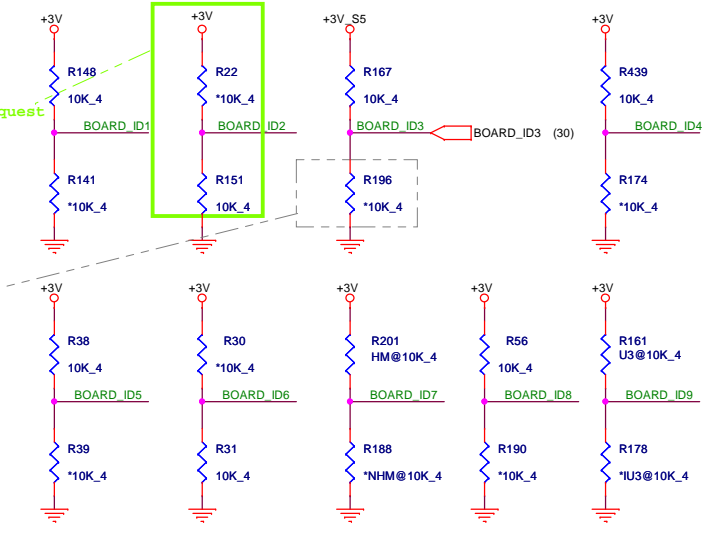









Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
BU6 SKU	H								
KZ1 SKU	L								
BY1D		H							
BY1		L							
W/O LED KB			H						
W/ LED KB			L						
Reserve				H					
Reserve					H				
W/O CCD						H			
W/ CCD					L				
W/ HDMI							H		
W/O HDMI							L		
BY1								H	
BU6 or KZ1								L	
W/ USB3.0									H
W/O USB3.0									L



BY1-A1A Del RAM Configuration Table-0811

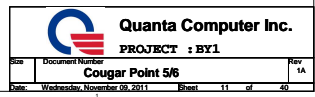


**Quanta Computer Inc.**  
PROJECT : BY1

Size	Document Number	Rev
	<b>Cougar Point 4/6</b>	1A
Date:	Wednesday, November 09, 2011	Sheet 10 of 40

COUGAR POINT (POWER)

BY1\_B Del R72,R75,R80 for saving spacing-1007

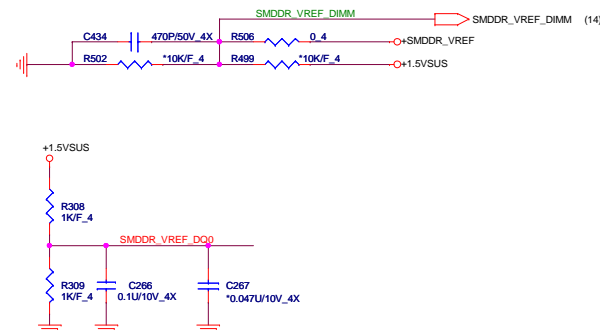
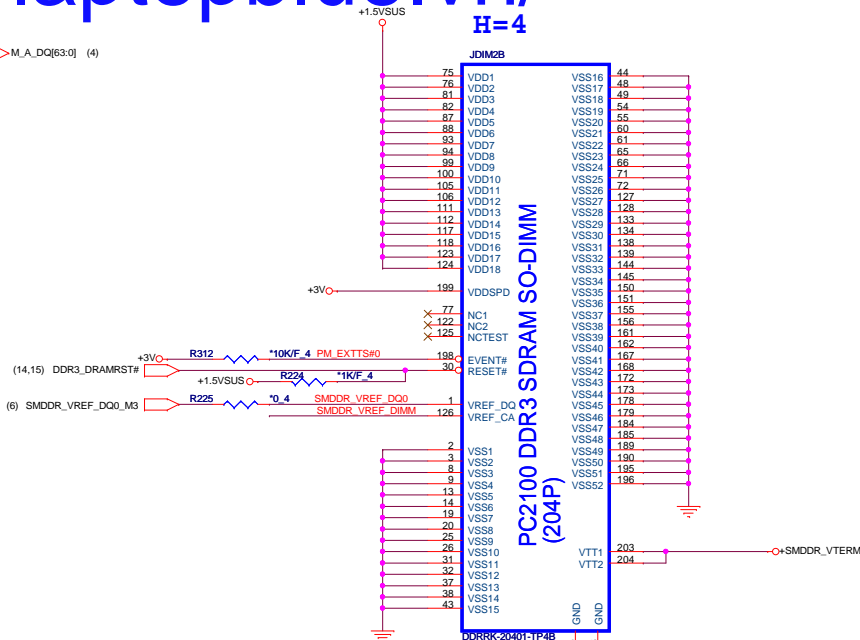




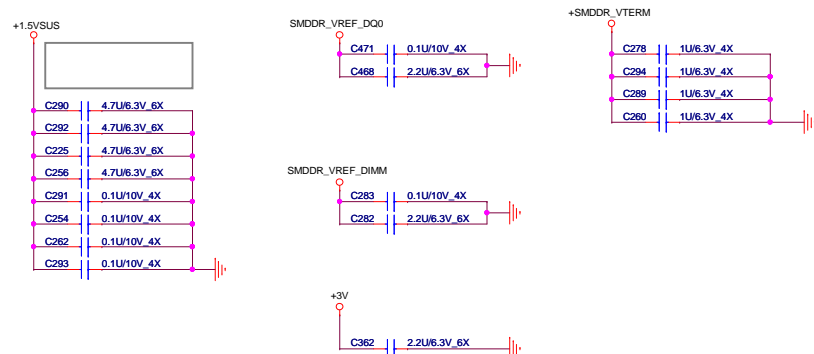
Quanta Computer Inc.

PROJECT :BY1

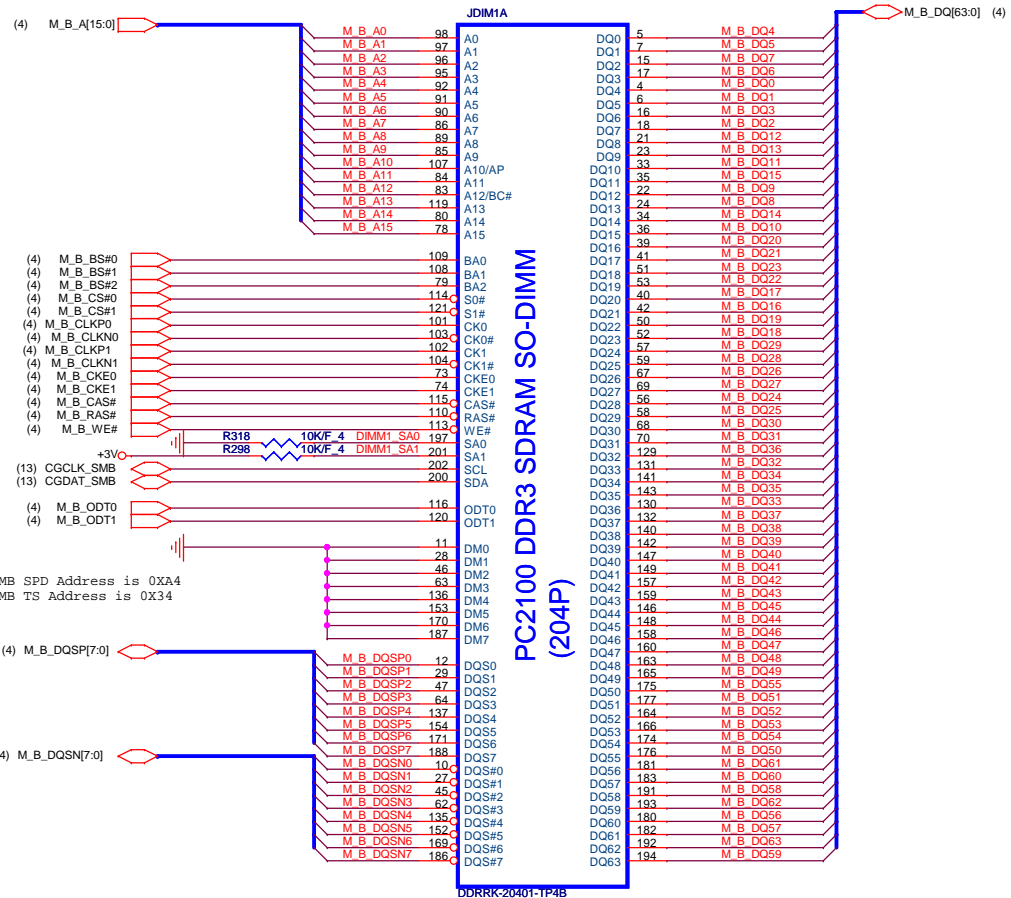
Size	Document Number	Rev
	Cougar Point 6/6	1A
Date:	Wednesday, November 09, 2011	Sheet 12 of 40



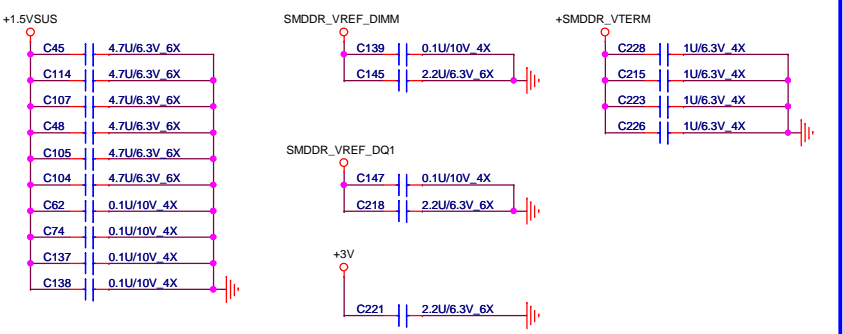
BY1 Del C218 and C255 for saving space 0720



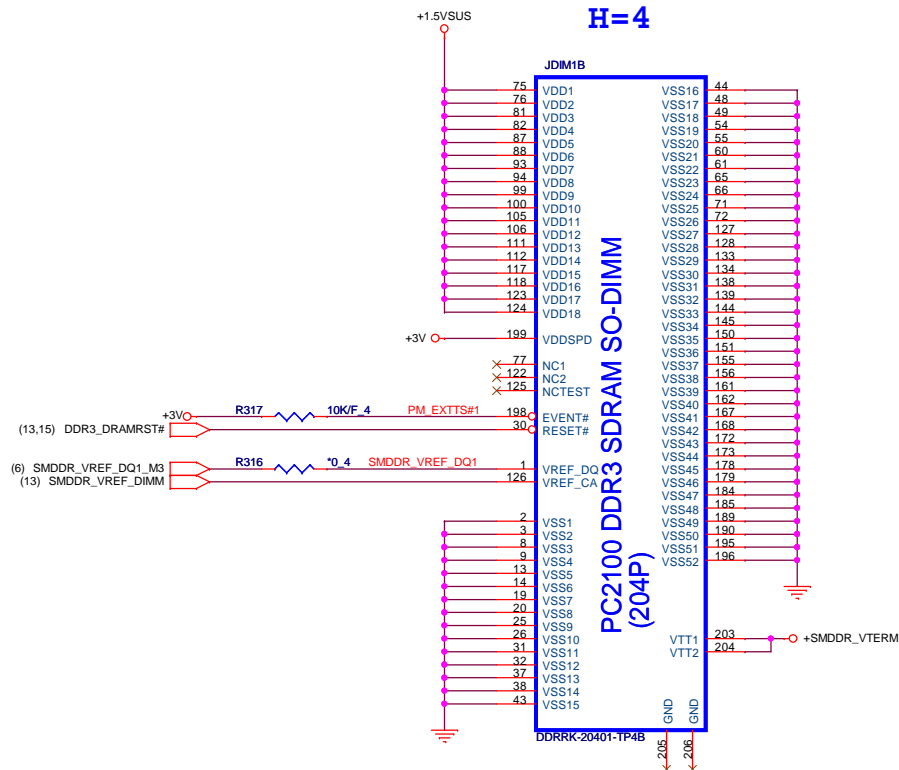
H=4



Place these Caps near So-Dimm1.

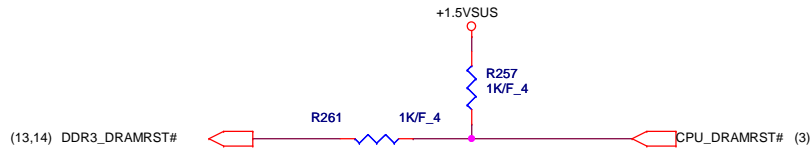


H=4



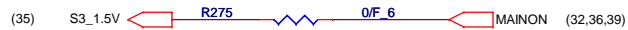
## S3 power Reduction (SM\_DRAMRST#) <S3P> <4>

BY1-A1A Del S3 power reduction-0714



## For S3 power Reduction Sequence <S3P> <3>

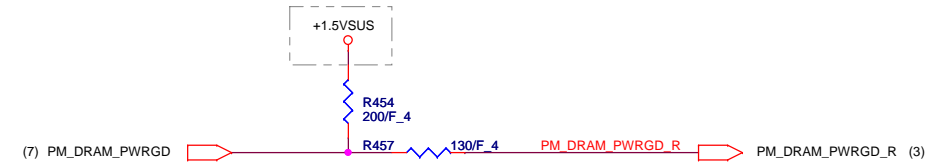
BY1-A1A Del S3 power reduction-0714



## For S3 power Reduction VTT discharge <S3P> <13>

## S3 power Reduction (SM\_DRAMPWROK) <S3P> <3>

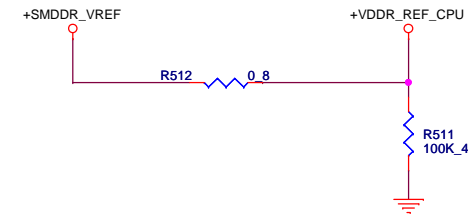
BY1-A1A Del S3 power reduction-0714



R454 external pull-up resistor  
close to the processor.  
A series-resistor of R457 is required between  
the pull-up resistor and the processor

## S3 power Reduction (CPU Power) <S3P> <5>

BY1-A1A Del S3 power reduction and change +1.5V\_CPU to +1.5VSUS 0714



Quanta Computer Inc.

PROJECT : BY1

Size	Document Number	Rev
	S3 power Reduction	1A
Date:	Wednesday, November 09, 2011	Sheet 15 of 40



<http://laptopblue.vn/>

BLANK



**Quanta Computer Inc.**

**PROJECT : BY1**

Size	Document Number	Rev
	<b>ROBSON_XT_PCIE_Interface</b>	<b>1A</b>
Date:	Wednesday, November 09, 2011	Sheet 16 of 40

<http://laptopblue.vn/>

16

BLANK



BLANK

<http://laptopblue.vn/>

21

BLANK

<http://laptopblue.vn/>

22

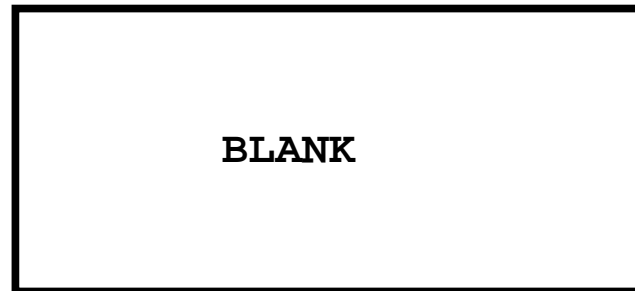
BLANK



**Quanta Computer Inc.**

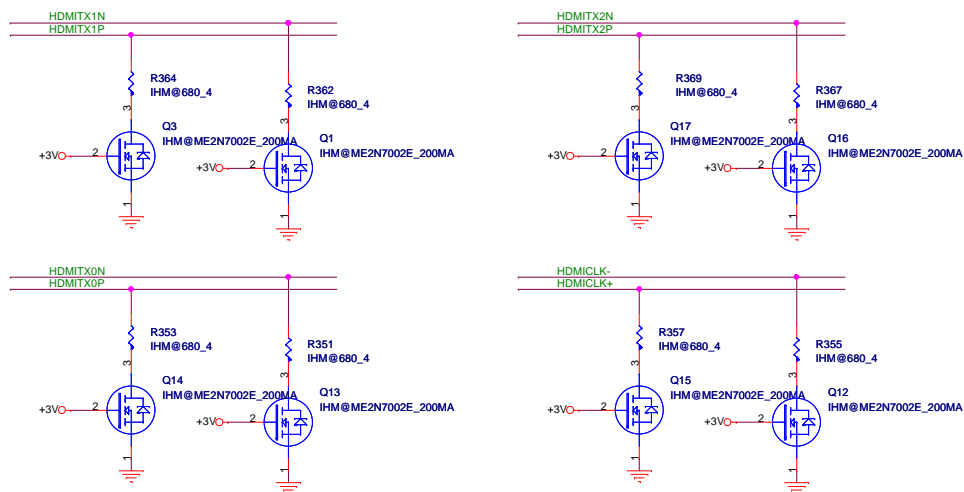
**PROJECT : BY1**

Size	Document Number	Rev
	<b>Seymour S3 VRAM(DDR3 BGA96)</b>	<b>1A</b>
Date:	Wednesday, November 09, 2011	Sheet 21 of 40



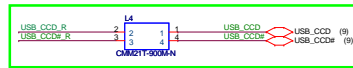






## CCD &lt;CCD&gt;

BY1\_C Change L4 footprint to choke-diplms900h12l-4p-1 -1102



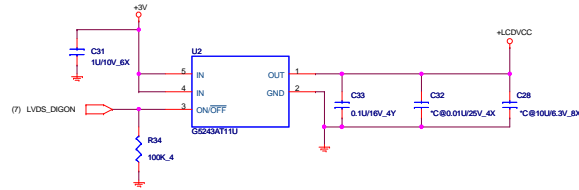
0.2A(20mils)

BY1-A1A Del 1000p-0817

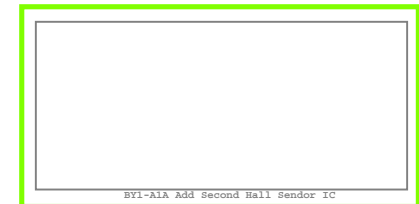
BY1\_B Del F1 1007

## LCD POWER SWITCH &lt;LDS&gt;

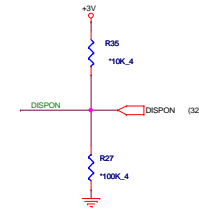
BY1-A1A Change U2 footprint from 6 pin to 5 pin and change 2nd source-0812



## HALL SENSOR&amp;BACK LIGHT SWITCH &lt;HSR&gt;

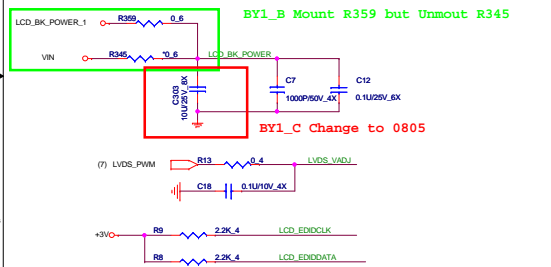


BY1\_B Del second hall sensor HRI,R300,C335 for save space -1006

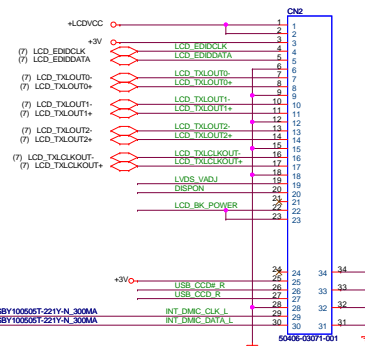


## LCD Panel Module &lt;LDS&gt;

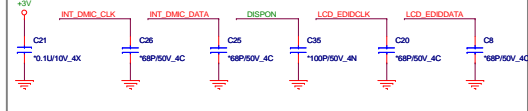
BY1\_B Mount R359 but Unmount R345



BY1\_C Change to 0805



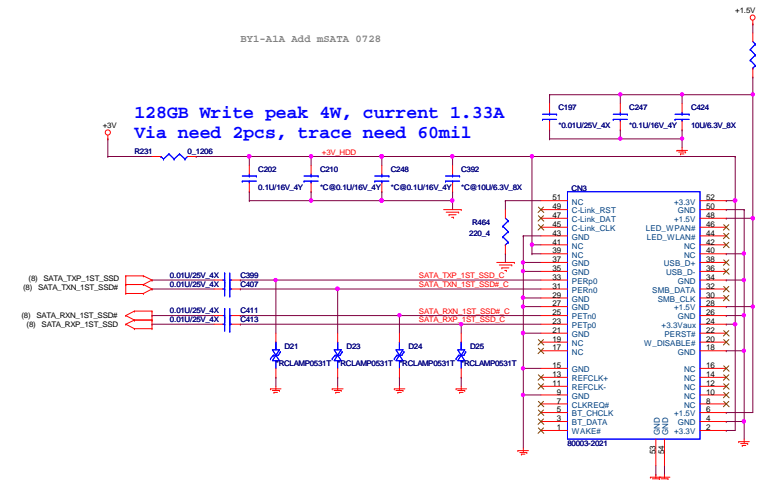
REV-A1A For EMI close to connector



## mSATA (SATA over mini PCIe)

&lt;H1D&gt;

BY1-A1A Add mSATA 0728

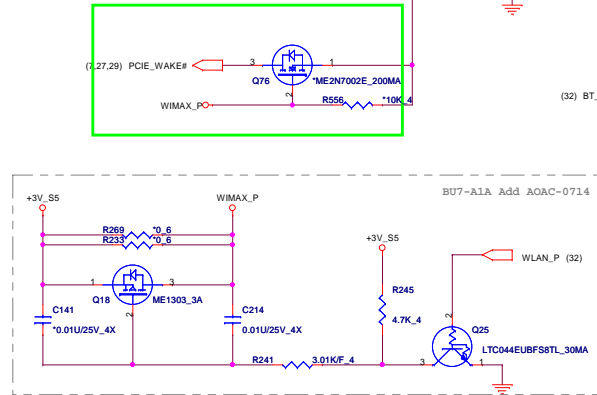
128GB Write peak 4W, current 1.33A  
Via need 2pcs, trace need 60mil

MINI Card Slot#1 <MNW>  
(WiFi)

Before RAMP must to remove  
debug card component

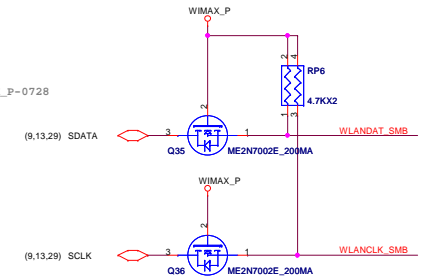
<http://laptopblue.vn/>

BY1\_C Disable Wire Lan wake up function 11/07

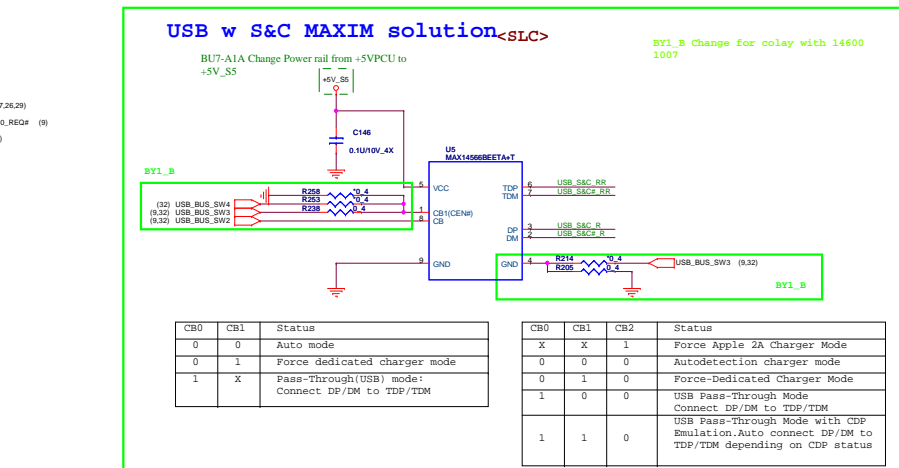
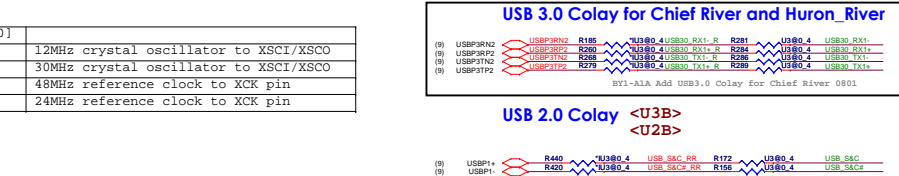
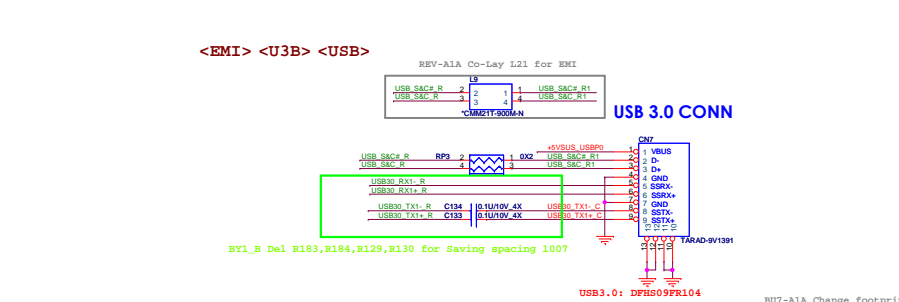
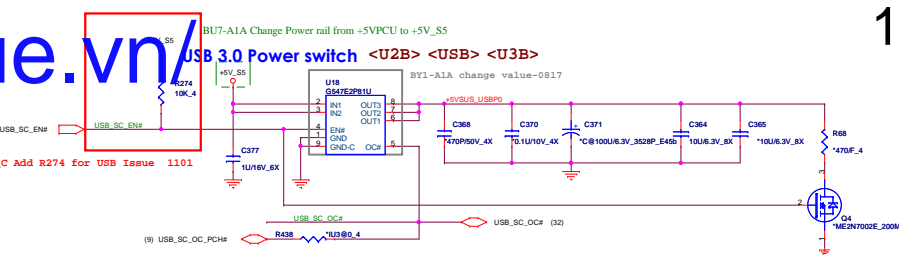
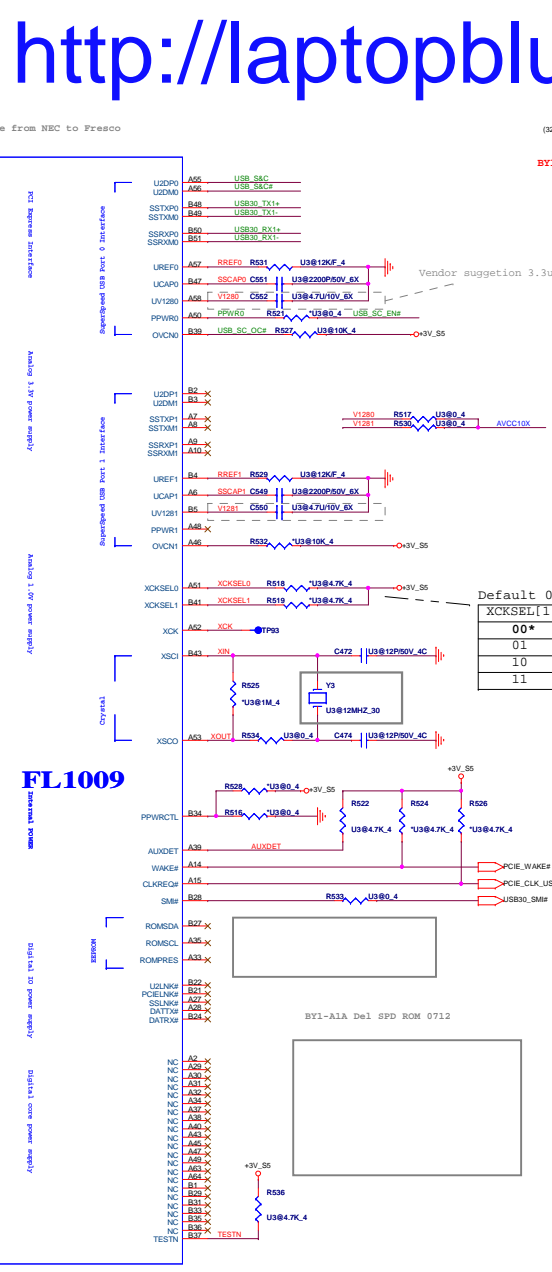
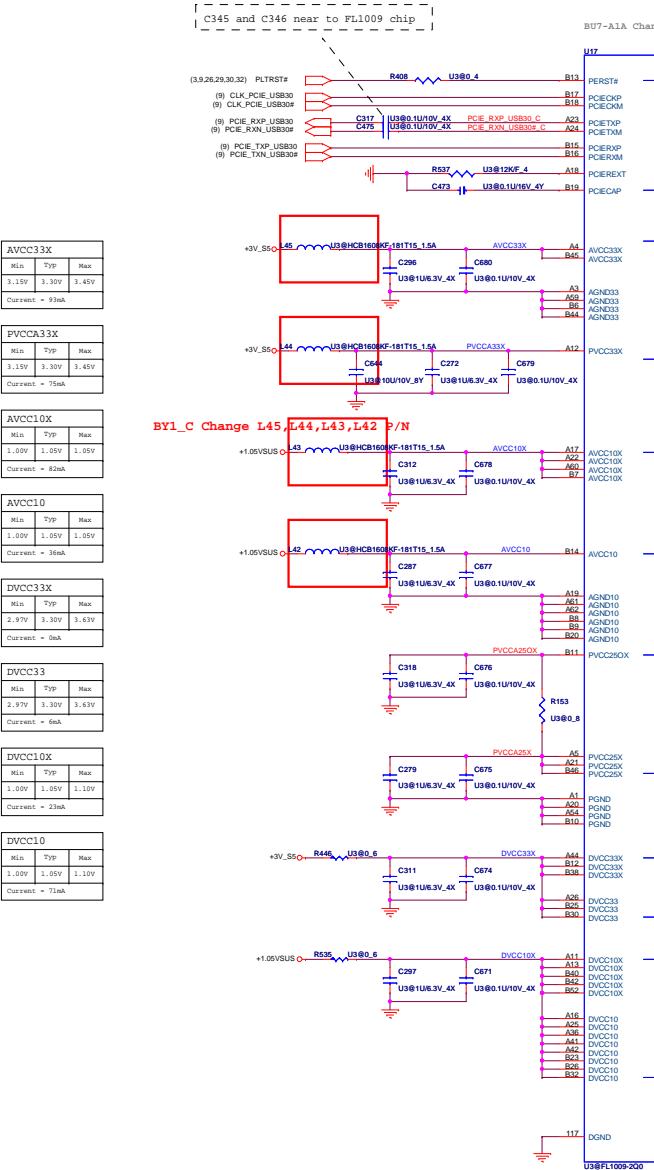


### SMBus(DDR3/WLAN/3G)

BY1-A1A Separate SMBUS level shift(WIMAX\_P)-0728



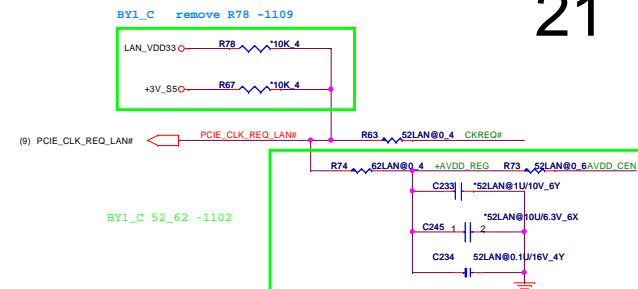
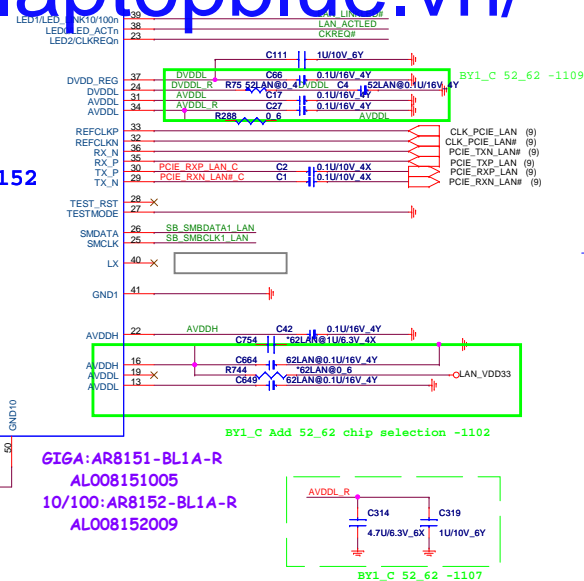
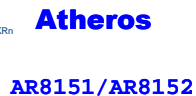
### USB 3.0 Controller <U3B>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

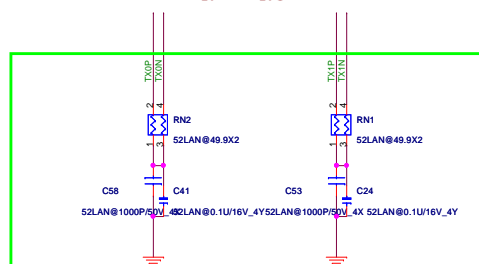
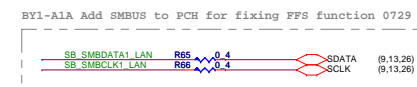
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation. Auto connect DP/DM to TDP/TDM depending on CDP status





| LAN-SM-Bus &lt;LAN&gt;

REV-A1A Because AR815x used PCIE protocol  
,so SMBus can reserve test point

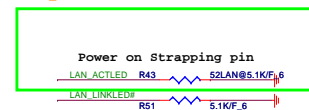


L  
A<LAN> <LNG>



R &lt;LAN&gt; &lt;LNG&gt; &lt;LN1&gt;

BY1\_C Remove R43 when mount AR8162-A -1107



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode



**Quanta Computer Inc.**

PROJECT : BY1

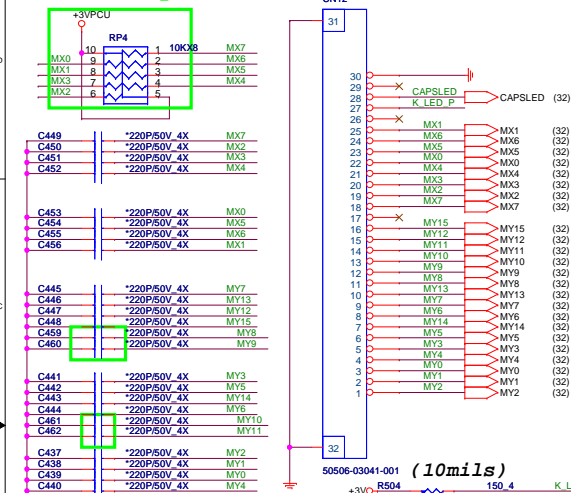
Size	Document Number	Rev
	<b>Atheros LAN (AR8151B/52B)</b>	<b>1A</b>
Date:	Wednesday, November 09, 2011	Sheet 29 of 40

Date: Wednesday, November 09, 2011 Sheet 29 of 40



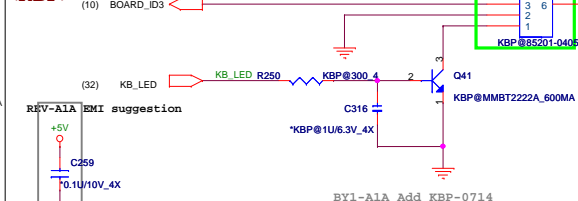
## INT KeyBoard &lt;KBC&gt; &lt;EMI&gt;

BU7-A1A Change to 30pin connector  
BY1-A1A NC-0817BY1\_C Add PU 10k for KB CN16... -1102



## K/B LED power

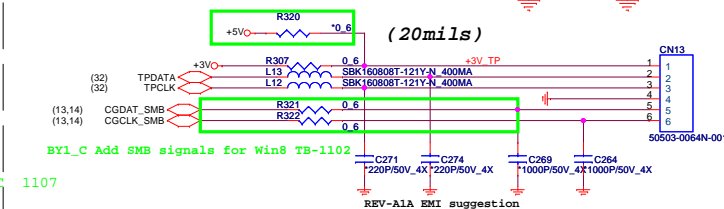
<KBP> +5VDC 0.35A (20mils)



## TP board &lt;TPD&gt; &lt;EMI&gt;

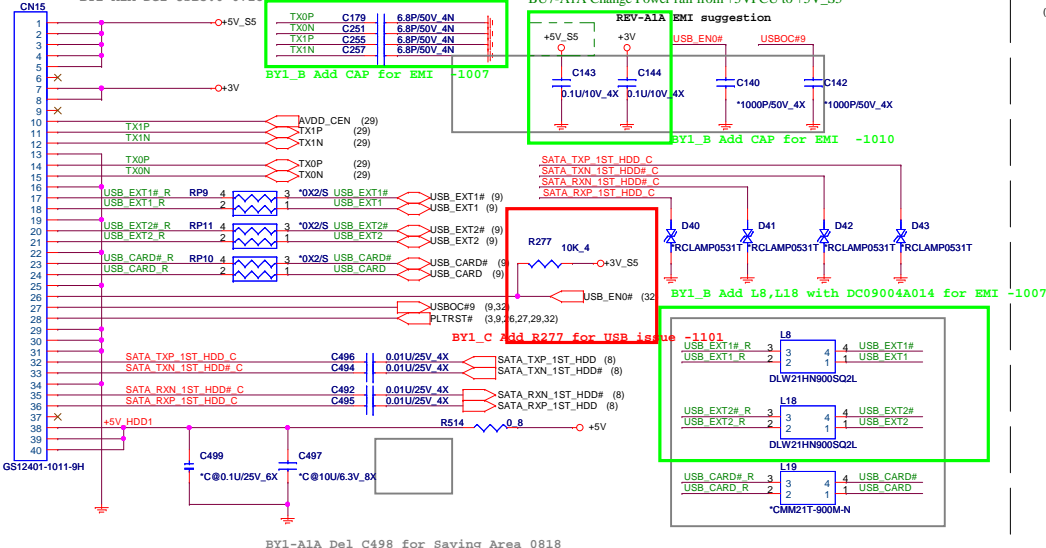
<http://laptopblue.vn/>

BY1\_C Add +5V for Win8 TB-1102



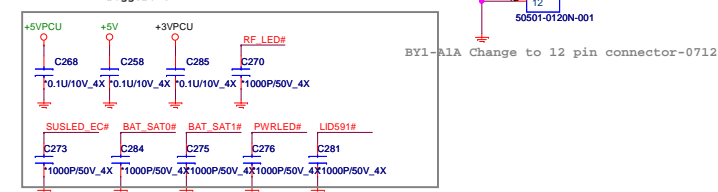
## LAN&amp;USB&amp;Cardreader &amp; HDD Interface &lt;U3B&gt; &lt;MMC&gt; &lt;EMI&gt; &lt;H1D&gt; &lt;LAN&gt;

BY1-A1A Del USB3.0 0728

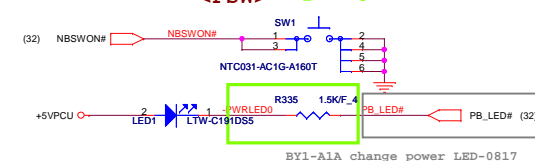


## LED &lt;LED&gt;

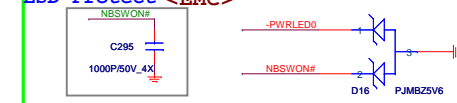
REV-A1A EMI suggestion



## Power Button &lt;PSW&gt; BY1\_B Change R335 from 150 to 1.5k



## ESD Protect &lt;EMC&gt;

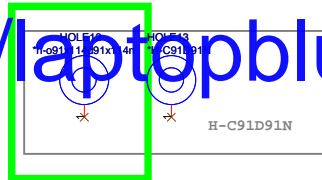
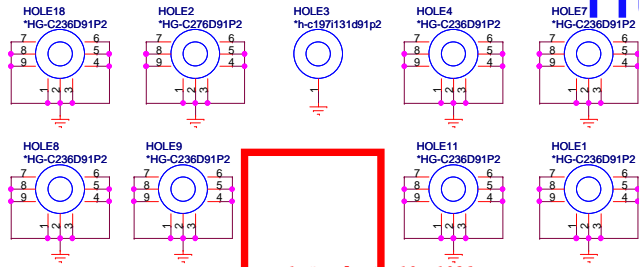


HOLE &lt;OTH&gt;

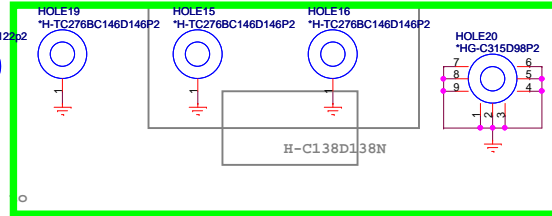
<http://laptopblue.vn/>

BY1\_B HOLE 20 Footprint

1012



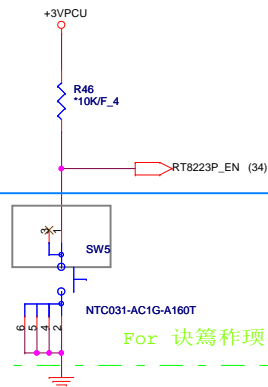
BY1\_B HOLE 12 change footprint to h-o91x114d91x114n

BY1\_C Del HOLE10 1026  
BY1\_B Change HOLE1,HOLE4,HOLE7,HOLE8,HOLE9,HOLE10,HOLE11,HOLE18 Footprint 1011hole 14 change footprint to  
h-c236d122p2  
Jerry 0902

BY1\_B HOLE 14,HOLE 15,HOLE19,HOLE16 to ground for EMI 1007

hole 17 footprint change to H-C236D142P2  
Jerry 0902BU7-A1A Add cut battery power circuit-0725  
BU7-A1A Del cut battery power circuit from HW solution, change to only control from ME solution-0727

BU7-A1A Modify cut battery power circuit-0729



BY1-A1A Modify SW5 PIN 3 to NC for fixing Layout issue 0819

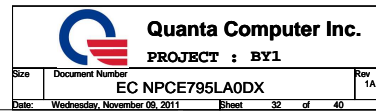
For EE&amp;SW solution



Quanta Computer Inc.

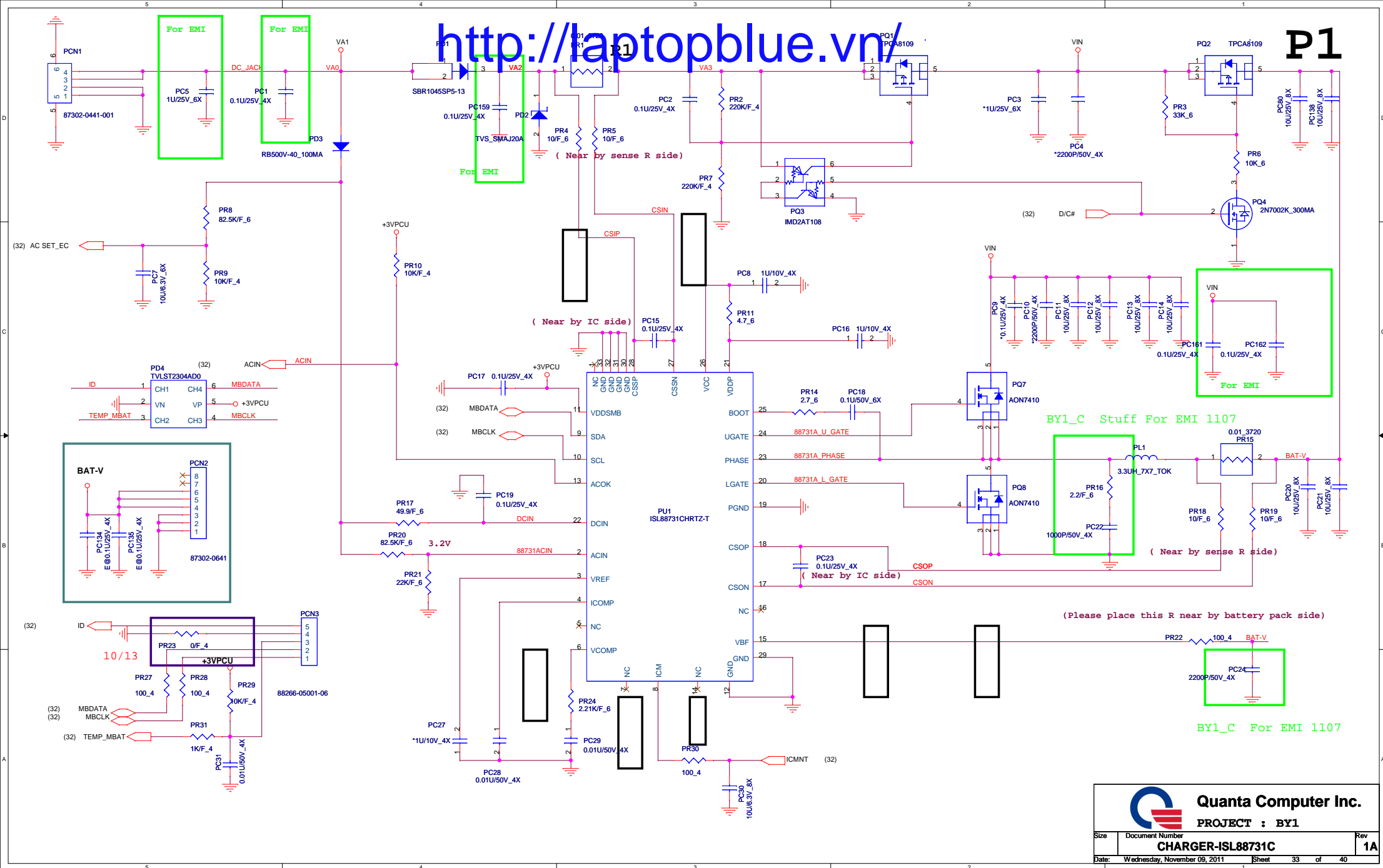
PROJECT : BY1

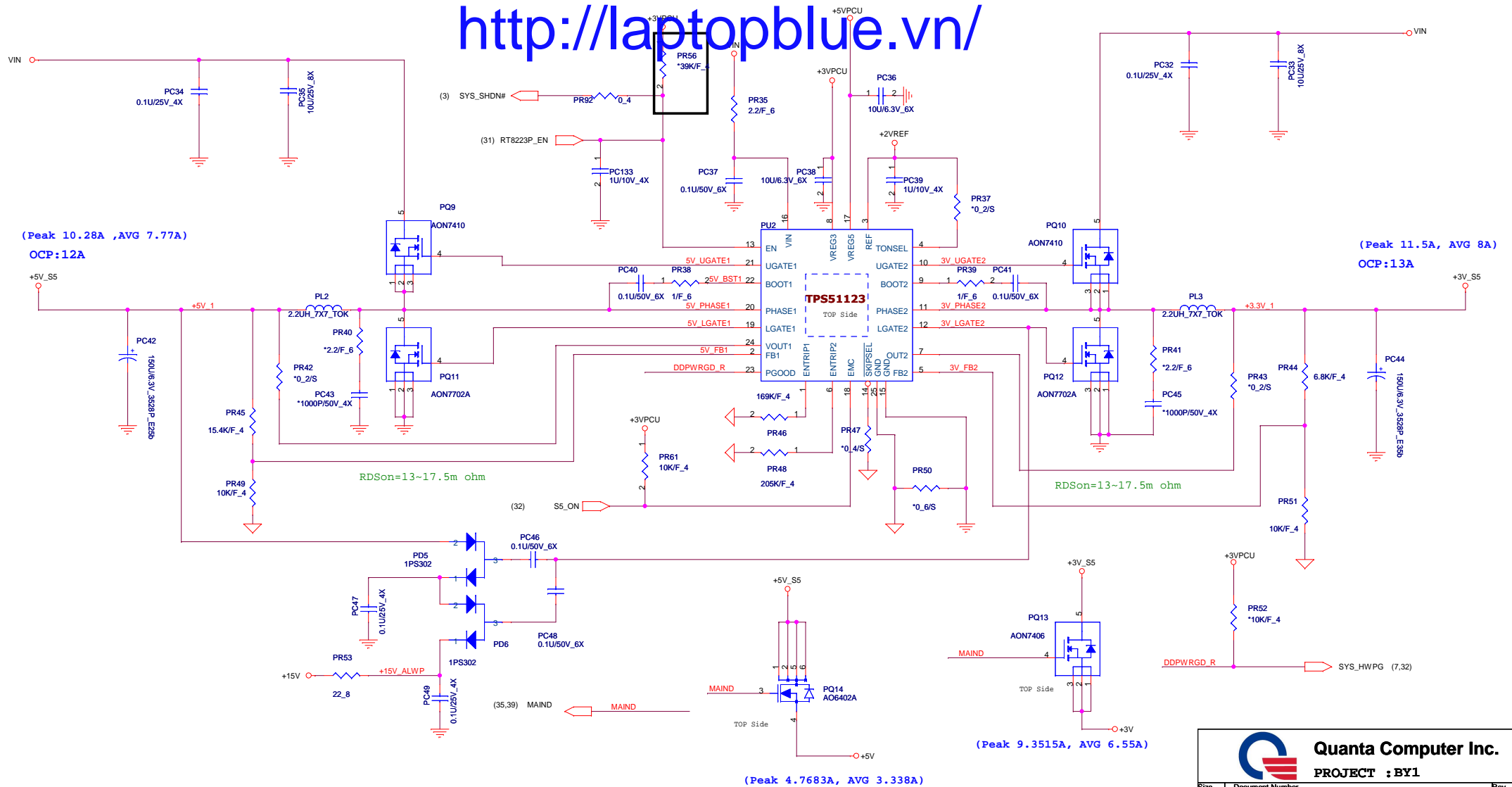
Size	Document Number	Rev
	CUT BAT Control/HOLE	1A
Date:	Wednesday, November 08, 2011	Sheet 31 of 40

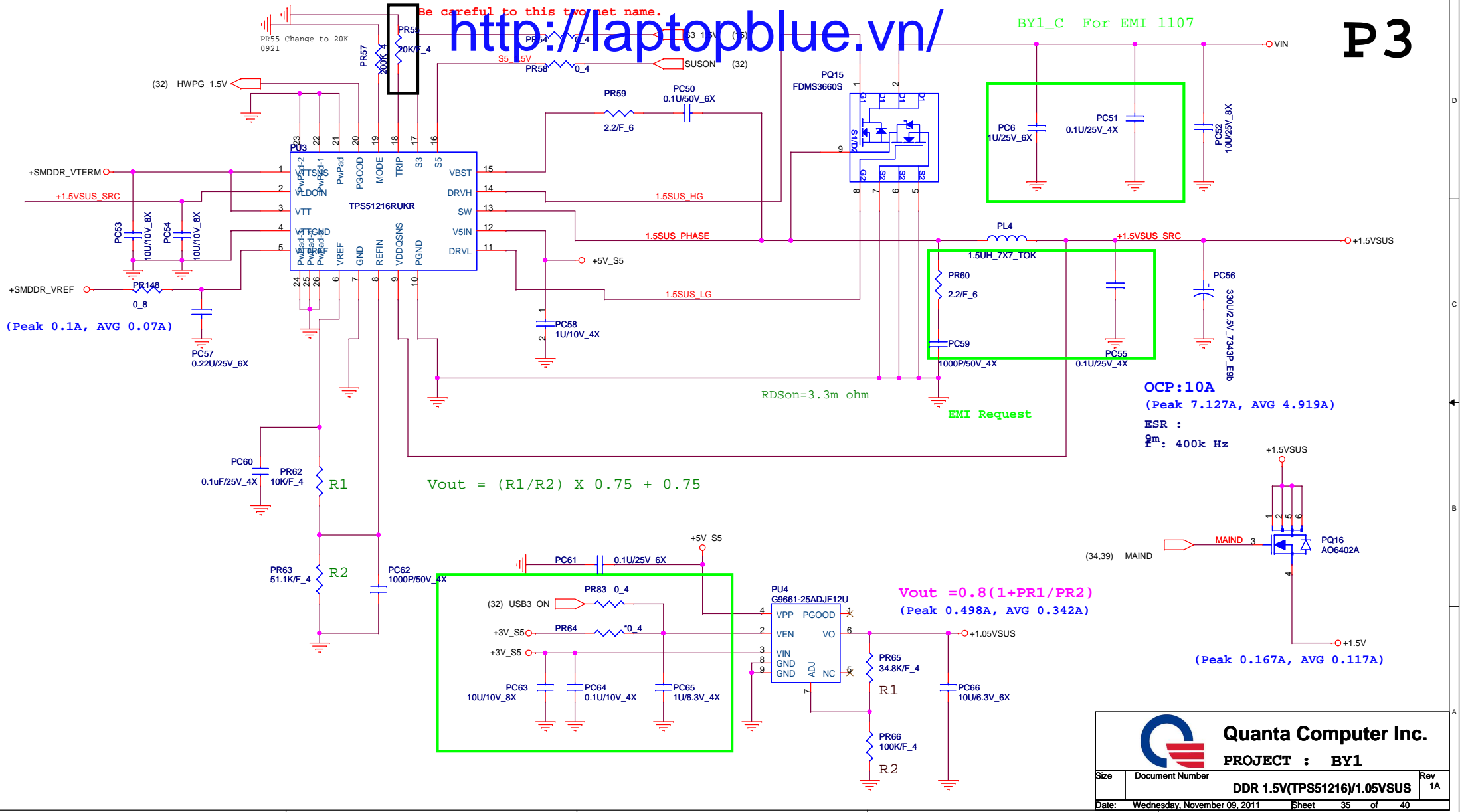


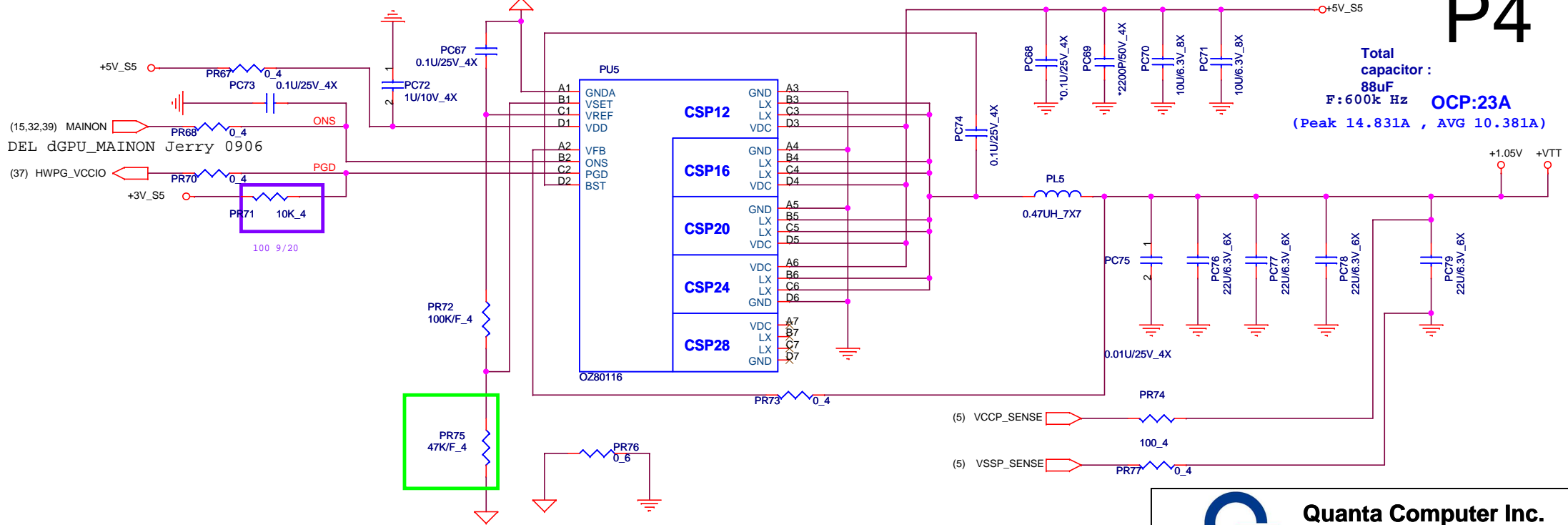
<http://laptopblue.vn/>

P1





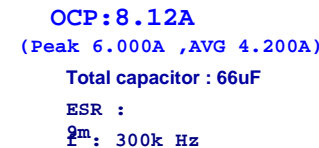




Quanta Computer Inc.

PROJECT : BY1

Size	Document Number	Rev
	VTT/1.05V(OZ80116)	1A
Date:	Wednesday, November 09, 2011	Sheet 36 of 40



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	*0.8V
0	1	*0.85V
1	0	0.725V
1	1	0.675V

\*0.8V FOR SV TYPE  
\*0.85V FOR LV/ULV TYPE



Date: Wednesday, November 09, 2011 Sheet 38 of 40

(Peak 1.24A, AVG 0.869A)

$$V_{out} = 0.8(1 + R1/R2)$$

f : 640k Hz  
(Peak 0.5A , AVG 0.2A) OCP: 2A

10/13

<http://laptopblue.vn/>

```

PAGE 31: HOLE 12 change footprint to h-ø91x114d91x114n for DXF
PAGE 25: BY1_B Del second hall sensor MR1,R300,C335 for Save space
PAGE 26: Change CN5 P/N to DFHD52MR047 for DXF
PAGE 27: Add R258,R253,R238,R214,R205 for colay with 14600
PAGE 10: Unmount R22,Mount R151 for BIOS Board ID request
PAGE 30: Change R335 from 150 to 1.5K
PAGE 32: BY1_B Add USB_BUS_SW4 -1007
PAGE 32: BY1_B Add LAN_P -1007
PAGE 32: BY1_B Add USB_BUS_SW4 -1007
PAGE 32: BY1_B Add R272
PAGE 32: BY1_B Add USB3_ON -1007
PAGE 32: BY1_B DEL AC_PRESENT -1007
PAGE 31: BY1_B HOLE 12 change footprint to h-ø91x114d91x114n
PAGE 31: BY1_B HOLE 15,HOLE19,HOLE16 to ground for EMI 1007
PAGE 30: BY1_B Change R335 from 150 to 1.5K
PAGE 30: BY1_B Add L8,L18 with DC09004A014 for EMI -1007
PAGE 30: BY1_B Add CAP for EMI -1007
PAGE 30: BY1_B Add CAP for EMI -1010
PAGE 29: BY1_B Add LAN power control circuit -1007
PAGE 29: BY1_B Del R448 -1007
PAGE 29: BY1_B Add R72 and remove R67 -1007
PAGE 28: BY1_B Mount C199,C224,C378 with 0ohm for EMI -1007
PAGE 27: BY1_B Change for colay with 14600 1007
PAGE 27: BY1_B Del R183,R184,R129,R130 for Saving spacing 1007
PAGE 25: BY1_B Del second hall sensor MR1,R300,C335 for save space -1006
PAGE 25: BY1_B Mount R359 but Unmount R345
PAGE 25: BY1_B Del F1 1007
PAGE 25: BY1_B Unmount C23 1007
PAGE 25: BY1_B EMI Request 1010
PAGE 11: BY1_B Del R36,R79,R86,R380,R137,L17,R349,R350,R85,R354,R2,R126,L20,C319,R74,R76,R146,L26,C374,R147,R110,R64,R88,R72,R75,R80,R384,R24,R25,R73,C89,R103,R29,R316,C306,C314 for saving spacing-1007
PAGE 11: BY1_B Change for BIOS Board ID request
PAGE 8: BY1_B Change for PCH Dual SPI
PAGE 8: BY1_B Del for saving spacing-1007
PAGE 7: BY1_B Del net AC_PRESENT -1007
PAGE 5: BY1_B Del R198,C174,C179,R124,C151,C393,C394,C400,C401 for saving spacing-1007
PAGE 31: BY1_B Change HOLE1,HOLE4,HOLE7,HOLE8,HOLE9,HOLE10,HOLE11,HOLE18 Footprint 1011
PAGE 7: BY1_B Add C151 For HDMI issue -1011
PAGE 3: BY1_B Change R357 from 24.9k to 25.5k -1013
PAGE 35: BY1_B Umount PR64 ,Mount PR83

```

PAGE 31: BY1 C Del HOLE10 1026  
PAGE 30: BY1 C Add R277 for USB issue -1101  
PAGE 28: BY1 C C420 Change to 0603 1101  
PAGE 27: BY1 C Change L45,L44,L43,L42 P/N  
PAGE 27: BY1 C Add R274 for USB Issue 1101  
PAGE 25: BY1 C Change to 0805

MODEL	PAGE	FROM	To
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		
	15		
	16		
	17		
	18		
	19		
	20		
	21		
	22		
	23		
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
	32		
	33		
	34		
	35		
	36		
	37		
	38		
	39		
	40		