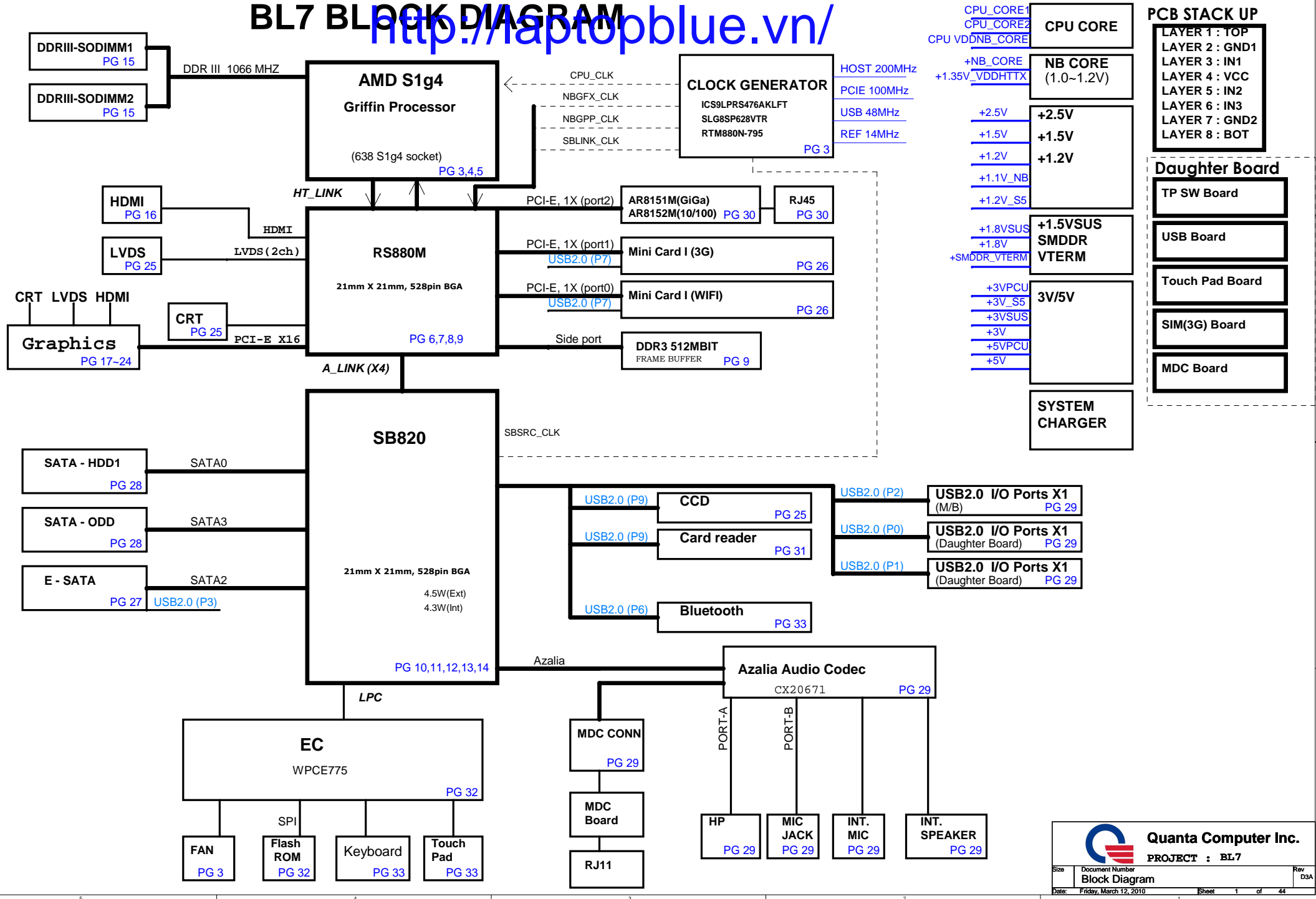


BL7 BLOCK DIAGRAM

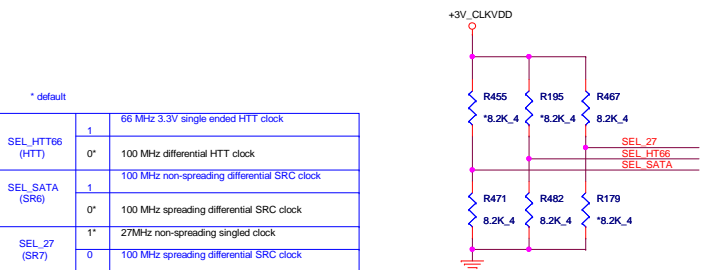
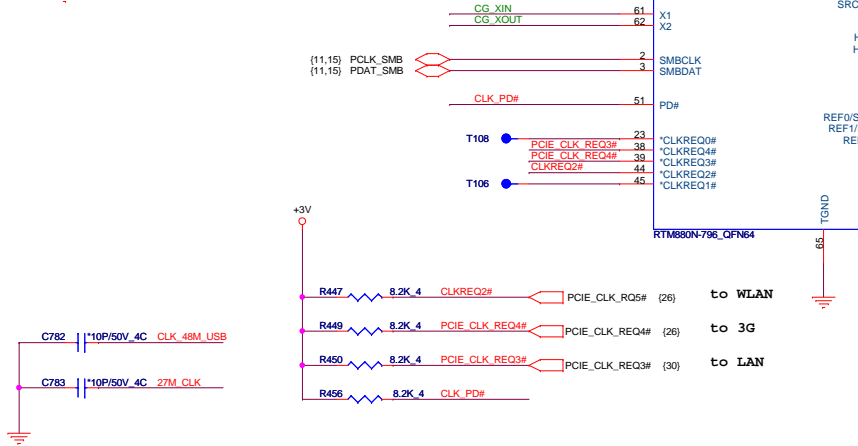
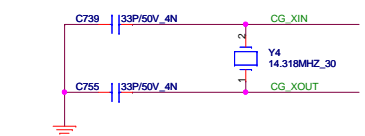
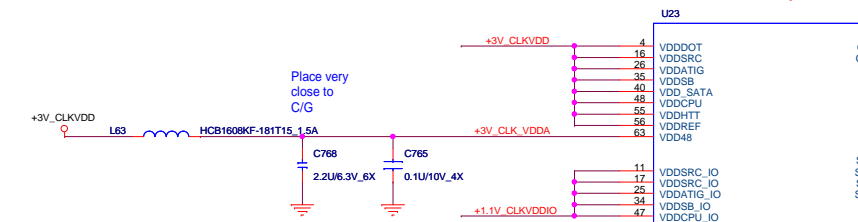
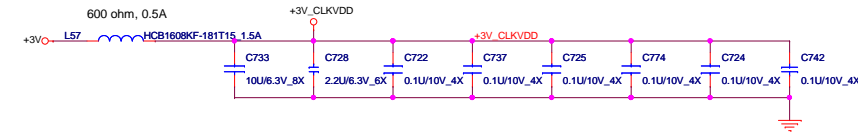
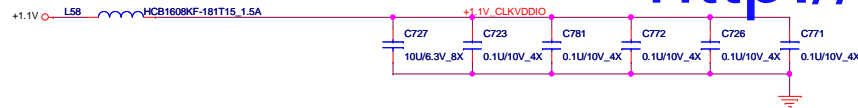
<http://laptopblue.vn/>



CLOCK GENERATOR

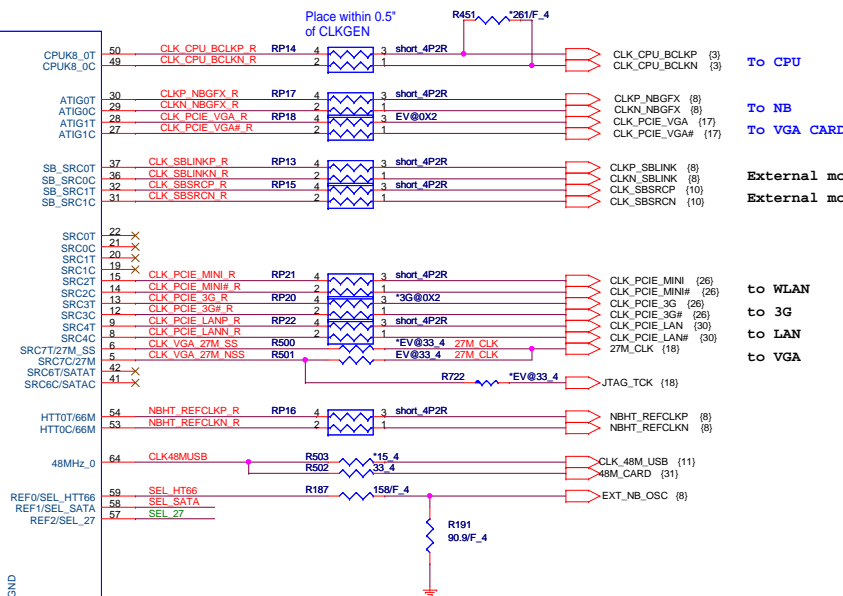
http://laptopblue.vn/

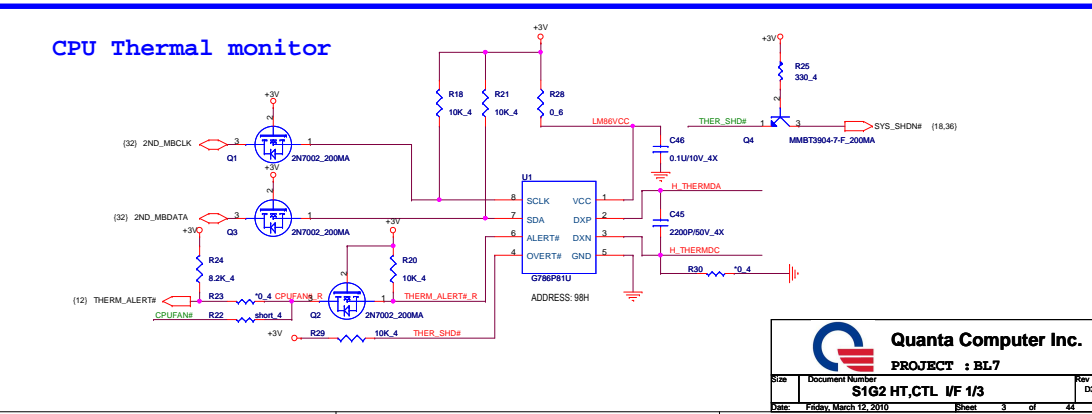
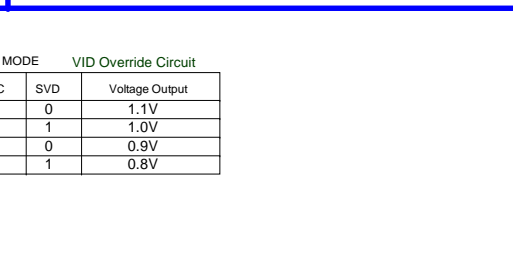
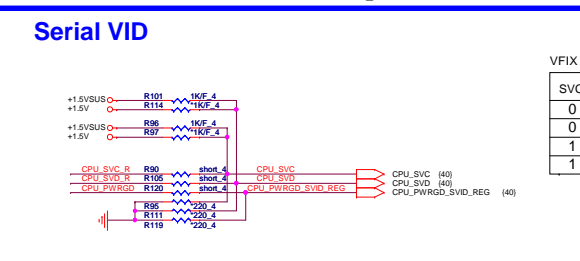
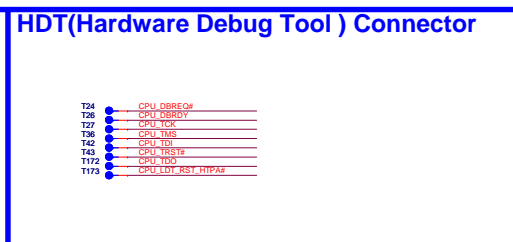
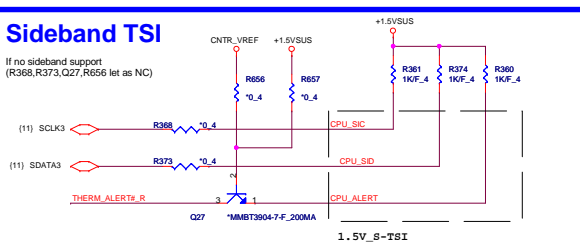
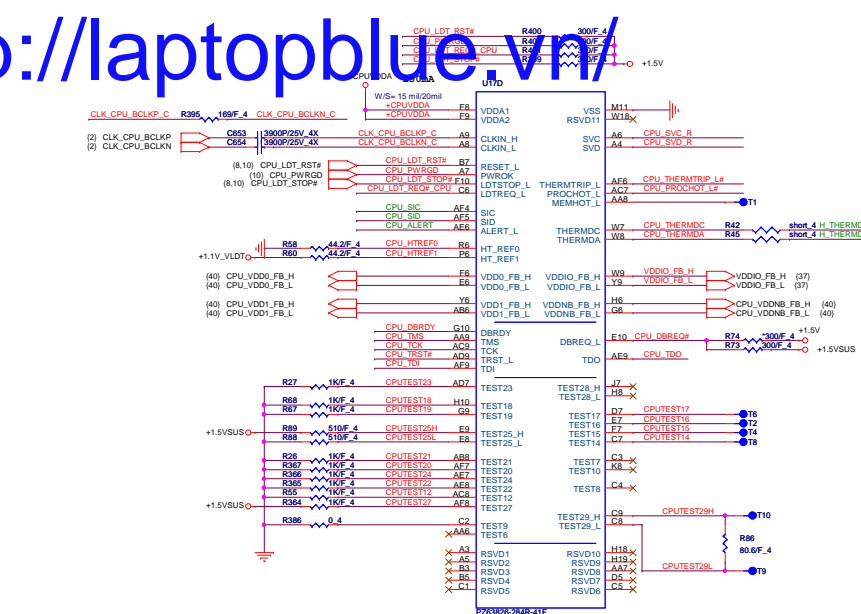
02

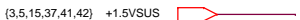


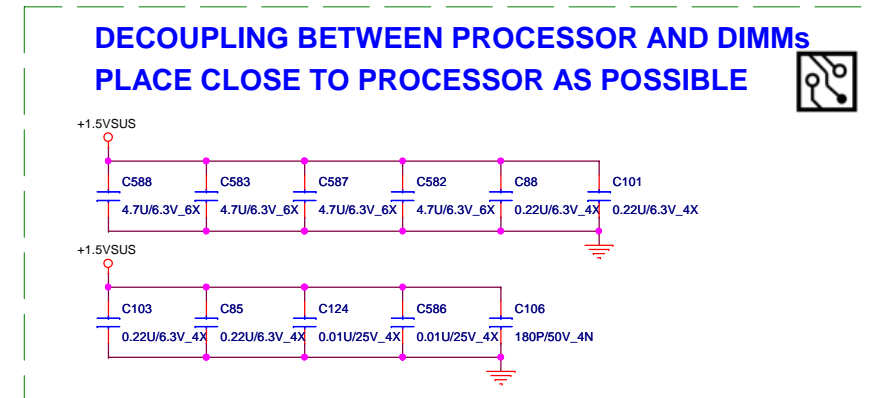
* default		
SEL_HTT66 (HTT)	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA (SR6)	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27 (SR7)	1*	27MHz non-spreading single clock
	0	100 MHz spreading differential SRC clock

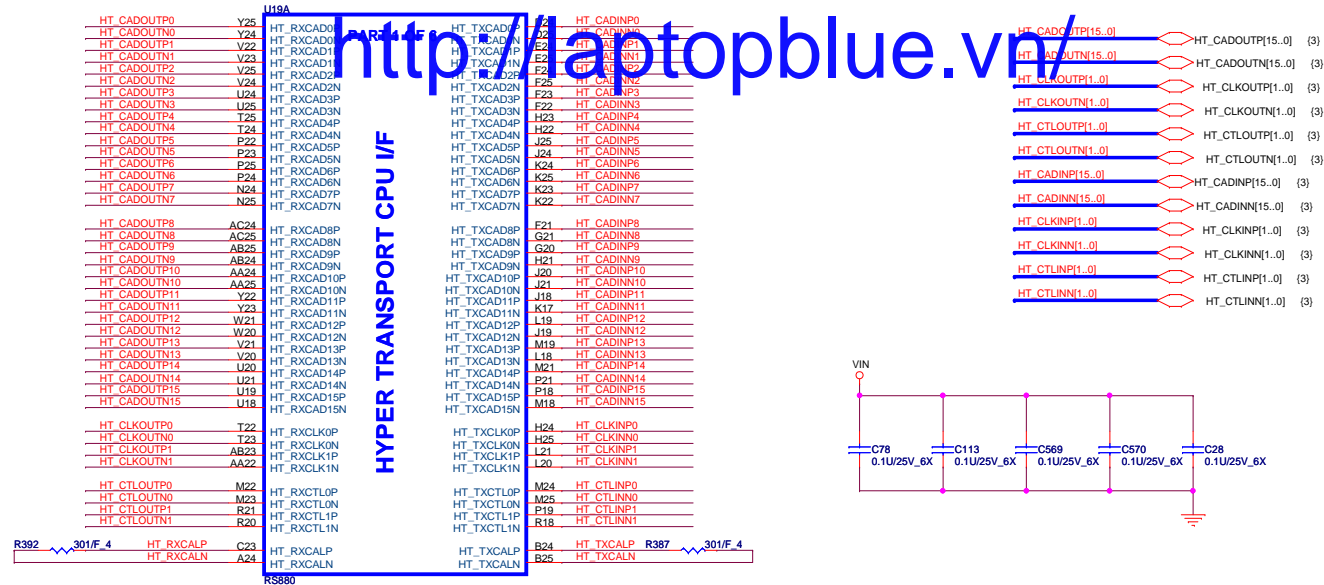
CLOCK Name	Discipline	Clock pin function
CLK_PCIE_X CLK_PCIE_VGA# CLK_PCIE_VGA#	RP8216 STUFF	Pin for VGA reference clock
CLK_PCIE_VGA CLK_PCIE_VGA#	RP8216 STUFF	to Park-S3 external reference clock -Discrete only
27M_CLK	R8377 --> SS R8379 --> NSS	To Park-S3 27Mhz - Discrete only

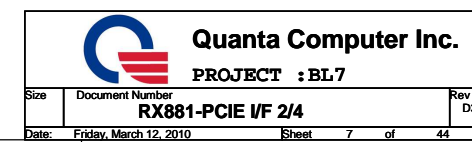
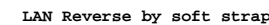


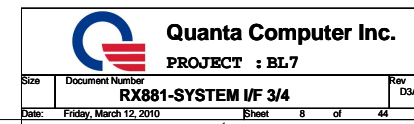
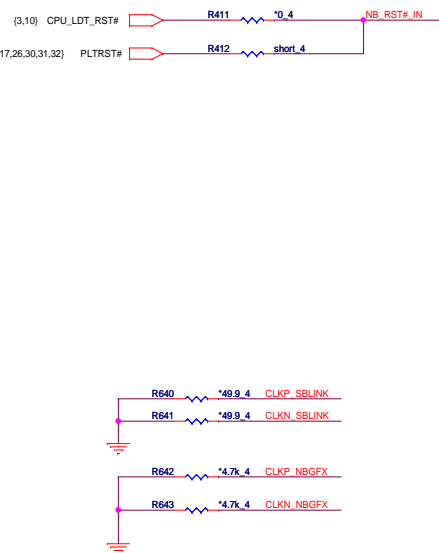




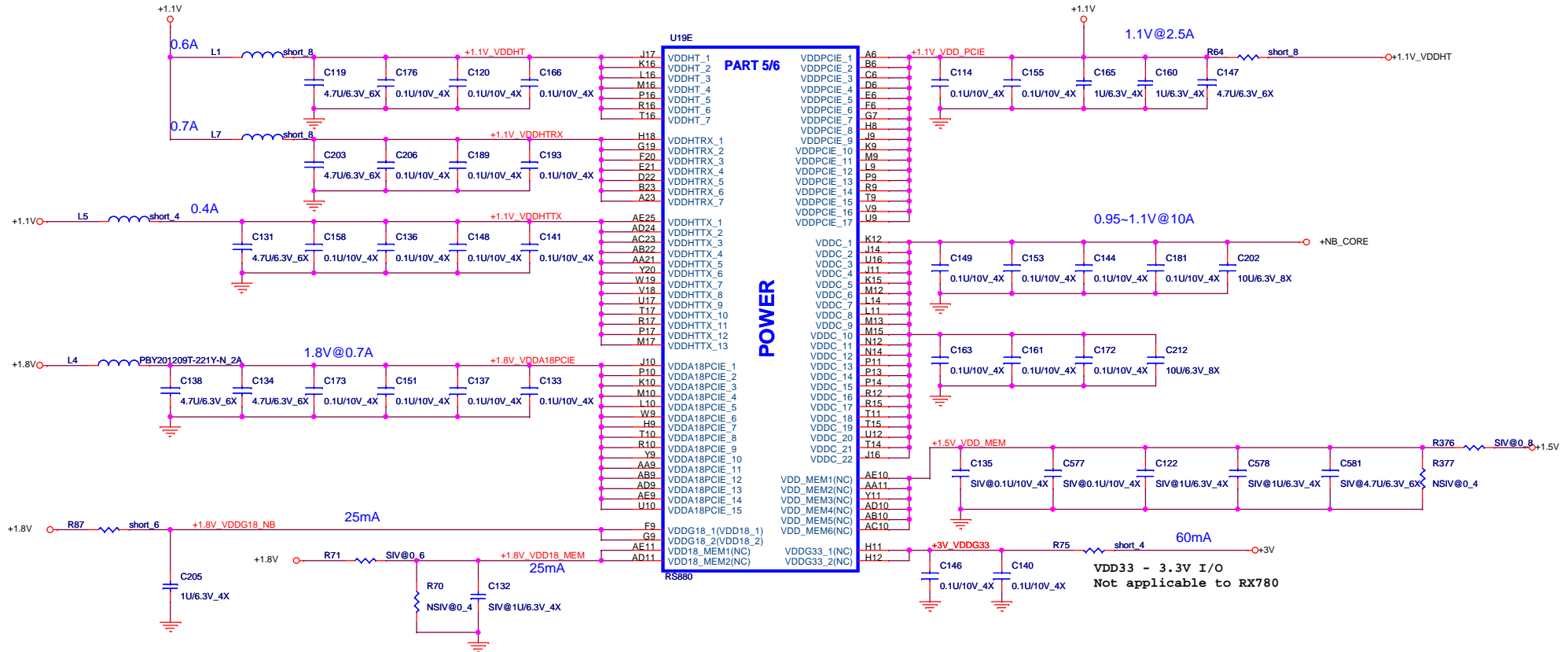
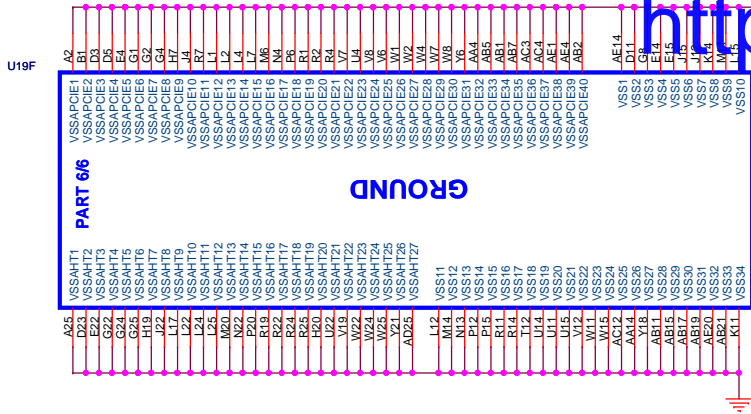


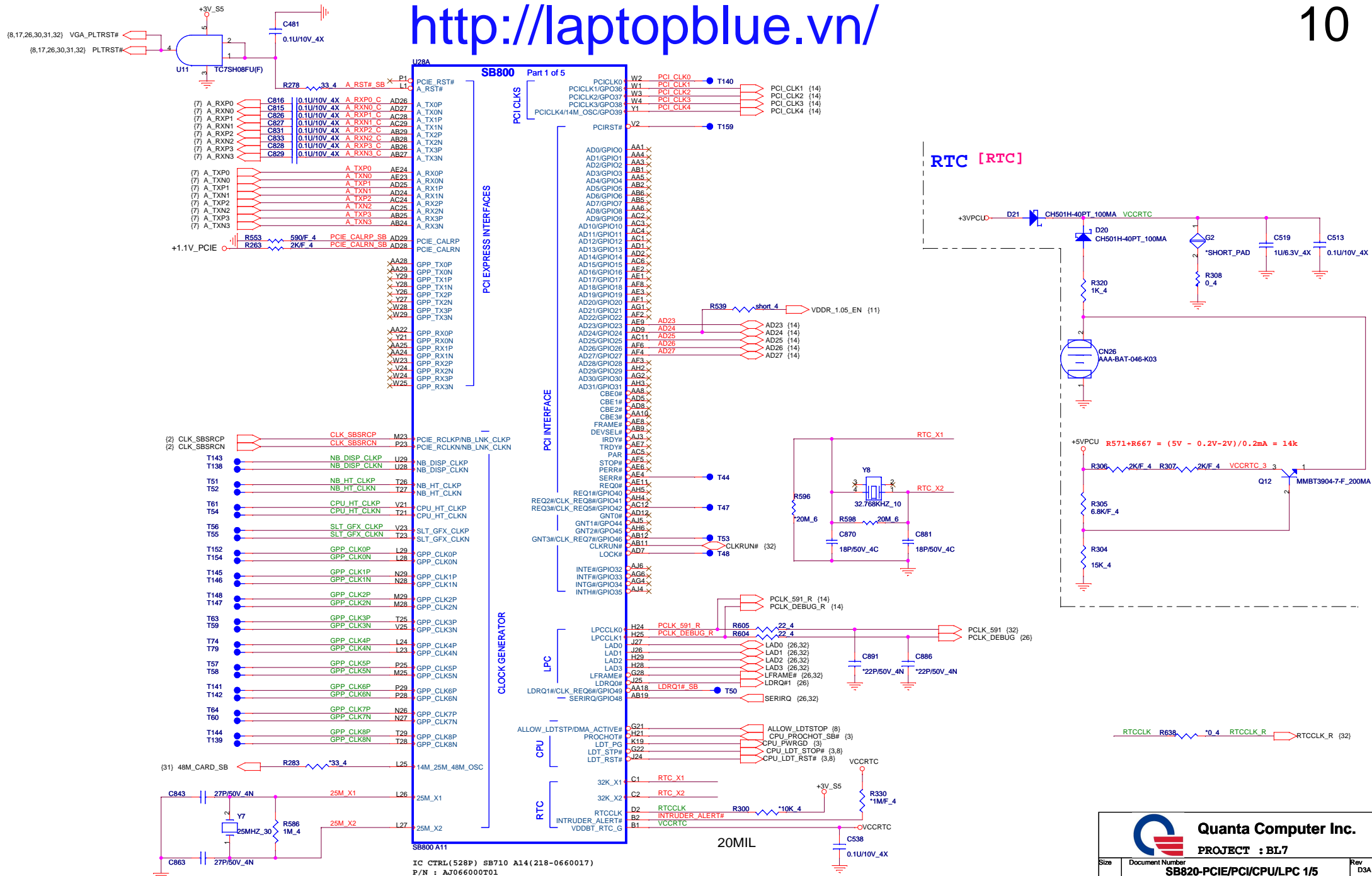






PIN NAME	RS880	PIN NAME	RS880
VDDHT	+1.1V	IOPLLVD0	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD0	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC





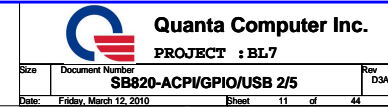
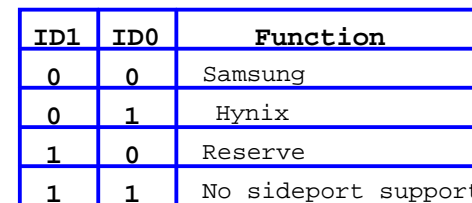
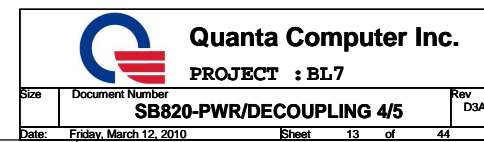




Figure 1: Schematic diagram of the board connections for the 100-pin connector. The diagram shows three rows of connections. The top row shows BOARD_ID3, BOARD_ID2, and BOARD_ID1 connected to +3V and ground through resistors R266, R267, R276, R275, R272, and R268. The middle row shows BOARD_ID8, BOARD_ID7, and BOARD_ID5 connected to +3V and ground through resistors R650, R649, R648, R647, R273, and R274. The bottom row shows BOARD_ID6 and BOARD_ID4 connected to +3V and ground through resistors R270 and R269. Each connection is labeled with a pin number in parentheses: (33) BT_Detect#, (11) BOARD_ID7, (26) CPUSB#, and (33) BT_Detect#.





REQUIRED STRAPS

<http://laptopblue.vn/>

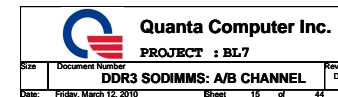
14

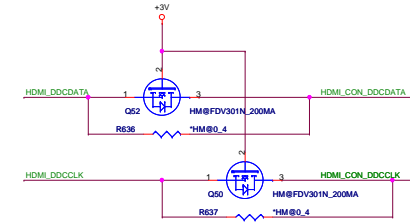
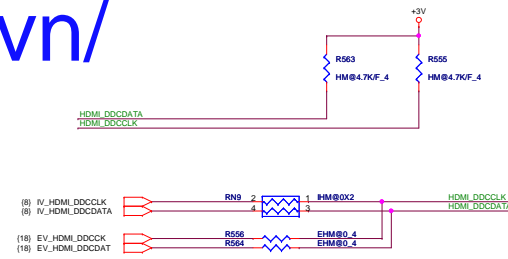
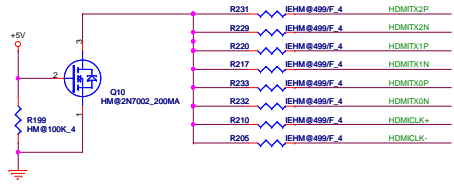
Ball Name	Strap Name	Default	Description	Setting
LPCCLK0	ECEnableStrap	0	0 -- Disable 1 -- Enable Enable to support enhanced hardware monitor feature	{10} PCLK_591_R +3V_S50 R624 *10K/F 4 R626 *10K/F 4
EC_PWM3 EC_PWM2	ROMTYPE_1 ROMTYPE_0	(0,1)	(0,0) = Firmware Hub (0,1) = LPC (1,0) = SPI (1,1) = Reserved	{11} EC_PWM3 +3V_S50 R323 *10K/F 4 R322 *2.2K 4 {11} EC_PWM2 +3V_S50 R302 *10K/F 4 R299 *2.2K 4
LPCCLK1	CLKGEN	0	0 -- External clock 1 -- Integrate clock	{10} PCLK_DEBUG_R +3V_S50 R603 *10K/F 4 R609 *10K/F 4
PCICLK1	BIF_GEN2_COM PLIANCE_Strap	1	0 -- PCIE at Gen I mode 1 -- PCIE at Gen II mode	{10} PCI_CLK1 +3V_S50 R572 *10K/F 4 R573 *10K/F 4
PCICLK2	BootFailTmeEn	0	0 -- Disable watchdog function 1 -- Enable watchdog function	{10} PCI_CLK2 +3V_S50 R568 *10K/F 4 R567 *10K/F 4
PCICLK3	DefaultStrapMode	0	0 -- Disable debug Straps 1 -- Select ext. Debug Straps	{10} PCI_CLK3 +3V_S50 R561 *10K/F 4 R565 *10K/F 4
PCICLK4	CPUClkSel	1	0 -- Reserved 1 -- Integrated clock mode	{10} PCI_CLK4 +3V_S50 R566 *10K/F 4 R562 *10K/F 4
AZ_SDOUT	CoreSpeedMode	0	0 -- Performance mode 1 -- Low Power mode	{11} ACZ_SDOUT +3V_S50 R581 *10K/F 4 R580 *10K/F 4

DEBUG STRAPS

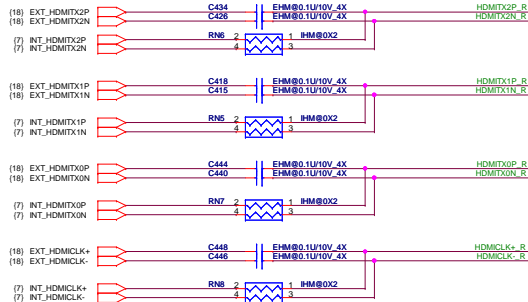
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

Ball Name	Strap Name	Default	Description	Setting
AD27	PciPl1Byp	1	0 -- ByPass Int PLL 1 -- Int. PLL	{10} AD27 +3V_S50 R560 *10K/F 4 R558 1 *2.2K 4
AD26	ILAAutronEnB	1	0 - IAL auto run enable 1 -- IAL auto run disable	{10} AD26 +3V_S50 R541 *10K/F 4 R540 1 *2.2K 4
AD25	FCClkByP	1	0 -- Bypass FC Clk 1 -- Int. FC Clk	{10} AD25 +3V_S50 R543 *10K/F 4 R554 1 *2.2K 4
AD24	I2CRomEn	1	0 -- Enable EEPROM 1 -- Disable EEPROM	{10} AD24 +3V_S50 R537 *10K/F 4 R538 1 *2.2K 4
AD23	PCI_ROM_BOOT	1	0 -- Disable PCI MEM Boot 1 -- Enable PCI MEM Boot	{10} AD23 +3V_S50 R536 *10K/F 4 R535 1 *2.2K 4
All signals ihas nternal PU				

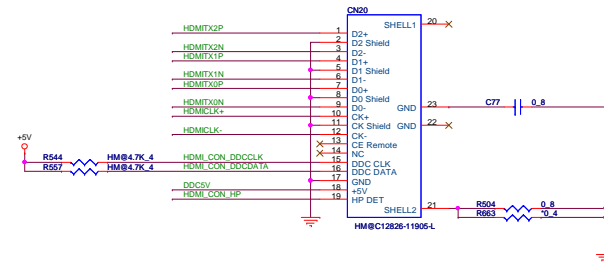
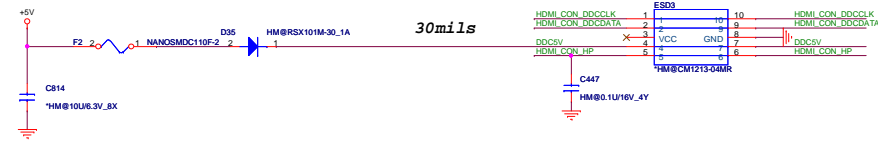
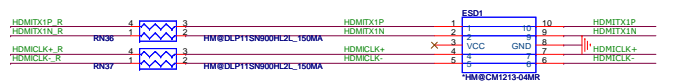
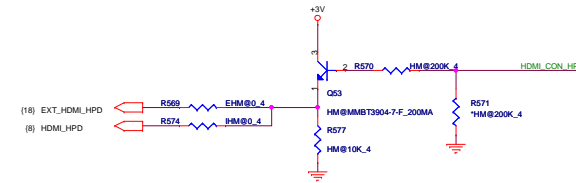




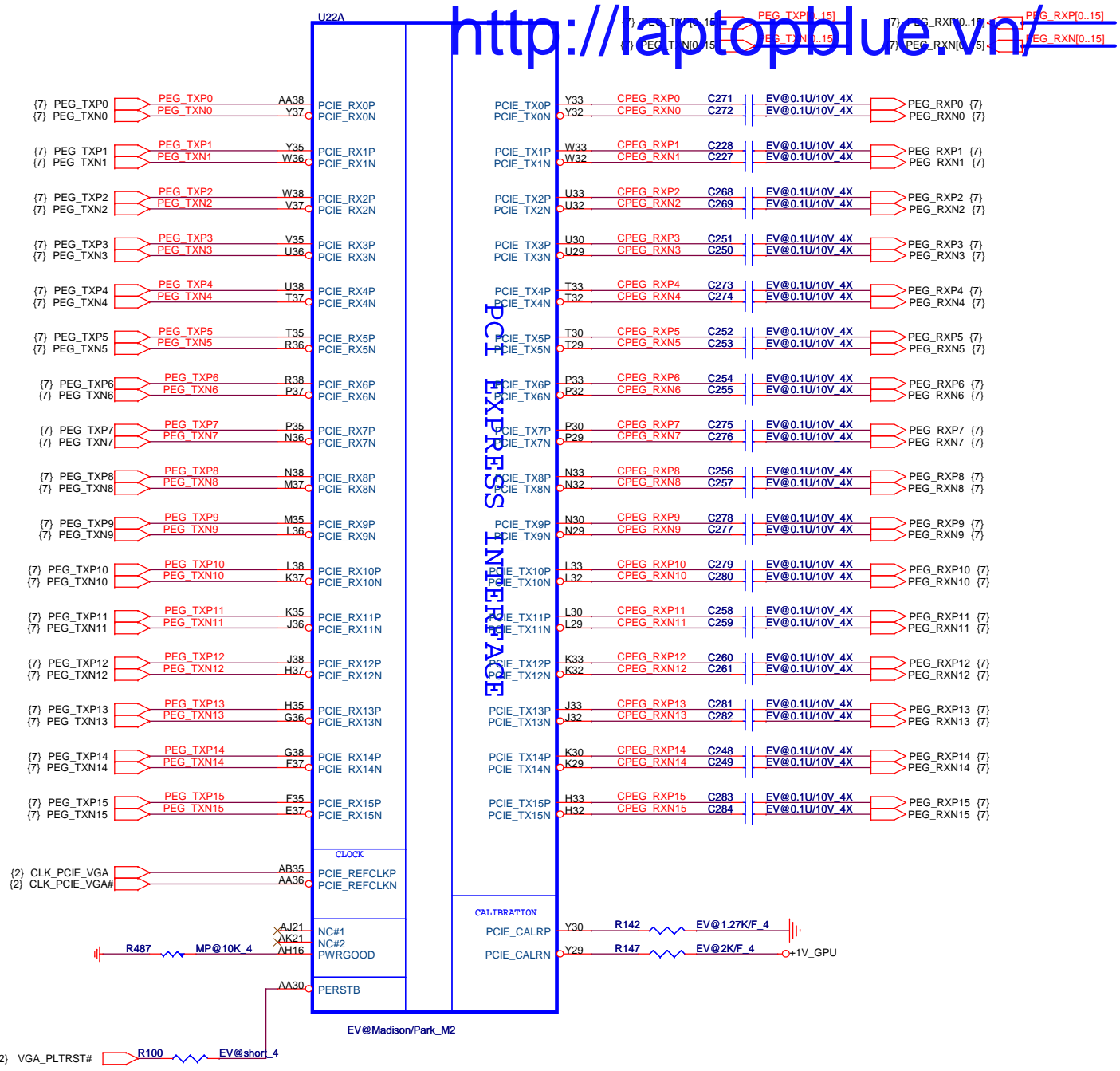
Discrete HDMI



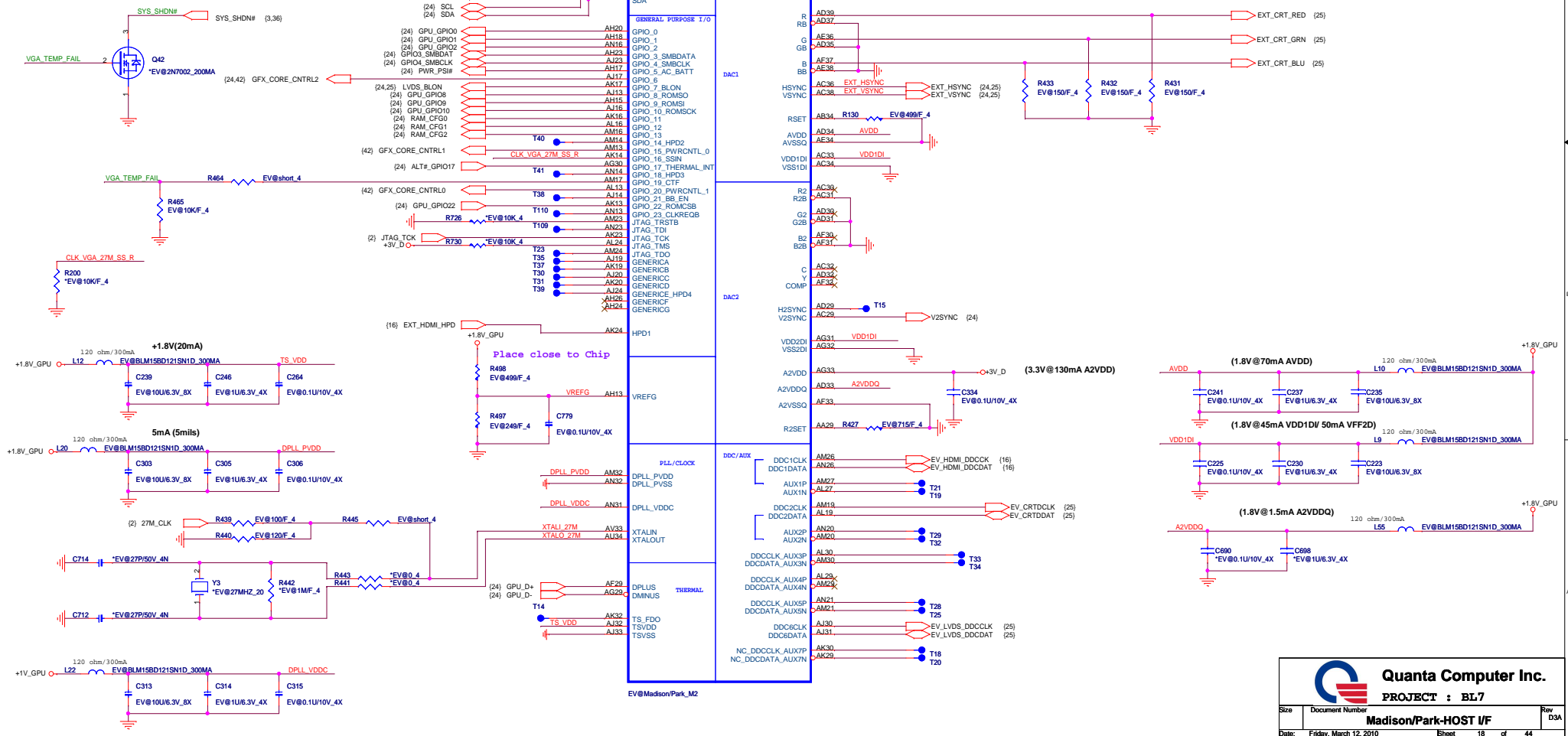
HDMI HPD



<http://laptopblue.vn/>



JTAG SIGNAL STUFF OPTION FOR OPTION2			
SIGNALS	NORMAL MODE	JTAG MODE (DEBU	
TESTEN	"1" (PU)	"1" (PU)	
GPIO24_TRSTB	"0" (PD)	"1" (PU)	
GPIO26_TCK	CLK	"1" (PU)	
GPIO27_TMS	"1" (PU)	"1" (PU)	

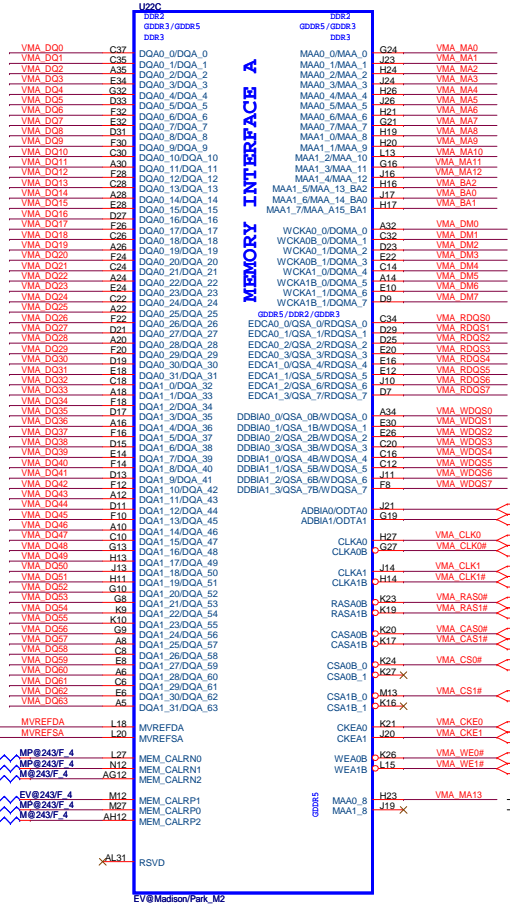


(20) VMA_DQ[63..0] \rightarrow VMA_DQ[63..0]
 (20) VMA_DM[7..0] \rightarrow VMA_DM[7..0]
 (20) VMA_RDQS[7..0] \rightarrow VMA_RDQS[7..0]
 (20) VMA_WDQS[7..0] \rightarrow VMA_WDQS[7..0]
 (20) VMA_MA[13..0] \rightarrow VMA_MA[13..0]

(20) VMA_BA0 \rightarrow VMA_BA0
 (20) VMA_BA1 \rightarrow VMA_BA1
 (20) VMA_BA2 \rightarrow VMA_BA2

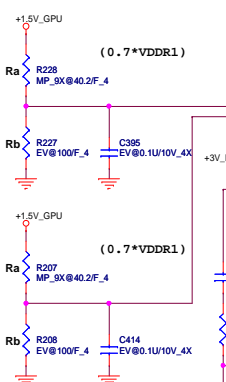
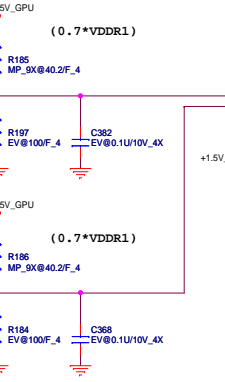
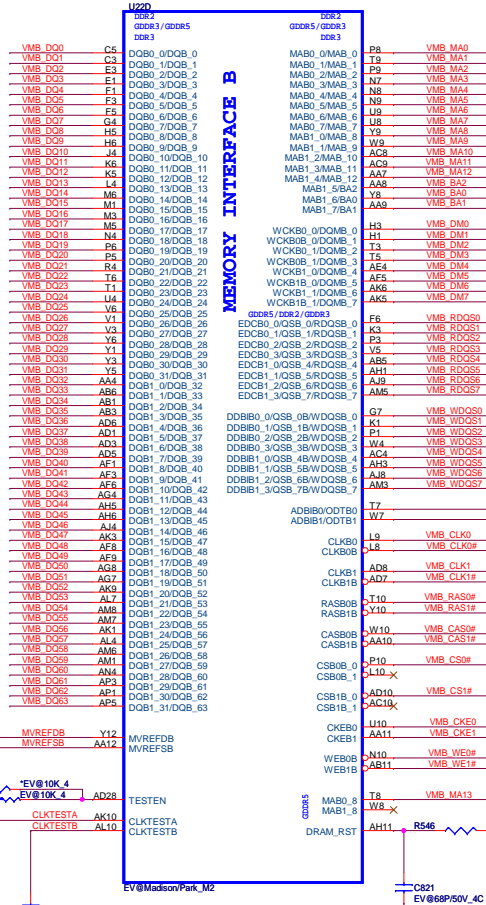
(21) VMB_DQ[63..0] \rightarrow VMB_DQ[63..0]
 (21) VMB_DM[7..0] \rightarrow VMB_DM[7..0]
 (21) VMB_RDQS[7..0] \rightarrow VMB_RDQS[7..0]
 (21) VMB_WDQS[7..0] \rightarrow VMB_WDQS[7..0]
 (21) VMB_MA[13..0] \rightarrow VMB_MA[13..0]

(21) VMB_BA0 \rightarrow VMB_BA0
 (21) VMB_BA1 \rightarrow VMB_BA1
 (21) VMB_BA2 \rightarrow VMB_BA2



MEMORY INTERFACE A

MEMORY INTERFACE B



DDR3/GDDR3 Memory Stuff Option

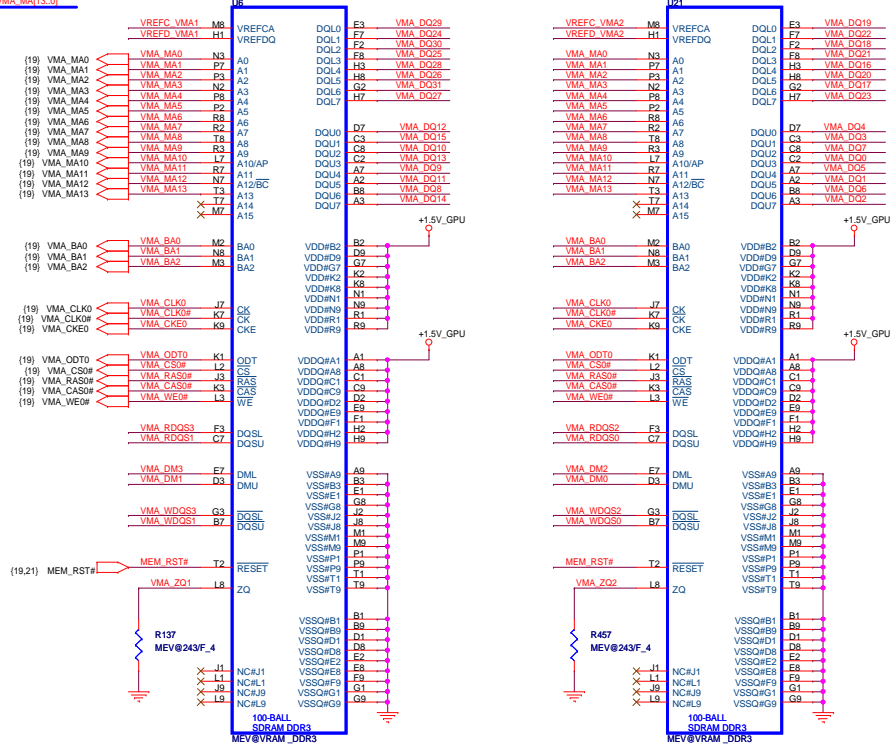
	DDR3	GDDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

	Value
R185	MP@ 40.2F_4 100F_4
R186	40.2F_4 100F_4
R207	40.2F_4 100F_4
R228	40.2F_4 100F_4

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V	V		
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

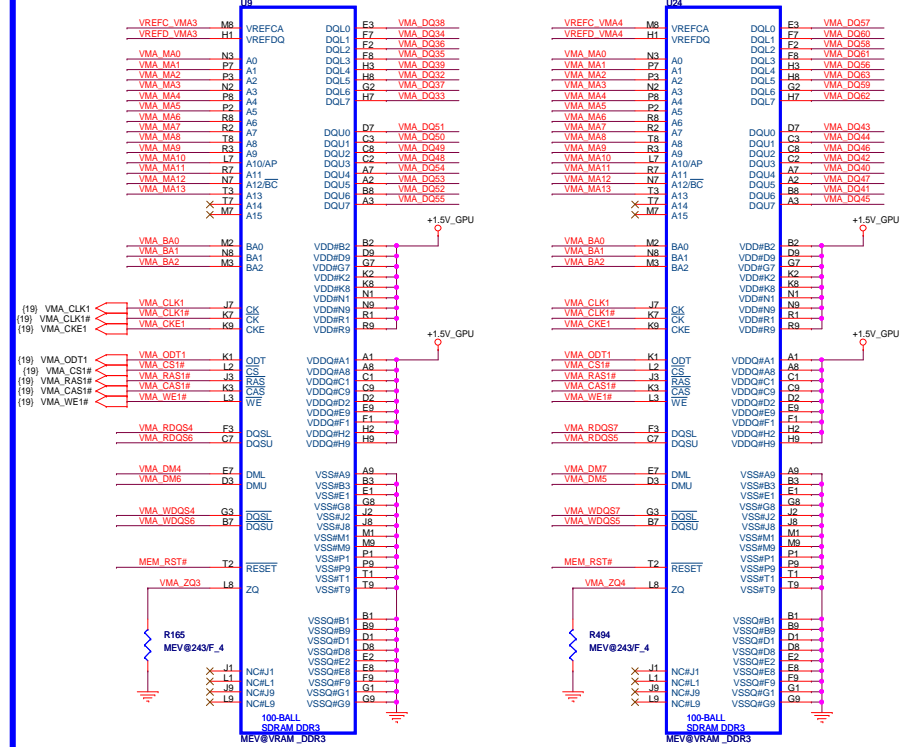
(19) VMA_DQ[63..0] VMA_DQ[63..0]
(19) VMA_DM[7..0] VMA_DM[7..0]
(19) VMA_RDQS[7..0] VMA_RDQS[7..0]
(19) VMA_WDQS[7..0] VMA_WDQS[7..0]
(19) VMA_MA[13..0] VMA_MA[13..0]

QSA[7..0]
QSA[7..0]



TOP Left

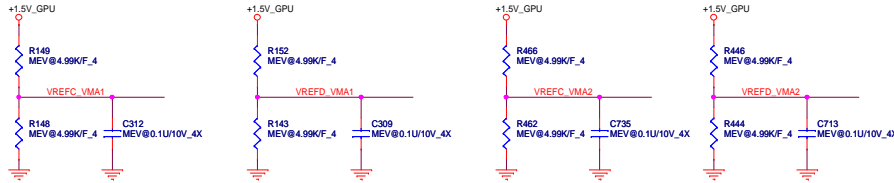
BOT Left



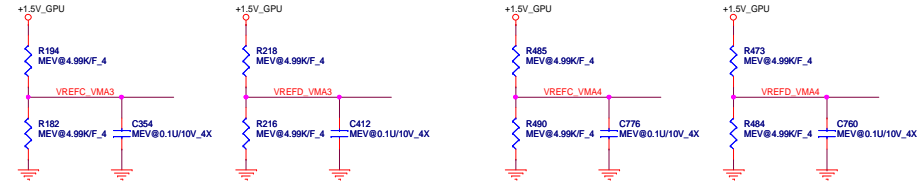
BOT Right

TOP Right

Group-A0 VREF

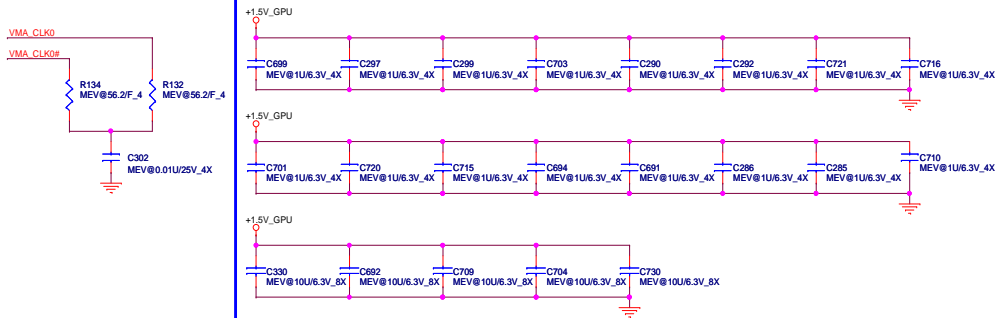


Group-A1 VREF

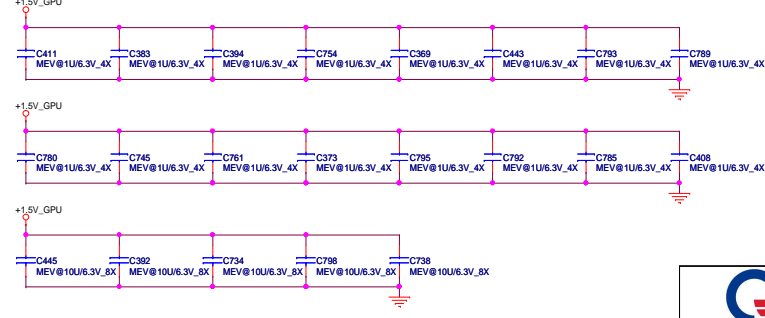


MEM_A0 CLK

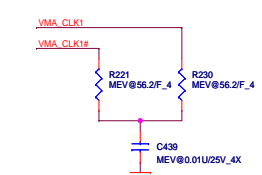
Group-A0 decoupling CAP

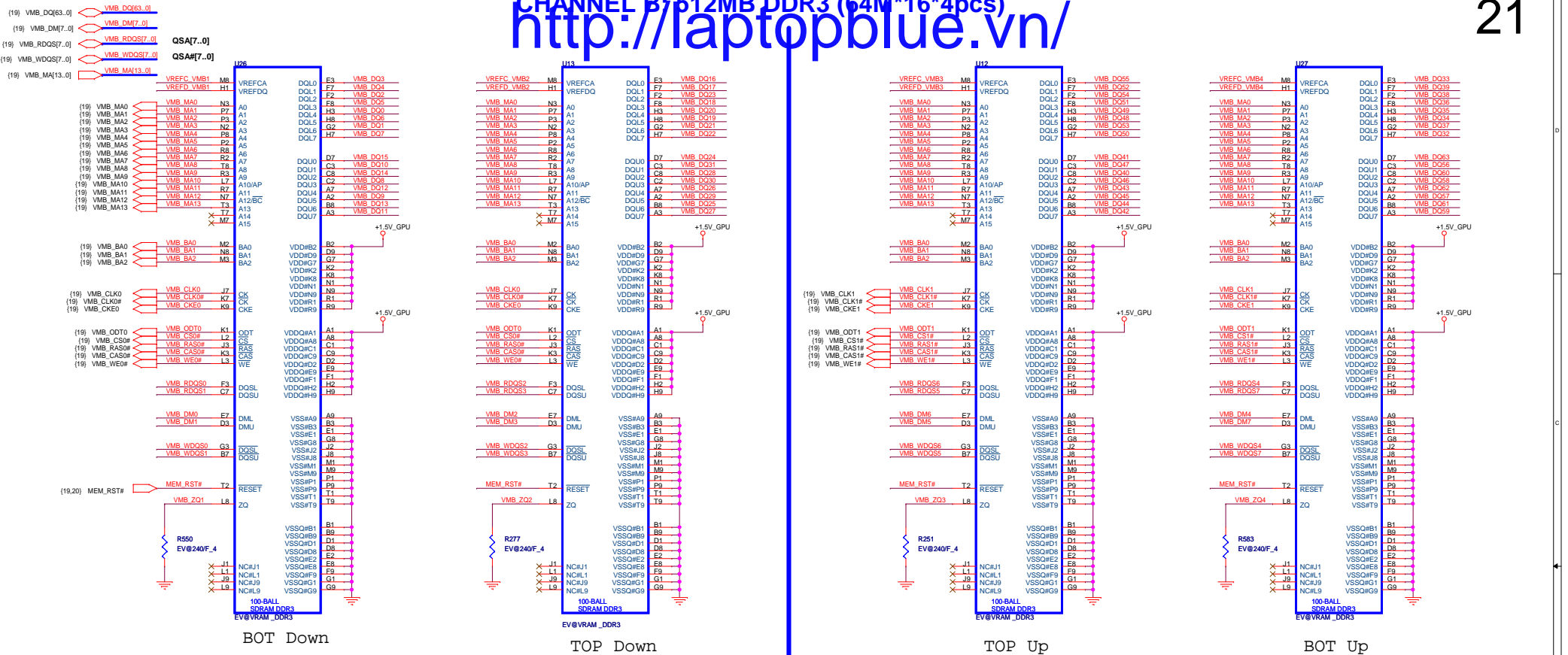


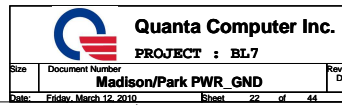
Group-A1 decoupling CAP

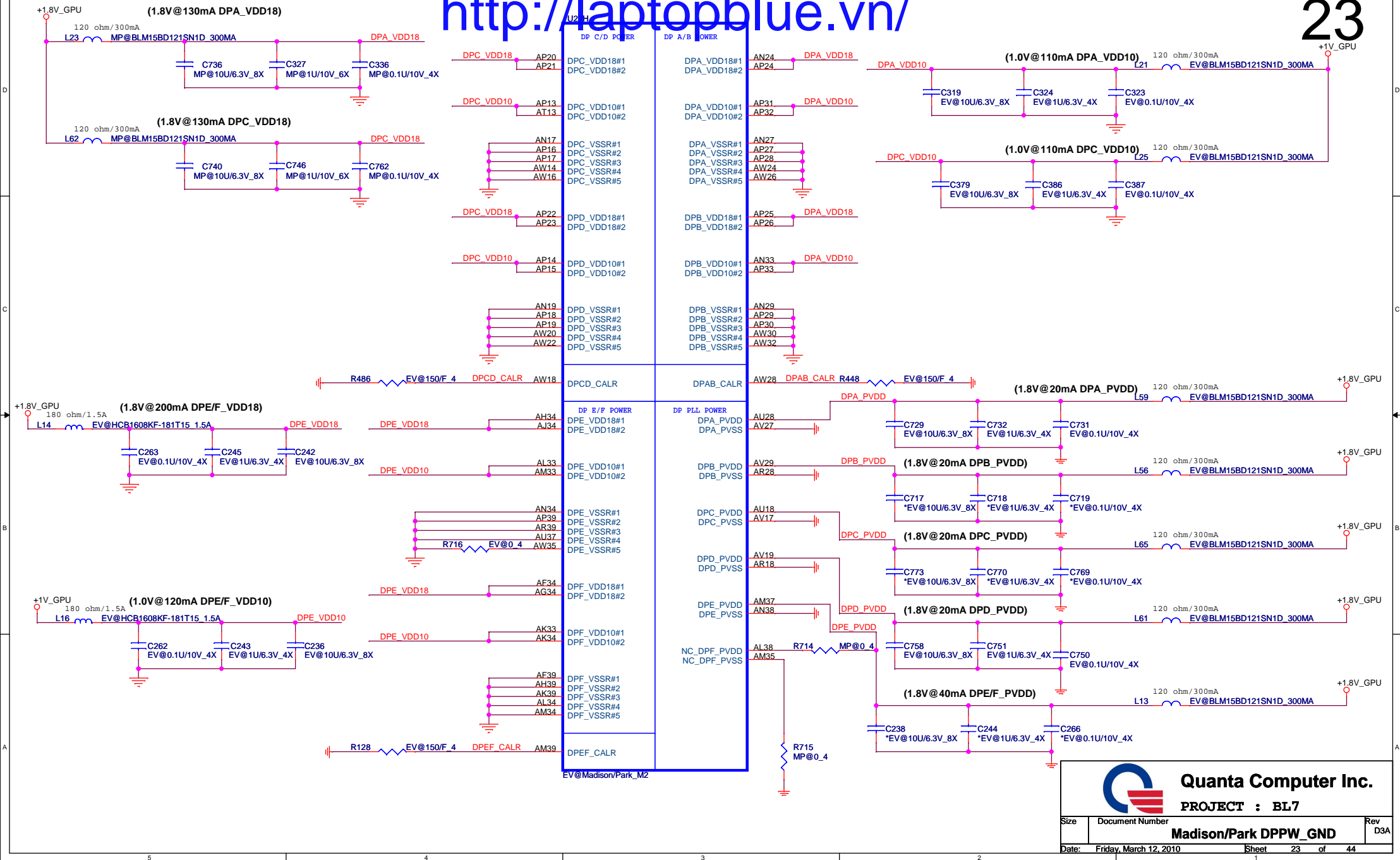


MEM_A1 CLK

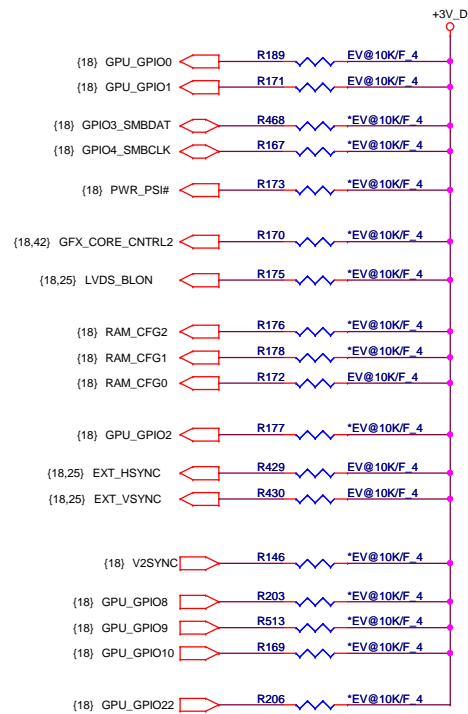




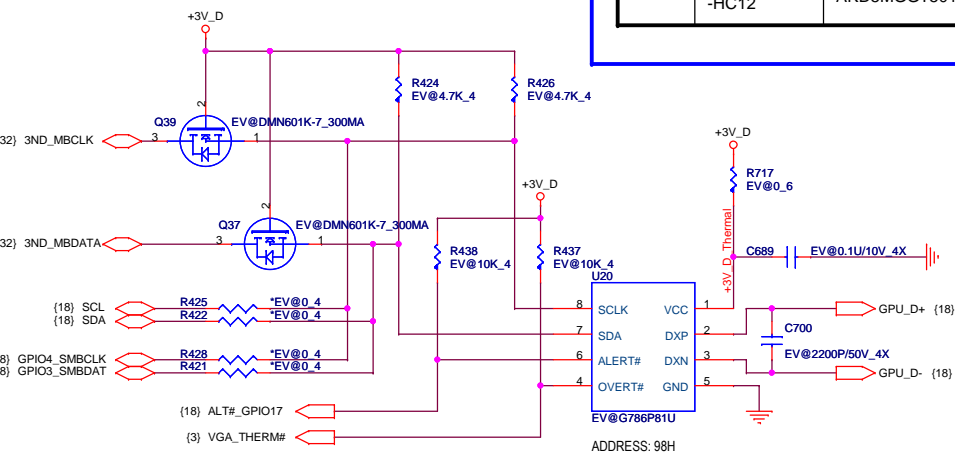




PIN STRAPS



Thermal Sensor

<http://laptopblue.vn/>

Memory Aperture Size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

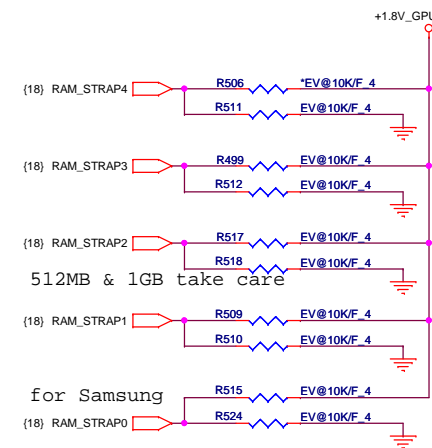
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

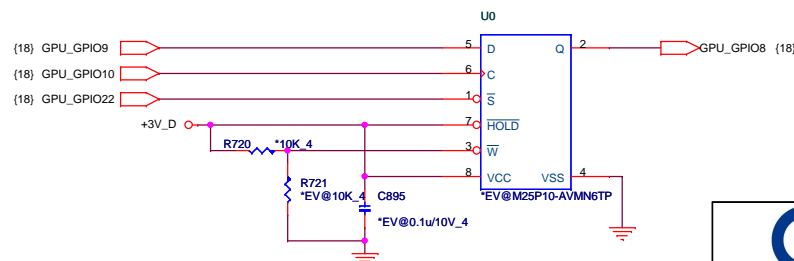
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4	
								15"	14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B-HC12	AKD5MGGT501	2GB	0	0	1	1	0	1

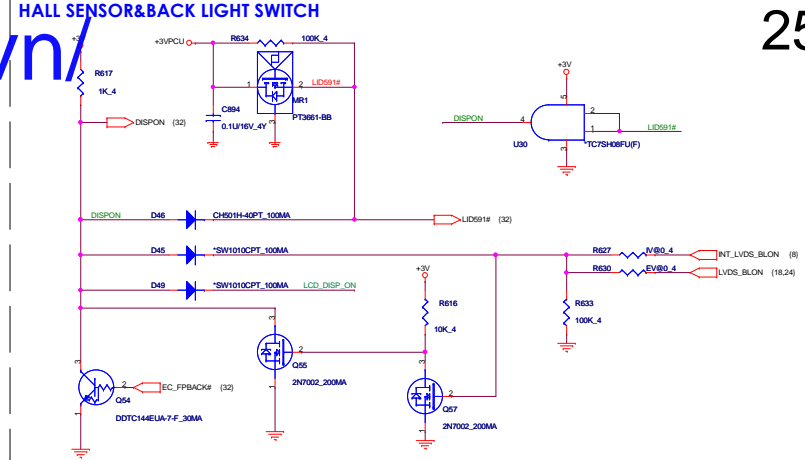
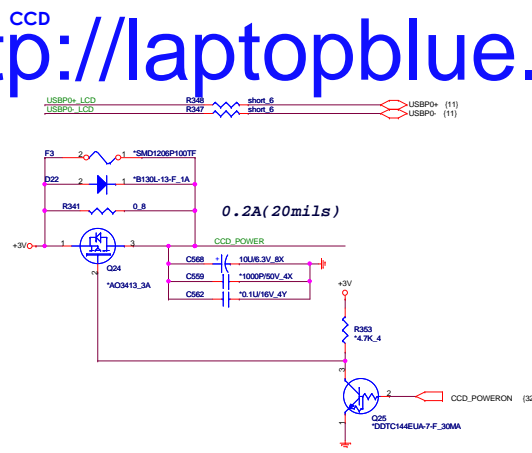
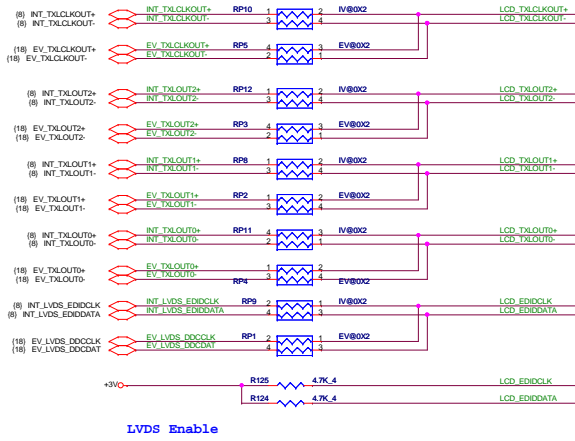


EEPROM

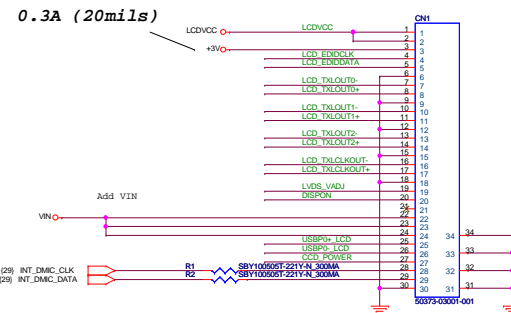
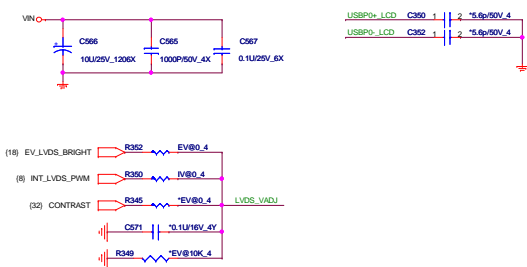


PROJECT : BL7

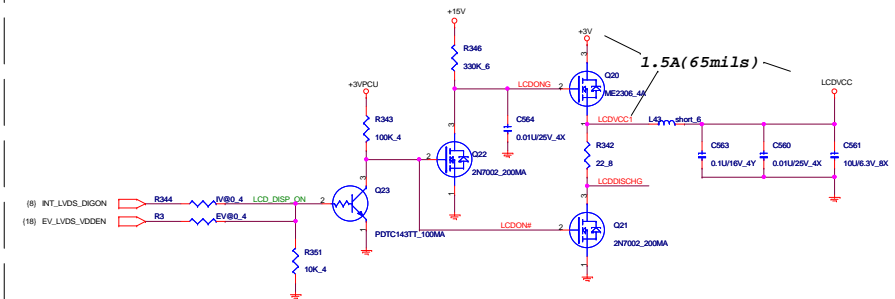
HALL SENSOR&BACK LIGHT SWITCH



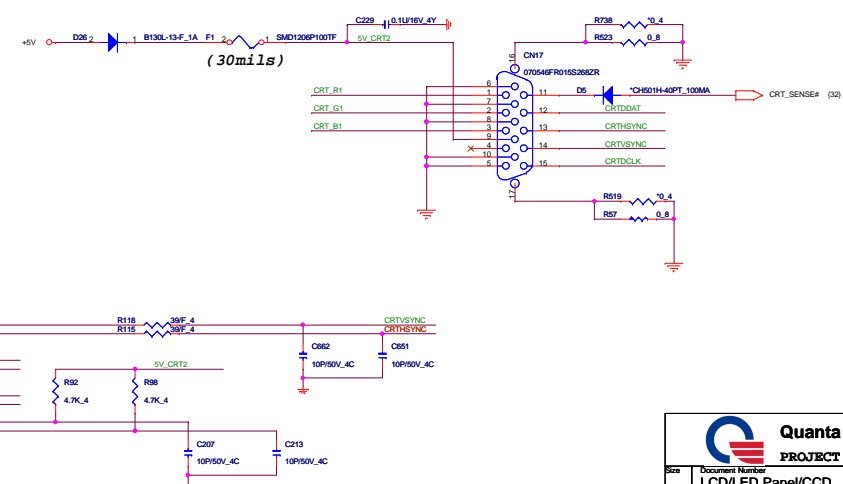
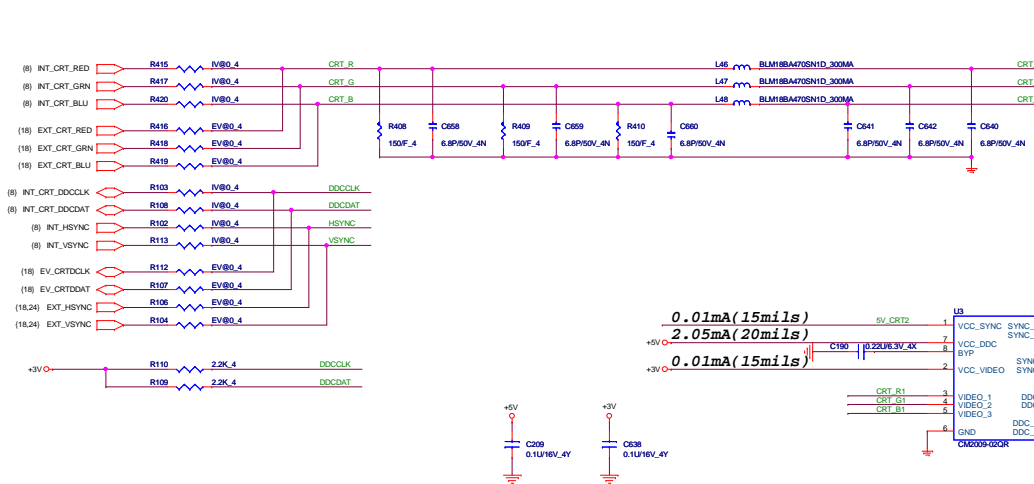
LCD Panel Module



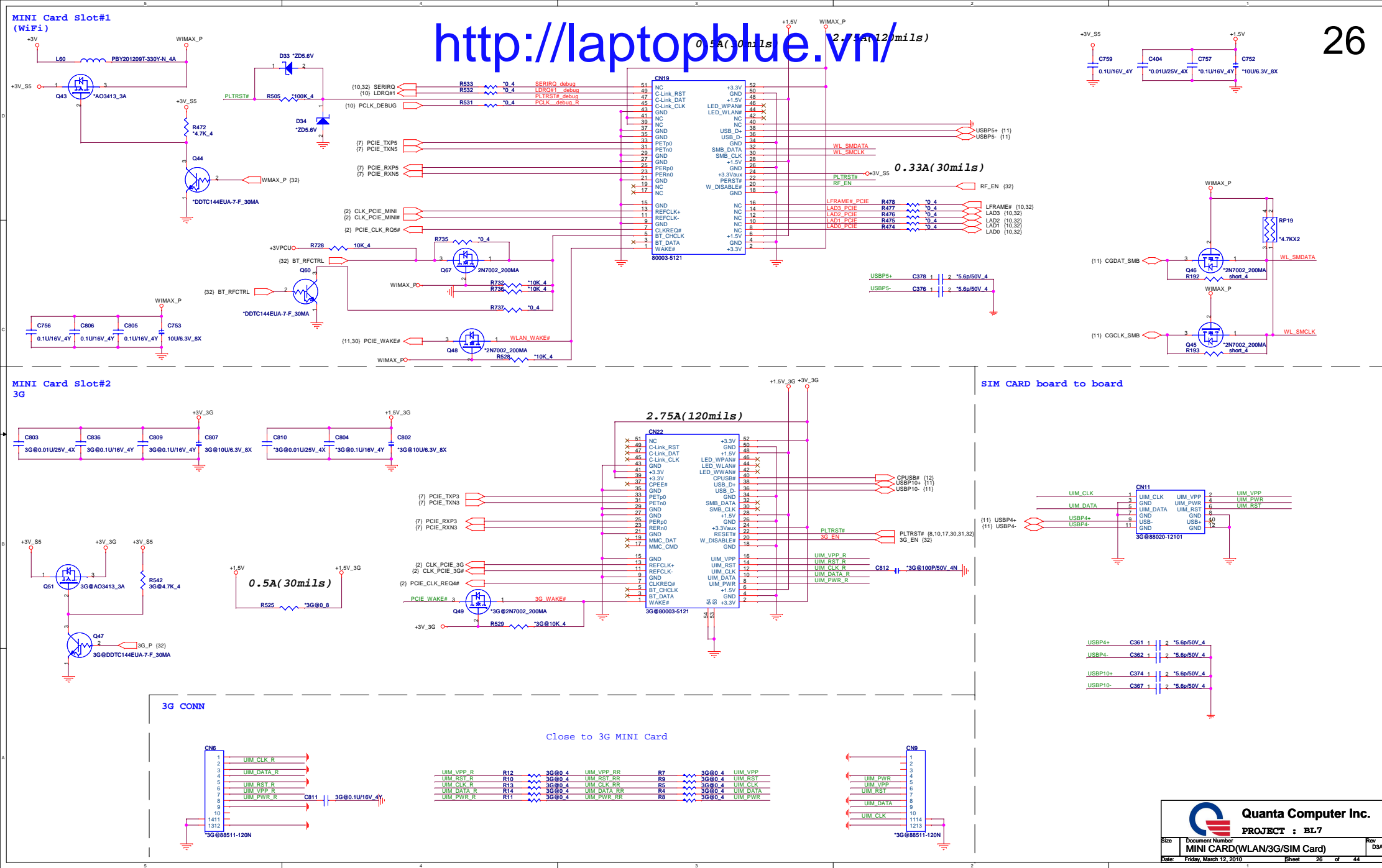
LCD POWER SWITCH

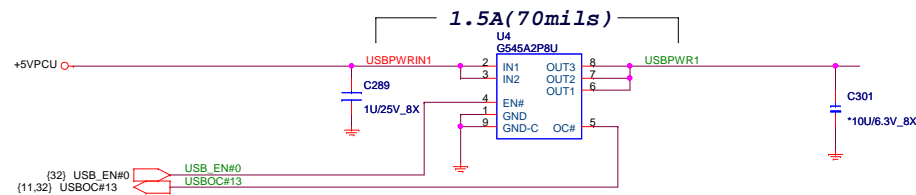
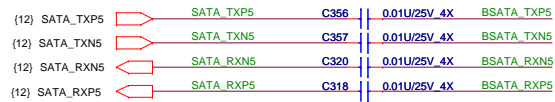


CRT

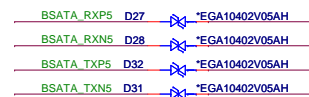
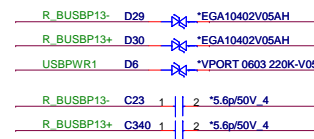
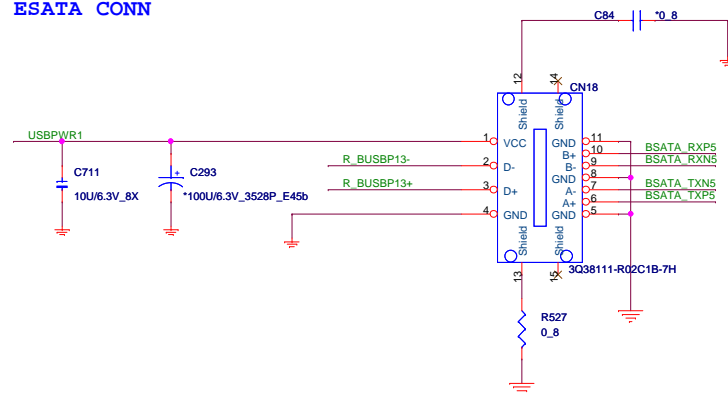


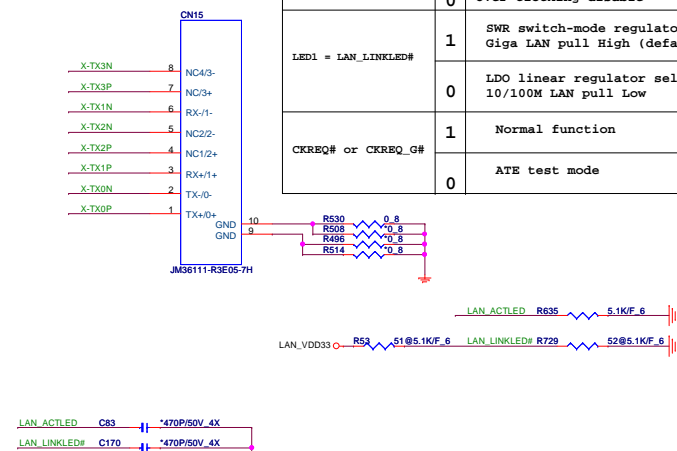
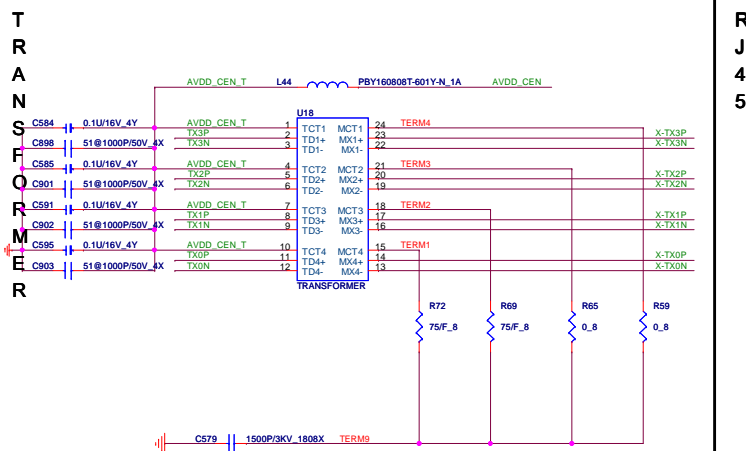
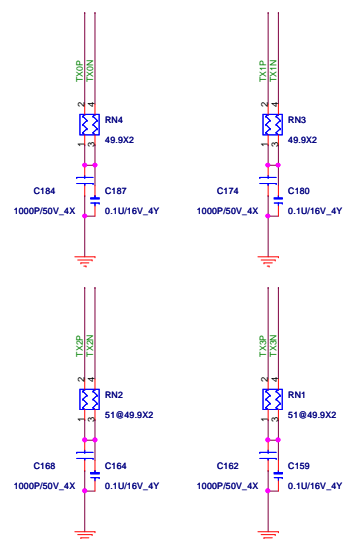
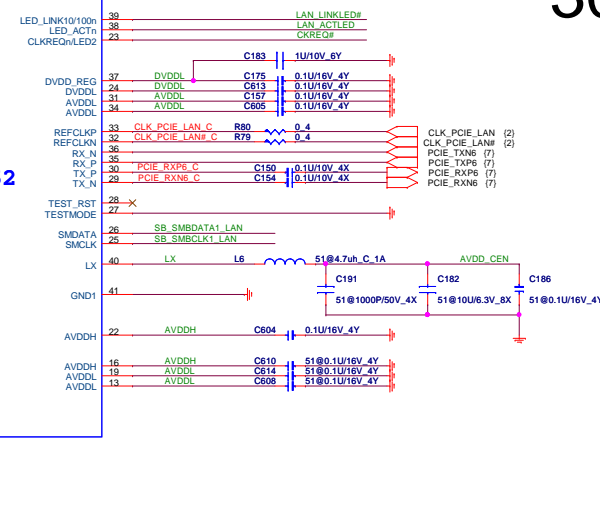
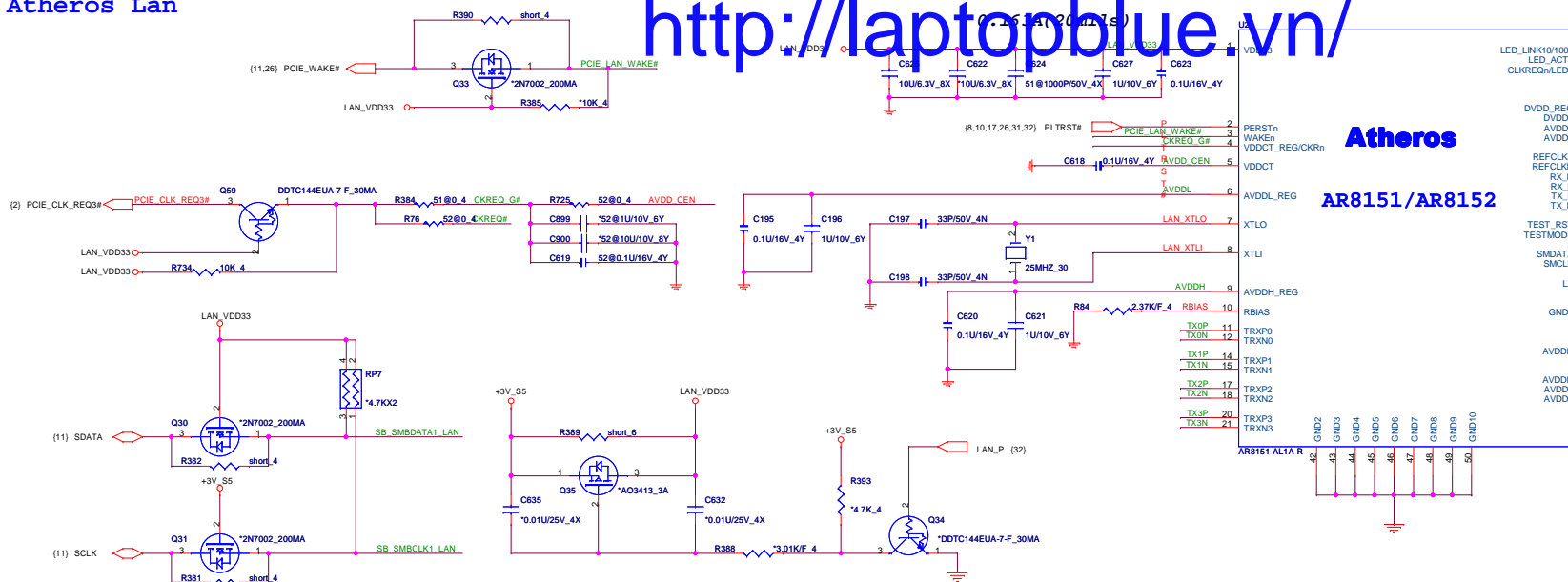
<http://laptopblue.vn/>





ESATA CONN





LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

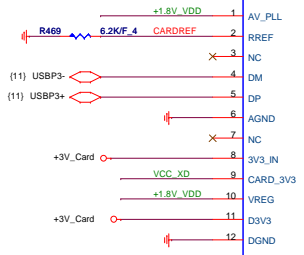
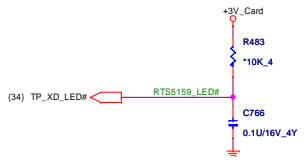
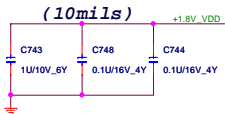
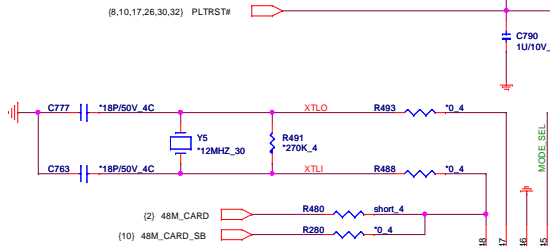
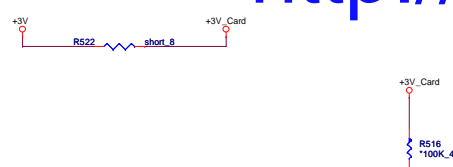
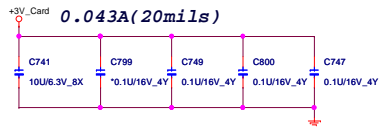


5 IN 1 CARD READER

<http://laptopblue.vn/>

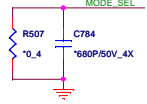
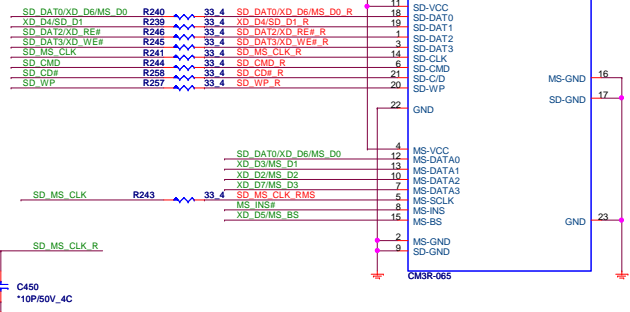
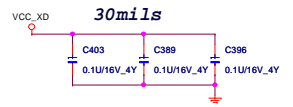
3 IN 1 CARD READER

31



RTS5159-VDD-GR

XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal



Quanta Computer Inc.

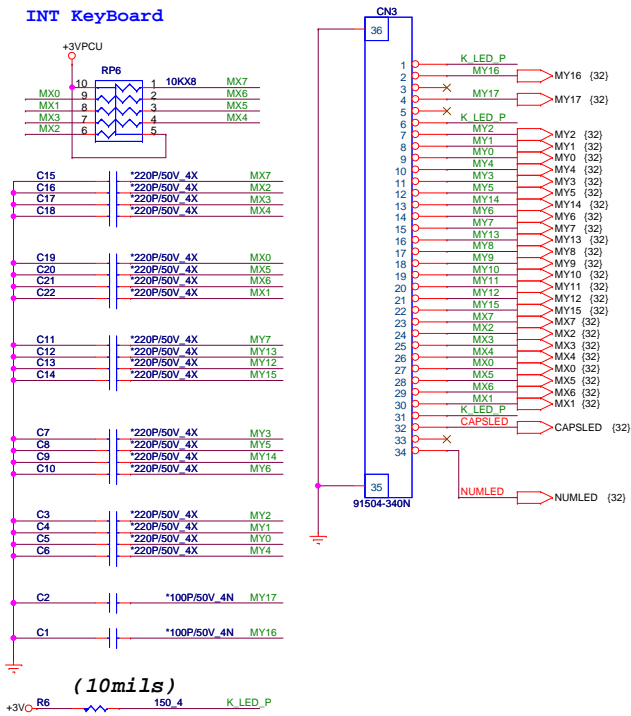
PROJECT : BL7

RTS5159 (Card Reader)

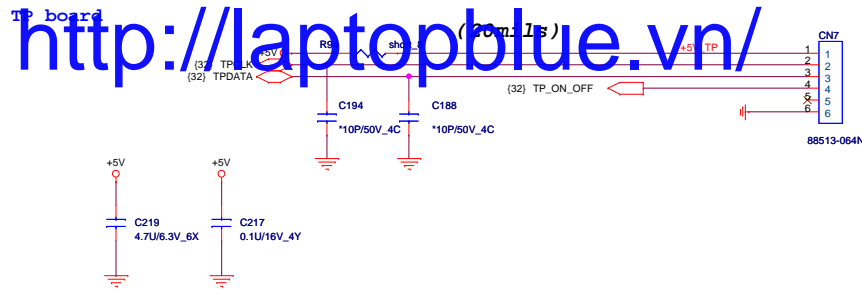
Size: Document Number: Rev: DSA

Date: Friday, March 12, 2010 Sheet: 31 of 44

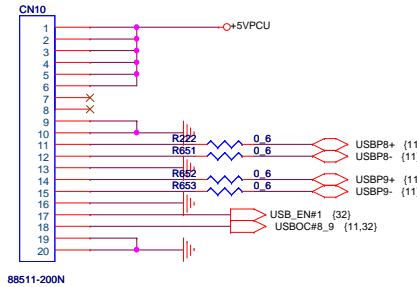
INT Keyboard



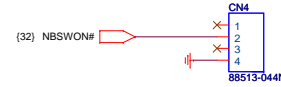
TP board



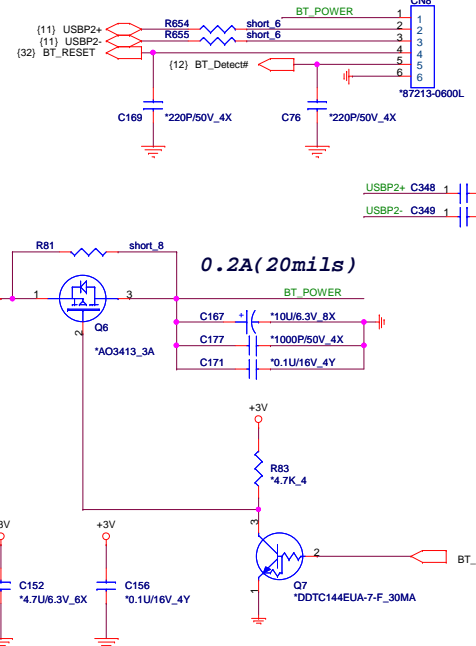
USB board



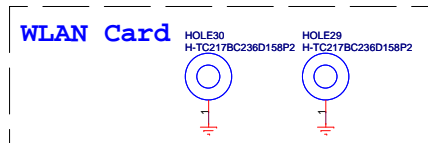
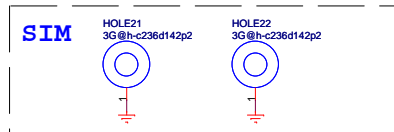
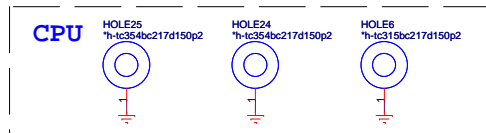
Power board



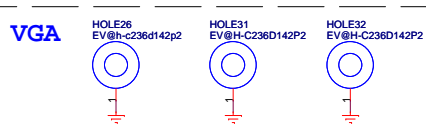
Bluetooth



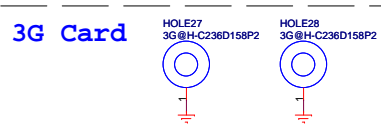
NUT



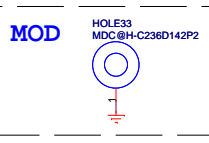
VGA



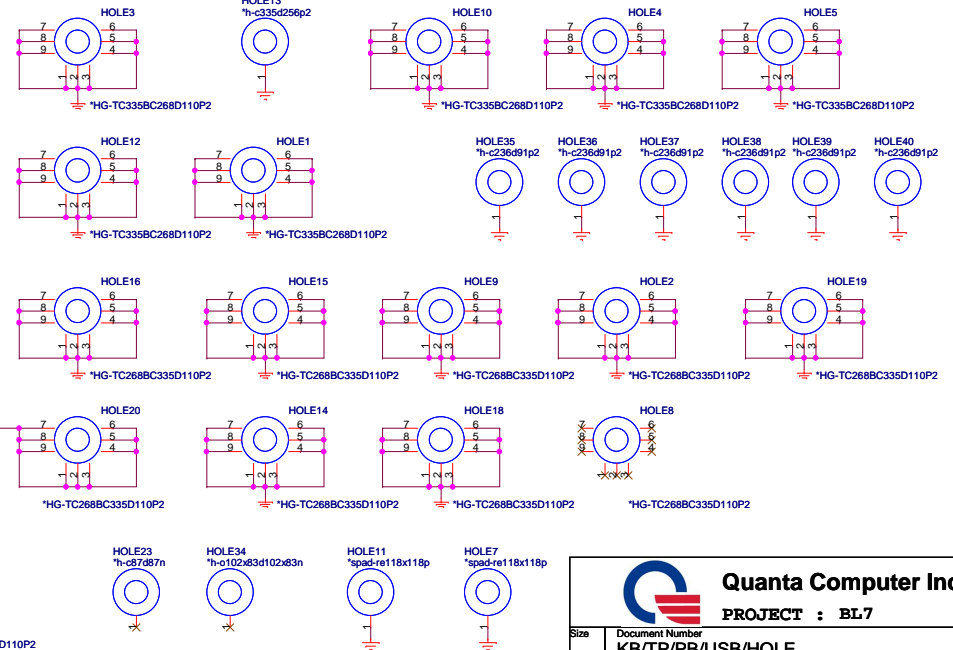
3G Card



MOD



HOLE

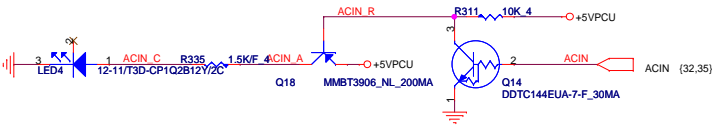


Quanta Computer Inc.
PROJECT : BL7

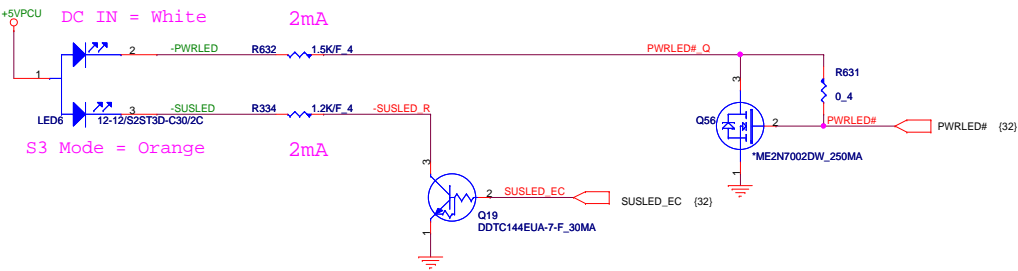
Size	Document Number	Rev
KB/TP/PB/USB/HOLE	D3A	
Date: Friday, March 12, 2010	Sheet 33 of 44	

LED

AC-IN



POWER



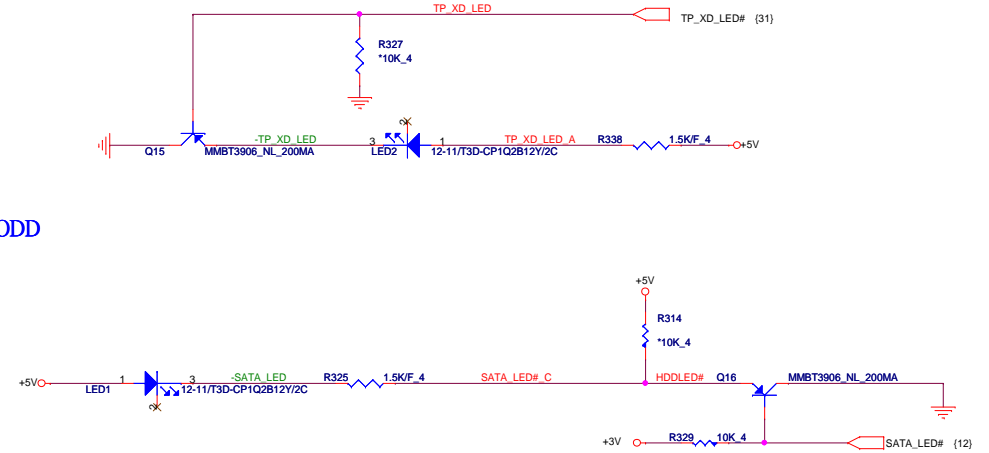
RF LED



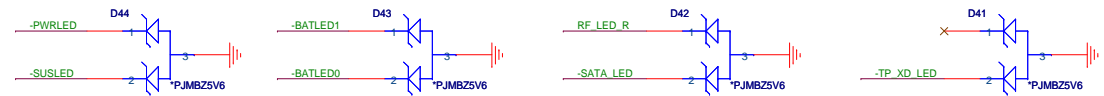
CARDREADER



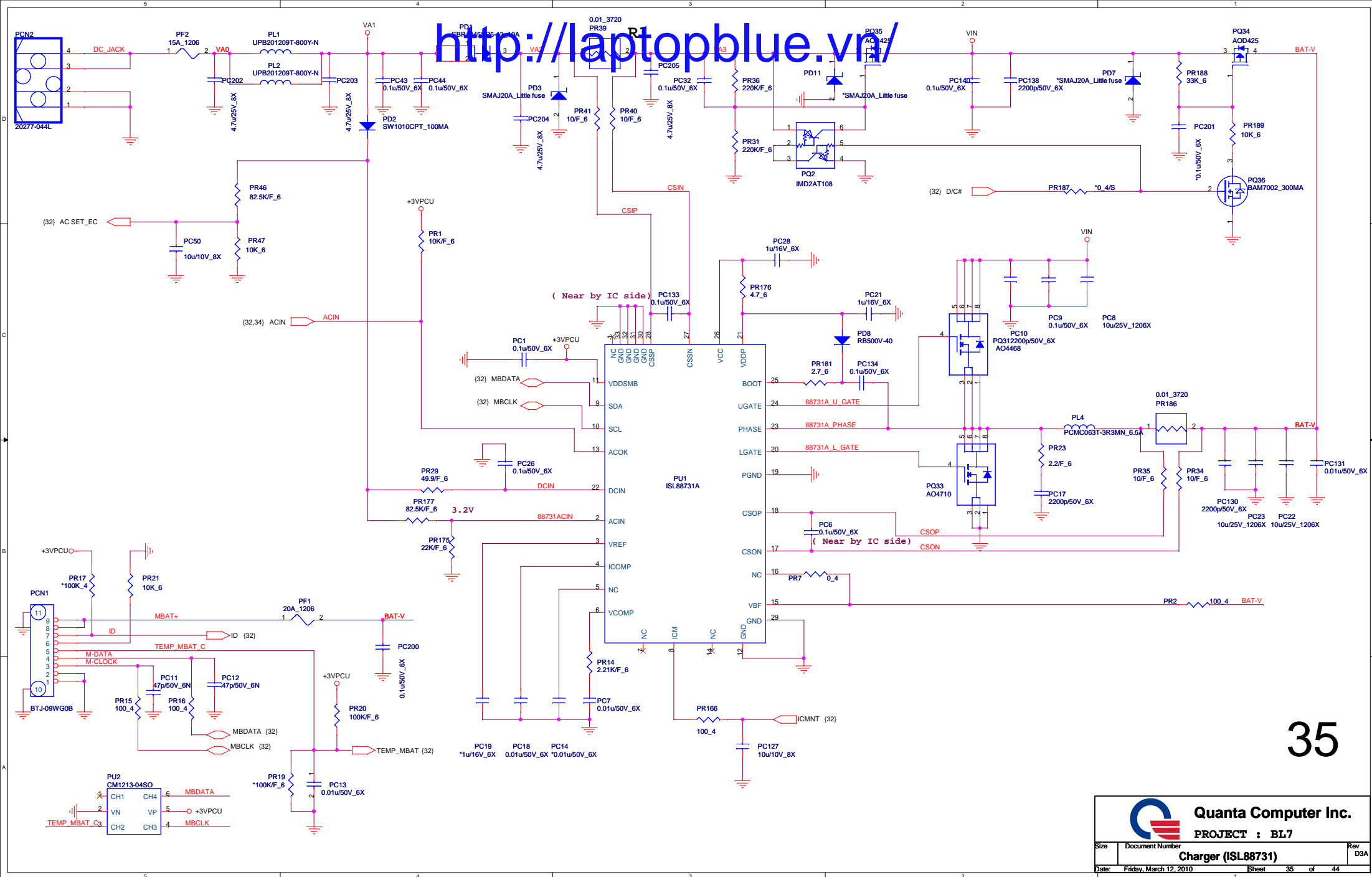
HDD/ODD



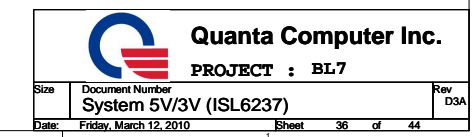
ESD Protect

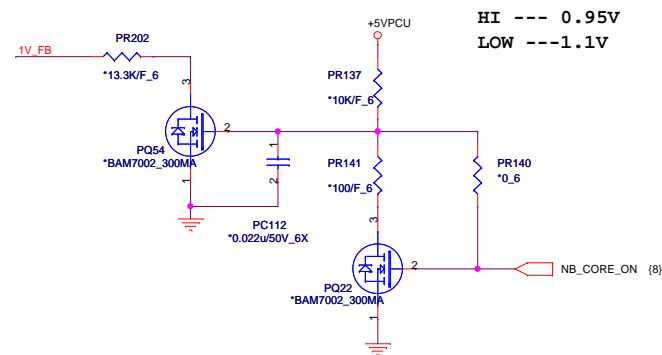
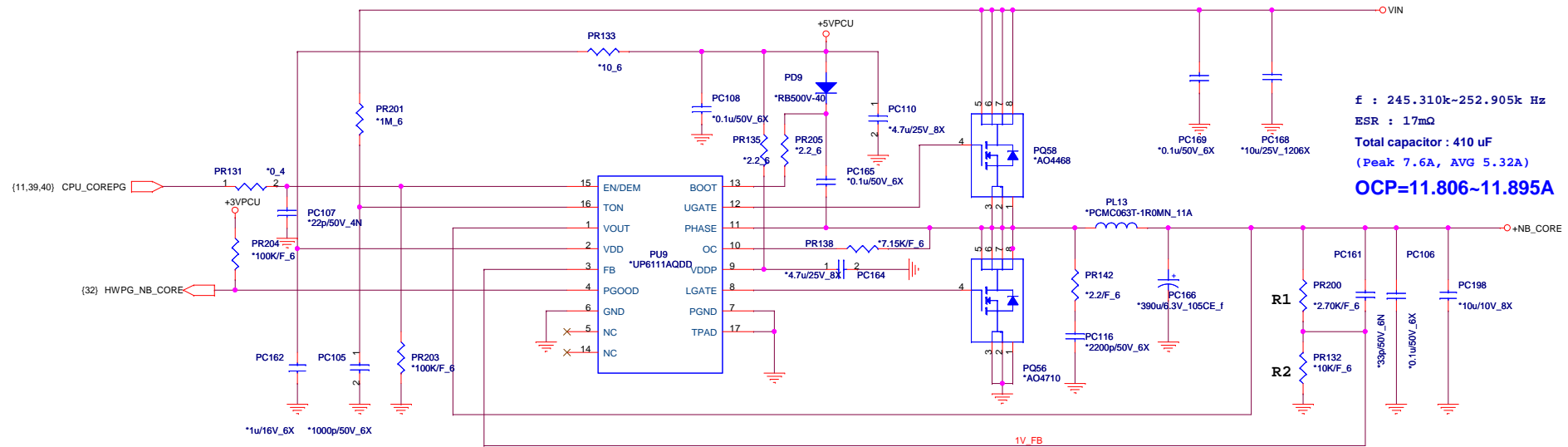


http://laptopblue.vni/

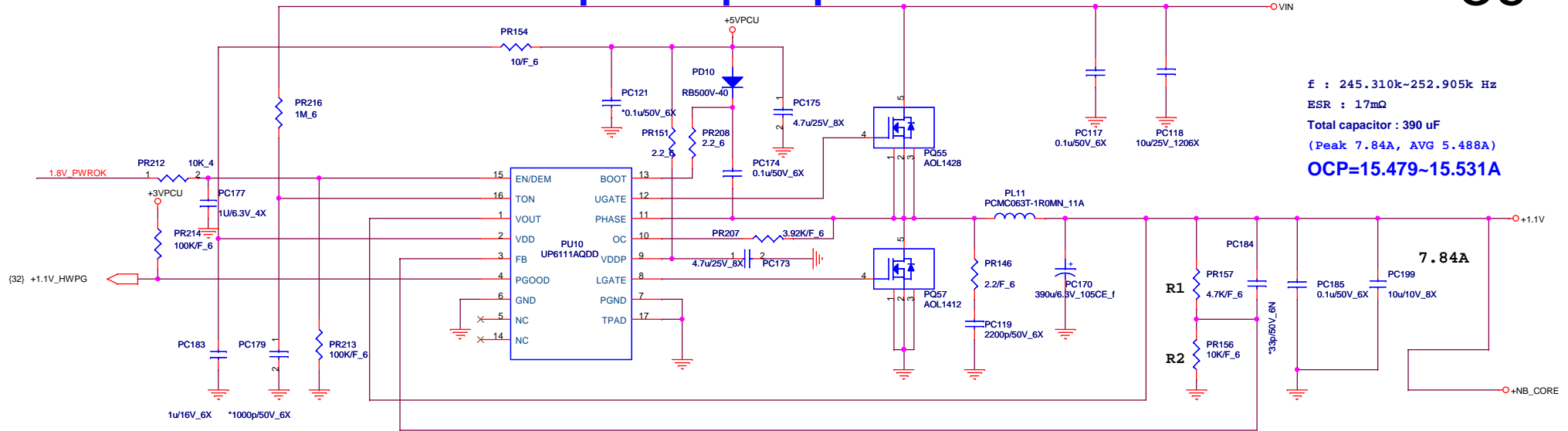


35





$V_{out} = 0.75 * [1 + (R1 + R2)]$
 $T_{on} = 3.85p * R_{ton} * V_{out} / (V_{in} - 0.5)$ $F = V_{out} / (V_{in} * T_{on})$
AO4710 $R_{dson} = 14.2m\Omega$.max.
Ripple current = $((V_{in} - V_o) / F * L) * (V_o / V_{in})$
OCP = $(R_{imax} * 20uA / L_{Rdson}) + (Ripple / 2)$
 $V_{out} = 0.75 * [1 + (R1 + R2)]$
R2=10KΩ, R1=2.7KΩ
So, $V_{in} = 19V ==>$
OCP=11.895A;
 $V_{in} = 9V ==>$
OCP=11.806A



$$V_{out} = 0.75 * [1 + (R1 + R2)]$$

$$T_{on} = 3.85p * R_{ton} * V_{out} / (V_{in} - 0.5) \quad F = V_{out} / (V_{in} * T_{on})$$

$$A04710 \quad R_{dson} = 14.2m\Omega \cdot \text{max.}$$

$$\text{Ripple current} = ((V_{in} - V_o) / f * L) * (V_o / V_{in})$$

$$OCP = (R_{imax} * 20uA / L_{rdson}) + (\text{Ripple} / 2)$$

$$V_{out} = 0.75 * [1 + (R1 + R2)]$$

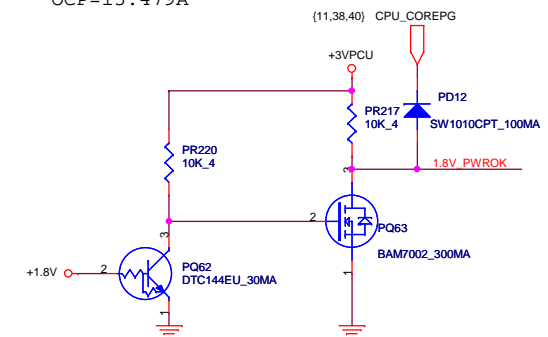
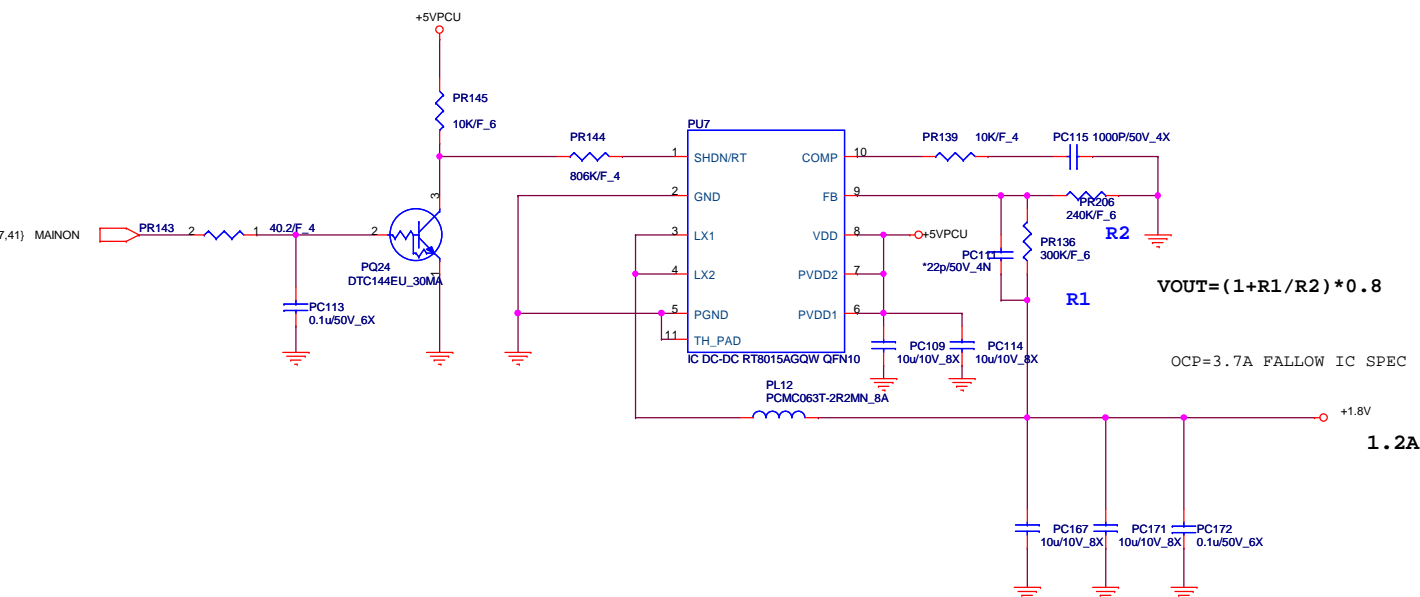
$$R2 = 10K\Omega, R1 = 4.7K\Omega$$

$$\text{So, } V_{in} = 19V \Rightarrow$$

$$OCP = 15.531A;$$

$$V_{in} = 9V \Rightarrow$$

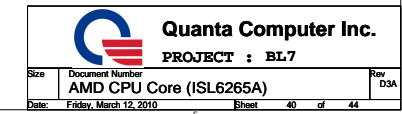
$$OCP = 15.479A$$

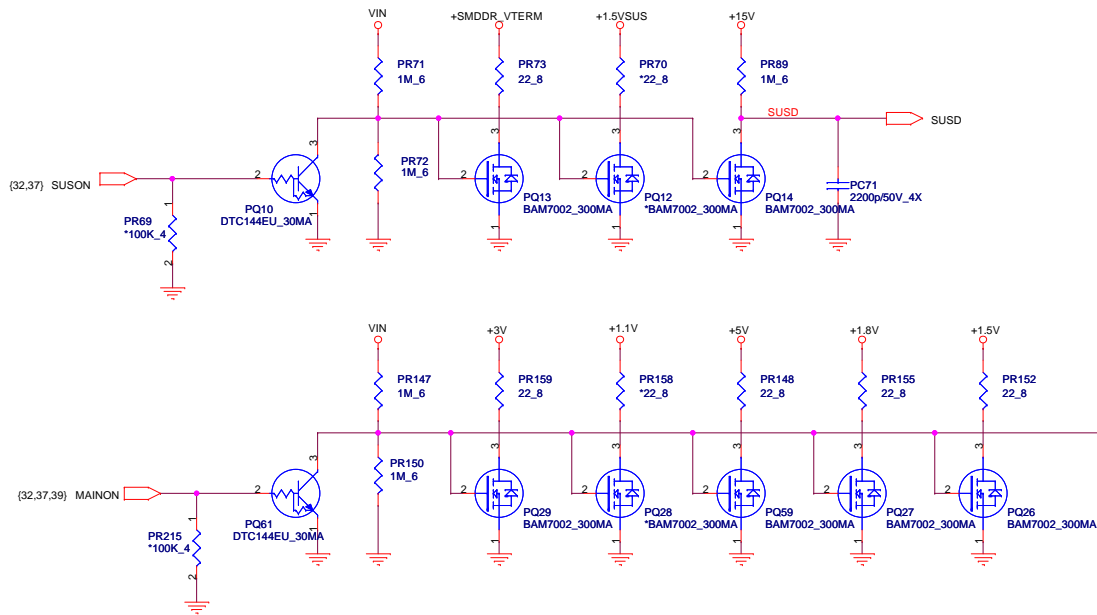
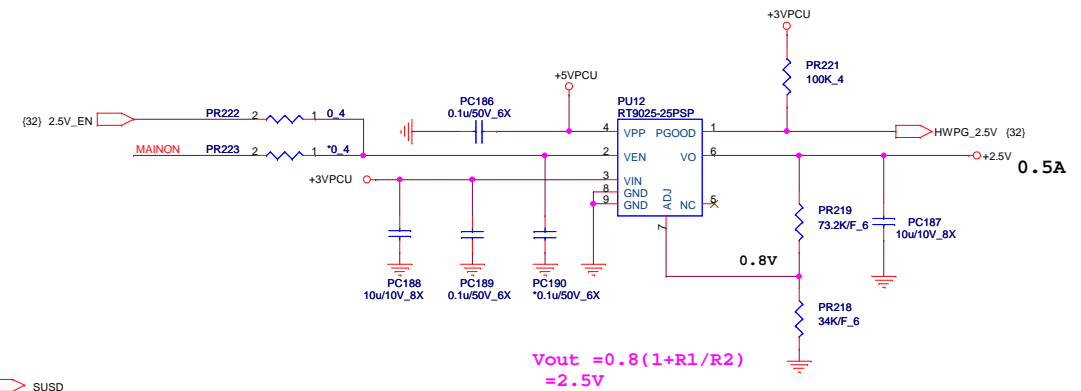
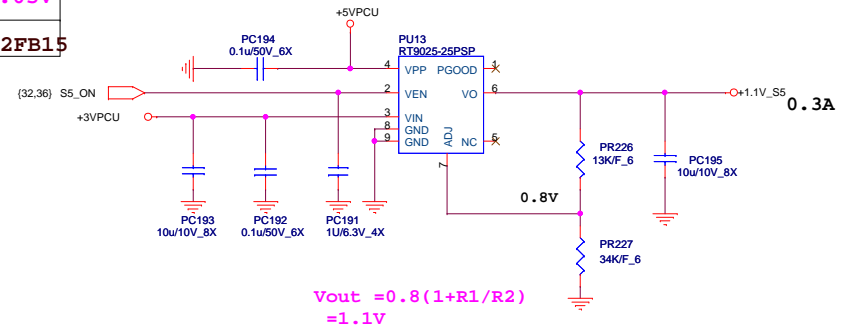


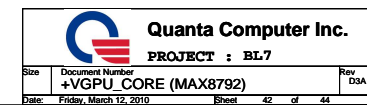
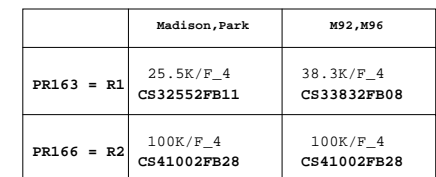
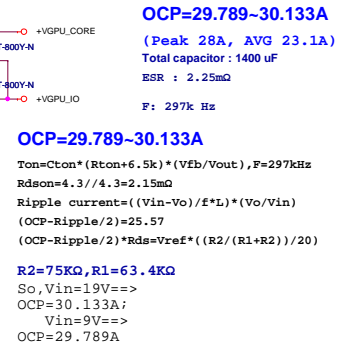
Metal VID Codes

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8







Model		REV	CHANGE LIST		MODEL		BL7		
			PAGE	FROM	To				
BL7 MB	B1B	PAGE 2 : Change RP18 Value and Add R722 for VGA SKU,Change RP20 Value for 3G,and change R187 to SEL_HT66	1	1A	1B				
		PAGE 3 : Mount R24,and Add Q58,R639,D47 and del R372,R33,Q5 for VGA Therm Detec	2	1A	1B				
		PAGE 6 : Mount C78,C113,C569,C570,C28 for EMI request	3	1A	1B				
		PAGE 11 : Add Board ID7 and Board ID8 and R644,R645,R646, and del R136 and change R578,R575,R559 for AMD suggestion	4	1A	1B				
		PAGE 14 : Mount R573 and Del R572 for Gen I mode	5	1A	1B				
		PAGE 18 : Change CTR port for Madison,Park,M92,M96 co-lay	6	1A	1B				
		PAGE 19 : Change R546 value to 51 ohm port for Madison,Park,M92,M96 co-lay	7	1A	1B				
		PAGE 22 : Delete reserve C423,C429,C427,C417,C430,C433,C422,C390,C409,C361,C376,C362,C378,C348,C349,C385,C374,C340,C352,C367,C350 for layout placement	8	1A	1B				
		PAGE 22 : Add L73,L74,C896,C897,R723,R724,L72,R713,R711,R712R709 for Madison,Park,M92,M96 co-lay	9	1A	1B				
		PAGE 23 : Add R714,R715,R716 for Madison,Park,M92,M96 co-lay	10	1A	1B				
		PAGE 24 : Add U0,R720,R721,C895,R717 for Madison,Park,M92,M96 co-lay	11	1A	1B				
		PAGE 25 : Change R1&R2 to bead for EMI request	12	1A	1B				
		PAGE 26 : Add Q67,R735,R732,R736 for WLAN & BT Combo Module	13	1A	1B				
		PAGE 27 : Del F2	14	1A	1B				
		PAGE 30 : Add R636,R637,R635,R729,Q59,R734,R725,C899,C900,C619 for non over clocking	15	1A	1B				
		PAGE 32 : Add R718,R719 for 3 cell Battery protect	16	1A	1B				
		PAGE 33 : Add R222,R651,R652,R653 for EMI request	17	1A	1B				
		PAGE 39 : Change PR207 to 3.92Kohm for OCP setting	18	1A	1B				
		PAGE 39 : change PQ55,PQ57 footprint for higher current requirement	19	1A	1B				
		PAGE 39 : Add PC199 for EMI	20	1A	1B				
			21	1A	1B				
			22	1A	1B				
			23	1A	1B				
			24	1A	1B				
			25	1A	1B				
		26	1A	1B					
		27	1A	1B					
	C3A	PAGE 2 : Change RP13,RP14,RP15,RP16,RP17,RP21 to shortpad,RP22,And Change CLKREQ3#/CLKREQ4# netname to PCIE_CLK_REQ4#/PCIE_CLK_REQ3#	28	1A	1B				
		PAGE 3 : Change R22,R90,R105,R120,R359,R34,R93,R42,R45 to shortpad,And Change T9,T10 Footprint and change R28 value,and mount R372,Q58,And del D25,D47,R368,R373,Q27,CN5,and Add Q65	29	1A	1B				
		PAGE 7 : Change C594,C593 value	30	1A	1B				
		PAGE 8 : Change R412,R402,R394,R423,R436,R413,R122 to shortpad	31	1A	1B				
		PAGE 9 : Change R64,R75,L1,L5,L7,R87 to shortpad	32	1A	1B				
		PAGE 10 : Change C843,C863,C870,C881 Value,and change R539 to shortpad	33	1A	1B				
		PAGE 11 : Add R659 and change R247,R250,R141,R138 to shortpad,and mount R139,and del C885,U29	34	1A	1B				
		PAGE 13 : Change R256,R262,R313,R310,R281,L42,L39 to shortpad	35	1A	1B				
		PAGE 16 : Del R523,R519,R514,R508,R504,R496,R530,R527,R259,R260, and Add RN34,RN35,RN36,RN37,R496,R504,R508,R514 for EMI	36	1A	1B				
		PAGE 17 : Change R100 to shortpad	37	1A	1B				
		PAGE 18 : Change R464,R445 to shortpad	38	1A	1B				
		PAGE 24 : Change R717 to 0 ohm	39	1A	1B				
		PAGE 25 : Change R347,R348,L43 to shortpad ,and mount Q55,Q57,and change R633 value and add D46 and del D45	40	1A	1B				
		PAGE 26 : Change R192,R193 to shortpad	41	1A	1B				
		PAGE 27 : Del C301	42	1A	1B				
		PAGE 28 : Change R383 and R489 to shortpad	43	1A	1B				
		PAGE 30 : Change R390,R382,R389,R381, and change C197,C198,R65,R59 Value	44	1A	1B				
		PAGE 31 : Change R480,R522,R242 to shortpad	45	1A	1B				
PAGE 32 : Add R727,and change R174,R181,R202 to shortpad,and change C355,C380 value,and reverse R658									
PAGE 33 : Change R94,R81,R654,R655 to shortpad									
PAGE 35 : Add PC202,PC203,PC204,PC205,PC201 for EMI									
PAGE 36 : CChange PR108 footprint to shortpad									
PAGE 37 : Change PQ43,PQ44 Value									
PAGE 39 : Change PQ55,PQ57,PR144,PL12,PR139 Value									
PAGE 40 : Change PL3,PQ41,PQ39,PQ40,PQ37,PQ38 Value,and Add PC206									
PAGE 41 : Reverse PR70,PQ12,PQ158,PQ28,PR149,PQ25									
D3A	PAGE 11 : Reverse R163 and change R584,R579,R576 Value to 0_4								
	PAGE 12 : Reverse R534,Y6,C817,C808								
	PAGE 13 : Reverse C904,C905								
	PAGE 16 : Add F2 for HDMI Safety issue								
	PAGE 27 : Reverse C23 and C340								
	PAGE 29 : Add R660,R661,R662								
	PAGE 34 : Change R335,R312,R338,R632,R325 value to 1.5K_4 for LED lightness issue								
DOC NO. 204		PROJECT MODEL : PART NUMBER:	BL7 31BL7MB0010	APPROVED BY: DRAWING BY:	Eric Lai Eric Lai	DATE: REVISION:	2010/03/11 D3A	Quanta Computer Inc. PROJECT : BL7	
						Size Document Number EE change list		Rev D3A	