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P. Leader	Check by	Design by

PCB P/N:

1P-0065102-80SA - FUBAI

1P-0065201-80SA - NANYA

1P-0065503-80SA - HANNSTAR

Project Code & Schematics Subject: MS60-L Main Board

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ***Index Page***

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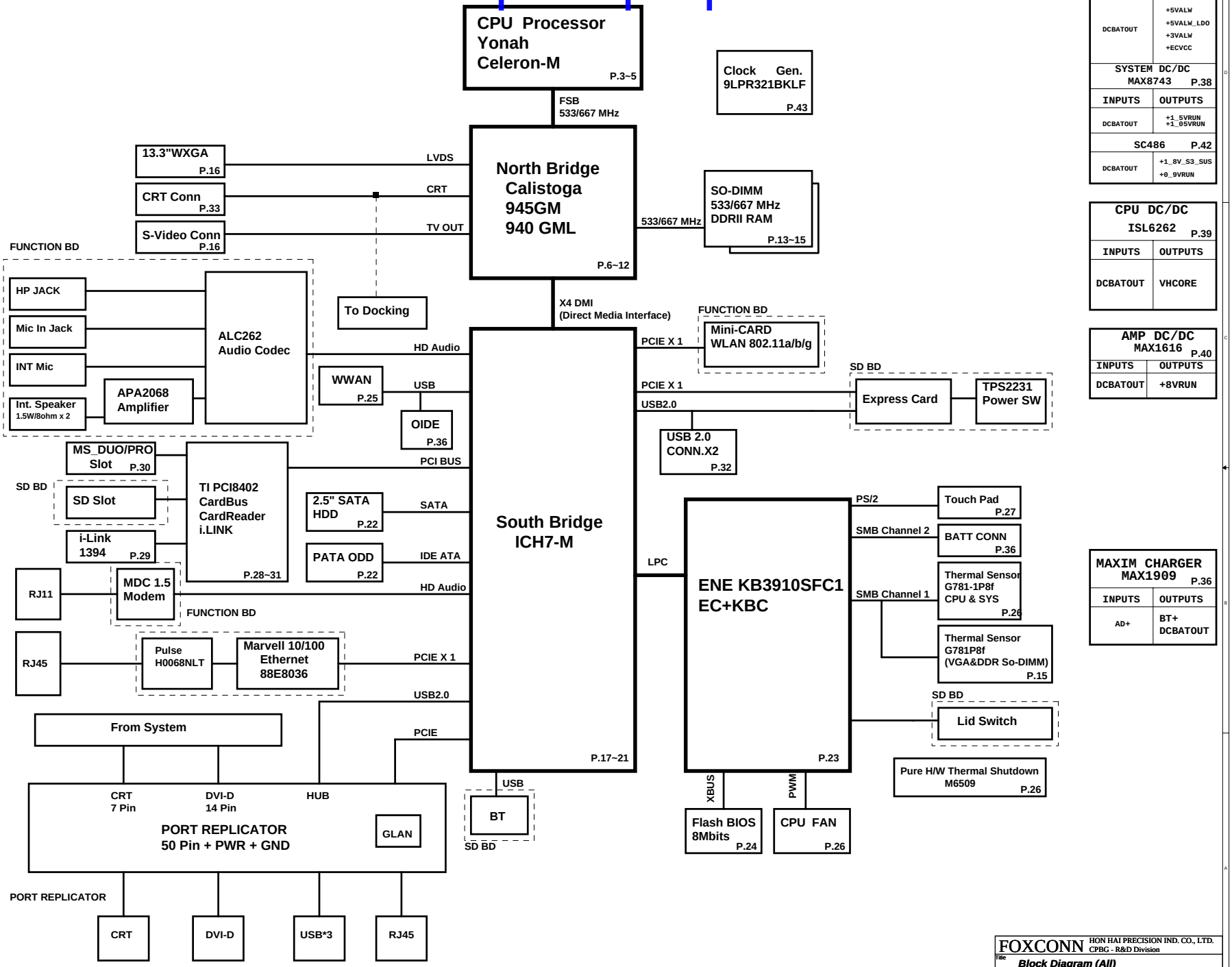
MS60 (CALISTOGA GM Block Diagram)



SYSTEM DC/DC MAX8734 P.37

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC MAX8743 P.38

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SC486 P.42

DCBATOUT	+1_8V_S3_SUS +0_9VRUN

CPU DC/DC ISL6262 P.39

INPUTS	OUTPUTS
DCBATOUT	VHCORE

AMP DC/DC MAX1616 P.40

INPUTS	OUTPUTS
DCBATOUT	+8VRUN

MAXIM CHARGER MAX1909 P.36

INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

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Title: *Block Diagram (All)*

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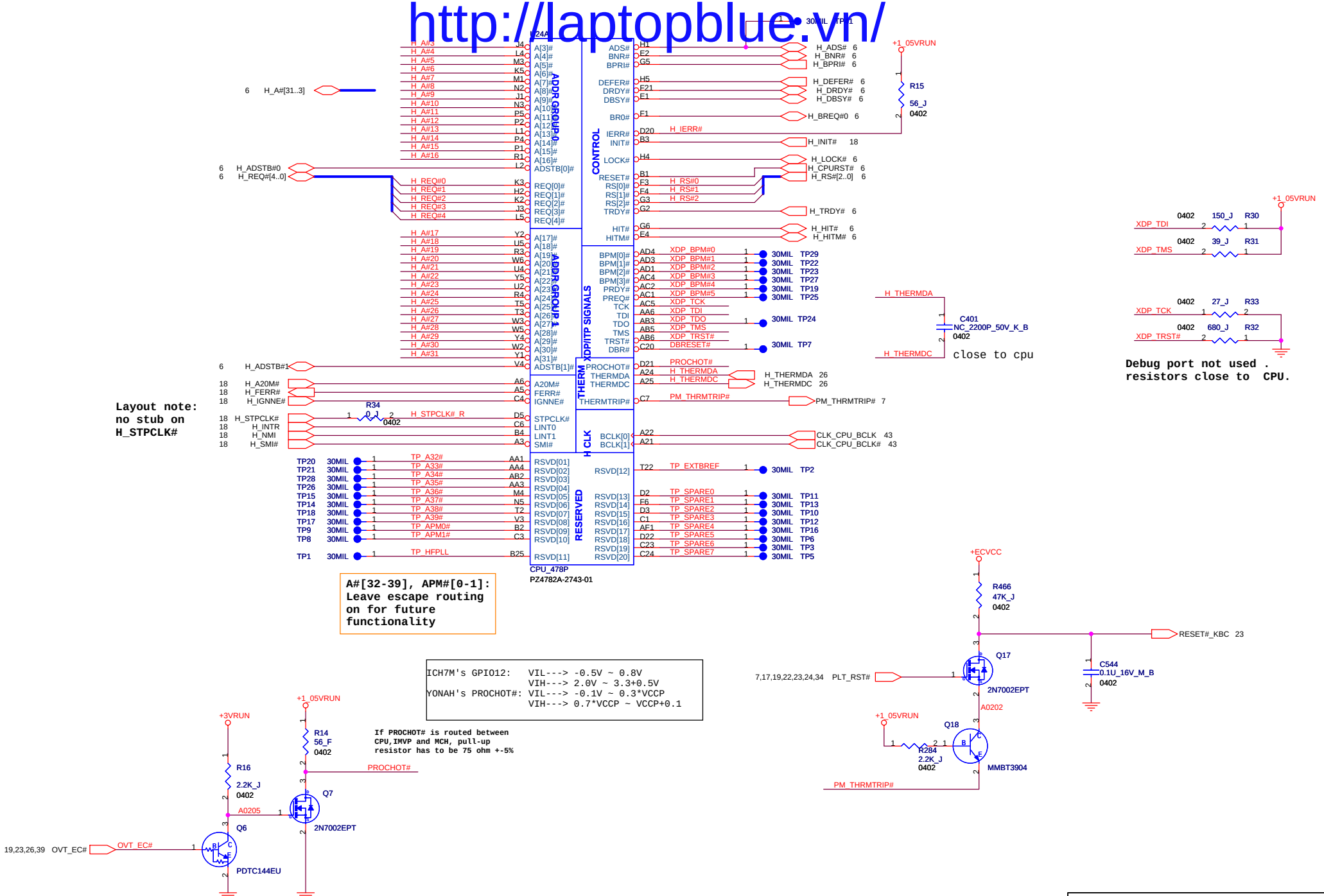

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*Yonah (HOST BUS) 1/3*
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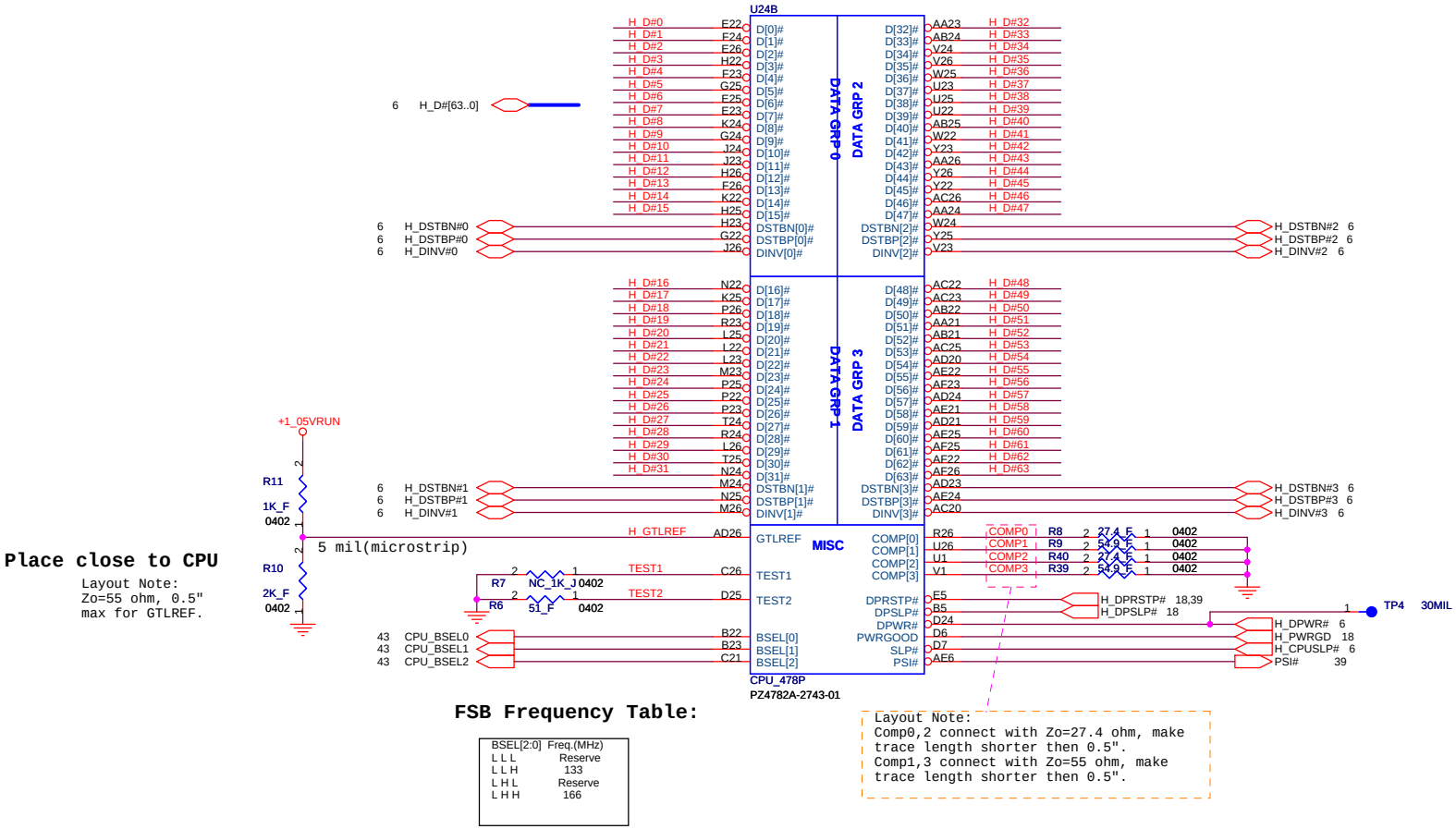

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Yonah (HOST BUS) 2/3
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CPU_VCCA---->130mA
CPU_VCCP----->2.5A
CPU_VCC------>36A for Yona
44A for Merom

maximum current is 130mA for CPU_VCCA in Merom and 600A/us slew rate for CPU_VCCA

Same Length

Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.

width=18 mil
spacing=7 mil

100 mil

20 mil

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Yonah (POWER/GROUND) 3/3
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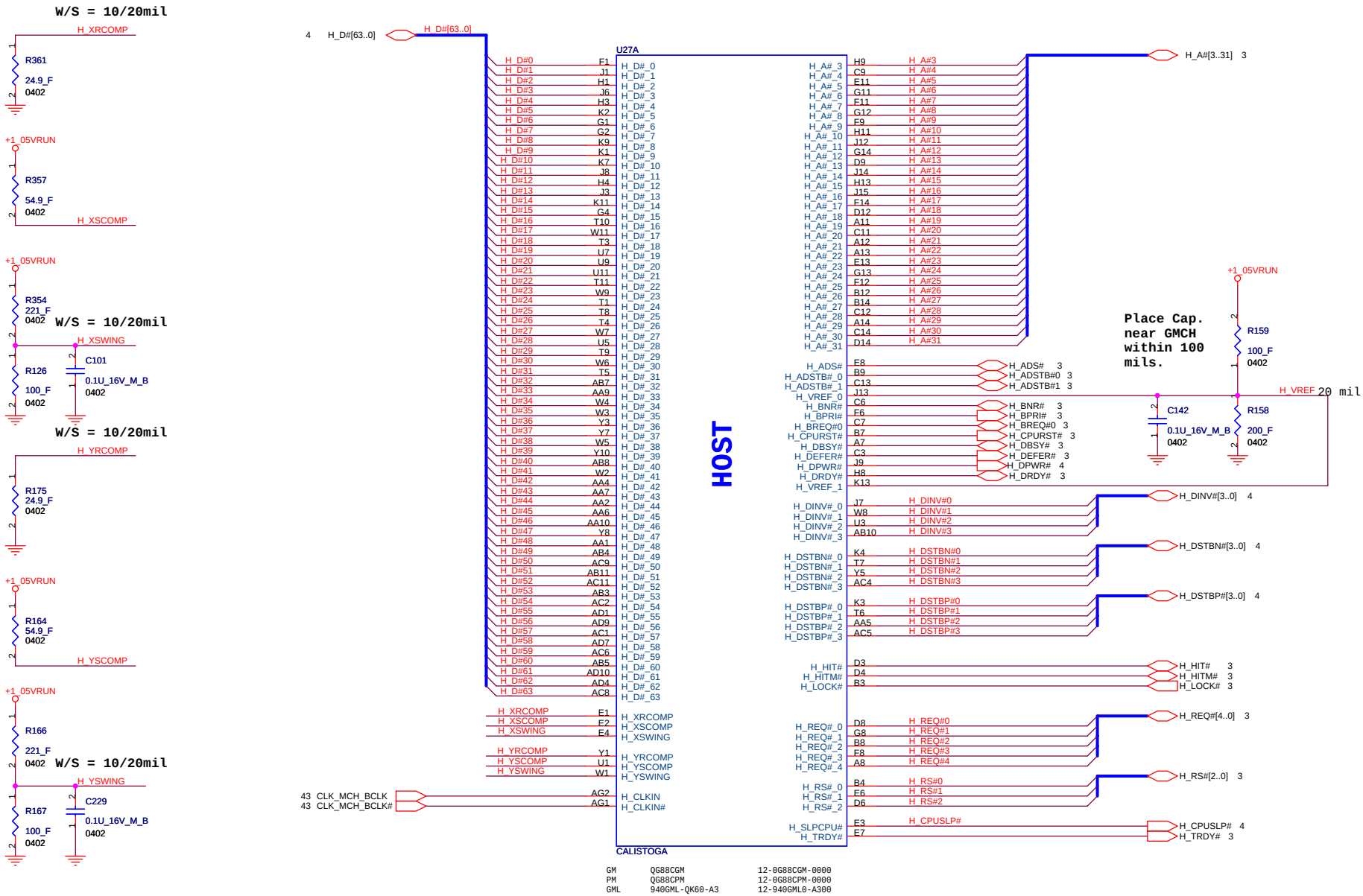

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOHA (HOST)	
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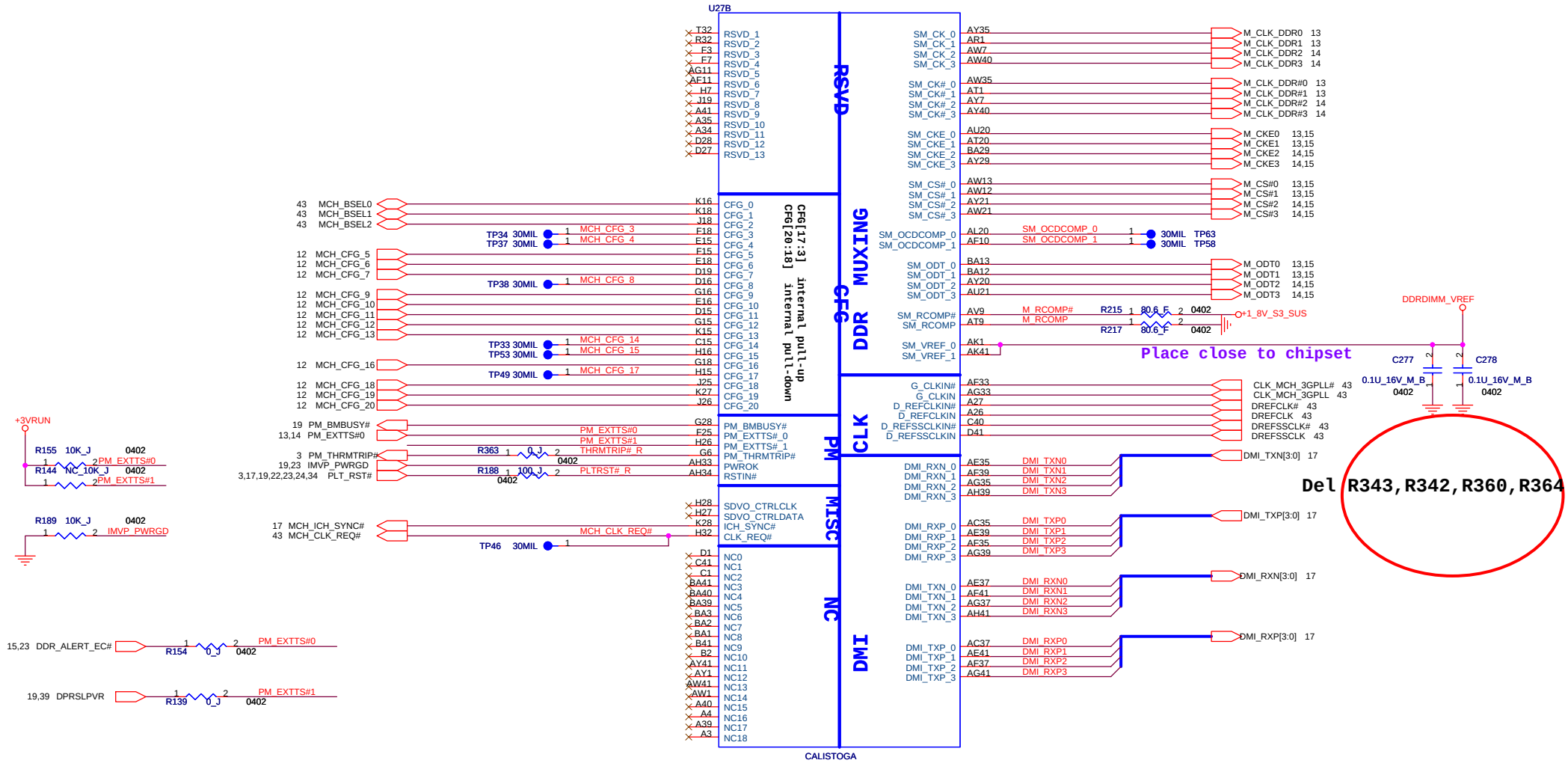

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOGA (DMI) 2 of 7	
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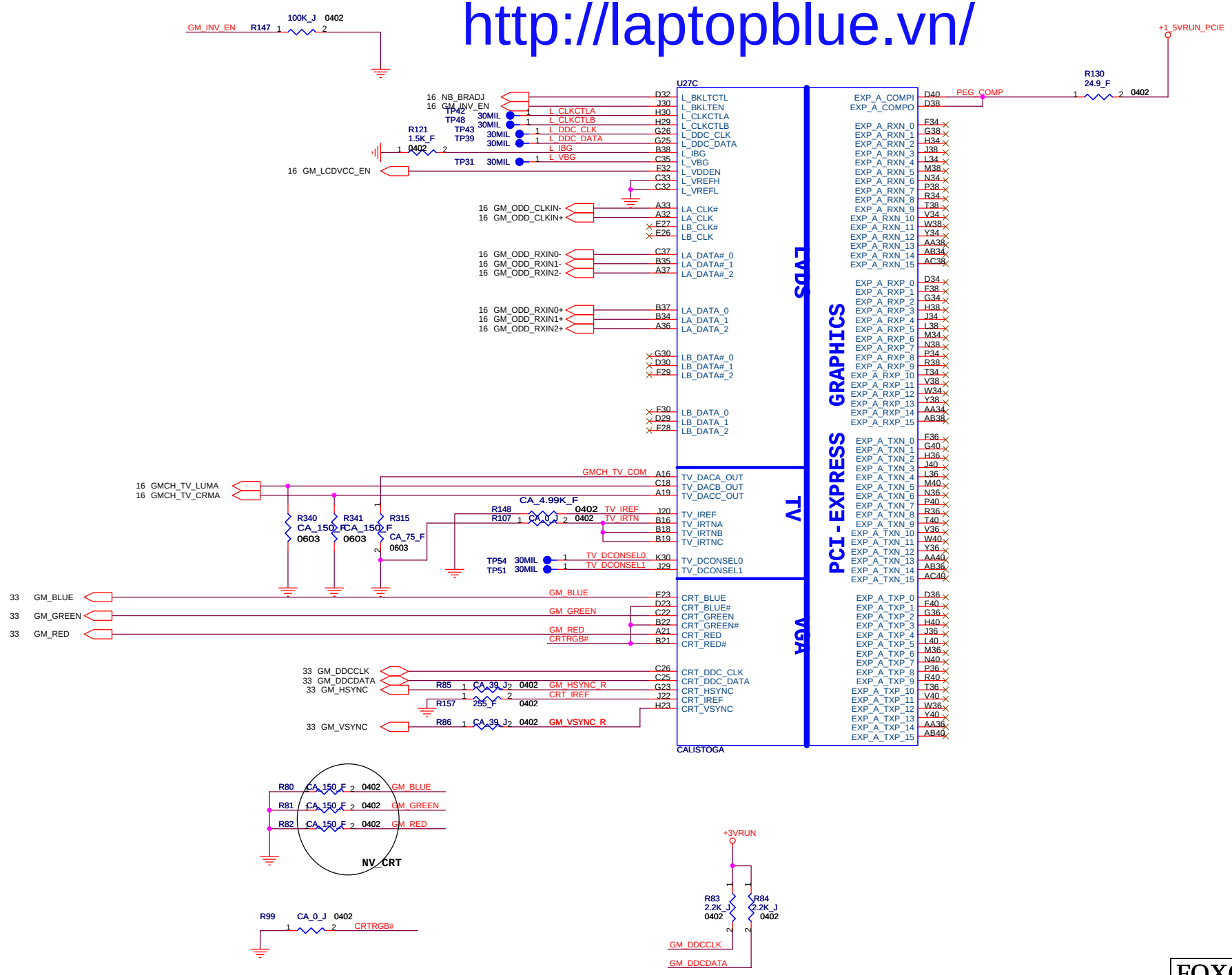

FOXCONN	HON HAI PRECISION IND. CO., LTD.
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Title	CALISTOGA (DMI) 3 of 7
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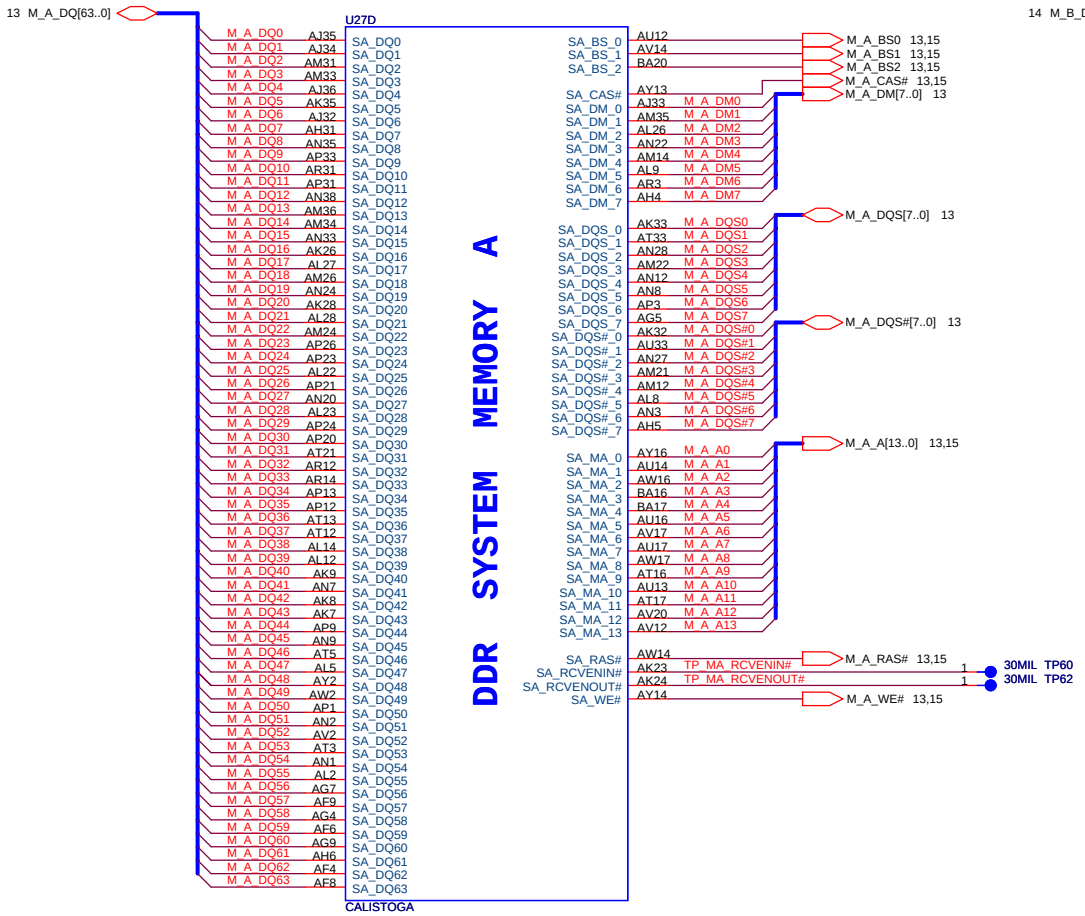

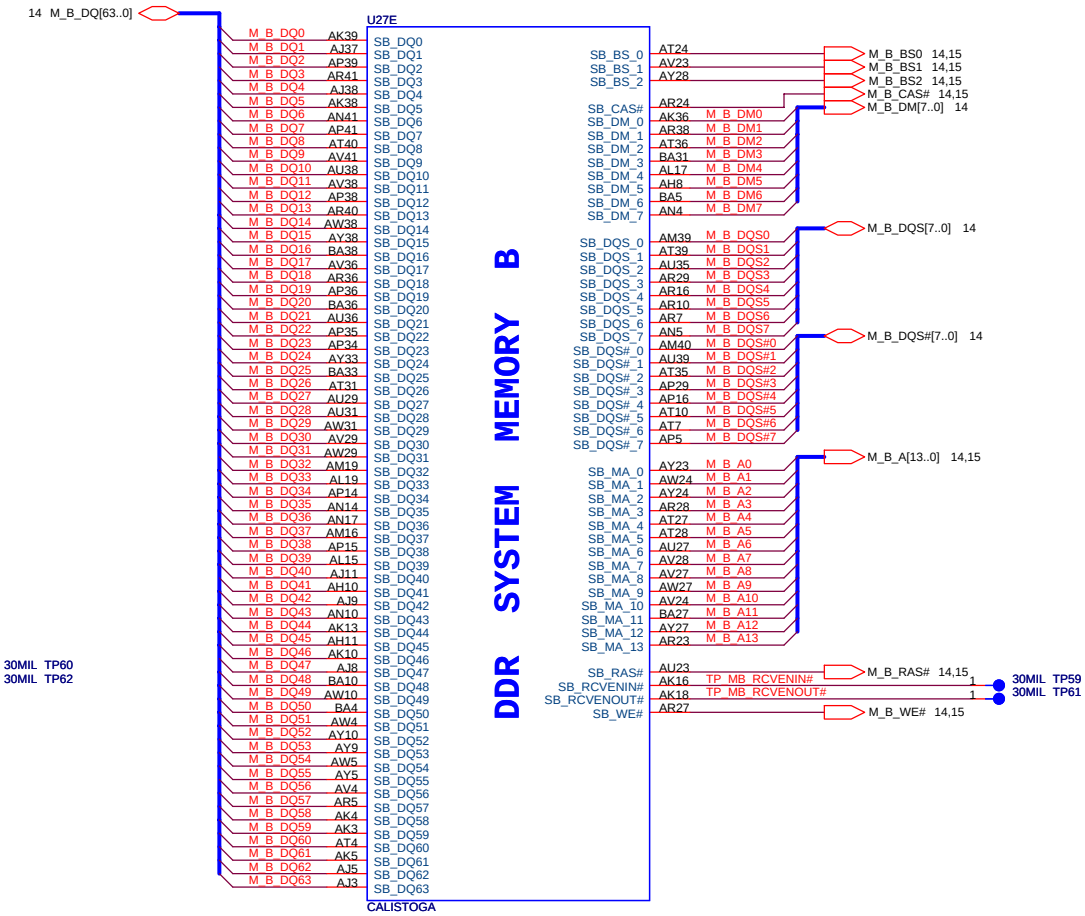

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CALISTOGA (DDRII) 4 of 7	
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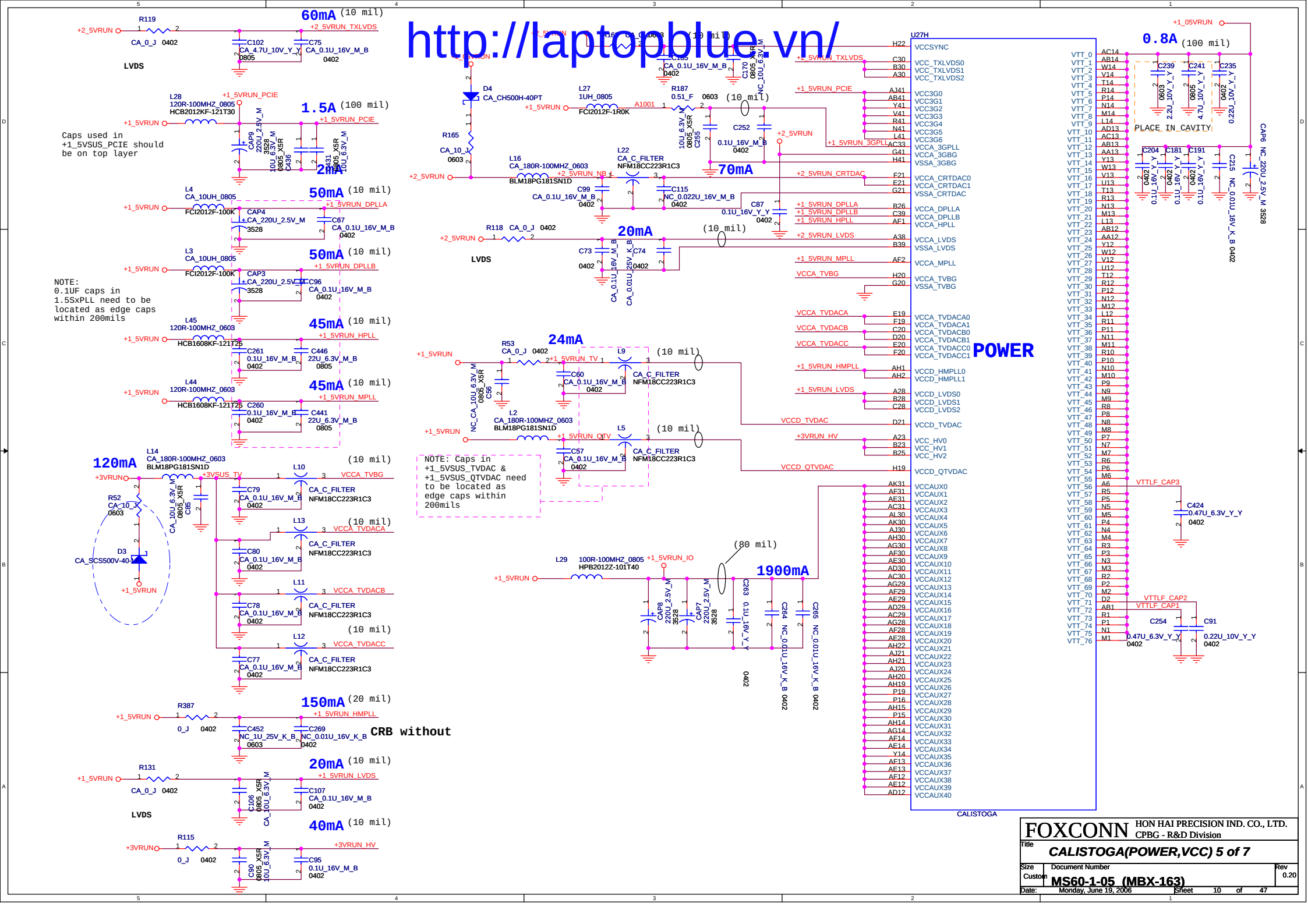

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CALISTOGA(POWER,VCC) 5 of 7
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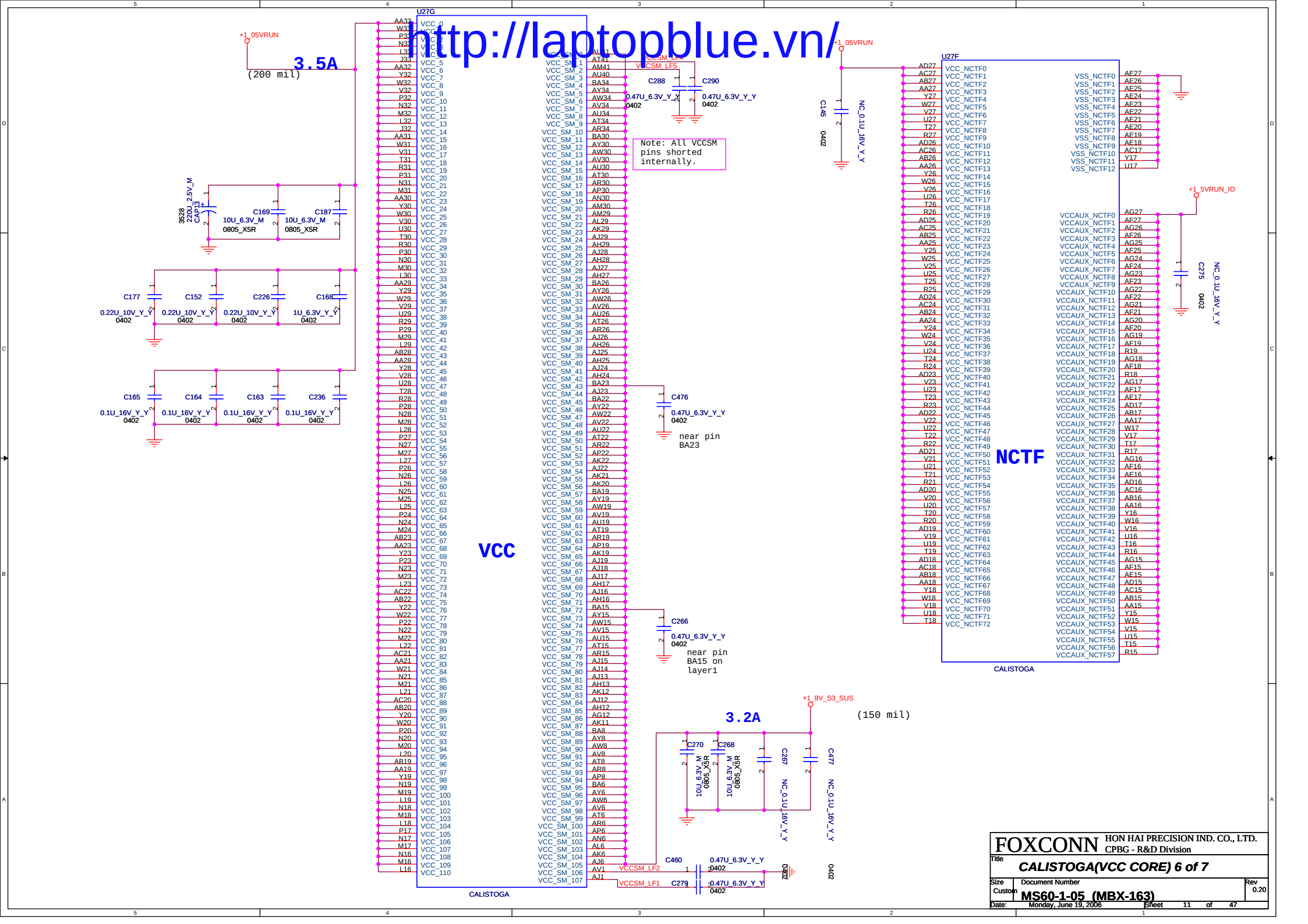

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Title: CALISTOGA(VCC CORE) 6 of 7

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7 MCH_CFG_5 — 30MIL TP45

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 — 30MIL TP40

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 — 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9 — R153 NC_2.2K_J 0402

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 — 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11 — R128 NC_2.2K_J 0402

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga

7 MCH_CFG_12 — 30MIL TP47
7 MCH_CFG_13 — 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16 — 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

+3VRUN — R156 NC_2.2K_J 0402 — 7 MCH_CFG_18

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

+3VRUN — R151 NC_2.2K_J 0402 — 7 MCH_CFG_19

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 — 30MIL TP52

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U27I — CALISTOGA

VSS

U27J — CALISTOGA

VSS

Title	
	CALISTOGA(VSS) 7 of 7
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1.8V per DIMM=3.08A

DDR2_VREF

C344 0.1U_16V_M_B 0402

C345 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS

CN25

DDR2 SO-DIMM_2x100P

FOX_AS0A426_N2RN_7F

DIMM_0

PC4800 DDR2 SDRAM SO-DIMM (200P)

1	VREF		2	VSS46			
3	VSS47		4	DQ4	M_A_DQ4		
5	DQ0	M_A_DQ0	6	DQ5	M_A_DQ5		
7	DQ1	M_A_DQ1	8	VSS15			
9	VSS37		10	DM0	M_A_DM0		
11	DQS#0	M_A_DQS#0	12	VSS5			
13	DQS0	M_A_DQS0	14	DQ6	M_A_DQ6		
15	VSS48		16	DQ7	M_A_DQ7		
17	DQ2	M_A_DQ2	18	VSS16			
19	DQ3	M_A_DQ3	20	DQ12	M_A_DQ12		
21	VSS38		22	DQ13	M_A_DQ13		
23	DQ8	M_A_DQ8	24	VSS17			
25	DQ9	M_A_DQ9	26	DM1	M_A_DM1		
27	VSS49		28	VSS53			
29	DQS#1	M_A_DQS#1	30	CK0	M_CLK_DDR0	7	
31	DQS1	M_A_DQS1	32	CK0#	M_CLK_DDR#0	7	
33	VSS39		34	VSS41			
35	DQ10	M_A_DQ10	36	DQ14	M_A_DQ14		
37	DQ11	M_A_DQ11	38	DQ15	M_A_DQ15		
39	VSS50		40	VSS54			
41	VSS18		42	VSS20			
43	DQ16	M_A_DQ16	44	DQ20	M_A_DQ20		
45	DQ17	M_A_DQ17	46	DQ21	M_A_DQ21		
47	VSS1		48	VSS6			
49	DQS#2	M_A_DQS#2	50	NC3	DDR2_EXTTS#0	1	R469 NC_0_J 0402 2 PM_EXTTS#0 7,14
51	DQS2	M_A_DQS2	52	DM2	M_A_DM2		
53	VSS19		54	VSS21			
55	DQ18	M_A_DQ18	56	DQ22	M_A_DQ22		
57	DQ19	M_A_DQ19	58	DQ23	M_A_DQ23		
59	VSS22		60	VSS24			
61	DQ24	M_A_DQ24	62	DQ28	M_A_DQ28		
63	DQ25	M_A_DQ25	64	DQ29	M_A_DQ29		
65	VSS23		66	VSS25			
67	DM3	M_A_DM3	68	DQS#3	M_A_DQS#3		
69	NC4		70	DQS3	M_A_DQS3		
71	VSS9		72	VSS10			
73	DQ26	M_A_DQ26	74	DQ30	M_A_DQ30		
75	DQ27	M_A_DQ27	76	DQ31	M_A_DQ31		
77	VSS4		78	VSS8			
79	CKE0	7,15 M_CKE0	80	CKE1	M_CKE1	7,15	
81	VDD7		82	VDD8			
83	NC1		84	A15			
85	A16_BA2	9,15 M_A_BS2	86	A14			
87	VDD9		88	VDD11			
89	A12	M_A_A12	90	A11	M_A_A11		
91	A9	M_A_A9	92	A7	M_A_A7		
93	A8	M_A_A8	94	A6	M_A_A6		
95	VDD5		96	VDD4			
97	A5	M_A_A5	98	A4	M_A_A4		
99	A3	M_A_A3	100	A2	M_A_A2		
101	A1	M_A_A1	102	A0	M_A_A0		
103	VDD10		104	VDD12			
105	A10/AP	M_A_A10	106	BA1	M_A_BS1	9,15	
107	BA0	9,15 M_A_BS0	108	RAS#	M_A_RAS#	9,15	
109	WE#	9,15 M_A_WE#	110	S0#	M_CS#0	7,15	
111	VDD2		112	VDD1			
113	CAS#	9,15 M_A_CAS#	114	ODT0	M_ODT0	7,15	
115	S1#	7,15 M_CS#1	116	A13	M_A_A13		
117	VDD3		118	VDD6			
119	ODT1	7,15 M_ODT1	120	NC2			
121	VSS11		122	VSS12			
123	DQ32	M_A_DQ32	124	DQ36	M_A_DQ36		
125	DQ33	M_A_DQ33	126	DQ37	M_A_DQ37		
127	VSS26		128	VSS28			
129	DQS#4	M_A_DQS#4	130	DM4	M_A_DM4		
131	DQS4	M_A_DQS4	132	VSS42			
133	VSS2		134	DQ38	M_A_DQ38		
135	DQ34	M_A_DQ34	136	DQ39	M_A_DQ39		
137	DQ35	M_A_DQ35	138	VSS55			
139	VSS27		140	DQ44	M_A_DQ44		
141	DQ40	M_A_DQ40	142	DQ45	M_A_DQ45		
143	DQ41	M_A_DQ41	144	VSS43			
145	VSS29		146	DQS#5	M_A_DQS#5		
147	DM5	M_A_DM5	148	DQS5	M_A_DQS5		
149	VSS51		150	VSS56			
151	DQ42	M_A_DQ42	152	DQ46	M_A_DQ46		
153	DQ43	M_A_DQ43	154	DQ47	M_A_DQ47		
155	VSS40		156	VSS44			
157	DQ48	M_A_DQ48	158	DQ52	M_A_DQ52		
159	DQ49	M_A_DQ49	160	DQ53	M_A_DQ53		
161	VSS52		162	VSS57			
163	NCTEST		164	CK1	M_CLK_DDR1	7	
165	VSS30		166	CK1#	M_CLK_DDR#1	7	
167	DQS#6	M_A_DQS#6	168	VSS45			
169	DQS6	M_A_DQS6	170	DM6	M_A_DM6		
171	VSS31		172	VSS32			
173	DQ50	M_A_DQ50	174	DQ54	M_A_DQ54		
175	DQ51	M_A_DQ51	176	DQ55	M_A_DQ55		
177	VSS33		178	VSS35			
179	DQ56	M_A_DQ56	180	DQ60	M_A_DQ60		
181	DQ57	M_A_DQ57	182	DQ61	M_A_DQ61		
183	VSS3		184	VSS7			
185	DM7	M_A_DM7	186	DQS#7	M_A_DQS#7		
187	VSS34		188	DQS7	M_A_DQS7		
189	DQ58	M_A_DQ58	190	VSS36			
191	DQ59	M_A_DQ59	192	DQ62	M_A_DQ62		
193	VSS14		194	DQ63	M_A_DQ63		
195	SDA	14,19,34,43 SMB_DATA_SB	196	VSS13			
197	SCL	14,19,34,43 SMB_CLK_SB	198	SA0	SA0_DIM0		R471 10K_J 1 0402 2
199	VDD(SPD)	+3VRUN	200	SA1	SA1_DIM0		R470 10K_J 1 0402 2
201	GND1		202	GND2			
203	NPTH1		204	NPTH2			

C523 2.2U_10V_Y_Y 0603

C517 0.1U_16V_M_B 0402

SMBus Address: A0(W)/A1(R)

M_A_DM[0..7] 9
M_A_DQ[0..63] 9
M_A_DQS[0..7] 9
M_A_DQS#[0..7] 9
M_A_A[0..13] 9,15

DDRDIMM_VREF +1_8V_S3_SUS

R287 0_J 0402

R286 NC_10K_F 0402

DDR2_VREF

(20 mil)

C364 0.1U_16V_M_B 0402

R288 NC_10K_F 0402

Close to DIMM

Place these Caps near So-Dimm0.

+1_8V_S3_SUS

C519 2.2U_10V_Y_Y 0603

C562 2.2U_10V_Y_Y 0603

C521 2.2U_10V_Y_Y 0603

C518 2.2U_10V_Y_Y 0603

C358 2.2U_10V_Y_Y 0603

Place these Caps near So-Dimm0.

+1_8V_S3_SUS

C520 0.1U_16V_Y_Y 0402

C360 0.1U_16V_Y_Y 0402

C522 0.1U_16V_Y_Y 0402

C516 0.1U_16V_Y_Y 0402

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: **DDR(II)SO-DIMM_0**

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1.8V per DIMM=3.08A

DDR2_VREF

C363 0.1U_16V_M_B 0402

C362 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS

CN26

1	VREF	VSS46	2
3	VSS47	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS15	8
9	VSS37	DM0	10
11	DQS#0	VSS5	12
13	DQS0	DQ6	14
15	VSS48	DQ7	16
17	DQ2	VSS16	18
19	DQ3	DQ12	20
21	VSS38	DQ13	22
23	DQ8	VSS17	24
25	DQ9	DM1	26
27	VSS49	VSS53	28
29	DQS#1	CK0	30
31	DQS1	CK0#	32
33	VSS39	VSS41	34
35	DQ10	DQ14	36
37	DQ11	DQ15	38
39	VSS50	VSS54	40
41	VSS18	VSS20	42
43	DQ16	DQ20	44
45	DQ17	DQ21	46
47	VSS1	VSS6	48
49	DQS#2	NC3	50
51	DQS2	DM2	52
53	VSS19	VSS21	54
55	DQ18	DQ22	56
57	DQ19	DQ23	58
59	VSS22	VSS24	60
61	DQ24	DQ28	62
63	DQ25	DQ29	64
65	VSS23	VSS25	66
67	DM3	DQS#3	68
69	NC4	DQS3	70
71	VSS9	VSS10	72
73	DQ26	DQ30	74
75	DQ27	DQ31	76
77	VSS4	VSS8	78
79	CKE0	CKE1	80
81	VDD7	VDD8	82
83	NC1	A15	84
85	A16_BA2	A14	86
87	VDD9	VDD11	88
89	A12	A11	90
91	A9	A7	92
93	A8	A6	94
95	VDD5	VDD4	96
97	A5	A4	98
99	A3	A2	100
101	A1	A0	102
103	VDD10	VDD12	104
105	A10/AP	BA1	106
107	BA0	RAS#	108
109	WE#	S0#	110
111	VDD2	VDD1	112
113	CAS#	ODT0	114
115	S1#	A13	116
117	VDD3	VDD6	118
119	ODT1	NC2	120
121	VSS11	VSS12	122
123	DQ32	DQ36	124
125	DQ33	DQ37	126
127	VSS26	VSS28	128
129	DQS#4	DM4	130
131	DQS4	VSS42	132
133	VSS2	DQ38	134
135	DQ34	DQ39	136
137	DQ35	VSS55	138
139	VSS27	DQ44	140
141	DQ40	DQ45	142
143	DQ41	VSS43	144
145	VSS29	DQS#5	146
147	DM5	DQS5	148
149	VSS51	VSS56	150
151	DQ42	DQ46	152
153	DQ43	DQ47	154
155	VSS40	VSS44	156
157	DQ48	DQ52	158
159	DQ49	DQ53	160
161	VSS52	VSS57	162
163	NCTEST	CK1	164
165	VSS30	CK1#	166
167	DQS#6	VSS45	168
169	DQS6	DM6	170
171	VSS31	VSS32	172
173	DQ50	DQ54	174
175	DQ51	DQ55	176
177	VSS33	VSS35	178
179	DQ56	DQ60	180
181	DQ57	DQ61	182
183	VSS3	VSS7	184
185	DM7	DQS#7	186
187	VSS34	DQS7	188
189	DQ58	VSS36	190
191	DQ59	DQ62	192
193	VSS14	DQ63	194
195	SDA	VSS13	196
197	SCL	SA0	198
199	VDD(SPD)	SA1	200
201	GND1	GND2	202
203	NPTH1	NPTH2	204

PC4800 DDR2 SDRAM SO-DIMM (200P)

9.2mm

DDR2 SO-DIMM_2x100P

FOX_AS0A426_NARN_7F

DIMM_1

M_B_DM[0..7] 9
M_B_DQ[0..63] 9
M_B_DQS[0..7] 9
M_B_A[0..13] 9,15

M_CLK_DDR3 7
M_CLK_DDR#3 7

M_CLK_DDR2 7
M_CLK_DDR#2 7

R509 NC_0_J 0402

PM_EXTTS#0_DIMM2 → PM_EXTTS#0 7,13

7,15 M_CKE2 → M_CKE3 7,15

9,15 M_B_BS2

9,15 M_B_BS0 → M_B_BS1 9,15

9,15 M_B_WE# → M_CS#2 7,15

9,15 M_B_CAS# / 7,15 M_CS#3

7,15 M_ODT3 → M_ODT2 7,15

M_B_A13

13,19,34,43 SMB_DATA_SB

13,19,34,43 SMB_CLK_SB

+3VRUN

SMBus Address: A4(W)/A5(R)

R508 10K_J 0402

R507 10K_J 0402

SA0_DIM1

SA1_DIM1

+3VRUN

C365 2.2U_10V_Y_Y 0603

C372 0.1U_16V_M_B 0402

Place these Caps near So-Dimm1.

+1_8V_S3_SUS

C359 2.2U_10V_Y_Y 0603

C357 2.2U_10V_Y_Y 0603

C376 2.2U_10V_Y_Y 0603

C563 2.2U_10V_Y_Y 0603

C377 2.2U_10V_Y_Y 0603

Place these Caps near So-Dimm1.

+1_8V_S3_SUS

C564 0.1U_16V_Y_Y 0402

C375 0.1U_16V_Y_Y 0402

C378 0.1U_16V_Y_Y 0402

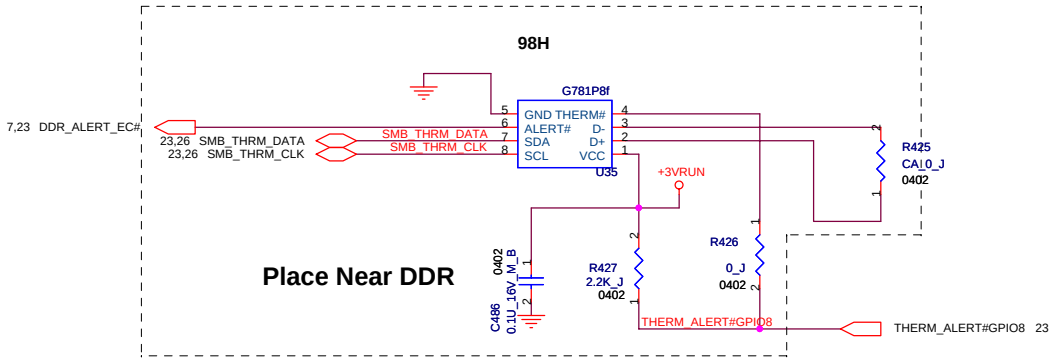
C374 0.1U_16V_Y_Y 0402

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DDR(II)SO-DIMM_1

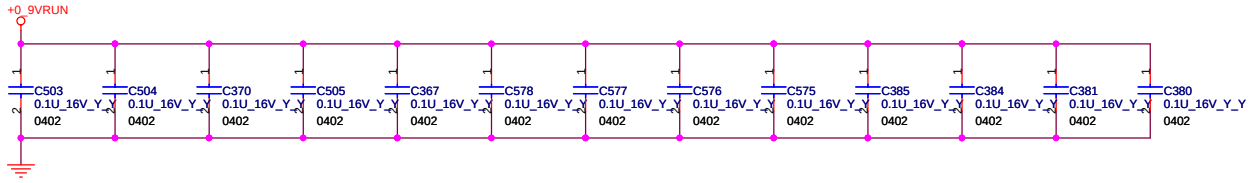
Size: Custom | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

Date: Monday, June 19, 2006 | Sheet 14 of 47

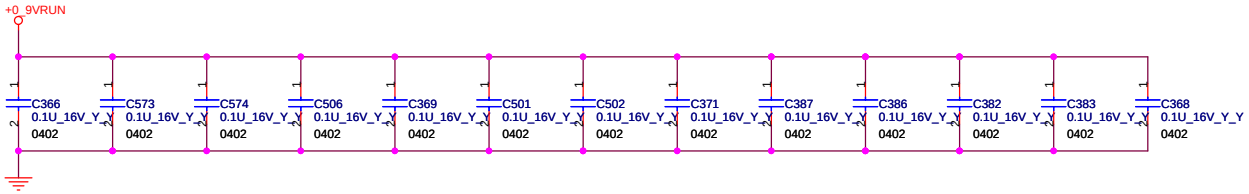


9,13 M_A_A[0..13]

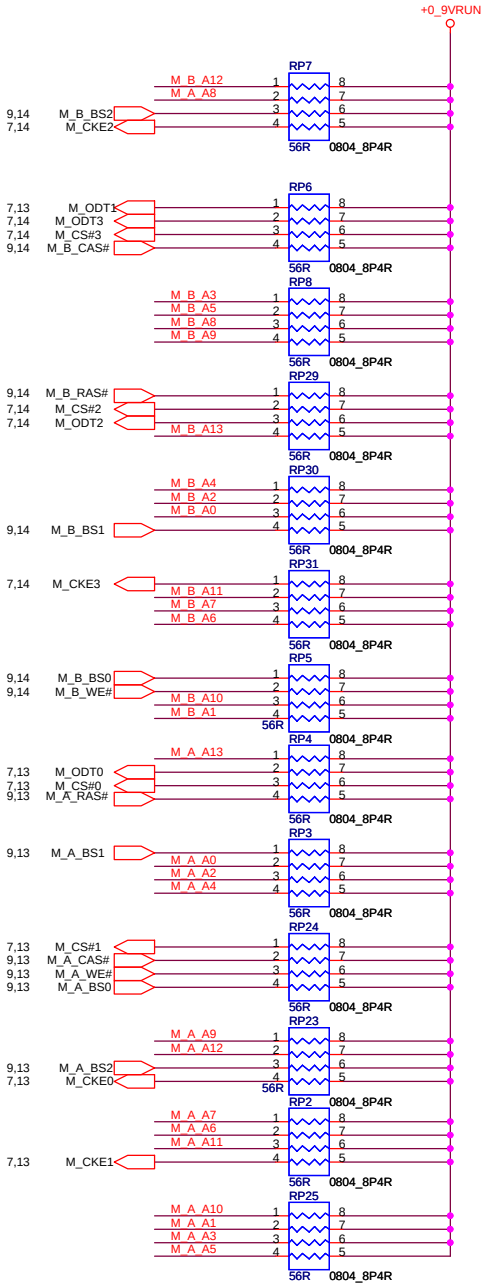
9,14 M_B_A[0..13]



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



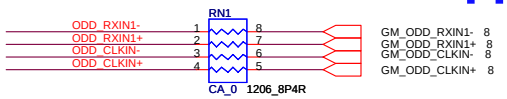
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

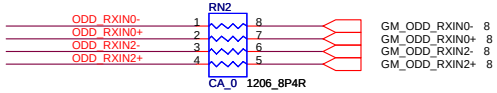
Title: ***DDR(II)Termination***

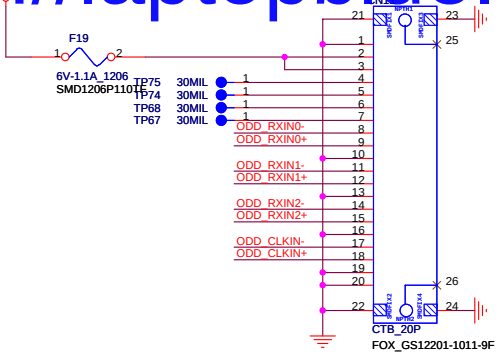
Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

Date: Monday, June 19, 2006 Sheet 15 of 47

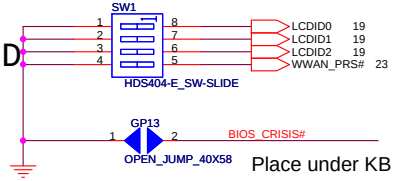
LVDS





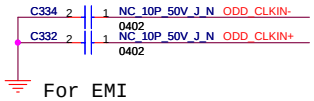


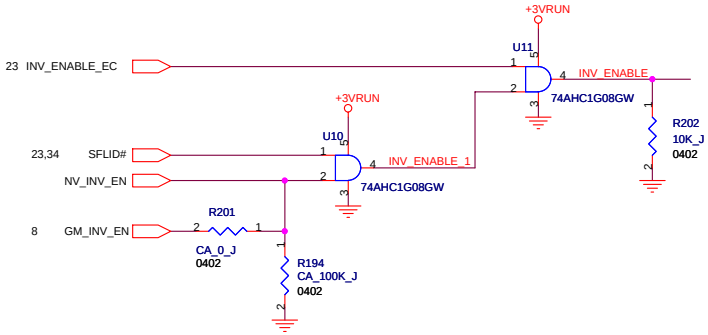
PANEL ID



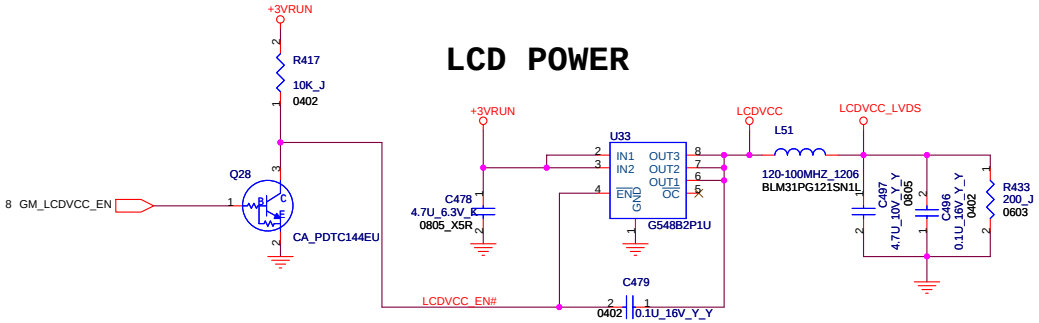
Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

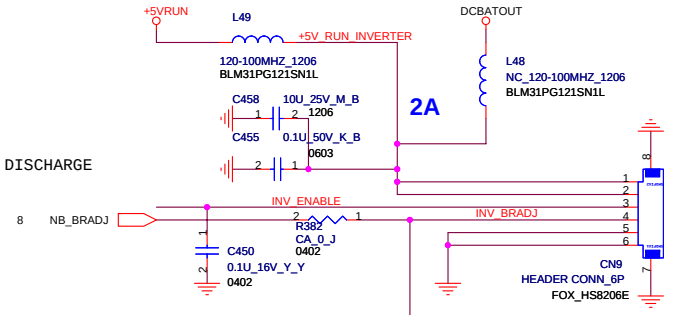
LVDS CONNECTOR



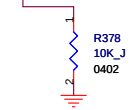


LCD POWER

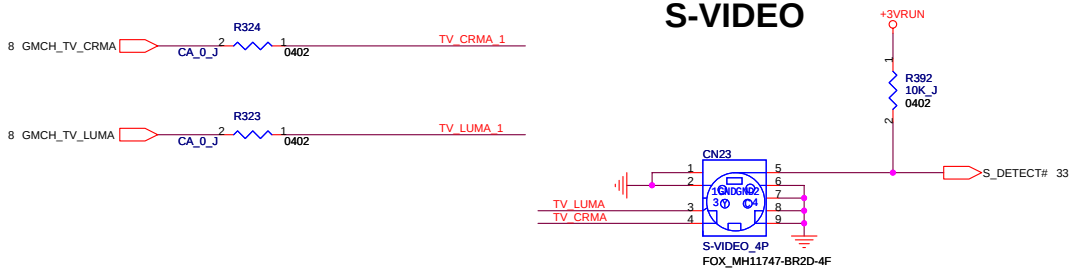


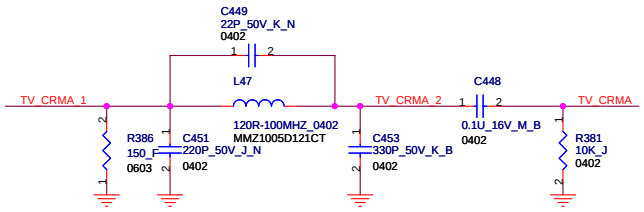


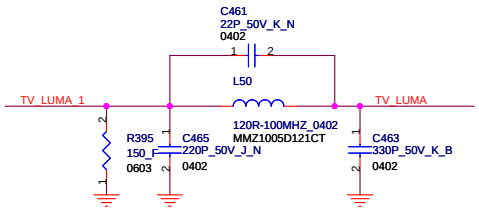
INVERTER CONNECTOR



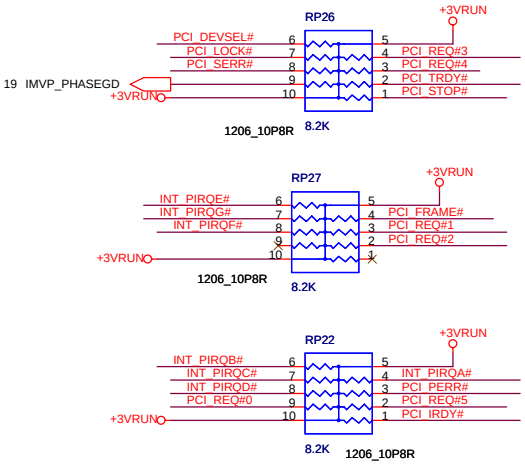
S-VIDEO



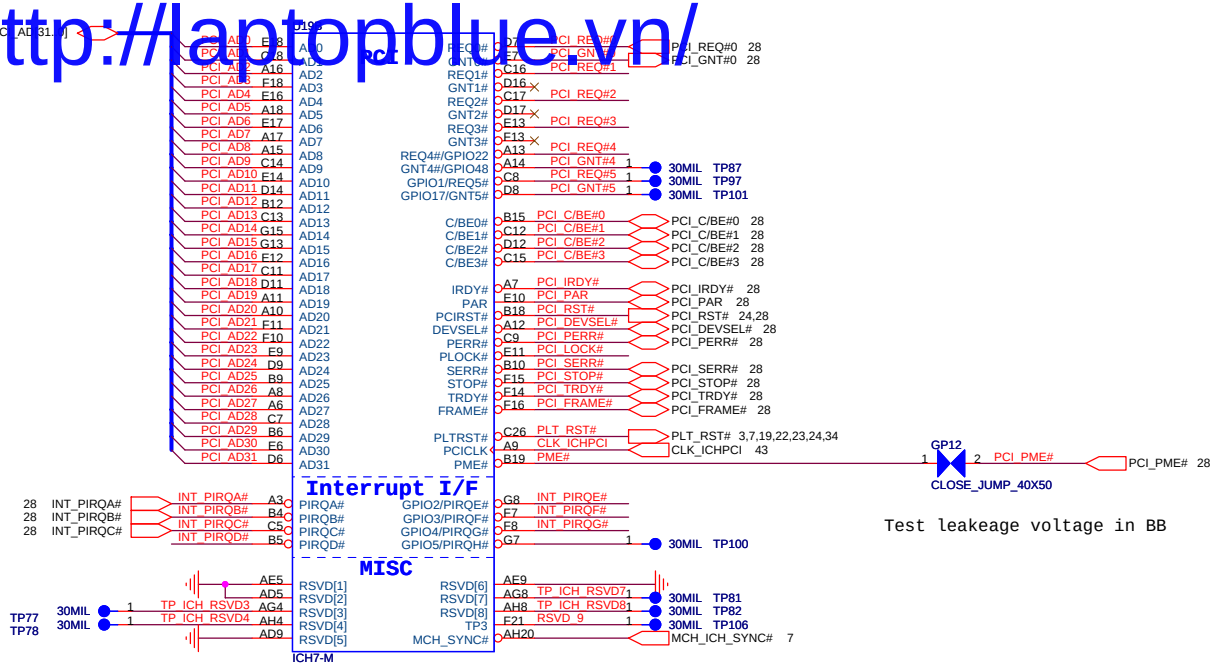


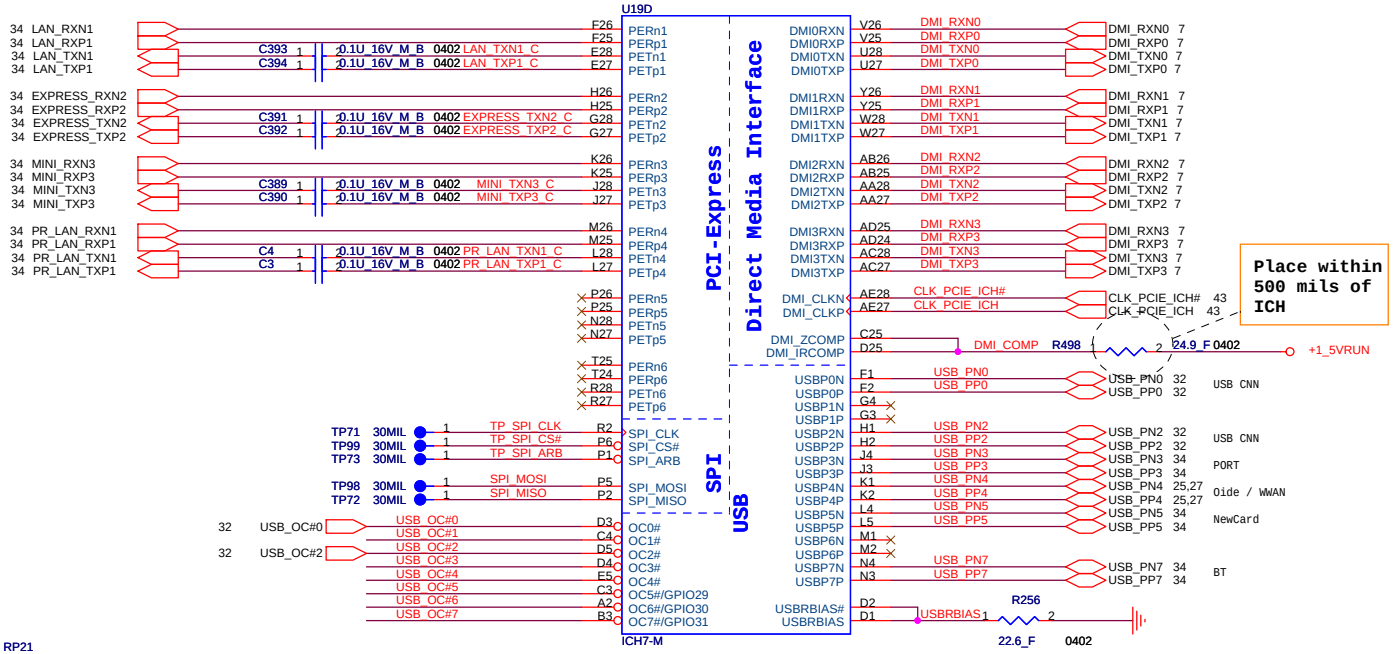


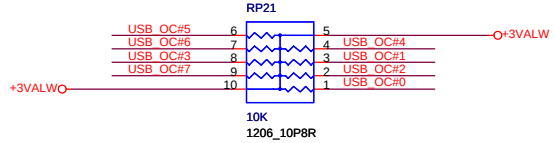
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	LVDS / S_VIDEO	
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 16 of 47	



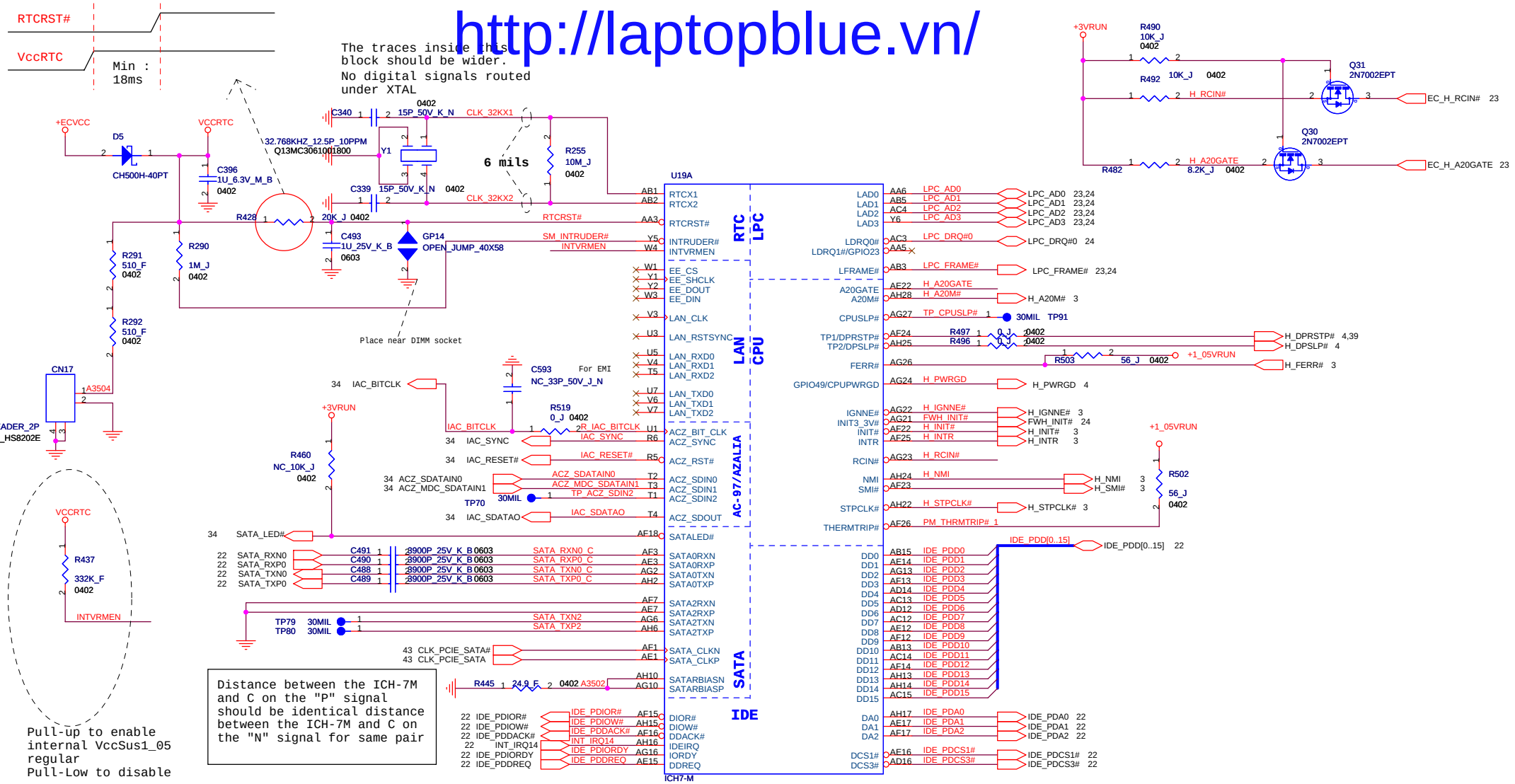
PCI Pullups







FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	ICH7-M(PCI/DMI/USB/PCIE) 1/5		
Size A3	Document Number MS60-1-05 (MBX-163)		Rev 0.20
Date: Monday, June 19, 2006	Sheet 17 of 47		



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	ICH7-M(LPC,IDE,SATA) 2/5		
Size A3	Document Number MS60-1-05 (MBX-163)		Rev 0.20
Date: Monday, June 19, 2006	Sheet 18 of 47		

Stuff for No-reboot

+3VRUN R467 NC_1K_J 0402 AC_SPKR

+3VALW RP28 10K 0804_8P4R SMLINK1 SMLINK0 SMB_LINK_ALERT# PM_RI#

U19C ICH7-M

SMB: SMB_CLK_SB C22 SMBCLK; SMB_DATA_SB B22 SMBDATA; SMB_LINK_ALERT# A26 LINKALERT#; SMLINK0 B25 SMLINK0; SMLINK1 A25 SMLINK1

PM_RI# A28 RI#

AC_SPKR A19 SPKR; PM_SUS_STAT# A27 SUS_STAT#; PM_SYSRST# A22 SYS_RST#

PM_BMBUSY# AB18 GPIO0/BM_BUSY#

SMB_ALERT# B23 GPIO11/SMBALERT#

PM_STPPCI# AC20 GPIO18/STPPCI#; STP_CPU# AE21 GPIO20/STPCPU#

EC_OUT1 A21 GPIO26

TP_GPIO27 B21 GPIO27; TP_GPIO28 E23 GPIO28

PM_CLKRUN# AG18 GPIO32/CLKRUN#

GPIO33/AZ_DOCK_EN# AC19; GPIO34/AZ_DOCK_RST# U2

PCIE_WAKE# F20 WAKE#; INT_SERIRQ AH21 SERIRQ; SB_THRM# AE20 THRM#

IMVP_OK AD22 VRMPWRGD

ID_LPC_PCI# AC21 GPIO6; RUNTIME_SCI# AC18 GPIO7; EXTSMI# F21 GPIO8

GPIO: GPIO21/SATA0GP AE19; GPIO19/SATA1GP AH18; GPIO36/SATA2GP AH19; GPIO37/SATA3GP AE19

Clocks: CLK14 AC1 CLK_ICH14; CLK48 B2 CLK_USB48; SUSCLK C20 SUS_CLK

Power MGT: SLP_S3# B24; SLP_S4# D23; SLP_S5# F22; PWROK AA4; GPIO16/DPRSLPVR AC22 A3601; TP0/BATLOW# C21; PWRBTN# C23; LAN_RST# C19; RSMRST# Y4 A3602

GPIO: GPIO9 E20 SB_RST#; GPIO10 A20; GPIO12 F19 GPIO12; GPIO13 E19 GPIO13; GPIO14 R4 WAKE_SCI#; GPIO15 F22 GPIO15; GPIO24 R3 PID0; GPIO25 D20 PID1; GPIO35 AD21; GPIO38 AD20 LCDID2; GPIO39 AE20 LCDID3

80 Port I/F:
H: LPC bus
L: PCI bus

+3VALW: R485 GPIO15 10K_J 0402; R473 SB_RST# 10K_J 0402; R487 PM_SYSRST# 10K_J 0402; R479 BATLOW# 8.2K_J 0402; R474 PCIE_WAKE# 1K_J 0402; R465 GPIO12 10K_J 0402; R493 SMB_ALERT# 10K_J 0402; R475 EXTSMI# 10K_J 0402; R439 WAKE_SCI# 10K_J 0402; R457 GPIO13 10K_J 0402

+3VRUN: R463 10K_J 0402; Q29 2N7002EPT; R458 RUNTIME_SCI# 8.2K_J 0402 → EC_RUNTIME_SCI# 23; R477 SB_THRM# 8.2K_J 0402; R491 INT_SERIRQ 10K_J 0402; R461 PM_CLKRUN# 8.2K_J 0402; R481 ID_LPC_PCI# 10K_J 0402

After check with SW team .
We don't use this pin but reserve to CORE power rail

R434 PM_RSMRST# 10K_J 0402

+3VRUN: R430 NC_10K_J 0402; R464 NC_10K_J 0402; PID0; PID1; R429 10K_J 0402; R468 10K_J 0402

+3VRUN: R488 4.7K_J 0402; R480 4.7K_J 0402; SMB_CLK_SB → SMB_CLK_SB 13,14,34,43; SMB_DATA_SB → SMB_DATA_SB 13,14,34,43

Adds.AEH
U14 EEPROM_SOP-8_256x8 HT24LC02
VCC WP SCL SDA A0 A1 A2 VSS
C330 0.1U_16V_M_B 0402

CLK_USB48 → R432 NC_10_J 0402; C487 NC_10P_50V_J_N 0402

R472 10K_J 0402

+3VRUN: R267 10K_J 0402; R269 10K_J 0402

LCDID0 16 BIOS_CRISIS# 16
LCDID1 16

CLK_ICH14 43
CLK_USB48 43

30MIL TP107

R495 100_J 0402 → PM_SLP_S3# 23
R499 100_J 0402 → PM_SLP_S4# 23
R486 100_J 0402 → PM_SLP_S5# 23

IMVP_PWRGD 7,23

R484 100_J 0402 CRB 0826 → DPRSLPVR 7,39

R483 NC_100K_J 0402

ICH_PWRBTN_# 23

PLT_RST# 3,7,17,22,23,24,34

R435 100_J 0402 → PM_RSMRST# → PM_RSMRST# 23

SB_RST# 24
IMVP_PHASEGD 17
OVT_EC# 3,23,26,39

R459 0_J 0402

WAKE_SCI# 23

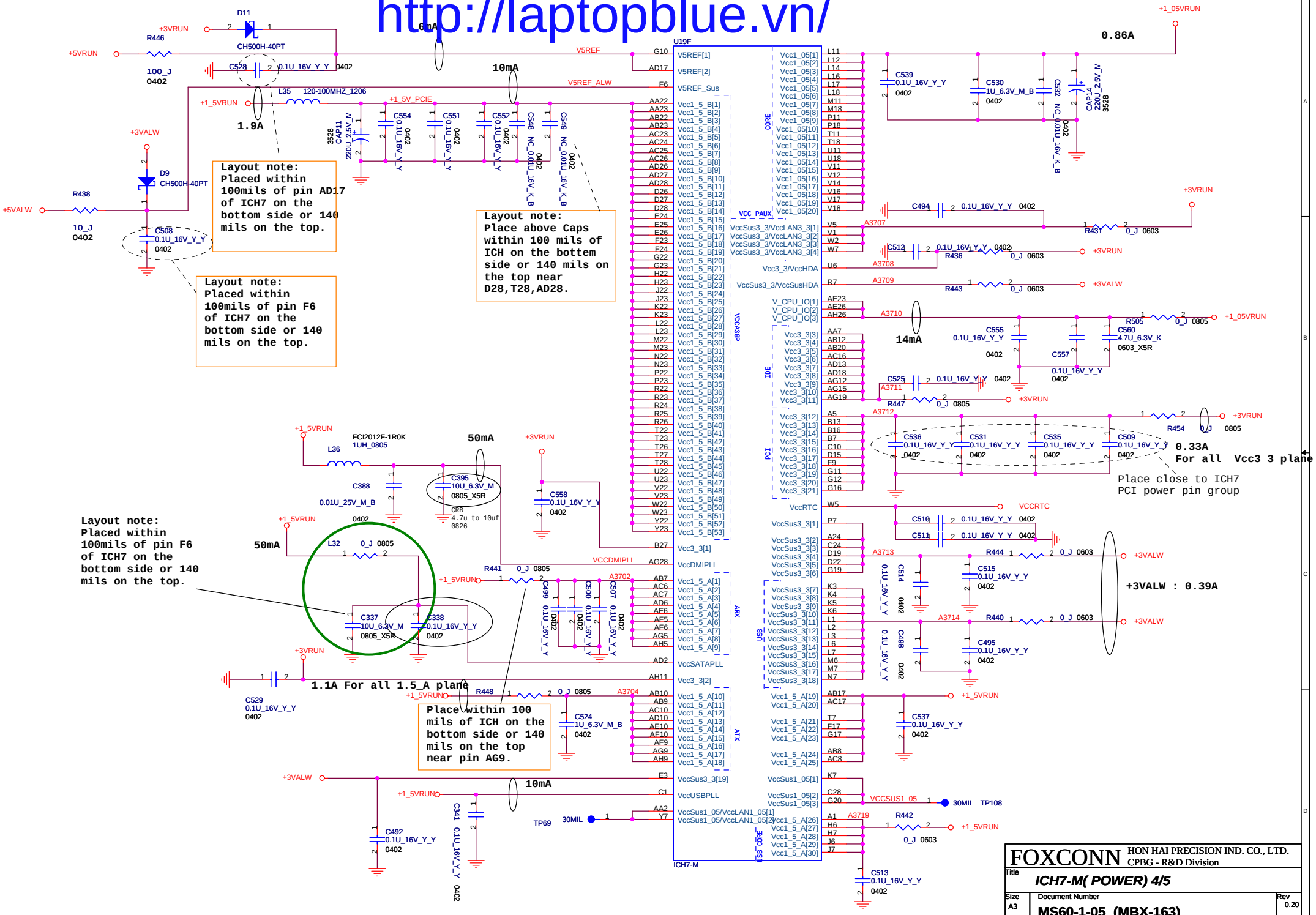
SATACLKREQ# 43
LCDID2 16

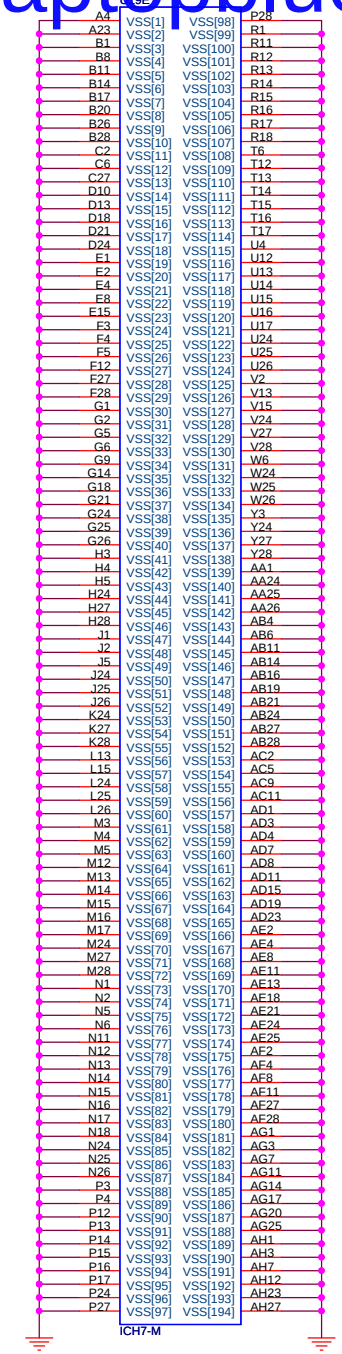
+3VRUN: R270 10K_J 0402; R476 10K_J 0402

TP109 30MIL; TP90 30MIL; TP110 30MIL

27 AC_SPKR; 24 PM_SUS_STAT#; 7 PM_BMBUSY#; 43 PM_STPPCI#; 43 STP_CPU#; 24 EC_OUT1; 34 PCIE_WAKE#; 23,24,28 INT_SERIRQ; 23,24,28 PM_CLKRUN#; 23,39 IMVP_OK; 24 ID_LPC_PCI#; 23 EXTSMI#

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	ICH7-M(GPIO) 3/5
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 19 of 47





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*ICH7-M(GND) 5/5*	
Size A3	Document Number **MS60-1-05 (MBX-163)**	Rev 0.20
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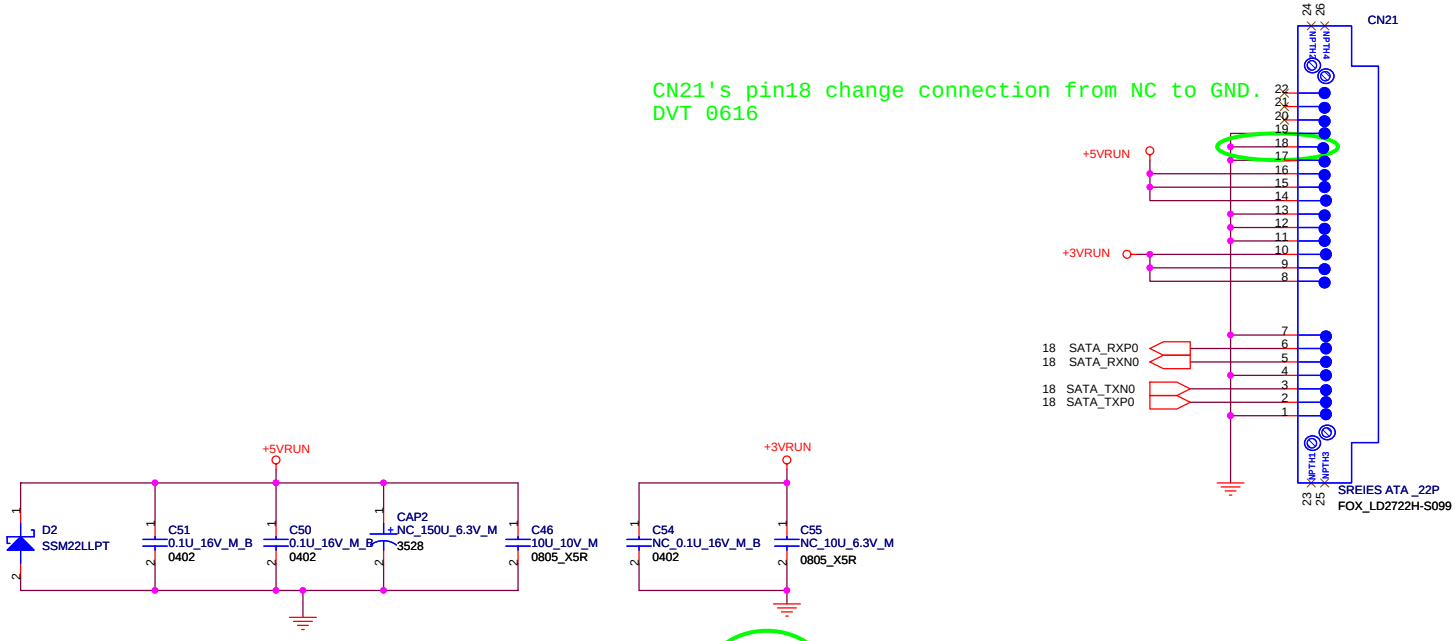
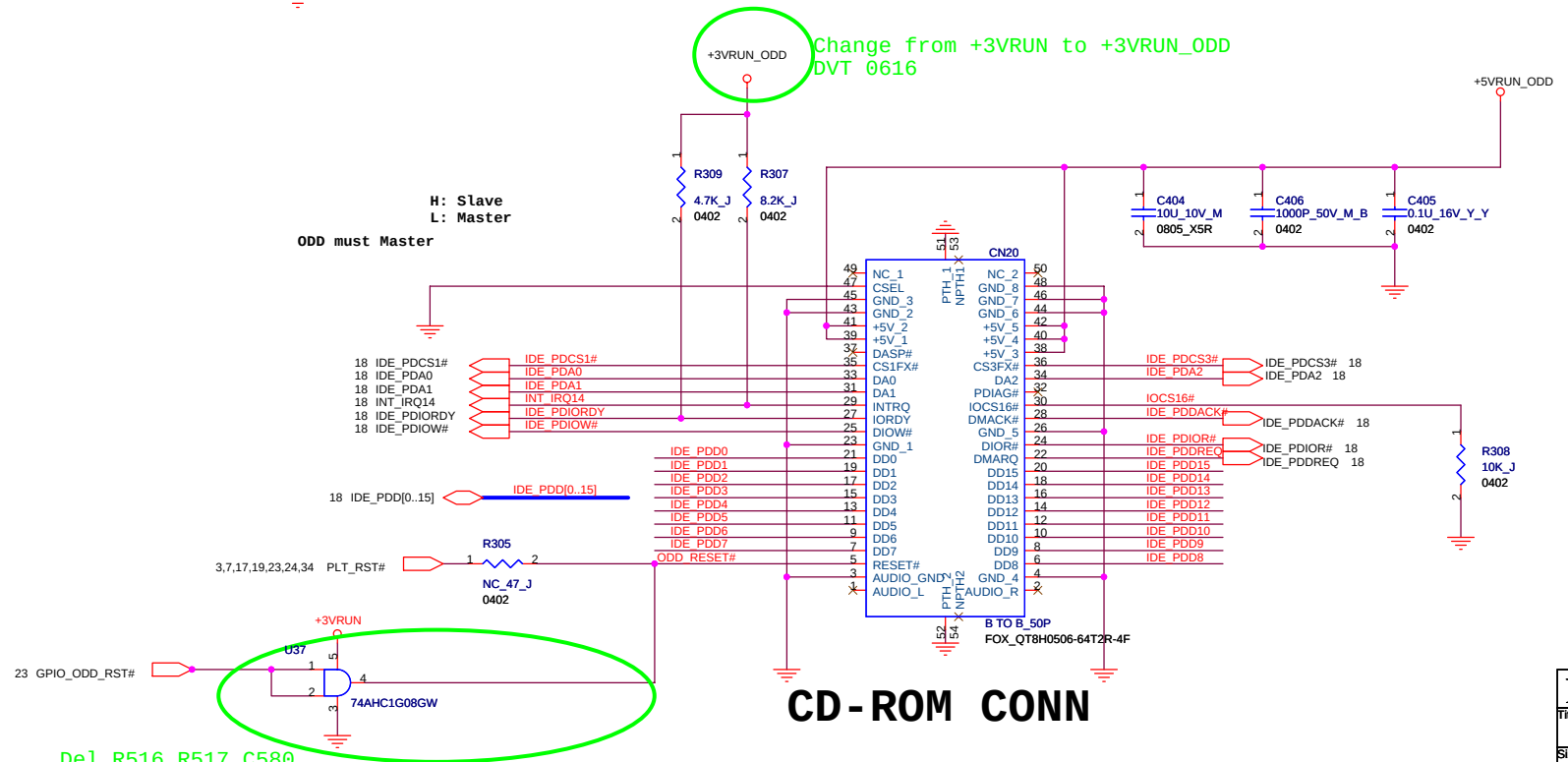
SATA HDD CONN





CD-ROM CONN

Del R516,R517,C580
DVT 0615

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 22 of 47	

Consider short FB after BB test.

FOX_GB21240-0002-7F
FPC CONN_24P
CN4

RP1 10K 0804_8P4R

U16
KB3910SFC1

Add R521
DVT 0615

MODEL ID check with software define

M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM

M-ID 5: 0- MS60 and the following MS60 type
1- MS70 and the following MS70 type
M-ID 2~4: 1- Reserved
M-ID 1: 0- Intel 940 series
1- Intel 945 series
M-ID 0: 0- External Gfx.
1- Internal Gfx.

change R244 connection form
''ALW_ON'' to ''ALW_ON_1''
DVT 0615

PORT_DET# change from pin81 to pin176
TP85 change from pin176 to pin81
DVT 0616

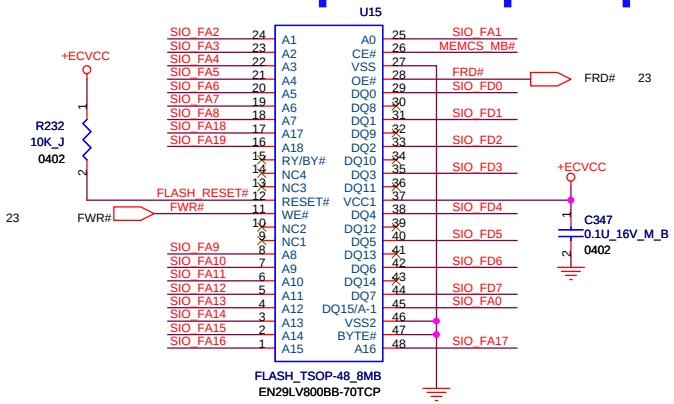
Add VISTA_SUPPORT# for Vista.
DVT 0616

Add GPIO_ODD_RST# for ODD reset.
DVT 0615

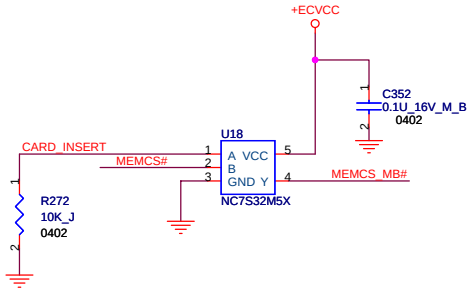
CN3
FPC_12P
FOX_GB5RF120-1200-7F

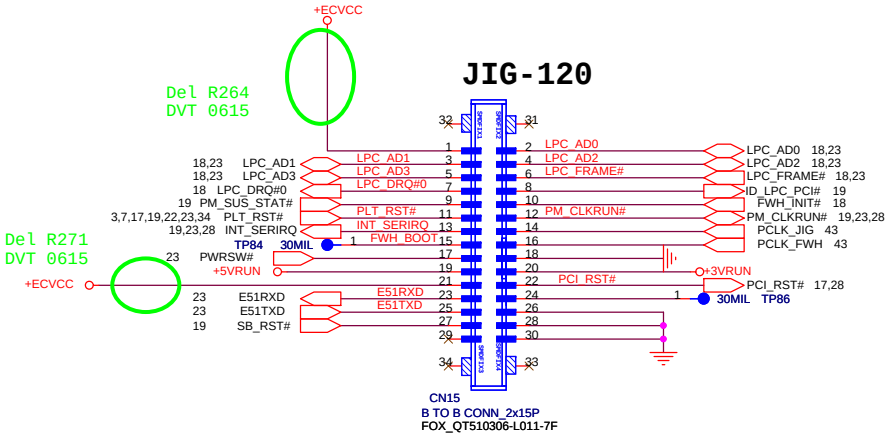
FOXCONN	HON HAI PRECISION IND. CO., LTD.
	CPBG - R&D Division
Title	EC+KBC
Size: Custom	Document Number: MS60-1-05 (MBX-163)
Rev	0.20
Date:	Monday, June 19, 2006
Sheet	23 of 47

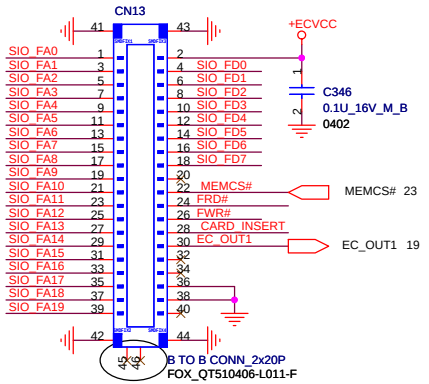
23 SIO_FA[19..0]
23 SIO_FD[7..0]



BIOS ROM







FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *Flash ROM/X-Bus CONN*

Size	Document Number	Rev
A3	MS60-1-05 (MBX-163)	0.20

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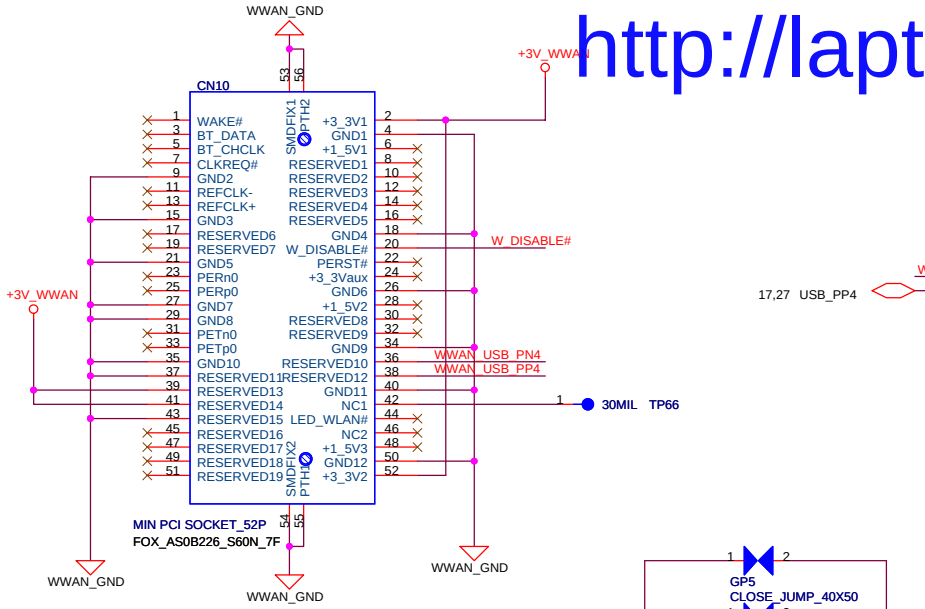
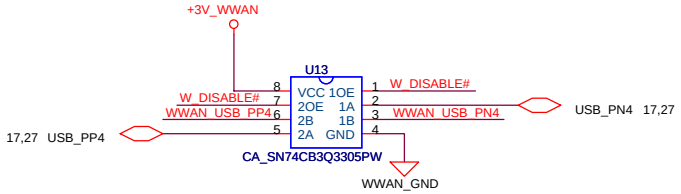
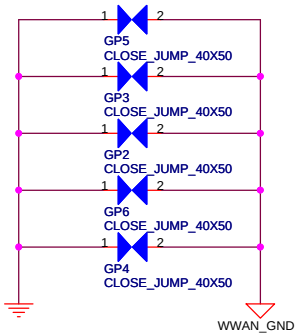
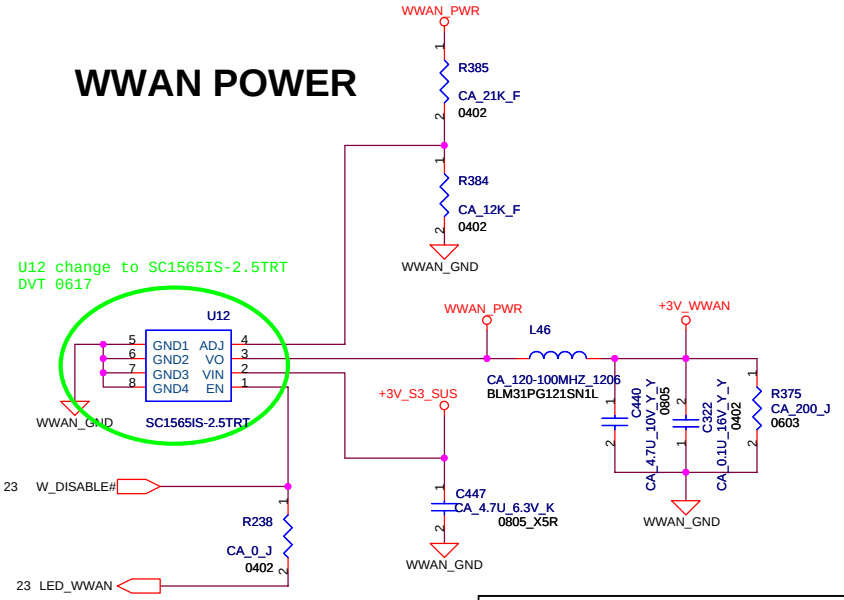




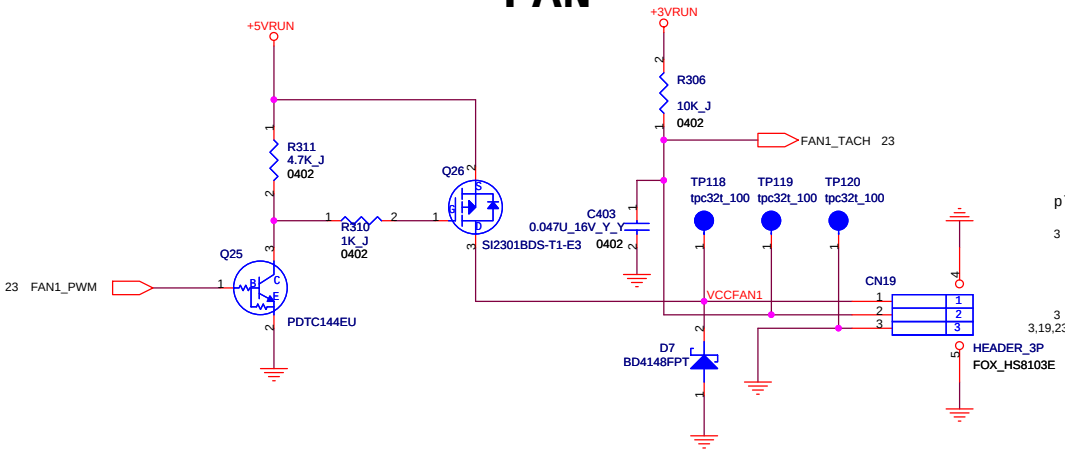


WWAN POWER

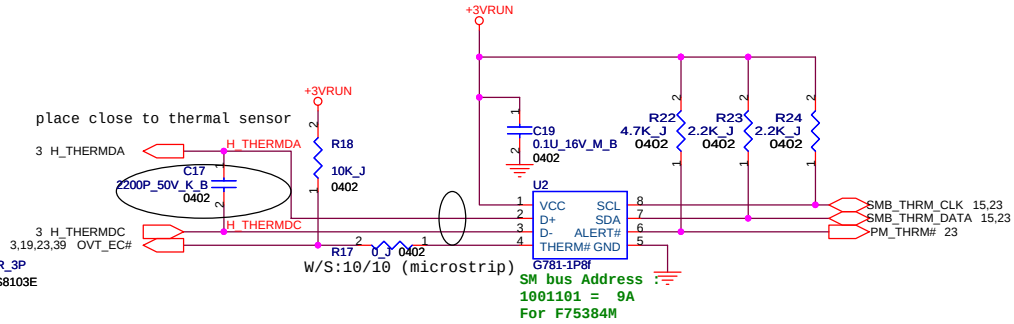


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: WWAN		
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 25 of 47	

FAN

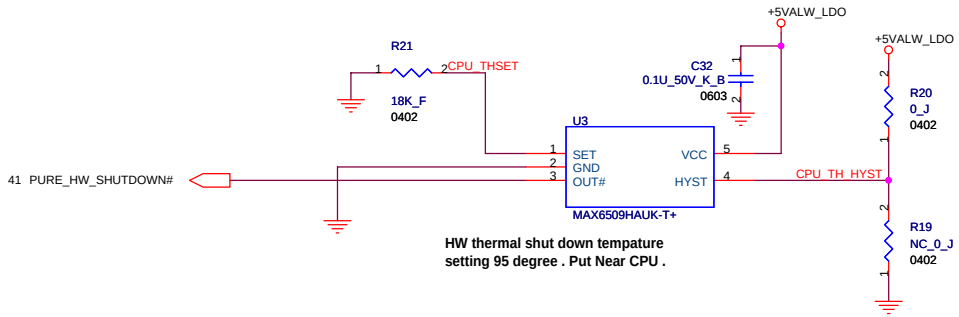


CPU SENSOR



Place Thermal-Sensor near CPU & GMCH.

HW THERMAL PROTECTION



HW thermal shut down tempature setting 95 degree . Put Near CPU .

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FAN/HW THERMAL PROTECT	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
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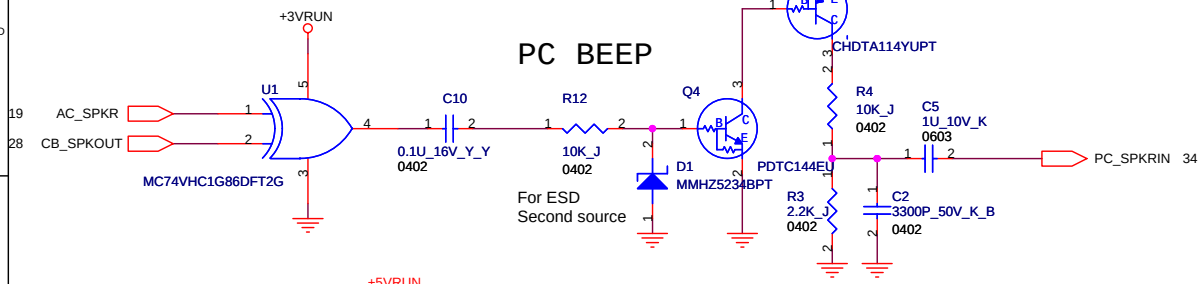
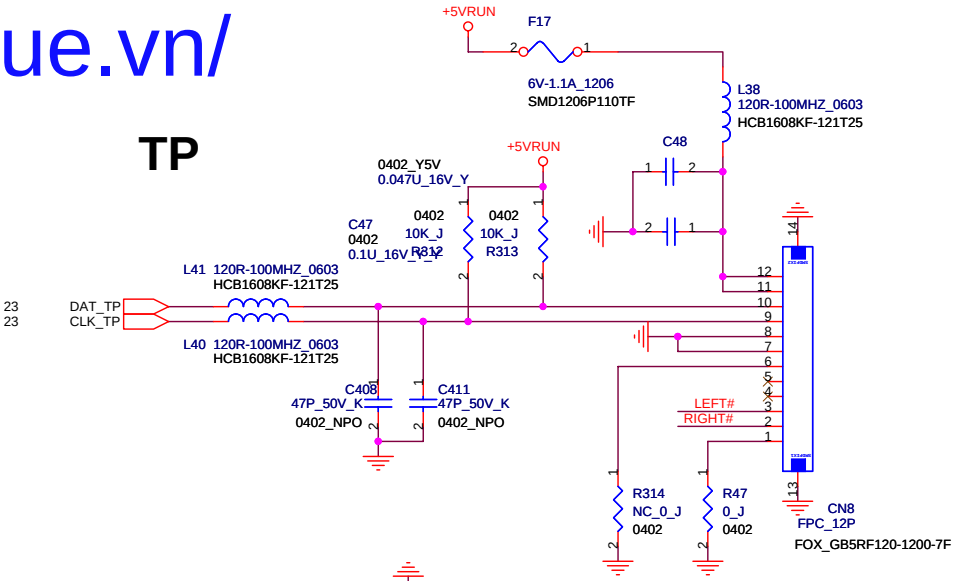
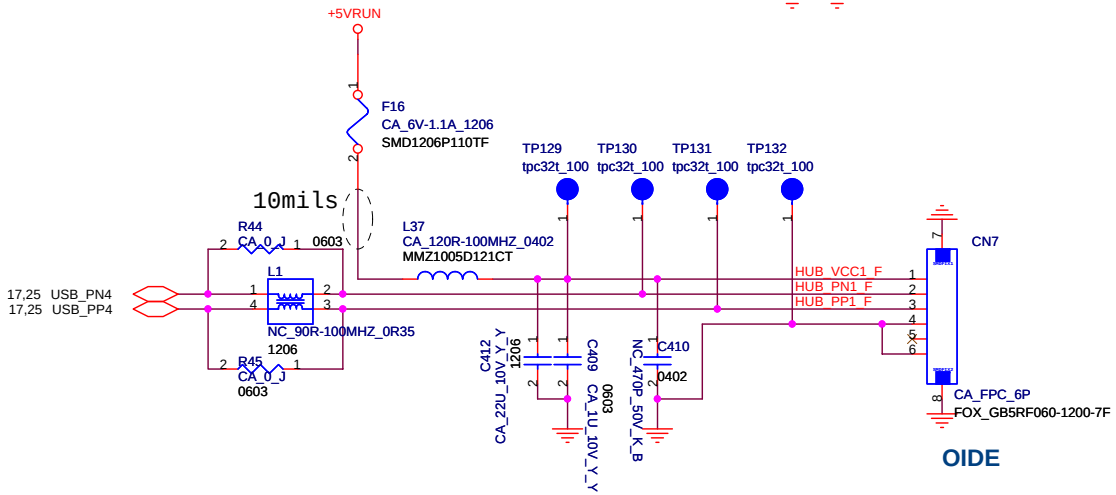
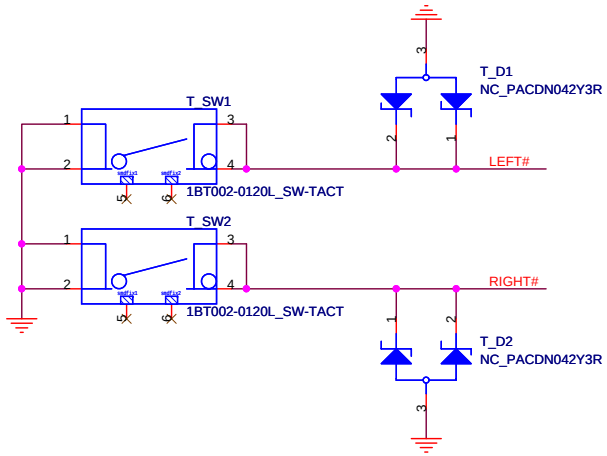
PC BEEP



TP

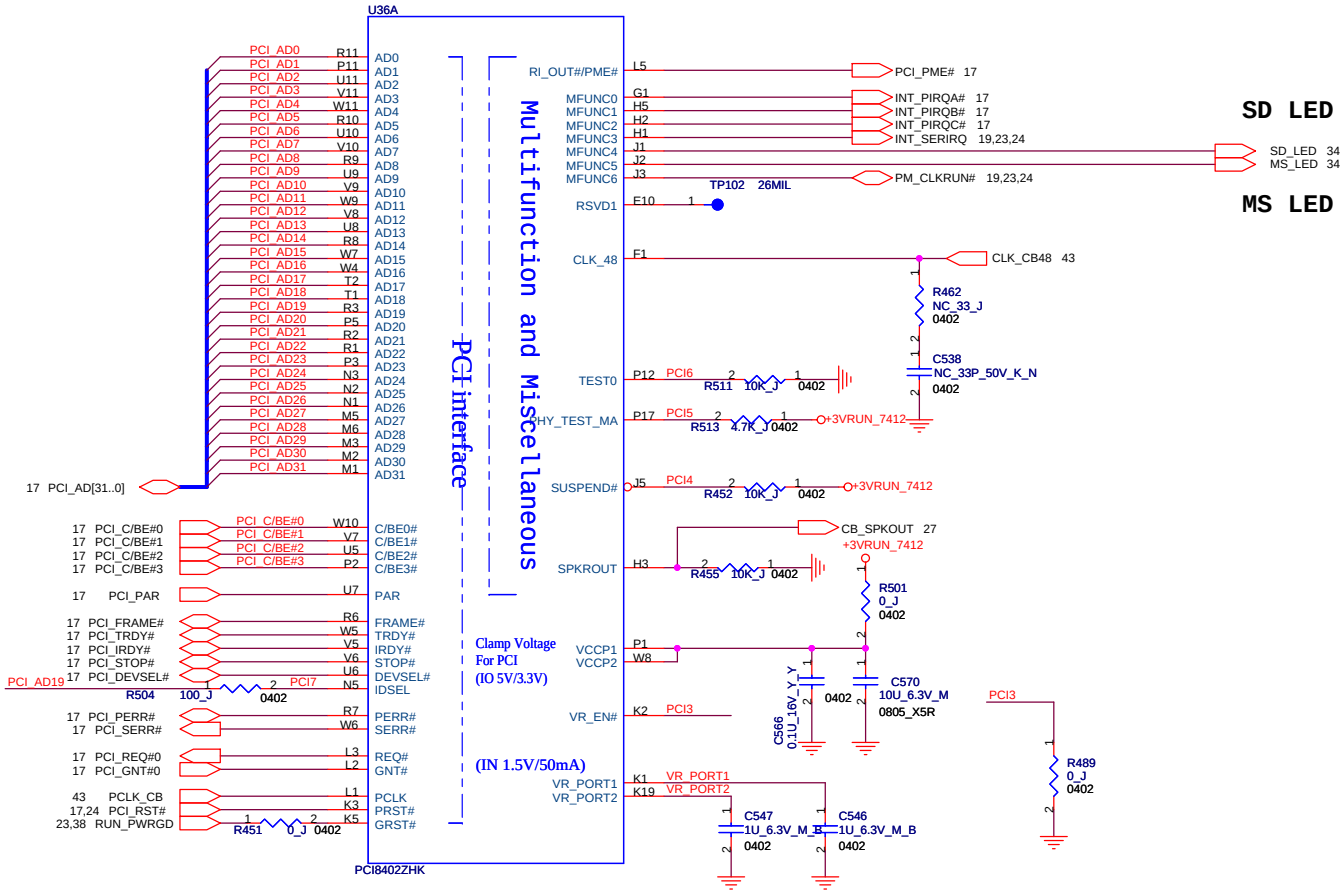


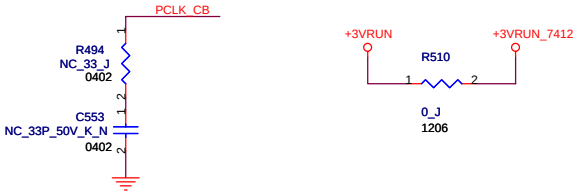




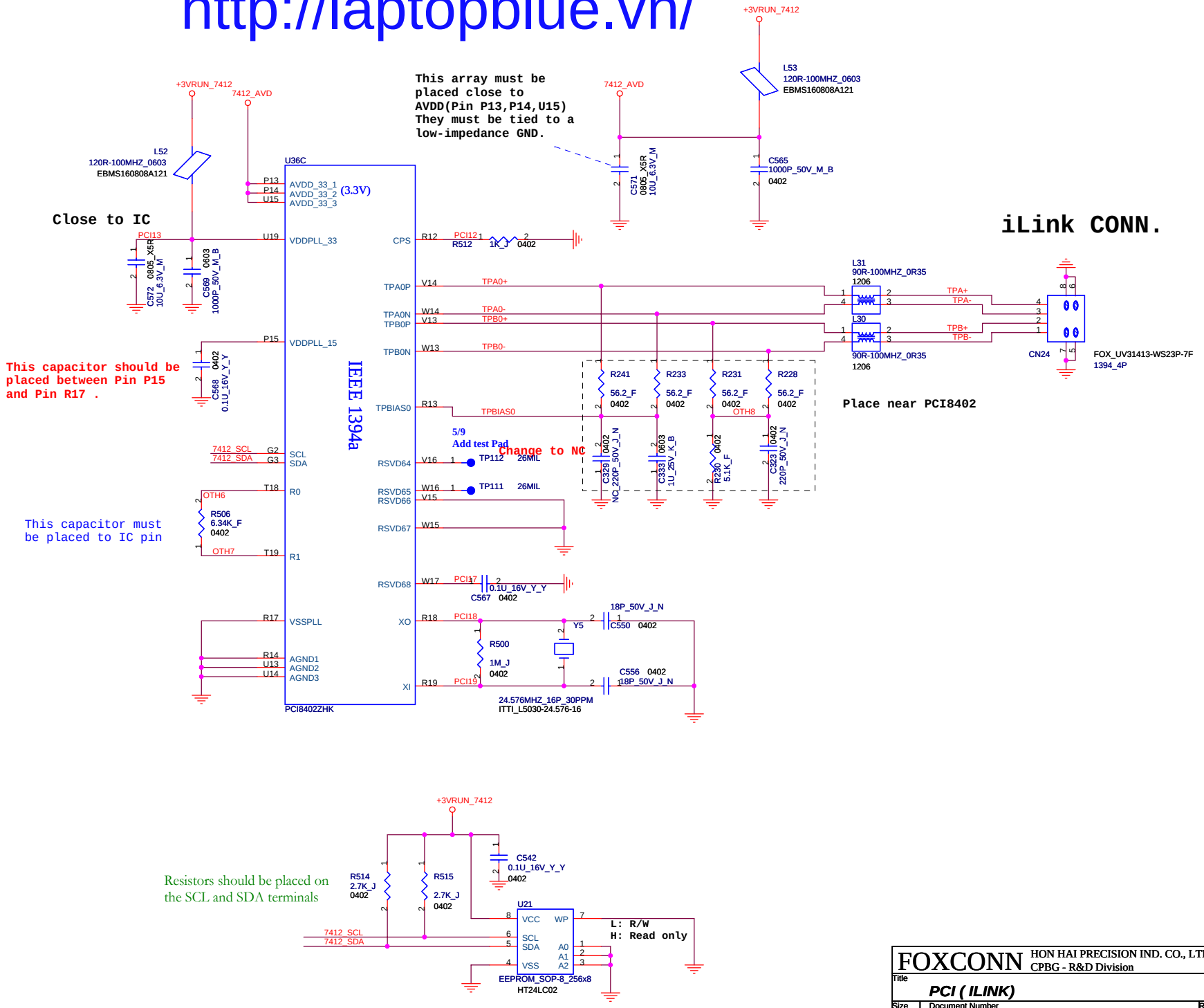
OIDE

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *OIDE/TP*		
Size: Custom	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 27 of 47	



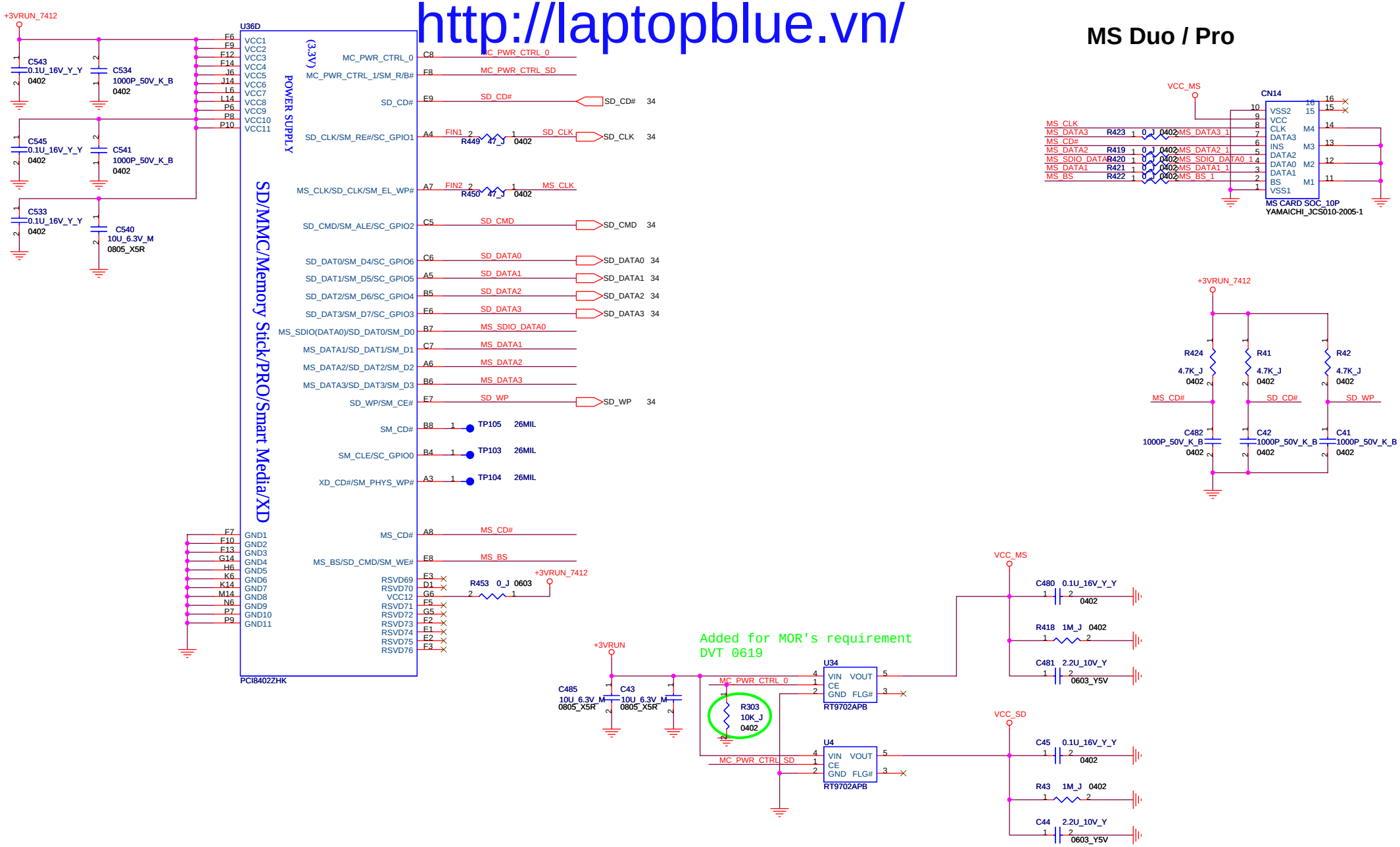


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (PCI BUS)		
Size: A3	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 28 of 47	

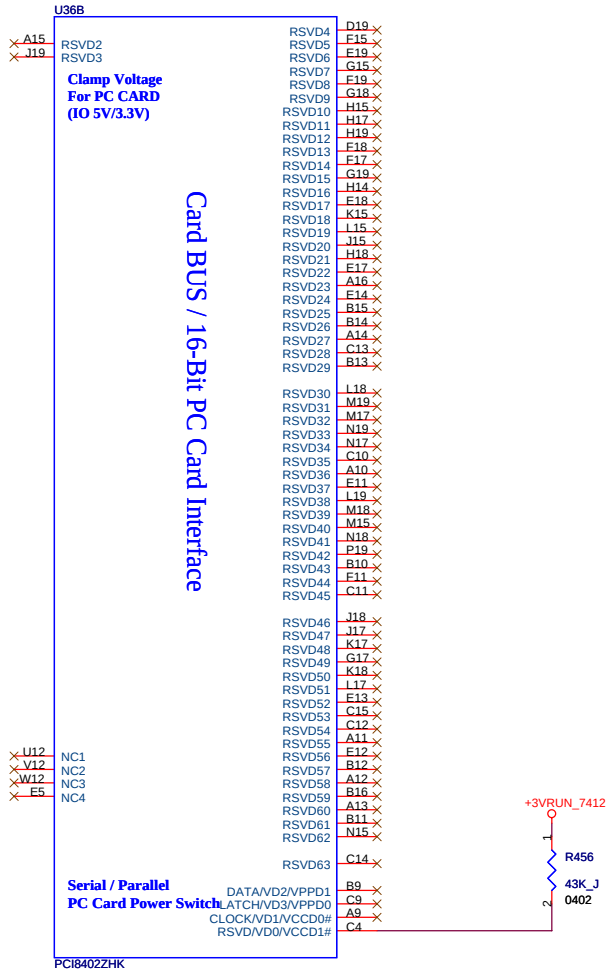


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (ILINK)
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 29 of 47

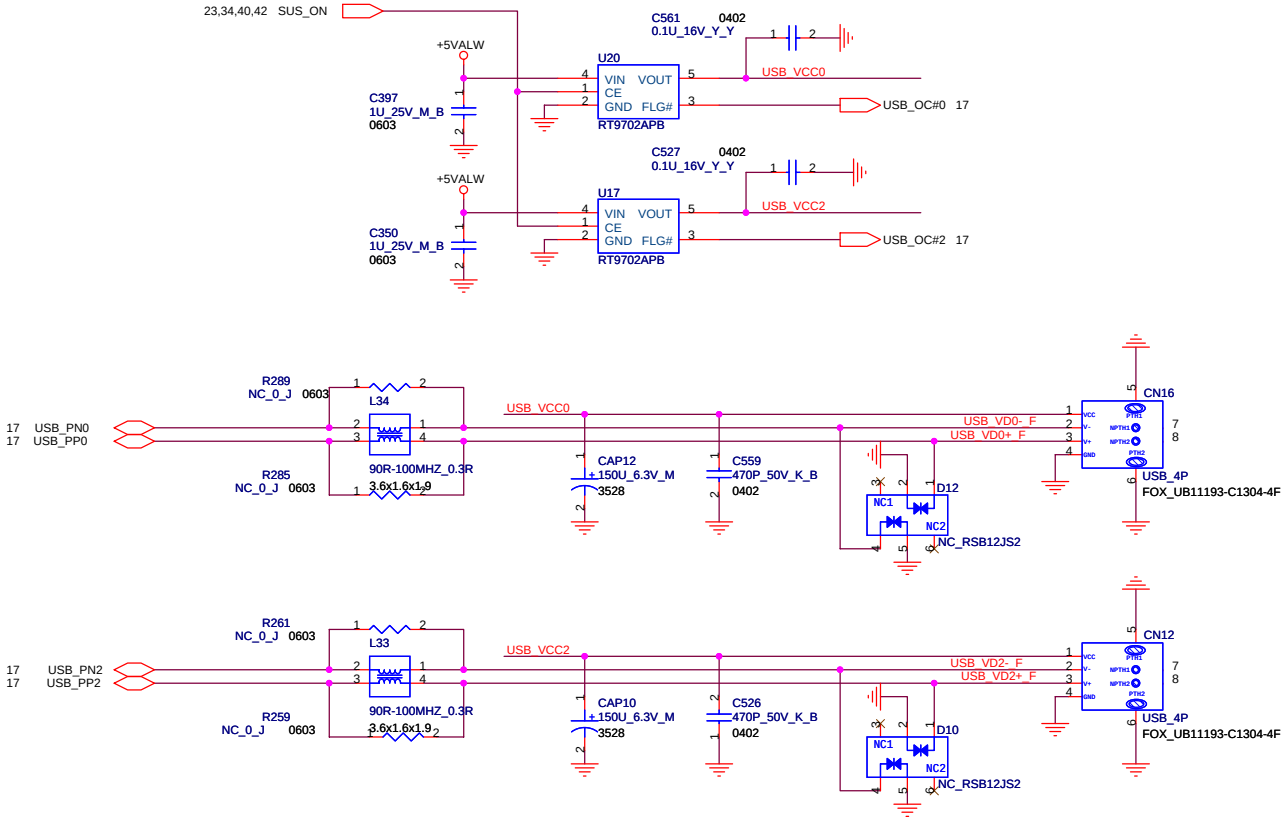
MS Duo / Pro



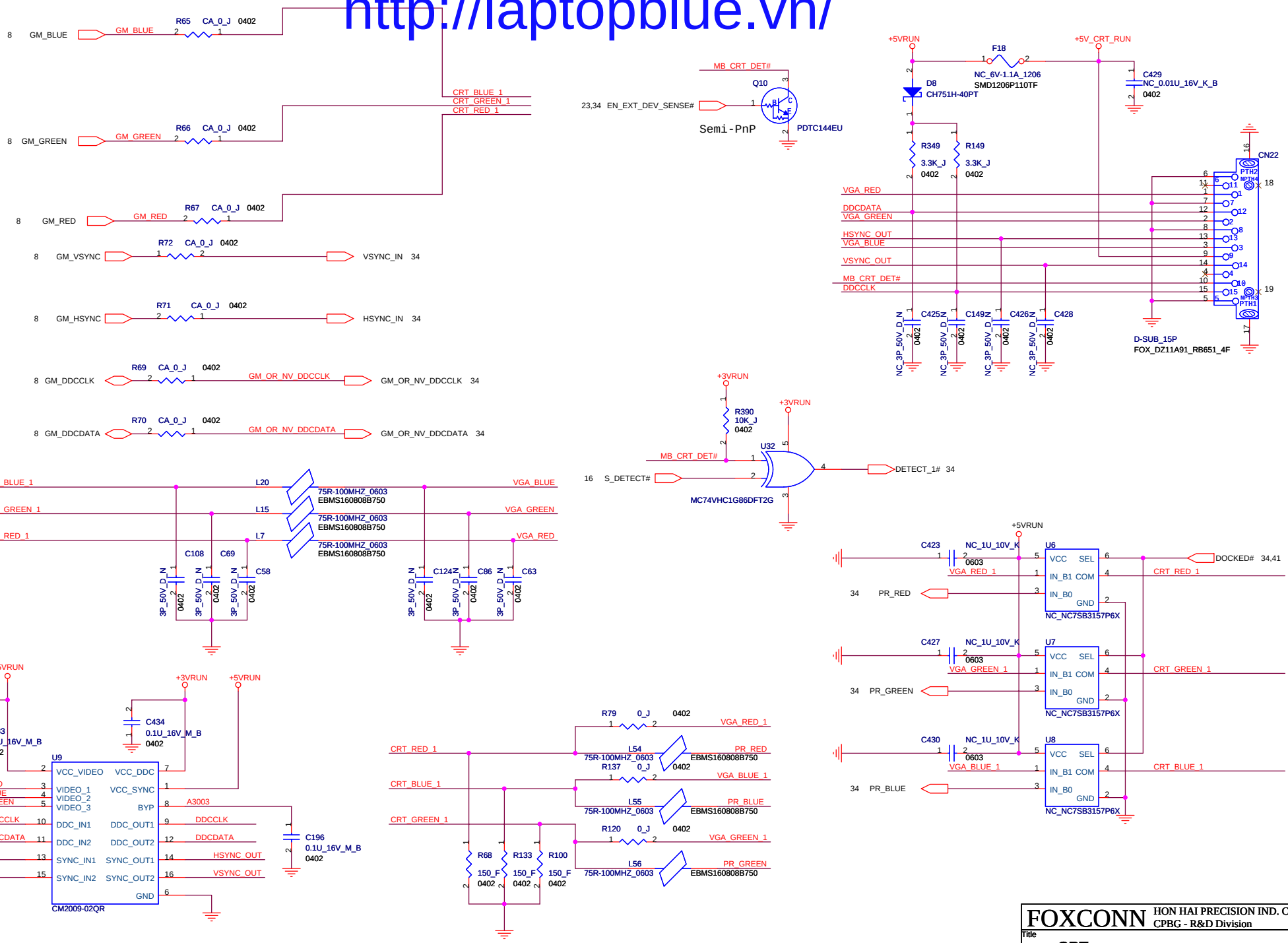
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (MS)
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 30 of 47



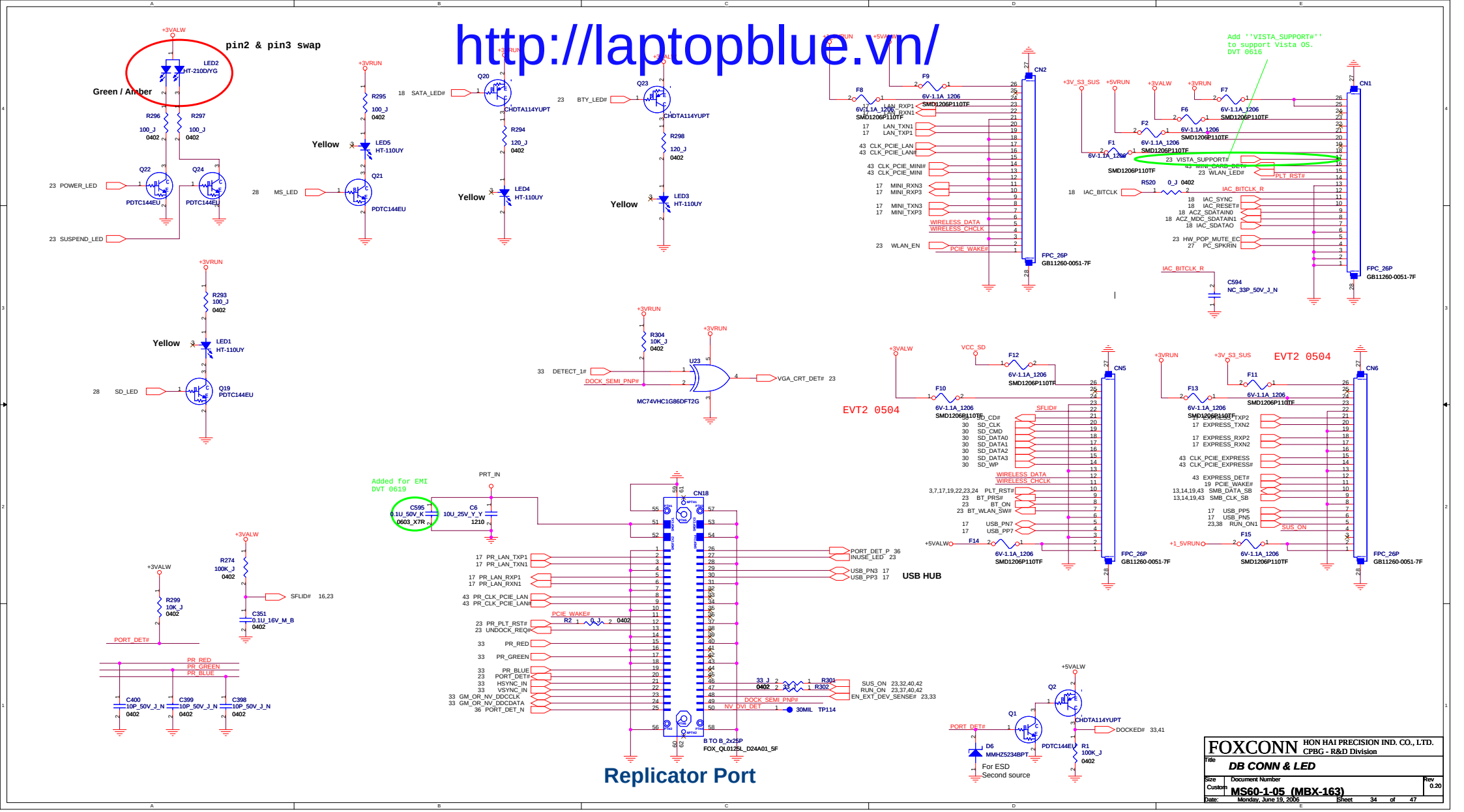
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (PCMCIA)		
Size: A3	Document Number: MS60	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 31 of 47	

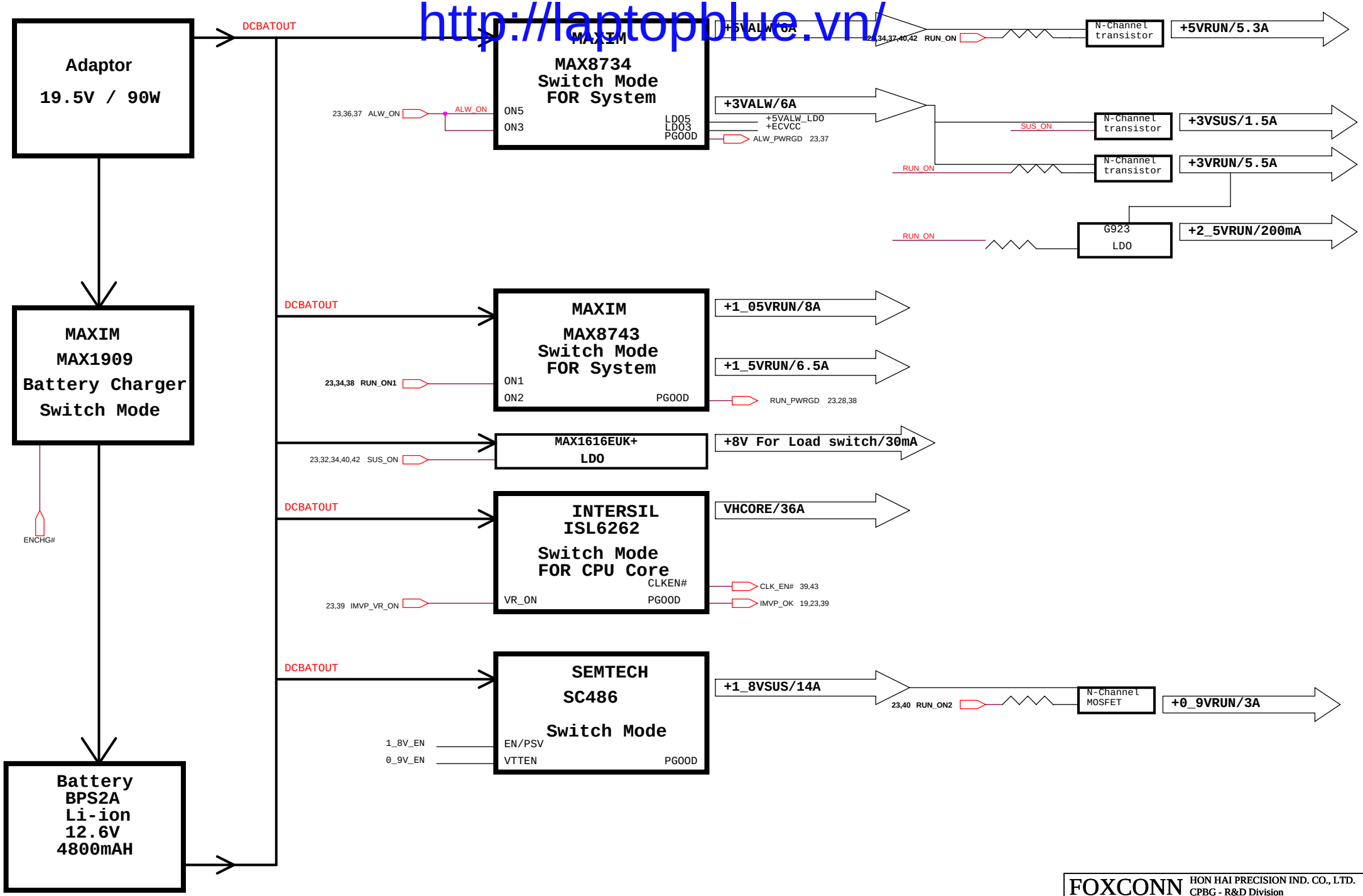


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***USB2.0/DOCKING CONN.***	
Size A3	Document Number **MS60-1-05 (MBX-163)**	Rev 0.20
Date: Monday, June 19, 2006	Sheet 32 of 47	

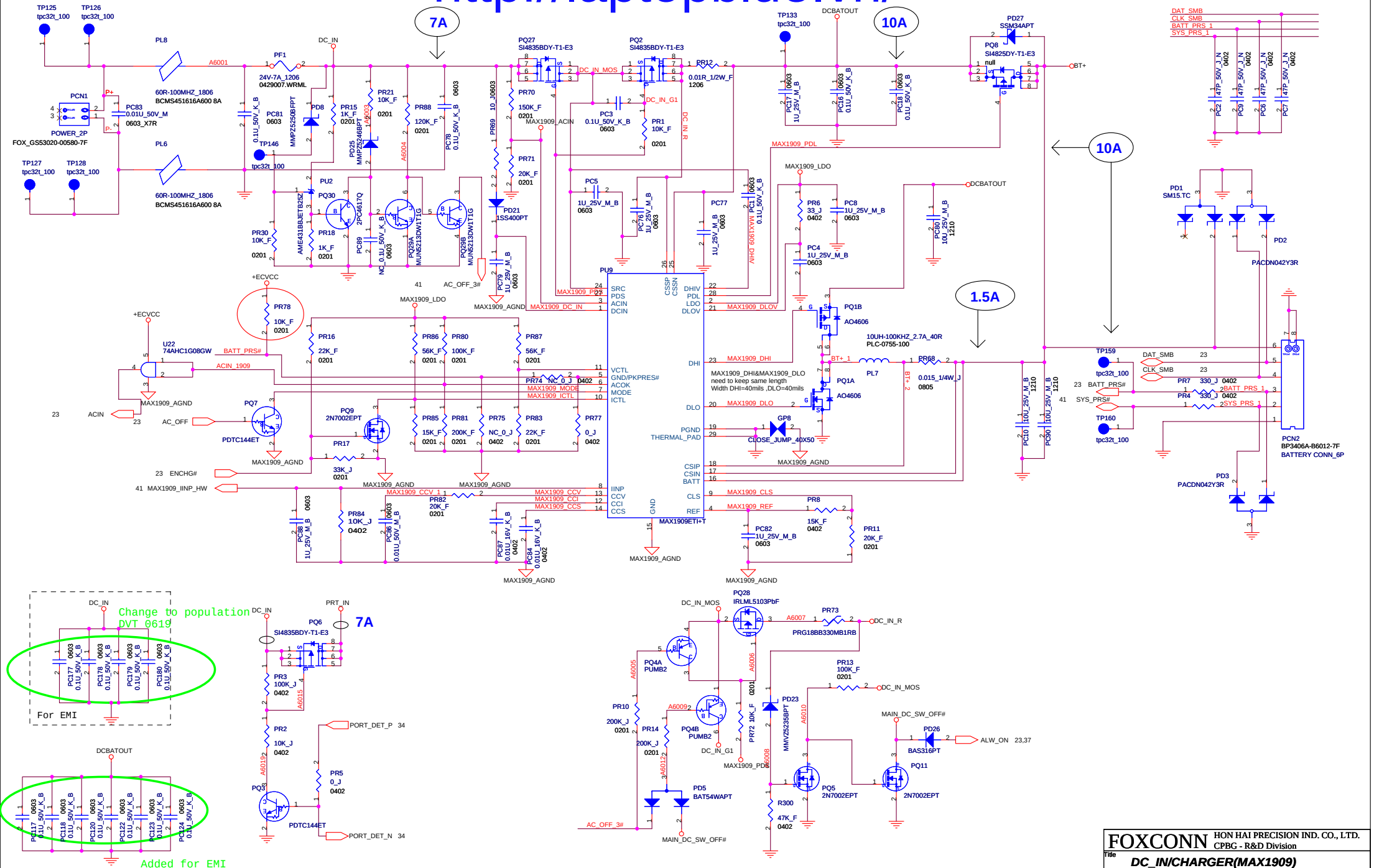


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: CRT			
Size: A3	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 33 of 47		

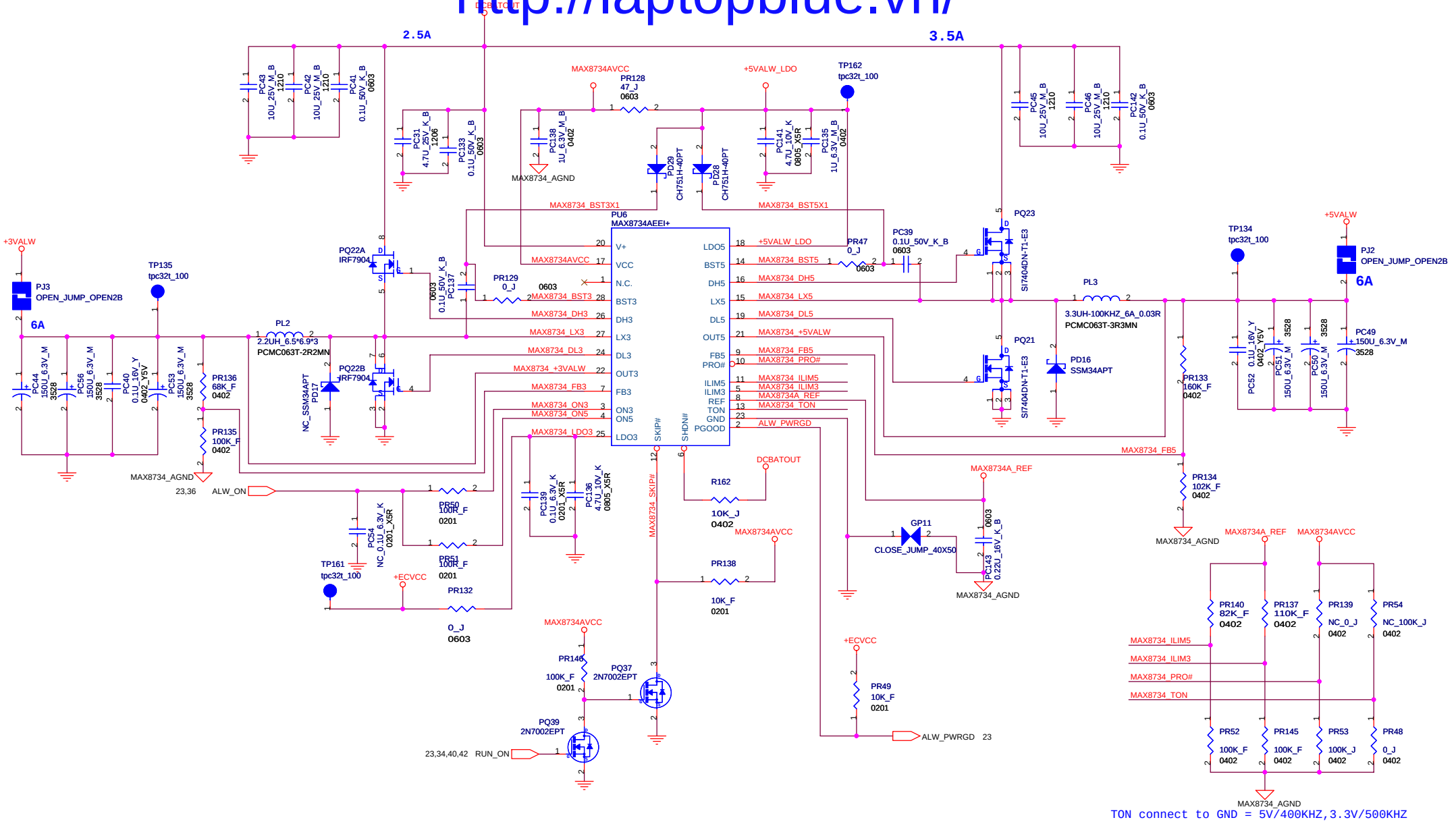




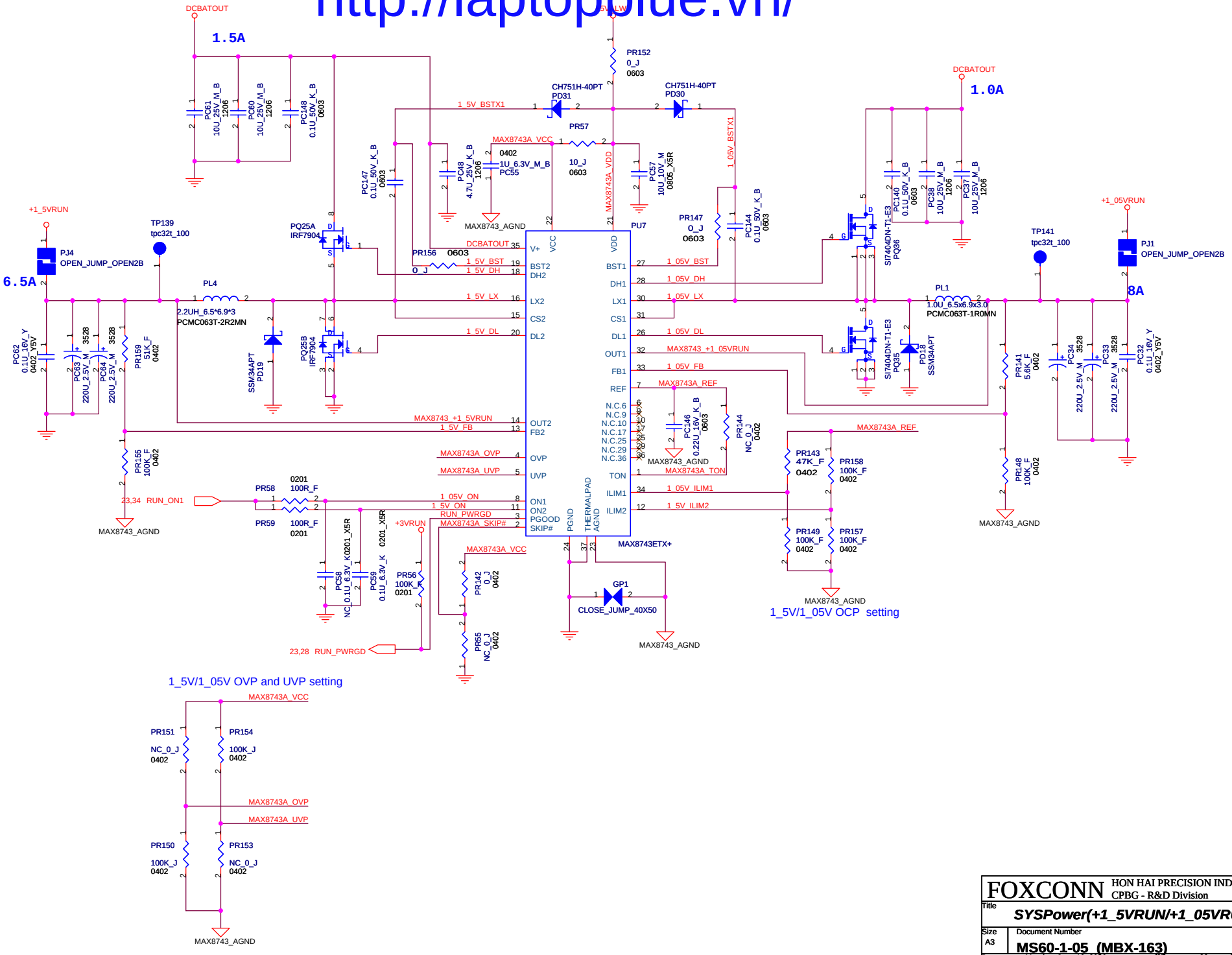
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Power Design Diagram*		
Size: A3	Document Number: MS60-1-05 (MBX-163)	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 35 of 47	



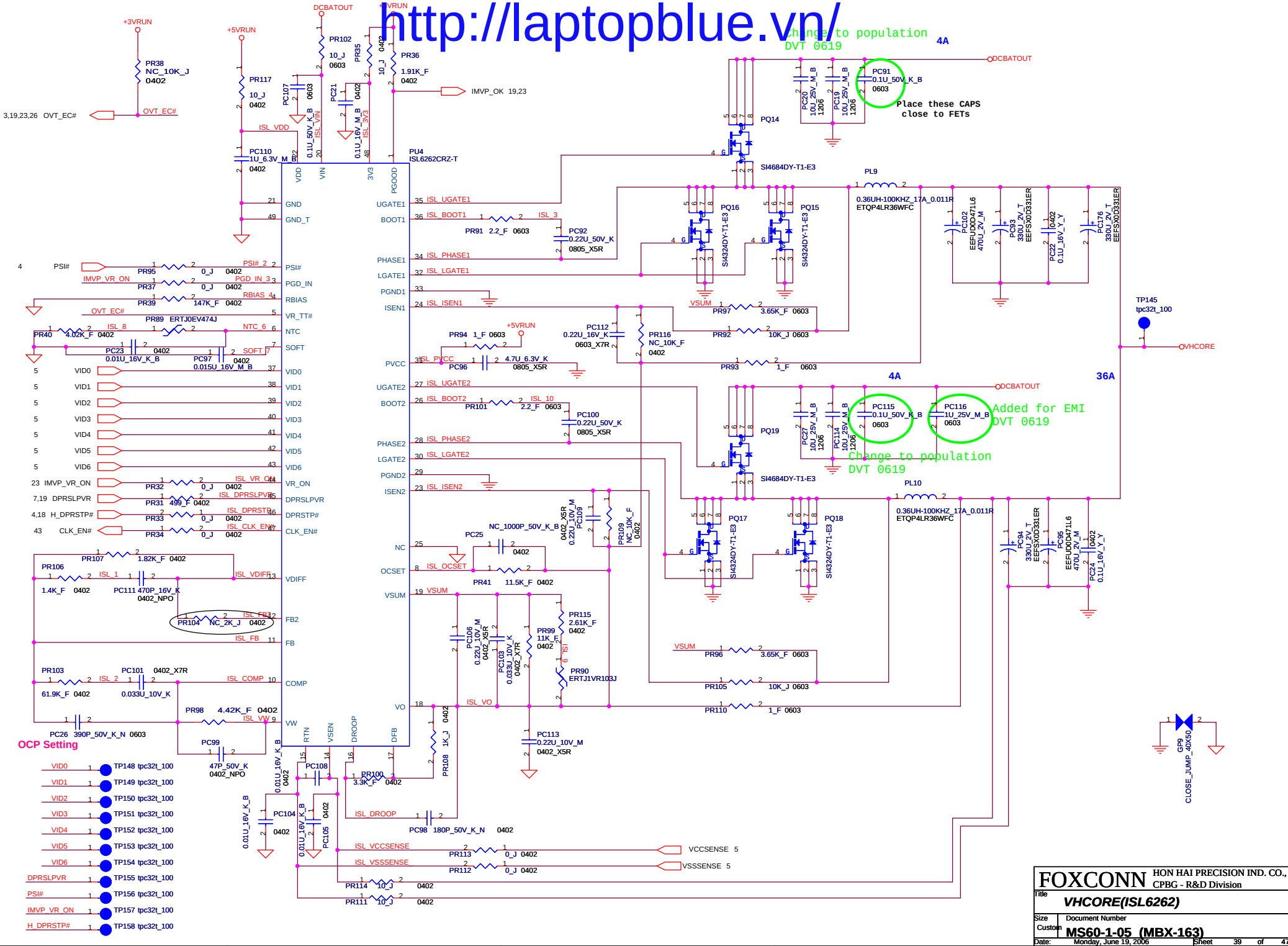
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	DC_IN/CHARGER(MAX1909)		
Size: Custom	Document Number: MS60-1-05 (MBX-163)		Rev: 0.20
Date: Monday, June 19, 2006	Sheet 36 of 47		



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYS Power (3D3VALW/5VALW)	
Size A3	Document Number MS60-1-05 (MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 37 of 47	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYSPower(+1_5VRUN/+1_05VRUN)	
Size A3	Document Number MS60-1-05_(MBX-163)	Rev 0.20
Date: Monday, June 19, 2006	Sheet 38 of 47	



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *VHCORE(ISL6262)*

Size: Custom | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

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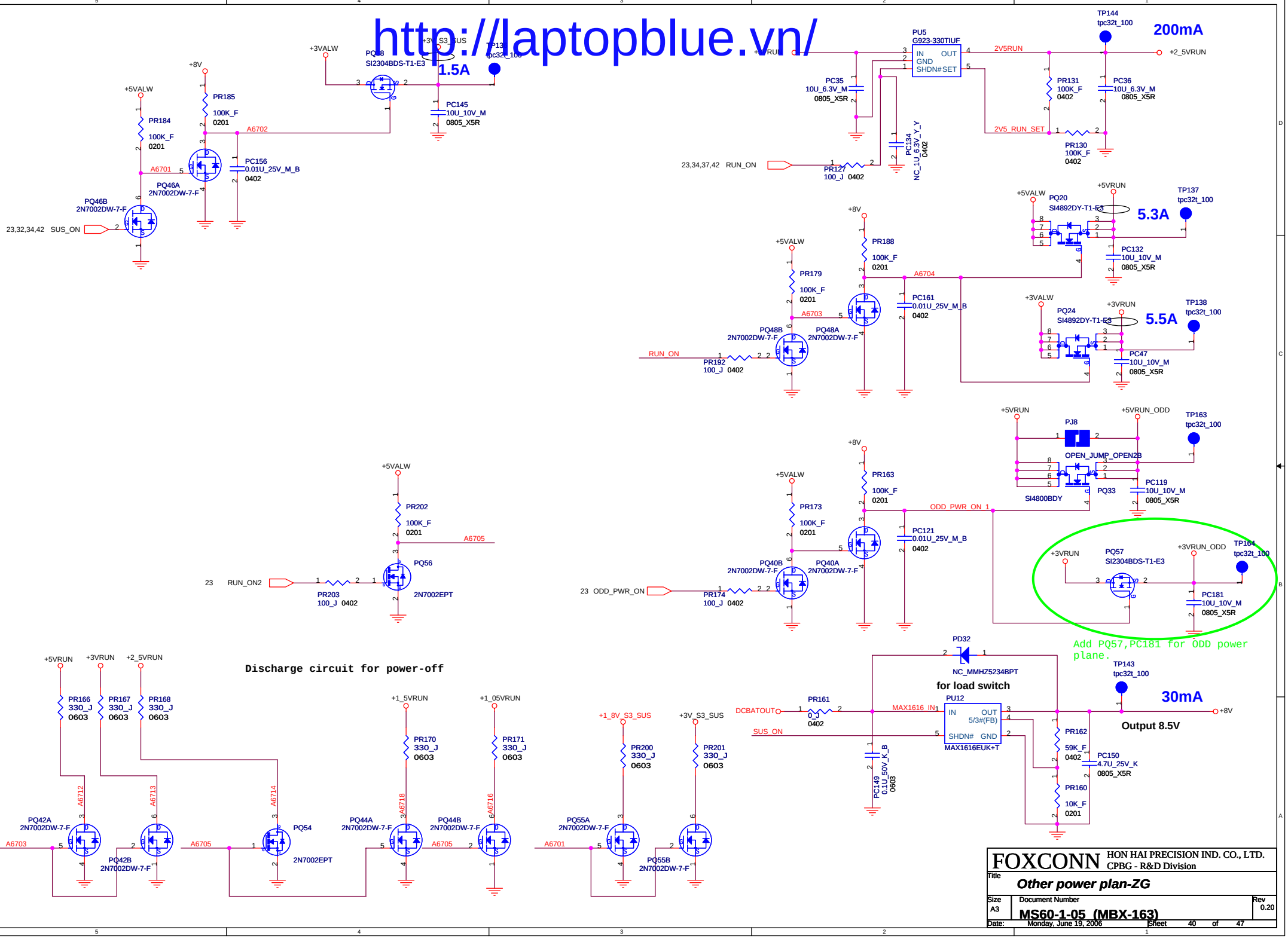

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*Other power plan-ZG*	
Size A3	Document Number **MS60-1-05 (MBX-163)**	Rev 0.20
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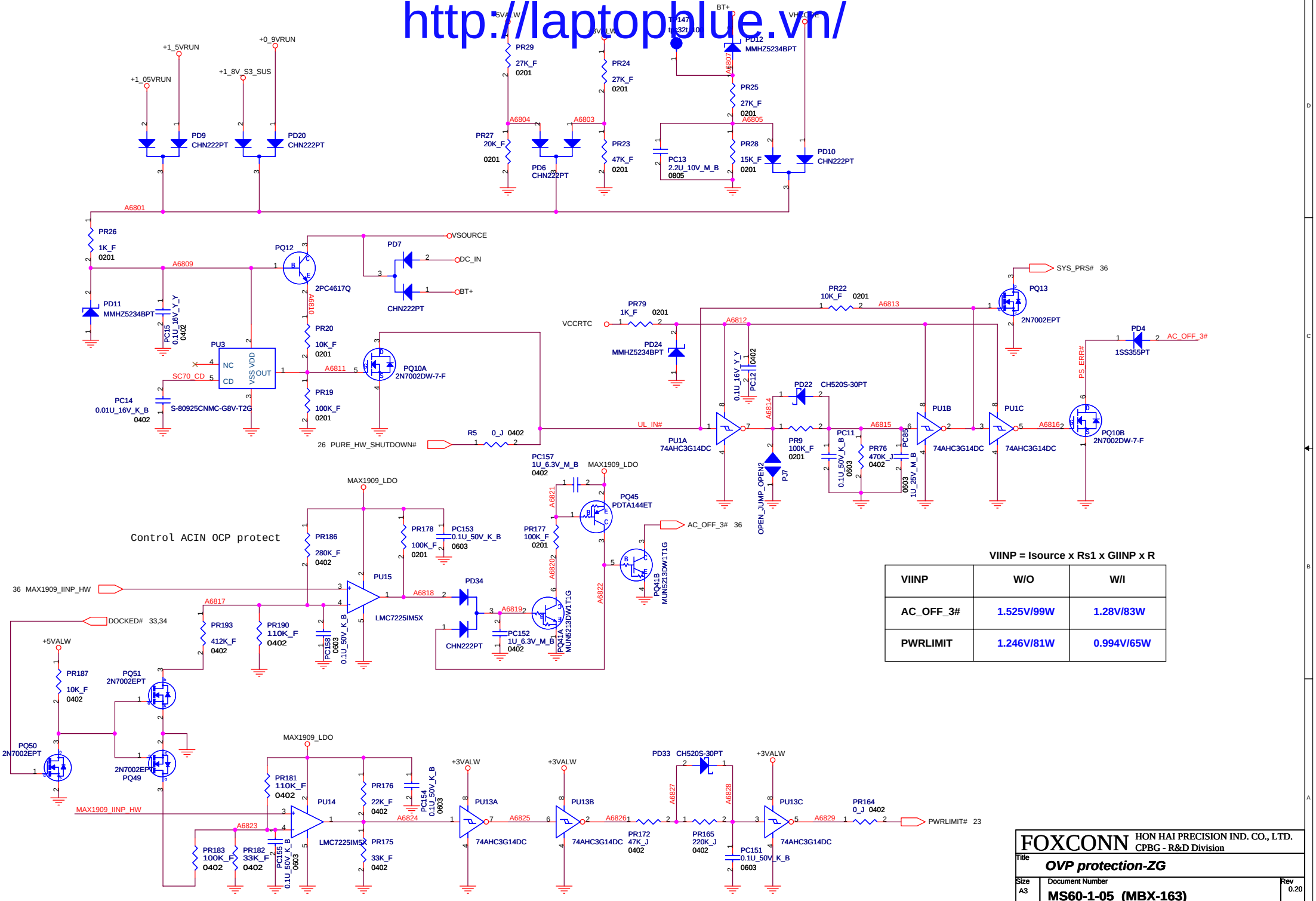
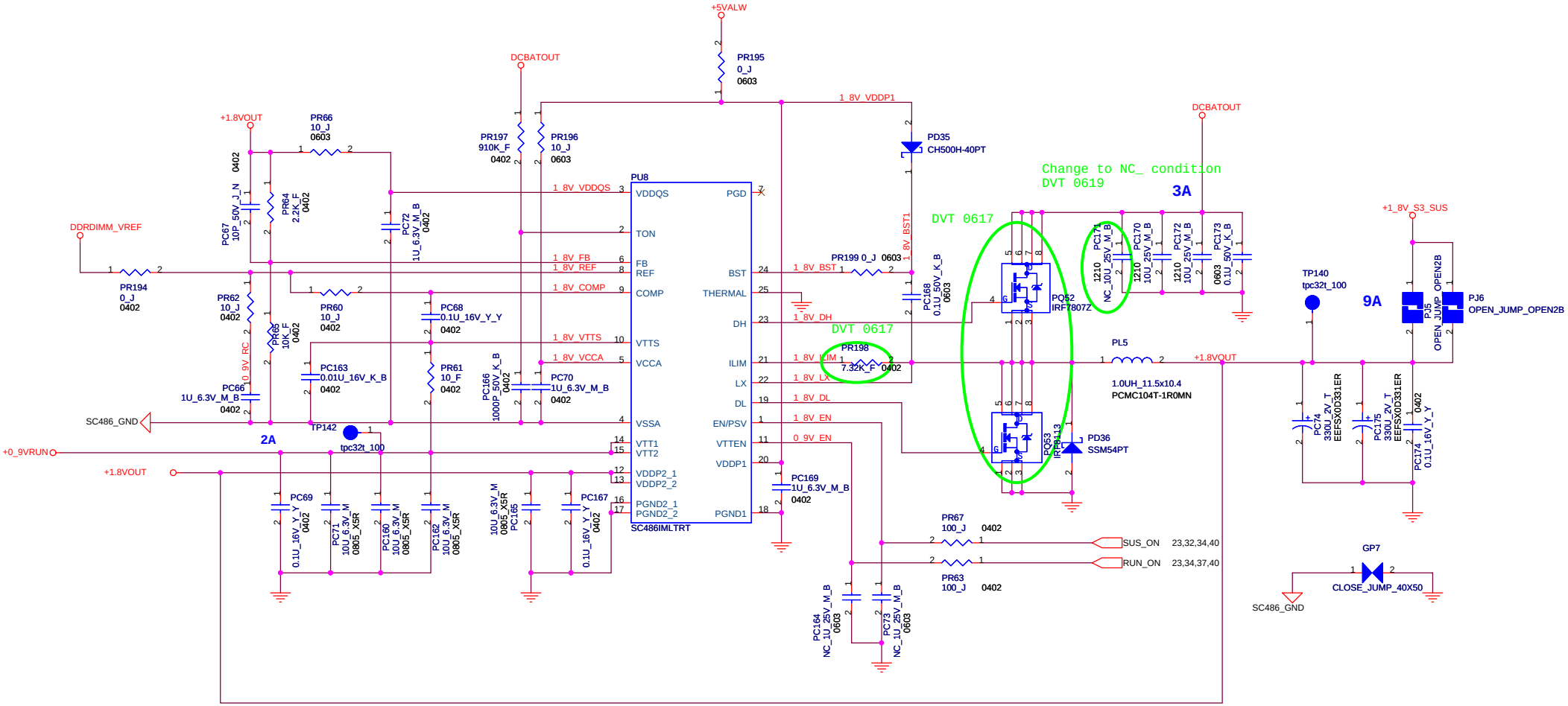


VIINP = Isource x Rs1 x GIINP x R

VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	OVP protection-ZG
Size A3	Document Number MS60-1-05 (MBX-163) Rev 0.20
Date: Monday, June 19, 2006	Sheet 41 of 47



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number MS60-1-05_(MBX-163)	Rev 0.20
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close to clk gen (For EMI)

Length as short as possible.

Pin Straps Pin 53/59/60/64 100K ohm pull-up	
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU_2_ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)

CALISTOGA Chip HOST

CPU

ICH7M SATA

ICH7 DMI

CALISTOGA DOT96

CALISTOGA SSCK

Add R522,R523 to replace RP13 DVT 0616

SM bus Address :
1101001 (ICH7)
For clock generator

CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor
(R69,R40,R41,R70,R1126,R1127)
If EVT ok, del them in DVT

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: CLOCK GEN

Size: A3 | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

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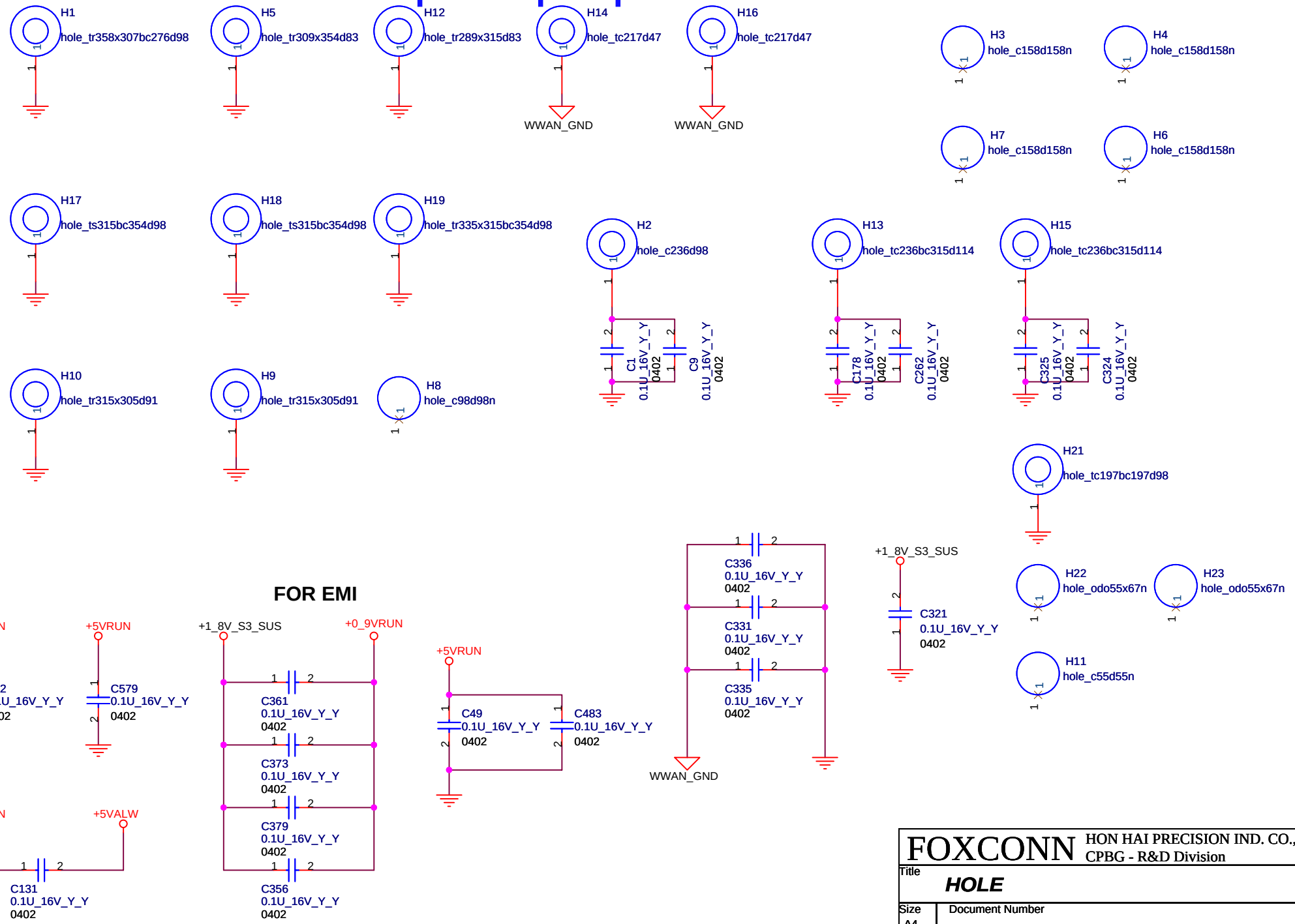


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: ***HOLE***		
Size: A4	Document Number: **MS60-1-05 (MBX-163)**	Rev: 0.20
Date: Monday, June 19, 2006	Sheet 44 of 47	

MS60 Power On Sequerce Timing

Version : 0.0
Modified date : 2/14/2006

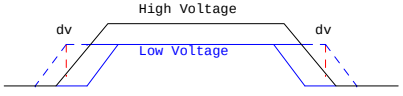
NOTE : (EC KB3910 Min. response time is 1ms)

1. T00 : R=47K , C = 0.1uF is ENE recommand value please refer to KB3910B0-AN4A-200
2. T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
   PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
3. T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
4. T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
5. T05 : RSMRST# active High to SLP_S5# avtive High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing
6. T06(Please reference Intel 16971 Page 301 of t234 timing
7. T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
8. T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
9. T09 : For MS01 current SPEC
10. T10 :Please refer to Intel 16971 Page 300 of t214 timing
11. T11 :Please refer to Intel 16971 Page 303 of t216 timing
12. T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
13. T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
14. T14 : For MS01 current SPEC Min. is 5 ms
15. DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
16. IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
17. In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
18. T15 : Please refer to MAX8771 datasheet
20. T16: Please refer to MAX8771 datasheet
21. T17 : Please refer to Intel CK410(14690) page 53
22. T18 : The ICH7 drives PLTRST# active a mininum of 1ms when initiated through the Reset Control register I/O Register CF9h)
23. CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
24. T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add dischage circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV

R/C delay (47K/ 0.1uF)



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms

T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min :1s

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Power Sequence

Size: C | Document Number: MS60-1-05 (MBX-163) | Rev: 0.20

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<1>2006/3/28 remove U36.SW no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.
P/N : FOX_UB11193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.
P/N : FOXCONN_QT8H0506_64T2R_4F

<5>2006/3/29 Change PC359,PC360 to 10uF
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.
P/N : FOX_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.
P/N : FOXCONN_BP34063_B6012_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV_ENABLE_EC logic dur to BIOS Code merge issue.add new component :
U53.U54 P/N : 14-74AHC1G-0800
R762 P/N : 1R-0000103-J200
R763 P/N : 1R-0000000-J200
R764 P/N : 1R-0000104-J200
Delete R176.R177

<12>2006/3/31 Add C20,C21,C22,C31,C33,C68 for EMI slution.
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :
U55.U56 P/N : 15-RT9702A-0000
C521.C522 P/N : 1C-2Y20104-Y000
R569.R573 P/N : 1R-0000105-J200
C870.C871 P/N : 1C-2Y30225-Y000
C535.C751 P/N : 1C-2B70106-M100
Deleted Component :
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32.CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31.CN32.CN33 CN34 Connector change.
P/N : GB11261_1051_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR_MIZER circuit.
U6J GPIO10 with new signal "NV_PWR_MIZER"
new Components added and modified as below :
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.
and R66.R69.R98.R101 change to 120Ohm.
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V_S3_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.
P/N : 1C-2B20102-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118.R119.R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN_EXT_DEV_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :
PQ183 P/N : 17-2N7002D-W000
PR115 P/N : 1R-0000101-J200
PR103.PR114 P/N : 1R-0000104-F100
PC87 P/N : 1C-2B20103-M000
PQ38 P/N : 17-S14800B-DY00
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :
PR273 P/N : 1R-0000103-F200
PR773 P/N : 1R-0004992-F200
PQ20 P/N : 17-2N7002E-PT00
PR774 P/N : 1R-0000102-J200
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21~H24.

<48>2006/4/10 Rename Schematic Part referene.
new version since 4/11

<49>2006/4/11 change R68.R133.R100
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.
Add U37 P/N : 15-MAX809S-0000
Add R516 P/N : 1R-0000104-J200
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.
Add R517 P/N : 1R-0000103-J200
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.
P/N : 1R-0000100-J200

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MS60-L change list base on MS60-H

<58>2006/5/02 Del all NV_ components for L-model only.

<59>2006/5/03 Remove +1_8VRUN discharge circuit.Delete PR169,PQ44. Add PQ54 P/N:17-2N7002E-PT00

<60>2006/5/03 LED2 pin2,pin3 swap for Power LED color opposite issue

<61>2006/5/03 Change CAP93,CAP94 to NEC,TEPSGV0E337M9-12R,330uF,2.5V
P/N:1C-31T0337-MX00
Add CAP95 P/N:1C-31T0337-MX00

<62>2006/5/04 F1,F2,F3,F4,F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16,F17,F19 change to fuse,1.1A PTC type
P/N:1M-F06V1A1-F000

<63>2006/5/05 follow M/E change to exchange PCN1 pin1 & pin2 connection.Layout change placement form top side to bottom side.

<64>2006/5/05 Add GP14,GP15 open jump for repair conveniently

<65>2006/5/05 Add C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592 for 22uF_0805_6.3V shortage.

<66>2006/5/08 As to M/E assemble issue, we will need rotat 180degree about T/P module.So that R47 change to stuff

<67>2006/05/09 Rename CAP93,CAP94,CAP95 to PC93,PC94,PC176.And change component to Panasonic,EEFSX0D331ER,330uF,2V
P/N:1C-42T0337-MX00

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<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage.
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout convenient.

<70>2006/05/12 PR198 change to 5.6k/0402_1% to modify 1.8V OCP seting value.
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to ''FOX_MH11747-BR2D-4F'' for ME requirement.
P/N:2N-000400N-FKG0

<72>2006/05/12 CN3,CN8 change to ''FOX_GB5RF120-1200-7F'' for ME requirement.
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to ''FFOXCONN_GB5RF060_1200_7F'' for ME requirement.
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to ''FOXCONN_UB11193_C1304_4F'' for ME requirement.
P/N:1N-0004000-FEG0

<75>2006/05/12 CN9 change to ''FOXCONN_HS8206E'' for ME requirement.
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to ''Panasonic,EEFSX0D331ER'' .Del PC75 for power requirement.
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.
P/N:17-2N7002D-W000
P/N:1R-0000331-J300
P/N:1R-0000104-F100
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to ''FOXCONN_PZ4782A_2743_01'' for ME requirement.
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.
P/N:1C-2N20100-J000

<80>2006/05/18   CN12,CN16 change footprint to ''FOXCONN_UB11193_C1304_4F_HM'' for DFM.

<81>2006/05/18   Add R519,R520,C593,C594 on ''IAC_BITCLK'' signal for EMI requirement.
P/N:1R-0000000-J200
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to '' hole_tc236bc315d114'' for ME requirement.
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC_IN trace for EMI requirement.
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.
P/N:1R-0000000-J200

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DVT change list

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and connect GPIO_ODD_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form ''ALW_ON'' to ''ALW_ON_1'' for customer's requirement.
P/N : 1R-0000102-J200

<90>2006/06/16 PORT_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal ''VISTA_SUPPORT#'' that is connected form EC's pin99 to CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PR187 for ODD power plane.
P/N:17-SI2304-DS00
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.
P/N:17-1RF7807-2000
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT_IN power trace for EMI requirement.
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.
P/N:1C-2B30105-M000
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC_ condition for power requirement.

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