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Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2010-02-16

LA-7552P REV: 0.03

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Title: Cover Page

Size: B | Document Number: QBL60 LA-7552P | Rev: 0.03

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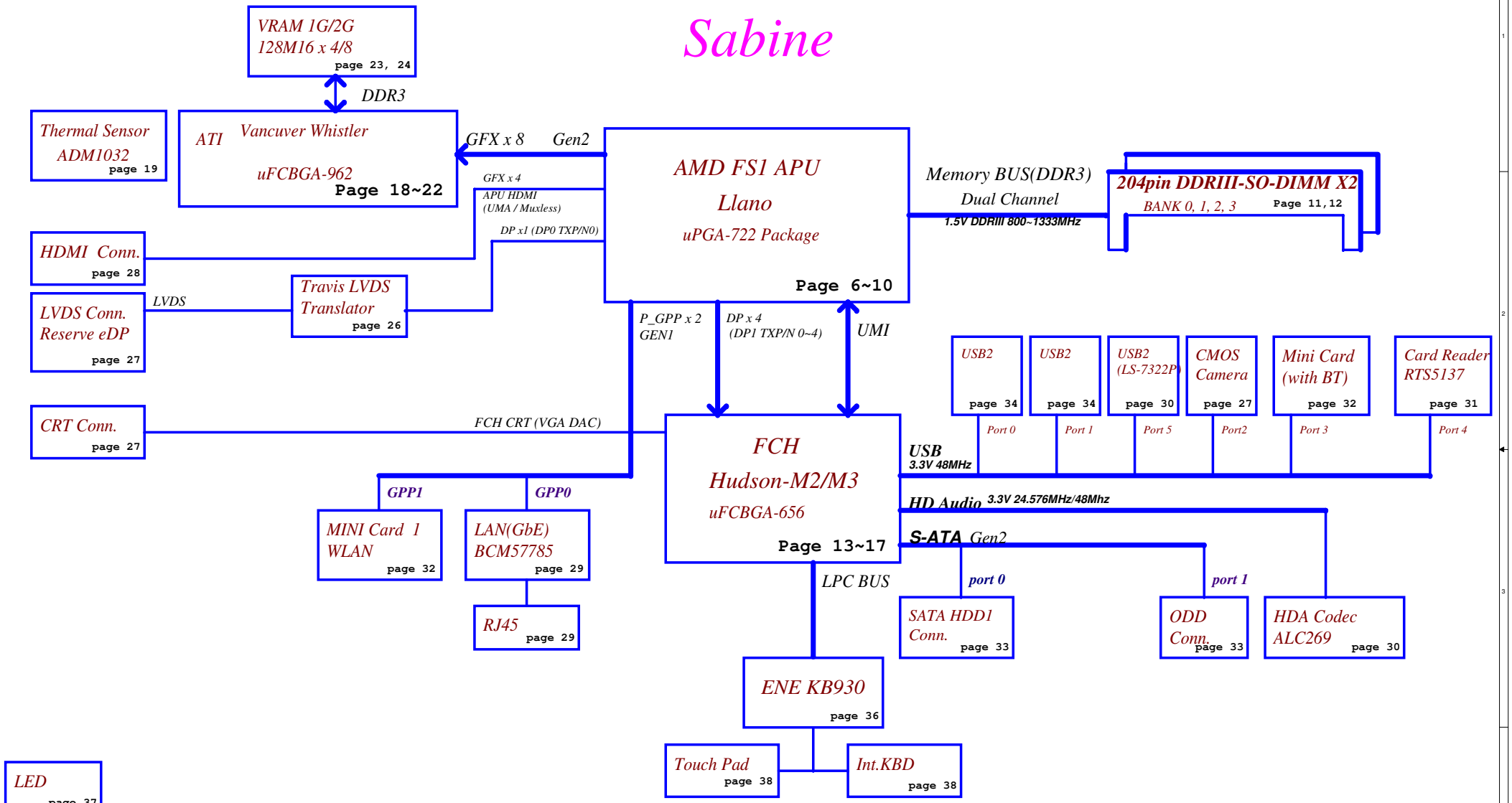
Model Name : QBL60

Sabine



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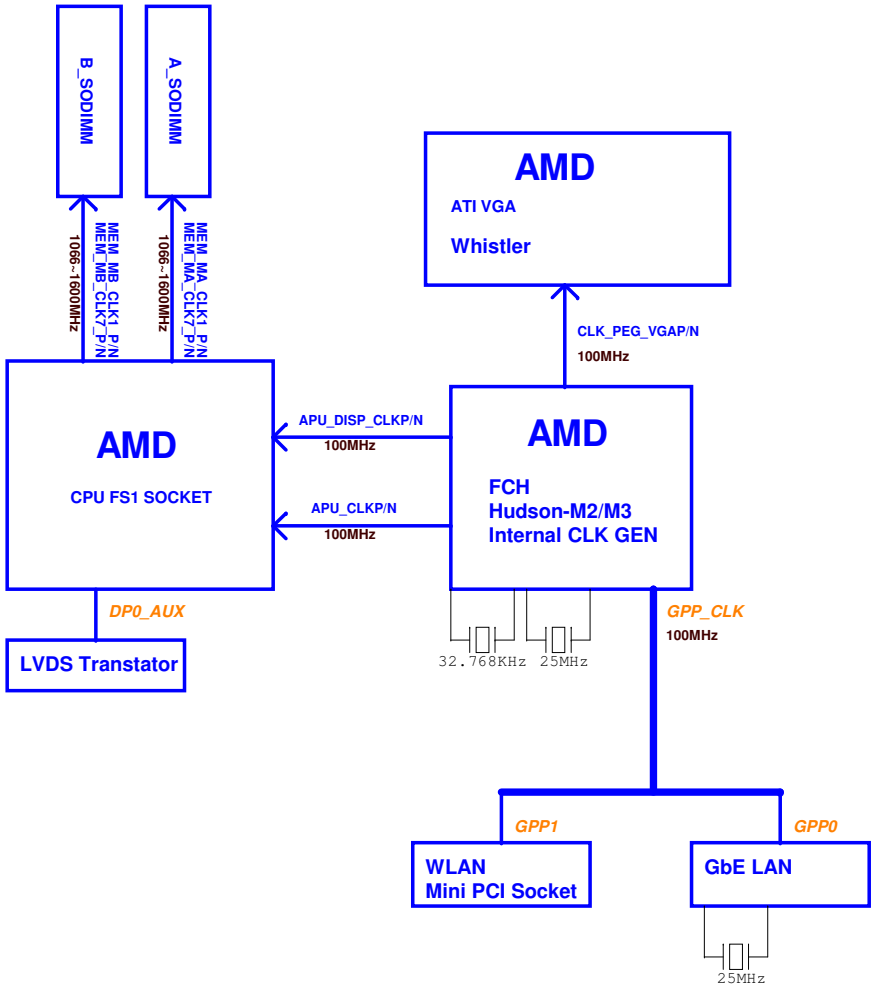
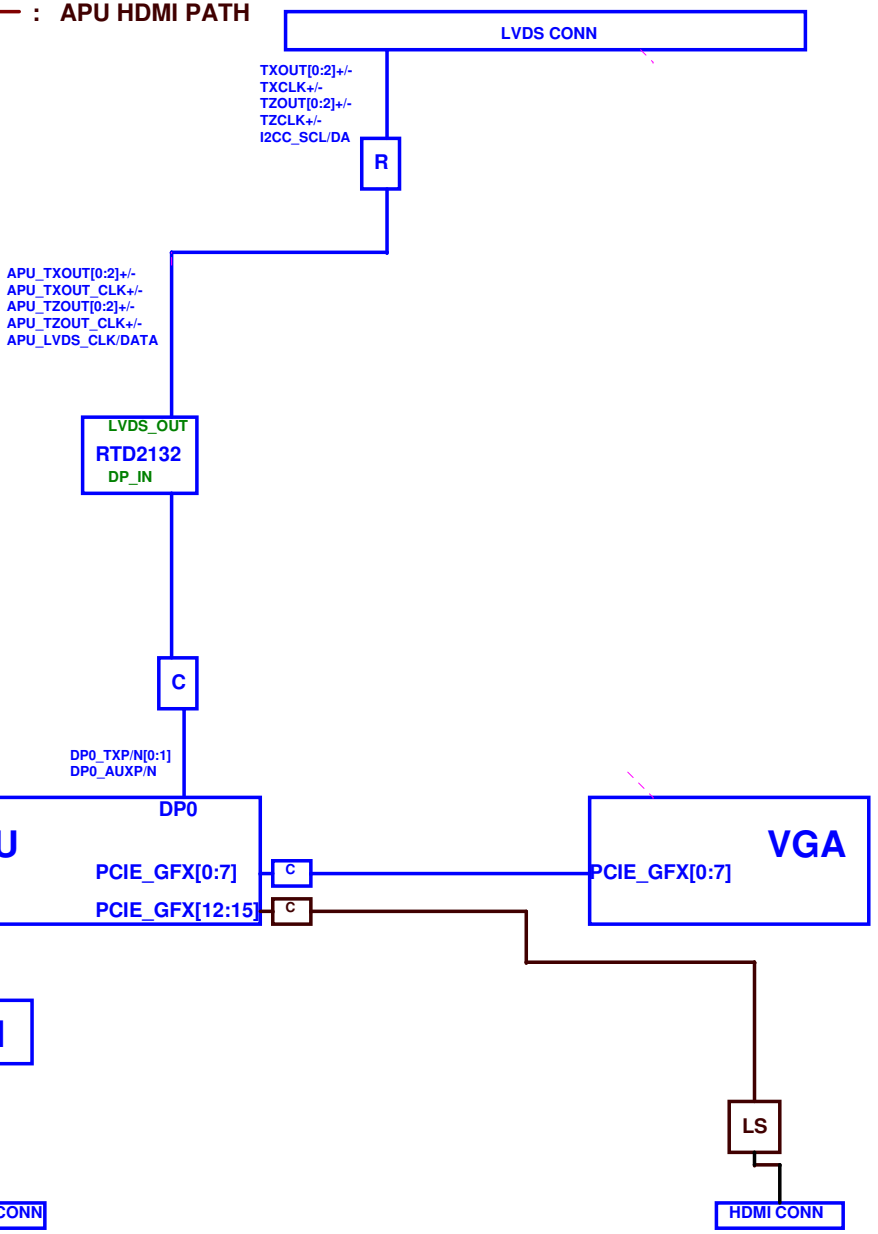
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043I90

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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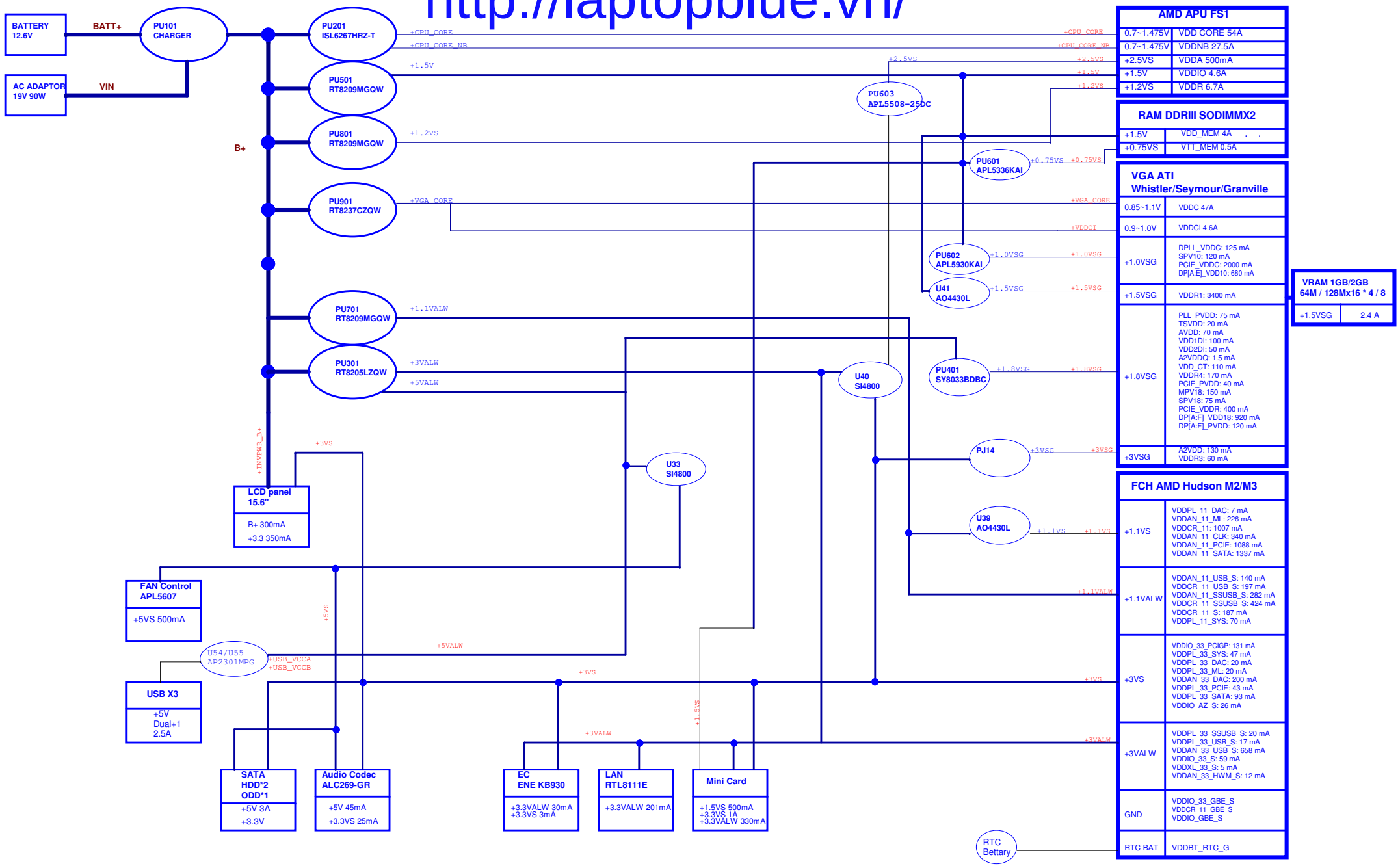

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Title: POWER DELIVERY CHART

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18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

JCPU1A — CONN@ — PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0	
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0	
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1	
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1	
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2	
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2	
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C923 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3	
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3	
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C925 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P4	
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4	
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5	
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PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932 VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7	
	R5	P_GFX_RXP8	P_GFX_TXP8	T4					
	R6	P_GFX_RXN8	P_GFX_TXN8	T5					
	R8	P_GFX_RXP9	P_GFX_TXP9	R2					
	R9	P_GFX_RXN9	P_GFX_TXN9	R3					
	P7	P_GFX_RXP10	P_GFX_TXP10	P2					
	P8	P_GFX_RXN10	P_GFX_TXN10	P1					
	N5	P_GFX_RXP11	P_GFX_TXP11	P4					
	N6	P_GFX_RXN11	P_GFX_TXN11	P5					
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	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12				
	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13				
	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13				
	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14				
	L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14				
	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15				
	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15				

For UMA Mux.

2 / 1 / 0 / CK — To HDMI

29 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29	GLAN
29 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29	
32 PCIE_DTX_C_FRX_P1	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2	PCIE_FTX_DRX_P1	C952	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32	WLAN
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	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

GPP

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13
13 UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C957	0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13
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13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963	0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13

UMI-LINK

+1.2VS — R539 1 2 P_ZVDDP 196_0402_1%
P_ZVDDP K5
P_ZVSS K4 — P_ZVSS R540 1 2 196_0402_1% — GND

AMD_TOPEDO_FS-1

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

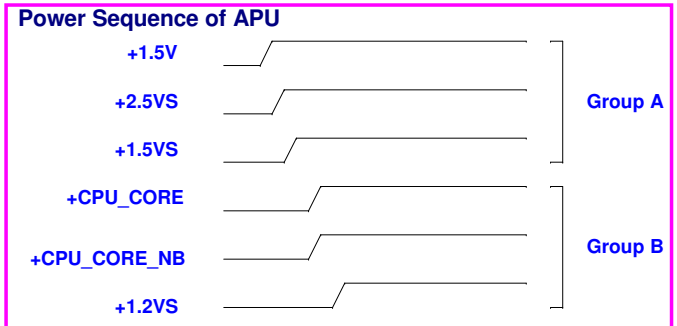
C935 1 2 0.1U_0402_16V4Z
+3VS — R535 1 2 31.6K_0402_1% — R536 1 2 30K_0402_1%

Q9
8,14 APU_SID — APU_SID — EC_SMB_DA — R537 1 2 0_0402_5% — EC_SMB_DA2 19,26,36
BSH111 1N_SOT23-3

Q10
8,14 APU_SIC — APU_SIC — EC_SMB_CK — R538 1 2 0_0402_5% — EC_SMB_CK2 19,26,36
BSH111 1N_SOT23-3

To EC

Power Sequence of APU



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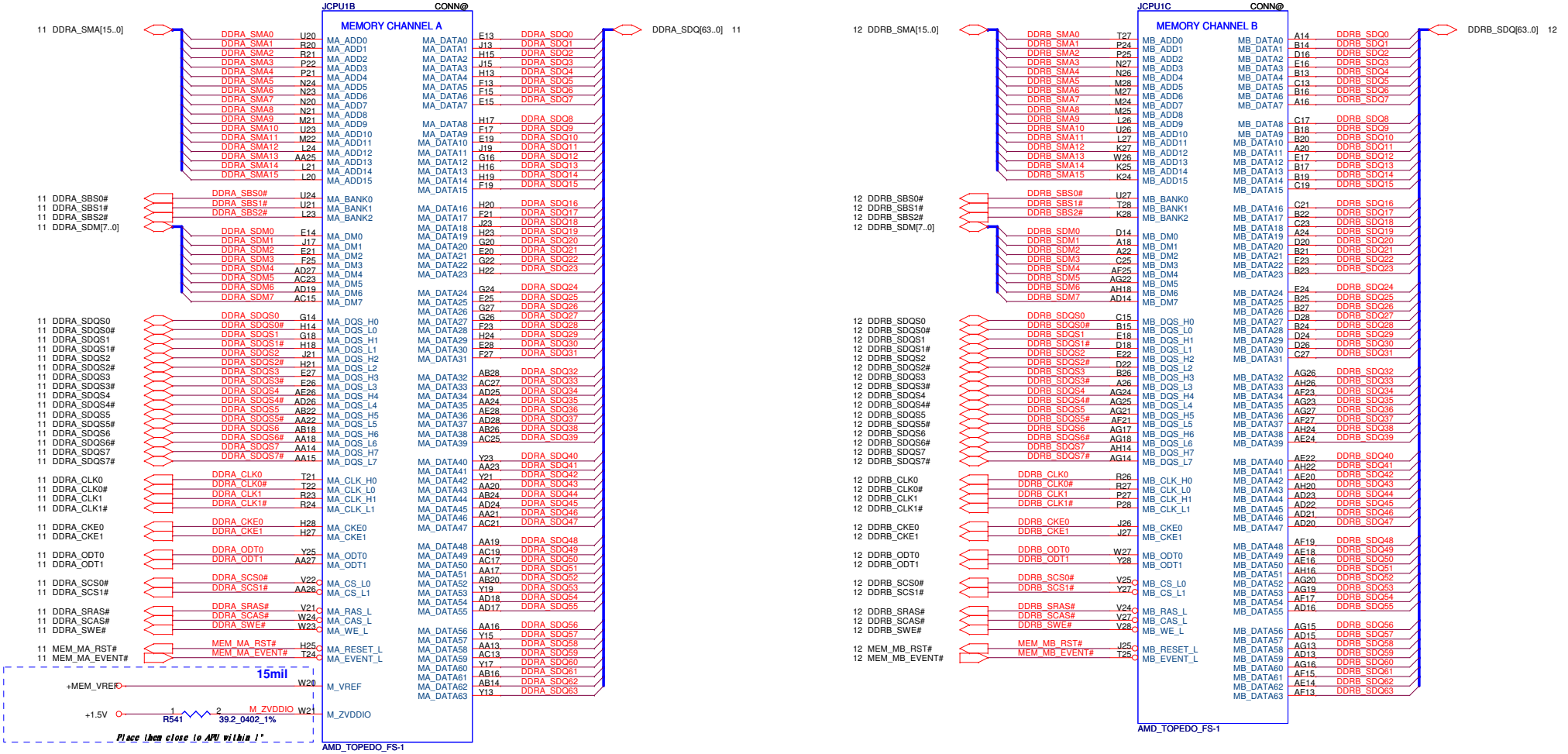
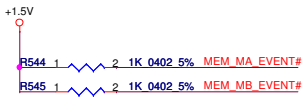
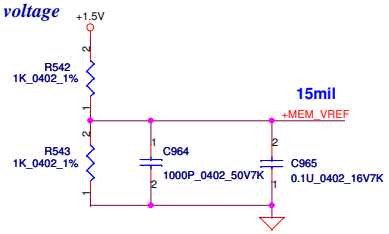


EVENT# pull high



0.75V reference voltage



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Title: AMD FS1 DDRIII I/F

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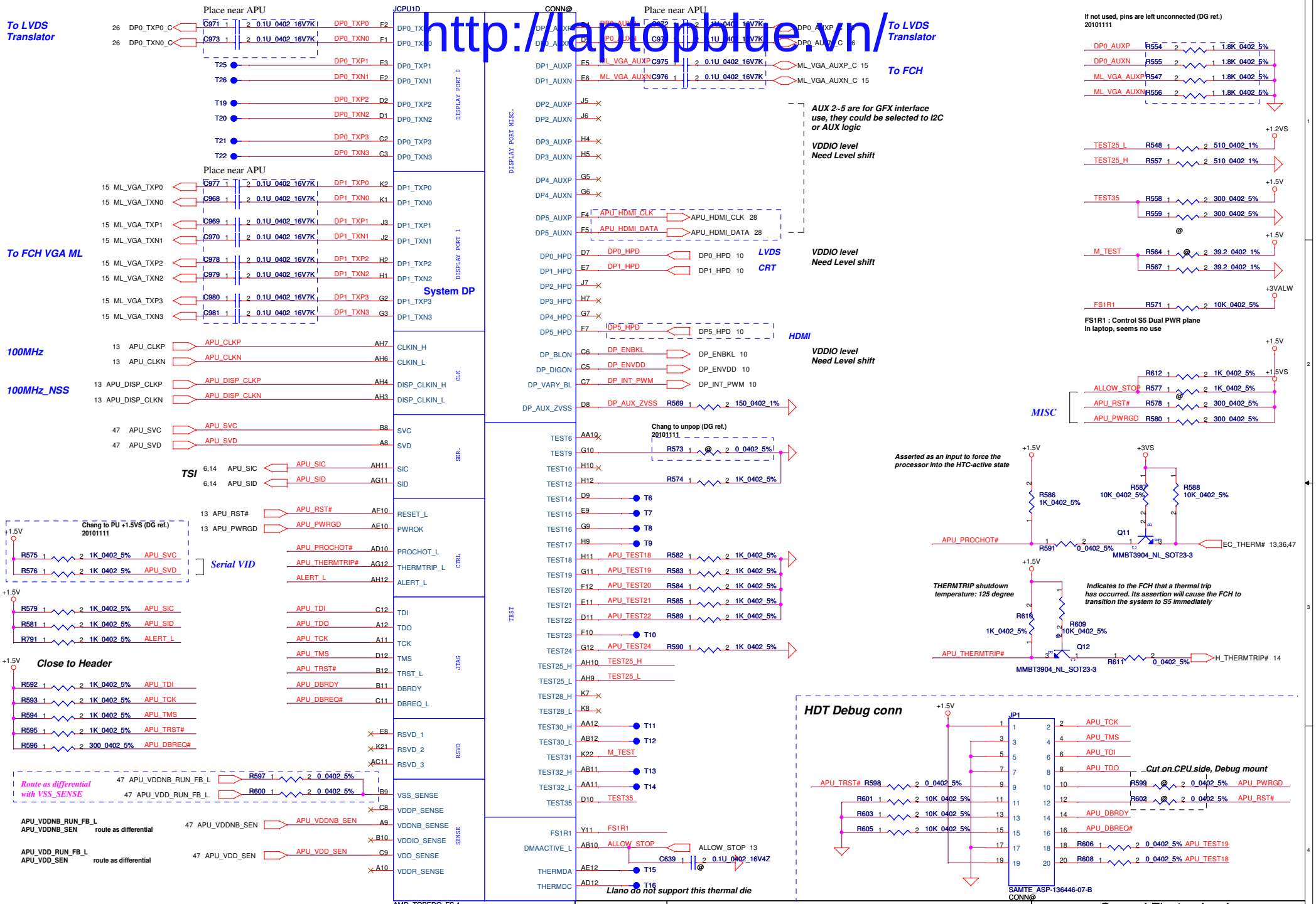

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Title: AMD FS1 Display / MISC / HDT

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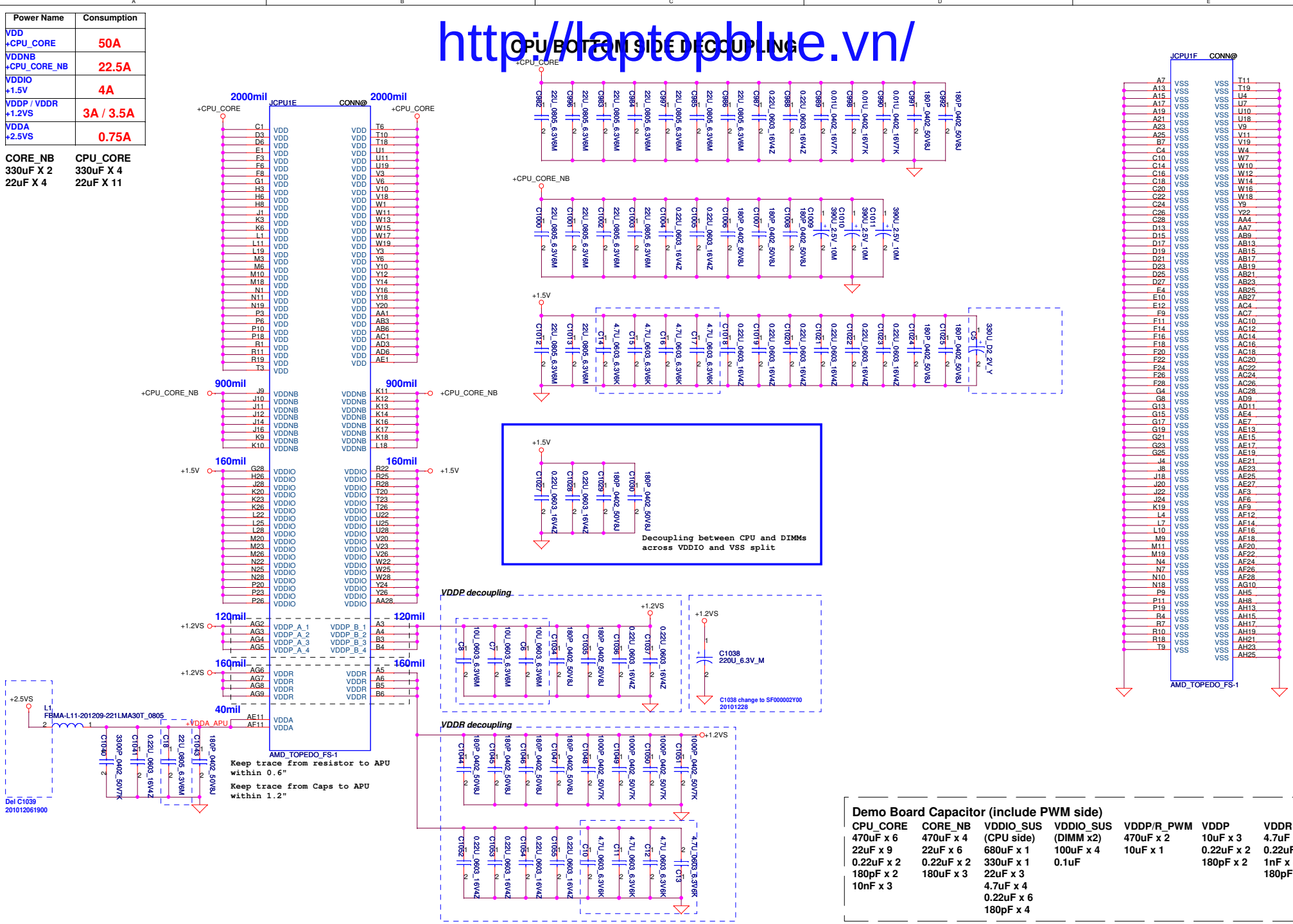
CPU BOTTOM SIDE DECOUPLING

Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11



Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

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Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

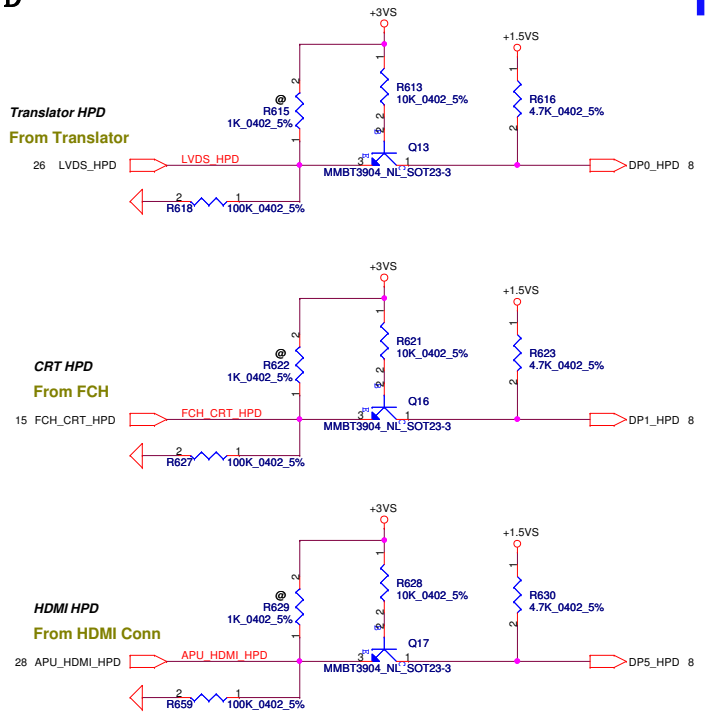
Title: AMD FS1 PWR / GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.02

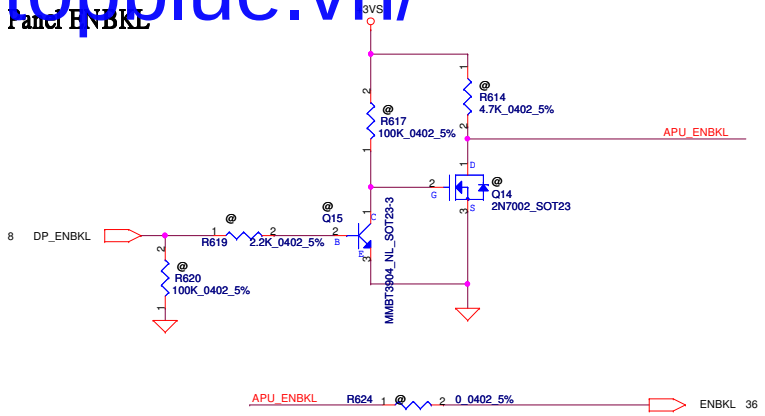
Date: Tuesday, February 22, 2011 | Sheet 9 of 49

http://laptopblue.vn/

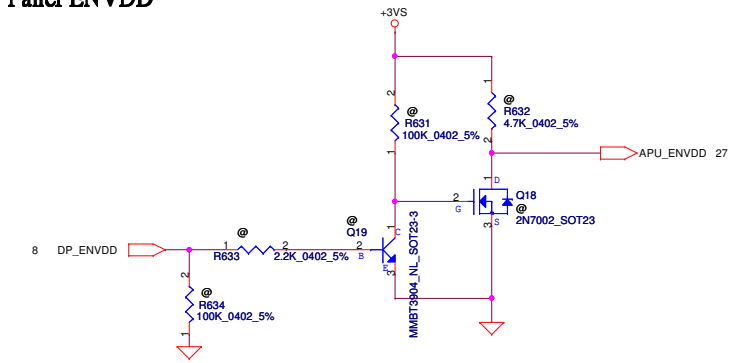
HPD



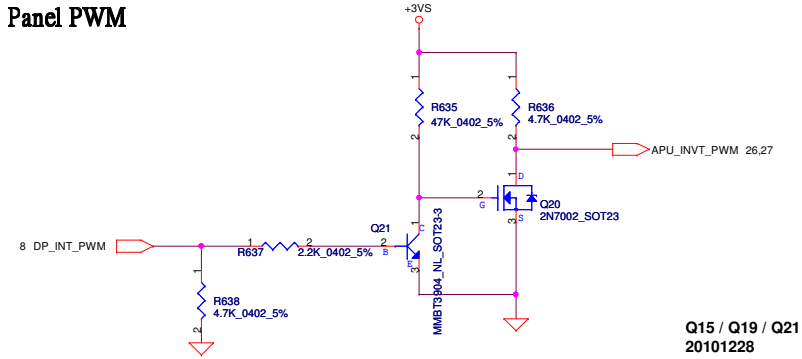
Panel ENBKL



Panel ENVDD



Panel PWM



Q15 / Q19 / Q21 change to SB000006A00
20101228

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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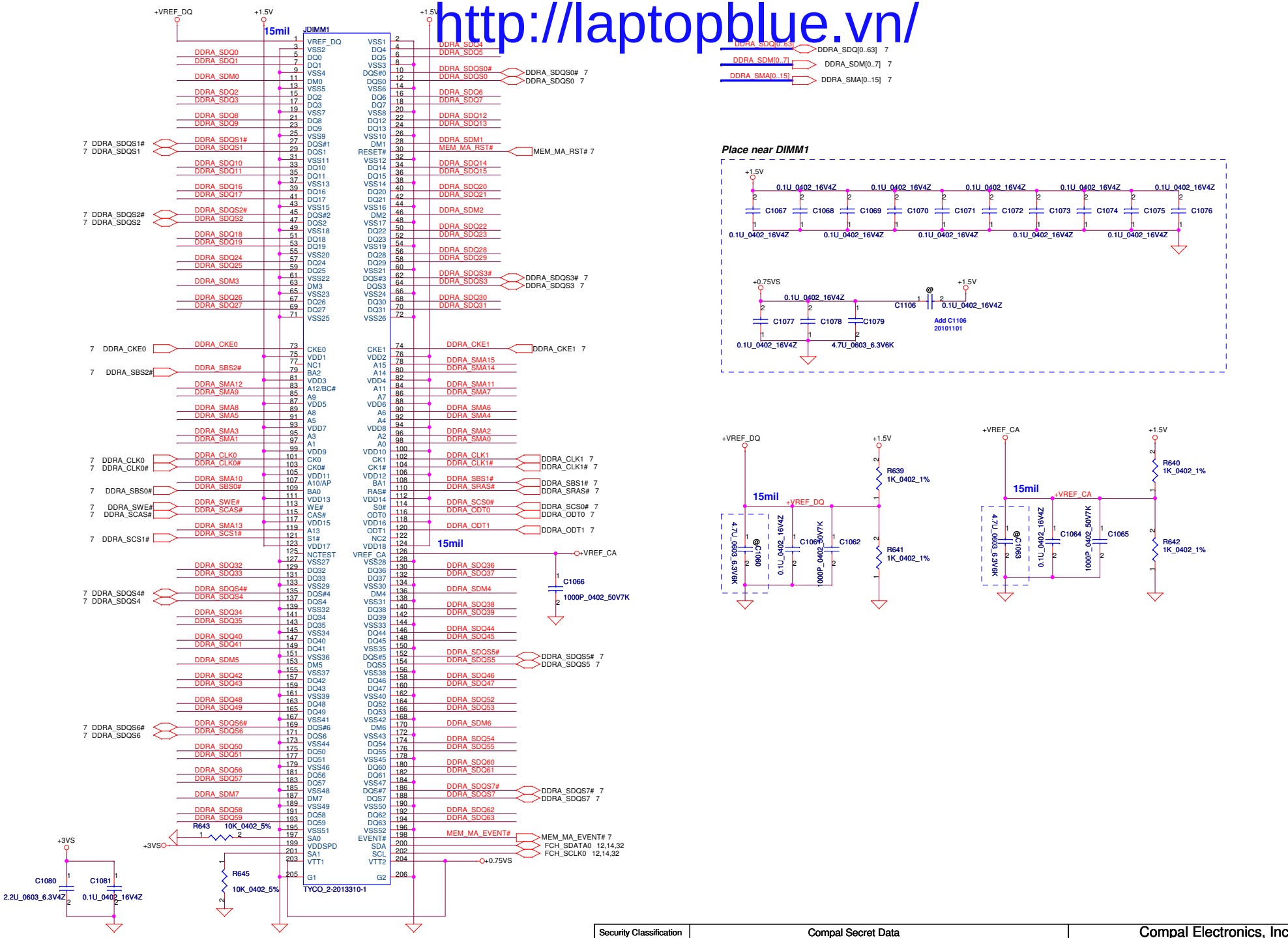
Title	AMD FS1 Singal Level Shifter		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 10 of 49		

http://laptopblue.vn/



DIMM_A STD H:9.2mm

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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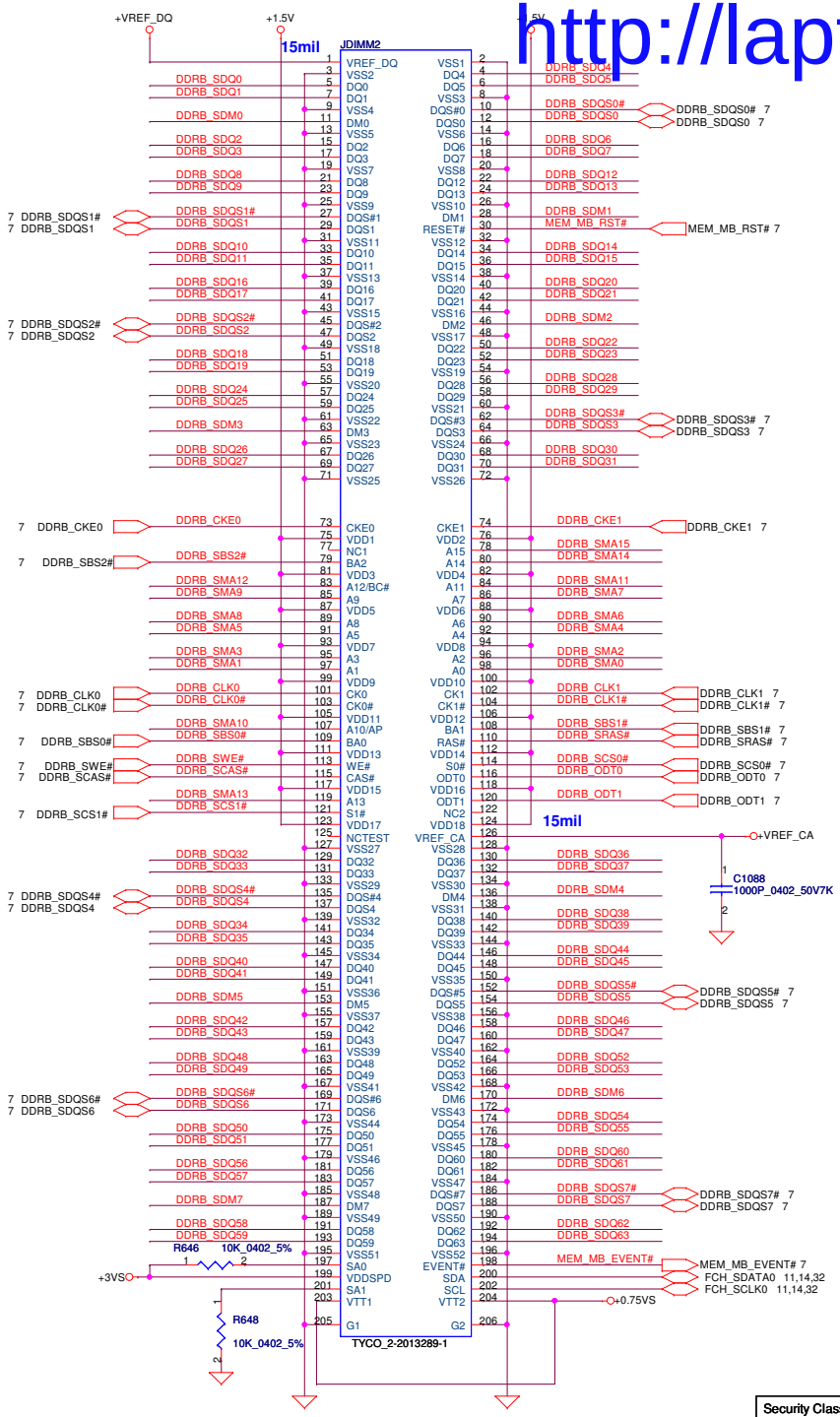
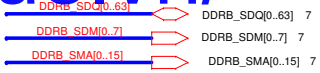
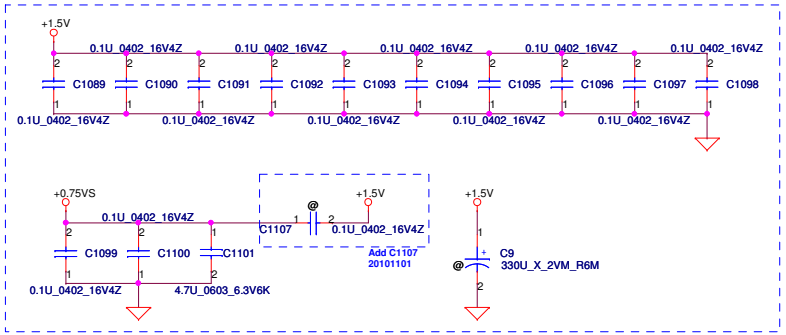
Compal Electronics, Inc.			
Title: DDRIII SO-DIMM 1			
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 11 of 49		

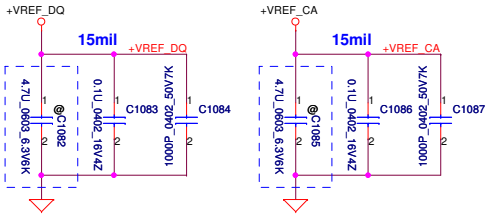
http://laptopblue.vn/





Place near DIMM2





DIMM_B STD H:5.2mm

<Address: 01>

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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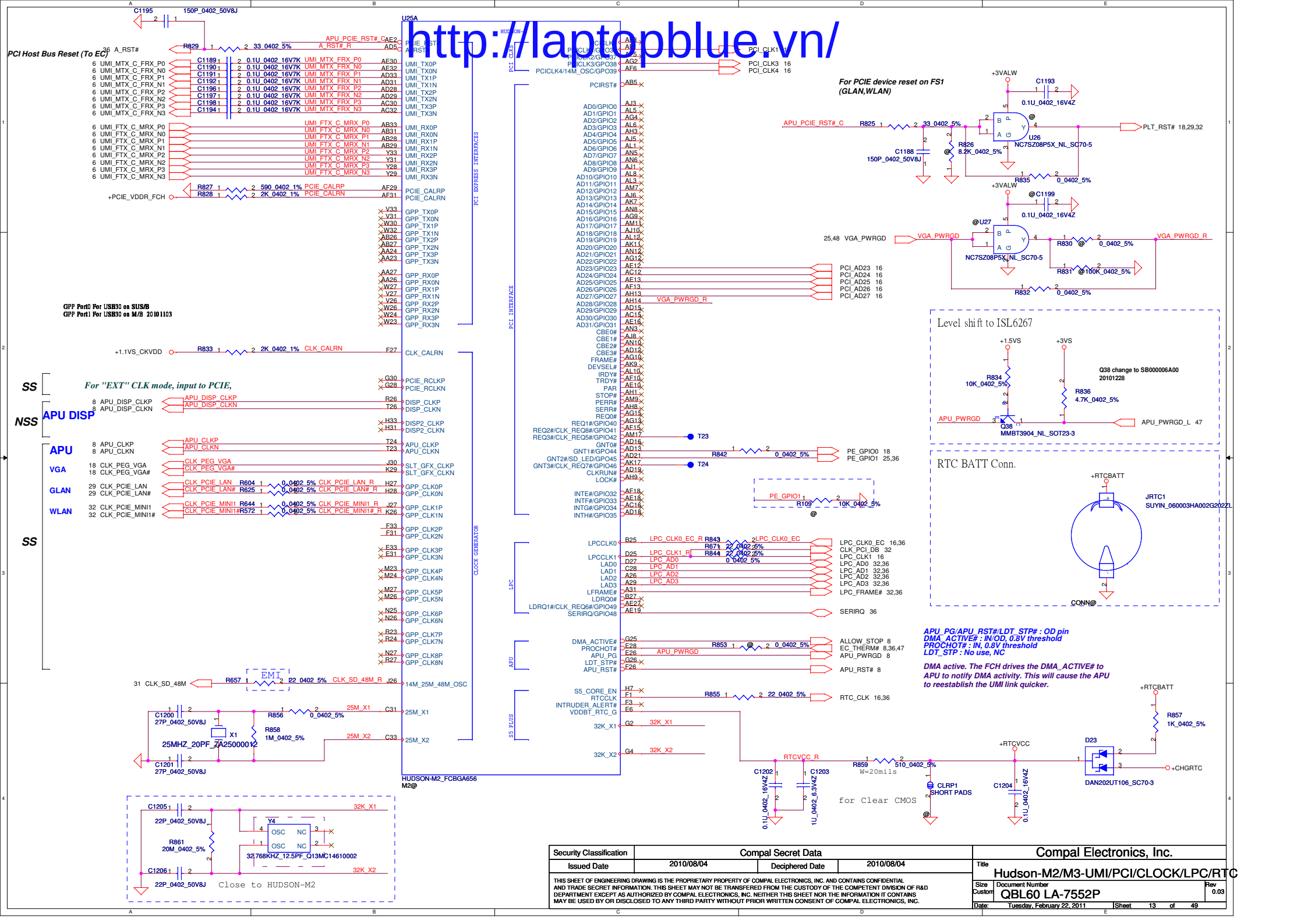
Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 12 of 49

http://laptopblue.vn/



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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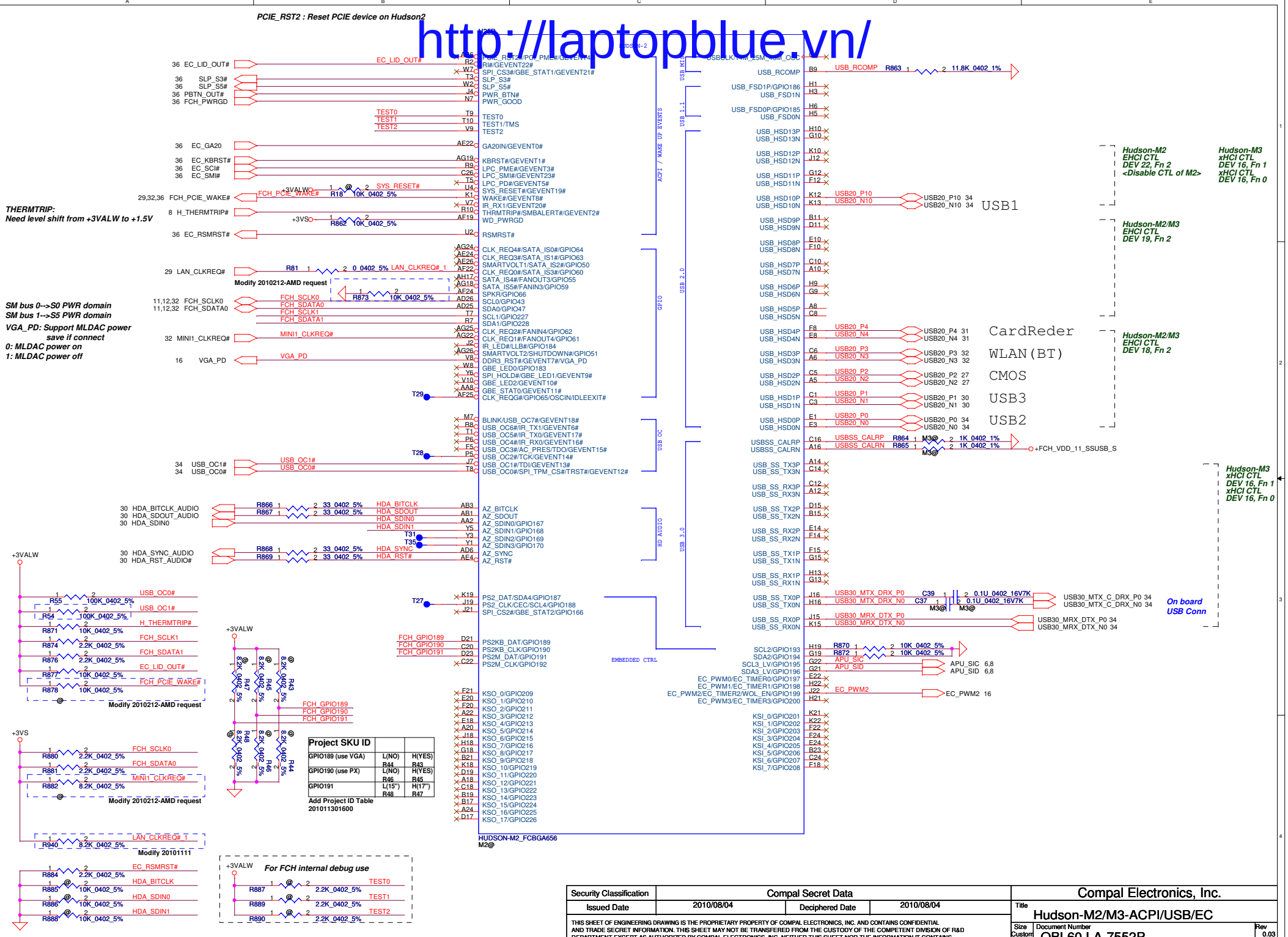
Compal Electronics, Inc.			
Title	Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 13 of 49		

http://laptopblue.vn/



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 14 of 49

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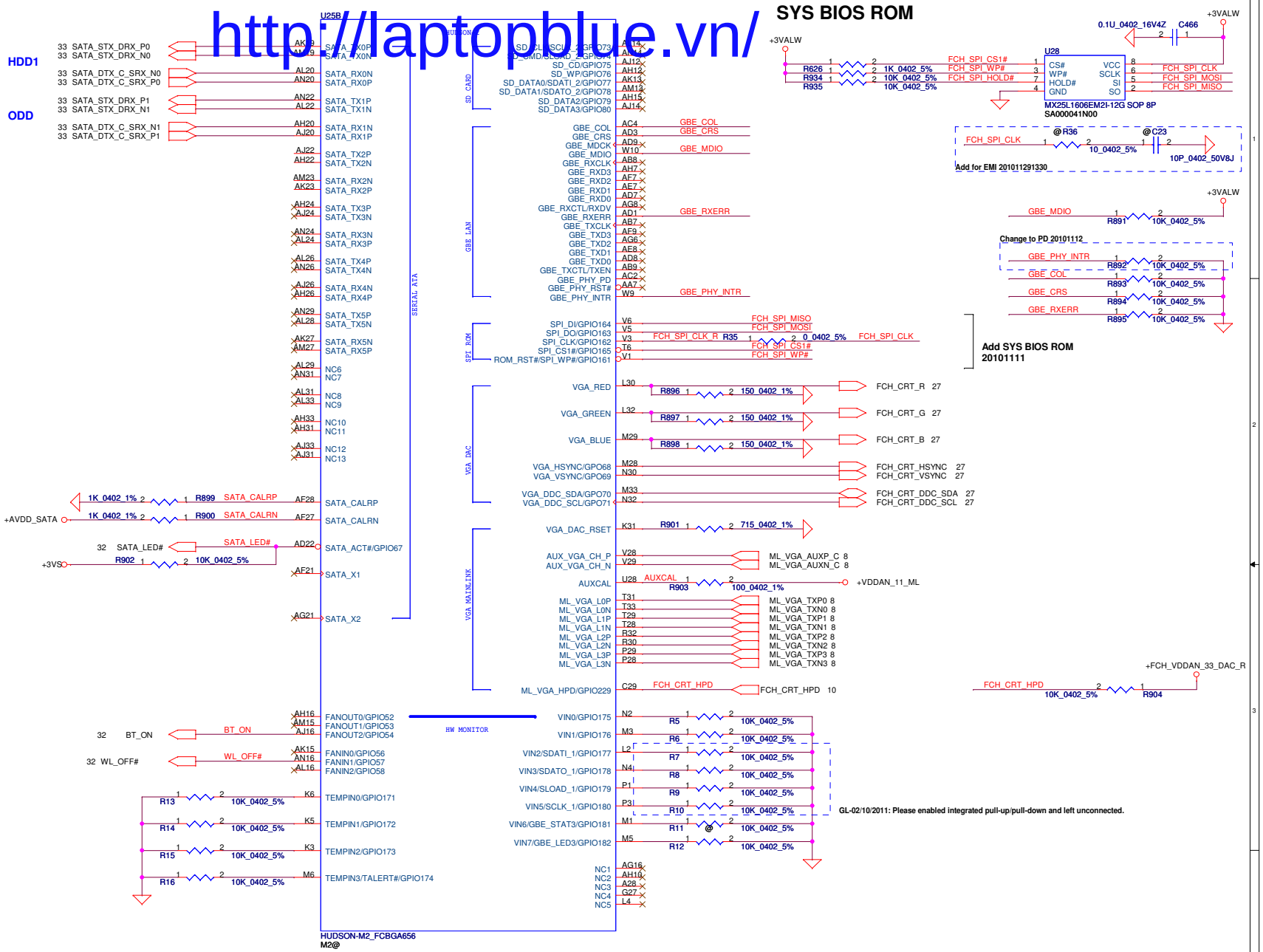

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.	
Title	Hudson-M2/M3-SATA/GBE/HWM
Size: Custom	Document Number: QBL60 LA-7552P
Rev	0.03
Date: Tuesday, February 22, 2011	Sheet 15 of 49

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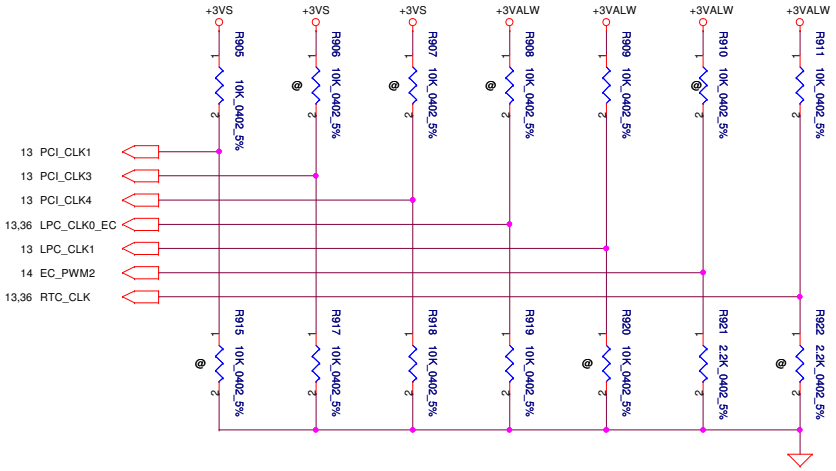
STRAP PINS

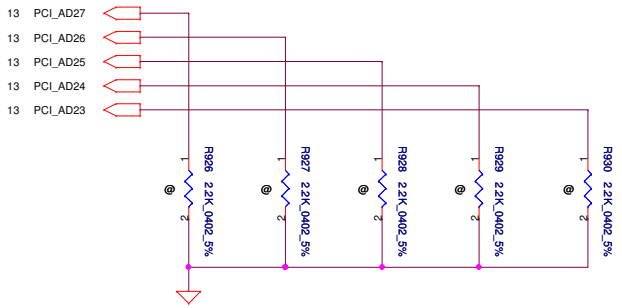
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

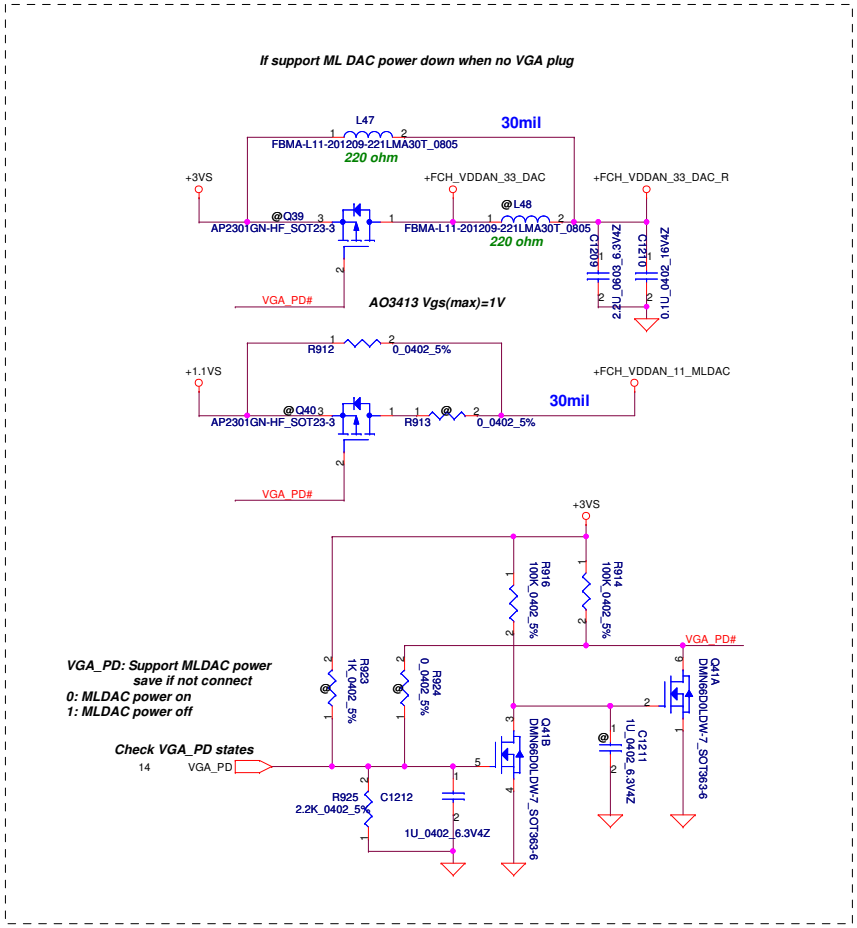


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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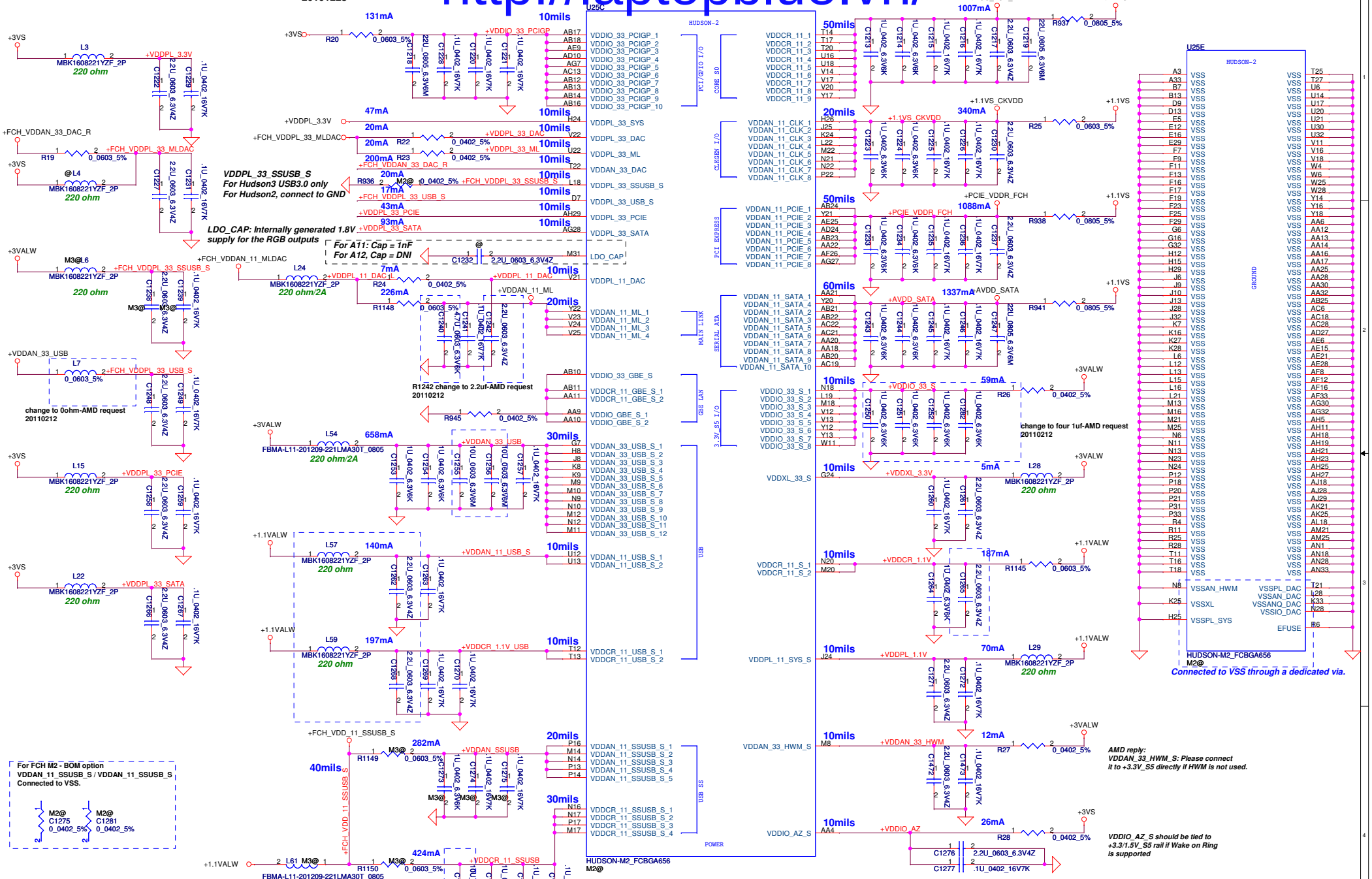
Compal Electronics, Inc.			
Title	Hudson-M2/M3-STRAP		
Size: Custom	Document Number: QBL60 LA-7552P		Rev: 0.03
Date: Tuesday, February 22, 2011	Sheet 16 of 49		

http://laptopblue.vn/

C1218 / C1219 / C1247 Change to SE00000010
20101228



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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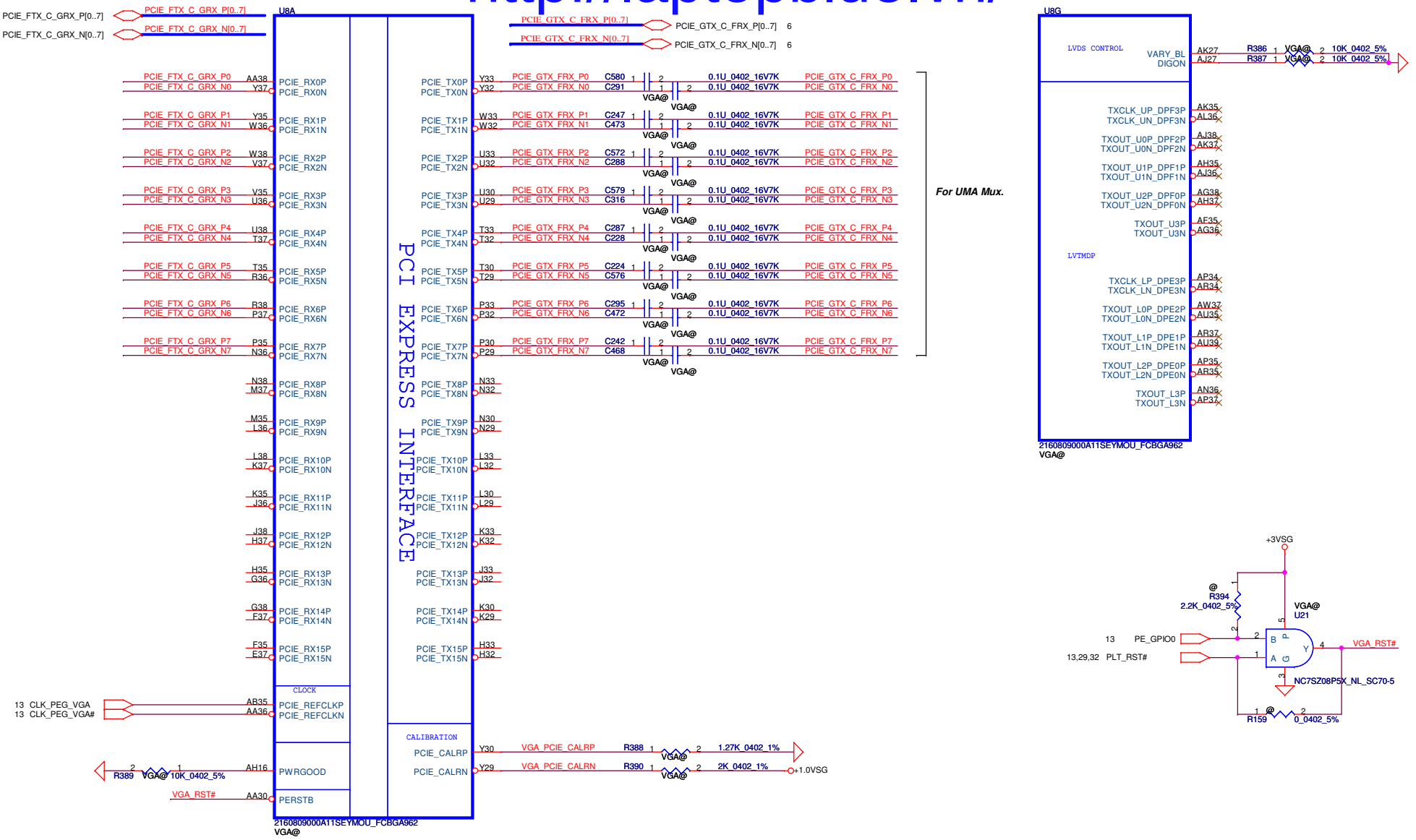
GFX PCIE LANE REVERSAL

http://laptopblue.vn/

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need



For UMA Mux.

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this feature on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

External VGA Thermal Sensor

U9 VGA@ ADM1032ARMZ-2REEL_MSOP8

Q8A DMN66D0LDW-7_SOT363-6

Q8B DMN66D0LDW-7_SOT363-6

VRAM ID

GPIO5 fast-power reduction:
HW control will casue display disturb
should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

GPIO7 Controls backlight on/off.
Active High ,need external PD
if GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

ROM

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

SM010030010
200ma 120ohm@100mhz DCR 0.2

Future ASIC call MLPS.
OLD ASIC is Fan PWM

120ohm/0.3A

Back compatibility(Manhattan)

Whistler and Seymour
Except A2VSSQ change to TSVSSQ,
others are NC

GPIO8 Serial-ROM output from ROM, GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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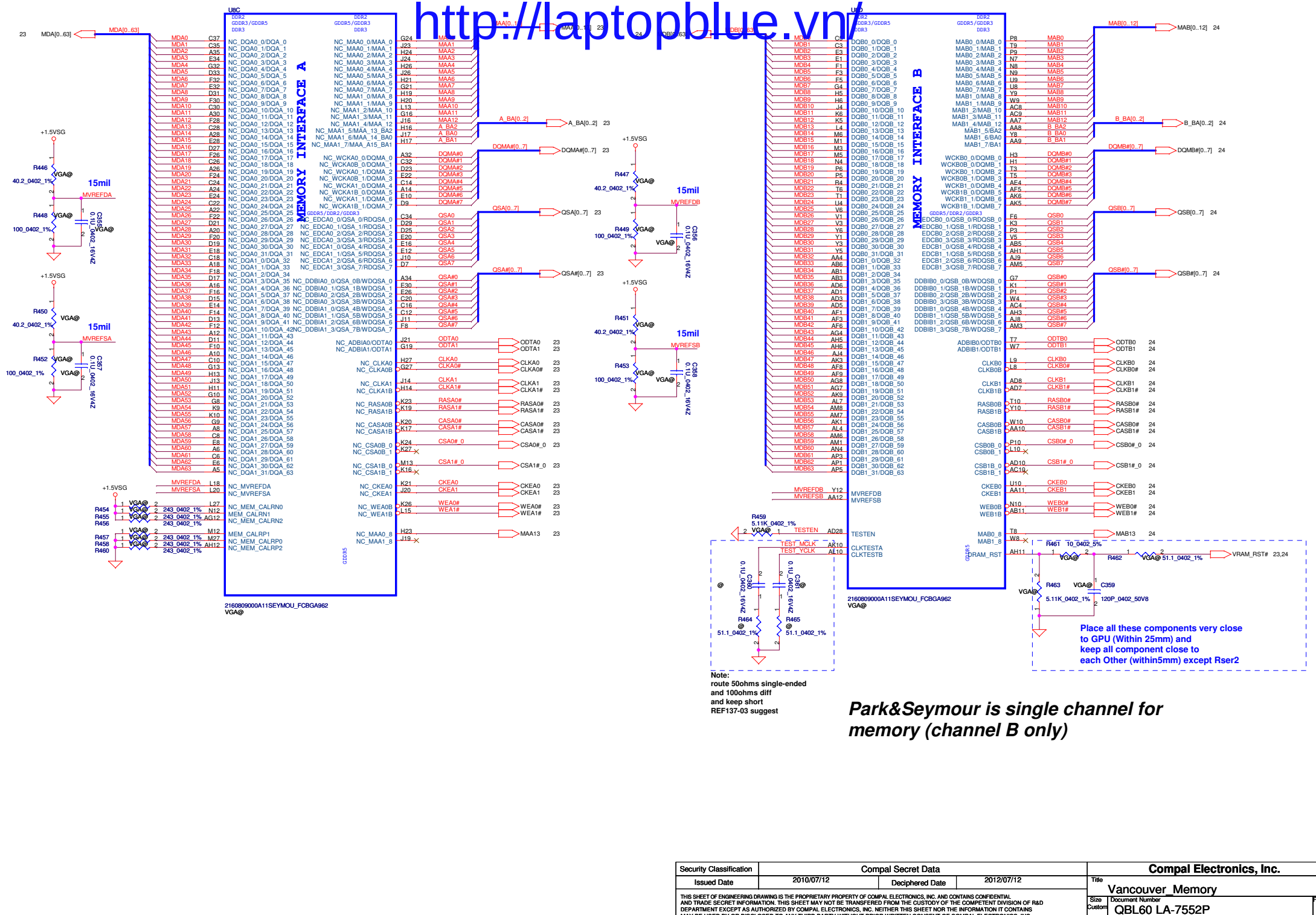

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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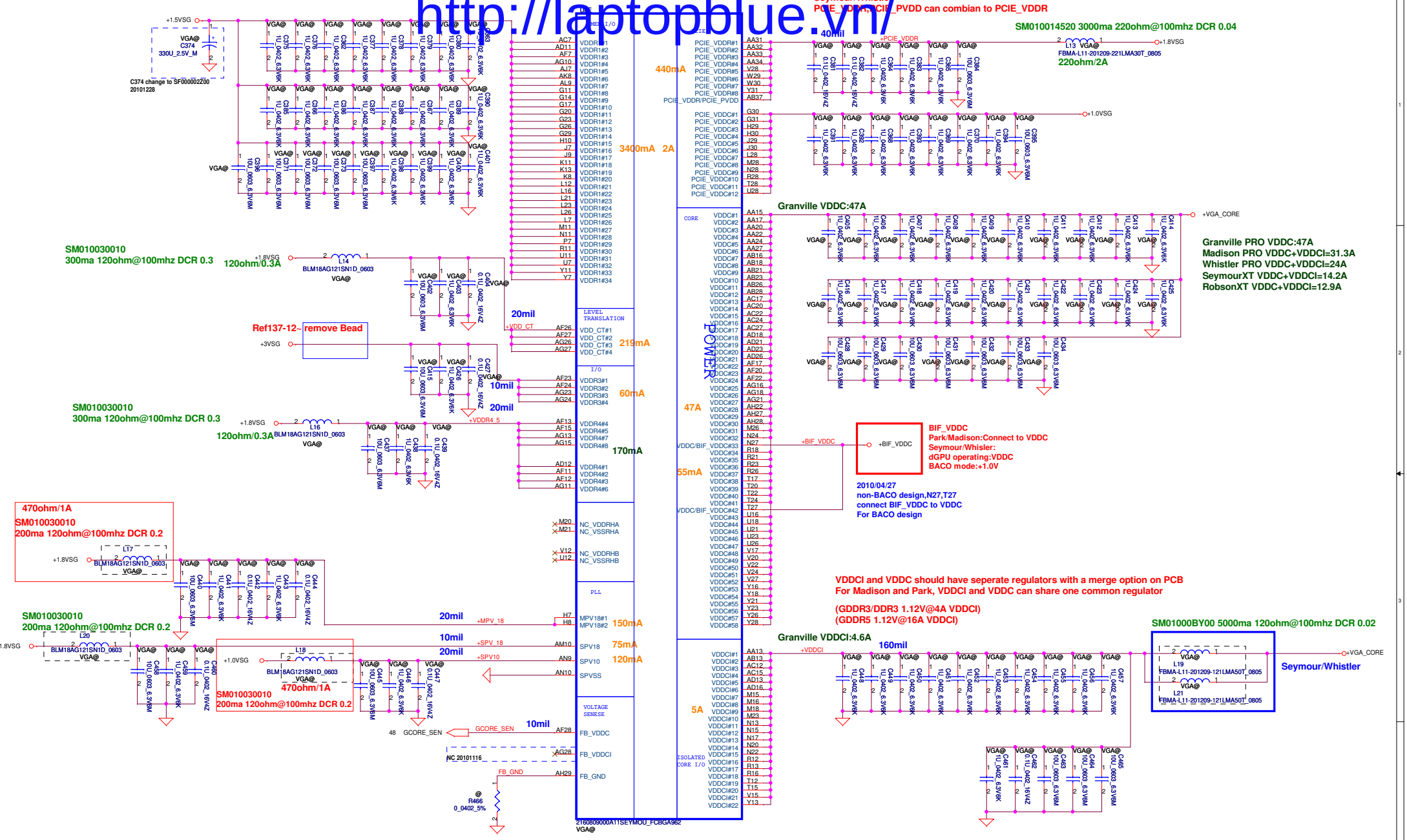

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

PCIE_VSS#1 PCIE_VSS#2 PCIE_VSS#3 PCIE_VSS#4 PCIE_VSS#5 PCIE_VSS#6 PCIE_VSS#7 PCIE_VSS#8 PCIE_VSS#9 PCIE_VSS#10 PCIE_VSS#11 PCIE_VSS#12 PCIE_VSS#13 PCIE_VSS#14 PCIE_VSS#15 PCIE_VSS#16 PCIE_VSS#17 PCIE_VSS#18 PCIE_VSS#19 PCIE_VSS#20 PCIE_VSS#21 PCIE_VSS#22 PCIE_VSS#23 PCIE_VSS#24 PCIE_VSS#25 PCIE_VSS#26 PCIE_VSS#27 PCIE_VSS#28 PCIE_VSS#29 PCIE_VSS#30 PCIE_VSS#31 PCIE_VSS#32 PCIE_VSS#33 PCIE_VSS#34 PCIE_VSS#35

GND

GND#100 GND#101 GND#102 GND#103 GND#104 GND#105 GND#106 GND#107 GND#108 GND#109 GND#110 GND#111 GND#112 GND#113 GND#114 GND#115 GND#116 GND#117 GND#118 GND#119 GND#120 GND#121 GND#122 GND#123 GND#124 GND#125 GND#126 GND#127 GND#128 GND#129 GND#130 GND#131 GND#132 GND#133 GND#134 GND#135 GND#136 GND#137 GND#138 GND#139 GND#140 GND#141 GND#142 GND#143 GND#144 GND#145 GND#146 GND#147 GND#148 GND#149 GND#150 GND#151 GND#153 GND#154 GND#155 GND#156 GND#157 GND#158 GND#159 GND#160 GND#161 GND#163 GND#164 GND#165 GND#166 GND#167 GND#168 GND#169 GND#170 GND#171 GND#172 GND#173 GND#174 GND#175 GND#152 GND#162

GND#1 GND#2 GND#3 GND#4 GND#5 GND#6 GND#7 GND#8 GND#9 GND#10 GND#11 GND#12 GND#13 GND#14 GND#15 GND#16 GND#17 GND#18 GND#19 GND#20 GND#21 GND#22 GND#23 GND#24 GND#25 GND#26 GND#27 GND#28 GND#29 GND#30 GND#31 GND#32 GND#33 GND#34 GND#35 GND#36 GND#37 GND#38 GND#39 GND#40 GND#41 GND#42 GND#43 GND#44 GND#45 GND#46 GND#47 GND#48 GND#49 GND#50 GND#51 GND#52 GND#53 GND#54 GND#55 GND#56 GND#57 GND#58 GND#59 GND#60 GND/PX_EN#61 GND#62 GND#63 GND#64 GND#65 GND#66 GND#67 GND#68 GND#69 GND#70 GND#71 GND#72 GND#73 GND#74 GND#75 GND#76 GND#77 GND#78 GND#79 GND#80 GND#81 GND#82 GND#83 GND#84 GND#85 GND#86 GND#87 GND#88 GND#89 GND#90 GND#91 GND#92 GND#93 GND#94 GND#95 GND#96 GND#97 GND#98

VSS_MECH#1 VSS_MECH#2 VSS_MECH#3

2160809000A11SEYMOU_FCBGA962
VGA@

REF137-13 update

PX_EN PX_EN 25

PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

U8H

Manhatann:300mA
Seymour:150mA

20mil +DPABCD_VDD18 AP20 AP21 DPCD/DPC_VDD18#1 DPCD/DPC_VDD18#2
20mil +DPABCD_VDD10 AP13 AT13 DPCD/DPC_VDD10#1 DPCD/DPC_VDD10#2
AN17 AP16 AP17 AW14 AW16 DP/DPC_VSSR#1 DP/DPC_VSSR#2 DP/DPC_VSSR#3 DP/DPC_VSSR#4 DP/DPC_VSSR#5
20mil +DPABCD_VDD18 AP22 AP23 DPCD/DPD_VDD18#1 DPCD/DPD_VDD18#2
20mil +DPABCD_VDD10 AP14 AP15 DPCD/DPD_VDD10#1 DPCD/DPD_VDD10#2

Manhatann:220mA
Seymour:110mA

AN19 AP18 AP19 AW20 AW22 DP/DPD_VSSR#1 DP/DPD_VSSR#2 DP/DPD_VSSR#3 DP/DPD_VSSR#4 DP/DPD_VSSR#5

R467 150_0402_1% VGA@ AW18 DPCD_CALR

DP mode:300mA
LVDS mode:440mA

20mil +DPEF_VDD18 AH34 AJ34 DPEF/DPE_VDD18#1 DPEF/DPE_VDD18#2
20mil +DPEF_VDD10 AL33 AM33 DPEF/DPE_VDD10#1 DPEF/DPE_VDD10#2
AN34 AP39 AR39 AU37 DP/DPE_VSSR#1 DP/DPE_VSSR#2 DP/DPE_VSSR#3 DP/DPE_VSSR#4

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L26 MBK1608221YZF_2P VGA@
+1.8VSG
FootPrint
VGA@ C478 10U_0603_6.3V6M
VGA@ C479 1U_0402_6.3V6K
VGA@ C480 0.1U_0402_16V4Z

20mil +DPEF_VDD18 AF34 AG34 DPEF/DPF_VDD18#1 DPEF/DPF_VDD18#2
20mil +DPEF_VDD10 AK33 AK34 DPEF/DPF_VDD10#1 DPEF/DPF_VDD10#2
AF39 AH39 AK39 AL34 AM34 DP/DPF_VSSR#1 DP/DPF_VSSR#2 DP/DPF_VSSR#3 DP/DPF_VSSR#4 DP/DPF_VSSR#5

R470 VGA@ 150_0402_1% AM39 DPEF_CALR

DP mode:220mA
LVDS mode:240mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L27 MBK1608221YZF_2P VGA@
+1.0VSG
FootPrint
VGA@ C481 10U_0603_6.3V6M
VGA@ C482 1U_0402_6.3V6K
VGA@ C483 0.1U_0402_16V4Z

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

2160809000A11SEYMOU_FCBGA962
VGA@

DPAB_CALR

20mil +DPABCD_VDD18 AN24 AP24 DPAB/DPA_VDD18#1 DPAB/DPA_VDD18#2
20mil +DPABCD_VDD10 AP31 AP32 DPAB/DPA_VDD10#1 DPAB/DPA_VDD10#2
AN27 AP27 AP28 AW24 AW26 DP/DPA_VSSR#1 DP/DPA_VSSR#2 DP/DPA_VSSR#3 DP/DPA_VSSR#4 DP/DPA_VSSR#5
20mil +DPABCD_VDD18 AP25 AP26 DPAB/DPB_VDD18#1 DPAB/DPB_VDD18#2
20mil +DPABCD_VDD10 AN33 AP33 DPAB/DPB_VDD10#1 DPAB/DPB_VDD10#2
AN29 AP29 AP30 AW30 AW32 DP/DPB_VSSR#1 DP/DPB_VSSR#2 DP/DPB_VSSR#3 DP/DPB_VSSR#4 DP/DPB_VSSR#5

R468 150_0402_1% VGA@ AW28

300mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23 MBK1608221YZF_2P VGA@
+1.8VSG
FootPrint
VGA@ C469 10U_0603_6.3V6M
VGA@ C470 0.1U_0402_16V4Z
VGA@ C471 1U_0402_6.3V6K

220mA
SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L25 MBK1608221YZF_2P VGA@
+1.0VSG
FootPrint
VGA@ C475 0.1U_0402_16V4Z
VGA@ C476 1U_0402_6.3V6K
VGA@ C477 10U_0603_6.3V6M

20mA 10mil +DPABCD_VDD18 AU28 AV27 DPAB_VDD18/DPA_PVDD DP_VSSR/DPA_PVSS
20mA 10mil +DPABCD_VDD18 AV29 AR28 DPAB_VDD18/DPB_PVDD DP_VSSR/DPB_PVSS
20mA 10mil +DPABCD_VDD18 AU18 AV17 DPCD_VDD18/DPC_PVDD DP_VSSR/DPC_PVSS
20mA 10mil +DPABCD_VDD18 AV19 AR18 DPCD_VDD18/DPD_PVDD DP_VSSR/DPD_PVSS
20mA 10mil +DPEF_VDD18 AM37 AN38 DPEF_VDD18/DPE_PVDD DP_VSSR/DPE_PVSS
20mA 10mil +DPEF_VDD18 AL38 AM35 DPEF_VDD18/DPF_PVDD DP_VSSR/DPF_PVSS

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

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ZZZ1 — 1GVRAM-SAM — X76L01@
ZZZ2 — 2GVRAM-SAM — X76L02@
ZZZ3 — 1GVRAM-HYNIX — X76L03@
ZZZ4 — 2GVRAM-HYNIX — X76L04@

U11 / U12 / U13 / U14 — 96-BALL SDRAM DDR3 — K4B1G1646E-HC12_FBGA96 — X76@

Pull high for Madison and Park...

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 23 of 49

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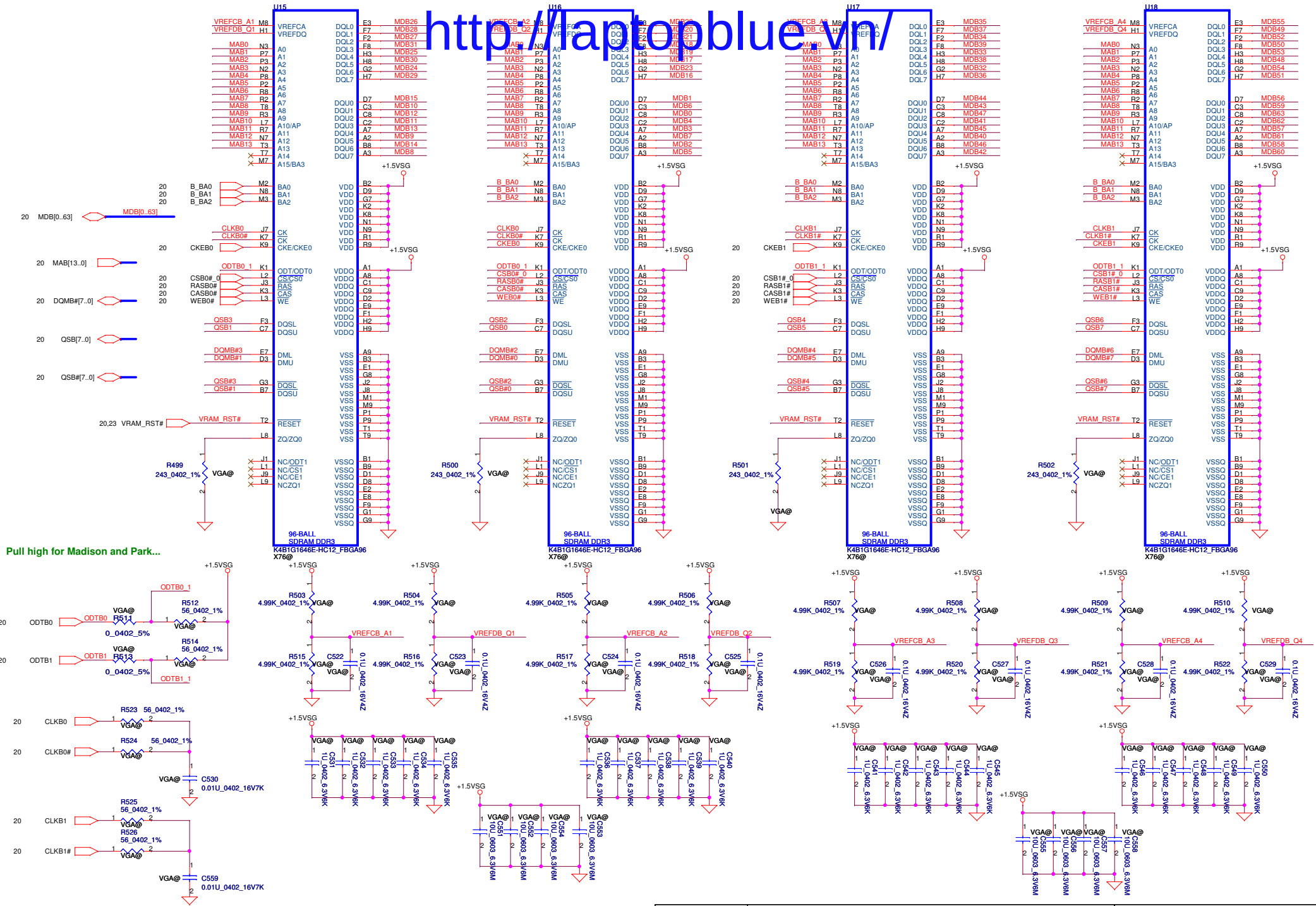

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

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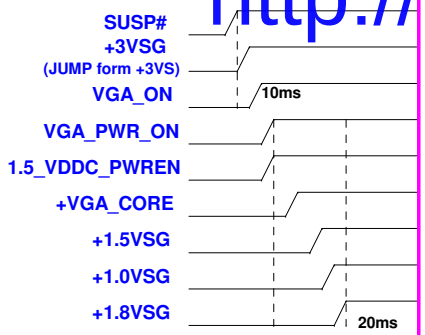
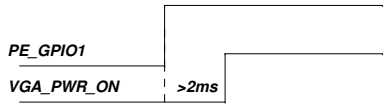
Power Sequence of Whistler and Seymou

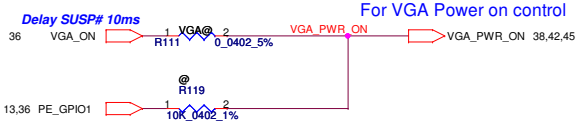


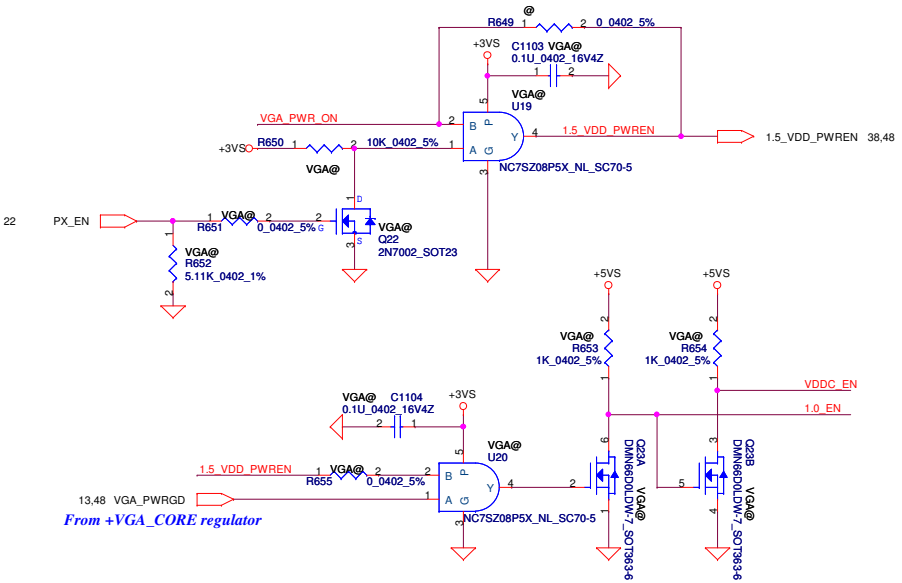
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON



VGA Modess with BACO Status Mapping Table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN





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Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: VGA power sequence and BACO

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+3VS — 40mil — R1160 0_0603_5% — 40mil — +3VS_PS

+1.2VS — 60mil — R1172 0_0603_5% — 60mil — +1.2VS_PS

Close to Pin3

DP_V33

10U_0603_6.3V6M C20 — 0.1U_0402_16V4Z C25 — 0.1U_0402_16V4Z C4

Close to P18

SWR_VDD

22U_0805_6.3V6M C27 — 0.1U_0402_16V4Z C28 — 0.1U_0402_16V4Z C29

Close to Pin13

Close to L3

+1.2VS_PS

22U_0805_6.3V6M C1489 — 0.1U_0402_16V4Z C2 — 0.1U_0402_16V4Z C30 — 0.1U_0402_16V4Z C31

Close to Pin27

+3VS_PS

+1.2VS_PS

L76 FBMA-L11-201209-221LMA30T_0805 DP_V33 40mil

L78 FBMA-L11-201209-221LMA30T_0805 SWR_VDD 60mil

@ L77 4.7UH_PG0031B-4R7MS_1.1A_20% SWR_LX 60mil

U46

DP_V33
SWR_VDD
PVCC
SWR_LX
SWR_VCCK
VCCK
DP_V12

Power

LVDS

TXEC+ TXEC- — APU_TXOUT_CLK+ APU_TXOUT_CLK- — APU_TXOUT_CLK+ 27 APU_TXOUT_CLK- 27

TXE2+ TXE2- — APU_TXOUT2+ APU_TXOUT2- — APU_TXOUT2+ 27 APU_TXOUT2- 27

TXE1+ TXE1- — APU_TXOUT1+ APU_TXOUT1- — APU_TXOUT1+ 27 APU_TXOUT1- 27

TXE0+ TXE0- — APU_TXOUT0+ APU_TXOUT0- — APU_TXOUT0+ 27 APU_TXOUT0- 27

RTD2132S

DP_IN

AUX_P
AUX_N
LANE0P
LANE0N

8 DP0_AUXP_C — DP0_AUXP_C
8 DP0_AUXN_C — DP0_AUXN_C
8 DP0_TXP0_C — DP0_TXP0_C
8 DP0_TXN0_C — DP0_TXN0_C

GPIO

GPIO(PWM OUT) — R1161 0_0402_5% — TL_INVT_PWM 27
GPIO(Panel_VCC) — TL_ENVDD 27
GPIO(PWM IN) — R1162 0_0402_5% — APU_INVT_PWM 10,27
GPIO(BL_EN) — TL_BKOFF# 27,36

Reserved for EC programming ROM
Need EC confirm

CSCL — CIICSCL1
CSDA — CIICSDA1

LVDS EDID — MIICSCL1 / MIICDA1 — APU_LVDS_CLK — APU_LVDS_CLK 27
APU_LVDS_DAT — APU_LVDS_DAT 27

Other

10 LVDS_HPD — HPD

R1168 100K_0402_5%

R30 12K_0402_1% Change to 12Kohm 1% (DG ref.) 20101114

DP_REXT
DP_GND

ROM — MIICSCL0 / MIICSDA0 — MIIC_SCL — R17 0_0402_5% — MIIC_SCL_R
MIIC_SDA — R3 0_0402_5% — MIIC_SDA_R

GND

RTD2132S-GR_QFN32_5X5

EEROM

+3VS_PS

U2

MIIC_SCL_R
MIIC_SDA_R

VCC WP SCL SDA — A0 A1 A2 GND

CAT24C64WI-GT3_SO8

+3VS_PS

APU_LVDS_DAT — R1163 4.7K_0402_5%
APU_LVDS_CLK — R1164 4.7K_0402_5%
MIIC_SCL — R1165 4.7K_0402_5%
MIIC_SDA — R1166 4.7K_0402_5%
CSCL — R1167 4.7K_0402_5%
CSDA — R1170 4.7K_0402_5%

+3VS_PS

@ Q90A

CSDA — DMN66D0LDW-7_SOT363-6 — EC_SMB_DA2 — EC_SMB_DA2 6,19,36

R1169 0_0402_5%

@ Q90B

CSCL — DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 6,19,36

R1171 0_0402_5%

For upgrade Firmwave

MIIC_SCL — @ R1175 4.7K_0402_5%

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Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Title: LVDS Translator - RTD2132S

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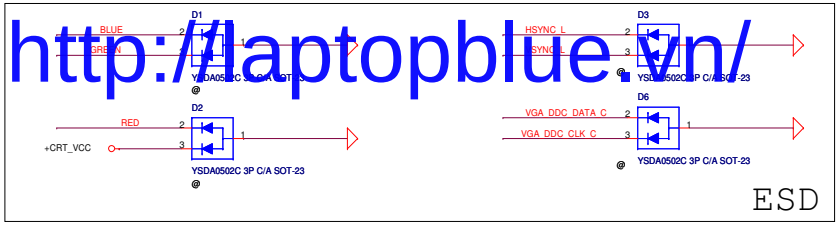
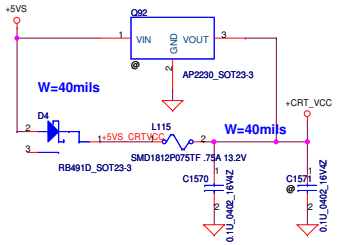
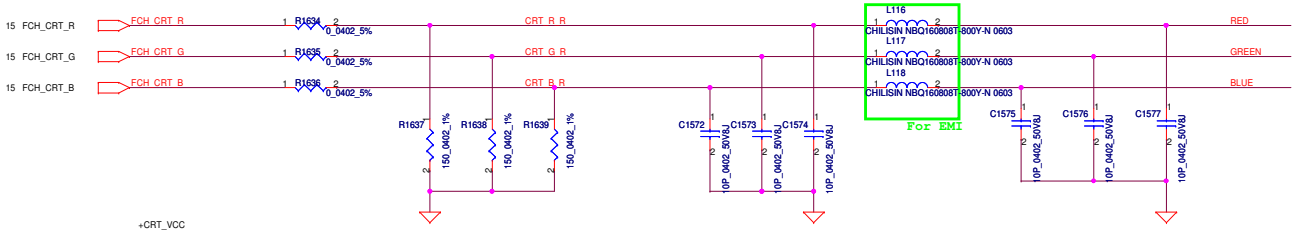
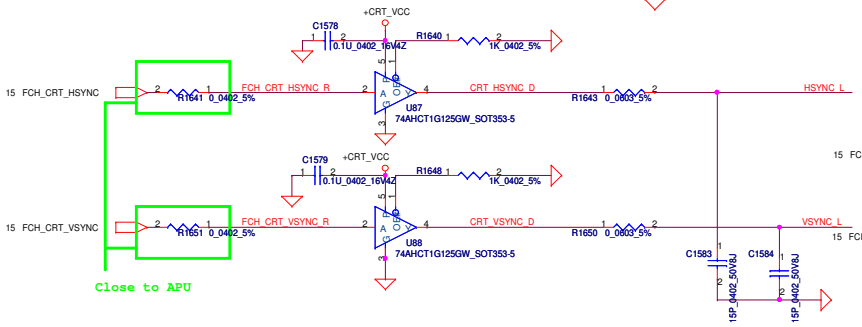
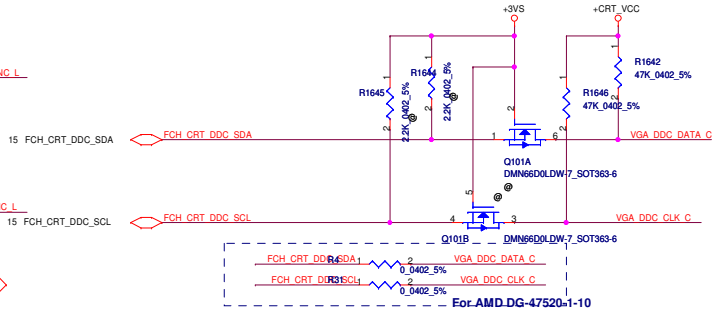
CRT

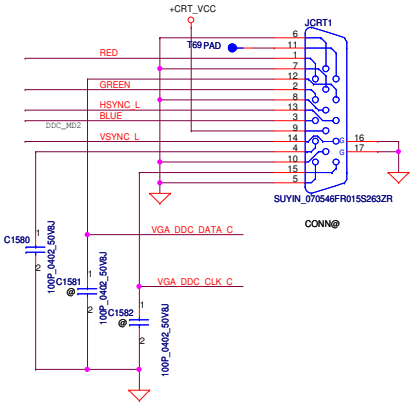




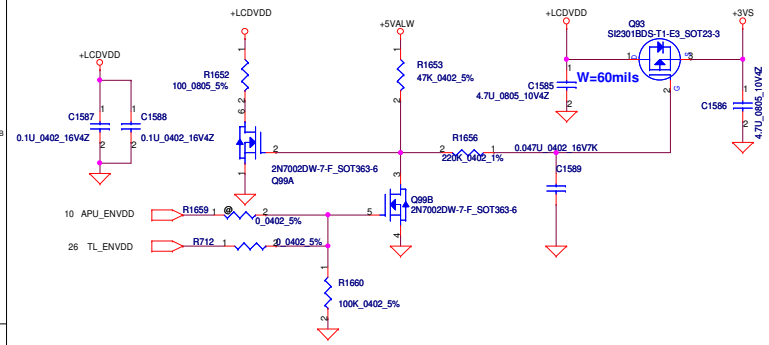


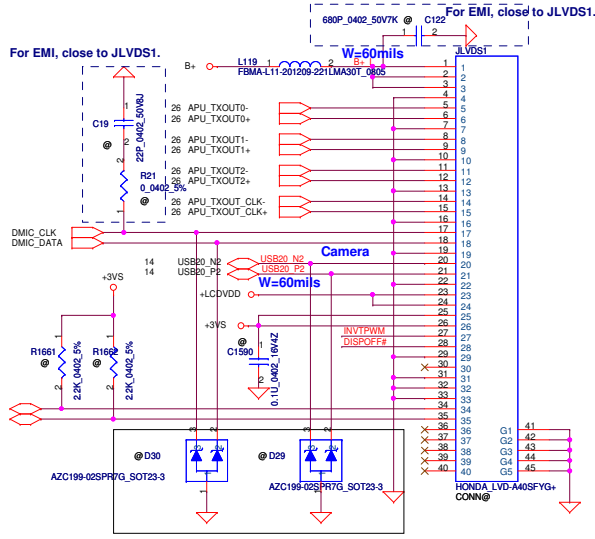




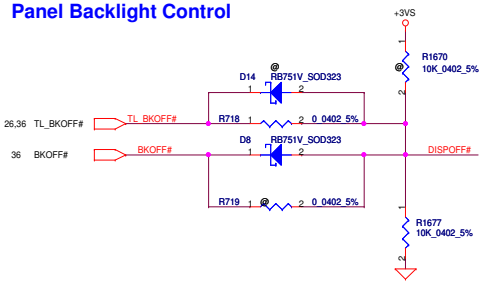


Panel LCDVDD Control

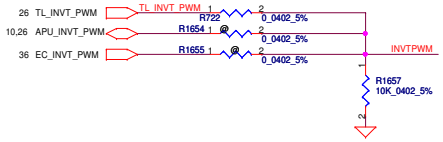




Panel Backlight Control



Panel PWM Control



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Size: C	Document Number: QBL60 LA-7552P
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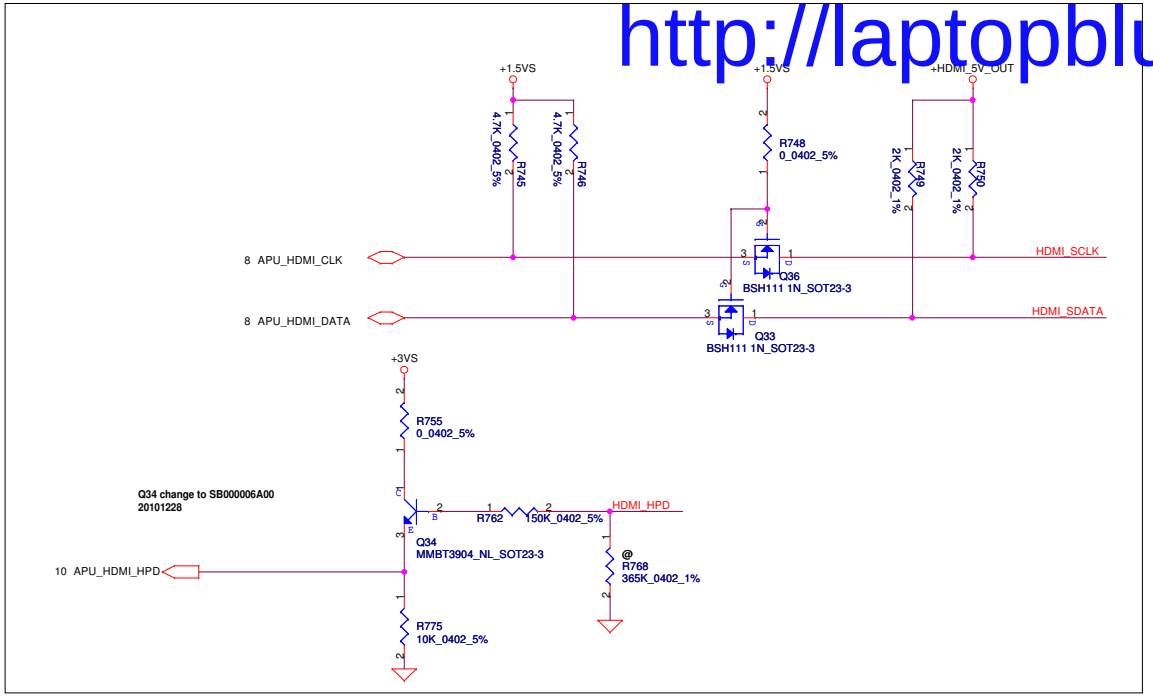
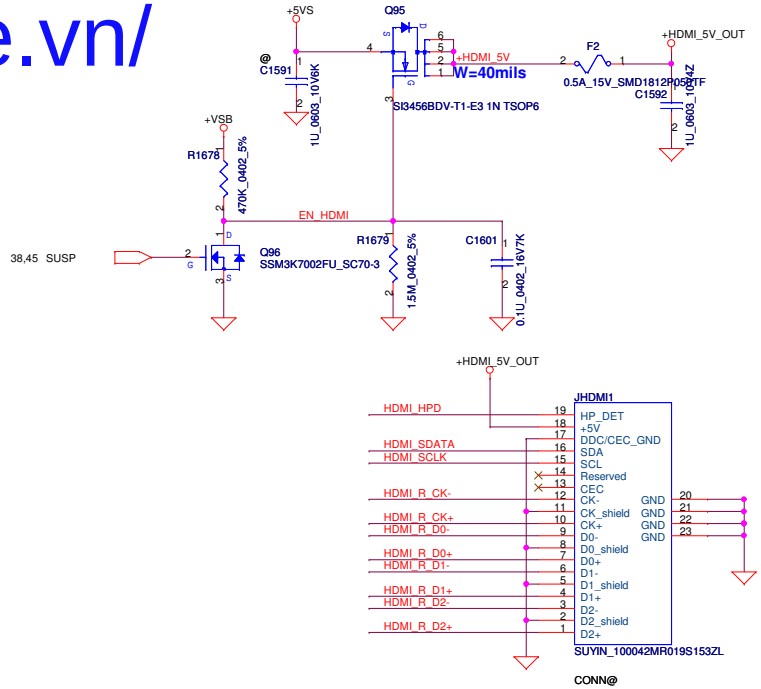
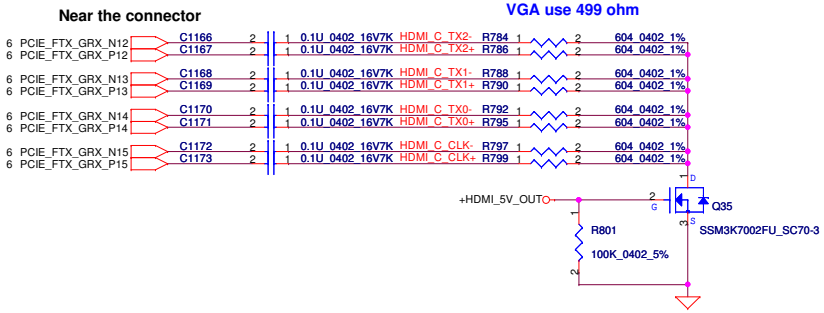


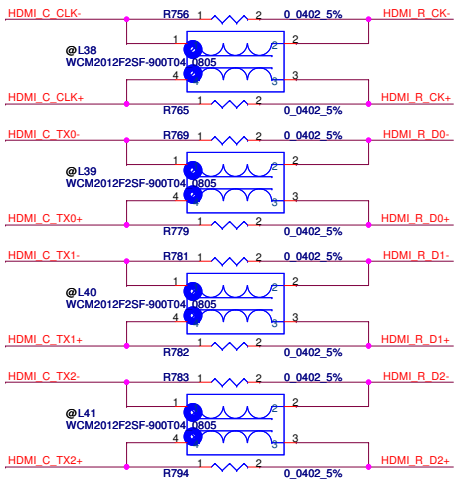


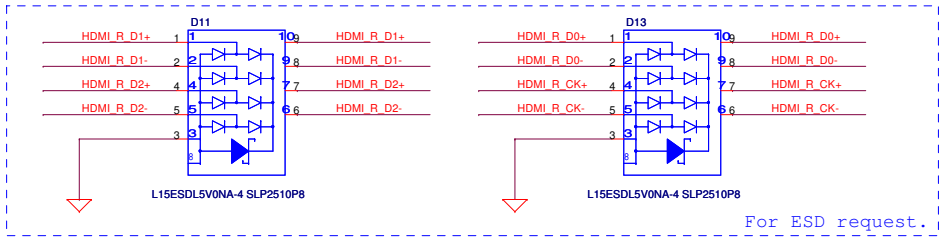
From APU

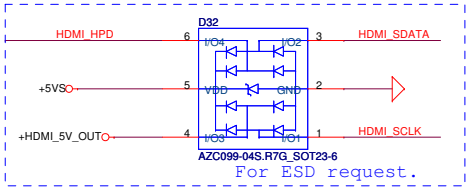
Near the connector

UMA use 604 ohm
VGA use 499 ohm









Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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http://laptopblue.vn/

W=60mils

W=60mils

1.1A

These caps close to Pin 12,27,39,42,47,48

These caps close to Pin 3,6,9,13,29,41,45

W=40mils

W=20mils

W=60mils

These components close to Pin 36
(Should be place within 200 mils)

For ESD request.

ESD

SOD323 package

ESD

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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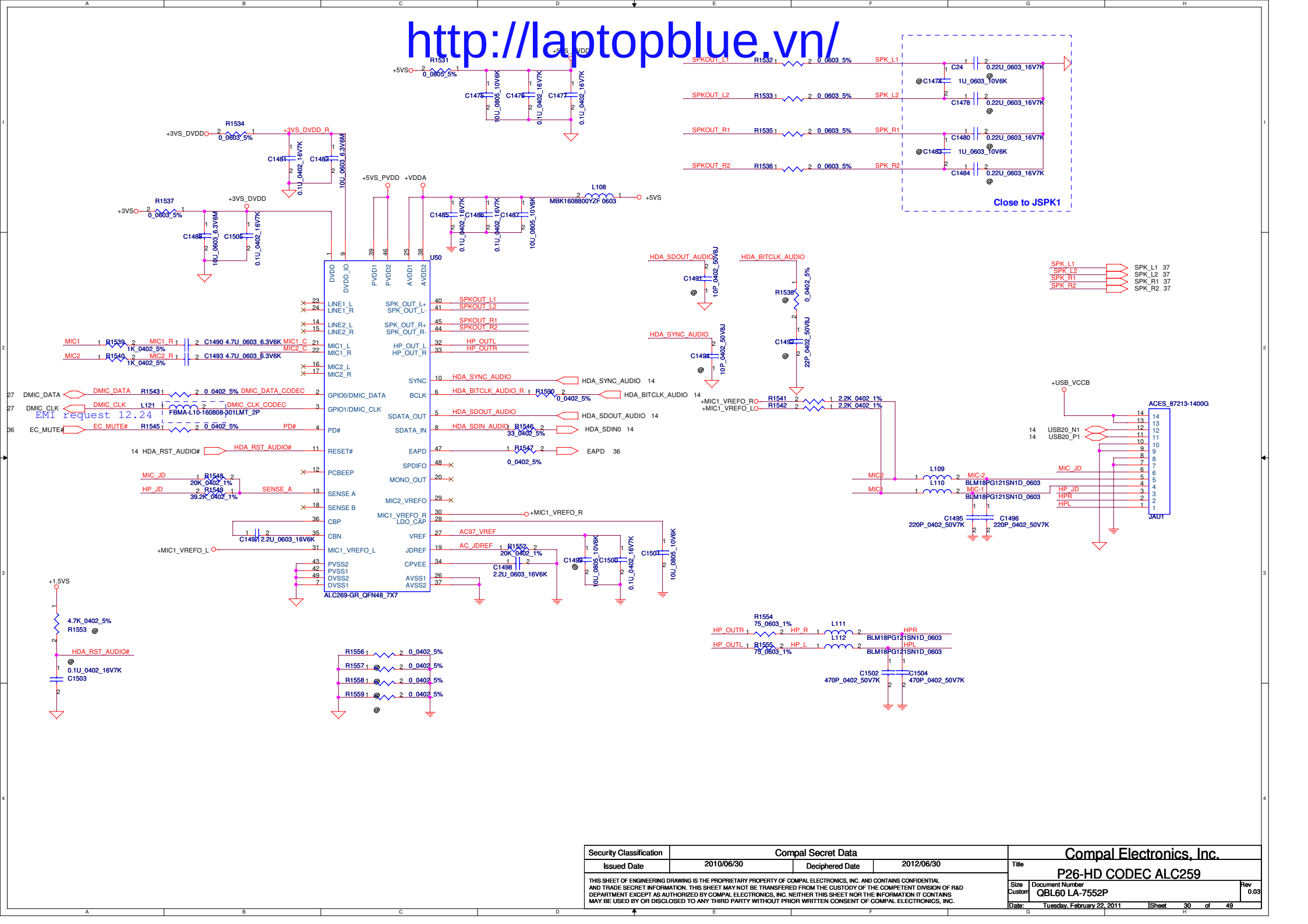
Compal Electronics, Inc.

Title: P25-LAN RTL8111E

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.02

Date: Tuesday, February 22, 2011 | Sheet 29 of 49

http://laptopblue.vn/



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 30 of 49

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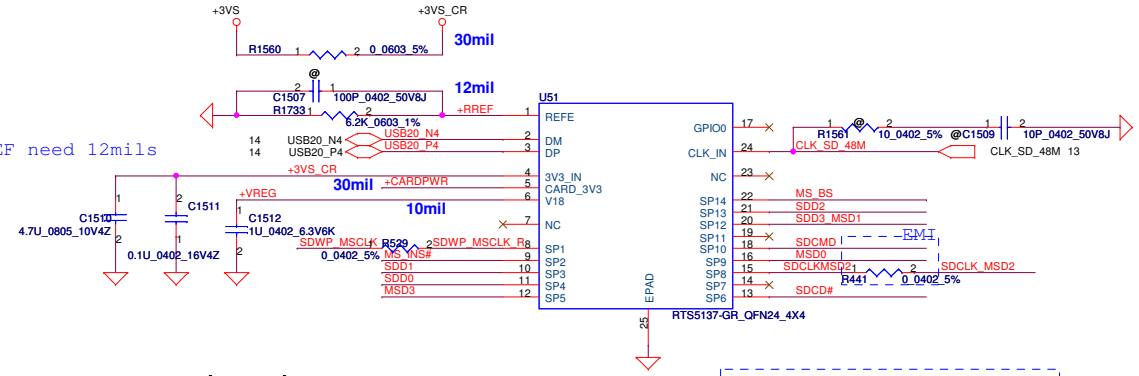
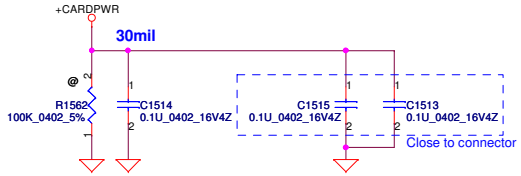
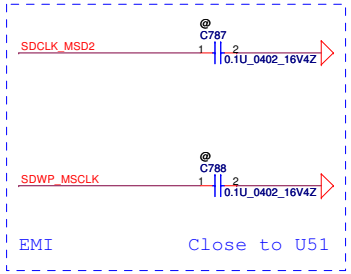
Card Reader RTS5137
(only SD/MMC/MS function)

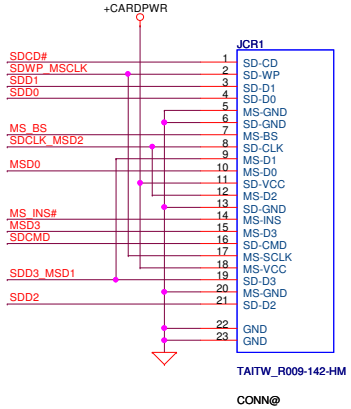
+RREF & +VREF need 12mils



Card Reader Connector







Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P27-RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	QBL60 LA-7552P	0.03

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Mini-Express Card for WLAN/WiMAX(Half)

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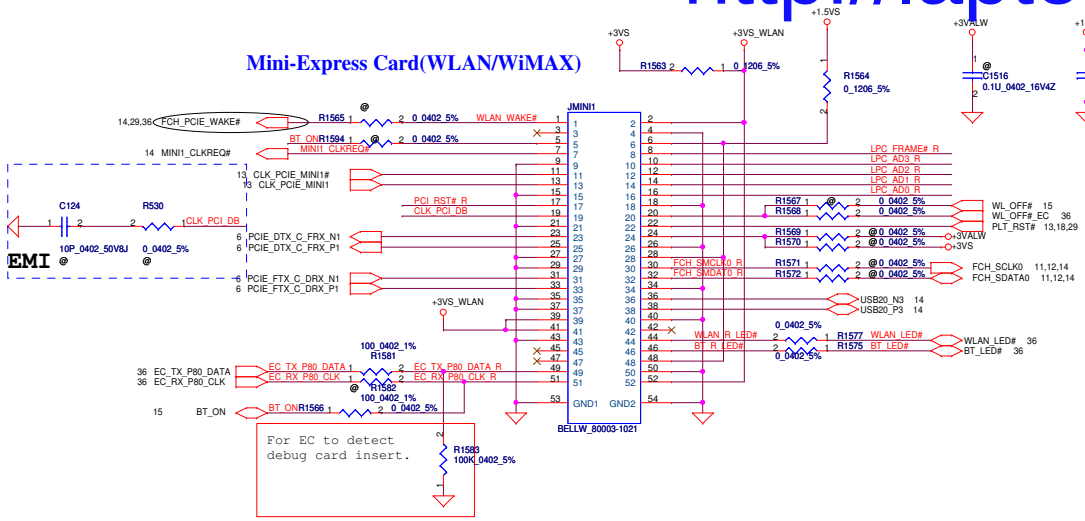
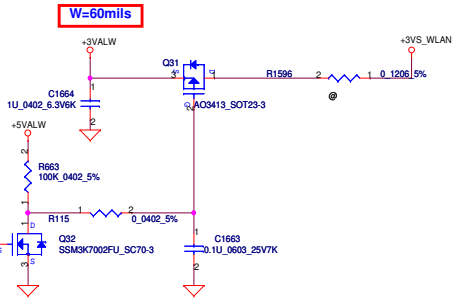
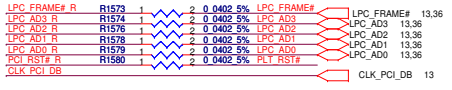
Mini-Express Card(WLAN/WiMAX)



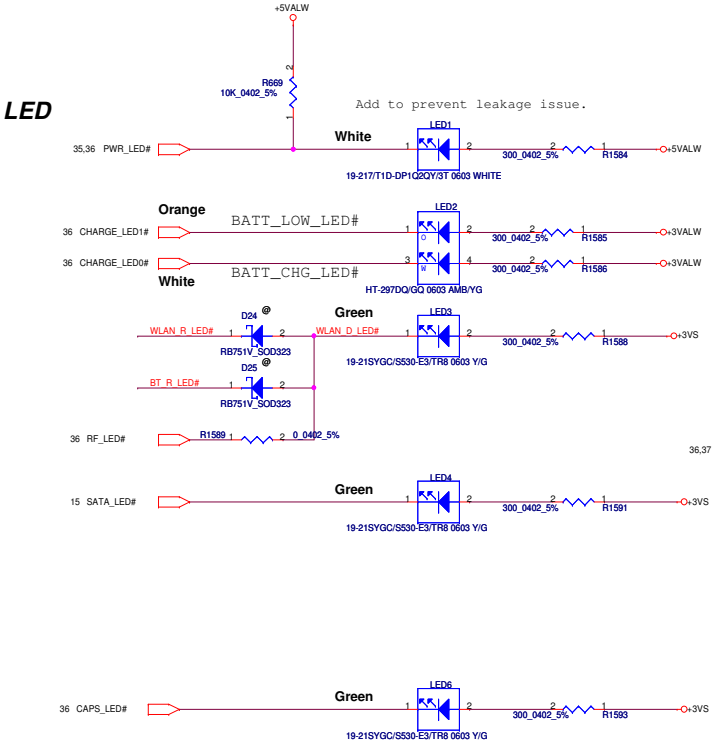
W=60mils

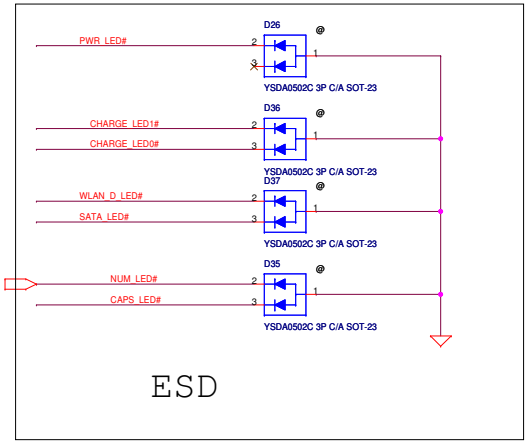


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



LED





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.			
Title	P28-Mini PCIE/LED		
Size	Document Number		Rev
	QBL60 LA-7552P		0.03
Date: Tuesday, February 22, 2011	Sheet 32 of 49		

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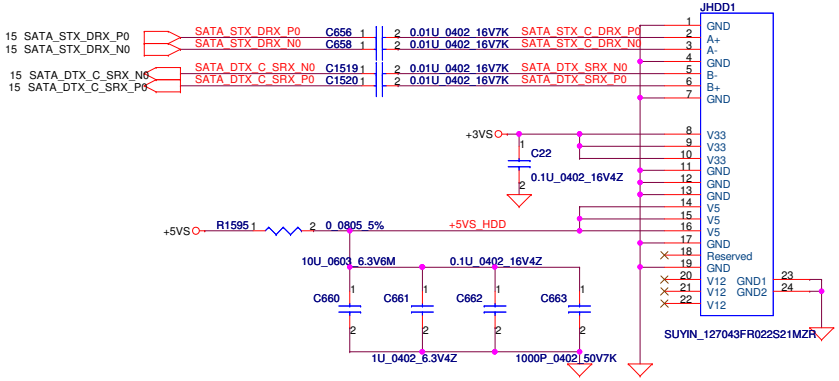
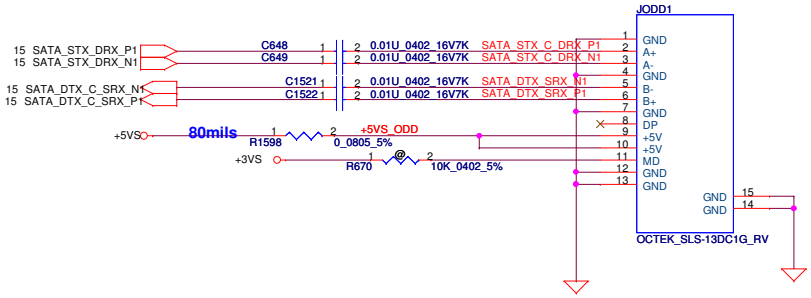
SATA HDD Conn.



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P29-HDD & ODD CONN

Size	Document Number	Rev
B	QBL60 LA-7552P	0.03

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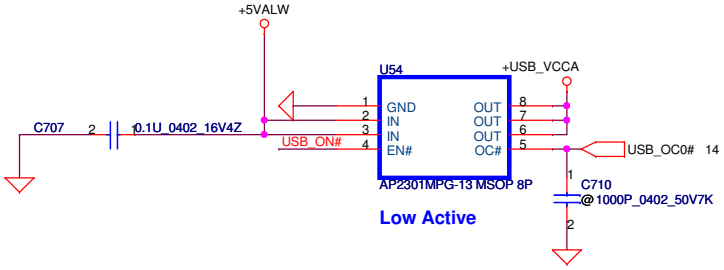

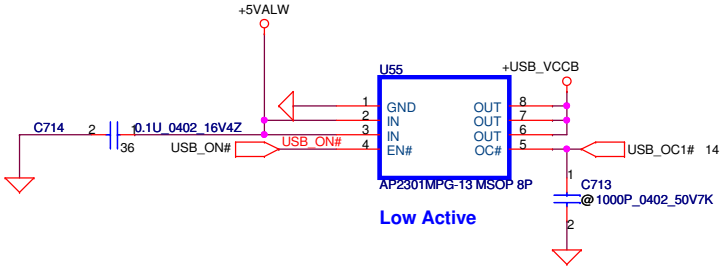

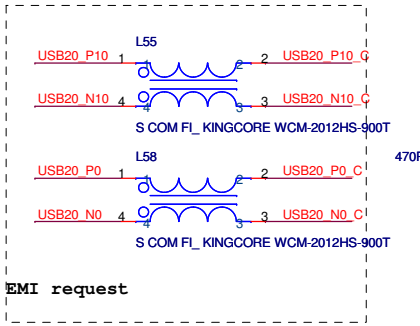

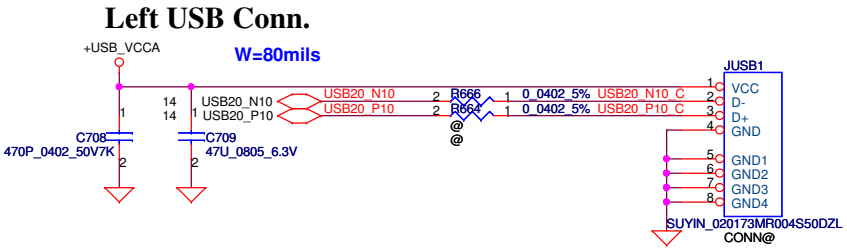

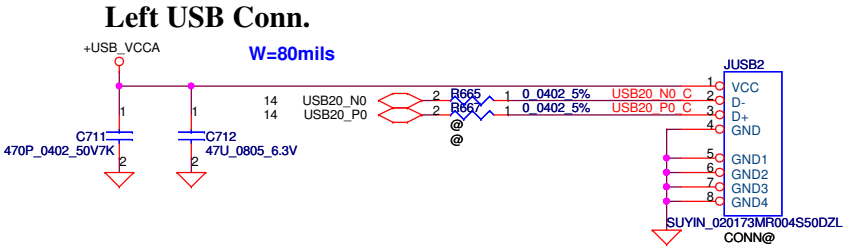

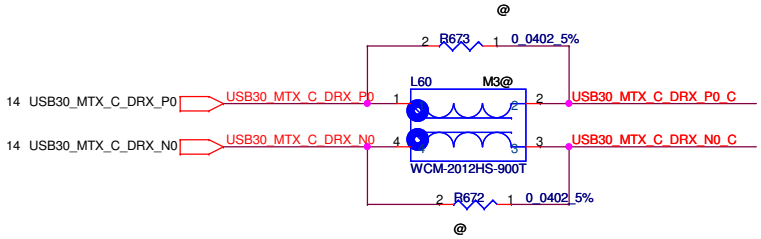

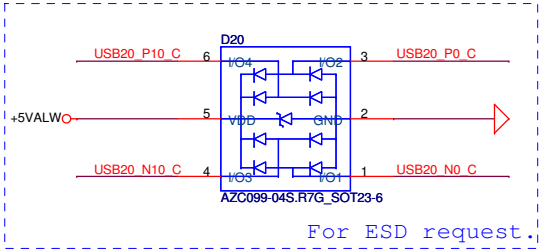

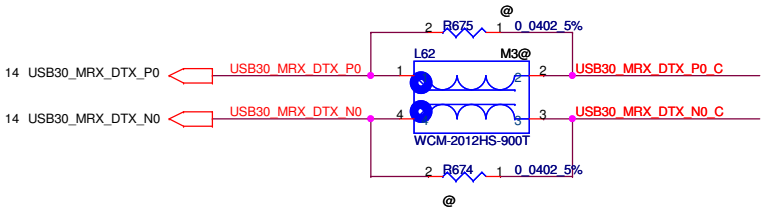

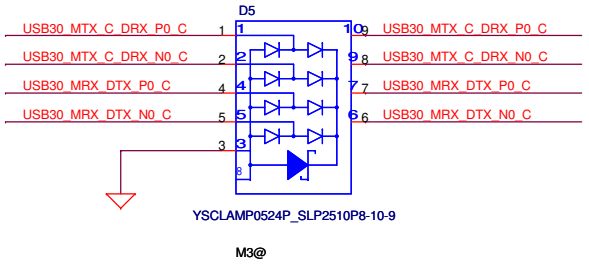

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P32-USB/BT/USBsub

Size: Custom | Document Number: QBL60 LA-7552P | Rev: 0.03

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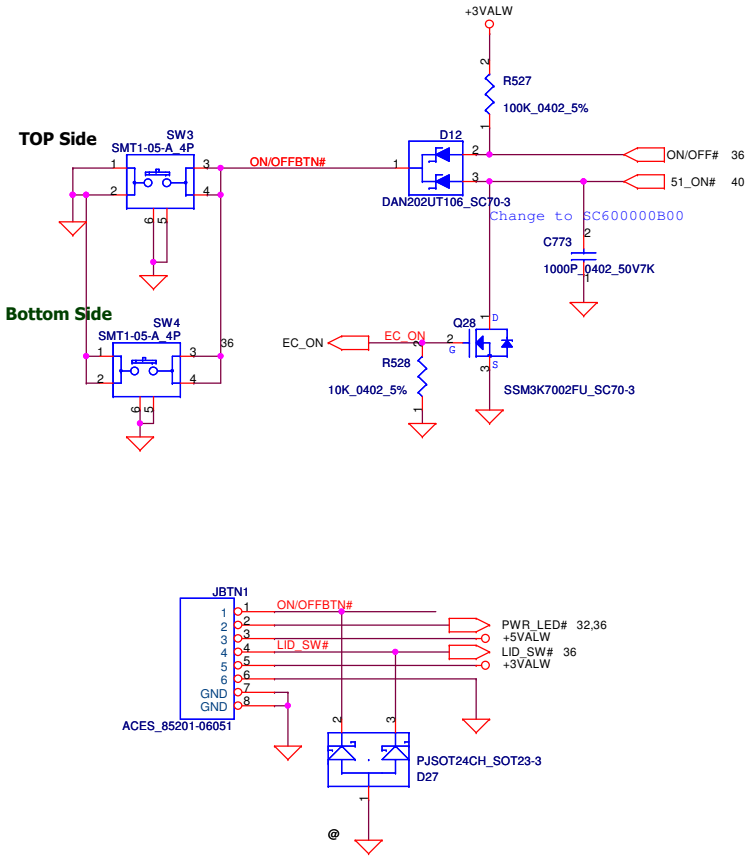
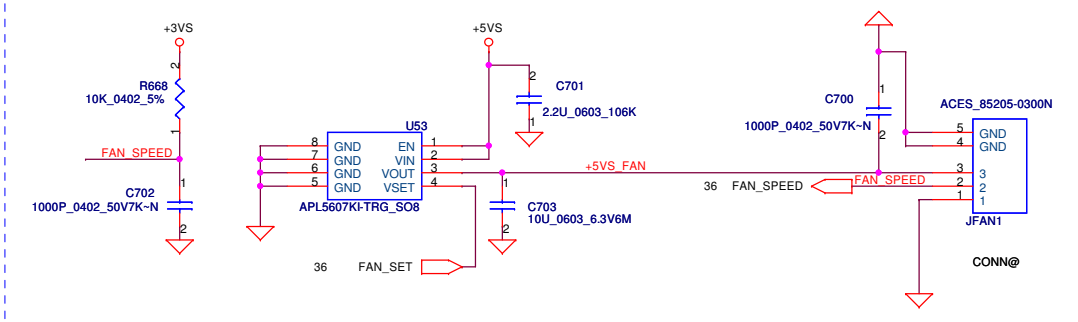
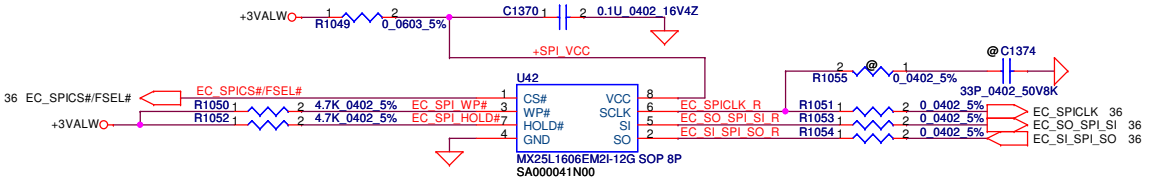
ON/OFF switch ***Power Button***



Fan Control Circuit



EC BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL60 LA-7552P | Rev: 0.03

Date: Tuesday, February 22, 2011 | Sheet 35 of 49

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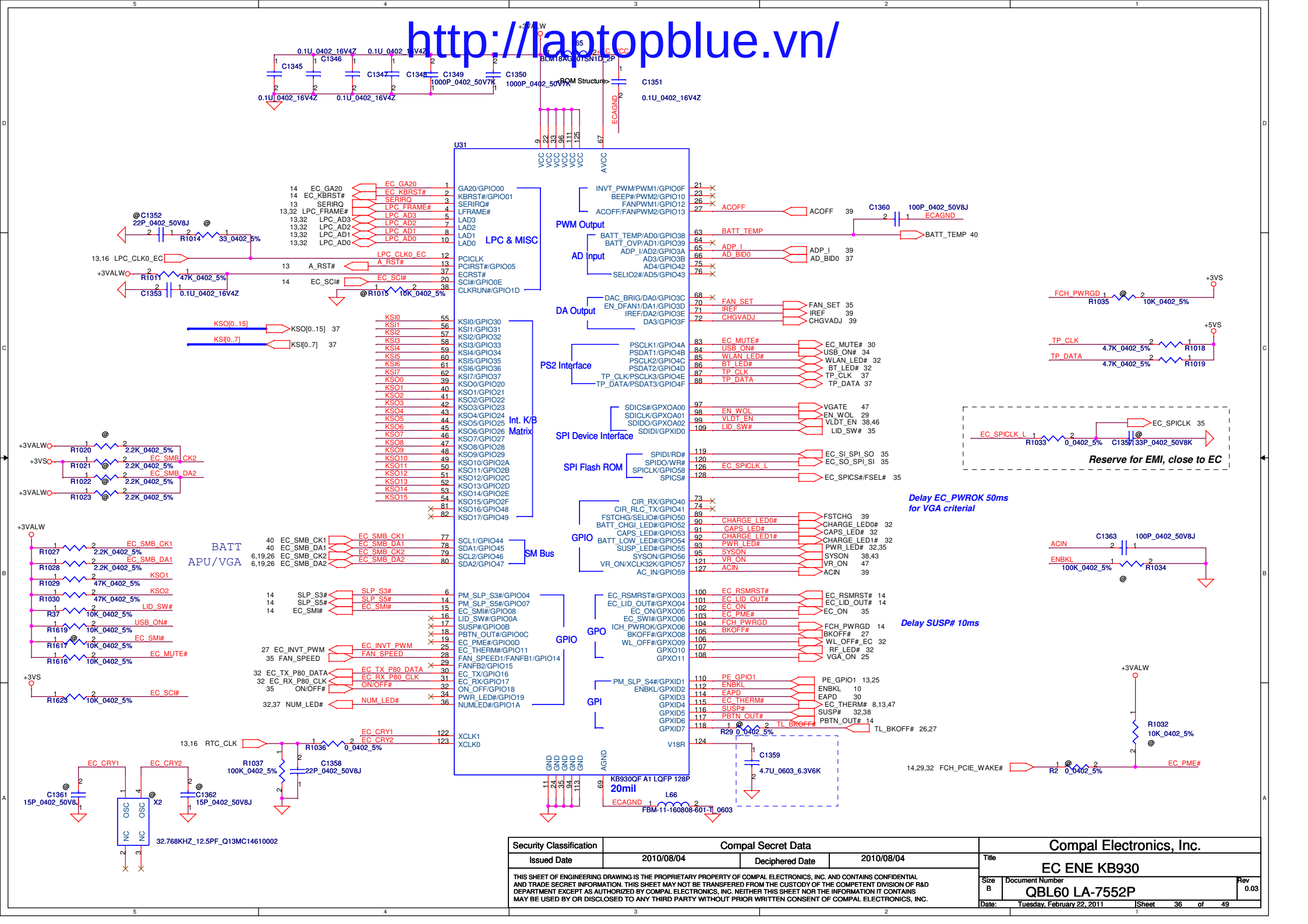

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: EC ENE KB930

Size	Document Number	Rev
B	QBL60 LA-7552P	0.03

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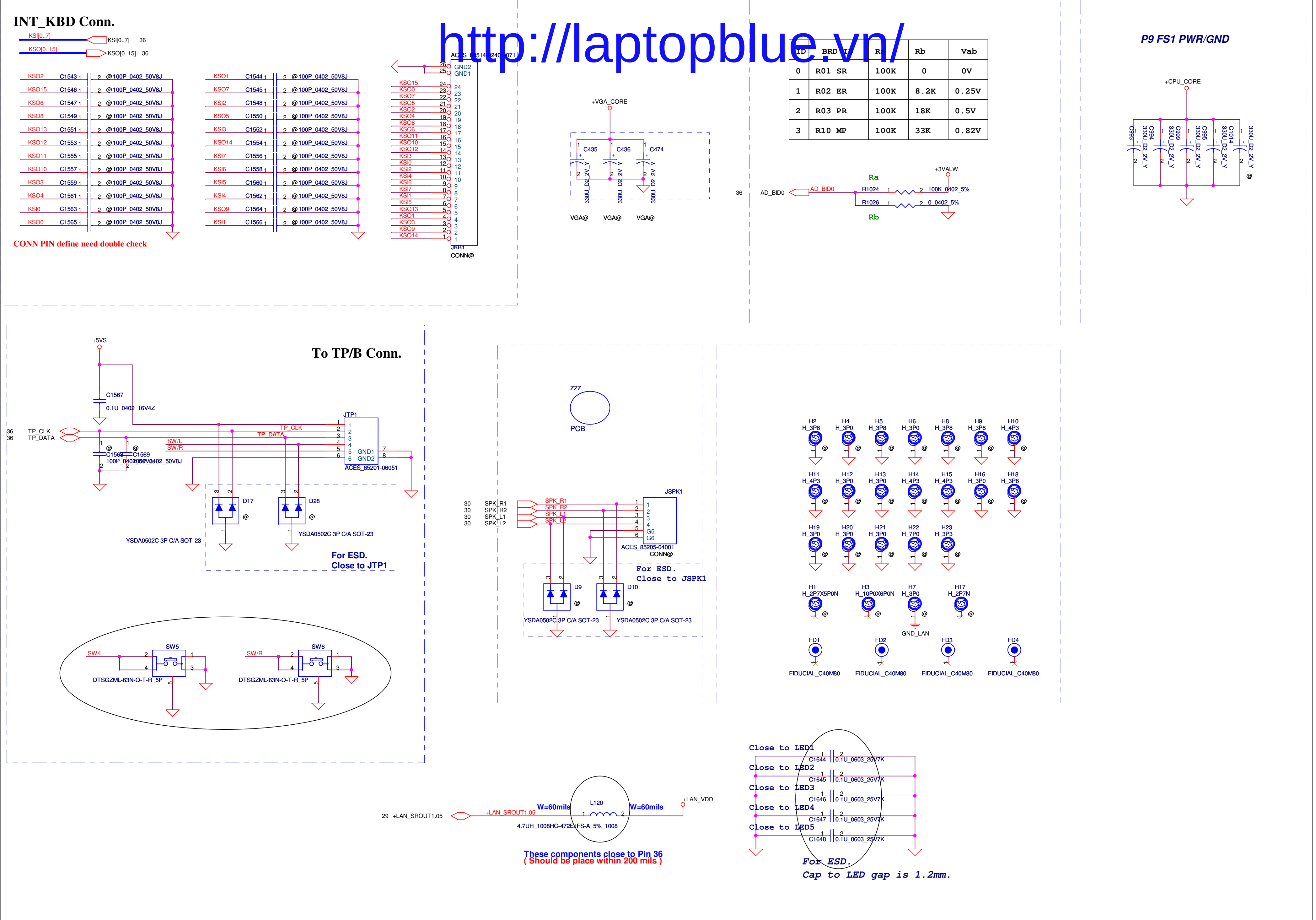

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V

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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/11/25	Deciphered Date	2011/12/31	Title: P33-Other IO/USB (right)

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Size: Custom | Document Number: QBL50 LA-7551P | Rev: 0.02

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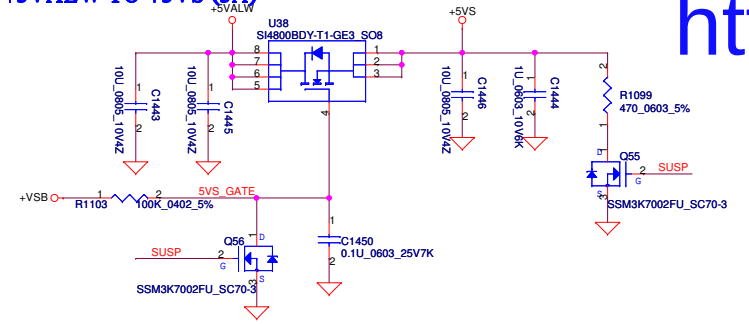
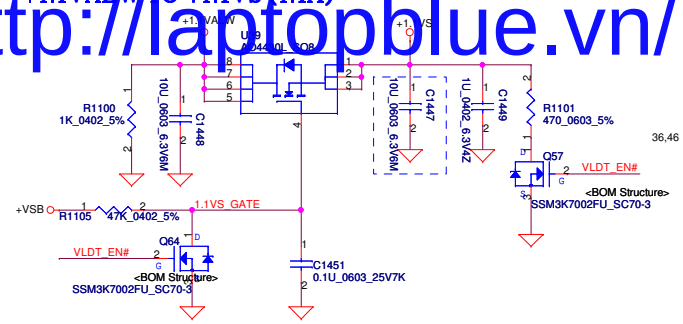
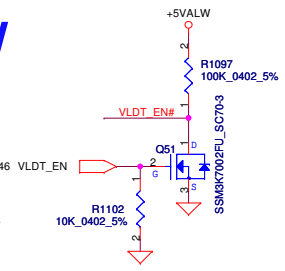
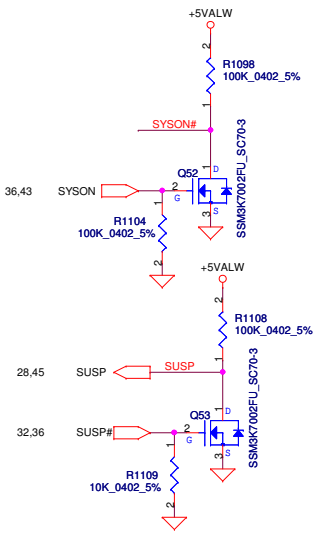
+5VALW TO +5VS (5A)



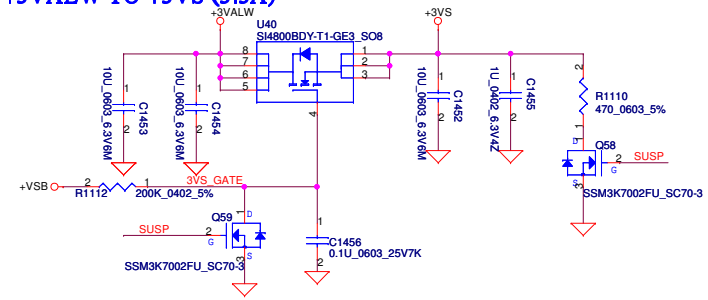
+1.1VALW TO +1.1VS (1.1A)



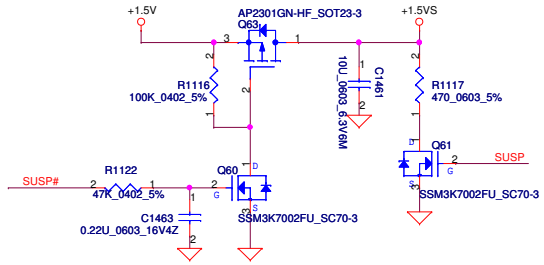




+3VALW TO +3VS (3.3A)

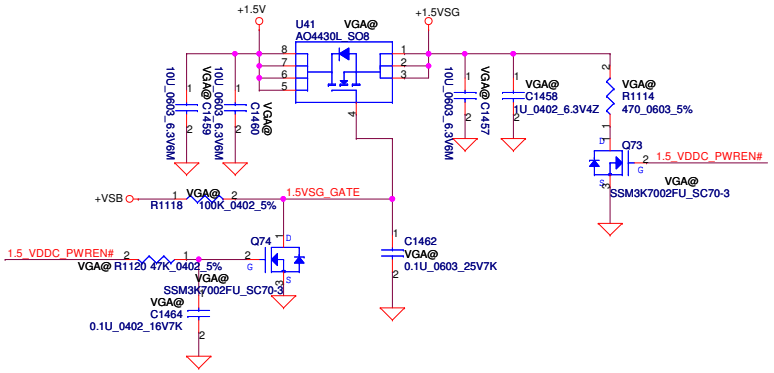


+1.5V TO +1.5VS (1.5A)

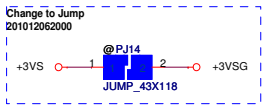


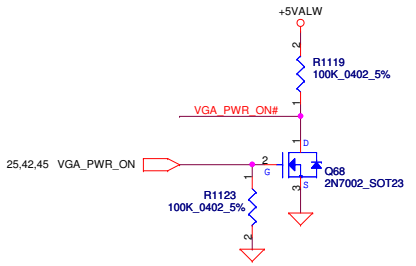
VGA Power

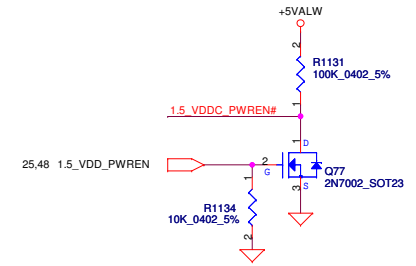
+1.5V to +1.5VSG (1.5A)

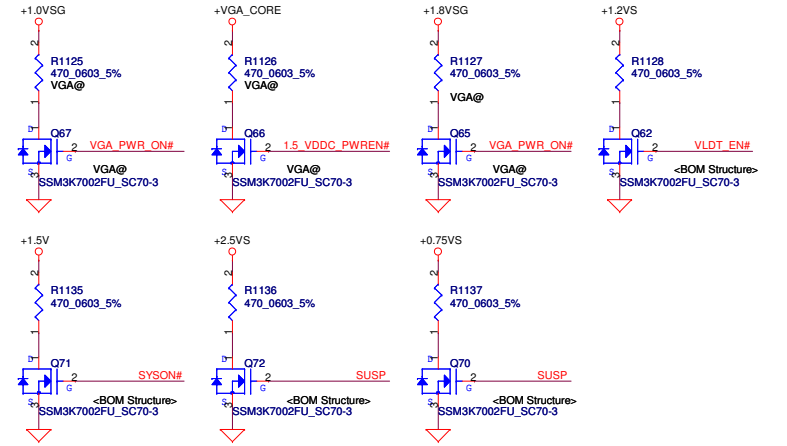


+3VS to +3VSG (3.3A)









Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	QBL60 LA-7552P	0.03

Date: Tuesday, February 22, 2011 | Sheet 38 of 49

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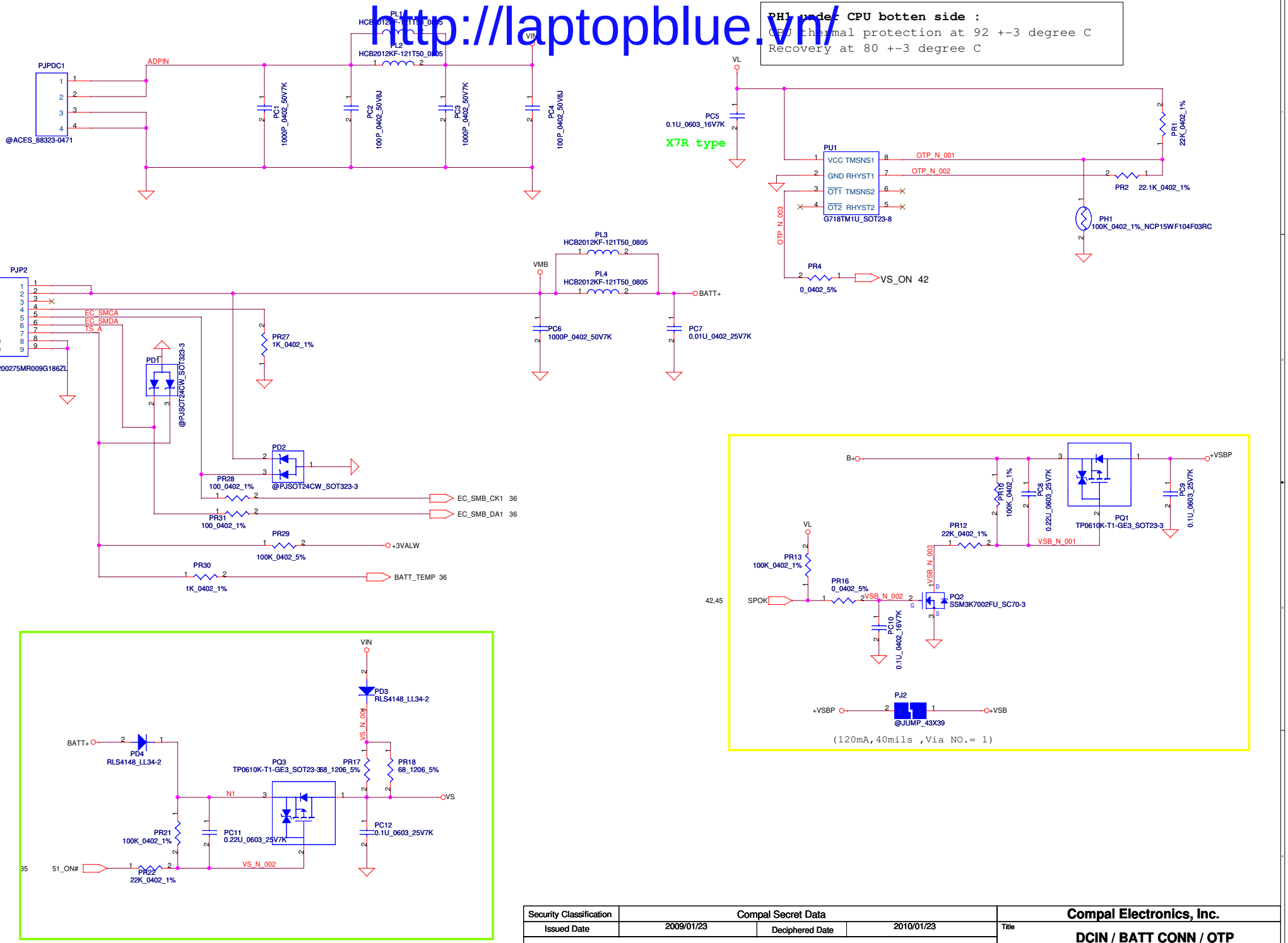
PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Tuesday, February 22, 2011 Sheet 40 of 44

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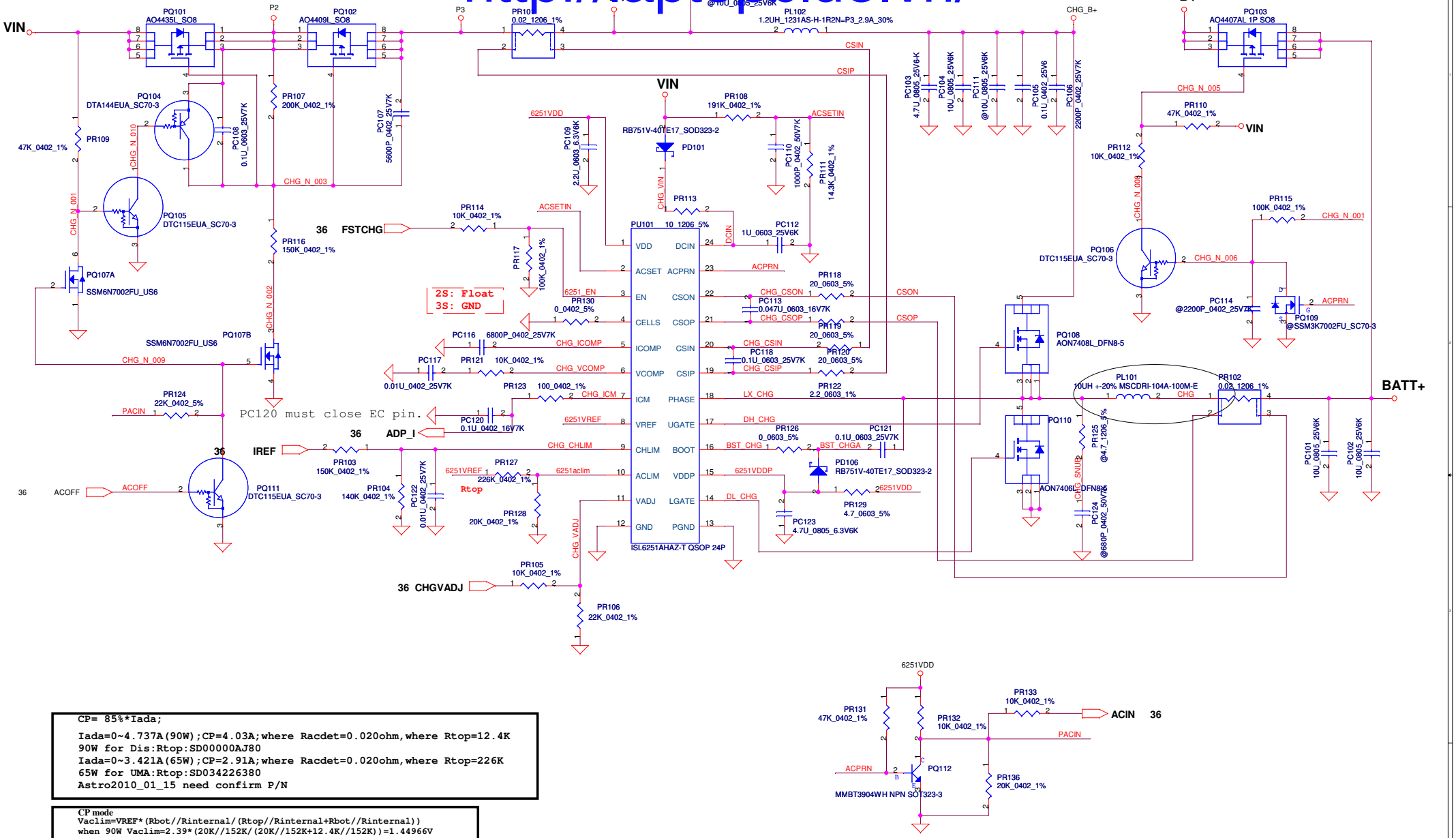


```
CP= 85%*Iada;
Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N
```

```
CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

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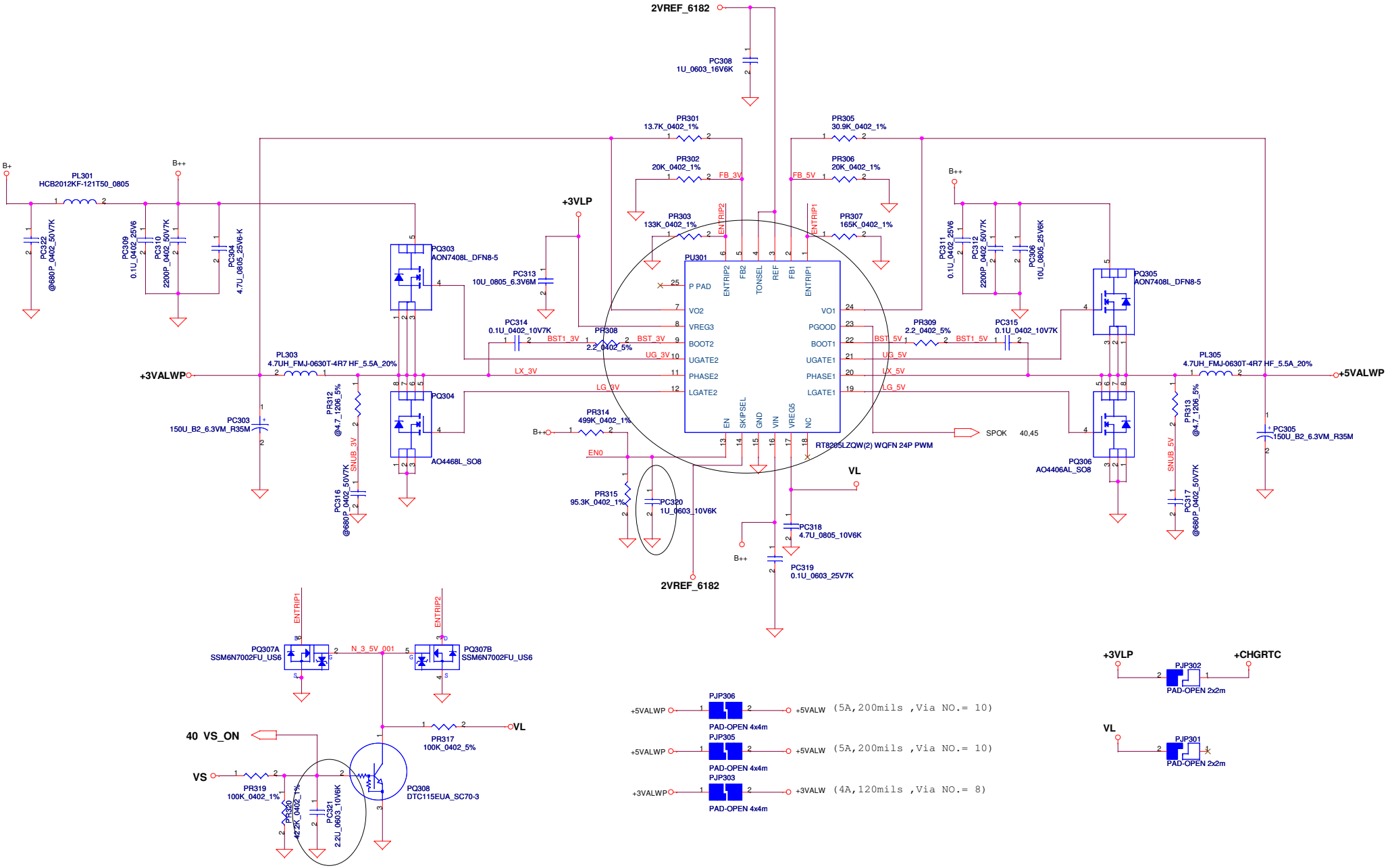

EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: LAXXXX		Rev: 0.1
Date: Tuesday, February 22, 2011	Sheet 42 of 44		

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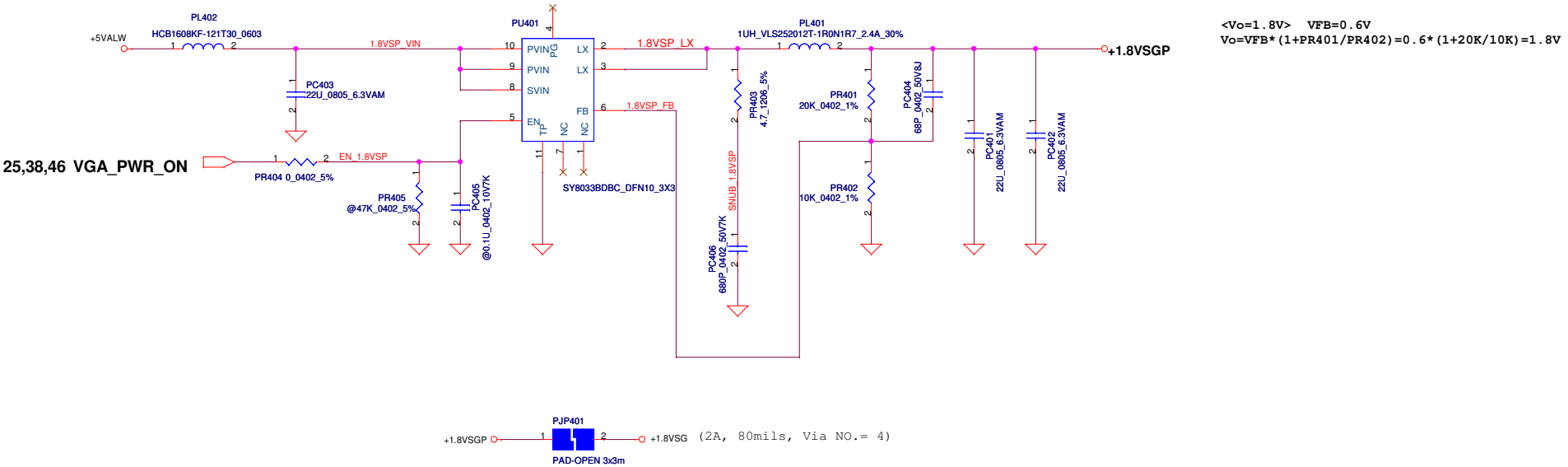

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **+1.8VSGP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Tuesday, February 22, 2011 | Sheet 43 of 44

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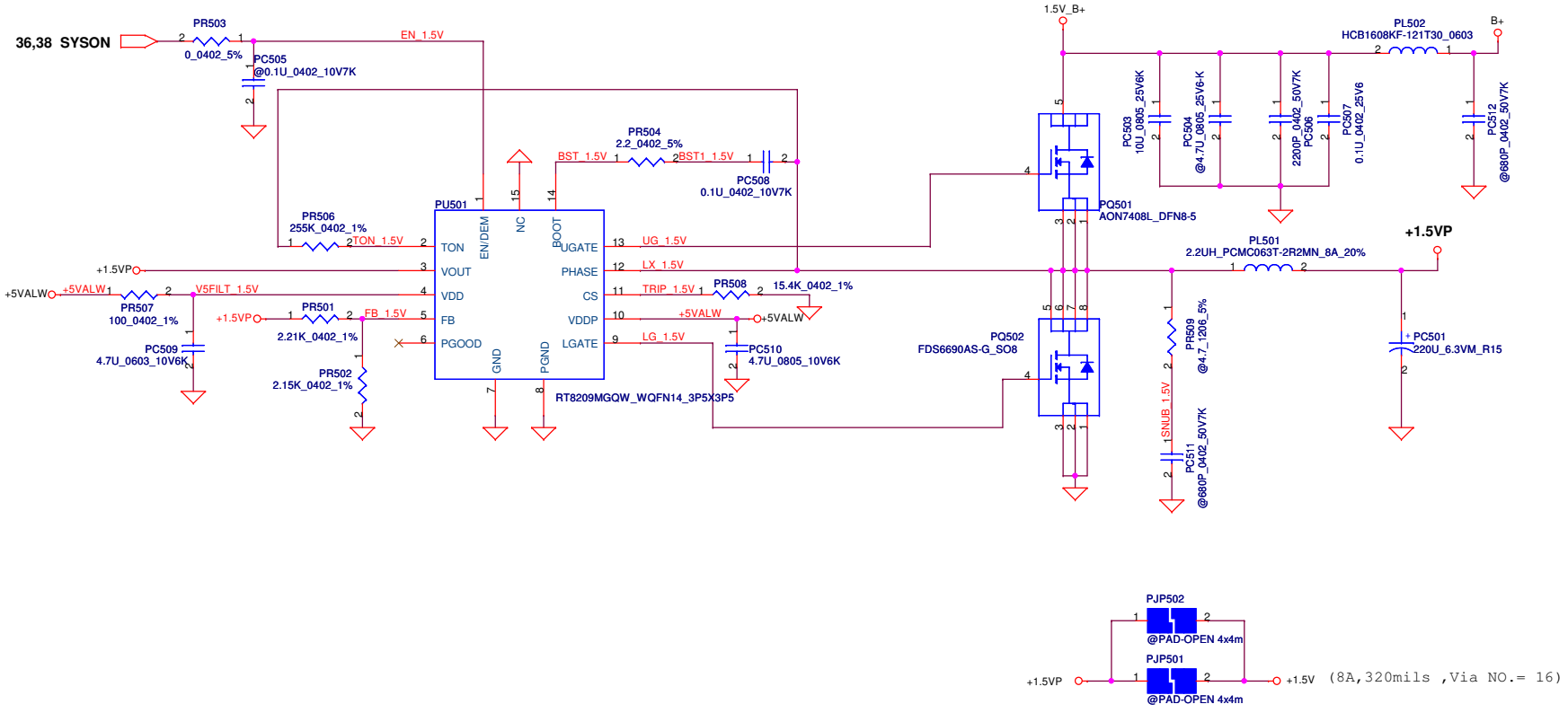

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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Compal Electronics, Inc.

Title: +1.5VP

Size | Document Number: LAXXXX | Rev: 0.1

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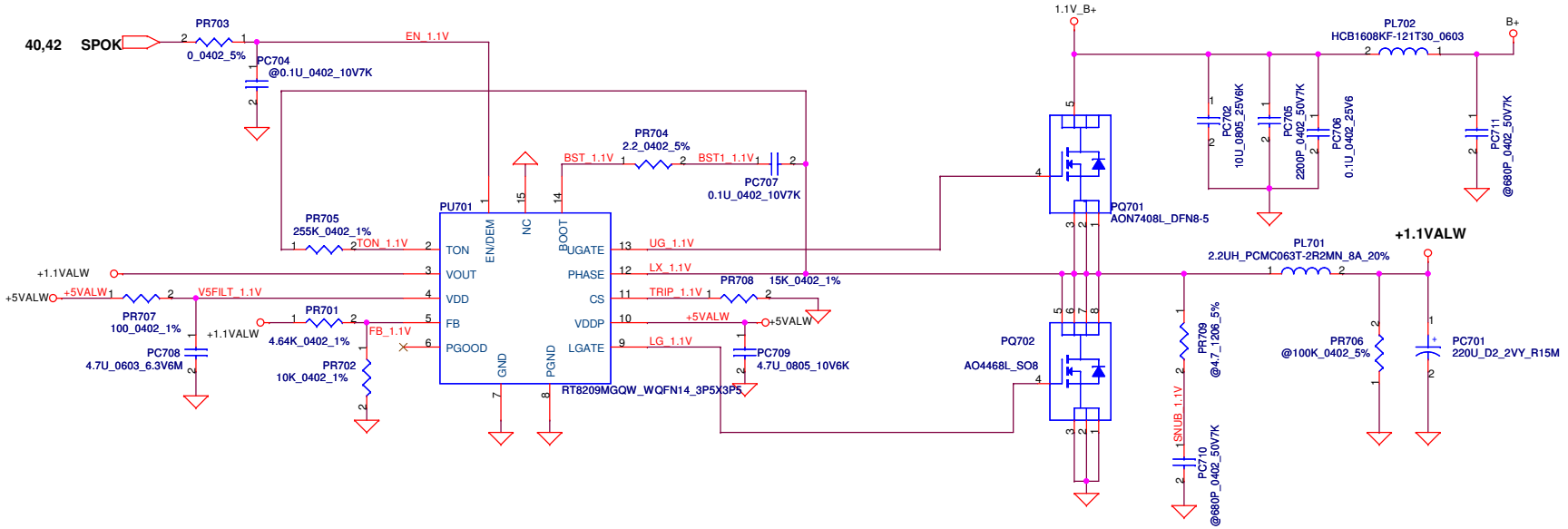

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR+1.1VALWP

Size: Custom | Document Number: LAXXXX | Rev: 0.1

Date: Tuesday, February 22, 2011 | Sheet 45 of 44

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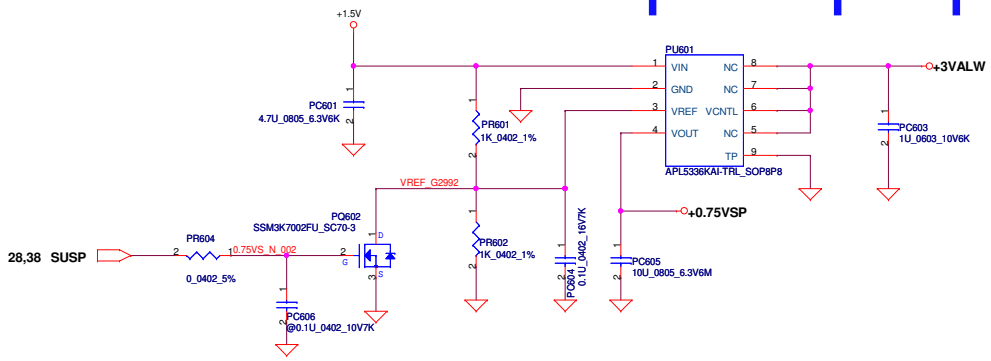

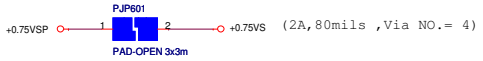

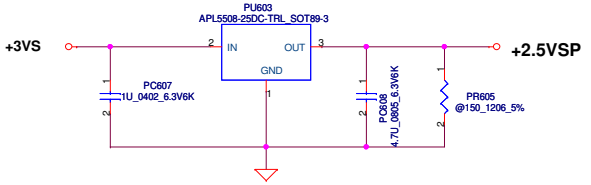

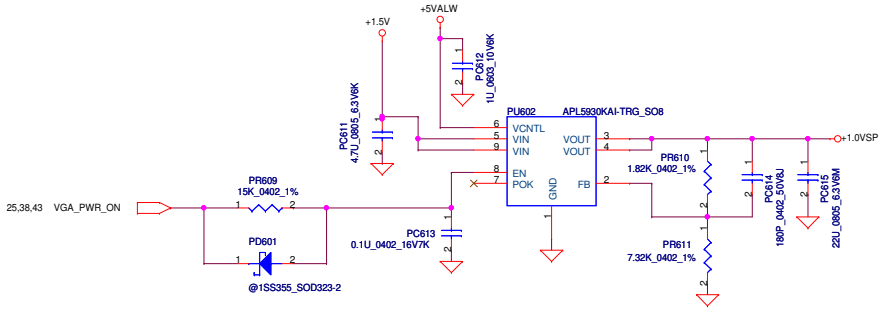

Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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Compal Electronics, Inc.			
Title	PWR 0.75VSP/1.0VSP/2.5VSP		
Size	Document Number		Rev
	LAXXXX		0.1
Date:	Tuesday, February 22, 2011	Sheet	46 of 44

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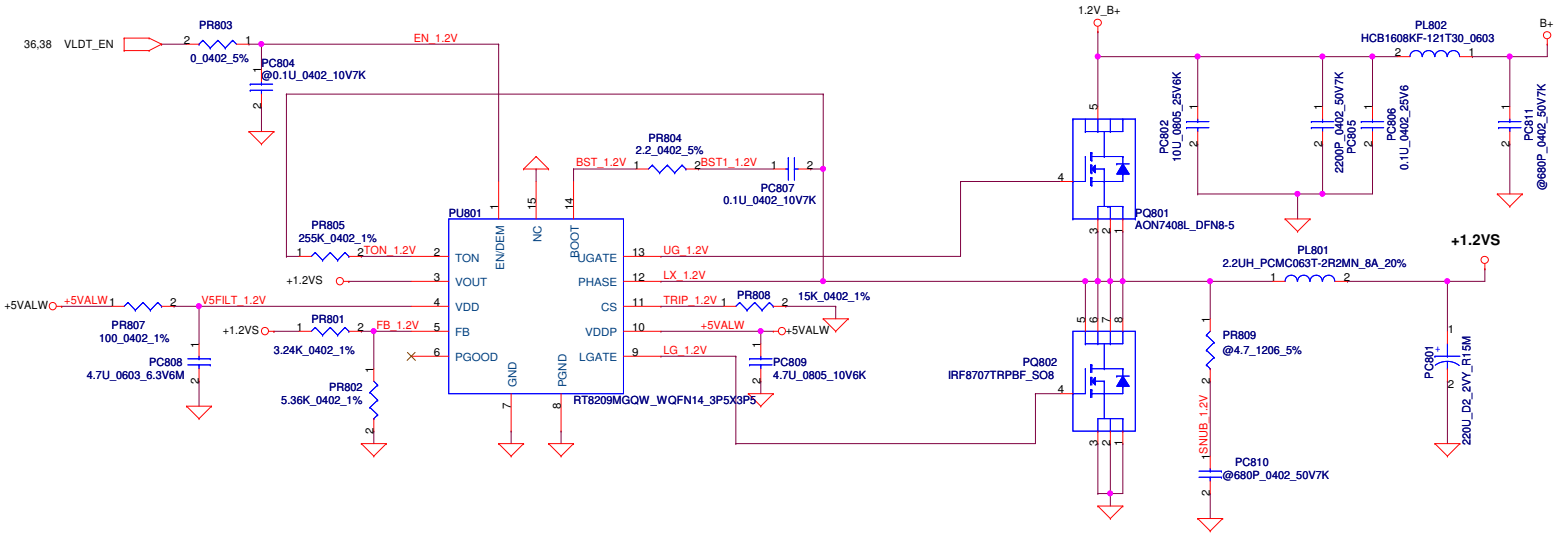

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **+1.2VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Tuesday, February 22, 2011 | Sheet 47 of 44

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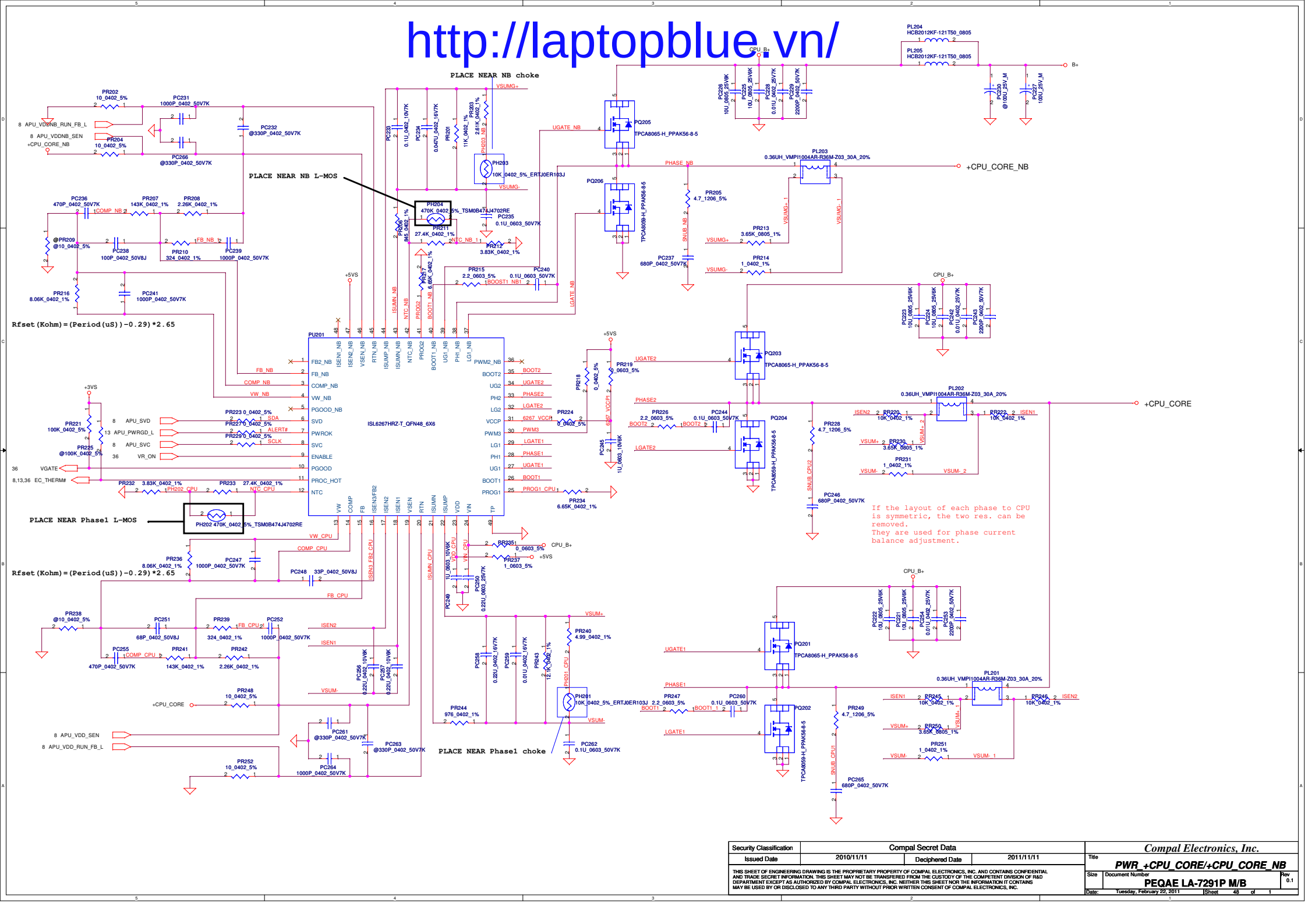

Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/11/11

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Compal Electronics, Inc.

Title: PWR_+CPU_CORE/+CPU_CORE_NB

Size	Document Number	Rev
	PEQAE LA-7291P M/B	0.1

Date: Tuesday, February 22, 2011 Sheet 48 of 1

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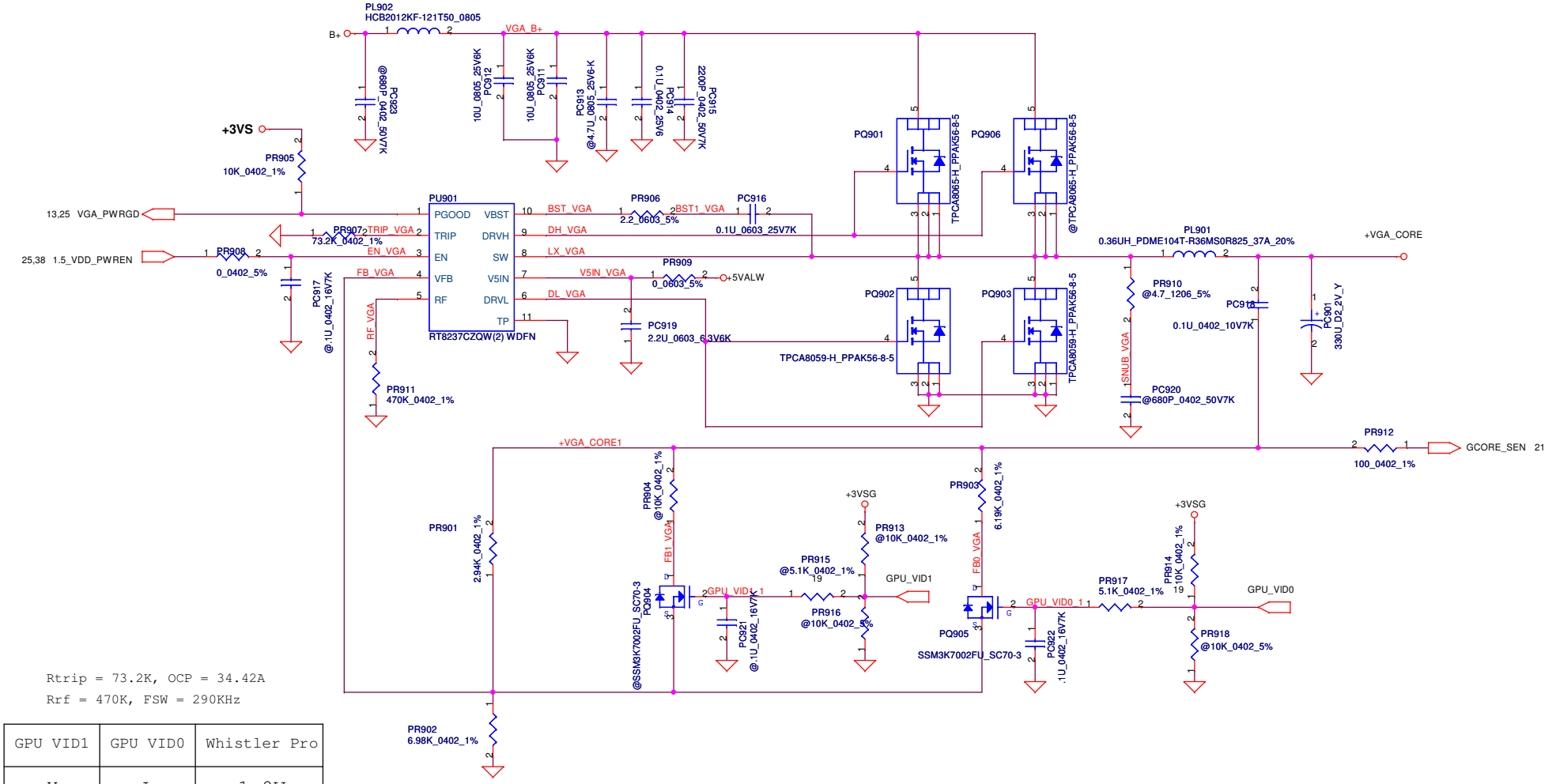

Rtrip = 73.2K, OCP = 34.42A

Rrf = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

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Compal Electronics, Inc.

Title: VGA_CORE

Size: | Document Number: LAXXXX | Rev: 0.1

Date: Tuesday, February 22, 2011 | Sheet 49 of 44

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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification: Compal Secret Data
Issued Date: 2008/09/15 Deciphered Date: 2010/12/31
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Compal Electronics, Inc.
Title: Changed-List History
Size: Document Number: LA-4902P Rev: 1.0
Date: Tuesday, February 22, 2011 Sheet 50 of 47