

Compal Confidential

QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

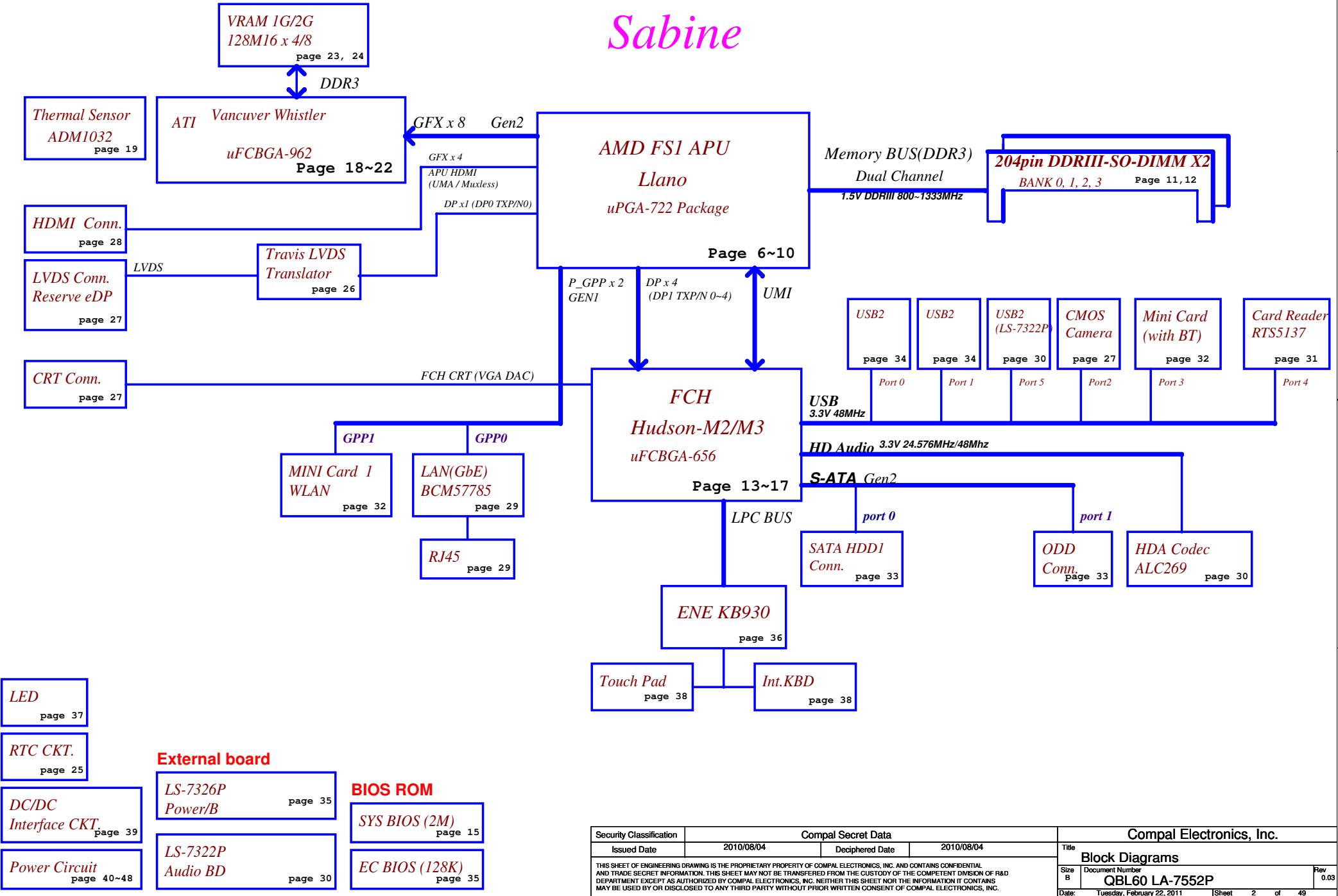
2010-02-16

LA-7552P REV: 0.03

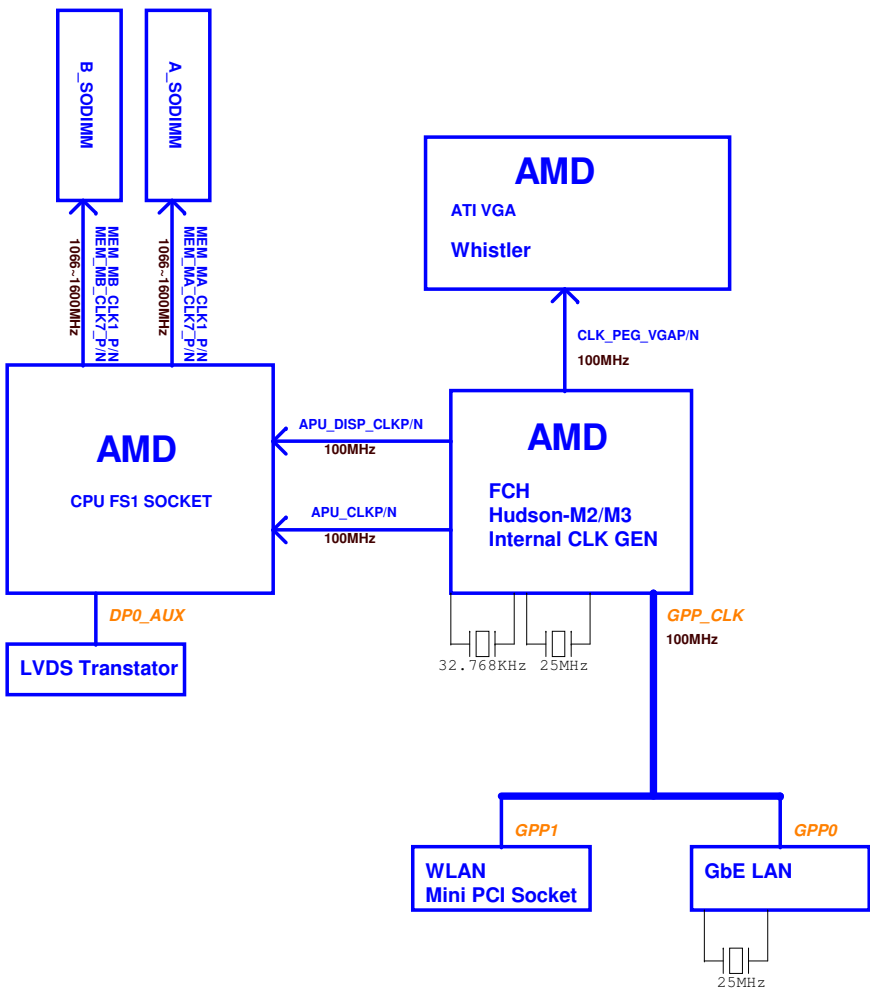
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title	
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				Size B	Document Number
				QBL60 LA-7552P	
Date: Tuesday, February 22, 2011				Sheet 1	Rev 0.03 of 49

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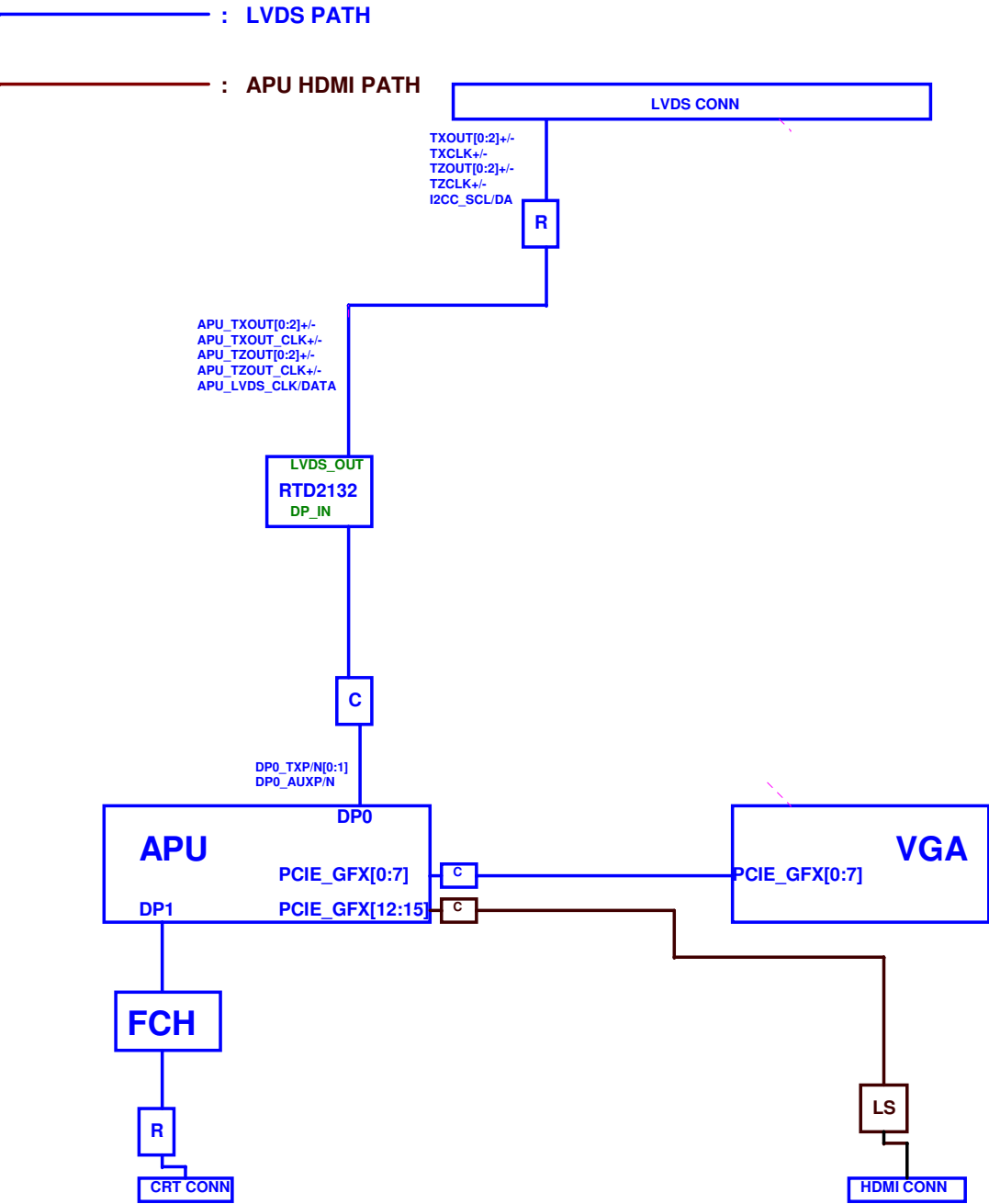
Model Name : QBL60



CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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				Sheet	3 of 49
				Rev	0.03

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			(APU)		
			RTD2132S (TL)		

FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

[illegible]

BOM Config

18 PCIE GTX_C_FRX_P[0..7]

18 PCIE GTX_C_FRX_N[0..7]

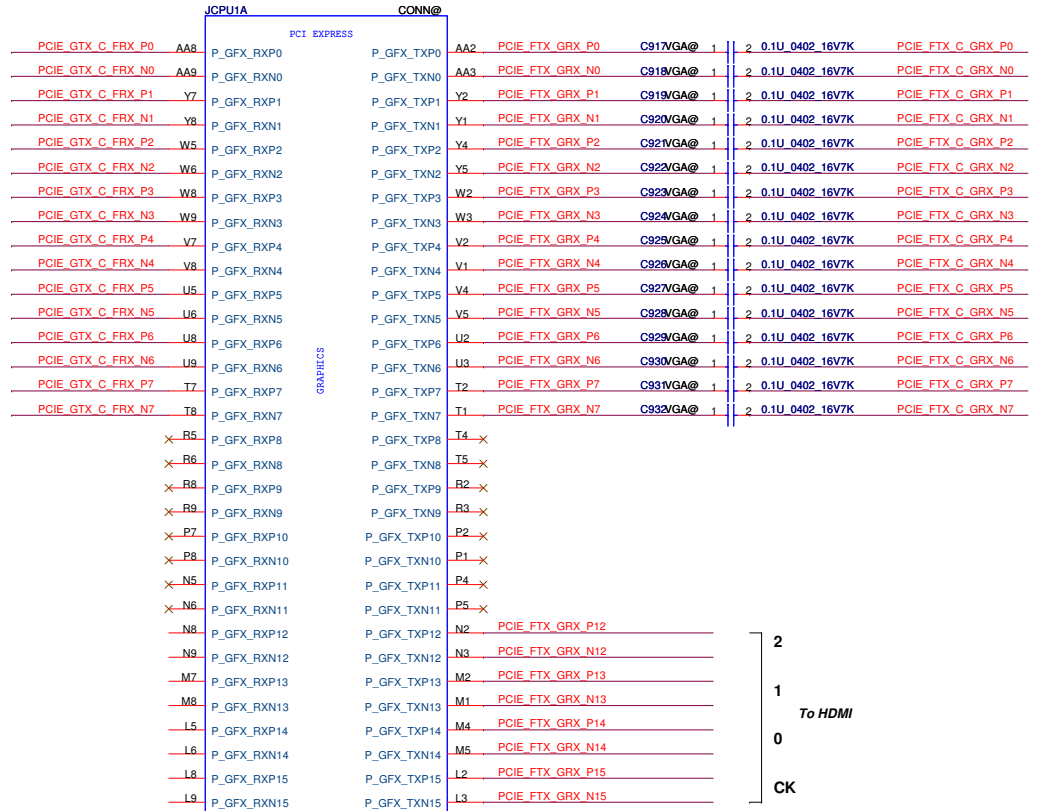
PCIE_FTX_C_GRX_P[0..7] 18

PCIE_FTX_C_GRX_N[0..7] 18

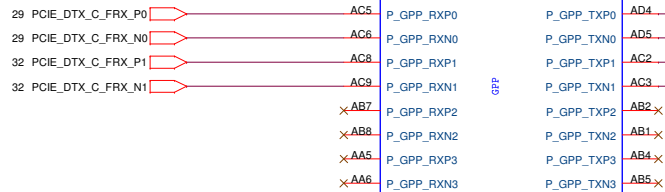
APU To HDMI

PCIE_FTX_GRX_P[12..15] 28

PCIE_FTX_GRX_N[12..15] 28

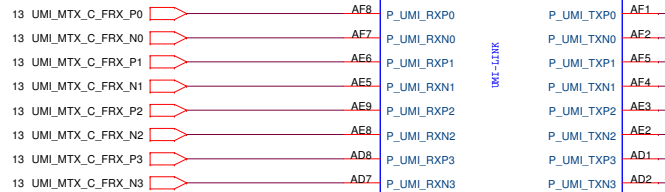


For UMA Mux.

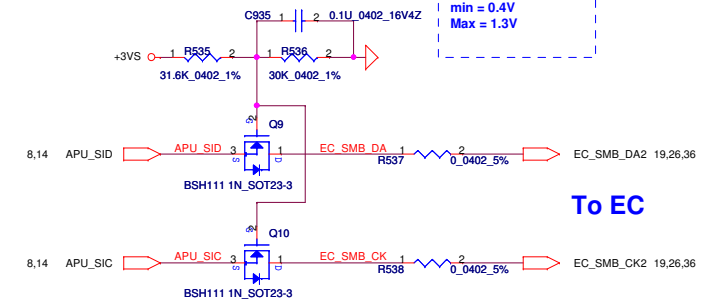


GLAN

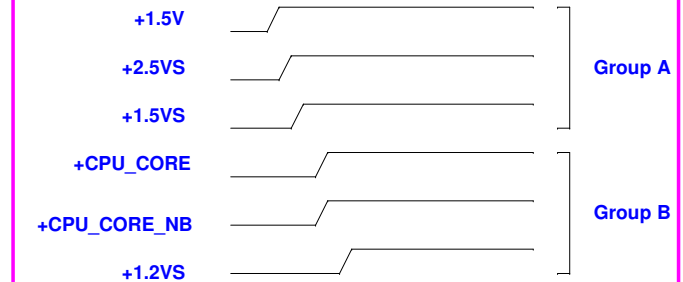
WLAN



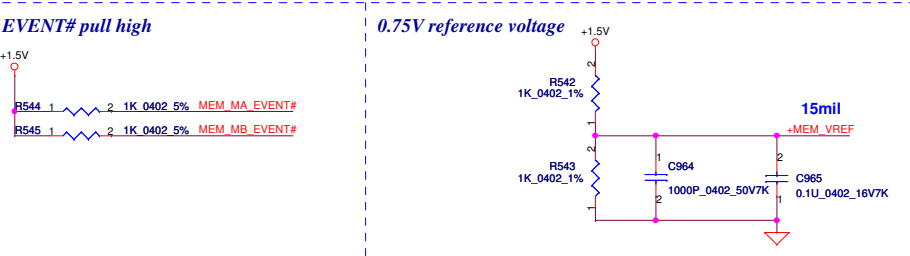
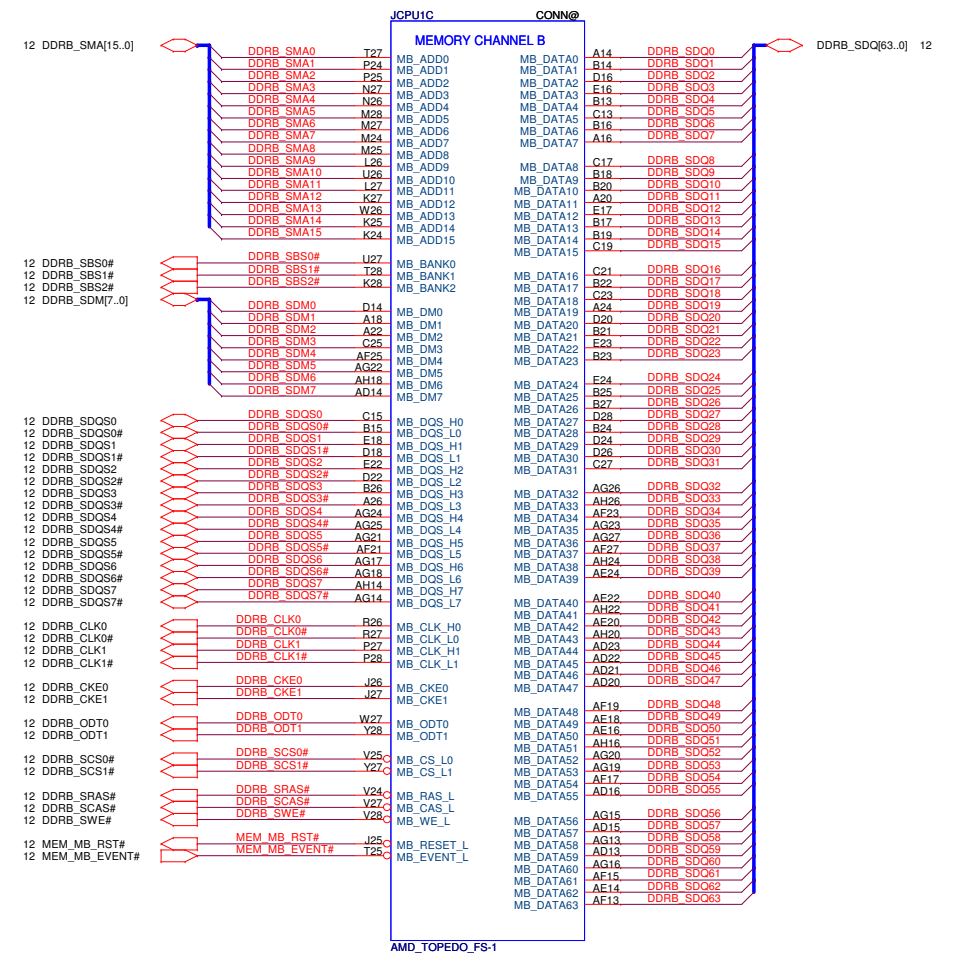
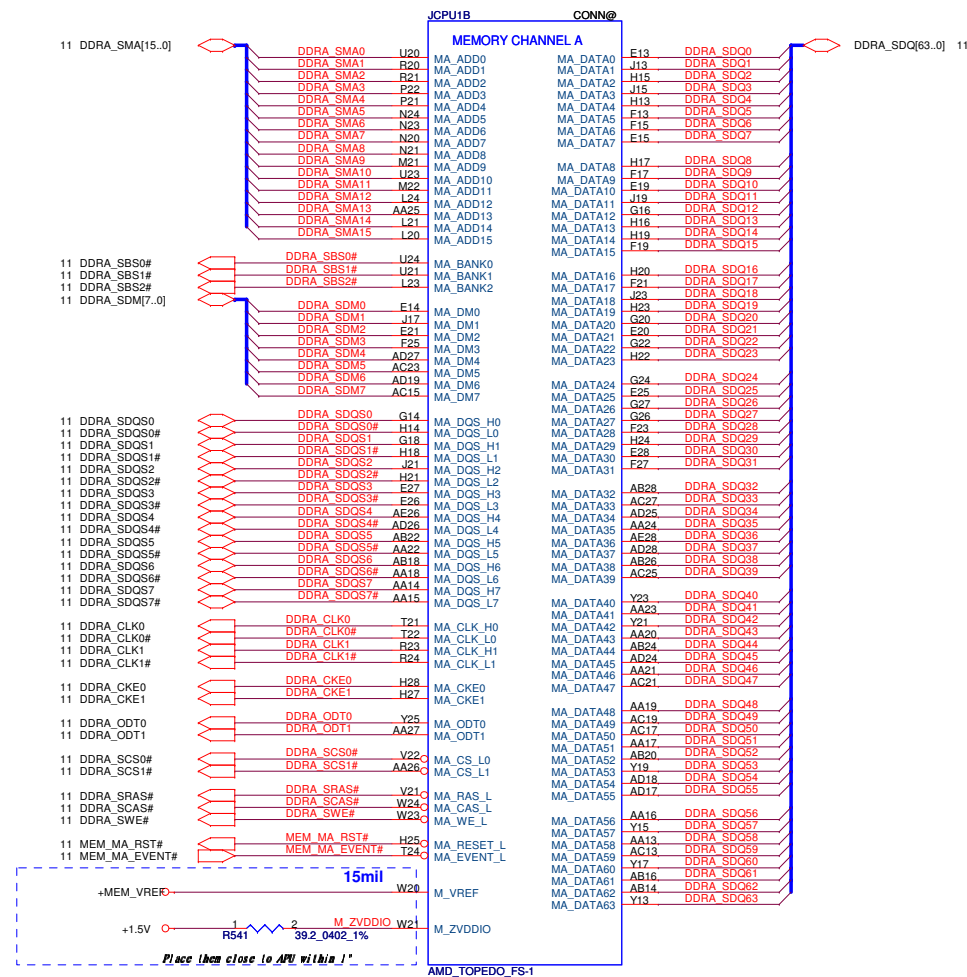
CPU TSI interface level shift



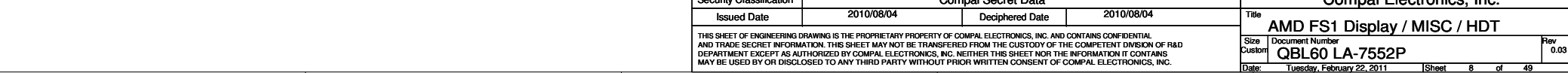
Power Sequence of APU



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				Size	Document Number
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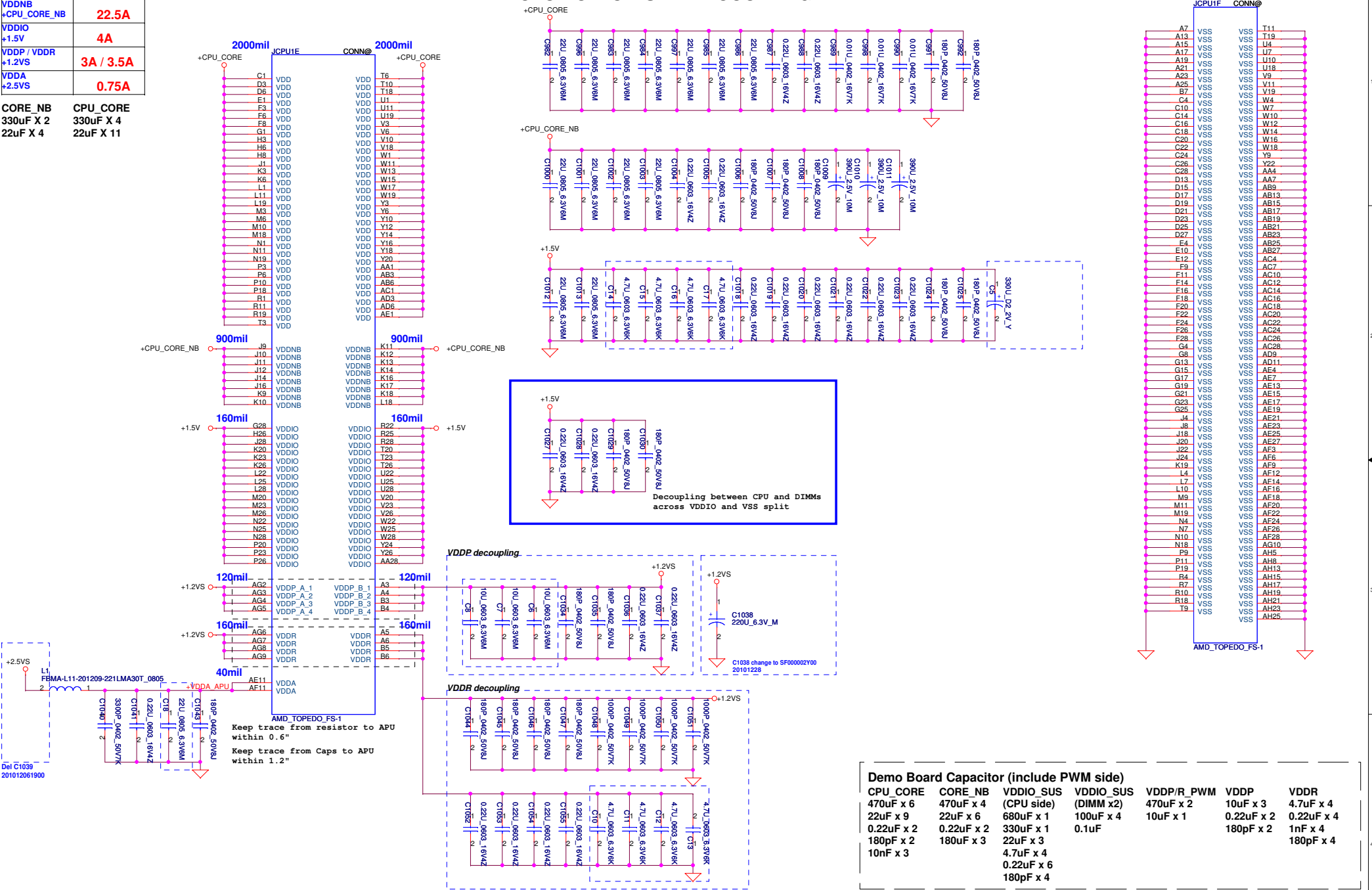
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Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

CPU BOTTOM SIDE DECOUPLING



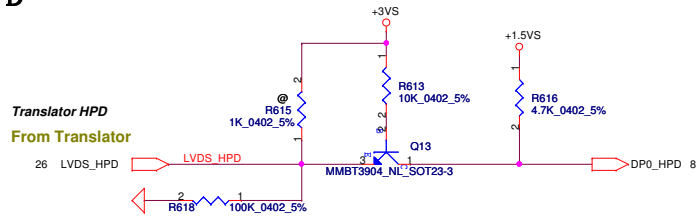
Demo Board Capacitor (include PWM side)						
CPU_CORE	CORE_NB	VDDIO_SUS	VDDIO_SUS	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	(CPU side)	(DIMM x2)	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	680uF x 1	100uF x 4	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	330uF x 1	0.1uF		180pF x 2	1nF x 4
180pF x 2	180uF x 3	22uF x 3				180pF x 4
10nF x 3		4.7uF x 4				
		0.22uF x 6				
		180pF x 4				

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HPD

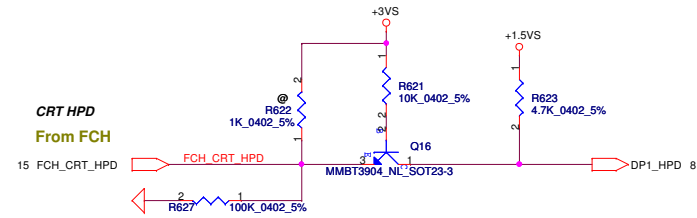
Translator HPD

From Translator



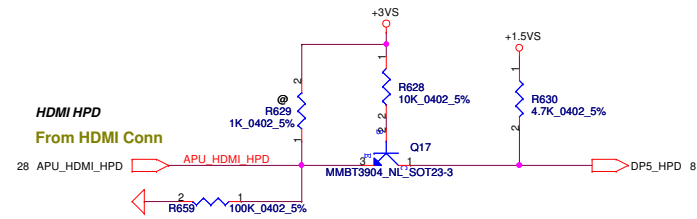
CRT HPD

From FCH

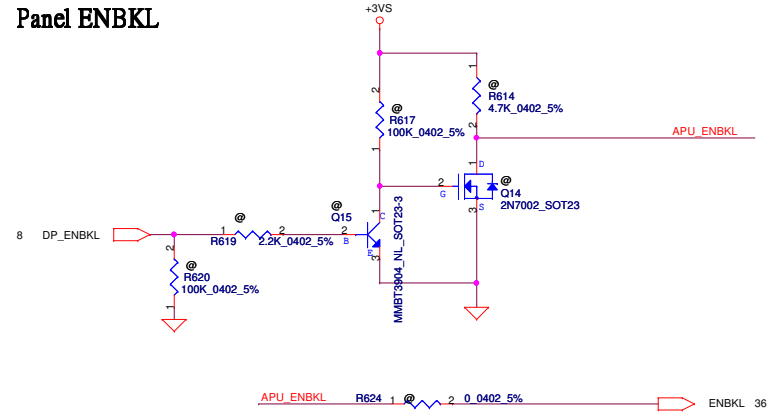


HDMI HPD

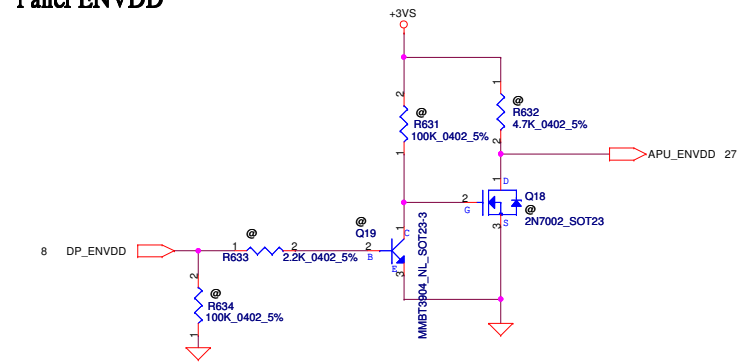
From HDMI Conn



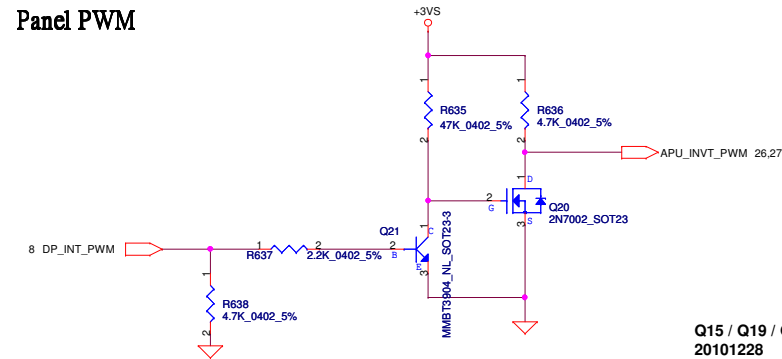
Panel ENBKL



Panel ENVDD

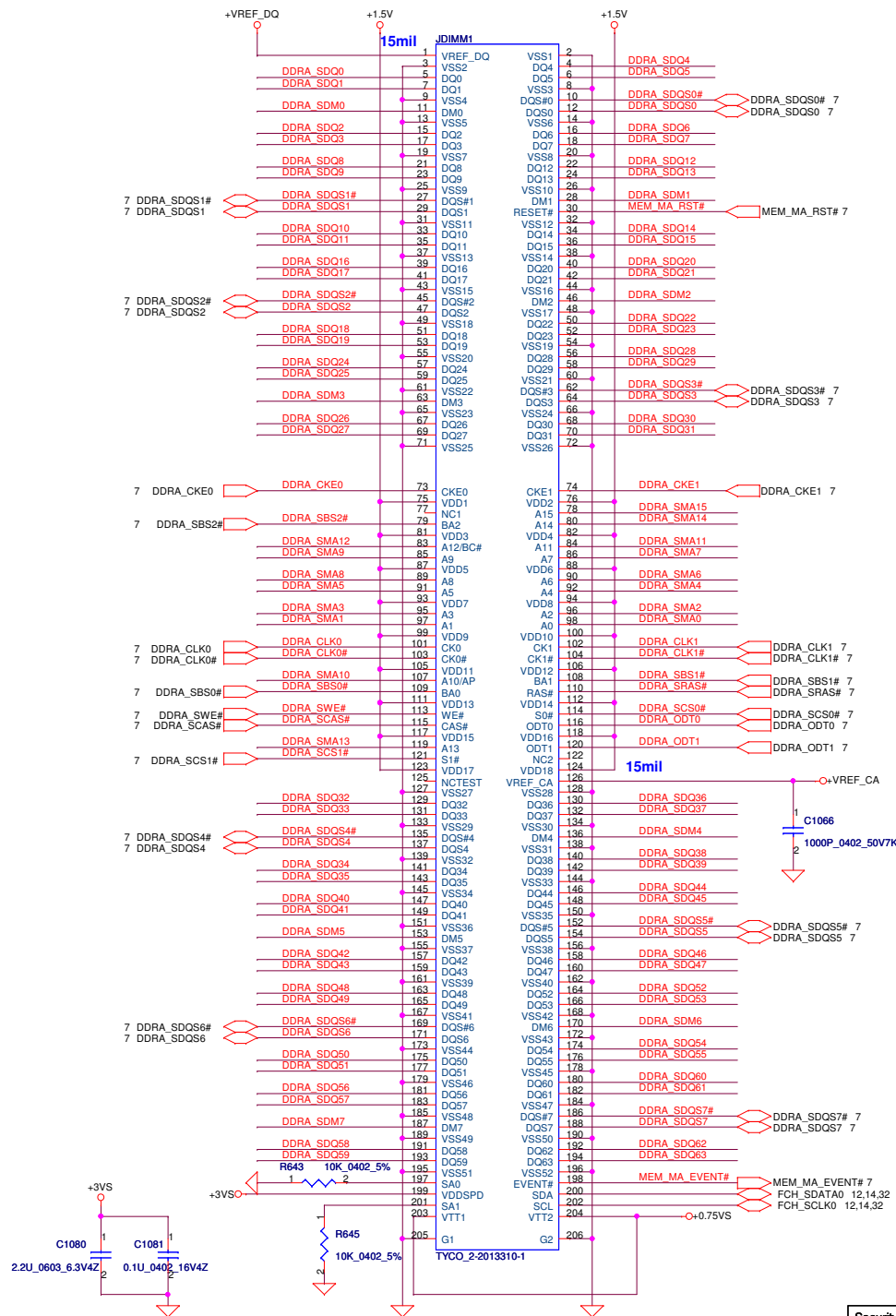


Panel PWM

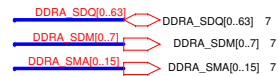


Q15 / Q19 / Q21 change to SB000006A00
20101228

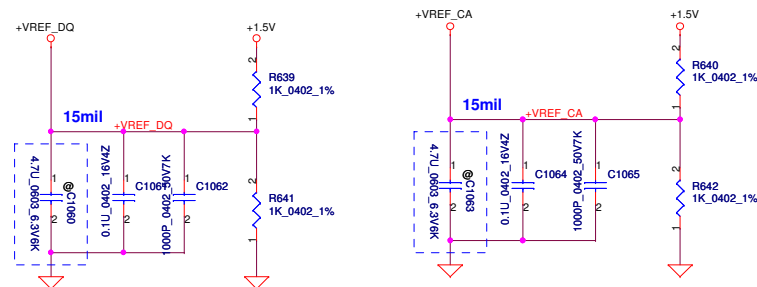
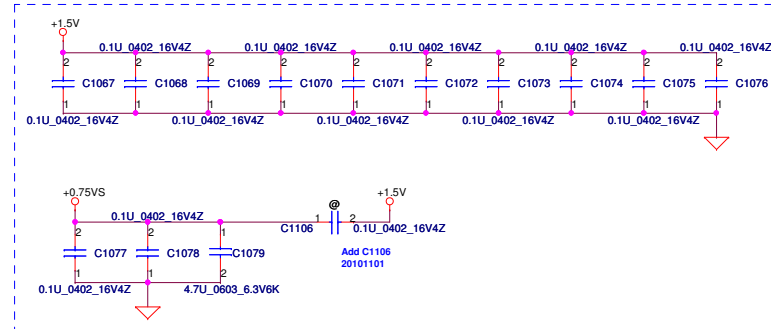
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								Size	Document Number	Rev
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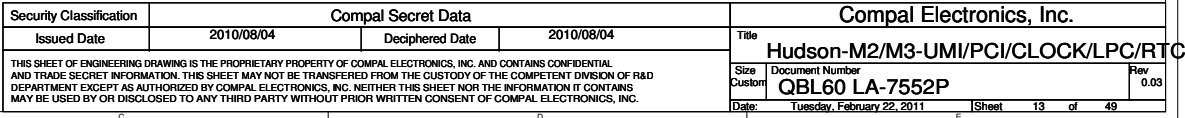
DIMM_A STD H:9.2mm
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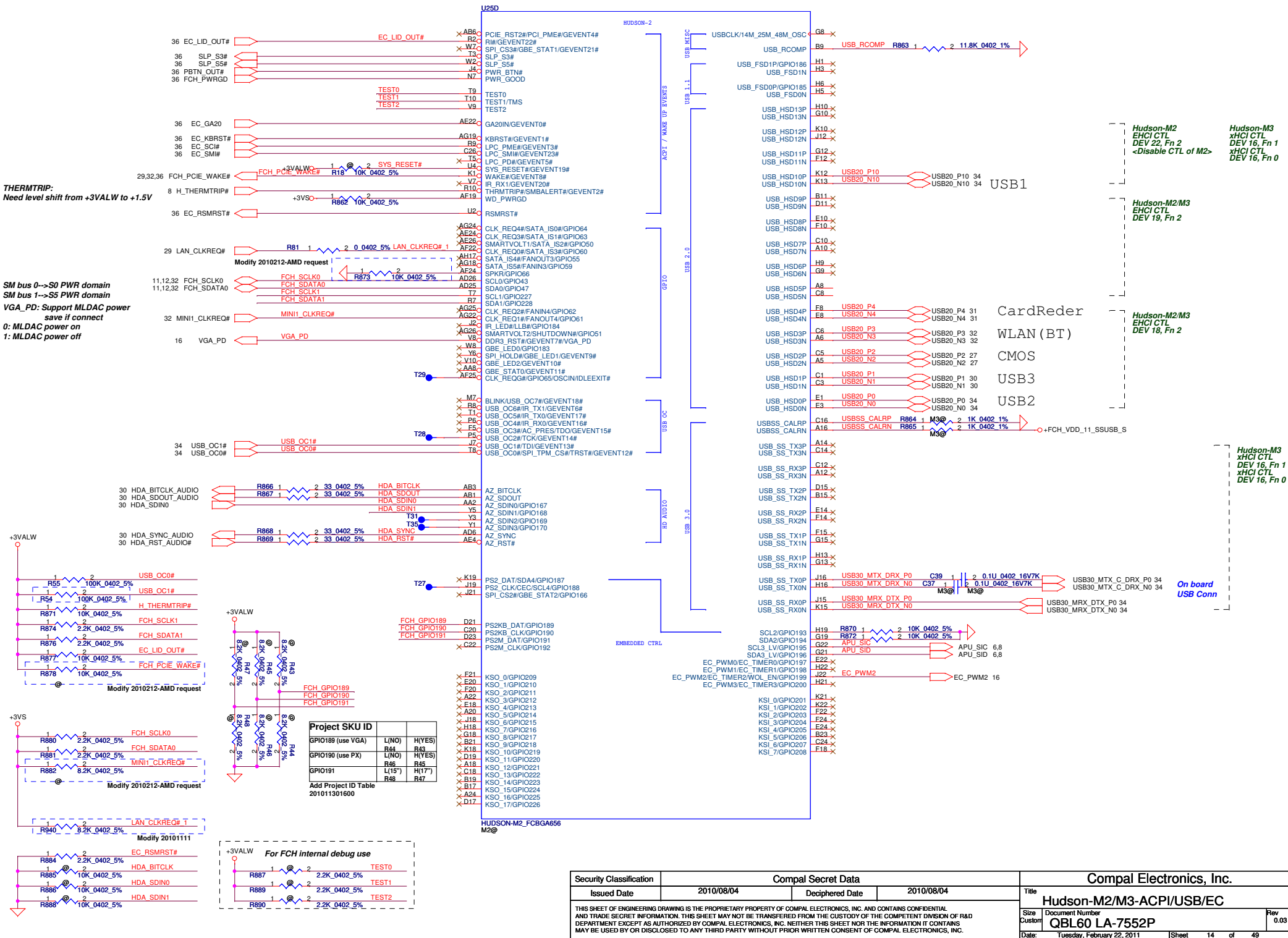


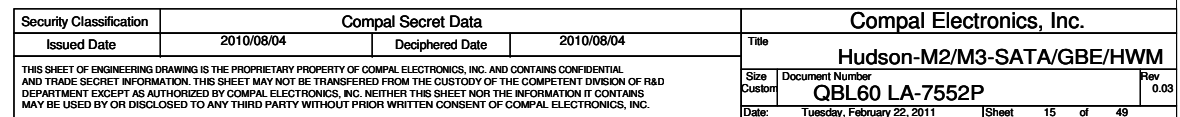
Place near DIMM1



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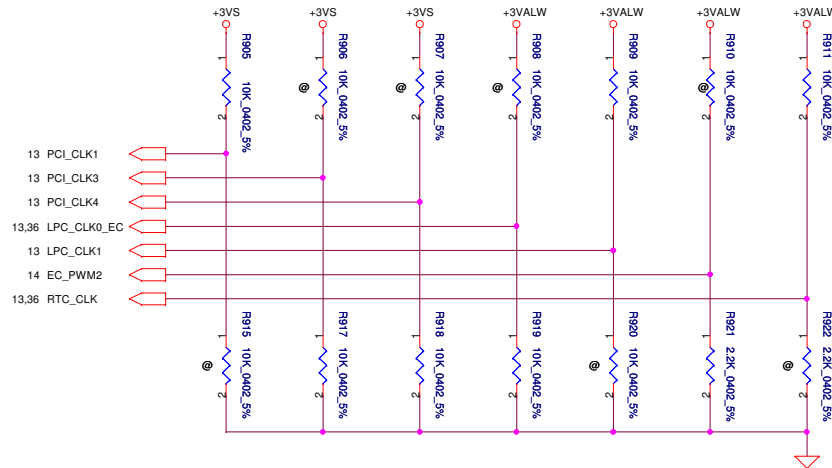






STRAP PINS

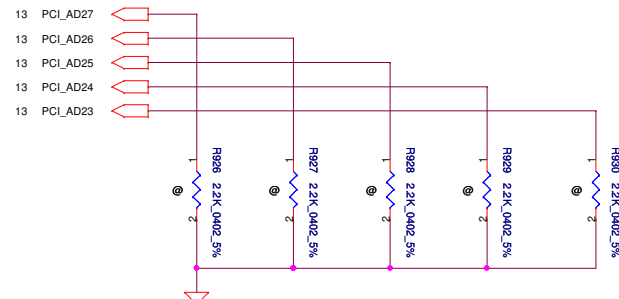
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



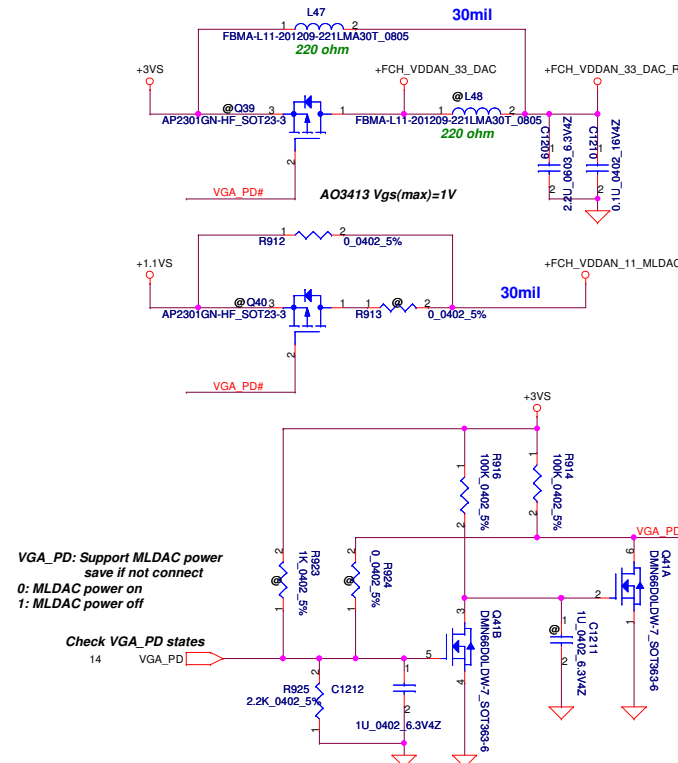
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

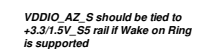
PCI_AD26		PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
	PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
	PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



If support ML DAC power down when no VGA plug

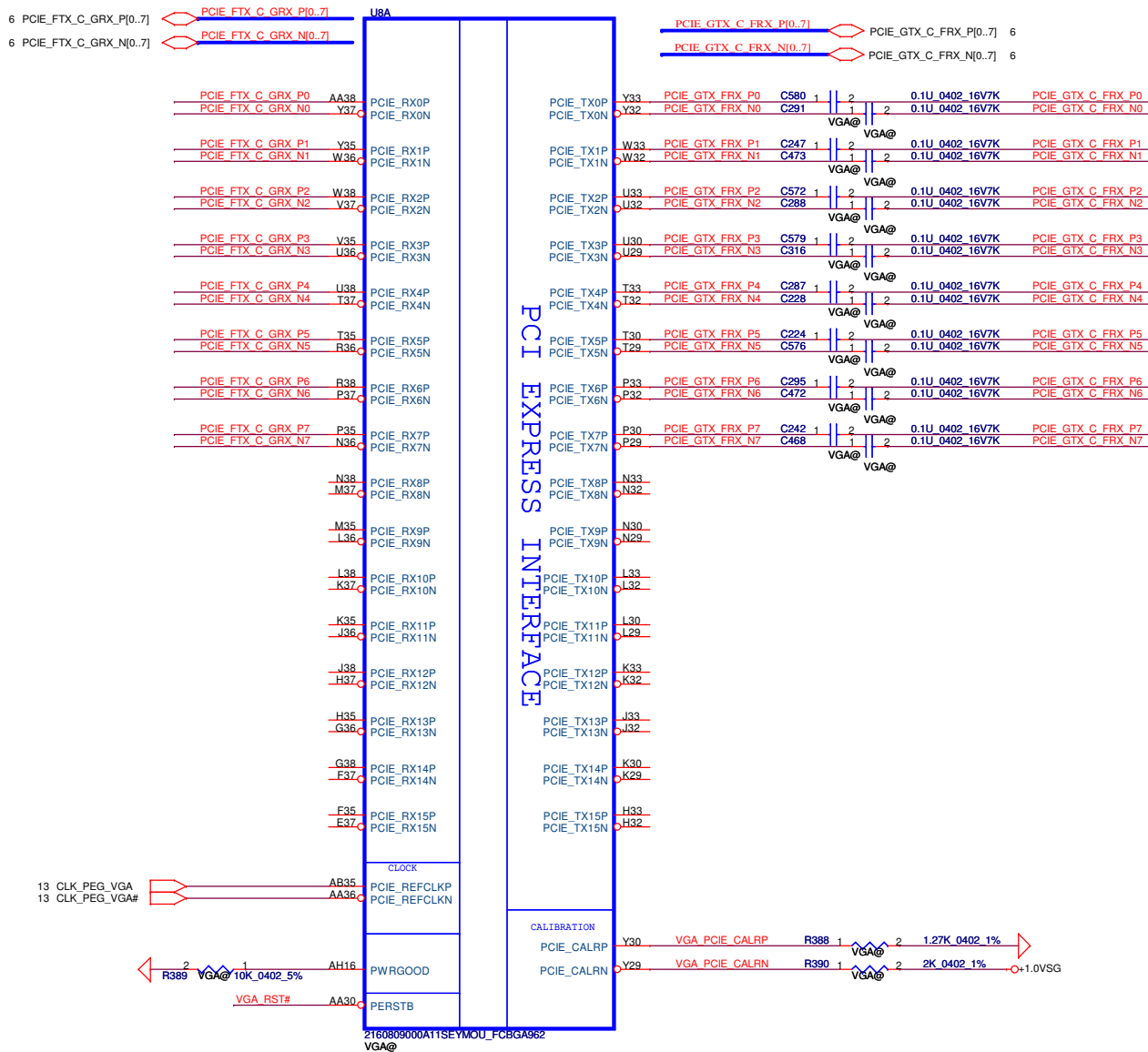


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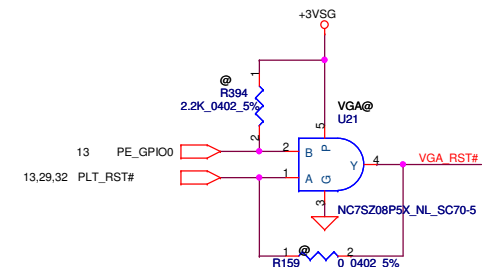
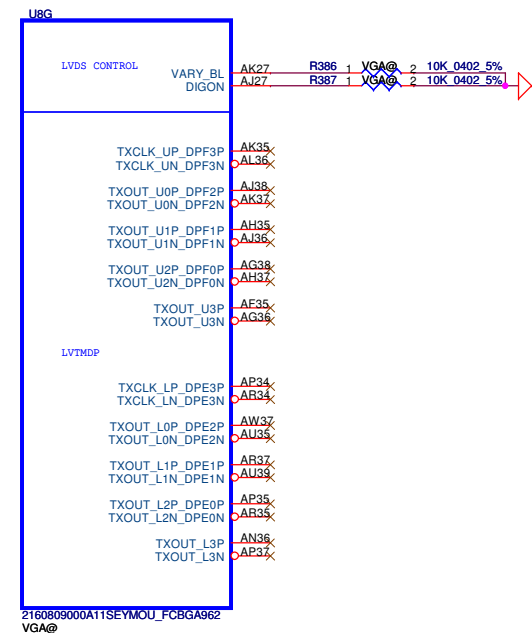
GFX PCIE LANE REVERSAL



For UMA Mux.

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High ,external PD need



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										Vancouver_PCIE / LVDS	
										Document Number	
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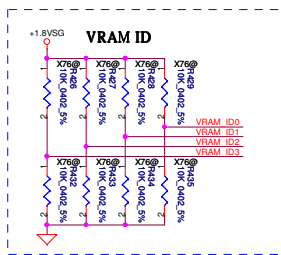
Strap Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNCR (GENLK_VSYNCR) VIP Device Strap Enable Indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHA0_0 during reset 1: VHA0_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPI09 VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPI00 Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPI01 PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPI013 GPI012 GPI011 GPI010 GPI013,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPI022 Enable external BIOS ROM device (Internal PD) 0: Disable, 1: Enable	0
AUD[1]	HSYNCR AUD[0] VSYNCR 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPI02 Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNCR GPI08 GPI021 Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs



GPI05 fast-power reduction:
HW control will cause display disturb
should use SW method control
GPI06 voltage control signal, No use can NC!

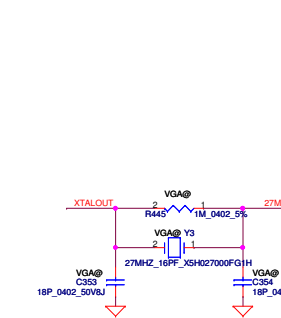
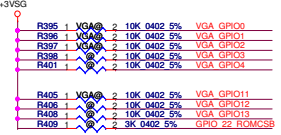
Move to DDCLKL_AUX3P,DDCDA2_AUX3N,

GPI07 Controls backlight on/off.
Active High, need external PD
If GPI022 High, GPI0 11-13->CFG[0:2]
Config ROM type, GPU has internal PD

GPI06,15,16,20
Voltage control signal
GPI06,15 no use can NC
Thermal monitor interrupt

Critical temperature fault
Reserved

External BIOS device
DN(1)/OFF(0) Inter PD
Internal Debug
no use can floating
ON(1)/OFF(0)
Stereo Sync
no use can NC
For ATI Cross fire
no use can NC



SM010030010
200ma 120ohm@100mhz DCR 0.2

AMD ref:470ohm/1A

AMD ref:470ohm/1A

AMD ref:470ohm/1A

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AMD ref:470ohm/1A

Future ASIC call MLPS.
OLD ASIC is Fan PWM

Future ASIC call MLPS.
OLD ASIC is Fan PWM

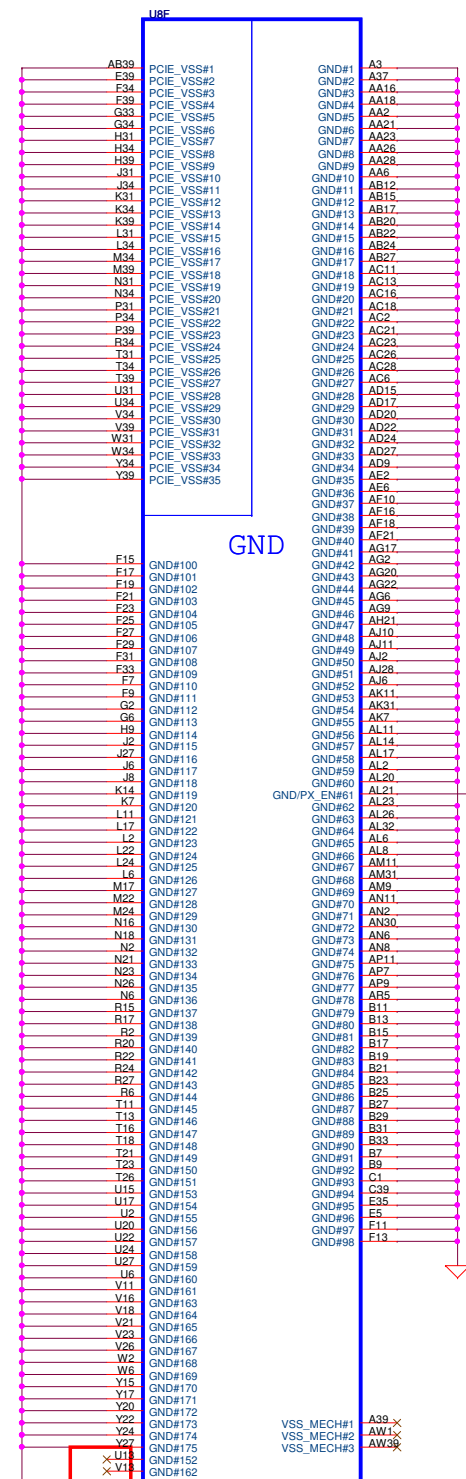
Future ASIC call MLPS.
OLD ASIC is Fan PWM

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OLD ASIC is Fan PWM

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OLD ASIC is Fan PWM

Future ASIC call MLPS.
OLD ASIC is Fan PWM

NUT1 GFX																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			</
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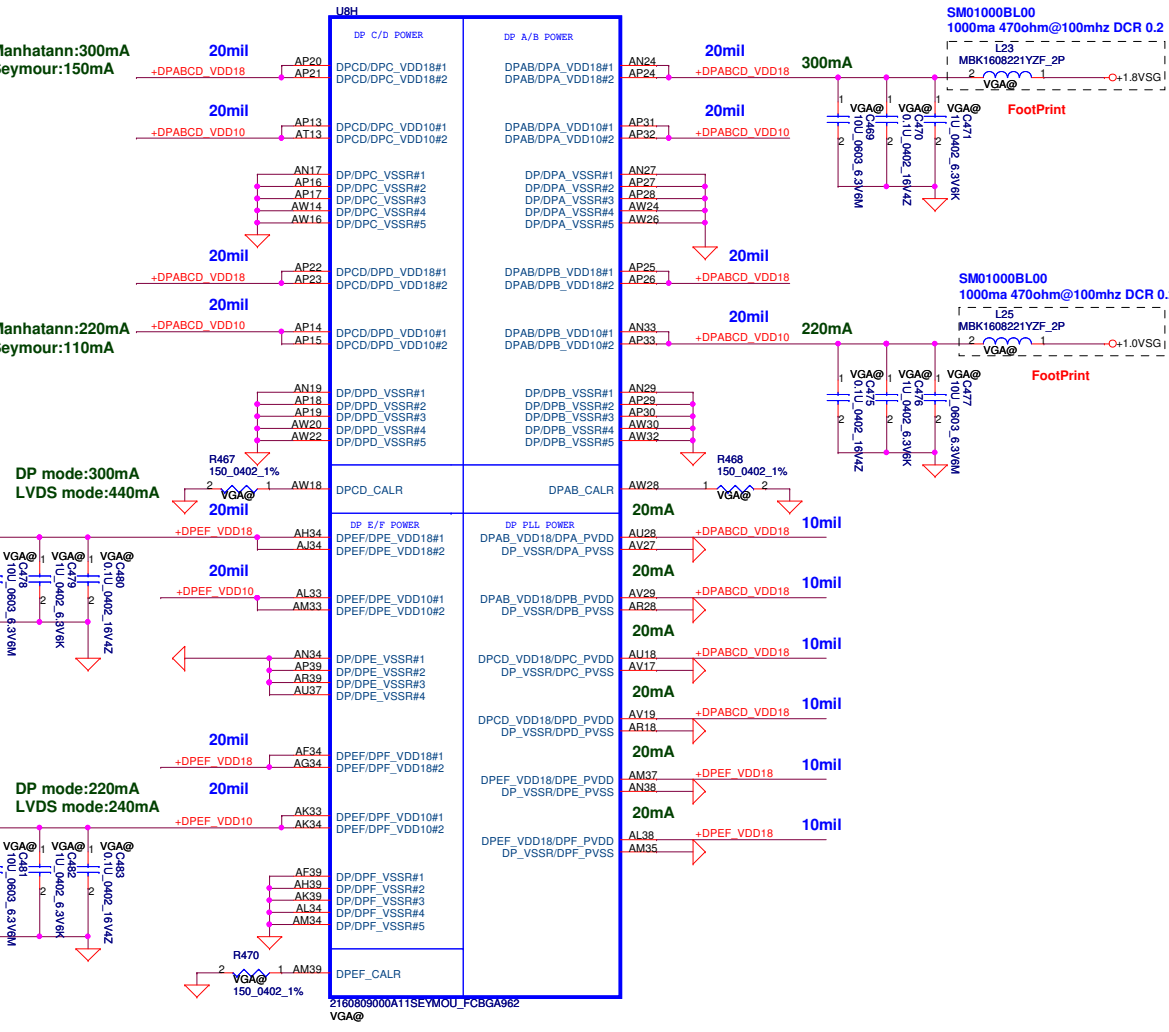
DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

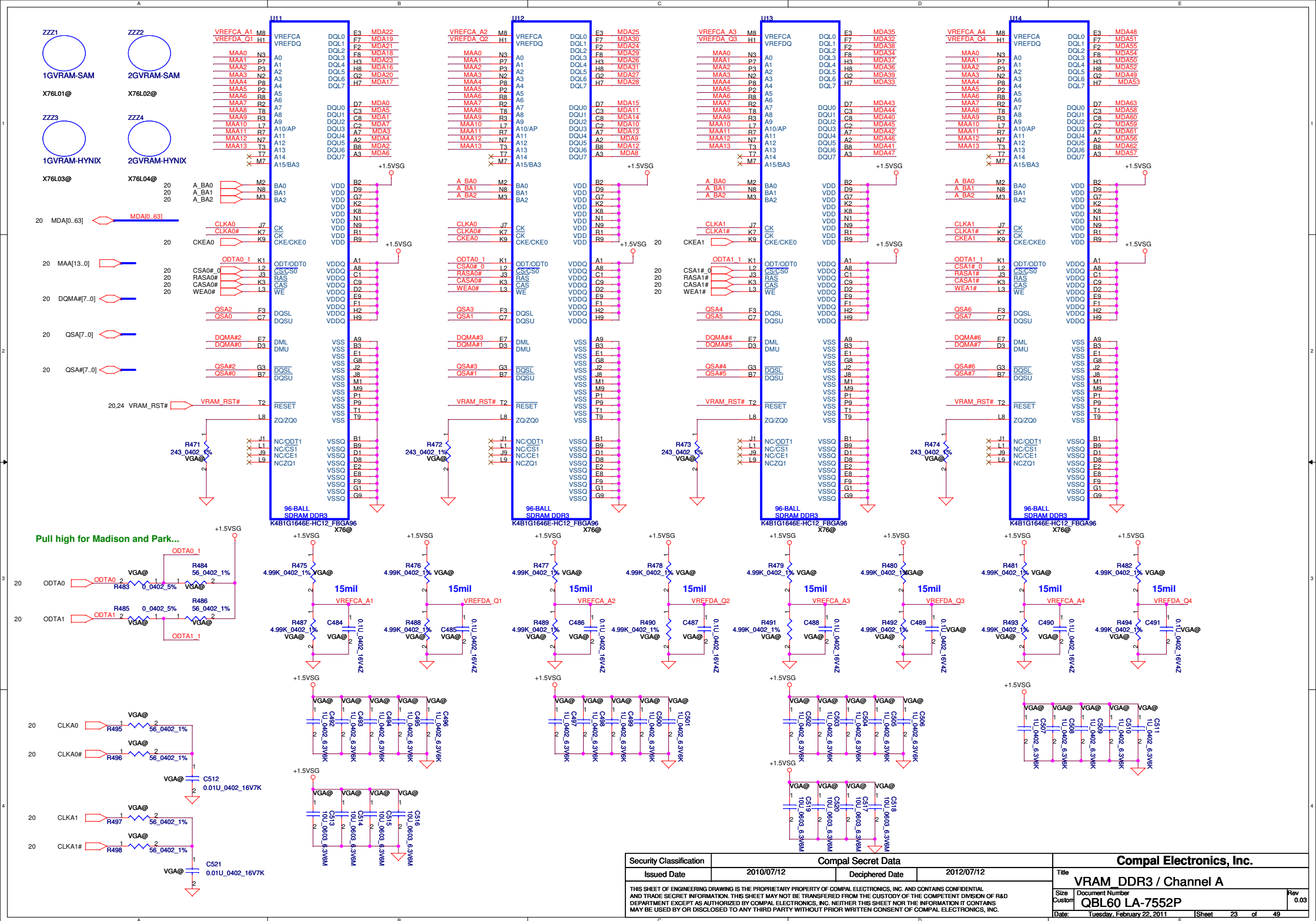
Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

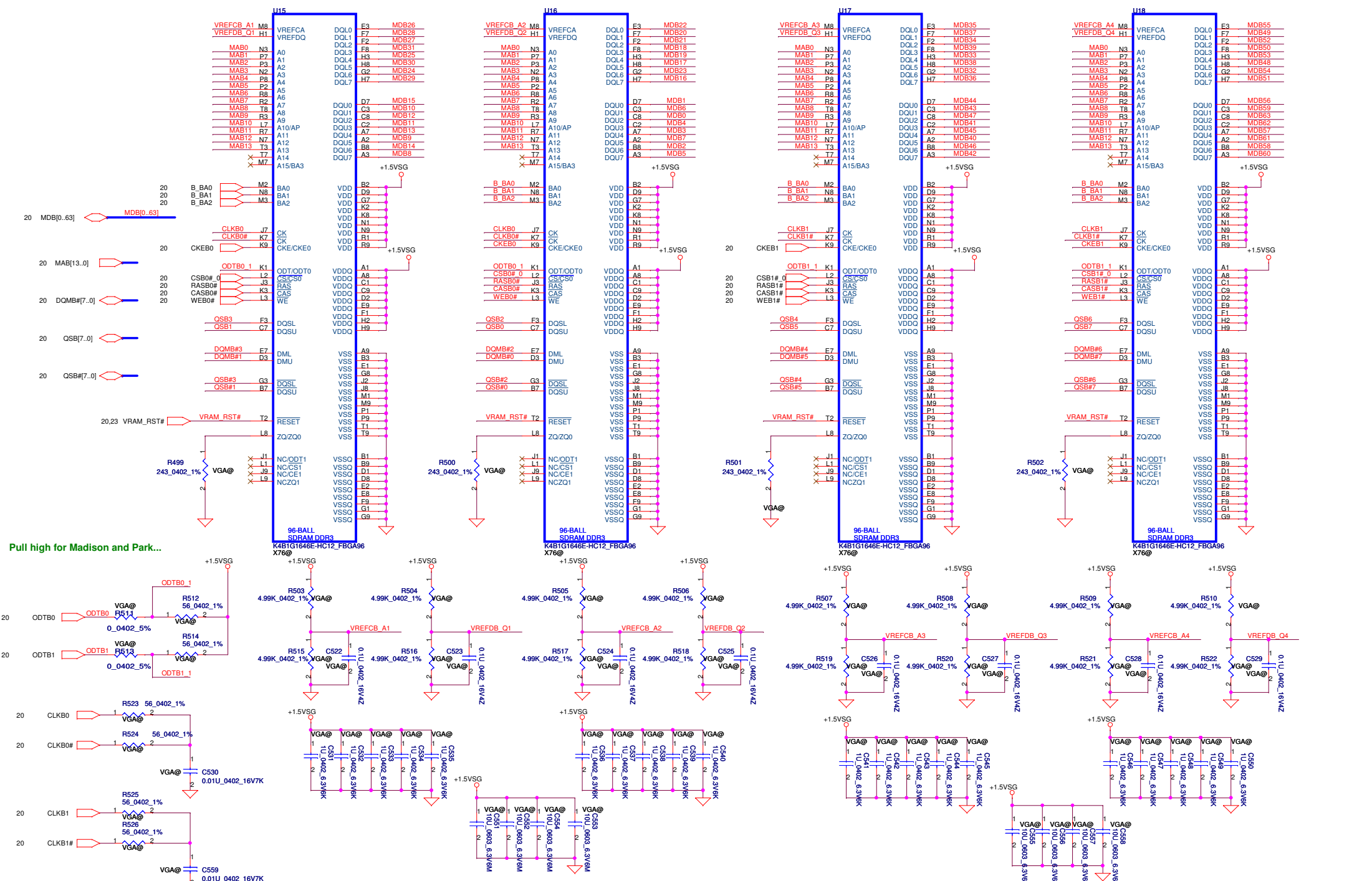
Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC



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				Date	Tuesday, February 22, 2011
				Sheet	22 of 49

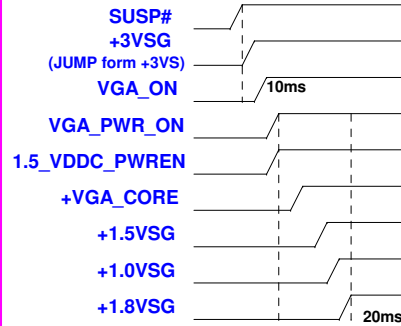




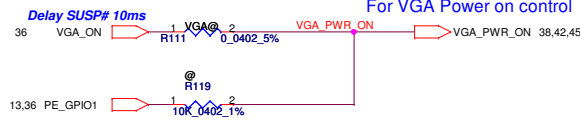
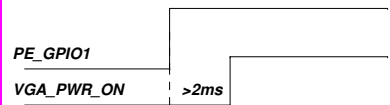
Pull high for Madison and Park...

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								VRAM DDR3 / Channel B			
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Power Sequence of Whistler and Seymour



For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

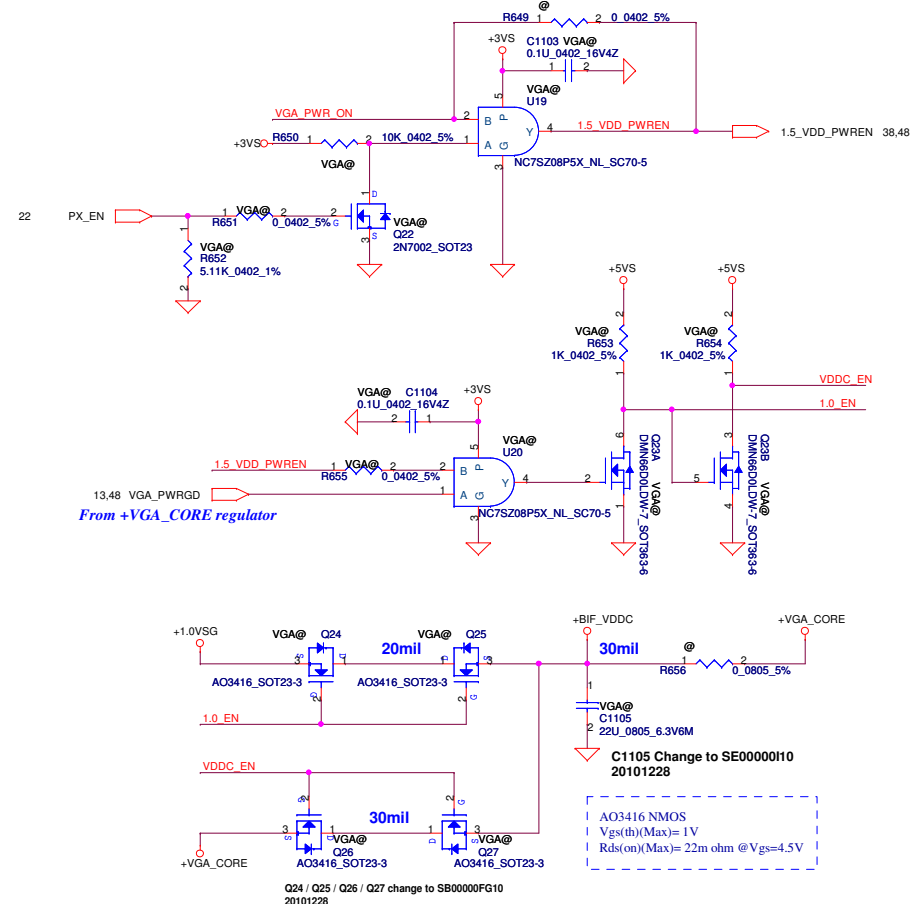


VGA Muxless with BACO Status Mapping table

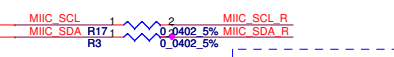
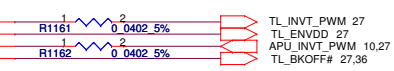
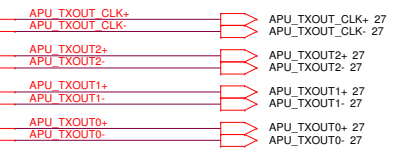
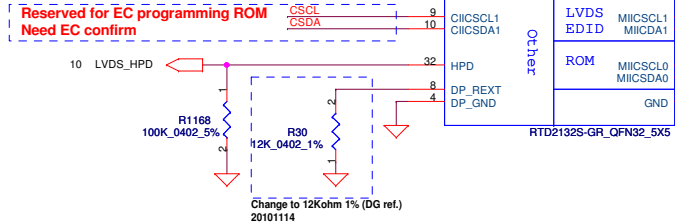
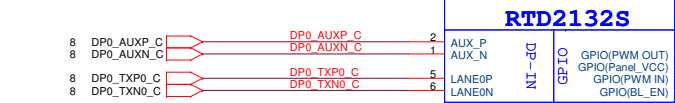
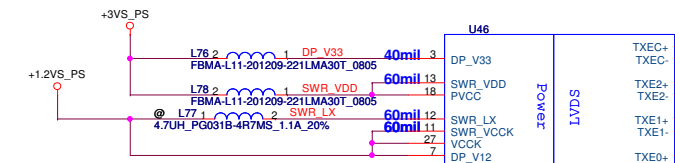
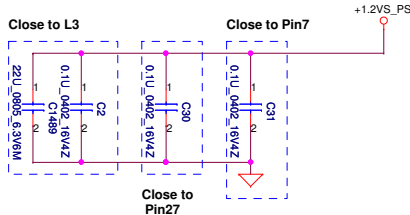
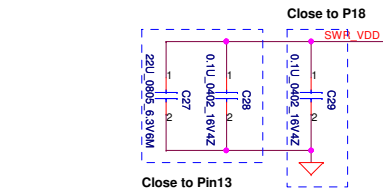
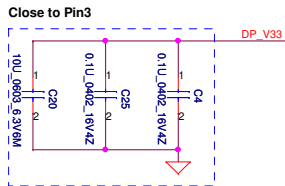
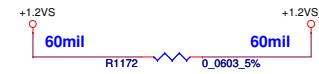
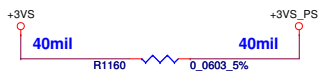
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

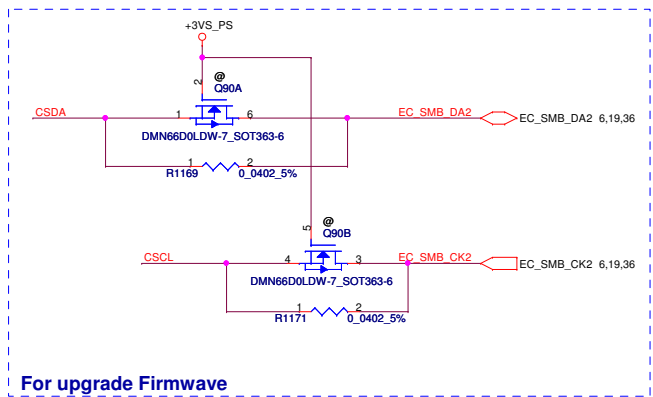
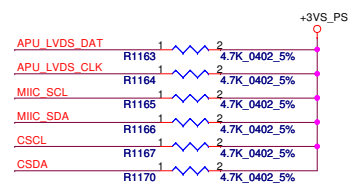
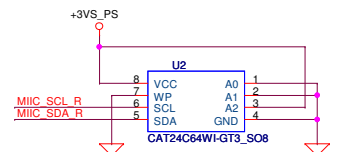
VGA_PWR_ON source signal	Whistler
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN



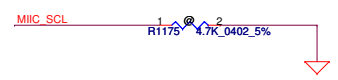
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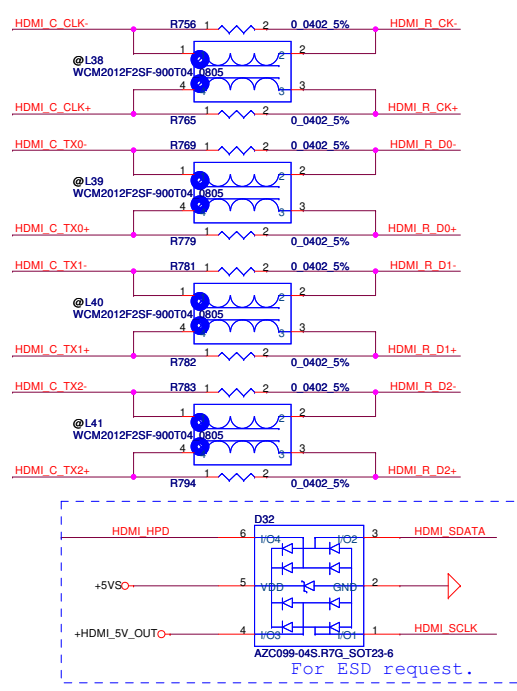
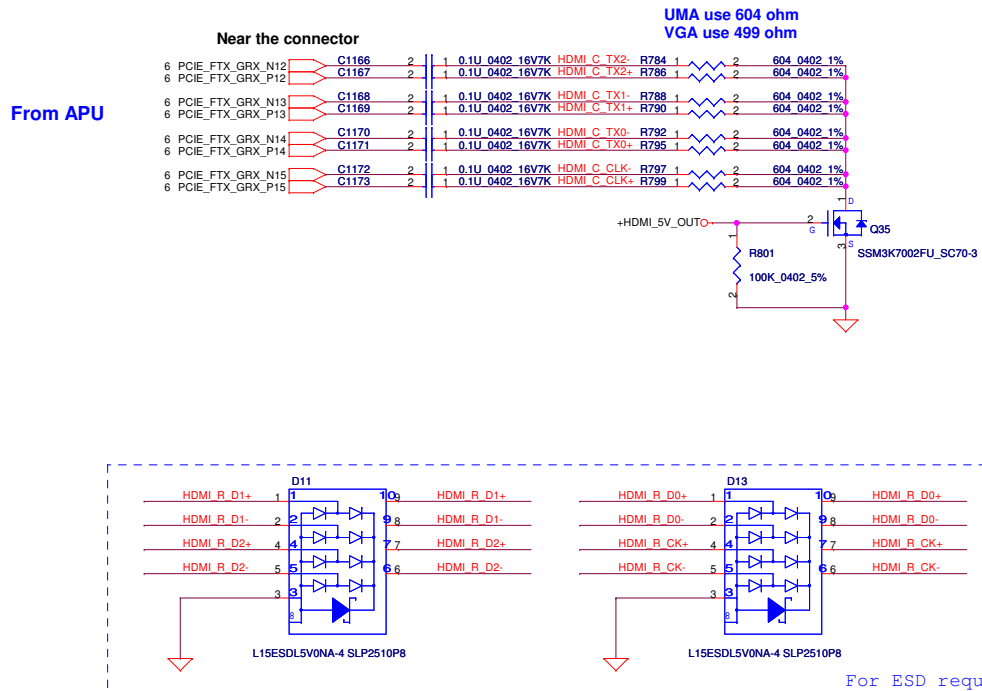
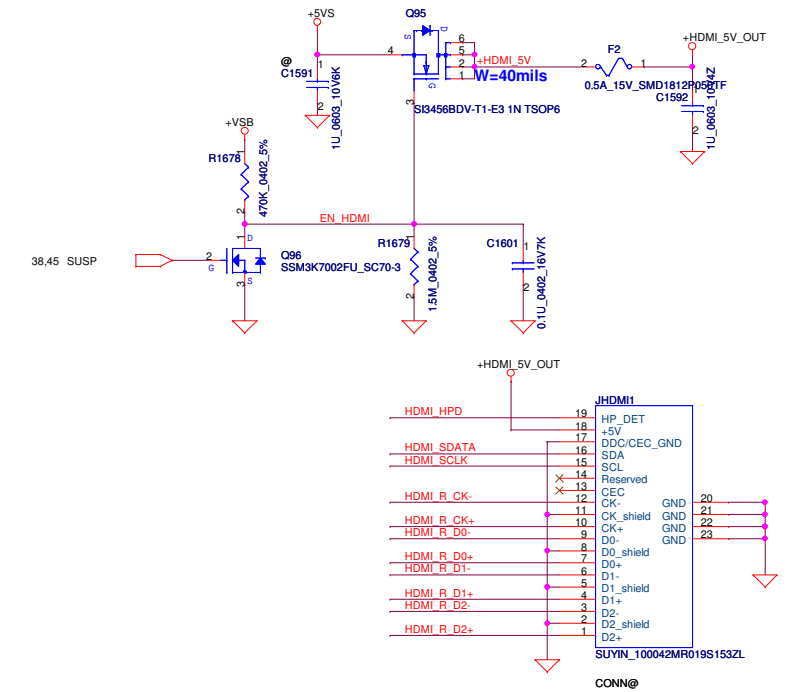
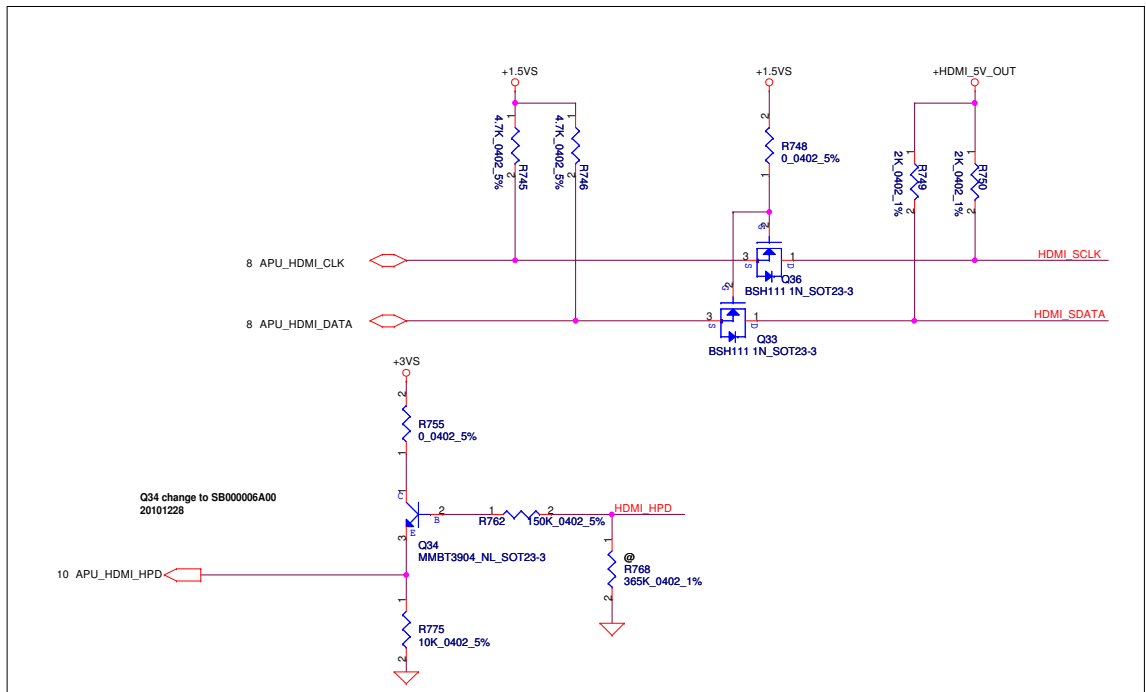
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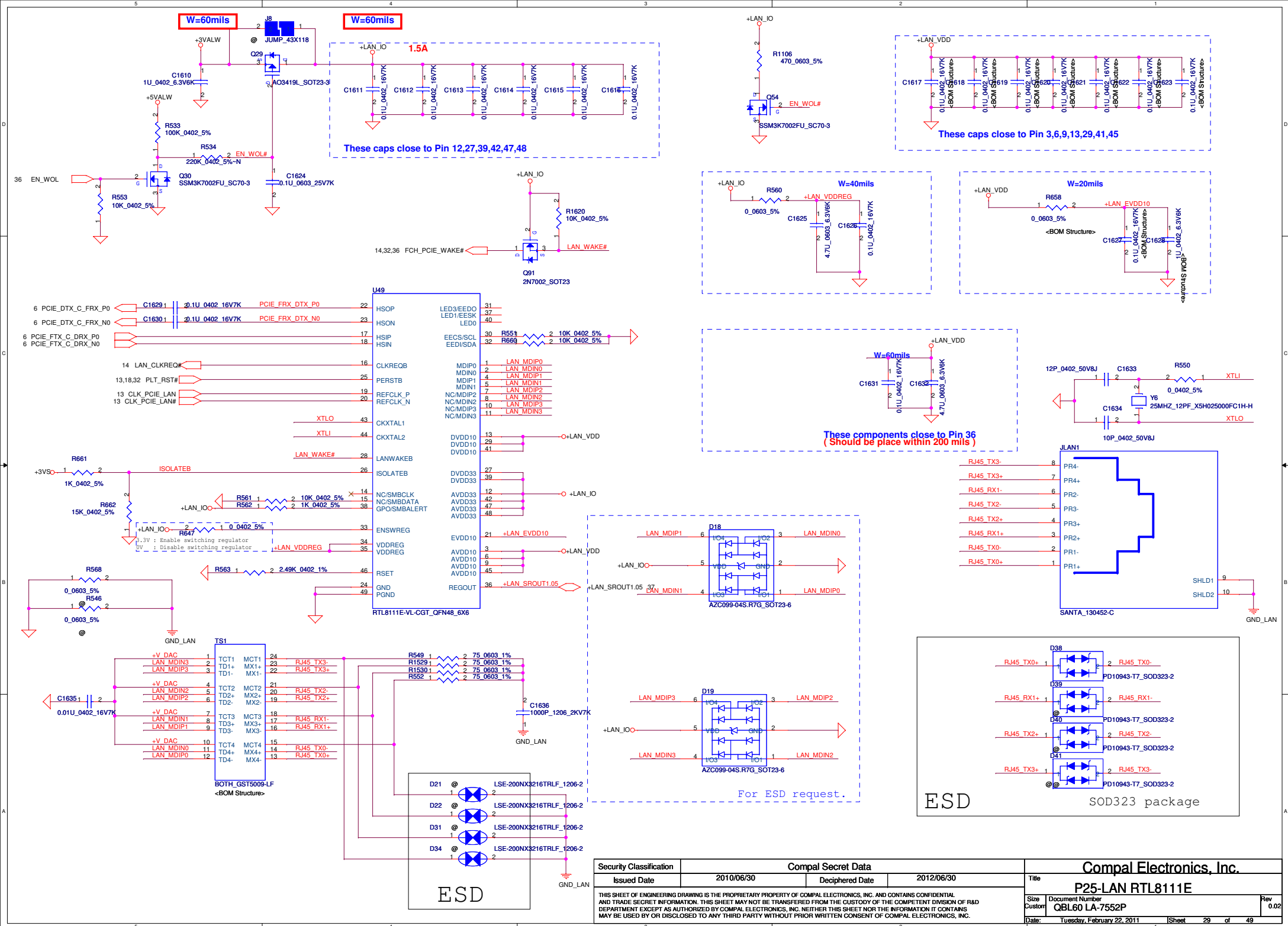
For upgrade Firmwave

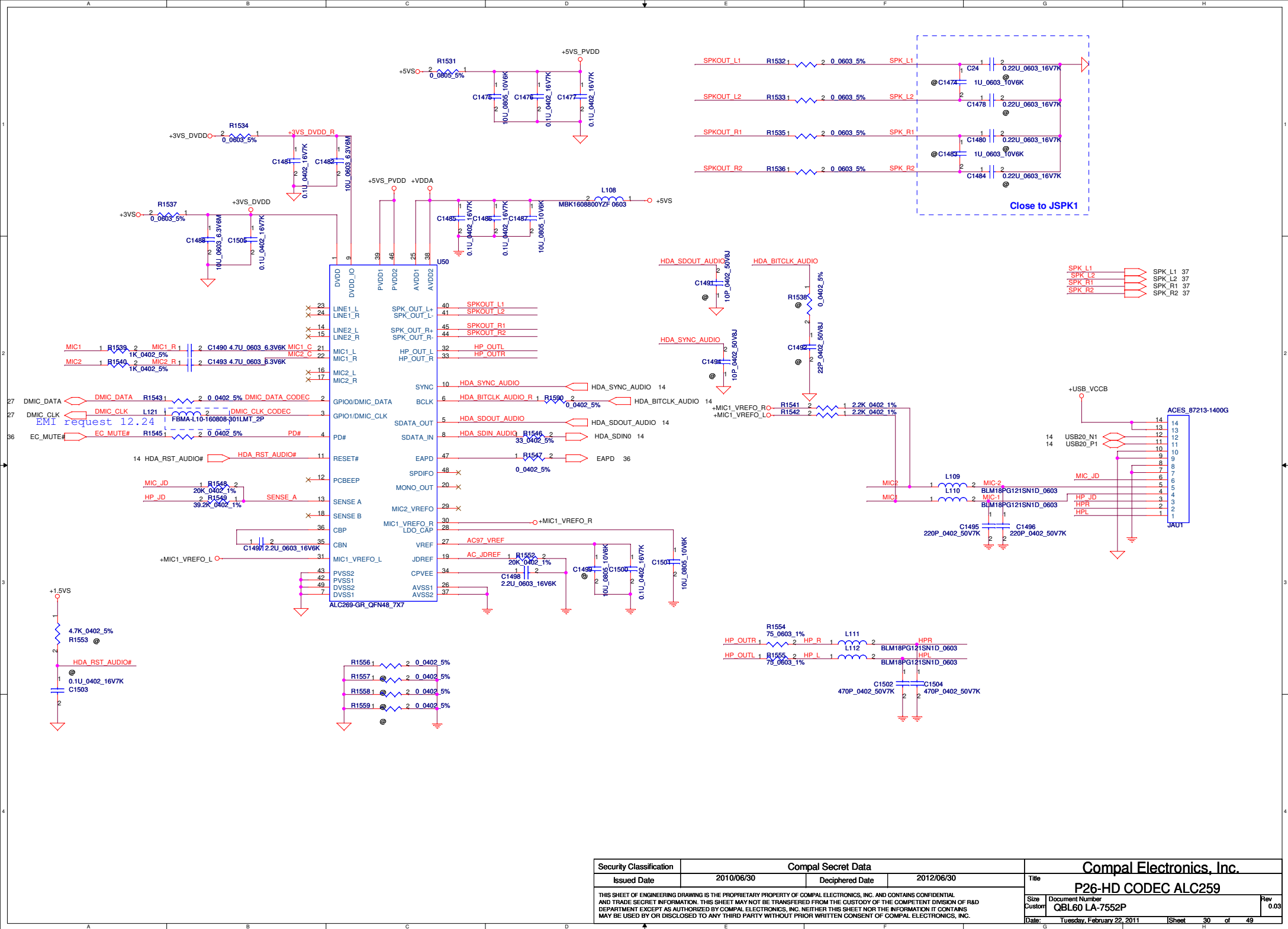


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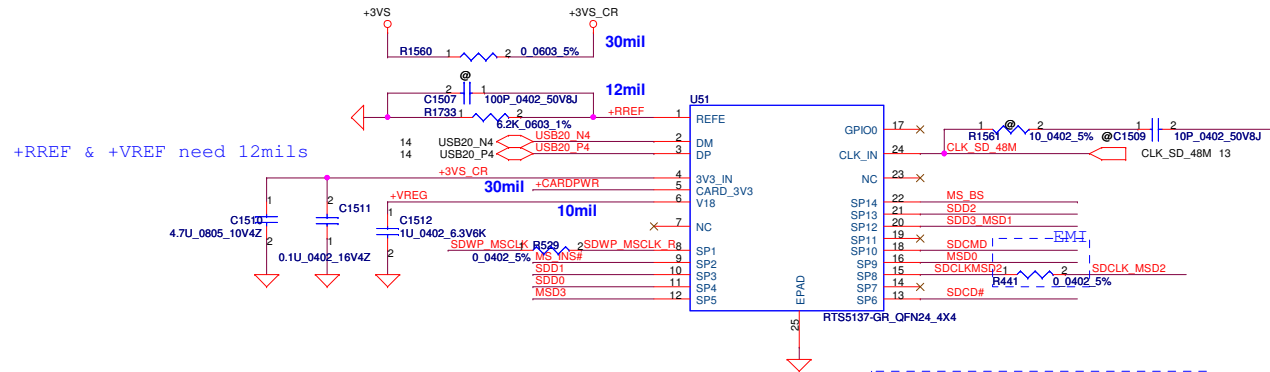


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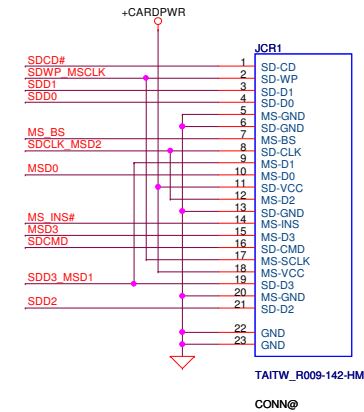
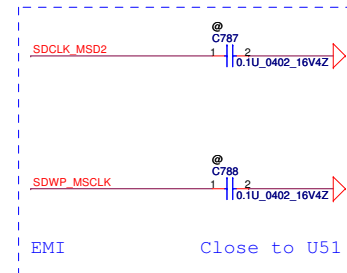
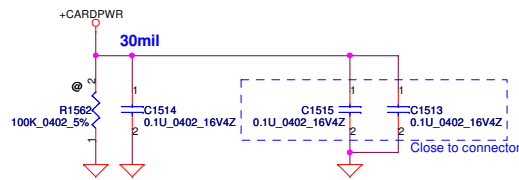




Card Reader RTS5137 (only SD/MMC/MS function)

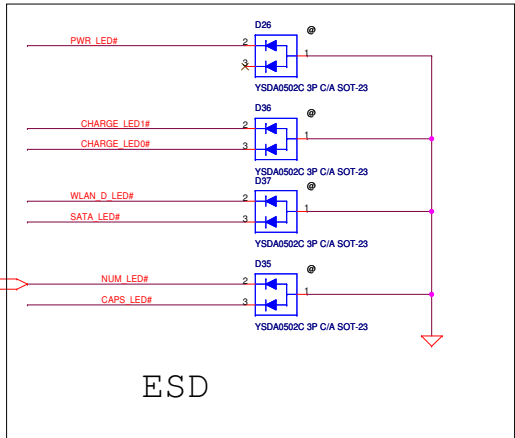
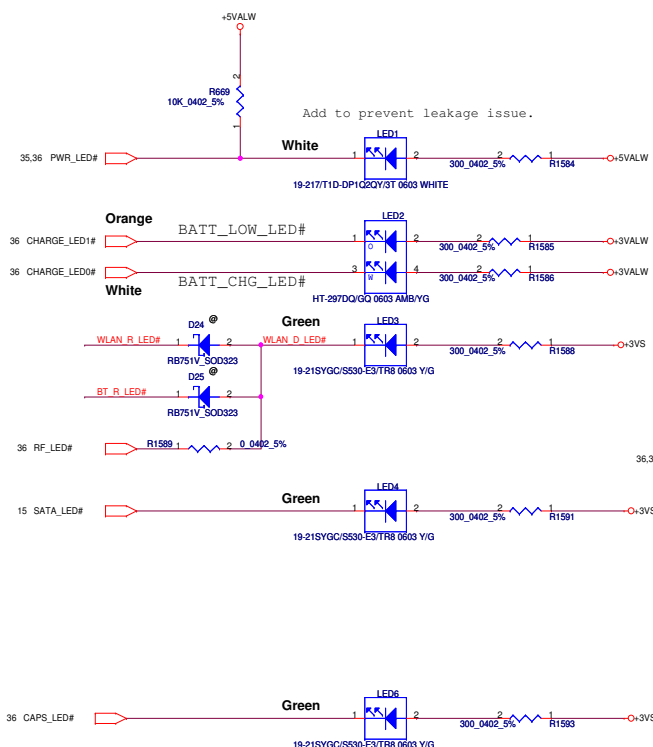
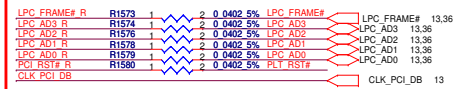
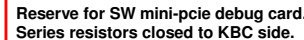


Card Reader Connector



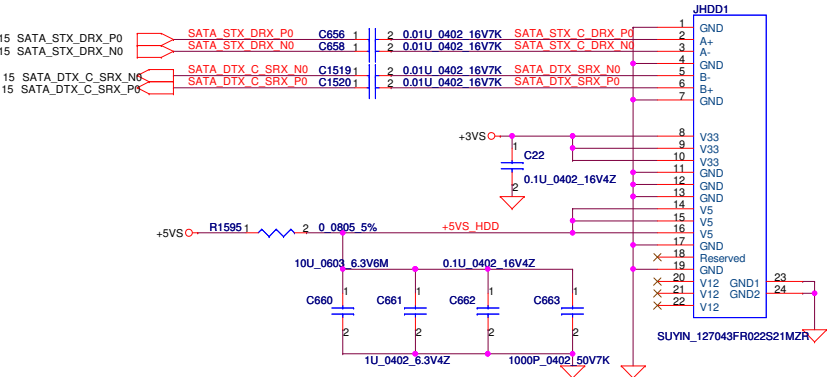
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Mini-Express Card(WLAN/WiMAX)

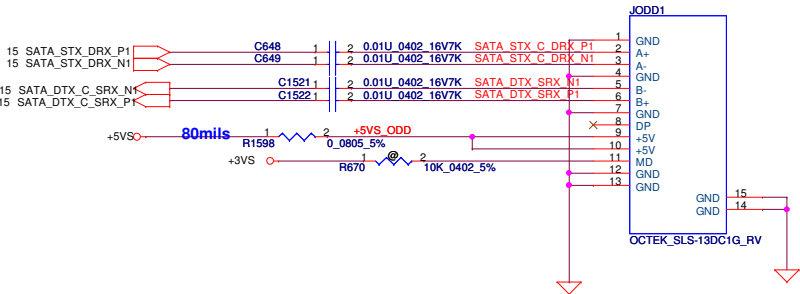


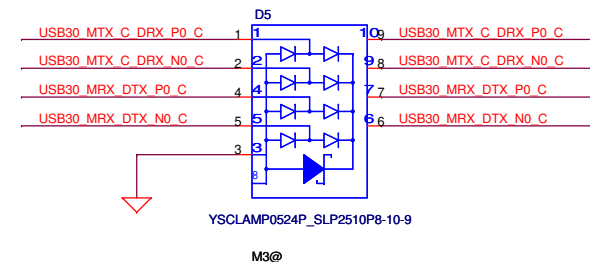
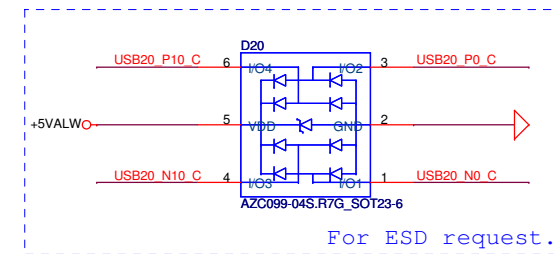
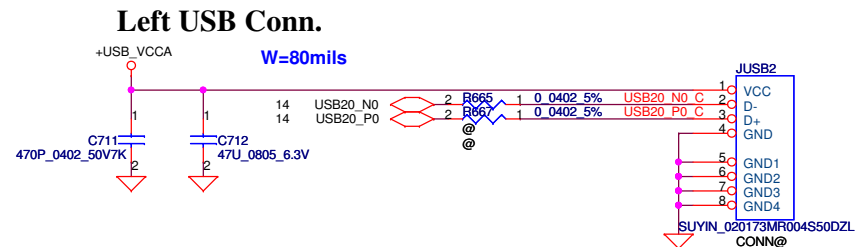
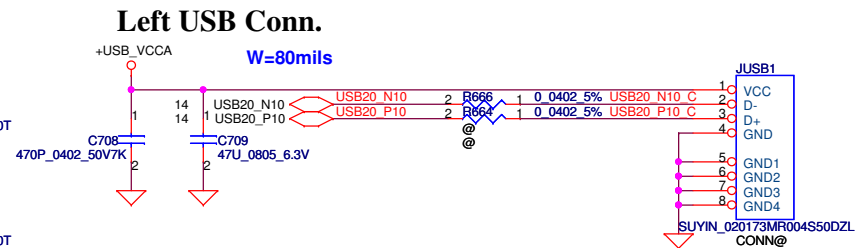
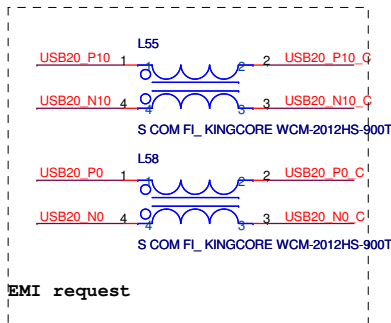
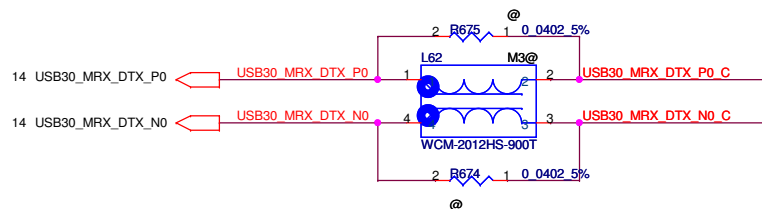
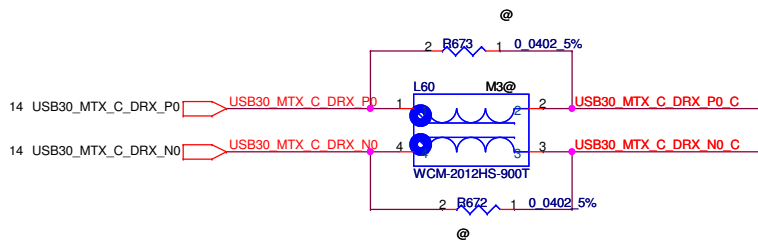
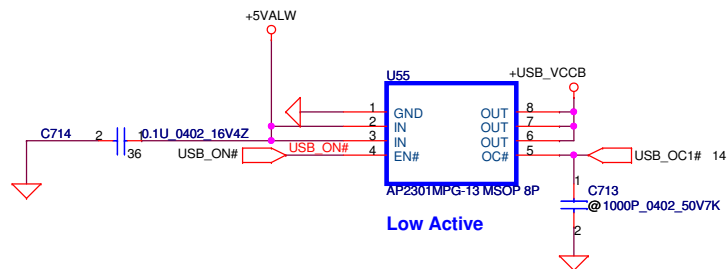
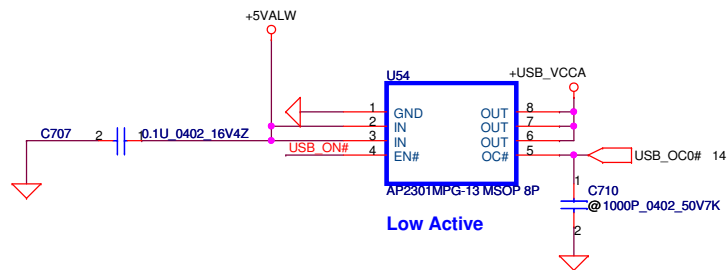
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					P28-M10 PCIE/LED
					QBL60 LA-7552P
				Date:	Tuesday, February 22, 2011
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SATA HDD Conn.



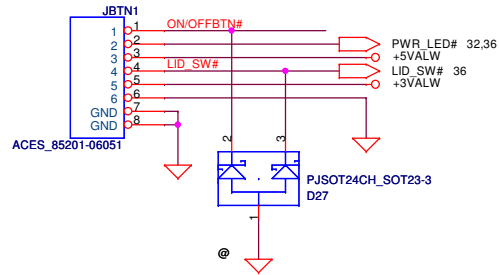
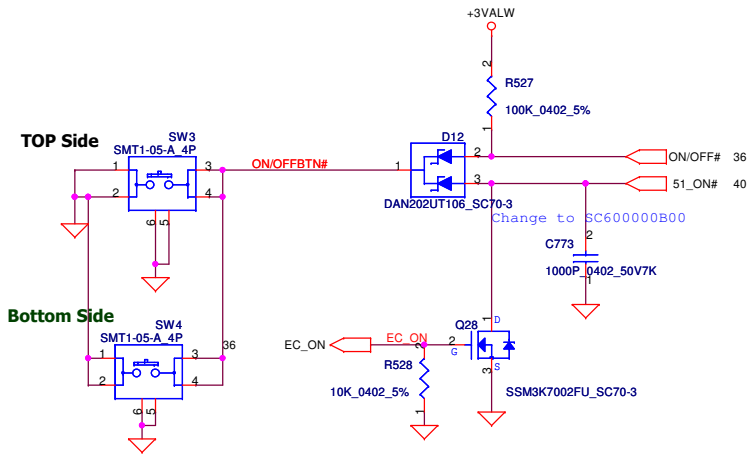
SATA ODD FFC Conn.



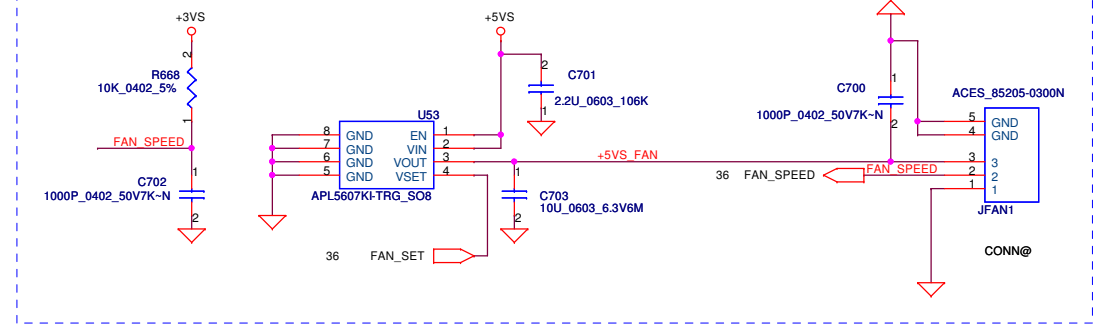


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Size		Document Number		Rev	
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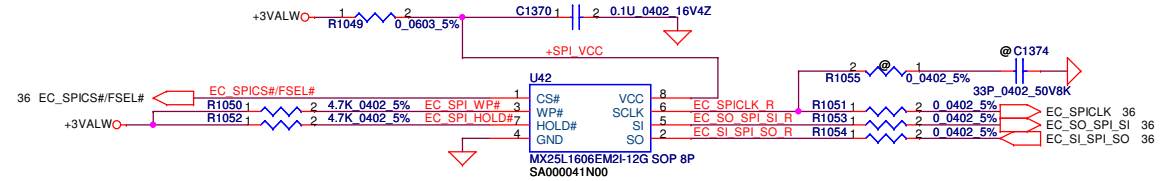
ON/OFF switch **Power Button**



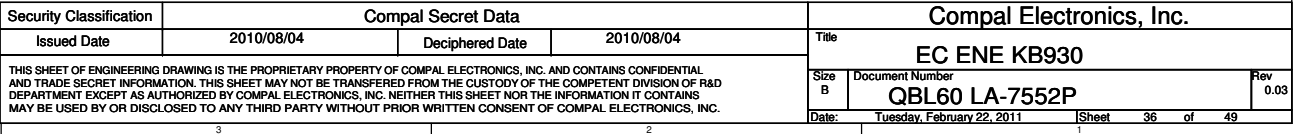
Fan Control Circuit



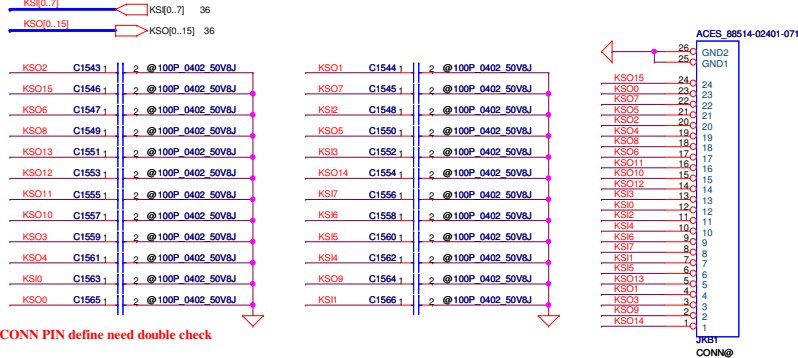
EC BIOS ROM



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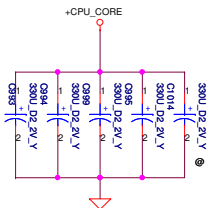


INT_KBD Conn.

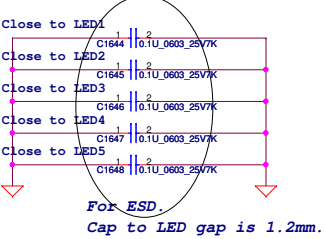
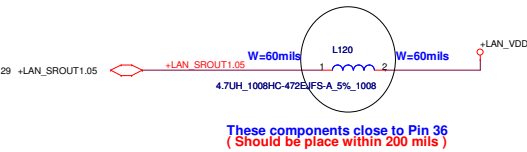
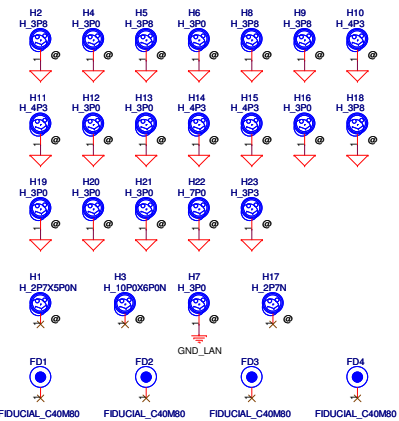
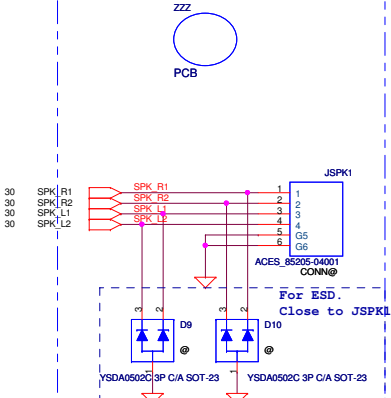
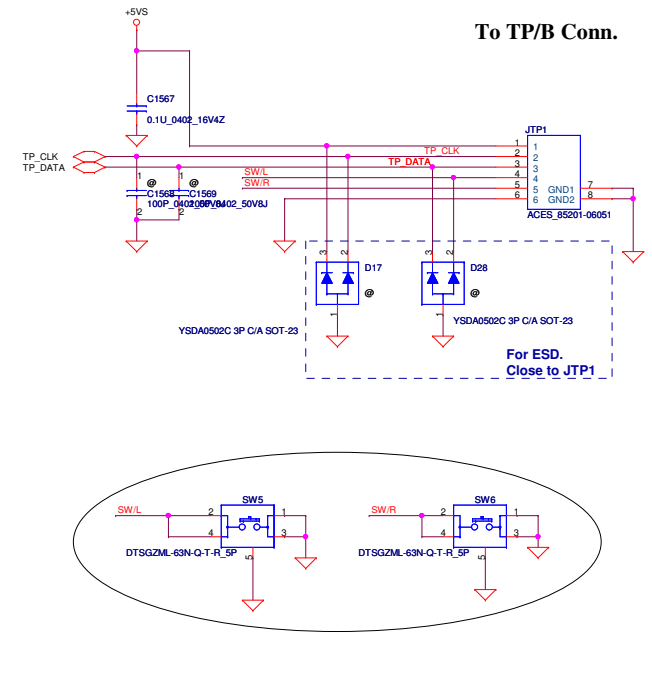


ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V

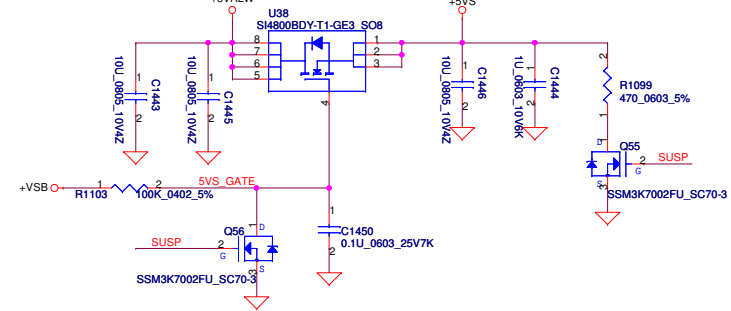
P9 FS1 PWR/GND



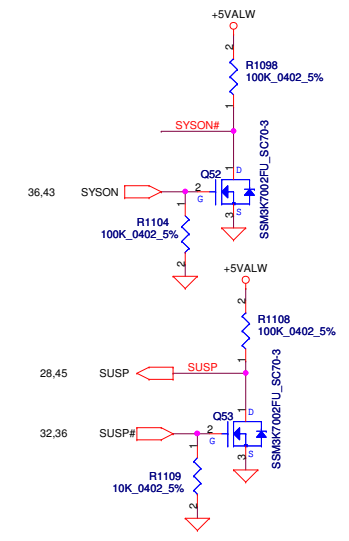
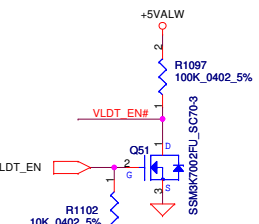
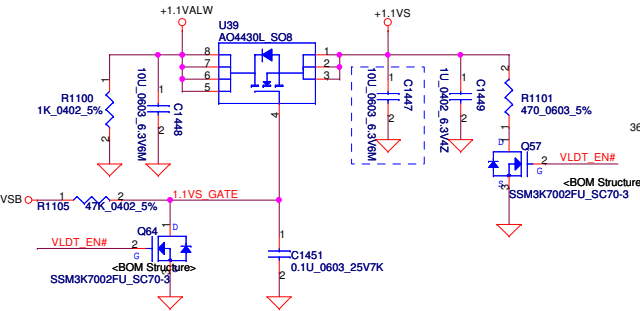
To TP/B Conn.



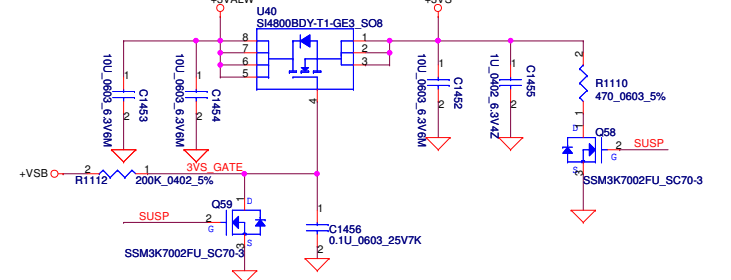
+5VALW TO +5VS (5A)



+1.1VALW TO +1.1VS (1.1A)

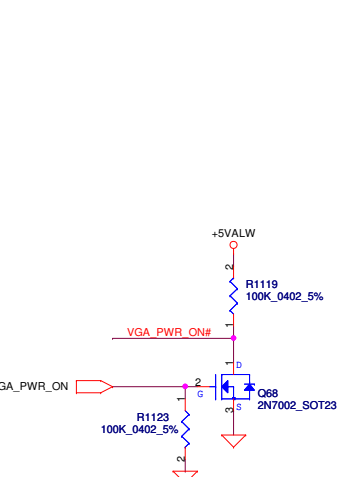
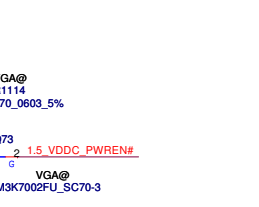
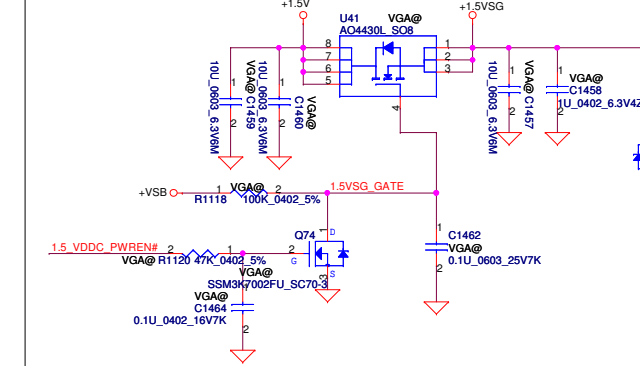


+3VALW TO +3VS (3.3A)

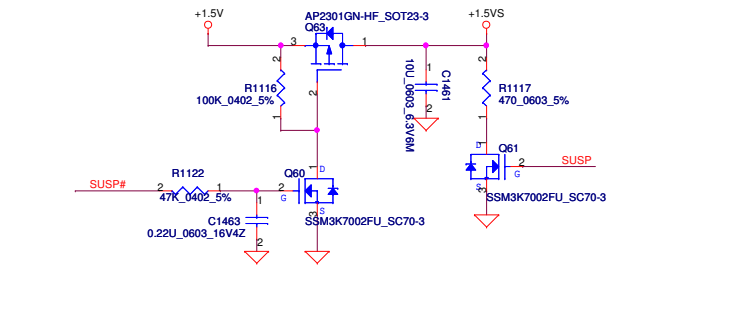


VGA Power

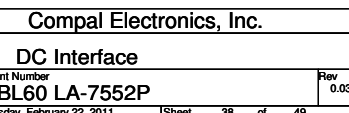
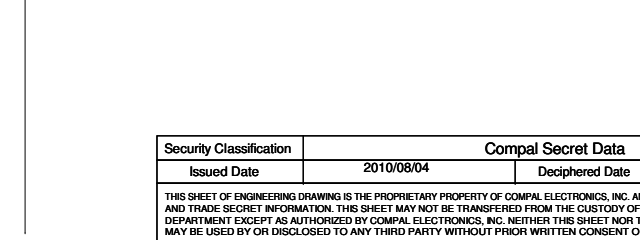
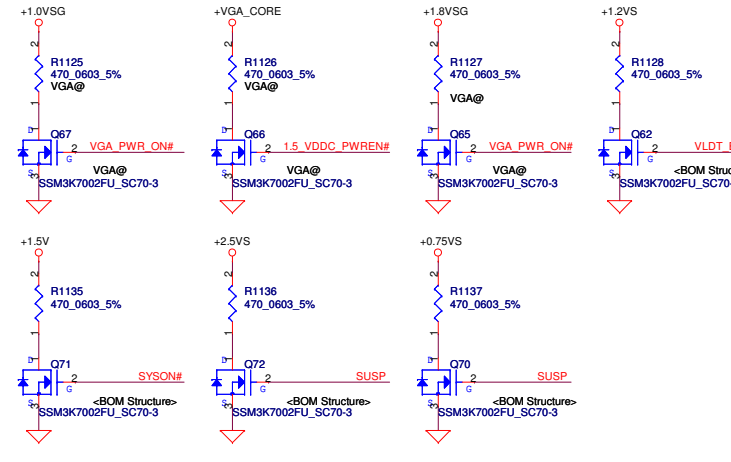
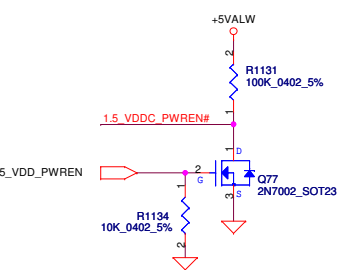
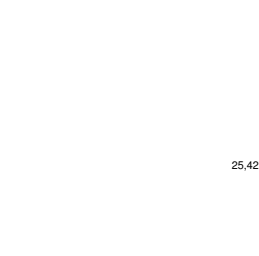
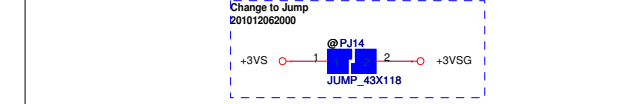
+1.5V to +1.5VSG (1.5A)



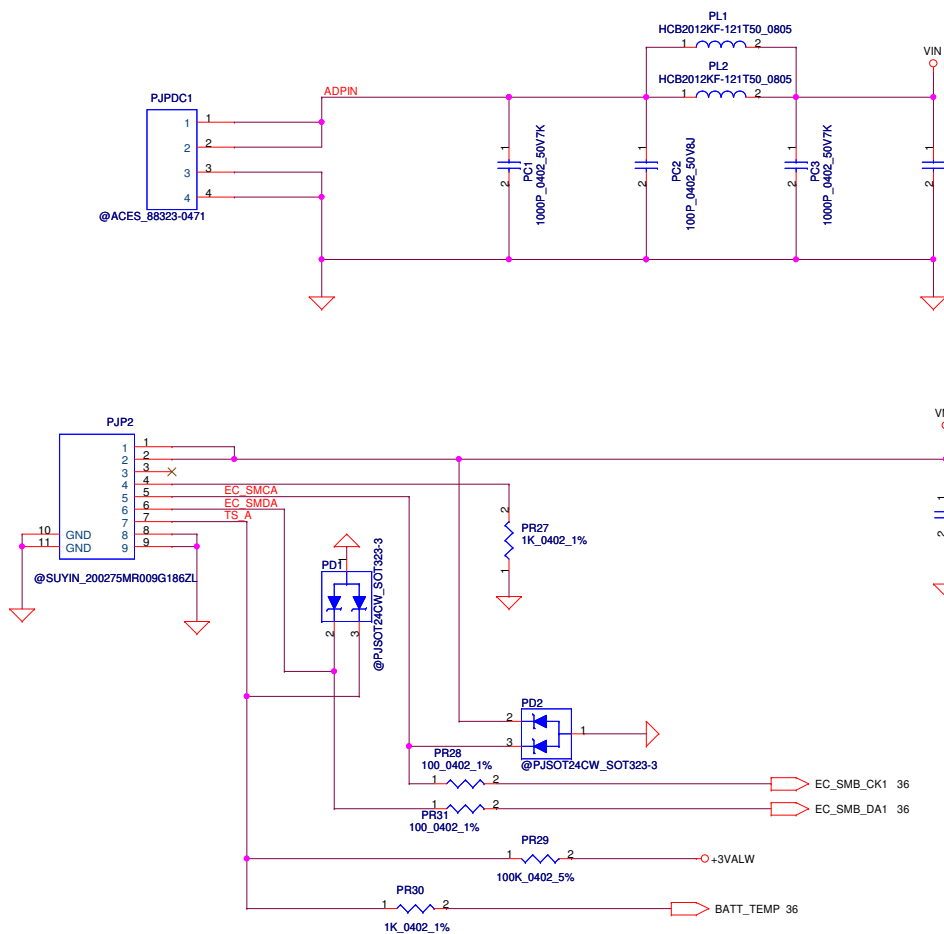
+1.5V TO +1.5VS (1.5A)



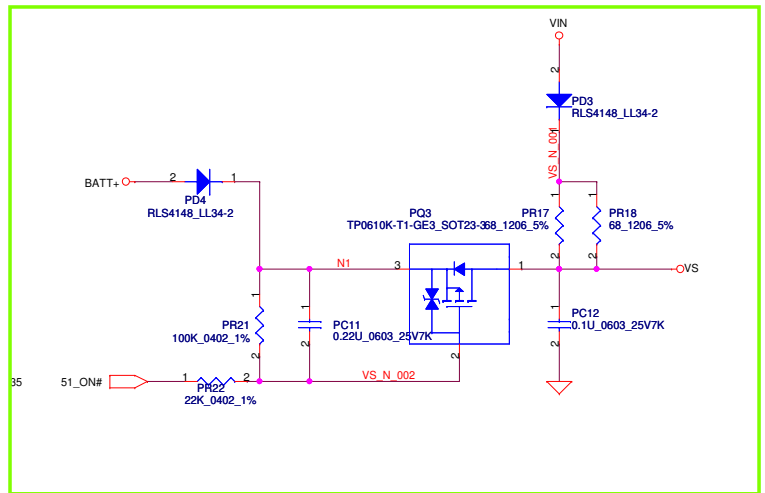
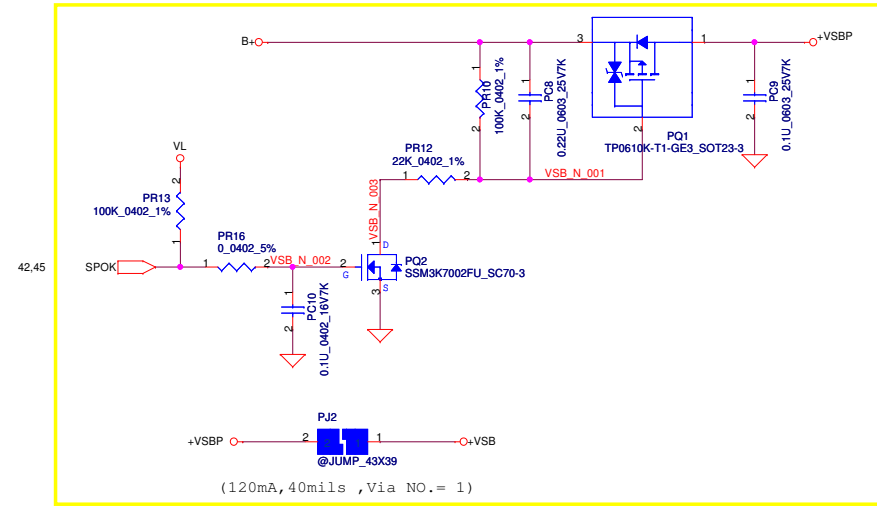
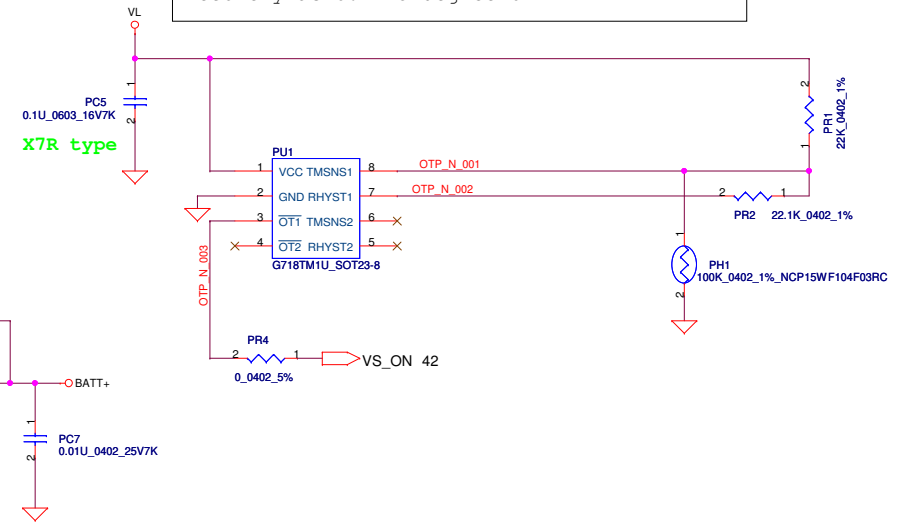
+3VS to +3VSG (3.3A)



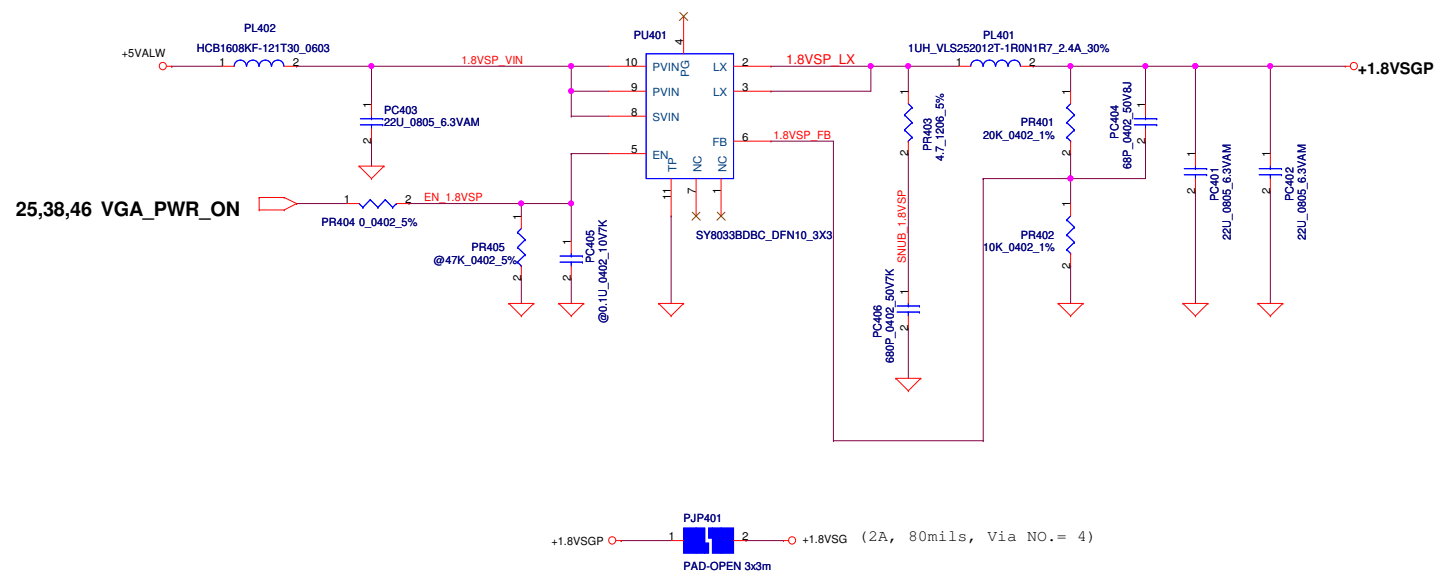
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PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C

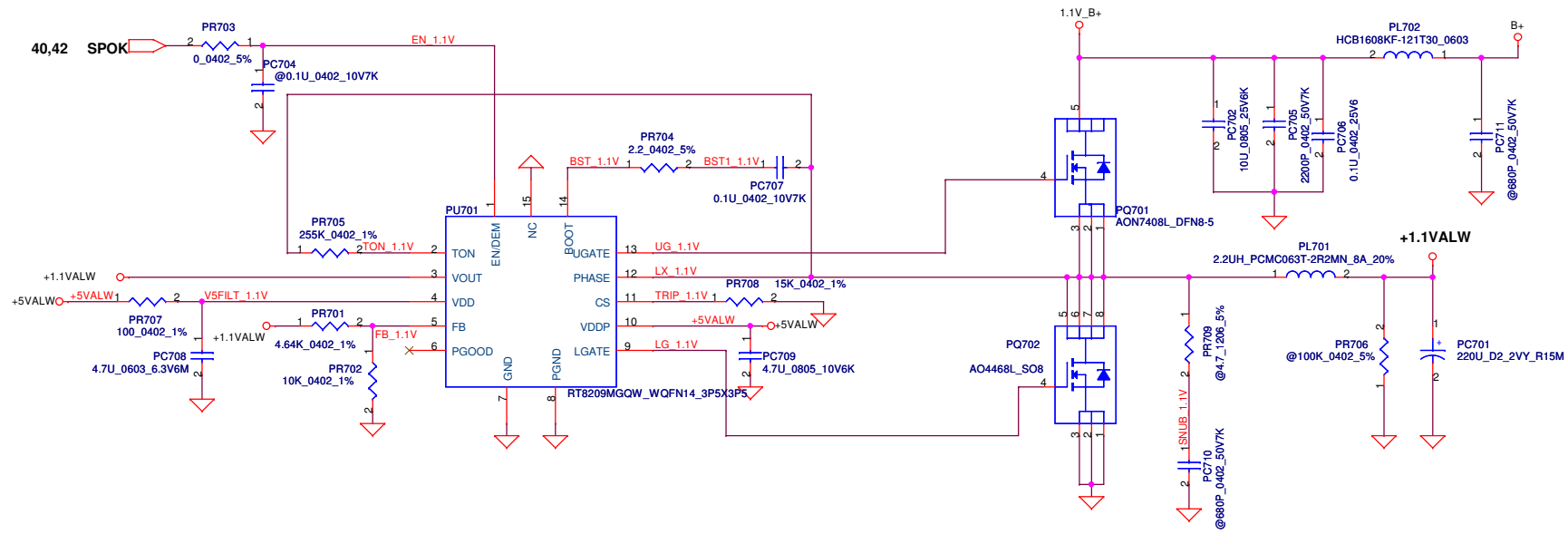


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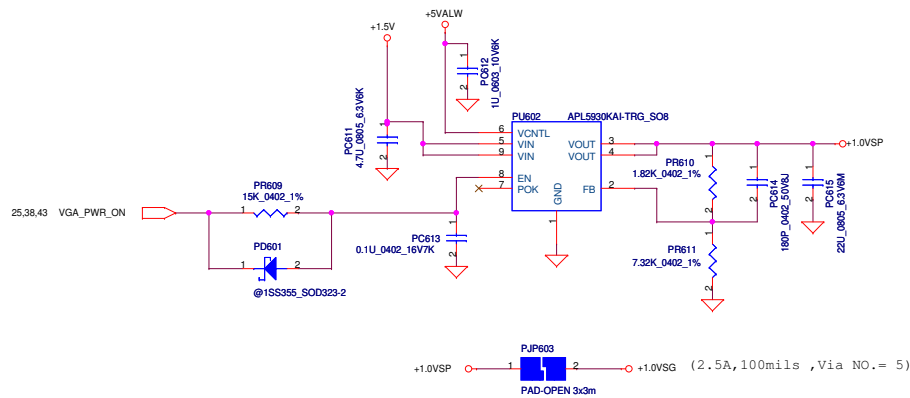
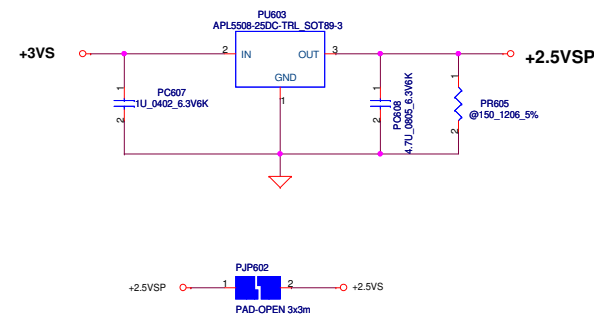
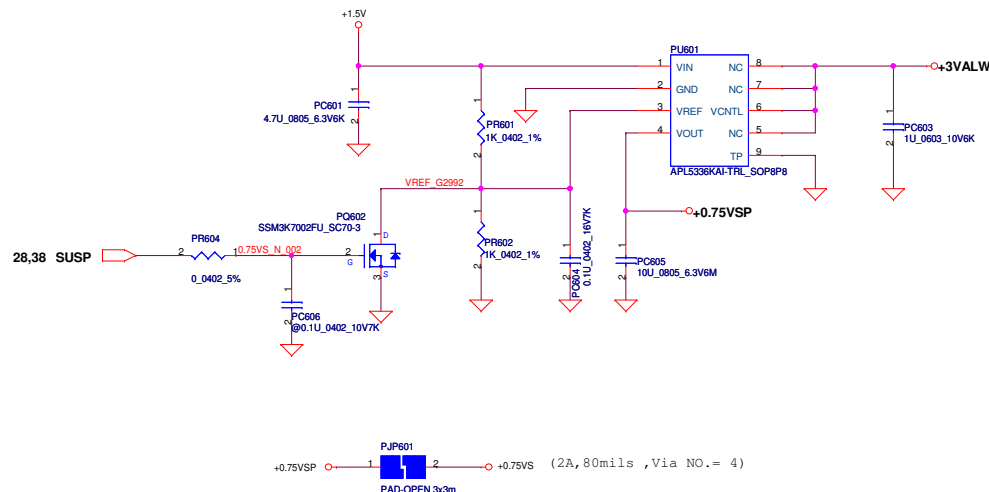


$\langle V_o = 1.8V \rangle$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401/PR402) = 0.6 * (1 + 20K/10K) = 1.8V$

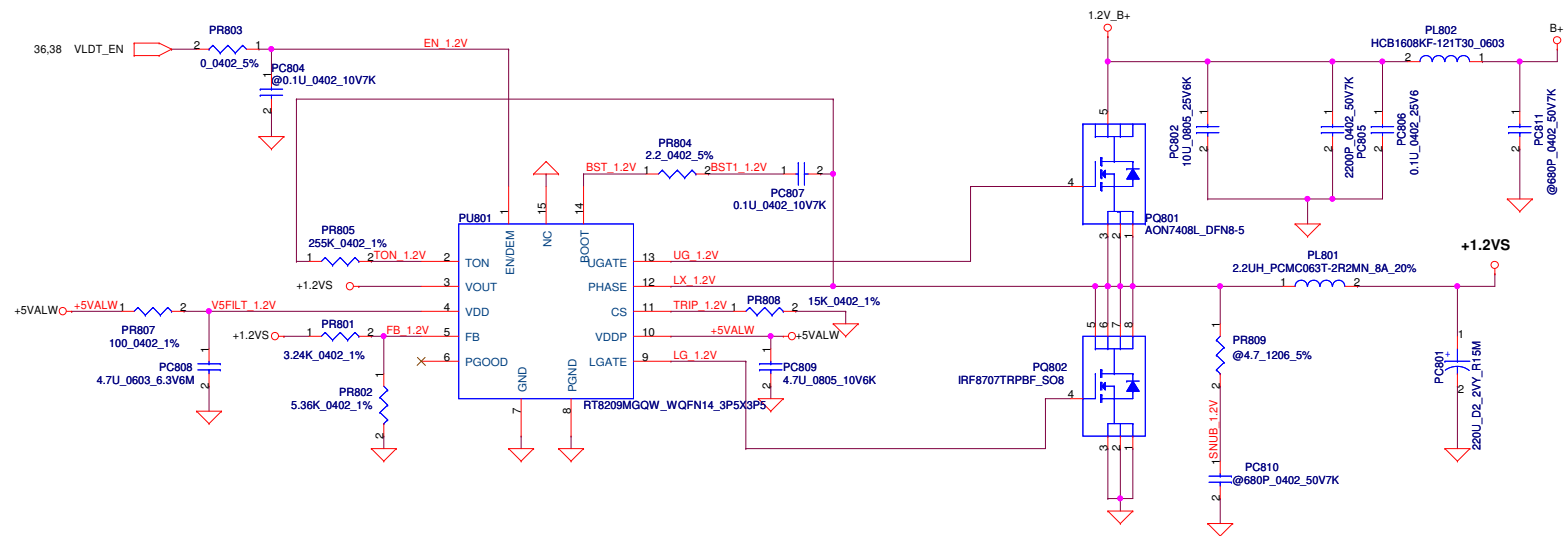
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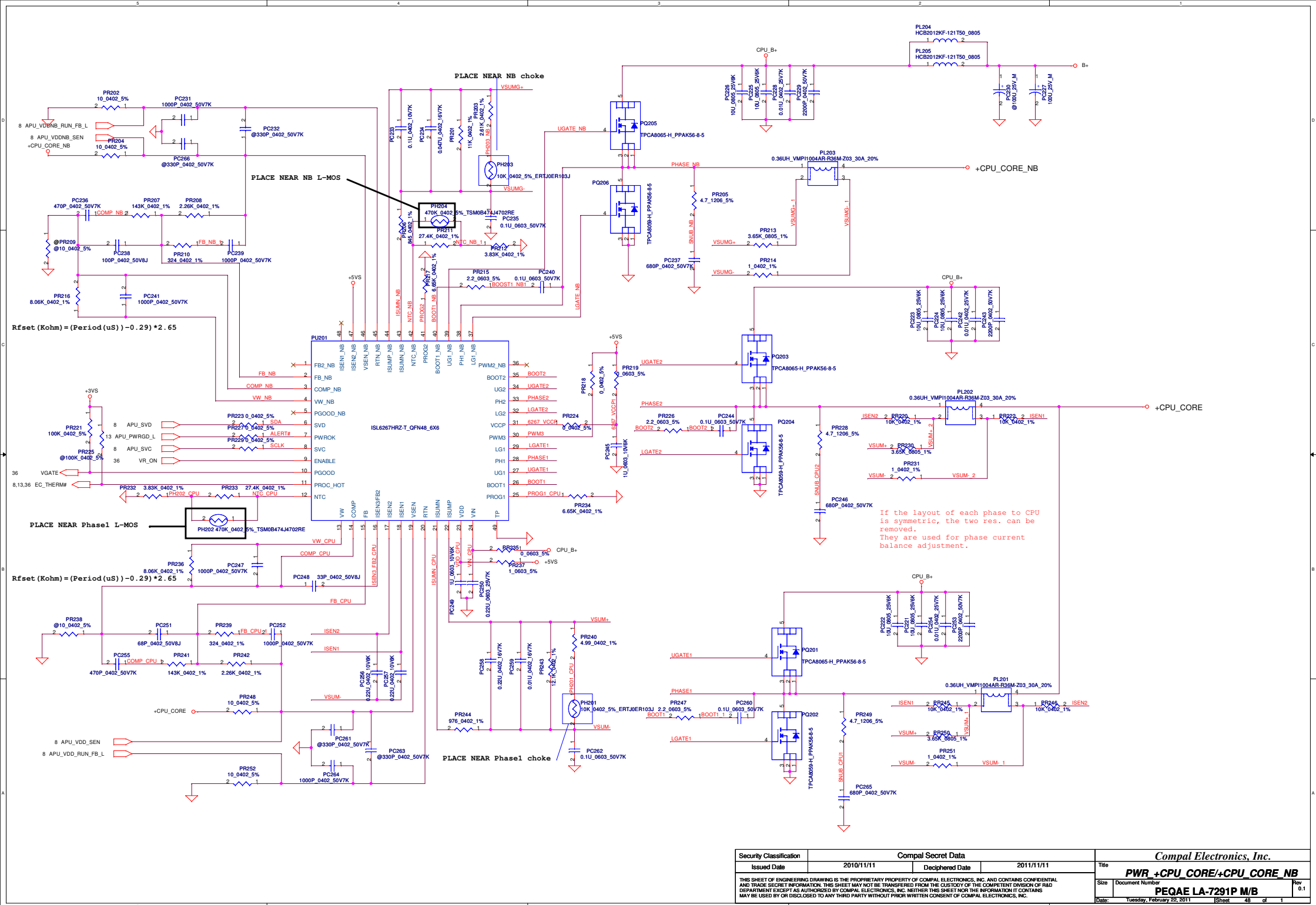
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