Aegis M/B

MS14-Additional
2010.12.10

A01 Build

DATE	CHANGE NO.	REV
Friday, December 10, 2010		

CHANGE by IEC DATE Friday, December 10, 2010

INVENTEC

TITLE Aegis

SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

SHEET 1 of 61

Schematic Page Description :

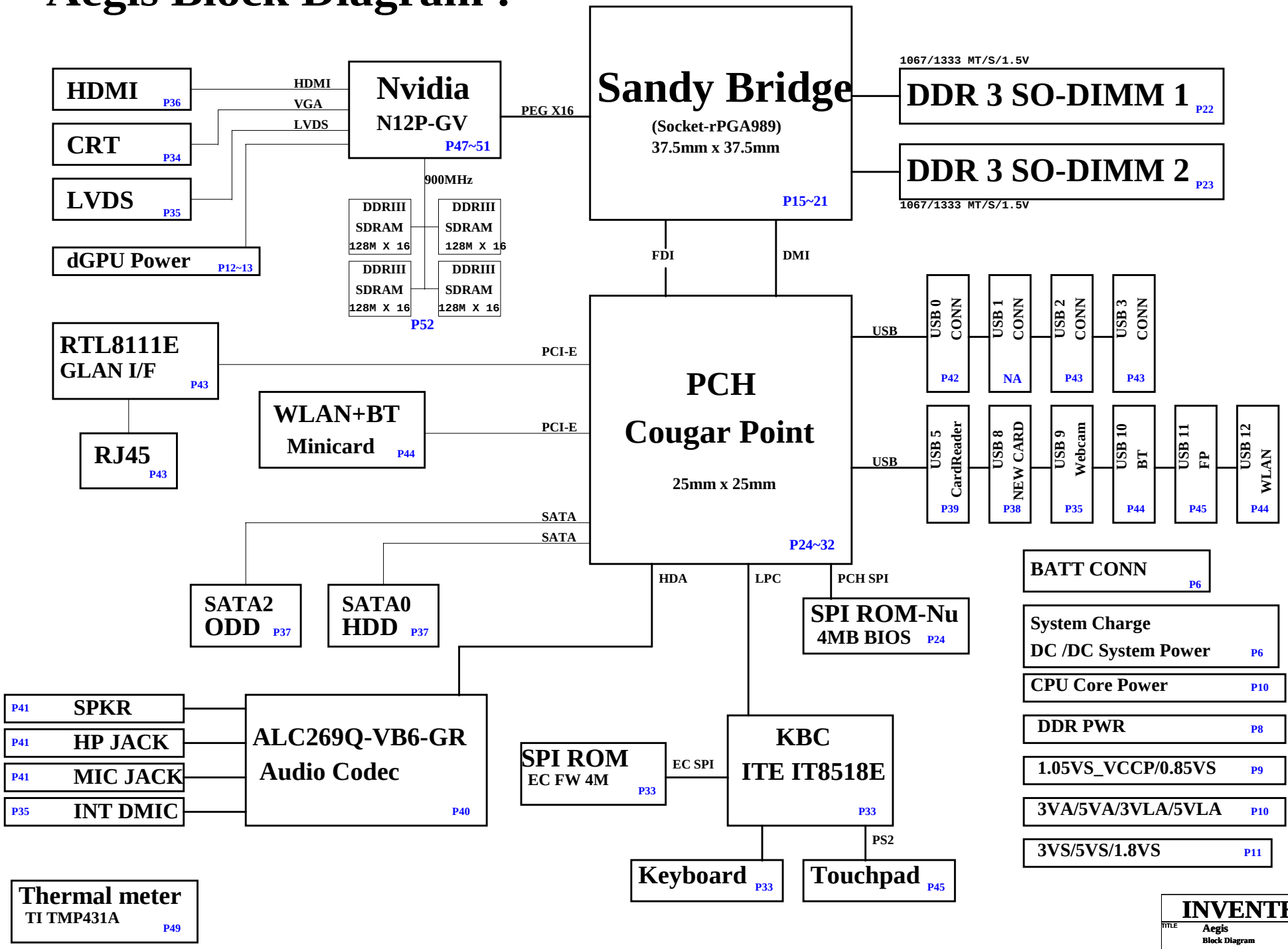
INVENTEC

TITLE Aegis
schematics page DESCR

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

CHANGE by IEC | DATE Friday, December 10, 2010 | SHEET 2 of 61

Aegis Block Diagram :



INVENTEC

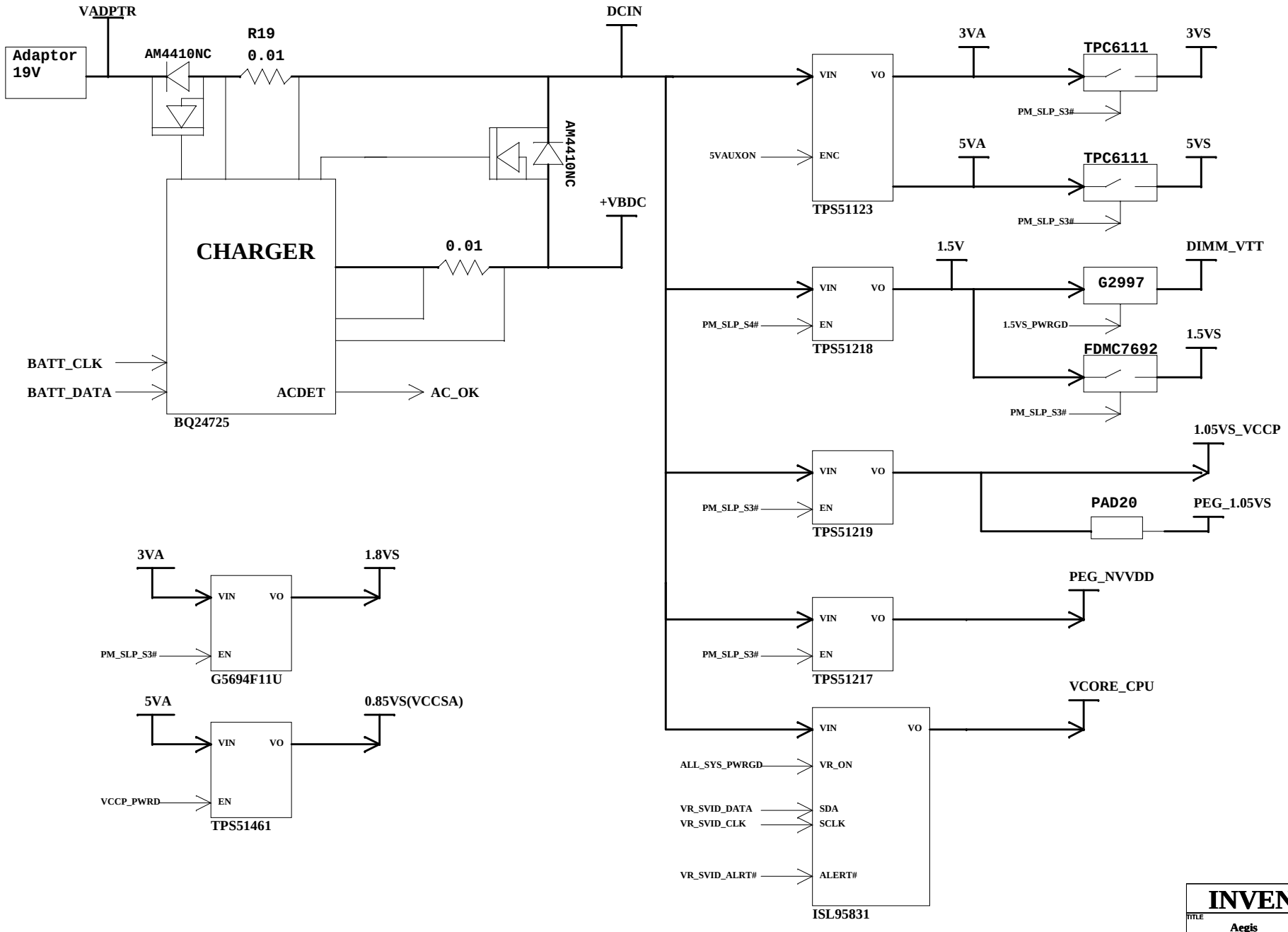
TITLE: Aegis
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

SHEET 3 of 61

CHANGE by IEC DATE Friday, December 10, 2010

Power Block Diagram :



INVENTEC

TITLE: Aegis
Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

CHANGE by IEC | DATE Friday, December 10, 2010 | SHEET 4 of 61

Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
3VLA_EC	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
5VACP	5.0V always on power rail by 5VAUXON
1.5V	1.5V switched power rail by PM_SLP_S4#
1.8V	1.8V power rail by PM_SLP_S4#
3VS	3.3V power rail by PM_SLP_S3#
5VS	5.0V power rail by PM_SLP_S3#
1.5VS	1.5V power rail by PM_SLP_S3#
1.05VS_VCCP	1.05V power rail by PM_SLP_S3#
DIMM_VTT	0.75V DDR Termination Voltage by 1.5VS_PWRGD
PEG_1.5VS	1.5V switched power rail for N12P-GV by PM_SLP_S3#
PEG_1.05VS	1.05V switched power rail for N12P-GV by PM_SLP_S3#
PEG_NVVDD	Variable switched power rail for N12P-GV by PM_SLP_S3#
VCORE_CPU	Core switched power rail for CPU by ALL_SYS_PWRGD
1.8VS	1.8V power rail by PM_SLP_S3#

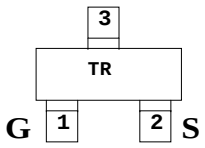
Part Naming Conventions

C	=	Capacitor	Q	=	Transistor
CN	=	Connector	R	=	Resistor
D	=	Diode	RP	=	Resistor Pack
F	=	Fuse	U	=	Arbitrary Logic Device
L	=	Inductor	Y	=	Crystal and Osc

Name Suffix

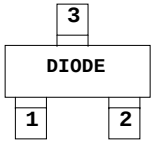
#	=	Active Low signal
NU	=	No Stuff

D



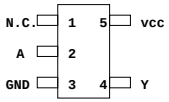
SOT-24

BAT54/BAT54A
BAT54C/BAT54S



SOT-23

NXP_74LVC1G07GW



TSSOP_5P

Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Mother Board ID setting by PCH

FJ Mother Board ID setting by PCH

Project	MB_ID2	MB_ID1	MB_ID0
	0	0	0
Aegis (Discrete)	0	0	1
Neurron (UMA)	0	1	0
Neuron-V (Optimus)	0	1	1
Strike (UMA)	1	0	0
Strike-V (Optimus)	1	0	1
Silk (UMA)	1	1	0
Silk-V (Optimus)	1	1	1
PCH ---------->	GPIO41	GPIO40	GPIO59

Mother Board ID setting by EC

FJ Mother Board ID setting by EC

Project	EC_ID0
Aegis (Discrete)	1
Neurron (UMA)	0
Neuron-V (Optimus)	1
Strike (UMA)	0
Strike-V (Optimus)	1
Silk (UMA)	0
Silk-V (Optimus)	1
EC ---------->	GPC0 (pin 119)

Please pull up 10k for "1". Pull down 10k for "0"

INVENTEC

TITLE: Aegis Annotations

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

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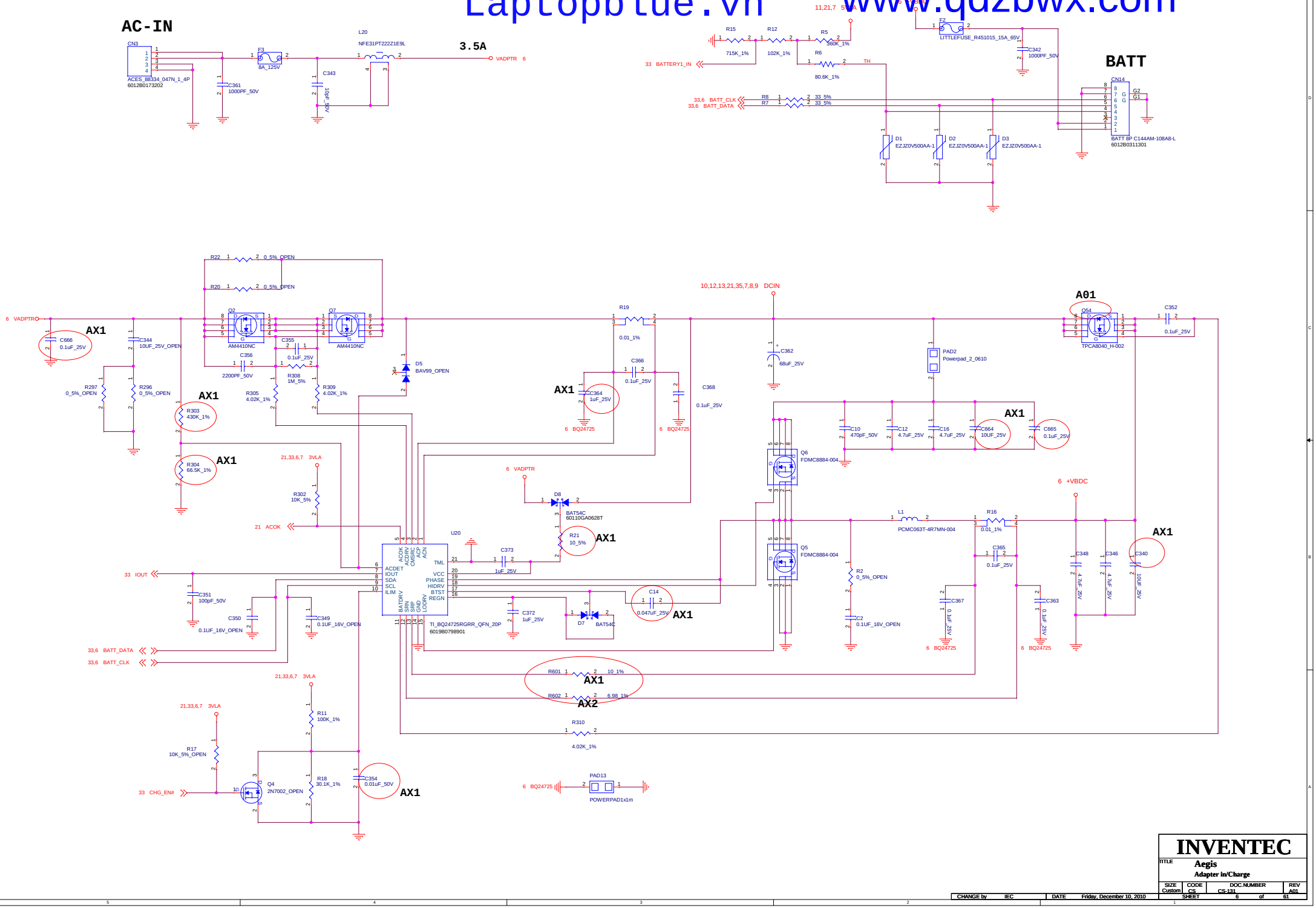
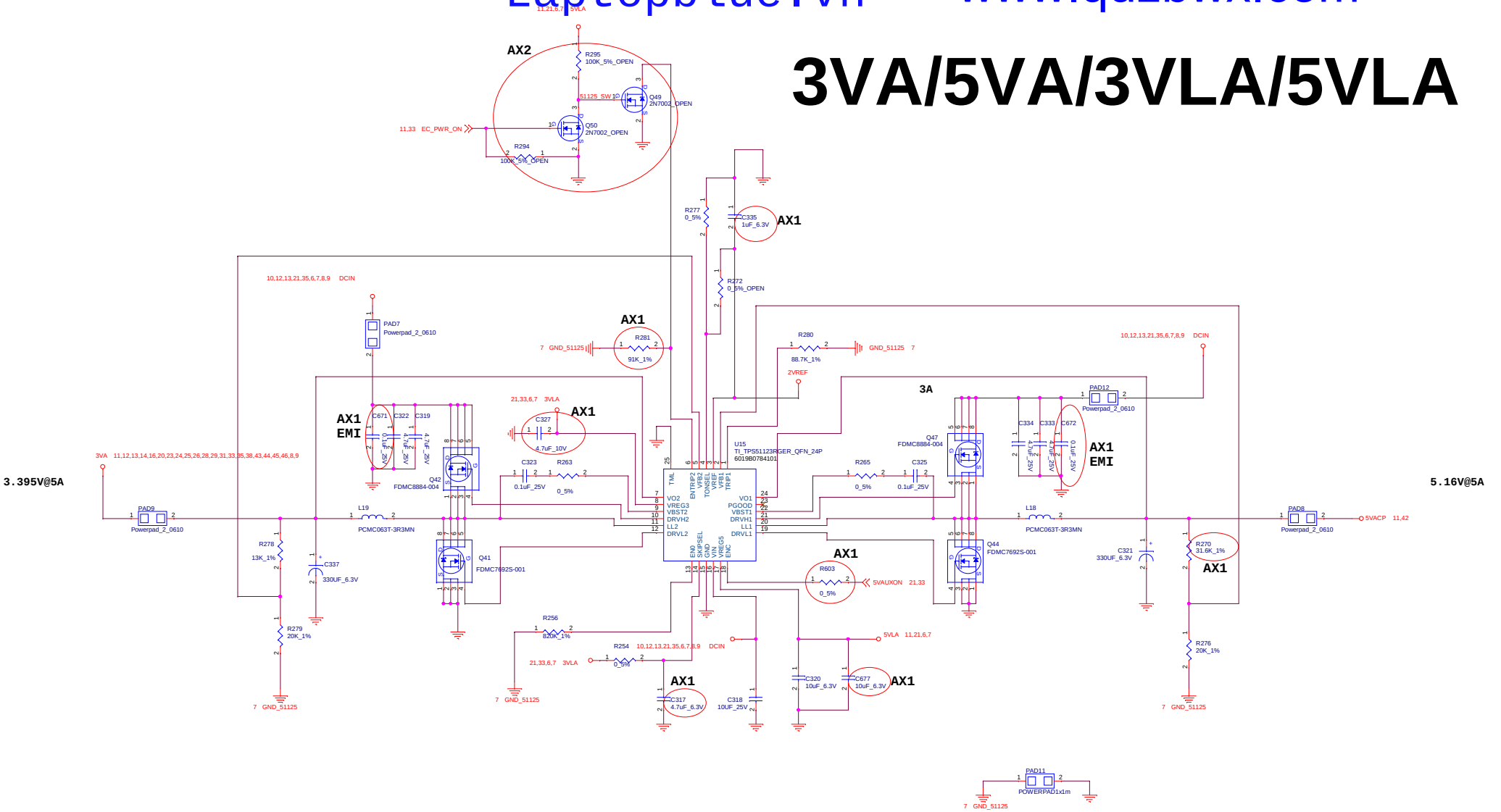


CHANGE by	IEC	DATE	Friday, December 10, 2010

INVENTEC

TITLE	Aegis Adapter in/Charge		
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	A01
SHEET	6	of	61

3VA/5VA/3VLA/5VLA



CHANGE by	IEC	DATE	Friday, December 10, 2010

INVENTEC

TITLE: Aegis
3VA/5VA/3VLA/5VLA

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	A01

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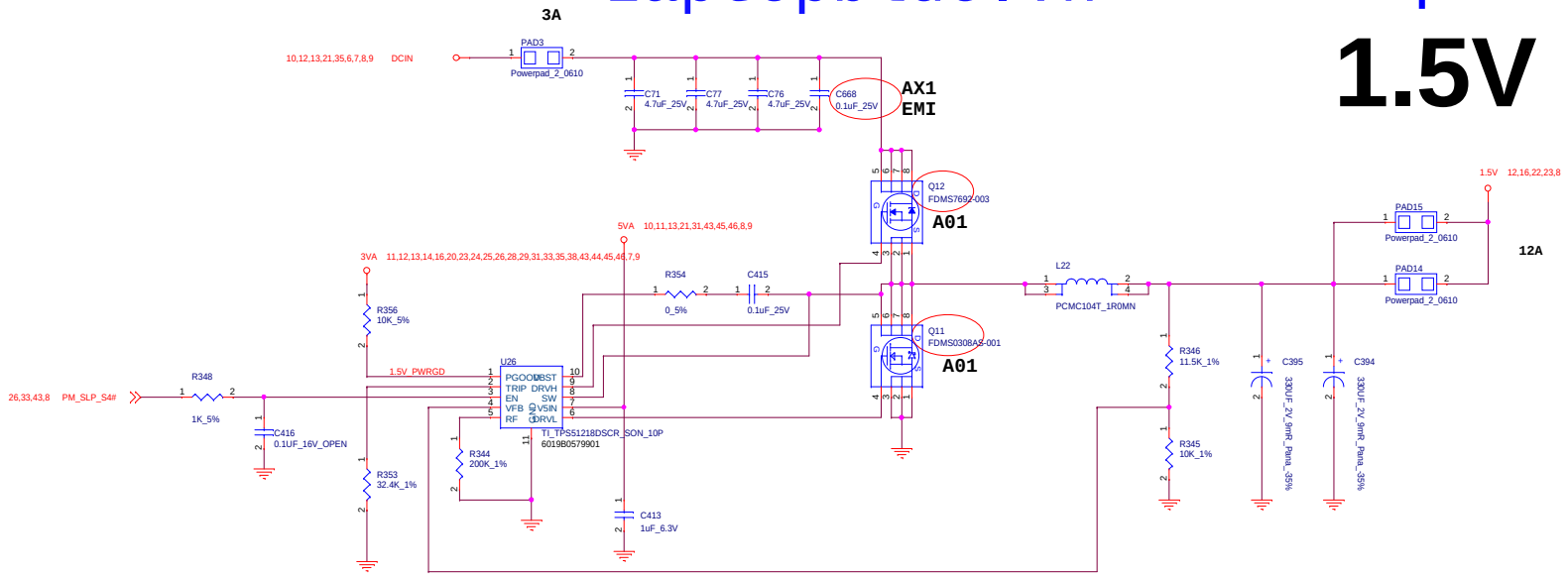
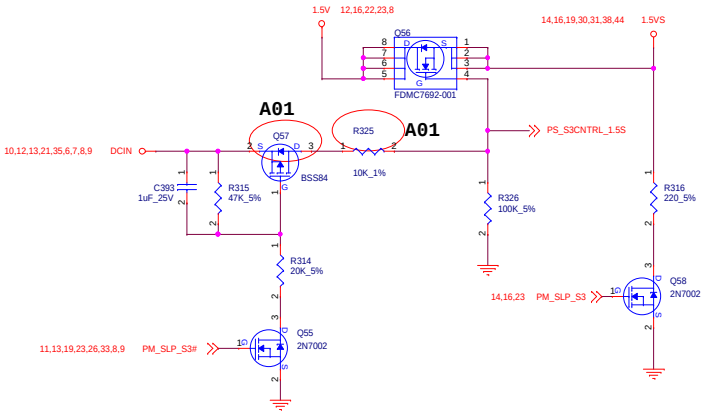
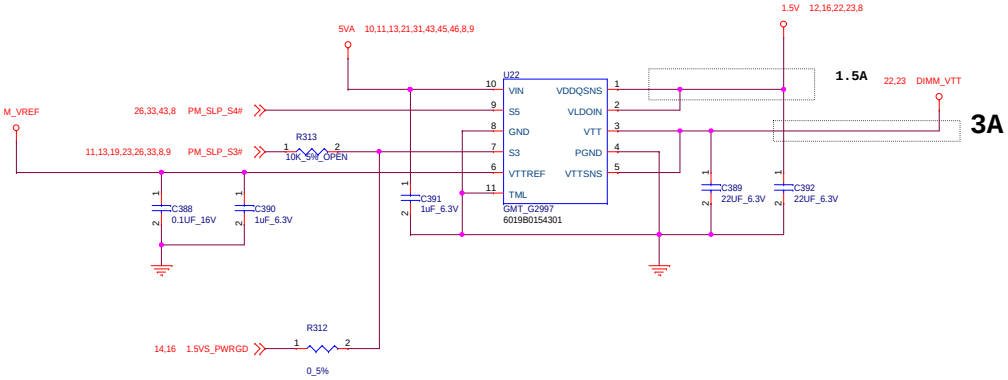
1.5V



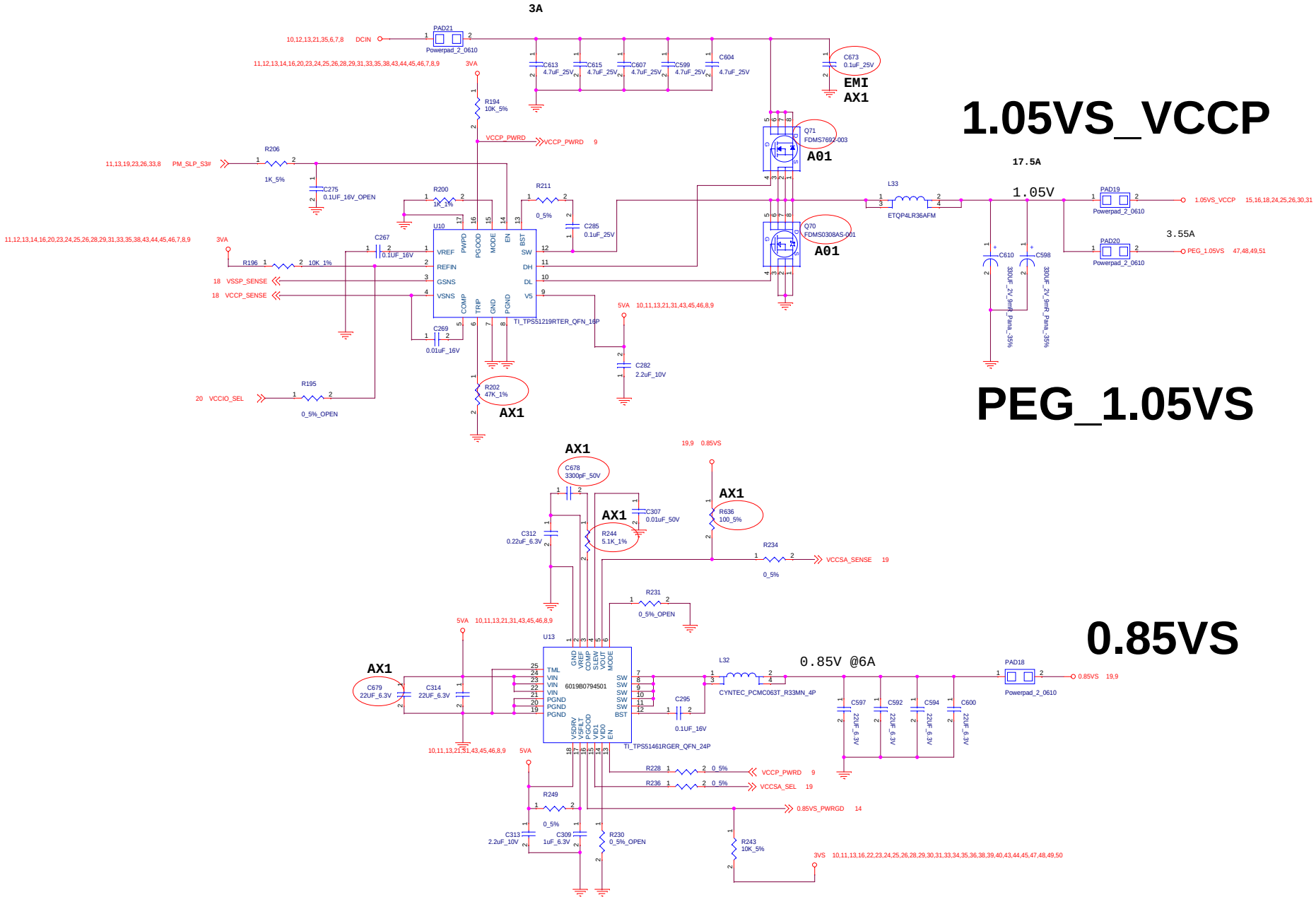
1.5VS



0.75V

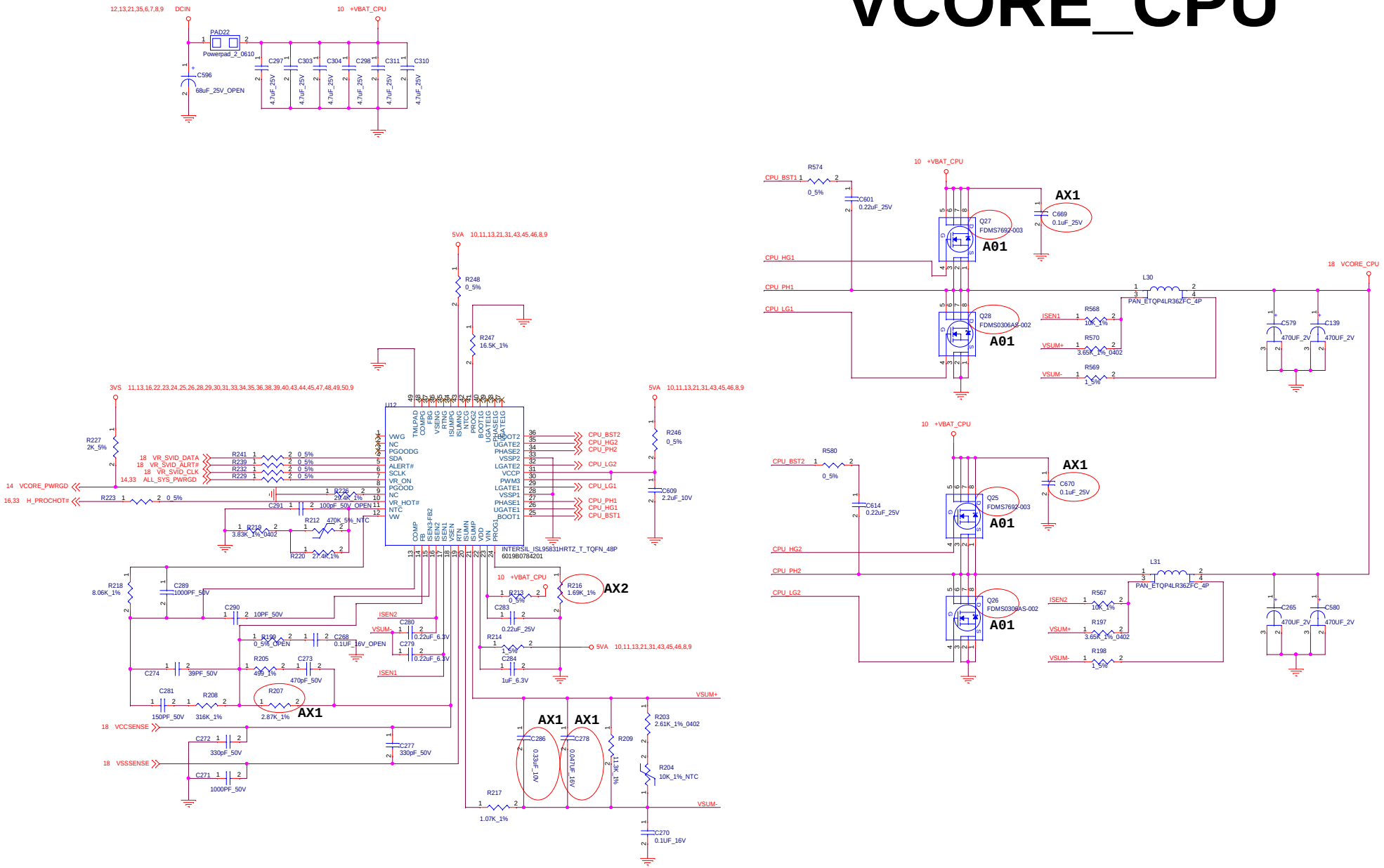


INVENTEC			
TITLE: Aegis 1.5V / 0.75V / 1.5VS			
SIZE: C	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 8 of 61	

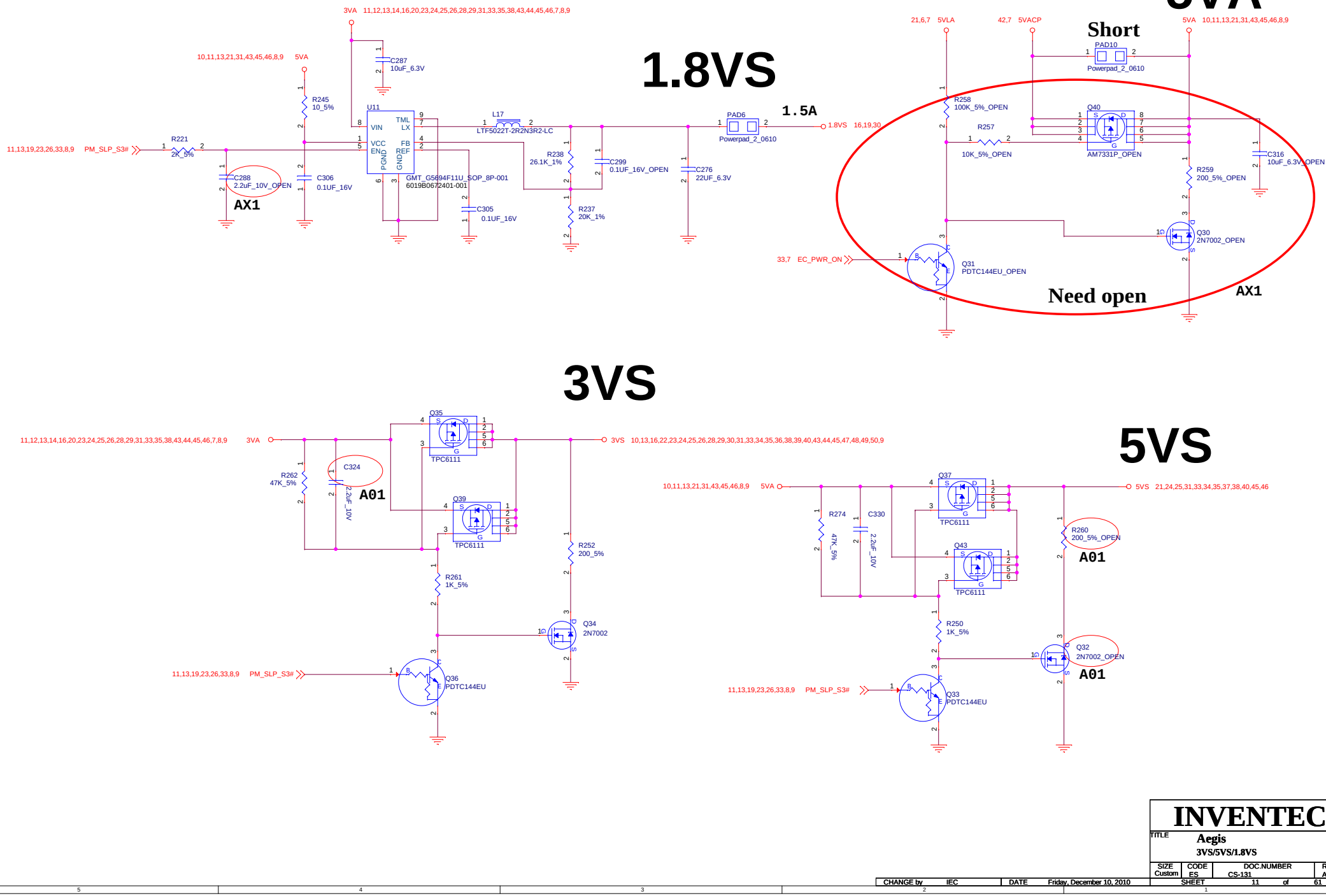


INVENTEC			
TITLE	Aegis		
	0.85VS/1.05VS_VCCP		
SIZE C	CODE ES	DOC.NUMBER CS-131	REV A01
CHANGE by IEC	DATE Friday, December 10, 2010	SHEET 9 of 61	

VCORE_CPU

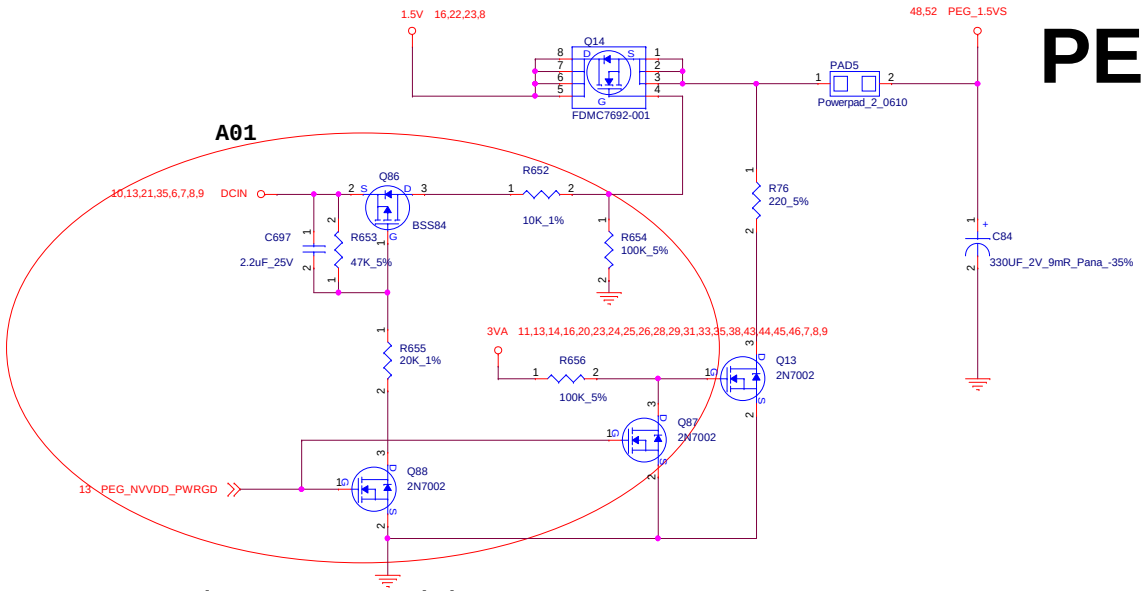


INVENTEC			
TITLE: Aegis PWR_CPU Core Power			
SIZE: C	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 10 of 61	



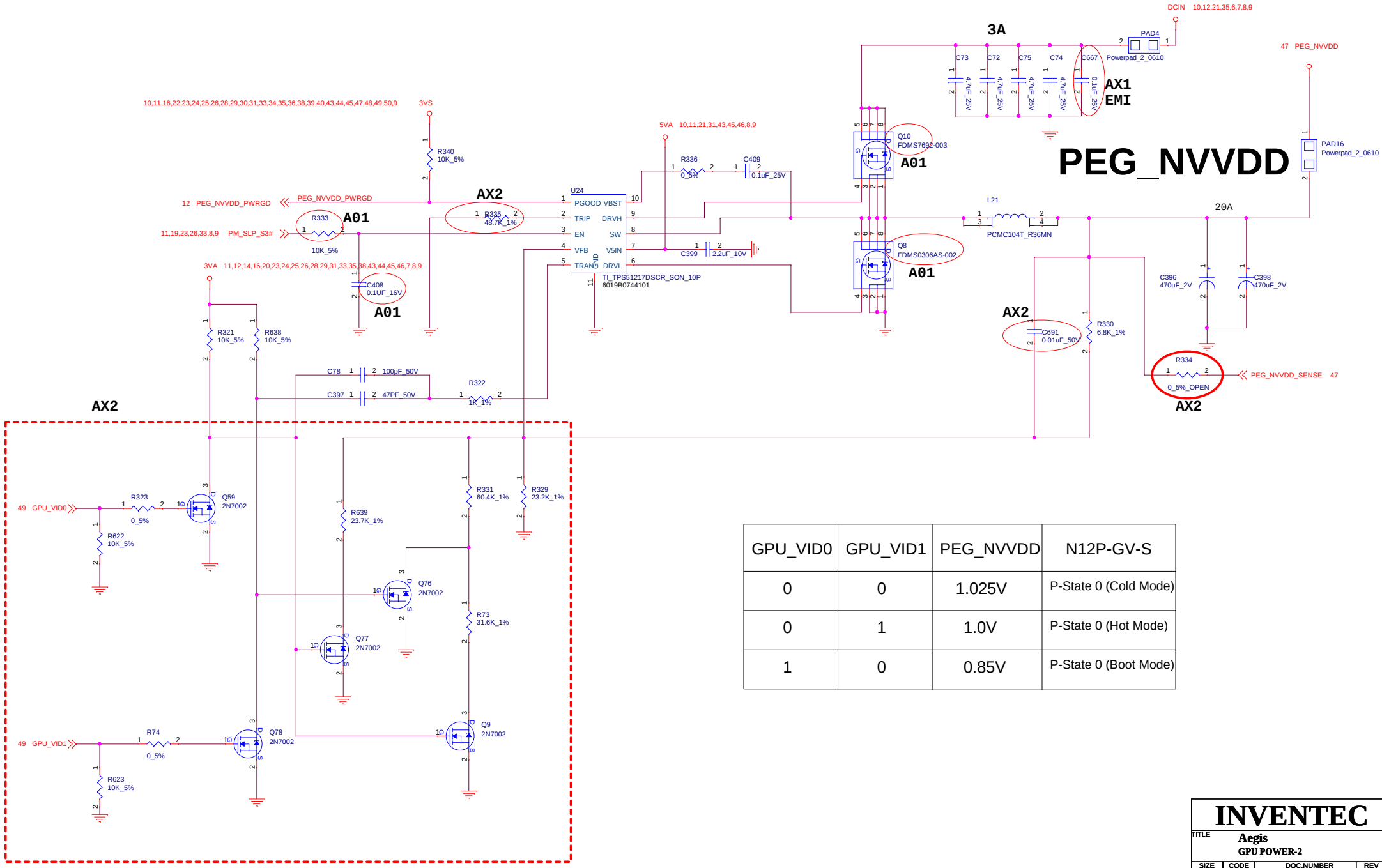
INVENTEC			
TITLE: Aegis 3VS/5VS/1.8VS			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 11 of 61	

PEG_1.5VS



For dGPU PEG_1.5VS timing

INVENTEC					
TITLE: Aegis GPU Power-1					
SIZE: Custom	CODE IDENT: ES	DOC.NUMBER: CS-131		REV: A01	
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 12 of 61			



GPU_VID0	GPU_VID1	PEG_NVVDD	N12P-GV-S
0	0	1.025V	P-State 0 (Cold Mode)
0	1	1.0V	P-State 0 (Hot Mode)
1	0	0.85V	P-State 0 (Boot Mode)

INVENTEC

TITLE: Aegis
GPU POWER-2

SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

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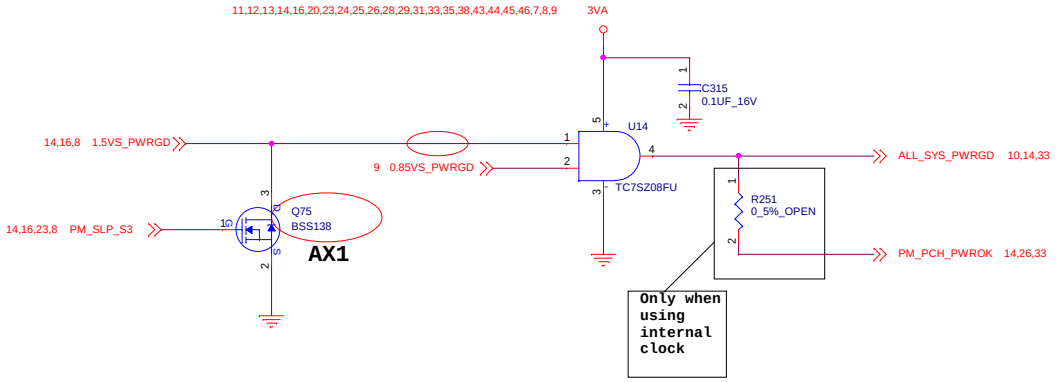
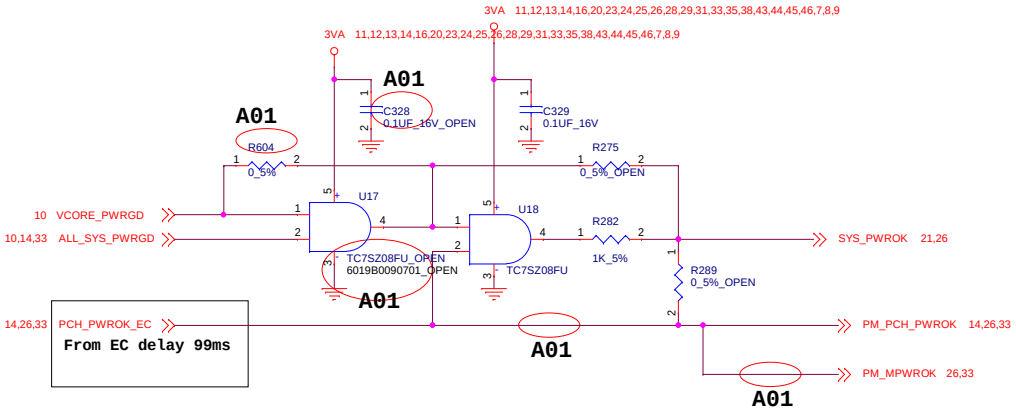
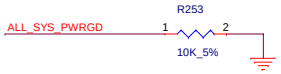
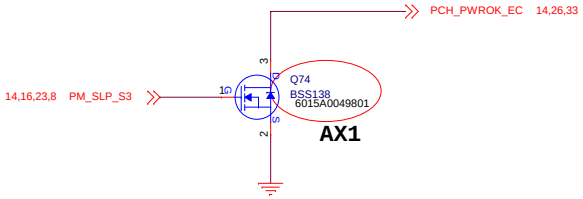
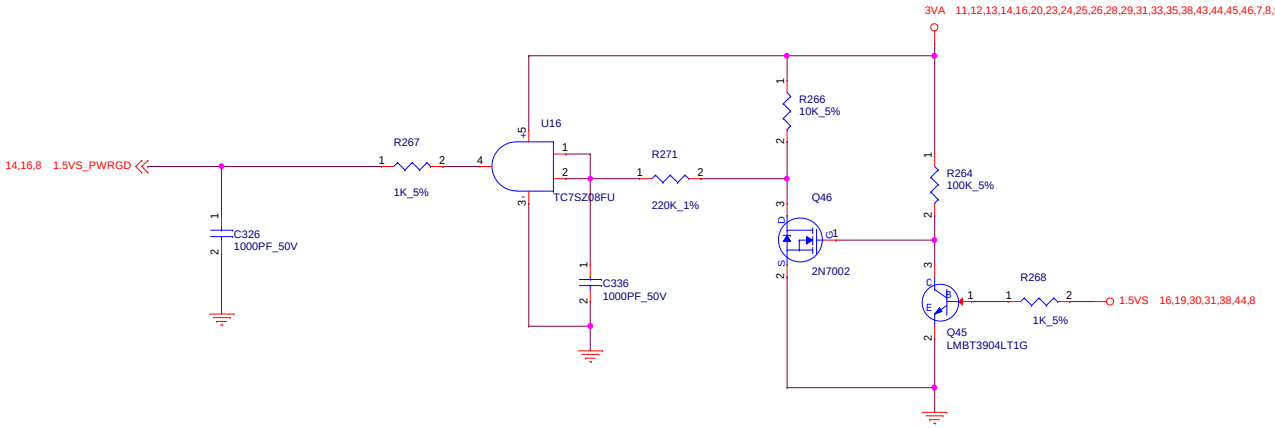
Main S0 PWROK Logic



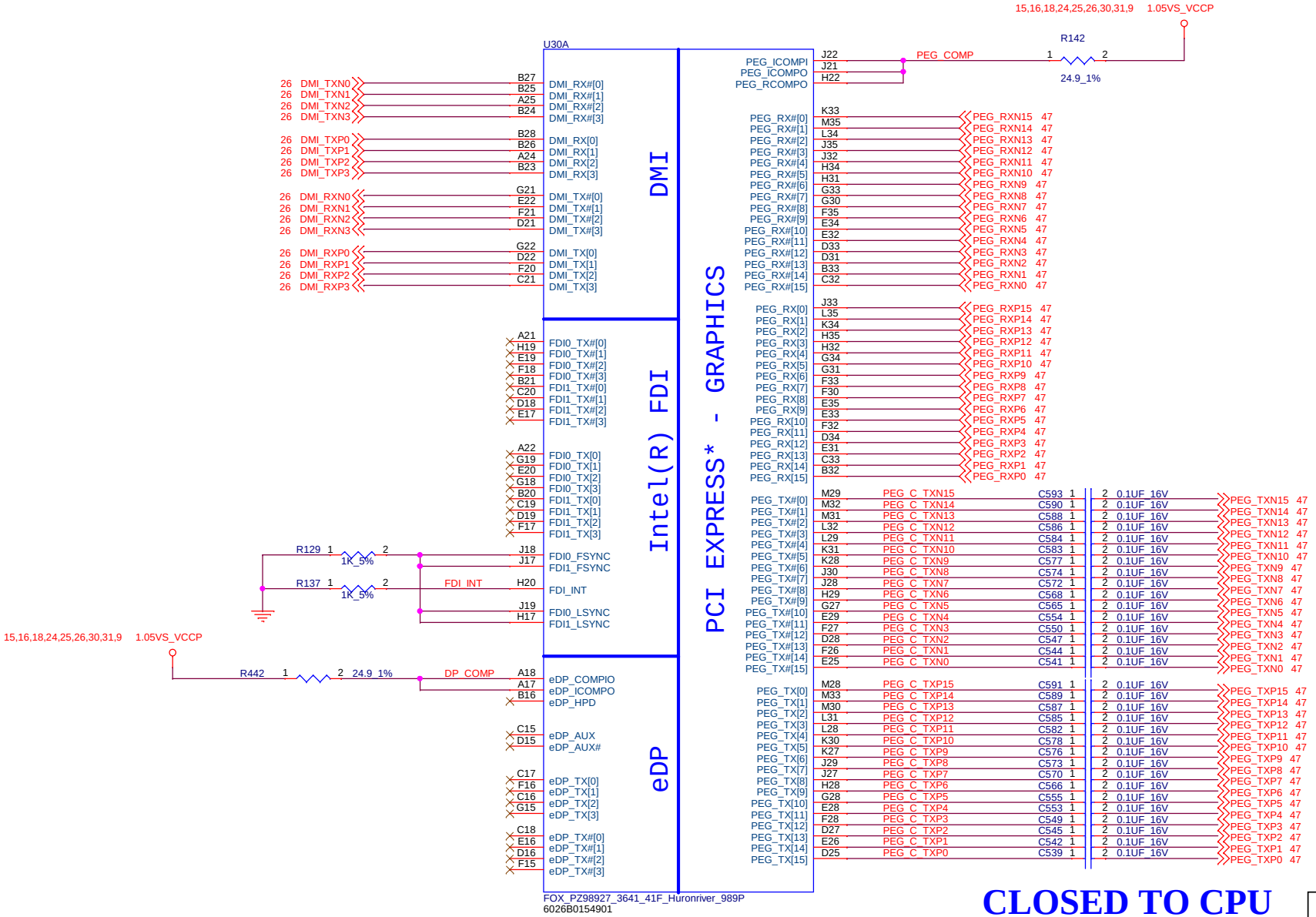








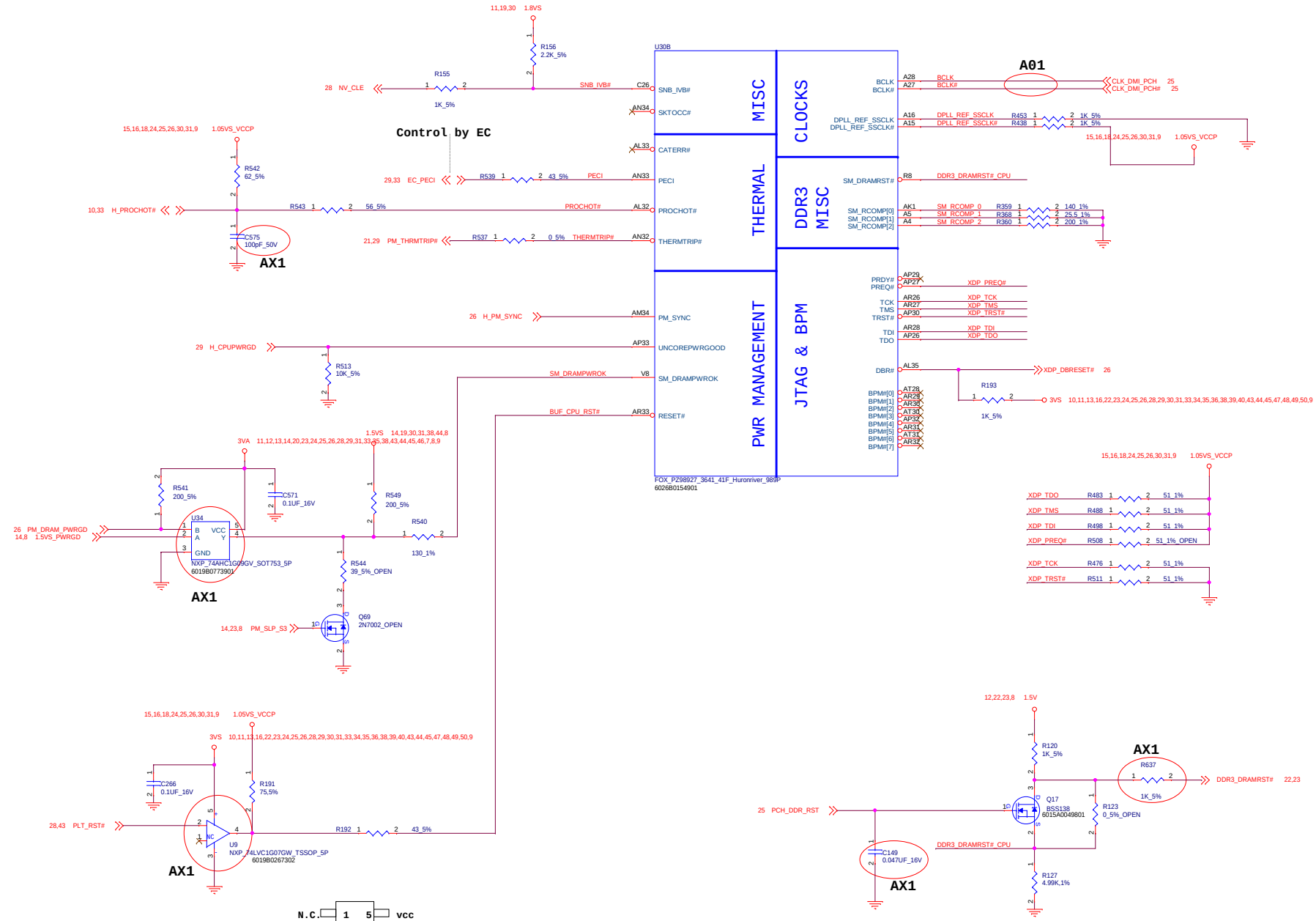
INVENTEC			
TITLE: Aegis Power Sequence			
SIZE: Custom	CODE IDENT: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 14 of 61	

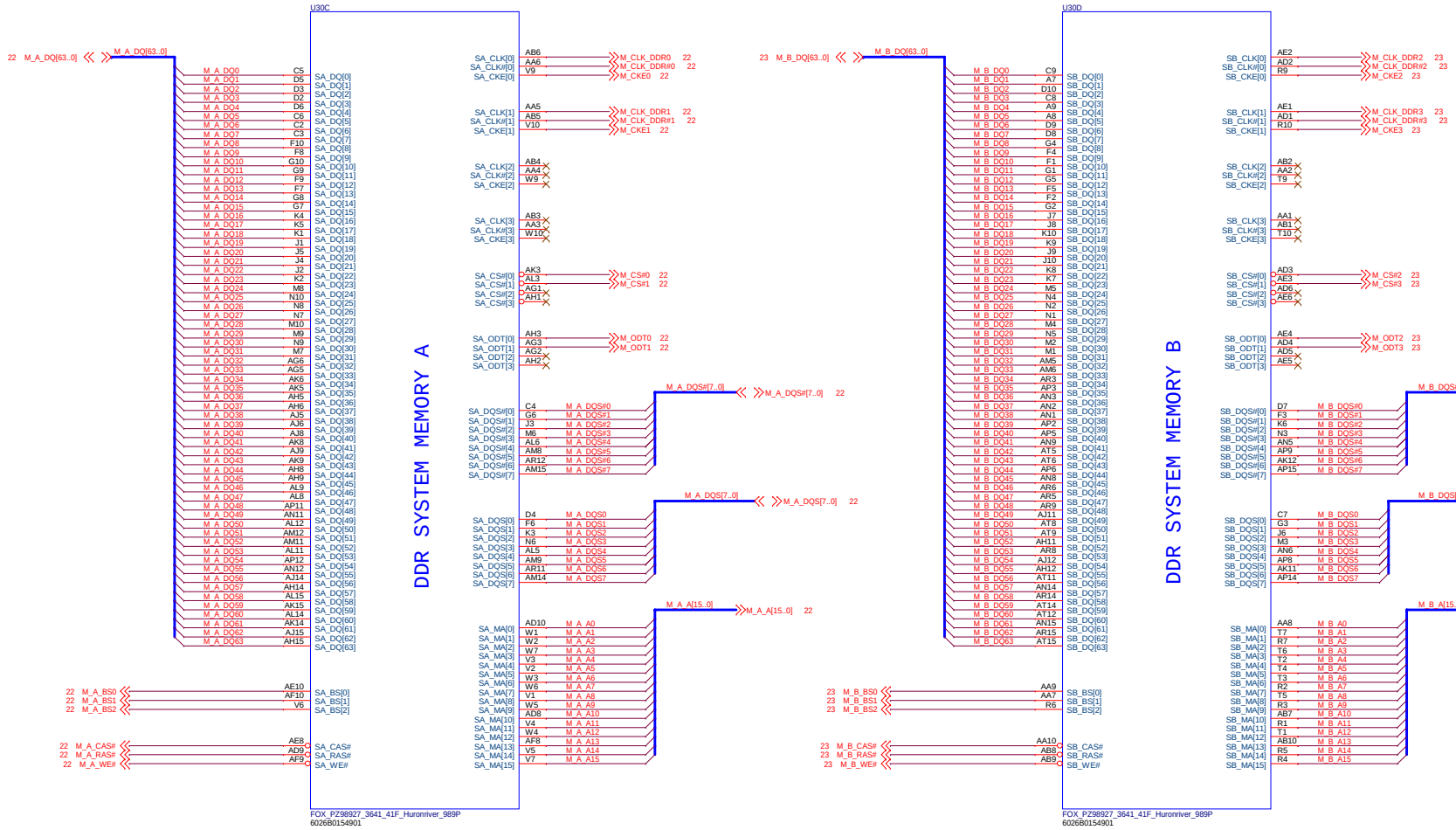


CLOSED TO CPU

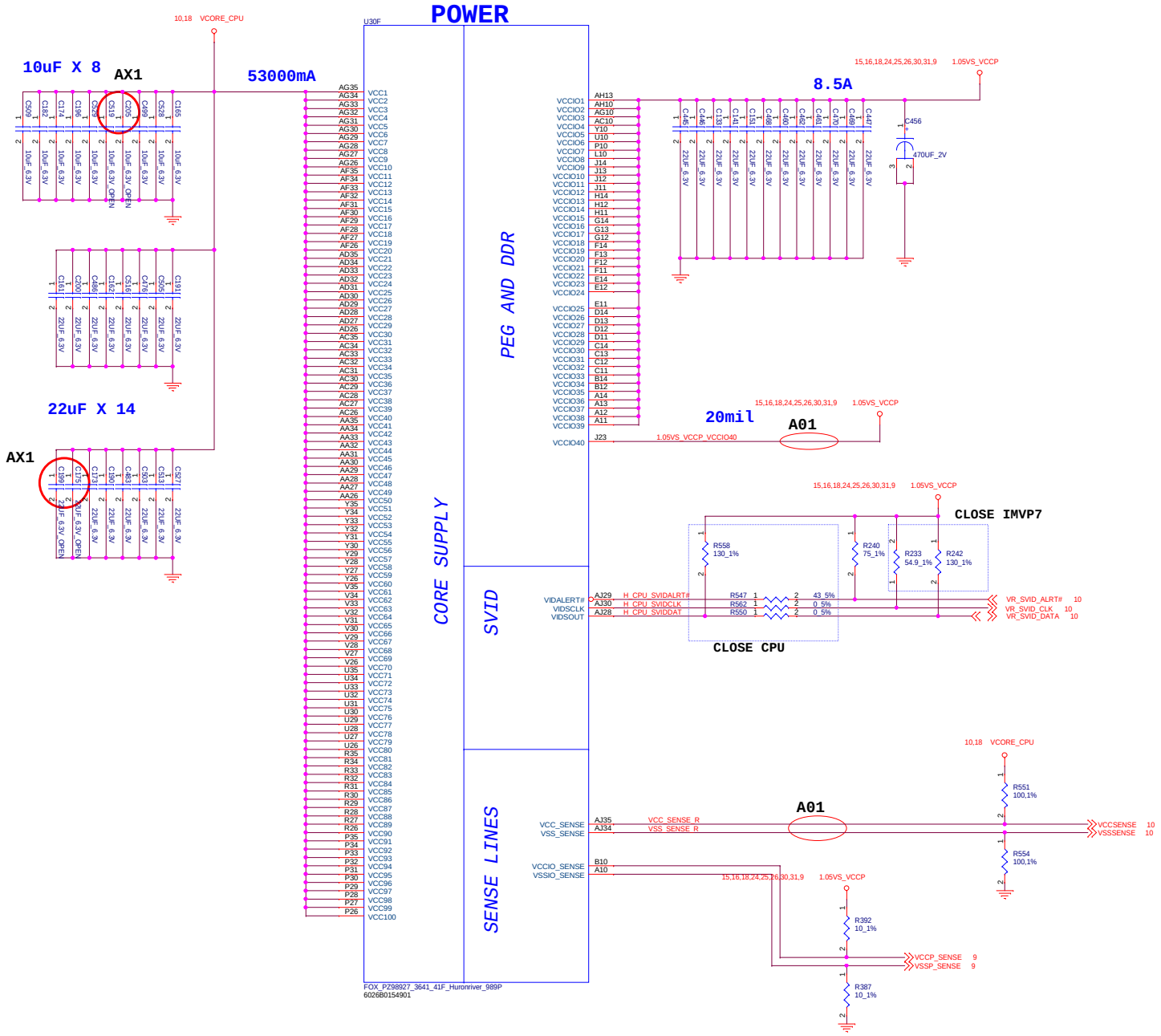
INVENTEC

TITLE	Aegis Processor(1/6)		
SIZE B	CODE ES	DOC.NUMBER CS-131	REV A01
CHANGE by IEC	DATE Friday, December 10, 2010	SHEET 15 of 61	





TITLE	Aegis Processor(3/6)		
SIZE C	CODE ES	DOC.NUMBER CS-131	REV A01
CHANGE by	IEC	DATE	Friday, December 10, 2010
SHEET	17	of	61



CHANGE by	IEC	DATE	Friday, December 10, 2010

INVENTEC

TITLE: Aegis
Processor(4/6)

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

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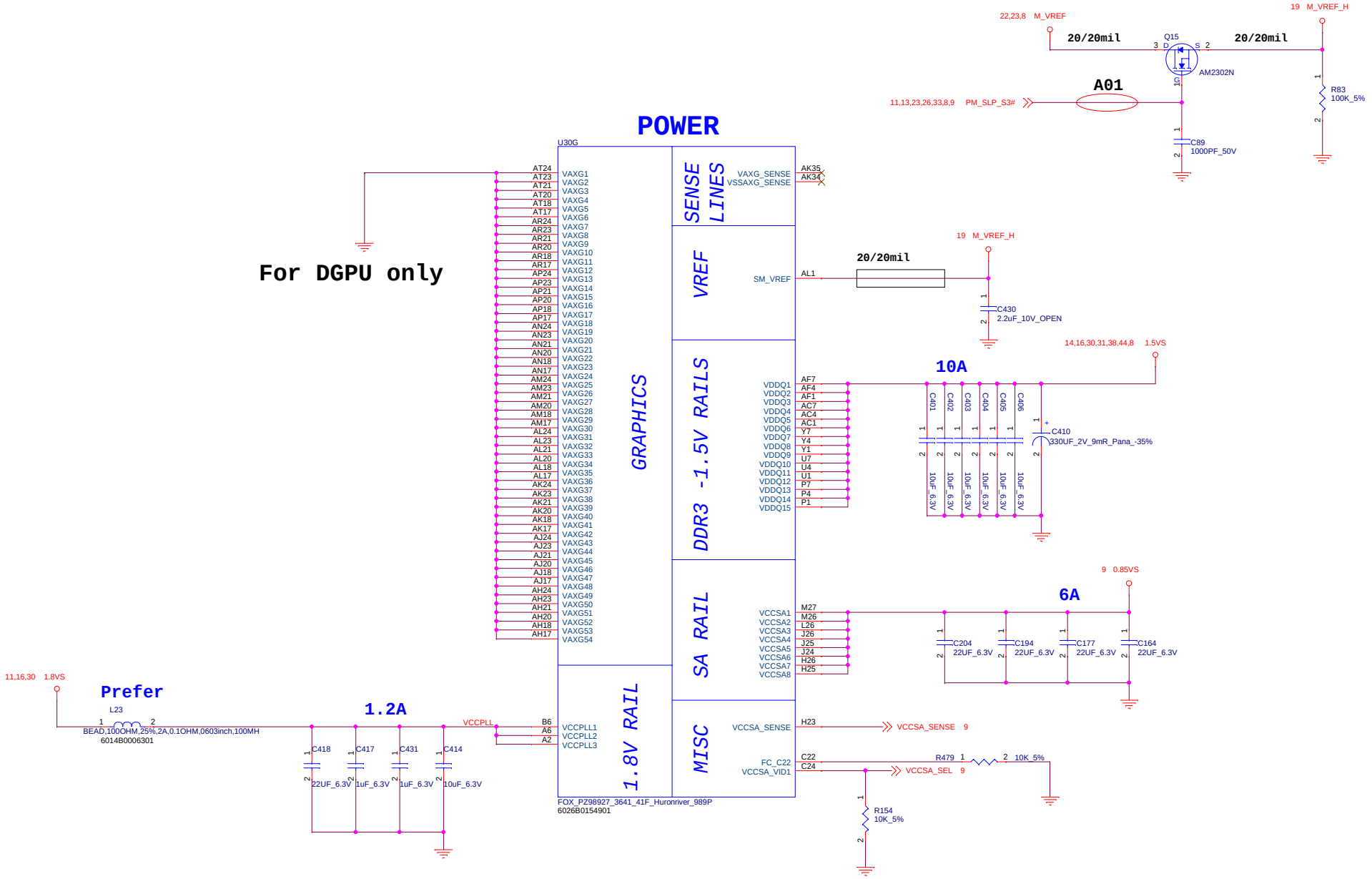
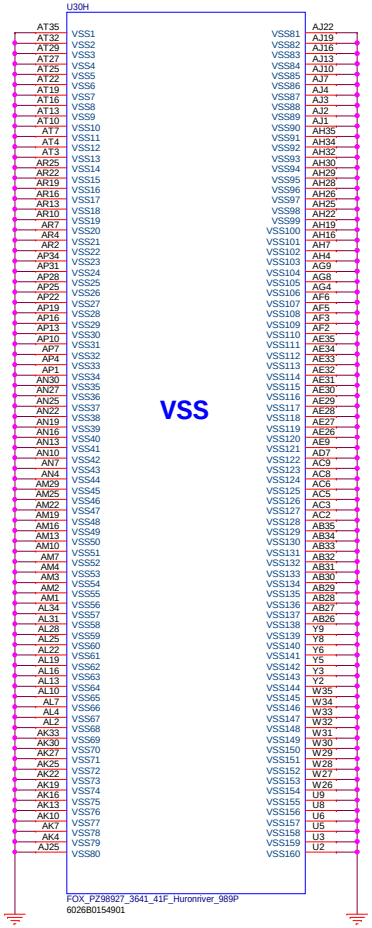
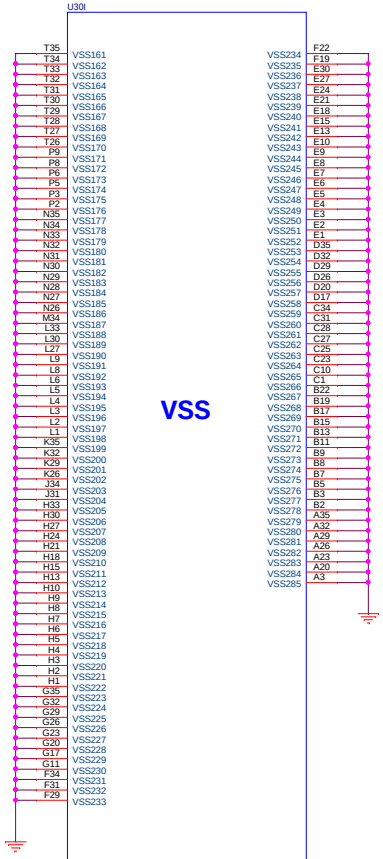
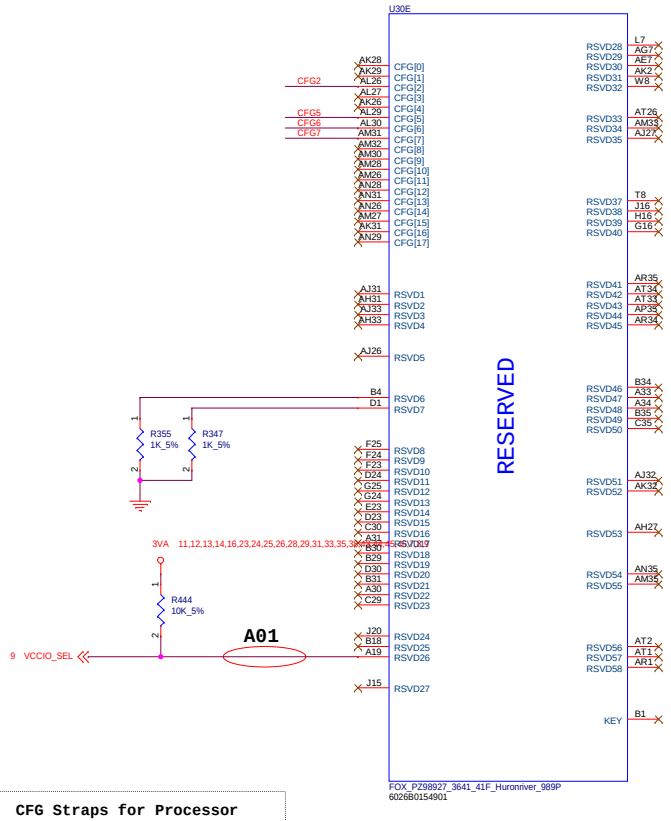
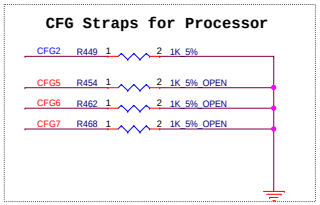


INVENTEC			
TITLE: Aegis Processor(5/6)			
SIZE: Custom	CODE IDENTIFY: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 19 of 61	









PEG Static Lane Reversal	- CFG2 is for the 16x
CFG2	1:(Default) Normal Operation; Line # definition matches socket pin map definition 0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default)x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1:(Default) PEG Train immediately following RESETB de assertion 0:PEG Wait for BIOS for training

INVENTEC

TITLE: Aegis
Processor(6/6)

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

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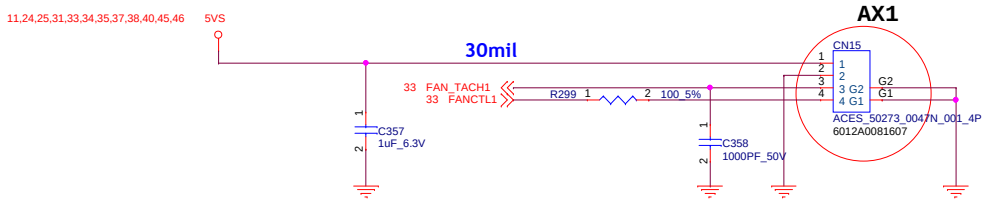
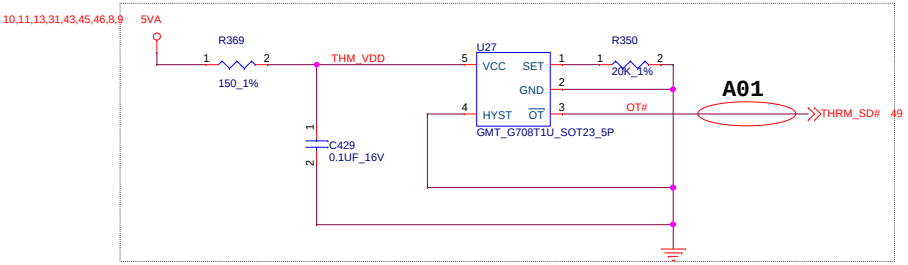
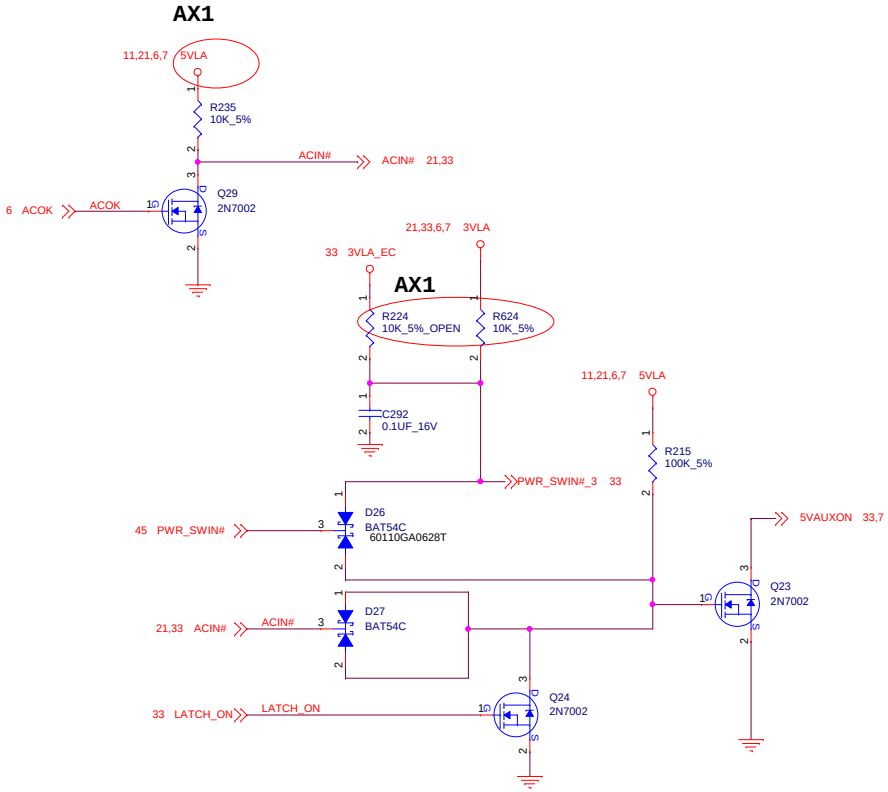
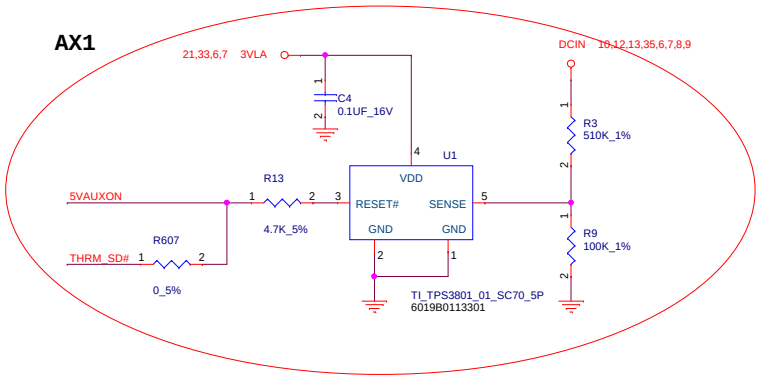
Fan control

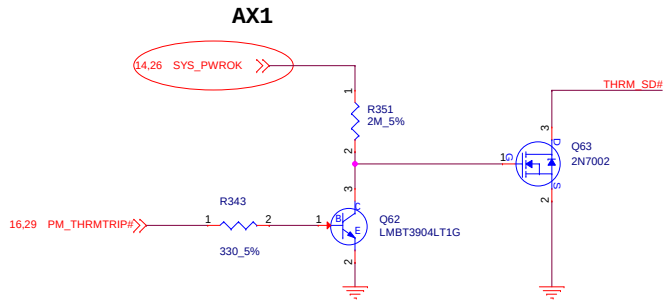


Temperature Security





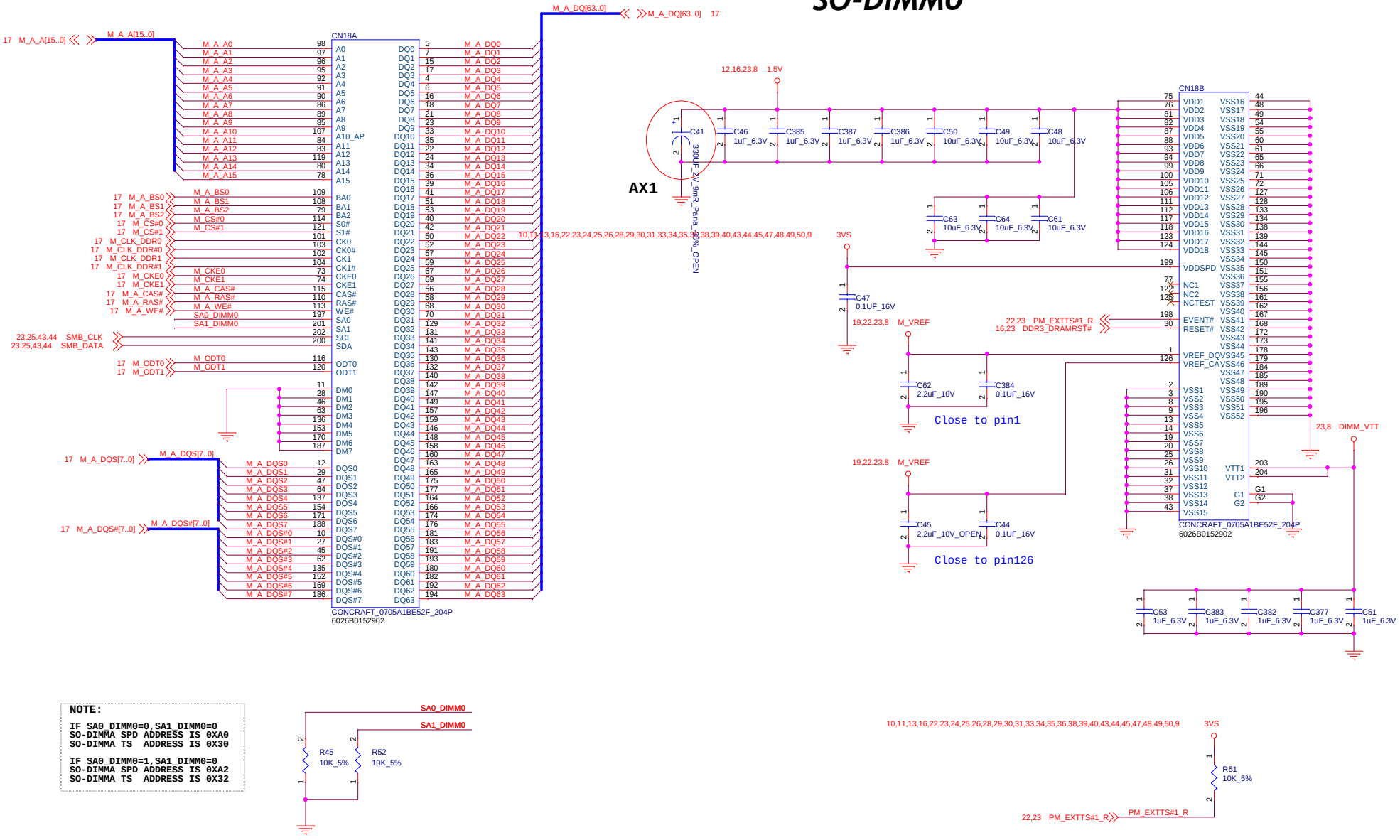




INVENTEC			
TITLE: Aegis FAN / THERMAL			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 21 of 61	

Need change for layout

SO-DIMM0



NOTE:

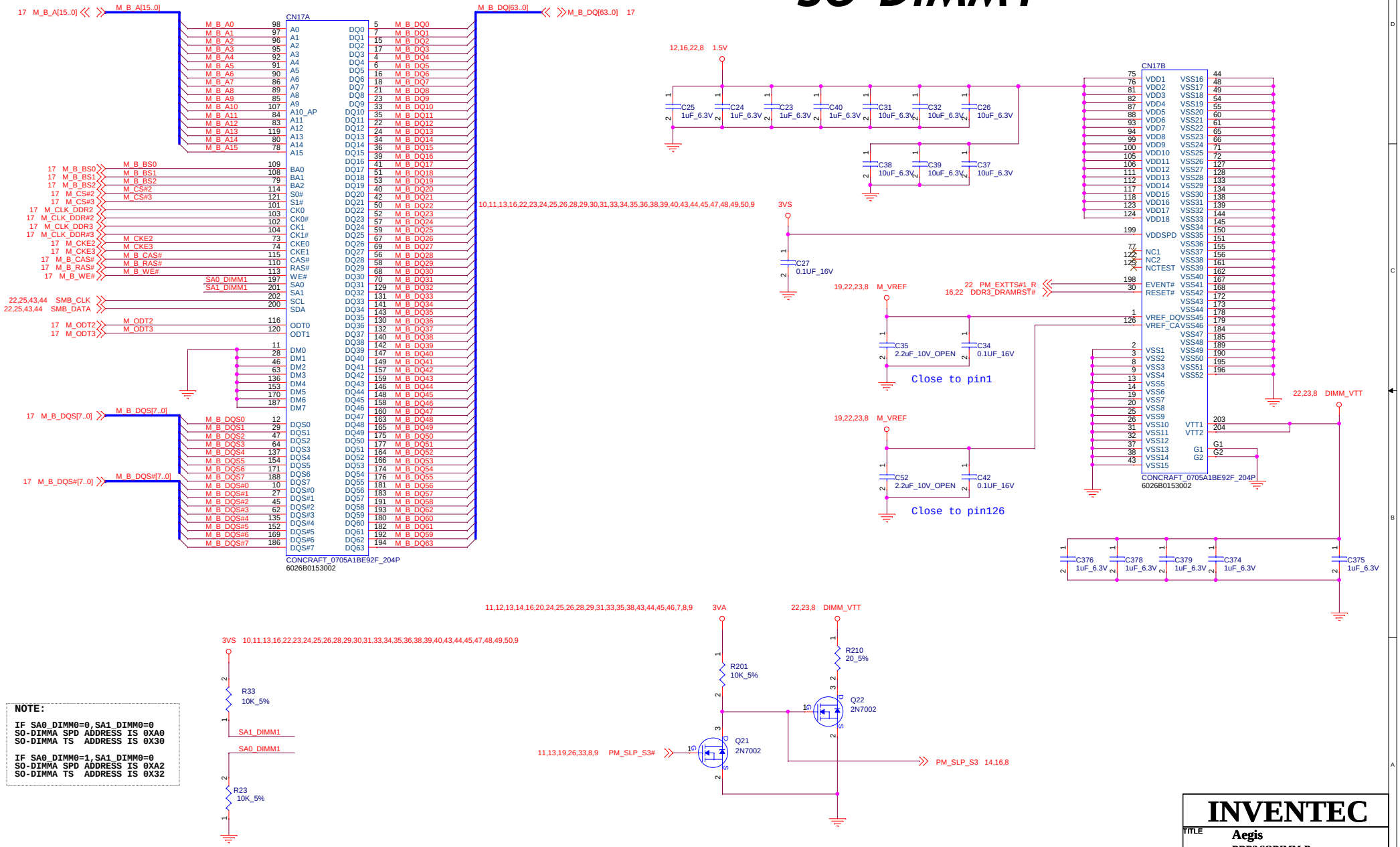
IF SA0_DIMM0=0,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

IF SA0_DIMM0=1,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

TITLE	Aegis DDR3 SODIMM-A		
SIZE Custom	CODE ES	DOC.NUMBER CS-131	REV A01
CHANGE by IEC	DATE Friday, December 10, 2010	SHEET 22 of 61	

INVENTEC

SO-DIMM1



NOTE:

IF SA0_DIMM0=0,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30

IF SA0_DIMM0=1,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

18.2:12.2

CHANGE by IEC	DATE Friday, December 10, 2010	SHEET 23 of 61	

INVENTEC

TITLE **Aegis**
DDR3 SODIMM-B

SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

FJ request

RTC Circuit

(HDA,JTAG,SPI,SATA)

located on DIMM window area.
CL1 CL2

NO Reboot Strap

Symbol OK

AX1

Close to PCH

Change to OPEN

HDD I/F

HDD I/F for 17"

ODD I/F

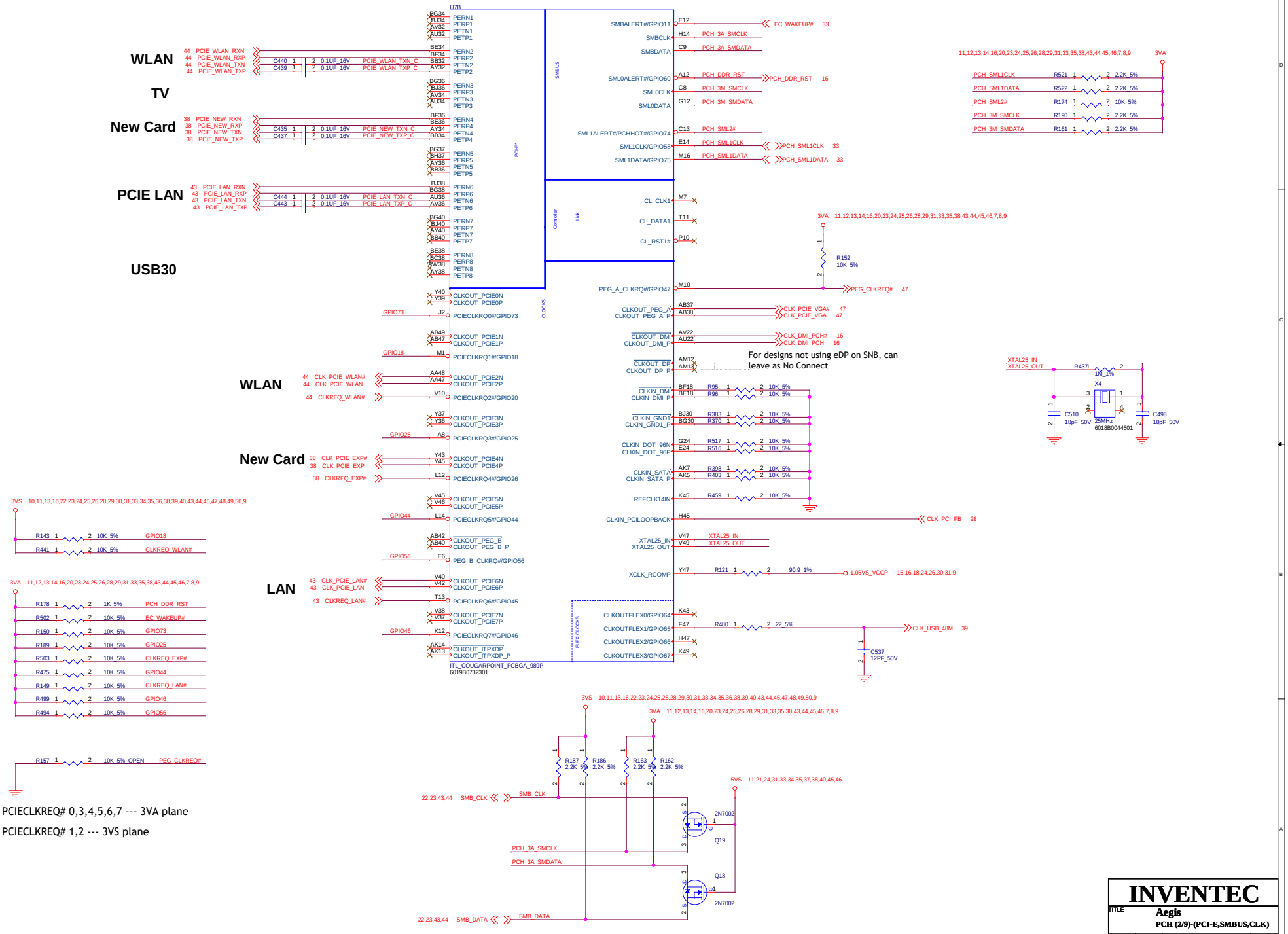
USB3.0 for 17"

ESATA I/F

Flash Descriptor Security Overide	
HDA_SDOUT_R	High : Enable Low : Disable

INVENTEC				
TITLE: Aegis PCH (1/9)-(HDA,JTAG,SATA)				
SIZE: C	CODE ES	DOC.NUMBER: CS-131	REV: A01	
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 24 of 61		

(PCI-E,SMBUS,CLK)



CHANGE by	IEC
DATE	Friday, December 10, 2010

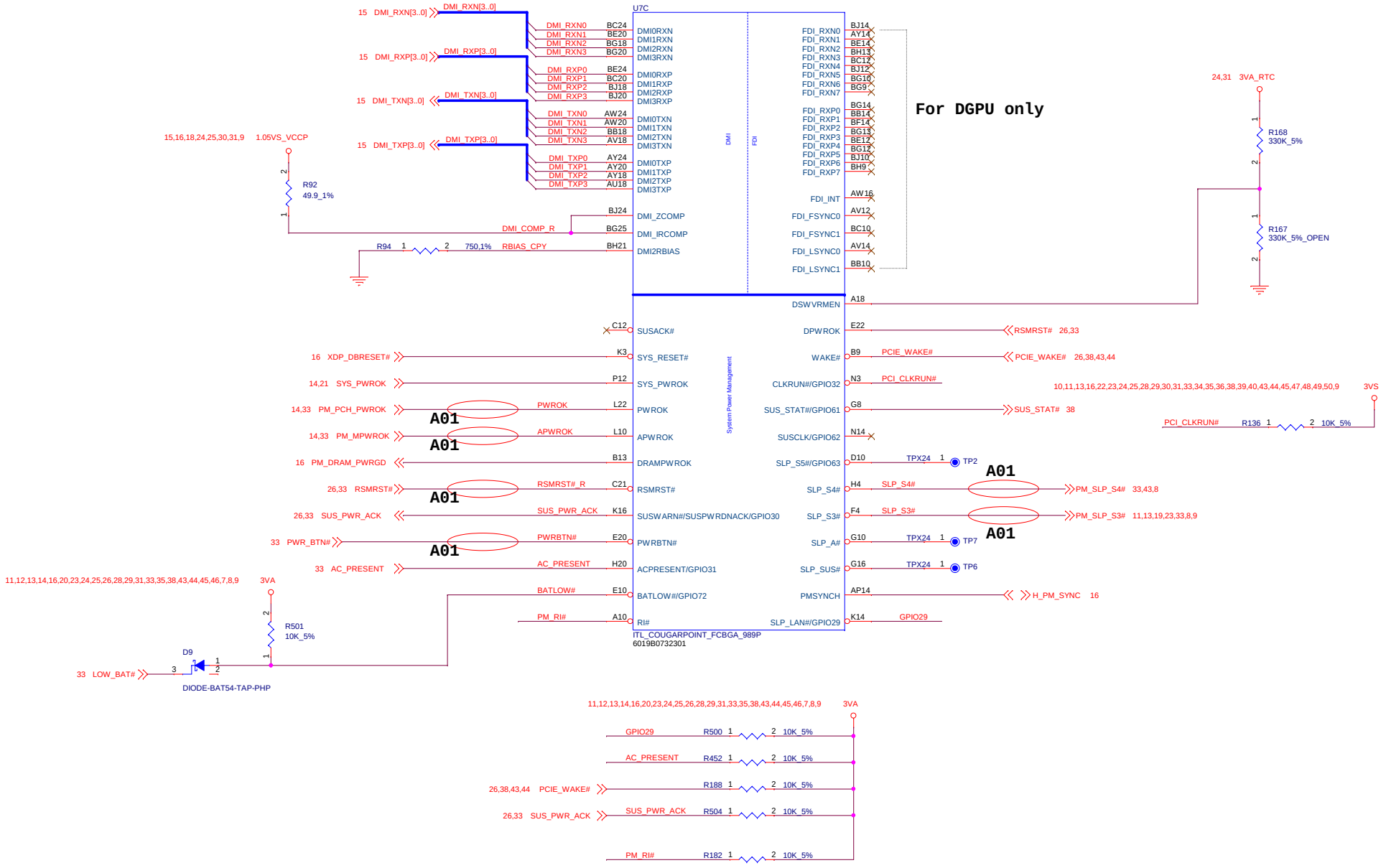
INVENTEC

TITLE: Aegis
PCH (2/9)-(PCI-E,SMBUS,CLK)

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

SHEET 25 of 61

(DMI,FDI,GPIO)



CHANGE by	IEC	DATE	Friday, December 10, 2010	SHEET	26 of 61

INVENTEC

TITLE: Aegis
PCH (3/9)-(DMI,FDI,GPIO)

SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

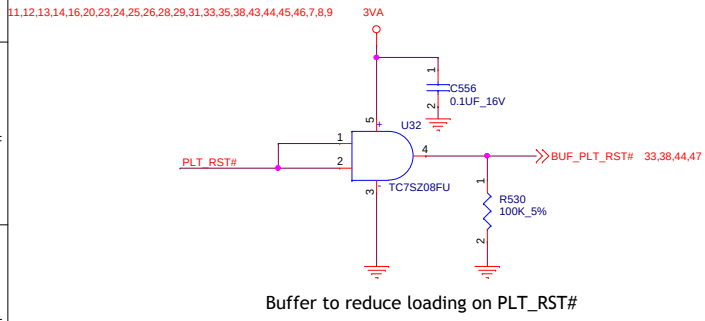
(LVDS,DDI)

Place 150ohm termination resistor close to GMCH

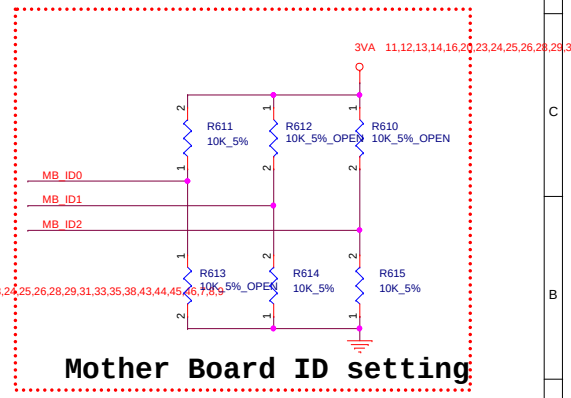
INVENTEC			
TITLE: Aegis PCH (4/9)-(LVDS,DDI)			
SIZE: B	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 27 of 61	

(PCI,USB,NVRAM)

FJ Mother Board ID setting			
Project	MB_ID2	MB_ID1	MB_ID0
	0	0	0
Aegis (Discrete)	0	0	1
Neurron (UMA)	0	1	0
Neuron-V (Optimus)	0	1	1
Strike (UMA)	1	0	0
Strike-V (Optimus)	1	0	1
Silk (UMA)	1	1	0
Silk-V (Optimus)	1	1	1
PCH ---------->	GPIO41	GPIO40	GPIO59



Buffer to reduce loading on PLT_RST#

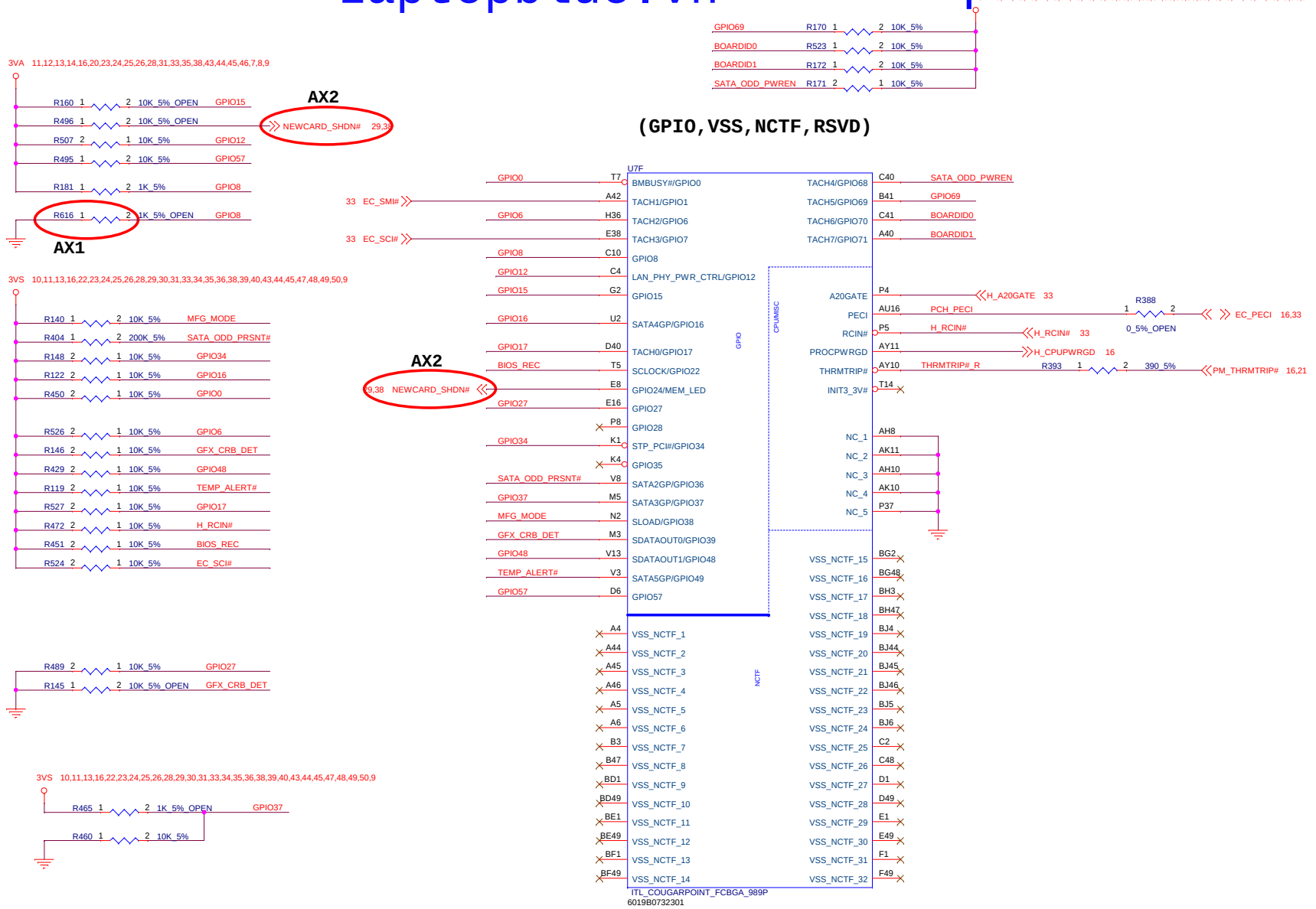


CHANGE by	IEC	DATE	Friday, December 10, 2010	SHEET	28 of 61

INVENTEC

TITLE: Aegis
PCH (5/9)-(PCI,USB,NVRAM)

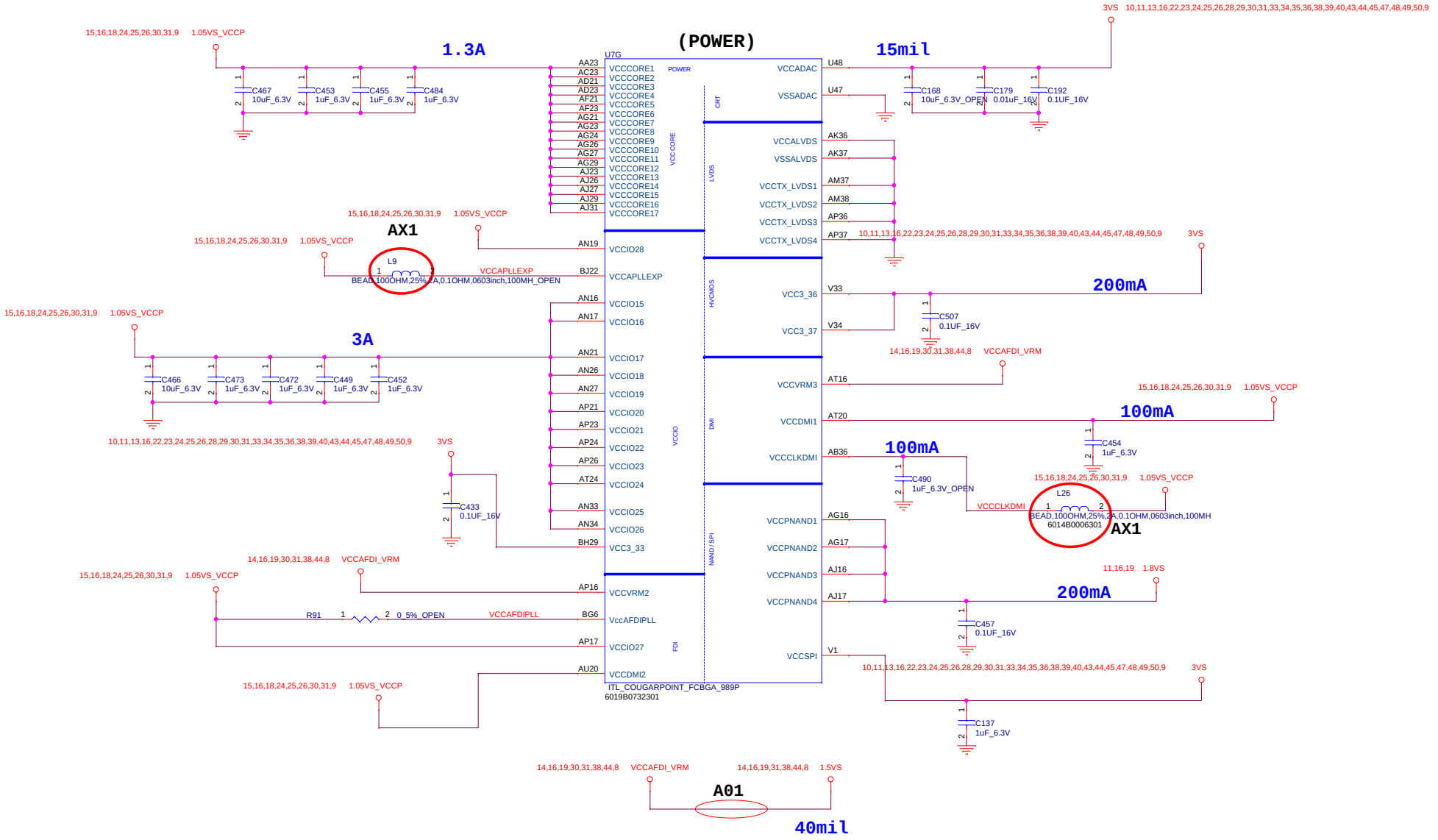
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01



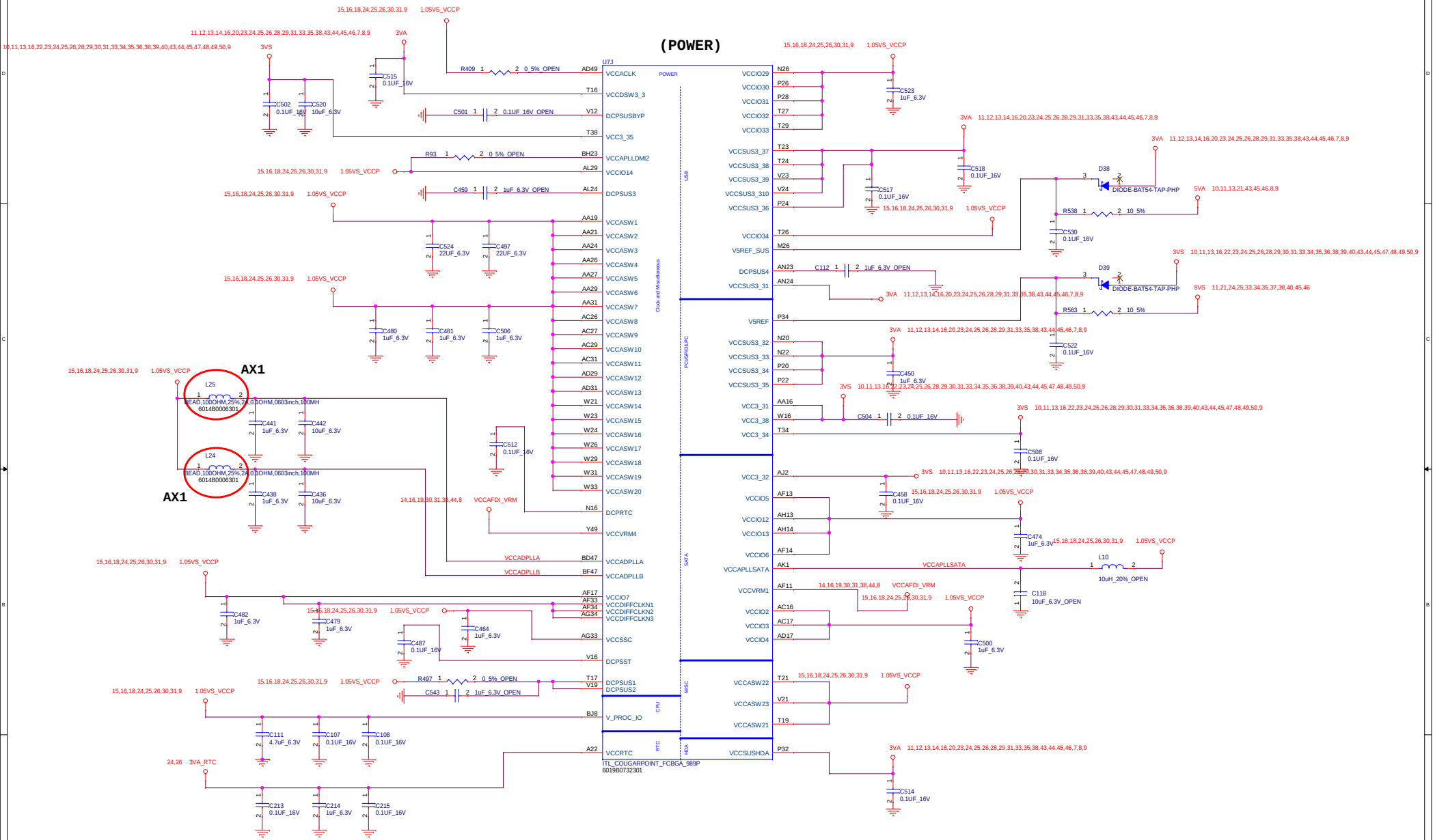
CHANGE by	IEC	DATE	Friday, December 10, 2010	SHEET	29 of 61

INVENTEC

TITLE	Aegis PCH (6/9)-(GPIO,VSS,NCTF,RSVD)			
SIZE	CODE	DOC.NUMBER		REV
Custom	ES	CS-131		A01



TITLE	INVENTEC Aegis PCH (7/9)-(POWER)
SIZE	Custom
CODE	ES
DOC.NUMBER	CS-131
REV	A01
CHANGE by	IEC
DATE	Friday, December 10, 2010
SHEET	30 of 61

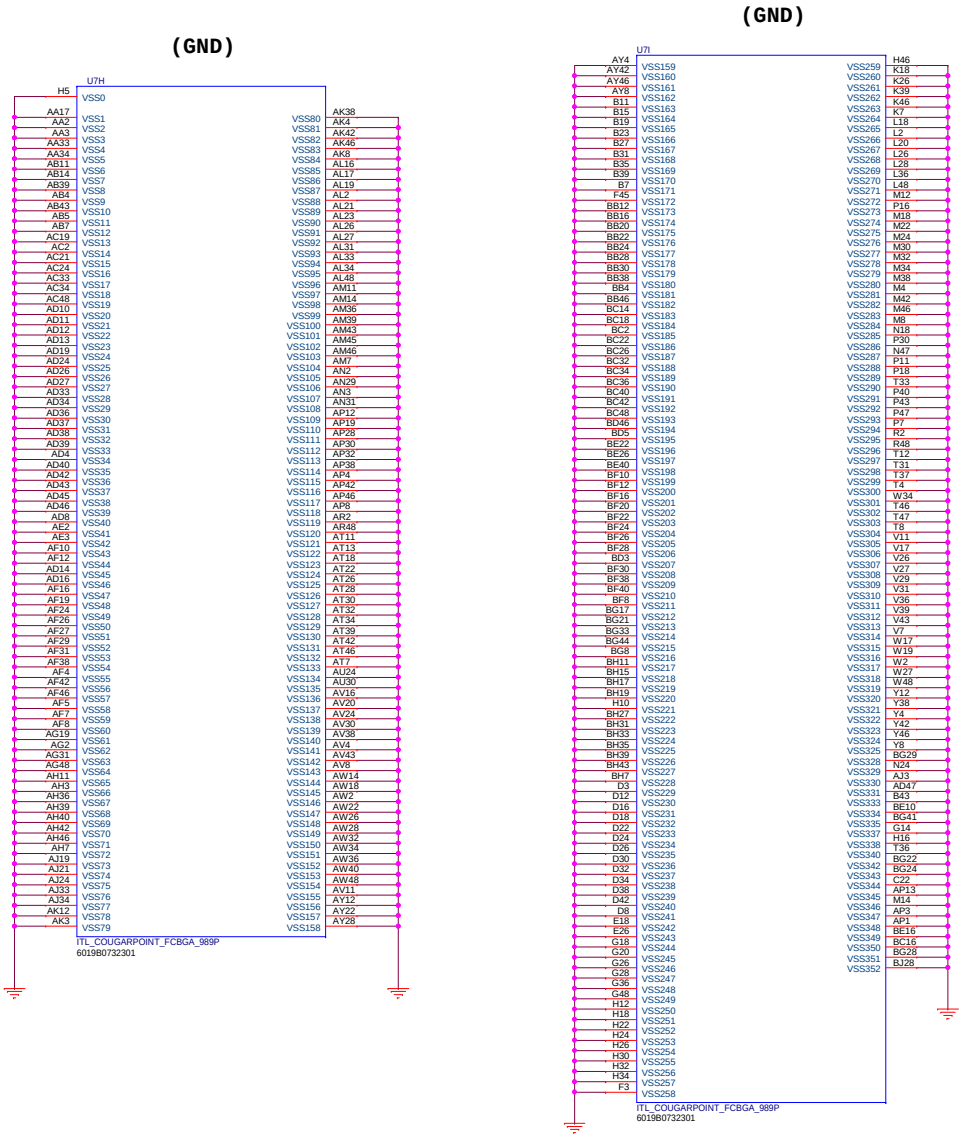


CHANGE by	IEC	DATE	Friday, December 10, 2010	SHEET	31 of 61

INVENTEC

TITLE: Aegis
PCH (8/9)-(POWER)

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

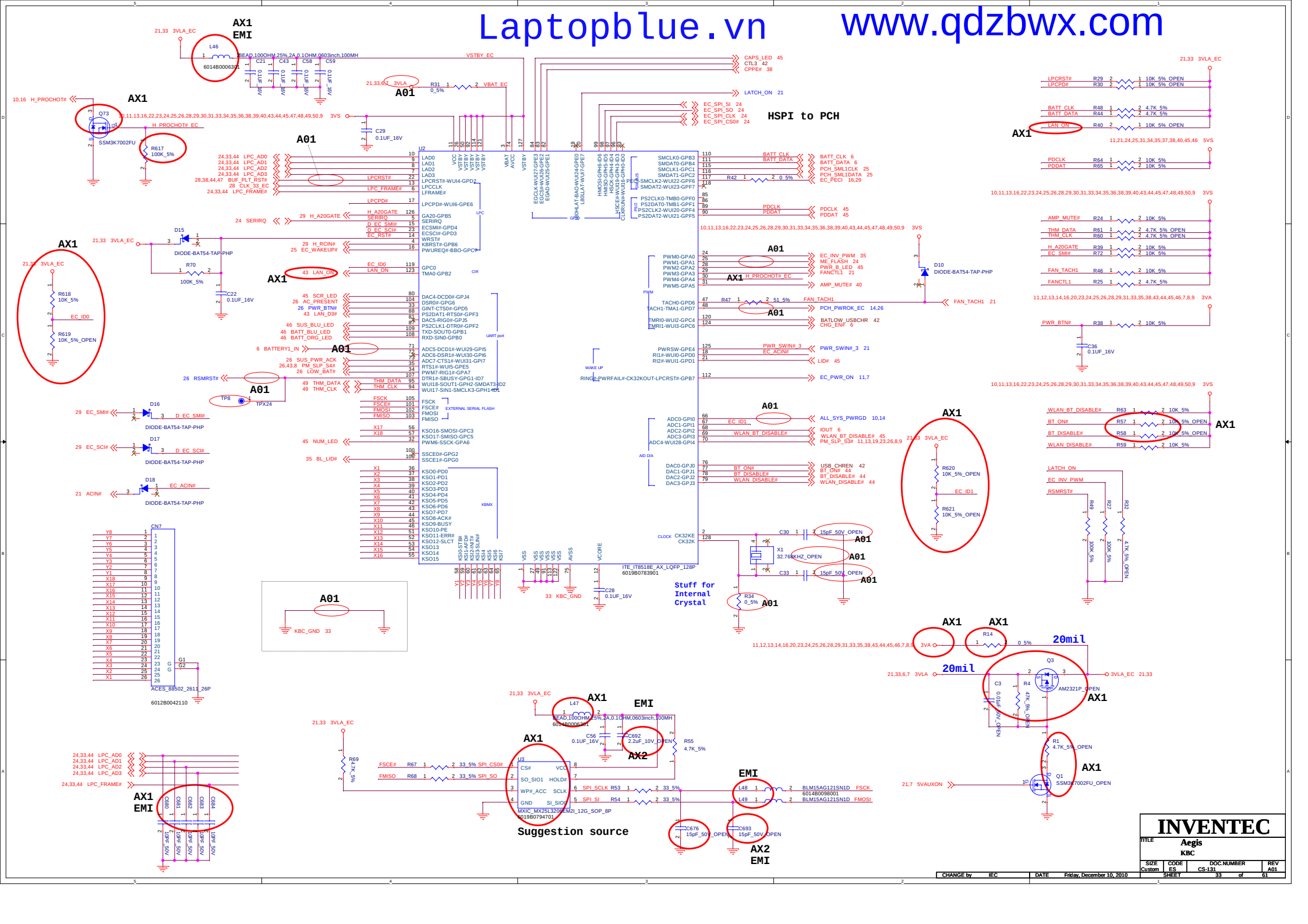


INVENTEC

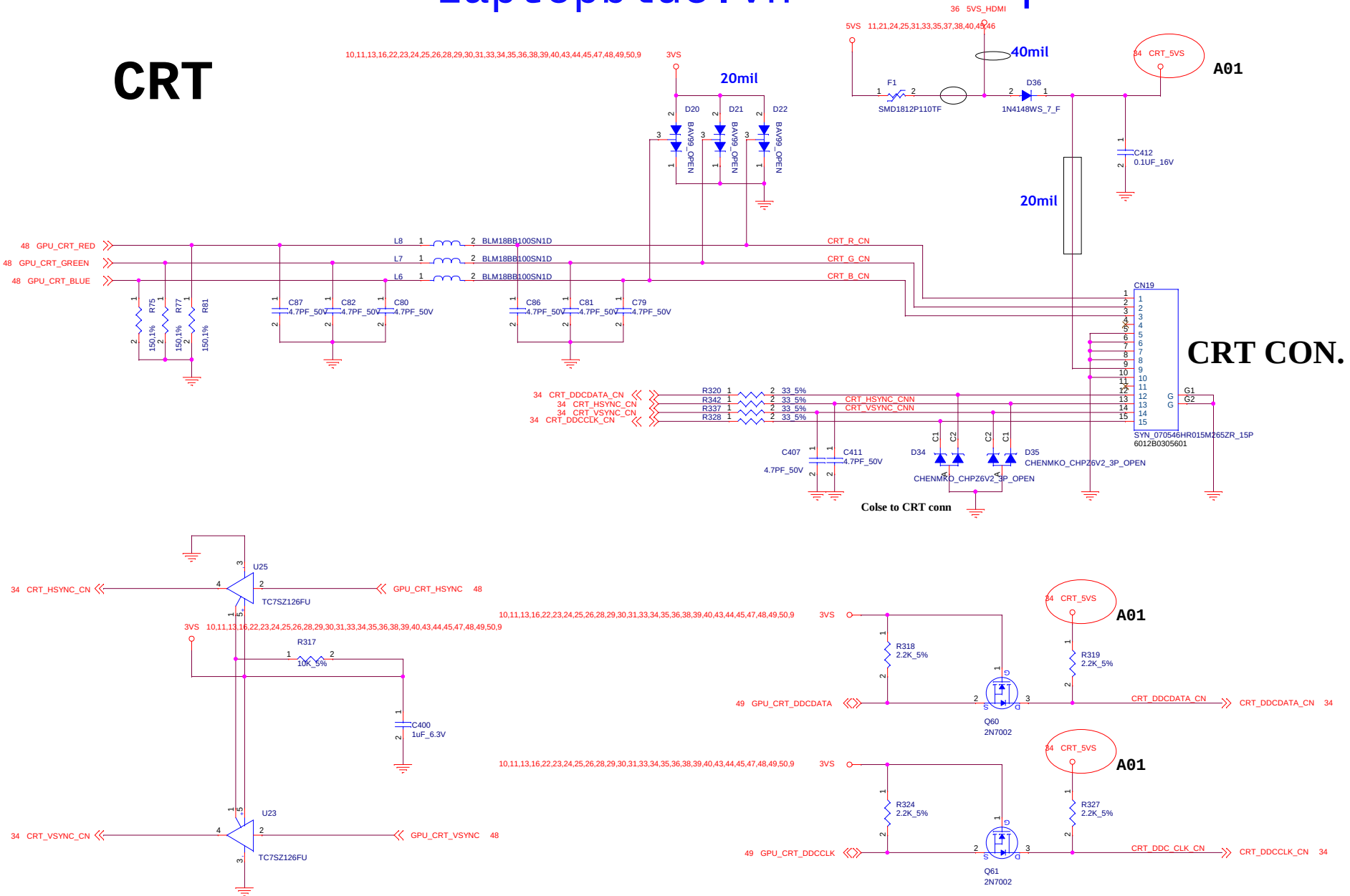
TITLE: Aegis
PCH (9/9)-(GND)

SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

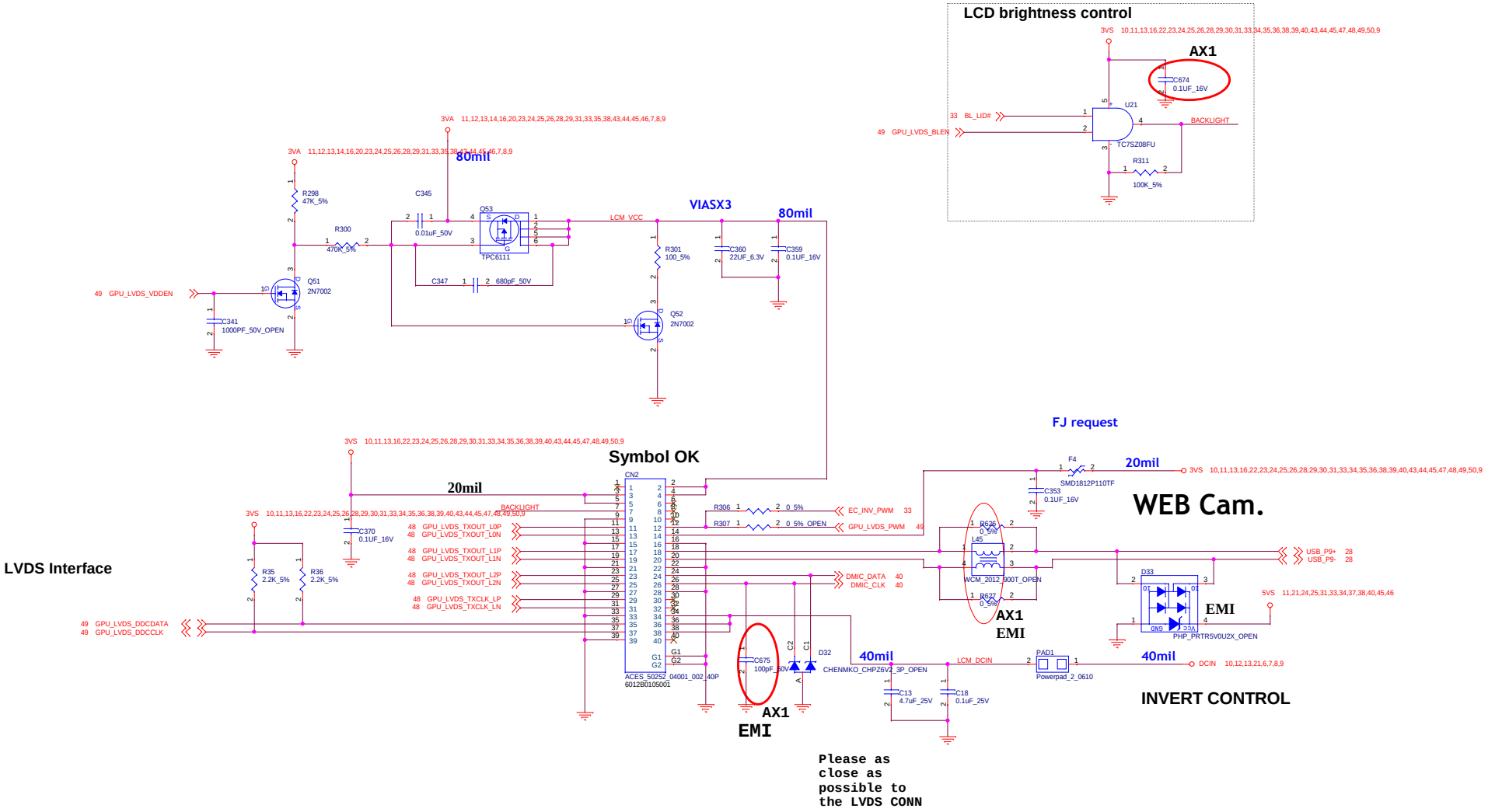
CHANGE by IEC | DATE Friday, December 10, 2010 | SHEET 32 of 61



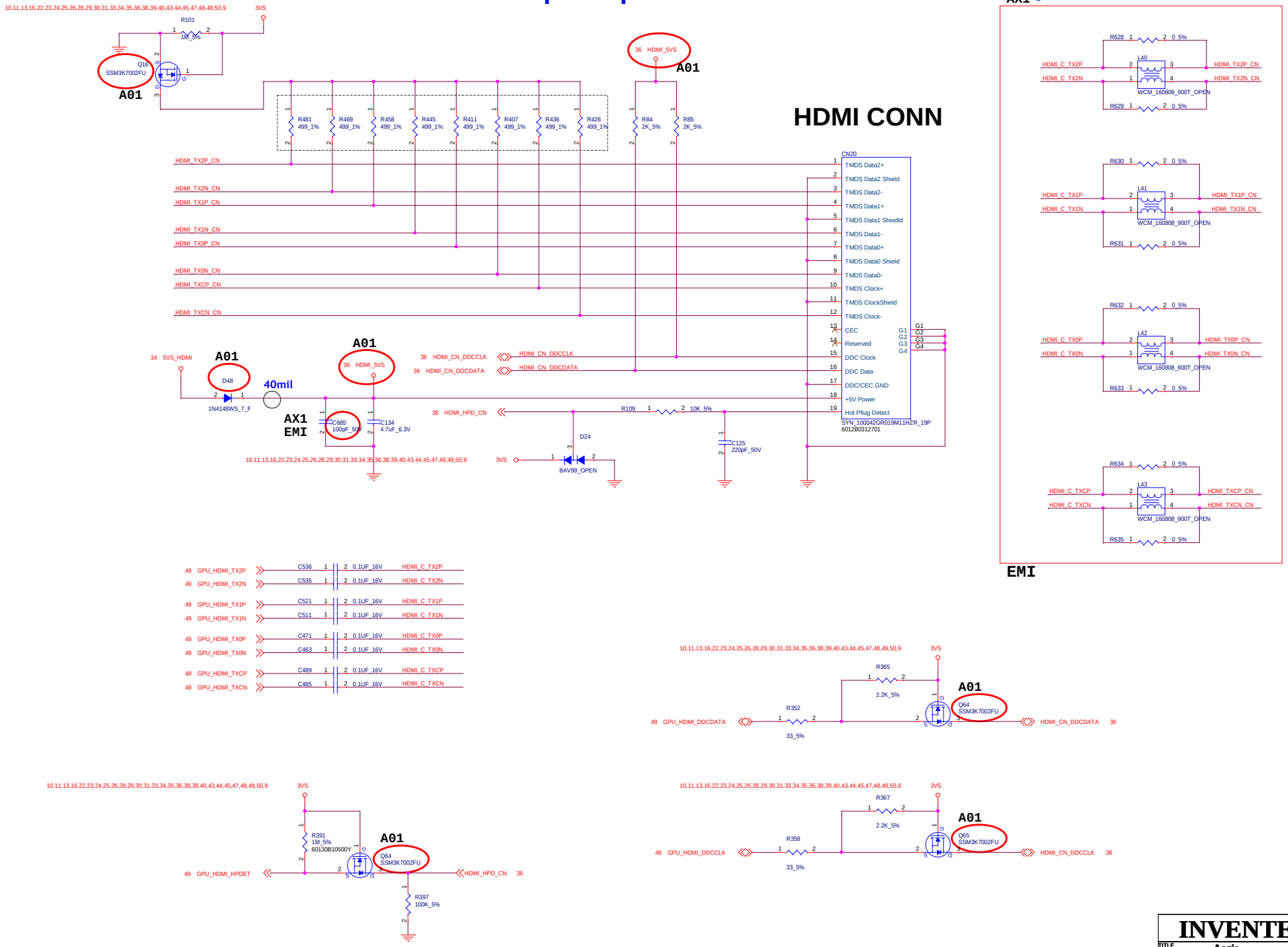
CRT



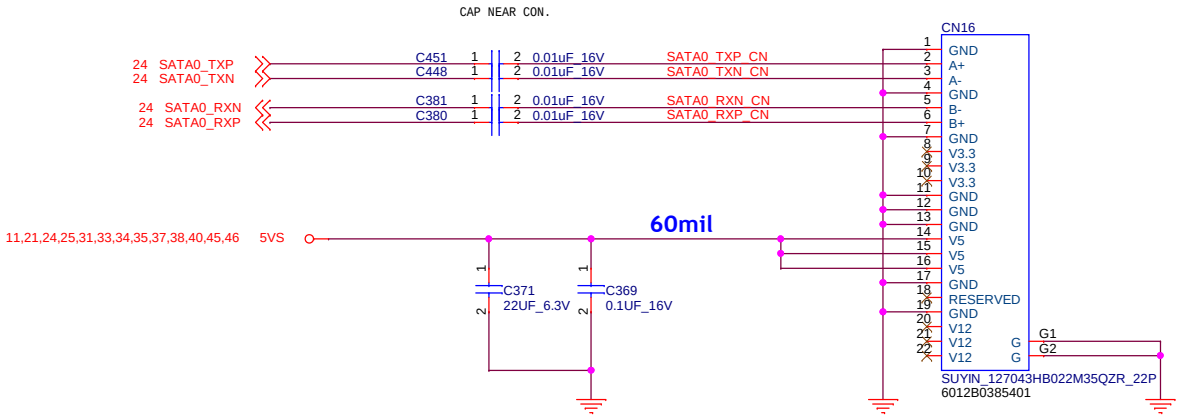
INVENTEC			
TITLE: Aegis CRT			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 34 of 61	



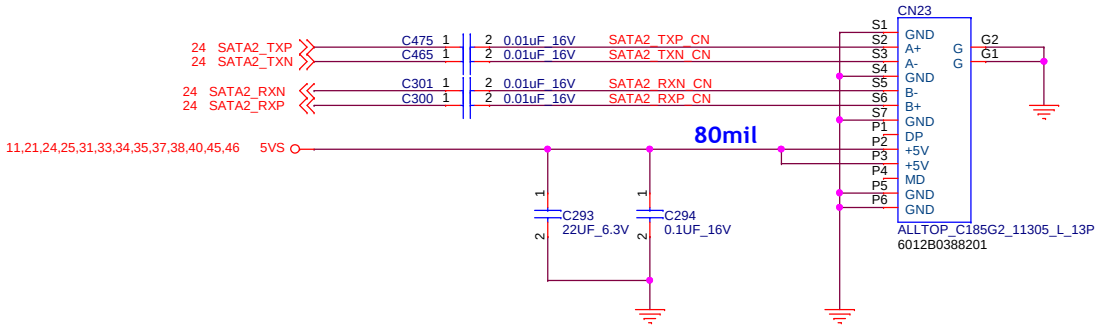
INVENTEC			
TITLE: Aegis LVDS			
SIZE: C	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 35 of 61	



HDD I/F

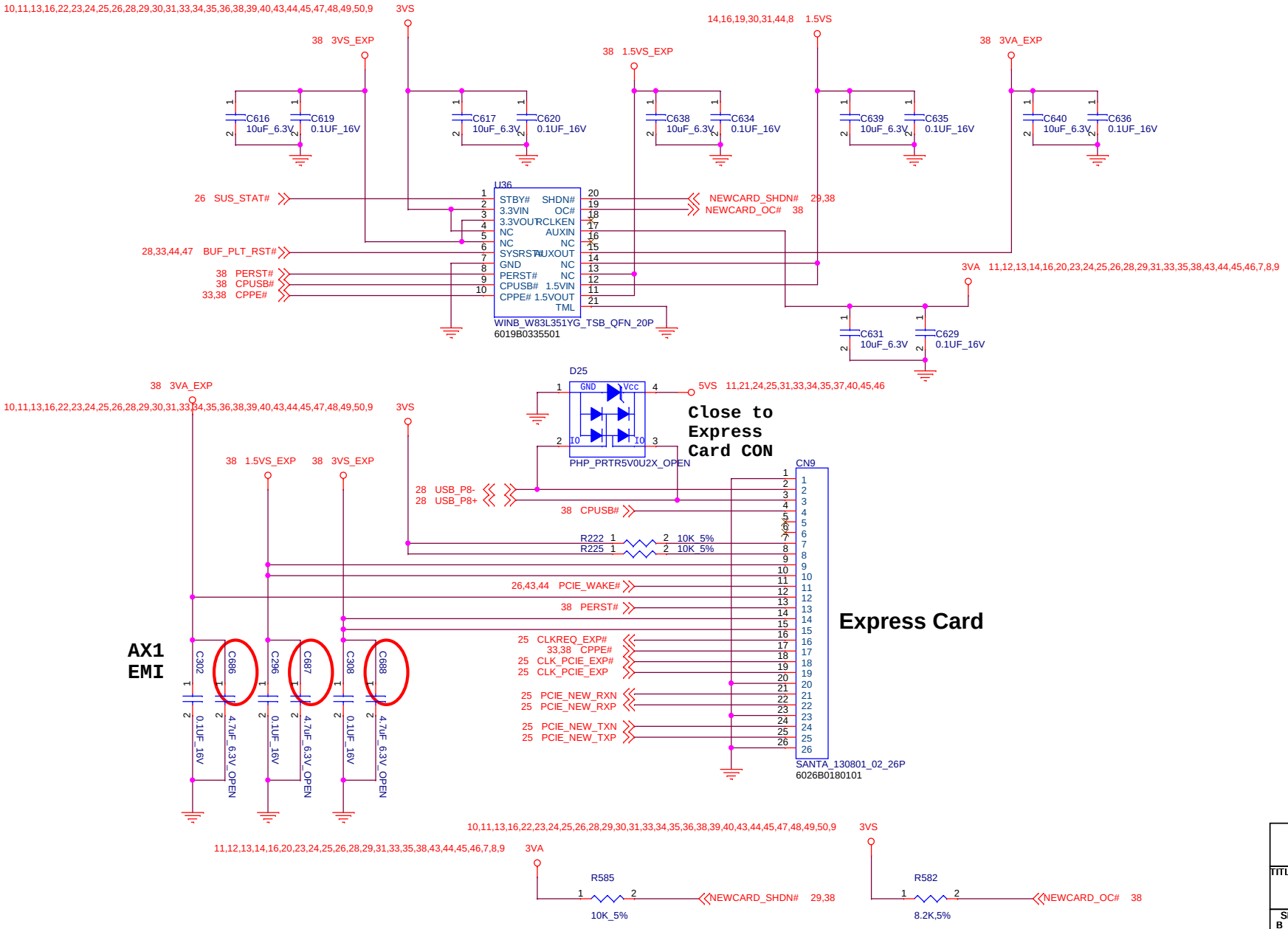


ODD I/F



INVENTEC			
TITLE: Aegis SATA HDD/ODD			
SIZE: B	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 37 of 61	

New Card Board

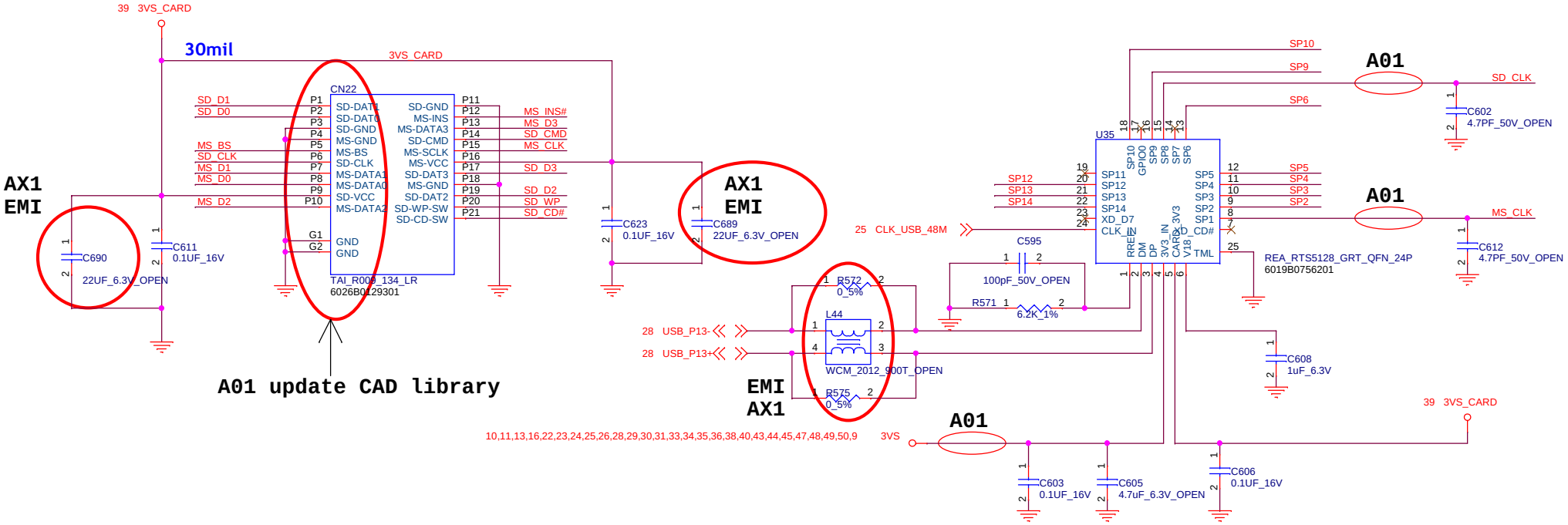


INVENTEC			
TITLE: Aegis Express Card			
SIZE: B	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 38 of 61	

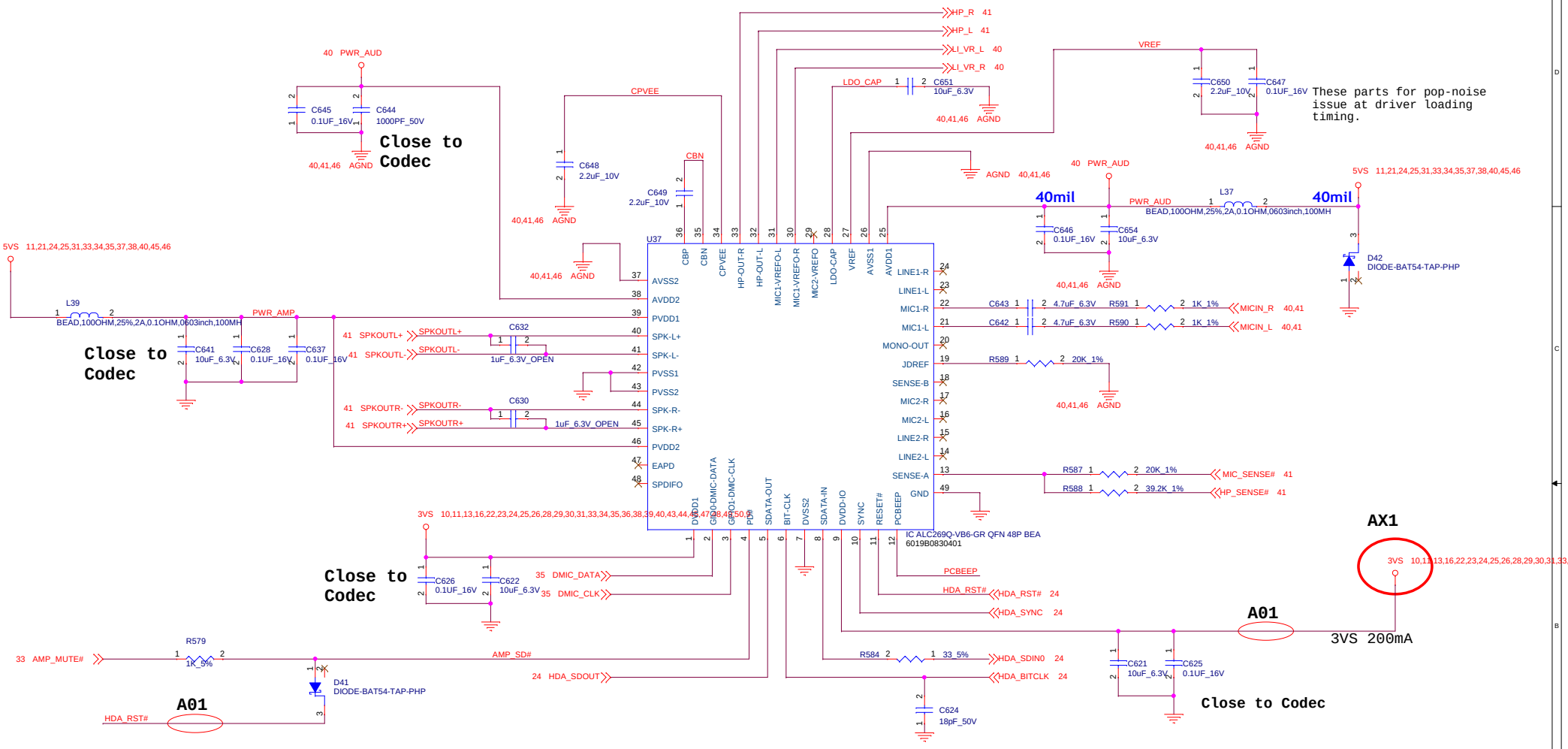
SP1 SD_WP MS_CLK
SP2 MS_INS#
SP3 SD_D1
SP4 SD_D0 MS_D7
SP5 SD_D7 MS_D3
SP6 SD_CD#

SP8 SD_CLK MS_D2
SP9 SD_D5 MS_D0
SP10 SD_CMD
SP12 SD_D3 MS_D1
SP13 SD_D2 MS_D5
SP14 MS_BS

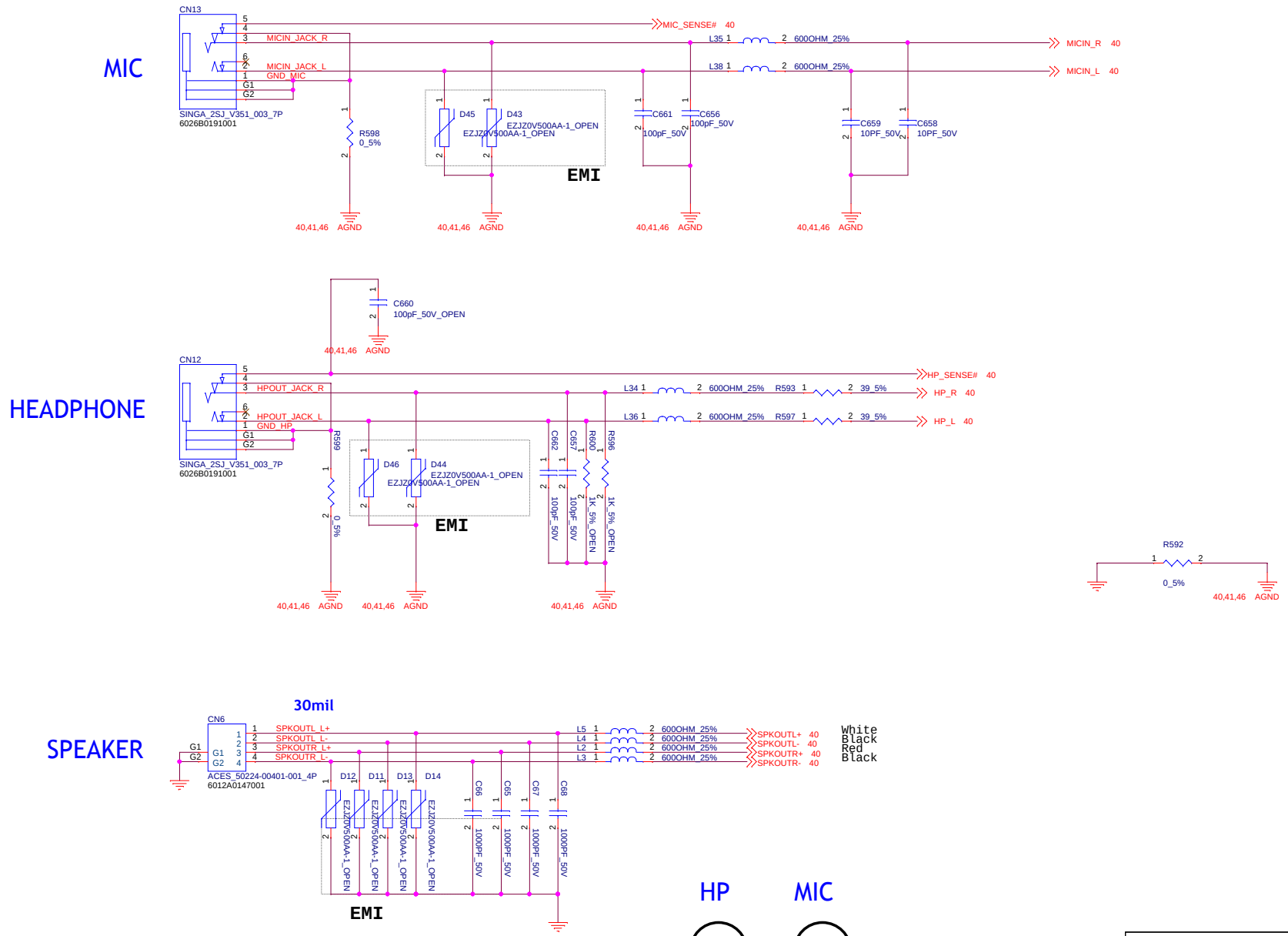
SD_CLK, MS_CLK trace layout be stripline layer.



INVENTEC			
TITLE: Aegis Card Reader			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 39 of 61	

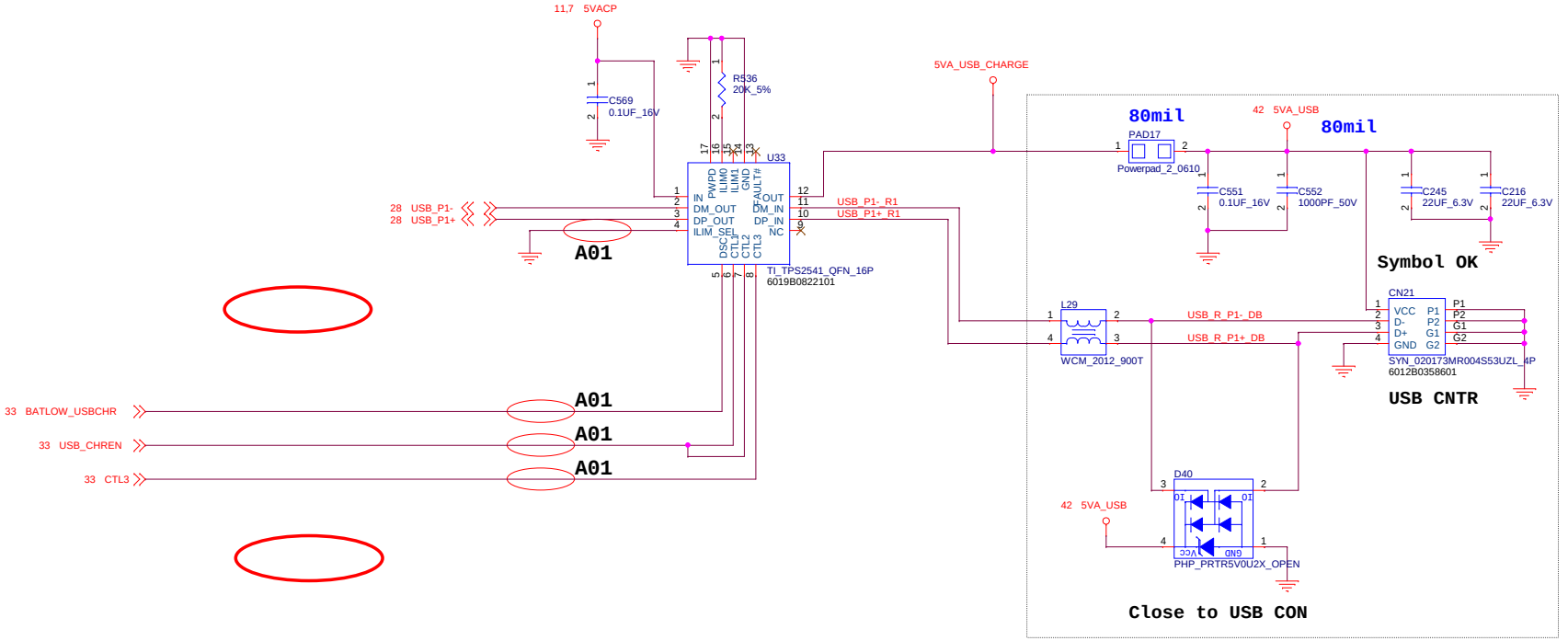


INVENTEC			
TITLE: Aegis Audio Codec			
SIZE: Custom	CODE: ES	DOC.NUMBER: D-CS-1310A22767-0-ALG	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 40 of 61	



INVENTEC			
TITLE: Aegis HP/ MIC JACK/SPK			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 41 of 61	

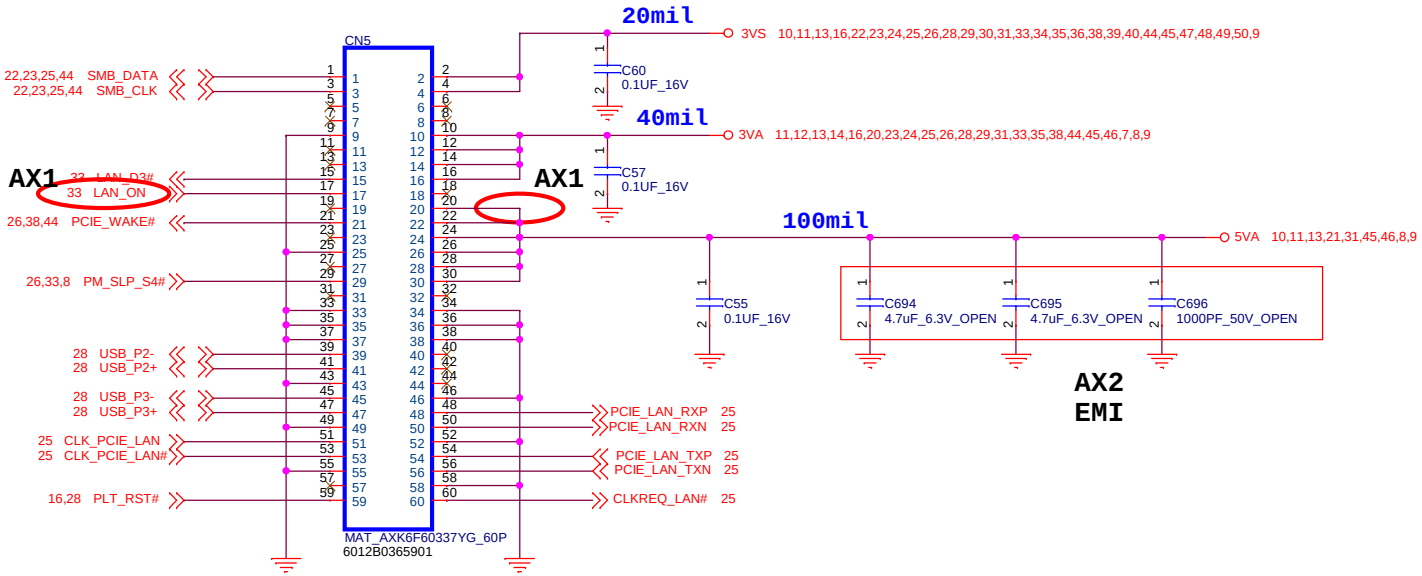
Power OFF Charge USB



INVENTEC			
TITLE: Aegis USB power off charger			
SIZE: Custom	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 42 of 61	

Symbol Ok

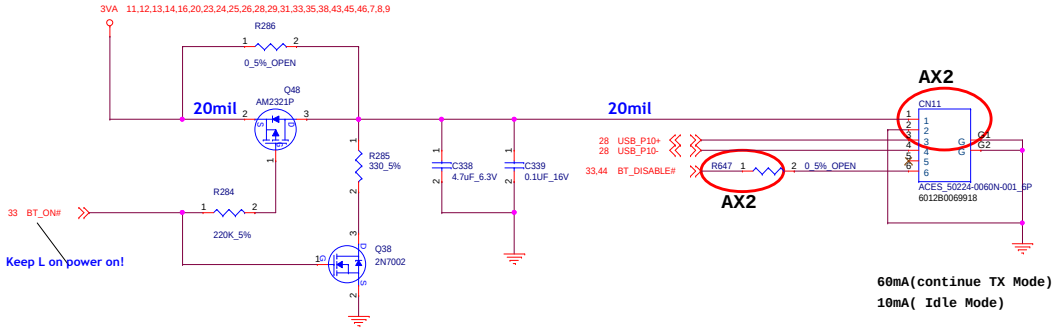
TO USB/LAN BOARD



NEW Symbol OK

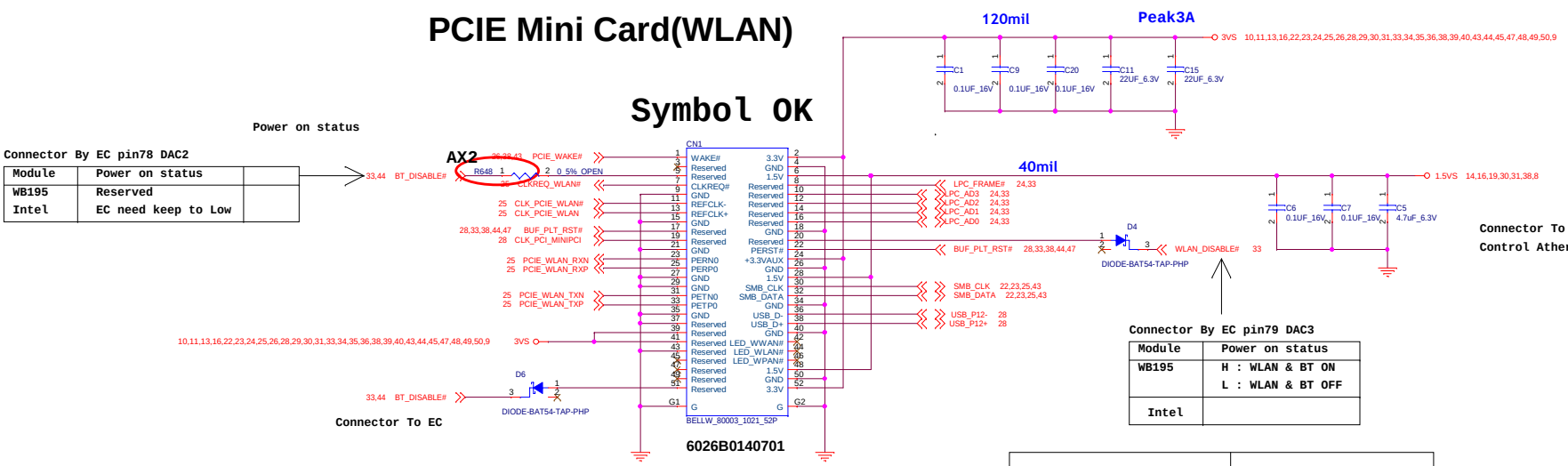
INVENTEC			
TITLE: Aegis USB/LAN I/F			
SIZE: B	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 43 of 61	

Bluetooth CNN.



PCIE Mini Card(WLAN)

Symbol OK



Idle mode: 252.1 mA(Max.) Connect AP: 265.6 mA(Max.)	Idle mode: 96.1 mA(Max.) Connect AP: 92.3 mA(Max.)

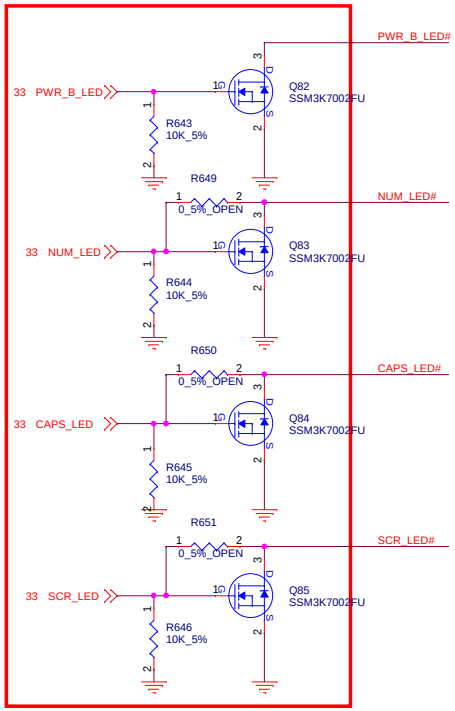
INVENTEC

TITLE: Aegis
WLAN/BT

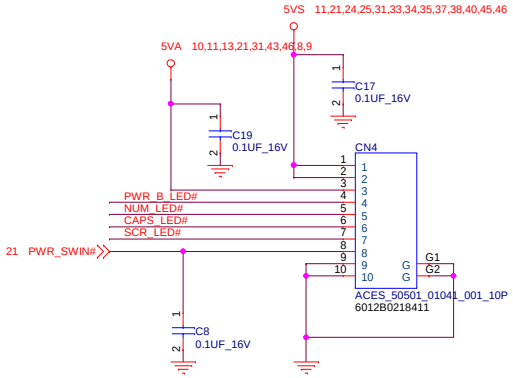
SIZE	CODE	DOC.NUMBER	REV
C	ES	CS-131	A01

CHANGE by IEC | DATE Friday, December 10, 2010 | SHEET 44 of 61

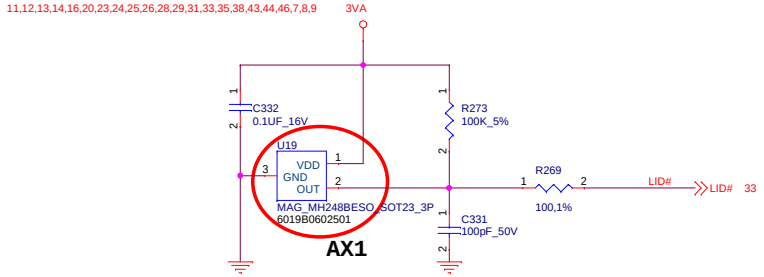
AX2



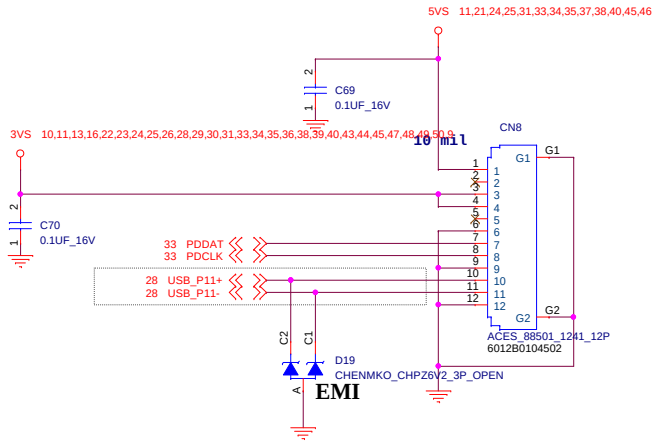
PWS + LED CNN.



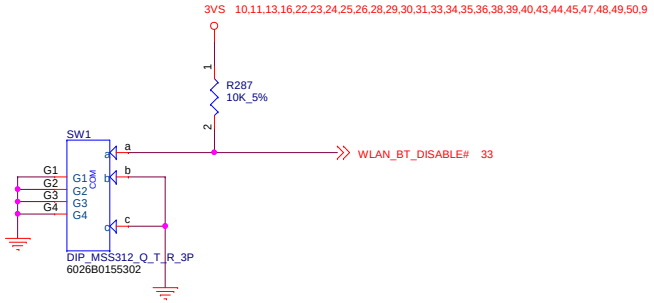
HALL Switch



GP + FP CNN.

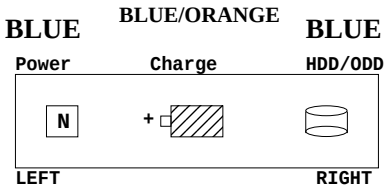


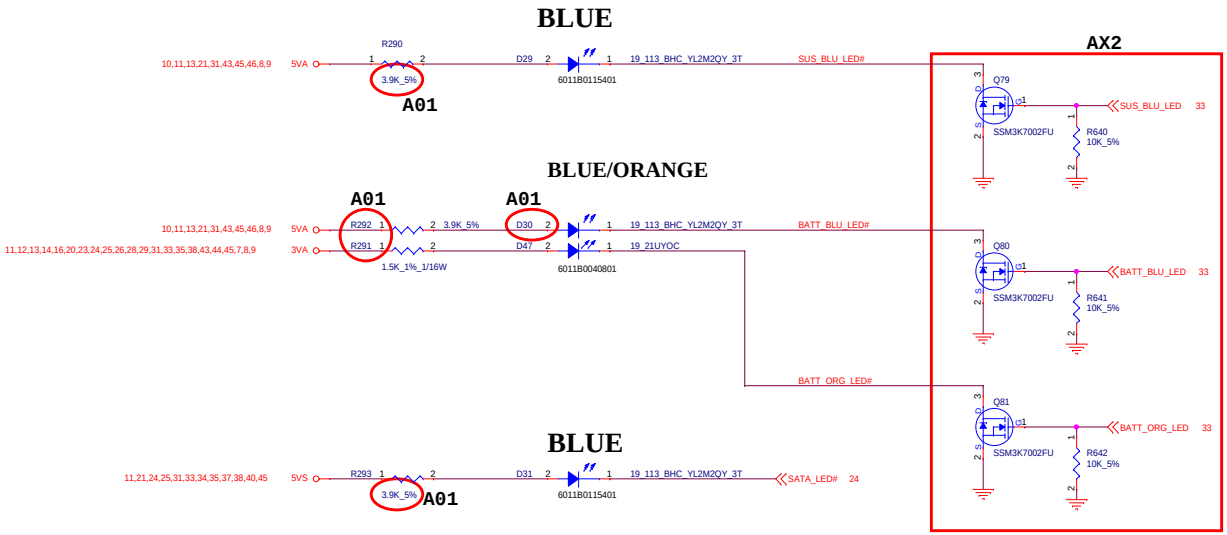
(W-LAN, BT) sliding switch

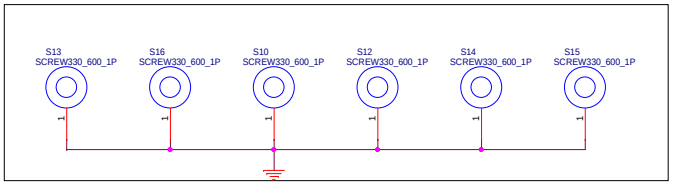


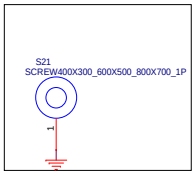
INVENTEC			
TITLE: Aegis PSW/LID/ GP/FP/SL SW			
SIZE: Custom	CODE ES:	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 45 of 61	

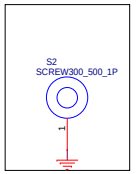
LED Seat

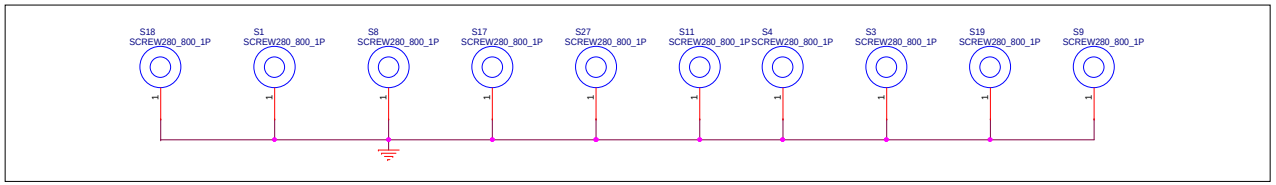




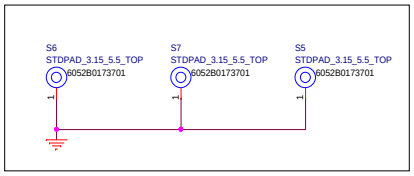




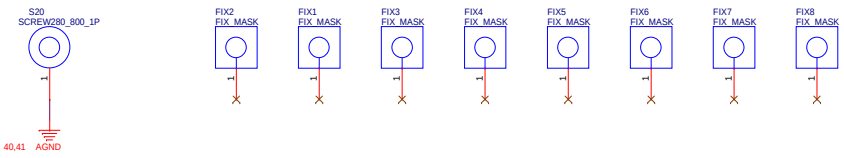


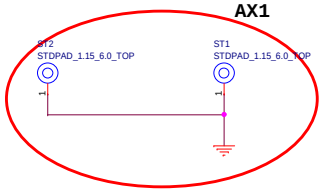


For USB B to B NUT

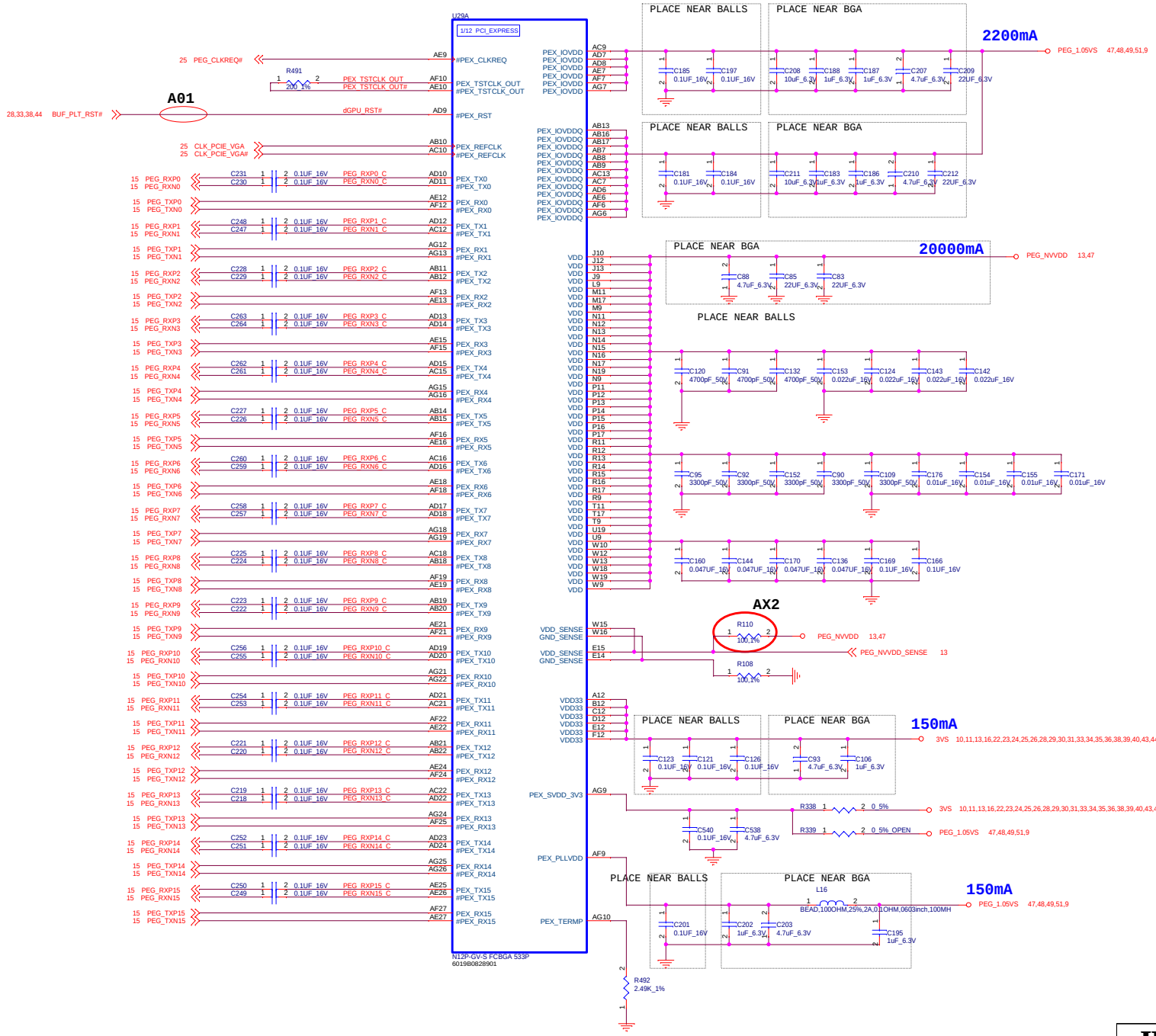


SCREW

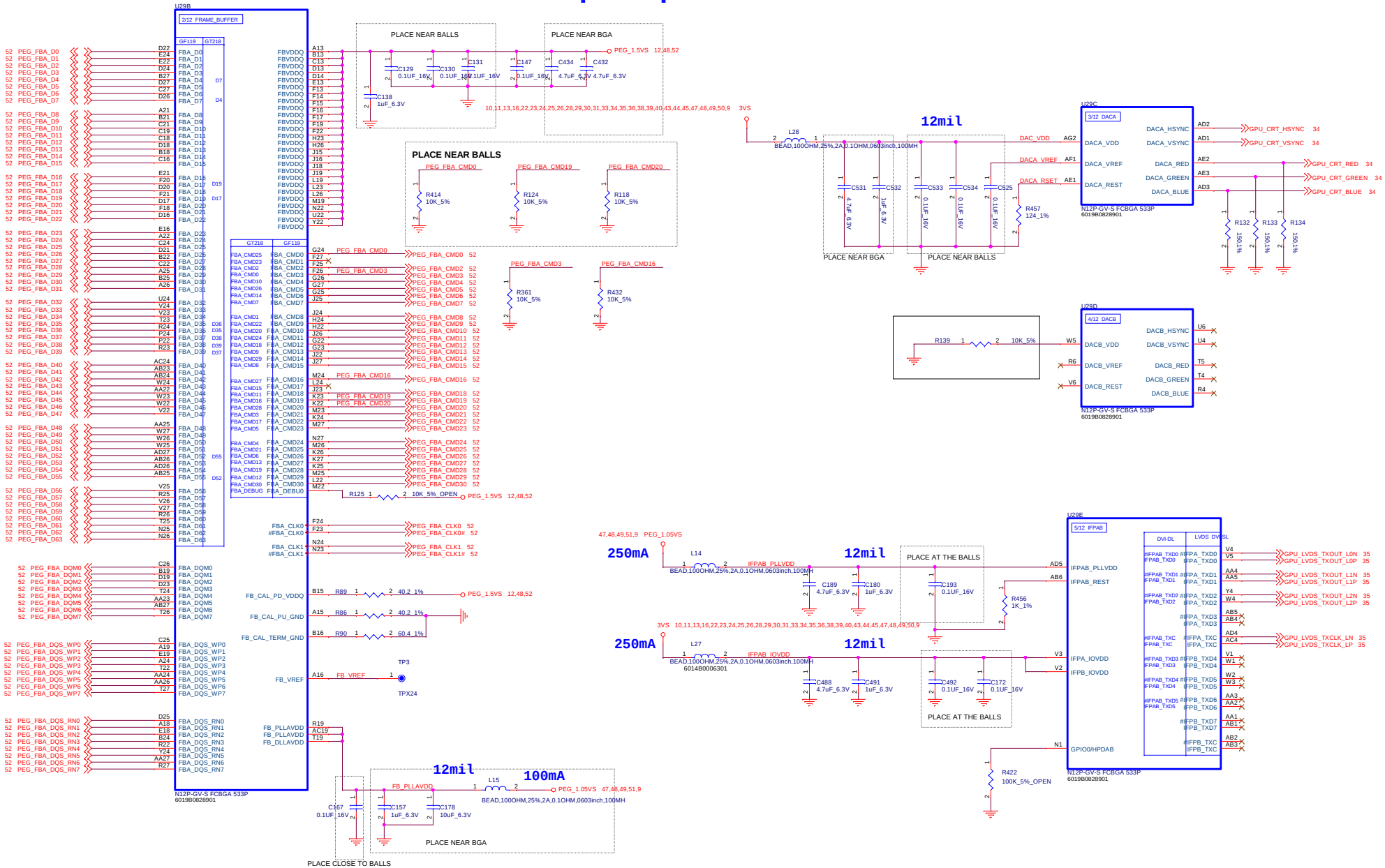




INVENTEC			
TITLE: Aegis LED / SCREW			
SIZE: C	CODE: ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 46 of 61	



INVENTEC			
TITLE	Aegis		
	N12P-GV (1/5)		
SIZE C	CODE ES	DOC.NUMBER CS-131	REV A01
CHANGE by IEC	DATE Friday, December 10, 2010	SHEET 47 of 61	



CHANGE by	IEC
DATE	Friday, December 10, 2010

INVENTEC

TITLE: Aegis
N12P-GV (2/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

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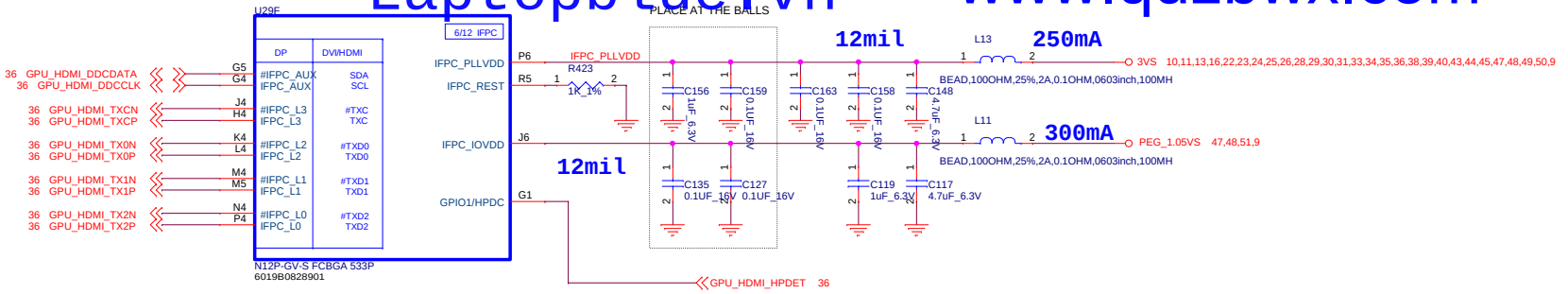
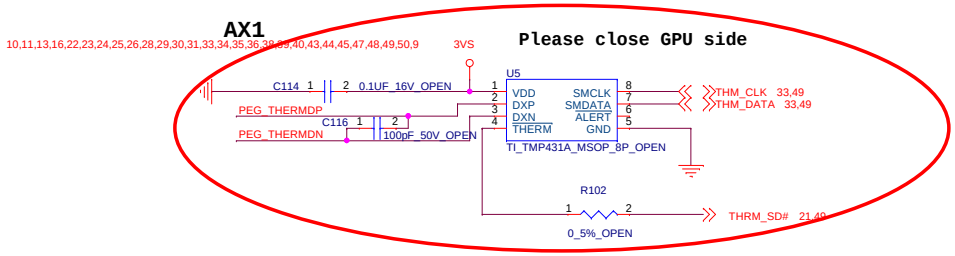
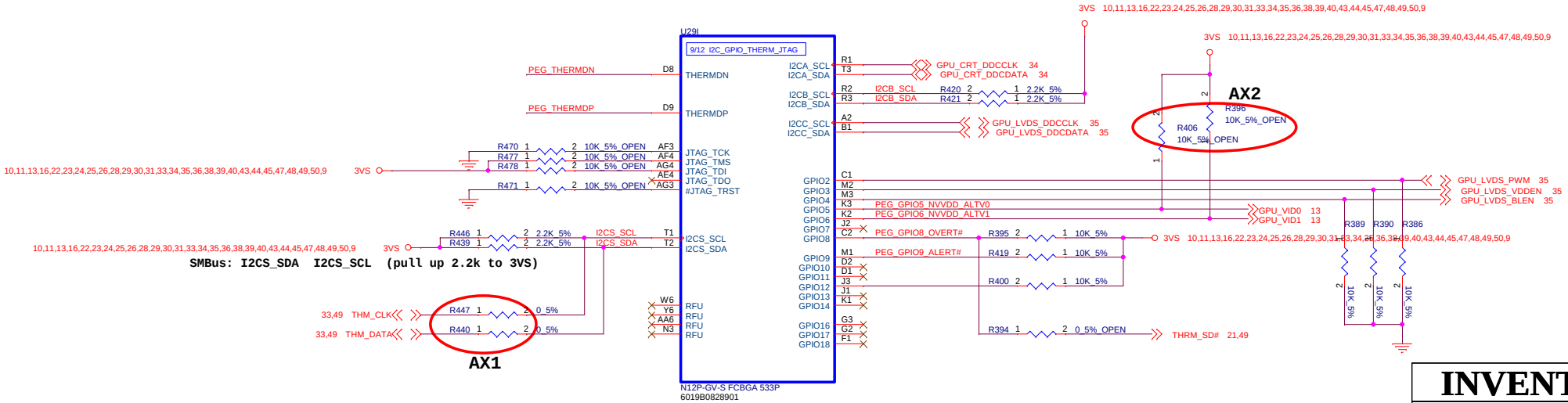
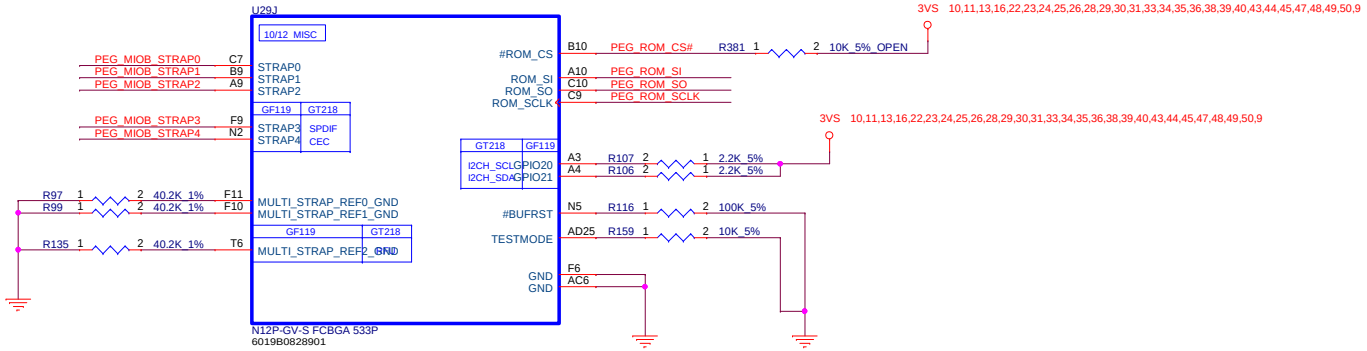


GPU Thermal sensor

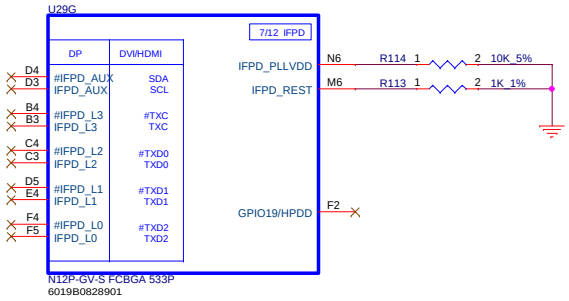


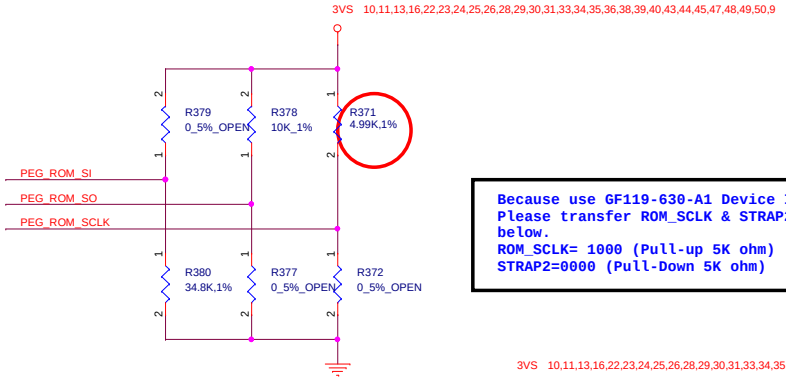


INVENTEC			
TITLE: Aegis N12P-GV (3/5)			
SIZE: Custom	CODE ES	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 49 of 61	

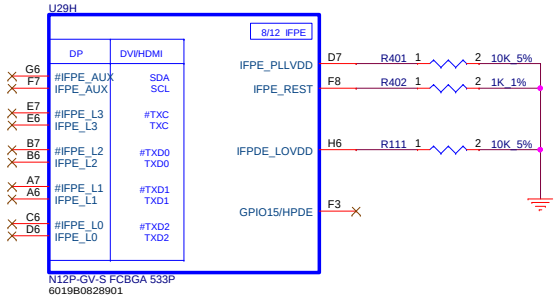


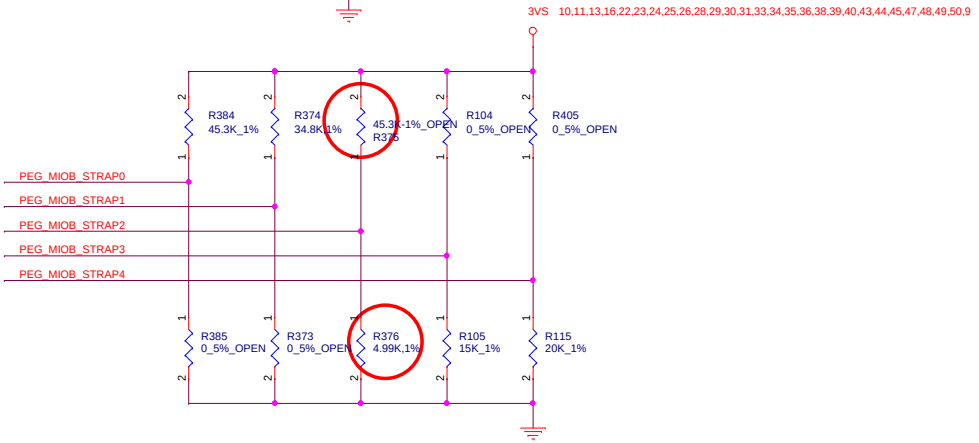
ROM_SO	1	0	0	1	PU 10K
ROM_SCLK	1	0	0	0	PU 5K
ROM_SI	0	1	1	0	PD 35K
STRAP0	1	1	1	1	PU 45K
STRAP1	1	1	1	0	PU 35K
STRAP2	0	0	0	0	PD 5K
STRAP3	0	0	1	0	PD 15K
STRAP4	0	0	1	1	PD 20K





Because use GF119-630-A1 Device ID (0x1050). Please transfer ROM_SCLK & STRAP2 setting as below.
ROM_SCLK= 1000 (Pull-up 5K ohm)
STRAP2=0000 (Pull-Down 5K ohm)



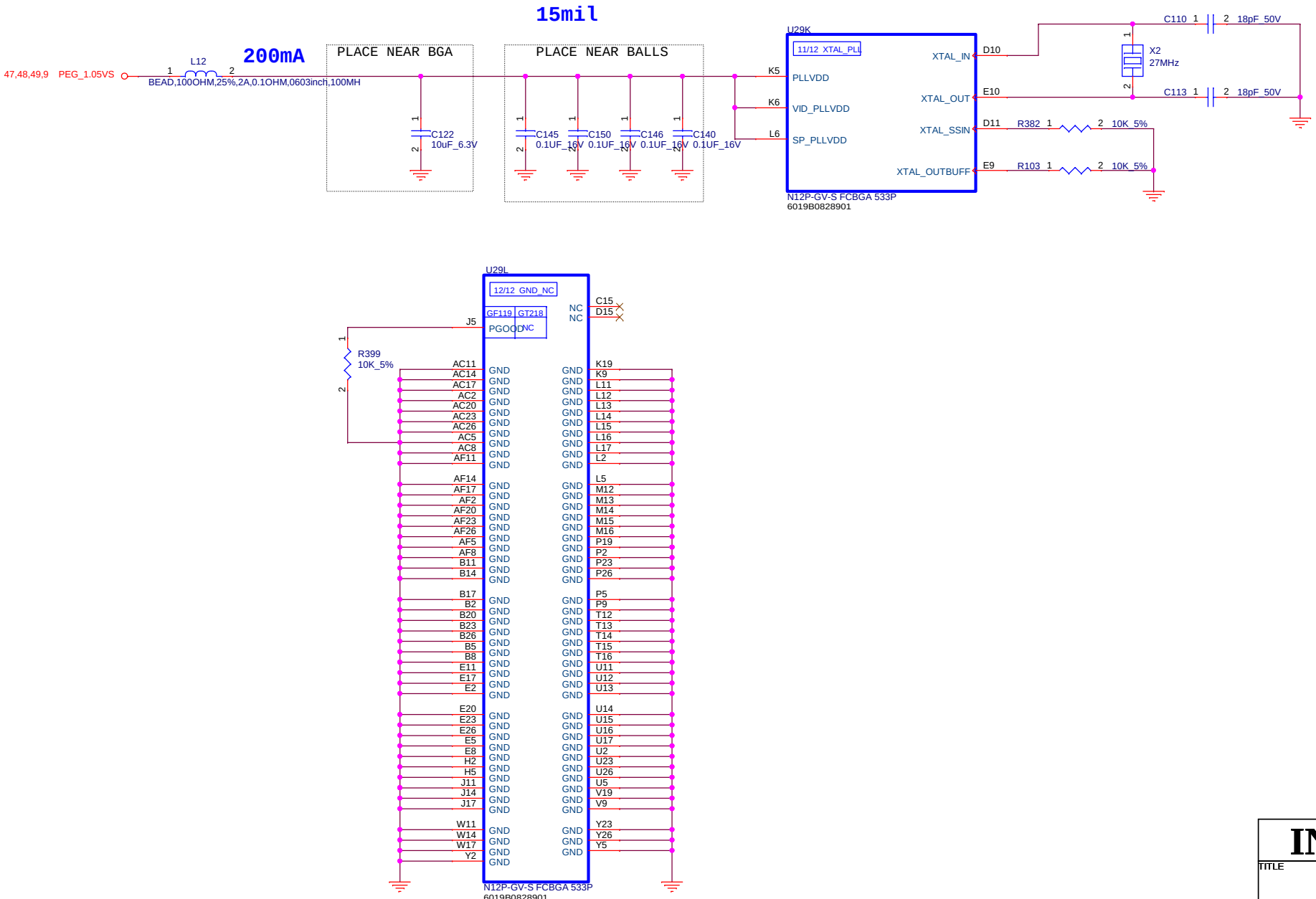


INVENTEC

TITLE: Aegis
N12P-GV (4/5)

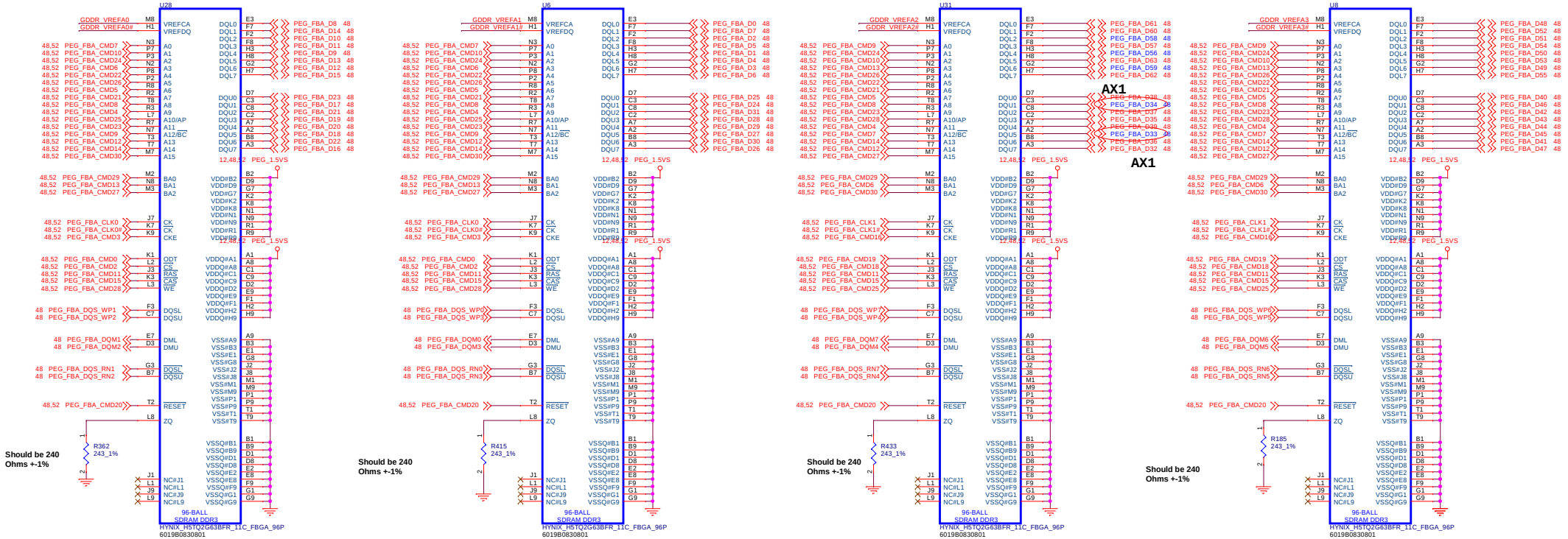
SIZE	CODE	DOC.NUMBER	REV
Custom	ES	CS-131	A01

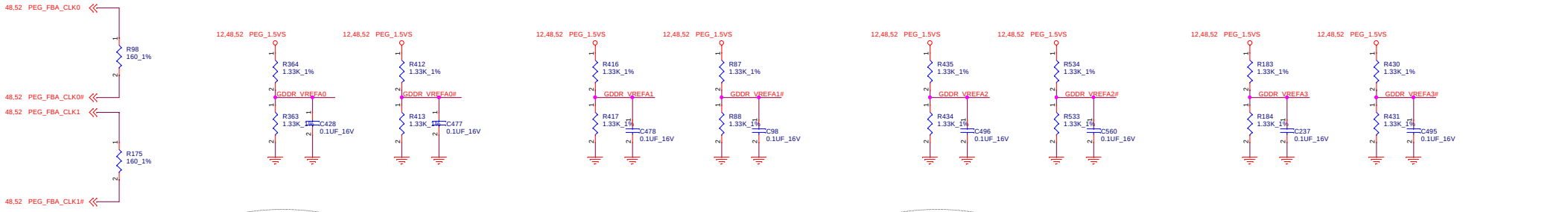
CHANGE by IEC | DATE Friday, December 10, 2010 | SHEET 50 of 61

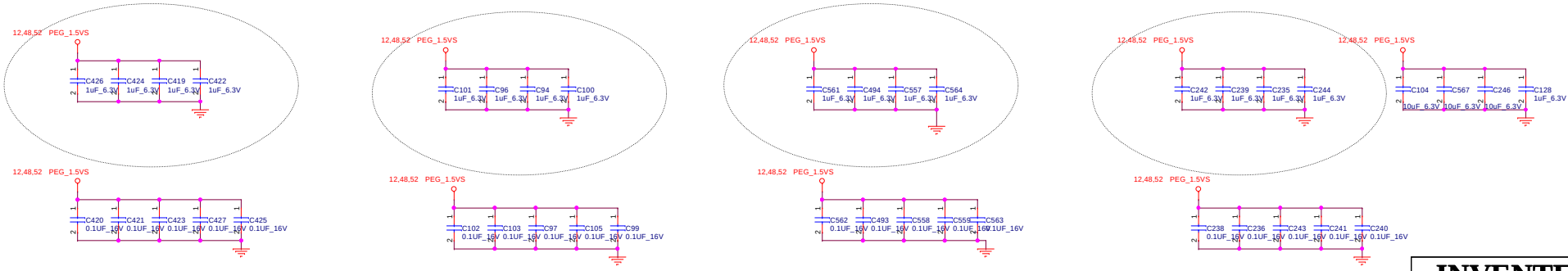


INVENTEC			
TITLE: Aegis N12P-GV (5/5)			
SIZE: B	CODE: ES	DOC.NUMBER: D-CS-1310A22767-0-ALG	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 51 of 61	

SWAP PINS







INVENTEC

TITLE	Aegis		
	VRAM		
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	A01
CHANGE by	IEC	DATE	Friday, December 10, 2010
		SHEET	52 of 61

Aegis

USB Board

2010.12.10 A01 Build

DATE	CHANGE NO.	REV
Thursday, Jun. 26 , 2008	3'rd issue	A01
Monday, May 26 , 2008	Second issue	AX1
Thur., April 17 , 2008	First issue	A01

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

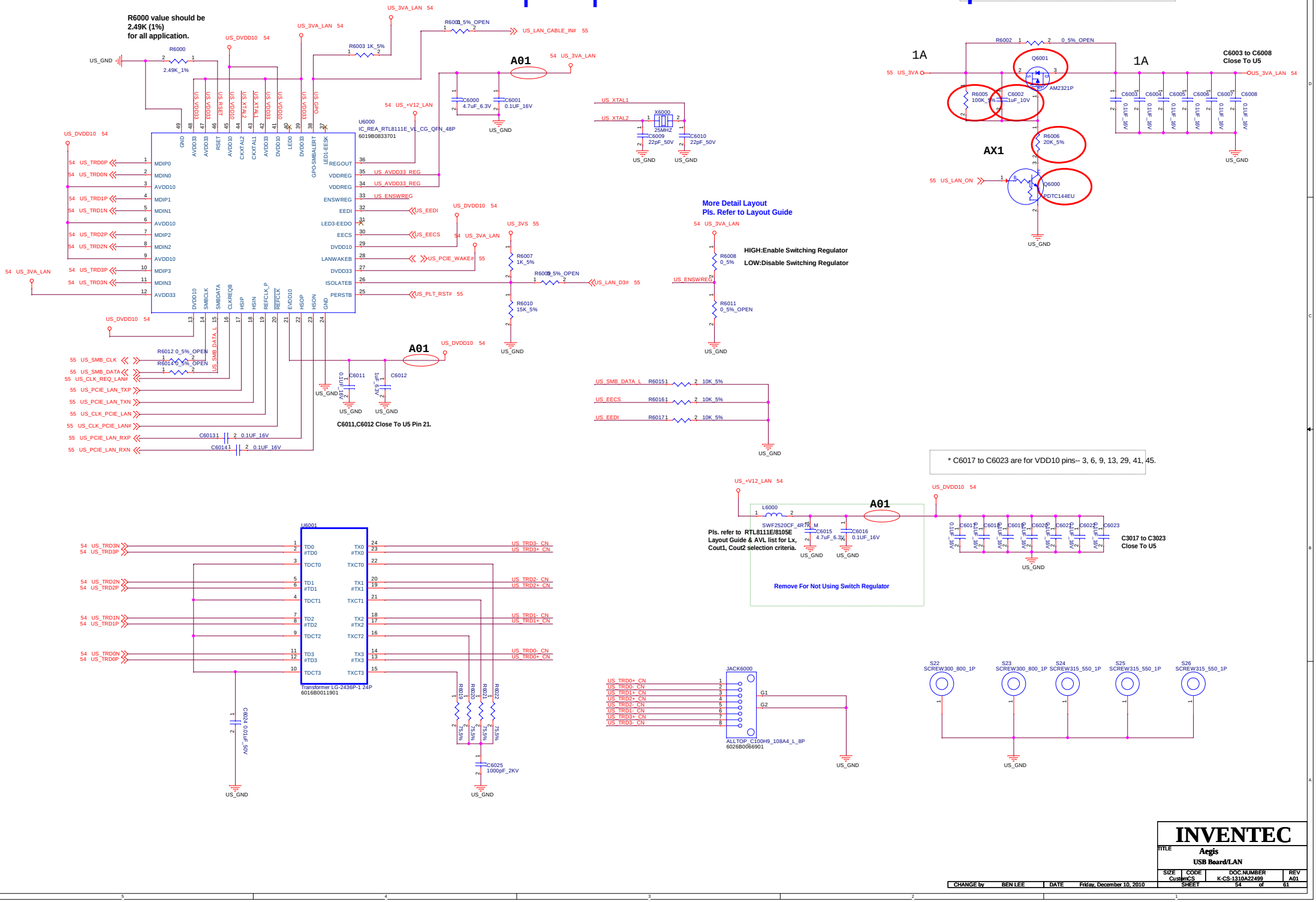
P/N XXXXXXXXXXX

INVENTEC

TITLE: USB Board

SIZE	CODE	DOC.NUMBER	REV
C	CS	K-CS-1310A22219-ALG	A01

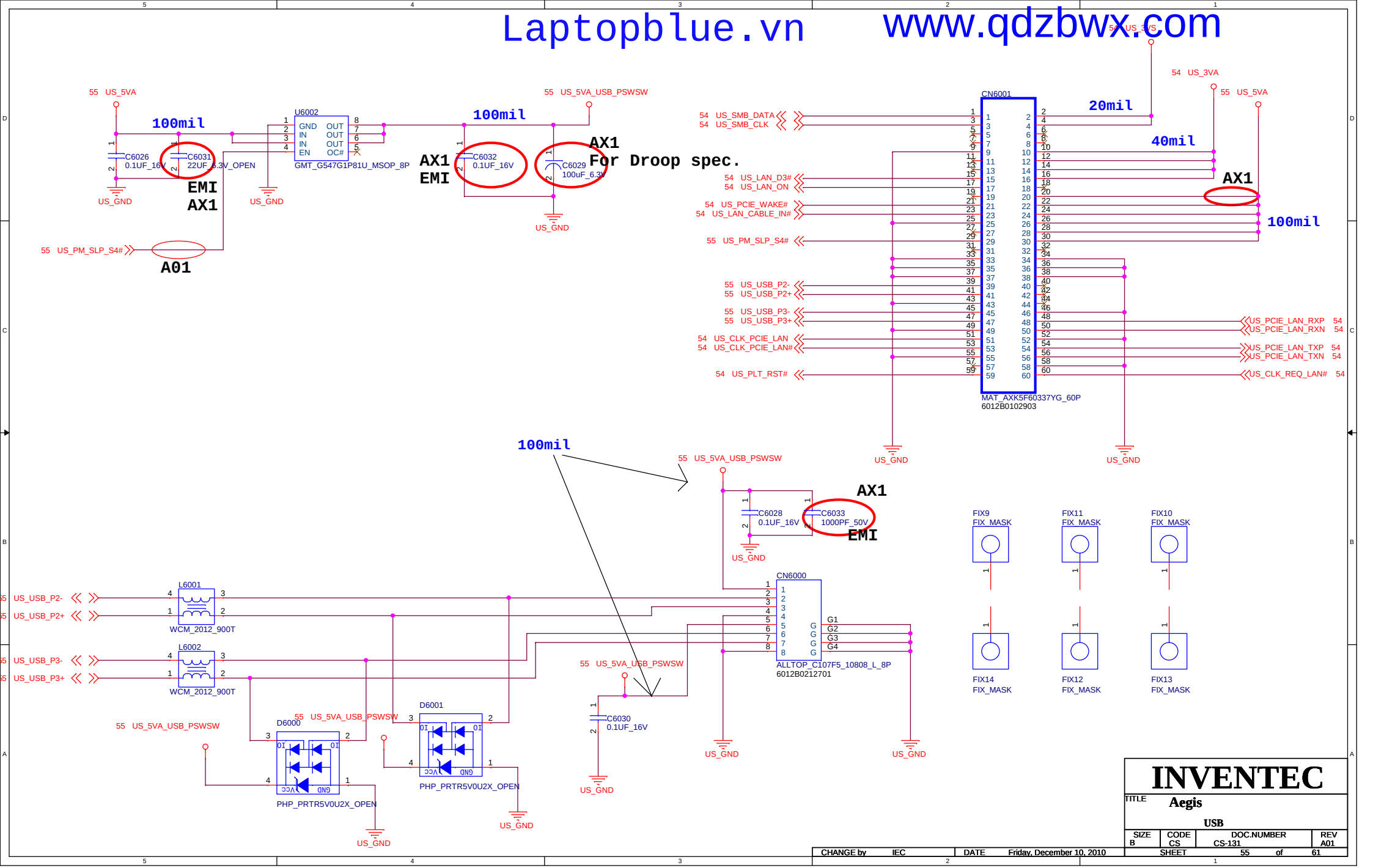
SHEET 53 of 61



CHANGE by	BEN LEE	DATE	Friday, December 10, 2010

INVENTEC

TITLE	Aegis USB Board/LAN		
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	K-CS-1310A22499	A01
		SHEET 54 of 61	



INVENTEC			
TITLE: Aegis			
USB			
SIZE: B	CODE: CS	DOC.NUMBER: CS-131	REV: A01
CHANGE by: IEC	DATE: Friday, December 10, 2010	SHEET: 55 of 61	

Aegis

PWR_SW BOARD

A01 Build

2010.12.10

DATE	CHANGE NO.	REV
		A01

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

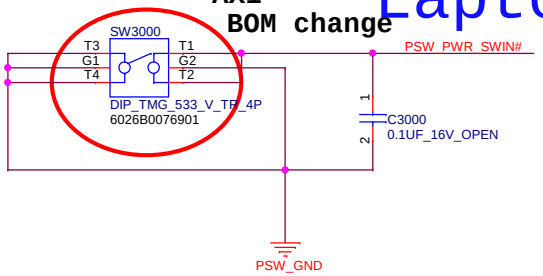
INVENTEC

TITLE PWR_SW BOARD

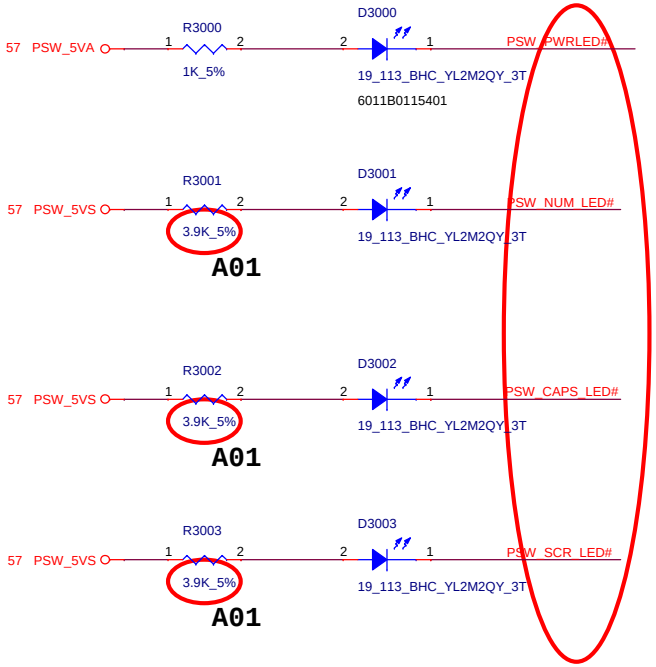
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	K-CS-1310A22219-ALG	A01

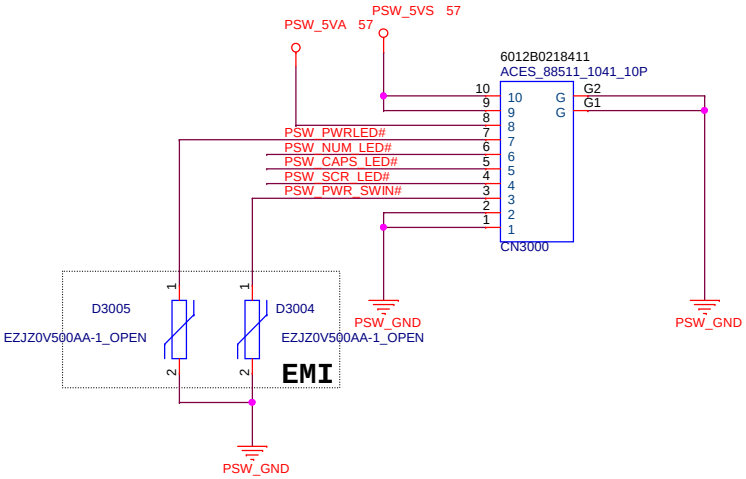
SHEET 56 of 61

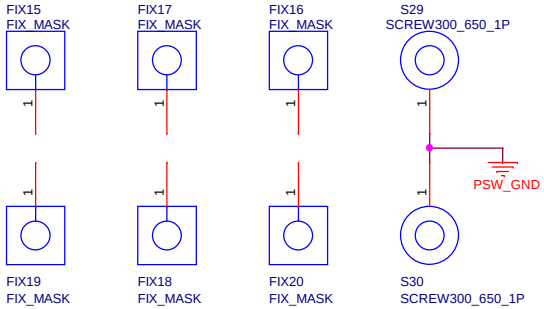
AX1
BOM change



AX1







INVENTEC			
TITLE Aegis Power Switch			
SIZE B	CODE CS	DOC.NUMBER K-CS-1310A22219-ALG	REV A01
CHANGE by BEN LEE	DATE Friday, December 10, 2010	SHEET 57 of 61	

Aegis

Finger Print board

2010.12.10 A01 Build

Friday, December 10, 2010		
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

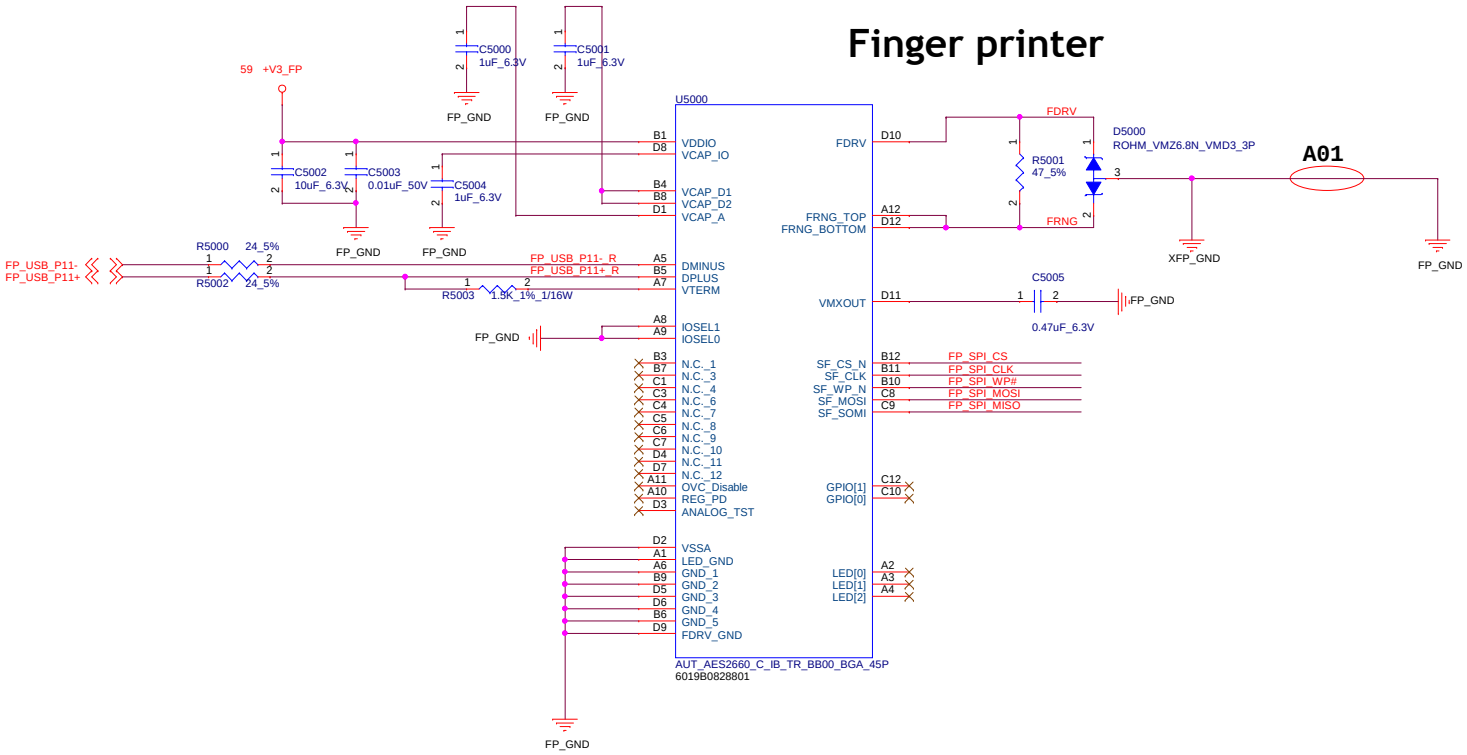
INVENTEC

TITLE Finger Print board

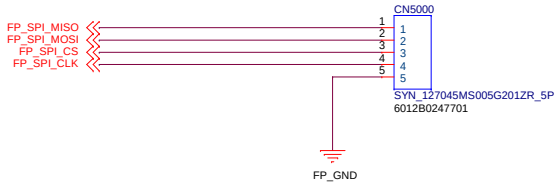
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	K-CS-1310A22499	A01

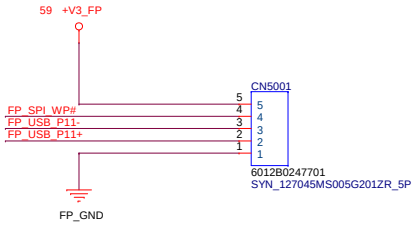
SHEET 58 of 61

Finger printer



TO GP PIN HEADER





INVENTEC			
TITLE: Aegis Finger Print			
SIZE: Custom	CODE: CS	DOC.NUMBER: K-CS-1310A22499	REV: A01
CHANGE by: BEN LEE	DATE: Friday, December 10, 2010	SHEET: 59 of 61	

Aegis

GP board

2010.12.10

A01 Build

Friday, December 10, 2010		
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:

FILE NAME: XXXX-XXXXXX-XX

P/N XXXXXXXXXXX

INVENTEC

TITLE

GP Board

SIZE	CODE	DOC NUMBER	REV
Custom	CS	K-CS-1310A22499	A01

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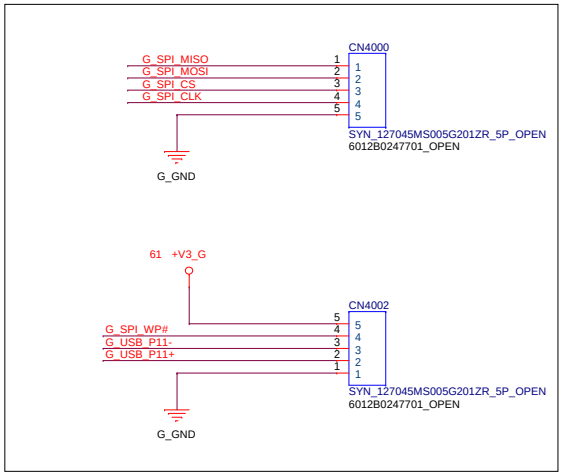
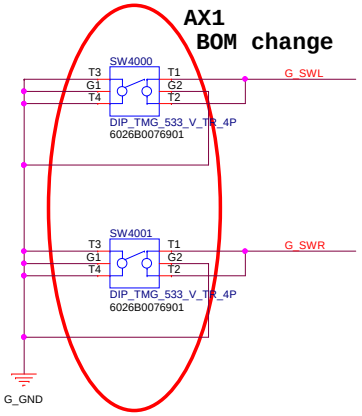
TO FP PIN HEADER

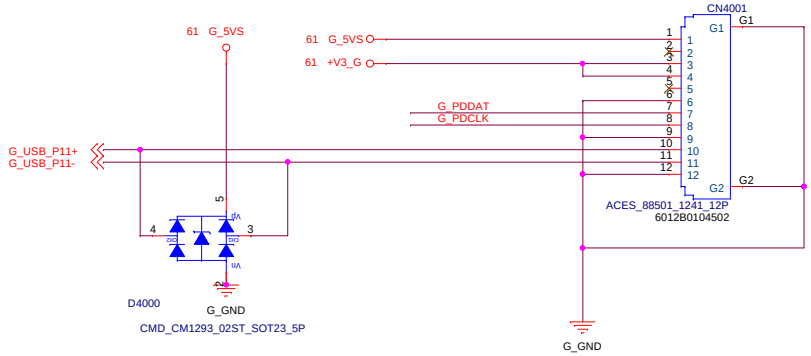


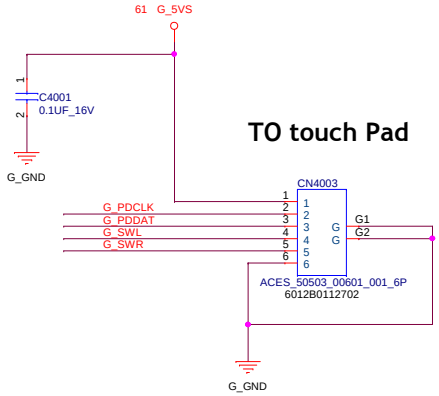
GP Button

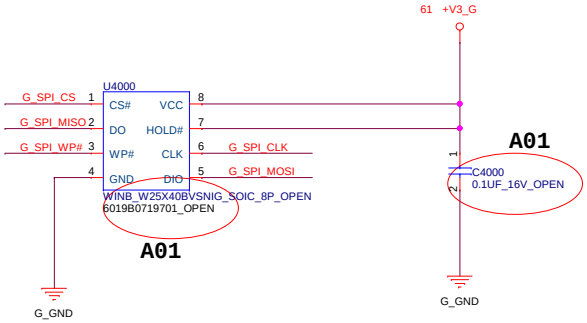
AX1
BOM change



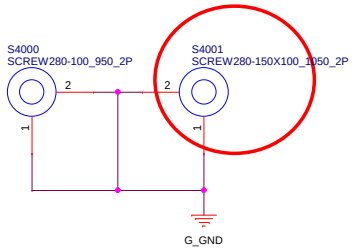
TO MB







AX2



INVENTEC			
TITLE: Aegis USB Board/GP			
SIZE: Custom	CODE: CS	DOC.NUMBER: K-CS-1310A22499	REV: A01
CHANGE by: BEN LEE	DATE: Friday, December 10, 2010	SHEET: 61 of 61	