

MODEL NAME : *PAP00*
PCB NO : *LA-6961P (DA*****)*
BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom (Huron River)

Sandy Bridge (BGA1023) + Cougar Point (SFF)

DISCRETE VGA N12P-GS (optimus)

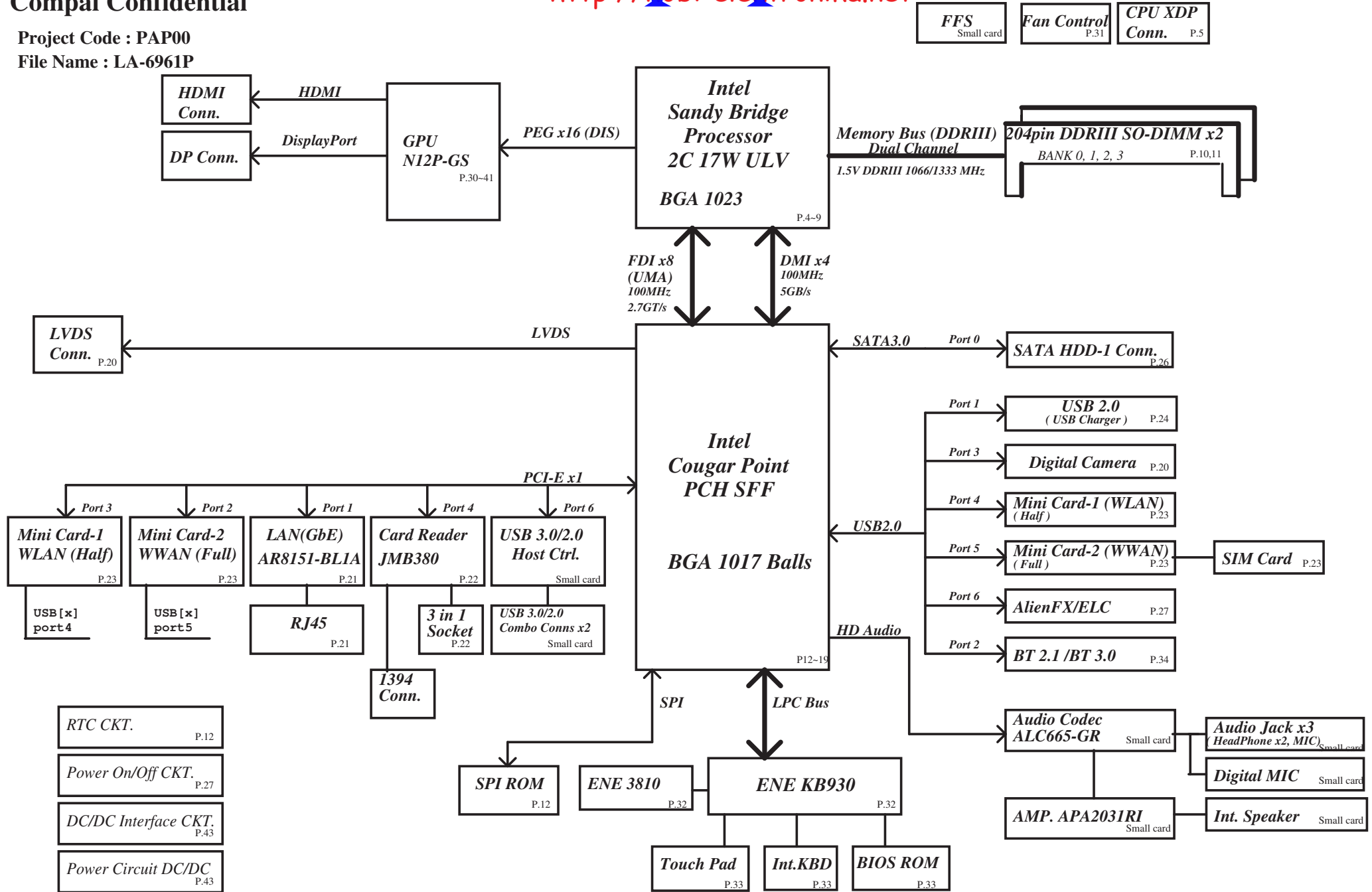
2010-11-29

Rev: 0.4

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				Rev	0.4

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Project Code : PAP00
File Name : LA-6961P



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN)
6	ELC
7	None
8	None
9	None
10	None
11	None
12	None
13	None

Link


CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

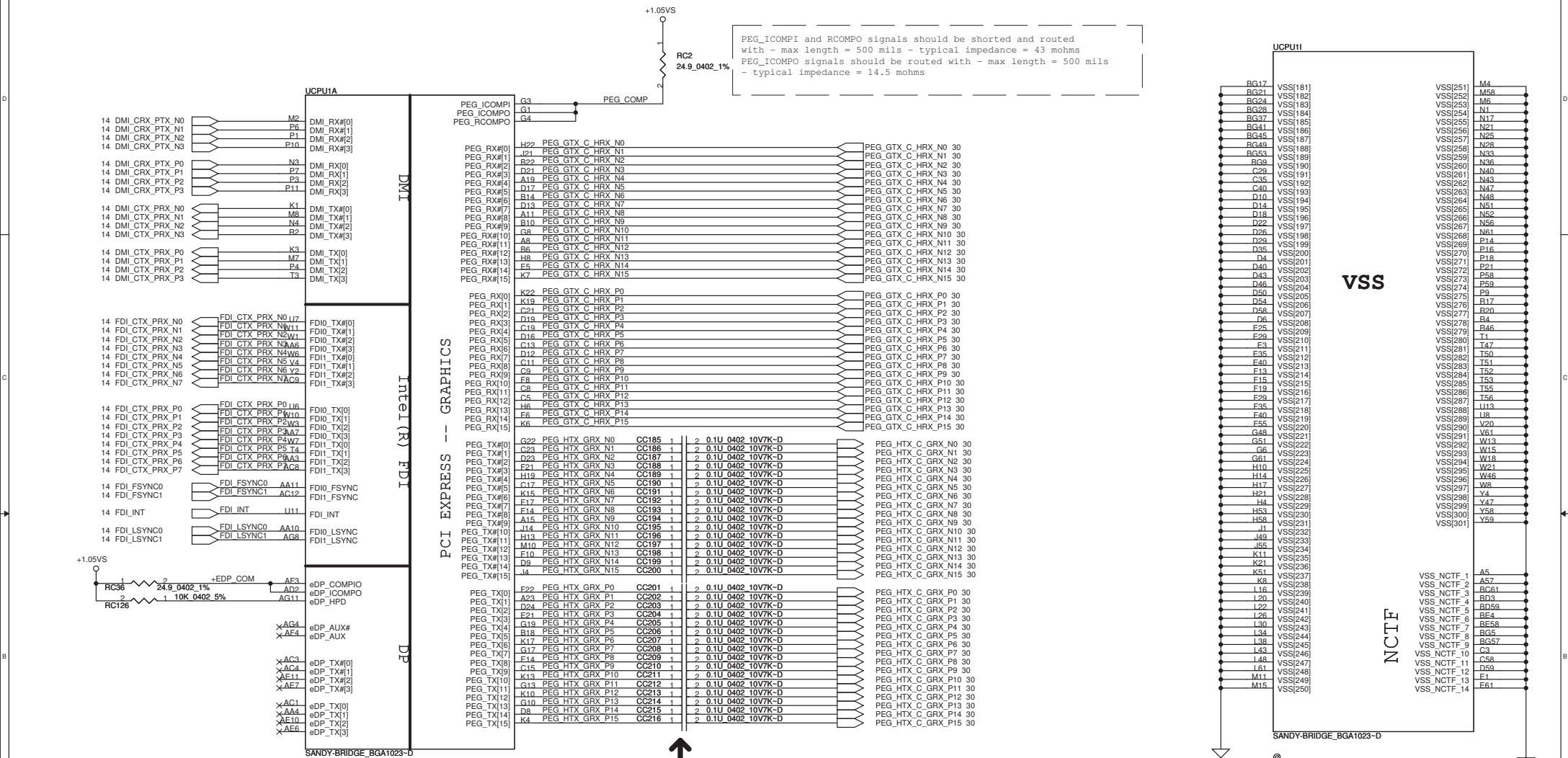
Symbol Note :

 : means Digital Ground

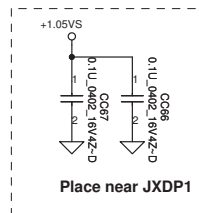
 : means Analog Ground

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

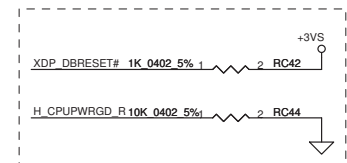
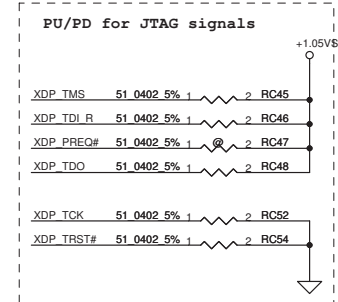
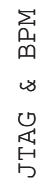
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Title <i>Notes List</i>					
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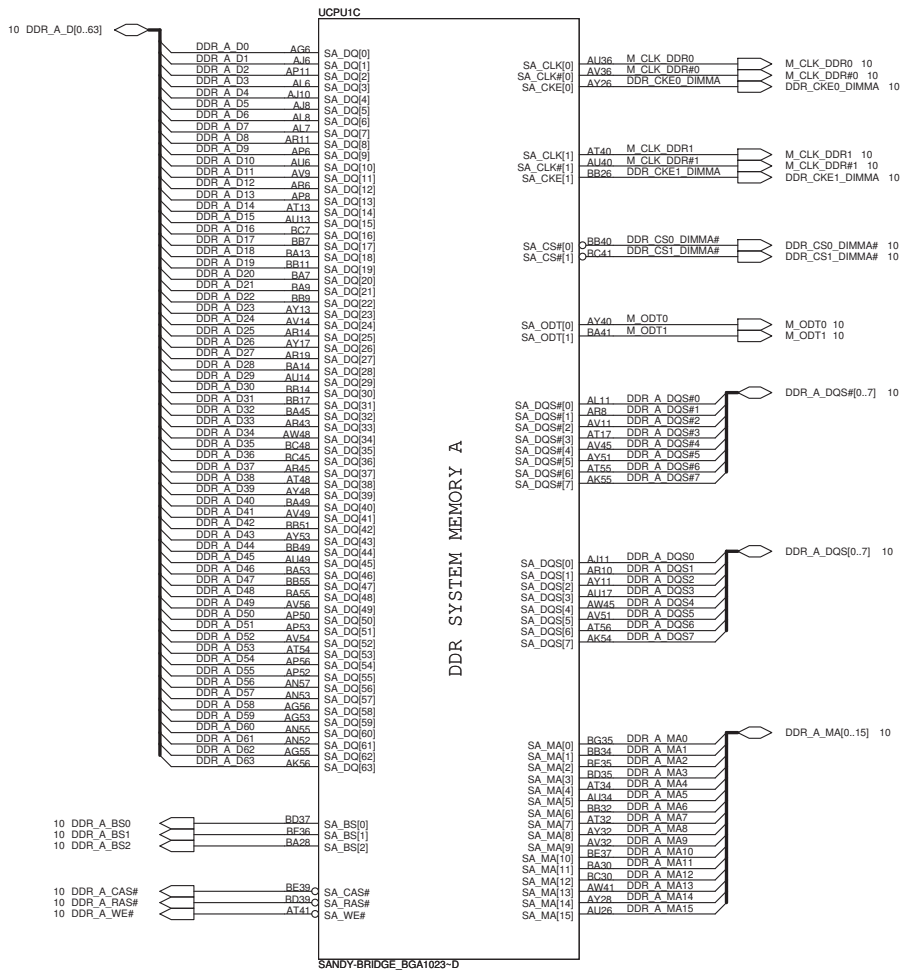
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)



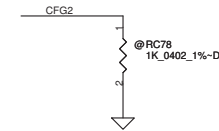
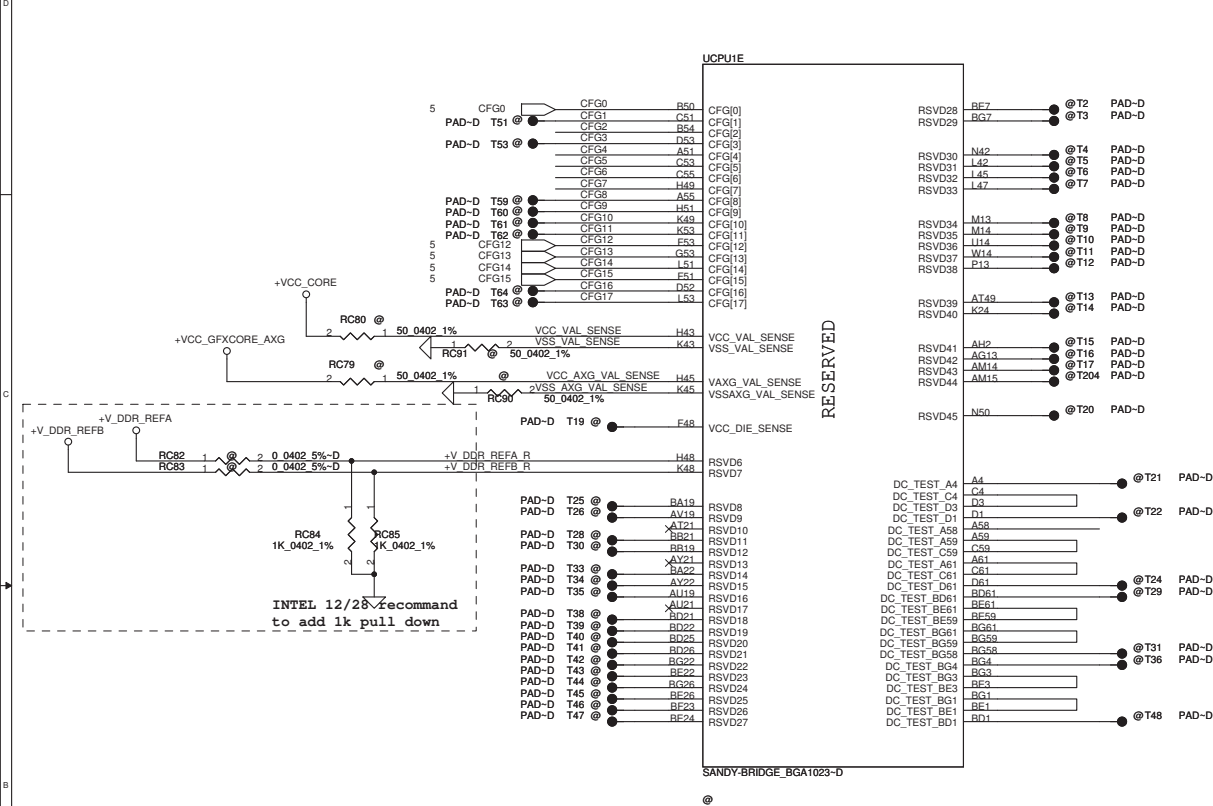
PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.



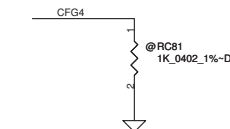
Security Classification		Compal Secret Data		Compal Electronics, Inc. PROCESSOR(2/6) PM,XDP,CLK	
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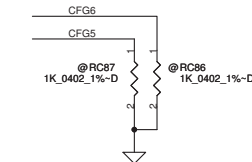
CFG Straps for Processor



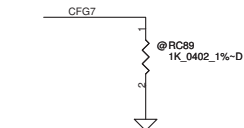
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



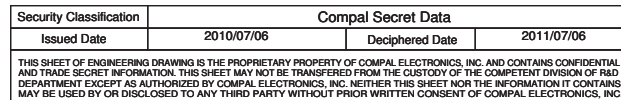
Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

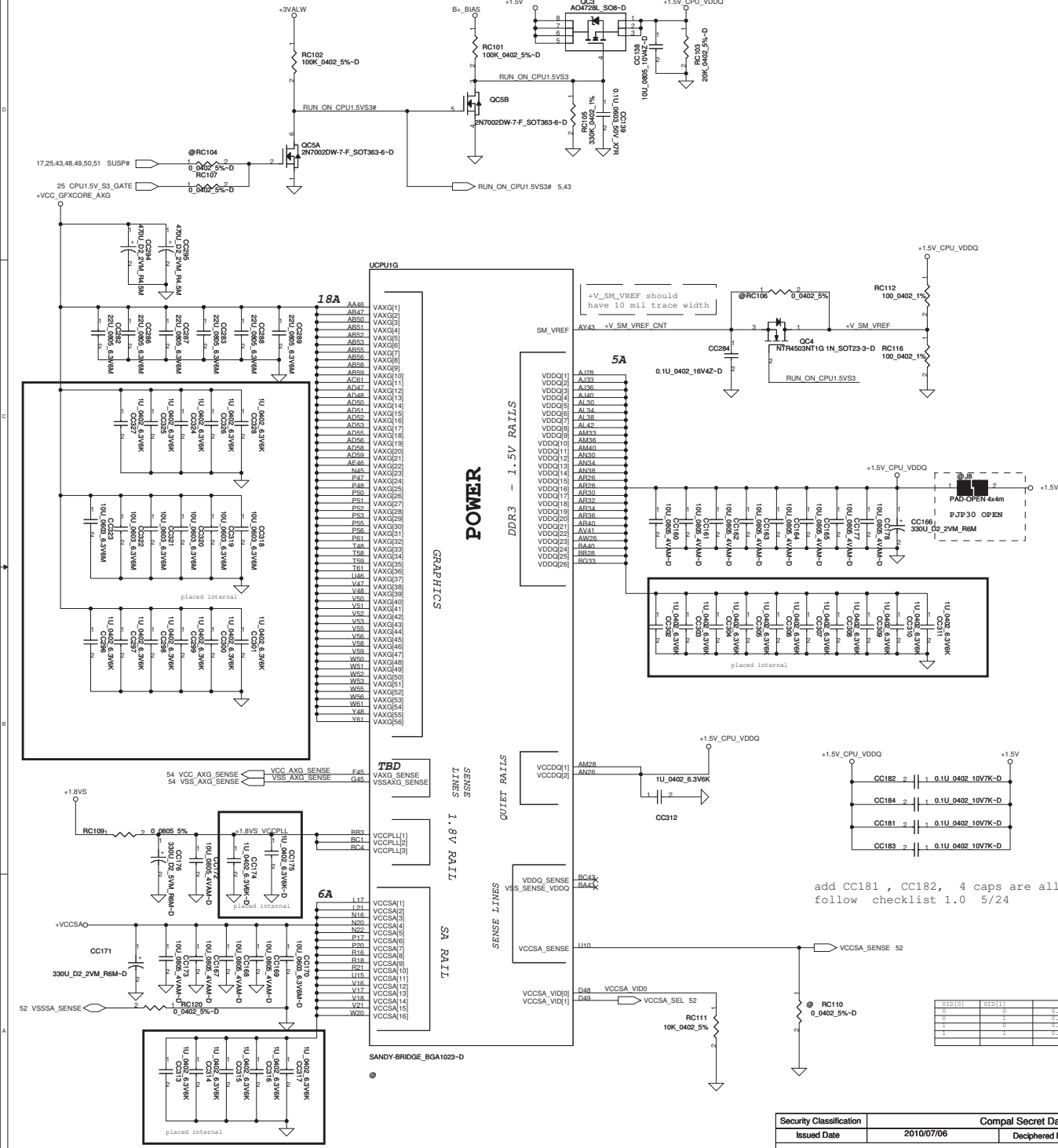


PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	★1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



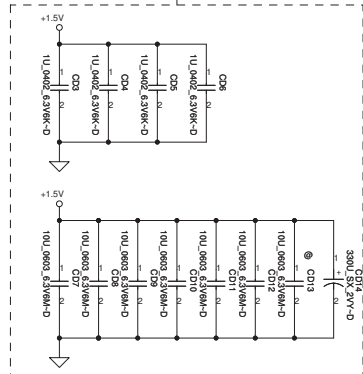


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Title				PROCESSOR(6/6) PWR,VSS					
Size				Document Number					
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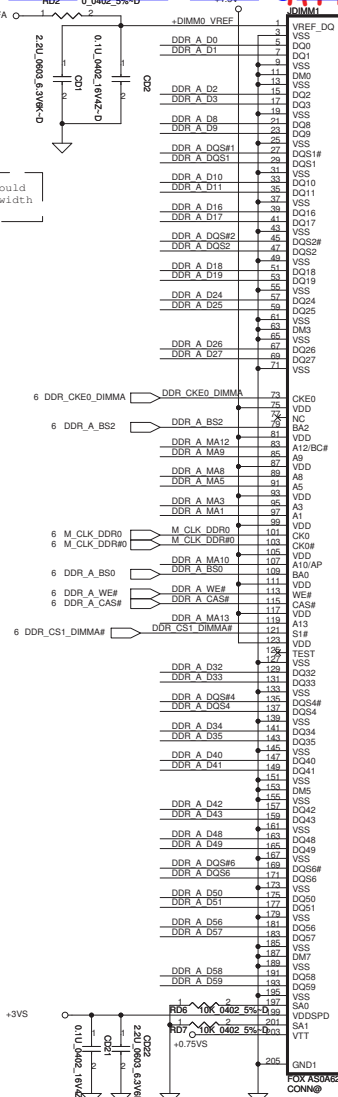
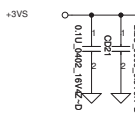
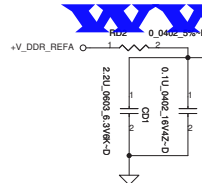
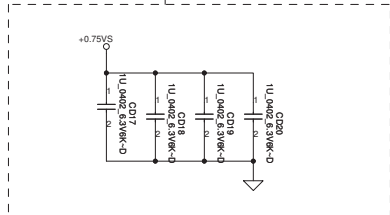
6 DDR_A_DQS[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_D[0..63]
6 DDR_A_MA[0..15]

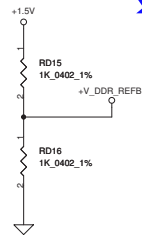
Layout Note:
Place near JDIMM1

All VREF traces should
have 10 mil trace width

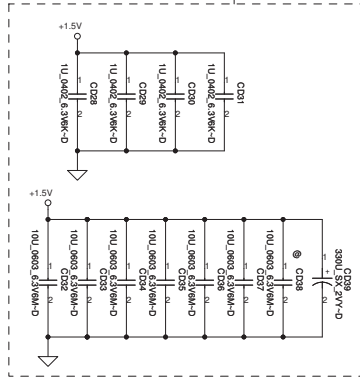
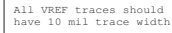


Layout Note:
Place near JDIMM1.203,204

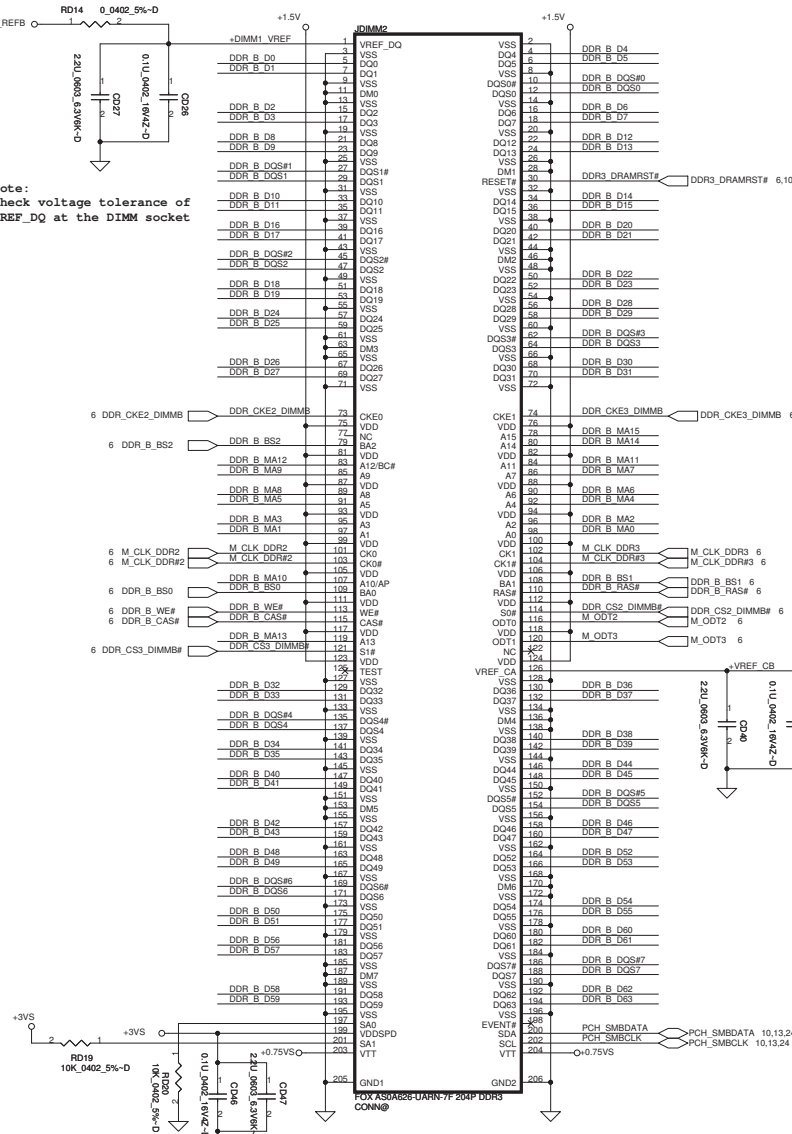
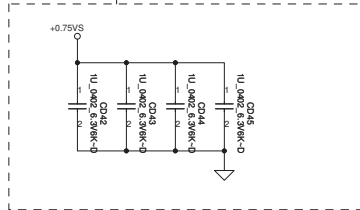




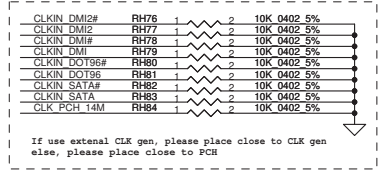
Layout Note:
Place near JDIMMB



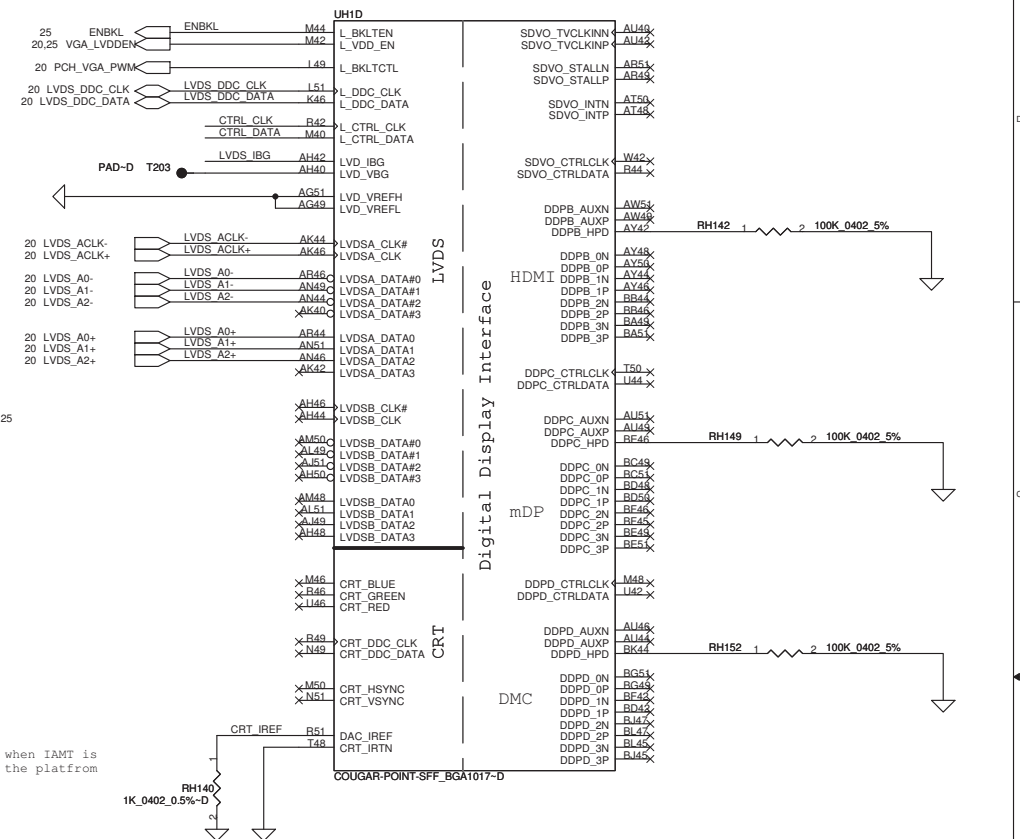
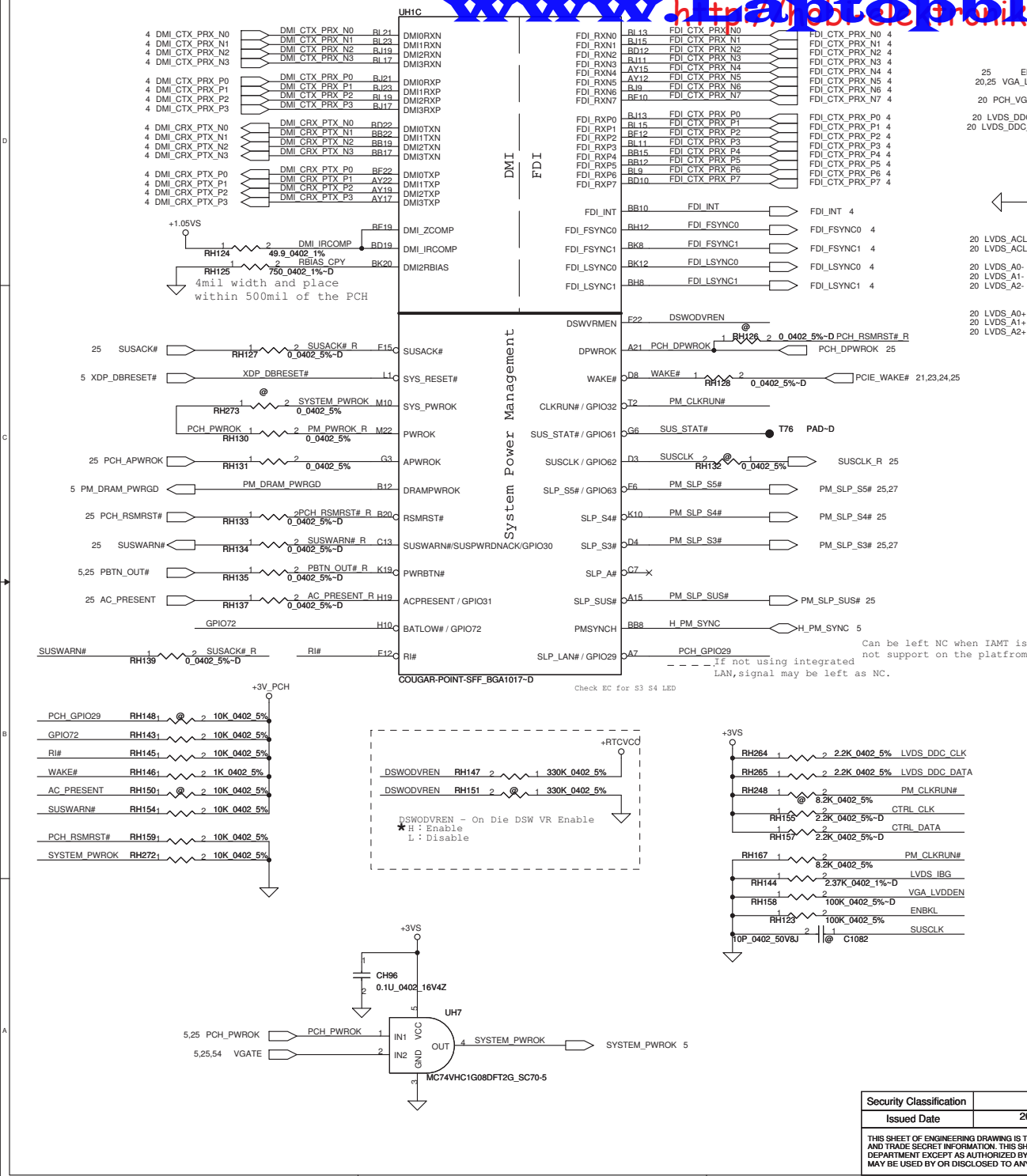
Layout Note:
Place near JDIMMB.203,204



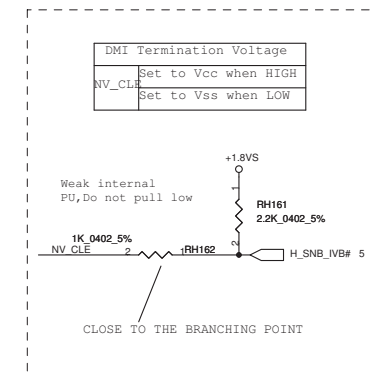
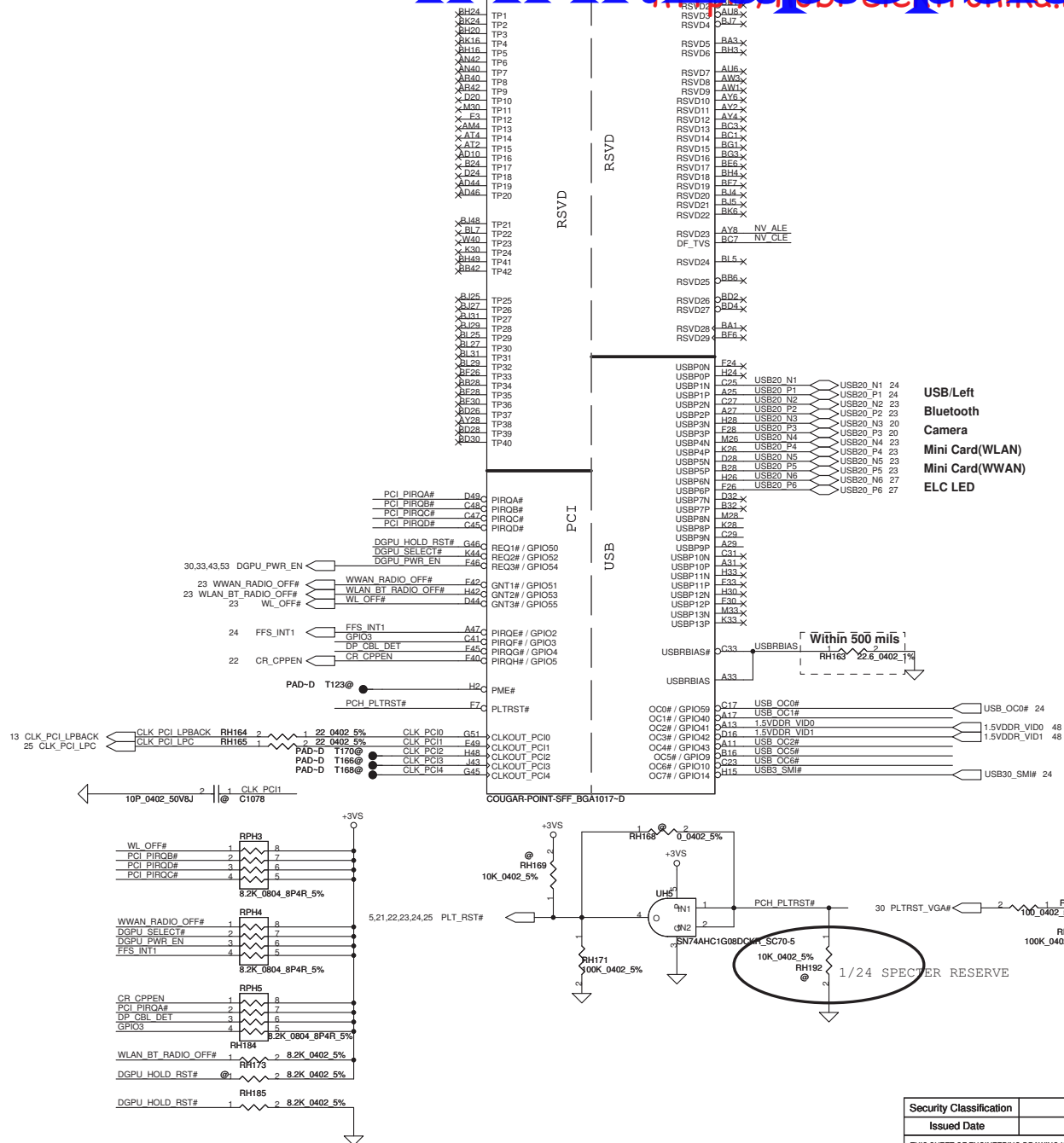
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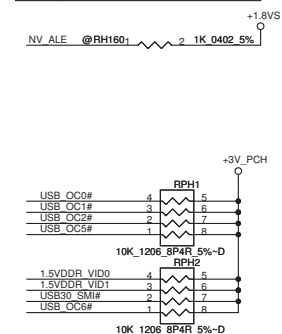
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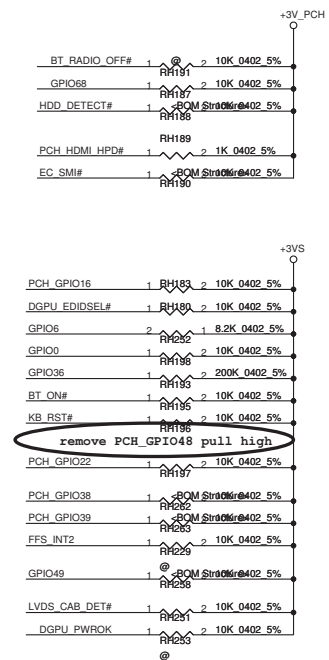
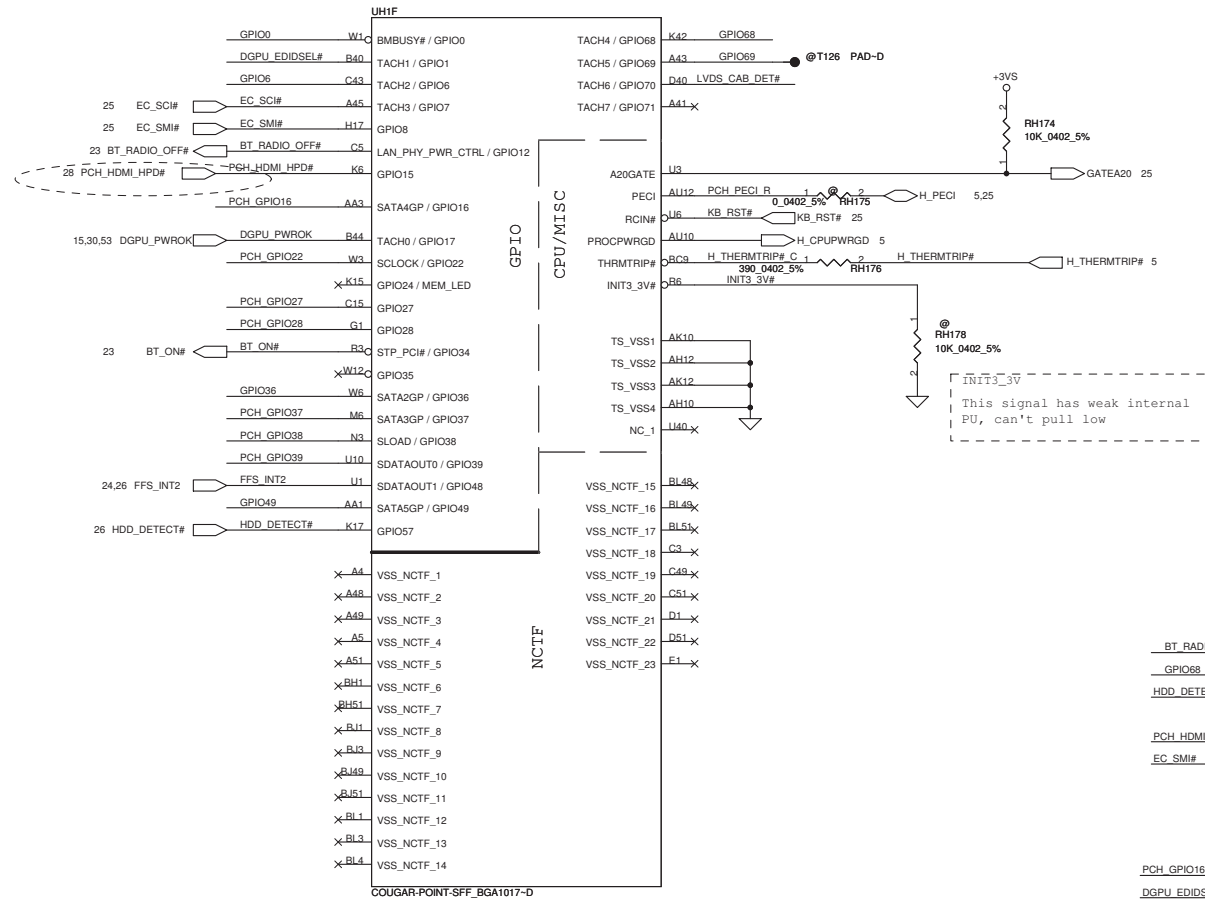
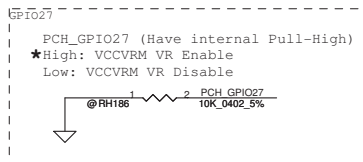
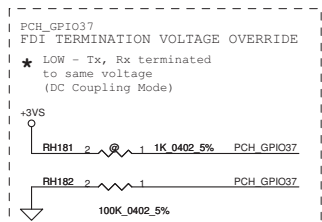
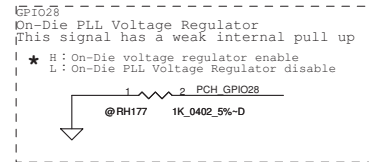
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Intel Anti-Theft Techonlogy	
NV_ALR	High=Enabled
	Low=Disable(floating) ★



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				PCH (4/8) PCI, USB, NVRAM	
				Size Document Number LA-6961P	
Date: Tuesday, January 25, 2011				Sheet 15 of 54	

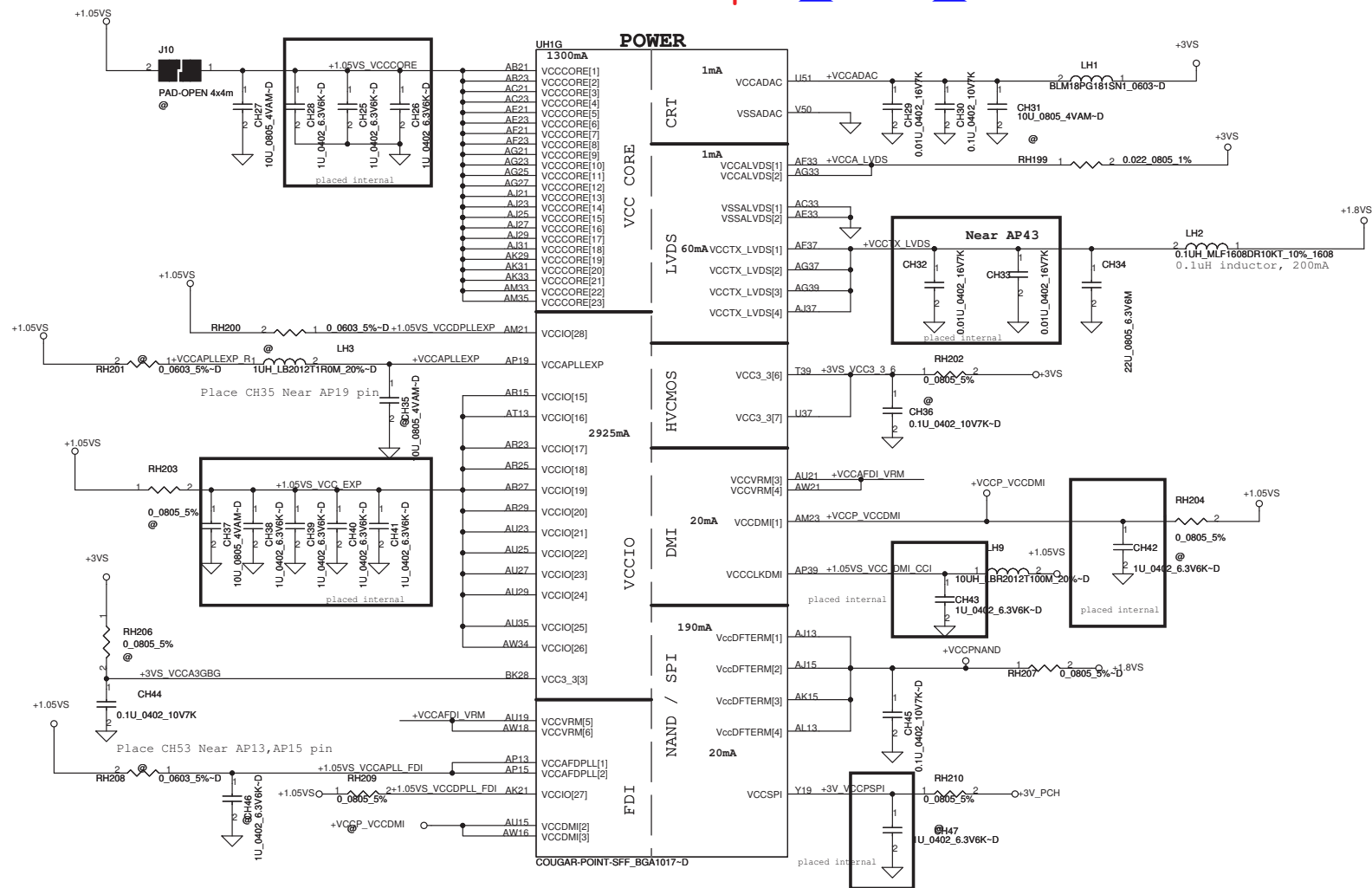


```
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5
```

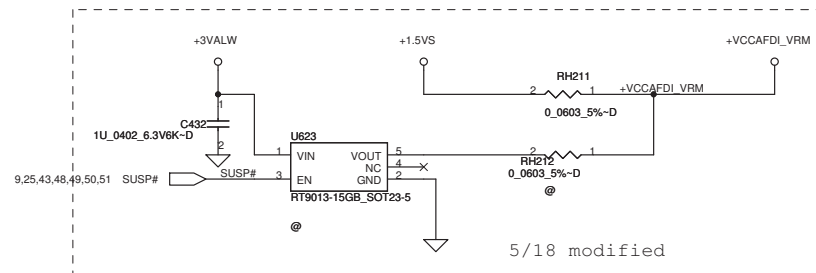
add RH185, RH229, RH251
5/25

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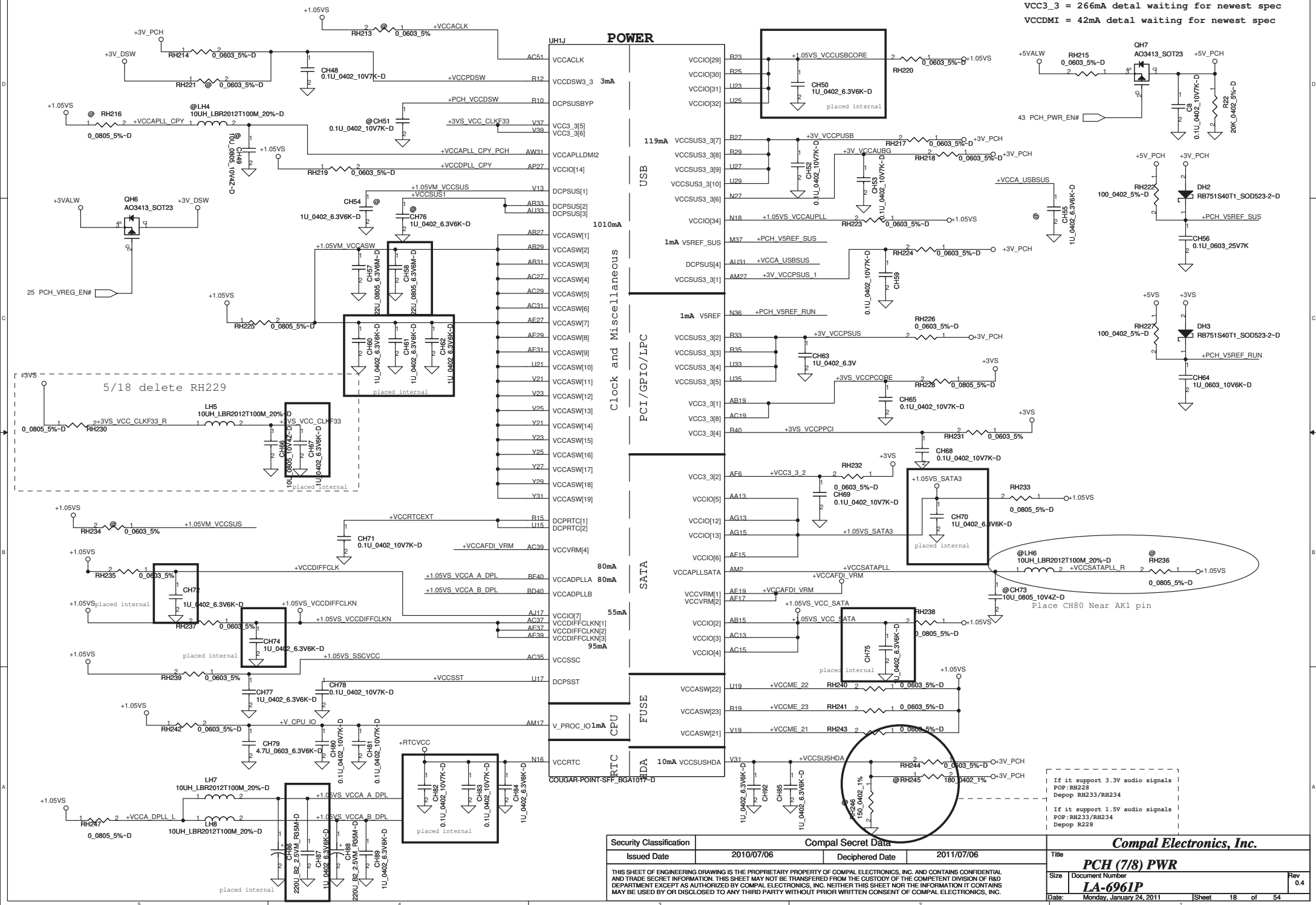


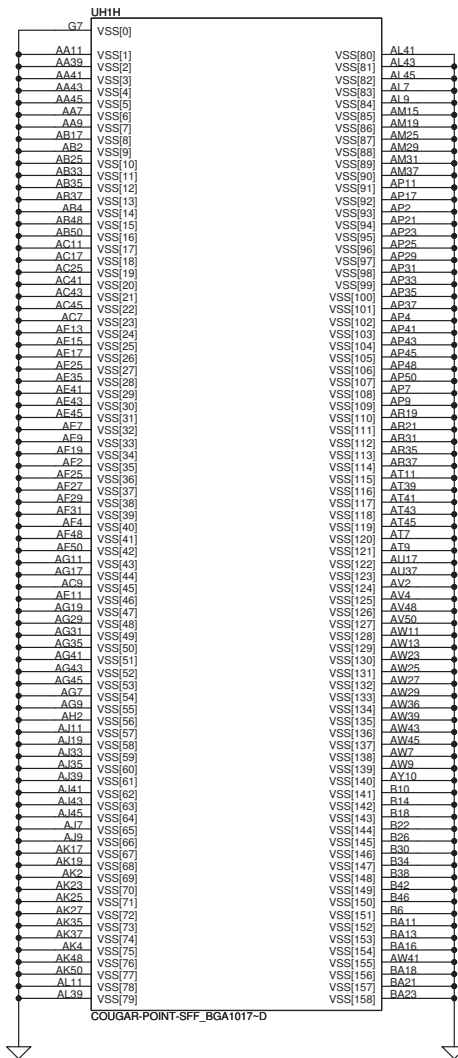
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

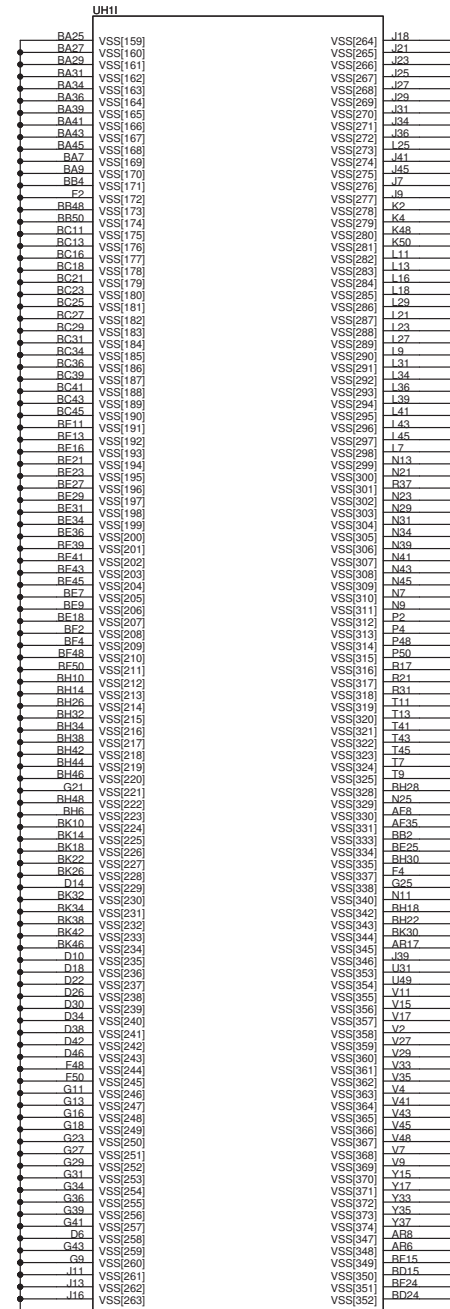


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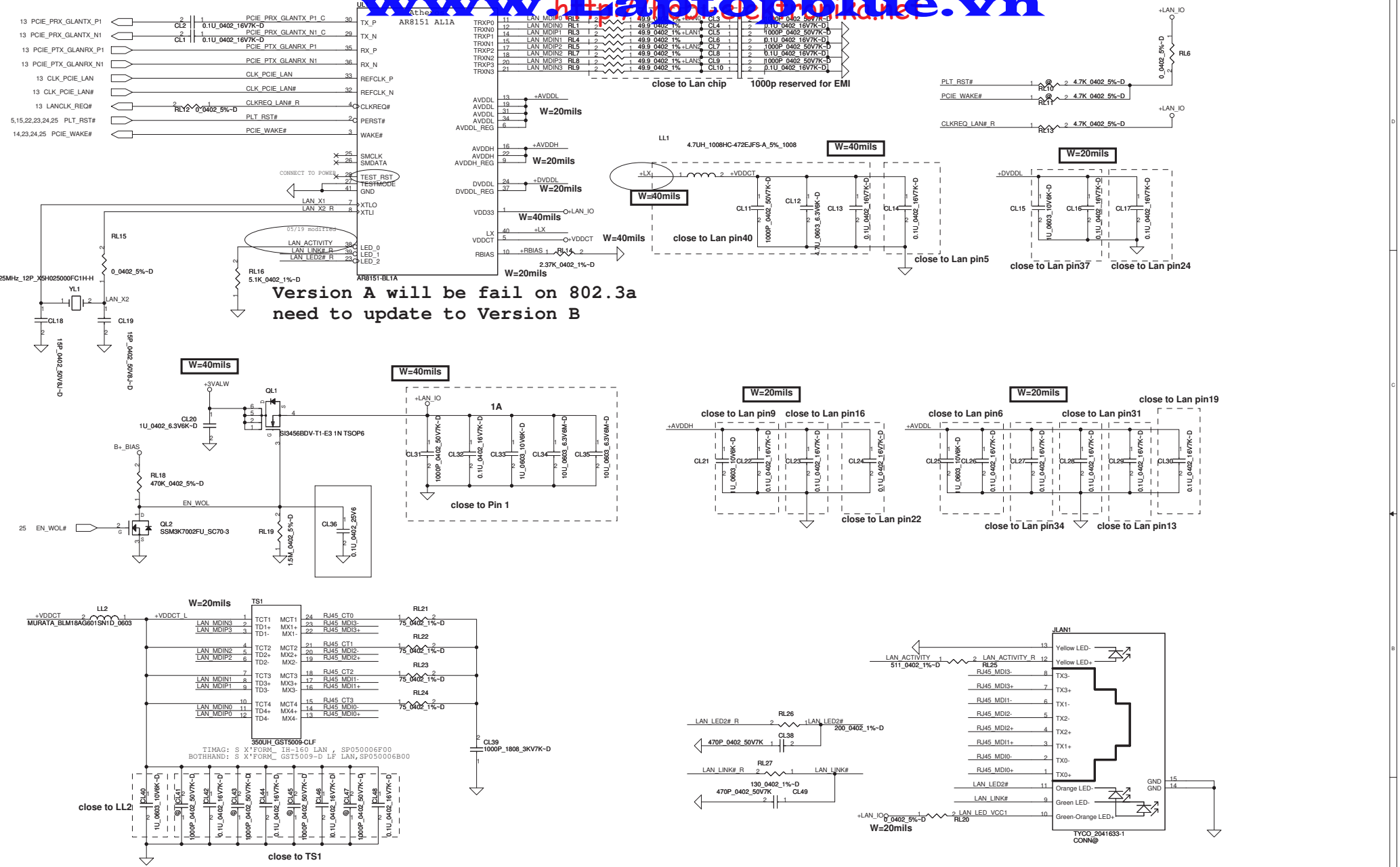


COUGAR-POINT-SFF_BGA1017-D

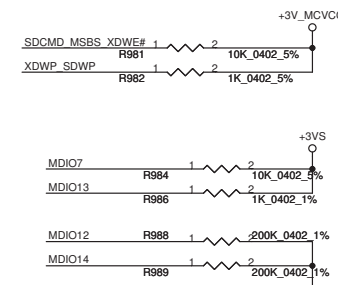
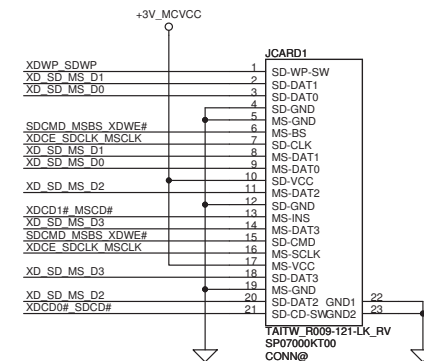


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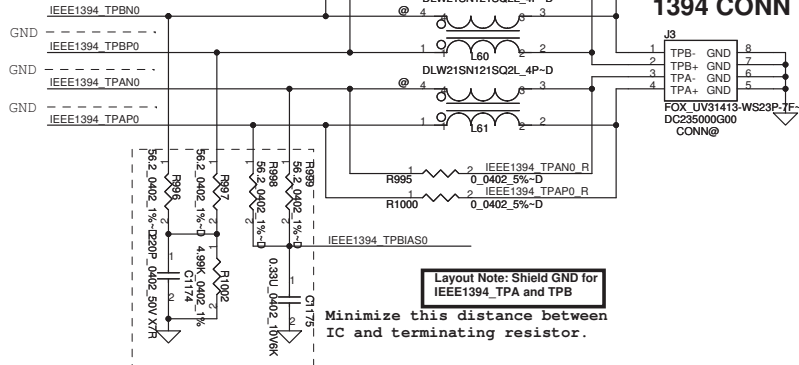
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3 in 1 Card Reader CONN



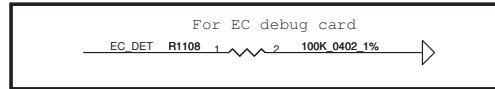
Layout Note:
Add GND shield for 1394.



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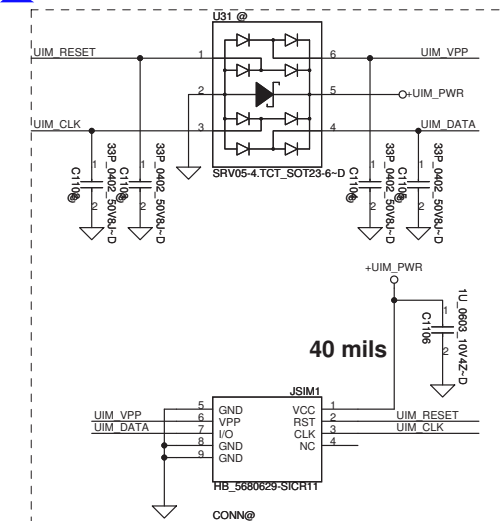
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Issued Date				Deciphered Date				2009/07/25			
2009/07/25				2010/07/25				2010/07/25			
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110 mils

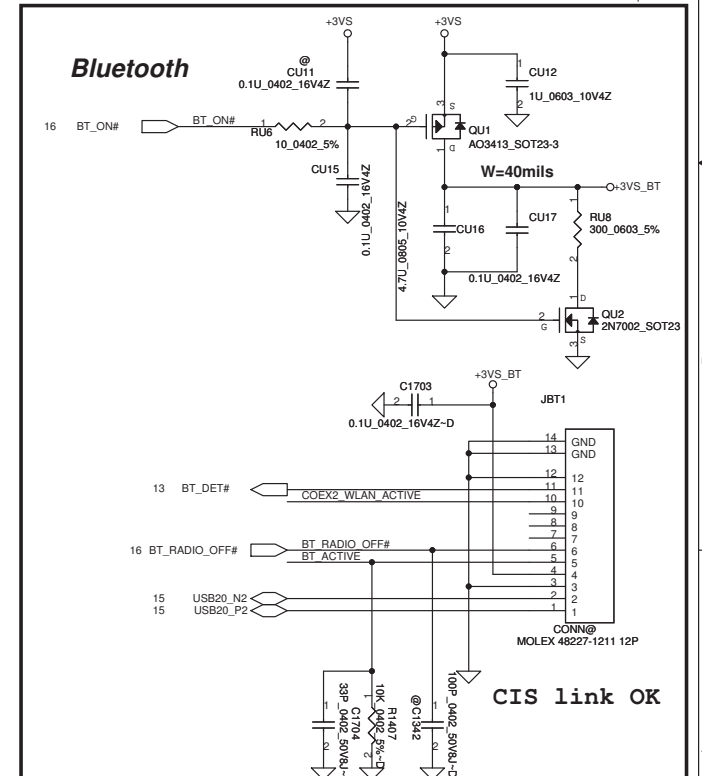


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+−9%	1000	750	
+3.3Vaux	+−9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+−5%	500	375	NA

20 mils



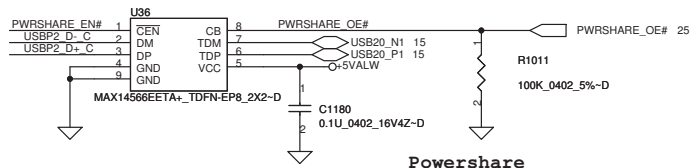
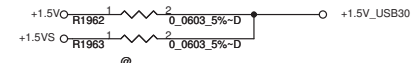
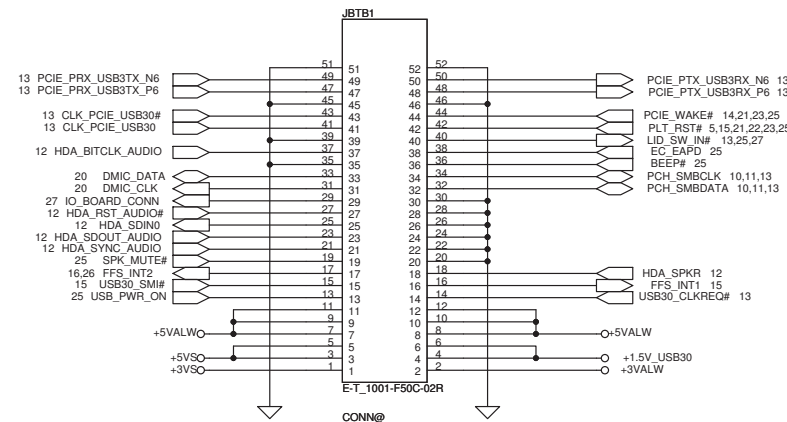
Bluetooth



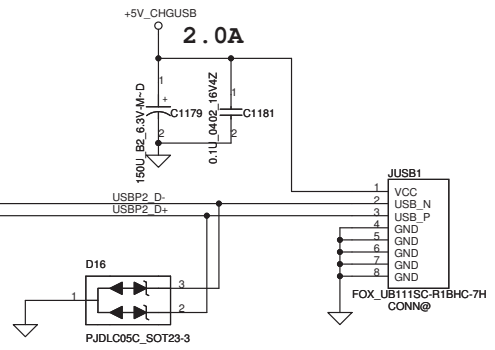
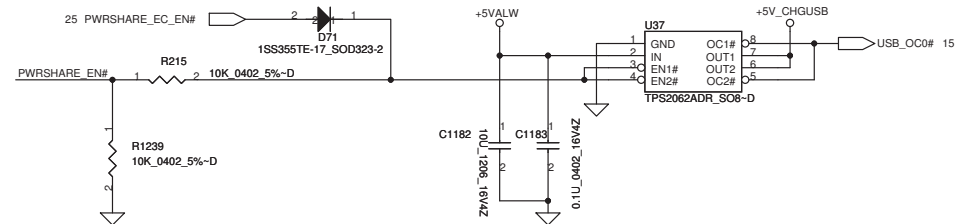
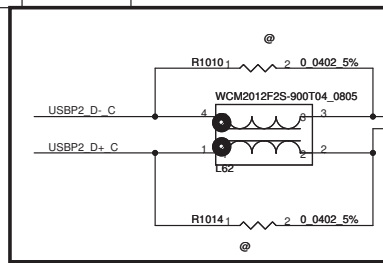
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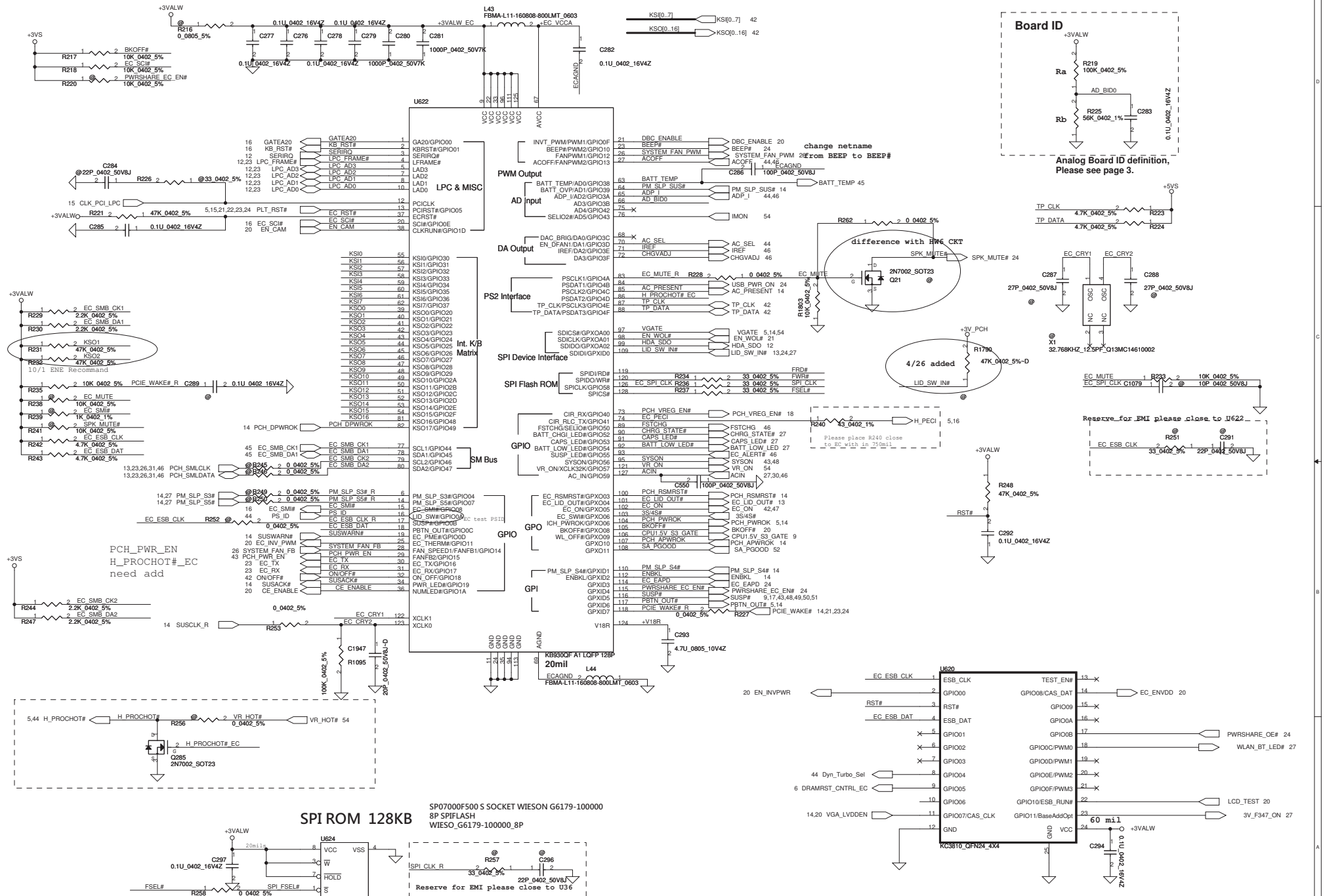
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IO Board CONN



OE#	Function
L	Dect charger
H	D=1D





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The diagram illustrates the JHDD1 connector pinout and its connections to various components:

- Pin 1:** GND
- Pin 2:** SATA_PTX_DRX_P0_C
- Pin 3:** SATA_PTX_DRX_N0_C
- Pin 4:** GND
- Pin 5:** SATA_PRX_DTX_N0_C
- Pin 6:** SATA_PRX_DTX_P0_C
- Pin 7:** GND
- Pin 8:** +3VS
- Pin 9:** +3VS
- Pin 10:** +3VS
- Pin 11:** GND
- Pin 12:** HDD_DETECT#
- Pin 13:** +5VS
- Pin 14:** GND
- Pin 15:** +5VS
- Pin 16:** FFS_INT2_Q
- Pin 17:** GND
- Pin 18:** FFS_INT2_Q
- Pin 19:** GND
- Pin 20:** VCC12
- Pin 21:** VCC12
- Pin 22:** VCC12

Additional components and connections shown:

- Capacitors:** C1085 (0.01U 0402 16V7K) and C1086 (0.01U 0402 16V7K) are connected to the SATA signal lines.
- Resistor:** R938 (100K 0402 5%-D) is connected to the +5VS line.
- Diode:** Q83 (SSM3K7002FU_SC70-3-D) is connected to the FFS_INT2_Q signal line.
- Connector:** LD2822F-SARL6 CONN@ is connected to the GND and VCC12 pins.

The top diagram shows the connection for the HDD CONN (JHDD1). It features a 5VS pin connected to a network of capacitors: C1087 (10U_0895_10V4Z), C1088 (10U_0402_16V4Z), C1089 (10U_0402_16V4Z), and C1090 (1000P_0402_25V6J). The other side of these capacitors is connected to a common ground point.

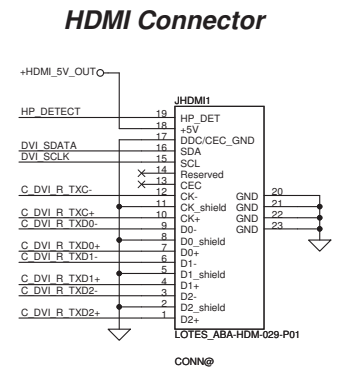
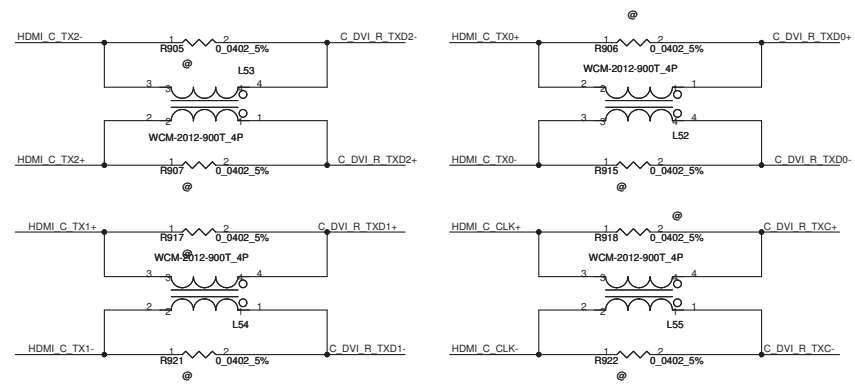
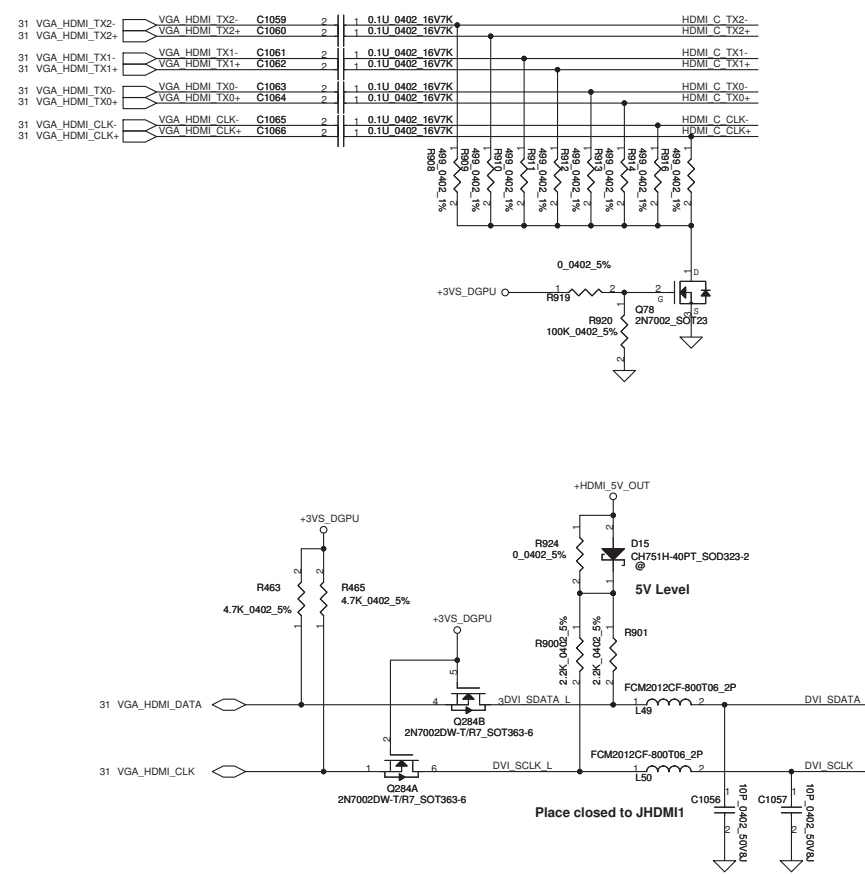
The bottom diagram shows the connection for the 3VS pin. It features a 3VS pin connected to a network of capacitors: C1195 (10U_0895_10V4Z) and C1196 (10U_0402_16V4Z). The other side of these capacitors is connected to a common ground point.



DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

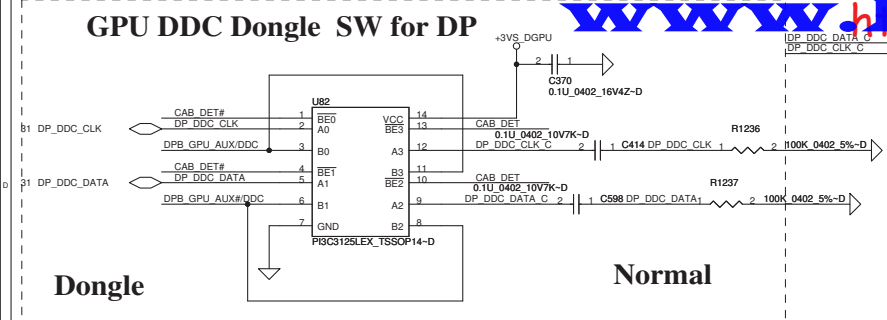
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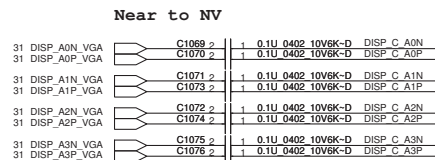
GPU DDC Dongle SW for DP

www.laptopblue.vn

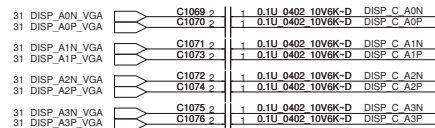


Dongle

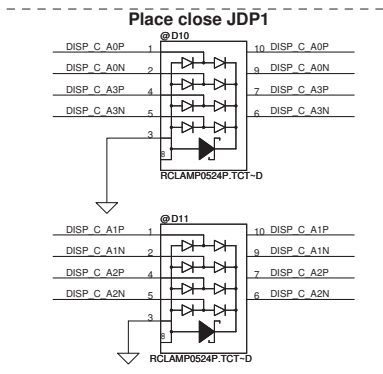
Normal



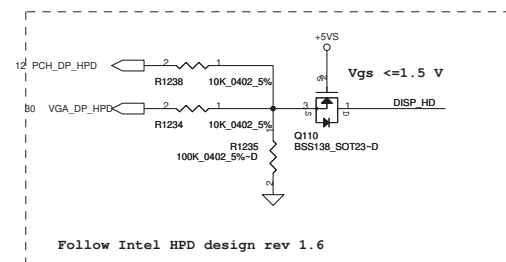
Near to NV



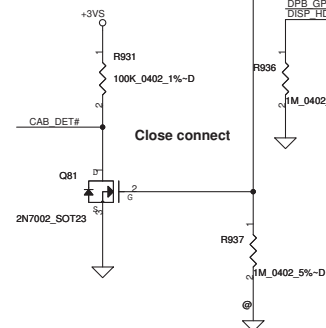
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PCBA@



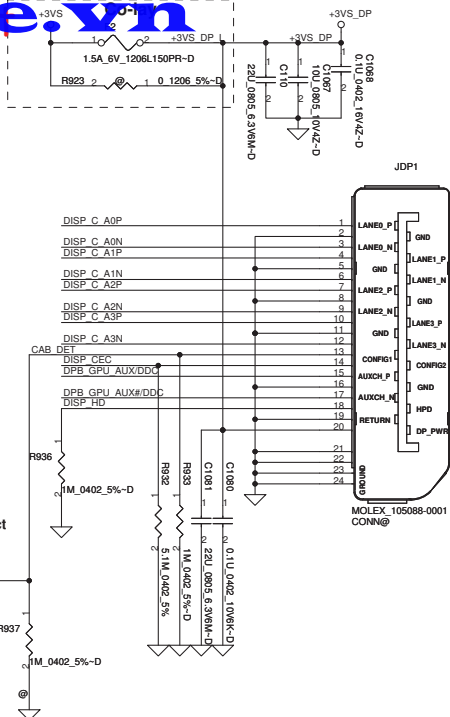
Place close JDP1



Follow Intel HPD design rev 1.6

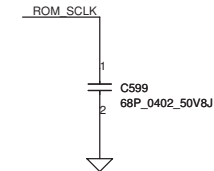


Close connect

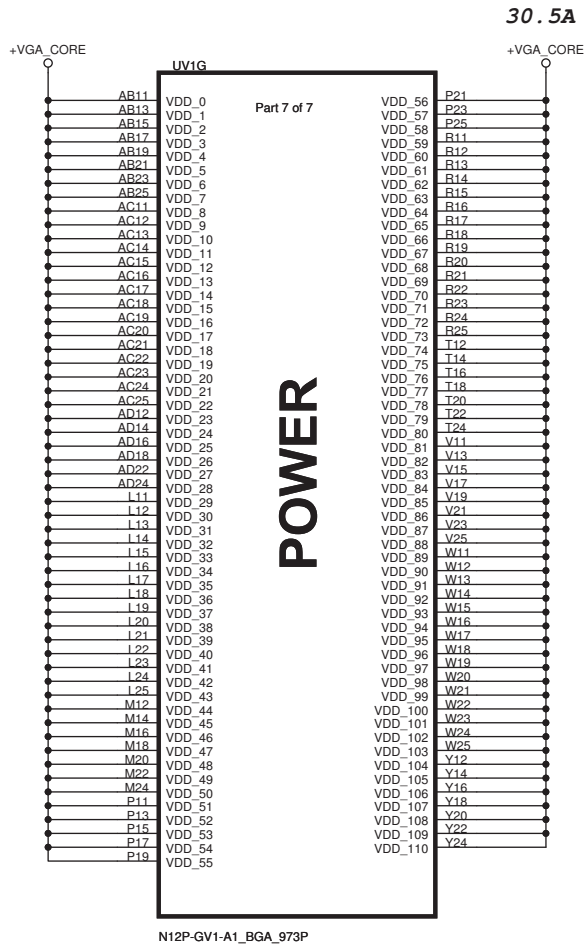
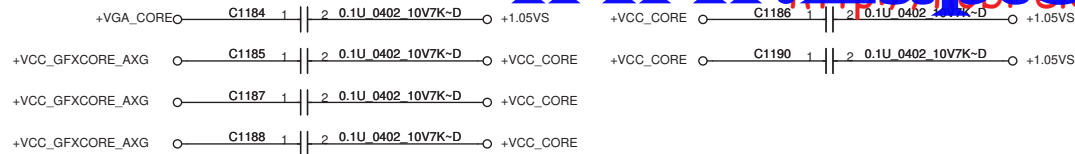


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						Size		Document Number			LA-6961P		Rev
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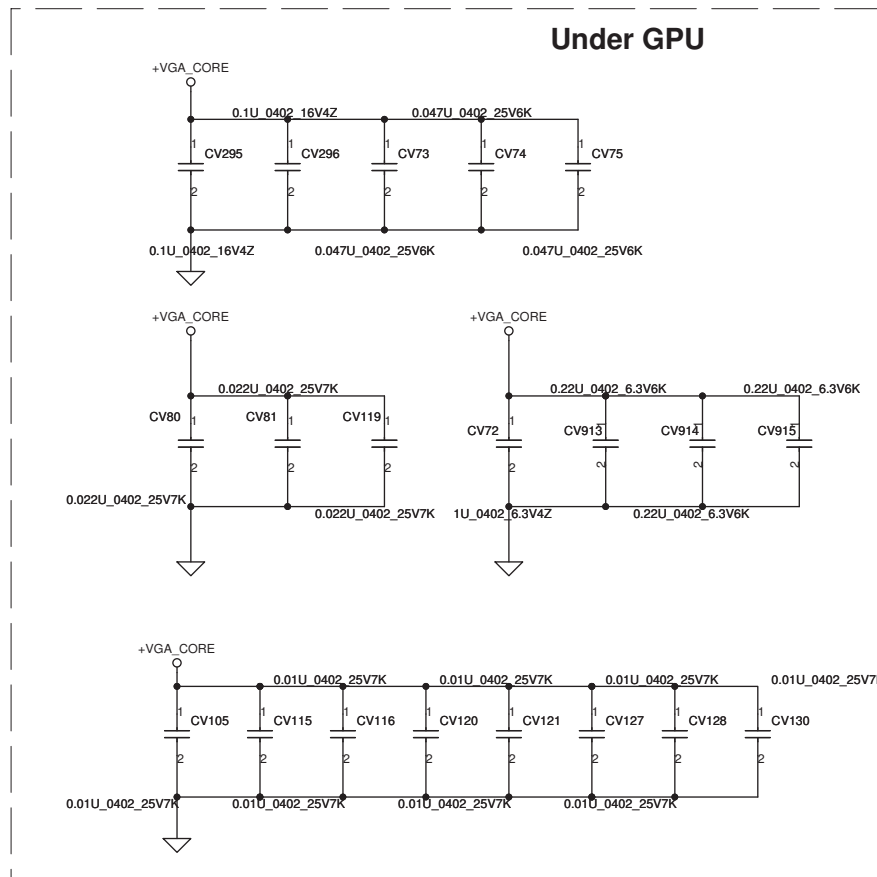
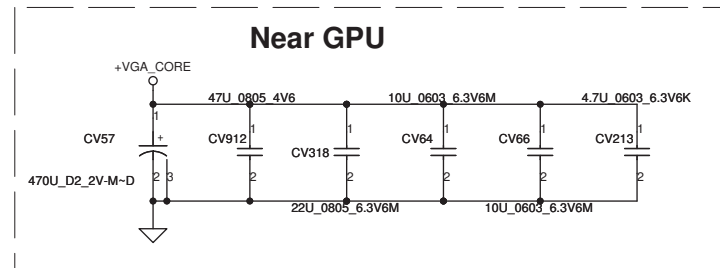
UV1G

Part 7 of 7

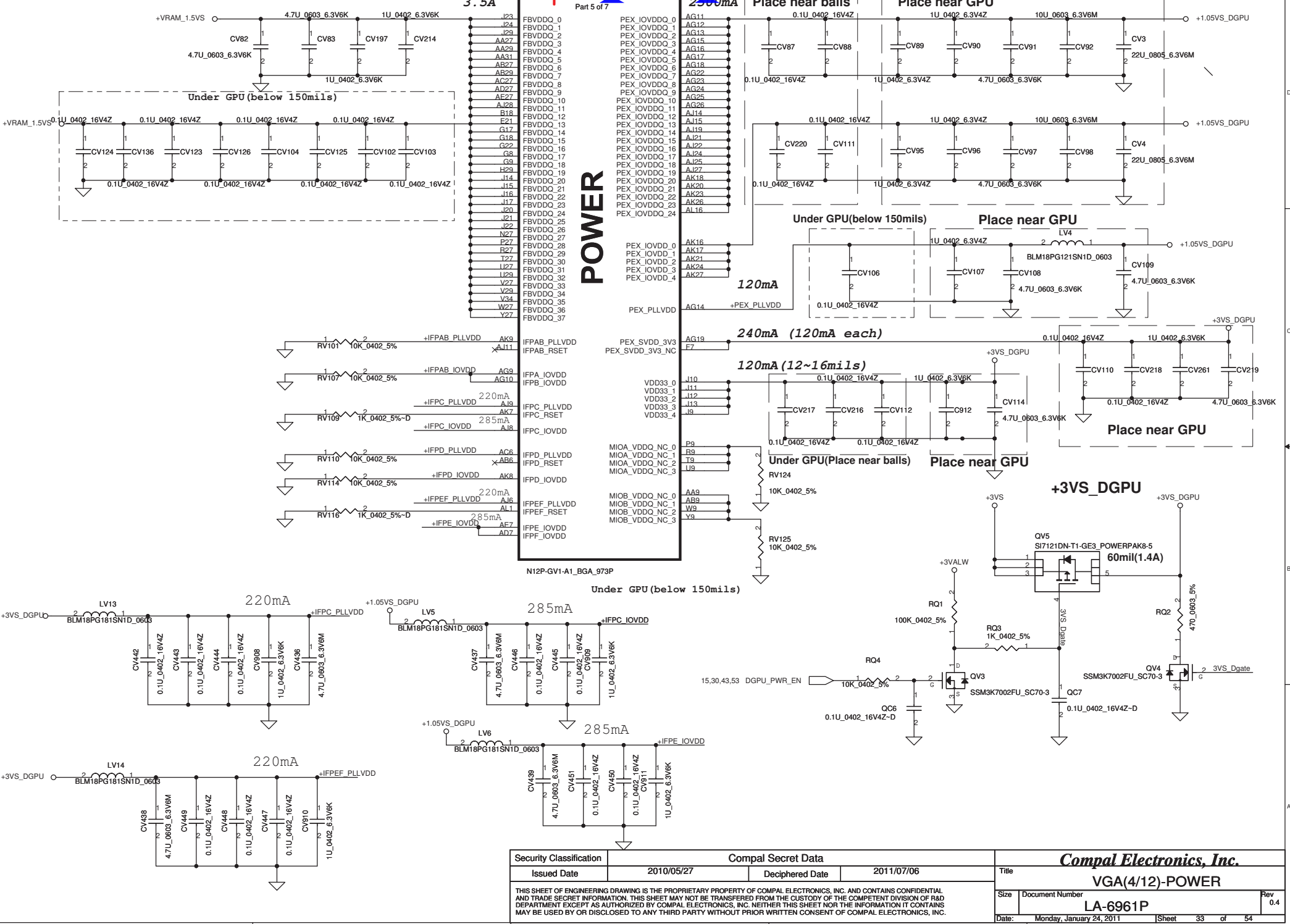
POWER

N12P-GV1-A1_BGA_973P

30.5A

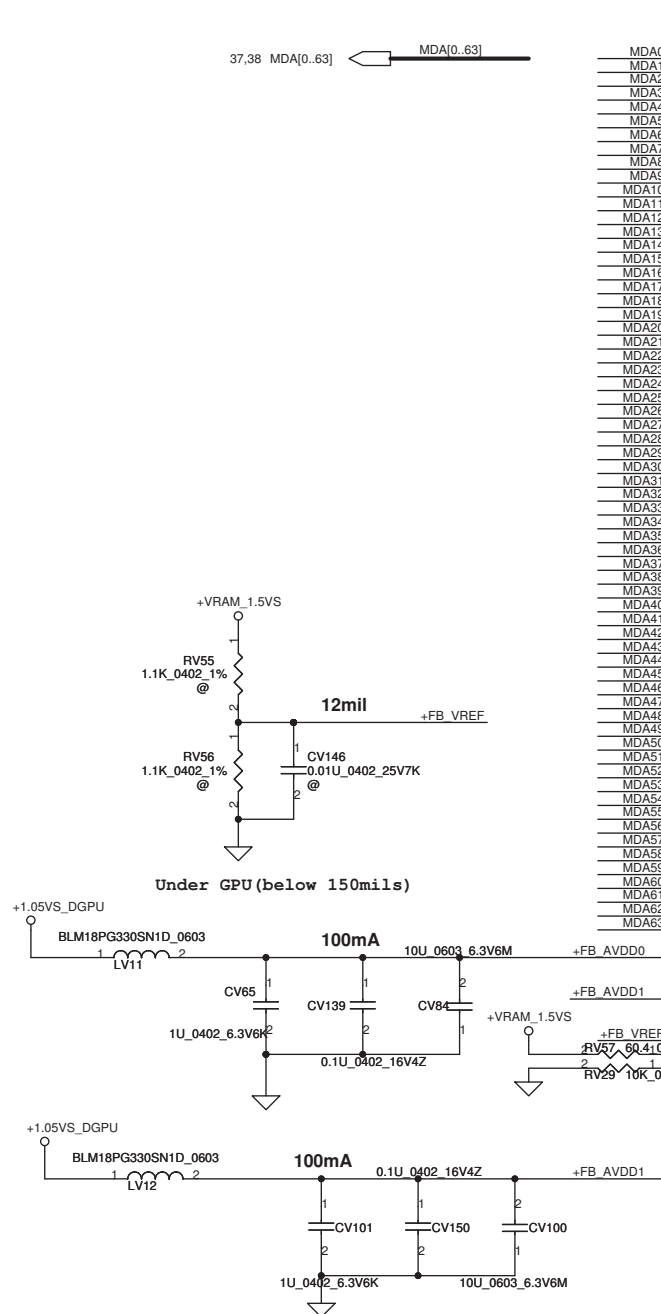


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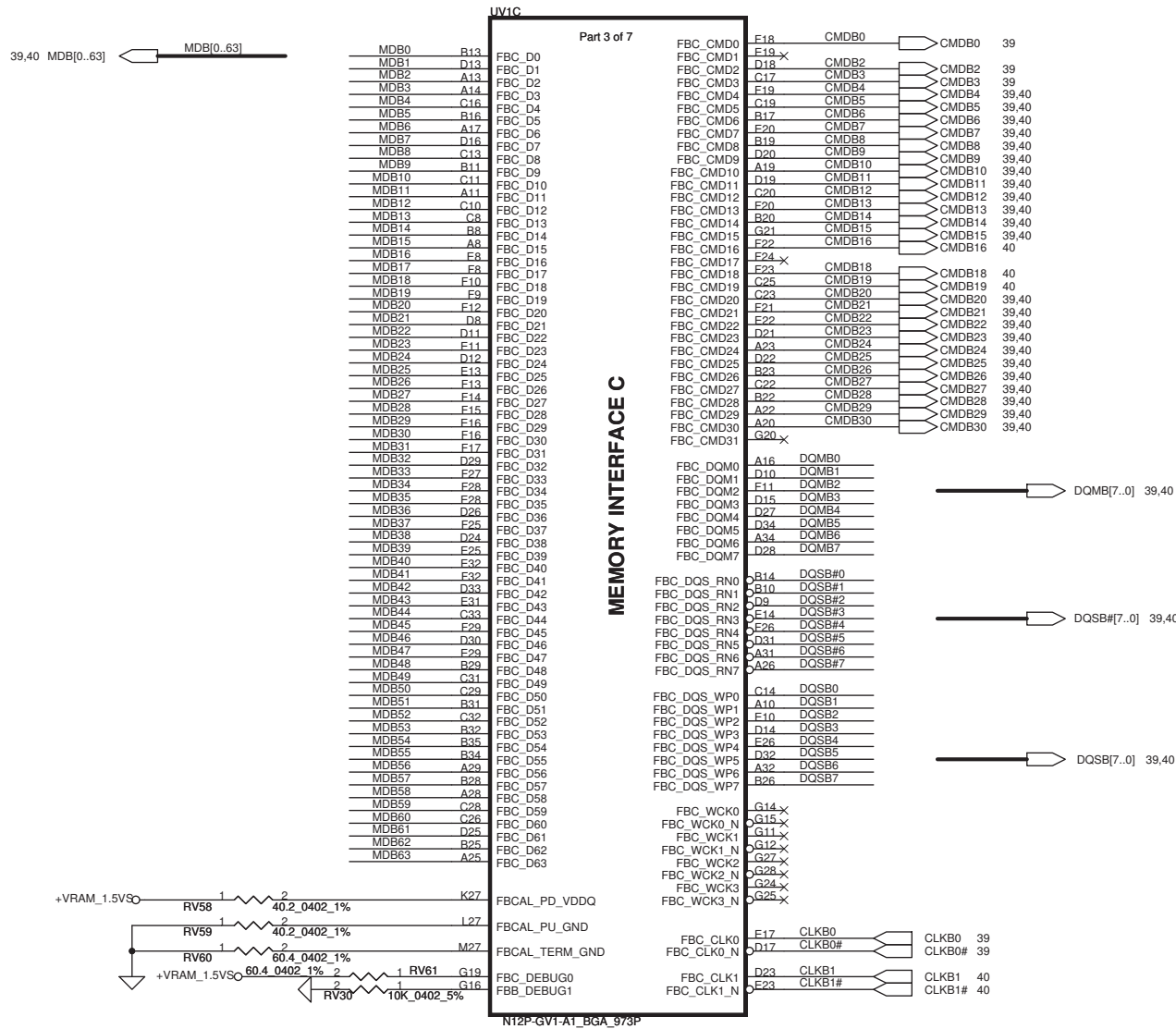
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Part 2 of 7

MEMORY INTERFACE A

N12P-GV1-A1_BGA_973P

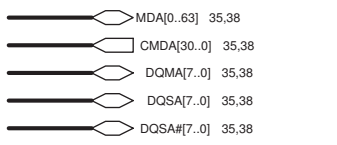
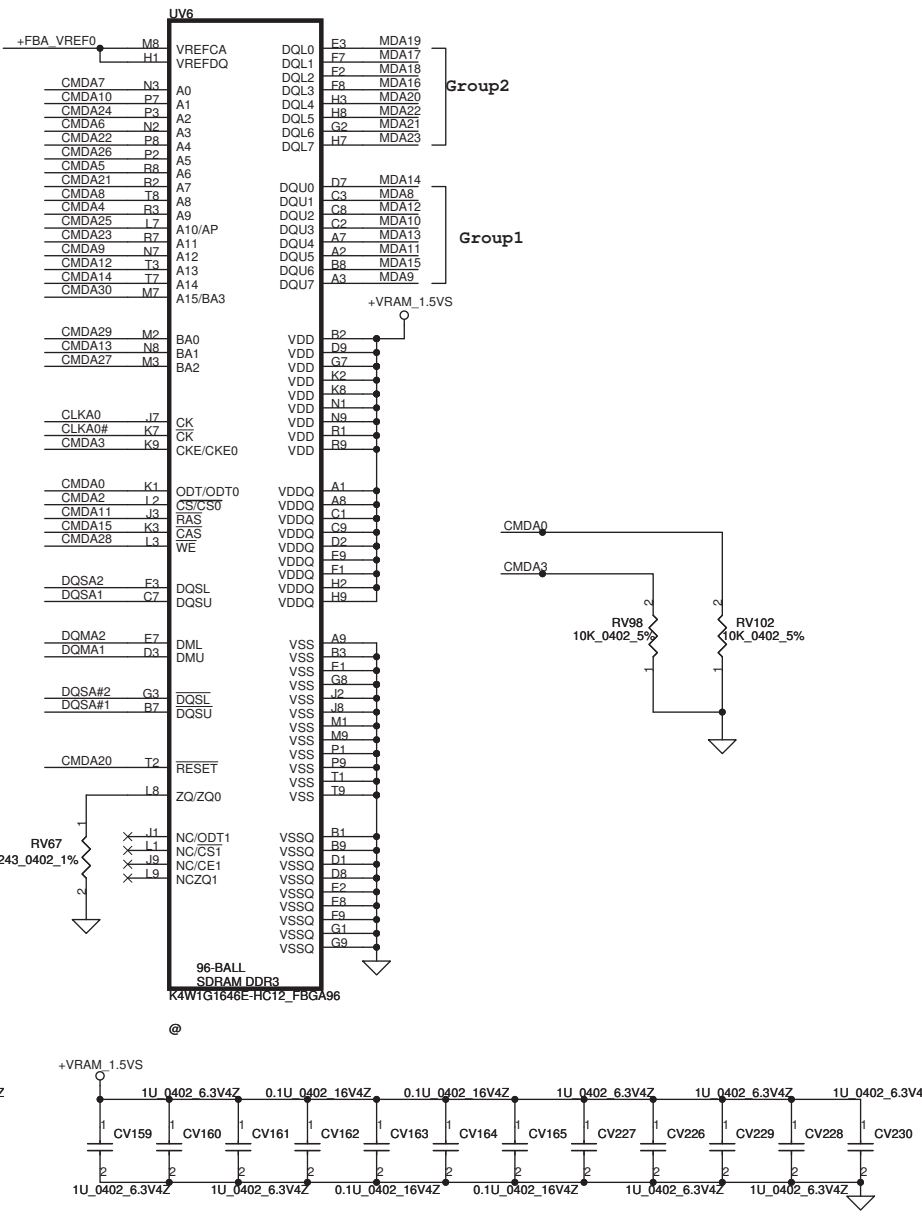
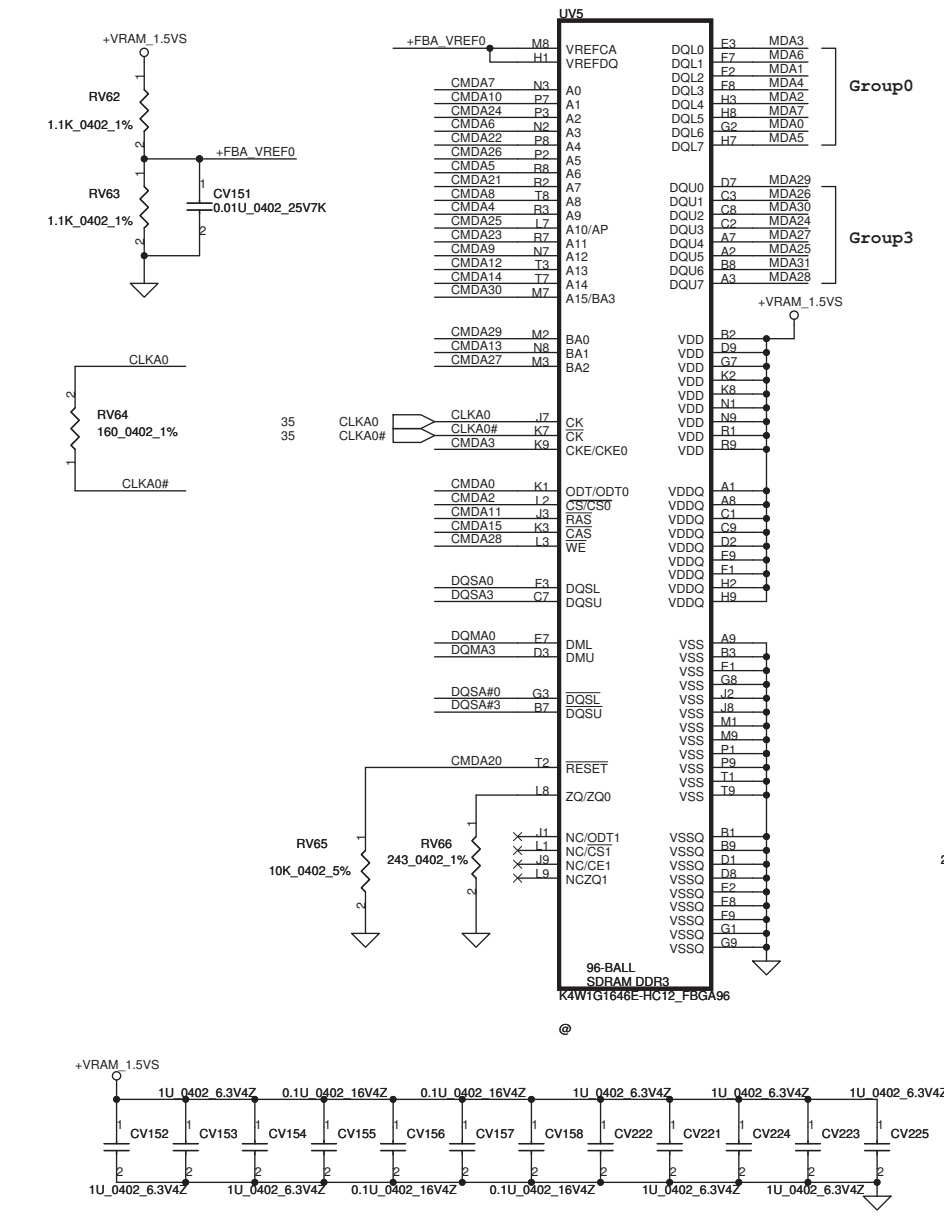
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FBA_CMD1	U30-X	CMDA1	CMDA1	37
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FBA_CMD3	U32	CMDA3	CMDA3	37
FBA_CMD4	U33	CMDA4	CMDA4	37,38
FBA_CMD5	U34	CMDA5	CMDA5	37,38
FBA_CMD6	U35	CMDA6	CMDA6	37,38
FBA_CMD7	U36	CMDA7	CMDA7	37,38
FBA_CMD8	U37	CMDA8	CMDA8	37,38
FBA_CMD9	U38	CMDA9	CMDA9	37,38
FBA_CMD10	U39	CMDA10	CMDA10	37,38
FBA_CMD11	U40	CMDA11	CMDA11	37,38
FBA_CMD12	U41	CMDA12	CMDA12	37,38
FBA_CMD13	U42	CMDA13	CMDA13	37,38
FBA_CMD14	U43	CMDA14	CMDA14	37,38
FBA_CMD15	U44	CMDA15	CMDA15	37,38
FBA_CMD16	U45	CMDA16	CMDA16	38
FBA_CMD17	U46	CMDA17	CMDA17	38
FBA_CMD18	U47	CMDA18	CMDA18	38
FBA_CMD19	U48	CMDA19	CMDA19	38
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FBA_CMD22	U51	CMDA22	CMDA22	37,38
FBA_CMD23	U52	CMDA23	CMDA23	37,38
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FBA_CMD45	U74	CMDA45	CMDA45	37,38
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FBA_CMD87	U116	CMDA87	CMDA87	37,38
FBA_CMD88	U117	CMDA88	CMDA88	37,38
FBA_CMD89	U118	CMDA89	CMDA89	37,38
FBA_CMD90	U119	CMDA90	CMDA90	37,38
FBA_CMD91	U120	CMDA91	CMDA91	37,38
FBA_CMD92	U121	CMDA92	CMDA92	37,38
FBA_CMD93	U122	CMDA93	CMDA93	37,38
FBA_CMD94	U123	CMDA94	CMDA94	37,38
FBA_CMD95	U124	CMDA95	CMDA95	37,38
FBA_CMD96	U125	CMDA96	CMDA96	37,38
FBA_CMD97	U126	CMDA97	CMDA97	37,38
FBA_CMD98	U127	CMDA98	CMDA98	37,38
FBA_CMD99	U128	CMDA99	CMDA99	37,38
FBA_CMD100	U129	CMDA100	CMDA100	37,38
FBA_CMD101	U130	CMDA101	CMDA101	37,38
FBA_CMD102	U131	CMDA102	CMDA102	37,38
FBA_CMD103	U132	CMDA103	CMDA103	37,38
FBA_CMD104	U133	CMDA104	CMDA104	37,38
FBA_CMD105	U134	CMDA105	CMDA105	37,38
FBA_CMD106	U135	CMDA106	CMDA106	37,38
FBA_CMD107	U136	CMDA107	CMDA107	37,38
FBA_CMD108	U137	CMDA108	CMDA108	37,38
FBA_CMD109	U138	CMDA109	CMDA109	37,38
FBA_CMD110	U139	CMDA110	CMDA110	37,38
FBA_CMD111	U140	CMDA111	CMDA111	37,38
FBA_CMD112	U141	CMDA112	CMDA112	37,38
FBA_CMD113	U142	CMDA113	CMDA113	37,38
FBA_CMD114	U143	CMDA114	CMDA114	37,38
FBA_CMD115	U144	CMDA115	CMDA115	37,38
FBA_CMD116	U145	CMDA116	CMDA116	37,38
FBA_CMD117	U146	CMDA117	CMDA117	37,38
FBA_CMD118	U147	CMDA118	CMDA118	37,38
FBA_CMD119	U148	CMDA119	CMDA119	37,38
FBA_CMD120	U149	CMDA120	CMDA120	37,38
FBA_CMD121	U150	CMDA121	CMDA121	37,38
FBA_CMD122	U151	CMDA122	CMDA122	37,38
FBA_CMD123	U152	CMDA123	CMDA123	37,38
FBA_CMD124	U153	CMDA124	CMDA124	37,38
FBA_CMD125	U154	CMDA125	CMDA125	37,38
FBA_CMD126	U155	CMDA126	CMDA126	37,38
FBA_CMD127	U156	CMDA127	CMDA127	37,38
FBA_CMD128	U157	CMDA128	CMDA128	37,38
FBA_CMD129	U158	CMDA129	CMDA129	37,38
FBA_CMD130	U159	CMDA130	CMDA130	37,38
FBA_CMD131	U160	CMDA131	CMDA131	37,38
FBA_CMD132	U161	CMDA132	CMDA132	37,38
FBA_CMD133	U162	CMDA133	CMDA133	37,38
FBA_CMD134	U163	CMDA134	CMDA134	37,38
FBA_CMD135	U164	CMDA135	CMDA135	37,38
FBA_CMD136	U165	CMDA136	CMDA136	37,38
FBA_CMD137	U166	CMDA137	CMDA137	37,38
FBA_CMD138	U167	CMDA138	CMDA138	37,38
FBA_CMD139	U168	CMDA139	CMDA139	37,38
FBA_CMD140	U169	CMDA140	CMDA140	37,38
FBA_CMD141	U170	CMDA141	CMDA141	37,38
FBA_CMD142	U171	CMDA142	CMDA142	37,38
FBA_CMD143	U172	CMDA143	CMDA143	37,38
FBA_CMD144	U173	CMDA144	CMDA144	37,38
FBA_CMD145	U174	CMDA145	CMDA145	37,38
FBA_CMD146	U175	CMDA146	CMDA146	37,38
FBA_CMD147	U176	CMDA147	CMDA147	37,38
FBA_CMD148	U177	CMDA148	CMDA148	37,38
FBA_CMD149	U178	CMDA149	CMDA149	37,38
FBA_CMD150	U179	CMDA150	CMDA150	37,38
FBA_CMD151	U180	CMDA151	CMDA151	37,38
FBA_CMD152	U181	CMDA152	CMDA152	37,38
FBA_CMD153	U182	CMDA153	CMDA153	37,38
FBA_CMD154	U183	CMDA154	CMDA154	37,38
FBA_CMD155	U184	CMDA155	CMDA155	37,38
FBA_CMD156	U185	CMDA156	CMDA156	37,38
FBA_CMD157	U186	CMDA157	CMDA157	37,38
FBA_CMD158	U187	CMDA158	CMDA158	37,38
FBA_CMD159	U188	CMDA159	CMDA159	37,38
FBA_CMD160	U189	CMDA160	CMDA160	37,38
FBA_CMD161	U190	CMDA161	CMDA161	37,38
FBA_CMD162	U191	CMDA162	CMDA162	37,38
FBA_CMD163	U192	CMDA163	CMDA163	37,38
FBA_CMD164	U193	CMDA164	CMDA164	37,38
FBA_CMD165	U194	CMDA165	CMDA165	37,38
FBA_CMD166	U195	CMDA166	CMDA166	37,38
FBA_CMD167	U196	CMDA167	CMDA167	37,38
FBA_CMD168	U197	CMDA168	CMDA168	37,38
FBA_CMD169	U198	CMDA169	CMDA169	37,38
FBA_CMD170	U199	CMDA170	CMDA170	37,38
FBA_CMD171	U200	CMDA171	CMDA171	37,38
FBA_CMD172	U201	CMDA172	CMDA172	37,38
FBA_CMD173	U202	CMDA173	CMDA173	37,38
FBA_CMD174	U203	CMDA174	CMDA174	37,38
FBA_CMD175	U204	CMDA175	CMDA175	37,38
FBA_CMD176	U205	CMDA176	CMDA176	37,38
FBA_CMD177	U206	CMDA177	CMDA177	37,38
FBA_CMD178	U207	CMDA178	CMDA178	37,38
FBA_CMD179	U208	CMDA179	CMDA179	37,38
FBA_CMD180	U209	CMDA180	CMDA180	37,38
FBA_CMD181	U210	CMDA181	CMDA181	37,38
FBA_CMD182	U211	CMDA182	CMDA182	37,38
FBA_CMD183	U212	CMDA183	CMDA183	37,38
FBA_CMD184	U213	CMDA184	CMDA184	37,38
FBA_CMD185	U214	CMDA185	CMDA185	37,38
FBA_CMD186	U215	CMDA186	CMDA186	37,38
FBA_CMD187	U216	CMDA187	CMDA187	37,38
FBA_CMD188	U217	CMDA188	CMDA188	37,38
FBA_CMD189	U218	CMDA189	CMDA189	37,38
FBA_CMD190	U219	CMDA190	CMDA190	37,38
FBA_CMD191	U220	CMDA191	CMDA191	37,38
FBA_CMD192	U221	CMDA192	CMDA192	37,38
FBA_CMD193	U222	CMDA193	CMDA193	37,38
FBA_CMD194	U223	CMDA194	CMDA194	37,38
FBA_CMD195	U224	CMDA195	CMDA195	37,38
FBA_CMD196	U225	CMDA196	CMDA196	37,38
FBA_CMD197	U226	CMDA197	CMDA197	37,38
FBA_CMD198	U227	CMDA198	CMDA198	37,38
FBA_CMD199	U228	CMDA199	CMDA199	37,38
FBA_CMD200	U229	CMDA200	CMDA200	37,38
FBA_CMD201	U230	CMDA201	CMDA201	37,38
FBA_CMD202	U231	CMDA202	CMDA202	37,38
FBA_CMD203	U232	CMDA203	CMDA203	37,38
FBA_CMD204	U233	CMDA204	CMDA204	37,38
FBA_CMD205	U234	CMDA205	CMDA205	37,38
FBA_CMD206	U235	CMDA206	CMDA206	37,38
FBA_CMD207	U236	CMDA207	CMDA207	37,38
FBA_CMD208	U237	CMDA208	CMDA208	37,38
FBA_CMD209	U238	CMDA209	CMDA209	37,38
FBA_CMD210	U239	CMDA210	CMDA210	37,38
FBA_CMD211	U240	CMDA211	CMDA211	37,38
FBA_CMD212	U241	CMDA212	CMDA212	37,38
FBA_CMD213	U242	CMDA213	CMDA213	37,38
FBA_CMD214	U243	CMDA214	CMDA214	37,38
FBA_CMD215	U244	CMDA215	CMDA215	37,38
FBA_CMD216	U245	CMDA216	CMDA216	37,38
FBA_CMD217	U246	CMDA217	CMDA217	37,38
FBA_CMD218	U247	CMDA218	CMDA218	37,38
FBA_CMD219	U248	CMDA219	CMDA219	37,38
FBA_CMD220	U249	CMDA220	CMDA220	37,38
FBA_CMD221	U250	CMDA221	CMDA221	37,38
FBA_CMD222	U251	CMDA222	CMDA222	37,38
FBA_CMD223	U252	CMDA223	CMDA223	37,38
FBA_CMD224	U253	CMDA224	CMDA224	37,38
FBA_CMD225	U254	CMDA225	CMDA225	37,38
FBA_CMD226	U255	CMDA226	CMDA226	37,38
FBA_CMD227	U256	CMDA227	CMDA227	37,38
FBA_CMD228	U257	CMDA228	CMDA228	37,38
FBA_CMD229	U258	CMDA229	CMDA229	37,38
FBA_CMD230	U259	CMDA230	CMDA230	37,38
FBA_CMD231	U260	CMDA231	CMDA231	37,38
FBA_CMD232	U261	CMDA232	CMDA232	37,38
FBA_CMD233	U262	CMDA233	CMDA233	37,38
FBA_CMD234	U263	CMDA234	CMDA234	37,38
FBA_CMD235	U264	CMDA235	CMDA235	37,38



Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition A - Lower 32 bits

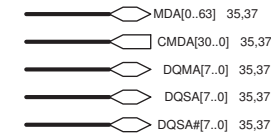
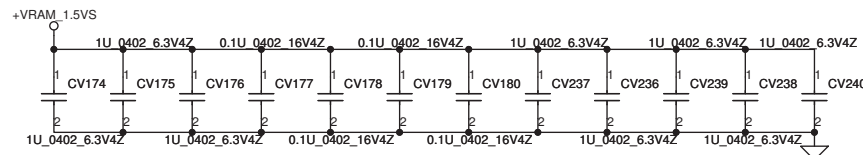
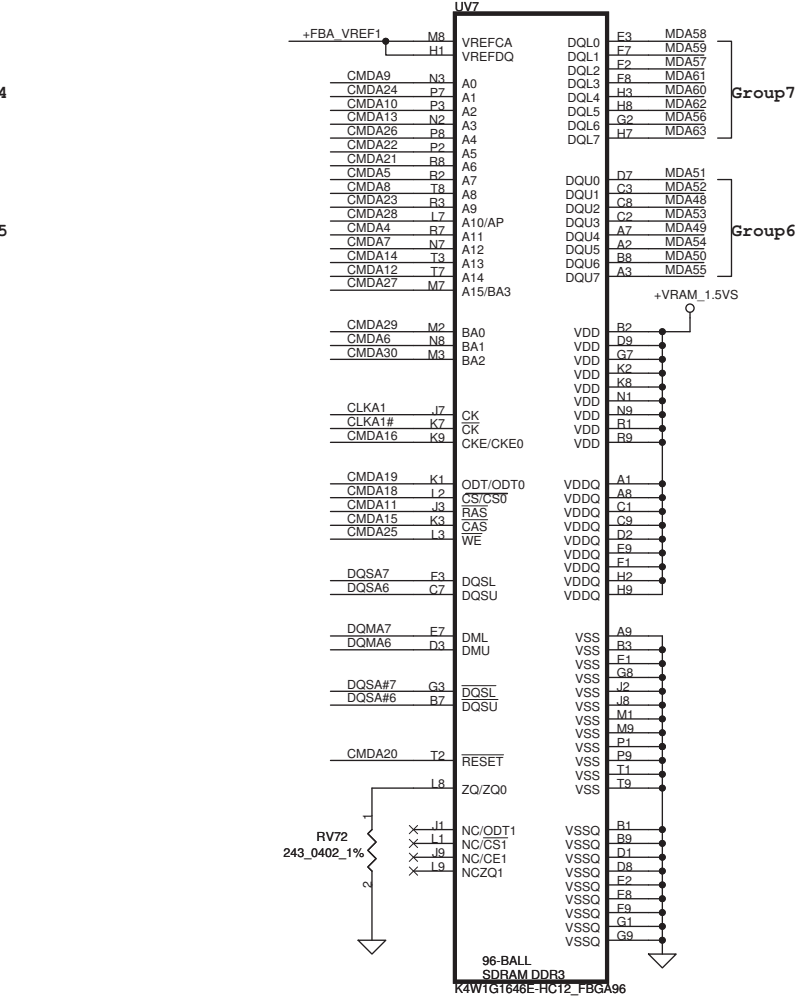
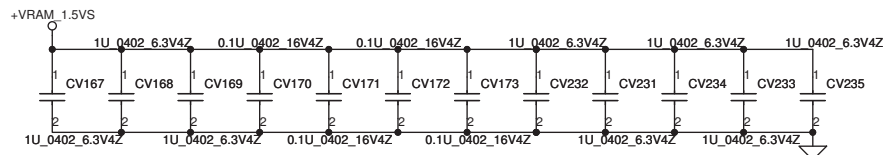
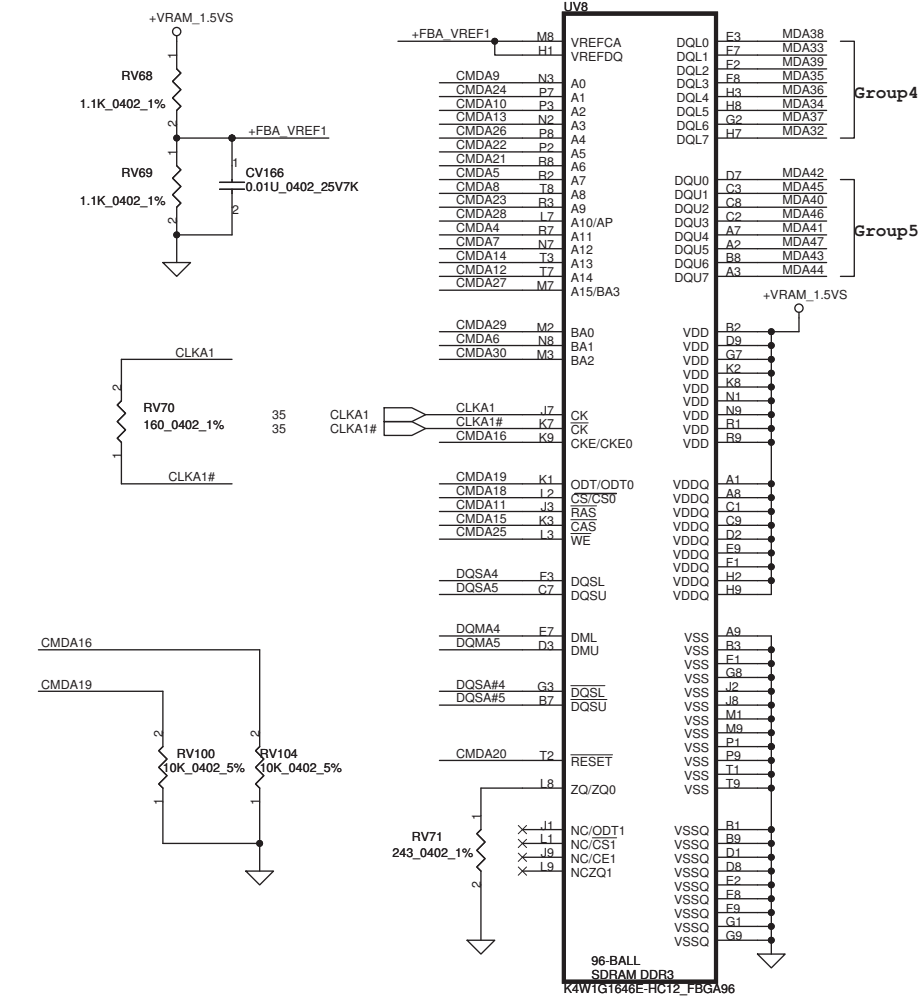


Mode E - Mirror Mode Mapping

Address	DATA	Bus
CMD3	CKE_L	32..63
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition A

Upper 32 bits <https://laptopblue.vn>

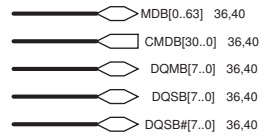
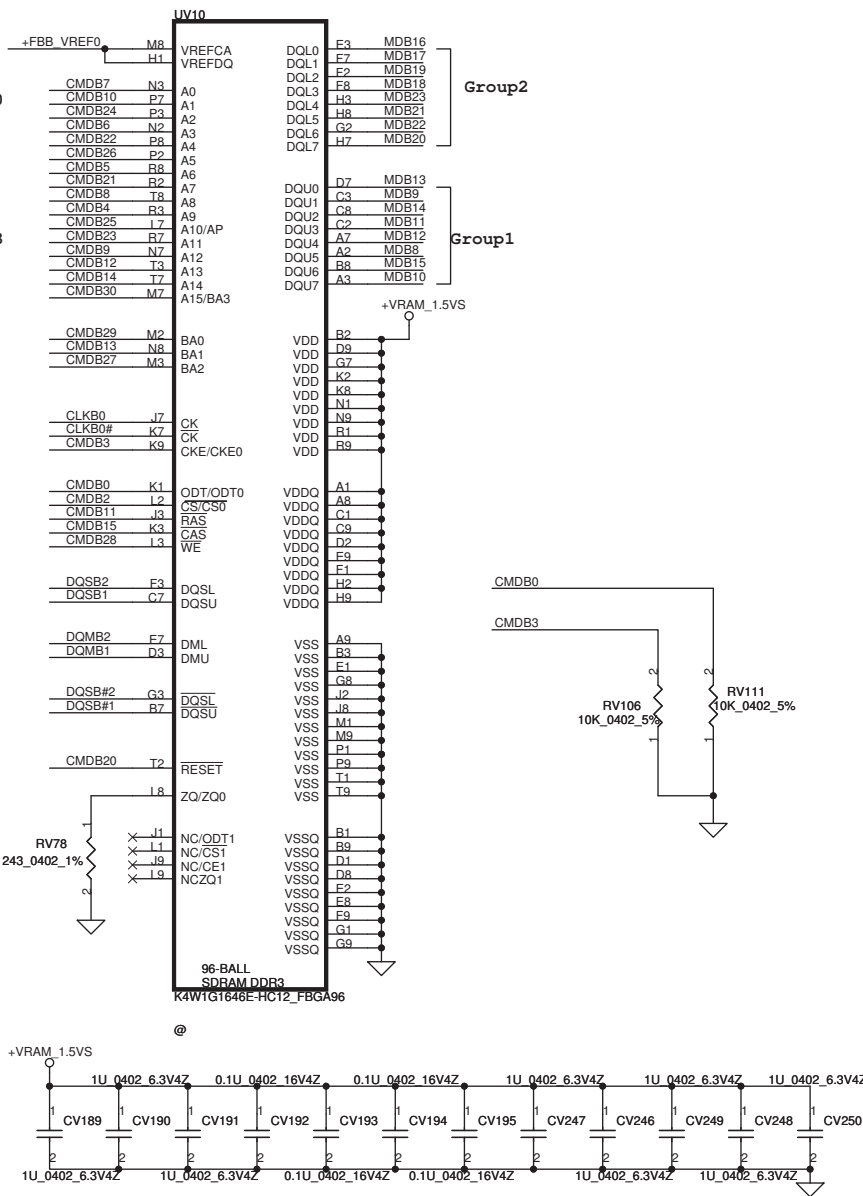
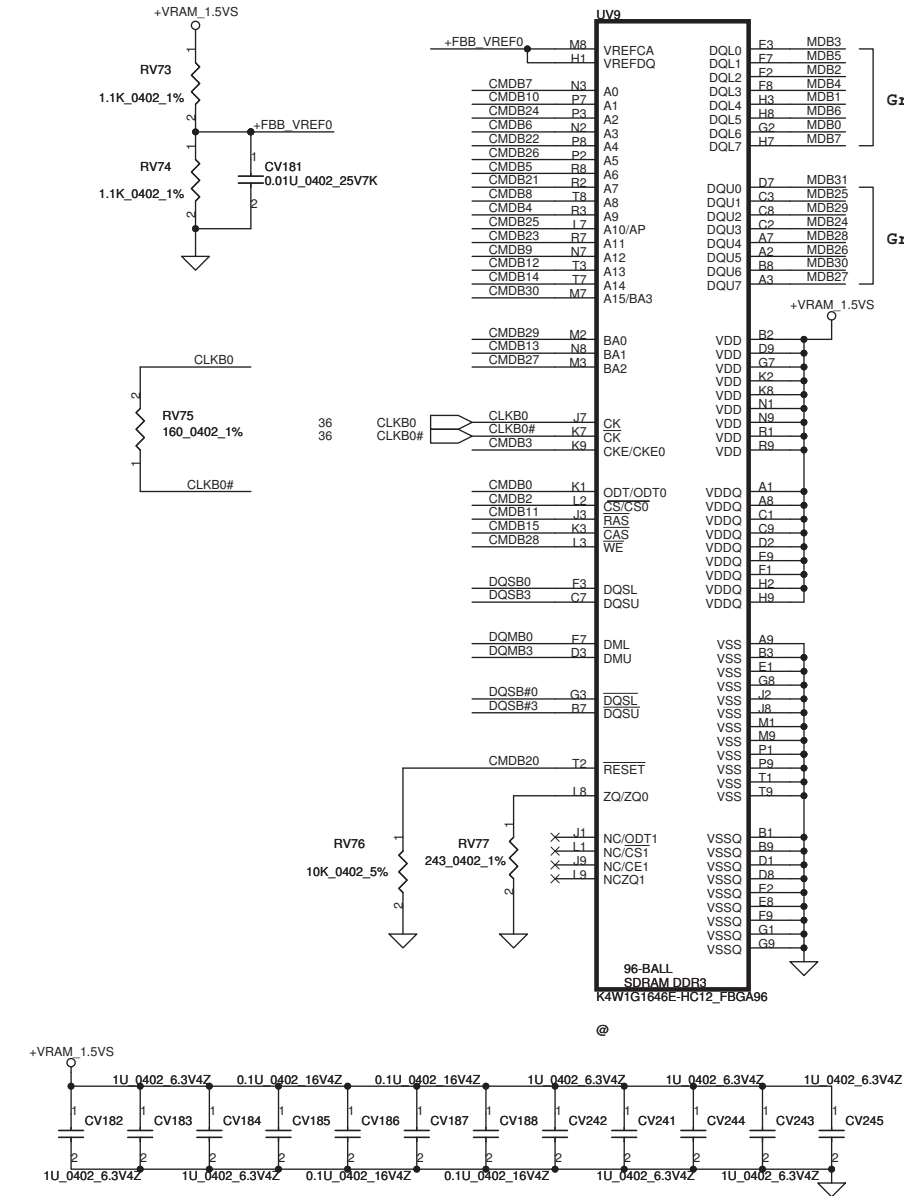


Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Lower 32 bits

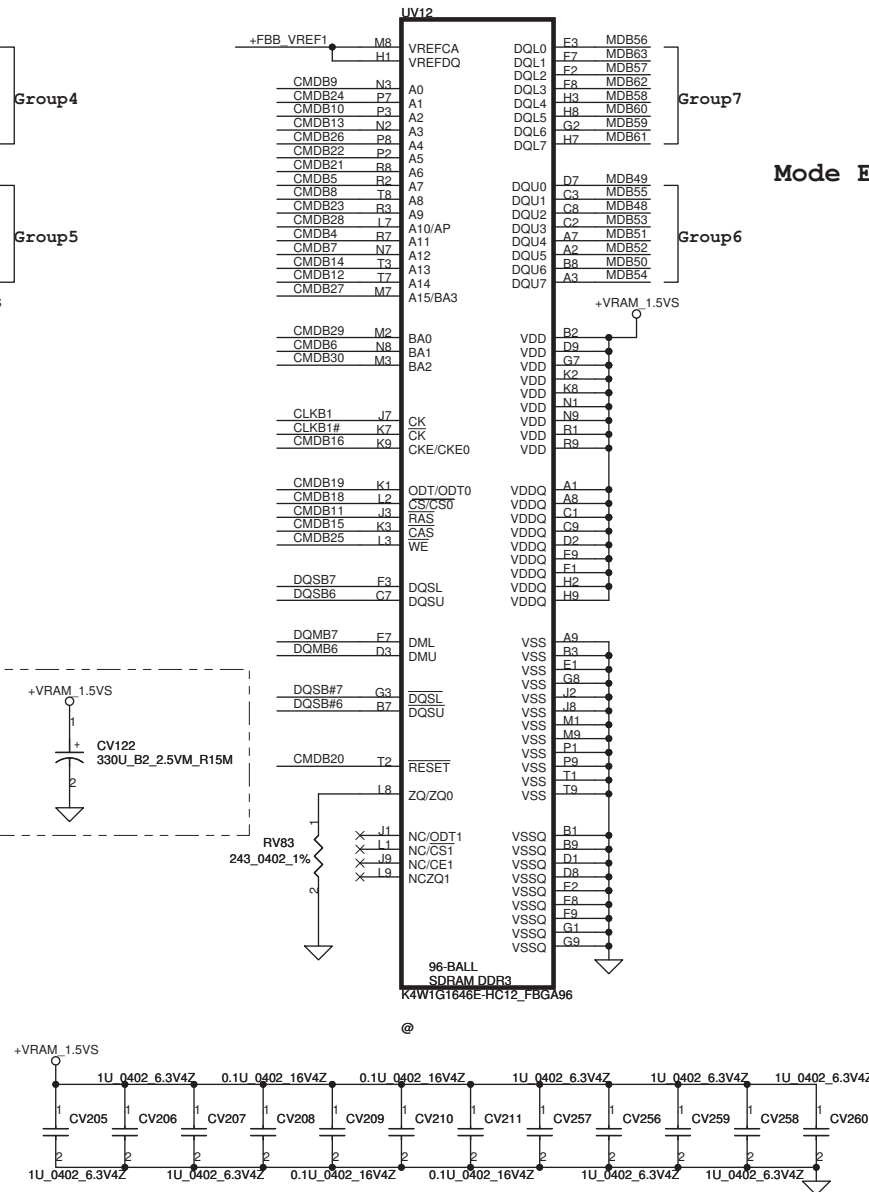
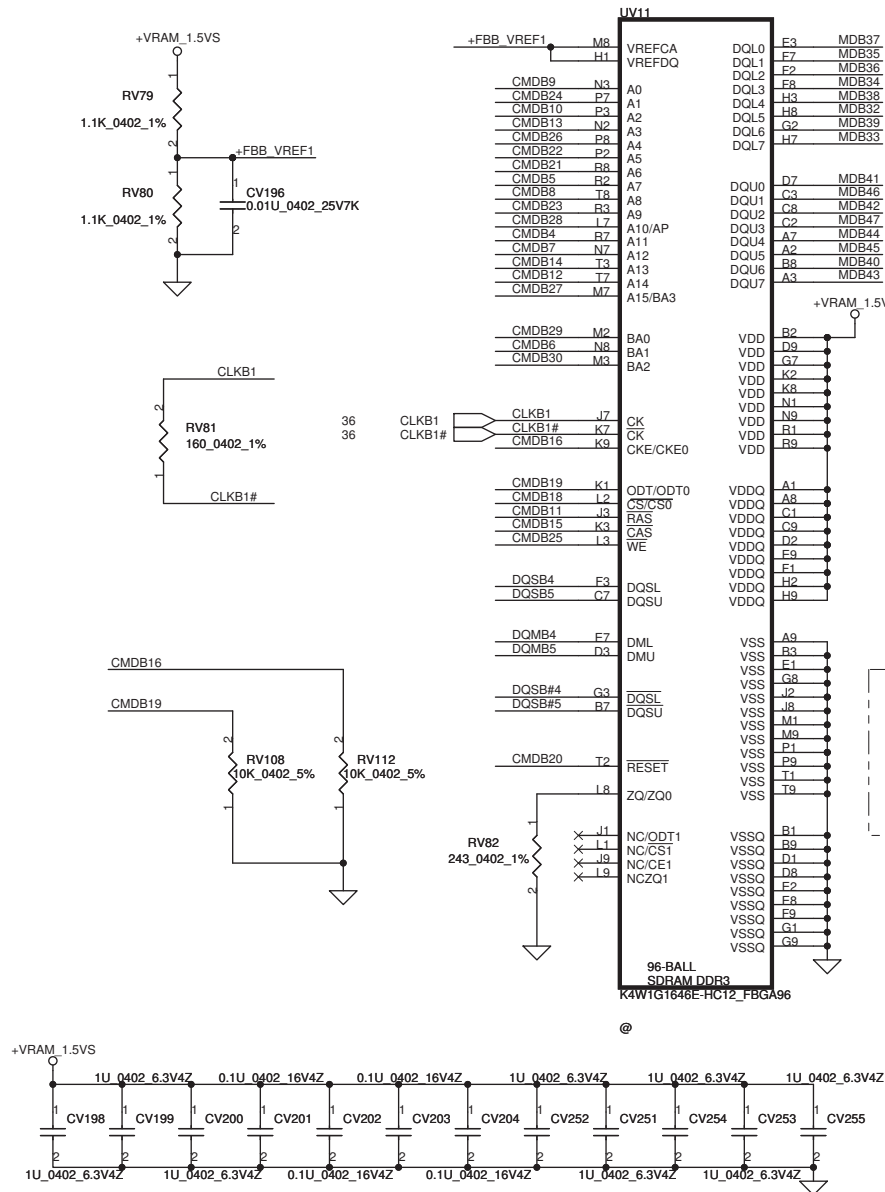
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Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits



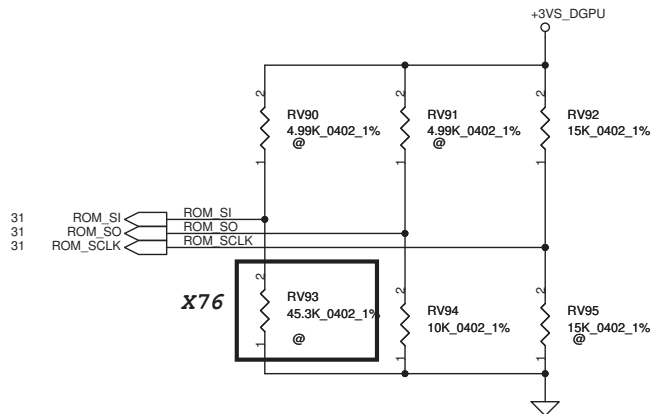
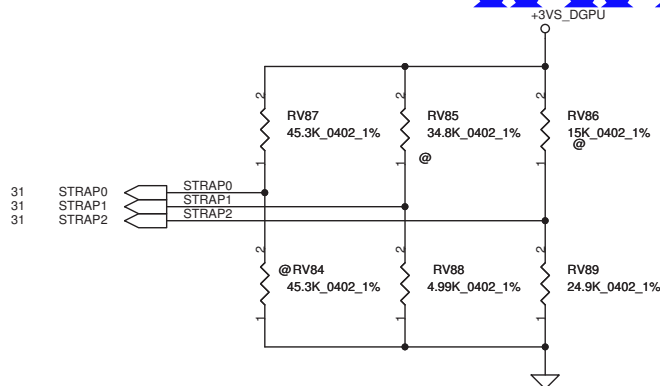
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Strapping pin	Strapping Bit3	Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]
				USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K



N12P-GS-A1 :
ROM_SO : PL-10K
ROM_CLK : PH-15K
ROM_SI : PL45.3K (Samsung 2GB)
Strap 2 : PL-5K
Strap 1 : PH-35K
Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

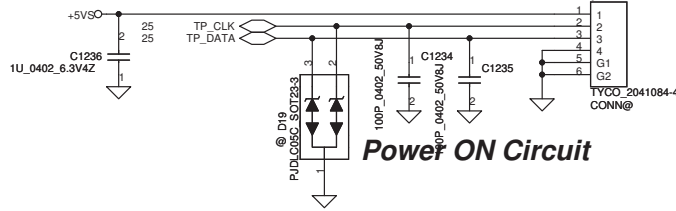
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

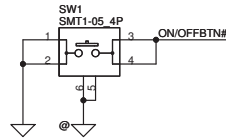
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/05/27	Deciphered Date	2011/07/06	Title VGA(12/12)-MISC		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-6961P	Rev 0.4
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Touch pad Connector

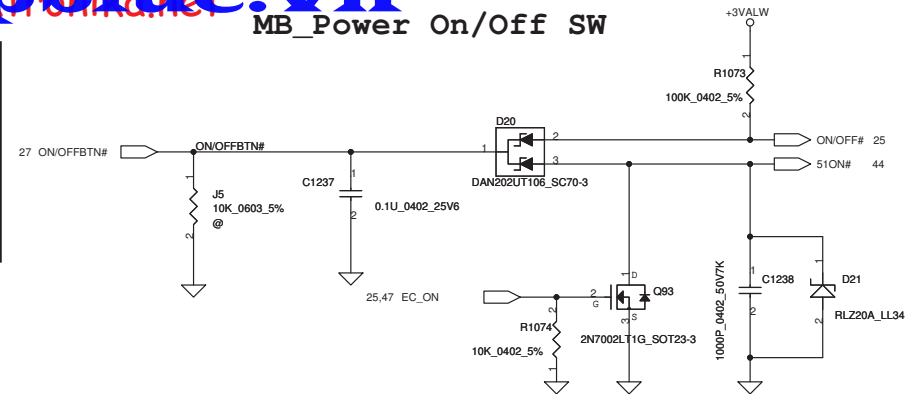


Power ON Circuit

For Debug Only

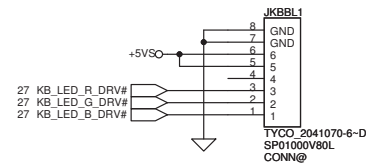


MB_Power On/Off SW

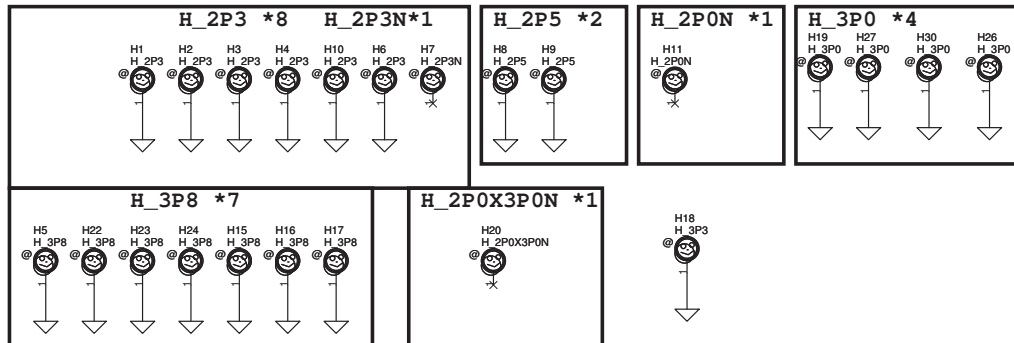


KSO8 @C736	100P_0402_25V8K	100P_0402_25V8K	C737@ KSI7
KSI3 @C738	100P_0402_25V8K	100P_0402_25V8K	C739@ KSI6
KSO9 @C740	100P_0402_25V8K	100P_0402_25V8K	C741@ KSI5
KSI2 @C742	100P_0402_25V8K	100P_0402_25V8K	C743@ KSO0
KSI1 @C744	100P_0402_25V8K	100P_0402_25V8K	C745@ KSO1
KSO10 @C746	100P_0402_25V8K	100P_0402_25V8K	C747@ KSO2
KSO11 @C750	100P_0402_25V8K	100P_0402_25V8K	C751@ KSI4
KSI0 @C752	100P_0402_25V8K	100P_0402_25V8K	C753@ KSO3
KSO12 @C754	100P_0402_25V8K	100P_0402_25V8K	C755@ KSO4
KSO13 @C756	100P_0402_25V8K	100P_0402_25V8K	C757@ KSO5
KSO14 @C760	100P_0402_25V8K	100P_0402_25V8K	C761@ KSO6
KSO15 @C762	100P_0402_25V8K	100P_0402_25V8K	C763@ KSO7
KSO16 @C764	100P_0402_25V8K	100P_0402_25V8K	

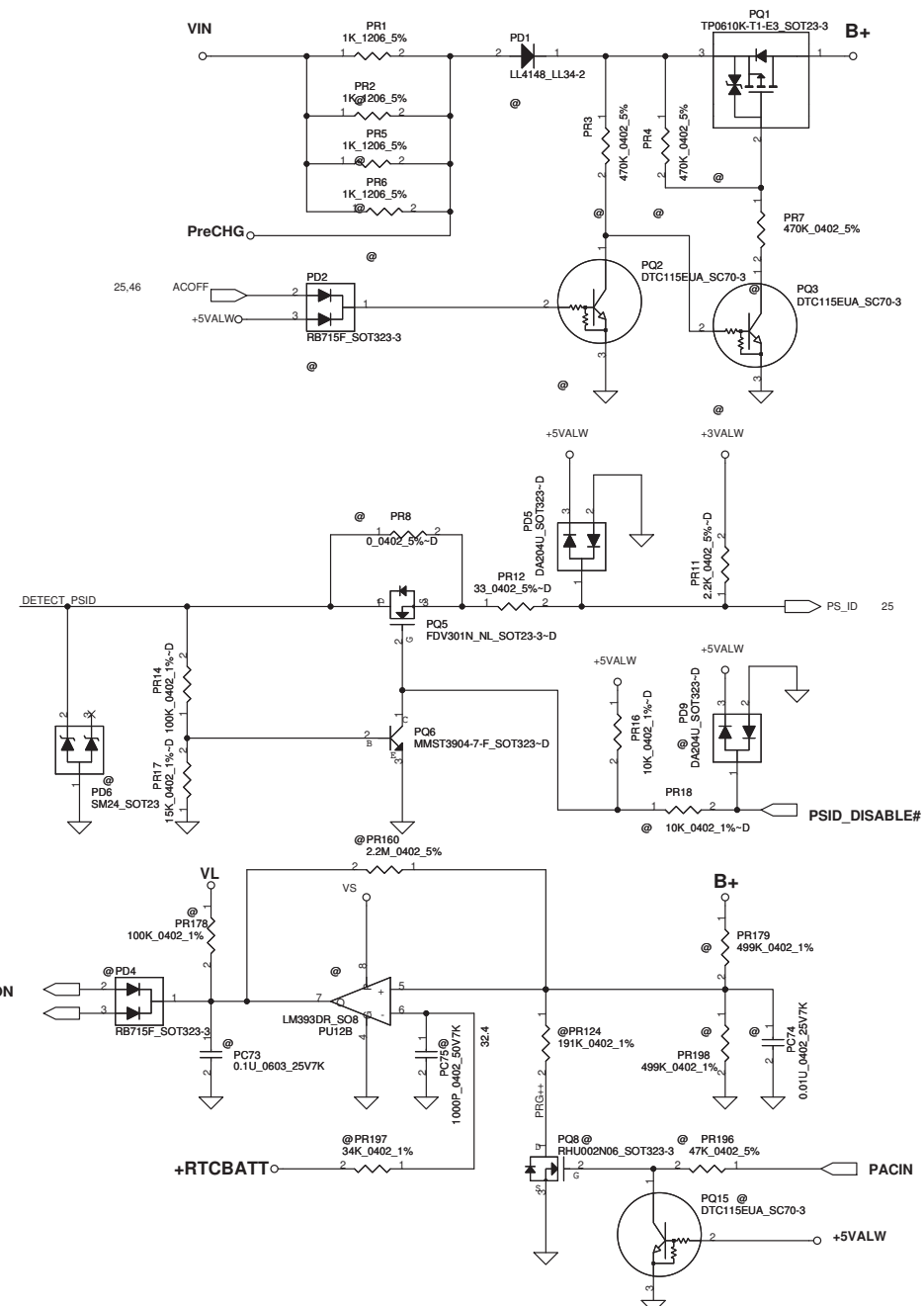
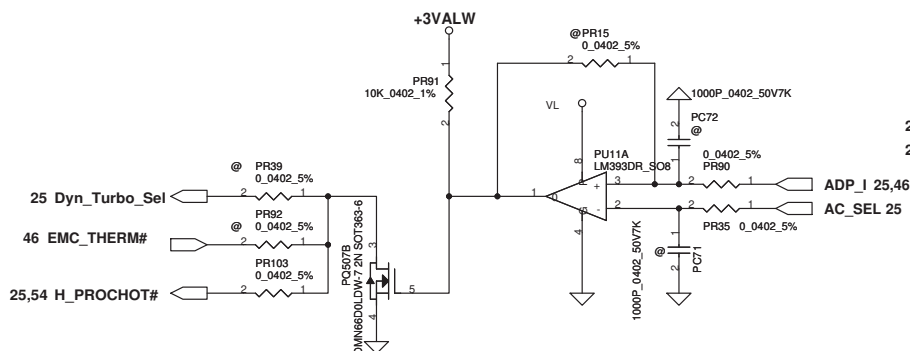
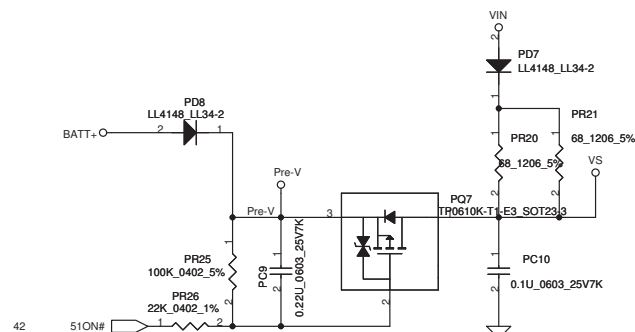
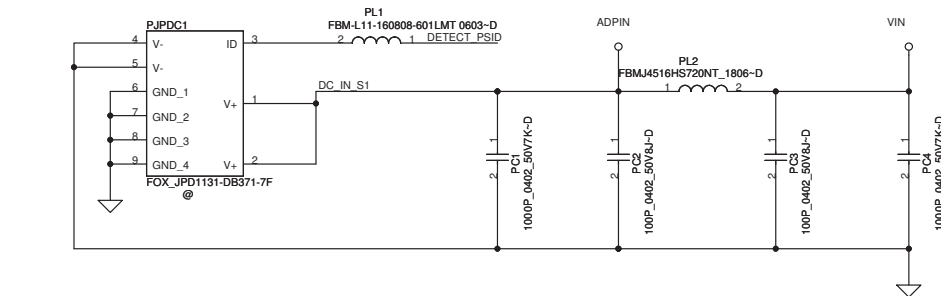
KSI7	1
KSI6	2
KSI4	3
KSI2	4
KSI5	5
KSI1	6
KSI3	7
KSI0	8
KSO5	9
KSO4	10
KSO7	11
KSO6	12
KSO8	13
KSO3	14
KSO1	15
KSO2	16
KSO0	17
KSO12	18
KSO13	19
KSO15	20
KSO14	21
KSO9	22
KSO11	23
KSO10	24
GND	25
GND	26



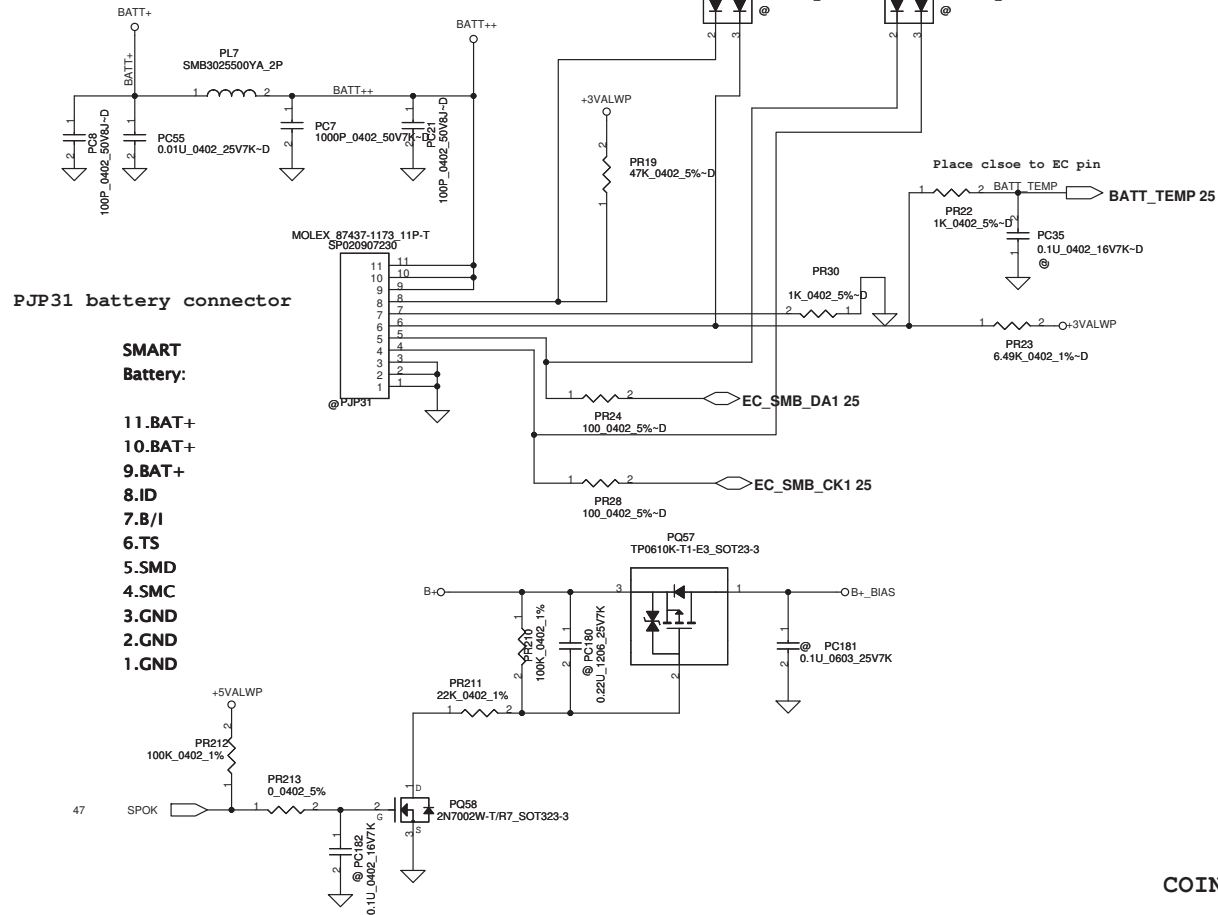
KSI[0..7] KSI[0..7] 25
KSO[0..16] KSO[0..16] 25



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Date: Monday, January 24, 2011				Sheet	42 of 54

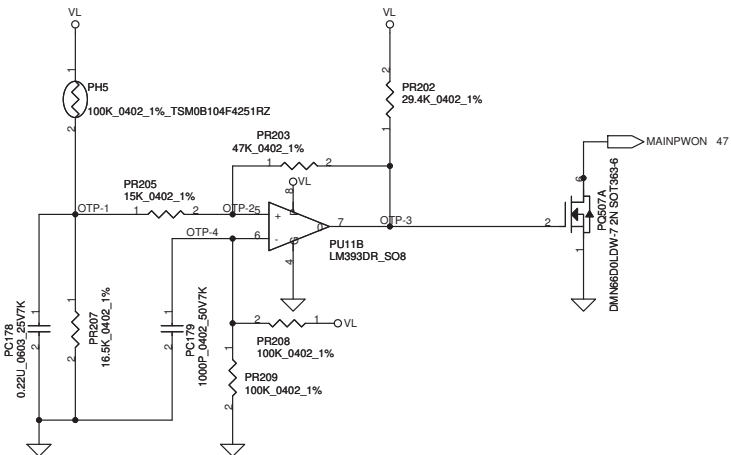


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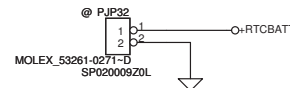


Battery Connect/OTP

PH3 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



COIN RTC Battery

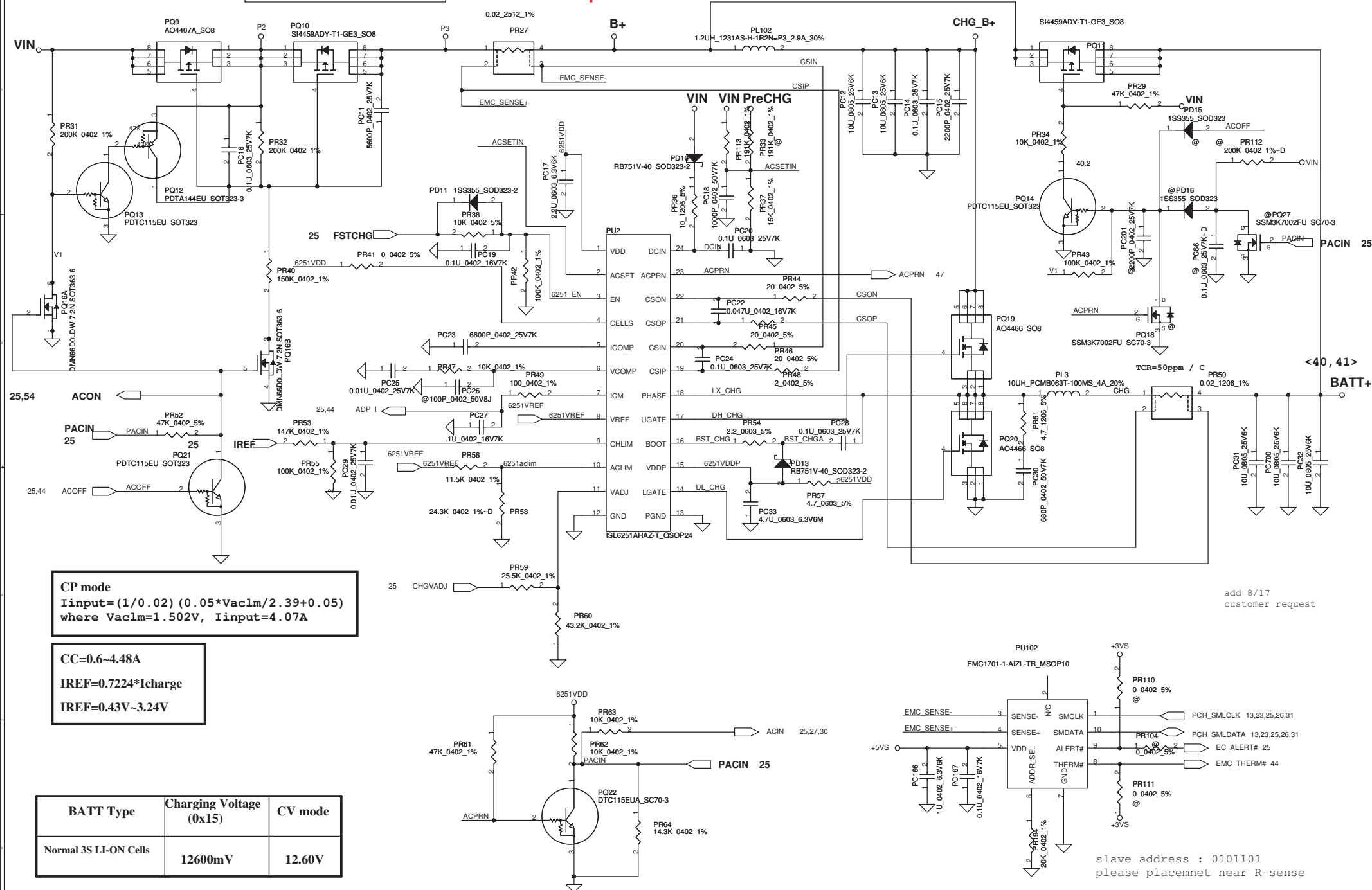


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I_{ada}=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9 * I_{adapter} * R_{sense}

www.kaptopblue.vn



CP mode

$I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6-4.48A

$I_{REF} = 0.7224 * I_{charge}$

$I_{REF} = 0.43V \sim 3.24V$

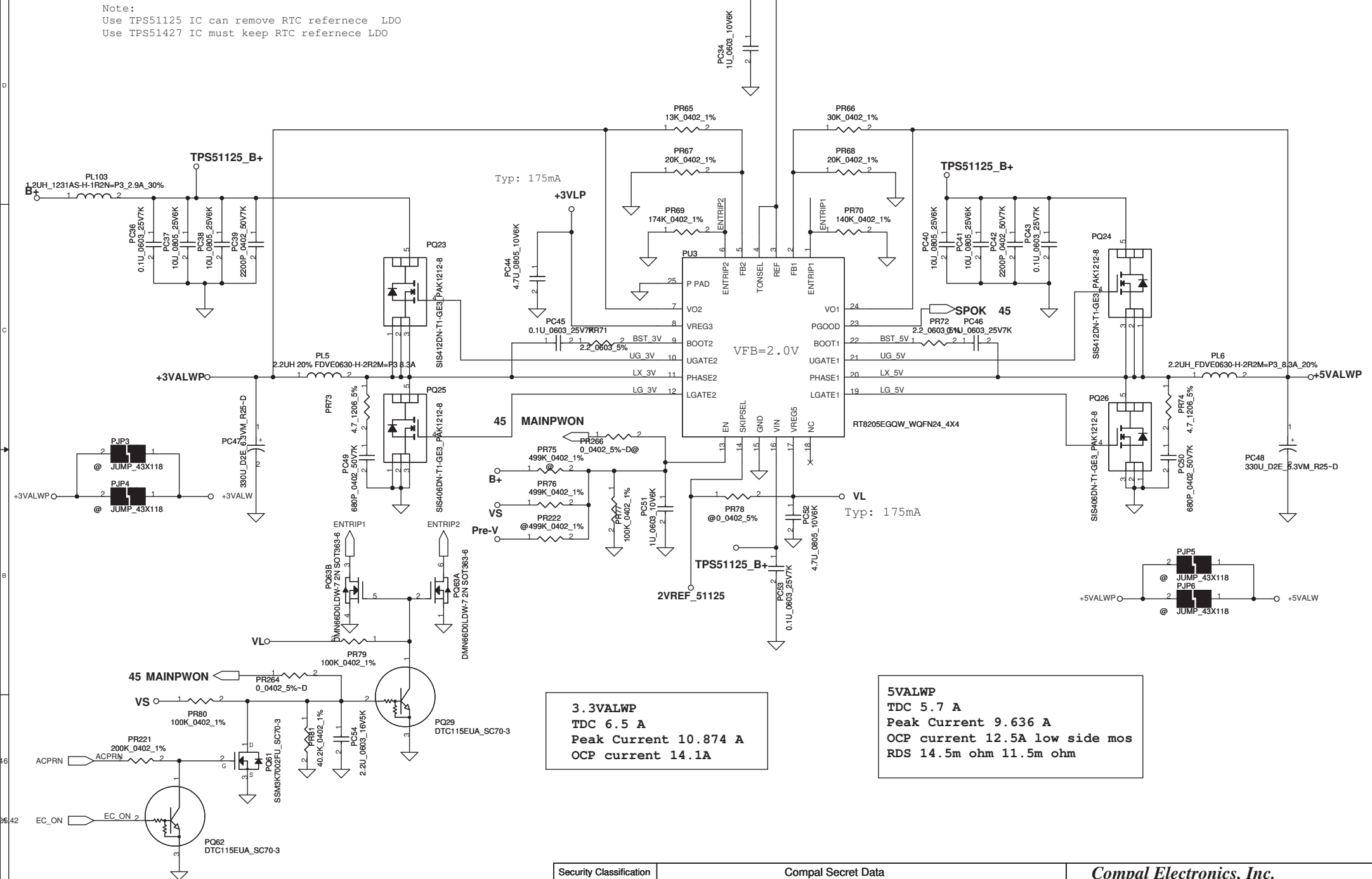
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

add 8/17
customer request

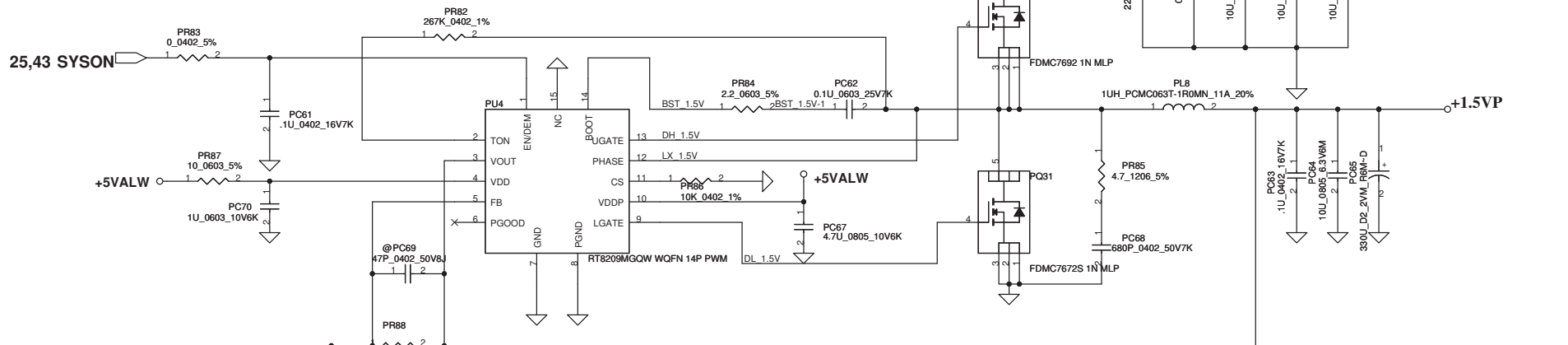
slave address : 0101101
please placemnet near R-sense

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Size	Custom	Document Number	LA-6961P	Rev	
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Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

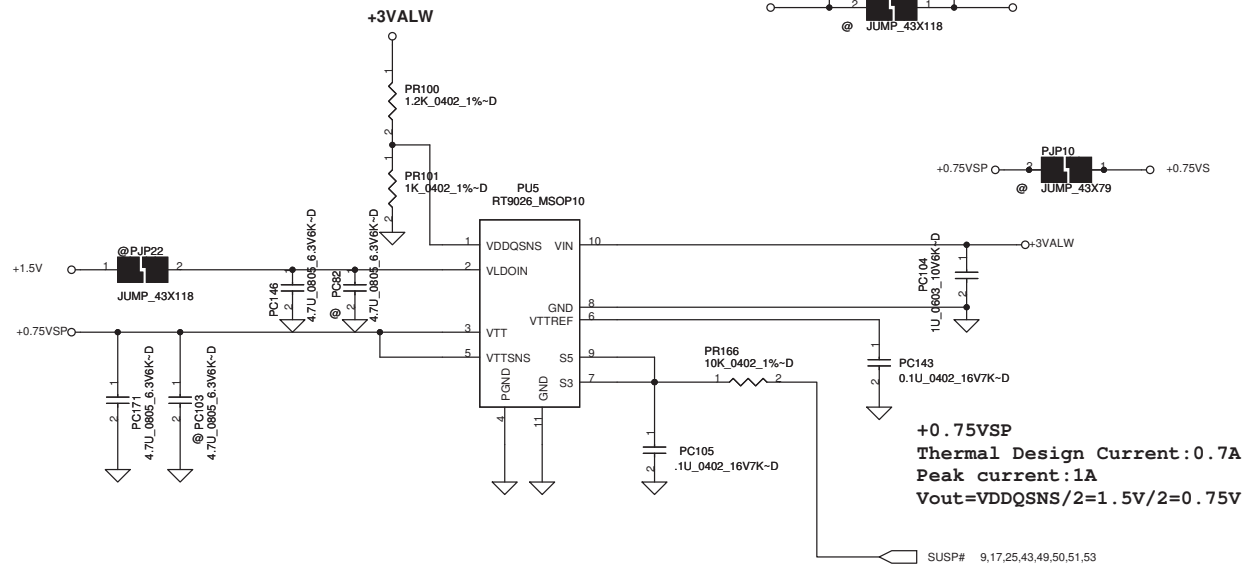
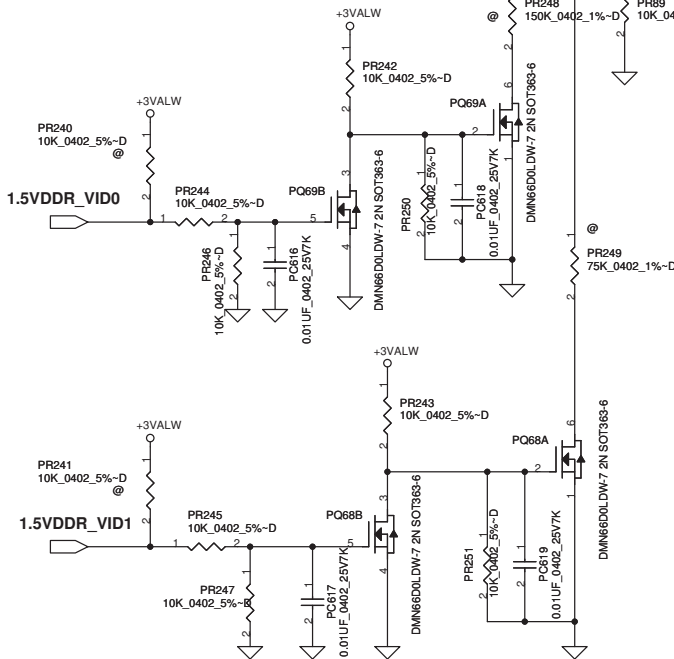
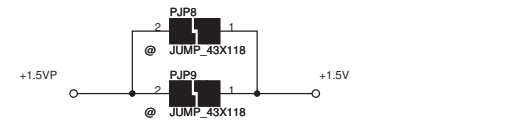


Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> 3VALWP/5VALWP	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	Title	3VALWP/5VALWP Document Number LA-6961P
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				Customer	
				Date:	Monday, January 24, 2011
				Sheet	47 of 54



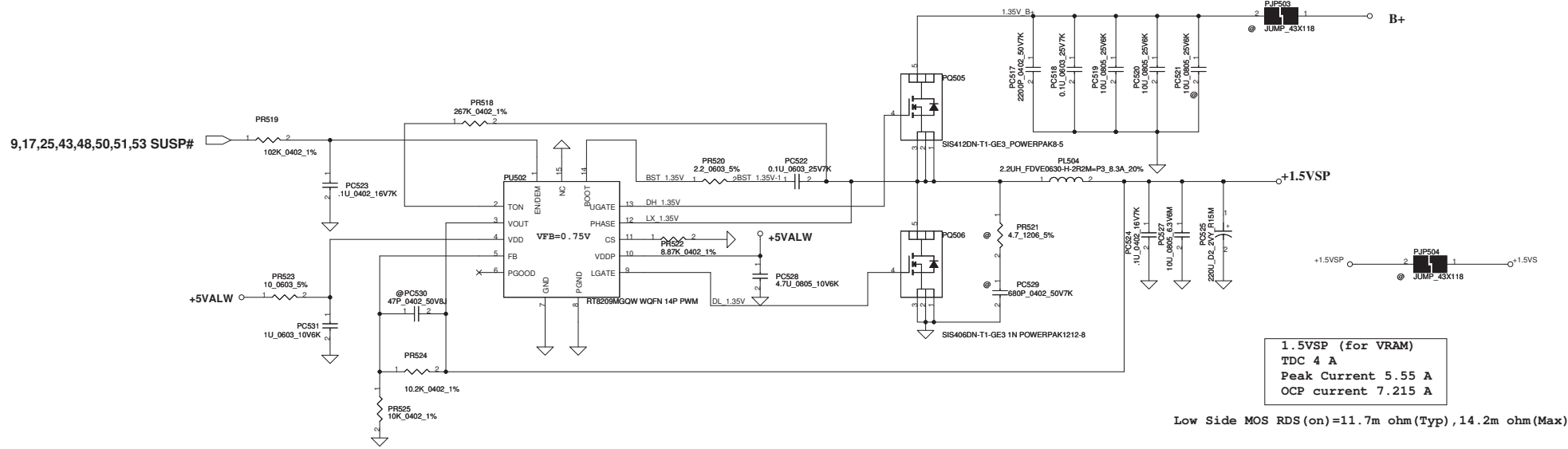
DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

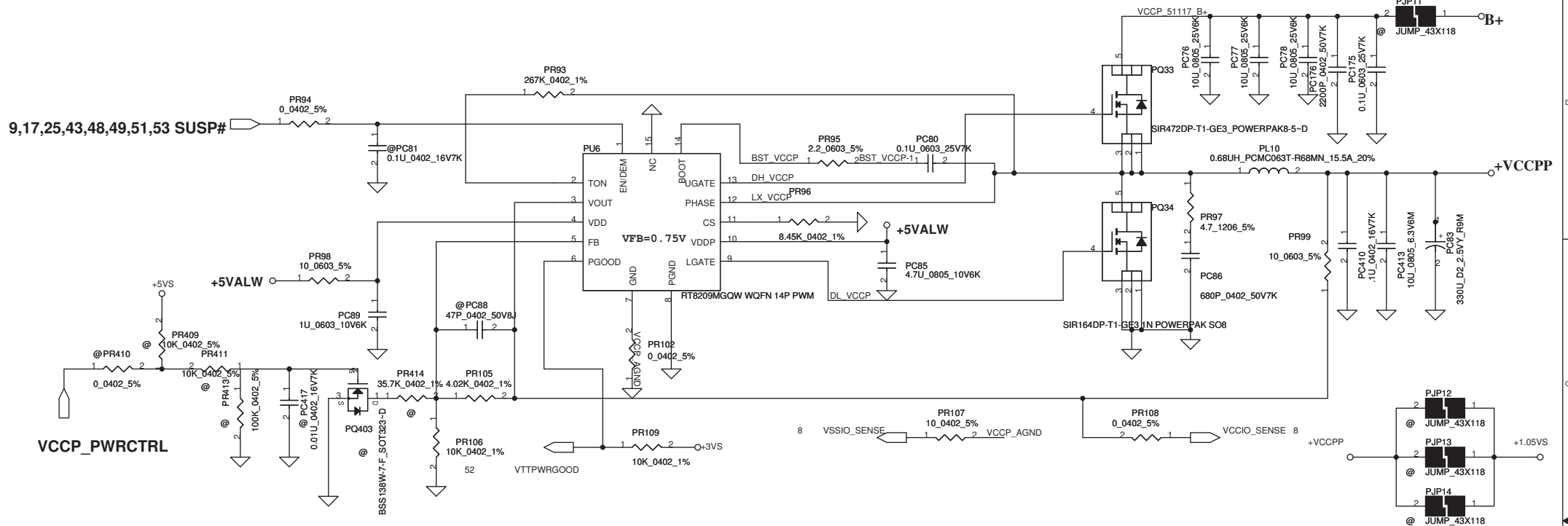
1.5VP
TDC 8.9A
Peak Current 12.72 A
OCF current 16.5A
low side mos RDS 4.5ohm 3.6ohm



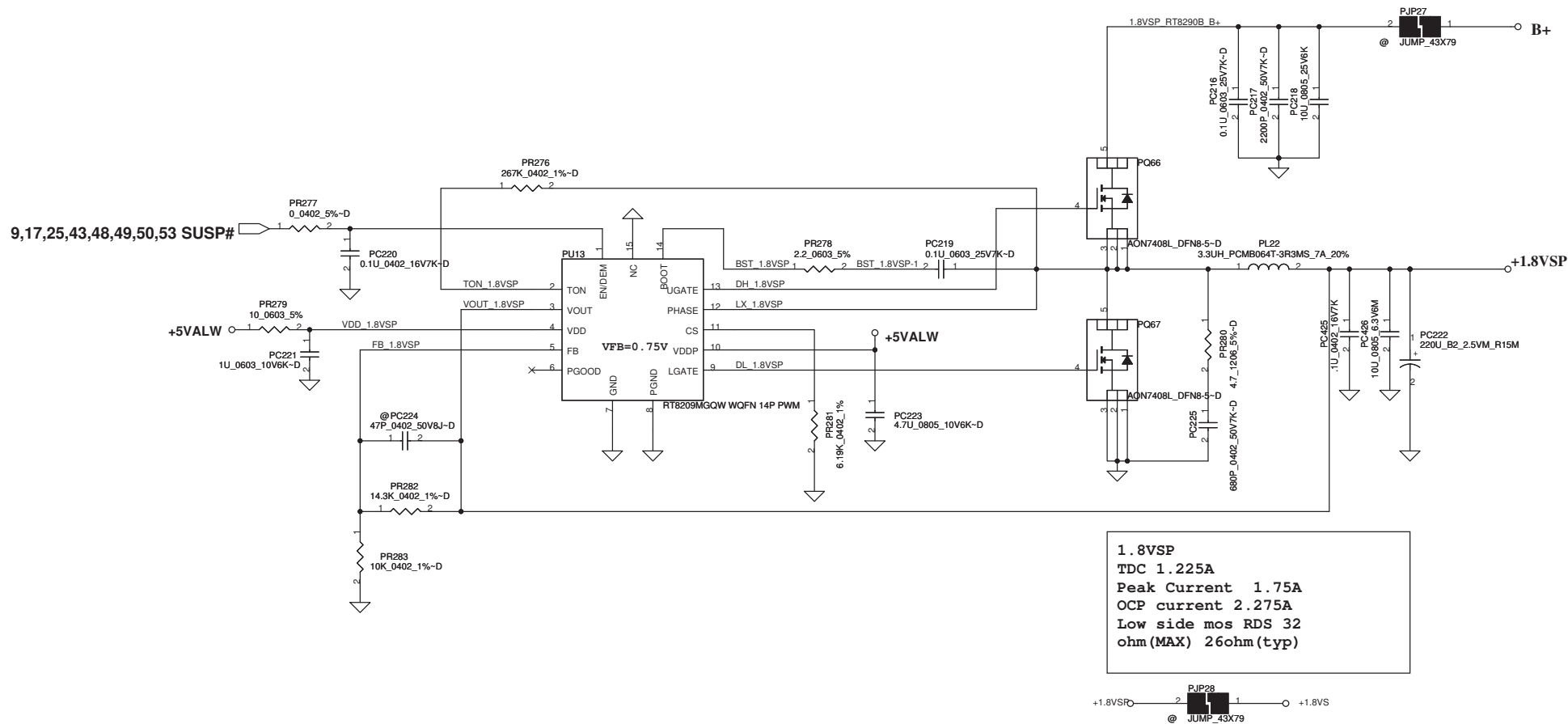
+0.75VSP
Thermal Design Current: 0.7A
Peak current: 1A
Vout=VDDQSNS/2=1.5V/2=0.75V

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				Date:	Monday, January 24, 2011
				Sheet	48 of 54

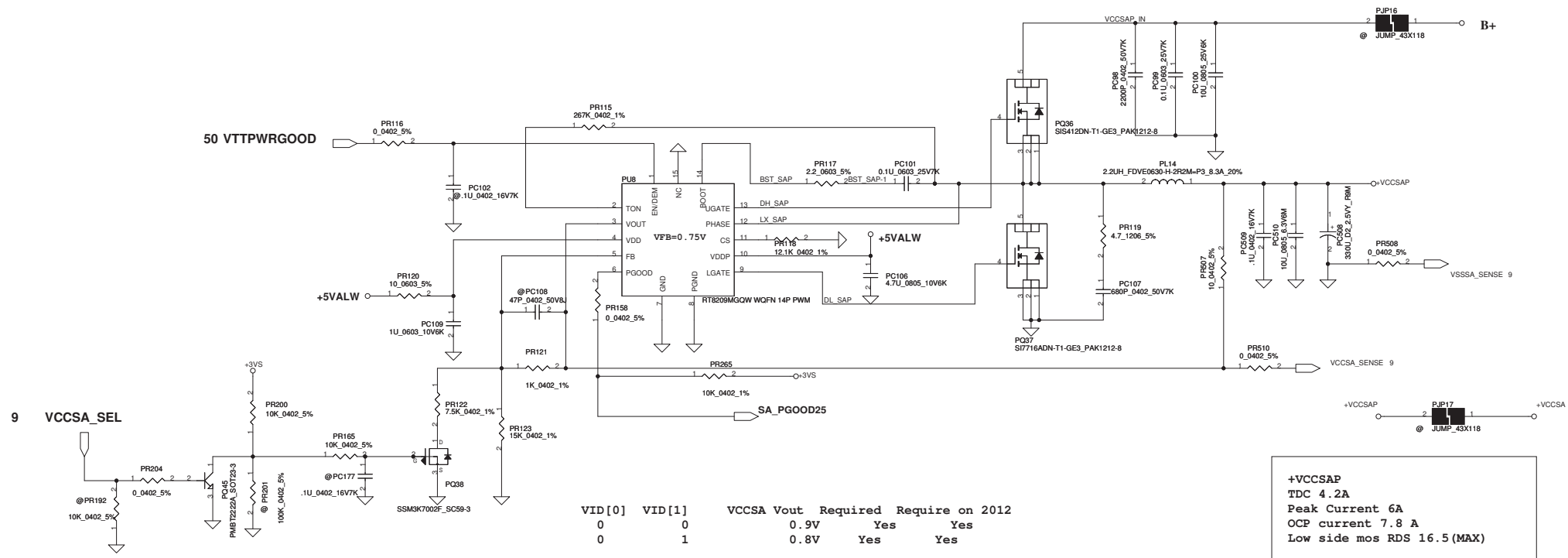




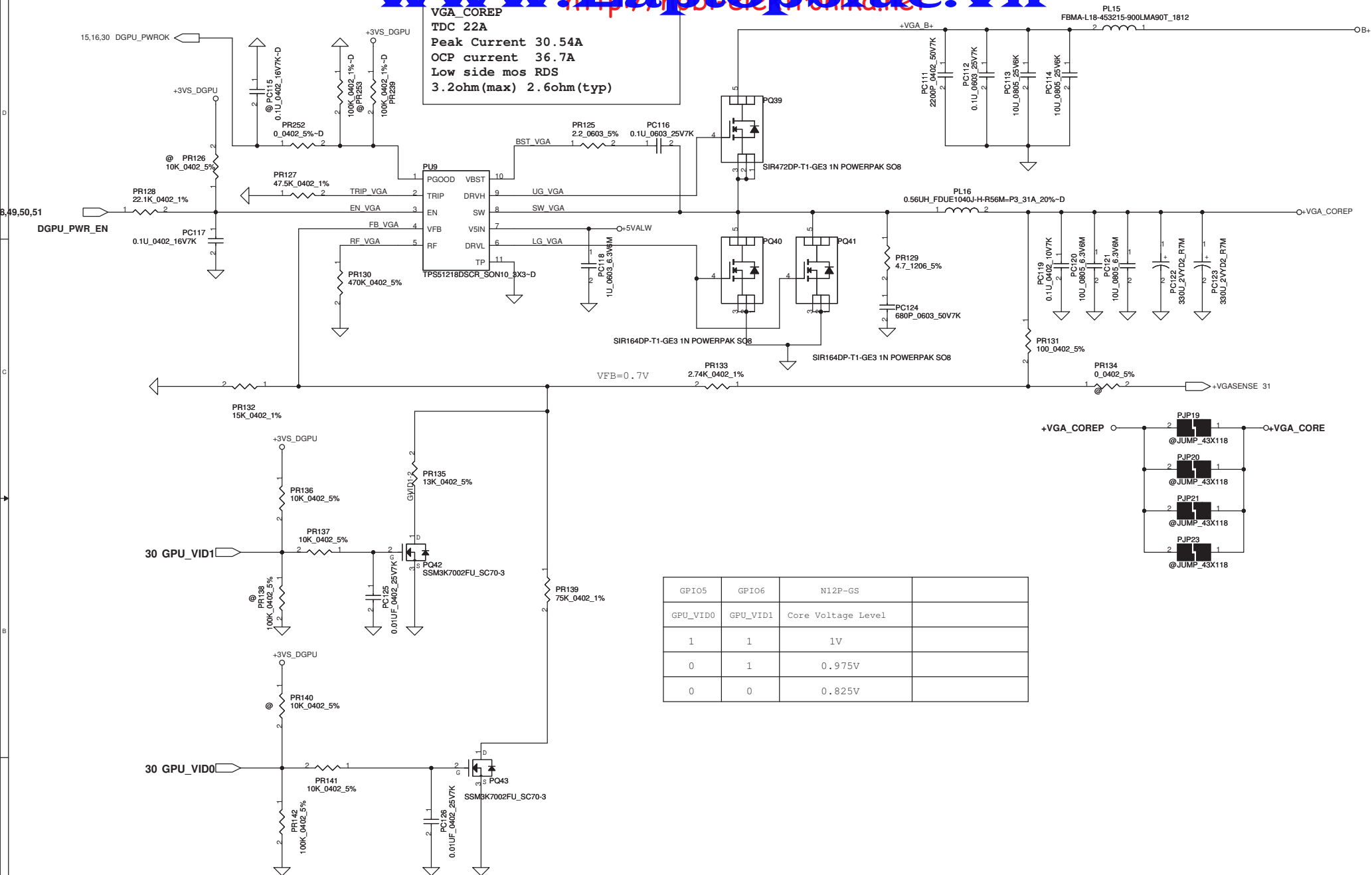
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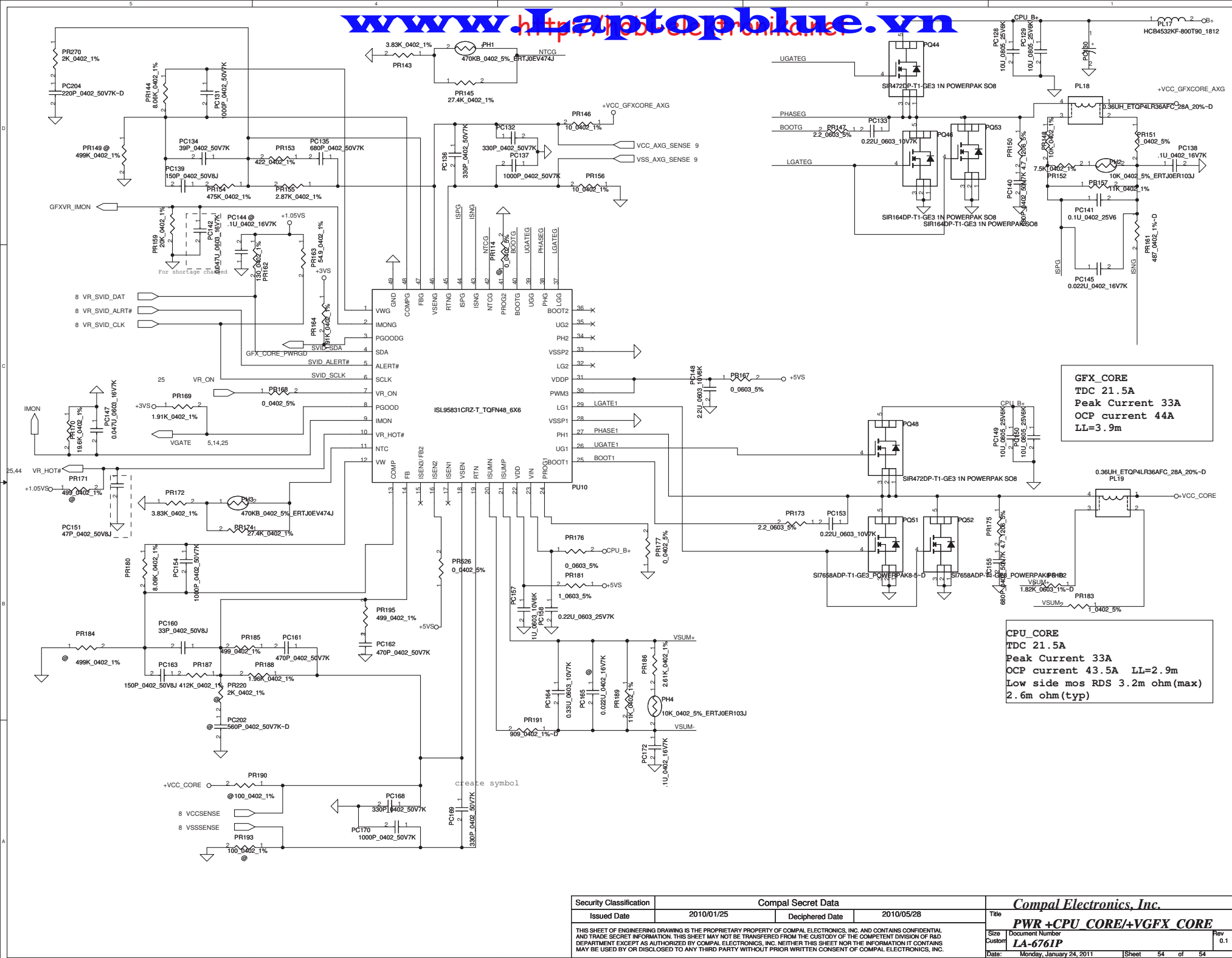
Security Classification		Compal Secret Data			
Issued Date	2009/12/01	Deciphered Date	2010/05/28	Title	PWR-+1.8VSP
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VGA_COREP
TDC 22A
Peak Current 30.54A
OCP current 36.7A
Low side mos RDS
3.2ohm(max) 2.6ohm(typ)



GPIO5	GPIO6	N12P-GS	
GPU_VID0	GPU_VID1	Core Voltage Level	
1	1	1V	
0	1	0.975V	
0	0	0.825V	



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Issued Date	2010/01/25	Deciphered Date	2010/05/28	Size	Rev
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of CL18,CL19	2010/10/15	PT
9	High pot	21	Change CL39 to SB120102KIL	2010/10/15	PT
10	DFX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCB change version	12	Change BOM UH1 SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DG updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resistor connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUO requirement	20	Add R2005,R2006 to reserve EN_INVFWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUO requirement	20	Add R2013,R2014,Q305 to reserve INVFWR_B+ Discharge Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AF1DAPA	24	Add R1962,R1963 to UPD720200AF1DAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_BGPV	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1Kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change RI095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,RI095 to 100Kohm,C287,C288, XI resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to D7I	2010/10/26	PT
26	Intel request	12-19	Change BOM UH1 SA00004IVIL	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM CI167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SB07I200J6L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPIO14	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	17I2 add D13, R395		
41					
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								HW Changed-List History-1		
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								Date: Monday, January 24, 2011		