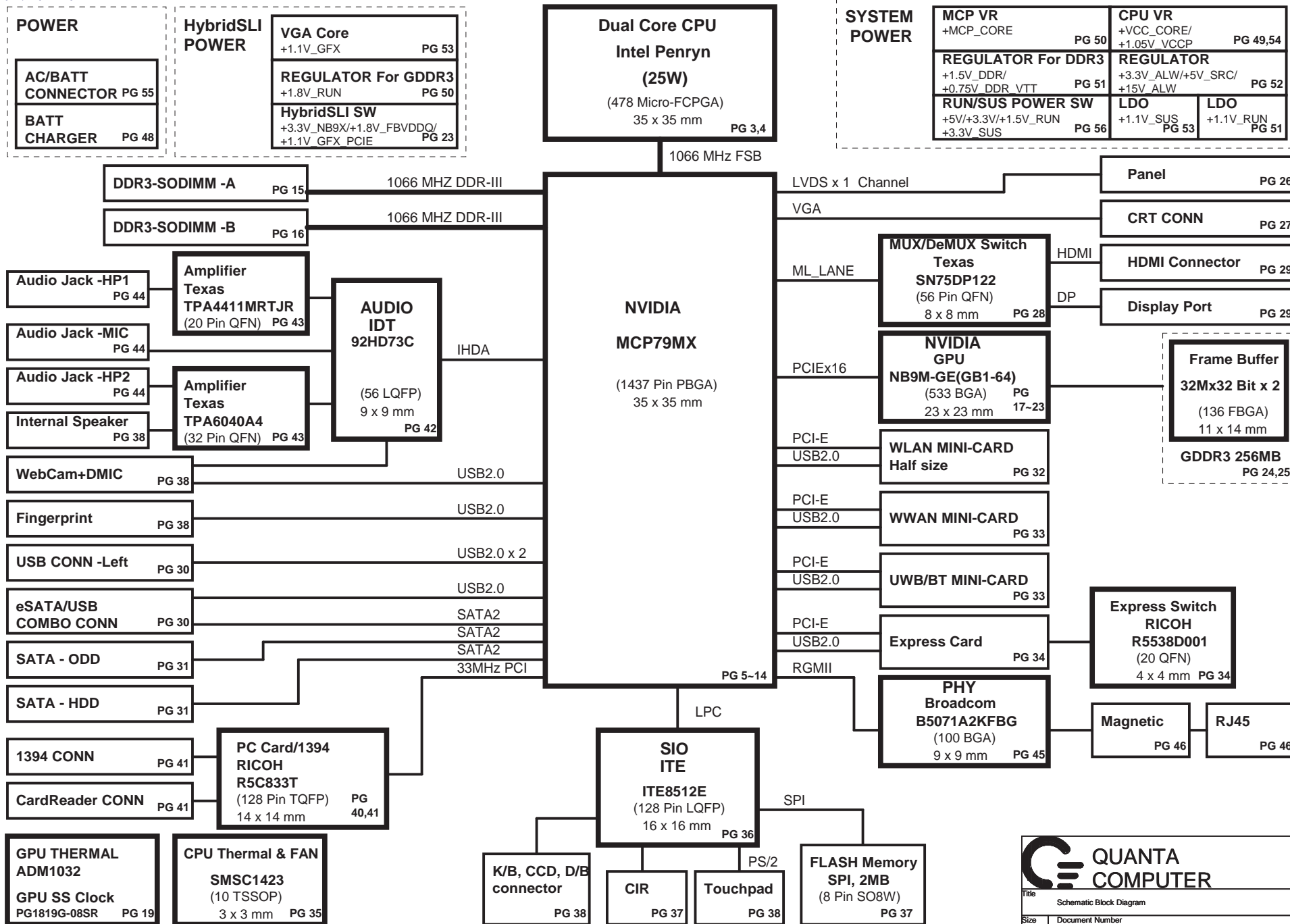


# IM3 (Jolie) Discrete 256M & UMA Block Diagram

VER : 3A

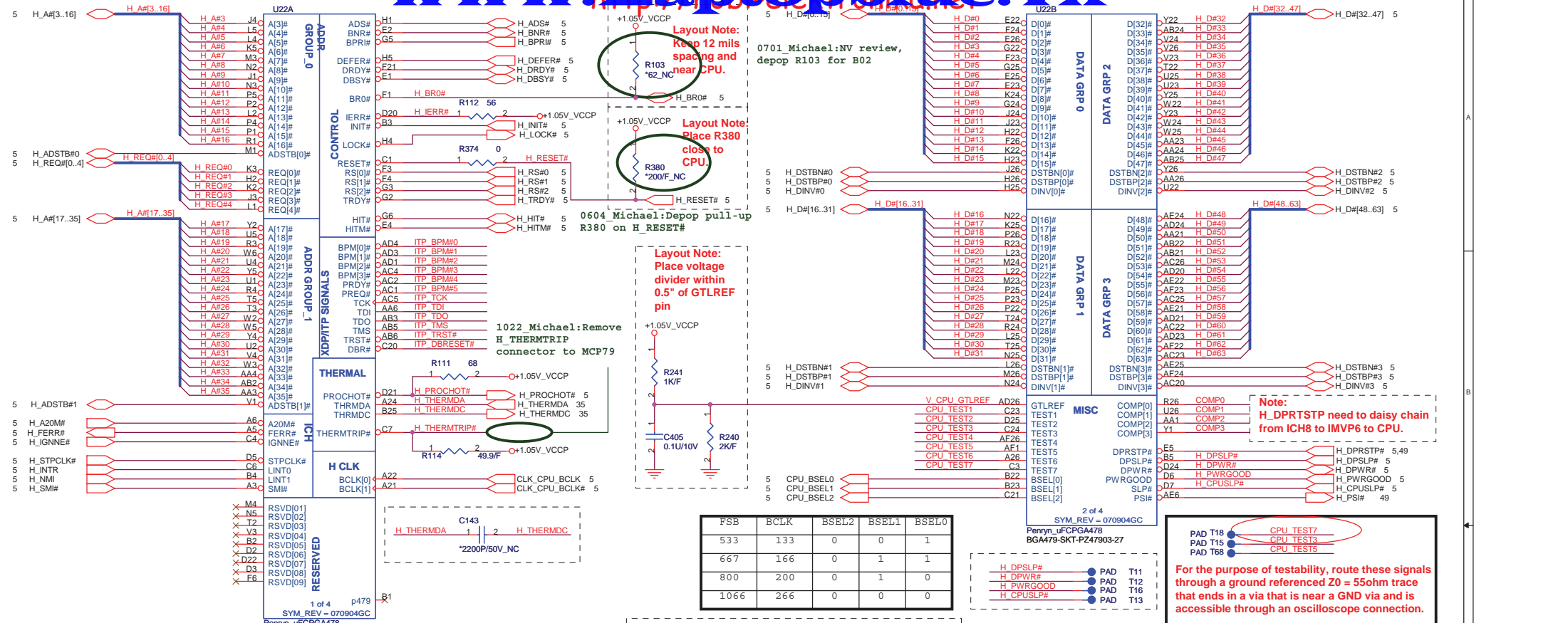
**QUANTA  
COMPUTER**

# INDEX

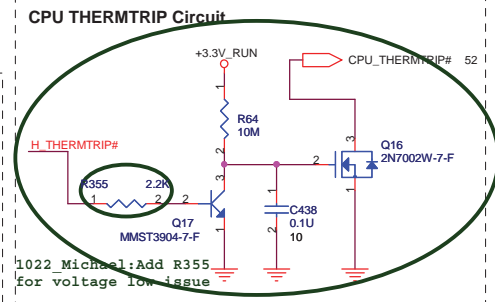
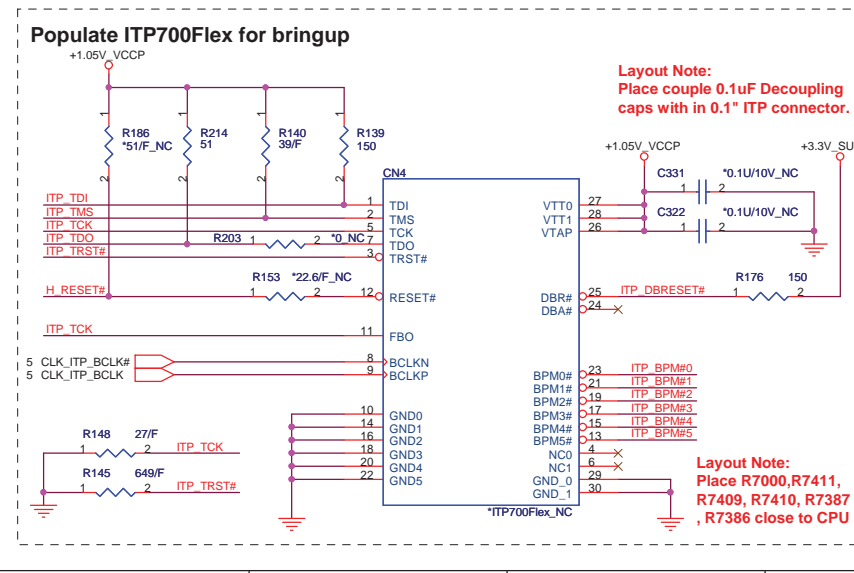
Page#	Description
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2	Front Page
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26	LCD CONN
27	CRT CONN
28	DeMux SW (SN75DP122)
29	HDMI & DP CONN
30	USB & eSATA & TV
31	HDD & ODD (SATA)
32	MINI-CARD (WLAN)
33	MINI-CARD (WPAN,WWAN)
34	Express Card
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36	SIO (ITE8512)
37	Flash ROM/ RTC/ CIR
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54	GRAM_1.8V (TPS51117)
55	DCIN,Batt
56	RUN POWER SW
57	Debug Port (Mini PCI)
58	PAD & SCREW

## Power States

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBVDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0



**0823\_Michael: Follow RM2 to change CPU THERMTRIP circuit**

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

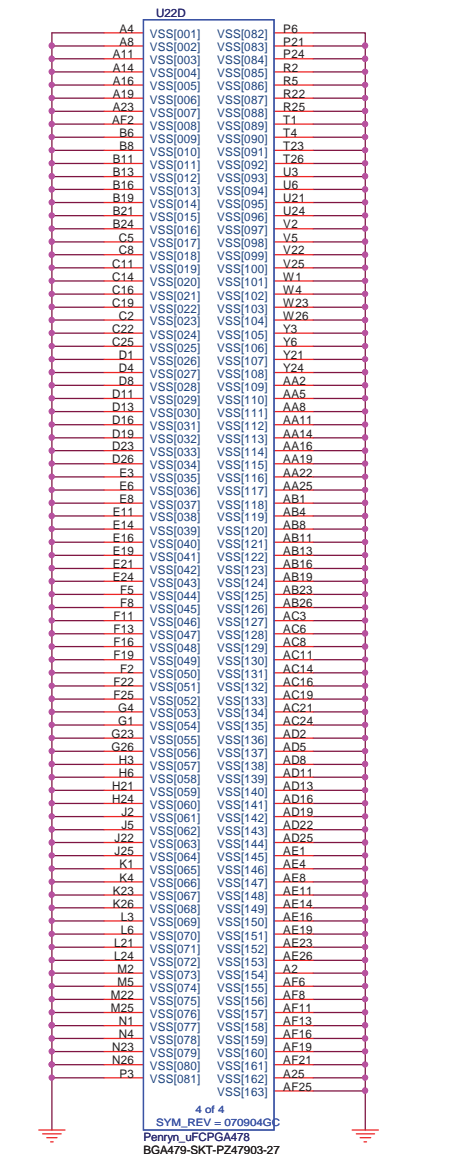
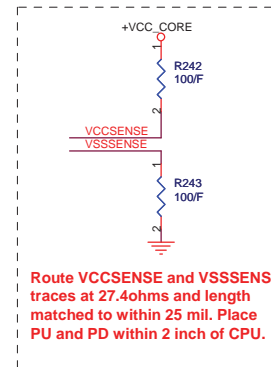
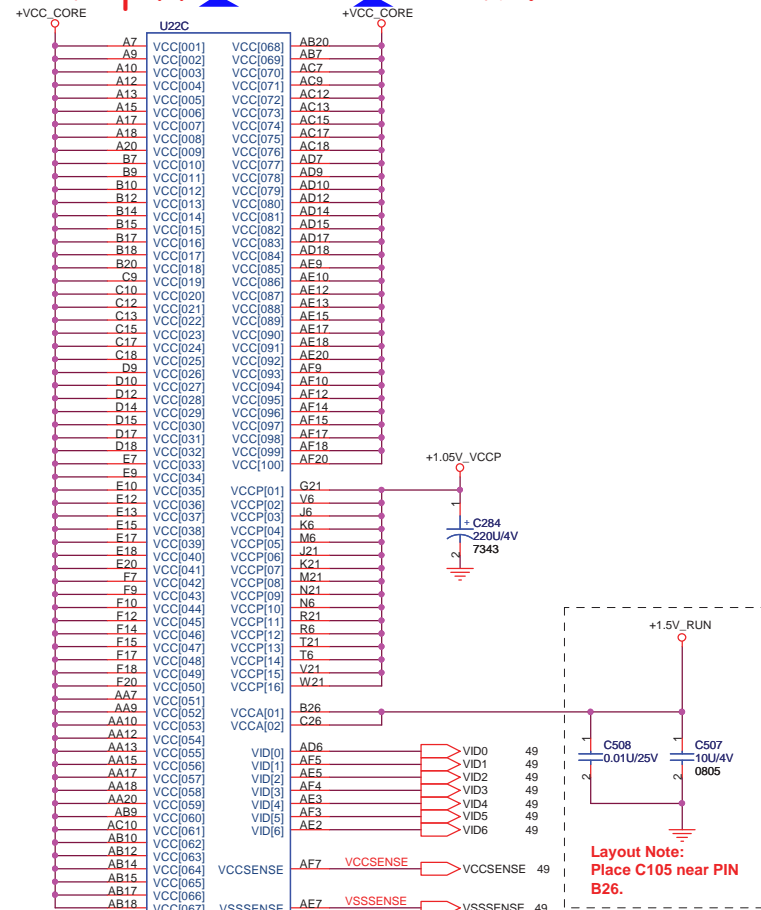
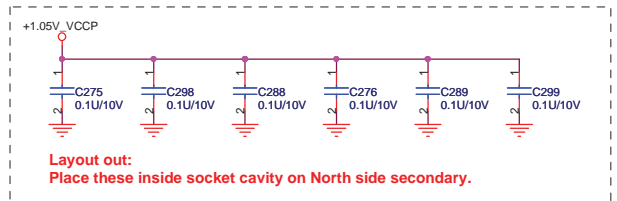
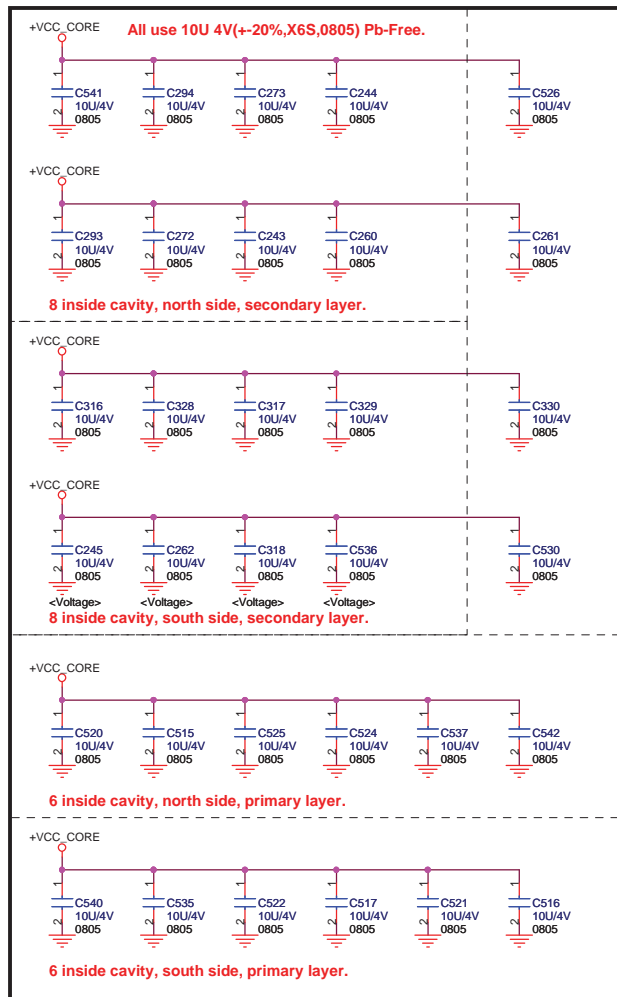
**ITP disable guidelines**

**QUANTA COMPUTER**

Penryn Processor (HOST BUS)

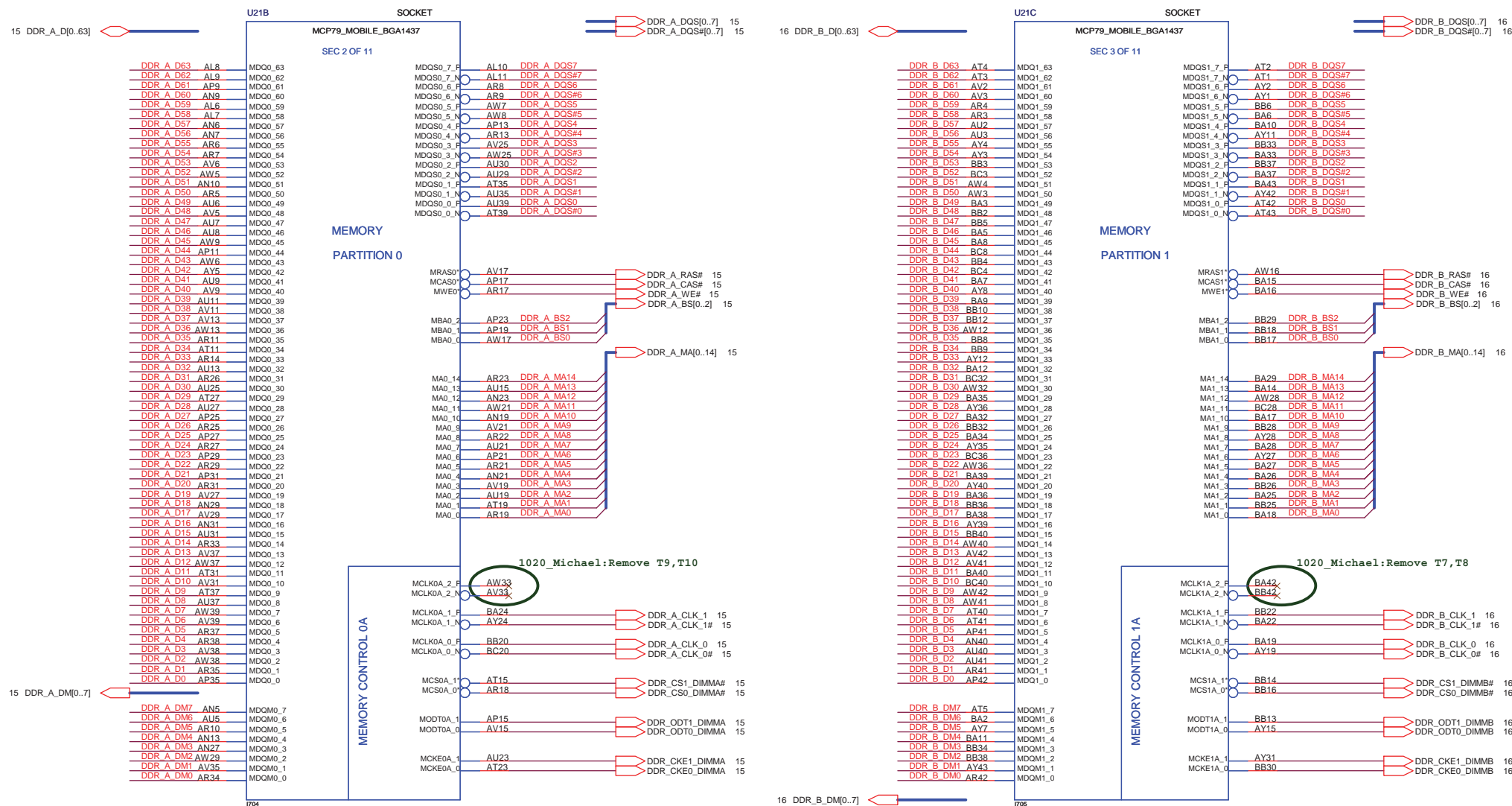
Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, October 23, 2008 Sheet 3 of 59







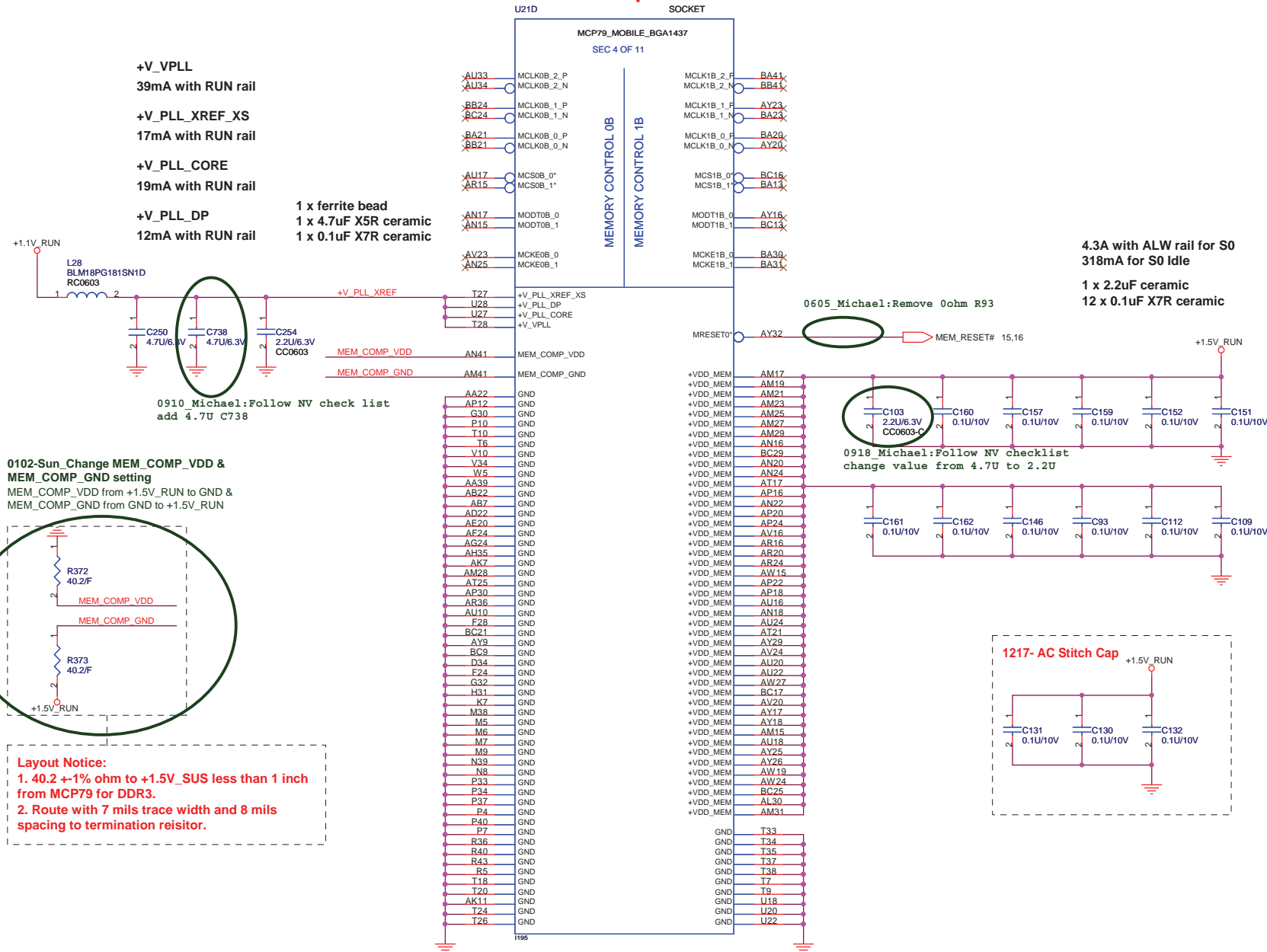


**Layout Notice:**  
**Memory Data Signal Group**  
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.  
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.  
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

**Memory Data Strobes**  
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

**Memory Clock Signal Group**  
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.  
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

**Memory Address/Command/Control Signal Group**  
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.  
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.  
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.



17 PCIE\_MRX\_GTX\_P[0..15]  
17 PCIE\_MRX\_GTX\_N[0..15]

**PCIE Layout Notice:**  
**MCP79 BGA Breakout (<27ps):**  
Route at 50 ohm impedance and 1.5x dielectric height spacing.  
**After Breakout:**  
Route at 50 Signal end and 90 ohm differential.  
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

0605 Michael:Remove 0ohm  
R185 on MXM\_ON#  
R433,R435,168 pull-down to GND  
R177 on PE\_RESET\_MXM#  
R458 on PCIE\_WAKE#

**Express Card**

**WLAN**

**UWB/BT**

**WWAN**

0314\_Change MXM\_PRESENT#  
pull down RES (R210)  
to 1k ohm base on  
NV suggestion

0825 Michael:Add KB  
detect function

0918 Michael:Remove  
KB detect function

0920 Michael:Add KB  
detect function

**Express Card**

**WLAN**

**UWB/BT**

**WWAN**

482mA with RUN rail

0312-Sun\_Change footprint to  
normal short type "short40x18"

1 x 2.2uF X5R ceramic  
2 x 1uF X7R ceramic  
2 x 0.1uF X7R ceramic

0918 Michael:Follow NV checklist  
change value from 4.7U to 2.2U and add 1U

82mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
1 x 2.2uF X7R ceramic

0918 Michael:Follow NV checklist  
change value from 4.7U to 2.2U

pad-s1  
1221-Sun\_Add dummy  
part for +AVDD\_PEX

PCIE MRX GTX P0 E7  
PCIE MRX GTX N0 E7  
PCIE MRX GTX P1 D7  
PCIE MRX GTX N1 C7  
PCIE MRX GTX P2 E6  
PCIE MRX GTX N2 D6  
PCIE MRX GTX P3 E5  
PCIE MRX GTX N3 D5  
PCIE MRX GTX P4 E4  
PCIE MRX GTX N4 D4  
PCIE MRX GTX P5 E3  
PCIE MRX GTX N5 D3  
PCIE MRX GTX P6 E5  
PCIE MRX GTX N6 D5  
PCIE MRX GTX P7 E5  
PCIE MRX GTX N7 D5  
PCIE MRX GTX P8 E5  
PCIE MRX GTX N8 D5  
PCIE MRX GTX P9 L11  
PCIE MRX GTX N9 L10  
PCIE MRX GTX P10 L9  
PCIE MRX GTX N10 L8  
PCIE MRX GTX P11 L7  
PCIE MRX GTX N11 L6  
PCIE MRX GTX P12 N11  
PCIE MRX GTX N12 N10  
PCIE MRX GTX P13 N9  
PCIE MRX GTX N13 N8  
PCIE MRX GTX P14 N7  
PCIE MRX GTX N14 N6  
PCIE MRX GTX P15 N5  
PCIE MRX GTX N15 N4

PCIE

SOCKET

PCIE MTX GRX C P0 C347  
PCIE MTX GRX N0 C340  
PCIE MTX GRX C P1 C373  
PCIE MTX GRX N1 C384  
PCIE MTX GRX C P2 C556  
PCIE MTX GRX N2 C565  
PCIE MTX GRX C P3 C552  
PCIE MTX GRX N3 C548  
PCIE MTX GRX C P4 C358  
PCIE MTX GRX N4 C367  
PCIE MTX GRX C P5 C333  
PCIE MTX GRX N5 C323  
PCIE MTX GRX C P6 C547  
PCIE MTX GRX N6 C544  
PCIE MTX GRX C P7 C543  
PCIE MTX GRX N7 C539  
PCIE MTX GRX C P8 C311  
PCIE MTX GRX N8 C319  
PCIE MTX GRX C P9 C534  
PCIE MTX GRX N9 C538  
PCIE MTX GRX C P10 C297  
PCIE MTX GRX N10 C307  
PCIE MTX GRX C P11 C291  
PCIE MTX GRX N11 C280  
PCIE MTX GRX C P12 C532  
PCIE MTX GRX N12 C529  
PCIE MTX GRX C P13 C523  
PCIE MTX GRX N13 C527  
PCIE MTX GRX C P14 C263  
PCIE MTX GRX N14 C267  
PCIE MTX GRX C P15 C519  
PCIE MTX GRX N15 C518

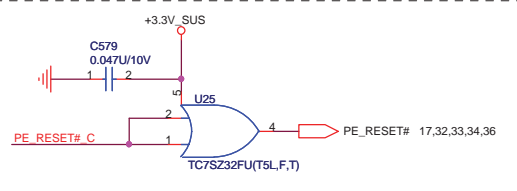
PCIE\_MTX\_GRX\_P[0..15]  
PCIE\_MTX\_GRX\_N[0..15]

PE0\_TX0\_P C5  
PE0\_TX0\_N D4  
PE0\_TX1\_P C4  
PE0\_TX1\_N B4  
PE0\_TX2\_P A4  
PE0\_TX2\_N B3  
PE0\_TX3\_P B2  
PE0\_TX3\_N C1  
PE0\_TX4\_P D1  
PE0\_TX4\_N D2  
PE0\_TX5\_P E1  
PE0\_TX5\_N E2  
PE0\_TX6\_P F2  
PE0\_TX6\_N F3  
PE0\_TX7\_P F4  
PE0\_TX7\_N G3  
PE0\_TX8\_P H4  
PE0\_TX8\_N H3  
PE0\_TX9\_P H2  
PE0\_TX9\_N H1  
PE0\_TX10\_P J1  
PE0\_TX10\_N J2  
PE0\_TX11\_P J3  
PE0\_TX11\_N K2  
PE0\_TX12\_P K3  
PE0\_TX12\_N L4  
PE0\_TX13\_P L3  
PE0\_TX13\_N M4  
PE0\_TX14\_P M3  
PE0\_TX14\_N M2  
PE0\_TX15\_P M1  
PE0\_TX15\_N M1

CLK\_PCIE\_VGA 17  
CLK\_PCIE\_VGA# 17  
CLK\_PCIE\_EXPCARD 34  
CLK\_PCIE\_EXPCARD# 34  
CLK\_PCIE\_MINI1 32  
CLK\_PCIE\_MINI1# 32  
CLK\_PCIE\_MINI2 33  
CLK\_PCIE\_MINI2# 33  
CLK\_PCIE\_MINI3 33  
CLK\_PCIE\_MINI3# 33

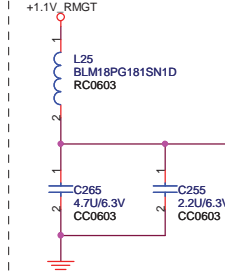
0624 Michael:Change  
L6 type from  
BLM21PG600SN1D to  
BLM21PG600SN1D

1304mA with RUN rail  
1x ferrite bead  
1x 10uF  
1 x 2.2uF X5R ceramic  
2 x 1uF X5R ceramic  
2 x 0.1uF X7R ceramic

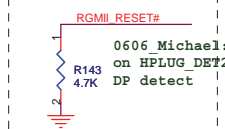
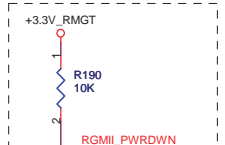




1 x ferrite bead  
1 x 4.7uF X5R ceramic  
1 x 2.2uF X7R ceramic



**Layout Notice:**  
124 ohm  $\pm 1\%$  to GND and within 750 mils of MCP79.  
0.01uF to GND and within 500 mils of MCP79.



0312-Sun\_Change footprint to normal short type "short40x18"



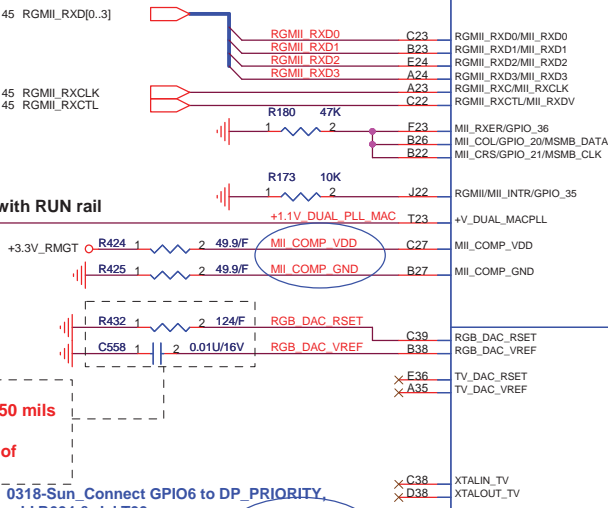
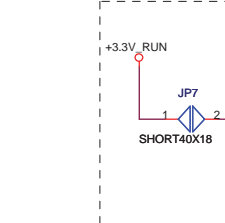
1 x 2.2uF X5R ceramic  
1 x 0.1uF X7R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U

95mA with RUN rail

2 x 2.2uF X5R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U



## LAN

## DACS

## FLAT PANEL

0318-Sun\_Connect GPIO6 to DP\_PRIORITY, add R604 & del T39



0606\_Michael:Add DR\_PLUG on HPLUG\_DET2 for DP detect



0312-Sun\_Change footprint to normal short type "short40x18"



1 x 2.2uF X5R ceramic  
1 x 0.1uF X7R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U

95mA with RUN rail

2 x 2.2uF X5R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U



8mA with RUN rail

1 x 4.7uF X5R ceramic  
1 x 0.1uF X7R ceramic

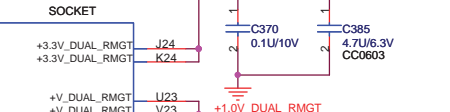
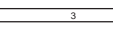
0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U



8mA with RUN rail

1 x 4.7uF X5R ceramic  
1 x 0.1uF X7R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U0.1U to 2.2U



131mA with ALW rail

1 x 2.2uF X5R ceramic  
1 x 0.1uF X7R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U to 2.2U



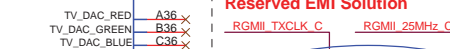
0319-Sun\_Change RGMII\_TXCLK damping RES to 22 ohm for EMI



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

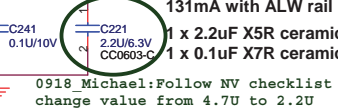
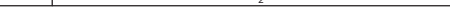
L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

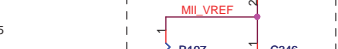
L43 BLM18PG181SN1D RC0603



131mA with ALW rail

1 x 2.2uF X5R ceramic  
1 x 0.1uF X7R ceramic

0918\_Michael:Follow NV checklist change value from 4.7U to 2.2U



0319-Sun\_Change RGMII\_TXCLK damping RES to 22 ohm for EMI



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

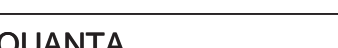
L43 BLM18PG181SN1D RC0603



103mA with RUN rail

1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

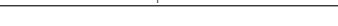
L43 BLM18PG181SN1D RC0603



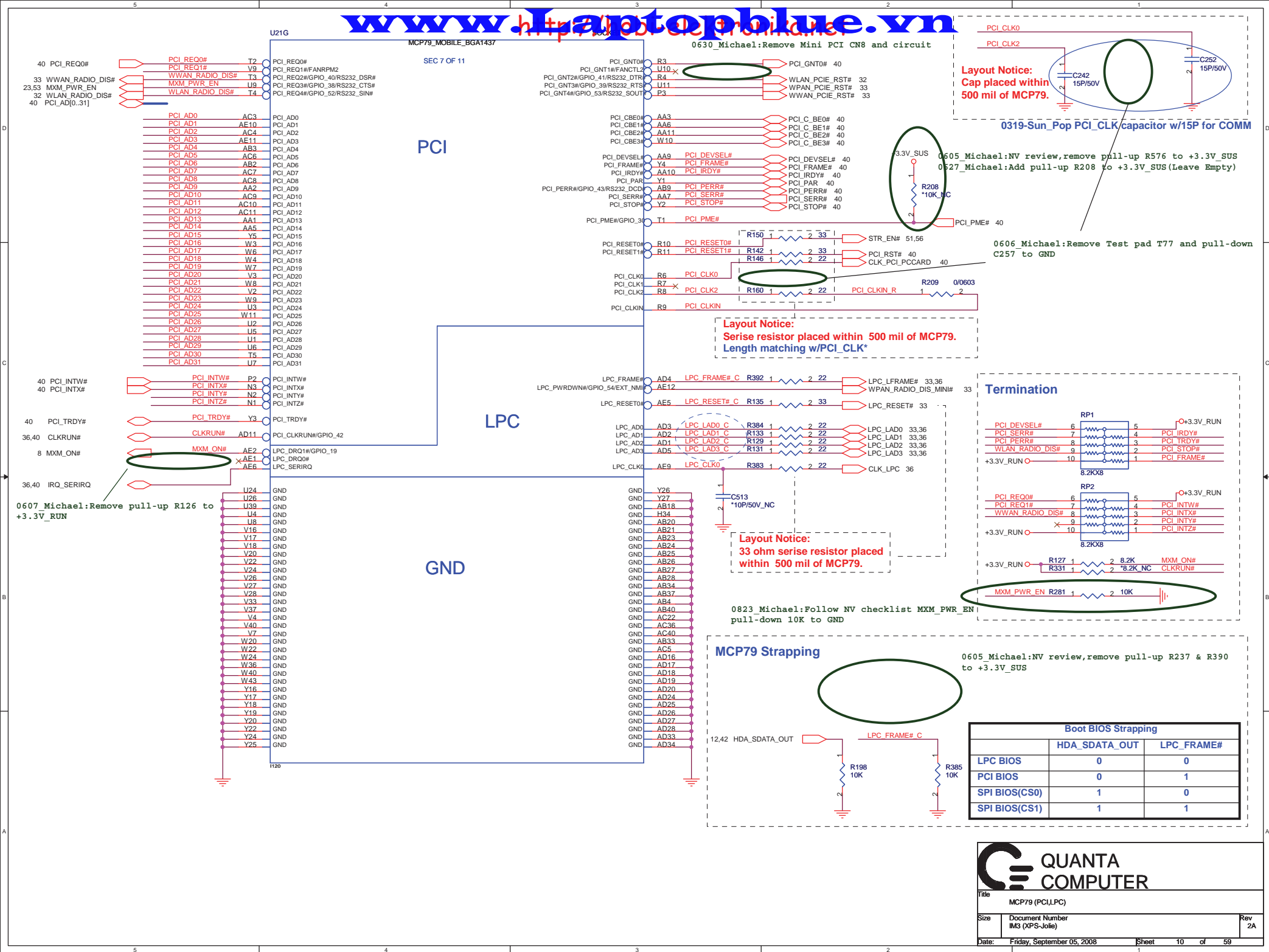
103mA with RUN rail

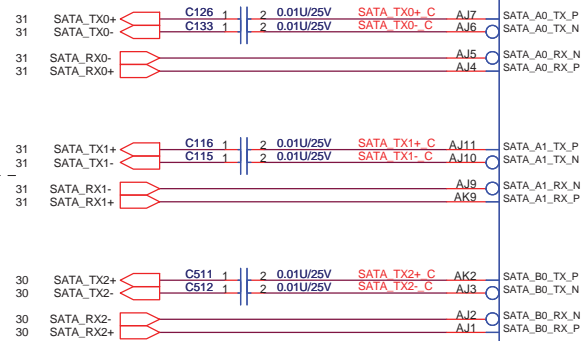
1 x ferrite bead  
1 x 4.7uF X5R ceramic  
2 x 0.1uF X7R ceramic

L43 BLM18PG181SN1D RC0603



Title			MCP79 (LAN,DACS,LVDS)
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	2A	
Date:	Thursday, September 18, 2008	Sheet	9 of 59





**SATA Layout Notice:**  
**BGA Breakout:**  
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 400 mils of MCP79.  
**BGA Fan-out:**  
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 500 mils.  
**After Brackout:**  
Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.  
TX and RX intra-pair skew for a differential pair is 5 mils.

SATA

USB

Left Side (froth)

Left Side

Combo (eSATA/USB)

Mini Card (WLAN)

Mini Card (WWAN)

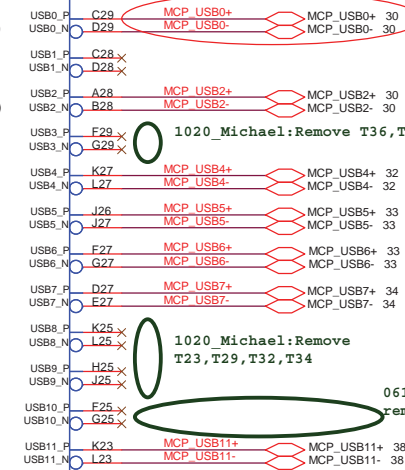
Mini Card (WPAN)

Express Card

Biometric

Camera

0312-Sun\_Change left USB port from port1 to port0 for NV remote SW debug.



0605\_Michael: Follow NV command change power rail from +3.3V RUN to +3.3V SUS  
0704\_Michael: Move R7 pull-up to +3.3V\_SUS close to MCP79

0616\_Michael: Cancel fingerprinter and remove MCP\_USB10+/-

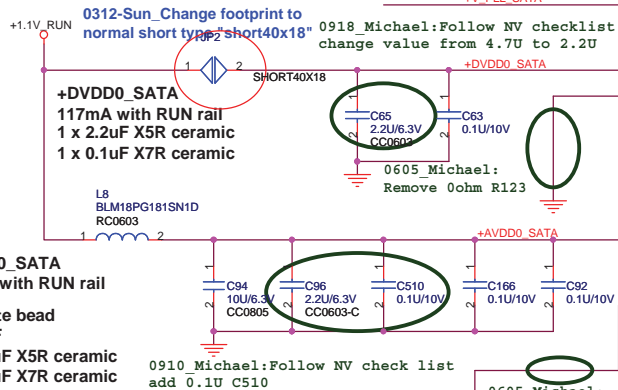
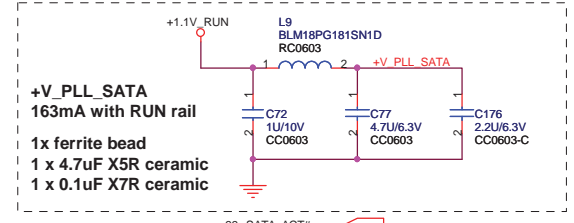
0625\_Michael: Add R403 for debug if have need



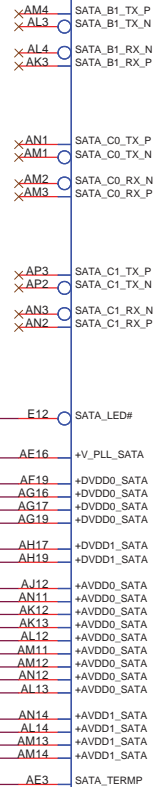
**+V\_PLL\_USB**  
18mA with Run rail  
1 x ferrite bead  
1 x 4.7uF X5R ceramic  
1 x 0.1uF X7R ceramic

0311-Sun\_Changes USB RBIAS resistor to 806ohm. (NV)

**Layout Notice:**  
909 ohm +-1% to GND within 1000 mil of MCP79.  
Routing trace at least 8 mil wide to resistor.



**+AVDD0\_SATA**  
363mA with RUN rail  
1x ferrite bead  
1x 10uF  
1 x 2.2uF X5R ceramic  
3 x 0.1uF X7R ceramic



**USB Layout Notice:**  
**BGA Breakout:**  
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 300 mils of MCP79.  
**BGA Fan-out:**  
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 400 mils.  
**After Brackout:**  
Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals. Each USB pair must be length matched to within 50 mil.



Title		MCP79 (SATA,USB)	
Size	Document Number IM3 (XPS-Jolie)		Rev 2A
Date:	Monday, October 20, 2008	Sheet 11 of 59	

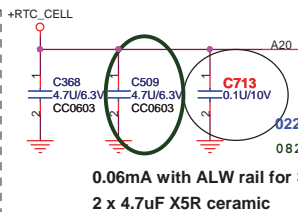
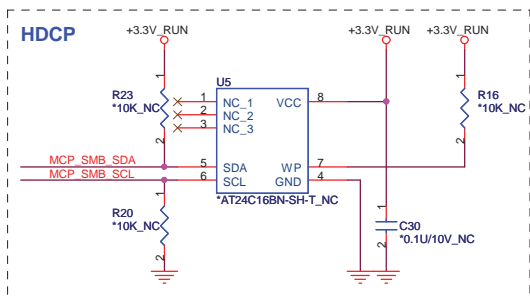
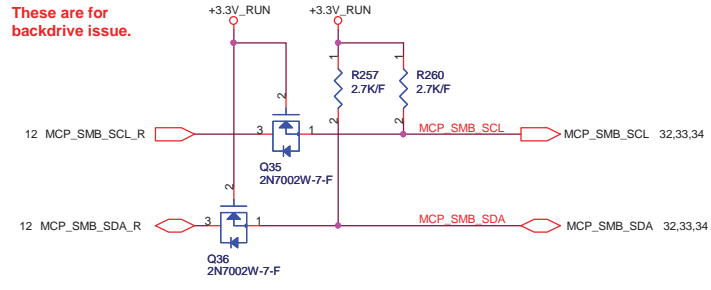
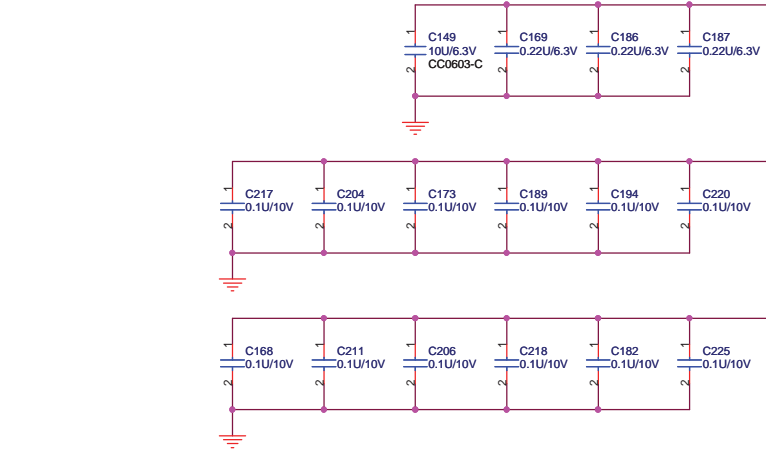




1 x 10uF ceramic  
2 x 2.2uF X5R ceramic  
3 x 1uF X5R ceramic  
3 x 0.22uF X5R ceramic  
12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0  
2850mA for S0 Idle

0918 Michael:Follow NV checklist  
change value from 10U to 2.2U



0229-Sun\_Add C713 with 0.1U on +VBAT of MCP79  
0829 Michael:Follow NV new DG add C509 on +RTC\_CELL of MCP79

POWER

MCP79\_MOBILE\_BGAT437

SEC

10 OF 11

SOCKET

AA25

AC23

U25

AH12

AG10

AG5

Y21

Y23

AA16

AA26

AA27

AA28

AC16

AC17

AC18

AC19

AC20

AC21

AA17

AC24

AC25

AC26

AC27

AC28

AD21

AD23

W27

Y26

AA18

AE19

AE21

AE23

AE25

AE26

AE27

AE28

AF10

AF11

AF19

AA19

AF2

AF21

AF23

AF25

AF3

AF4

AF7

AH23

AF9

AF9

AA20

AG11

AG12

AG21

AG23

AG25

AG3

AG4

AA21

AG6

AG7

AG8

AG9

AH1

AH10

AH11

W26

AH2

AA23

W28

AH25

AH21

AH3

AH4

AH5

AH6

AH7

AH9

AA24

W21

W23

W25

AF12

+VDD\_CORE

+VDD\_CORE

+VDD\_CORE

+VDD\_CORE

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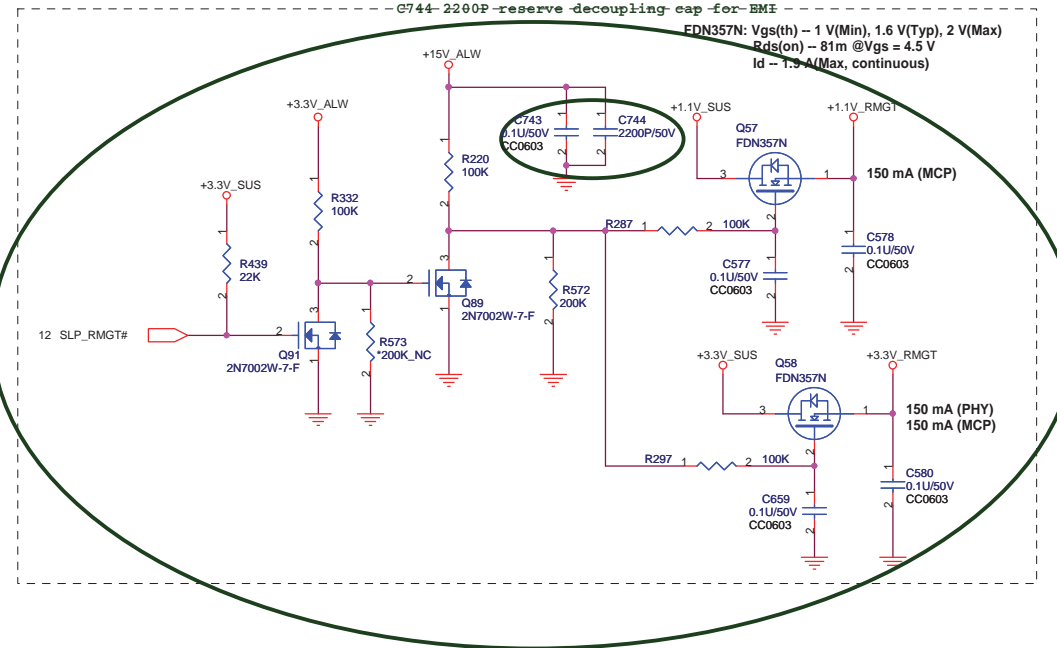
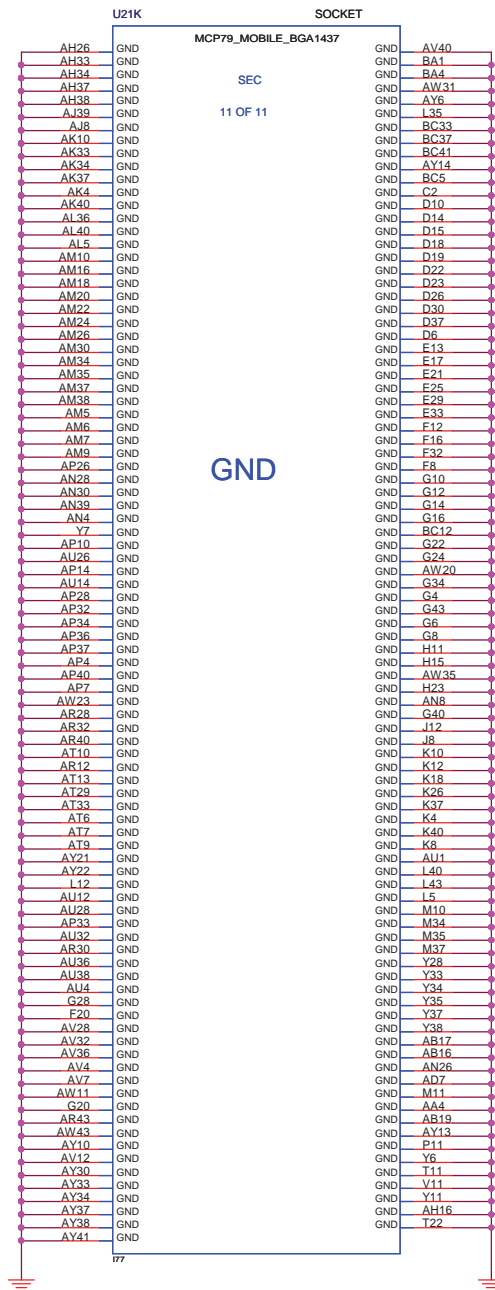
+VDD\_CORE

+VDD\_CORE

+VDD\_CORE

+VDD\_CORE





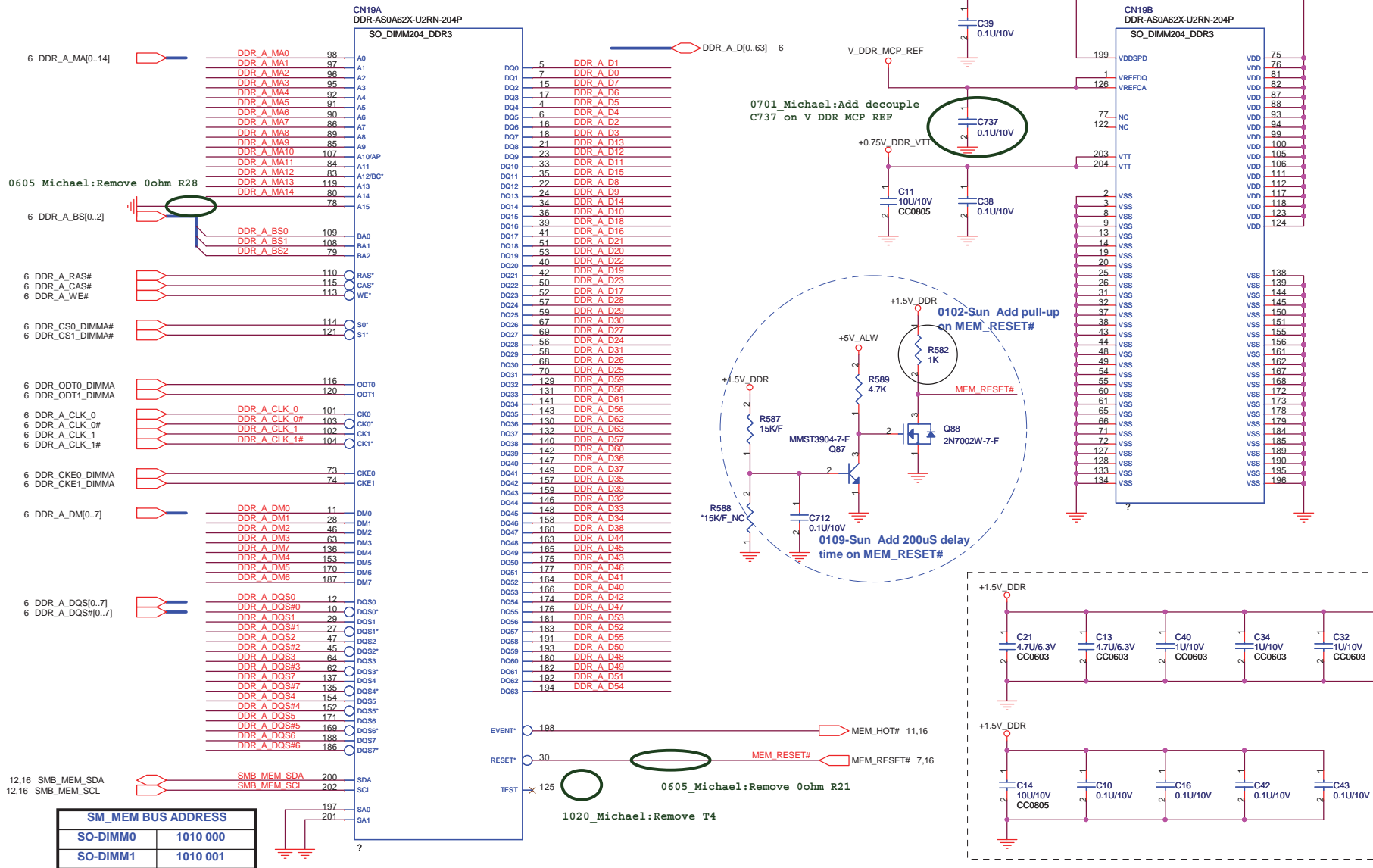
0229-Sun 1.1V\_RMGT & +3.3V\_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB  
(Del JP11, JP12)

Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3  
Add Q89 with 2N7002, R591 with 10K

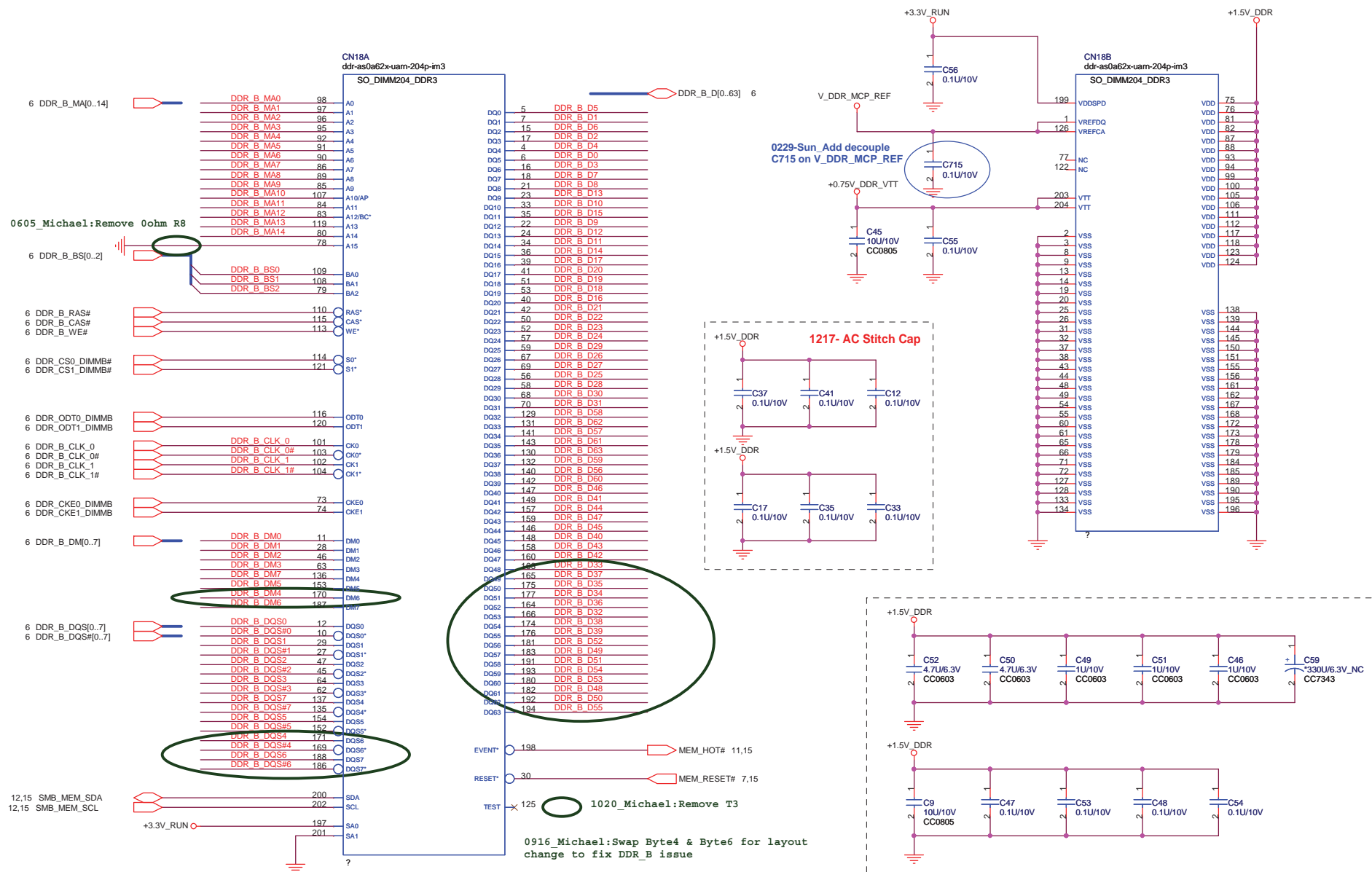
0825 Michael: Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F, R&C for  
+1.1V\_RMGT and +3.3V\_RMGT power low issue



Title		
MCP79 (GND)		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A
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For EMI Reserved

DDR B CLK 1	R9	1		2	*200/F_NC	DDR B CLK 1#
DDR B CLK 0	R11	1		2	*200/F_NC	DDR B CLK 0#



Title DDR3 SO-DIMM (204P)

Size	Document Number IM3 (XPS-Jolie)
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Rev  
2A

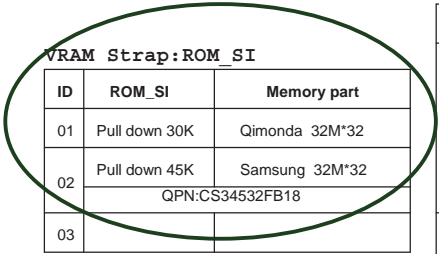
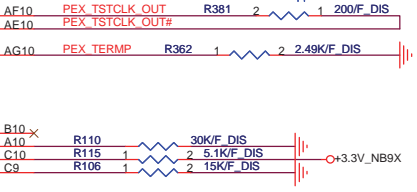
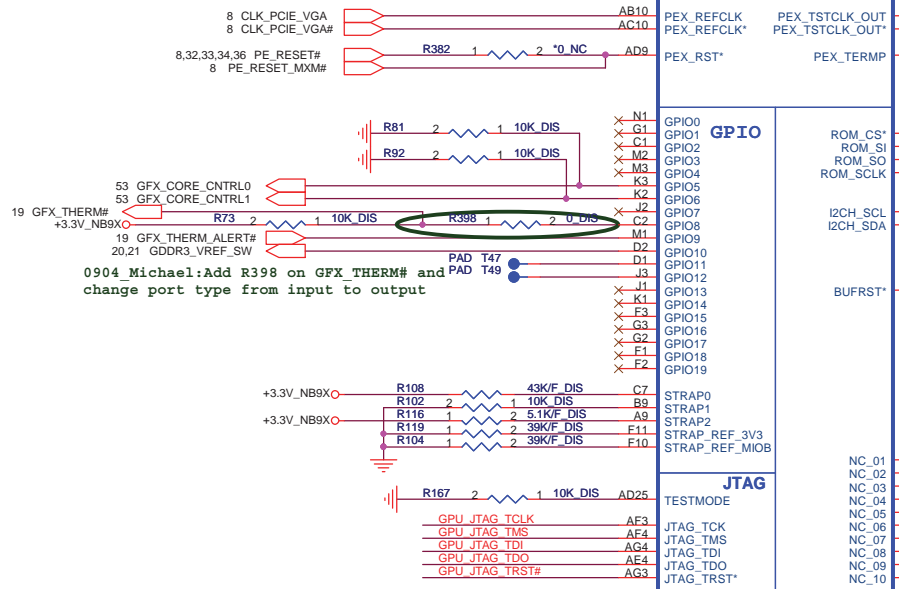
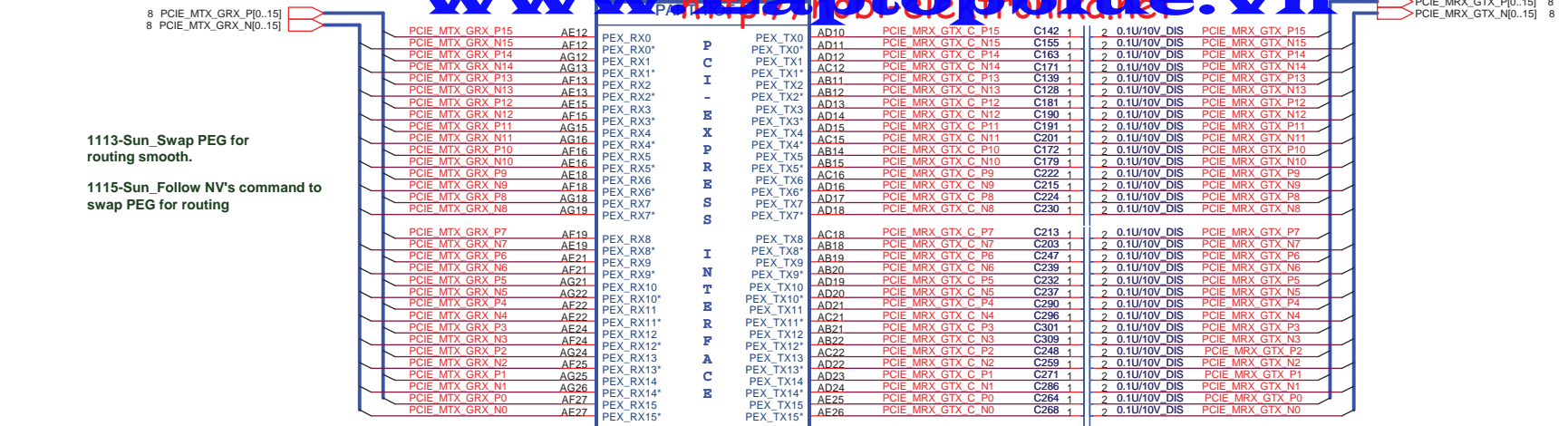
Date: Monday, October 20, 2008

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8

1113-Sun\_Swap PEG for routing smooth.

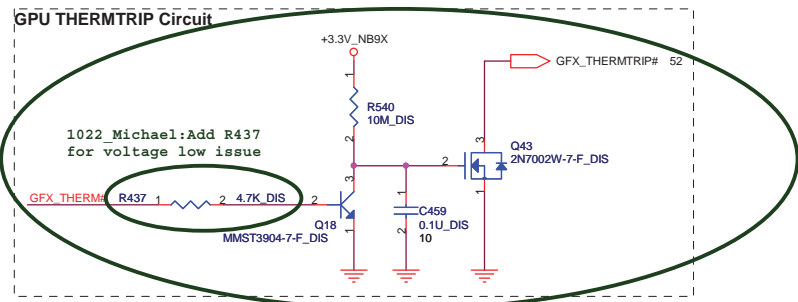
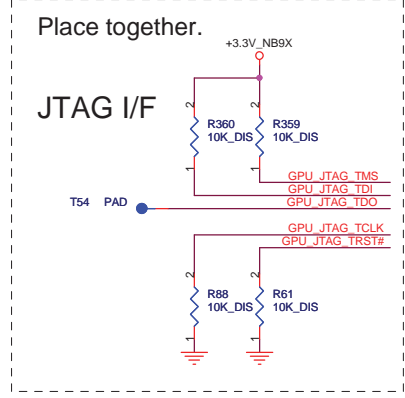
1115-Sun\_Follow NV's command to swap PEG for routing



0604\_Michael: Follow NV command to modify VRAM Strap resistor value

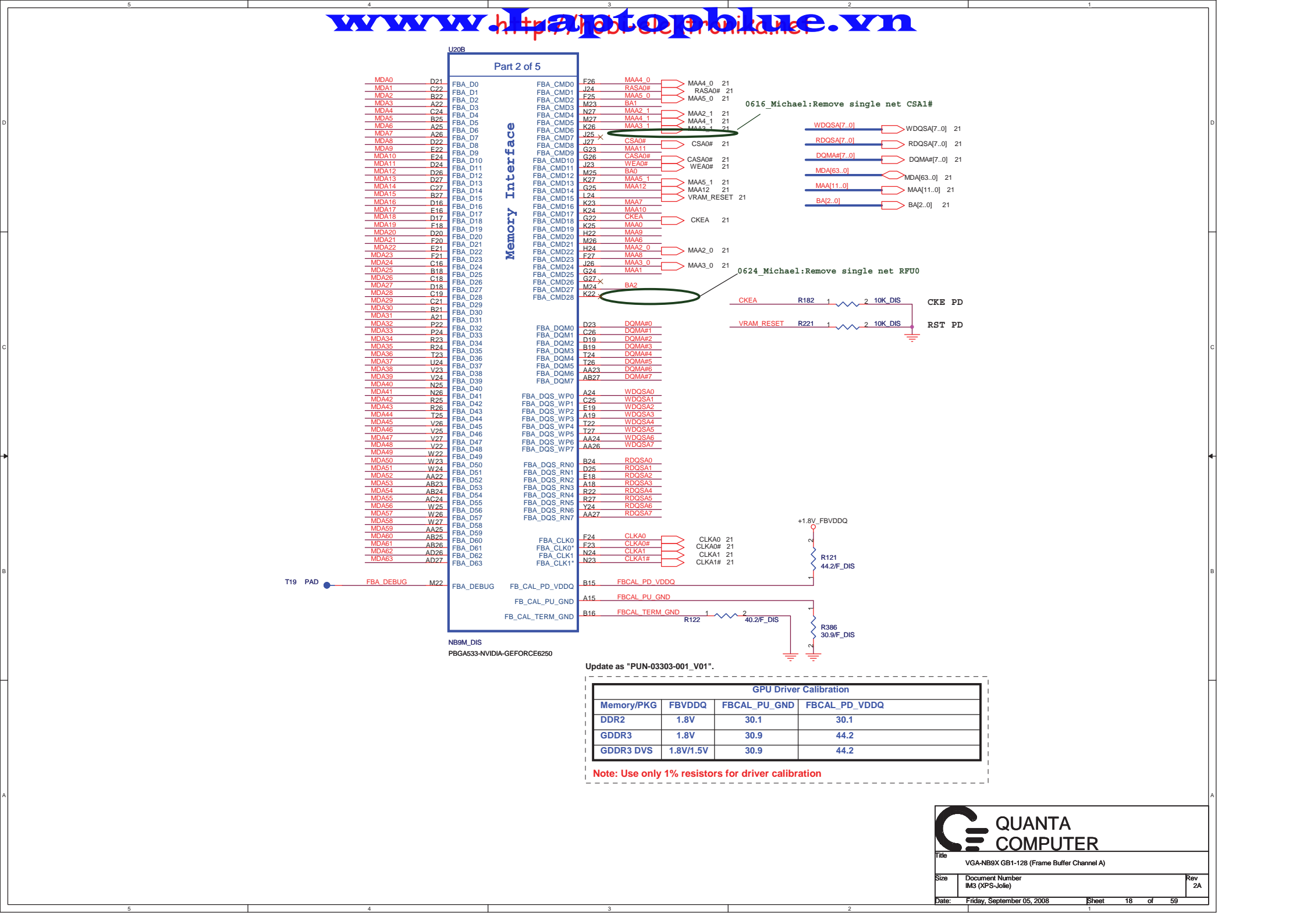
GPIO USAGE

GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVVDD ALTV0	
6	OUT	HIGH	NVVDD ALTV1	
7	OUT	HIGH	FBVDD VID0	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 ( not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No



0825 Michael:Modify THERMTRIP circuit,add MOS and CAP





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**Part 2 of 5**

**Memory Interface**

**U20B**

**T19 PAD**

**FBA DEBUG M22**

**NB9M\_DIS**

**PBG533-NVIDIA-GEFORCE6250**

**Update as "PUN-03303-001\_V01".**

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

Note: Use only 1% resistors for driver calibration

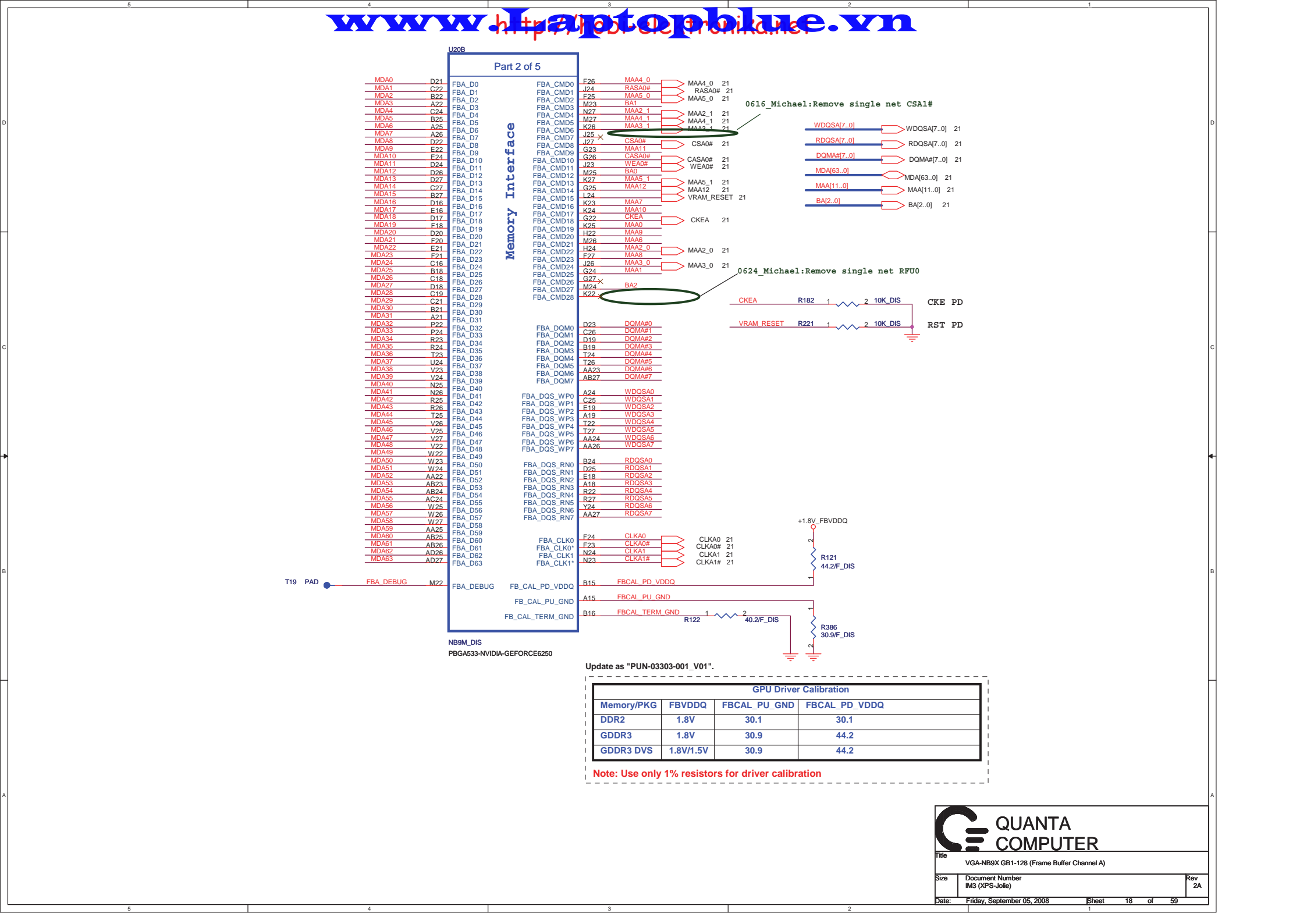
**QUANTA COMPUTER**

Title: VGA-NB9X GB1-128 (Frame Buffer Channel A)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Friday, September 05, 2008 Sheet 18 of 59

The schematic diagram illustrates the memory interface for the U20B component. It shows a central vertical column of pins labeled from MDA0 to MDA63, organized into groups of 16 (MDA0-MDA15, MDA16-MDA31, MDA32-MDA47, MDA48-MDA63). To the left of this column are labels for T19 PAD, FBA DEBUG, and M22. To the right, there are detailed signal paths for FBA\_CMD0 through FBA\_CMD28, FBA\_DQS\_WP0 through FBA\_DQS\_WP7, FBA\_DQS\_RN0 through FBA\_DQS\_RN7, FBA\_CLK0 through FBA\_CLK1, and FBA\_DEBUG. These signals connect to various external components: FBA\_CMD0-FBA\_CMD28 to MAA0\_0 through MAA12\_0 and MAA2\_0 through MAA3\_0; FBA\_DQS\_WP0-FBA\_DQS\_WP7 to WDQSA0 through WDQSA7 and RDQSA0 through RDQSA7; FBA\_DQS\_RN0-FBA\_DQS\_RN7 to RDQSA0 through RDQSA7; FBA\_CLK0-FBA\_CLK1 to CLKA0 through CLKA1#; and FBA\_DEBUG to FB\_CAL\_PD\_VDDQ, FB\_CAL\_PU\_GND, and FB\_CAL\_TERM\_GND. Specific components like R182, R221, R121, R122, R386, and CKEA are shown with their values and connections. Annotations include '0616\_Michael: Remove single net CSA1#' and '0624\_Michael: Remove single net RFU0'. The bottom section contains a table for GPU Driver Calibration with columns for Memory/PKG, FBVDDQ, FBCAL\_PU\_GND, and FBCAL\_PD\_VDDQ, listing values for DDR2, GDDR3, and GDDR3 DVS. A note specifies 'Use only 1% resistors for driver calibration'. The Quanta Computer logo and document information (Title, Size, Date, Sheet number) are at the bottom.

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Part 2 of 5

**Memory Interface**

U20B

MDA0 D21 FBA\_D0  
MDA1 C22 FBA\_D1  
MDA2 B22 FBA\_D2  
MDA3 A22 FBA\_D3  
MDA4 C24 FBA\_D4  
MDA5 B25 FBA\_D5  
MDA6 A25 FBA\_D6  
MDA7 A26 FBA\_D7  
MDA8 D22 FBA\_D8  
MDA9 E22 FBA\_D9  
MDA10 E24 FBA\_D10  
MDA11 D24 FBA\_D11  
MDA12 D26 FBA\_D12  
MDA13 D27 FBA\_D13  
MDA14 C27 FBA\_D14  
MDA15 B27 FBA\_D15  
MDA16 D16 FBA\_D16  
MDA17 E16 FBA\_D17  
MDA18 D17 FBA\_D18  
MDA19 F18 FBA\_D19  
MDA20 D20 FBA\_D20  
MDA21 F20 FBA\_D21  
MDA22 E21 FBA\_D22  
MDA23 F21 FBA\_D23  
MDA24 C16 FBA\_D24  
MDA25 B18 FBA\_D25  
MDA26 C18 FBA\_D26  
MDA27 D18 FBA\_D27  
MDA28 C19 FBA\_D28  
MDA29 C21 FBA\_D29  
MDA30 B21 FBA\_D30  
MDA31 A21 FBA\_D31  
MDA32 P22 FBA\_D32  
MDA33 P24 FBA\_D33  
MDA34 R23 FBA\_D34  
MDA35 R24 FBA\_D35  
MDA36 T23 FBA\_D36  
MDA37 U24 FBA\_D37  
MDA38 V23 FBA\_D38  
MDA39 V24 FBA\_D39  
MDA40 N25 FBA\_D40  
MDA41 N26 FBA\_D41  
MDA42 R25 FBA\_D42  
MDA43 R26 FBA\_D43  
MDA44 T25 FBA\_D44  
MDA45 V26 FBA\_D45  
MDA46 V25 FBA\_D46  
MDA47 V27 FBA\_D47  
MDA48 W22 FBA\_D48  
MDA49 W22 FBA\_D49  
MDA50 W23 FBA\_D50  
MDA51 W24 FBA\_D51  
MDA52 AA22 FBA\_D52  
MDA53 AB23 FBA\_D53  
MDA54 AB24 FBA\_D54  
MDA55 AC24 FBA\_D55  
MDA56 W25 FBA\_D56  
MDA57 W26 FBA\_D57  
MDA58 W27 FBA\_D58  
MDA59 AA25 FBA\_D59  
MDA60 AB25 FBA\_D60  
MDA61 AB26 FBA\_D61  
MDA62 AD26 FBA\_D62  
MDA63 AD27 FBA\_D63

FBA\_CMD0 J26 MAA\_0\_ 21  
FBA\_CMD1 J24 RASAO# 21  
FBA\_CMD2 F25 MAA5\_0 21  
M23 BA1  
N27 MAA2\_1 21  
M27 MAA4\_1 21  
K26 MAA3\_1 21  
J25 X  
J27 CSA0# 21  
G23 CASAO# 21  
G26 WEA0# 21  
J23 WEA0# 21  
M25 BA0  
K27 MAA5\_1 21  
G25 MAA12 21  
L24 VRAM\_RESET 21  
K23 MAA7  
K24 MAA10  
G22 CKEA 21  
K25 MAA0  
H22 MAA6  
M26 MAA2\_0 21  
H24 MAA8  
E27 MAA3\_0 21  
J26 MAA3\_0 21  
G24 MAA1  
G27 X  
M24 BA2  
K22

D23 DQMA#0  
C26 DQMA#1  
D19 DQMA#2  
B19 DQMA#3  
T24 DQMA#4  
T26 DQMA#5  
AA23 DQMA#6  
AB27 DQMA#7

A24 WDQSA0  
C25 WDQSA1  
E19 WDQSA2  
A19 WDQSA3  
T22 WDQSA4  
T27 WDQSA5  
AA24 WDQSA6  
AA26 WDQSA7

B24 RDQSA0  
D25 RDQSA1  
E18 RDQSA2  
A18 RDQSA3  
R22 RDQSA4  
R27 RDQSA5  
Y24 RDQSA6  
AA27 RDQSA7

F24 CLKA0 21  
F23 CLKA0# 21  
N24 CLKA1 21  
N23 CLKA1# 21

B15 FBAL PD\_VDDQ  
A15 FBAL PU\_GND  
B16 FBAL TERM\_GND

R182 1 2 10K\_DIS  
R221 1 2 10K\_DIS  
R121 44.2/F\_DIS  
R122 1 2 40.2/F\_DIS  
R386 30.9/F\_DIS

CKE PD  
RST PD

T19 PAD FBA\_DEBUG M22 FBA\_DEBUG FB\_CAL\_PD\_VDDQ  
FB\_CAL\_PU\_GND  
FB\_CAL\_TERM\_GND

NB9M\_DIS  
PBG533-NVIDIA-GEFORCE6250

Update as "PUN-03303-001\_V01".

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBAL PU_GND	FBAL PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

Note: Use only 1% resistors for driver calibration

**QUANTA COMPUTER**

Title VGA-NB9X GB1-128 (Frame Buffer Channel A)

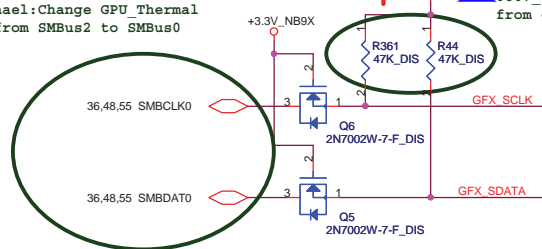
Size Document Number IM3 (XPS-Jolie) Rev 2A

Date: Friday, September 05, 2008 Sheet 18 of 59

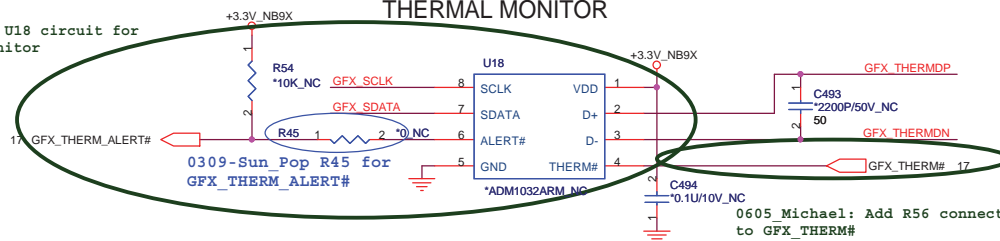
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from 4.7k to 47k for battery issue

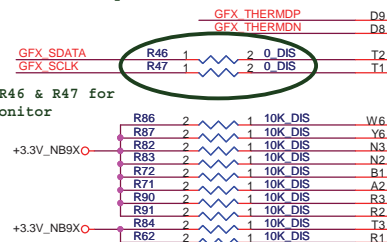


0708\_Michael:Depop U18 circuit for  
nternal thermal monitor

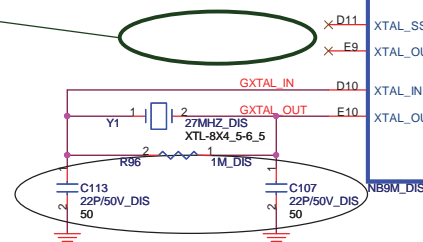


```
0605_Michael: Add R56 connect
to GFX_THERM#
0904_Michael: Remove R56 and
change port type from output
to input
```

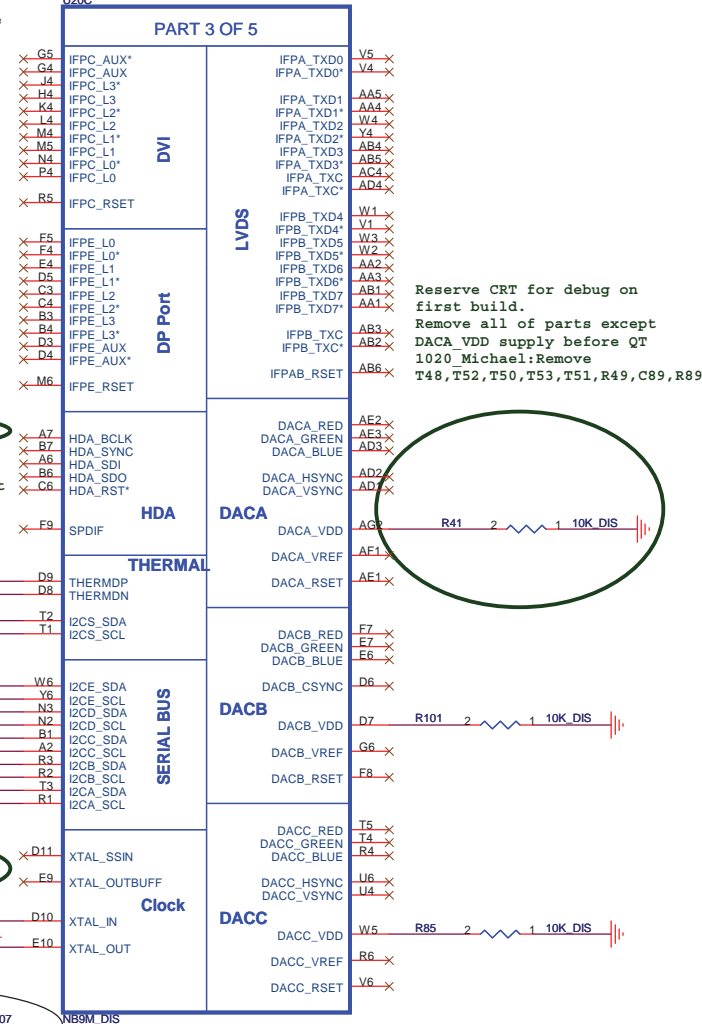
0708\_Michael:Pop R46 & R47 for  
nternal thermal monitor



0701 Michael:Remove SPREAD SPECTRUM circuit



0709-Steg: Change CAP Value from 18p to 22p



```

Reserve CRT for debug on
first build.
Remove all of parts except
DACA_VDD supply before QT
1020_Michael:Remove
T48,T52,T50,T53,T51,R49,C89,R89

```



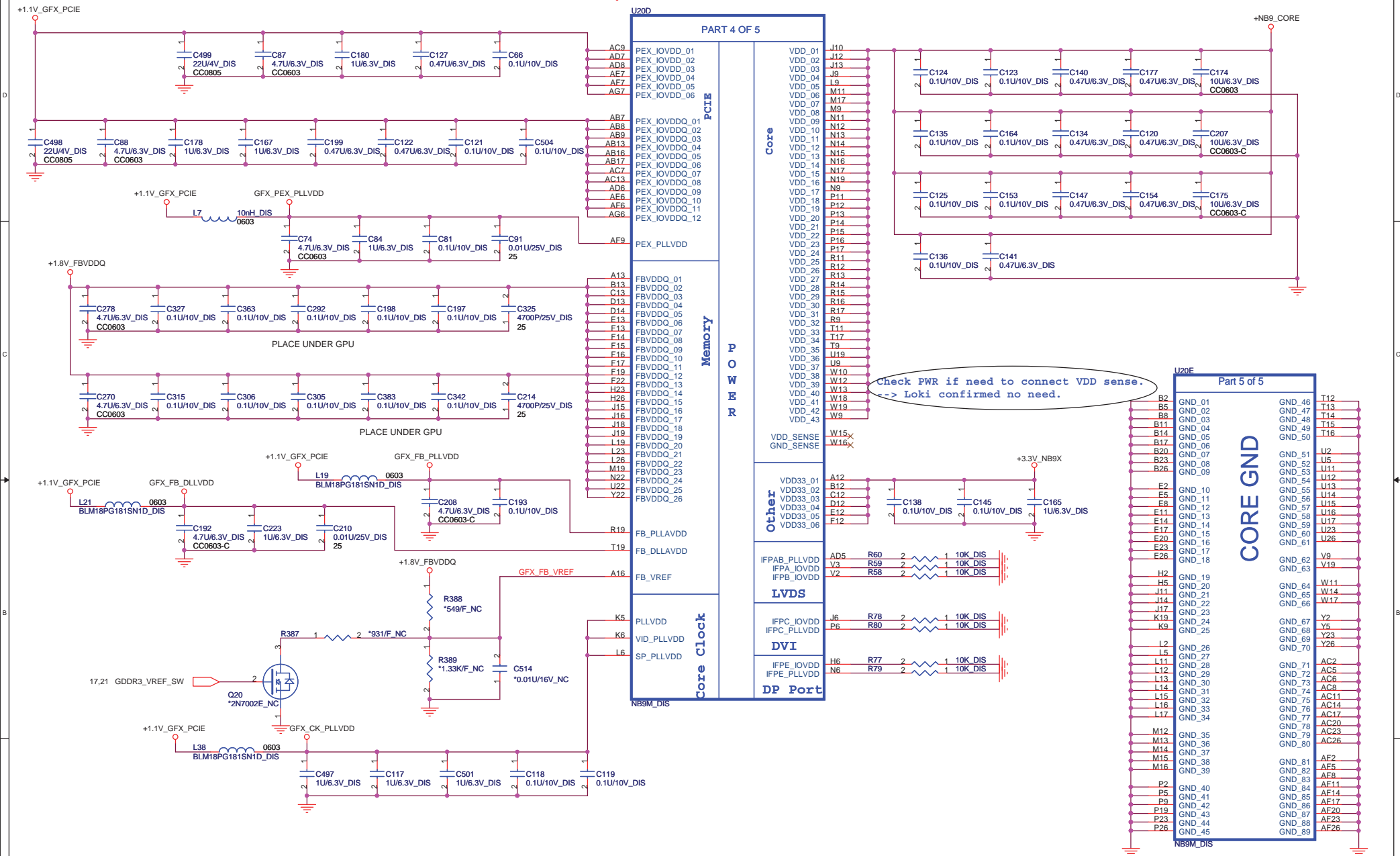
Title	VGA-NB9X GB1-64 (OUTPUT)
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Size	Document Num IM3 (XPS-Jolie)
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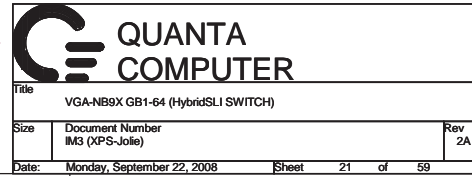
Rev	2/
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Date: Monday, October 20, 2008

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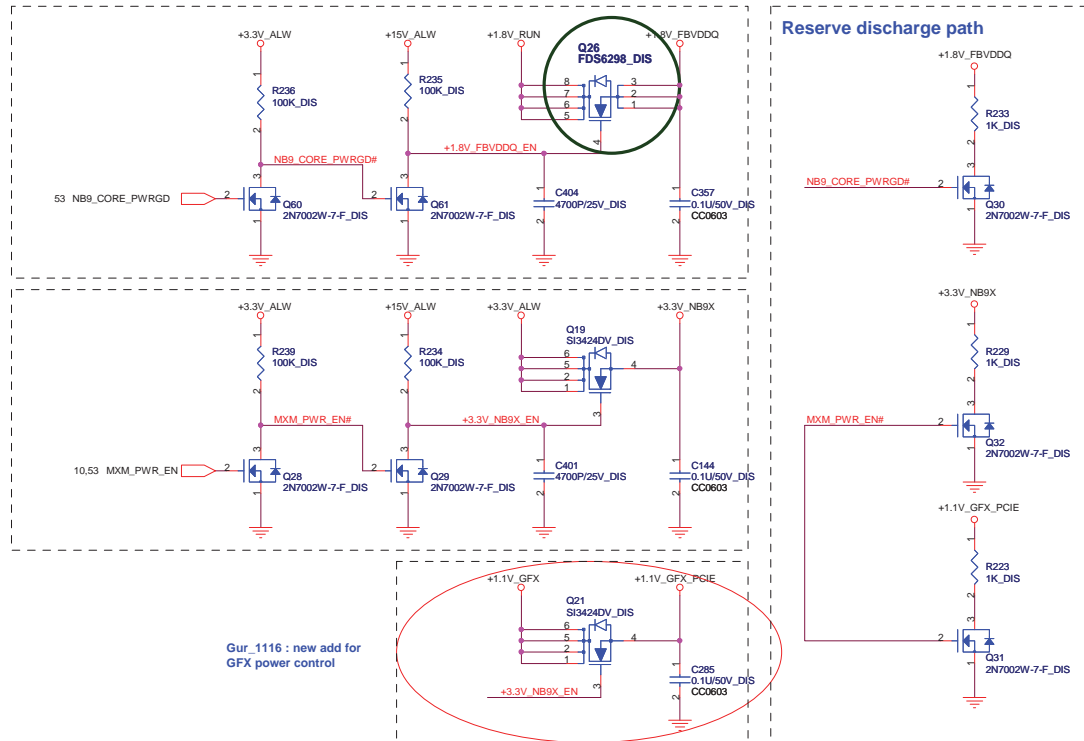


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1225-Sun\_Change Q26 from SI4812BDY to SI4800BDY-T1-E3  
1022\_Michael:Change Q26 from SI4800BDY-T1-E3 to BAM62980005

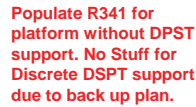
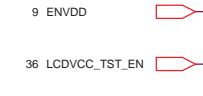


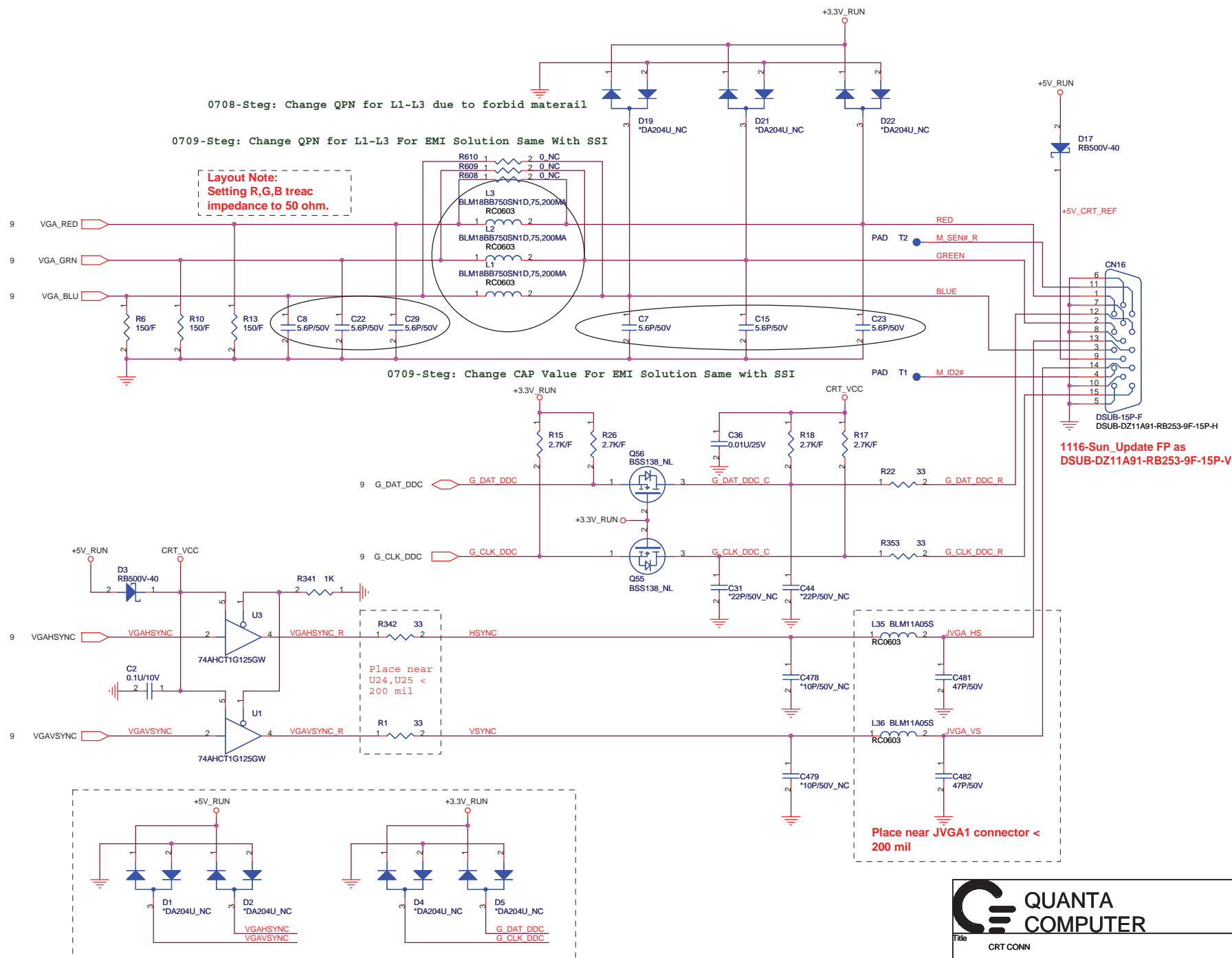


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 QUANTA COMPUTER		
Title		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
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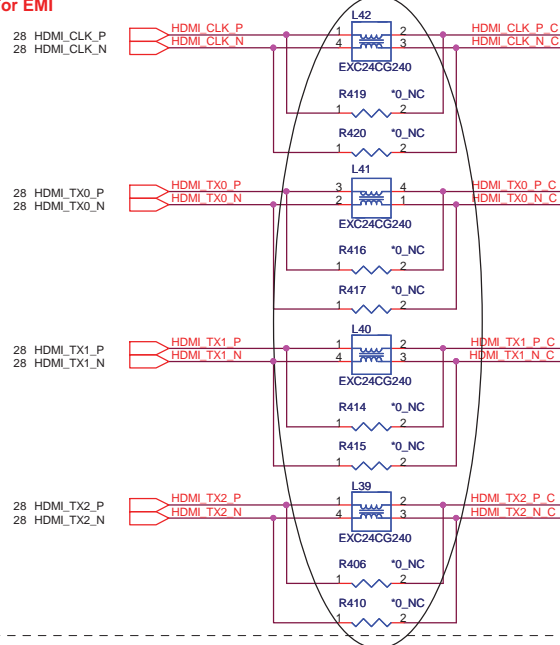




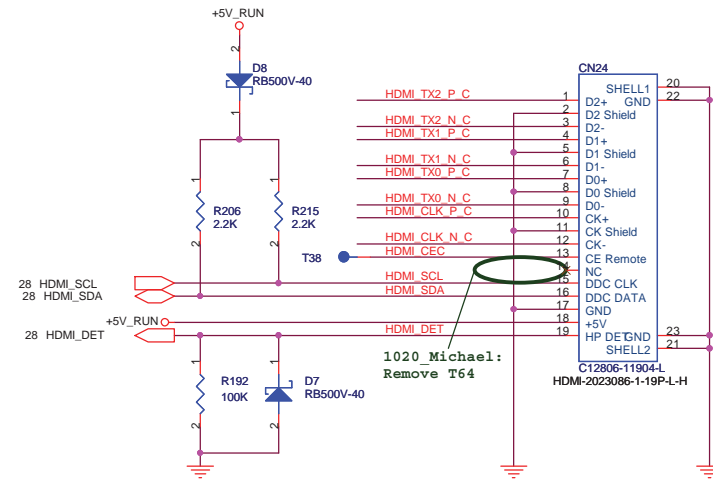




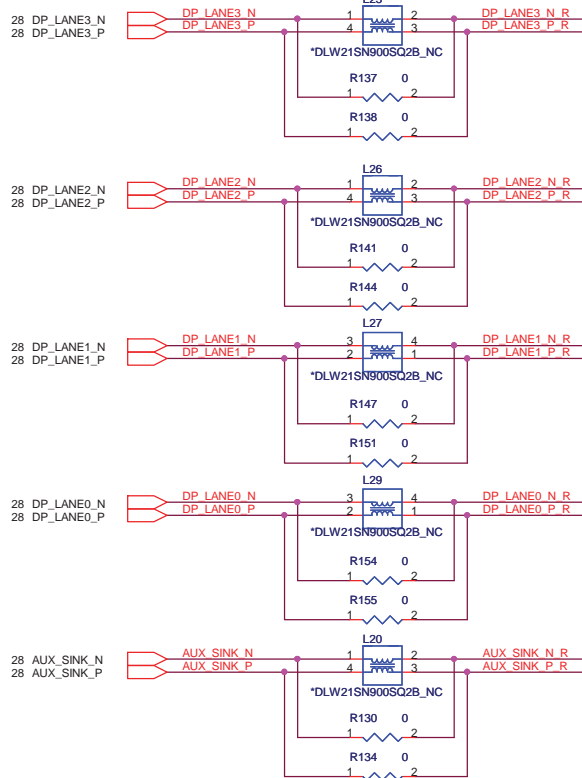
Reserve For EMI



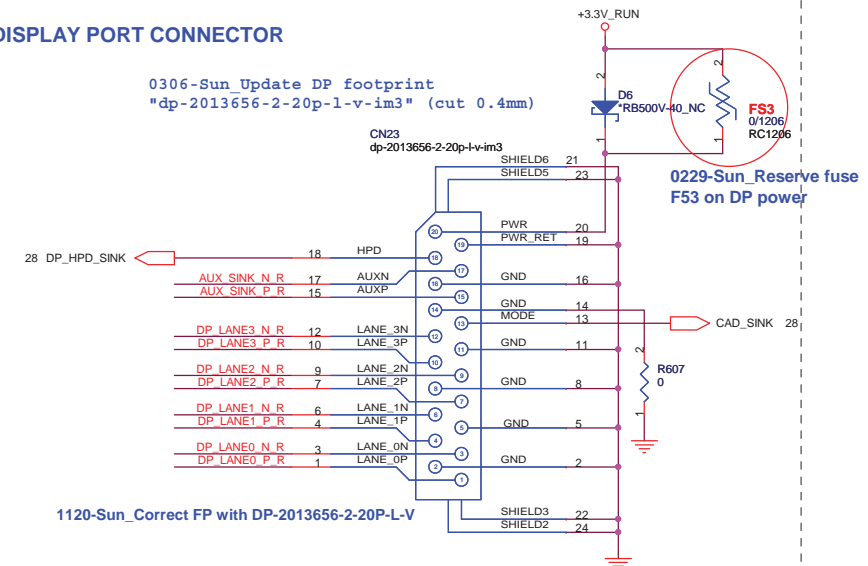
HDMI CONNECTOR

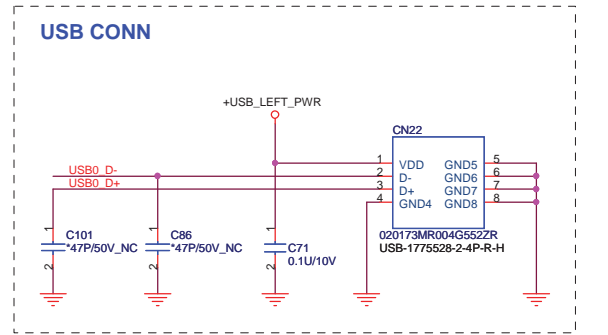
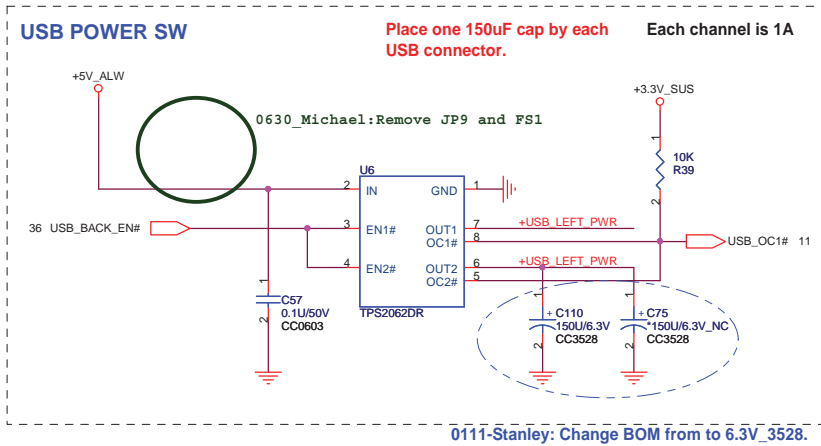
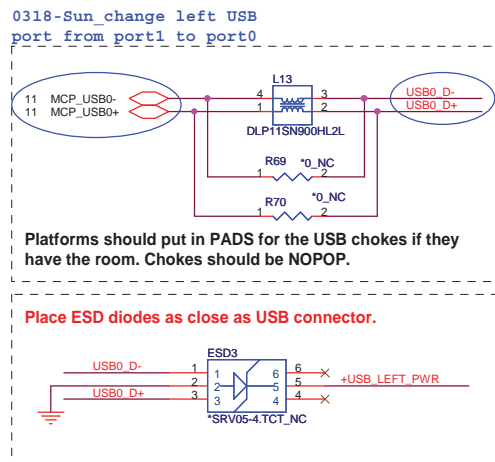
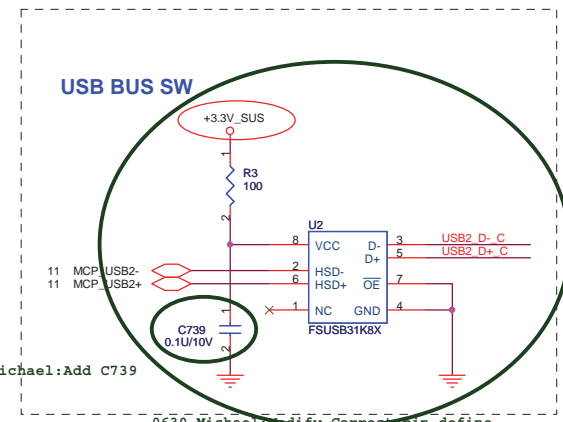
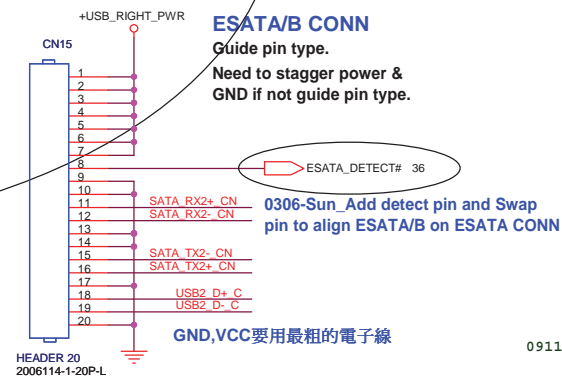
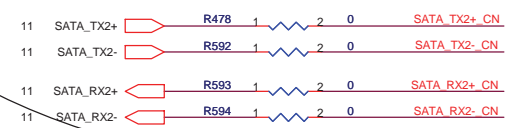
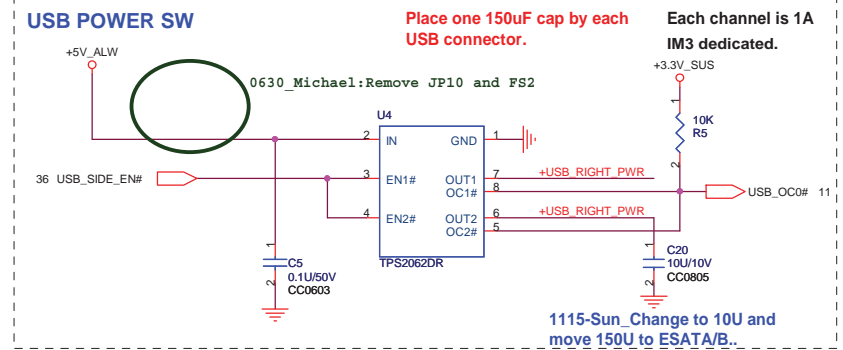
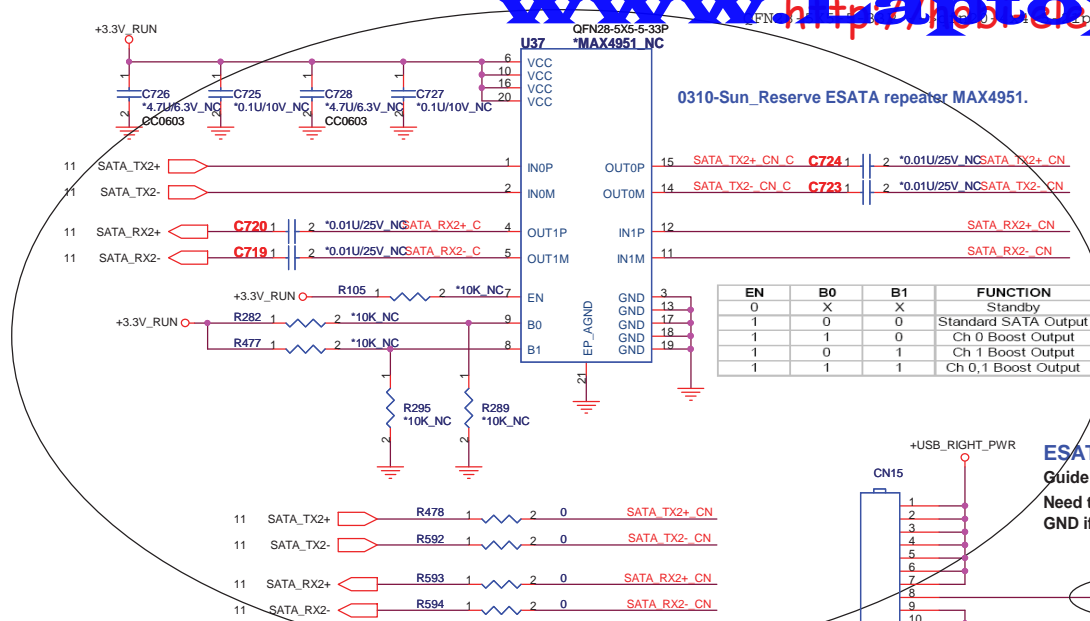


Reserve For EMI

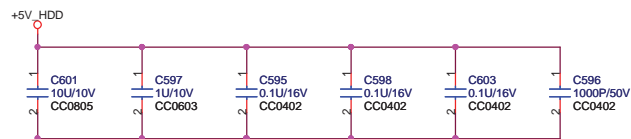
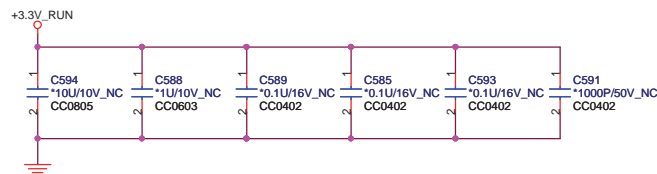
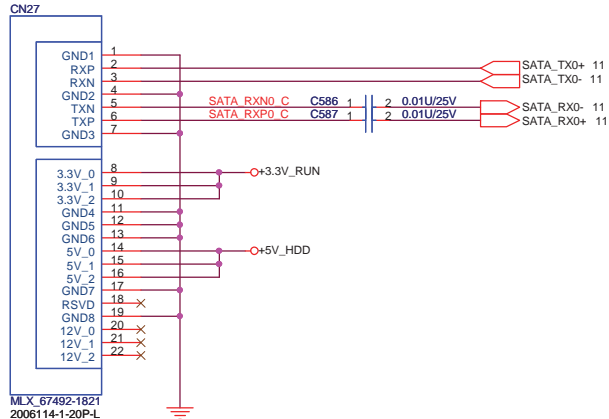


DISPLAY PORT CONNECTOR

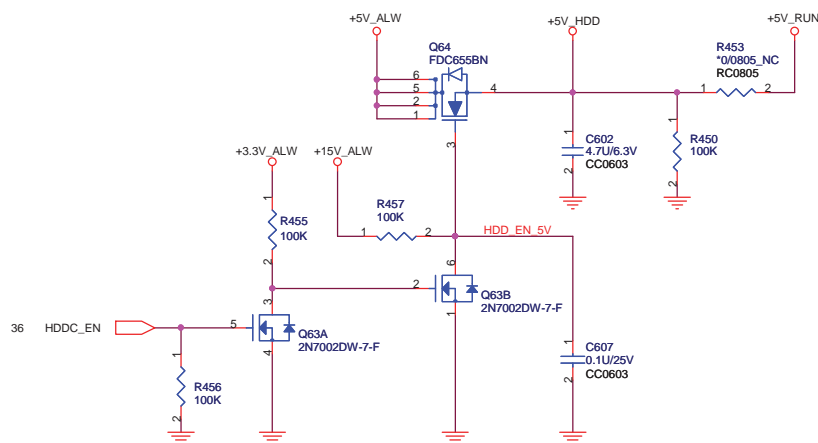




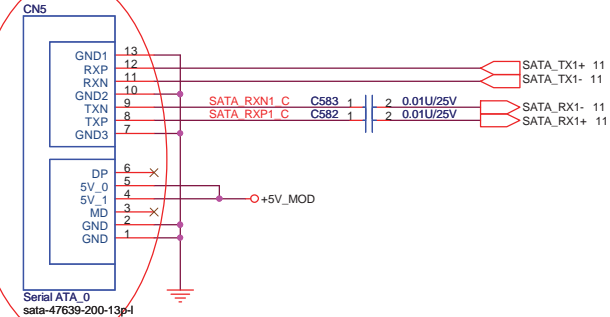
# SATA HDD Connector



Place caps close to connector.

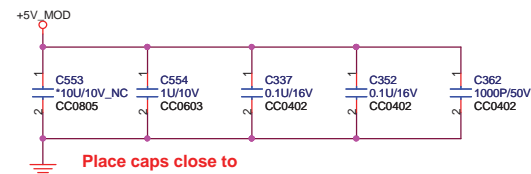


# SATA ODD Connector

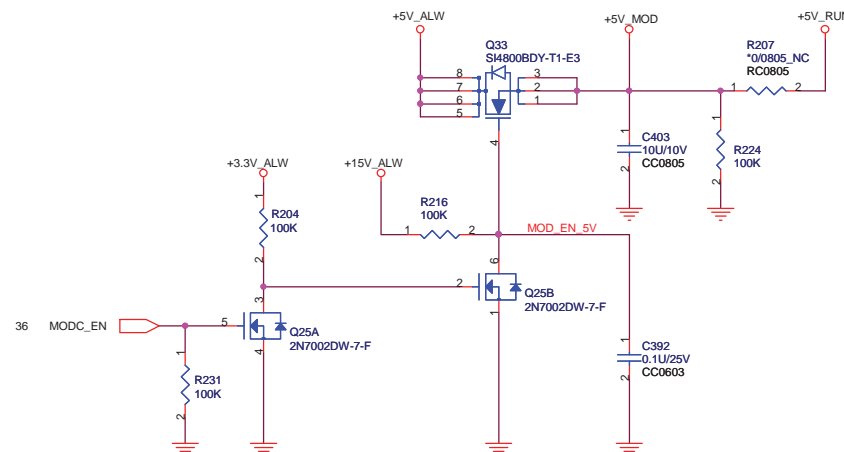


0306-Sun\_Change to new footprint\_sata-47639-200-13p-I

0407-Sun\_Swap pin assignment due to pin direction is reversed



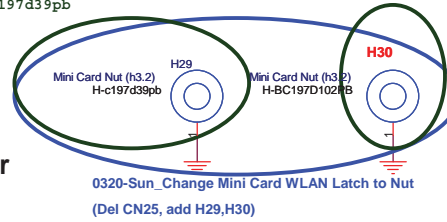
Place caps close to connector.



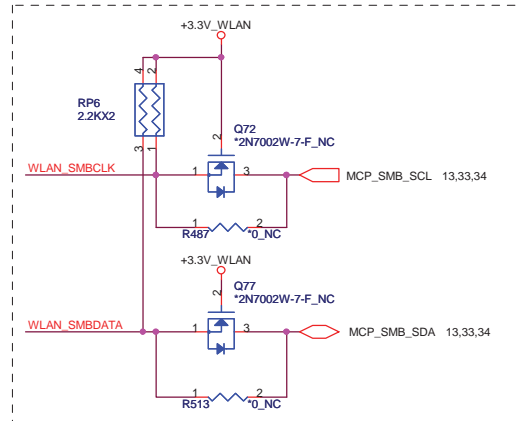
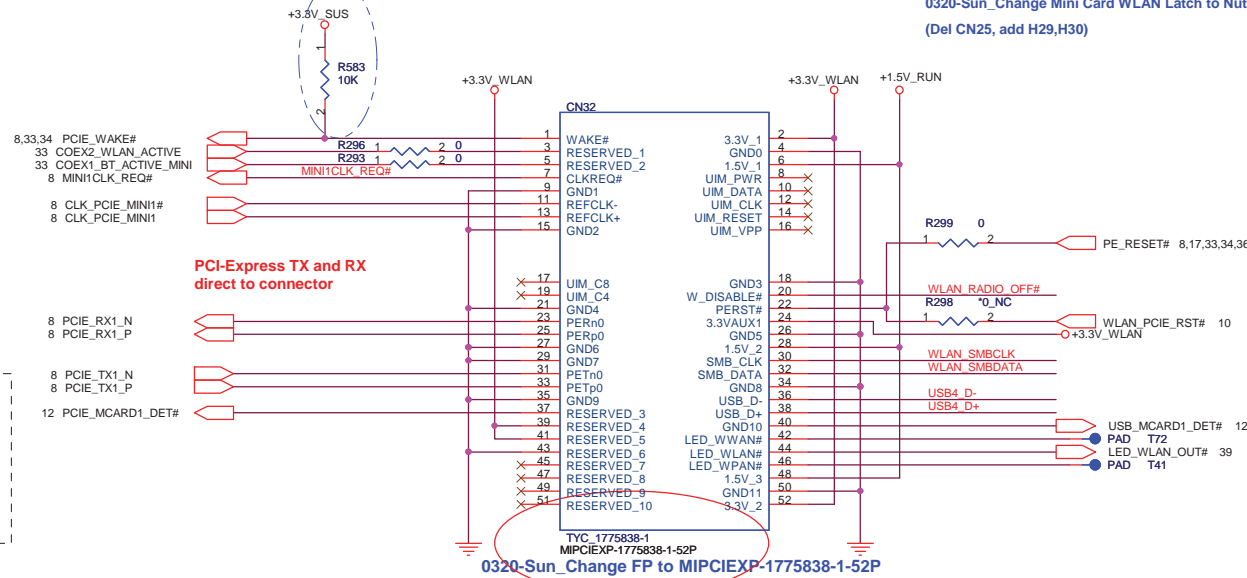
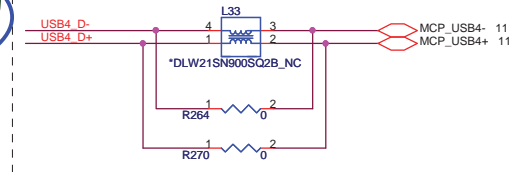
0829\_Michael:Change Footprint from  
H-C197PB to H-c197d39pb

0616\_Michael:Change footprint

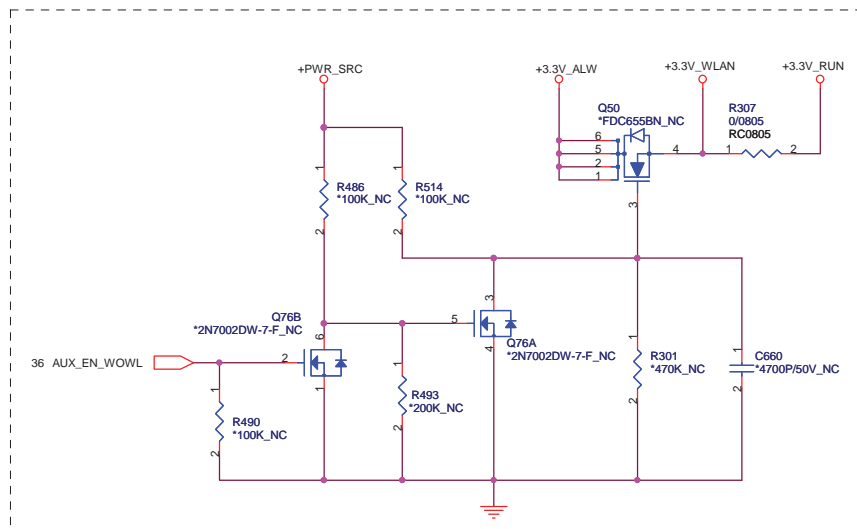
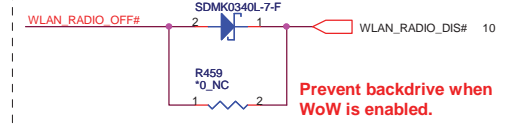
## MiniCard WLAN Connector



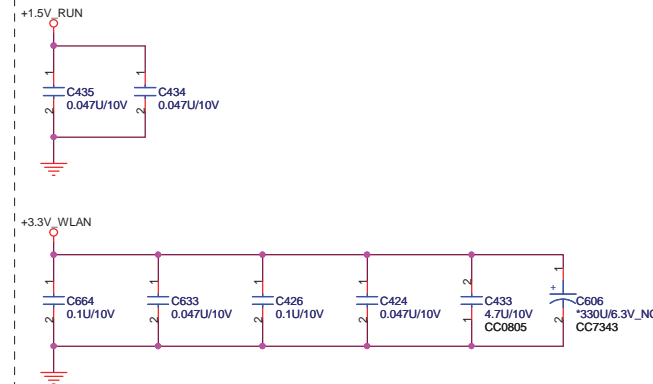
### Reserved PAD for EMI



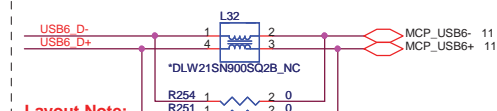
### Support for WoW



Place caps close to connector.

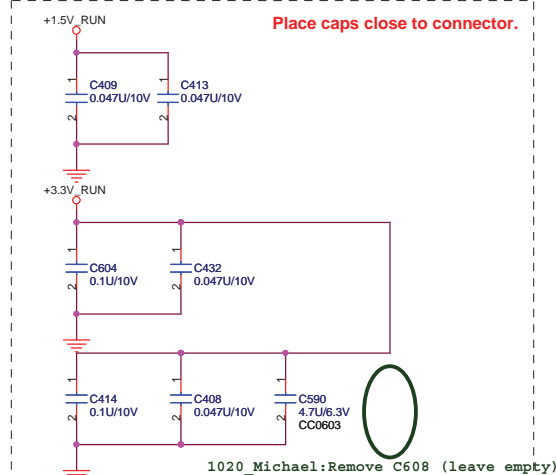


**QUANTA  
COMPUTER**

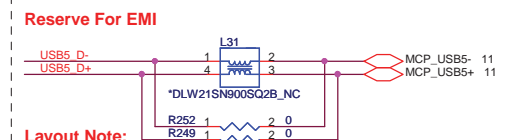


**Layout Note:**

- R240 and R244 close to choke as possible to minimize stubs.



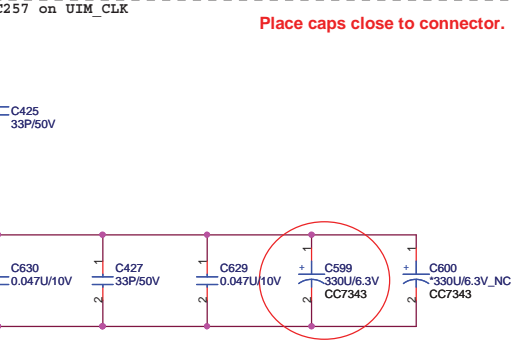
**Place caps close to connector.**



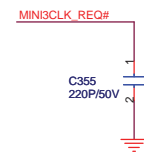
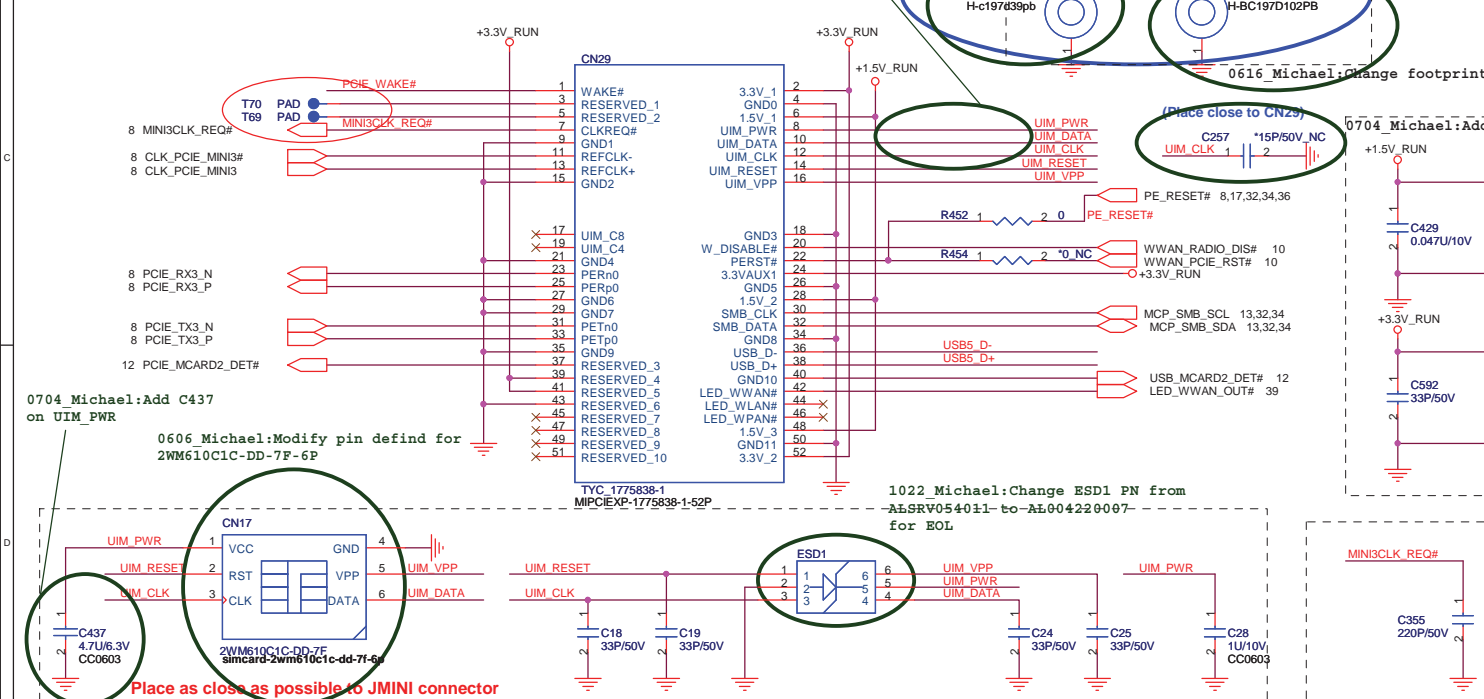
**Reserve For EMI**

**Layout Note:**

**R240 and R244 close to choke as possible to minimize stubs.**



**Place caps close to connector.**



Title	MINI-CARD (WWAN,WPAN)
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Size

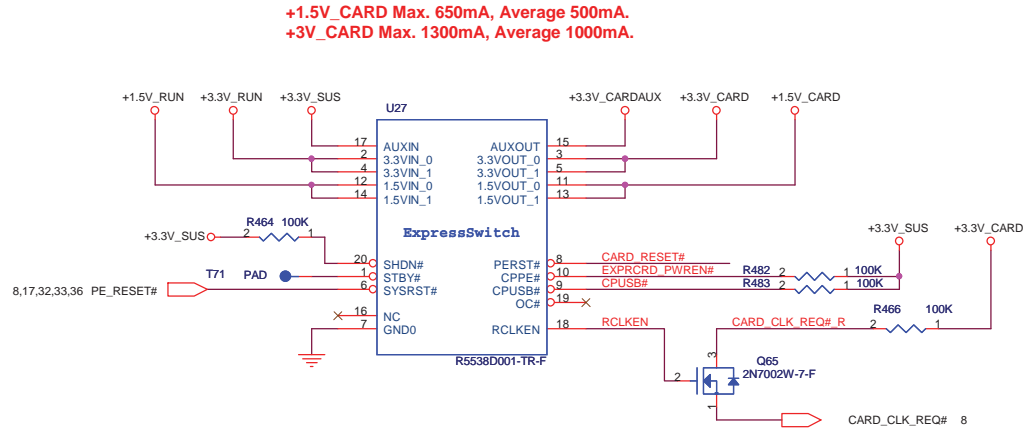
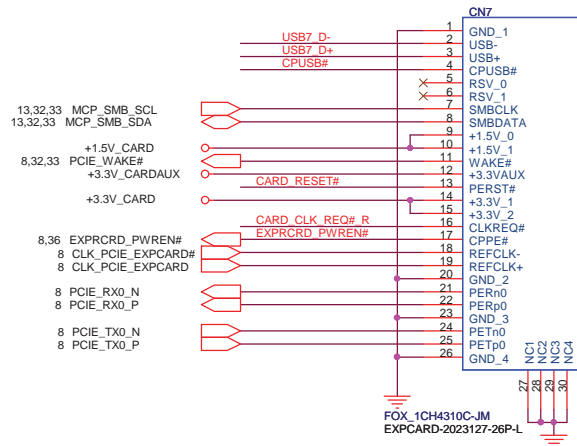
Document Number	IM3 (XPS-Jolie)
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Rev	2A
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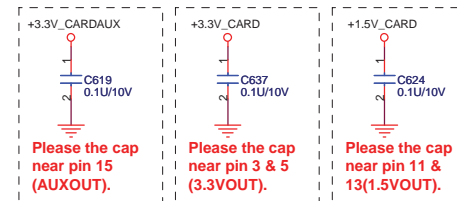
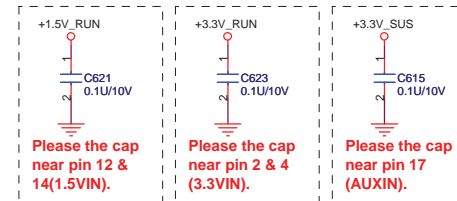
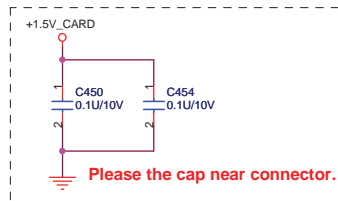
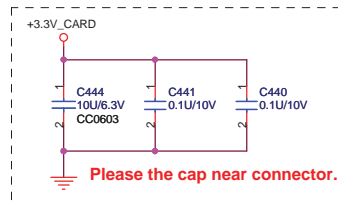
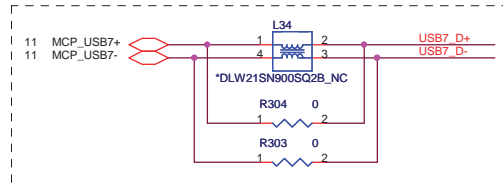
Date: Thursday, October 23, 2008

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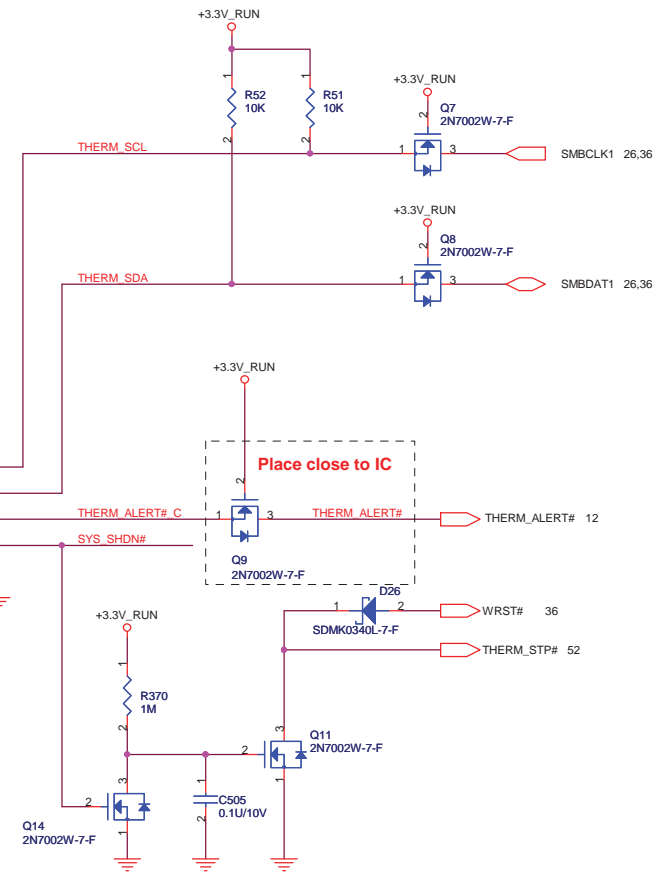
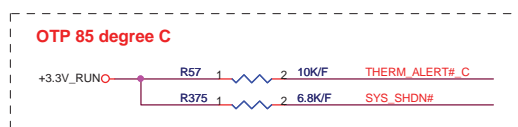
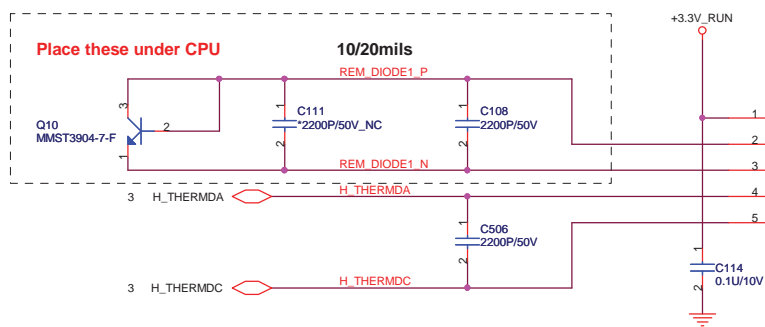
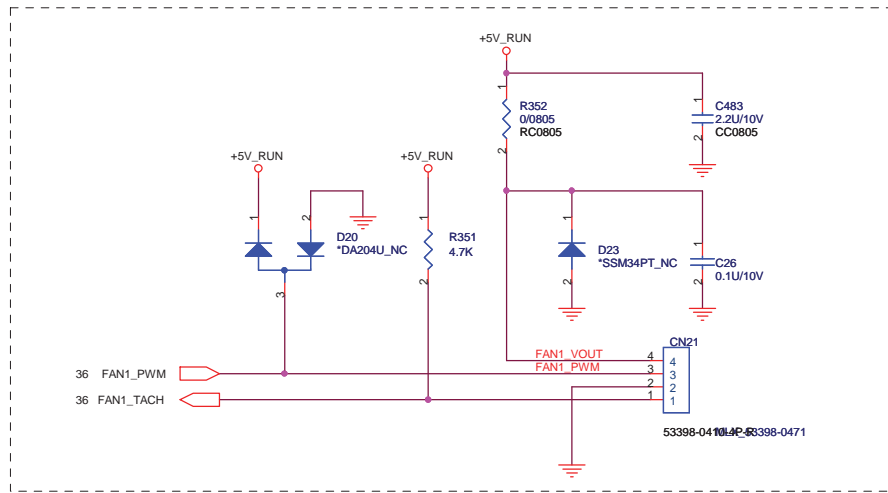
# Express Card

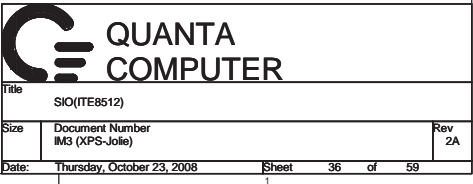


## PCI-Express TX and RX direct to connector.

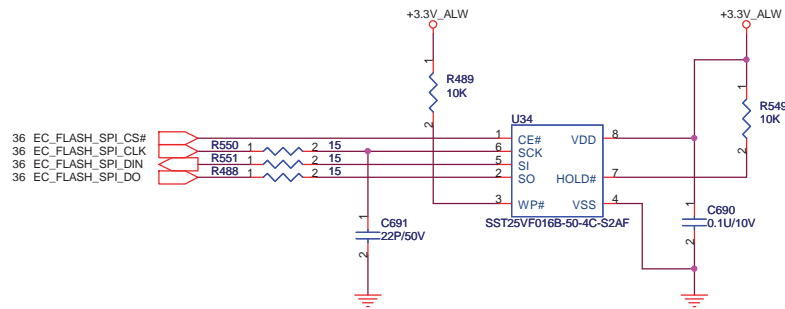




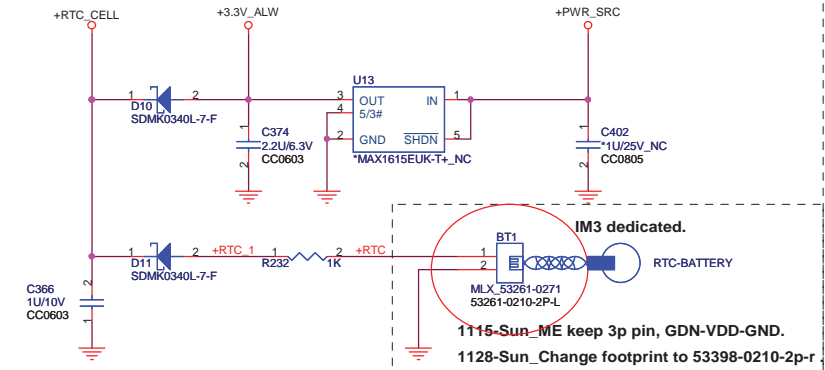




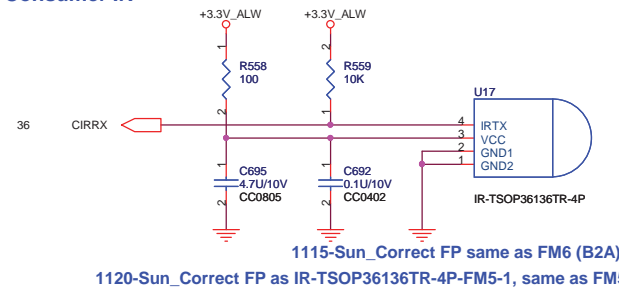
16Mbit (2M Byte), SPI



## RTC BATTERY



## Consumer IR



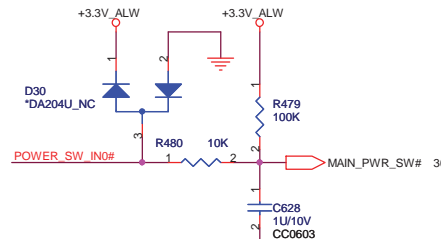
0605\_Michael: Change CN6 from 32pin to 28pin but need to check footprint and PN

### BREATH\_PWRLED\_BOT:

Solid = System On, Normal Activity; "Breathing" = System in Standby; Off = System Off (or in Hibernation)

0420 Michael: Add KB detect function  
1023 Michael: Disable KB LED function  
depop R722 and change R723 from 200K to 0 ohm

### Power Button

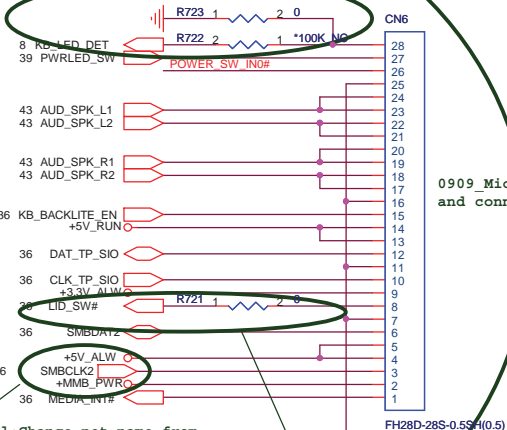


### Speaker

### KB LED

### Touch Pad

### Media Button

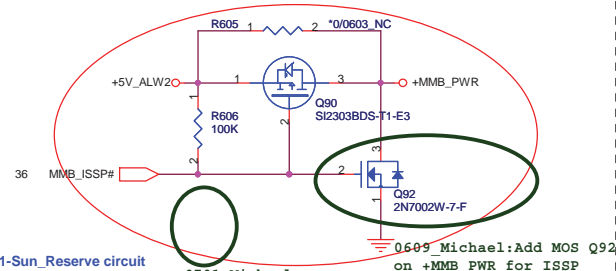


0624 Michael: Change net name from +5V\_ALW2 to +MMB\_PWR  
0704 Michael: Swap SMBCLK2 and +MMB\_PWR for Ass'y issue

0825 Michael: Add KB detect function  
0911 Michael: Change pin from 16 to 8  
0918 Michael: Return to LID\_SW#

0909 Michael: Remove LID\_SW# and connector to GND

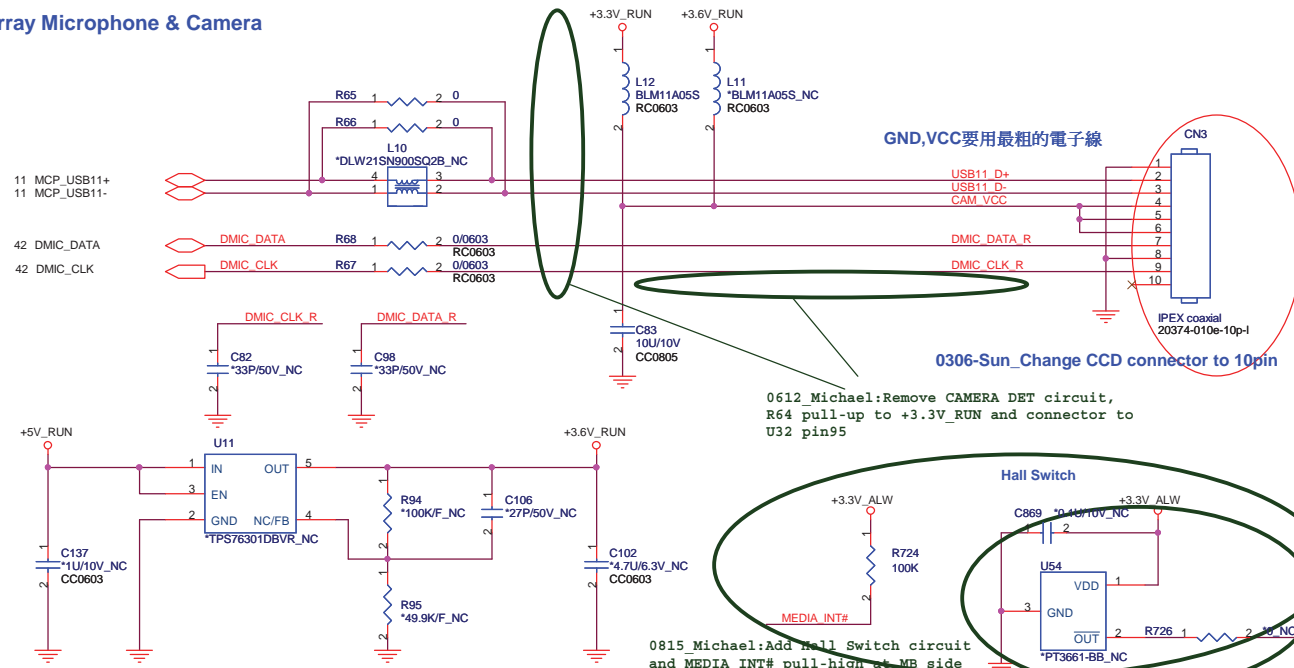
0411-Sun\_Reserve circuit for MMB ISSP support  
0414-Sun\_Change MOSFET control voltage level



0609 Michael: Add MOS Q92 on +MMB\_PWR for ISSP

0701 Michael: Remove Q91 for ISSP

### Array Microphone & Camera



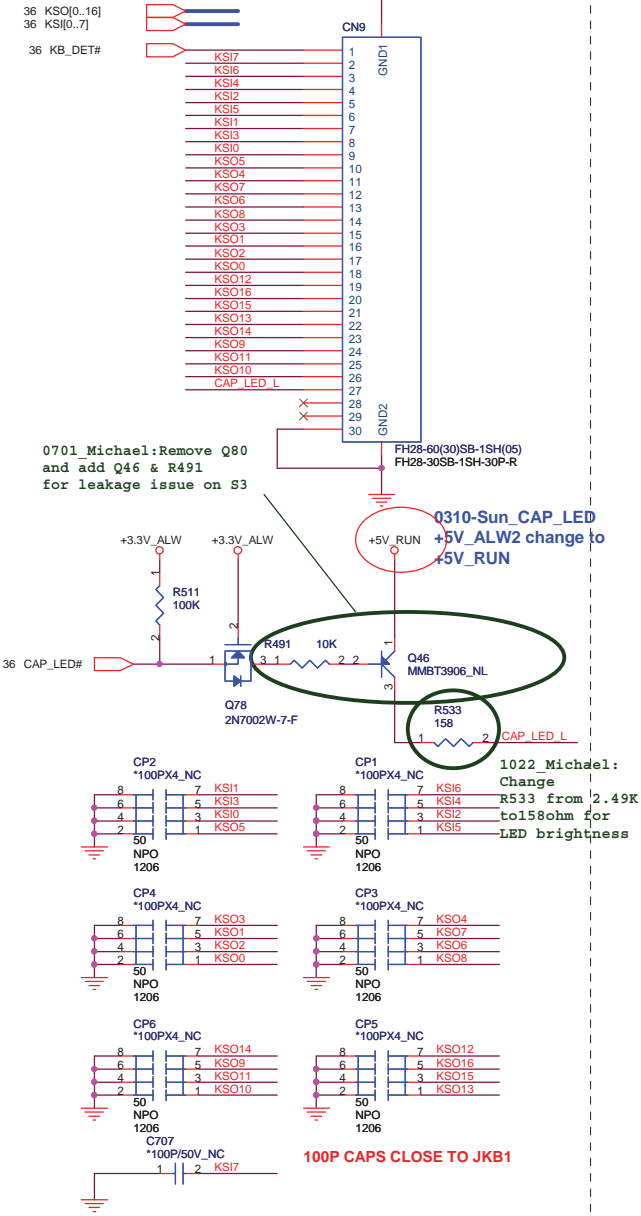
0612 Michael: Remove CAMERA DET circuit, R64 pull-up to +3.3V\_RUN and connector to U32 pin95

### Hall Switch

0815 Michael: Add Hall Switch circuit and MEDIA\_INT# pull-high at MB side

1023 Michael: Depop LID\_Switch function on MB side

### KEYBOARD CONNECTOR



0701 Michael: Remove Q80 and add Q46 & R491 for leakage issue on S3

0310-Sun\_CAP\_LED +5V\_ALW2 change to +5V\_RUN

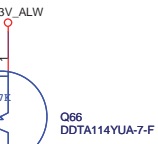
1022 Michael: Change R533 from 2.49K to 158ohm for LED brightness



## Battery status

0313-Sun\_Change battery LED to Amber (3.3V drive)  
(Remove Q68, R462, R460)

0229-Sun\_Remove BAT\_LED controlled by LID\_SW#  
[Del Q69 (2N7002), Q67 (DDTA114YUA); change R462 from 220 to 10K]



0606\_Michael:Add R462 connect to CN2 on BAT1\_LED



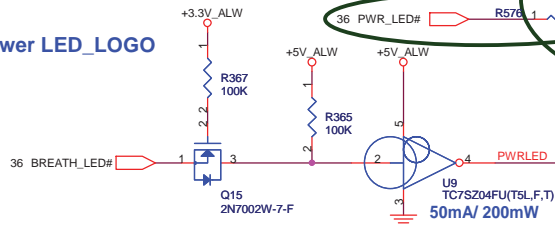
0922\_Michael:Remove BAT1\_AMB\_LED function

0229-Sun\_Del BAT\_LED2  
[Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

0229-Sun\_Change PWRLED\_SW control same as PWRLED\_LOGO  
[Del U10 (TC7S204F), Q16 (2N7002)]

0904\_Michael:Add R576 and connector to PWR\_LED# from ITE8512

## Power LED\_LOGO



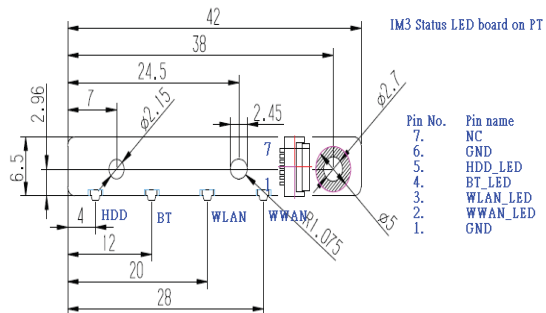
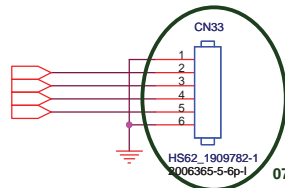
0618\_Michael:Follow DELL command modify circuit to change the LED behavior of Power button

1022\_Michael:Change R390 from 1K to 390ohm for LED brightness

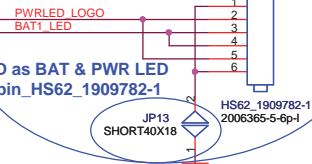
1022\_Michael:Change R366 from 220ohm to 100ohm for LED brightness

0229-Sun\_Remove LED control by LID\_SW#  
(Del R478,R477,Q75)

0704\_Michael:Change CN33 pin number from 7pin to 6pin and also change type from HEADER7 to HS62\_1909782-1 for cost down



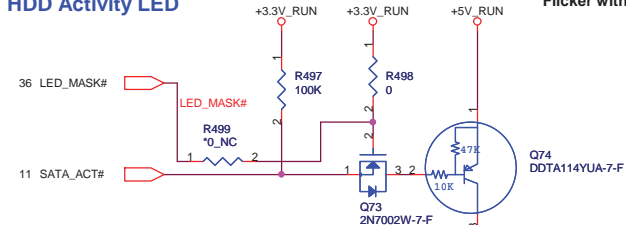
## Logo LED/B connector



0306-Sun\_Change Logo LED as BAT & PWR LED and change connector to 6pin\_HS62\_1909782-1

0314-Sun\_Add short pad on GND of Logo LED/B connector for EMI request.

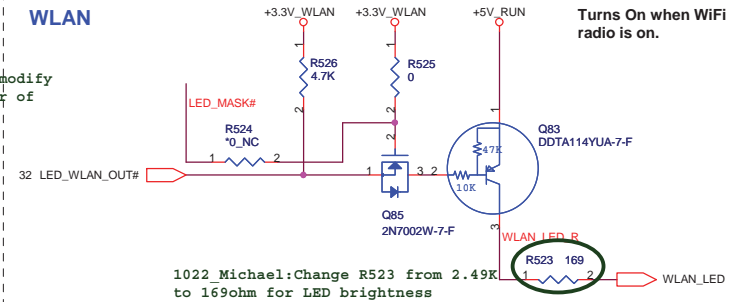
## HDD Activity LED



Flicker with HDD activity.

1022\_Michael:Change R500 from 2.49K to 169ohm for LED brightness

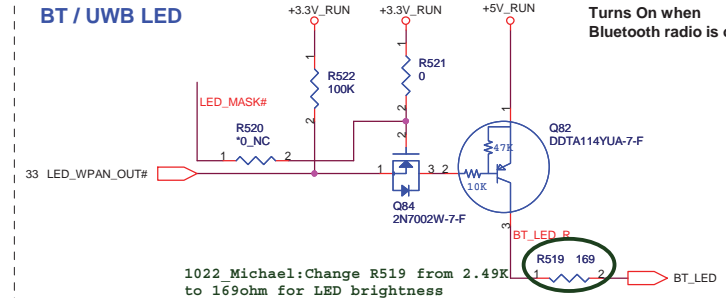
## WLAN



Turns On when WiFi radio is on.

1022\_Michael:Change R523 from 2.49K to 169ohm for LED brightness

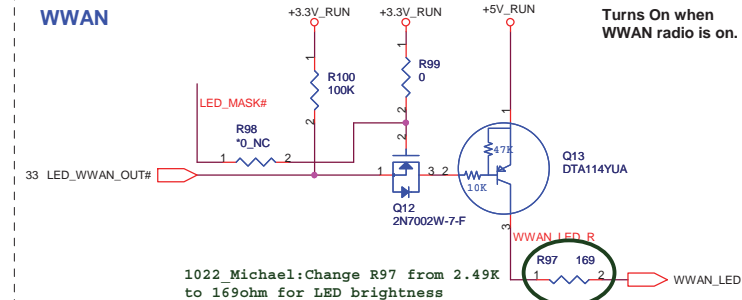
## BT / UWB LED



Turns On when Bluetooth radio is on.

1022\_Michael:Change R519 from 2.49K to 169ohm for LED brightness

## WWAN



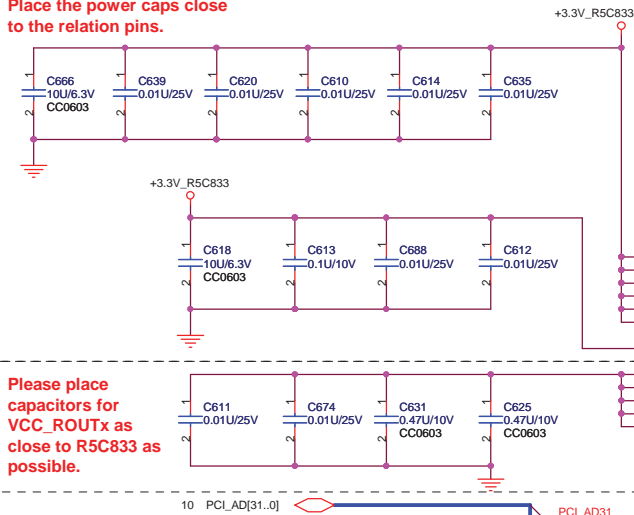
Turns On when WWAN radio is on.

1022\_Michael:Change R97 from 2.49K to 169ohm for LED brightness

QUANTA COMPUTER

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Place the power caps close to the relation pins.

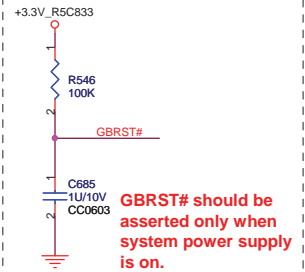
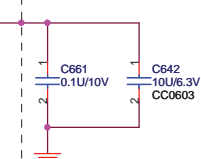


Please place capacitors for VCC\_ROUTx as close to R5C833 as possible.

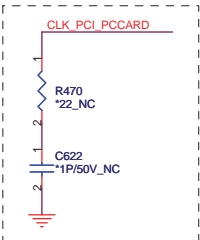


0606\_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)

Place the power caps close to the relation pins.



GBRST# should be asserted only when system power supply is on.



10 PCI\_PAR  
10 PCI\_C\_BE3#  
10 PCI\_C\_BE2#  
10 PCI\_C\_BE1#  
10 PCI\_C\_BE0#

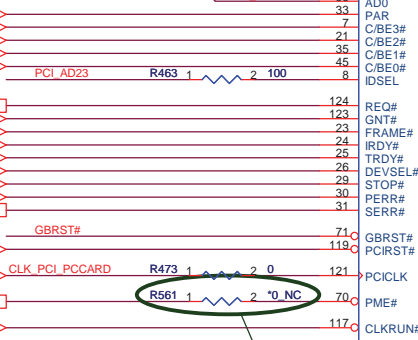
10 PCI\_REQ0#  
10 PCI\_GNT0#  
10 PCI\_FRAME#  
10 PCI\_IRDY#  
10 PCI\_TRDY#  
10 PCI\_DEVSEL#  
10 PCI\_STOP#  
10 PCI\_PERR#  
10 PCI\_SERR#

10 PCI\_RST#  
10 CLK\_PCI\_PCCARD  
10 PCI\_PME#  
10,36 CLKRUN#

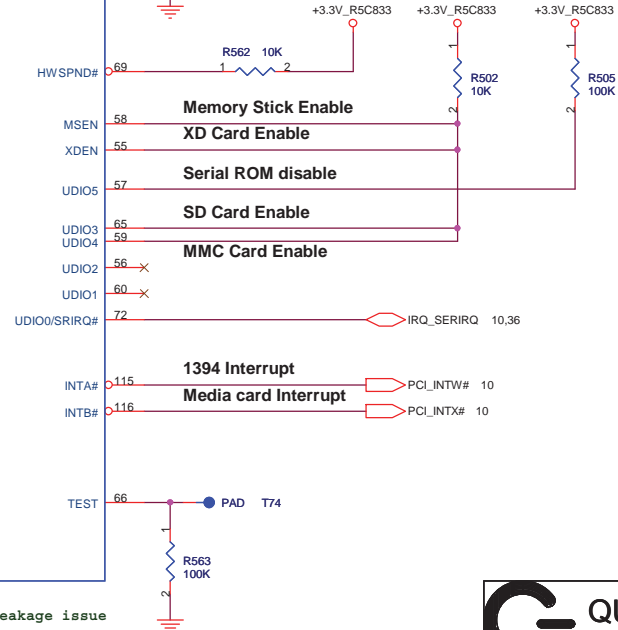
PCI AD23

GBRST#

CLK\_PCI\_PCCARD



PCI / OTHER



Memory Stick Enable  
XD Card Enable  
Serial ROM disable  
SD Card Enable  
MMC Card Enable

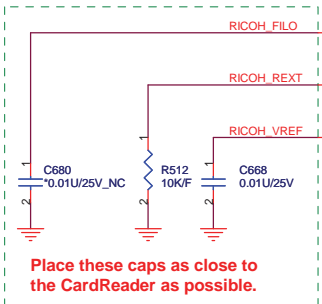
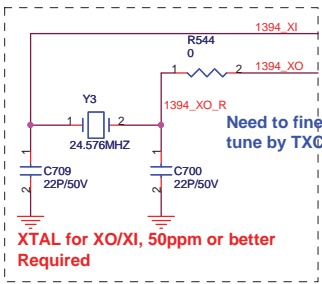
1394 Interrupt  
Media card Interrupt

0630\_Michael:Remove Mini PCI CN8 and circuit

0707\_Michael:Depop R561 for leakage issue

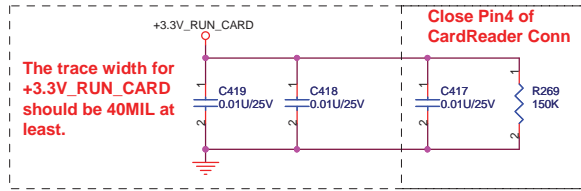
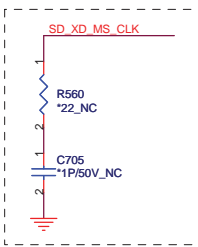






Card Reader interface signal mapping

PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#	MS_CD#	XD_CD#
MDIO01				XD_CD1#
MDIO02	SD_WP#	MMC_PWR	MS_PWR	XD_E/B#
MDIO03	SD_PWR0	MMC_PWR	MS_PWR	XD_PWR
MDIO04	SD_PWR1	MMC_PWR	MS_PWR	XD_PWR
MDIO05	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO06	MS_TEST			
MDIO07	SD_CMD	MMC_CMD	MS_CMD	XD_CMD
MDIO08	SD_CLK	MMC_CLK	MS_CLK	XD_CLK
MDIO09	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO10	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO11	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO12	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO13	SD_D4	MMC_D4	MS_D4	XD_D4
MDIO14	SD_D5	MMC_D5	MS_D5	XD_D5
MDIO15	SD_D6	MMC_D6	MS_D6	XD_D6
MDIO16	SD_D7	MMC_D7	MS_D7	XD_D7
MDIO17				XD_CLE
MDIO18				XD_ALE
MDIO19				



AVCC\_PHY1  
AVCC\_PHY2  
AVCC\_PHY3  
AVCC\_PHY4

IEEE1394 / SD

MDIO17 XD-D7 MS-D7

MDIO16 XD-D6 MS-D6

MDIO15 XD-D5 MS-D5

MDIO14 XD-D4 MS-D4

MDIO13 SD-D3 XD-D3 MS-D3

MDIO12 SD-D2 XD-D2 MS-D2

MDIO11 SD-D1 XD-D1 MS-D1

MDIO10 SD-D0 XD-D0 MS-D0

MDIO05 XD\_WP#

MDIO08 SD\_XD\_MS\_CMD

MDIO19 XD\_ALE

MDIO18 XD\_CLE

MDIO02 XD\_CE#

MDIO03 SD\_WP# XDR\_B#

MDIO00 SD\_CD#

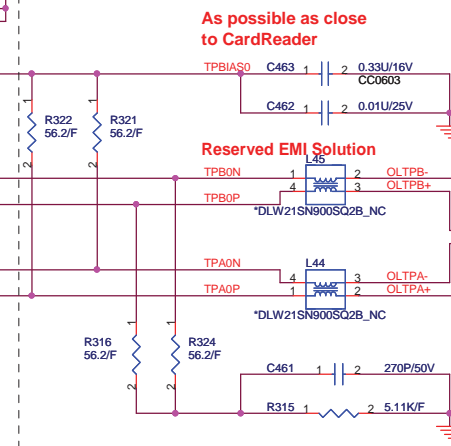
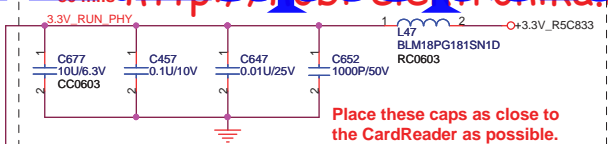
MDIO01 MS\_INS#

MDIO09 SD\_XD\_MS\_CLK

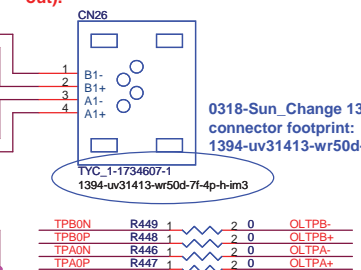
MDIO04 MC\_PWR\_CTRL\_0

MDIO06 T44 PAD

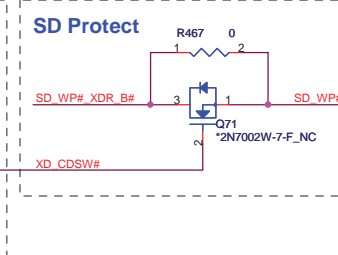
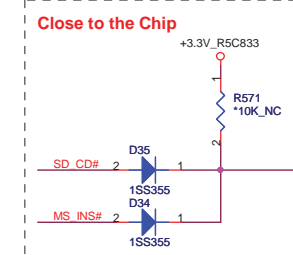
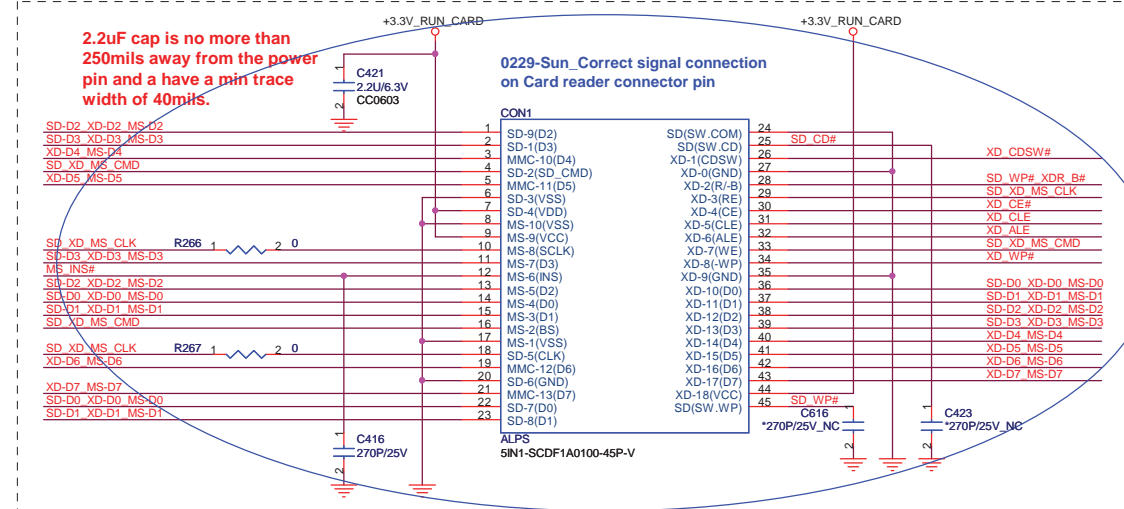
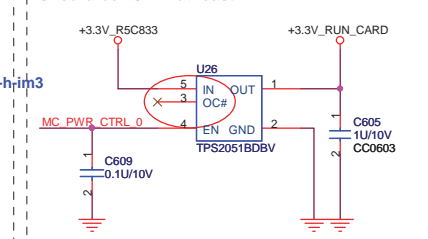
MDIO07

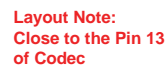
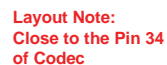


1. TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
2. TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
3. Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



- Layout Note:
- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
  - 2). The trace width for +3.3V\_RUN\_CARD should be 40MIL at least.
  - 3). The GND trace for Media Card Socket should be 40MIL at least.





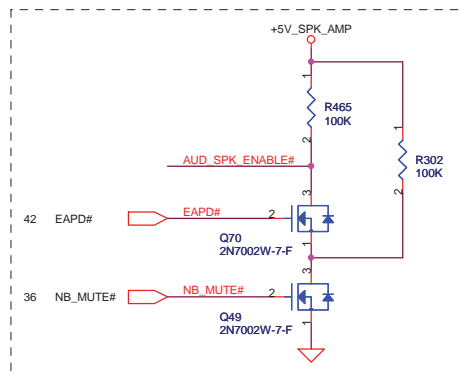
## AZALIA (HD) CODEC



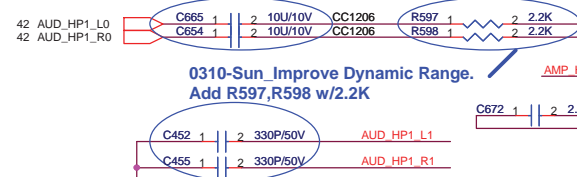
**Depop R403, R404, R409, and R411  
Pop R406, R407, R408, and R410  
for using 92HD71C1**

0315-Sun\_Change to DMIC\_CLK  
damping to 22 ohm

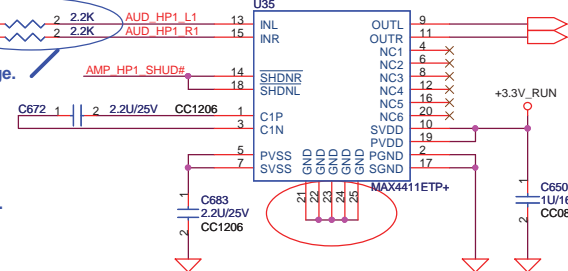
## Close to CODEC



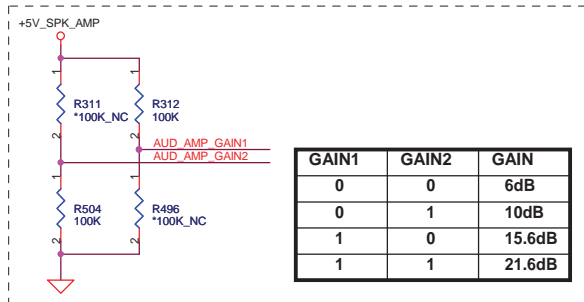
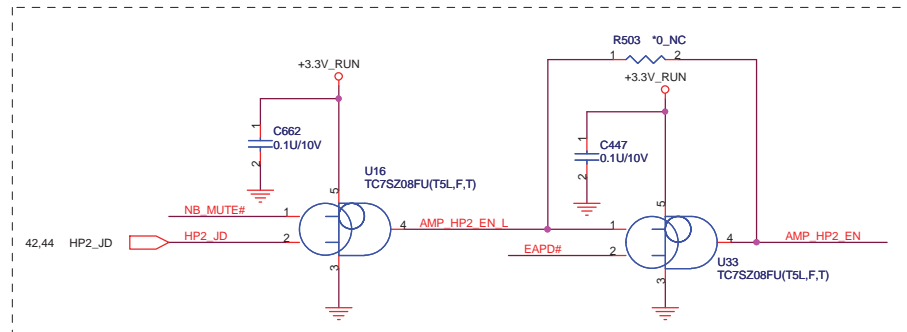
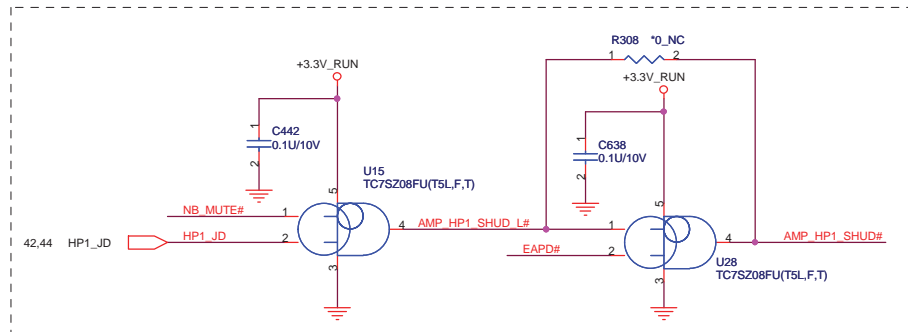
0315-Sun\_Improve Dynamic Range.  
0320-StegChange AC coupling to 10U/10V



0315-Sun\_Improve Dynamic Range.  
Pop C452,C455 to 330P

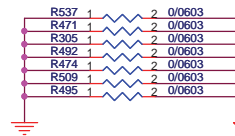


Layout Note:  
TPA 4411 : cannot connect EP to GND.  
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.

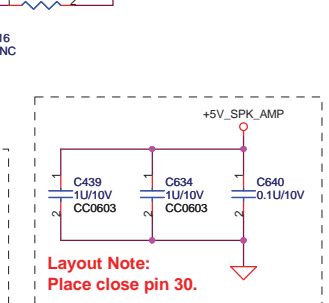
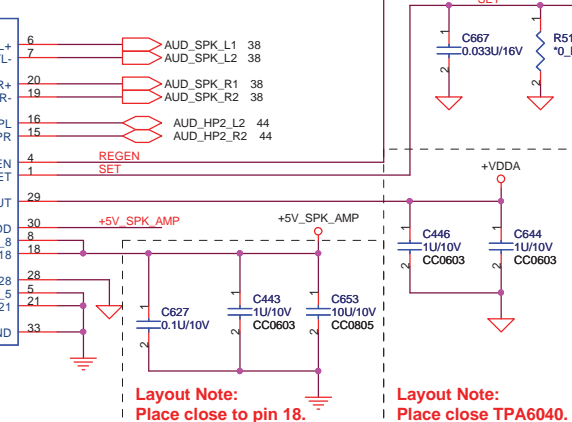
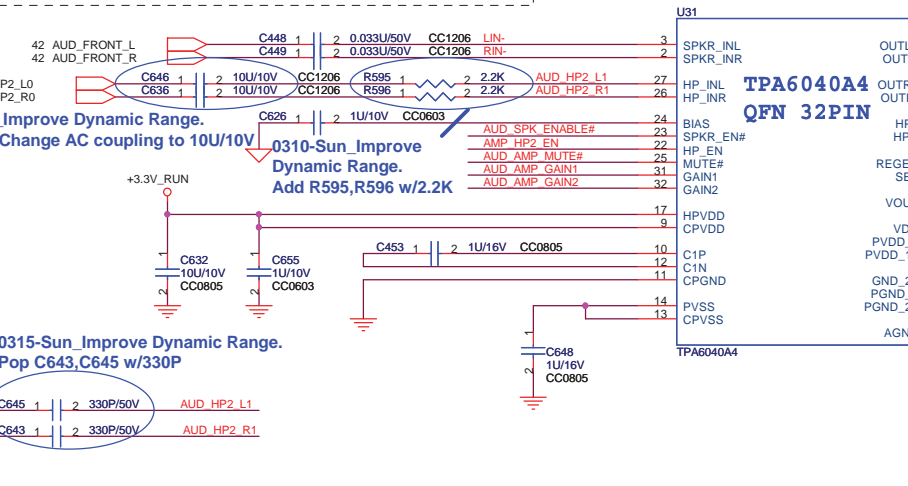


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

EMI Reserved



Layout Note:  
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.  
TPA 4411 : cannot connect EP to GND.  
MAX 4411: can connect EP to GND.

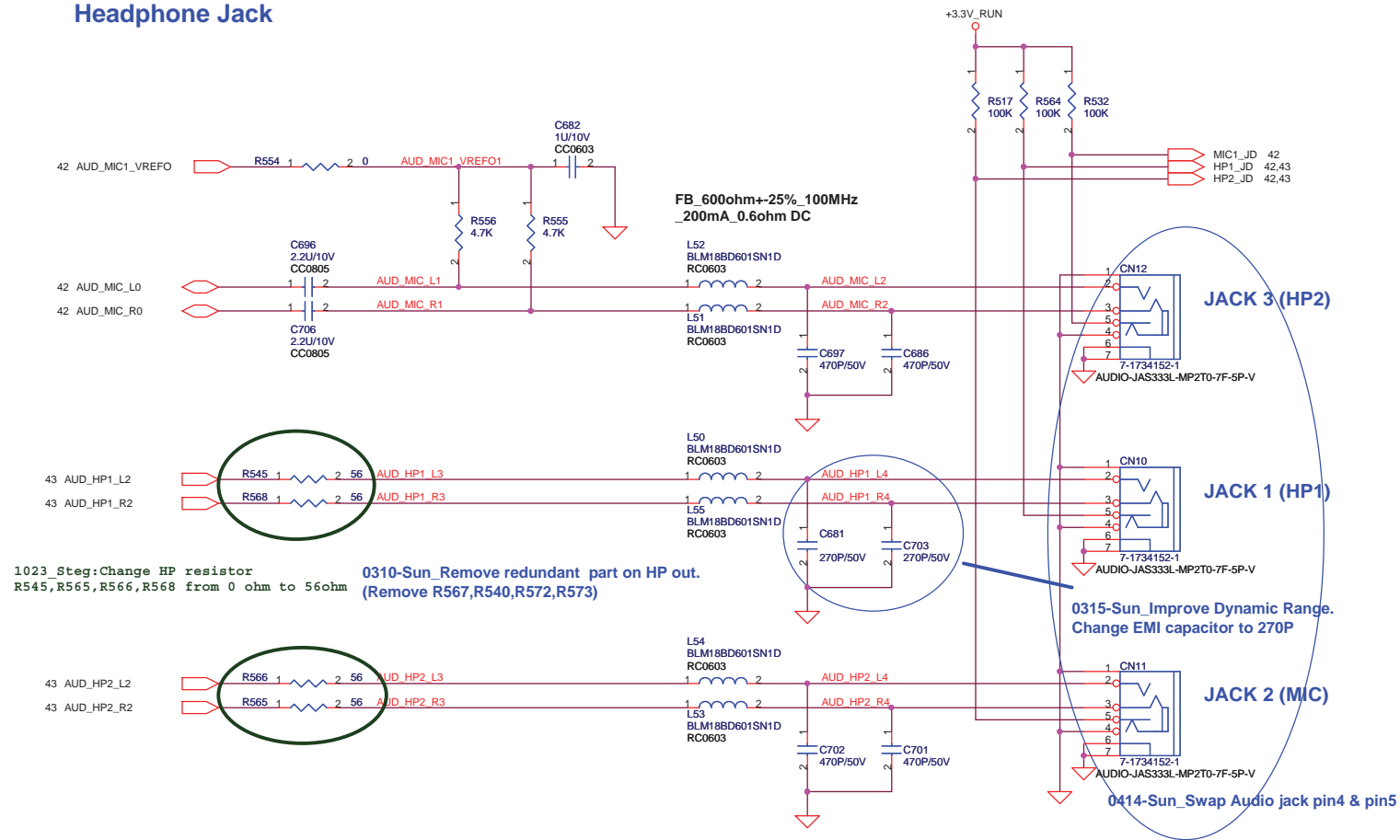


Layout Note:  
Place close pin 30.

Layout Note:  
Place close to pin 18.

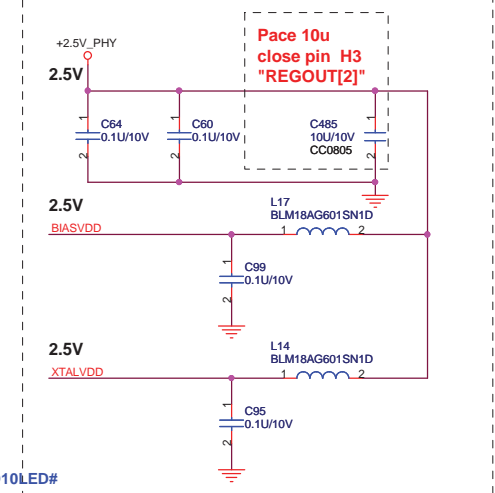
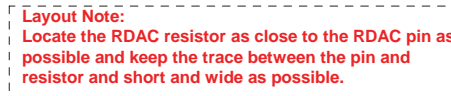
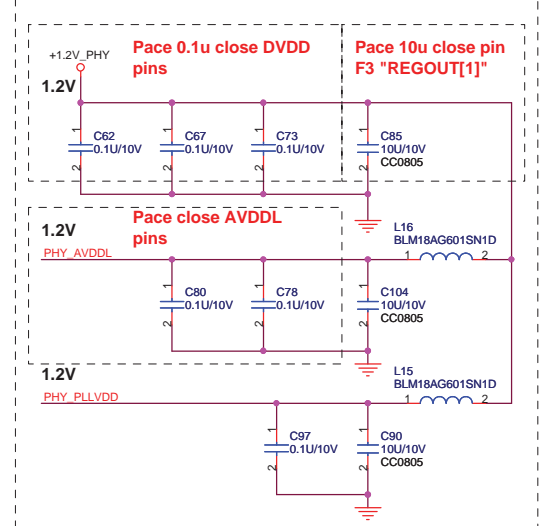
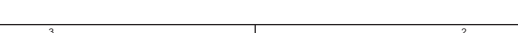
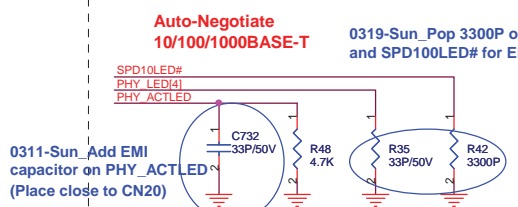
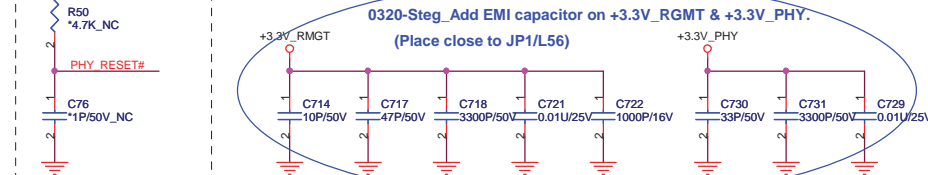
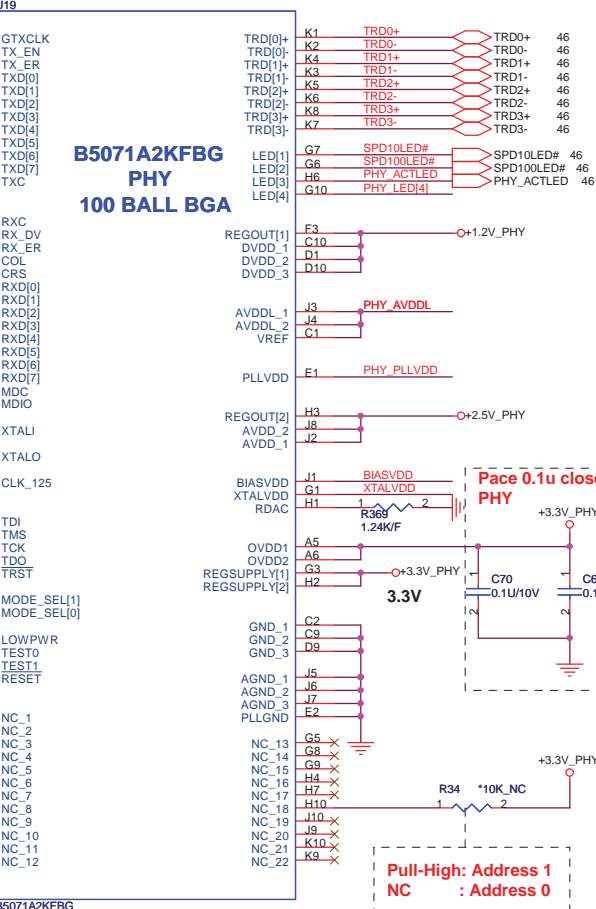
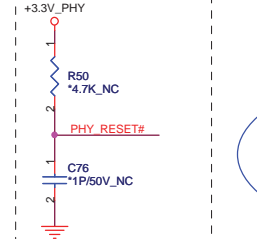
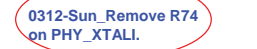
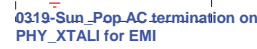
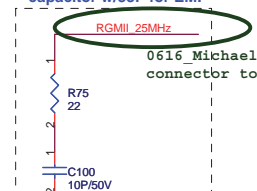
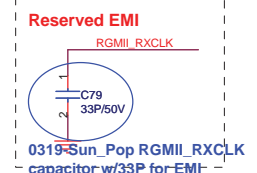
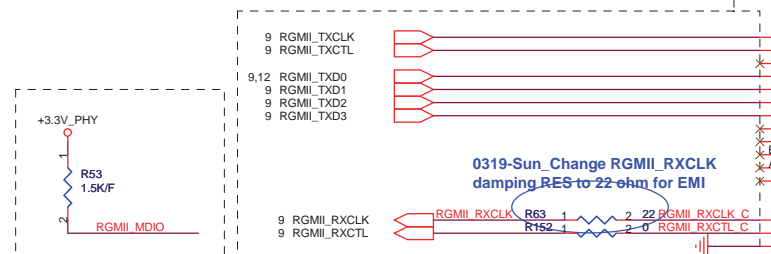
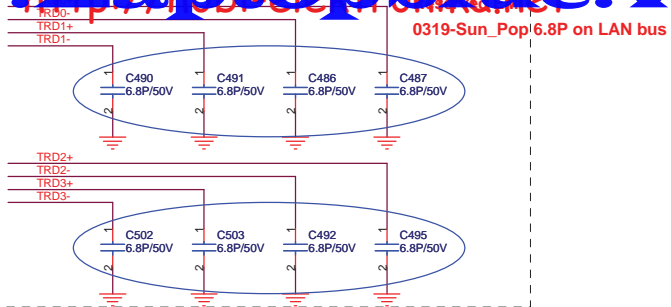
Layout Note:  
Place close TPA6040.

## Headphone Jack



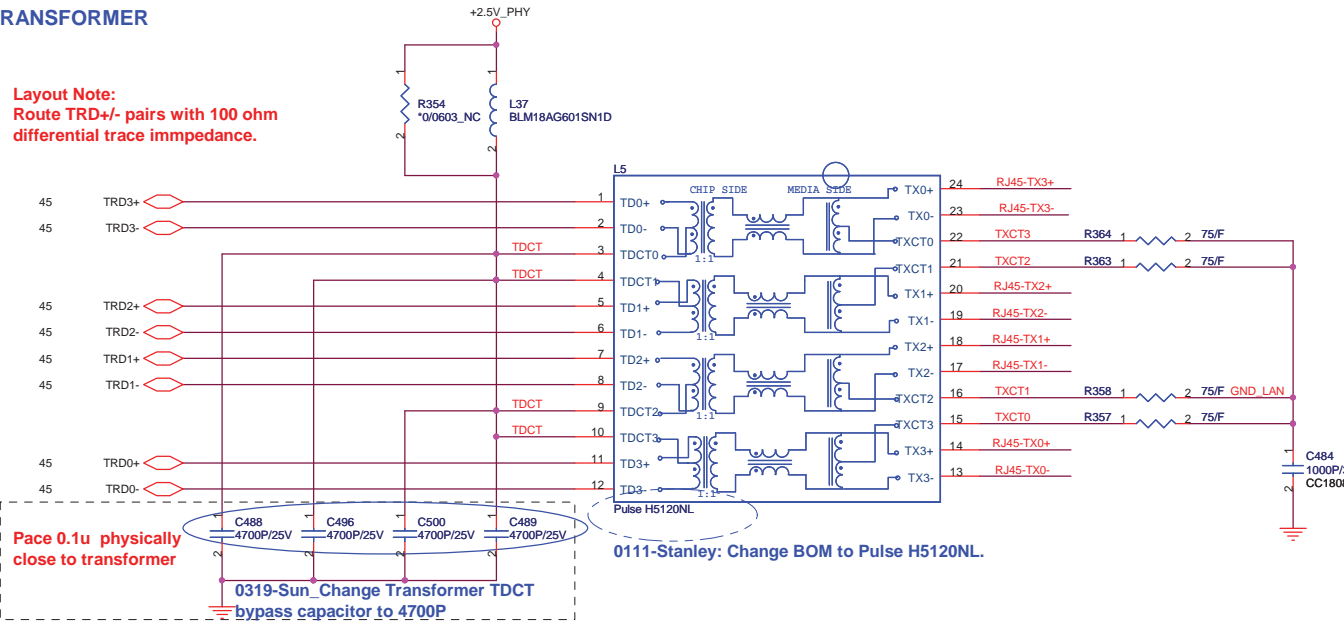
### Layout Note:

1. Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



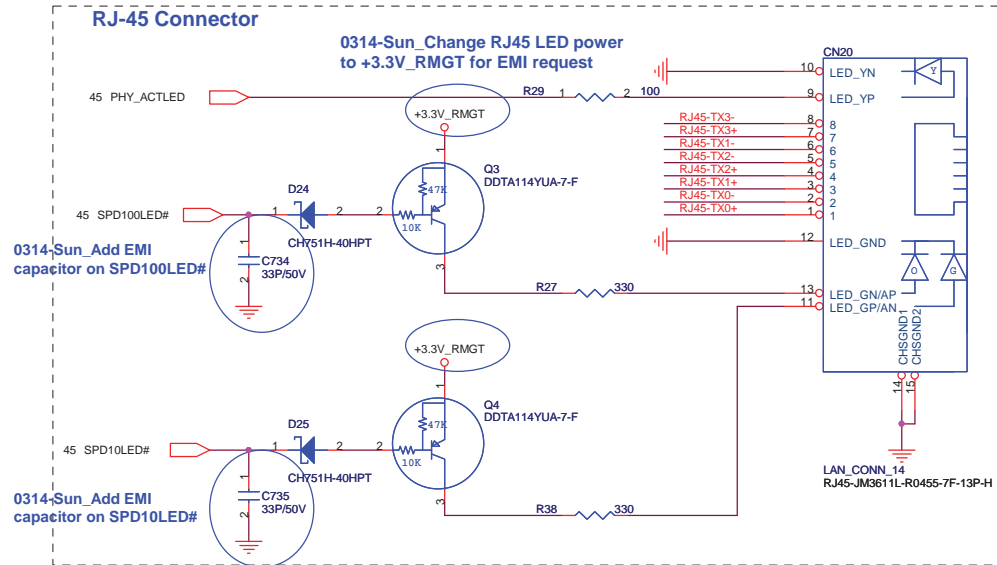
## TRANSFORMER

**Layout Note:**  
Route TRD+/- pairs with 100 ohm differential trace impedance.



## RJ-45 Connector

### 0314-Sun\_Change RJ45 LED power to +3.3V\_RMGT for EMI request



Title	LAN SWITCH
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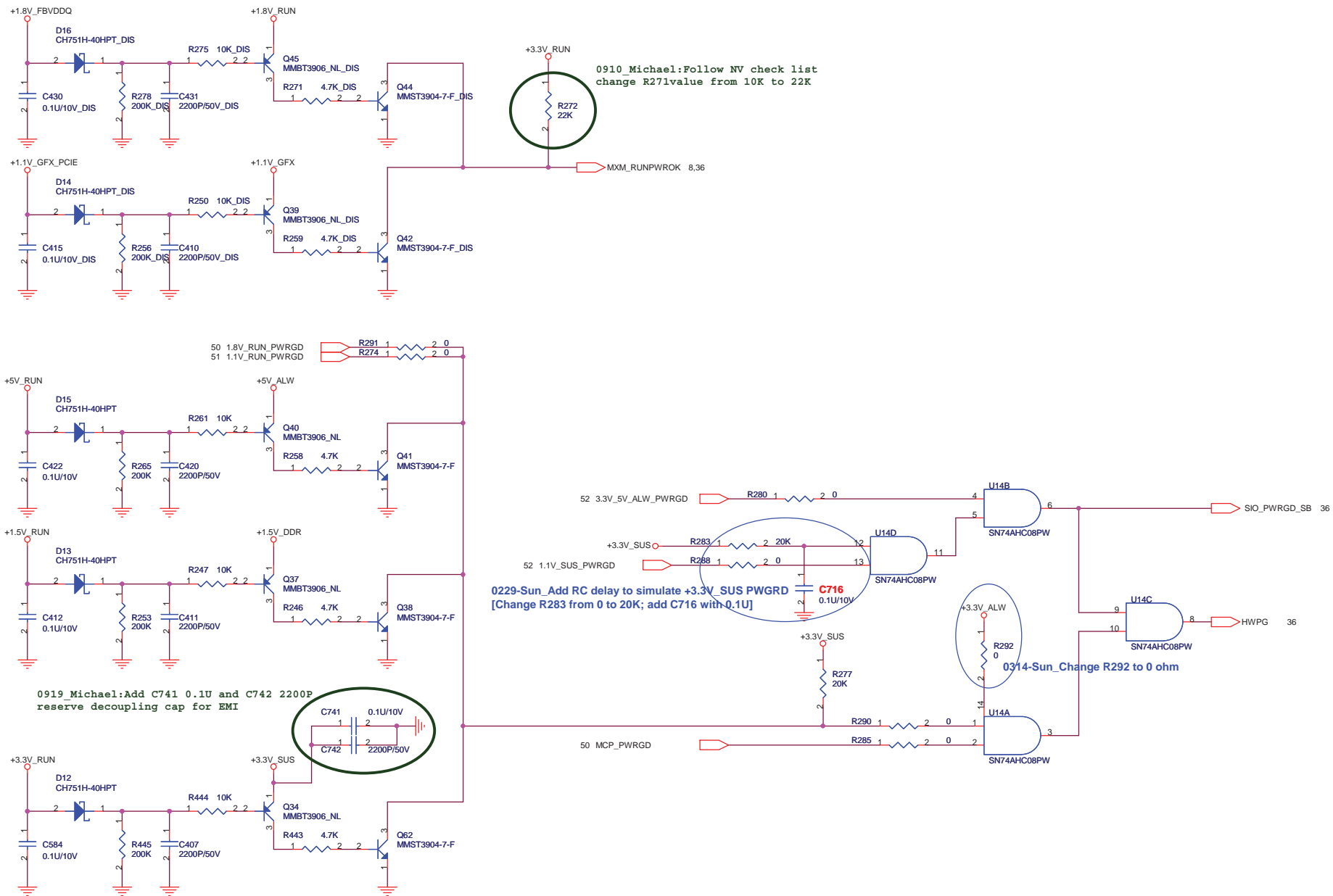
Size	Document Number IM3 (XPS-Jolie)
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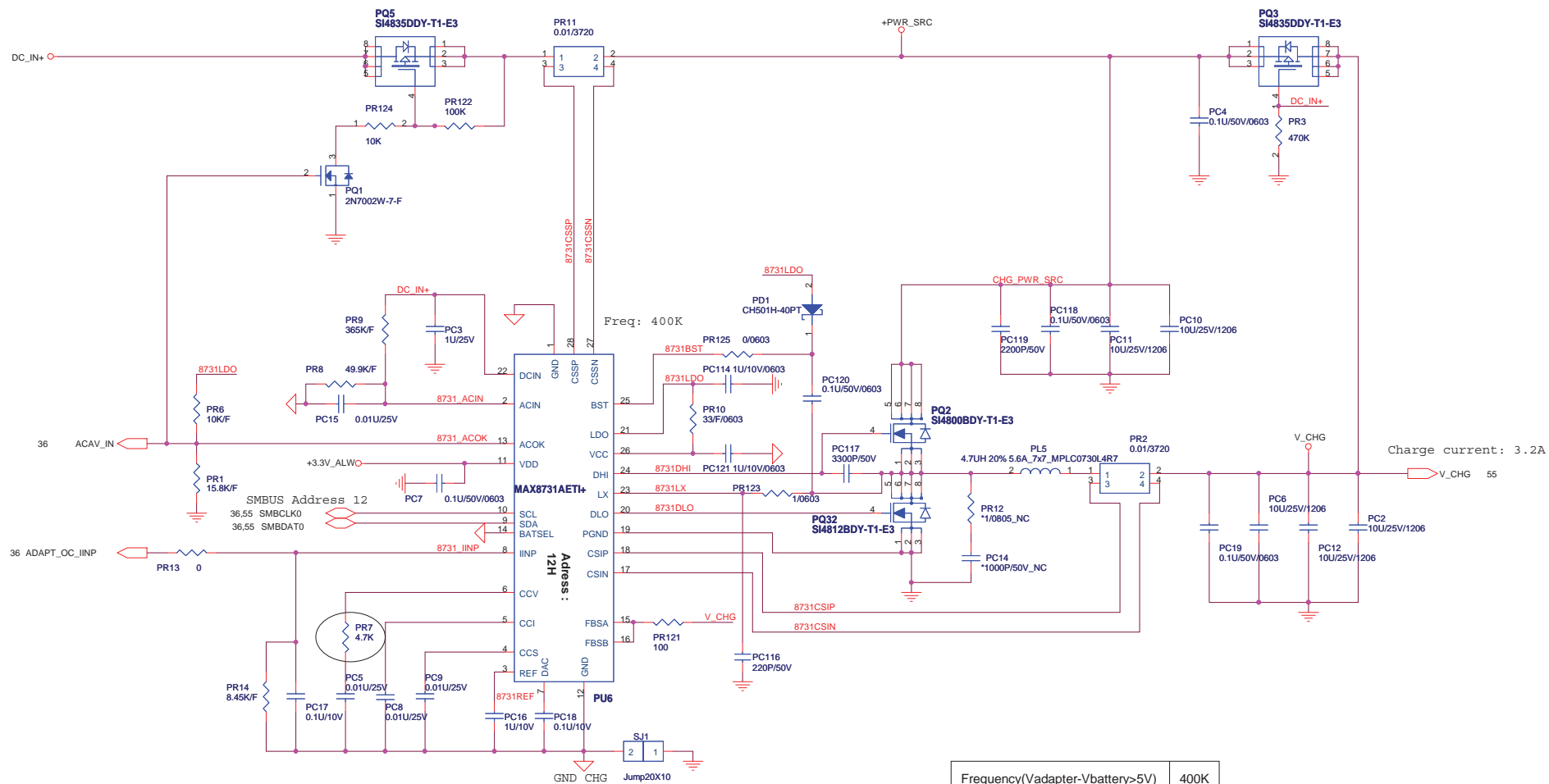
Rev	
2A	

Date: Friday, September 05, 2008

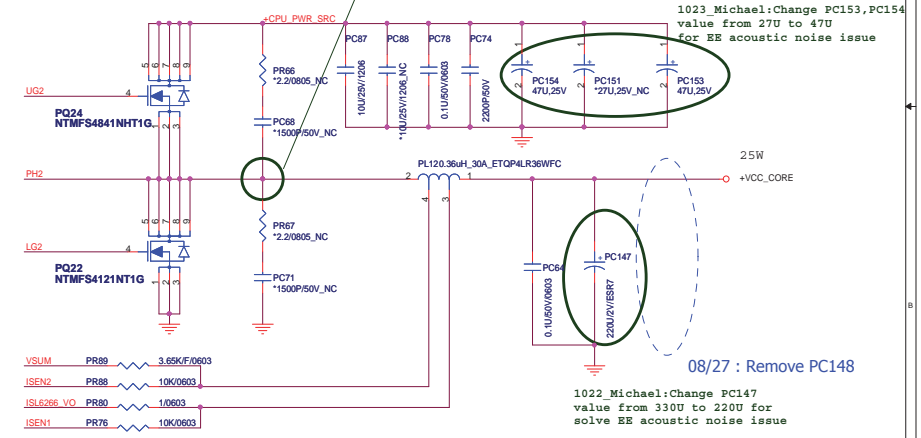
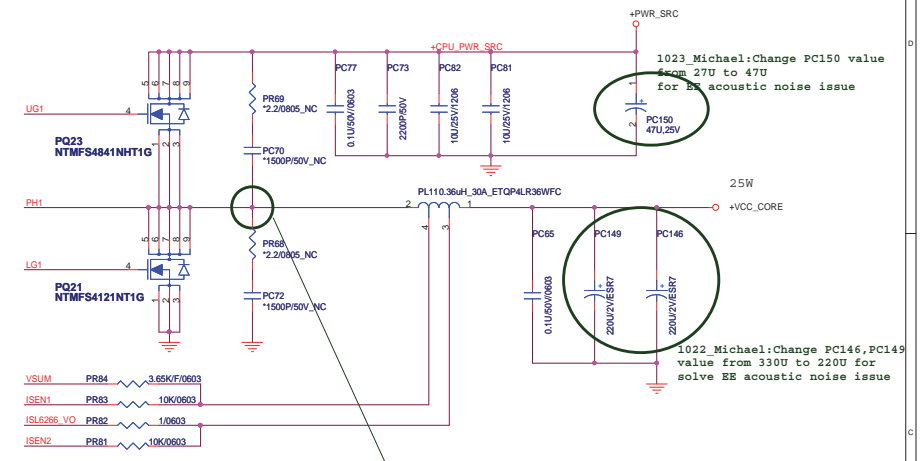
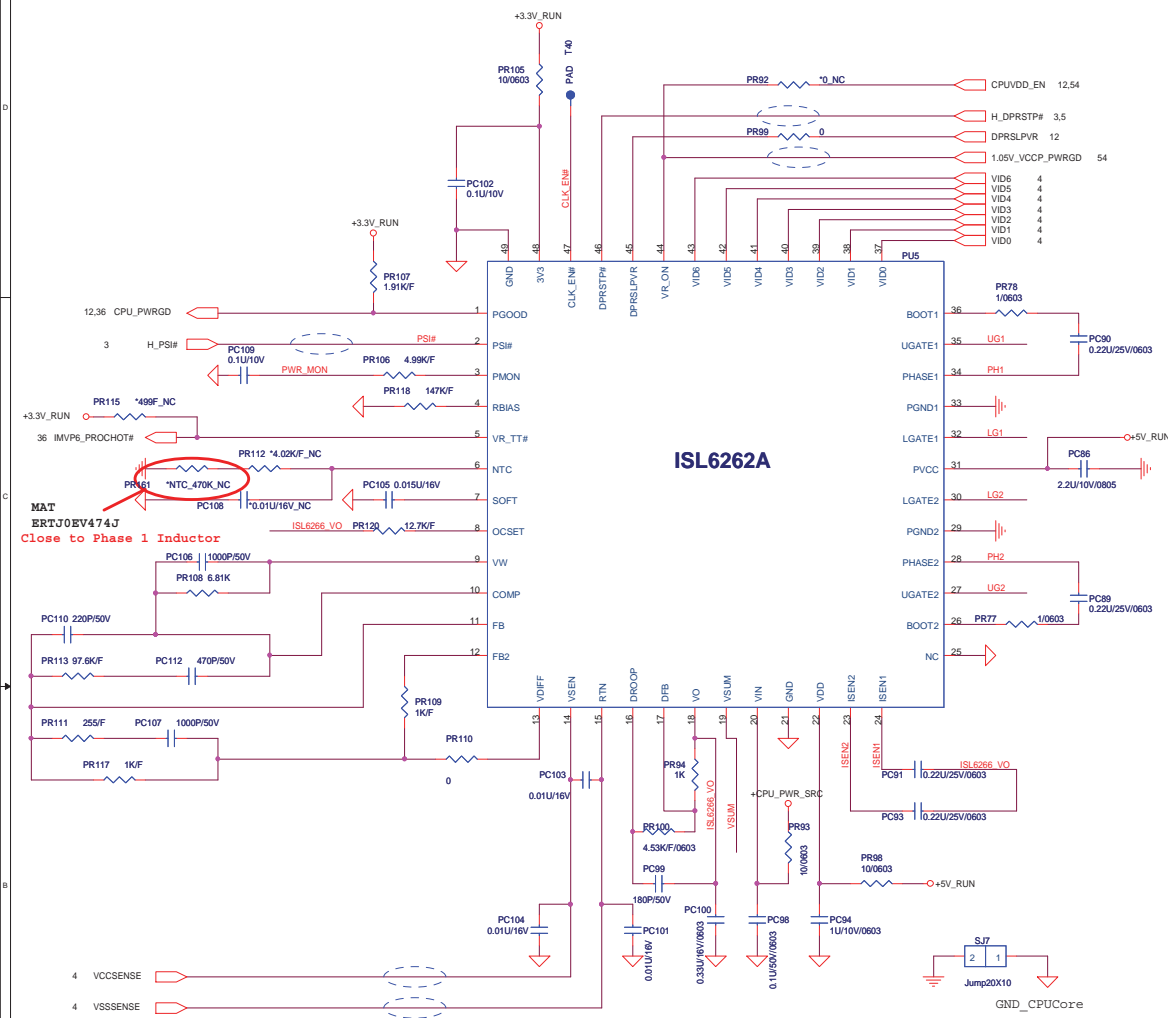
Sheet 46 of 59



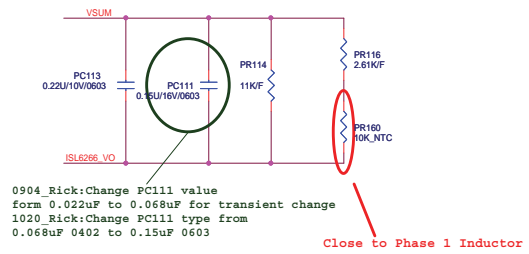




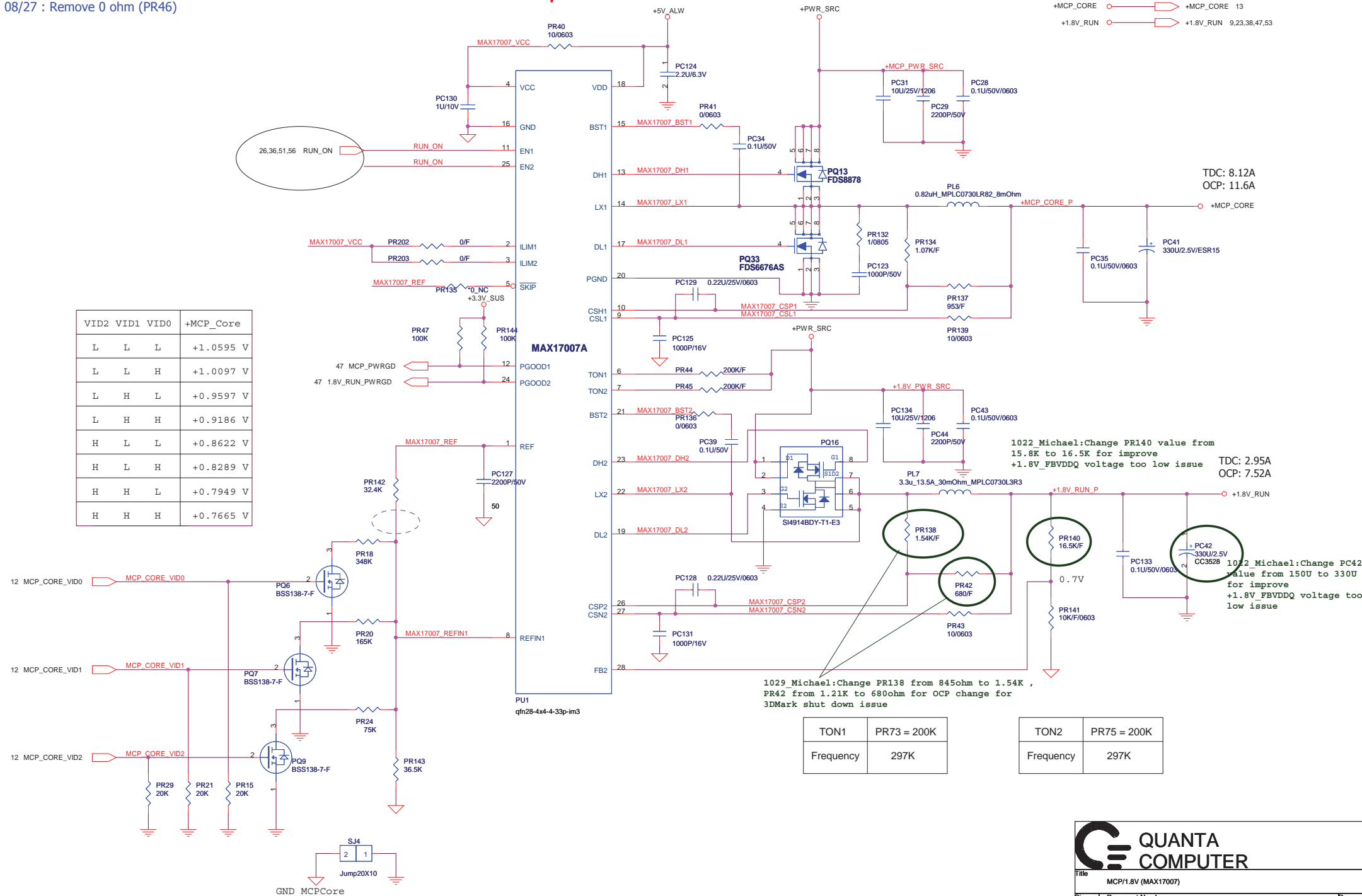
08/27 : Remove 0 ohm (PR102, PR97, PR119, PR104, PR103)



VW	PR37
Frequency	270KHZ@0A / 310KHZ@44A

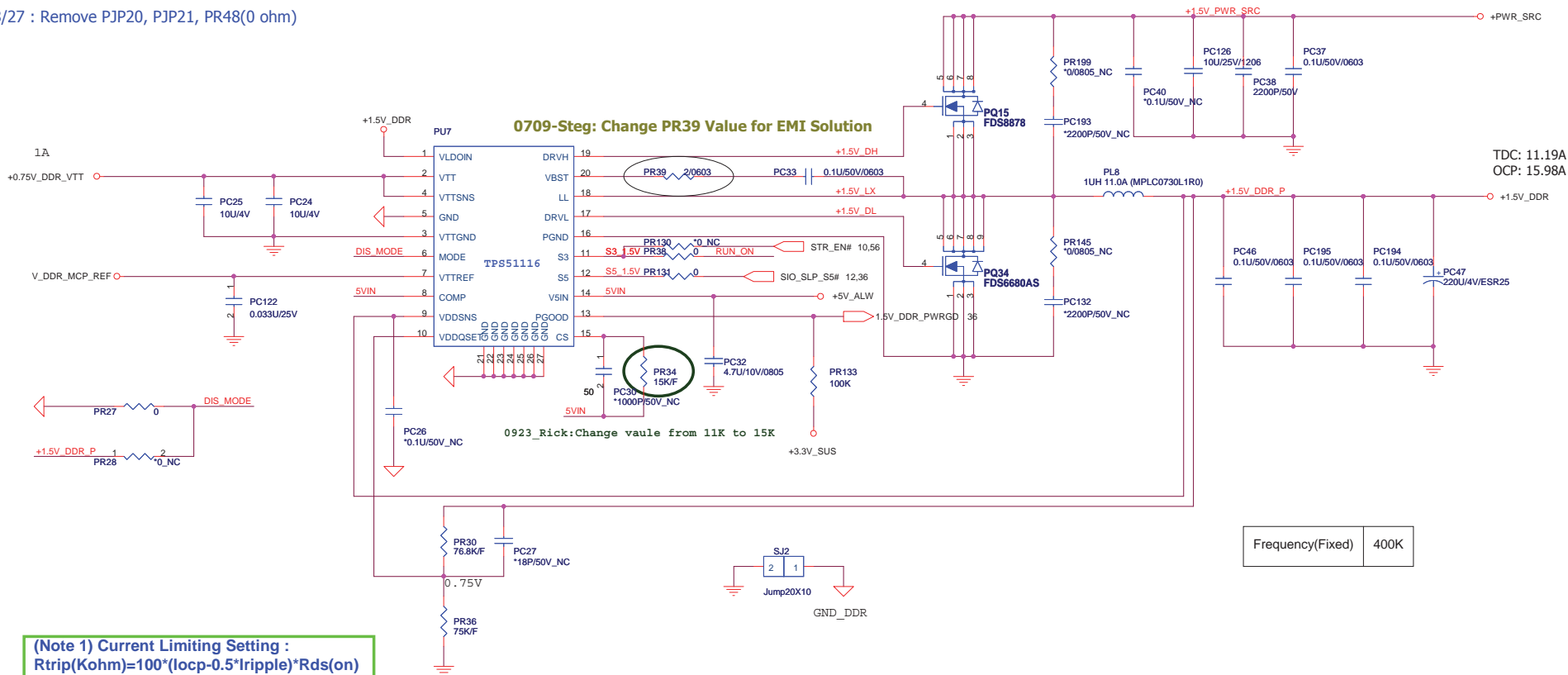


VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V

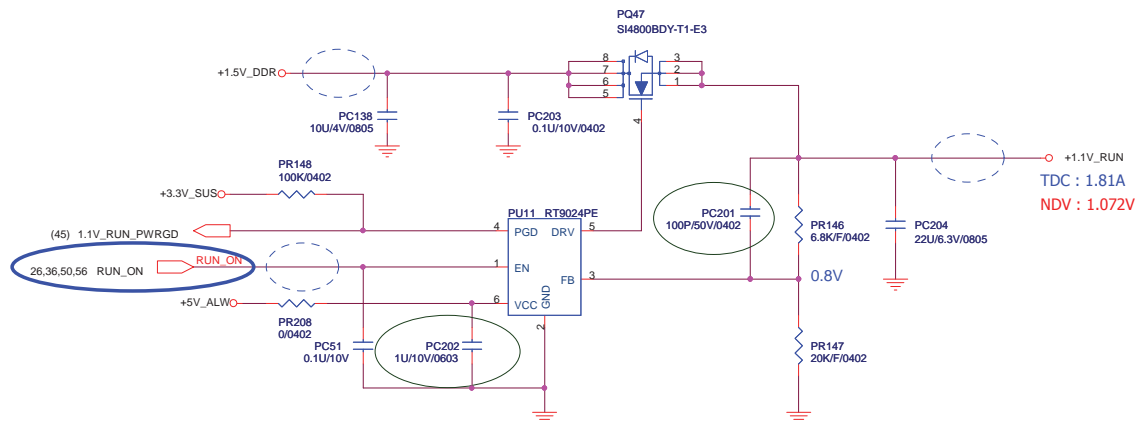


+1.5V\_DDR ○ → +1.5V\_DDR 15,16,47,56  
 +0.75V\_DDR\_VTT ○ → +0.75V\_DDR\_VTT 15,16,56  
 +1.1V\_RUN ○ → +1.1V\_RUN 5,7,8,9,11,12  
 V\_DDR\_MCP\_REF ○ → V\_DDR\_MCP\_REF 15,16

08/27 : Remove PJP20, PJP21, PR48(0 ohm)

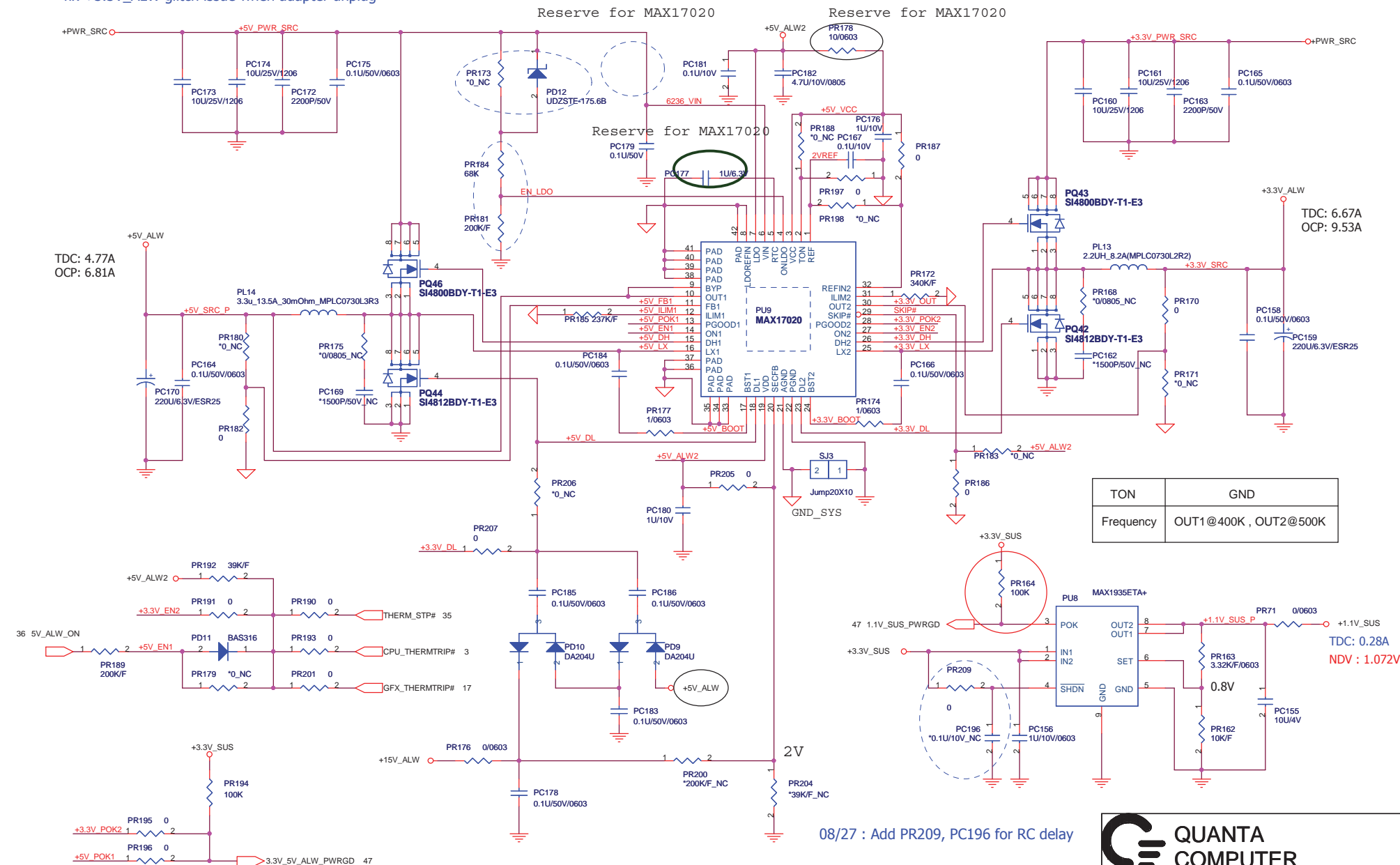


(Note 1) Current Limiting Setting :  
 $R_{trip(Kohm)} = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



0916 Rick:Change PC177 value from 0.1U to 1U

08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V\_ALW glitch issue when adapter unplug



08/27 : Add PR209, PC196 for RC delay

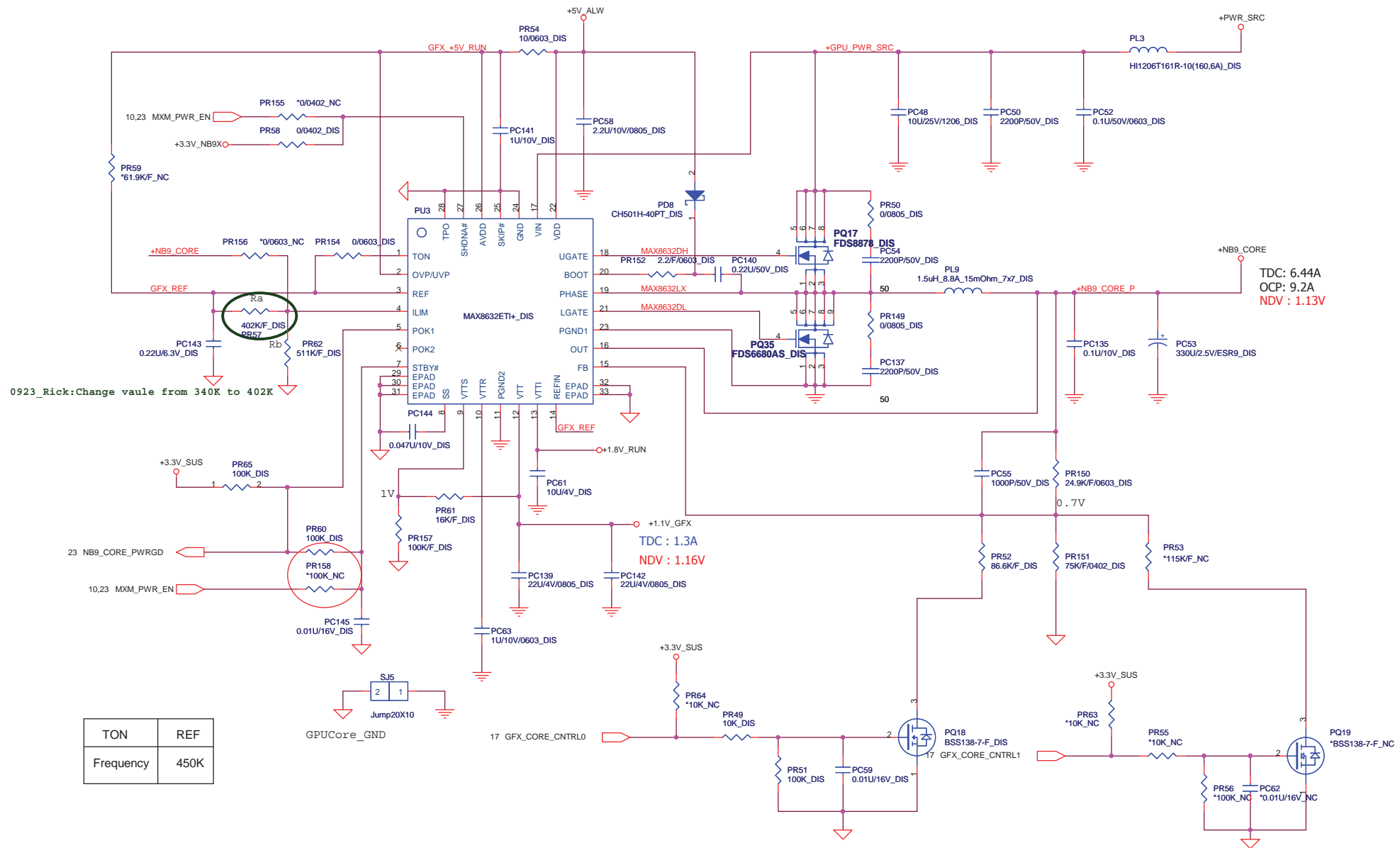


QUANTA  
COMPUTER

Title				SYS 5V/3V(MAX17020)			
Size	Document Number						Rev
	IM3 (XPS-Jolie)						1
Date:	Thursday, October 30, 2008				Sheet	52	of 59



+NB9\_CORE 20  
+1.1V\_GFX 23,47



ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

**QUANTA COMPUTER**

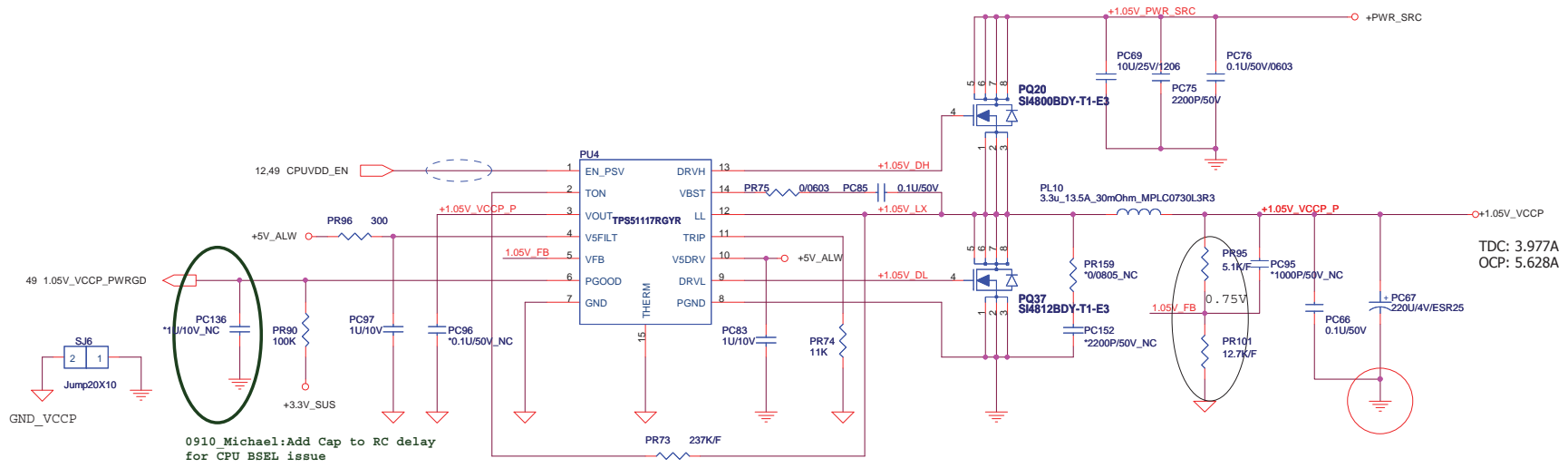
Title: VGA DC/DC

Size: Document Number IM3 (XPS-Jolie) Rev 1A

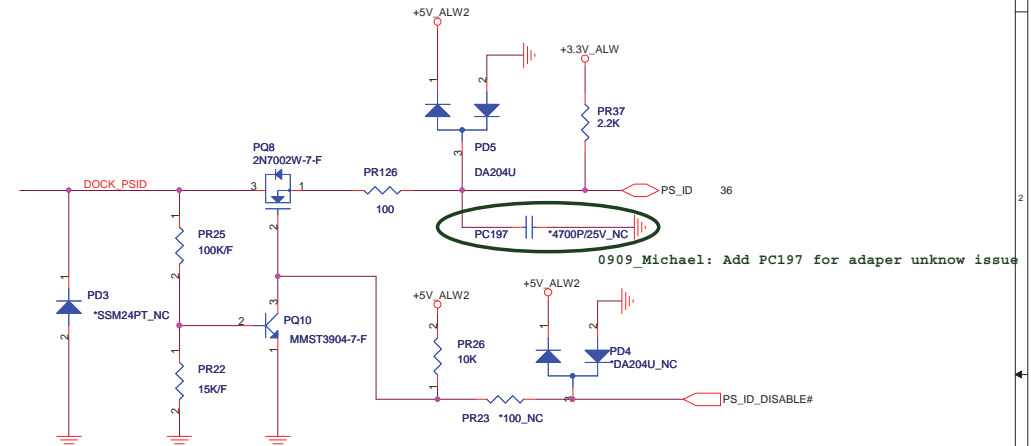
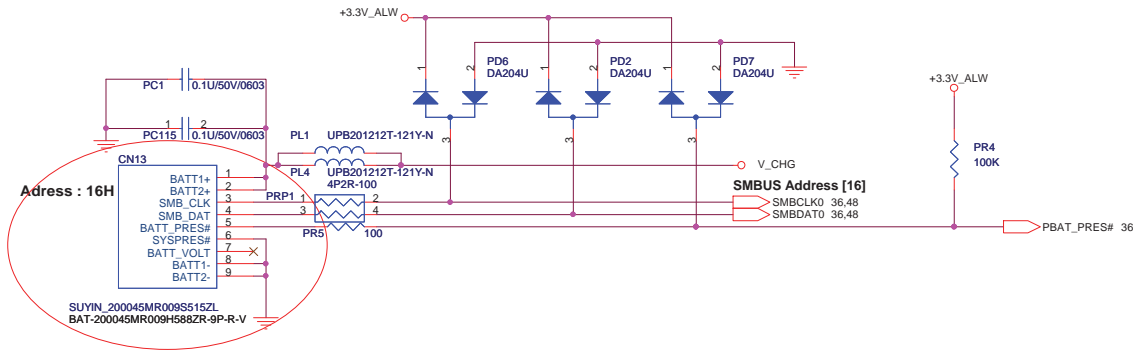
Date: Tuesday, October 26, 2008 Sheet 53 of 59

+1.05V\_VCCP

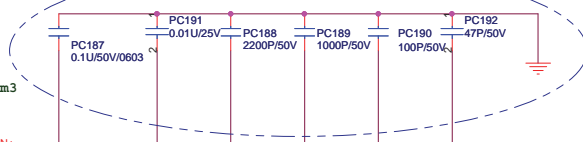
08/27 : Remove 0 ohm (PR79)



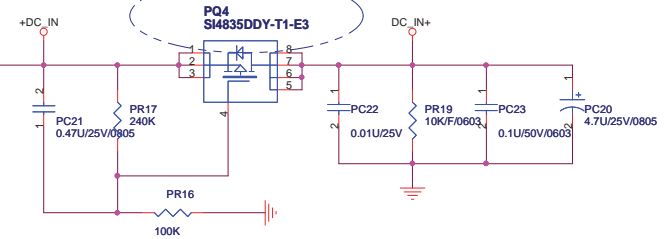
TON	PR185=237K
Frequency	300K



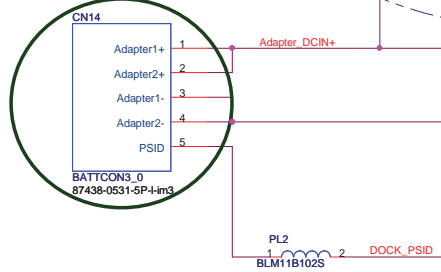
0311-Rick: Add PC187~PC192 for EMC

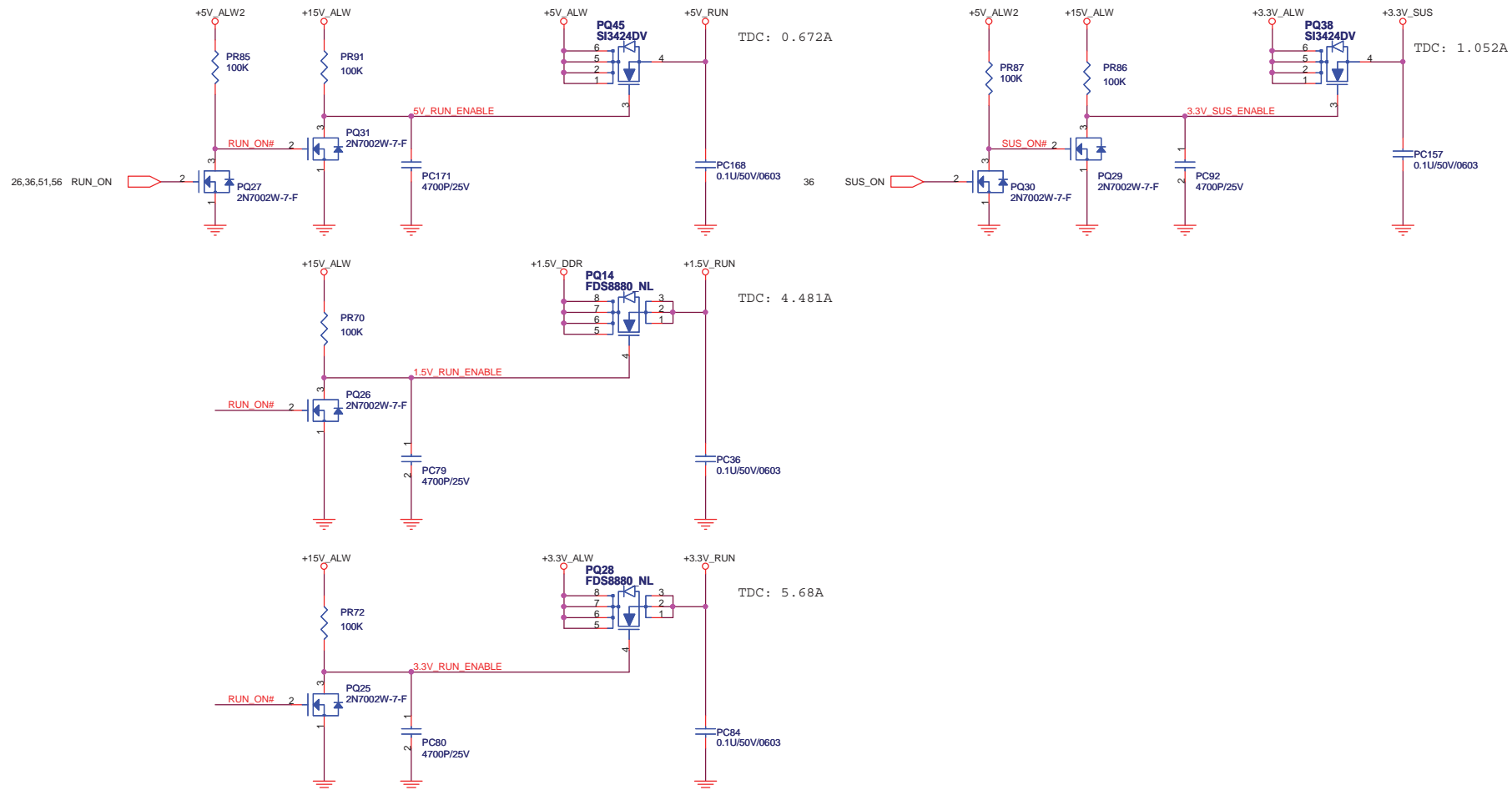


0709-Rick: Change PQ4 Value

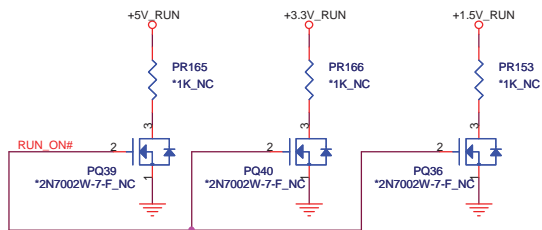


0823 Michael: Change Footprint from 87438-0531-5p-L to 87438-0531-5p-1-im3

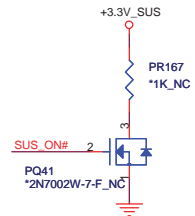




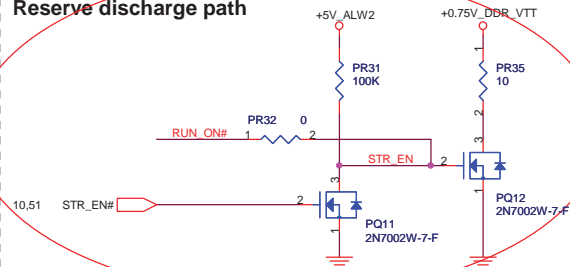
### Reserve discharge path



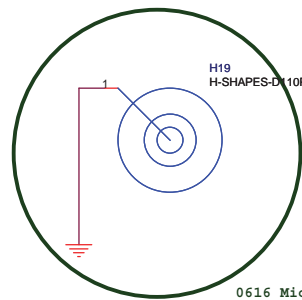
### Reserve discharge path



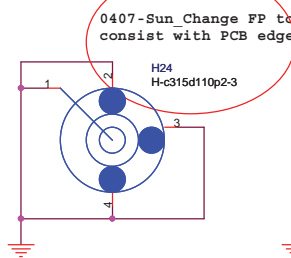
### Reserve discharge path



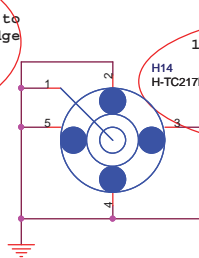
Title			RUN POWER SW
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Tuesday, September 09, 2008	Sheet	56 of 59



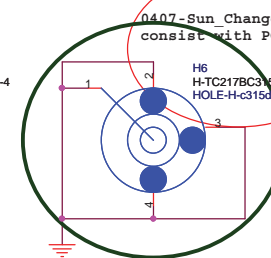
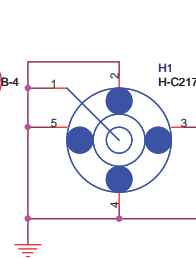
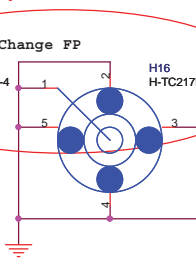
0616\_Michael:Change footprint



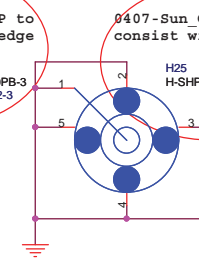
0407-Sun\_Change FP to consist with PCB edge



1123-Sun\_Change FP



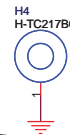
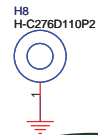
0616\_Michael:Change footprint



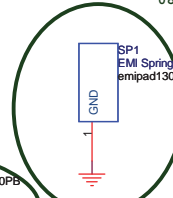
0407-Sun\_Change FP to consist with PCB edge



1123-Sun\_Change FP

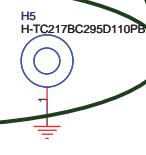
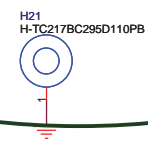
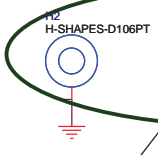
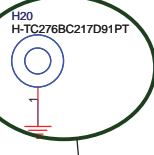
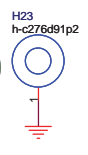
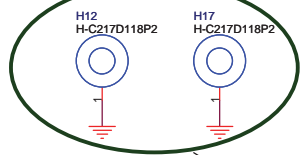


0829\_Michael:Remove H3



0411-Sun\_Add SP1

0605\_Michael: Add connect to GND



0616\_Michael:Change footprint