


Thurman Discrete VGA nVidia G86 Schematics Document

uFCPGA Mobile Merom

Intel Crestline-PM + ICH8M

2007-11-06

REV : -1(DELL:A00)

<Variant Name>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thurman Discrete			
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Thurman Discrete Block Diagram

Project code: 91.4C301.001
PCB P/N : 06247
REVISION : -1

System DC/DC TPS51120		45
INPUTS	OUTPUTS	
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO	
System DC/DC TPS51124		46
+PWR_SRC	+1.05V_VCCP +1.5V_RUN	
DDR2 DC/DC TPS51117		47
+PWR_SRC	+1.8V_SUS	
LDO TPS51100		47
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF	
VGA DC/DC TPS51117		48
+PWR_SRC	VGA_CORE	

Battery Charger MAX8731		42
INPUTS	OUTPUTS	
+PWR_SRC	+VCHGR	

CPU DC/DC ISL6260C		43, 44
INPUTS	OUTPUTS	
+PWR_SRC	+VCC_CORE	

PCB LAYER	
L1: TOP	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Signal	
L7: GND	
L8: BOT	

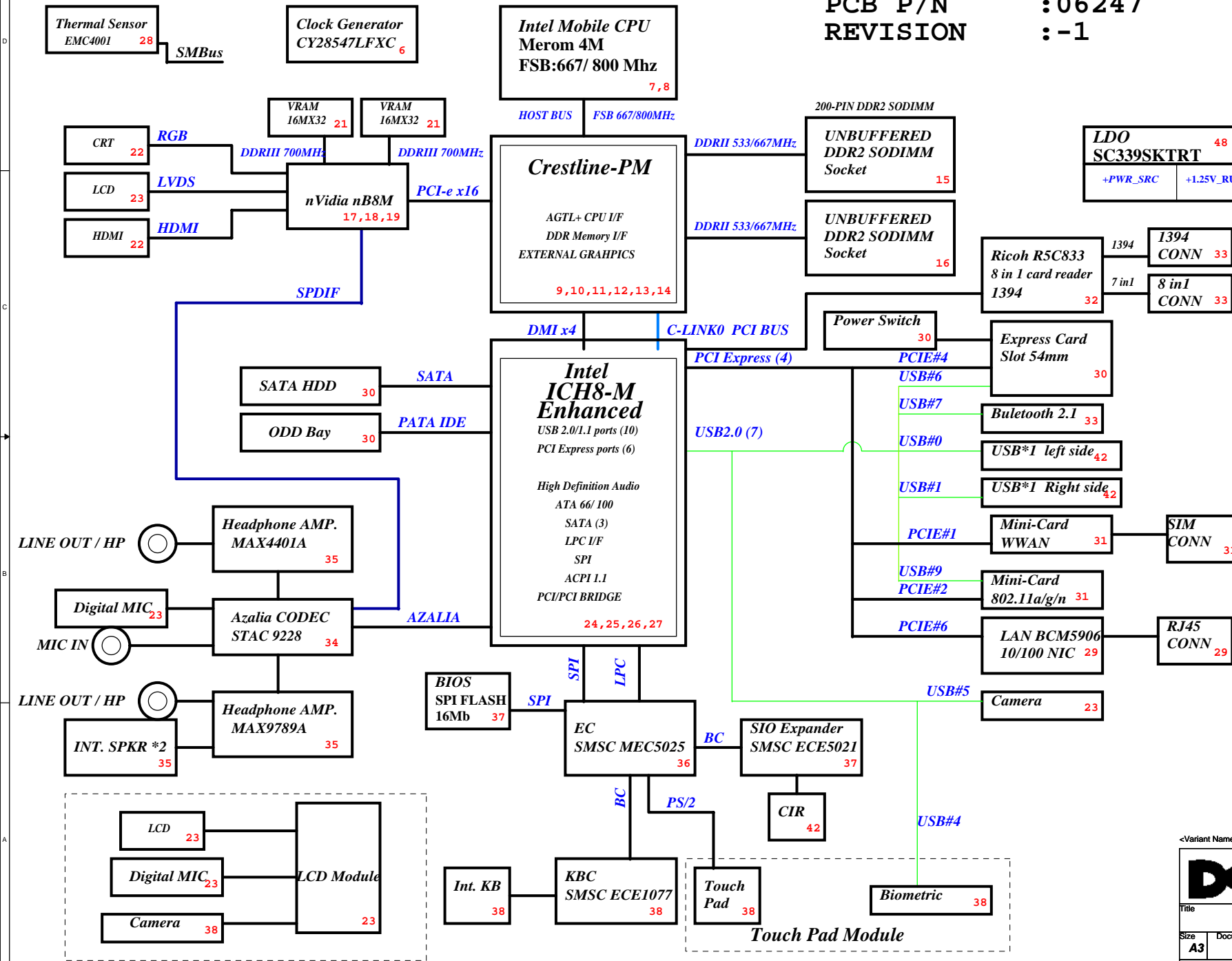
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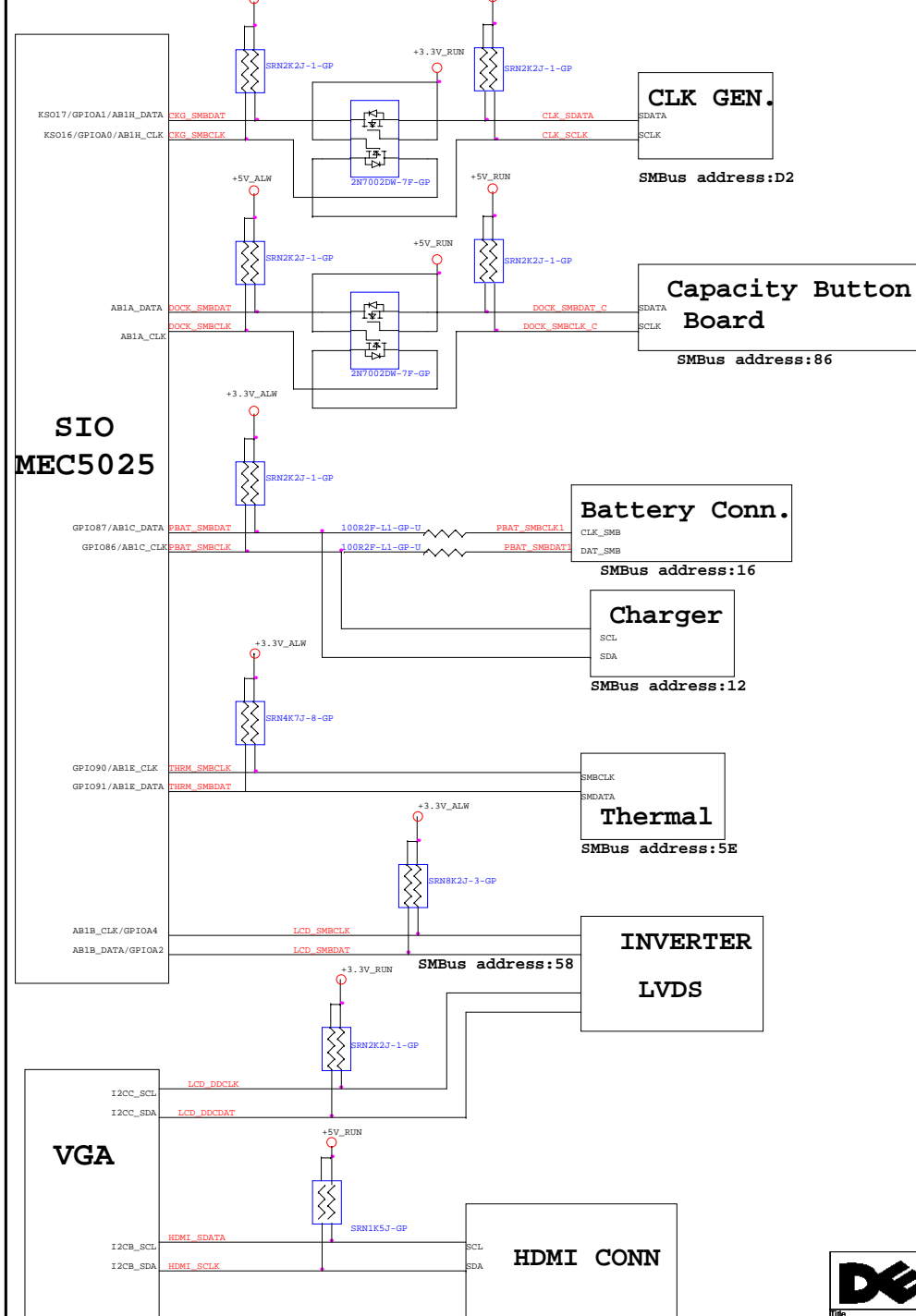
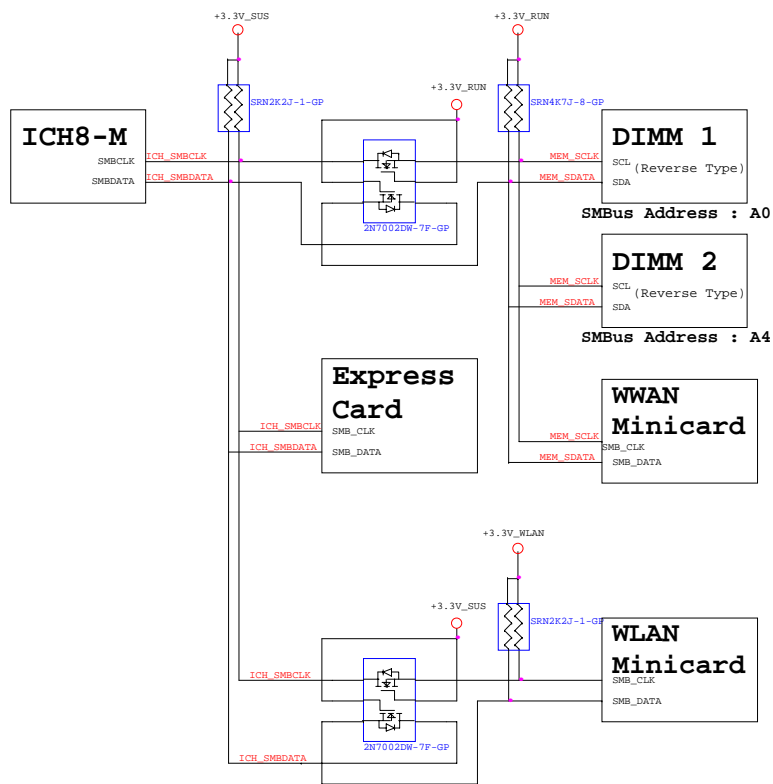
Title

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ICH8 SMBus Block Diagram



CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 15
IO_VOUT[2,1,0]

BYTE 10

bits S1	Bit4 S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05 VccSusi_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi_05,VccSusi_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVDtp3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSusi_05,VccSusi_5,VccCL1_5		
SM_INTVRMEN	High=Enable Low=Disable	
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable Low=Disable	

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

INTEL ICH8-M INTEGRATED
PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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Title

Thurman Discrete

Size
A3

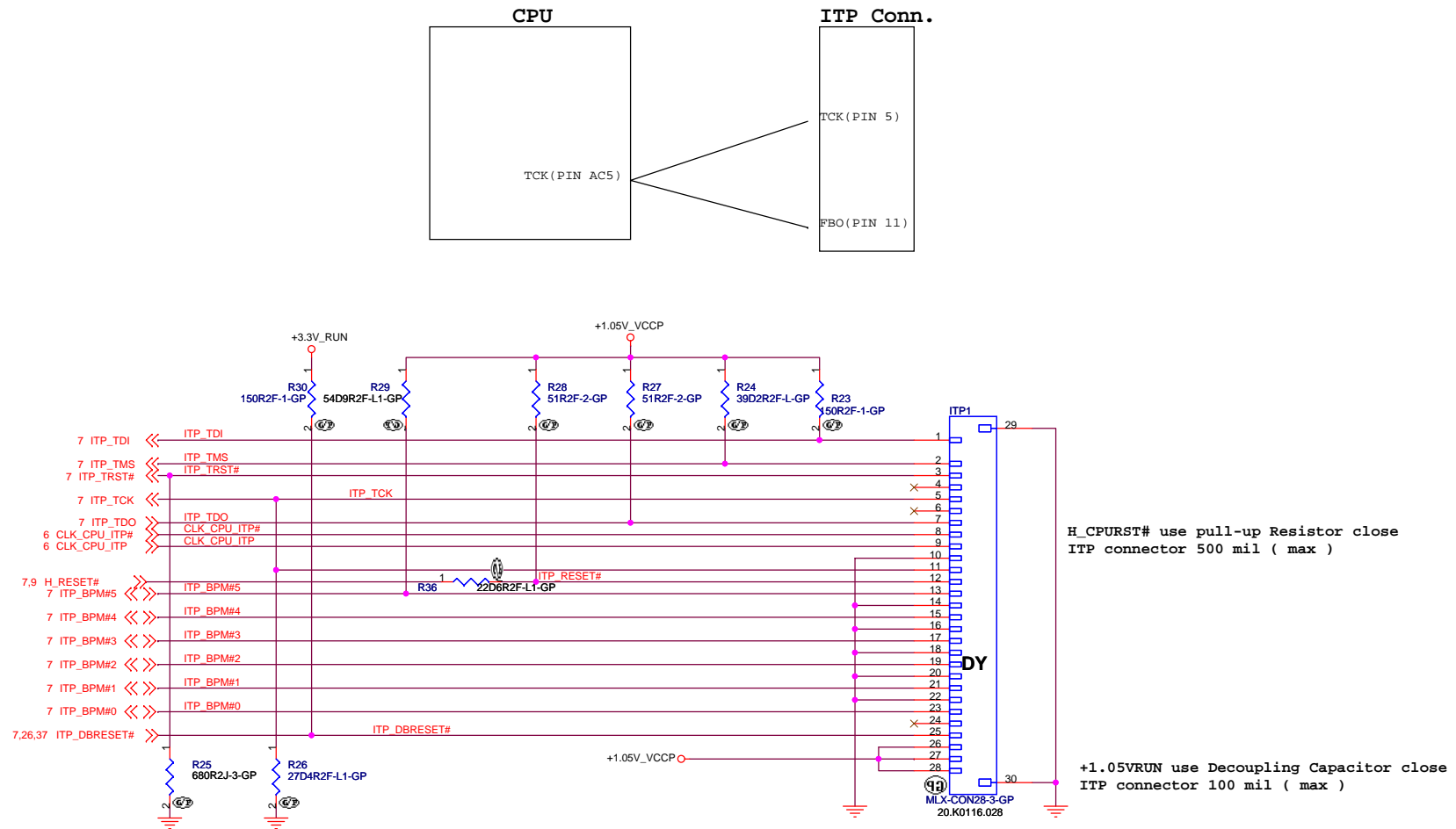
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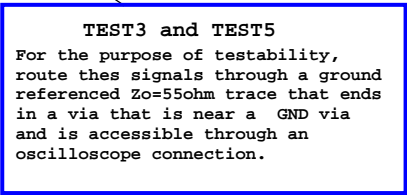
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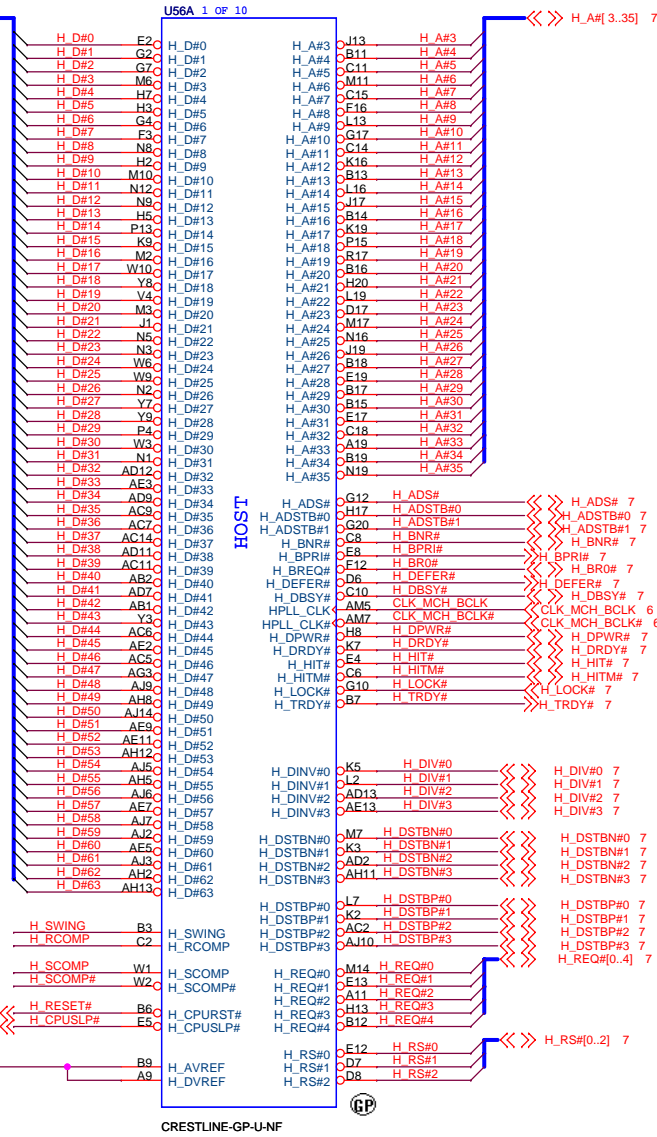
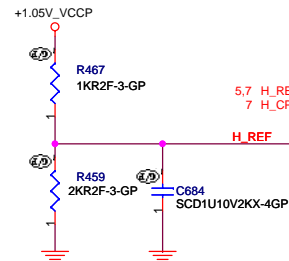
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original value:SKT-CPU478P-GP
```



TEST3 and TEST5

For the purpose of testability,
route the signals through a ground
referenced $Z_0=55\Omega$ trace that ends
in a via that is near a GND via
and is accessible through an
oscilloscope connection.

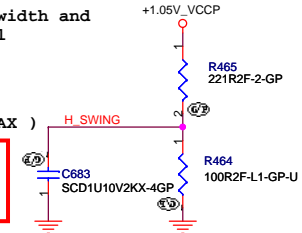
H_REF Decoupling Crestline
close Crestline 100 mil



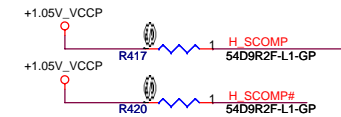
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

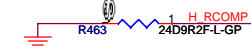
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



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GMCH-FSB LIBC (1/6)

Rev

-1

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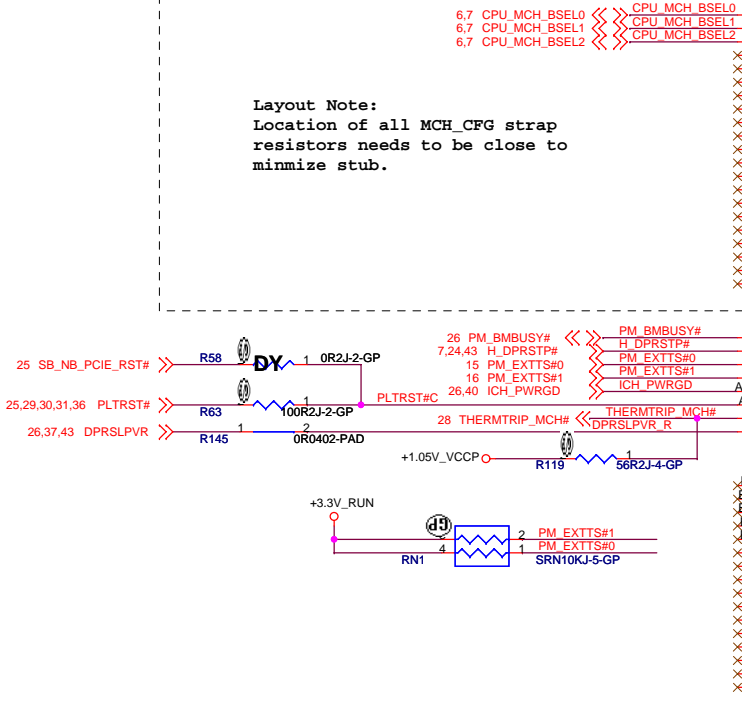
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* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16	Disabled	Enabled *
CFG 18	1.05V *	1.5V
CFG 19	Normal Operation *	Reserved Lane
CFG 20	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

CFG[13:12]	
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
CFG[2..0] FSB Select	
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.



<Variant Name>



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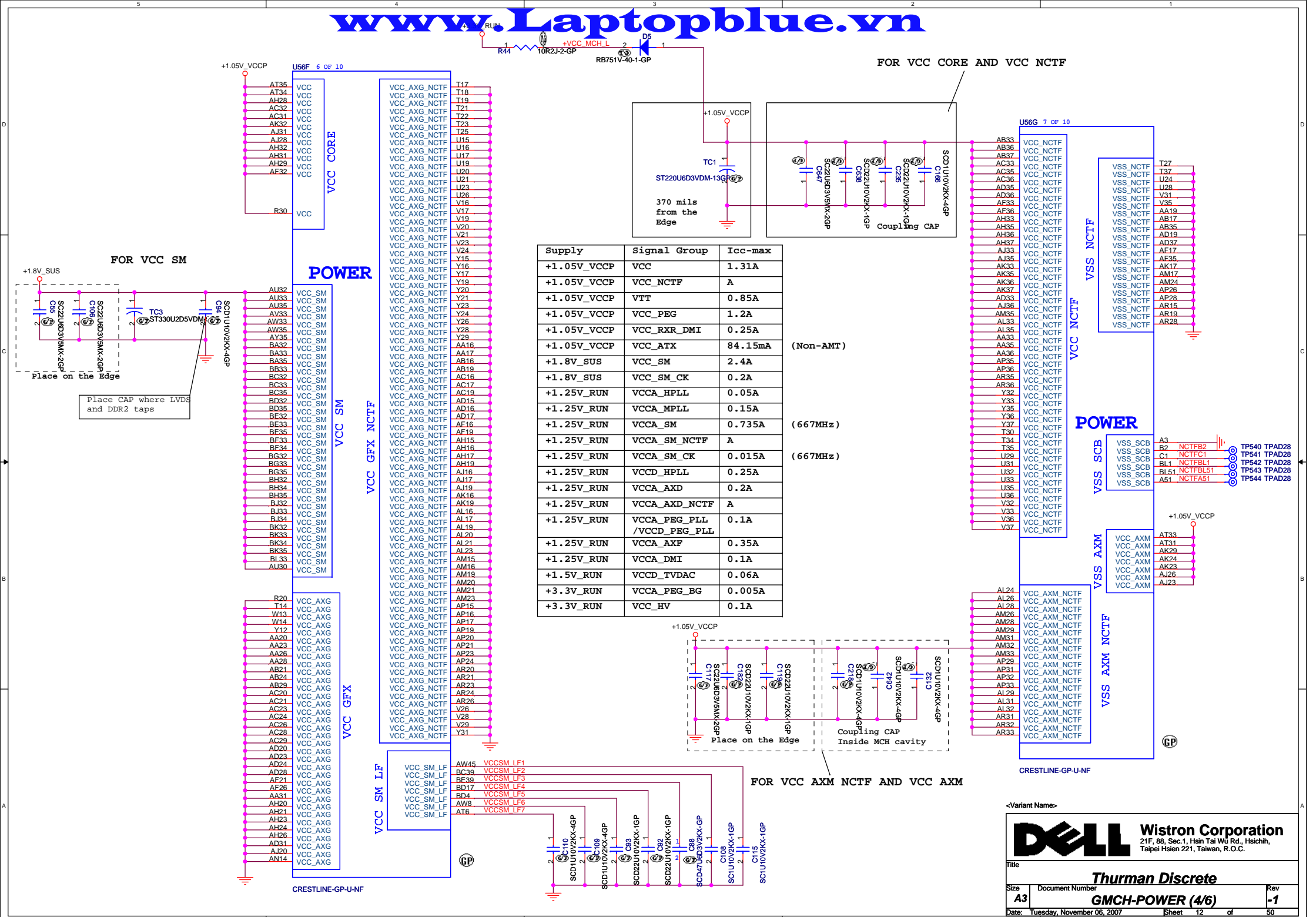
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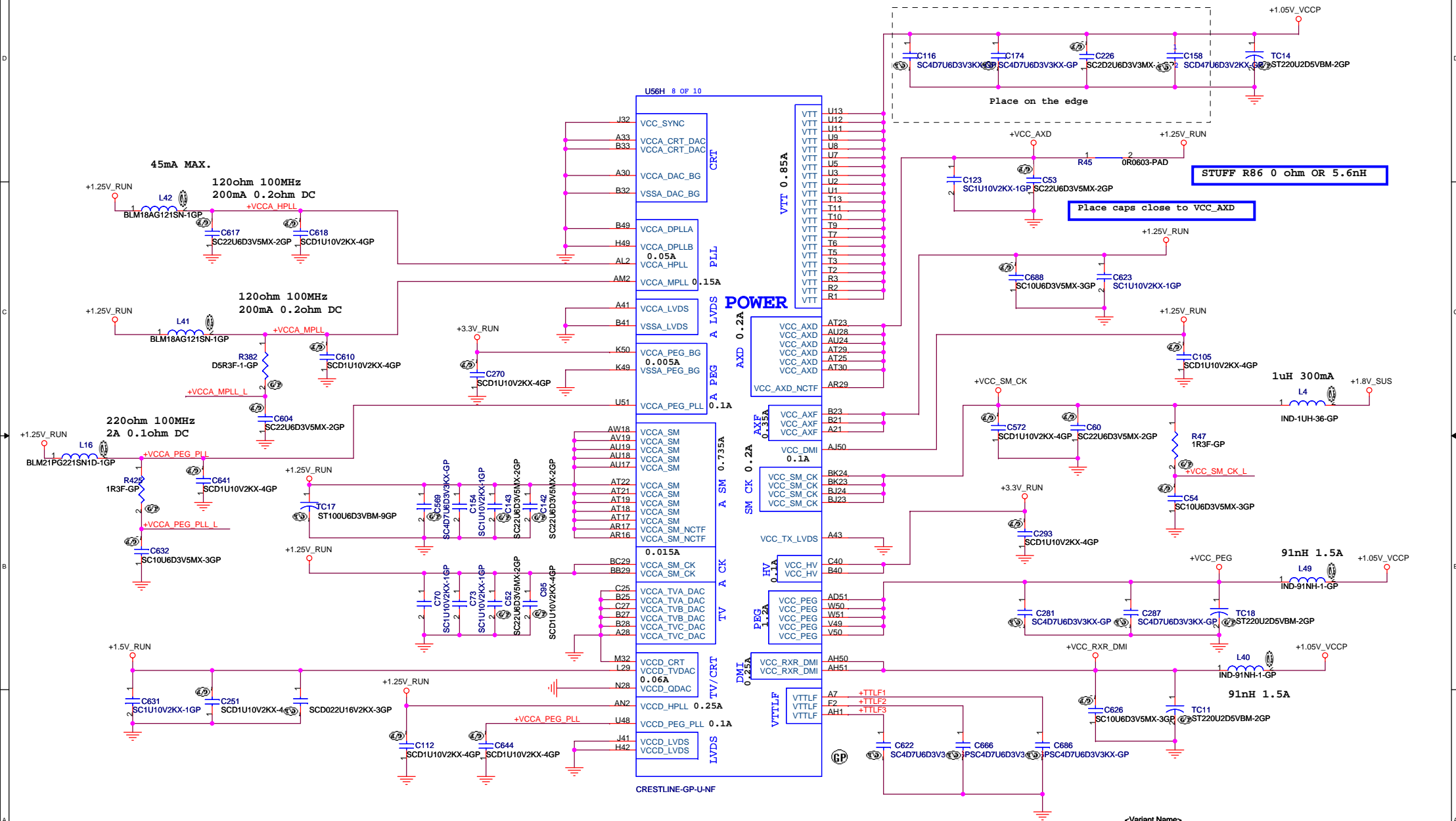
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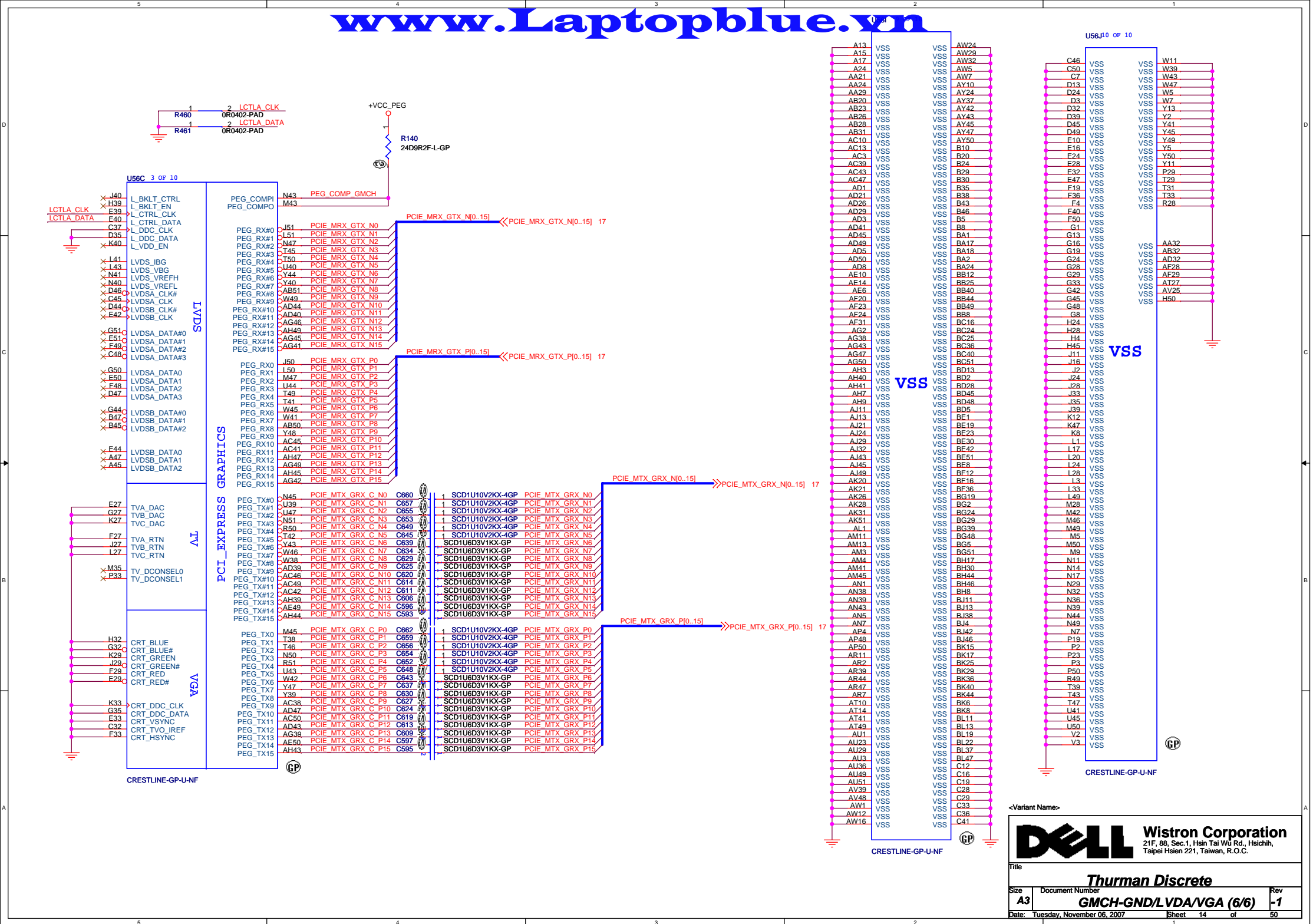
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A3	GMCH-DDR (3/6)	-1
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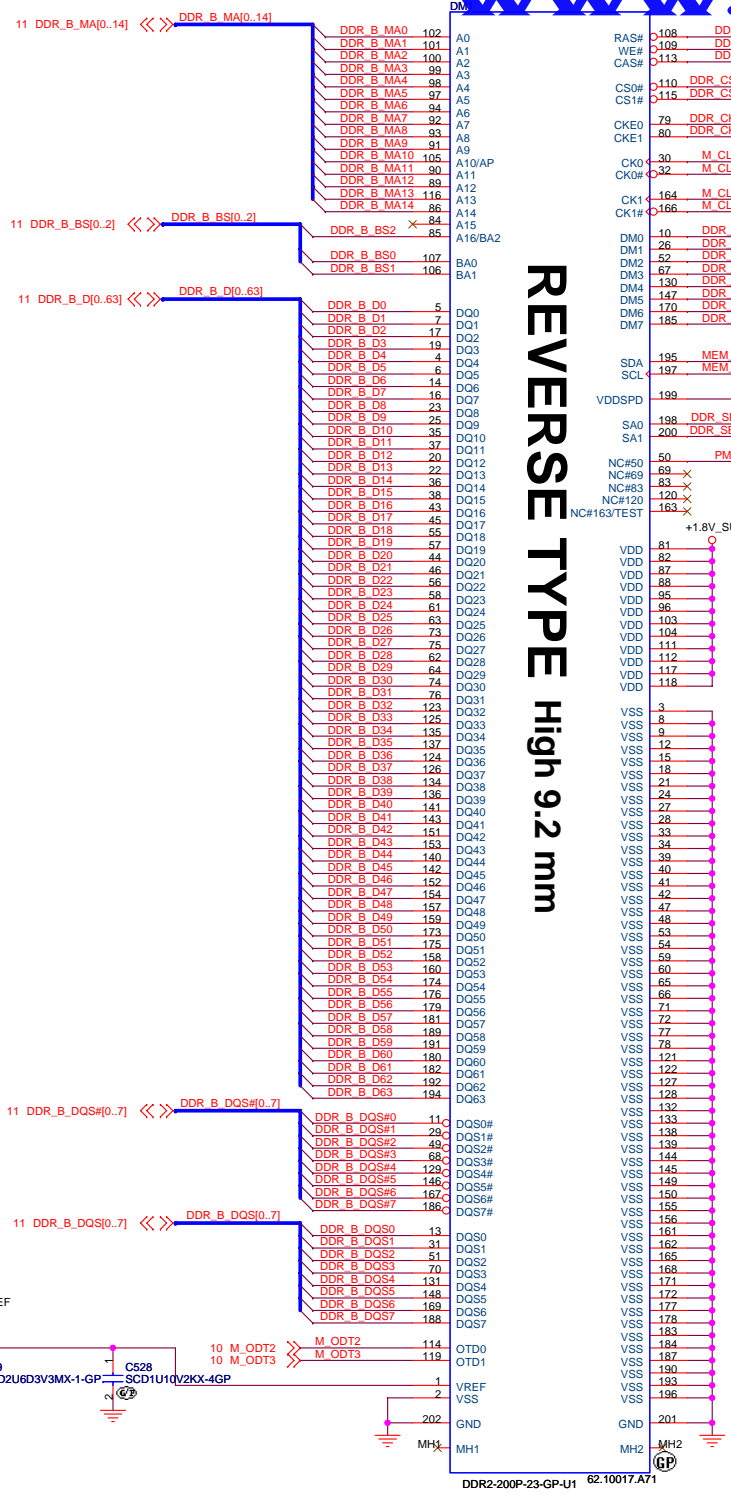
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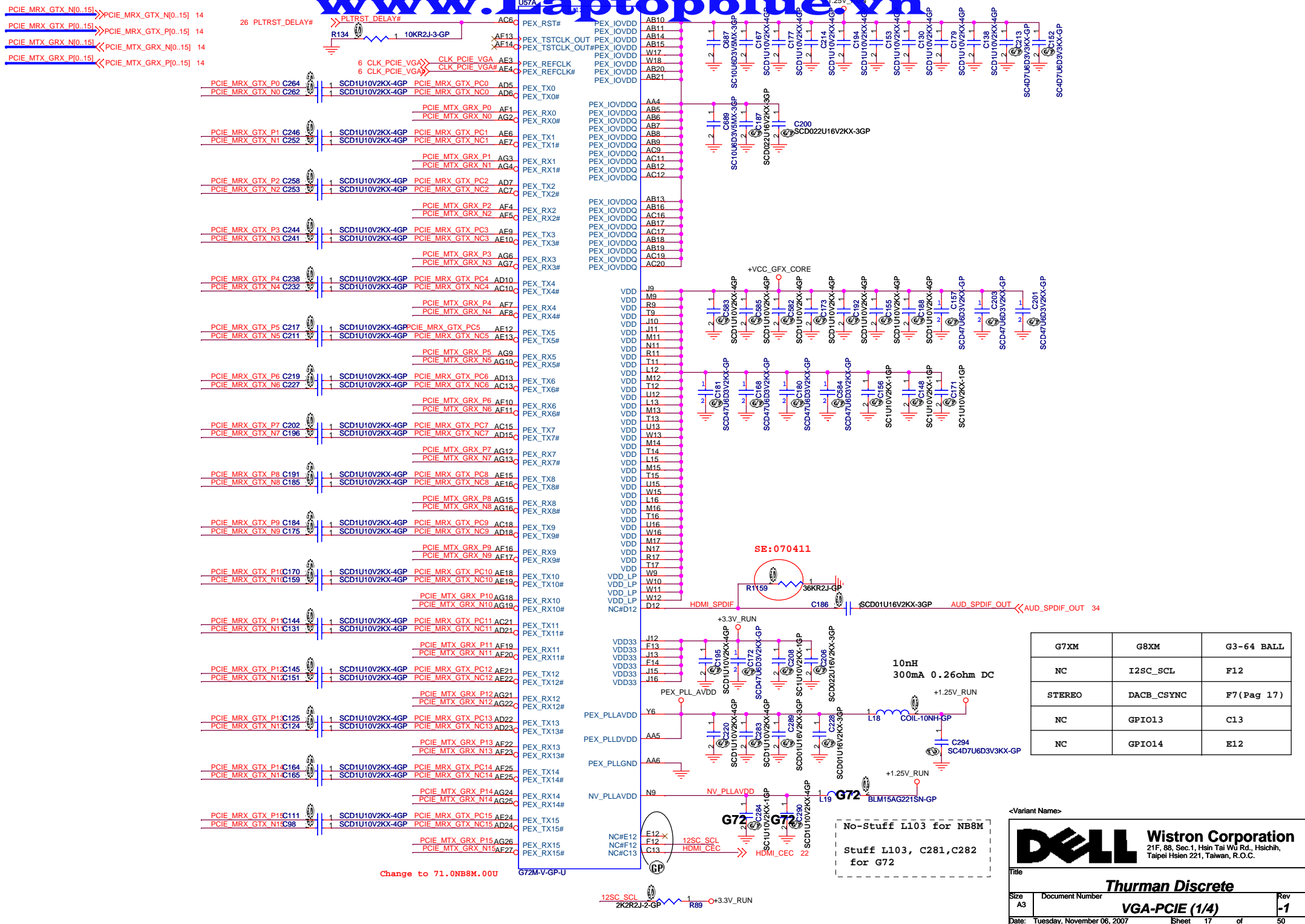






REVERSE TYPE High 9.2 mm





G7XM	G8XM	G3-64 BALL
NC	I2SC_SCL	F12
STEREO	DACB_CS	F7 (Pag 17)
NC	GPI013	C13
NC	GPI014	E12

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VGA-PCIE (1/4)

Rev -1

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No-Stuff L103 for NB8M

Stuff L103, C281, C282 for G72

Change to 71.0NB8M.00U

12SC_SCL 2K2R2J-2-GP 1 R89 +3.3V_RUN

10nH 300mA 0.26ohm DC

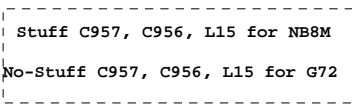
+1.25V_RUN

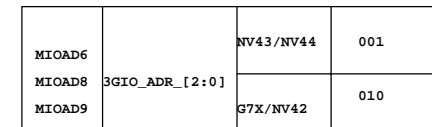
+1.25V_RUN

BLM15AG221SN-GP

G72

HDMI_CEC 22





	G72M	G8XM	DEFAULT	STRAP
MIOBD2	CRYSTALA0	CRYSTALA	0	No require
MIOBD6	CRYSTALA1	TVMODE2	0	No require
MIOB_HSYNC	-	3GIO_PADFG3	0	No require
MIOBD7	MIOBLE_FPIO	PCI_IOBAR	1	No require
MIOB_DE	-	BAR2_SIZE	0	No require

STRAPS	PIN	DESCRIPTION	Value
ROMTYPE [1:0]	MIOBD10 MIO_VSYNC	*	01
SUB_VENDOR	MIOAD1		0
PEX_PLL_TERM	MIOAD0		0

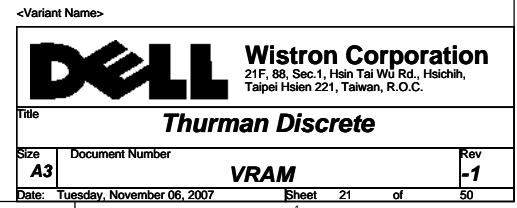
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Parallel=00, SERIAL AT25F=01
*   DEFAULT,Serial SST45VF=10,
    LPC=11
<Variant Name>

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Setting R,G,B trace impedance to 50 ohm.

VGA conn.

20 VGA_RED
20 VGA_GRN
20 VGA_BLU

20 G_DAT_DDC2
20 G_CLK_DDC2

100ohm 100MHz
500mA 0.25ohm DC

120ohm 100MHz
200mA 0.2ohm DC

CRT conn.

CRT1

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
JVGA_HS
JVGA_VS
VIDEO-15-54-GP
20.20410.015

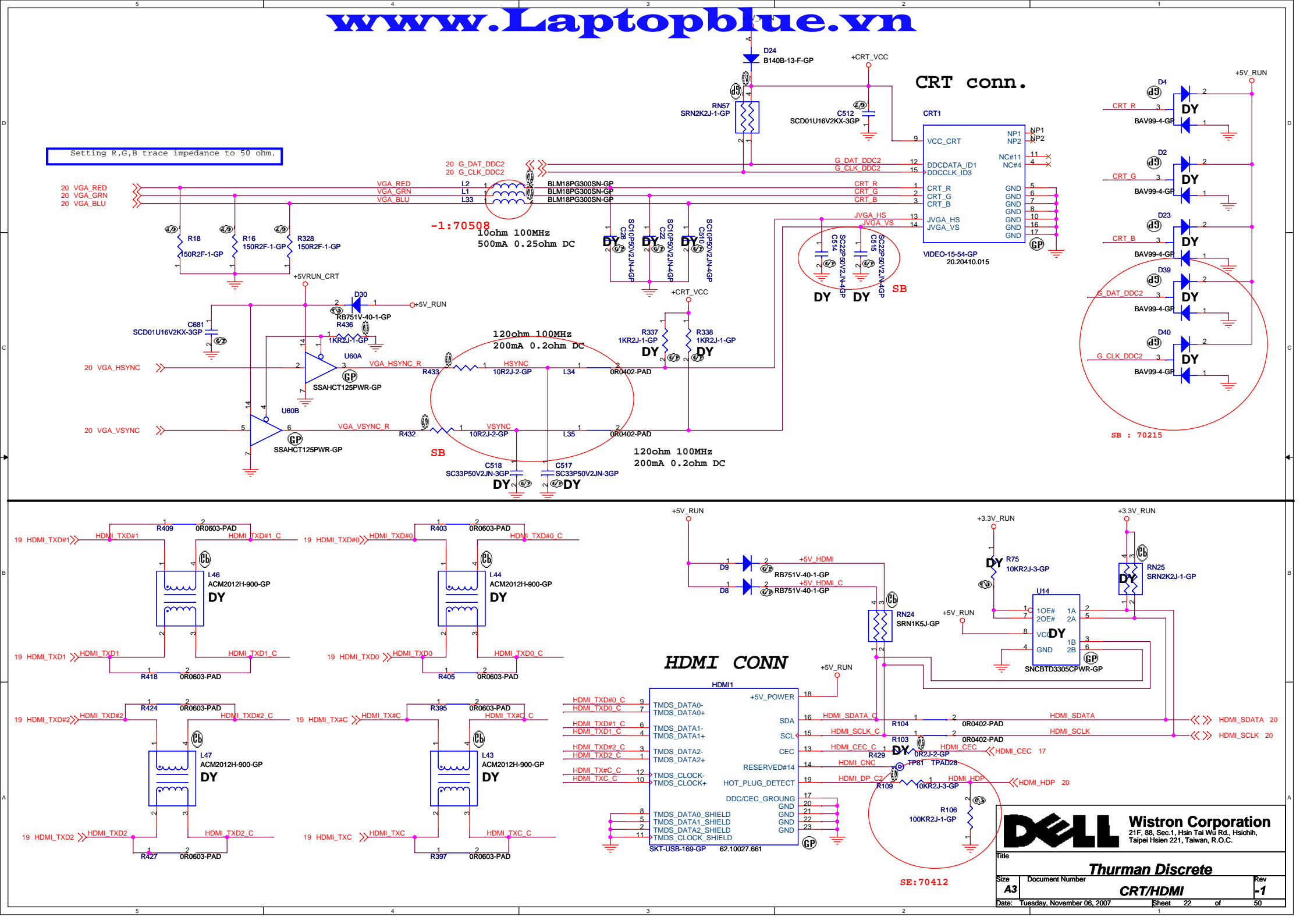
HDMI conn

HDMI1

HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC

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Setting R,G,B trace impedance to 50 ohm.

CRT conn.

HDMI CONN

SE: 70412

SB : 70215

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Thurman Discrete
CRT/HDMI

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Setting R,G,B trace impedance to 50 ohm.

CRT conn.

HDMI CONN

SE: 70412

SB : 70215

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CRT/HDMI

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Setting R,G,B trace impedance to 50 ohm.

VGA conn.

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20 G_DAT_DDC2
20 G_CLK_DDC2

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500mA 0.25ohm DC

120ohm 100MHz
200mA 0.2ohm DC

CRT conn.

CRT1

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
JVGA_HS
JVGA_VS
VIDEO-15-54-GP
20.20410.015

HDMI conn

HDMI1

HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC

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Setting R,G,B trace impedance to 50 ohm.

VGA conn.

20 VGA_RED
20 VGA_GRN
20 VGA_BLU

20 G_DAT_DDC2
20 G_CLK_DDC2

100ohm 100MHz
500mA 0.25ohm DC

120ohm 100MHz
200mA 0.2ohm DC

CRT conn.

CRT1

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
JVGA_HS
JVGA_VS
VIDEO-15-54-GP
20.20410.015

HDMI conn

HDMI1

HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC

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CRT/HDMI

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Setting R,G,B trace impedance to 50 ohm.

VGA conn.

20 VGA_RED
20 VGA_GRN
20 VGA_BLU

20 G_DAT_DDC2
20 G_CLK_DDC2

100ohm 100MHz
500mA 0.25ohm DC

120ohm 100MHz
200mA 0.2ohm DC

CRT conn.

CRT1

VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
JVGA_HS
JVGA_VS
VIDEO-15-54-GP
20.20410.015

HDMI conn

HDMI1

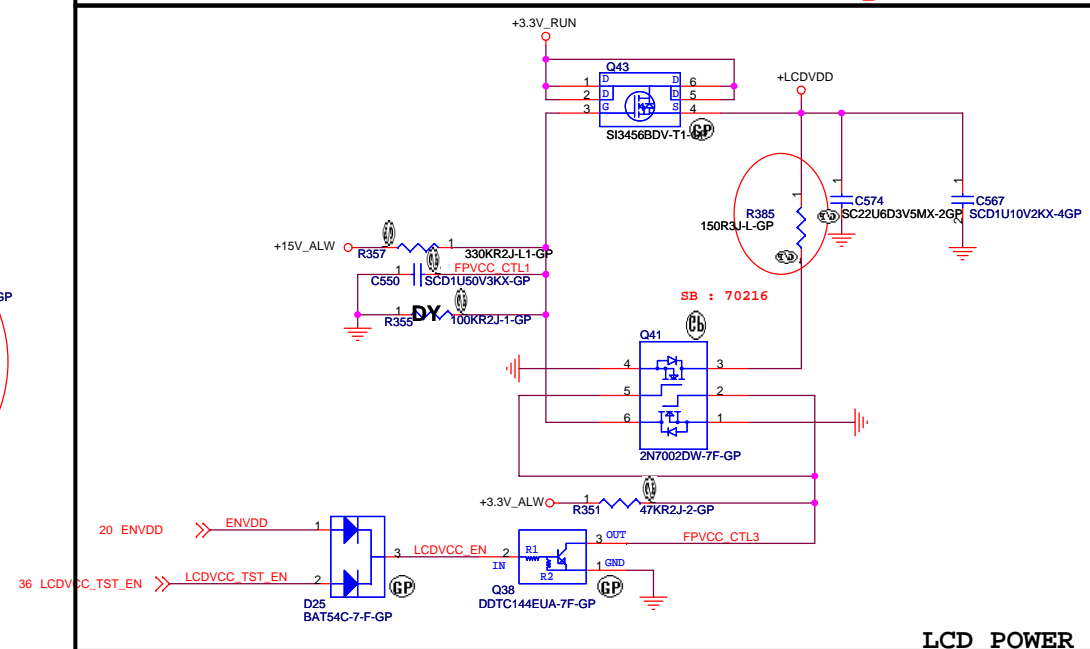
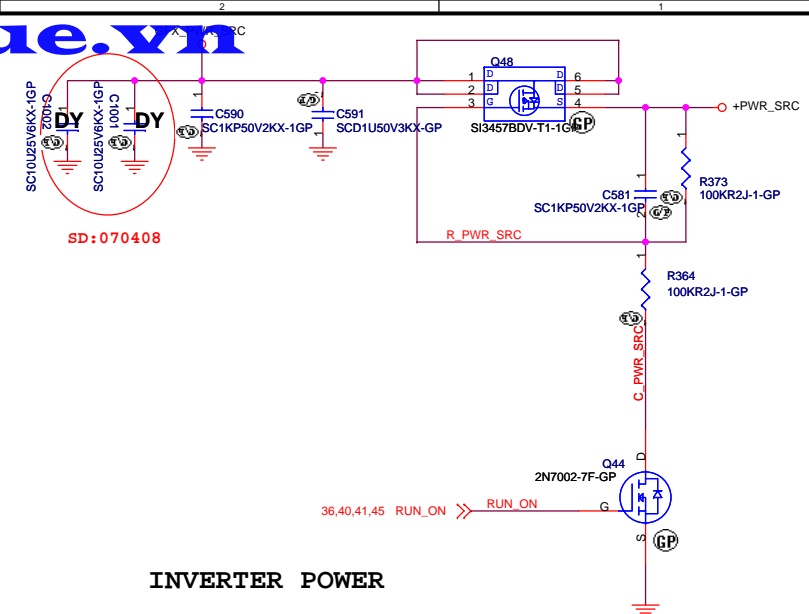
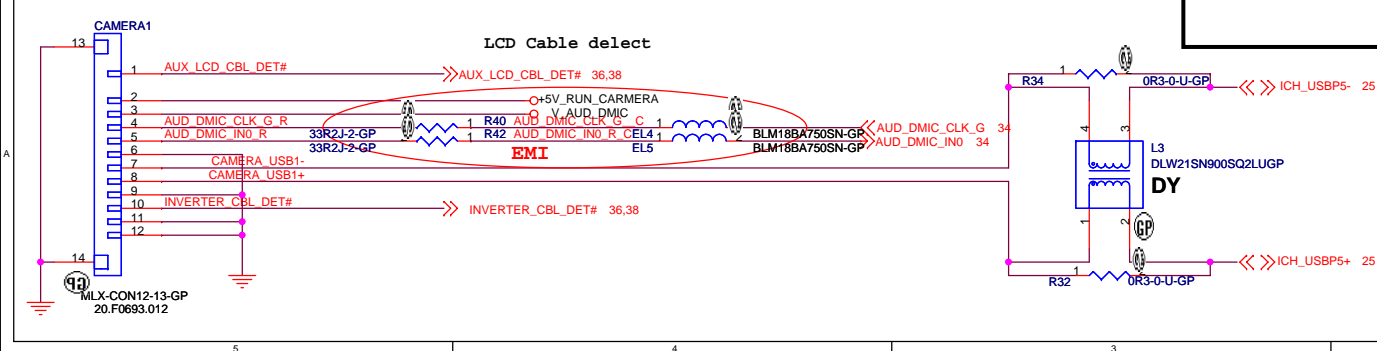
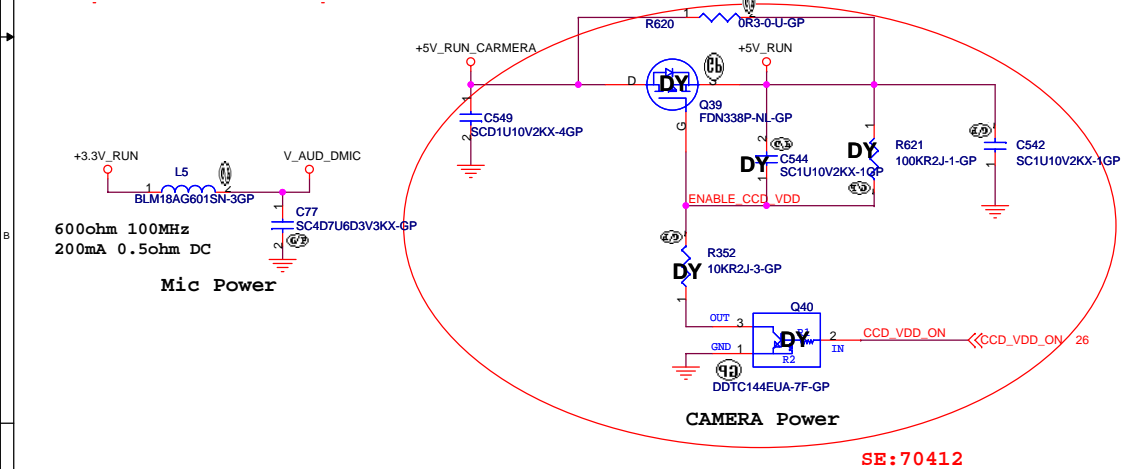
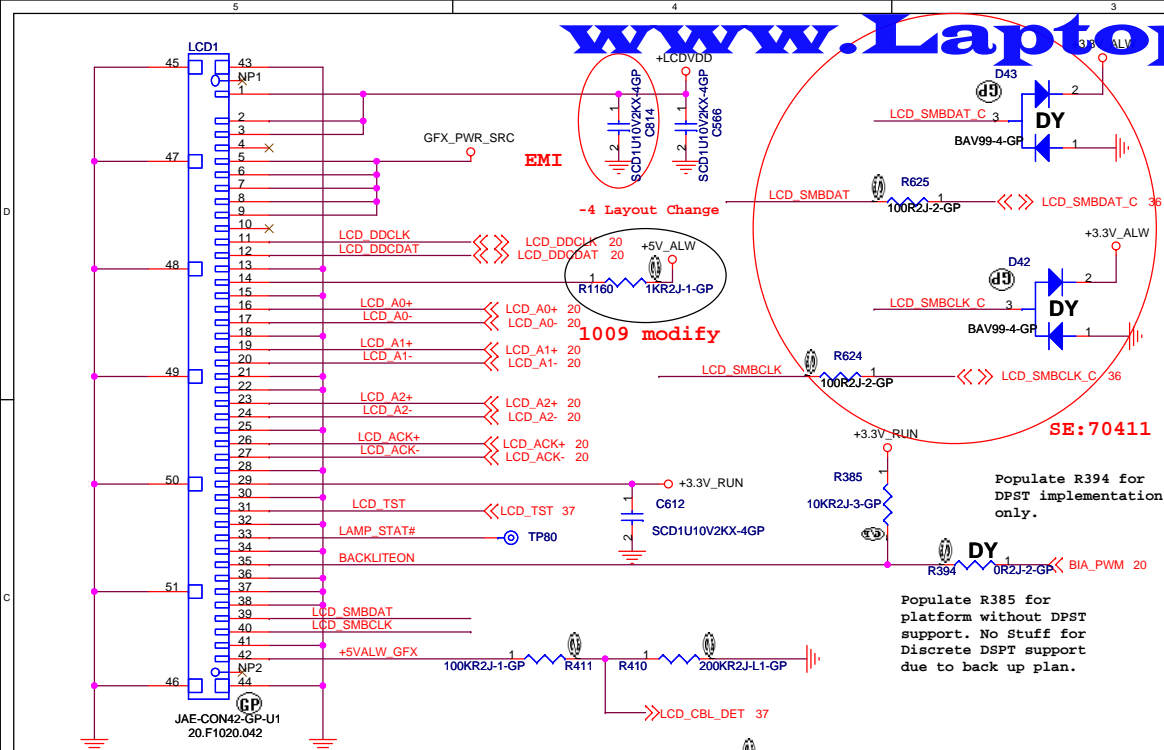
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC
HDMI_TXD#0_C
HDMI_TXD0_C
HDMI_TXD#1_C
HDMI_TXD1_C
HDMI_TXD#2_C
HDMI_TXD2_C
HDMI_TX#C
HDMI_TXC

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

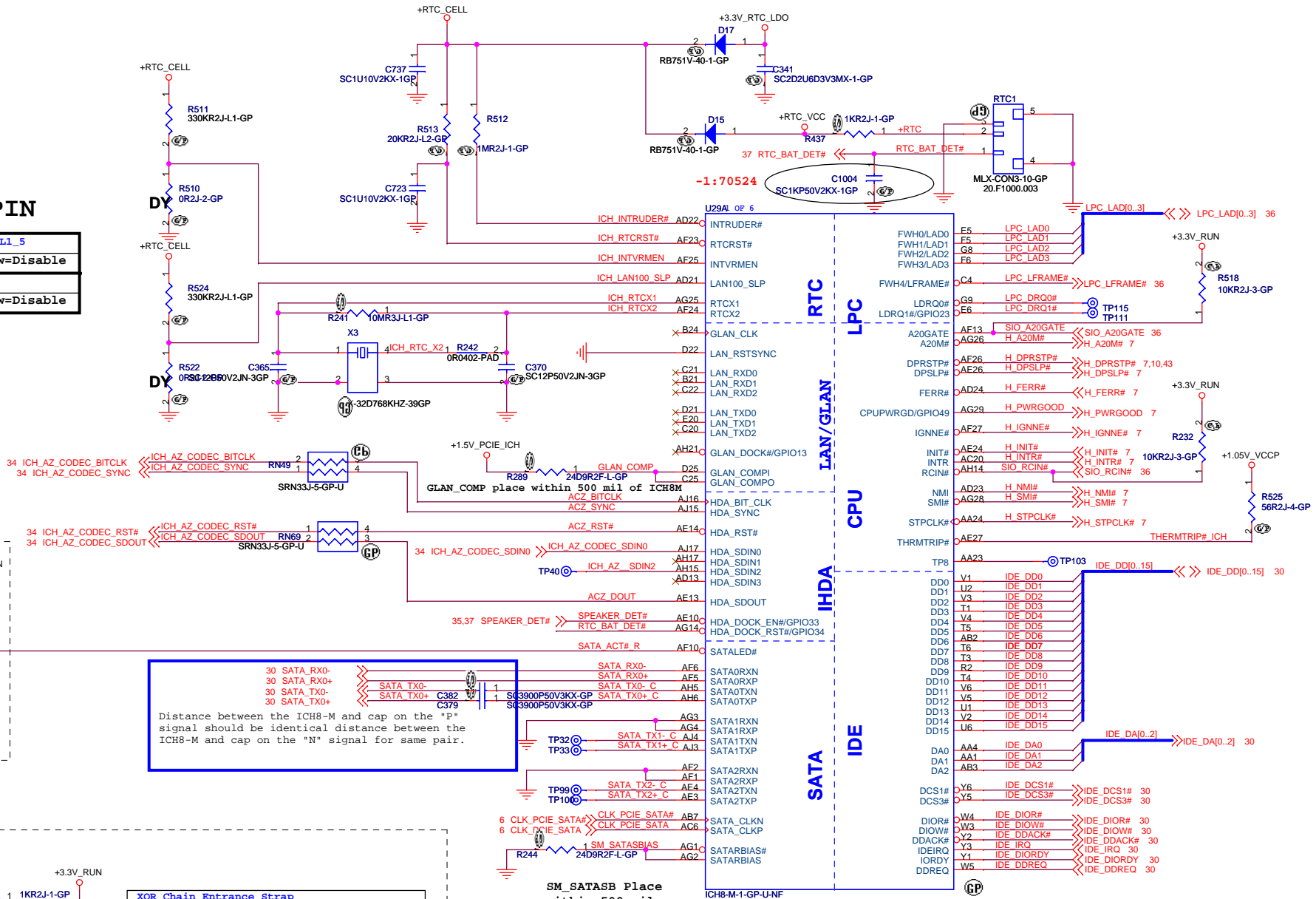
Thurman Discrete
CRT/HDMI

Size A3 Document Number Rev -1
Date: Tuesday, November 06, 2007 Sheet 22 of 50

[illegible]



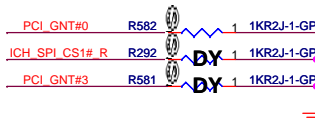
Sheet 24 of 50



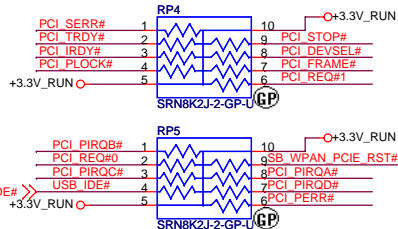
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

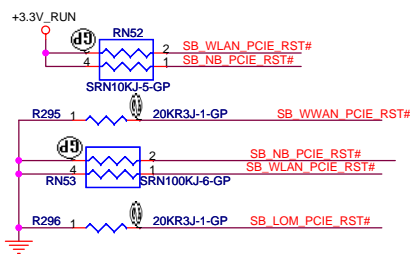
Al6 swap override strap	
PCI_GNT#3 (R168)	low = Al6 swap override enable high = default



PCI I/F PULL HIGH

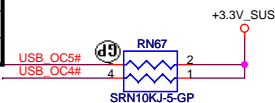


BIOS should not enable the internal GPIO pull up

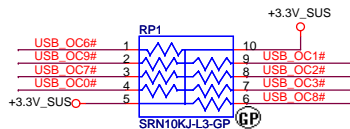


PCIe Interface Routing

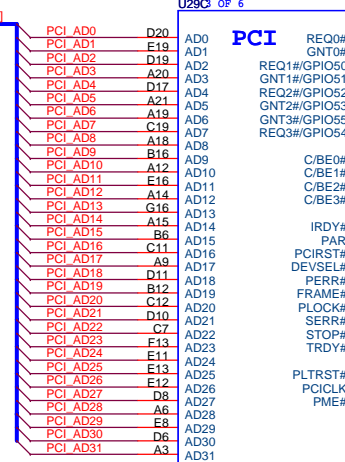
LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN



Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

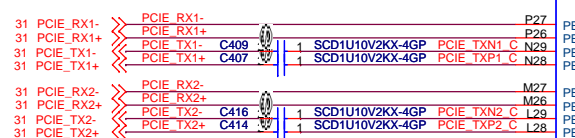


32 PCI_AD[0..31] <<>> PCI_AD[0..31]

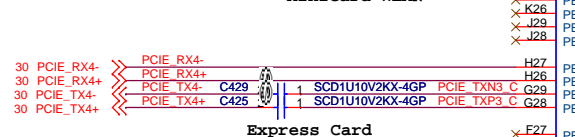


Interrupt I/F
ICH8-M-1-GP-U-NF

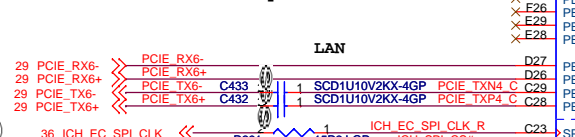
MiniCard WWAN



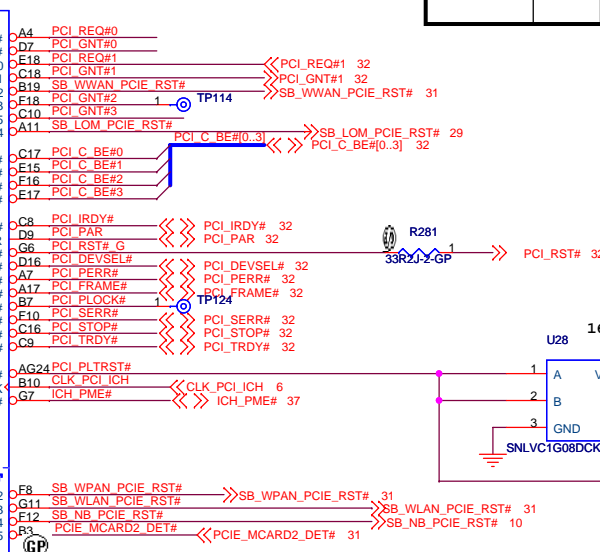
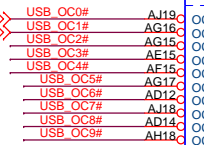
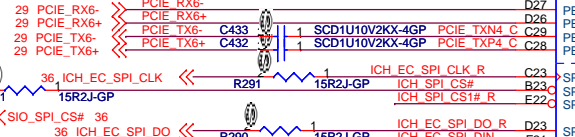
MiniCard WLAN



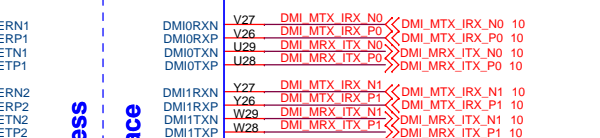
Express Card



LAN



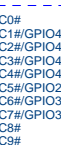
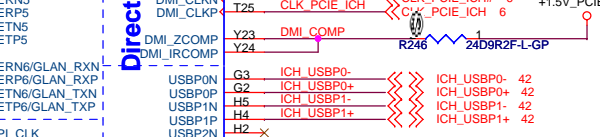
MiniCard WLAN



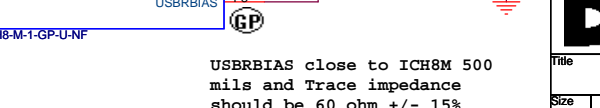
Express Card



LAN



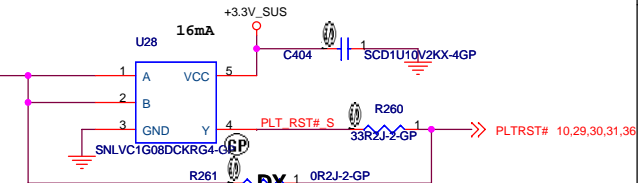
USB



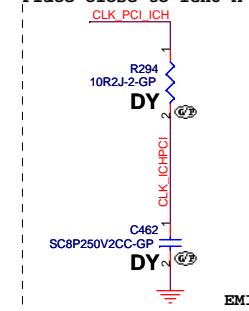
	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

PCI Interface Routing

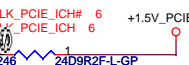
Add Buffers as need for Loading and Fanout concerns



CLK_ICH_14M EMI Mode
Place close to ICH8-M



DMICOMP R158 place within 500 mil of ICH8M



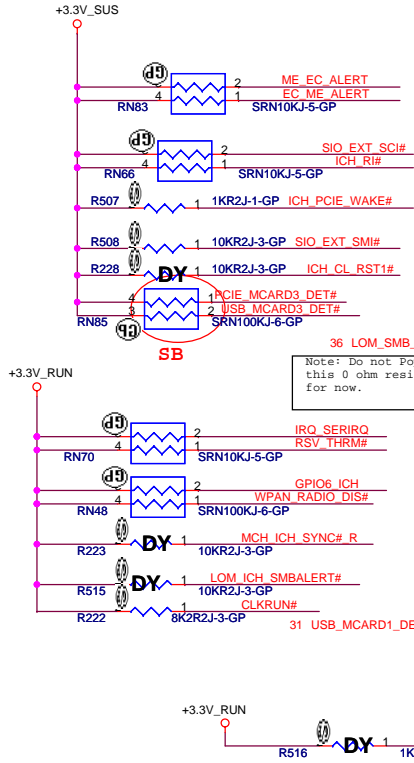
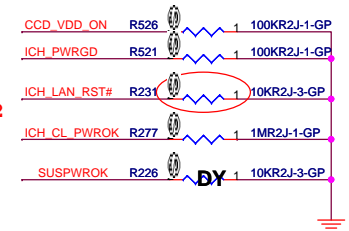
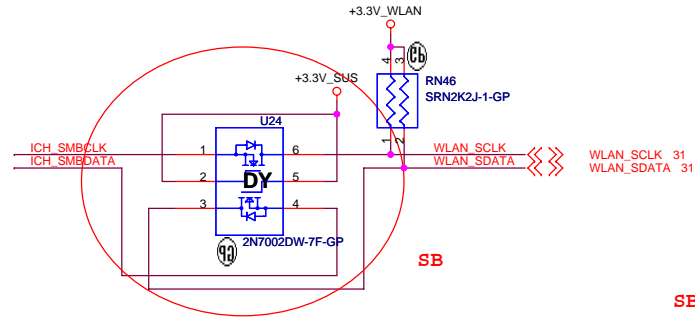
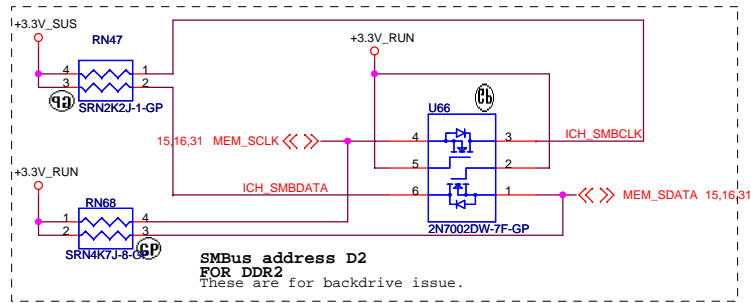
USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

<Variant Name>



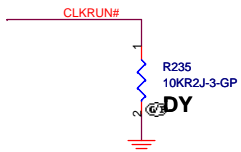
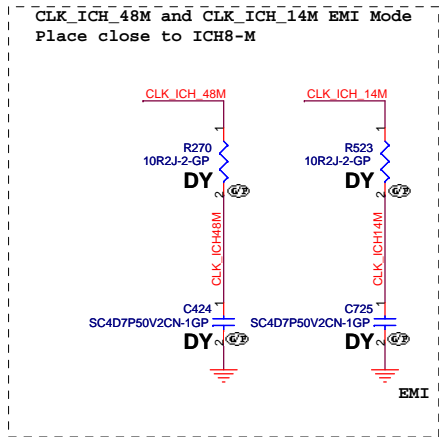
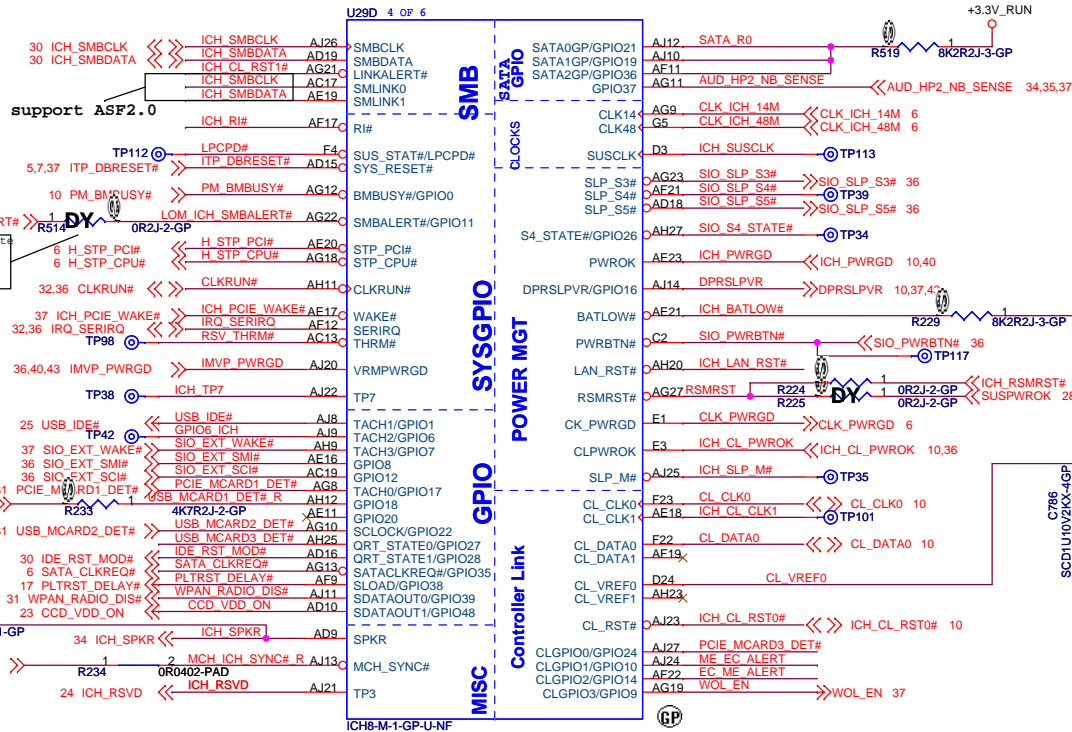
Thurman Discrete		
Size	Document Number	Rev
A3	ICH8M-PCIE/USB/SPI/DMI (2/4)	-1
Date:	Thursday, November 22, 2007	Sheet 25 of 50

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%



ICH8-Strap PIN

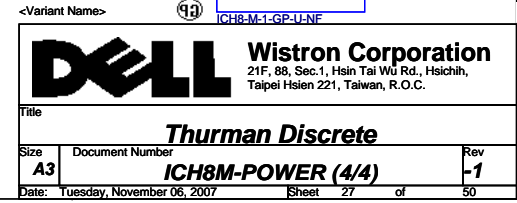
No Reboot Strap	
ICH_SPKR	LOW = Defaule
	High=No Reboot



<Variant Name>

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Size	Document Number	Rev
A3	ICH8M-CL/PM/GPIO (3/4)	-1
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SSID = THERMAL

C451 Please Close to Guardian

Place near the bottom SODIMM CONN

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

Place inside CPU socket

C455 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

REM_DIODE4_N and REM_DIODE4_P
routing Trace width and Spacing
use 10 / 10 mil

Thermal sensor for Mini Card
should be placed TOP Side under WWAN CARD

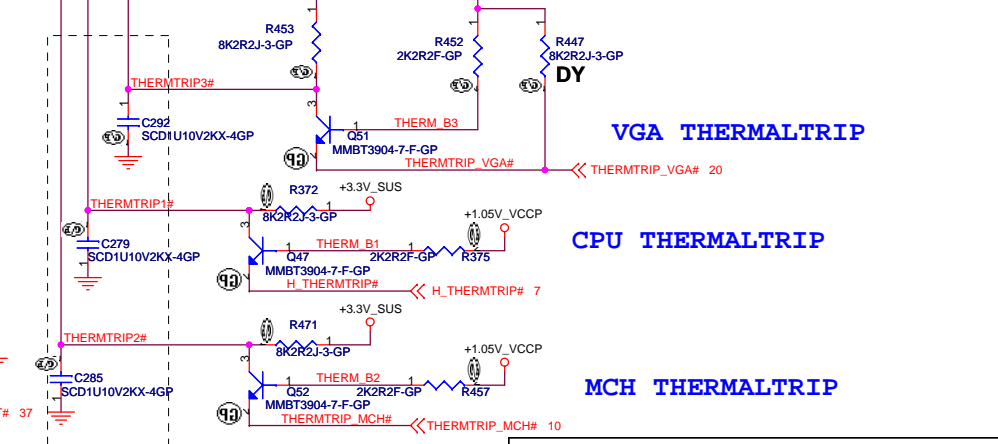
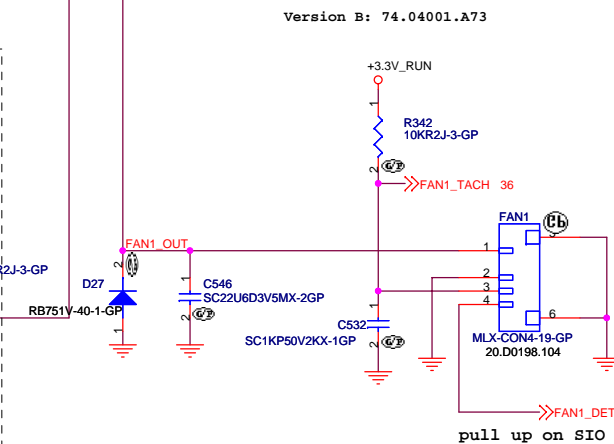
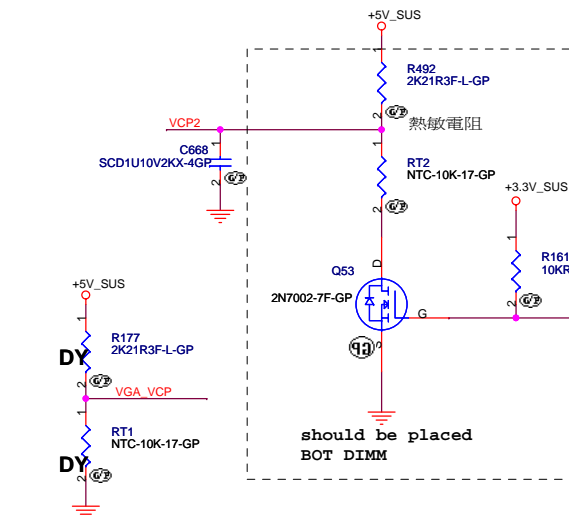
C459 Please Close to Guardian

Thermal sensor for VGA

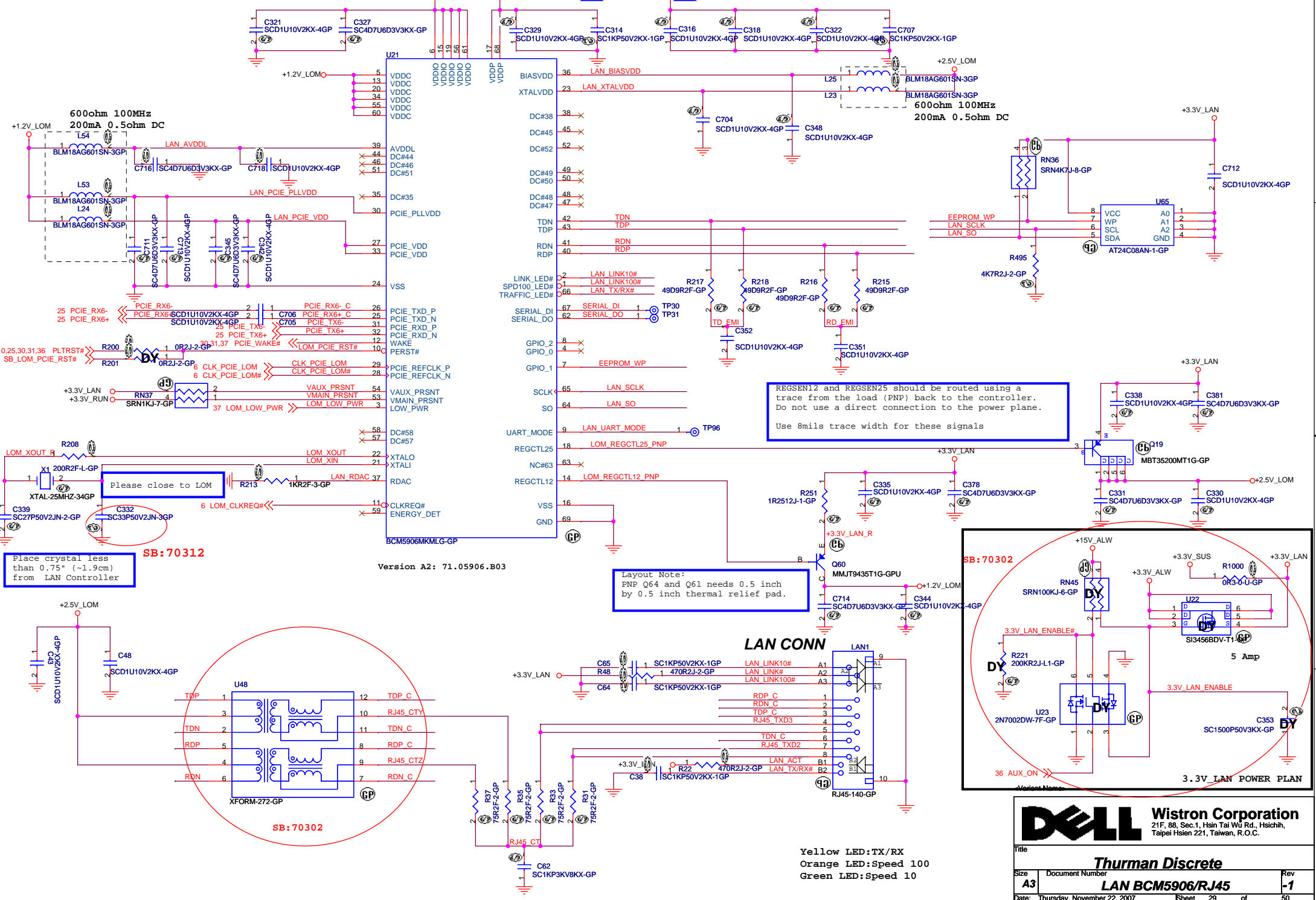
C453 Please Close to Guardian

Version B: 74.04001.A73

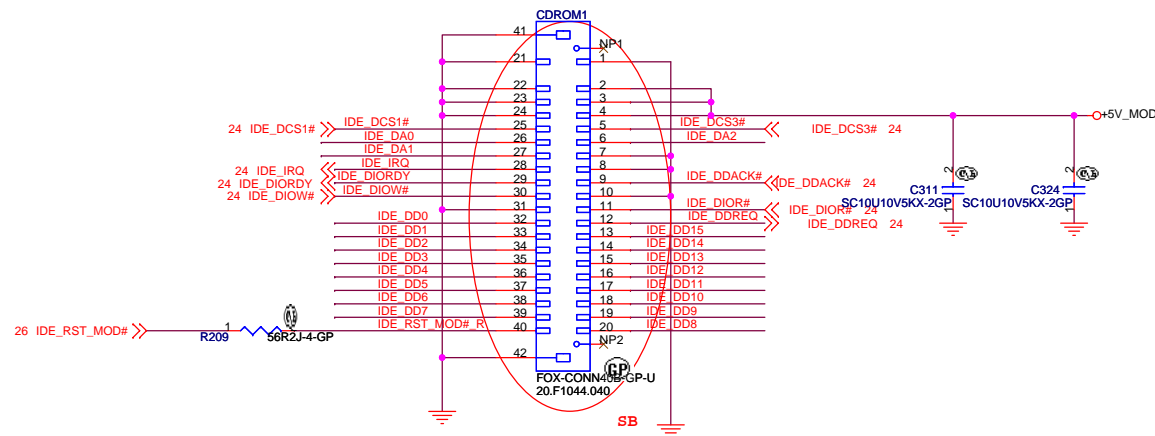
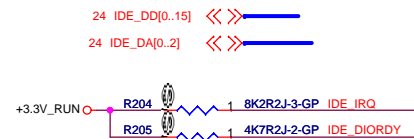
Note :
 $VSET = (Tp - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (Tp - 70) / 21$
 Where $Tp = 70$ to 101 degrees C
 Tp set at 88 degrees C
 Guardian temp tolerance = ± 3 degrees C



C916, C459, C472 Please Close to Guardian



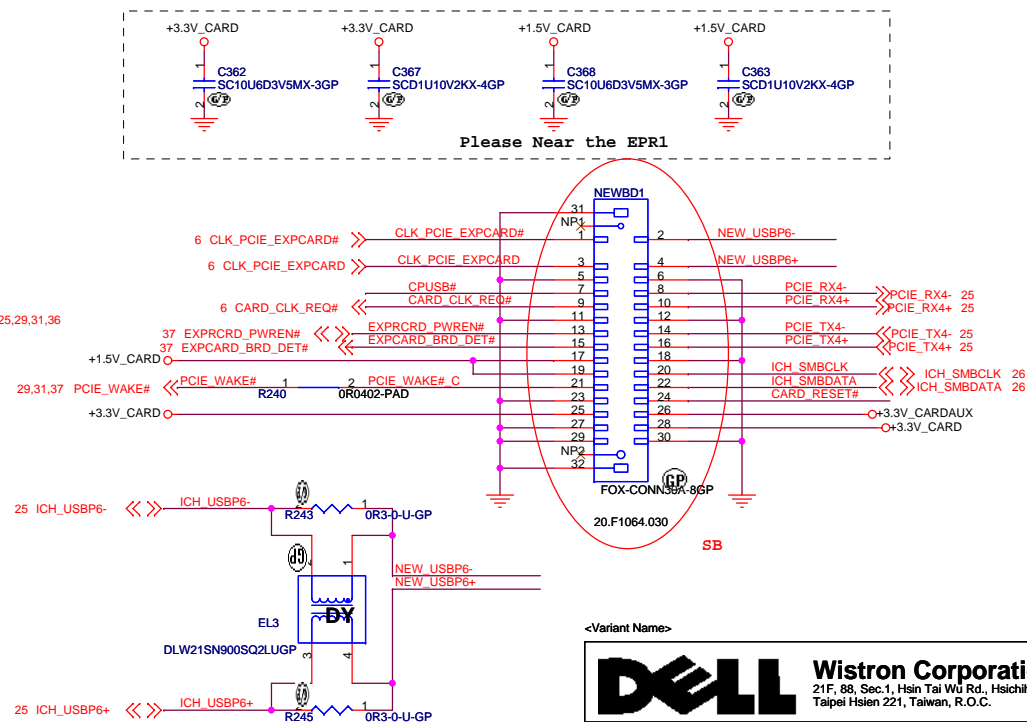
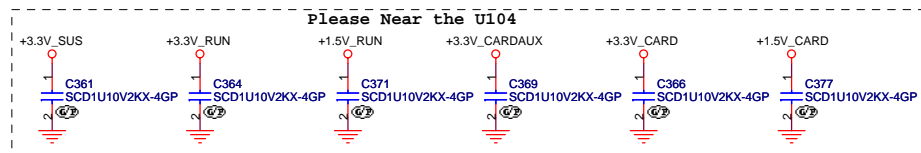
ODD Connector



Test circuit

Use Card and No Card

- +1.5V_CARD Max. 650mA, Average 500mA.
- +3.3V_CARD Max. 1300mA, Average 1000mA
- +3.3V_CARDAUX Max. 275mA



[illegible]

MiniCard WWAN connector

Close WLAN1

Thurman Discrete

MINICARD/WLAN/WWAN

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Taipei Hsien 221, Taiwan, R.O.C.

Date: Tuesday, November 06, 2007

Sheet 31 of 50

Revision: -1

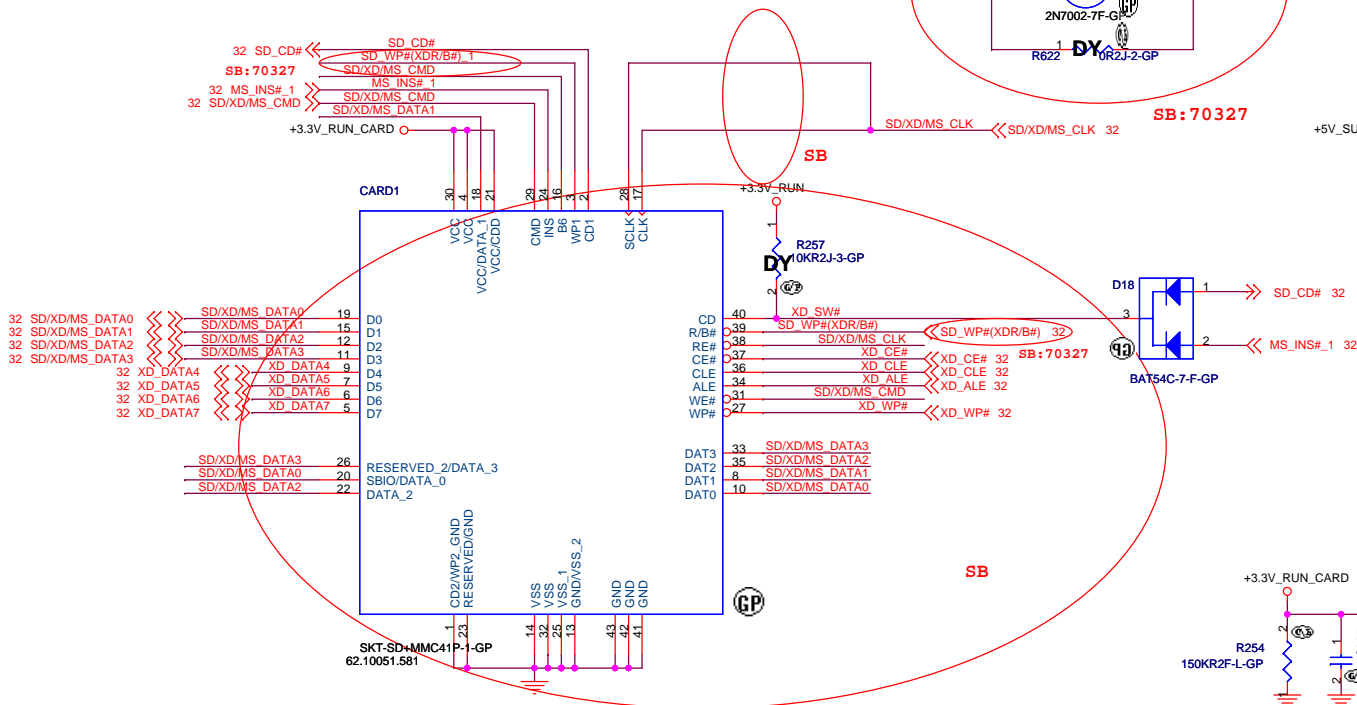
Title			
<i>Thurman Discrete</i>			
Size	Document Number	Rev	
A3	<i>MINICARD/WLAN/WWAN</i>	-1	
Date:	Tuesday, November 06, 2007	Sheet	31 of 50



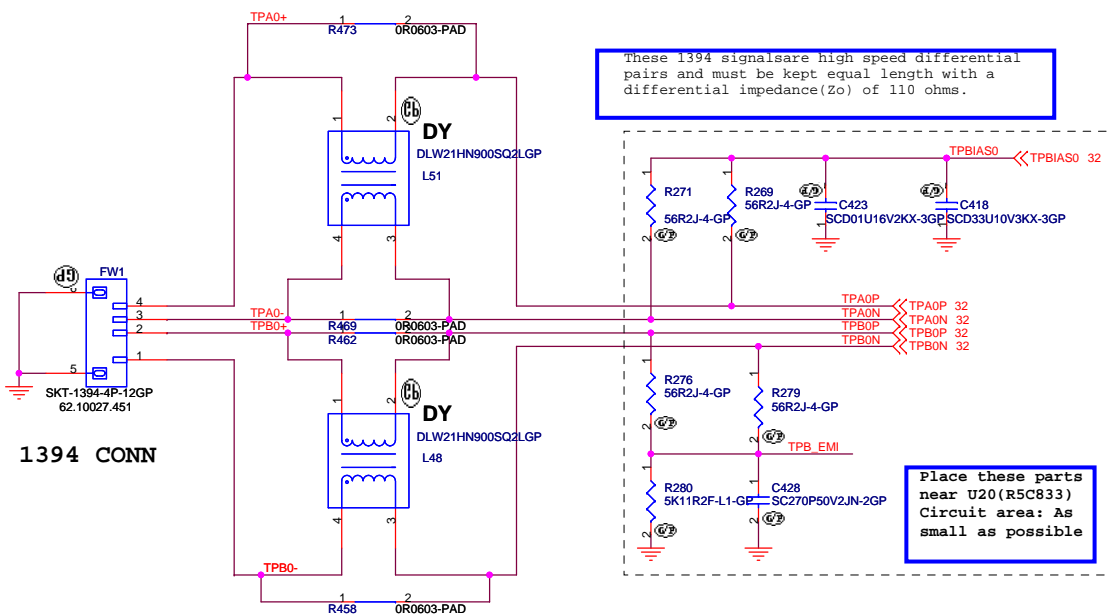
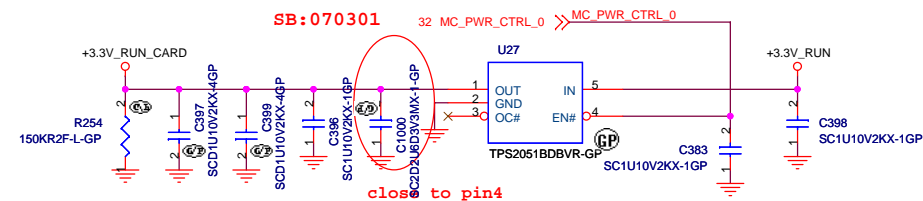
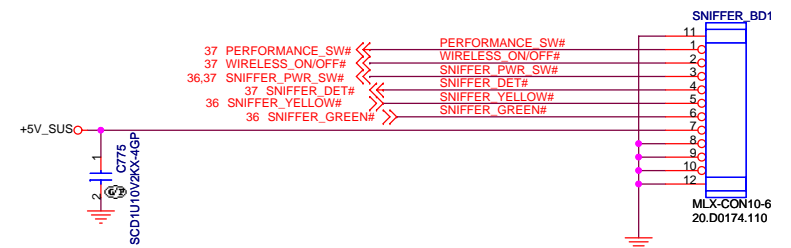
Thurman Discrete

1394 R5C833

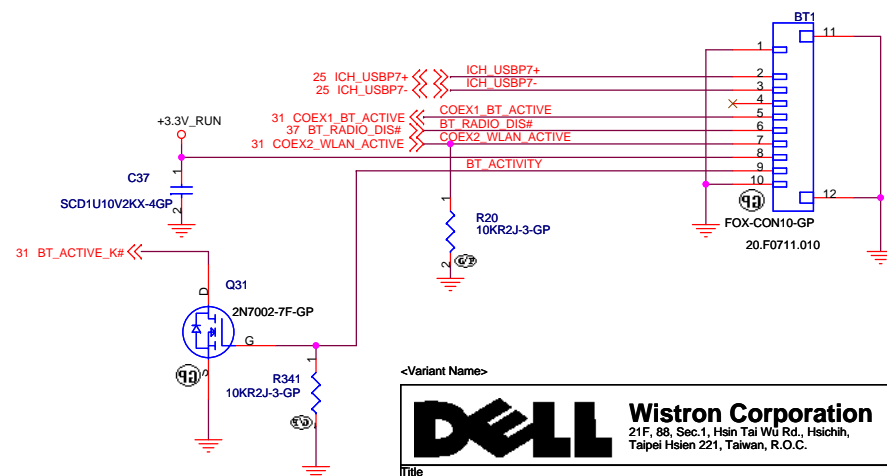
Sheet 32 of 50

Card Reader CONN

SNIFFER BOARD CONN



Bluetooth Module conn.



<Variant Name>

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Title

Thurman Discrete

Size

Document Number

A3 8in1 /1394/SNIFFER BD CON/BT

Date: Tuesday, November 06, 2007

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	R
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AUD_EXT_MIC_L

AUD_EXT_MIC_R

MIC_IN_L_2

MIC_IN_R_2

AUD_VREFOUT_B

AUD_MIC_SWITCH

100K R2J-1-GP

C790

SC10U10V5KX-2GP

R586

R594

R587

R599

4K7R2J-2-GP

4K7R2J-2-GP

C785

SC1U6D3V3KX-1GP

C789

MIC_IN_L_2

SC1U6D3V3KX-1GP

2MIC_IN_L_3

2MIC_IN_R_3

BLM18BD601SN1D-GP

L62

BLM18BD601SN1D-GP

L61

0R0402-PAD

0R0402-PAD

600ohm 100MHz

200mA 0.5ohm DC

EC25

EC24

SC100P60V2JN-3GP

SC100P60V2JN-3GP

1

2

3

4

5

6

7

8

9

10

AUDIO_IK85-GP-U

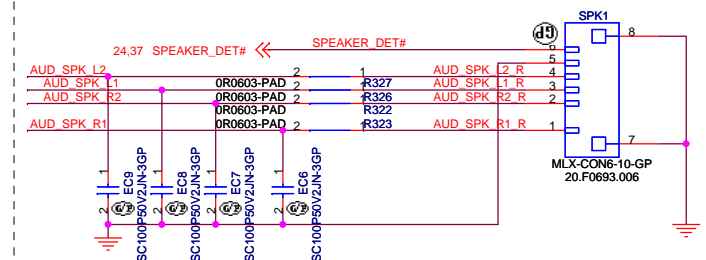
22.10088.D41

-1:70507

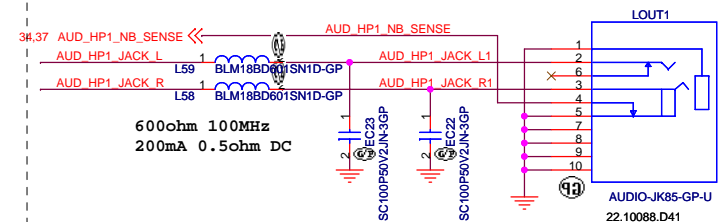
DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>Thurman Discrete</i>
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Size A3	Document Number CODEC STAC9228	Rev -1
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LINE1 OUT



GAIN SETTING



Thurman Discrete

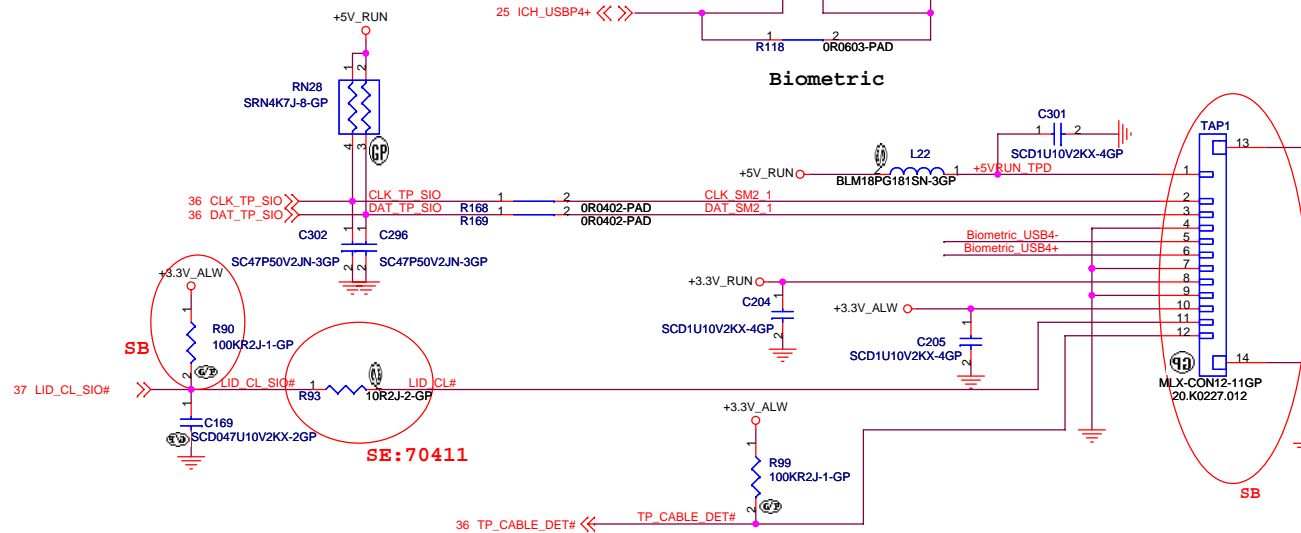
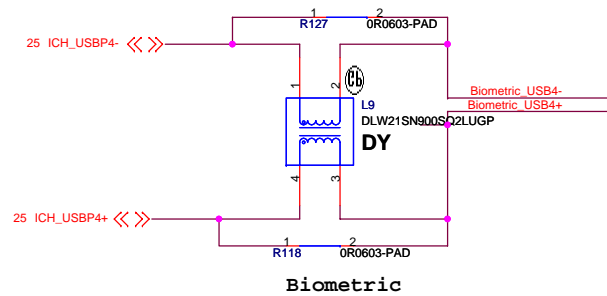
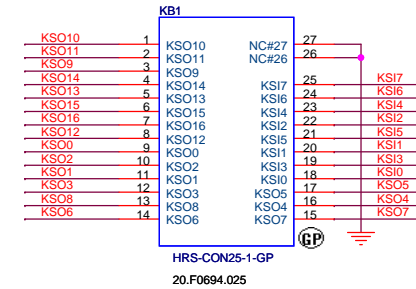
AUDIO AMP

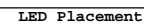
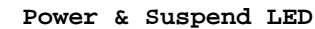
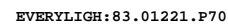
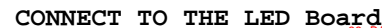
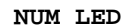
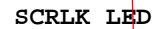
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GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Title			
Thurman Discrete			
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A3	KBC MEC5025/DEBUG CONN	-1	
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	Title
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Thurman Discrete

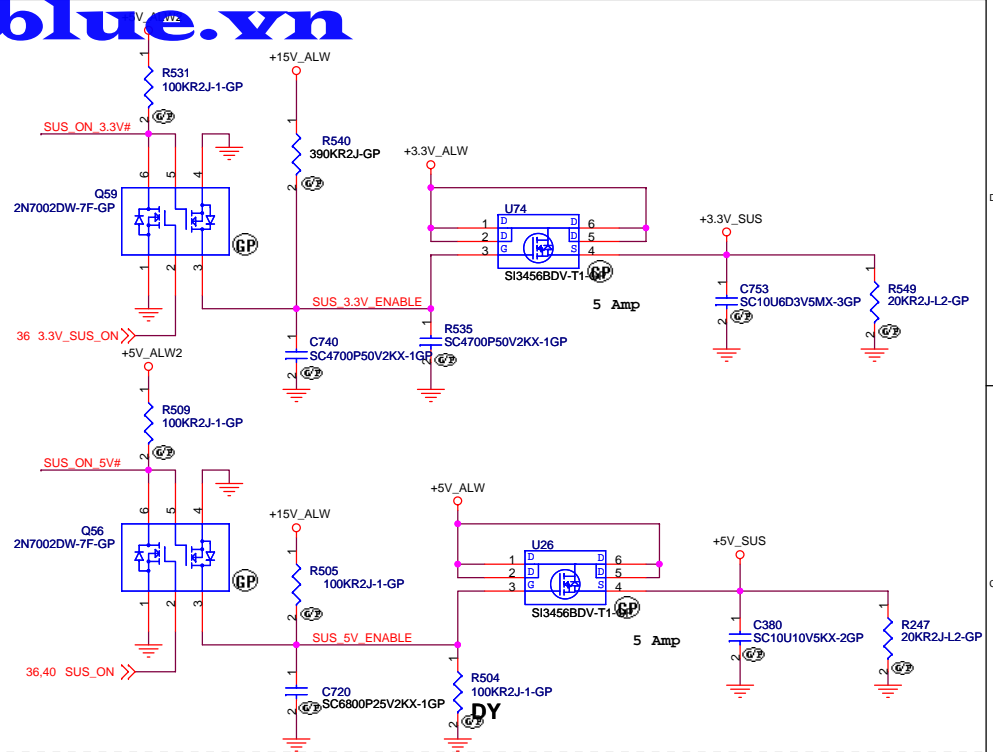
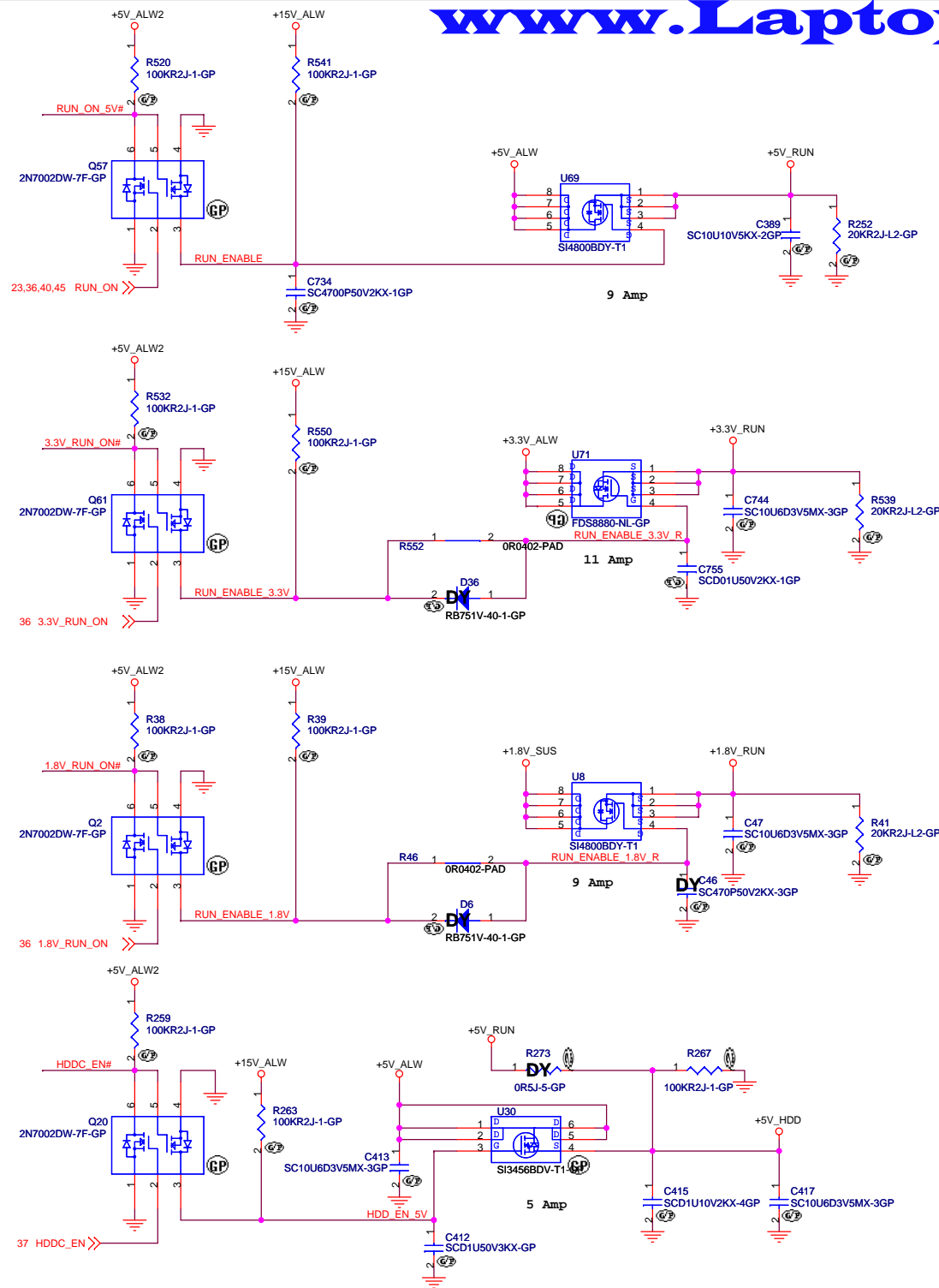
Size

Document Number

LED BD/Capacity Button BD

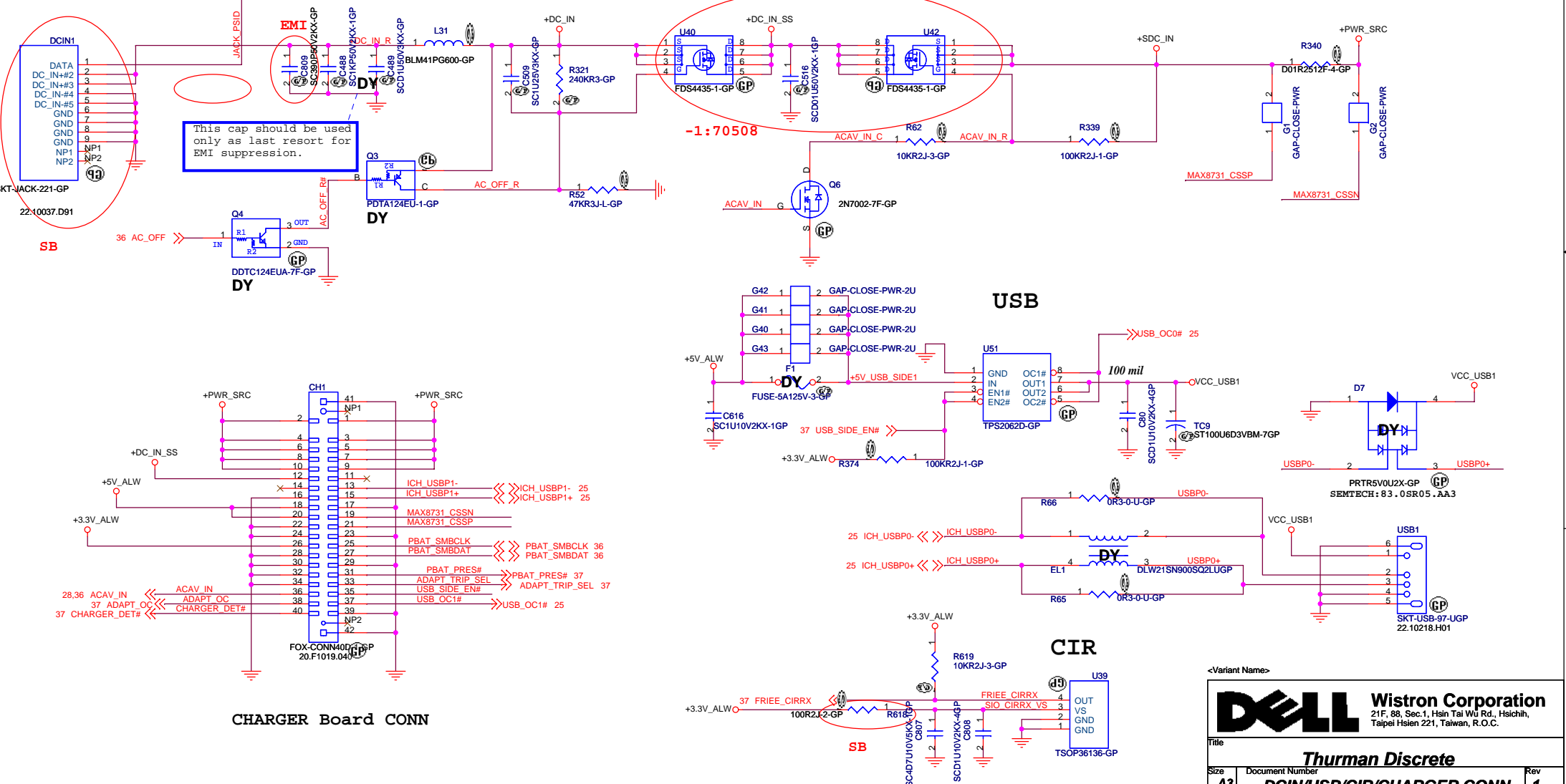
Date: Thursday, November 22, 2007

Sheet 39 of 50



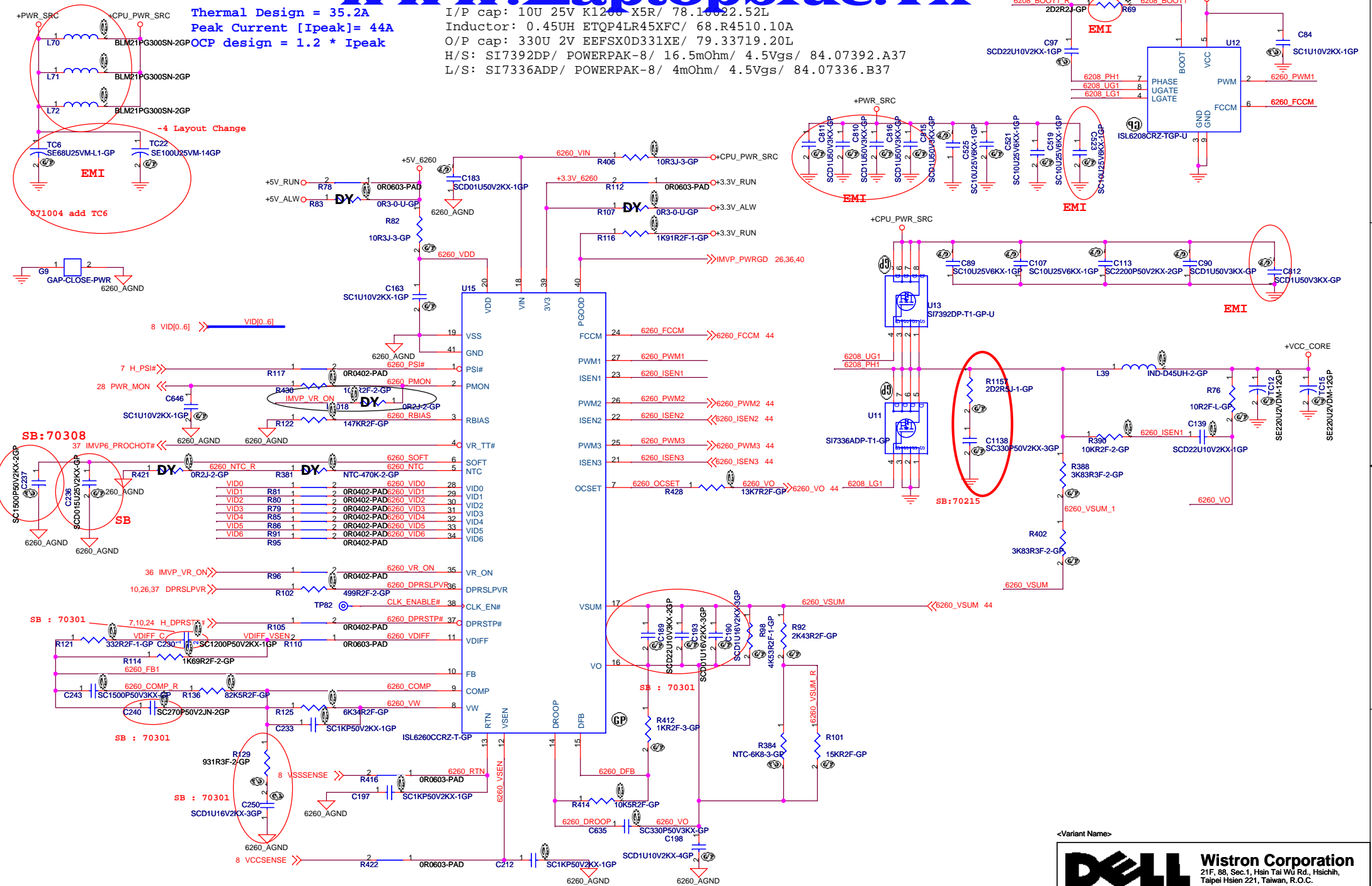
<Variant Name>

Adapter In



Thermal Design = 35.2A
Peak Current [Ipeak] = 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1200-X5R/ 78.10022.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEF5X0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



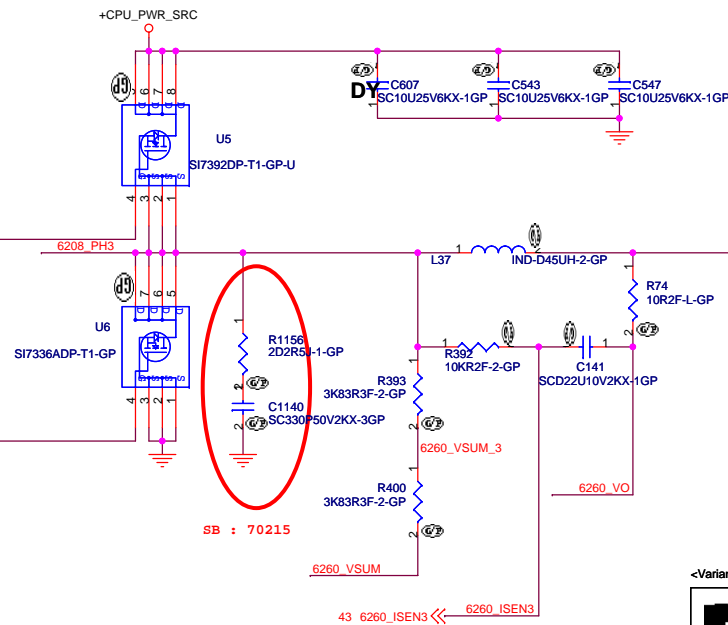
<Variant Name>

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Title: **Thurman Discrete**

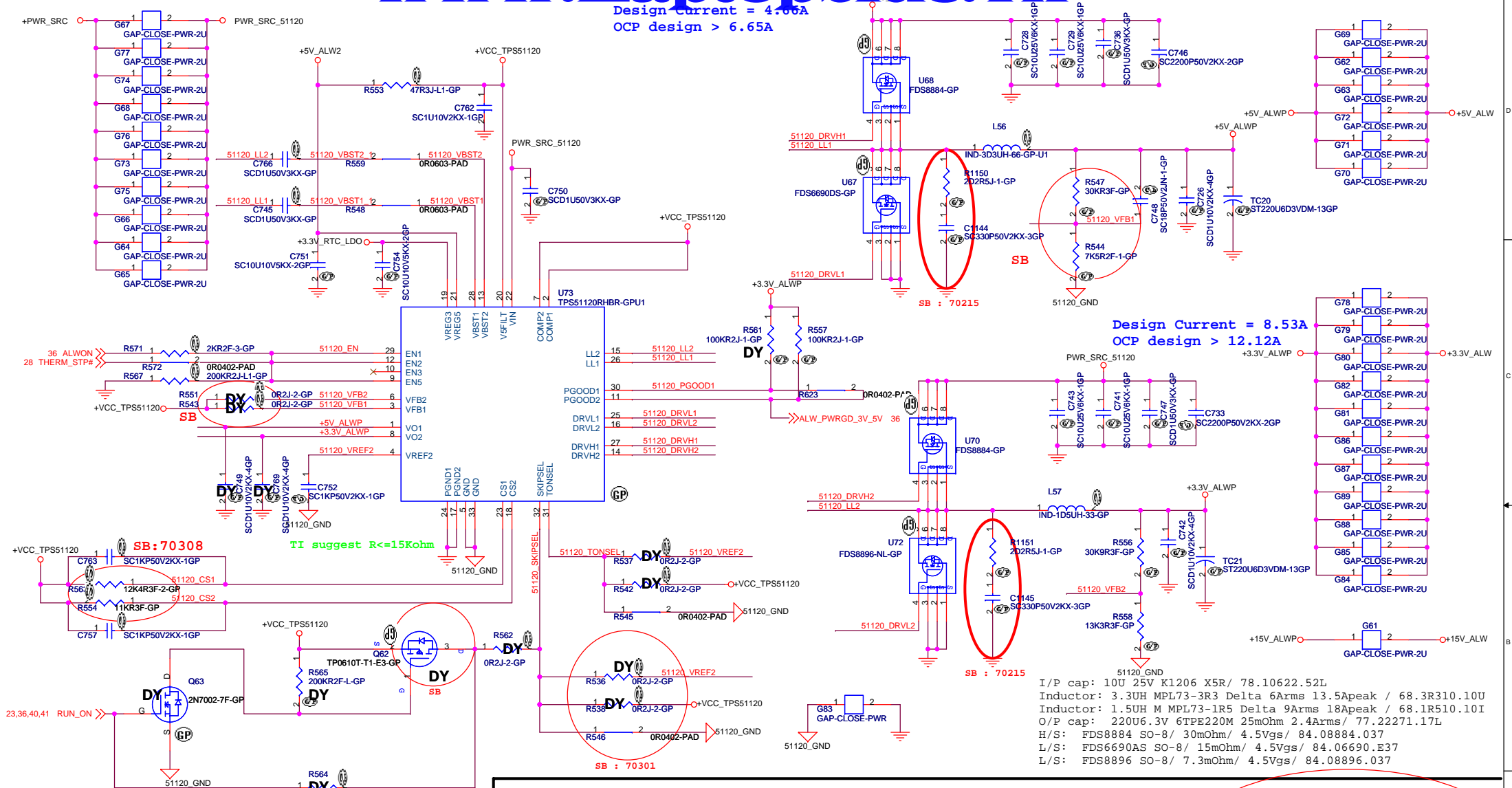
Size: **A3** Document Number: **CPU Core-01** Rev: **-1**

Date: Thursday, November 22, 2007 Sheet: 43 of 50

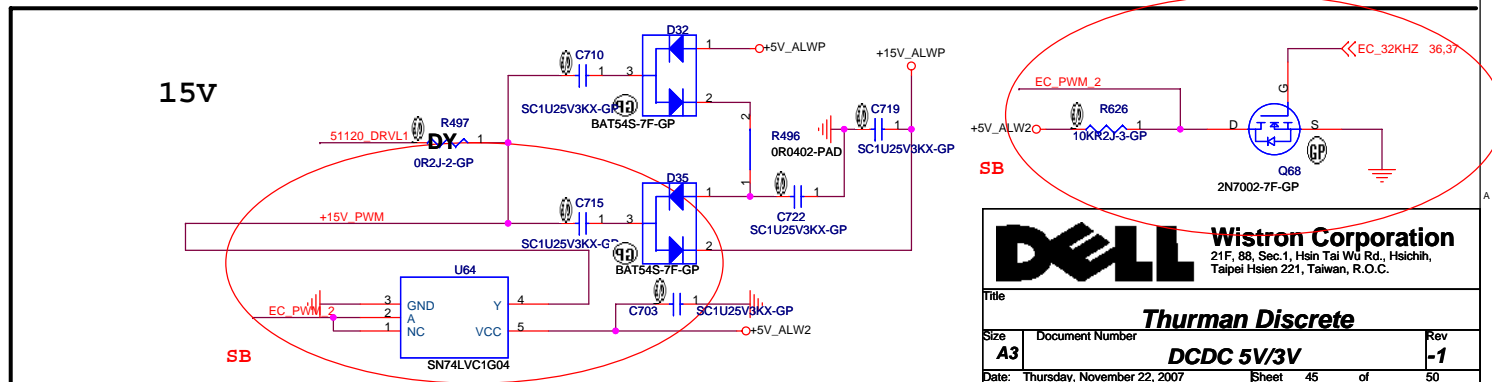


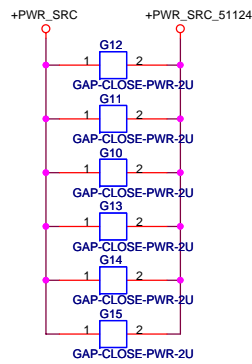
50

Design current = 4.06A
OCP design > 6.65A



	SKIPSEL	AUTOSKIP	TP50A1	V5FILET
SKIPSEL	SKIPSEL	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VR503 ON



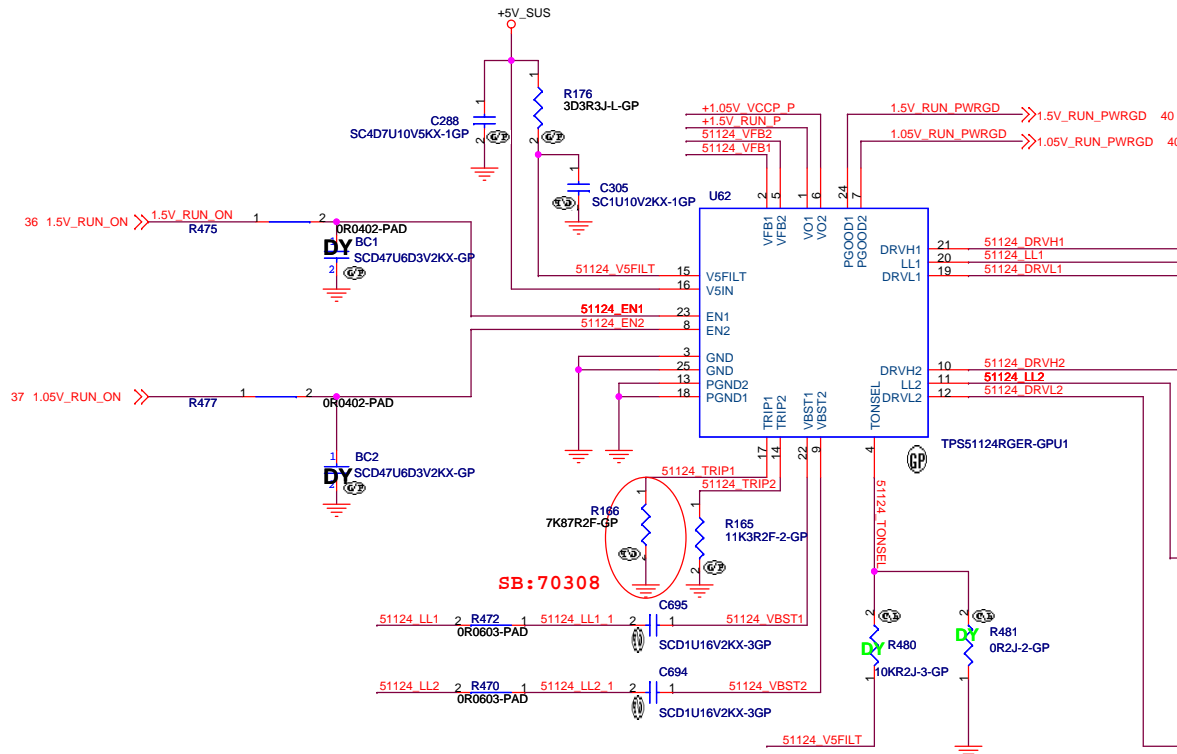


$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$$

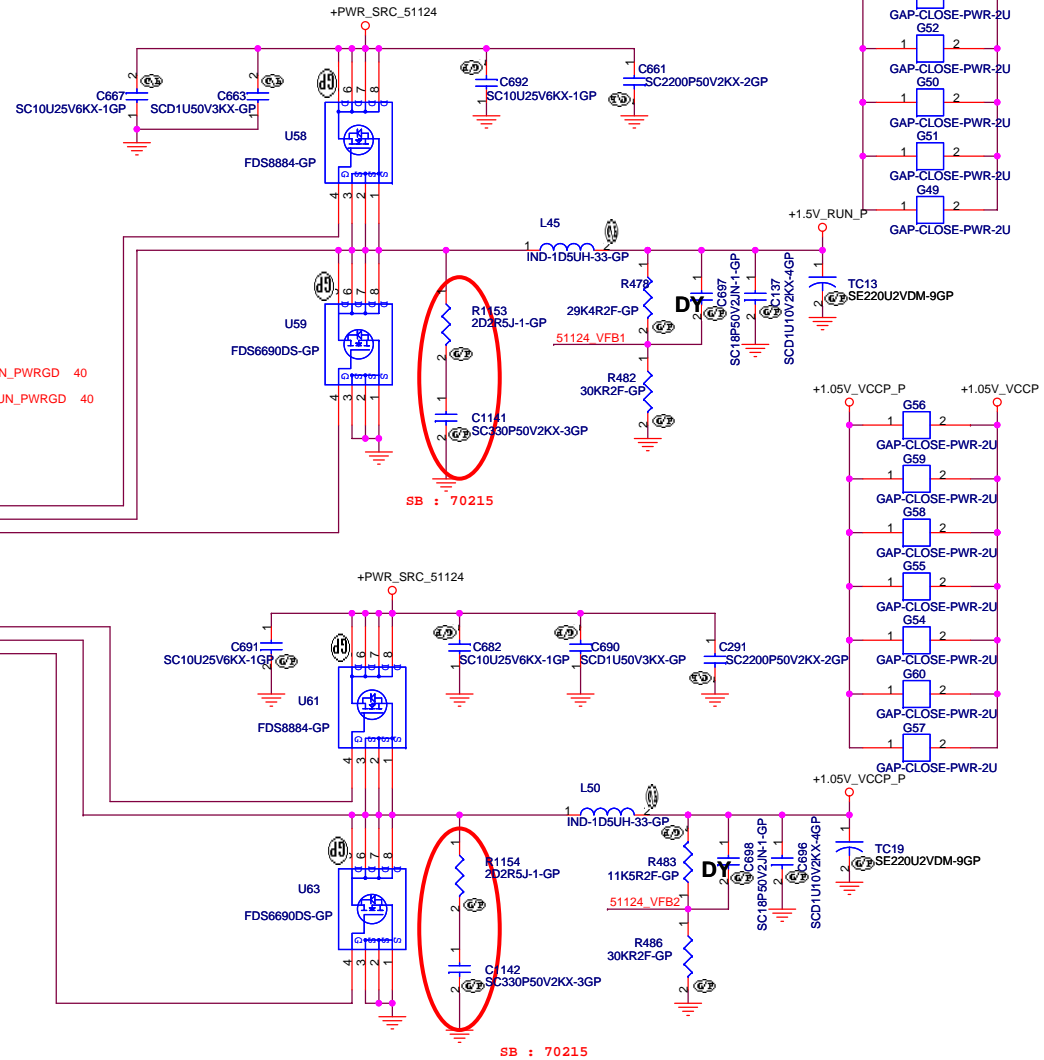
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



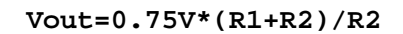
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2) / R2$ --> Skip Mode



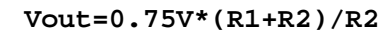
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 OCP design > 7.3A

<Variant Name>



Ton = 200KOhm --> 330KHz

<Variant Name>

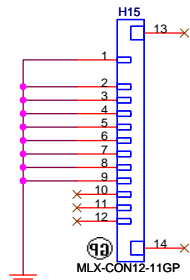
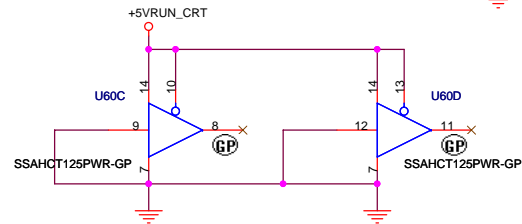
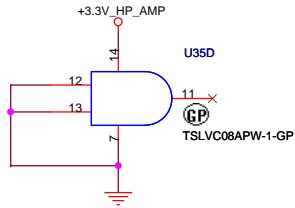
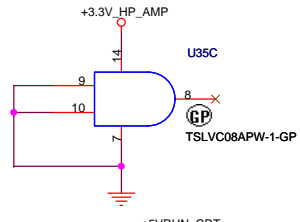
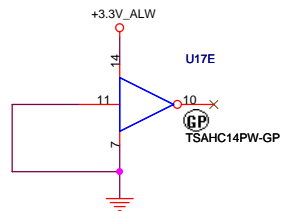


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 2V EEPF50D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz

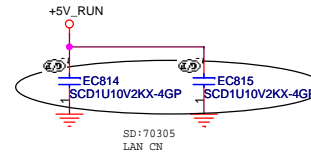
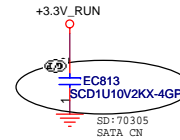
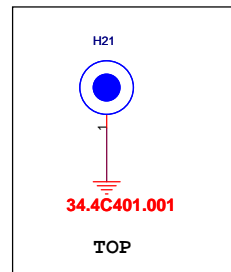
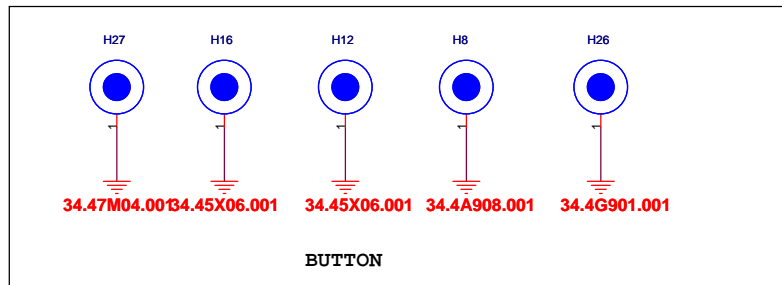
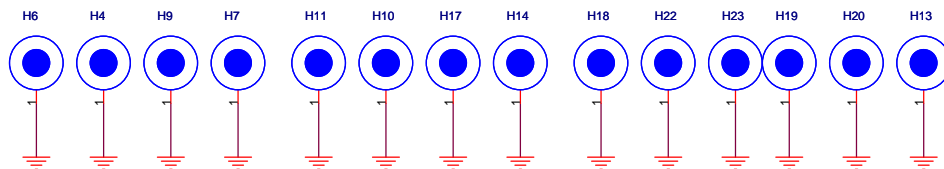
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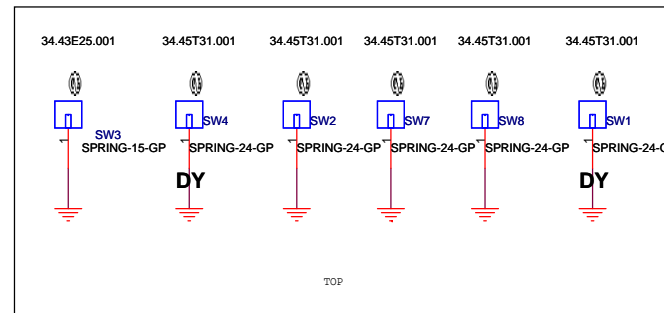
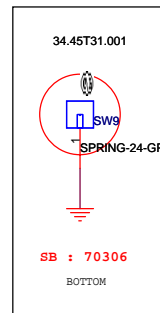
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34.4C309.001



SW3 - 34.43E25.001
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001



<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A3

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Date: Thursday, November 22, 2007

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