


# Thurman UMA Schematics Document

uFCPGA Mobile Merom

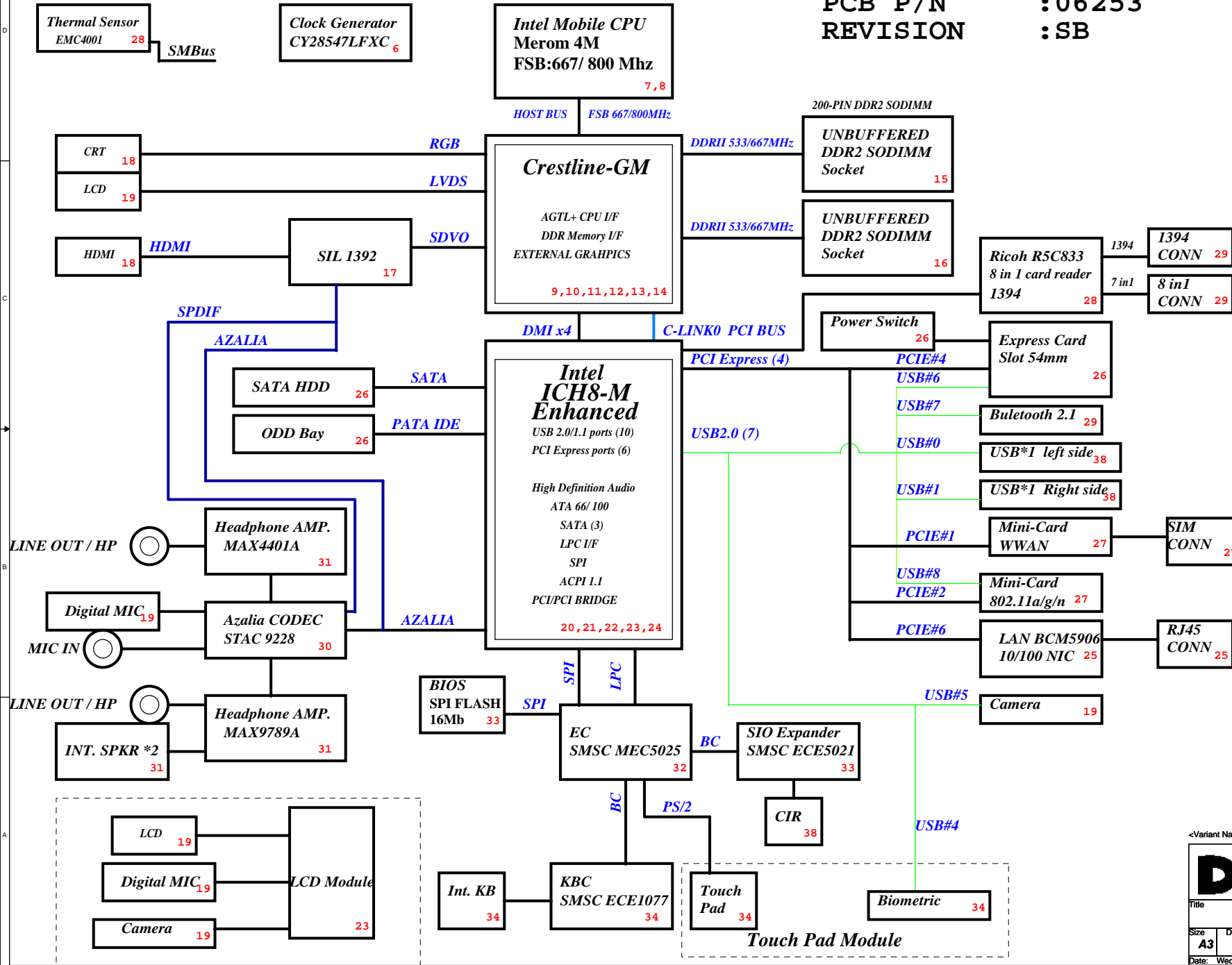
Intel Crestline-GM + ICH8M

2007-11-19

REV : -1 (DELL:A00)

<Variant Name>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>Thurman UMA</b>	
Size	Document Number	Rev	
<b>A3</b>		<b>-1</b>	
Date: Friday, January 18, 2008	Sheet 1 of 46		

Project code:91.4C301.001  
PCB P/N :06253  
REVISION :SB



<b>System DC/DC</b>		<b>41</b>
<b>TPS51120</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
<b>+PWR_SUS</b>	<b>+5V_ALW +5V_SUS</b> <b>+3.3V_SUS</b> <b>+3.3V_RTC_LDO</b>	
<b>System DC/DC</b>		<b>42</b>
<b>TPS51124</b>		
<b>+PWR_SUS</b>	<b>+1.05V_VCCP</b> <b>+1.5V_RUN</b>	
<b>DDR2 DC/DC</b>		<b>43</b>
<b>TPS51117</b>		
<b>+PWR_SUS</b>	<b>+1.8V_SUS</b>	
<b>LDO</b>		<b>43</b>
<b>TPS51100</b>		
<b>+1.8V_SUS</b>	<b>+0.9V_DDR_VTT</b> <b>V_DDR_MCH_REF</b>	
<b>LDO</b>		<b>44</b>
<b>SC339SKTRT</b>		
<b>+PWR_SUS</b>	<b>+1.25V_RUN</b>	

<b>Battery Charger</b> <b>MAX8731</b>		38
<i>INPUTS</i>	<i>OUTPUTS</i>	
+PWR_SRC	+VCHGR	

<b>CPU DC/DC</b> <b>ISL6260C</b> <span style="float: right;">39,40</span>	
<i>INPUTS</i>	<i>OUTPUTS</i>
<i>+PWR_SRC</i>	<i>+VCC_CORE</i>

PCB LAYER
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

<Variant Name>



Title

***Thurman UMA***

Size

Document Number

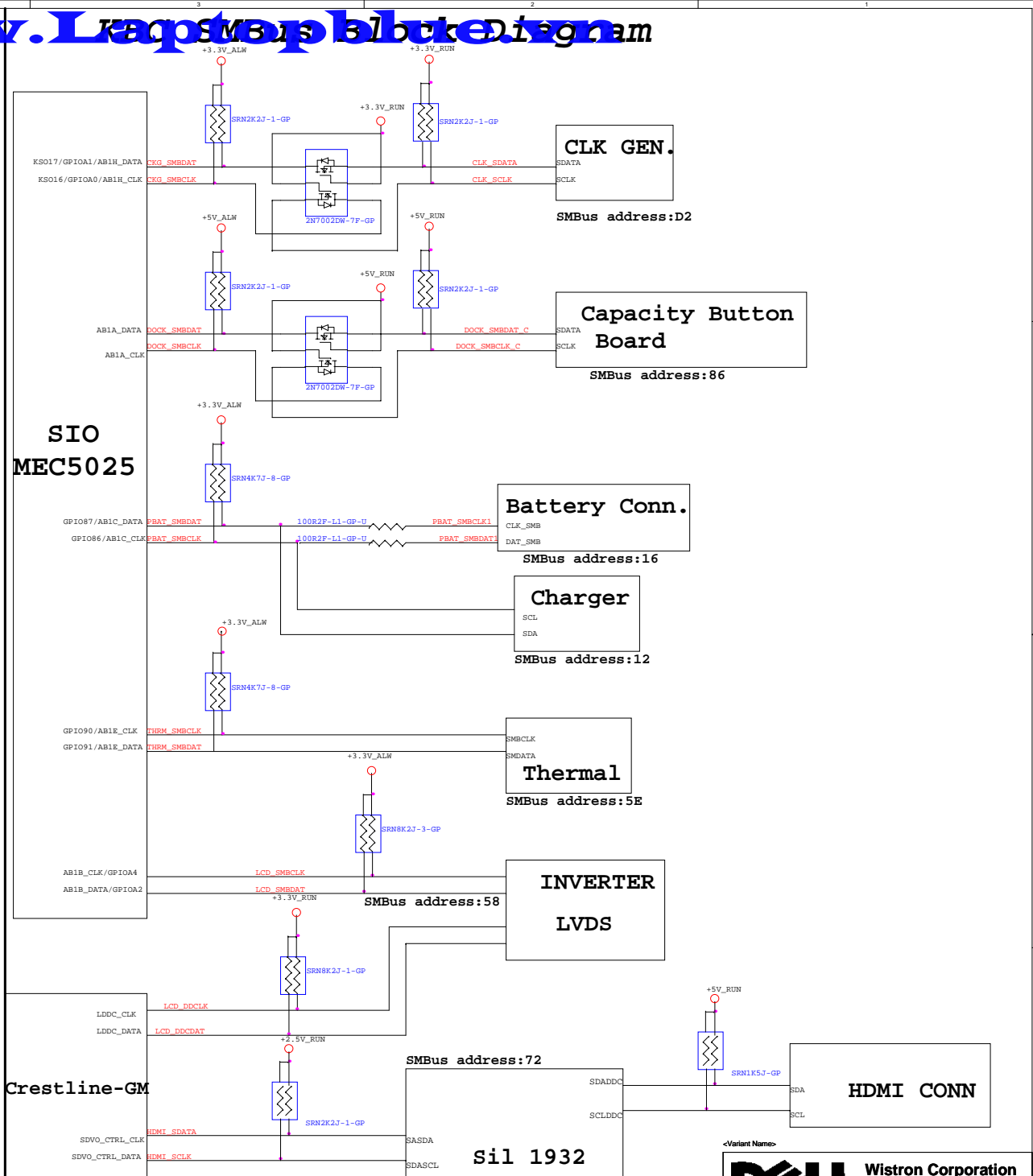
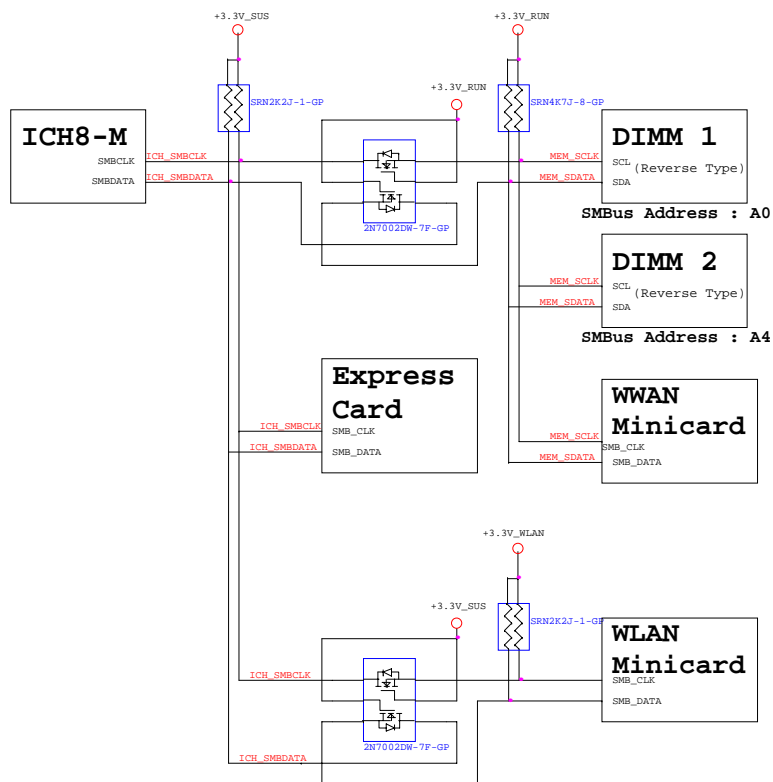
### BLOCK DIAGRAM

Date:

Wednesday, November 07, 2007

Sheet 2 of 46

ICH8 SMBus Block Diagram



## CLOCK GEN CY28547

27M\_SS/LCD96\_100M SELECTION TABLE

## BYTE 10

bits S1	Bit4 S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

## INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05 VccSusi_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi_05,VccSusi_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVDtp3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	DCT
1	1	LPC(Default)

Integrated VccSusi_05,VccSusi_5,VccCL1_5		
SM_INTVRMEN	High=Enable Low=Disable	
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable Low=Disable	

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

\* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

## PCI Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

## PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

## ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

INTEL ICH8-M INTEGRATED  
PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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A3

Document Number

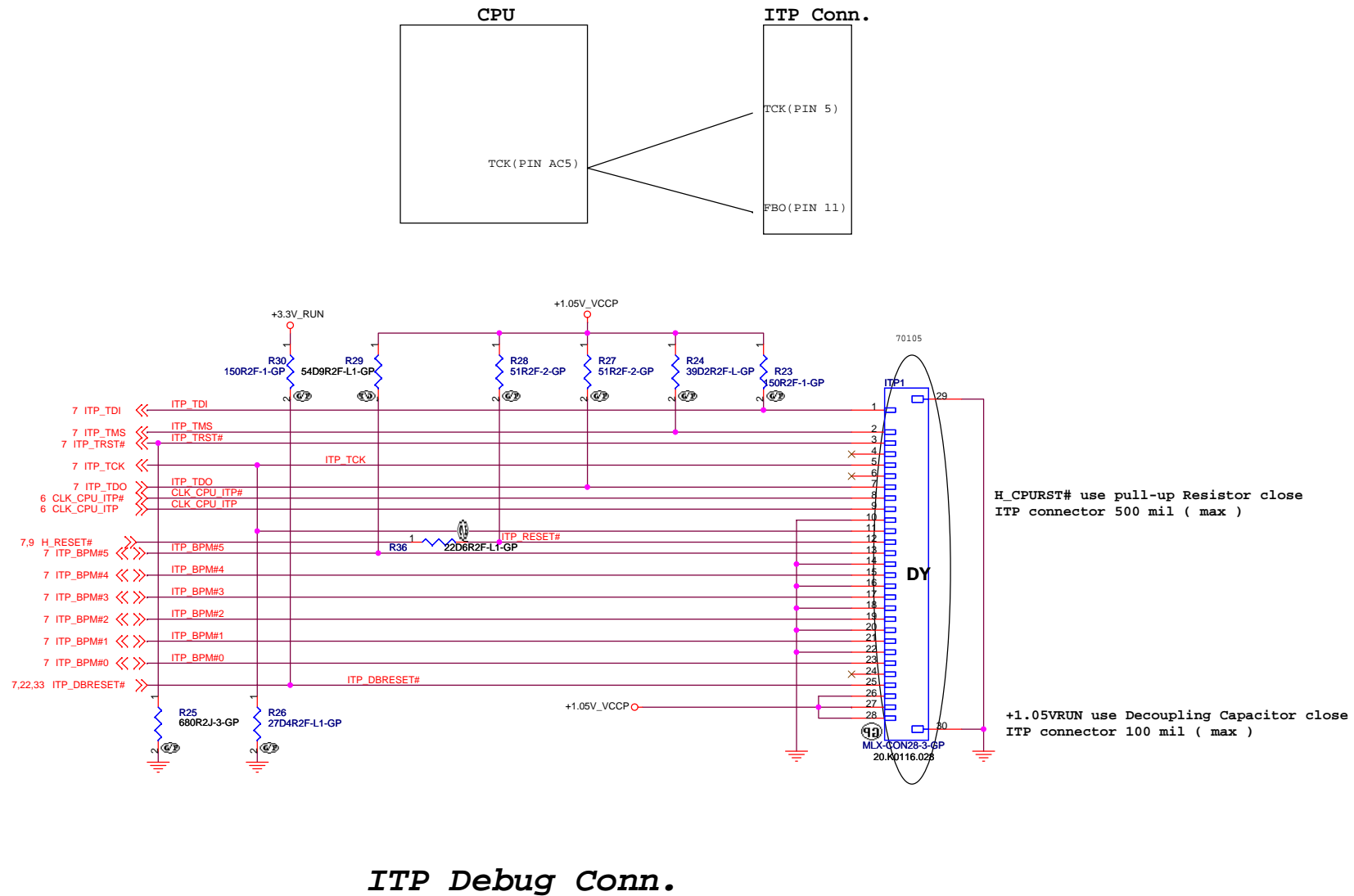
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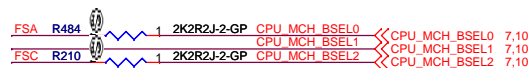
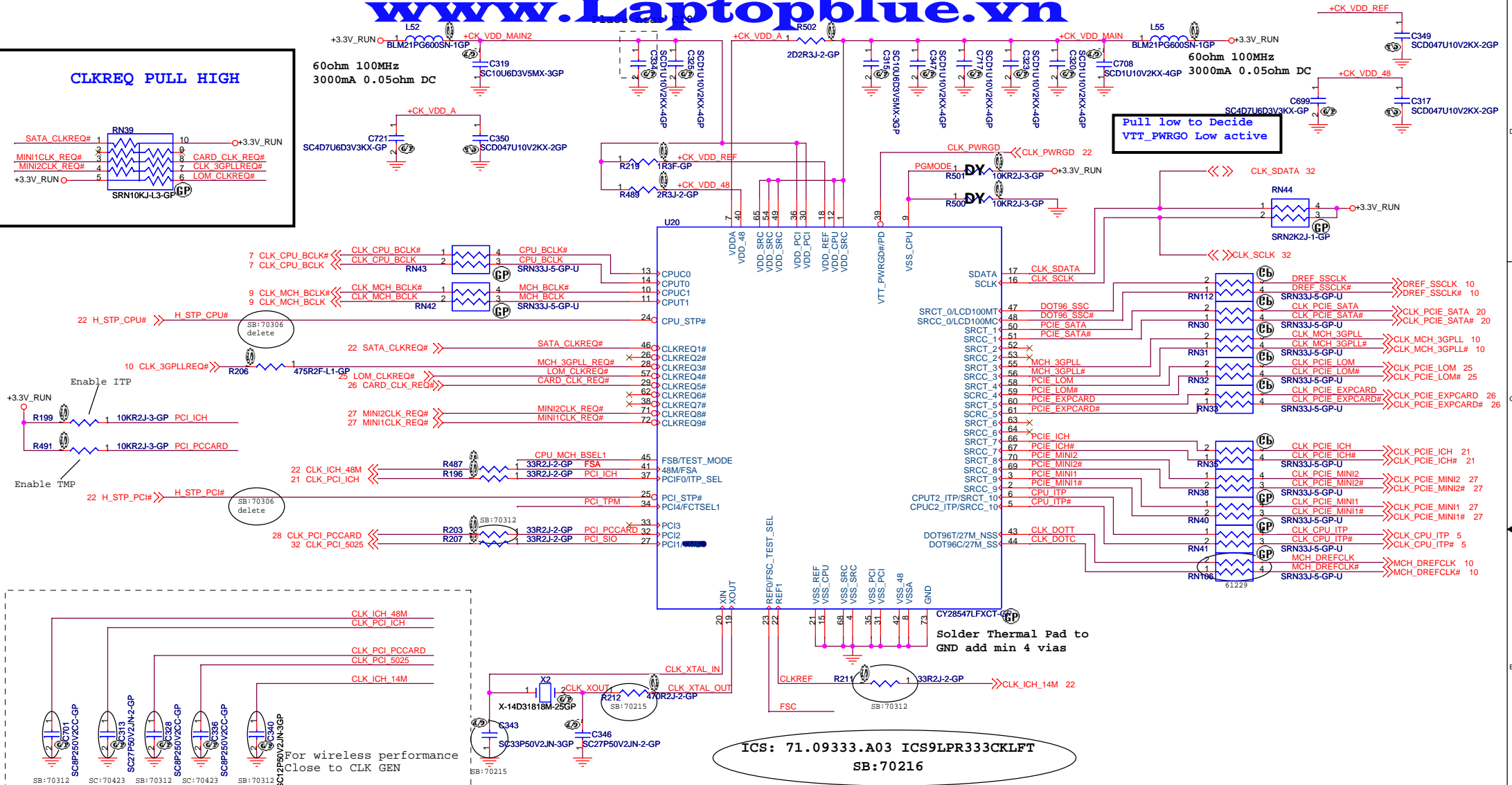
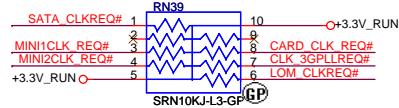
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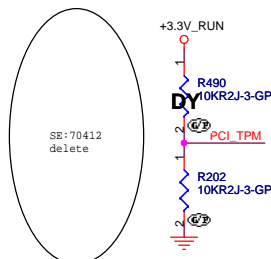
Sheet 4 of 46



CLKREQ PULL HIGH



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M



ICS: 71.09333.A03 ICS9LPR333CKLFT  
SB:70216

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC 0

PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

<Variant Name>



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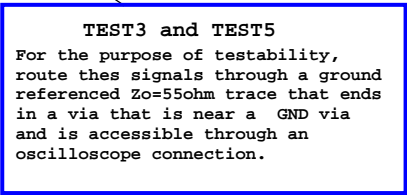
**CLK\_GEN CY28547**

Date \_\_\_\_\_

Wednesday, November 07, 2007

Sheet 6 of

Rev



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original value:SKT-CPU478P-GP
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**Thurman UMA**

Rev

**CPII-ESB(1/2)** **-1**

CF-0-F-SB(1/2)	-1
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Sheet 7 of 46

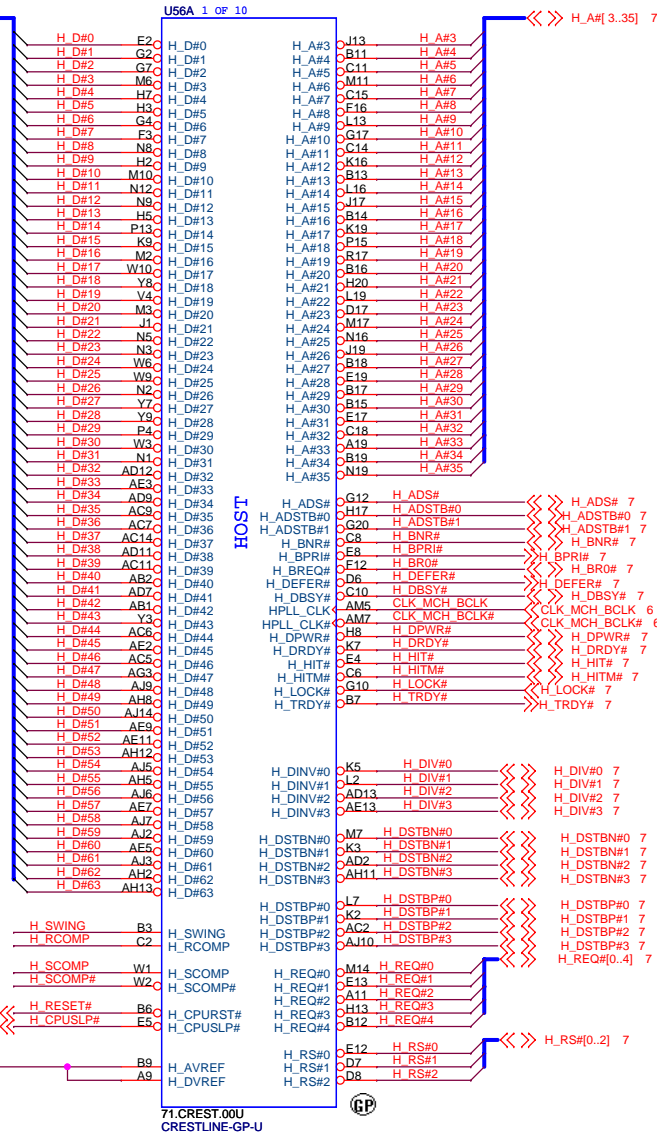
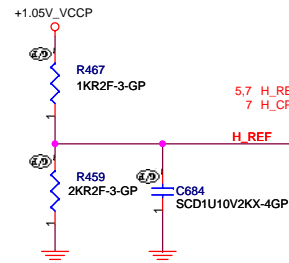




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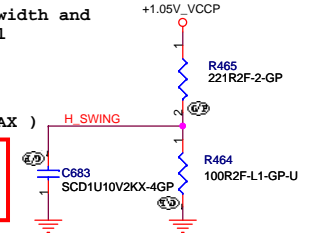
H\_REF Decoupling Crestline  
close Crestline 100 mil



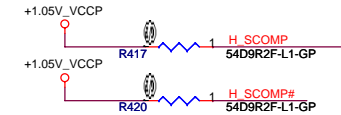
H\_SWING routing Trace width and  
Spacing use 10 / 20 mil

H\_SWING Resistors and  
Capacitors close  
Caliistoga 500 mil ( MAX )

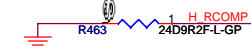
From Schematic Design  
Checklit v.1201  
221 1% pull high 100  
1% pull low



H\_SCOMP and H\_SCOMP# Resistors  
and Capacitors close Caliistoga  
500 mil ( MAX )  
Zo=55ohms



H\_RCOMP routing Trace width and  
Spacing use 10 / 20 mil



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Size  
**A3**

Document Number

**GMCH-FSB LIBC (1/6)**

Rev

**-1**

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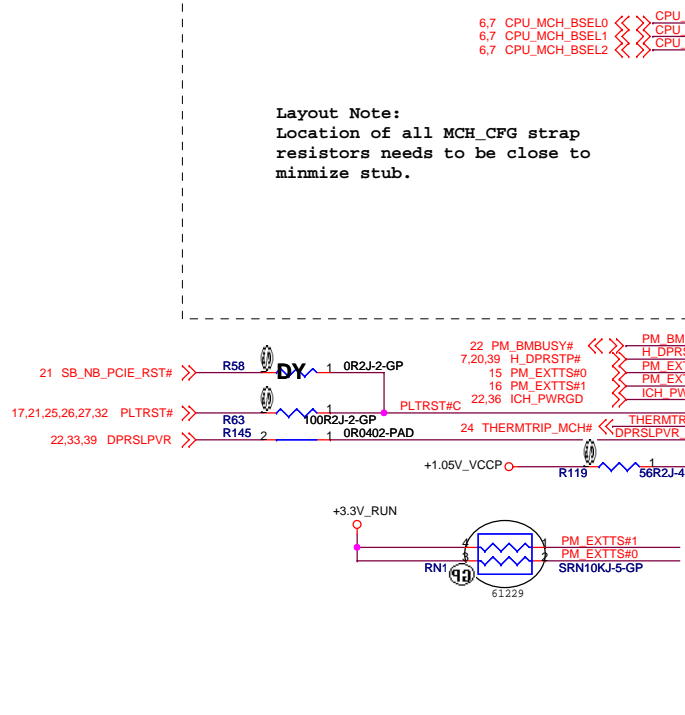
Sheet 9 of 46

\* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16	Disabled	Enabled *
CFG 18	1.05V *	1.5V
CFG 19	Normal Operation *	Reserved Lane
CFG 20	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

CFG[13:12]	
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
CFG[2..0] FSB Select	
LHL	FSB 800
LHH	FSB 667
Other	Reserved

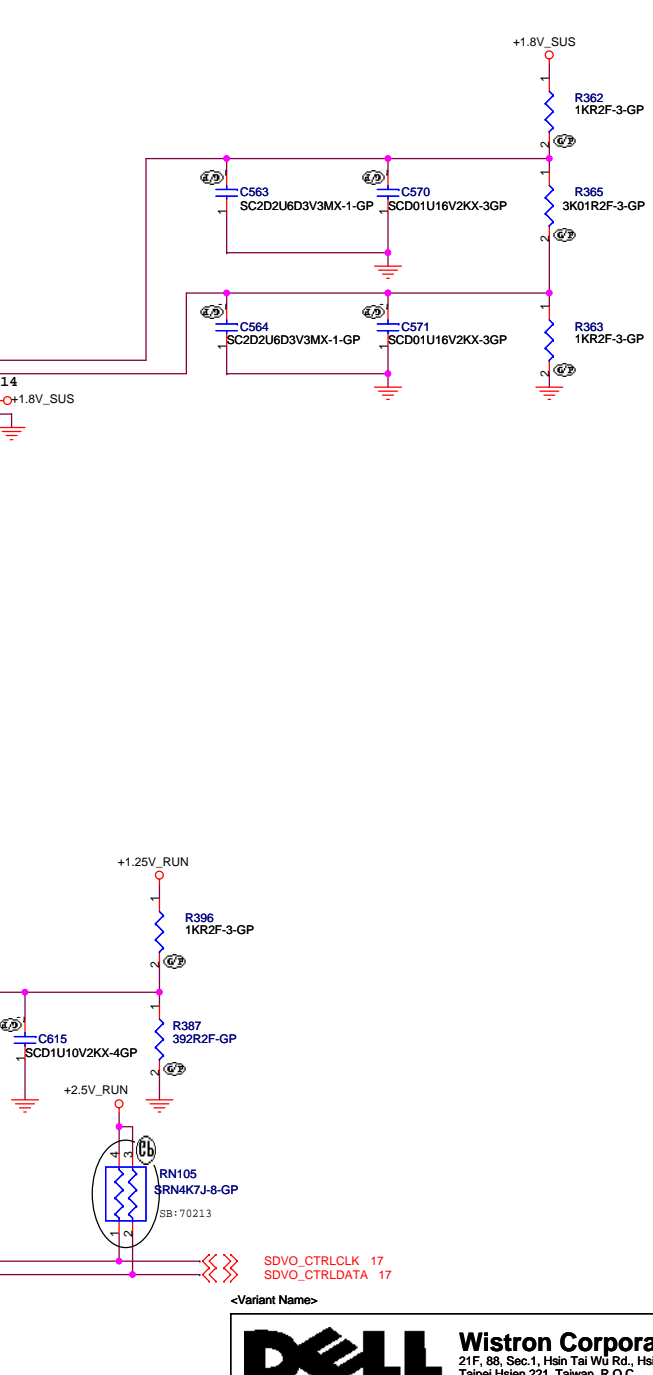
Layout Note:  
Location of all MCH\_CFG strap resistors needs to be close to minimize stub.



U56B 2 OF 10

- × P36 RSVD#P36
- × P37 RSVD#P37
- × R35 RSVD#R35
- × N35 RSVD#N35
- × AR12 RSVD#AR12
- × AR13 RSVD#AR13
- × AM12 RSVD#AM12
- × AN13 RSVD#AN13
- × J12 RSVD#J12
- × AR37 RSVD#AR37
- × AM36 RSVD#AM36
- × AL36 RSVD#AL36
- × AM37 RSVD#AM37
- × D20 RSVD#D20
- × H10 RSVD#H10
- × B51 RSVD#B51
- × BJ20 RSVD#BJ20
- × BK22 RSVD#BK22
- × BF19 RSVD#BF19
- × BK18 RSVD#BK18
- × BJ18 RSVD#BJ18
- × BF23 RSVD#BF23
- × BG23 RSVD#BG23
- × BC23 RSVD#BC23
- × BD24 RSVD#BD24
- × BH39 RSVD#BH39
- × AW20 RSVD#AW20
- × BK20 RSVD#BK20
- × B44 RSVD#B44
- × C44 RSVD#C44
- × A35 RSVD#A35
- × B37 RSVD#B37
- × B36 RSVD#B36
- × B34 RSVD#B34
- × C34 RSVD#C34
- × C21 CFG0
- × C23 CFG1
- × F23 CFG2
- × F23 CFG3
- × F23 CFG4
- × F23 CFG5
- × N23 CFG6
- × J23 CFG7
- × J23 CFG8
- × J23 CFG9
- × J23 CFG10
- × J23 CFG11
- × J23 CFG12
- × E23 CFG13
- × E20 CFG14
- × K23 CFG15
- × M20 CFG16
- × M24 CFG17
- × J32 CFG18
- × N33 CFG19
- × J35 CFG20
- × G41 PM\_BMBUSY#
- × L39 H\_DPRSTP#
- × L36 PM\_EXTTS#0
- × J36 PM\_EXTTS#1
- × AW49 ICH\_PWRGD
- × AV20 THERMTRIP\_MCH#
- × N20 DPRSLPVR
- × G36 THERMTRIP#
- × BJ51 NC#BJ51
- × BK51 NC#BK51
- × BL50 NC#BL50
- × BL49 NC#BL49
- × BL3 NC#BL3
- × BL2 NC#BL2
- × BK1 NC#BK1
- × BJ1 NC#BJ1
- × E1 NC#E1
- × A5 NC#A5
- × C51 NC#C51
- × B50 NC#B50
- × A50 NC#A50
- × A49 NC#A49
- × BK2 NC#BK2

- SM\_CLK0 AV29 M\_CLK\_DDR0 M\_CLK\_DDR0 15
- SM\_CLK1 BB23 M\_CLK\_DDR1 M\_CLK\_DDR1 15
- SM\_CLK3 BA25 M\_CLK\_DDR2 M\_CLK\_DDR2 16
- SM\_CLK4 AV23 M\_CLK\_DDR3 M\_CLK\_DDR3 16
- SM\_CLK0 AW30 M\_CLK\_DDR#0 M\_CLK\_DDR#0 15
- SM\_CLK#1 CA23 M\_CLK\_DDR#1 M\_CLK\_DDR#1 15
- SM\_CLK#3 AW25 M\_CLK\_DDR#2 M\_CLK\_DDR#2 16
- SM\_CLK#4 AW23 M\_CLK\_DDR#3 M\_CLK\_DDR#3 16
- SM\_CKE0 BE29 DDR\_CKE0\_DIMMA DDR\_CKE0\_DIMMA 15
- SM\_CKE1 AV32 DDR\_CKE1\_DIMMA DDR\_CKE1\_DIMMA 15
- SM\_CKE3 BD39 DDR\_CKE2\_DIMMB DDR\_CKE2\_DIMMB 16
- SM\_CKE4 BG37 DDR\_CKE3\_DIMMB DDR\_CKE3\_DIMMB 16
- SM\_CS0 BG20 DDR\_CS0\_DIMMA# DDR\_CS0\_DIMMA# 15
- SM\_CS#1 BK16 DDR\_CS1\_DIMMA# DDR\_CS1\_DIMMA# 15
- SM\_CS#2 BG16 DDR\_CS2\_DIMMB# DDR\_CS2\_DIMMB# 16
- SM\_CS#3 BE13 DDR\_CS3\_DIMMB# DDR\_CS3\_DIMMB# 16
- SM\_ODT0 BH18 M\_ODT0 M\_ODT0 15
- SM\_ODT1 BJ15 M\_ODT1 M\_ODT1 15
- SM\_ODT2 BJ14 M\_ODT2 M\_ODT2 16
- SM\_ODT3 BE16 M\_ODT3 M\_ODT3 16
- SM\_RCOMP\_VOH BK31 SM\_RCOMP\_VOH
- SM\_RCOMP\_VOL BL31 SM\_RCOMP\_VOL
- SM\_VREF#AR49 BL15 SM\_RCOMP 1 20R2F-GP
- SM\_VREF#AW4 BK14 SM\_RCOMP# 1 20R2F-GP
- AR49 O\_V\_DDR\_MCH\_REF
- DPDLL\_REF\_CLK B42 MCH\_DREFCLK# MCH\_DREFCLK# 6
- DPDLL\_REF\_CLK# C42 MCH\_DREFCLK# MCH\_DREFCLK# 6
- DPDLL\_REF\_SSCLK H48 DREF\_SSCLK# DREF\_SSCLK# 6
- DPDLL\_REF\_SSCLK# H47 DREF\_SSCLK# DREF\_SSCLK# 6
- PEG\_CLK K44 CLK\_MCH\_3GPLL# CLK\_MCH\_3GPLL# 6
- PEG\_CLK# K45 CLK\_MCH\_3GPLL# CLK\_MCH\_3GPLL# 6
- DMI\_RXN0 AN47 DMI\_MRX\_ITX\_N0 DMI\_MRX\_ITX\_N0 21
- DMI\_RXN1 AJ38 DMI\_MRX\_ITX\_N1 DMI\_MRX\_ITX\_N1 21
- DMI\_RXN2 AN42 DMI\_MRX\_ITX\_N2 DMI\_MRX\_ITX\_N2 21
- DMI\_RXN3 AN46 DMI\_MRX\_ITX\_N3 DMI\_MRX\_ITX\_N3 21
- DMI\_RXP0 AM47 DMI\_MRX\_ITX\_P0 DMI\_MRX\_ITX\_P0 21
- DMI\_RXP1 AJ39 DMI\_MRX\_ITX\_P1 DMI\_MRX\_ITX\_P1 21
- DMI\_RXP2 AN41 DMI\_MRX\_ITX\_P2 DMI\_MRX\_ITX\_P2 21
- DMI\_RXP3 AN45 DMI\_MRX\_ITX\_P3 DMI\_MRX\_ITX\_P3 21
- DMI\_TXN0 AJ46 DMI\_MTX\_IRX\_N0 DMI\_MTX\_IRX\_N0 21
- DMI\_TXN1 AJ41 DMI\_MTX\_IRX\_N1 DMI\_MTX\_IRX\_N1 21
- DMI\_TXN2 AM40 DMI\_MTX\_IRX\_N2 DMI\_MTX\_IRX\_N2 21
- DMI\_TXN3 AM44 DMI\_MTX\_IRX\_N3 DMI\_MTX\_IRX\_N3 21
- DMI\_TXP0 AJ47 DMI\_MTX\_IRX\_P0 DMI\_MTX\_IRX\_P0 21
- DMI\_TXP1 AJ42 DMI\_MTX\_IRX\_P1 DMI\_MTX\_IRX\_P1 21
- DMI\_TXP2 AM39 DMI\_MTX\_IRX\_P2 DMI\_MTX\_IRX\_P2 21
- DMI\_TXP3 AM43 DMI\_MTX\_IRX\_P3 DMI\_MTX\_IRX\_P3 21
- GFX\_VID0 E35
- GFX\_VID1 A39
- GFX\_VID2 C38
- GFX\_VID3 B39
- GFX\_VR\_EN E36
- CL\_CLK0 AM49 CL\_CLK0 22
- CL\_DATA0 AK50 CL\_DATA0 22
- ICH\_CL\_PWROK AT43 ICH\_CL\_PWROK 22,32
- ICH\_CL\_RST0 AN49 ICH\_CL\_RST0 22
- MCH\_CLVREF AM50 MCH\_CLVREF
- SDVO\_CTRL\_CLK H35 SDVO\_CTRLCLK
- SDVO\_CTRL\_DATA K36 SDVO\_CTRLDATA
- CLK\_3GPLLREQ# G39 CLK\_3GPLLREQ# 6
- MCH\_ICH\_SYNC# G40 MCH\_ICH\_SYNC# 22
- TEST1 A37 TEST1 GMCH
- TEST2 R32 TEST2 GMCH

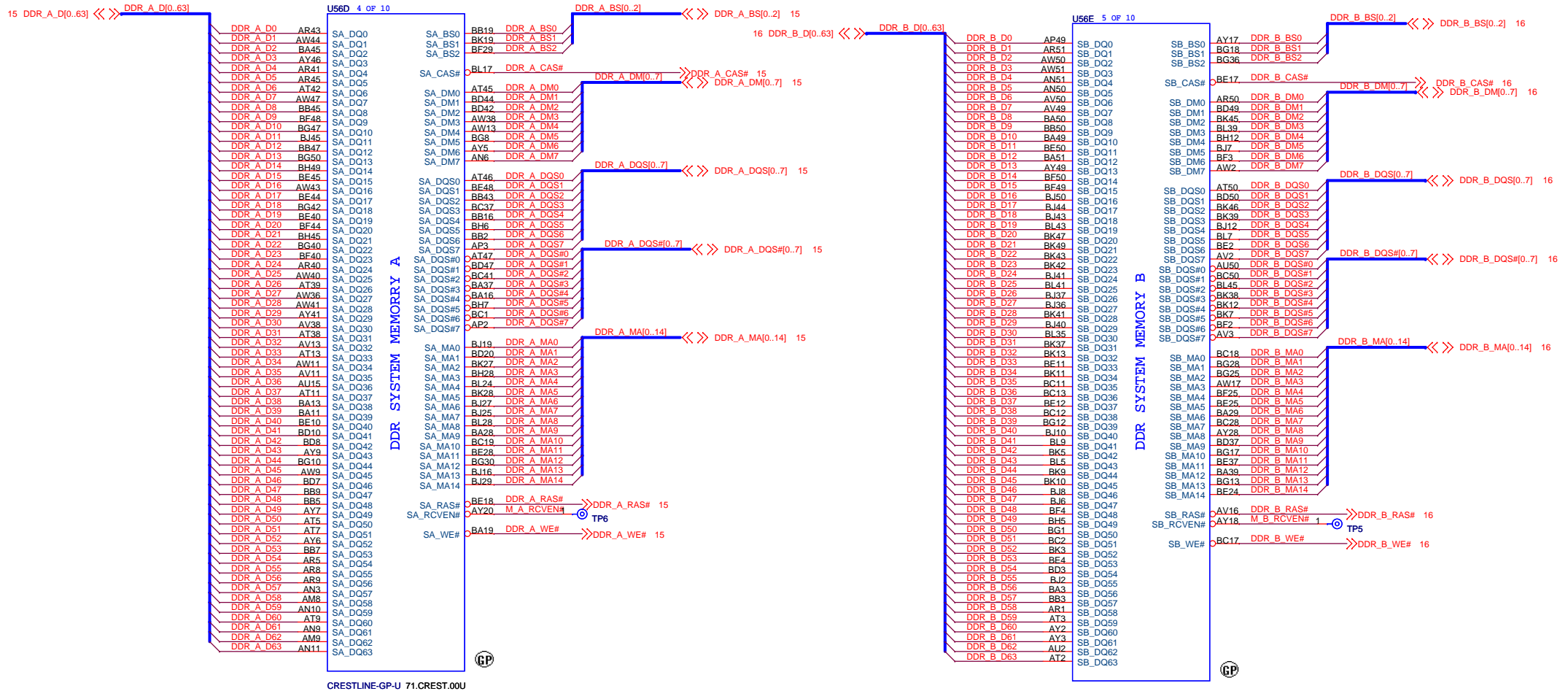


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Size A3 Document Number **Thurman UMA**  
**GMCH-DMI/DDR (2/6)** Rev -1

Date: Wednesday, November 07, 2007 Sheet 10 of 46

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Title
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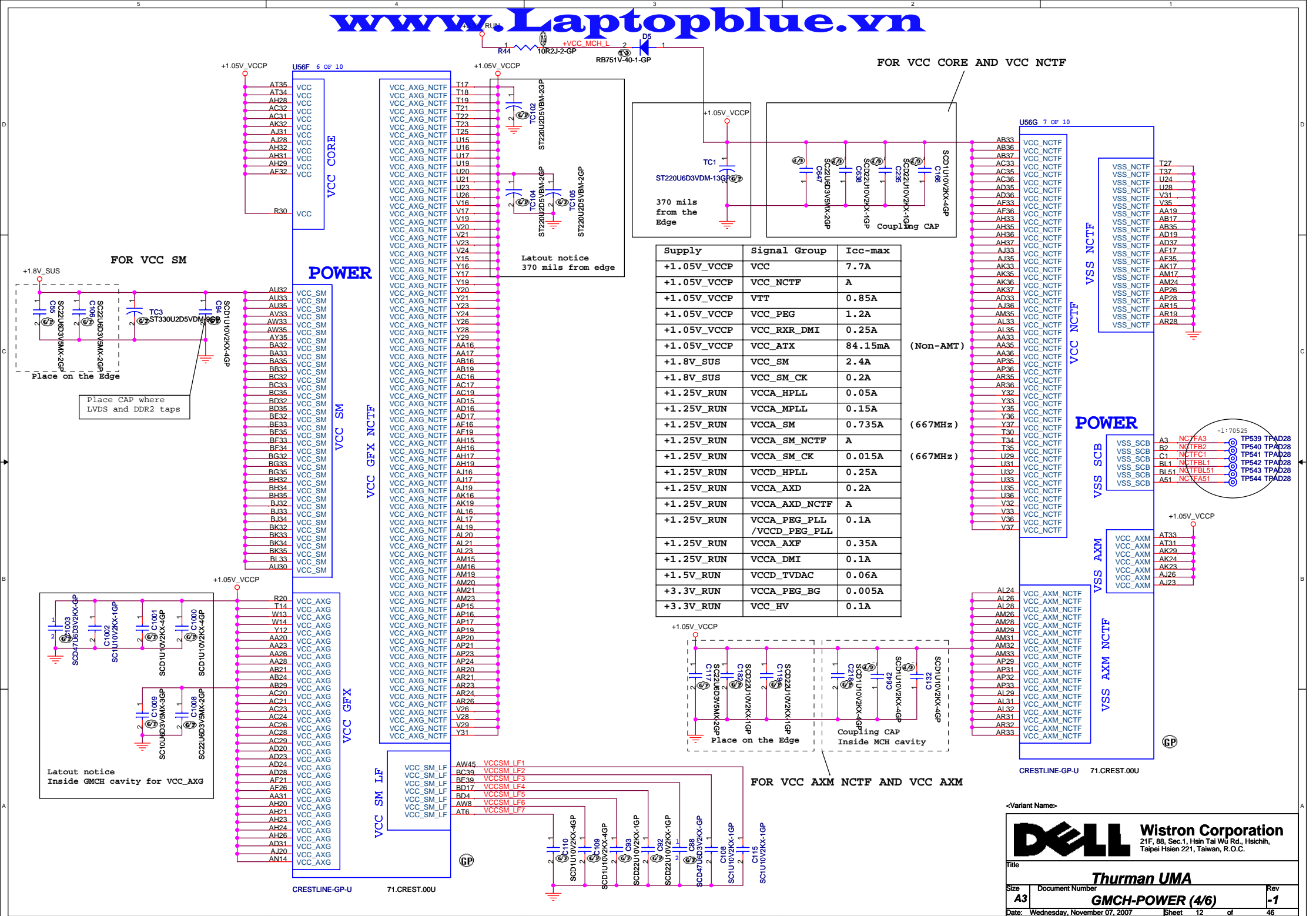
Document Number

**GMCH-DDR (3/6)**

Date:

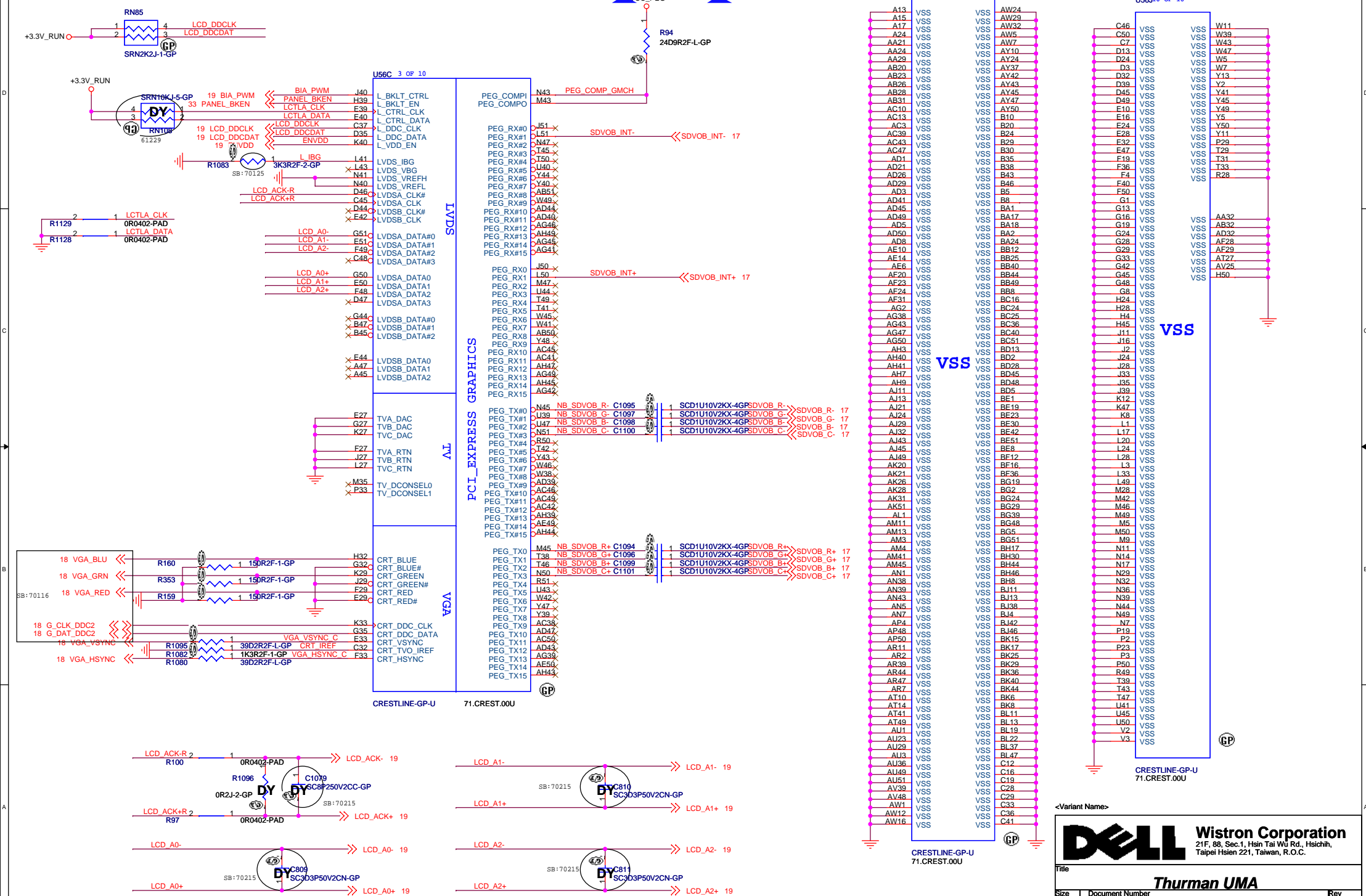
Date: Wednesday, November 07, 2007

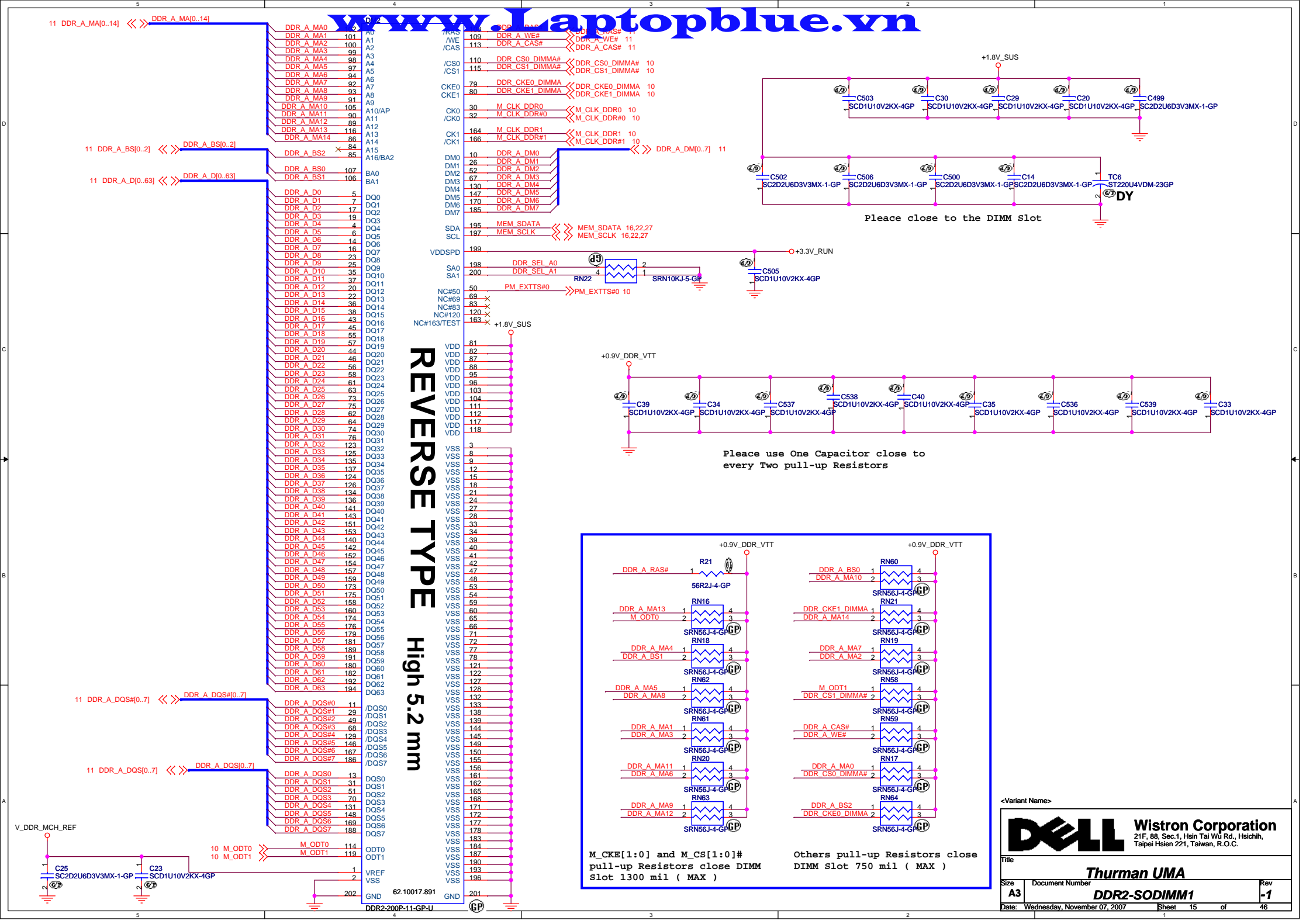
Sheet 11 of 46



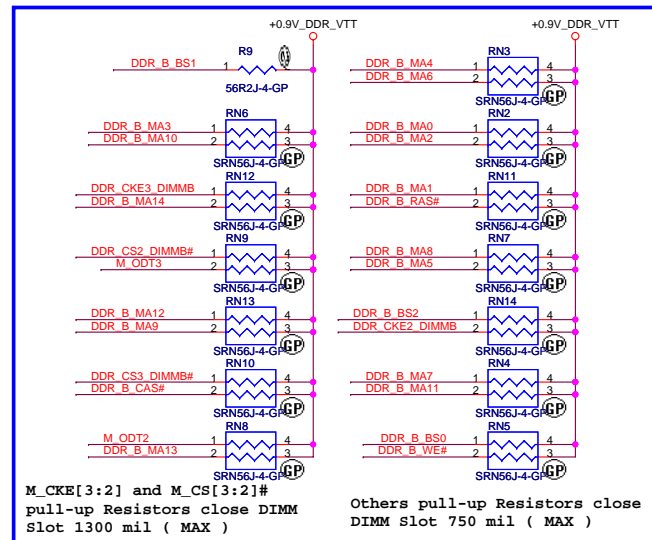
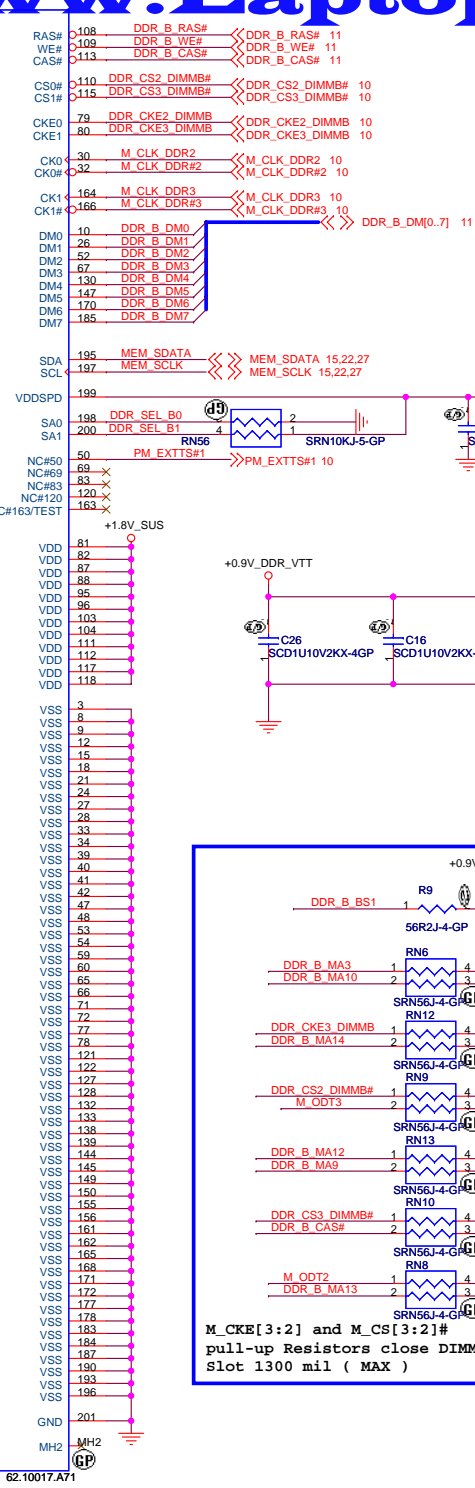
Title			
<b>Thurman UMA</b>			
Size	Document Number		Rev
<b>A3</b>	<b>GMCH-POWER/FILTER (5/6)</b>		<b>-1</b>
Date:	Thursday, November 22, 2007	Sheet 13 of	46







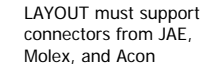




Others pull-up Resistors close  
DIMM Slot 750 mil ( MAX )

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>Thurman UMA</b>			
Size	Document Number	Rev	
<b>Custom</b>	<b>DDR2-SODIMM2</b>	<b>-1</b>	
Date: Wednesday, November 07, 2007		Sheet 16	of 46



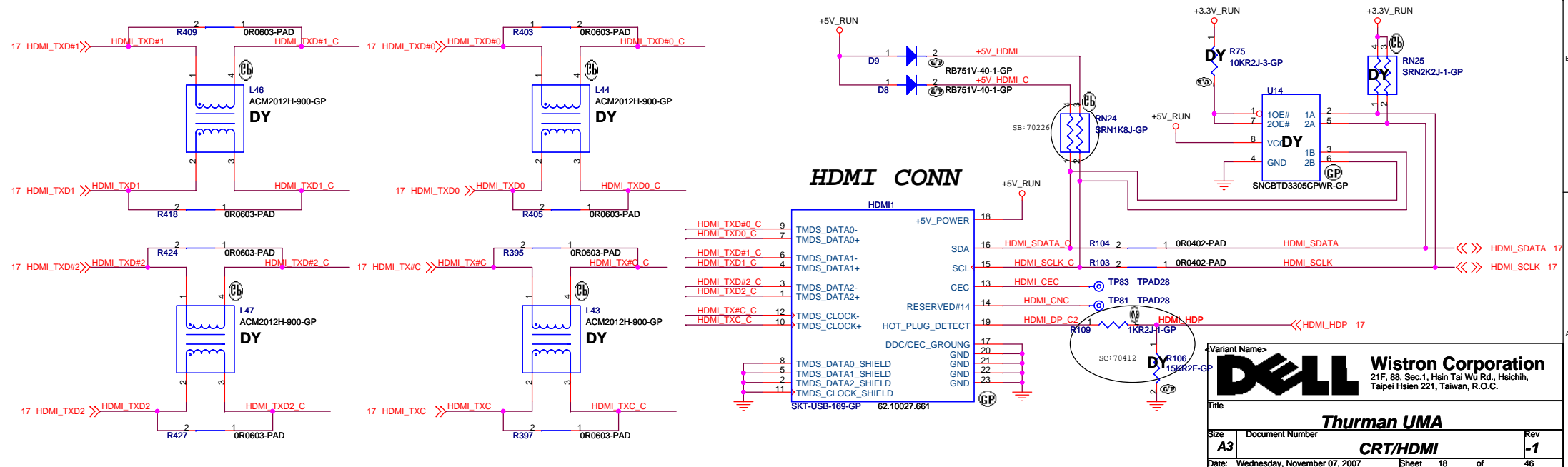
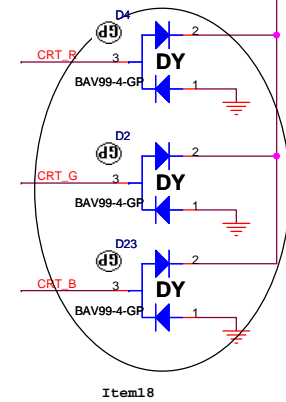
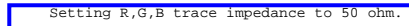
**<Variant Name>**



Rev

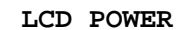
**-1**

Sheet 17 of 46





## INVERTER POWER



Title

**Thurman UMA**

Size

Document Number

**LVDS**

Date: Thursday, November 22, 2007

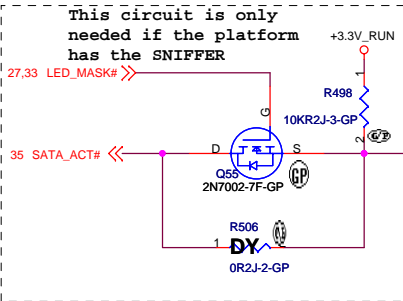
Sheet 19 of 46

Re

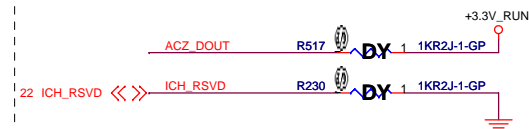
We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

## ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCl1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable

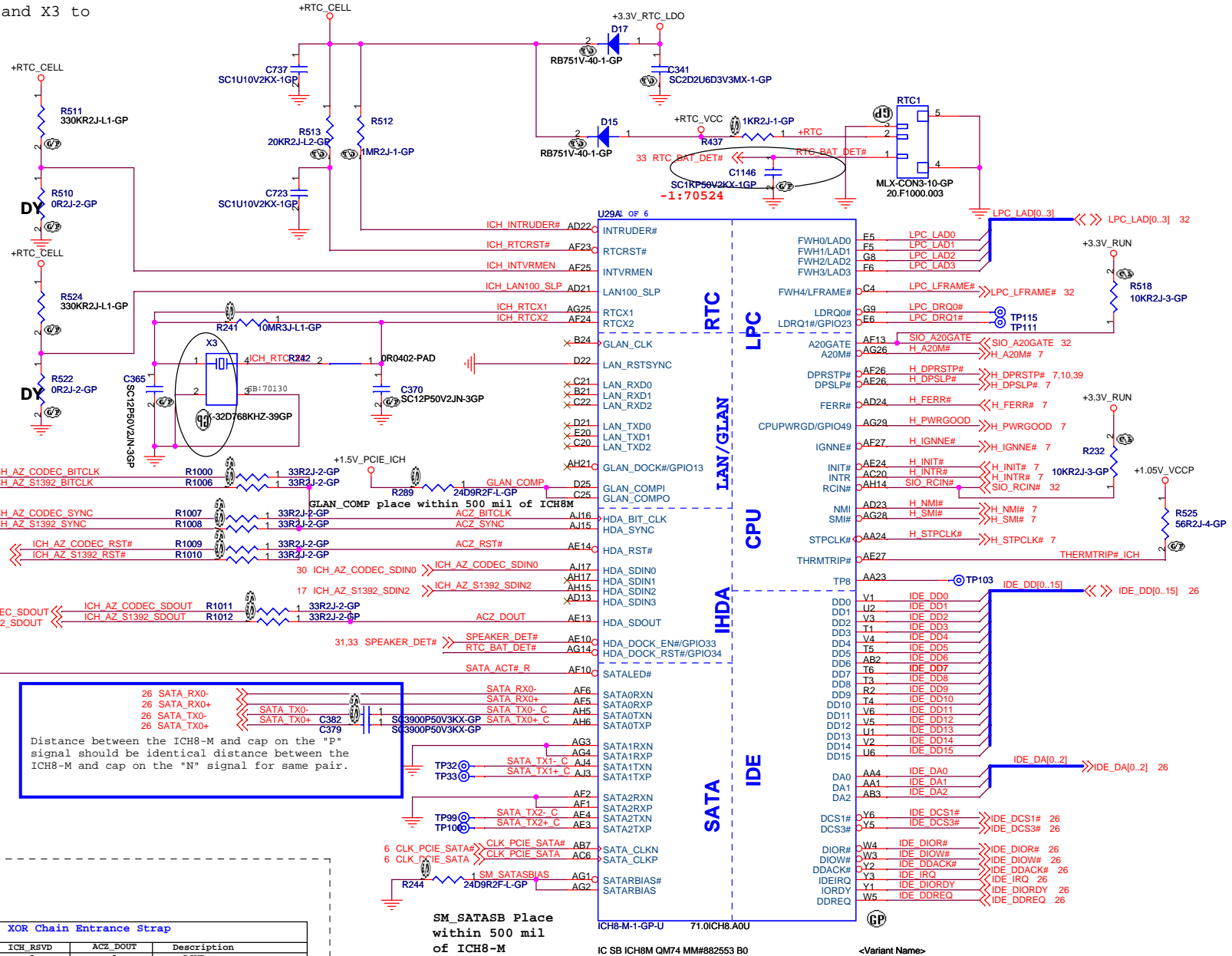


## ICH8-Strap PIN



XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
1	0	Enter XOR Chain
1	1	Normal Operation(default)
1	1	Set PCIE port cofig bit1

## RTC circuitry



SM\_SATASB Place within 500 mil of ICH8-M

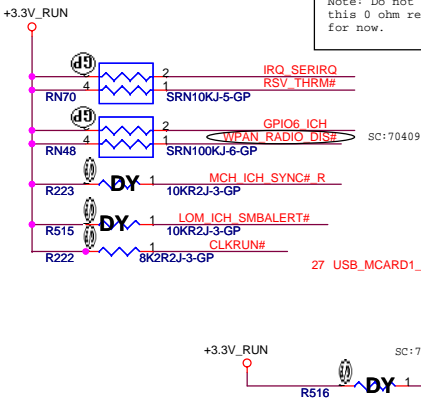
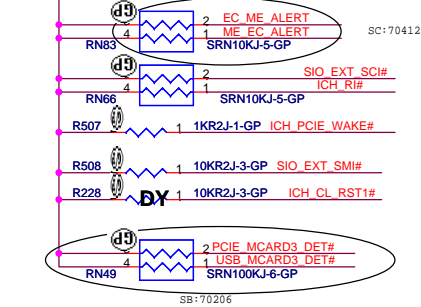
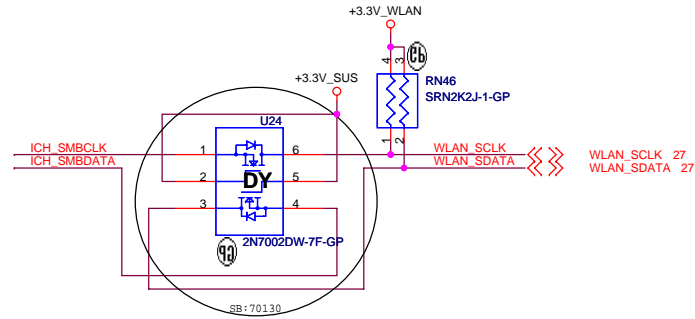
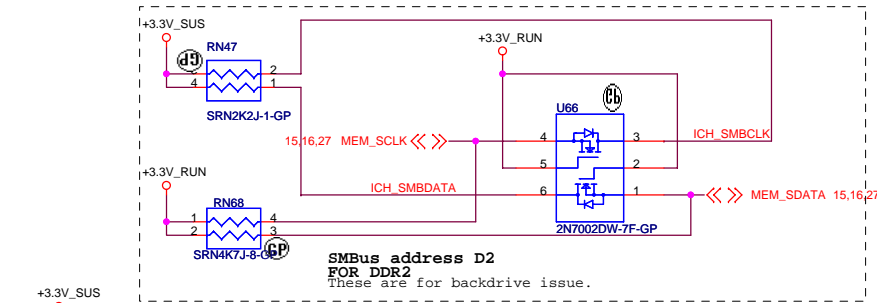
<Variant Name>

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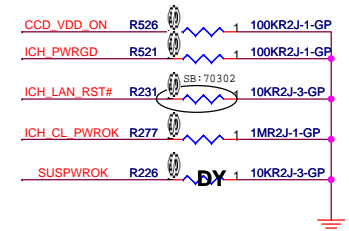
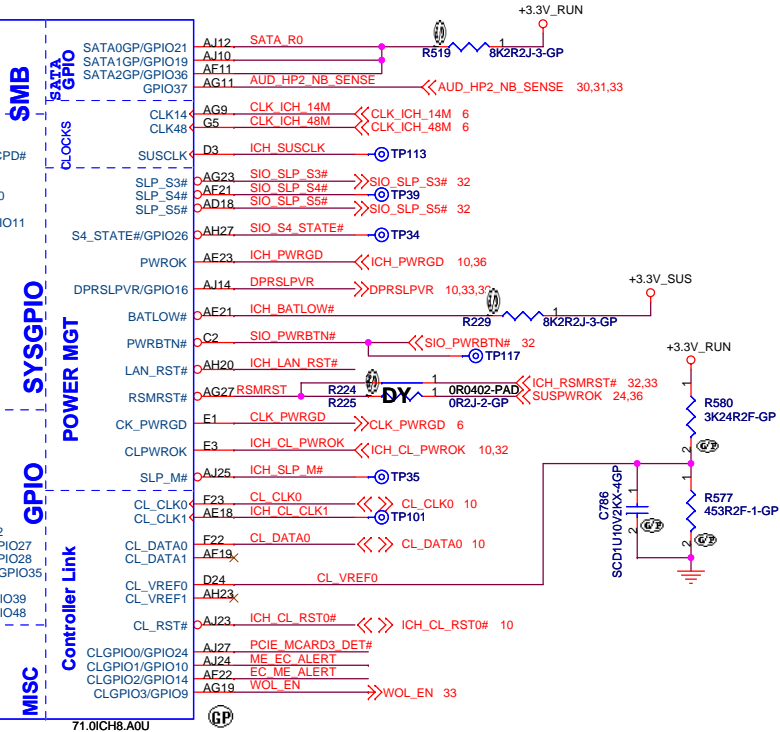
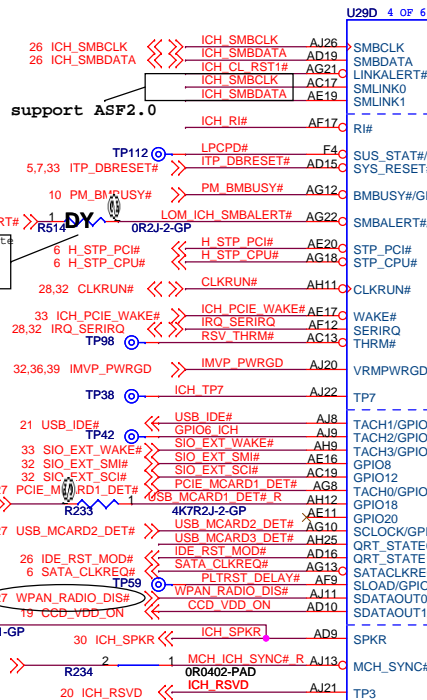
Title		
Thurman UMA		
Size	Document Number	Rev
A3	ICH8M-RTC/IDE/LPC/DHI (1/4)	-1
Date:	Thursday, November 22, 2007	Sheet 20 of 46



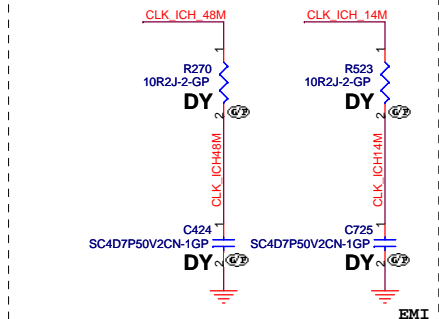




Note: Do not Populate this 0 ohm resistor for now.

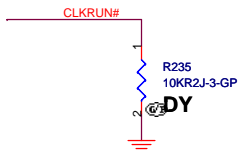


CLK\_ICH\_48M and CLK\_ICH\_14M EMI Mode  
Place close to ICH8-M



# ICH8-Strap PIN

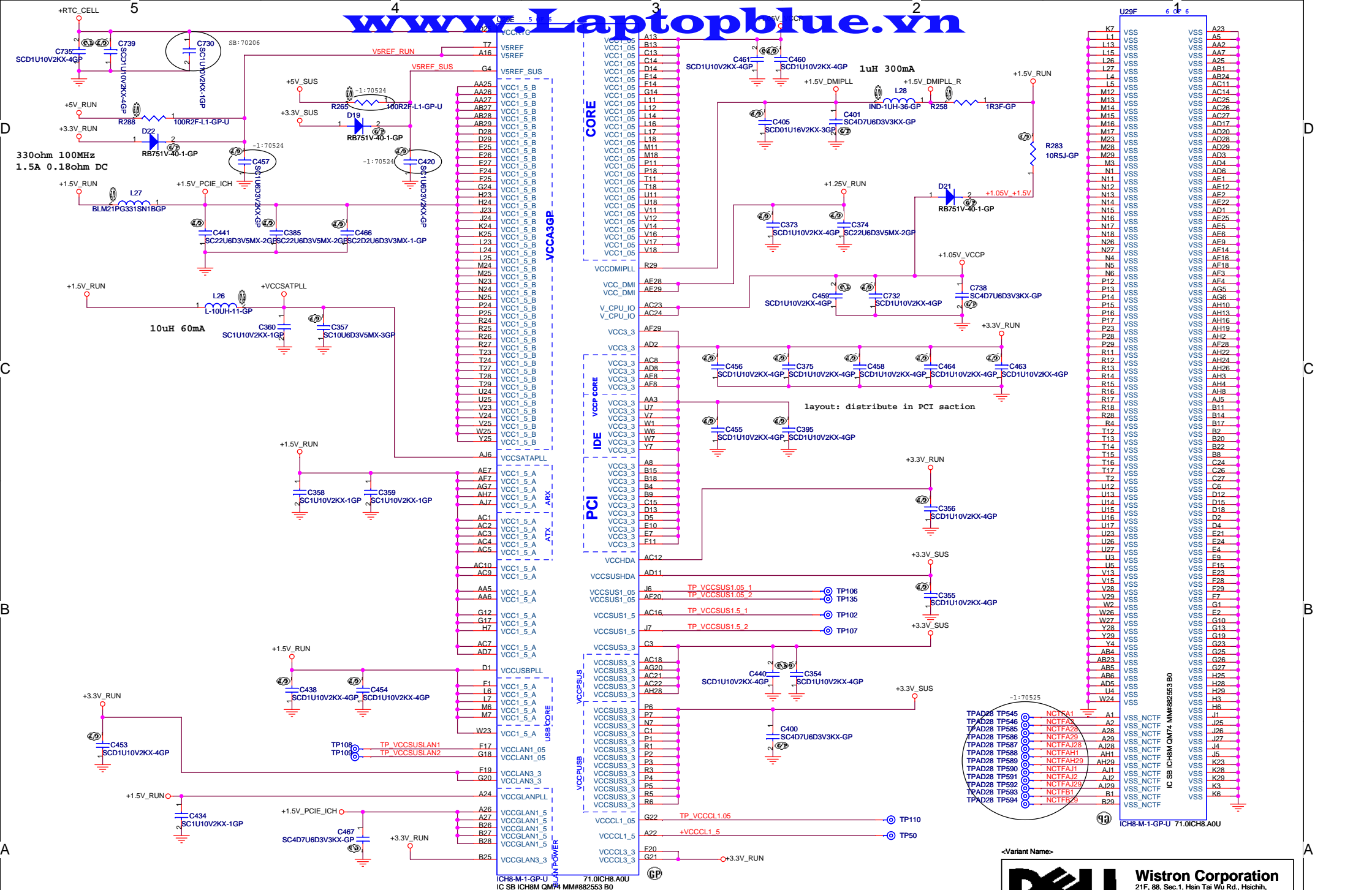
No Reboot Strap
ICH_SPKR LOW = Defaule
High=No Reboot



<Variant Name>







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Title			
<b>Thurman UMA</b>			
Size	Document Number	Rev	
<b>Custom</b>	<b>ICH8M-POWER (4/4)</b>	<b>-1</b>	
Date: Wednesday, November 07, 2007	Sheet 23	of	46

SSID = THERMAL

www.Laptopblue.com

REM\_DIODE1\_N and REM\_DIODE1\_P  
routing Trace width and Spacing  
use 10 / 10 mil

Place inside CPU socket

C300 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

H\_THERMDA and H\_THERMDC  
routing Trace width and  
Spacing use 10 / 10 mil

C295 Please close to Guardian

REM\_DIODE4\_N and REM\_DIODE4\_P  
routing Trace width and Spacing  
use 10 / 10 mil

Thermal sensor for Mini Card  
should be placed TOP Side under WWAN CARD

C260 Please Close to Guardian

Note :

$VSET = (T_p - 70) / 21$   
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$   
Where  $T_p = 70$  to 101 degrees C  
 $T_p$  set at 88 degrees C  
Guardian temp tolerance = +/- 3 degrees C

Version B: 74.04001.A73

CPU THERMALTRIP

MCH THERMALTRIP

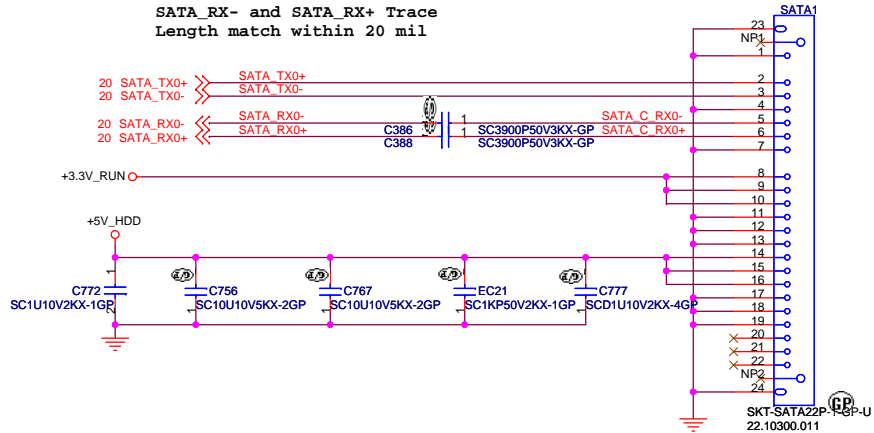
C916, C459, C472 Please Close to Guardian



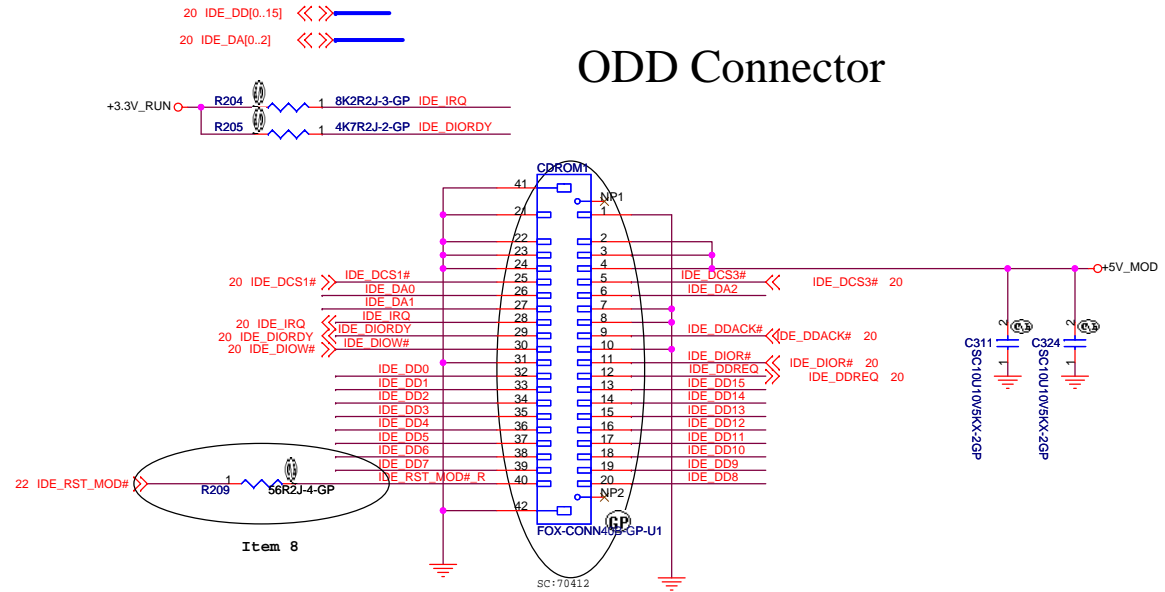
SSID = IDE & SATA

## SATA HDD Connector

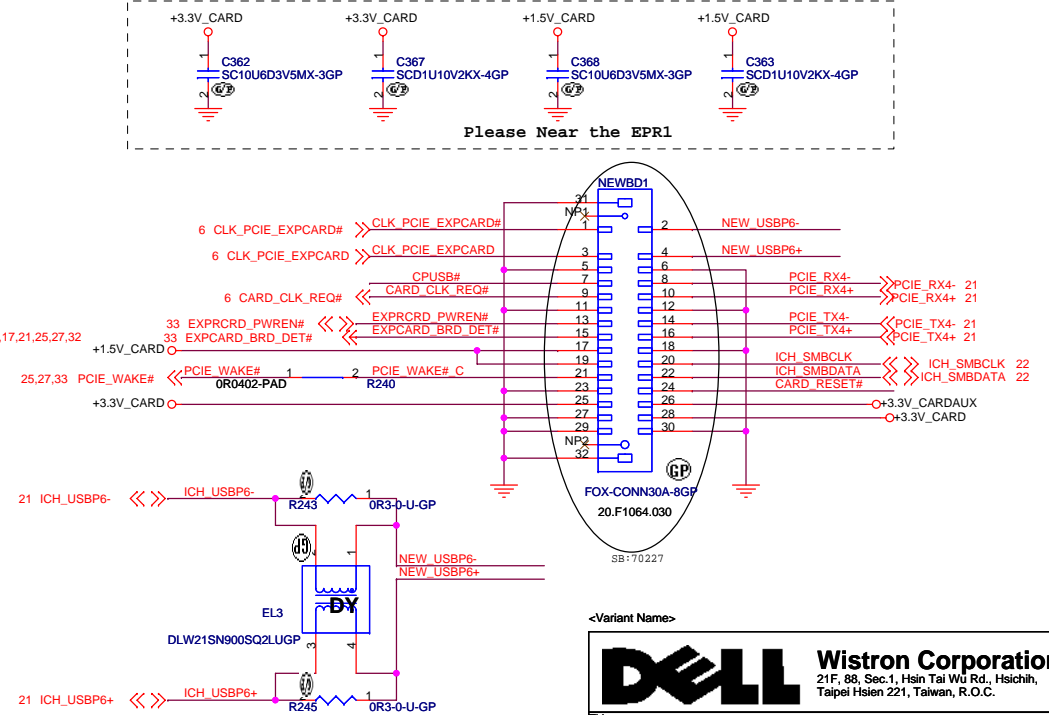
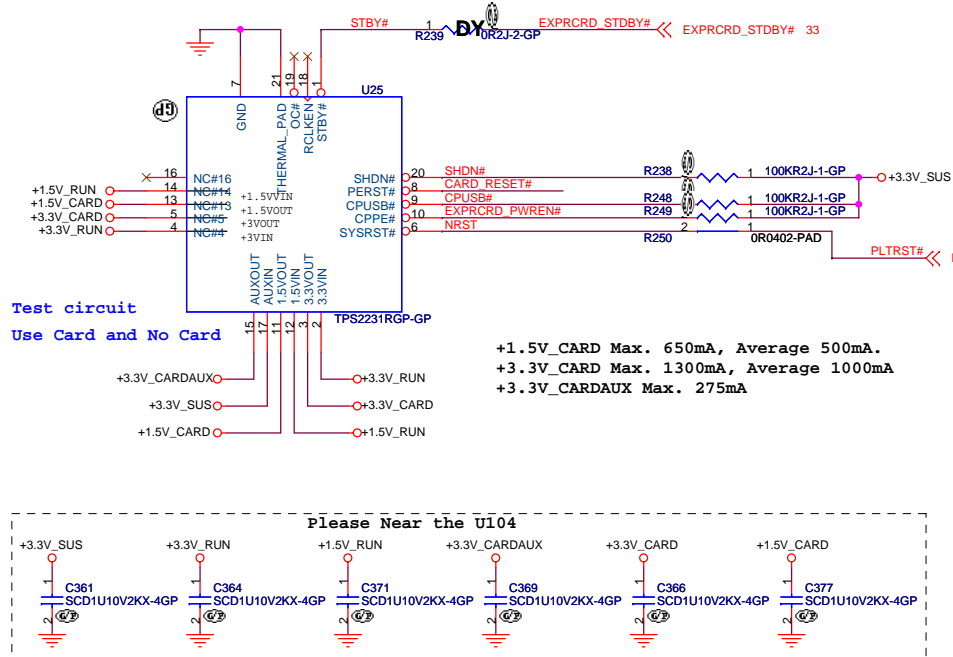
SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil



## ODD Connector

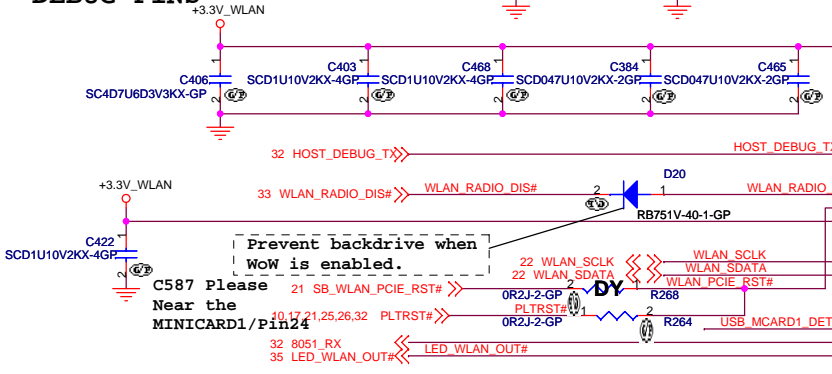


## Express Card

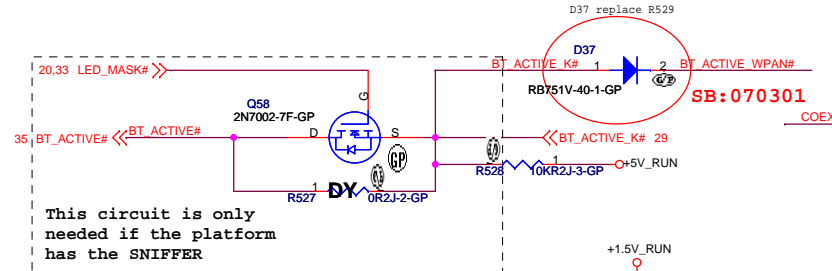
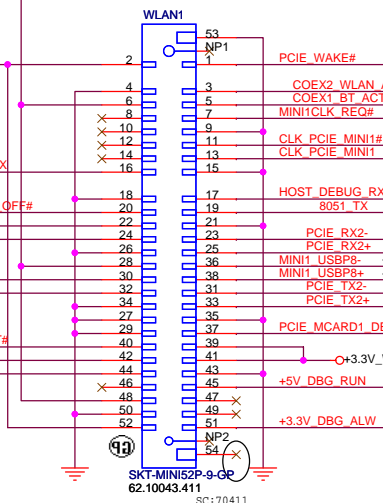


JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

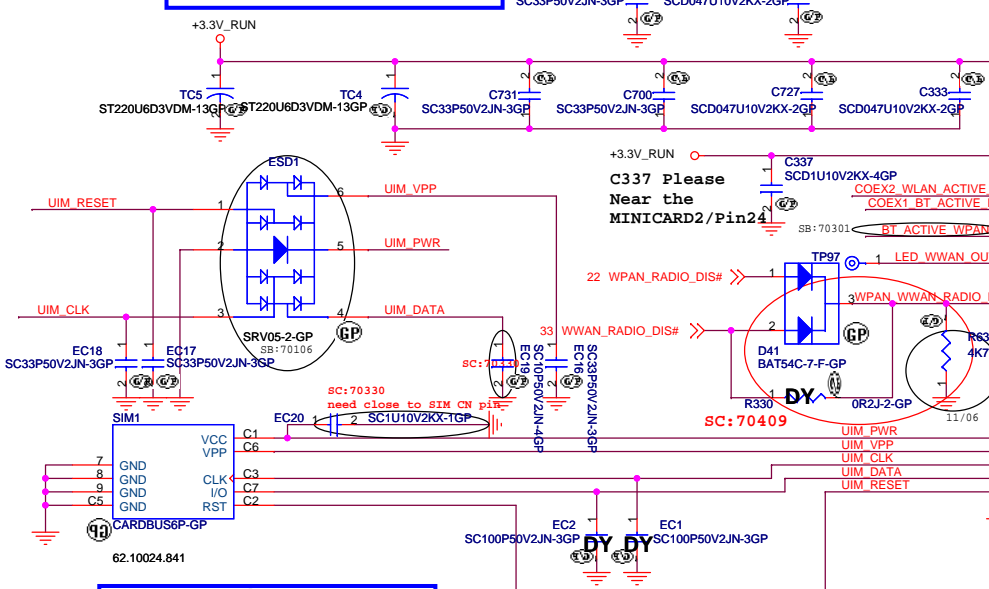
## DEBUG PINS



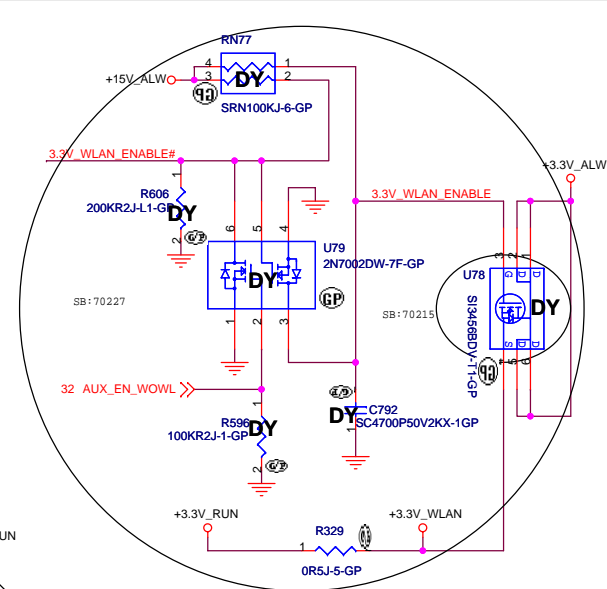
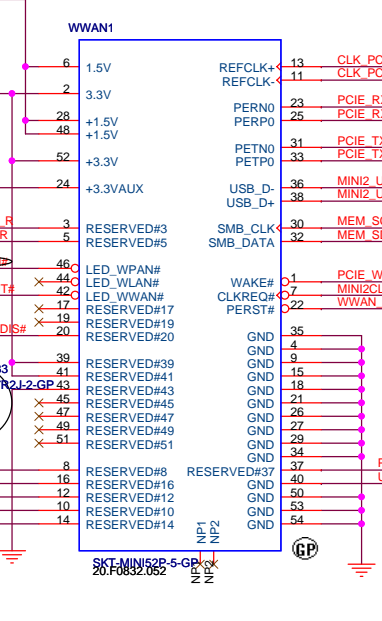
## MiniCard WLAN connector



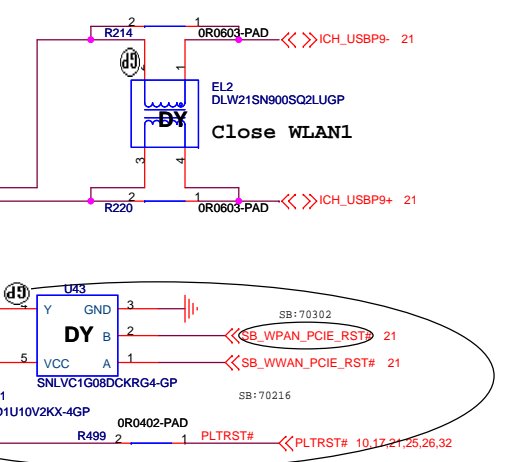
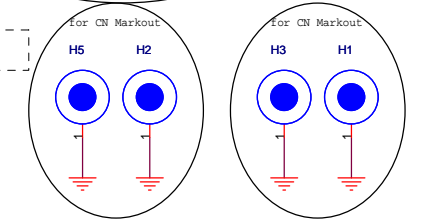
Layout note: Place caps EC10-EC14 close Mini Card connector.



## MiniCard WWAN connector



For Debug card used only.



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Title: **Thurman UMA**

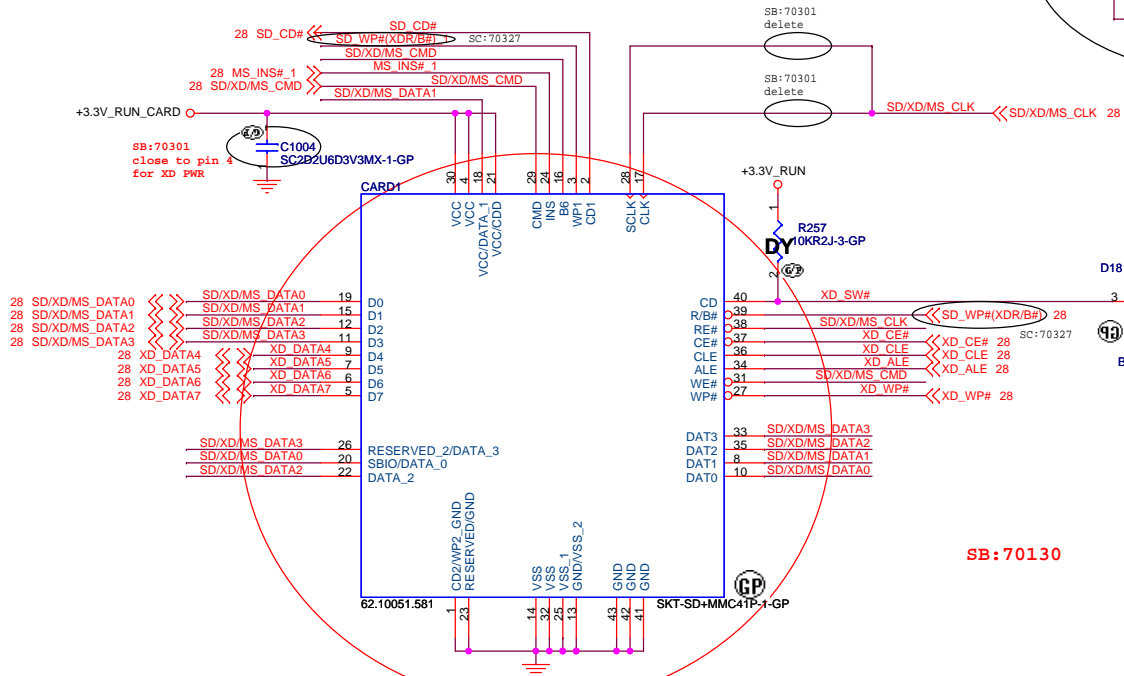
Size: **A3** Document Number: **MINICARD/WLAN/WWAN** Rev: **-1**

Date: Wednesday, November 07, 2007 Sheet 27 of 46



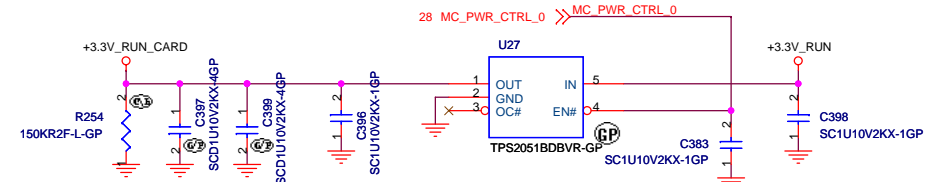
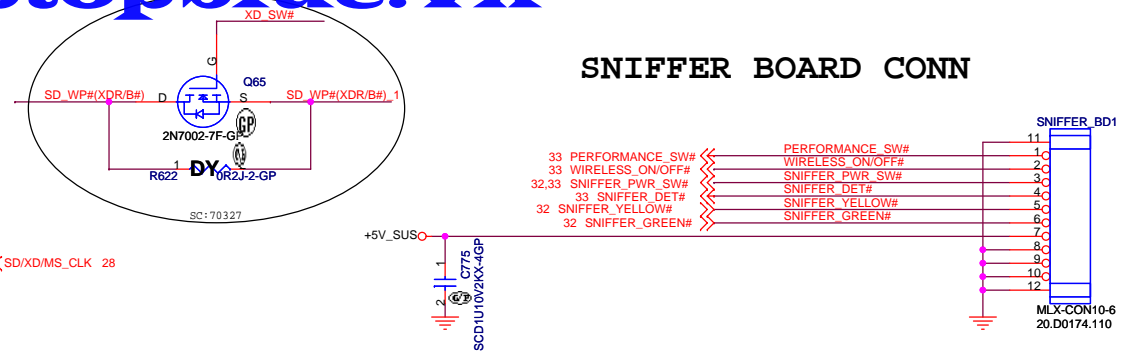


## Card Reader CONN

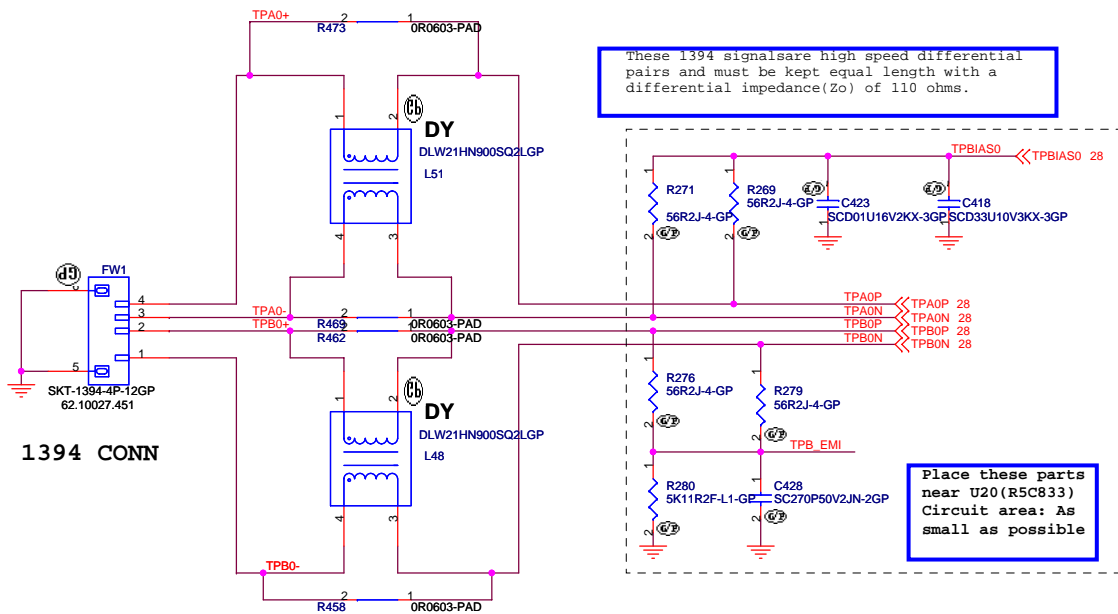


SB:70130

SNIFFER BOARD CONN



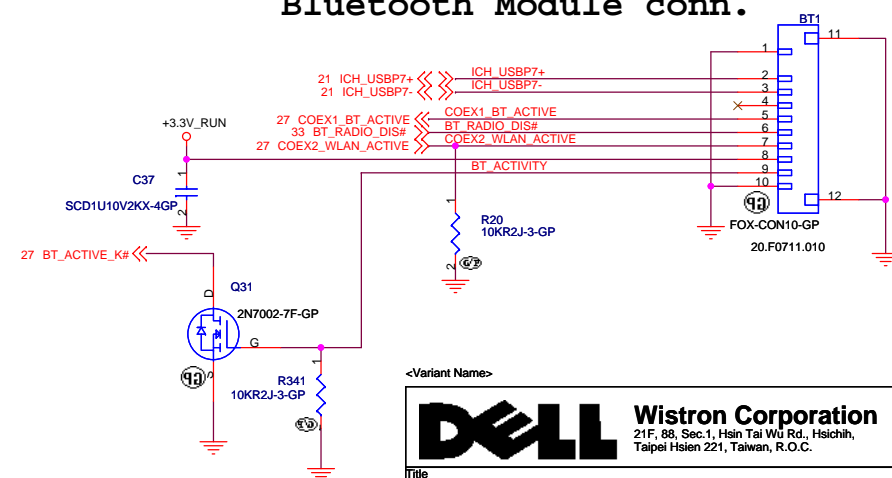
## 1394 CONN



These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance ( $Z_0$ ) of 110 ohms.

Place these parts  
near U20(R5C833)  
Circuit area: As  
small as possible

## Bluetooth Module conn.



<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thurman UMA**

Size

Document Number
-----------------

**8in1 /1394/SNIFFER BD CON/BT**

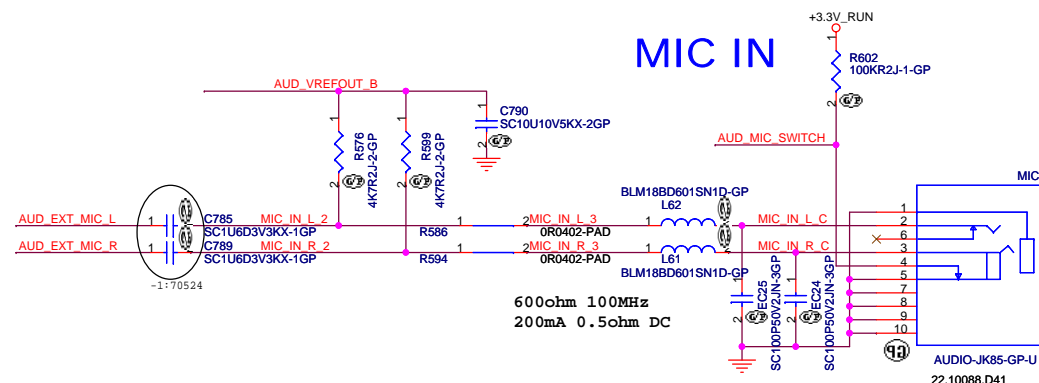
Rev

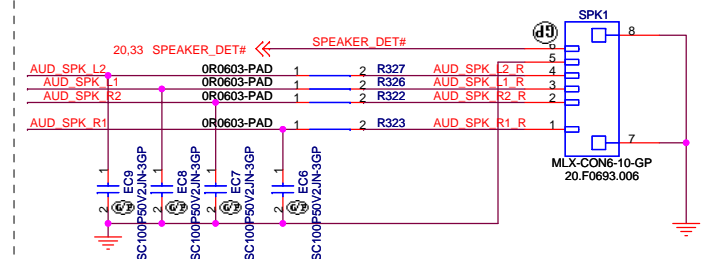
Date: Wednesday, November 07, 2007

Sheet 2

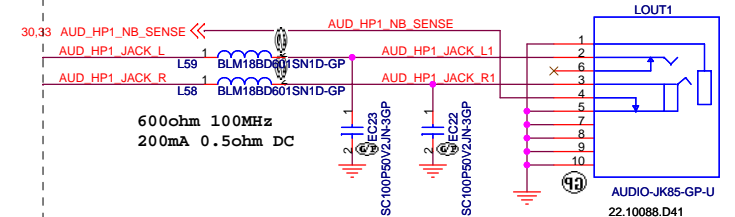
46



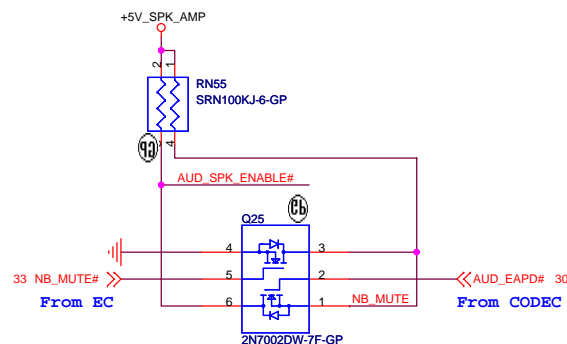




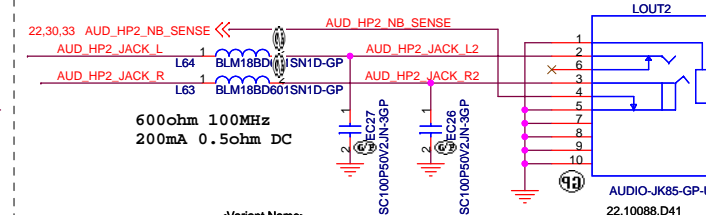
LINE1 OUT



## Signal inverter for speaker shutdown



### AND Gate for HP Mute Function



<Variant Name>

DELL

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Title

**Thurman UMA**

Size

Document Number

## AUDIO AMP

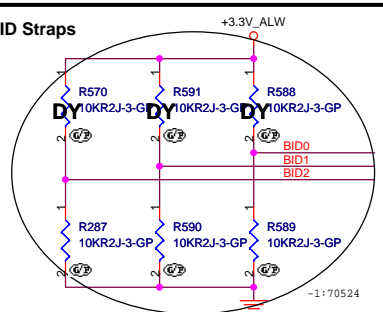
Date: Wednesday, November 07, 2007

Sheet 31 of 46



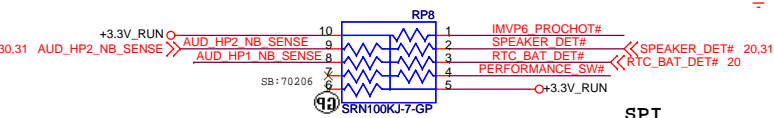
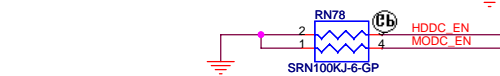
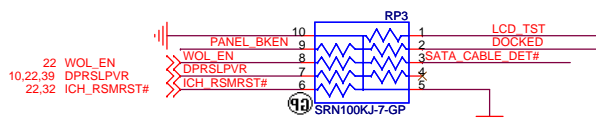
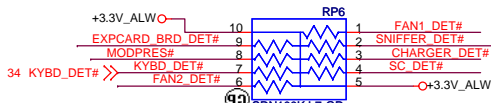
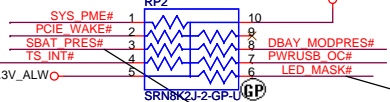
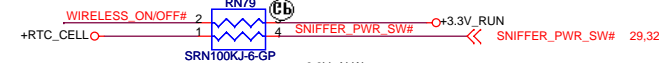
Title			
<b>Thurman UMA</b>			
Size	Document Number	Rev	
<b>A3</b>	<b>KBC MEC5025/DEBUG CONN</b>	<b>-1</b>	
Date:	Wednesday, November 07, 2007	Sheet	32 of 46

# Board ID Straps



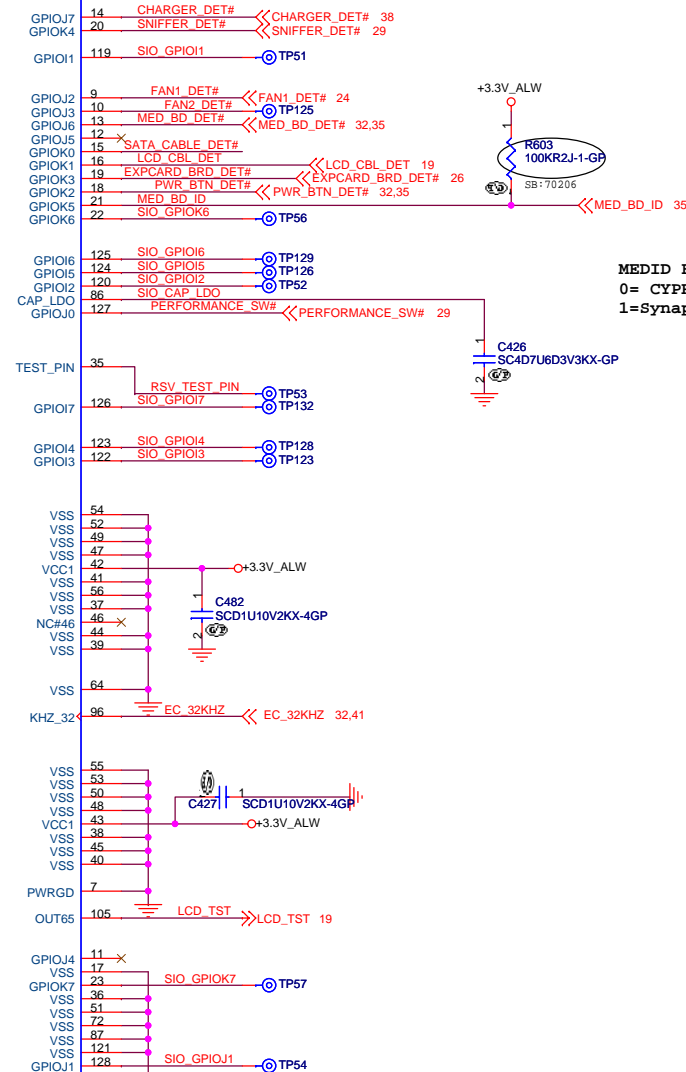
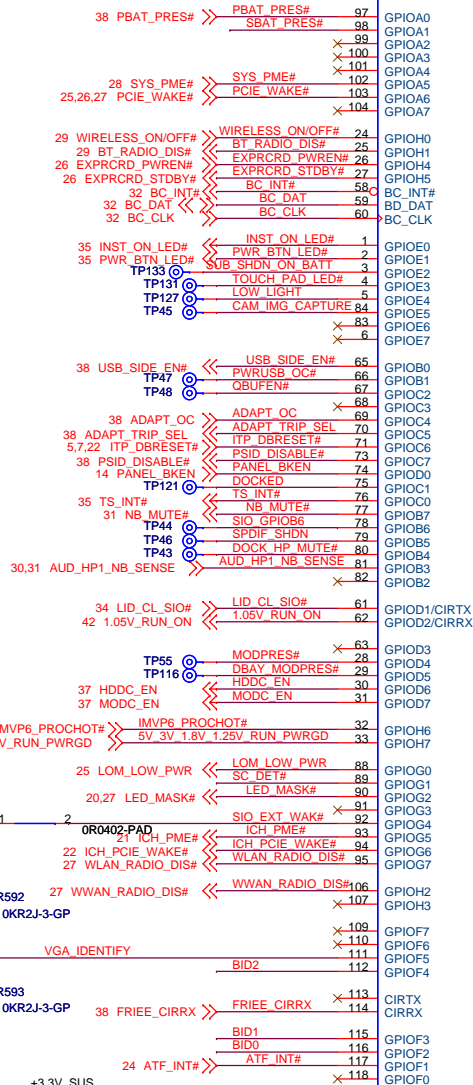
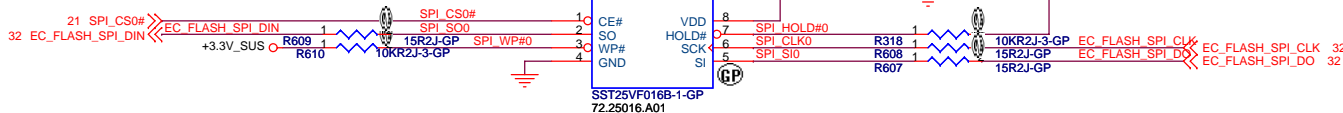
BID1	BID0	Board Rev.
0	0	ENG1 (M00)
0	1	ENG2 (X00)
1	0	ENG3 (X01)
1	1	ENG4 (X02)
0	0	RAMP (A00)

BID2:  
0: Intel CPU + Intel Chipset  
1: Intel CPU + ATI Chipset



VGA IDENTITY  
1= Discrete GFX  
0=UMA

## SPI



MEDID BD ID  
0= CYPRESS  
1=Synaptics

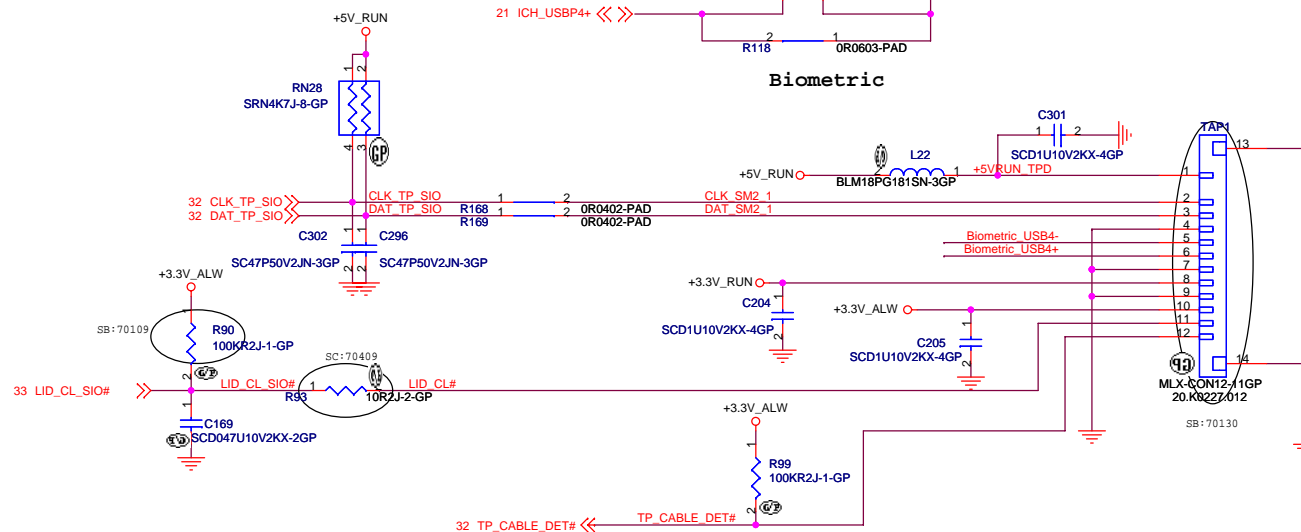
<Variant Name>

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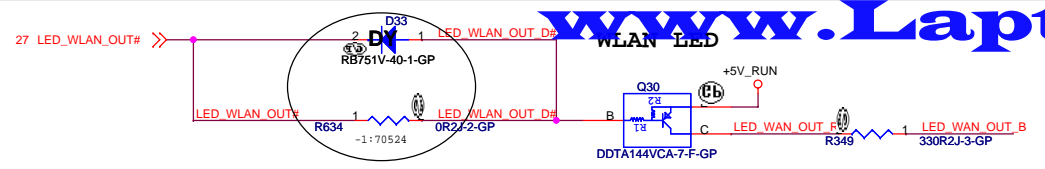
Title: **Thurman UMA**

Size: **A3** Document Number: **SIO ECE5011/SPI ROM** Rev: **-1**

Date: Wednesday, November 07, 2007 Sheet 33 of 46



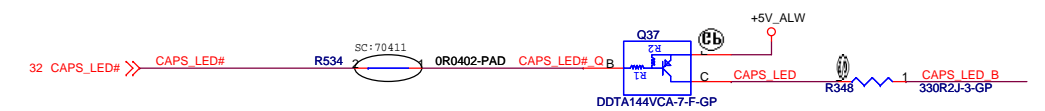




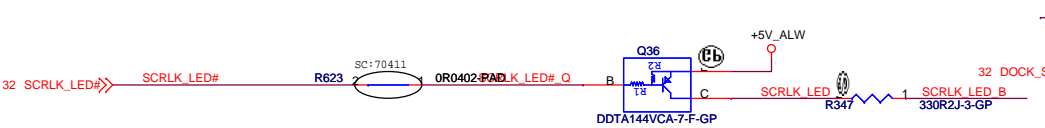
Bluetooth LED



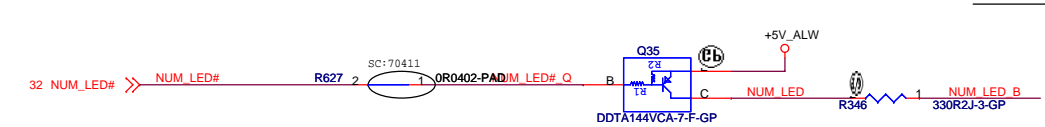
CAPS LED



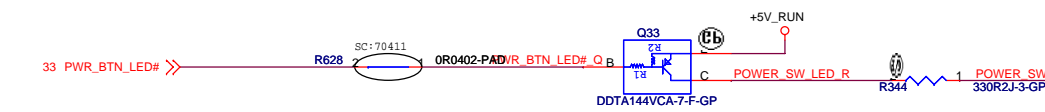
SCRLK LED



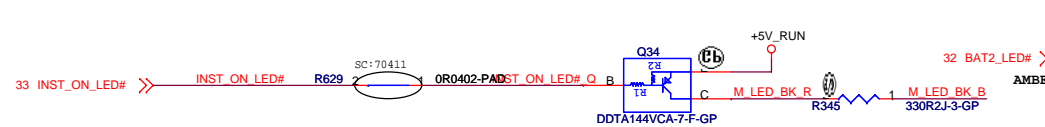
NUM LED



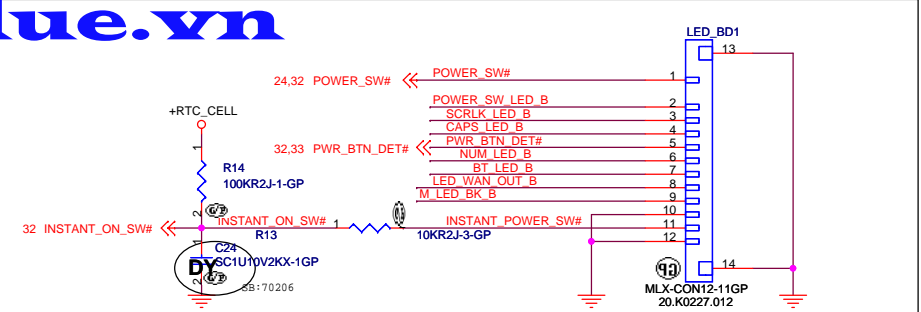
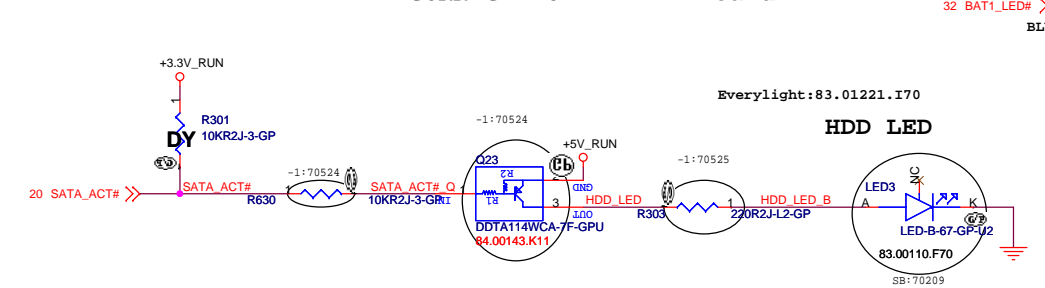
POWER BUTTON LED



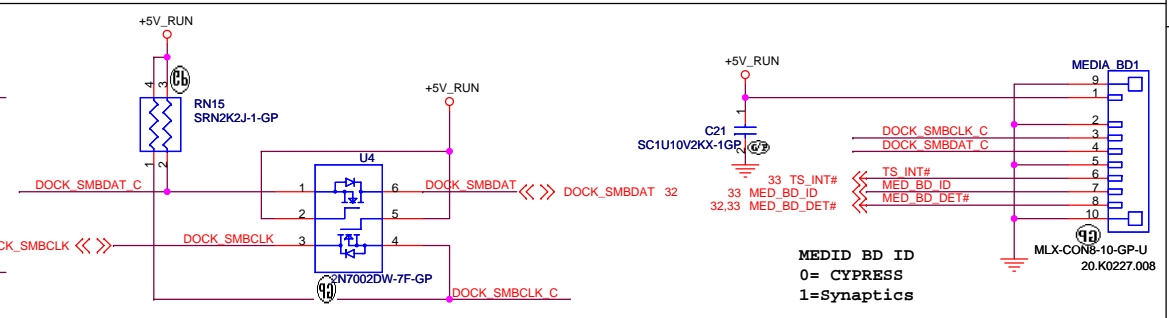
INSTANT POWER BUTTON LED



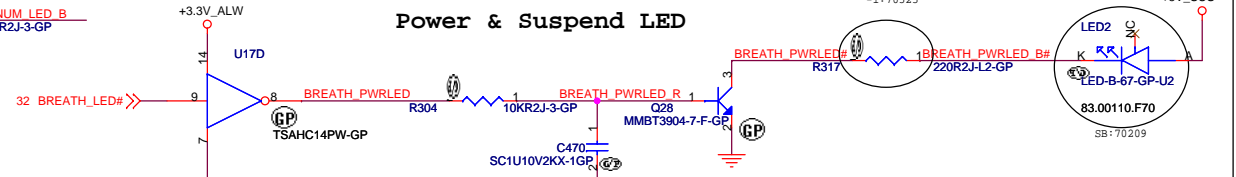
CONNECT TO THE LED Board



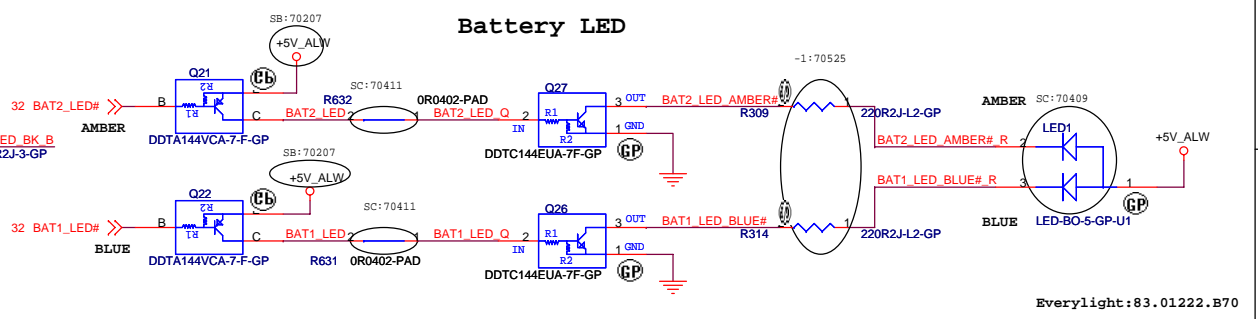
TO LED Board CONN



Power & Suspend LED



Battery LED



LED Placement

POWER	HDD	BATTERY
LED1	LED2	LED3

Variant Name:

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Title

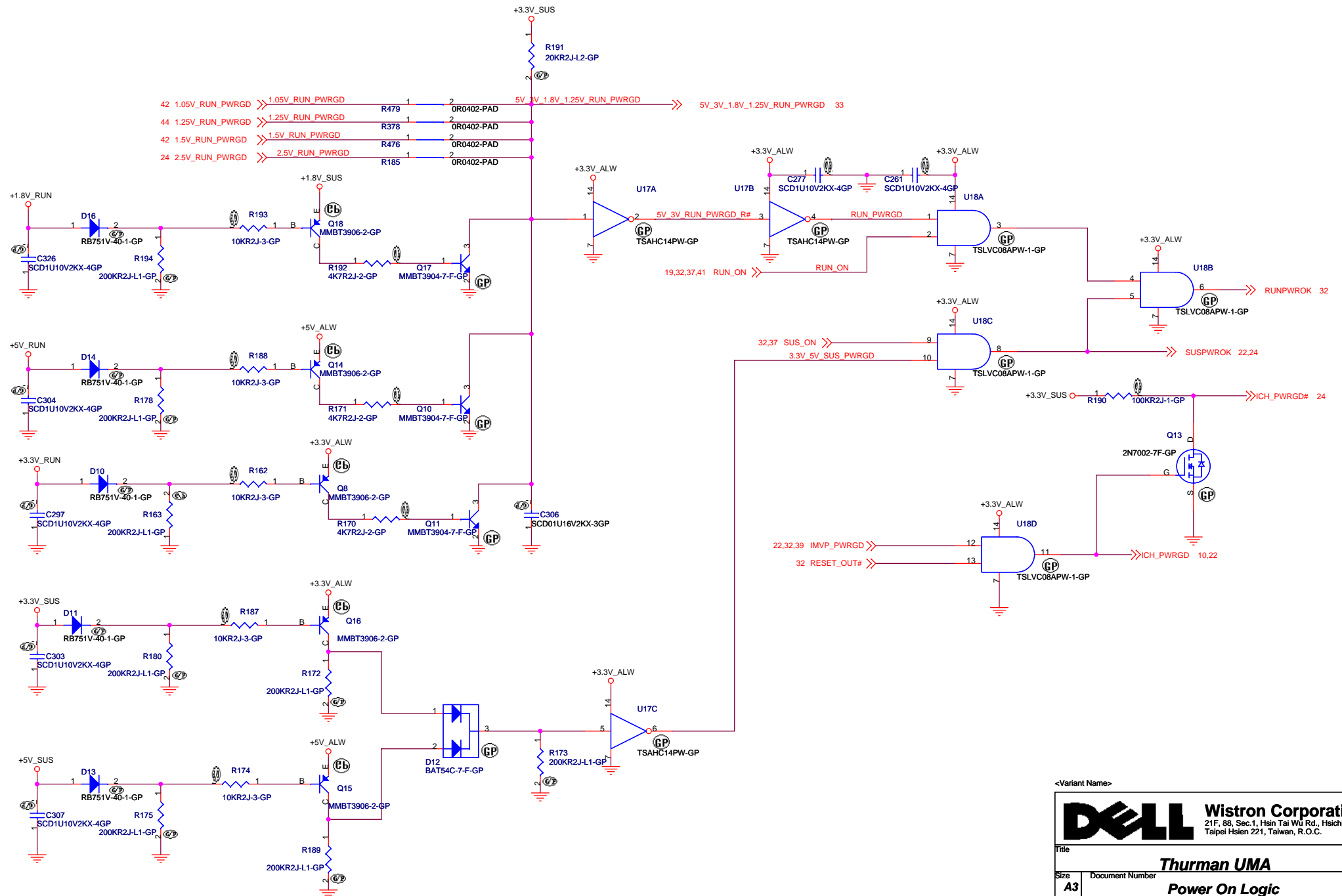
Thurman UMA

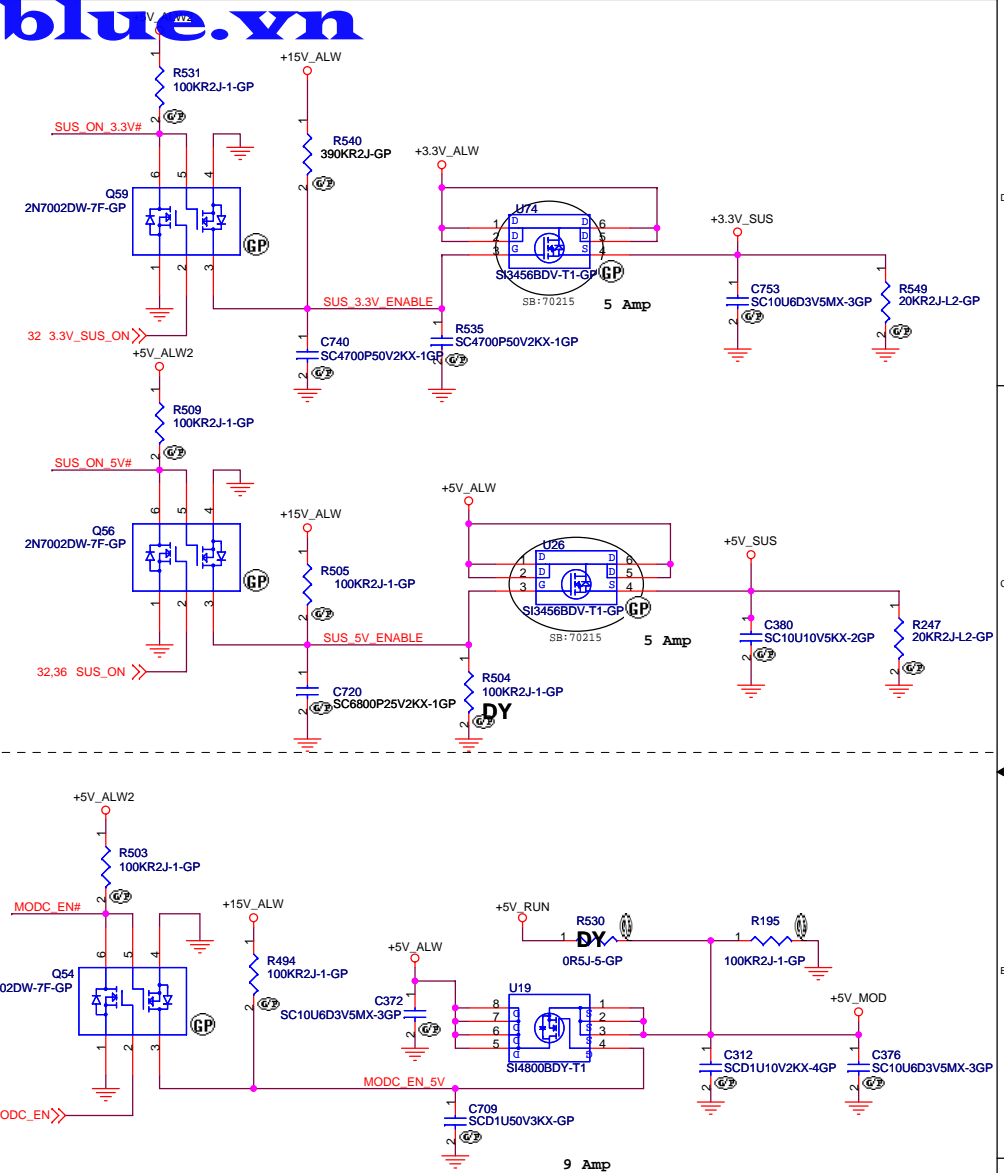
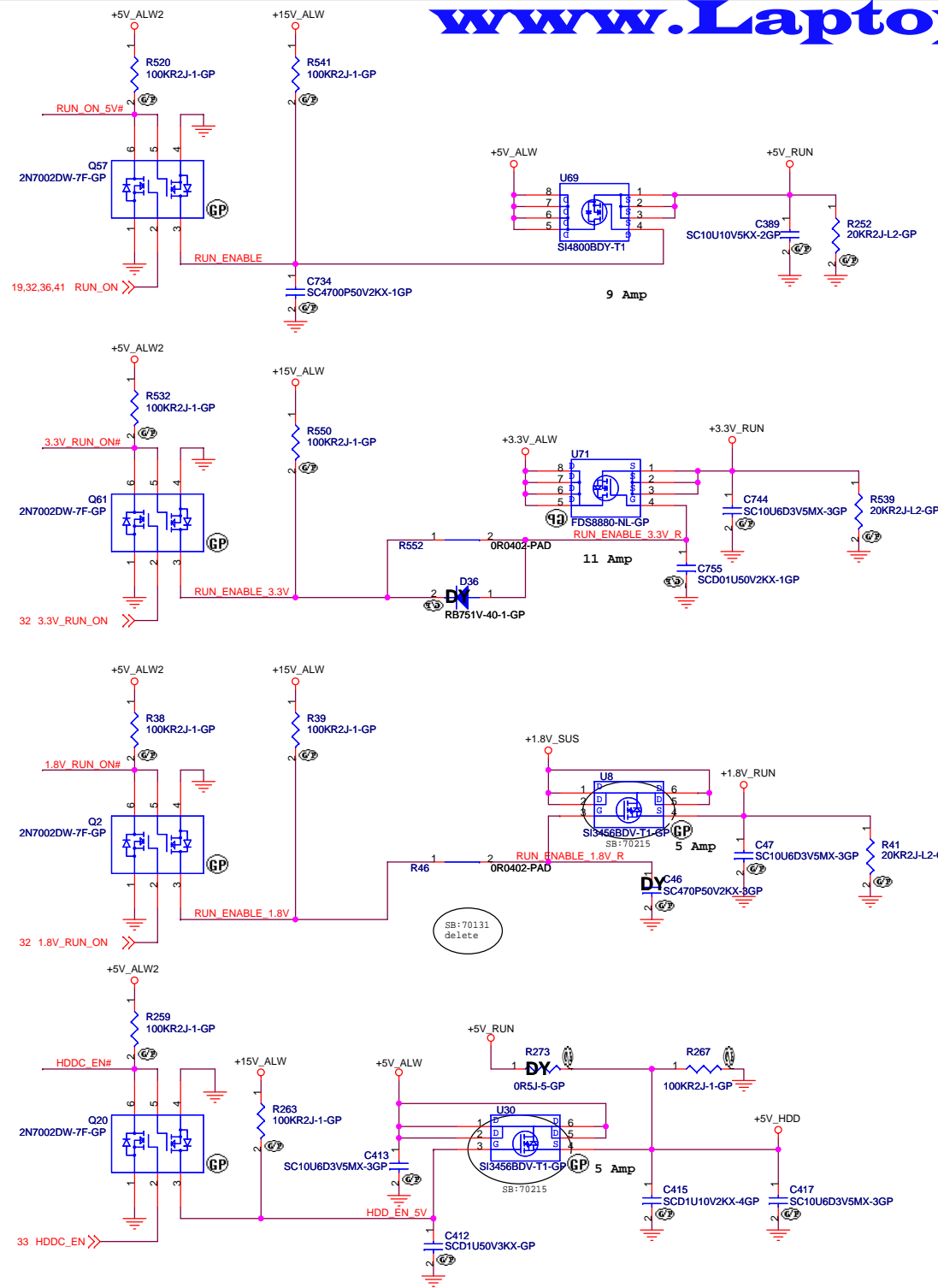
Size A3 Document Number

LED BD/Capacity Button BD

Date: Wednesday, November 07, 2007 Sheet 35 of 46

Rev -1

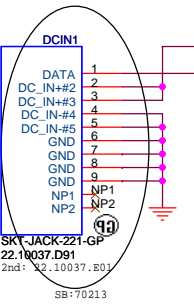
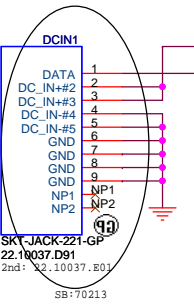
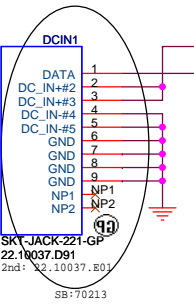
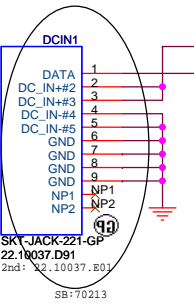
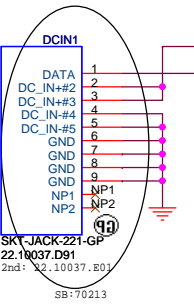
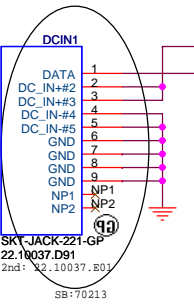
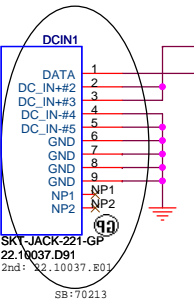
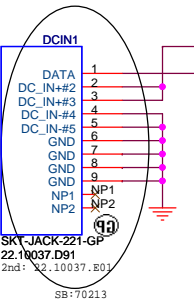
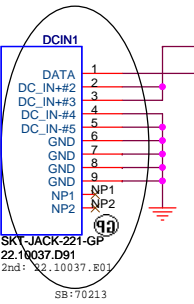
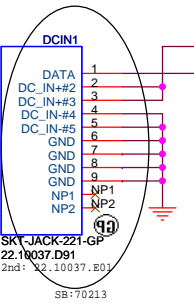
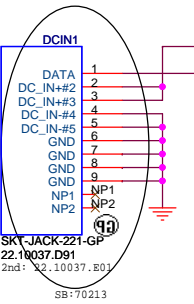
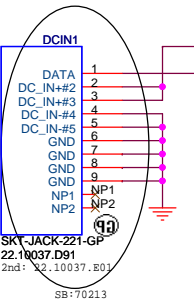
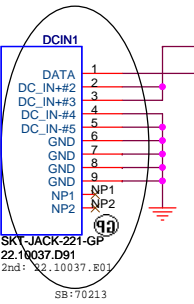
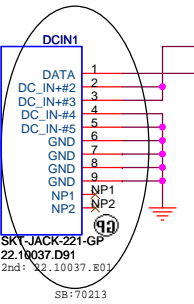
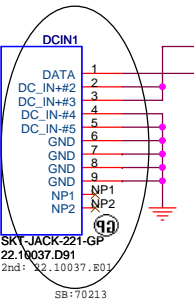
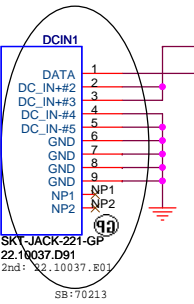
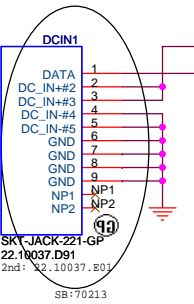
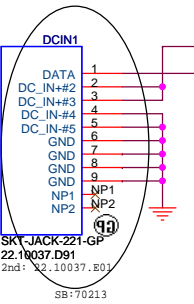
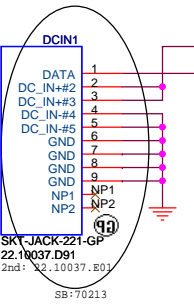
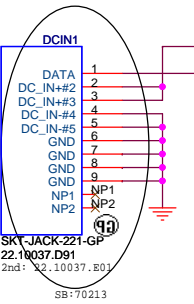
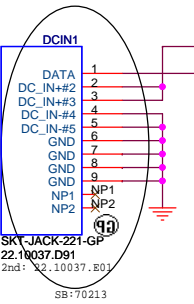
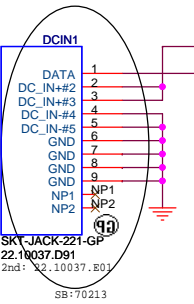
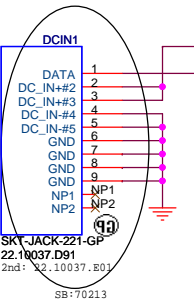
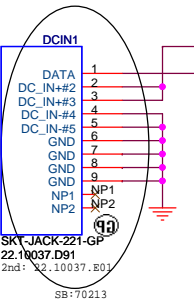
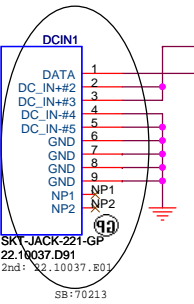
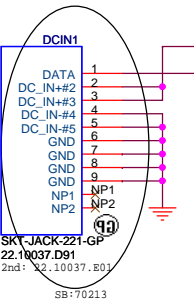
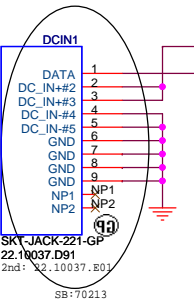
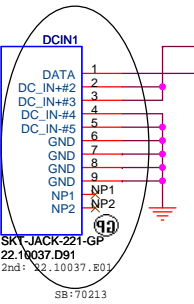
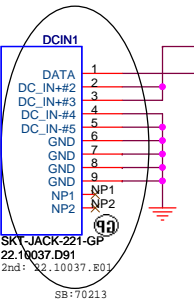
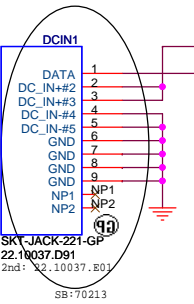
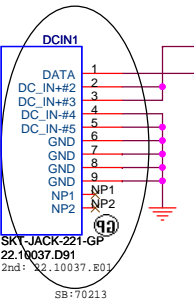
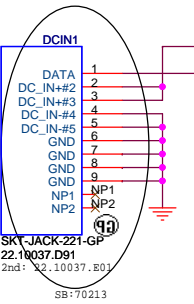
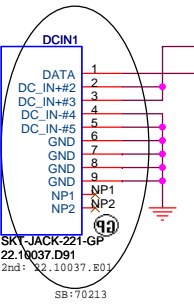
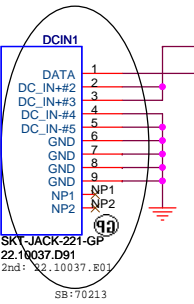
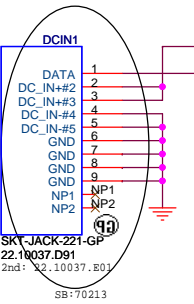
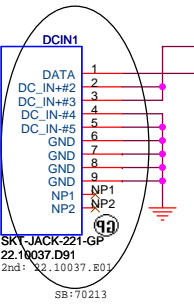
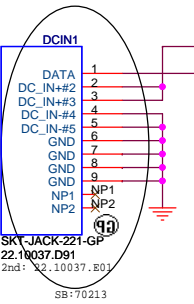
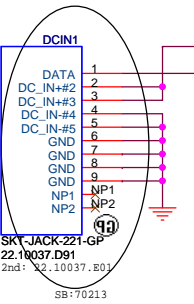
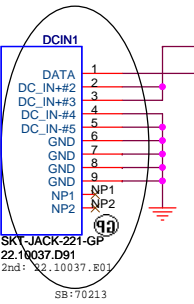
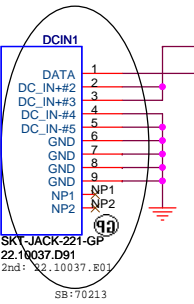
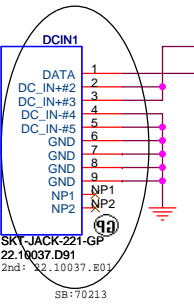
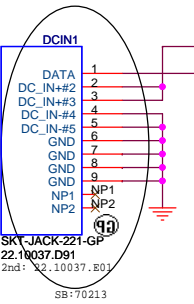
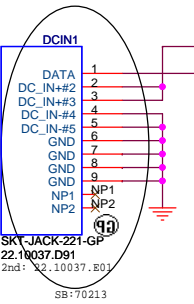
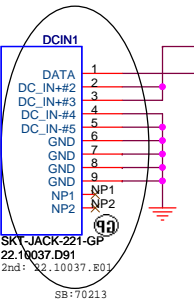
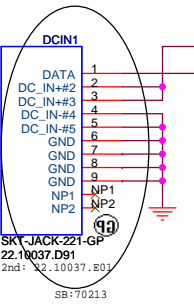
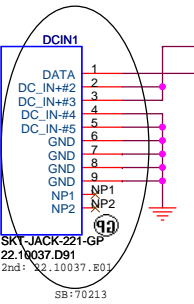
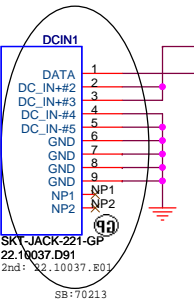
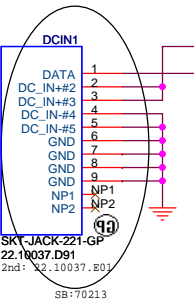
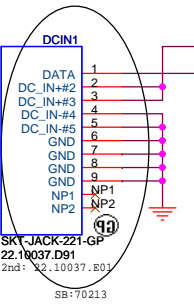
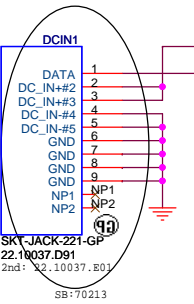
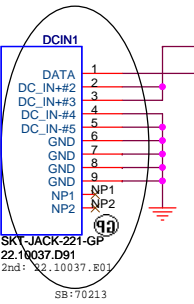
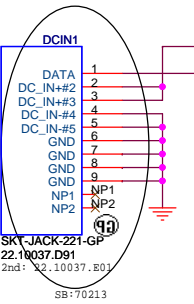
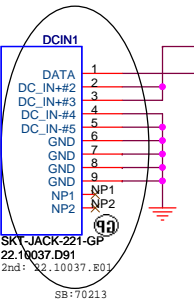
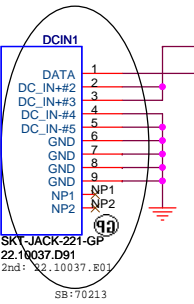
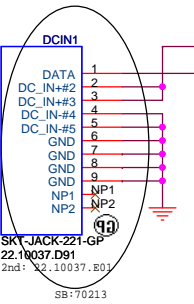
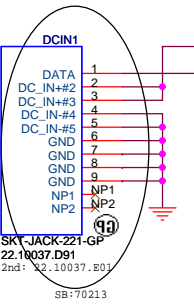
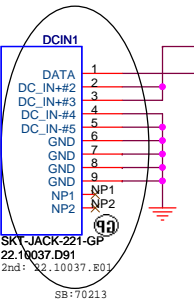
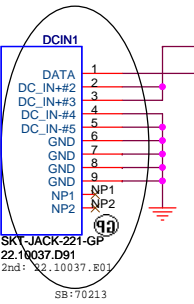
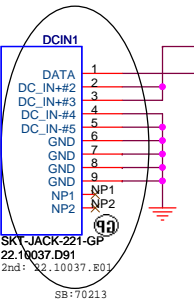
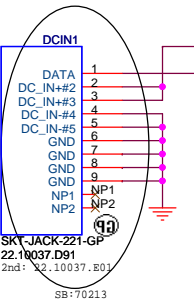
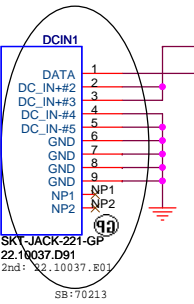
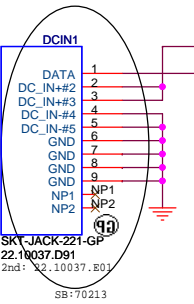
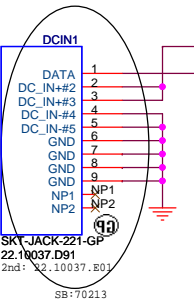
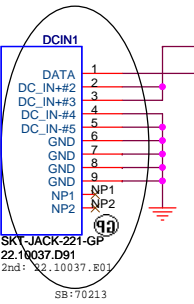
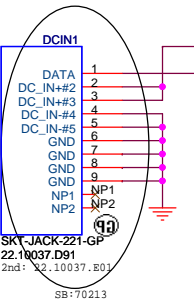
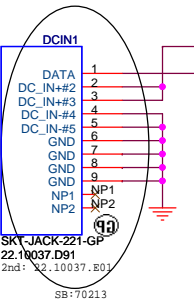
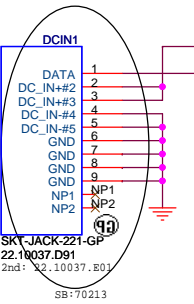
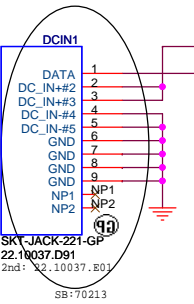
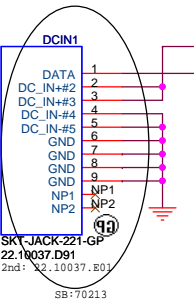
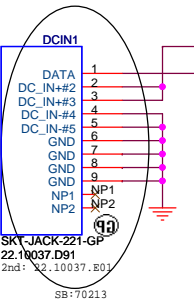
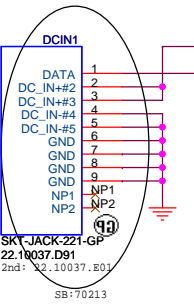
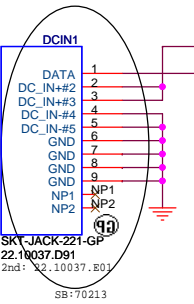
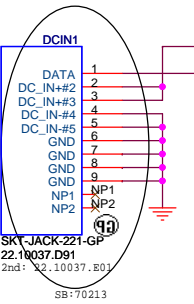
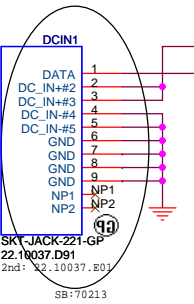
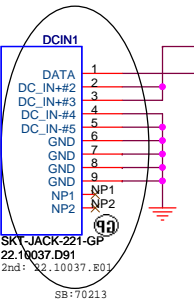
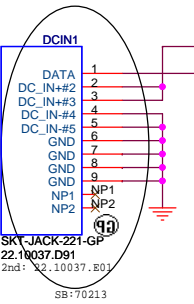
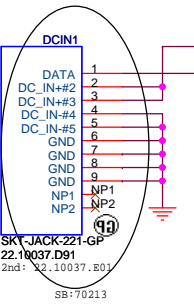
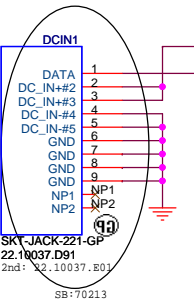
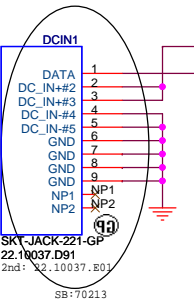
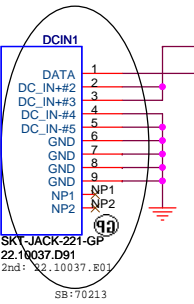
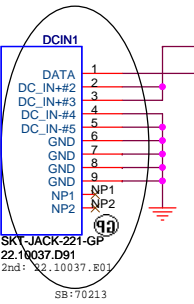
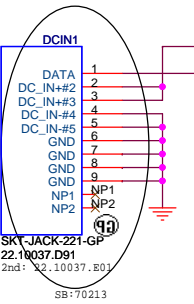
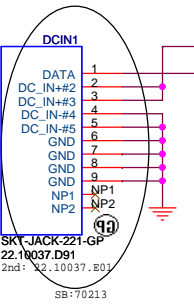
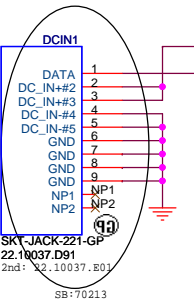
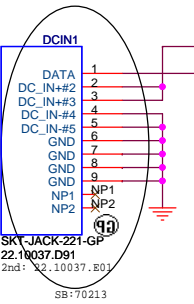
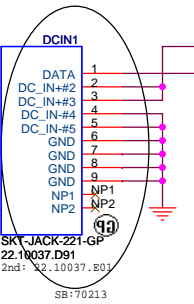
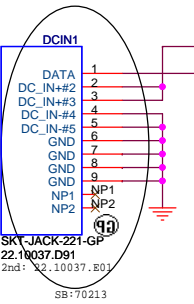
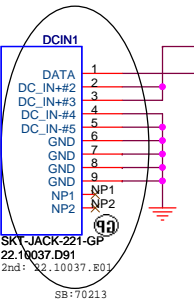
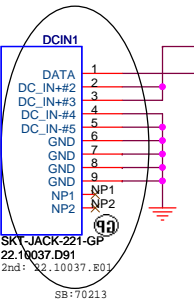
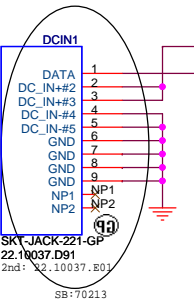
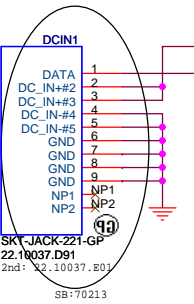
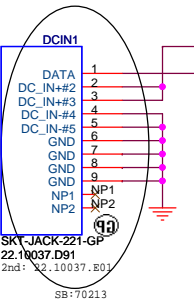
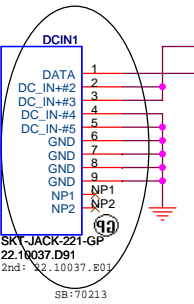
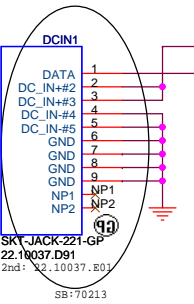
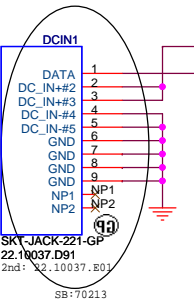
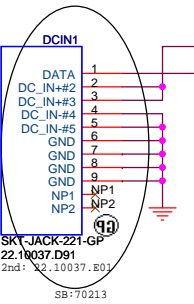
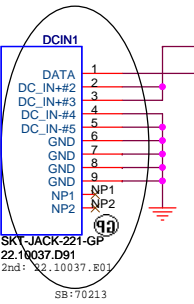
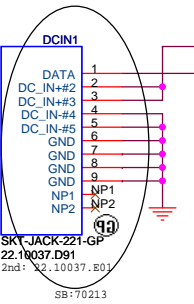
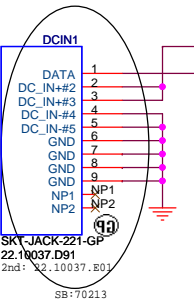
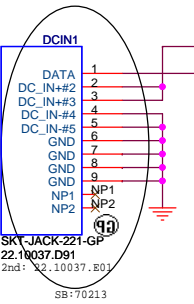
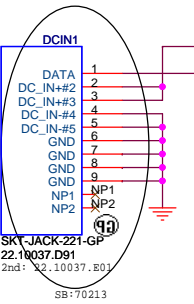
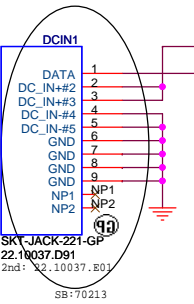
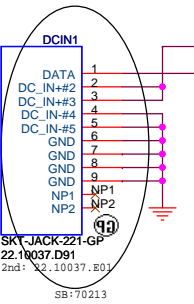
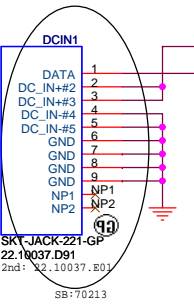
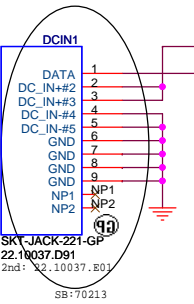
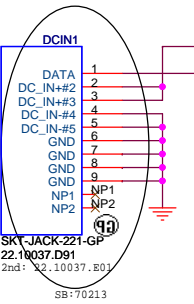
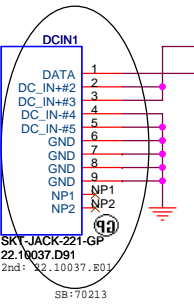
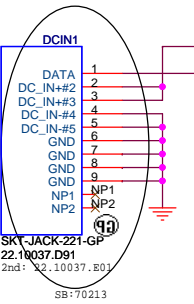
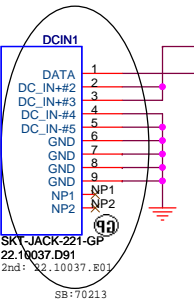
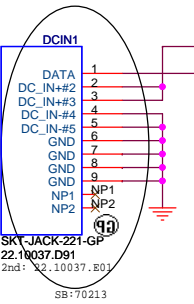
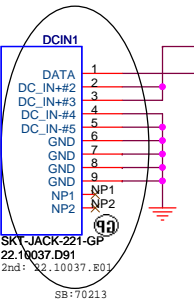
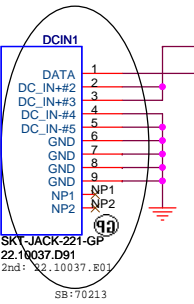
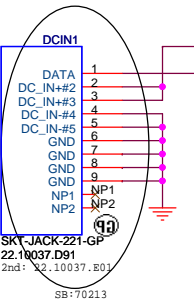
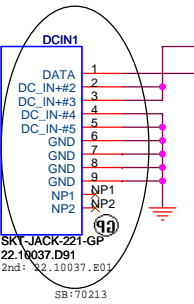
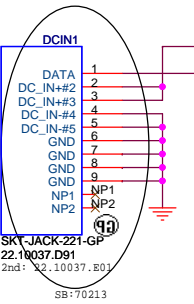
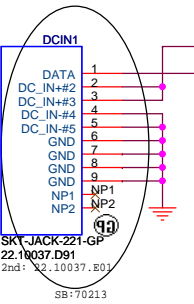
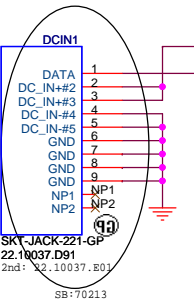
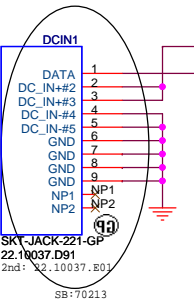
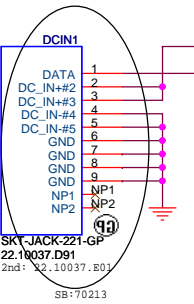
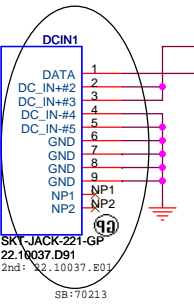
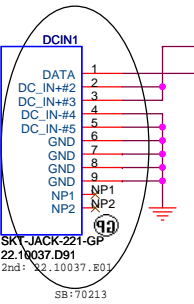
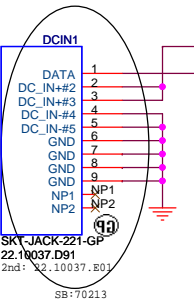
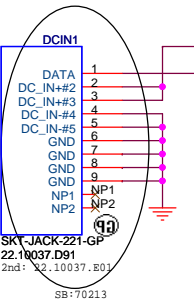
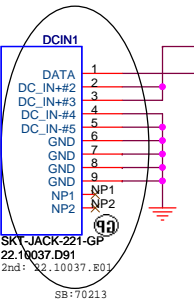
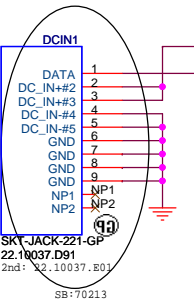
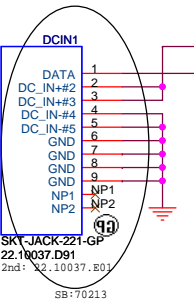
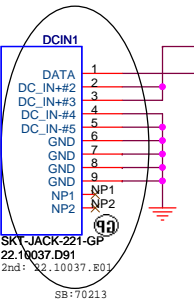
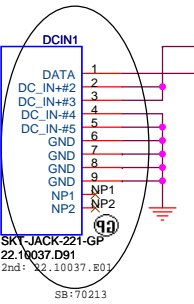
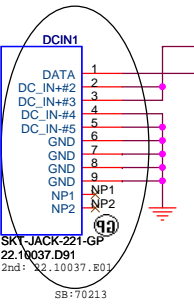
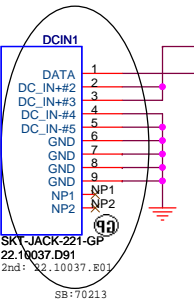
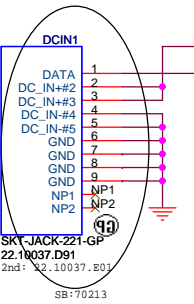
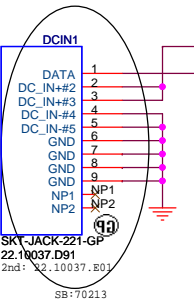
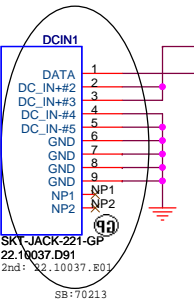
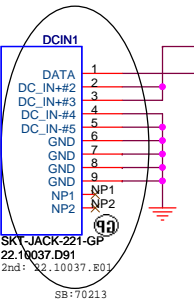
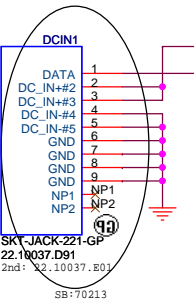
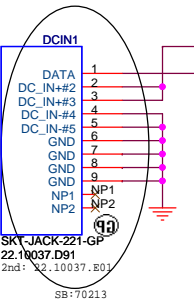
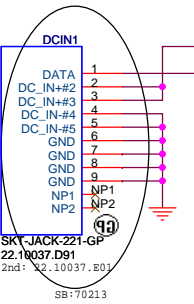
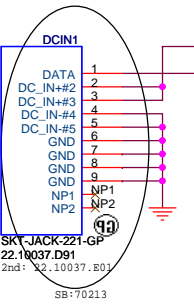
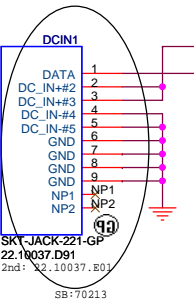
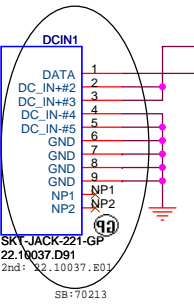
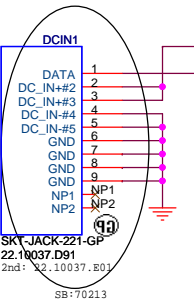
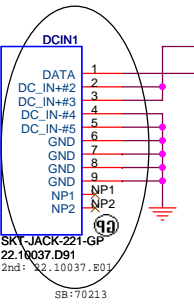
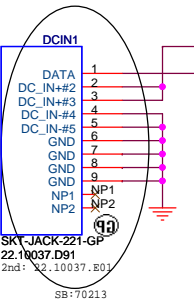
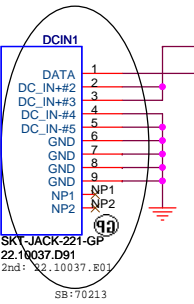
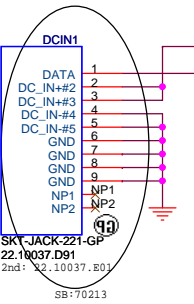
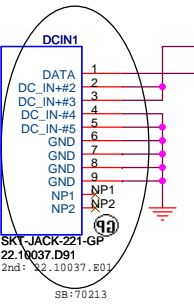
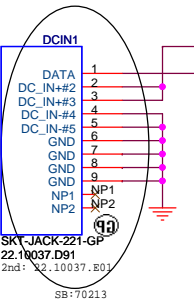
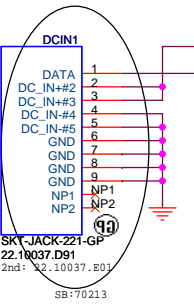
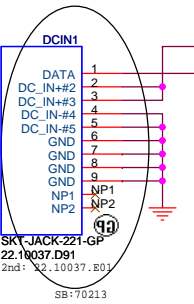
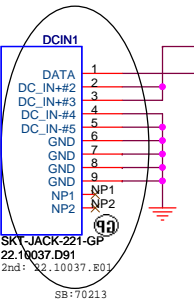
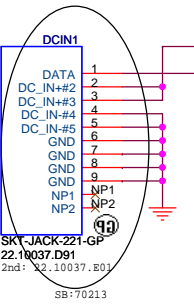
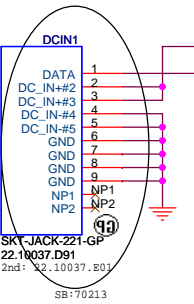
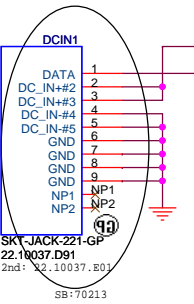
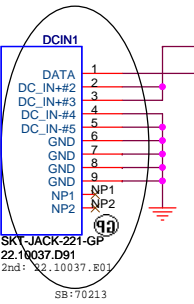
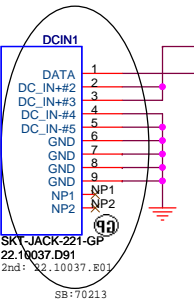
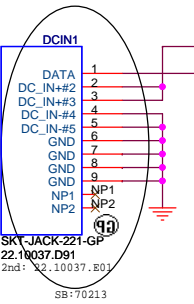
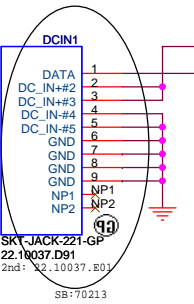
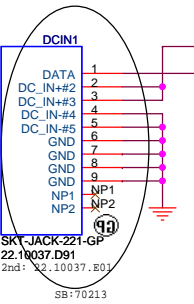
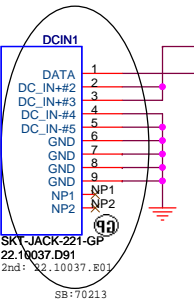
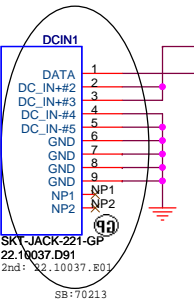
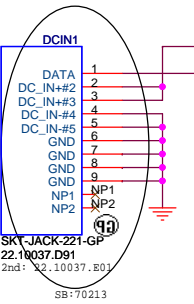
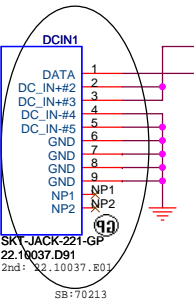




## Adapter In

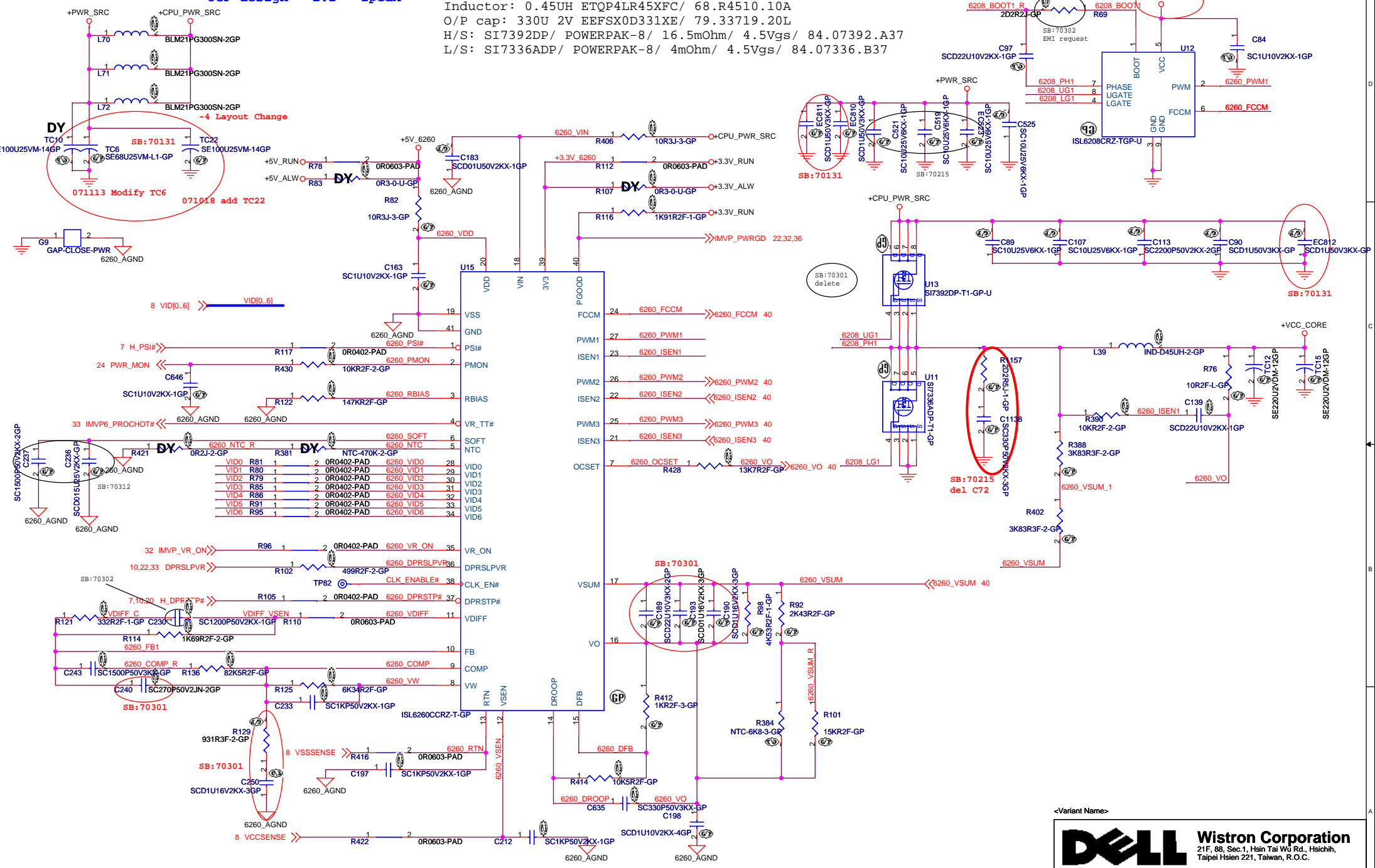
Reserved for EMI

Place near DCIN1



Thermal Design = 35.23  
Peak Current [Ipeak] = 44A  
OCP design = 1.2 \* Ipeak

I/P cap: 10U 25V K1200 X5R/ 78.10022.52L  
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A  
O/P cap: 330U 2V EEF5X0D331XE/ 79.33719.20L  
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37  
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

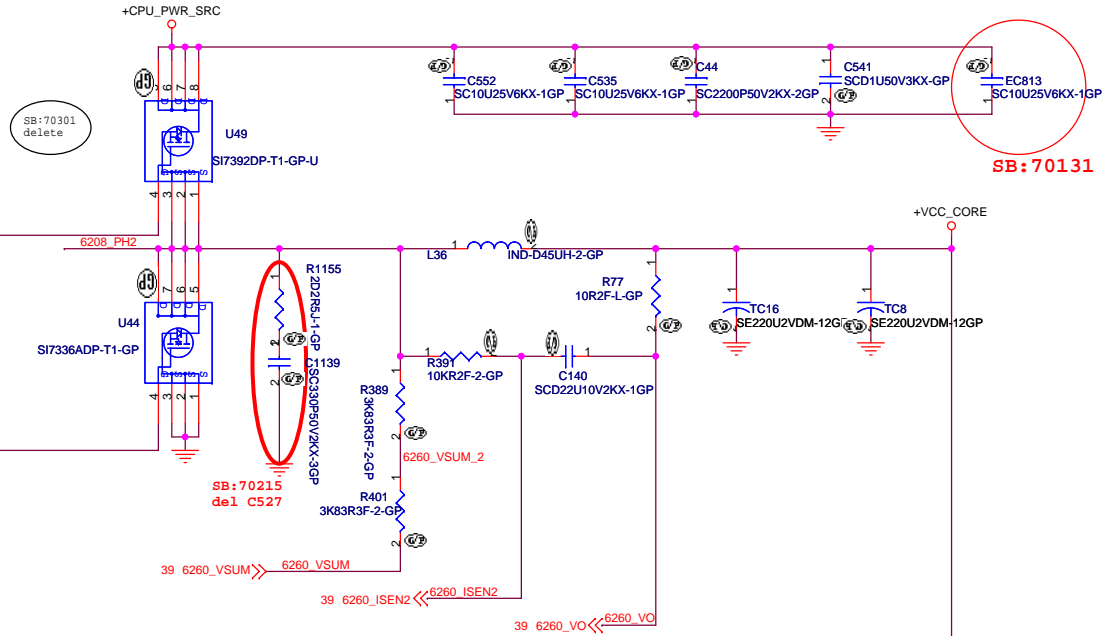
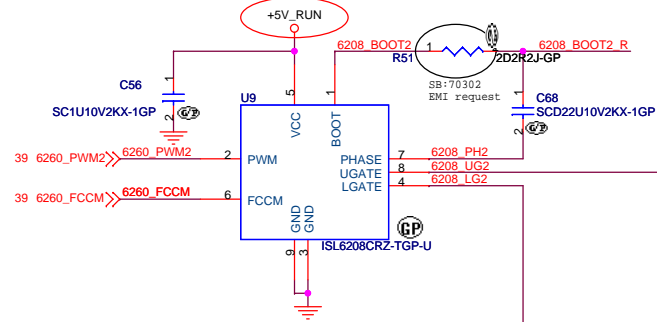
Title: **Thurman UMA**

Size: **A3** Document Number: **CPU Core-01** Rev: **-1**

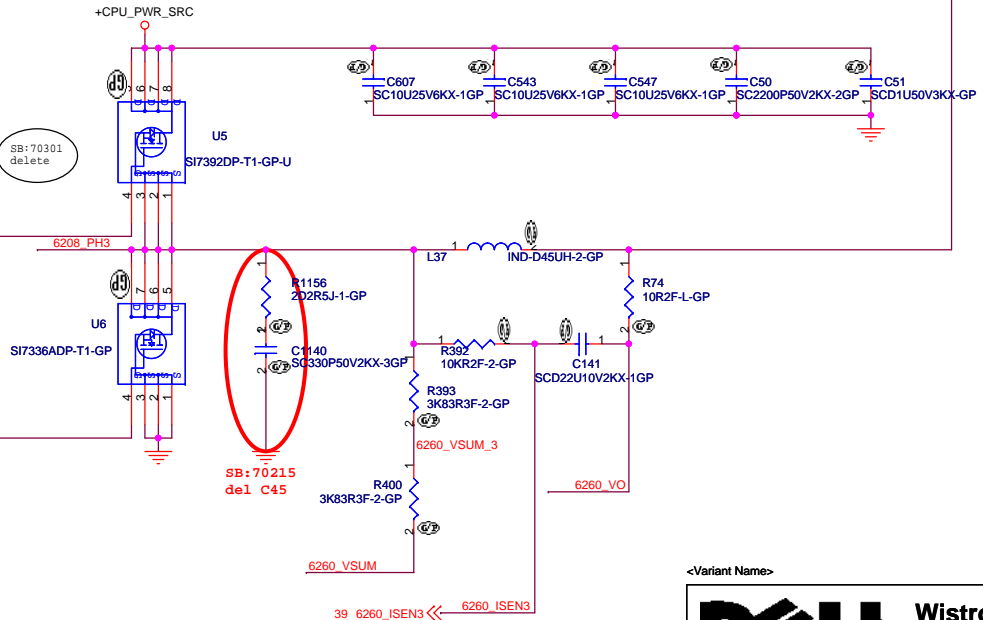
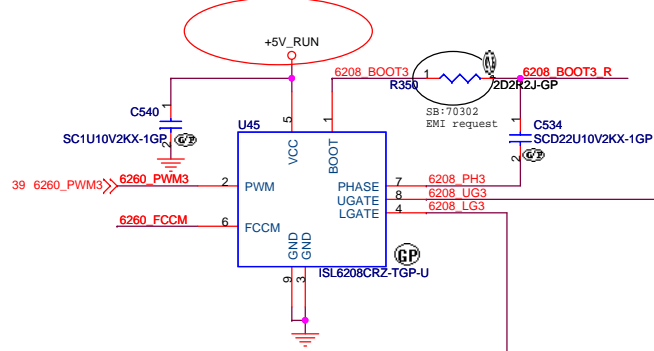
Date: Thursday, November 22, 2007 Sheet 39 of 46



Item 14



Item 14



<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thurman UMA**

Size  
**A3**

Document Number

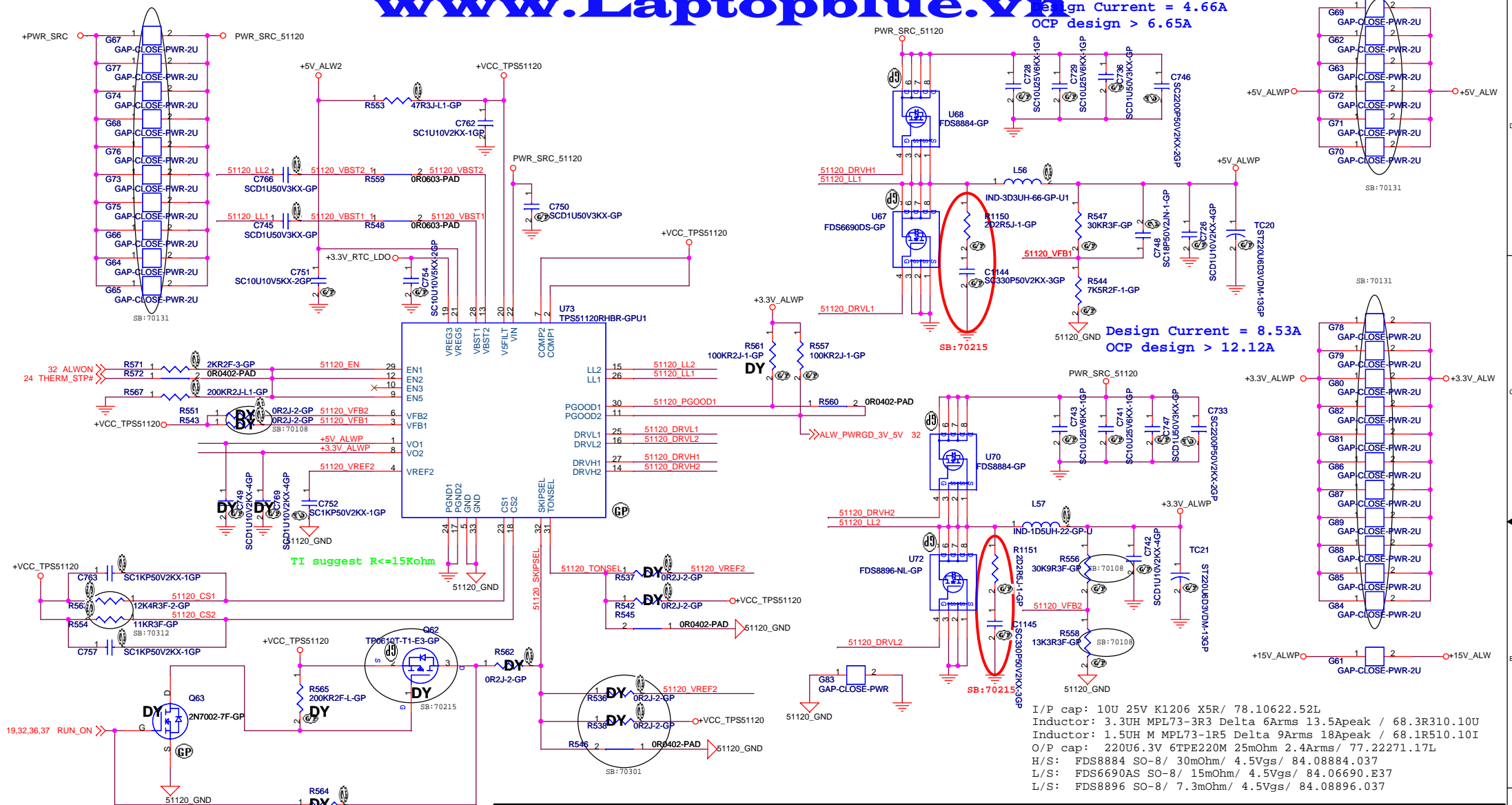
**CPU Core-02**

Rev

**-1**

Date: Wednesday, November 07, 2007

Sheet 40 of 46

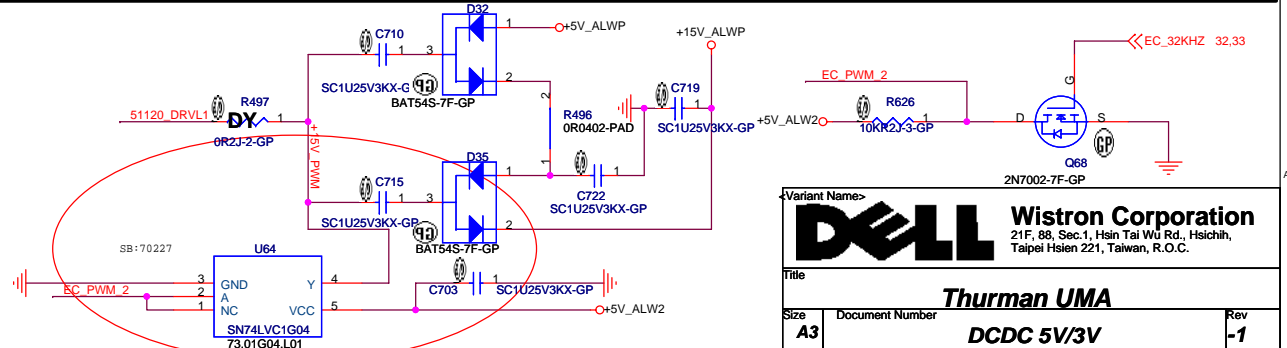


	SKIPSEL	AUTOSKIP	VREF2	PWM	V5FILT
COMP	N/A	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	not use	ADJ.	5V Fixed Output
VFB1	N/A	not use	ADJ.	ADJ.	3.3V Fixed Output
VFB2	N/A	not use	ADJ.	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VR503 ON	VR503 ON

15V

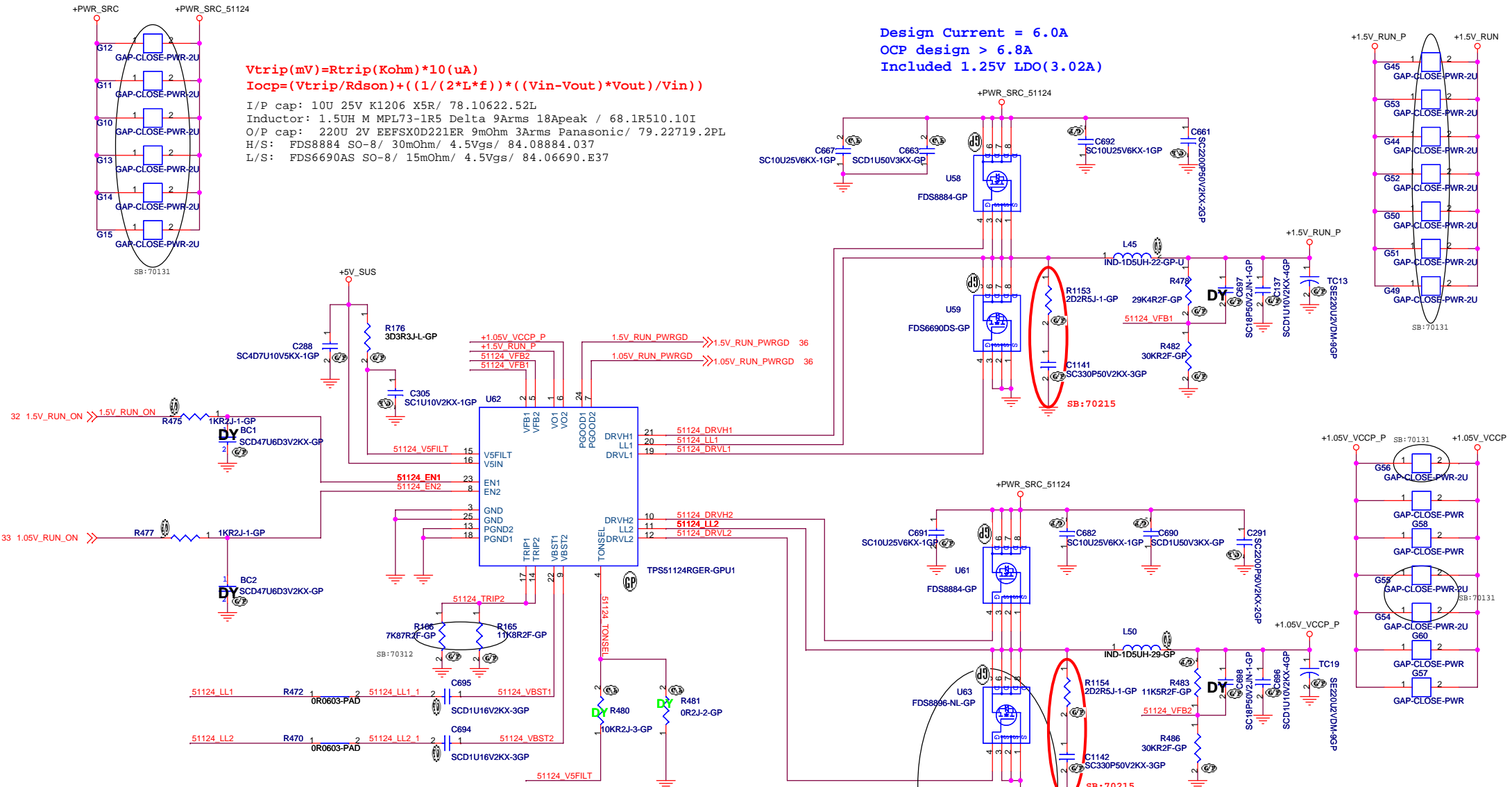


SB:70228 delete



Design Current = 6.0A  
 OCP design > 6.8A  
 Included 1.25V LDO(3.02A)

$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$   
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$   
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I  
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL  
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037  
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37



Design Current= 12.2A  
 OCP design > 15A

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

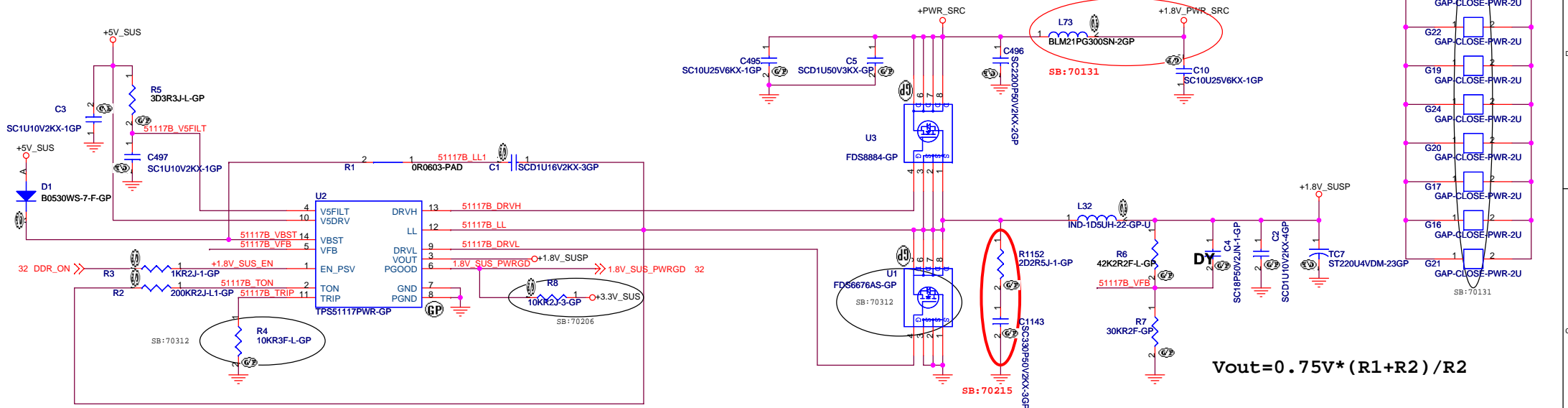
$V_{out} = 0.758V * (R1+R2)/R2$  --> PWM mode  
 $V_{out} = 0.764V * (R1+R2)/R2$  --> Skip Mode

<Variant Name>

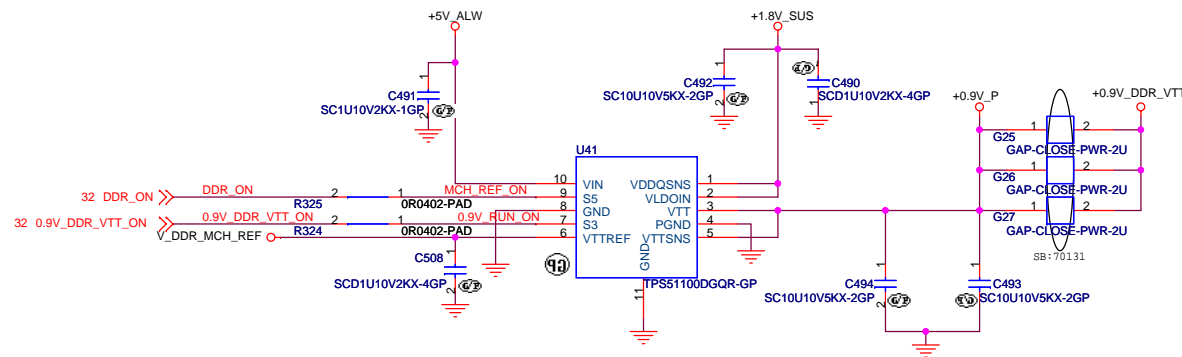
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thurman UMA**  
 Size: **A3** Document Number: **DCDC 1.5V/1.05V** Rev: **-1**  
 Date: Wednesday, November 07, 2007 Sheet 42 of 46

Design Current = 8.64A  
OCP design = 12.34A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I  
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161  
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037  
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037  
Ton = 200KOhm --> 330KHz



<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thurman UMA**

Size  
**A3**

Document Number

**DCDC 1.8V/0.9V**

Rev

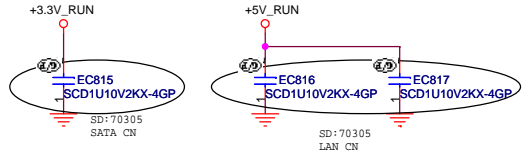
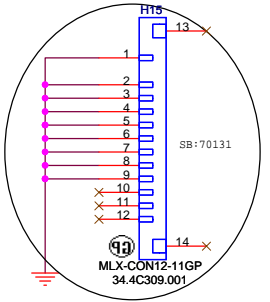
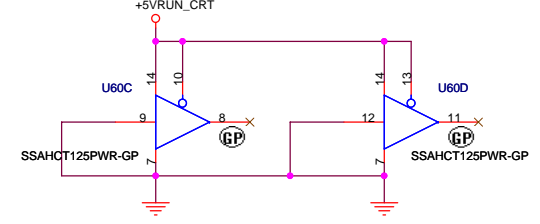
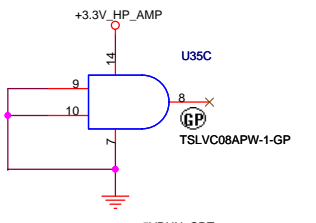
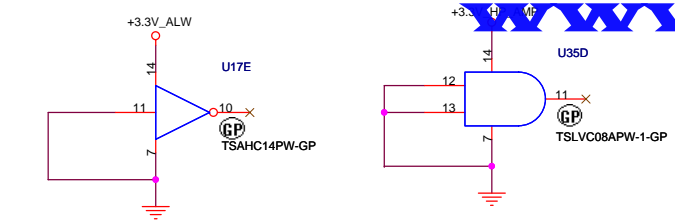
**-1**

Date: Wednesday, November 07, 2007

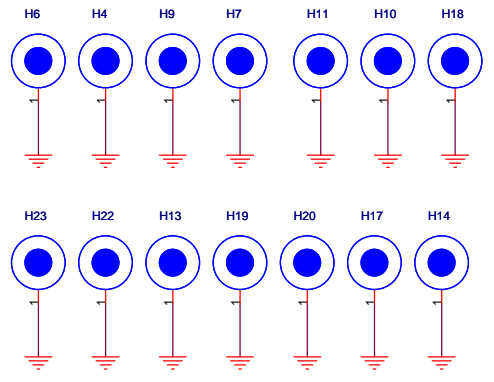
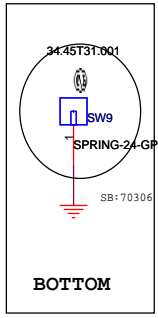
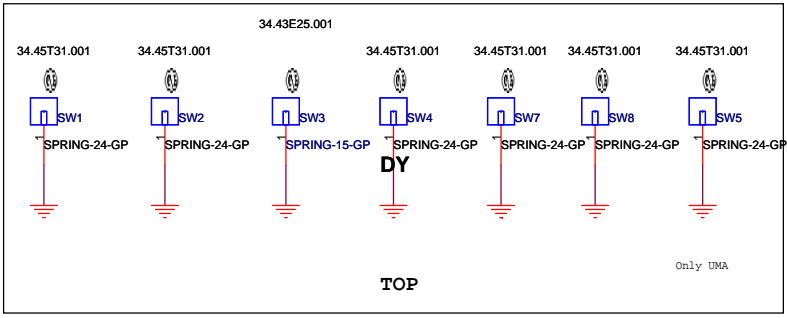
Sheet 43 of 46



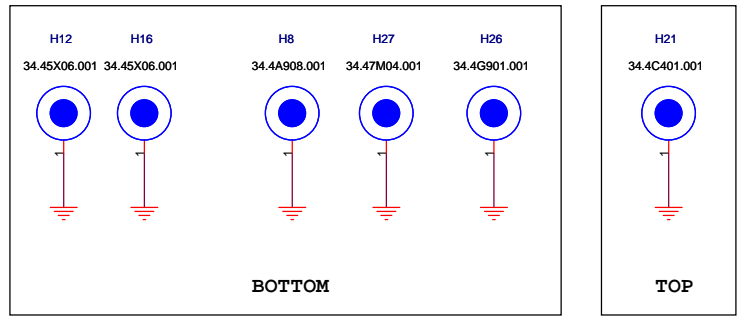




SW3 - 34.43E25.001  
SW9 - 34.49Q02.001  
SW5 - 34.34T31.001 (Only for UMA)  
others-34.45T31.001



H12, H16: 34.45X06.001  
H8: 34.4A908.001  
H27: 34.47M04.001  
H26: 34.4G901.001  
H21: 34.4C401.001



[illegible]