

Compal Confidential

NAT02 M/B Schematics Document

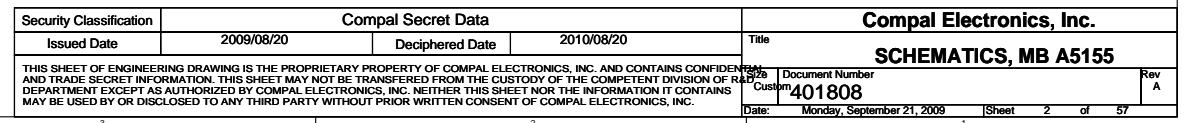
Intel Clarkfield Processor with DDRIII + Ibex Peak-M + Madison Pro

2009-08-20

REV: 0.1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/20	Deciphered Date	2010/08/20	Title	SCHEMATICS, MB A5155
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+GPU_CORE	Core voltage for GPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.1VS	1.1V power rail for PCIe of GUP	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
B+_BIAS	B+ always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	WWAN	
		WLAN	
		Express Card	
		VGA thermal sensor	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3191AKLFT, SLG8SP585)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
Free Fall Sensor	
CPU XDP	
PCH XDP	
XDCP_ISL90727	0101 110Xb
XDCP_ISL90728	0111 110Xb

STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

	Vcc	3.3V +/- 5%			
	Ra	100K +/- 1%			
Board ID	VGA	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
X00	M96	0	0 V	0 V	0.100 V
X01	M96	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
X02	M96	18K +/- 1%	0.436 V	0.503 V	0.538 V
MP	M96	33K +/- 1%	0.712 V	0.819 V	0.875 V
X00	Madison	56K +/- 1%	1.036 V	1.185 V	1.264 V
X01	Madison	100K +/- 1%	1.453 V	1.650 V	1.759 V
X02	Madison	200K +/- 1%	1.935 V	2.200 V	2.341 V
MP	Madison	NC	2.500 V	3.300 V	3.300 V

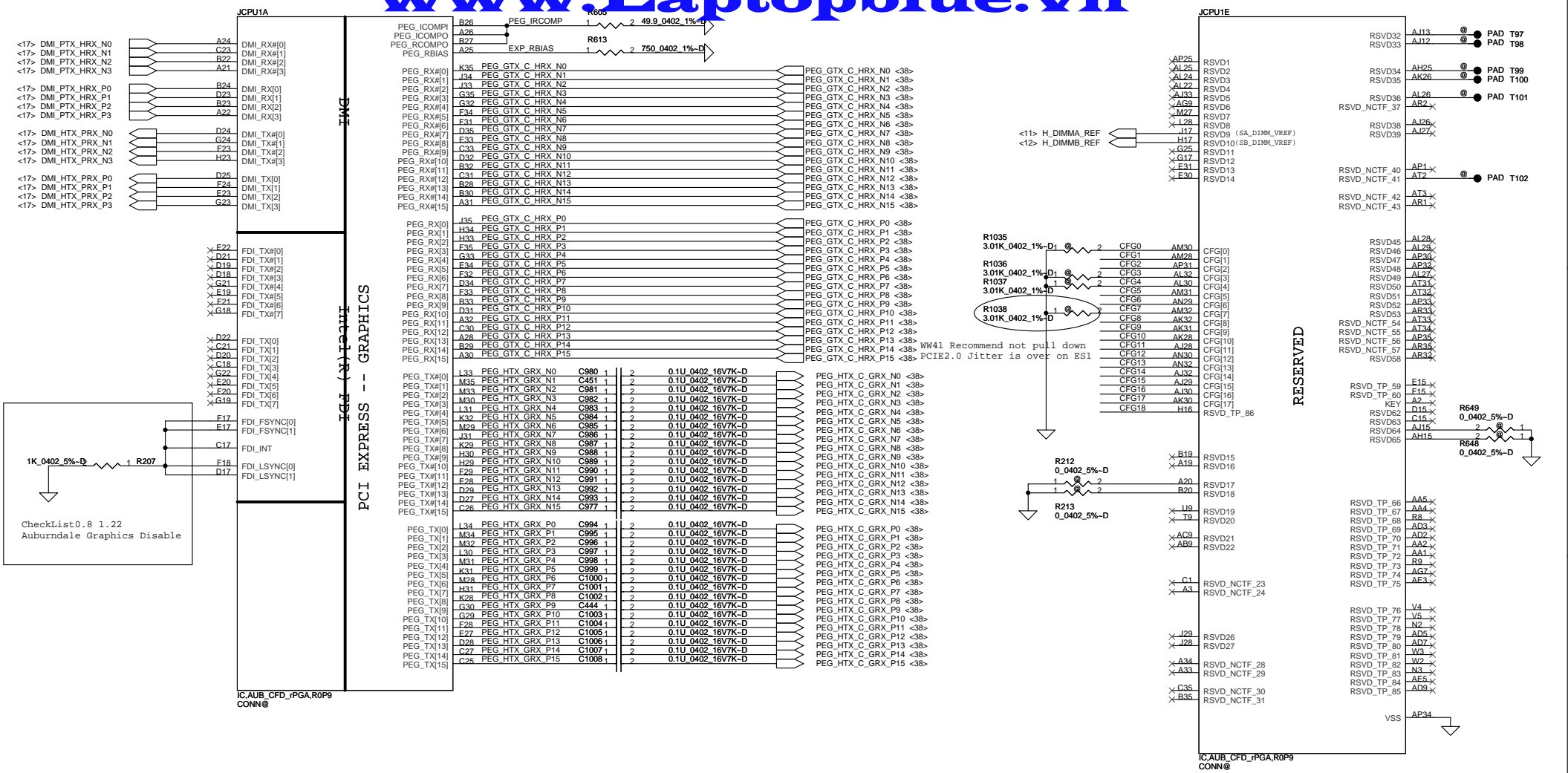
USB Port Table

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

BTO Option Table

[illegible]

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```
CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

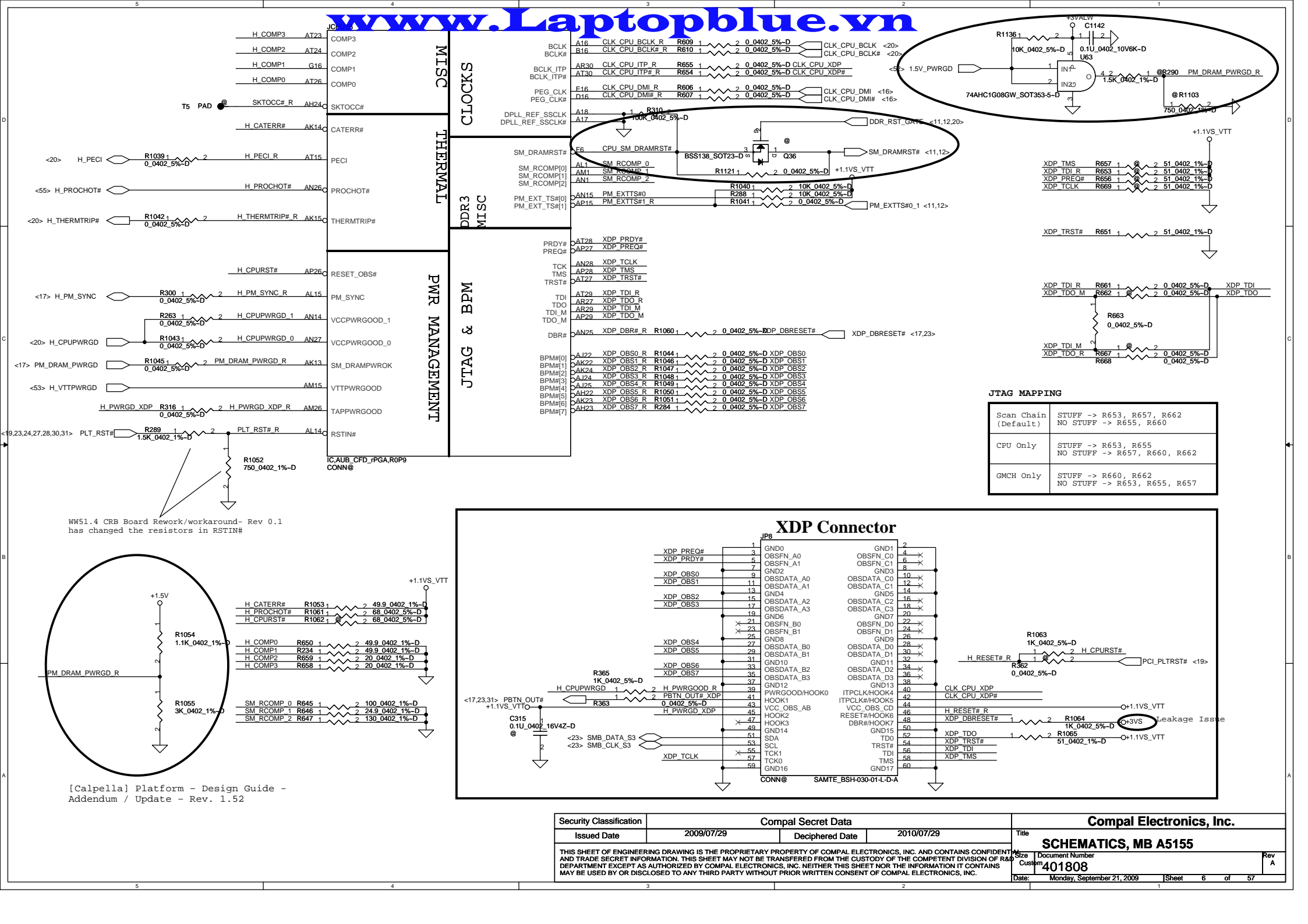
CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
    15 -> 0, 14 -> 1, ...
```

```
CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port
   attached to Embedded Display Port
0:Enabled; An external Display Port
   device is connected to the Embedded
   Display Port

*:Default
```



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COMPONENTS:

- H COMP3 AT23
- H COMP2 AT24
- H COMP1 G16
- H COMP0 AT26
- T5 PAD SKTOCC# R AH24
- H CATERR# AK14
- H_PECI# R1039 0.0402 5%-D
- H_PROCHOT# AN26
- H_THERMTRIP# R1042 0.0402 5%-D
- H_PM_SYNC# R300 0.0402 5%-D
- H_CPUPWRGD# R263 0.0402 5%-D
- PM_DRAMPWRGD R1045 0.0402 5%-D
- H_VTTPWRGD# AM15
- PLT_RST# R289 1.5K 0.402 1%-D
- R1052 750 0.402 1%-D
- R1054 1.1K 0.402 1%-D
- R1055 3K 0.402 1%-D
- H_CATERR# R1053 49.9 0.402 1%-D
- H_PROCHOT# R1061 68 0.402 5%-D
- H_CPURST# R1062 68 0.402 5%-D
- H_COMP0 R650 49.9 0.402 1%-D
- H_COMP1 R234 49.9 0.402 1%-D
- H_COMP2 R659 20 0.402 1%-D
- H_COMP3 R658 20 0.402 1%-D
- SM_RCOMP_0 R645 100 0.402 1%-D
- SM_RCOMP_1 R646 24.9 0.402 1%-D
- SM_RCOMP_2 R647 130 0.402 1%-D

CLOCKS:

- BCLK BCLK#
- AB30 CLK CPU ITP# R655 2 0.0402 5%-D CLK CPU XDP
- AT30 CLK CPU ITP# R654 2 0.0402 5%-D CLK CPU XDP#
- E16 CLK CPU DMI# R606 2 0.0402 5%-D CLK CPU DMI <16>
- D16 CLK CPU DMI# R607 2 0.0402 5%-D CLK CPU DMI# <16>
- DPLL_REF_SSCLK DPLL_REF_SSCLK#
- SM_DRAMRST#
- SM_RCOMP_0 AM1
- SM_RCOMP_1 AM1
- SM_RCOMP_2 AN1
- PM_EXT_TS#0 AN15
- PM_EXT_TS#1 R AP15
- PRDY# AT28
- PREQ# AP27
- TCK AN28
- TMS AP28
- TRST# AT27
- TDO AT29
- TDO_M AR27
- TDO_M AR29
- DBR# AN25
- BPM#0 AJ22
- BPM#1 AK22
- BPM#2 AJ24
- BPM#3 AJ25
- BPM#4 AJ26
- BPM#5 AK22
- BPM#6 AK23
- BPM#7 AH23

DDR3 MISC:

- DDR_RST_GATE <11,12,20>
- SM_DRAMRST# <11,12>
- PM_EXT_TS#0 <11,12>
- XDP_DBRESET# <17,23>

JTAG & BPM:

- XDP OBS0 R1044
- XDP OBS1 R1046
- XDP OBS2 R1047
- XDP OBS3 R1048
- XDP OBS4 R1049
- XDP OBS5 R1050
- XDP OBS6 R1051
- XDP OBS7 R284

JTAG MAPPING:

Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657

XDP Connector:

Signal	Pin	Signal	Pin
XDP_PREQ#	1	GND1	2
XDP_PRDY#	3	OBSFN_A0	4
XDP_OBS0	5	OBSFN_A1	6
XDP_OBS1	7	GND2	8
XDP_OBS2	9	OBSDATA_A0	10
XDP_OBS3	11	OBSDATA_A1	12
XDP_OBS4	13	GND4	14
XDP_OBS5	15	OBSDATA_A2	16
XDP_OBS6	17	OBSDATA_A3	18
XDP_OBS7	19	GND6	20
XDP_OBS8	21	OBSFN_B0	22
XDP_OBS9	23	OBSFN_B1	24
XDP_OBS10	25	GND8	26
XDP_OBS11	27	OBSDATA_B0	28
XDP_OBS12	29	OBSDATA_B1	30
XDP_OBS13	31	GND10	32
XDP_OBS14	33	OBSDATA_B2	34
XDP_OBS15	35	OBSDATA_B3	36
XDP_OBS16	37	GND12	38
XDP_OBS17	39	PWRGOOD/HOOK0	40
XDP_OBS18	41	ITPCLK/HOOK4	42
XDP_OBS19	43	VCC_OBS_CD	44
XDP_OBS20	45	RESET/HOOK6	46
XDP_OBS21	47	DBR/HOOK7	48
XDP_OBS22	49	GND14	50
XDP_OBS23	51	TDO	52
XDP_OBS24	53	TRST#	54
XDP_OBS25	55	TDI	56
XDP_OBS26	57	TMS	58
XDP_OBS27	59	GND16	60

Notes:

- WW51.4 CRB Board Rework/workaround- Rev 0.1 has changed the resistors in RSTIN#
- Leakage Issue: X3VS

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- H_CPUPWRGD# R263 0.0402 5%-D
- PM_DRAMPWRGD R1045 0.0402 5%-D
- H_VTTPWRGD# AM15
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- BPM#0 AJ22
- BPM#1 AK22
- BPM#2 AJ24
- BPM#3 AJ25
- BPM#4 AJ26
- BPM#5 AK22
- BPM#6 AK23
- BPM#7 AH23

DDR3 MISC:

- DDR_RST_GATE <11,12,20>
- SM_DRAMRST# <11,12>
- PM_EXT_TS#0 <11,12>
- XDP_DBRESET# <17,23>
- XDP_OBS0 R1044 2 0.0402 5%-D XDP OBS0
- XDP_OBS1 R1045 2 0.0402 5%-D XDP OBS1
- XDP_OBS2 R1047 2 0.0402 5%-D XDP OBS2
- XDP_OBS3 R1048 2 0.0402 5%-D XDP OBS3
- XDP_OBS4 R1049 2 0.0402 5%-D XDP OBS4
- XDP_OBS5 R1050 2 0.0402 5%-D XDP OBS5
- XDP_OBS6 R1051 2 0.0402 5%-D XDP OBS6
- XDP_OBS7 R284 2 0.0402 5%-D XDP OBS7

JTAG MAPPING:

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CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
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XDP_OBS0	5	OBSFN_A1	6
XDP_OBS1	7	GND2	8
XDP_OBS2	9	OBSDATA_A0	10
XDP_OBS3	11	OBSDATA_A1	12
XDP_OBS4	13	GND4	14
XDP_OBS5	15	OBSDATA_A2	16
XDP_OBS6	17	OBSDATA_A3	18
XDP_OBS7	19	GND6	20
XDP_OBS8	21	OBSFN_B0	22
XDP_OBS9	23	OBSFN_B1	24
XDP_OBS10	25	GND8	26
XDP_OBS11	27	OBSDATA_B0	28
XDP_OBS12	29	OBSDATA_B1	30
XDP_OBS13	31	GND10	32
XDP_OBS14	33	OBSDATA_B2	34
XDP_OBS15	35	OBSDATA_B3	36
XDP_OBS16	37	GND12	38
XDP_OBS17	39	PWRGOOD/HOOK0	40
XDP_OBS18	41	ITPCLK/HOOK4	42
XDP_OBS19	43	VCC_OBS_CD	44
XDP_OBS20	45	RESET#_HOOK6	46
XDP_OBS21	47	DBR#_HOOK7	48
XDP_OBS22	49	GND14	50
XDP_OBS23	51	TDO	52
XDP_OBS24	53	TRST#	54
XDP_OBS25	55	TDI	56
XDP_OBS26	57	TMS	58
XDP_OBS27	59	GND16	60

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<11> DDR_A_D[0.63]
<11> DDR_A_DM[0.7]
<11> DDR_A_DQS[0.7]
<11> DDR_A_MA[0.15]

DDR_A_D0	A10
DDR_A_D1	C10
DDR_A_D2	C7
DDR_A_D3	A7
DDR_A_D4	B10
DDR_A_D5	D10
DDR_A_D6	E10
DDR_A_D7	A8
DDR_A_D8	D8
DDR_A_D9	F10
DDR_A_D10	E6
DDR_A_D11	E7
DDR_A_D12	E9
DDR_A_D13	B7
DDR_A_D14	E7
DDR_A_D15	C6
DDR_A_D16	H10
DDR_A_D17	G8
DDR_A_D18	K7
DDR_A_D19	J8
DDR_A_D20	G7
DDR_A_D21	G10
DDR_A_D22	J7
DDR_A_D23	J10
DDR_A_D24	L7
DDR_A_D25	M6
DDR_A_D26	M8
DDR_A_D27	L9
DDR_A_D28	L6
DDR_A_D29	K8
DDR_A_D30	N8
DDR_A_D31	P9
DDR_A_D32	AH5
DDR_A_D33	AE5
DDR_A_D34	AK6
DDR_A_D35	AK7
DDR_A_D36	AE6
DDR_A_D37	AG5
DDR_A_D38	AJ7
DDR_A_D39	AJ6
DDR_A_D40	AJ10
DDR_A_D41	AJ9
DDR_A_D42	AL10
DDR_A_D43	AK12
DDR_A_D44	AK8
DDR_A_D45	AL7
DDR_A_D46	AK11
DDR_A_D47	AL8
DDR_A_D48	AN8
DDR_A_D49	AN10
DDR_A_D50	AR11
DDR_A_D51	AL11
DDR_A_D52	AM9
DDR_A_D53	AN9
DDR_A_D54	AT11
DDR_A_D55	AP12
DDR_A_D56	AM12
DDR_A_D57	AN12
DDR_A_D58	AM13
DDR_A_D59	AT14
DDR_A_D60	AT12
DDR_A_D61	AL13
DDR_A_D62	AR14
DDR_A_D63	AP14

JCPU1C

SA_CK[0] AA6
SA_CK[0] AA7
SA_CKE[0] P7

SA_CK[1] Y6
SA_CK[1] Y6
SA_CKE[1] P6

SA_CS[0] AE2
SA_CS[1] AE8

SA_ODT[0] AD8
SA_ODT[1] AF9

SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13

SA_DQS[0] C9
SA_DQS[1] E8
SA_DQS[2] J8
SA_DQS[3] J9
SA_DQS[4] AH7
SA_DQS[5] AK9
SA_DQS[6] AP11
SA_DQS[7] AT13

SA_DQS[0] C8
SA_DQS[1] E9
SA_DQS[2] H9
SA_DQS[3] M9
SA_DQS[4] AH8
SA_DQS[5] AK10
SA_DQS[6] AN11
SA_DQS[7] AR13

SA_MA[0] Y3
SA_MA[1] W1
SA_MA[2] AA8
SA_MA[3] AA3
SA_MA[4] V1
SA_MA[5] AA9
SA_MA[6] V8
SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] T2
SA_MA[12] U13
SA_MA[13] AG8
SA_MA[14] T3
SA_MA[15] V9

IC:AUB_CFD_rPGA,R0P9
CONN@

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<12> DDR_B_DM[0.7]
<12> DDR_B_DQS[0.7]
<12> DDR_B_MA[0.15]

DDR_B_D0	B5
DDR_B_D1	A5
DDR_B_D2	C3
DDR_B_D3	B3
DDR_B_D4	E4
DDR_B_D5	A6
DDR_B_D6	C4
DDR_B_D7	D1
DDR_B_D8	D2
DDR_B_D9	F2
DDR_B_D10	E1
DDR_B_D11	E2
DDR_B_D12	F3
DDR_B_D13	F3
DDR_B_D14	G4
DDR_B_D15	H6
DDR_B_D16	G2
DDR_B_D17	J6
DDR_B_D18	J3
DDR_B_D19	G5
DDR_B_D20	J2
DDR_B_D21	J1
DDR_B_D22	J5
DDR_B_D23	K2
DDR_B_D24	L3
DDR_B_D25	M1
DDR_B_D26	K5
DDR_B_D27	N5
DDR_B_D28	AE1
DDR_B_D29	AG1
DDR_B_D30	AK1
DDR_B_D31	AK1
DDR_B_D32	AG4
DDR_B_D33	AG3
DDR_B_D34	AJ4
DDR_B_D35	AJ4
DDR_B_D36	AH4
DDR_B_D37	AK4
DDR_B_D38	AM6
DDR_B_D39	AN2
DDR_B_D40	AK5
DDR_B_D41	AK2
DDR_B_D42	AM4
DDR_B_D43	AM3
DDR_B_D44	AP3
DDR_B_D45	AN5
DDR_B_D46	AT4
DDR_B_D47	AN6
DDR_B_D48	AN4
DDR_B_D49	AN3
DDR_B_D50	AT5
DDR_B_D51	AT6
DDR_B_D52	AN7
DDR_B_D53	AP6
DDR_B_D54	AP8
DDR_B_D55	AT9
DDR_B_D56	AT7
DDR_B_D57	AP9
DDR_B_D58	AR10
DDR_B_D59	AT10
DDR_B_D60	AT10
DDR_B_D61	AT10
DDR_B_D62	AT10
DDR_B_D63	AT10

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<12> DDR_B_BS1
<12> DDR_B_BS2

<12> DDR_B_CAS#
<12> DDR_B_RAS#
<12> DDR_B_WE#

DDR SYSTEM MEMORY - B

SB_CK[0] W8
SB_CK[0] W9
SB_CKE[0] M3

SB_CK[1] V7
SB_CK[1] V6
SB_CKE[1] M2

SB_CS[0] AB8
SB_CS[1] AD6

SB_ODT[0] AC7
SB_ODT[1] AD1

SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
SB_DM[7] AT8

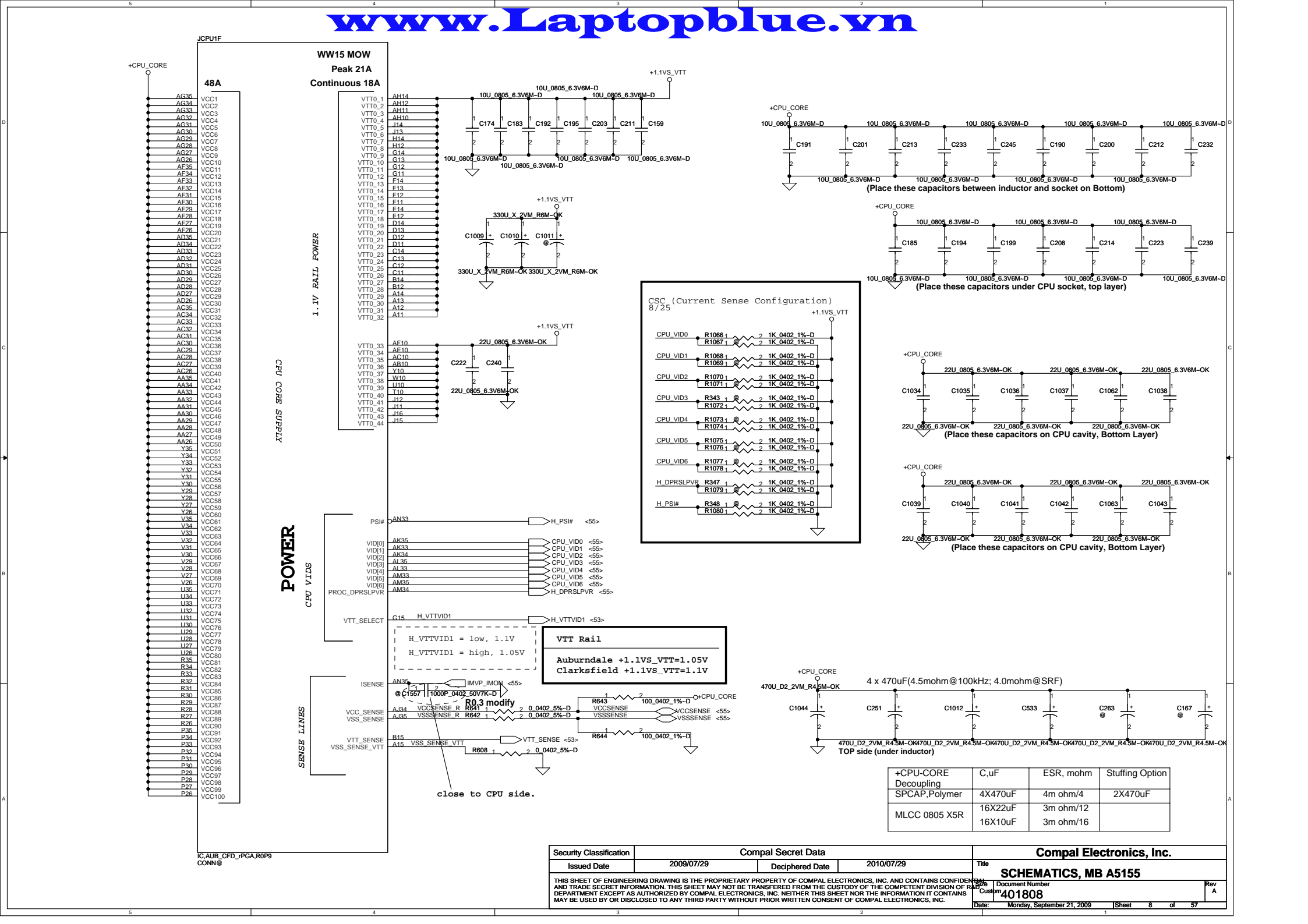
SB_DQS[0] D5
SB_DQS[1] E4
SB_DQS[2] D4
SB_DQS[3] D4
SB_DQS[4] AH2
SB_DQS[5] AR5
SB_DQS[6] AR8
SB_DQS[7] AR8

SB_DQS[0] C5
SB_DQS[1] E3
SB_DQS[2] H4
SB_DQS[3] M5
SB_DQS[4] AL5
SB_DQS[5] AP5
SB_DQS[6] AR7
SB_DQS[7] AR7

SB_MA[0] U5
SB_MA[1] V2
SB_MA[2] T5
SB_MA[3] V3
SB_MA[4] R1
SB_MA[5] TR
SB_MA[6] R2
SB_MA[7] R6
SB_MA[8] R4
SB_MA[9] R5
SB_MA[10] AR5
SB_MA[11] P3
SB_MA[12] R3
SB_MA[13] AF7
SB_MA[14] P5
SB_MA[15] N1

IC:AUB_CFD_rPGA,R0P9
CONN@

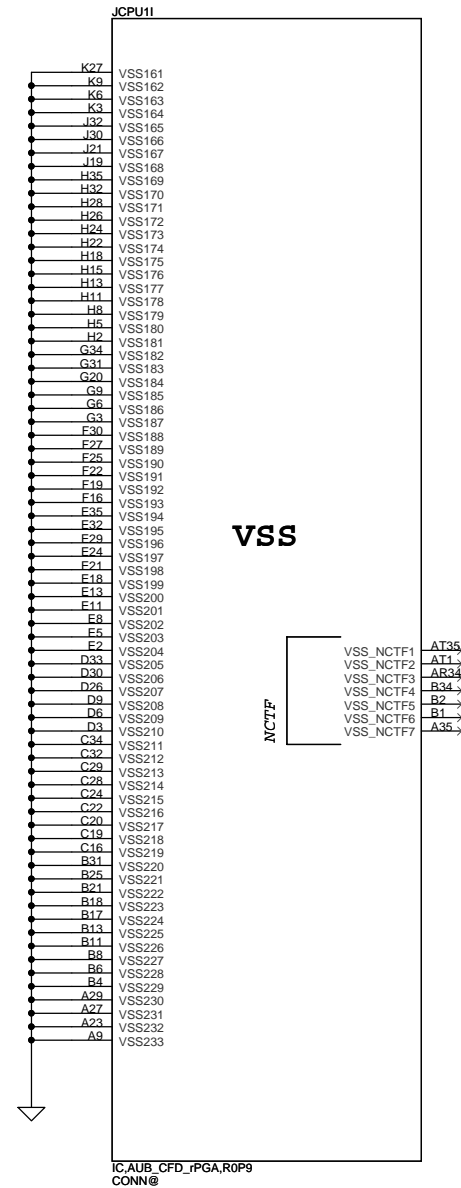
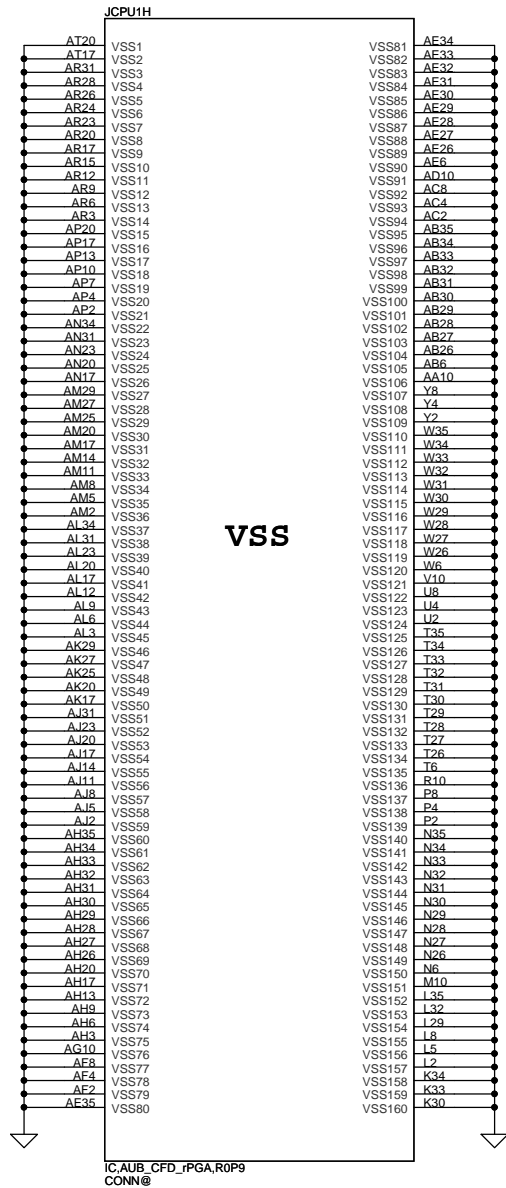
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								Document Number		Rev A
								401808		
								Date: Monday, September 21, 2009		



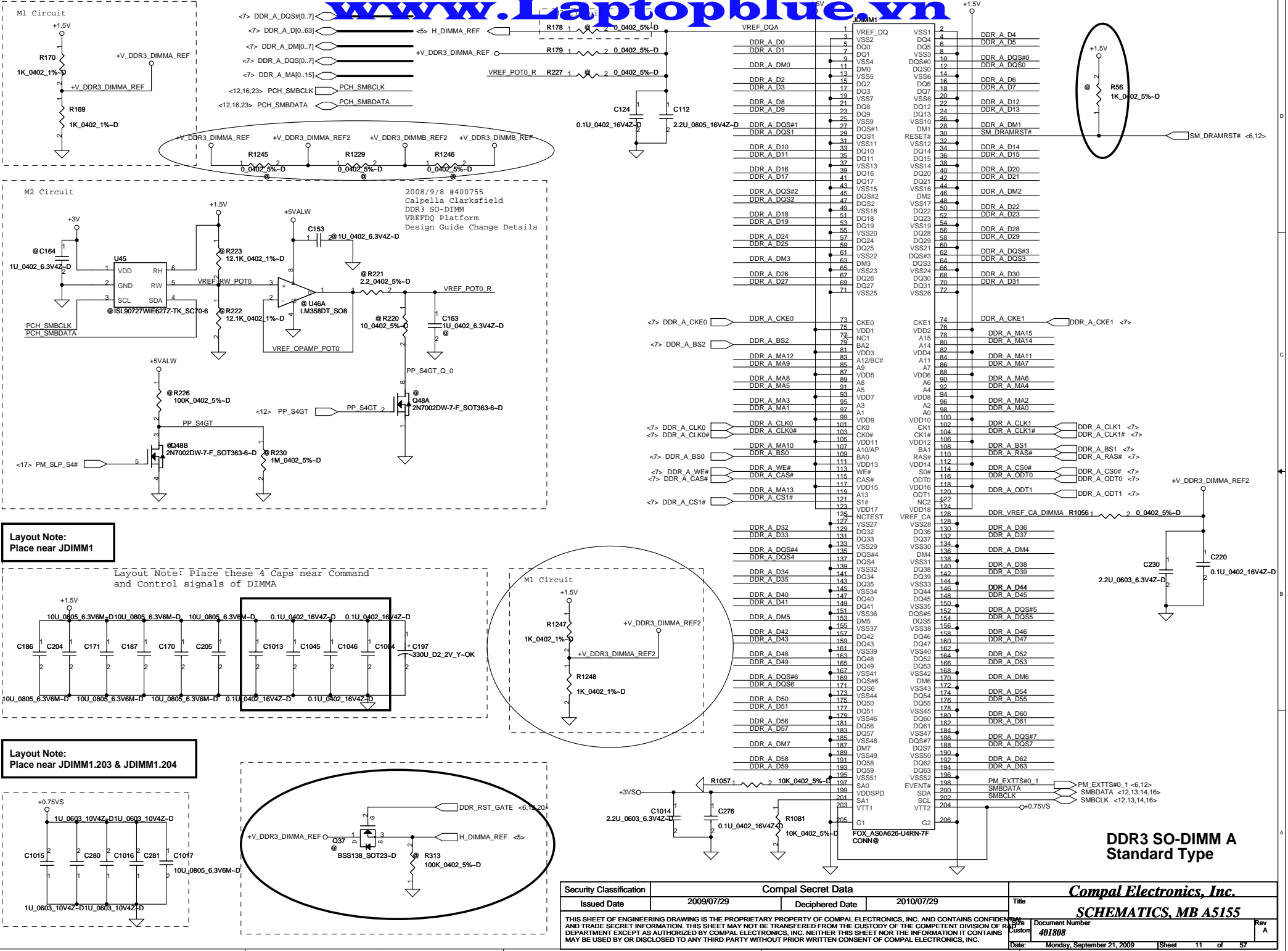
The diagram illustrates a complex power supply system for a laptop, featuring a central CPU core with various power rails (VTT0, VTT1, VTT2, VTT3, VTT4, VTT5, VTT6, VTT7, VTT8, VTT9, VTT10, VTT11, VTT12, VTT13, VTT14, VTT15, VTT16, VTT17, VTT18, VTT19, VTT20, VTT21, VTT22, VTT23, VTT24, VTT25, VTT26, VTT27, VTT28, VTT29, VTT30, VTT31, VTT32, VTT33, VTT34, VTT35, VTT36, VTT37, VTT38, VTT39, VTT40, VTT41, VTT42, VTT43, VTT44, VTT45, VTT46, VTT47, VTT48, VTT49, VTT50, VTT51, VTT52, VTT53, VTT54, VTT55, VTT56, VTT57, VTT58, VTT59, VTT60, VTT61, VTT62, VTT63, VTT64, VTT65, VTT66, VTT67, VTT68, VTT69, VTT70, VTT71, VTT72, VTT73, VTT74, VTT75, VTT76, VTT77, VTT78, VTT79, VTT80, VTT81, VTT82, VTT83, VTT84, VTT85, VTT86, VTT87, VTT88, VTT89, VTT90, VTT91, VTT92, VTT93, VTT94, VTT95, VTT96, VTT97, VTT98, VTT99, VTT100). The system includes a 1.1V RAIL POWER section, a CPU CORE SUPPLY section, and a SENSE LINES section. Key components include capacitors (C174, C183, C192, C195, C203, C211, C159, C191, C201, C213, C233, C245, C190, C200, C122, C232, C185, C194, C199, C208, C214, C223, C239, C1034, C1035, C1036, C1037, C1062, C1038, C1039, C1040, C1041, C1042, C1063, C1043, C1044, C251, C1012, C533, C263, C167), inductors (L174, L183, L192, L195, L203, L211, L159, L191, L201, L213, L233, L245, L190, L200, L122, L232, L185, L194, L199, L208, L214, L223, L239, L1034, L1035, L1036, L1037, L1062, L1038, L1039, L1040, L1041, L1042, L1063, L1043, L1044, L251, L1012, L533, L263, L167), and resistors (R174, R183, R192, R195, R203, R211, R159, R191, R201, R213, R233, R245, R190, R200, R122, R232, R185, R194, R199, R208, R214, R223, R239, R1034, R1035, R1036, R1037, R1062, R1038, R1039, R1040, R1041, R1042, R1063, R1043, R1044, R251, R1012, R533, R263, R167). The diagram also includes a table of component values and a security classification section.

Component	Value	ESR, mohm	Stuffing Option
+CPU-CORE Decoupling	4X470uF	4m ohm/4	2X470uF
SPCAP, Polymer	16X22uF	3m ohm/12	
MLCC 0805 X5R	16X10uF	3m ohm/16	

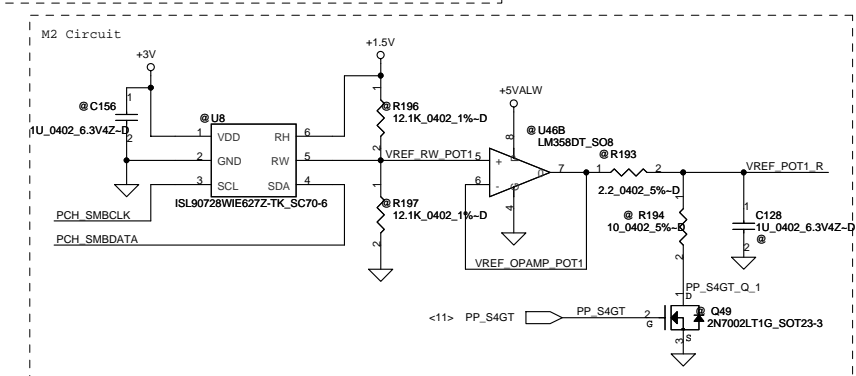
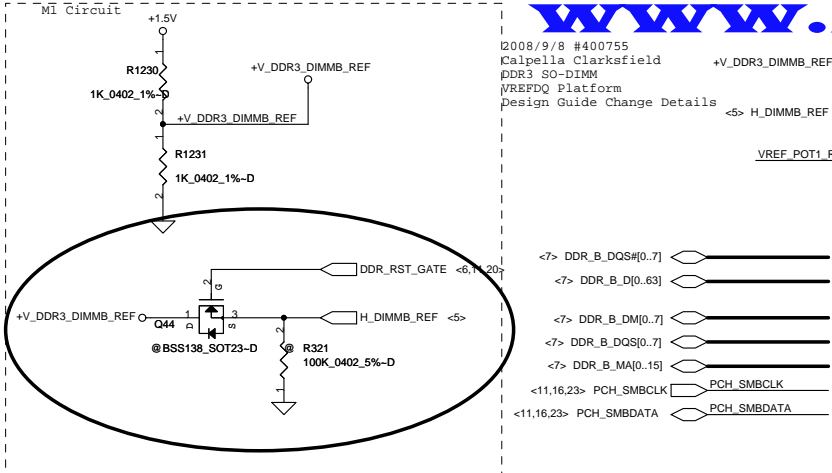
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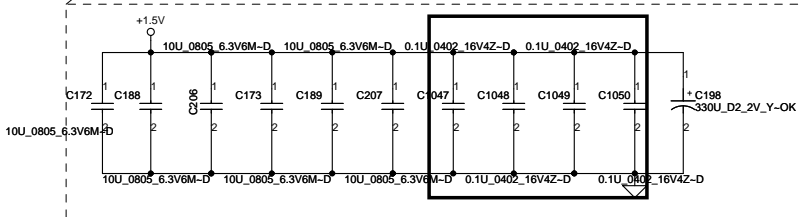


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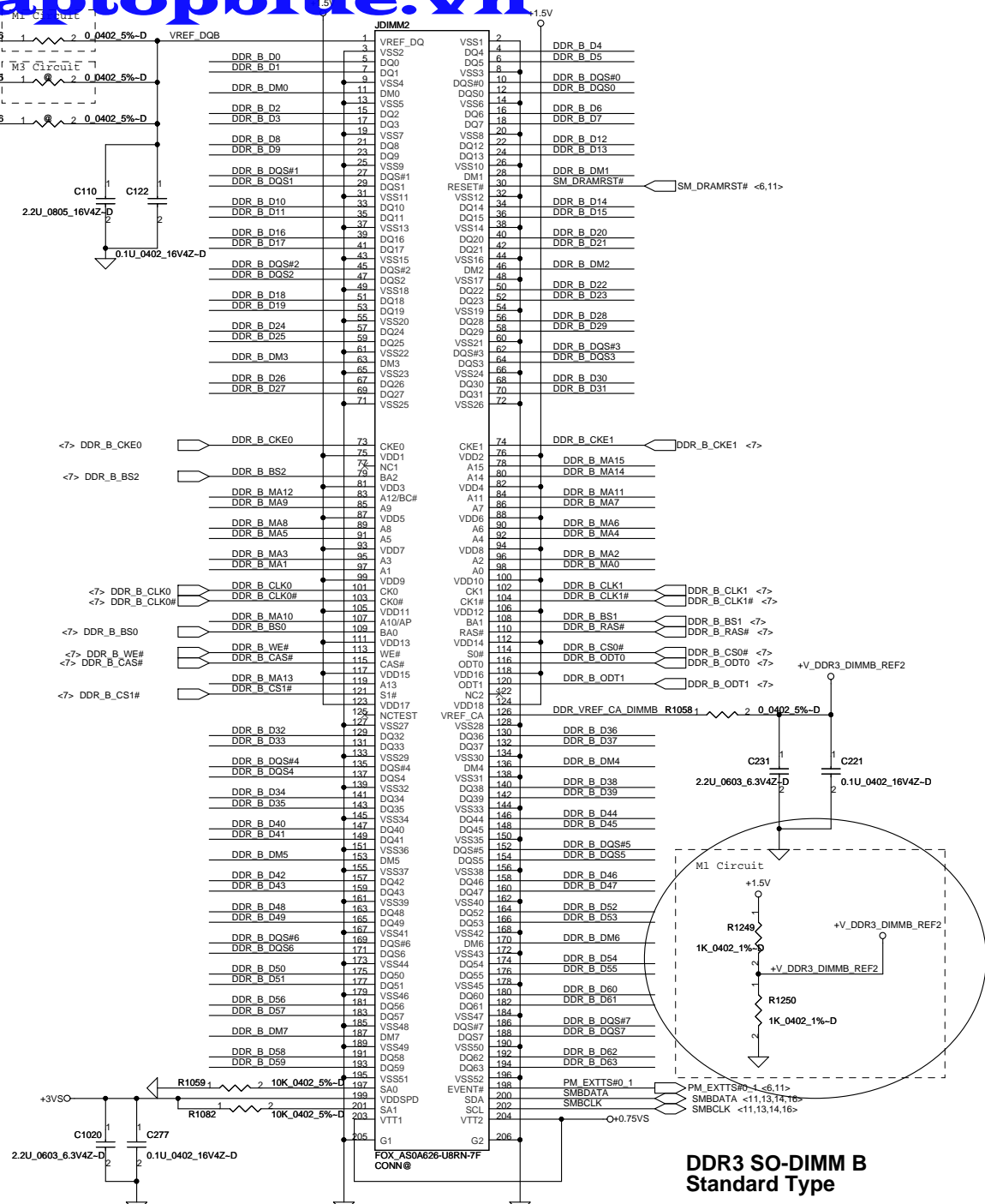
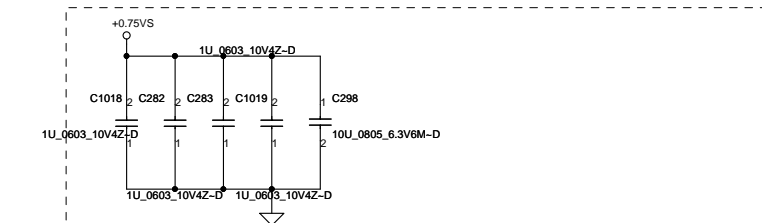


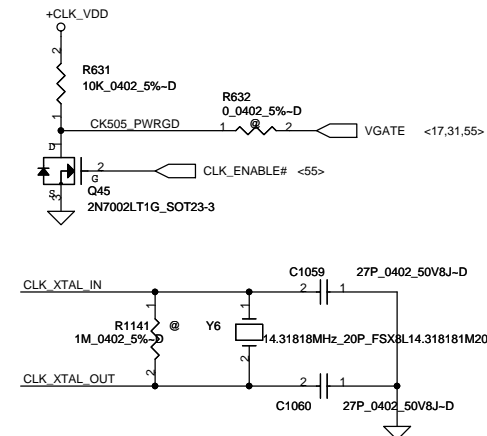
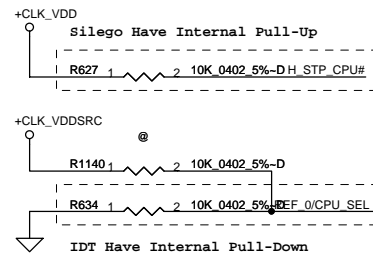
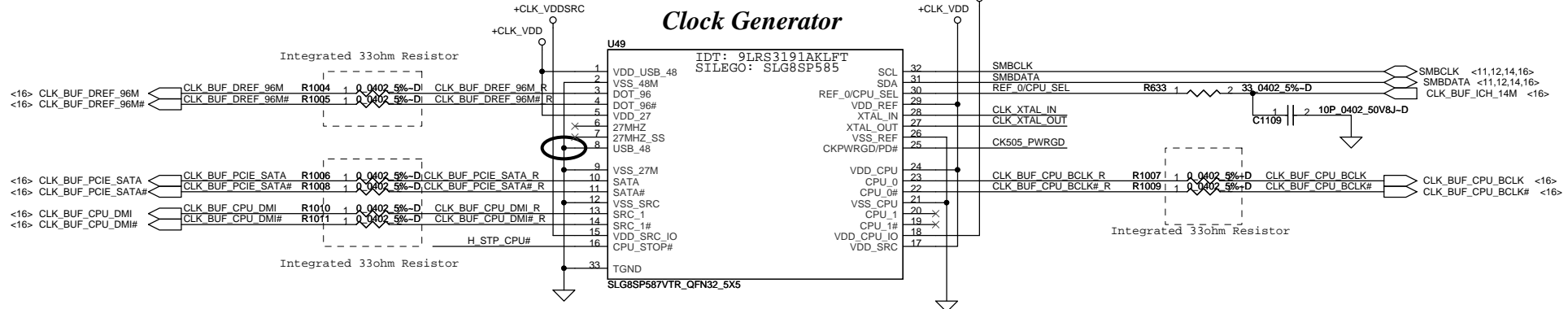
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



Layout Note:
Place near JDIMM2.203 & JDIMM2.204

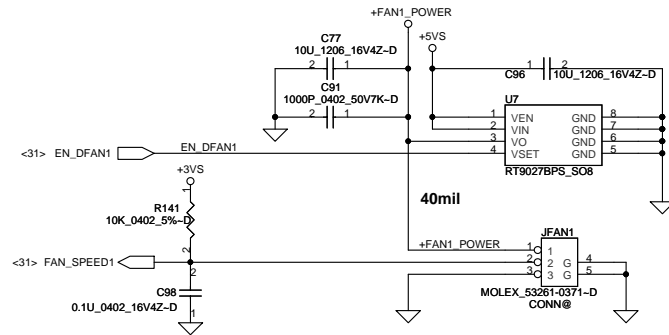




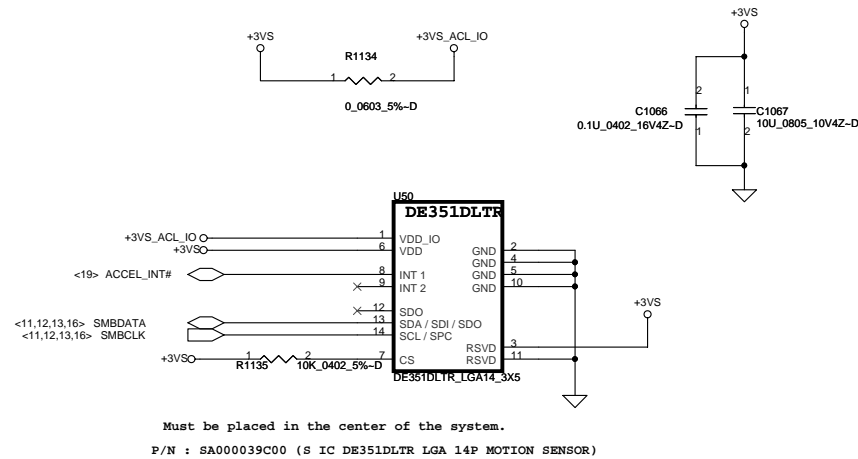
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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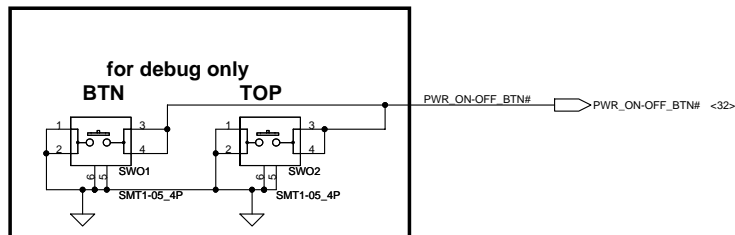
FAN Control circuit



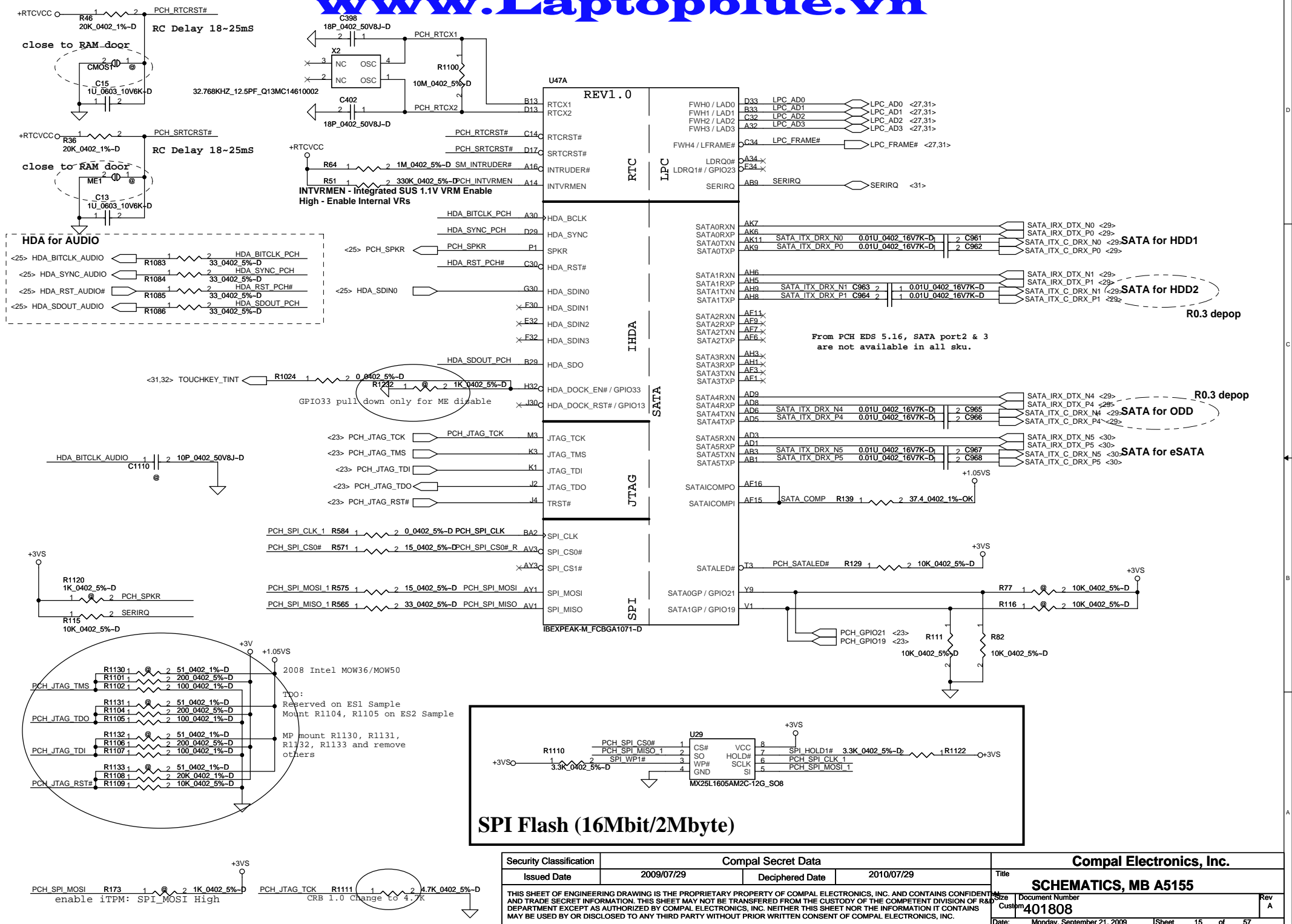
Free Fall Sensor



Power Button

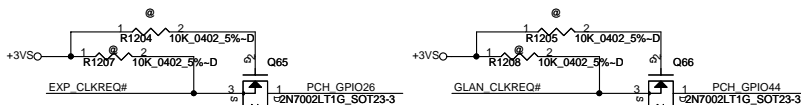
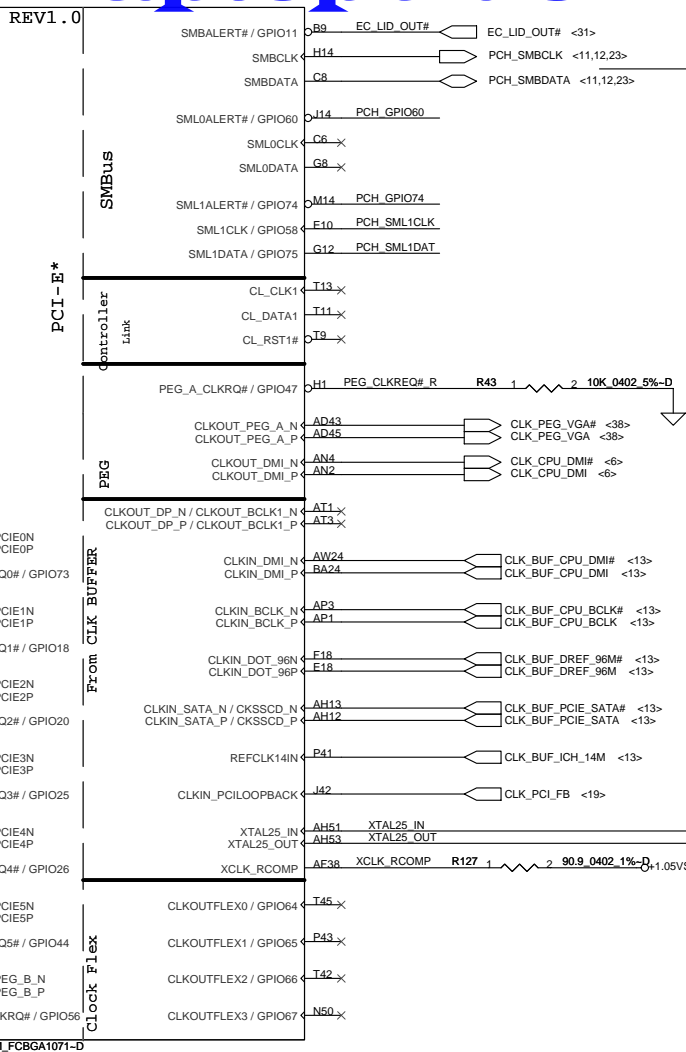
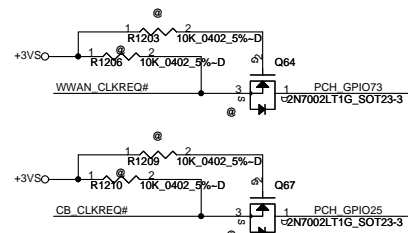
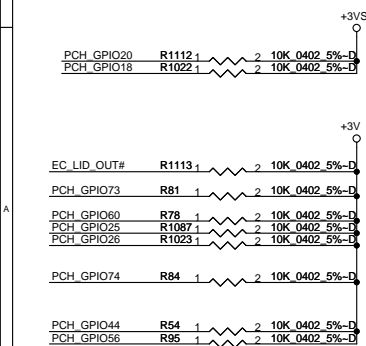
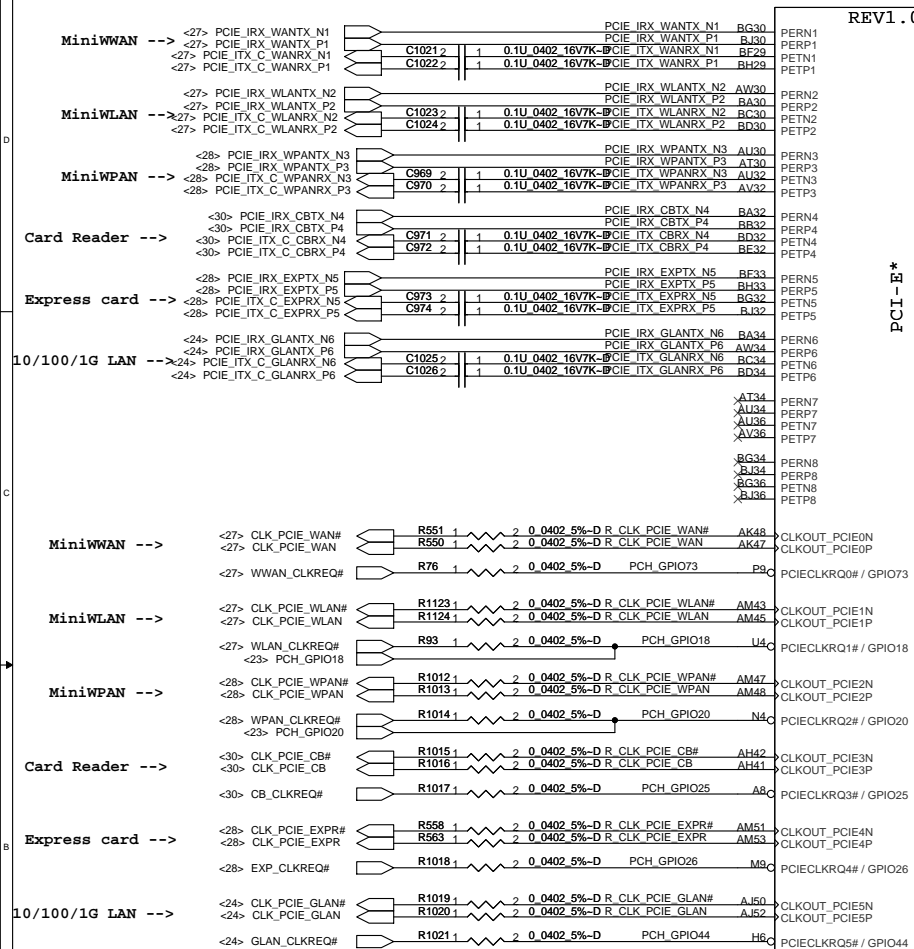


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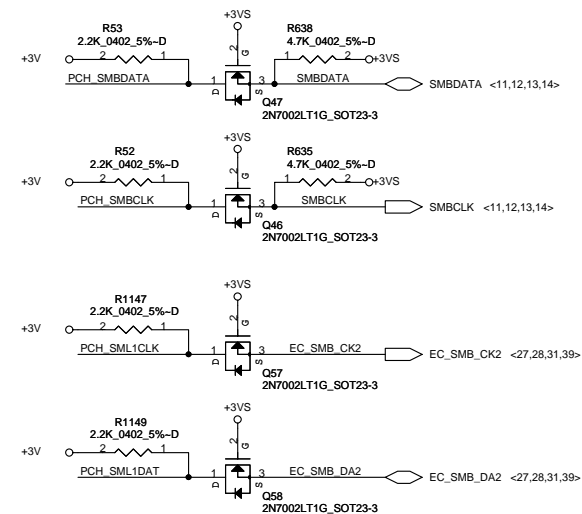


SPI Flash (16Mbit/2Mbyte)

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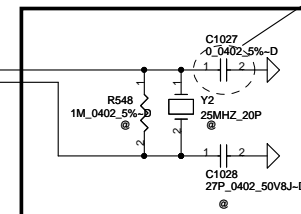


1. Connect Directly
XDCP of DDR3
2. Level Shift1, Pull-Up to +3VS
CLOCK GEN, DIMM1, DIMM2, FFS
3. Level Shift2, Pull-Up to +3VS
CPU & PCH XDP



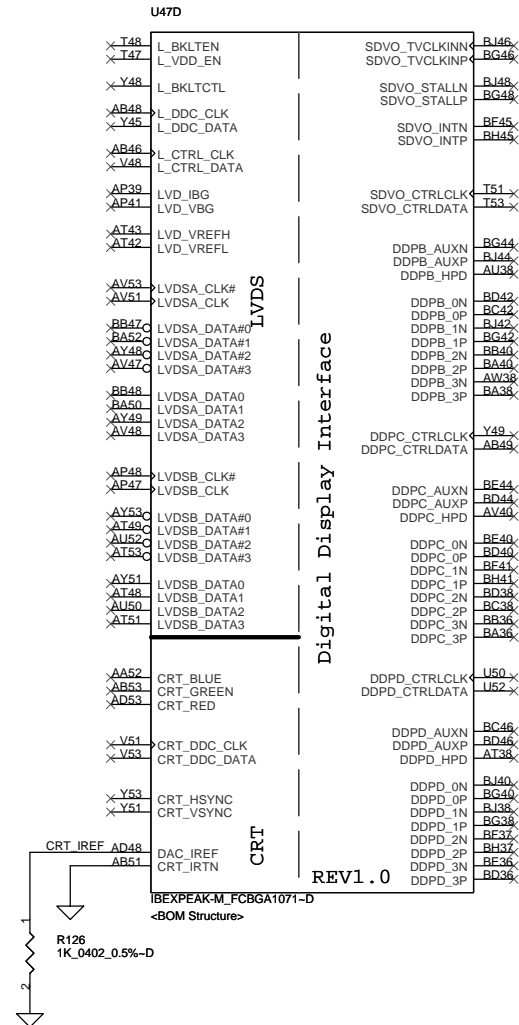
R0.3 Modify

XTAL25_IN should be pulled to
GND using a 0Ω resistor.
(Calpella_Schematic_Checklist_Rev1.6)

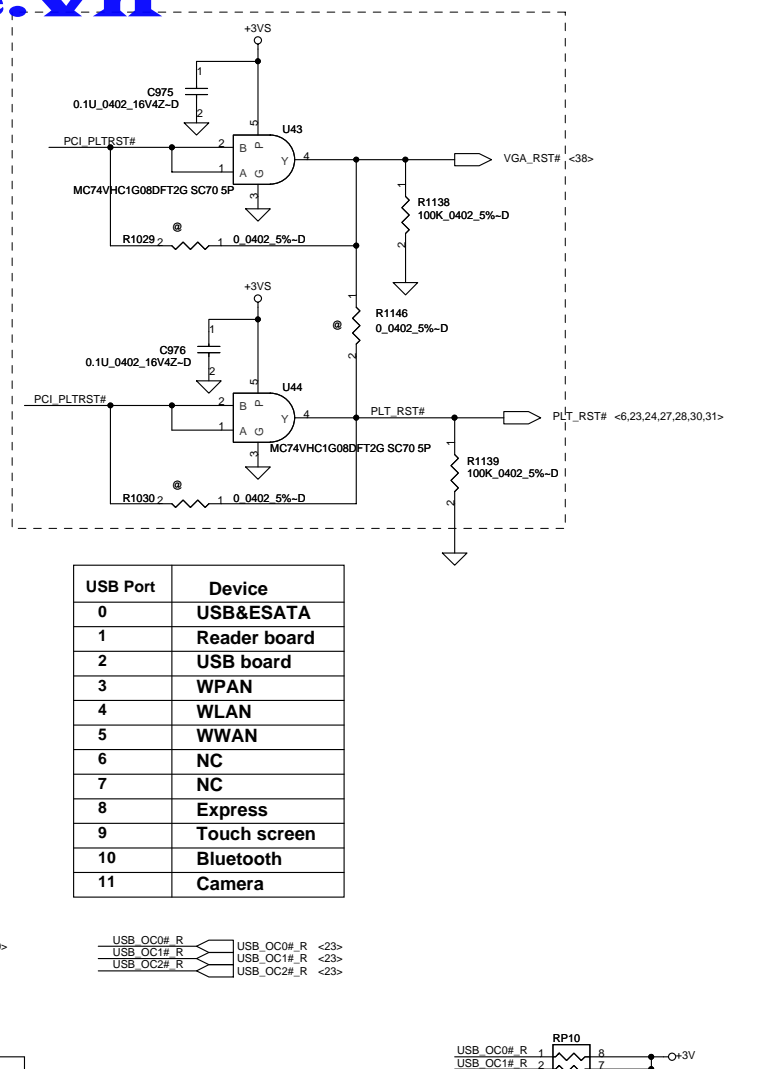
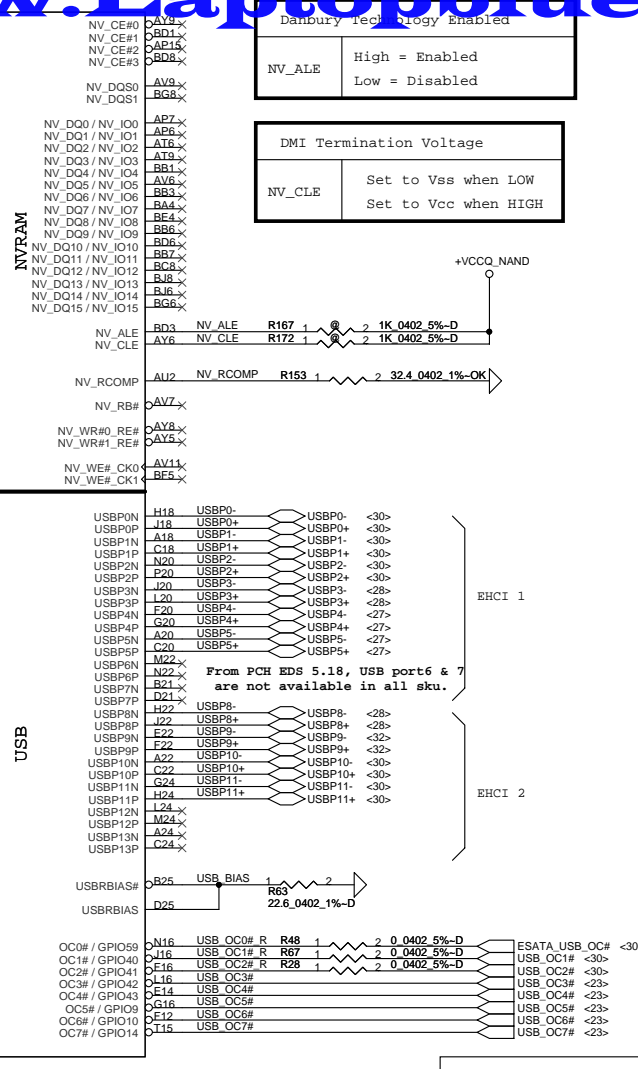
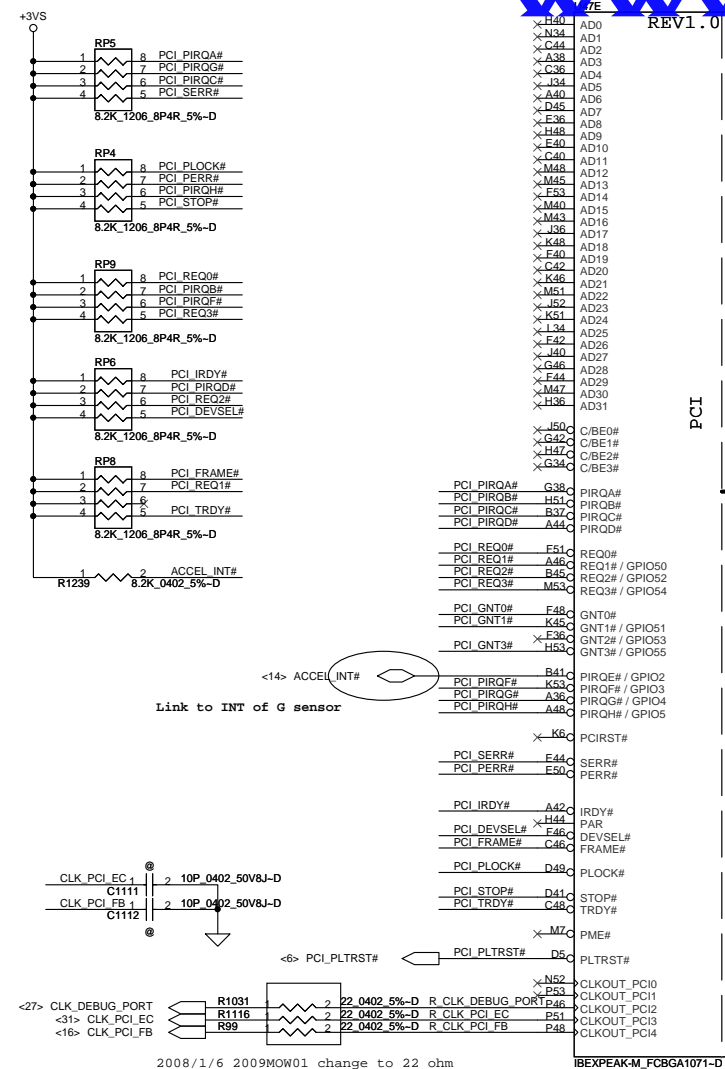


Note: remove 25MHz
crystal for ES2 silicon

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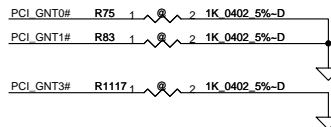


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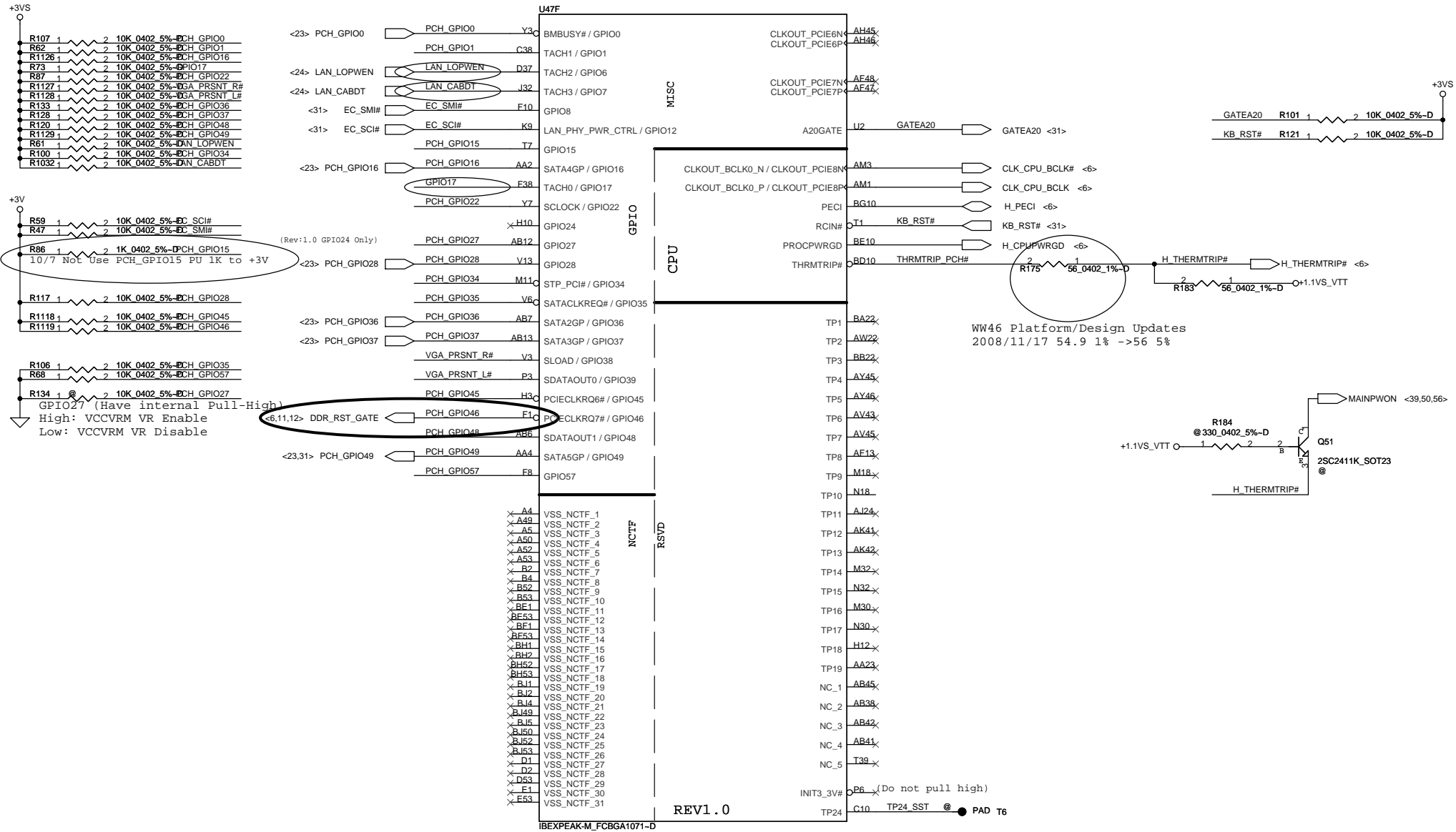
Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

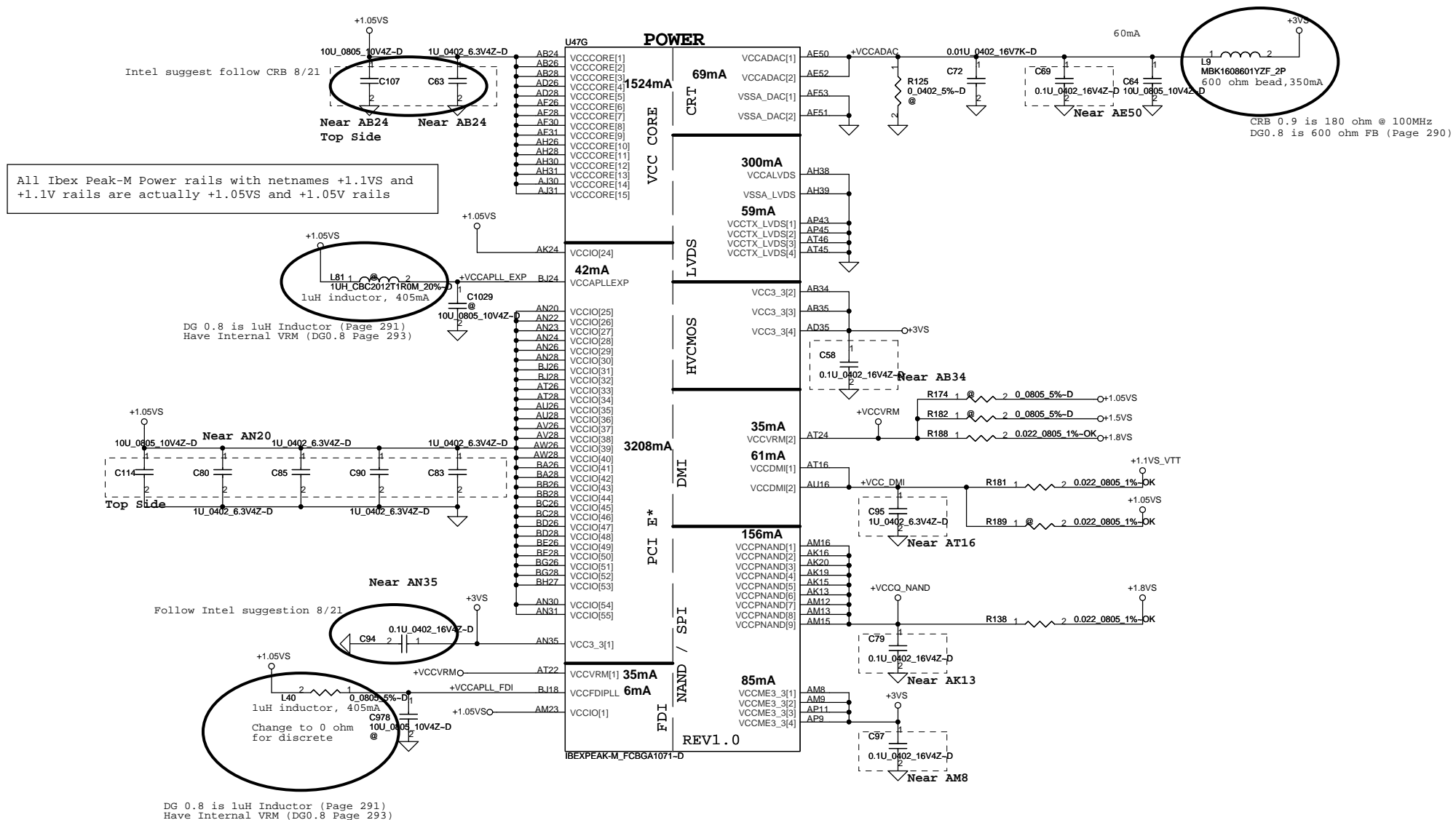
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



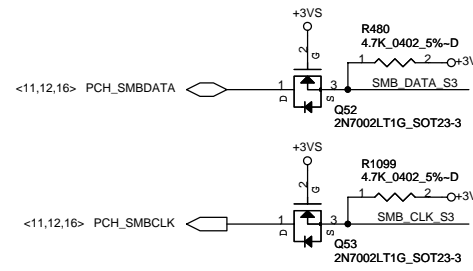
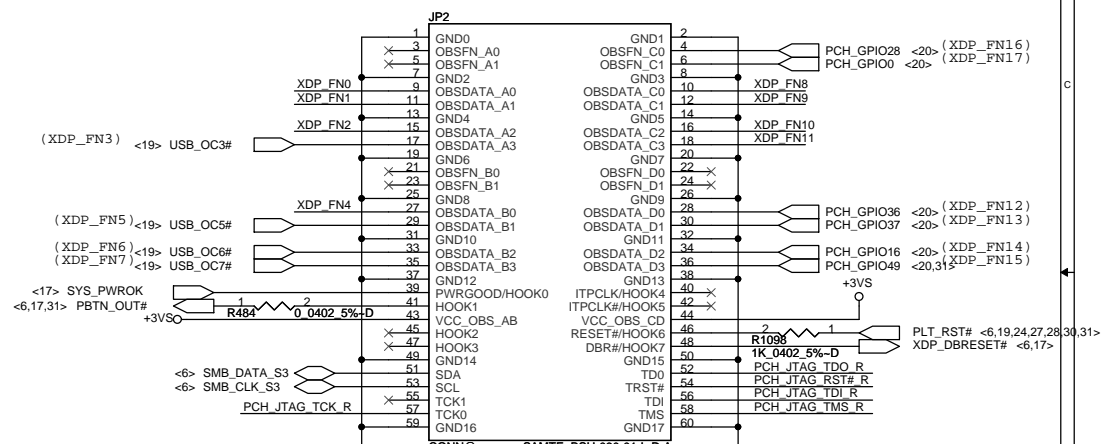
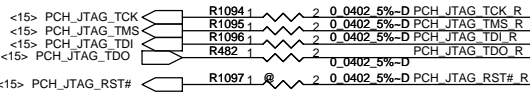
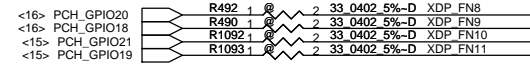
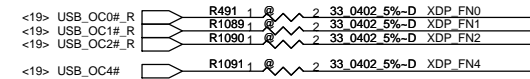
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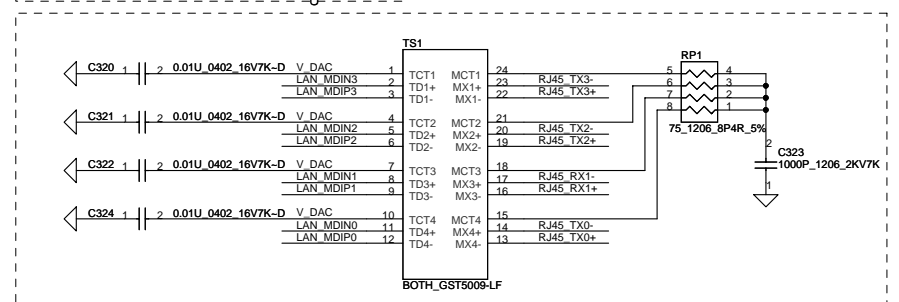
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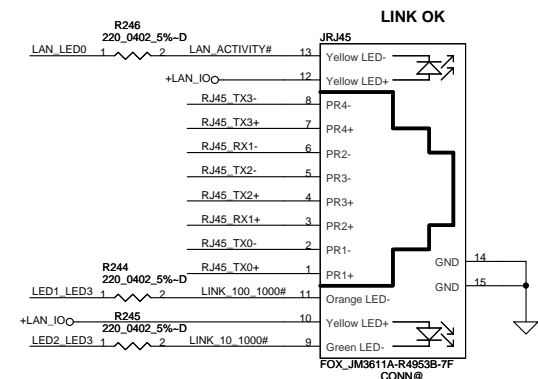
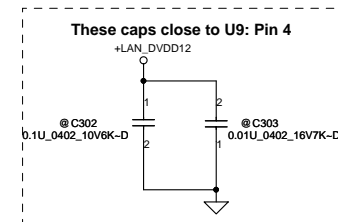
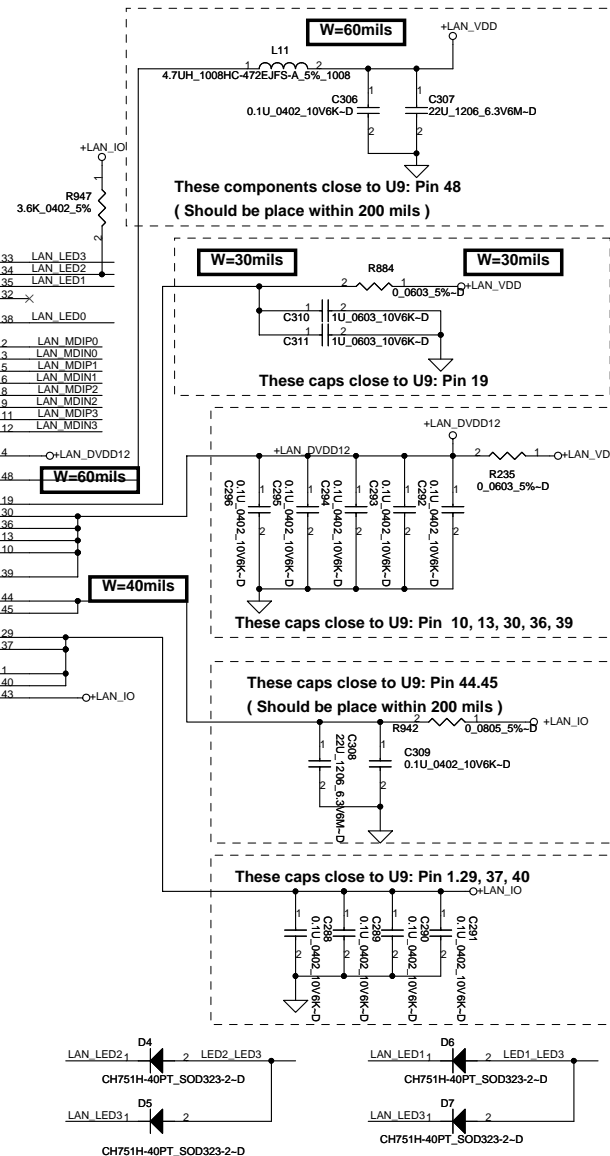


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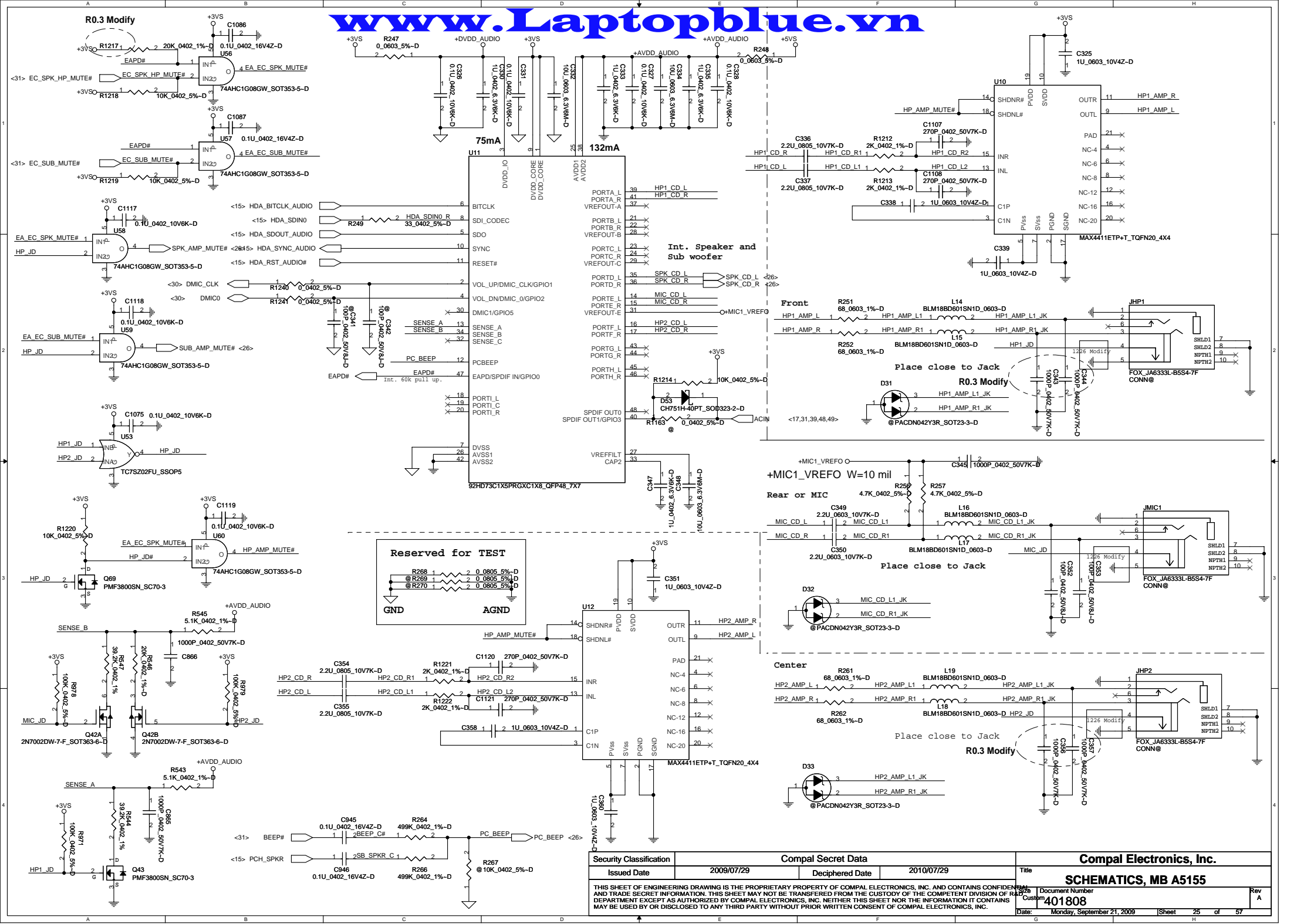


LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 / 100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT



12/11 reserve for EMI as Dell Tony request

LAN MDIN3	C873	1	2	6.8PF	0402	50V9-D
LAN MDIP3	C874	1	2	6.8PF	0402	50V9-D
LAN MDIN1	C875	1	2	6.8PF	0402	50V9-D
LAN MDIN2	C876	1	2	6.8PF	0402	50V9-D
LAN MDIP2	C877	1	2	6.8PF	0402	50V9-D
LAN MDIP1	C878	1	2	6.8PF	0402	50V9-D
LAN MDIN0	C879	1	2	6.8PF	0402	50V9-D
LAN MDIP0	C880	1	2	6.8PF	0402	50V9-D



R0.3 Modify

R0.3 Modify

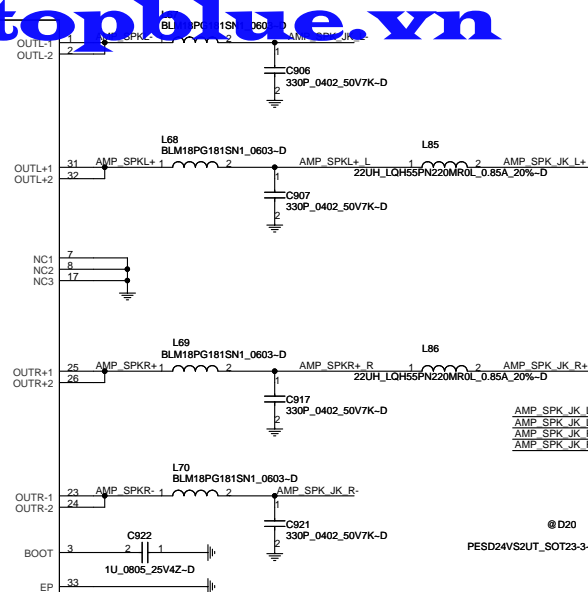
High-Pass Filter, $f_c=500\text{Hz}$, $A_v=1.45\text{V/V}$

R0.3 add

R0.3 Modify

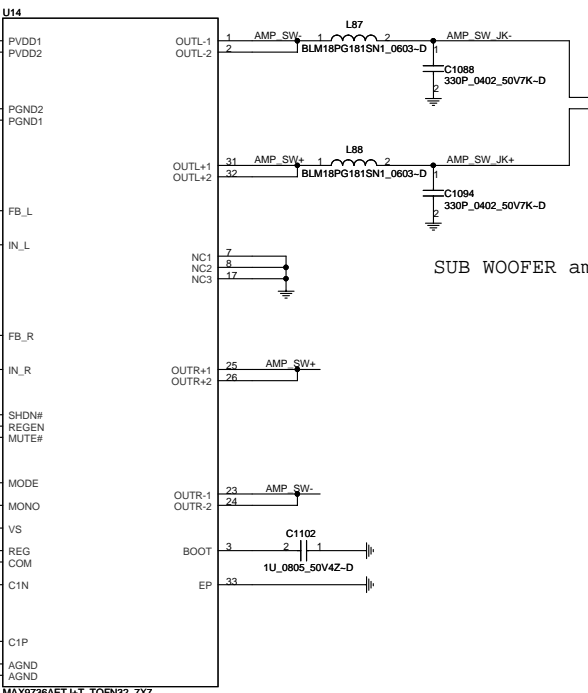
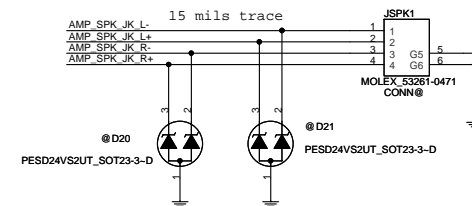
High-Pass Filter, $f_c=100\text{ Hz}$, 500Hz , $A_v=1.45\text{V/V}$

R1.0 add



Speaker amp impedance of JBL is 4 ohm.

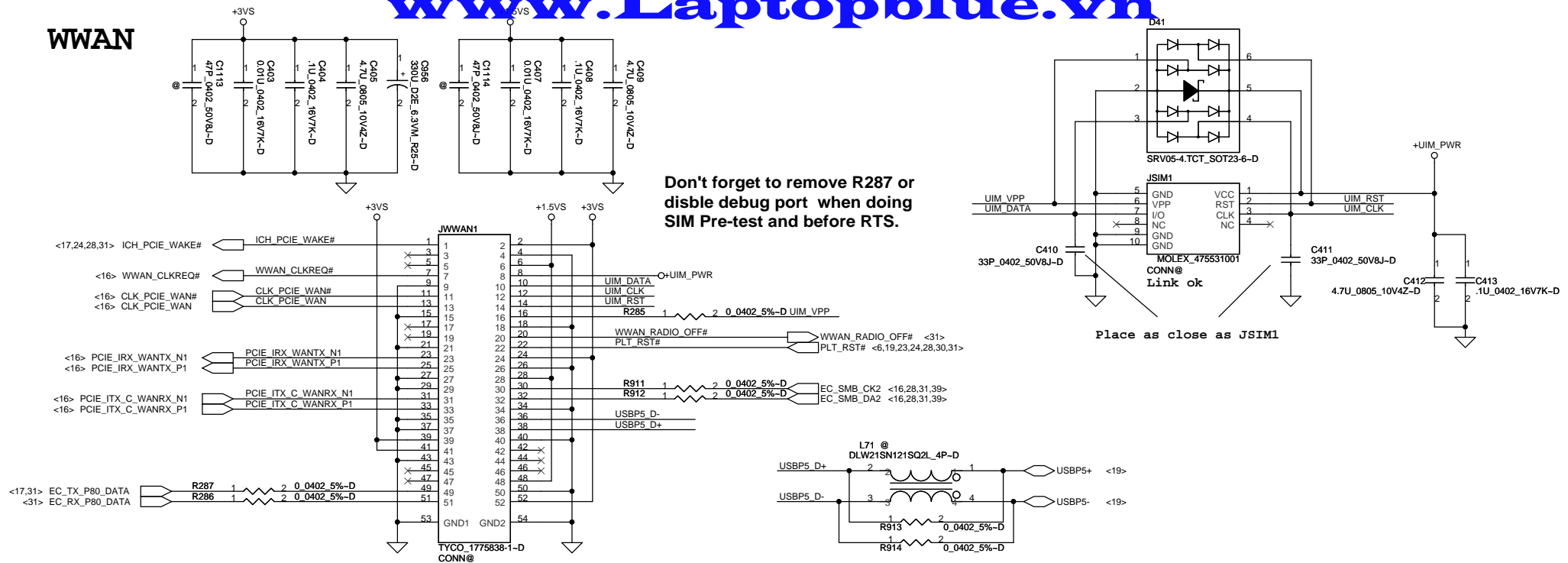
Speaker Connector



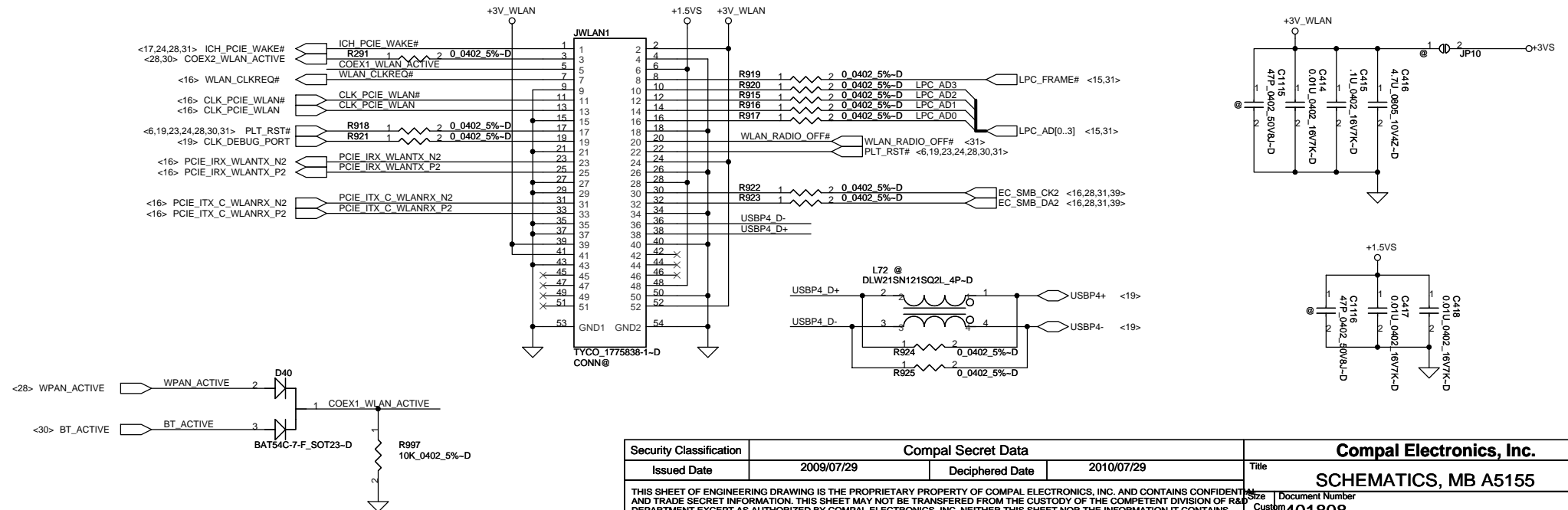
SUB WOOFER amp impedance of JBL is 4 ohm.

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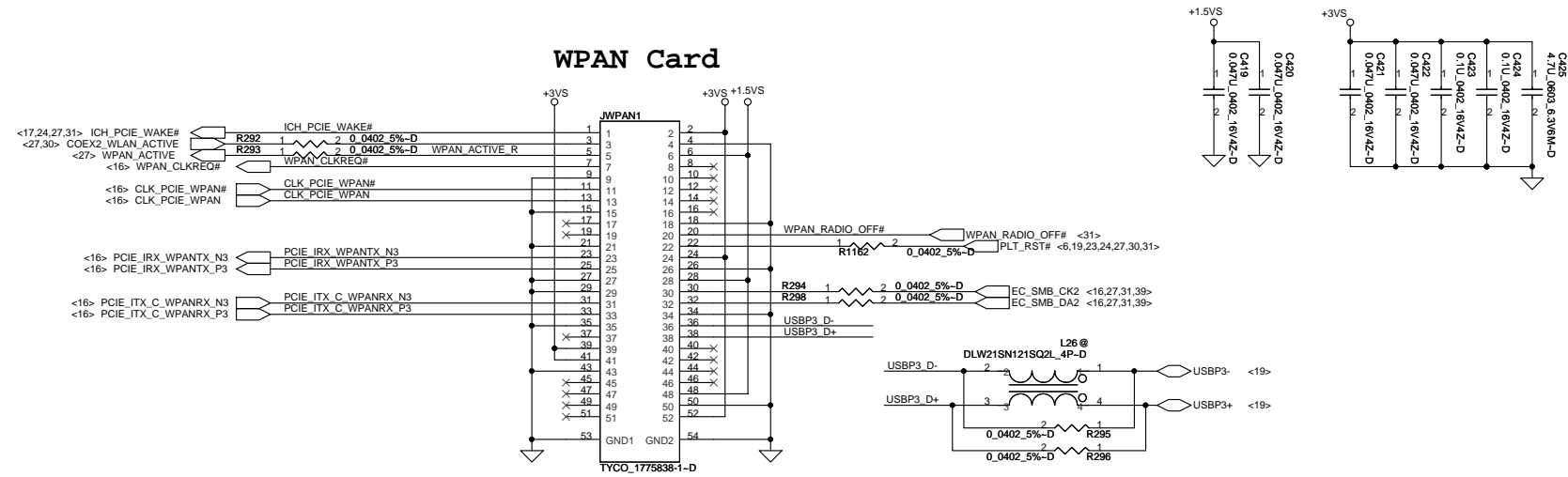
WWAN



WLAN



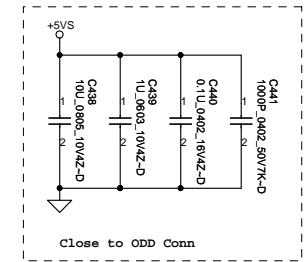
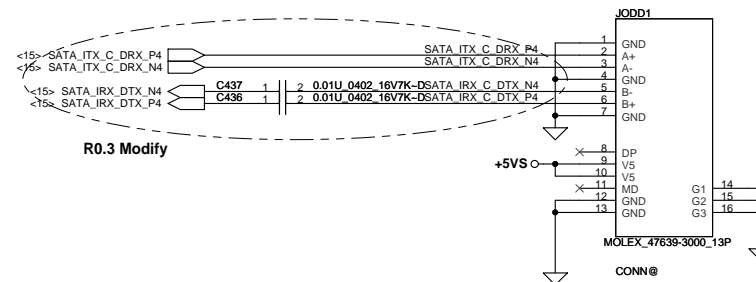
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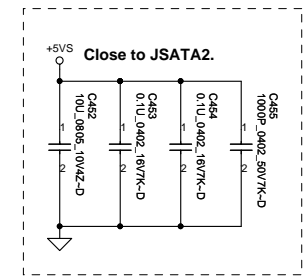
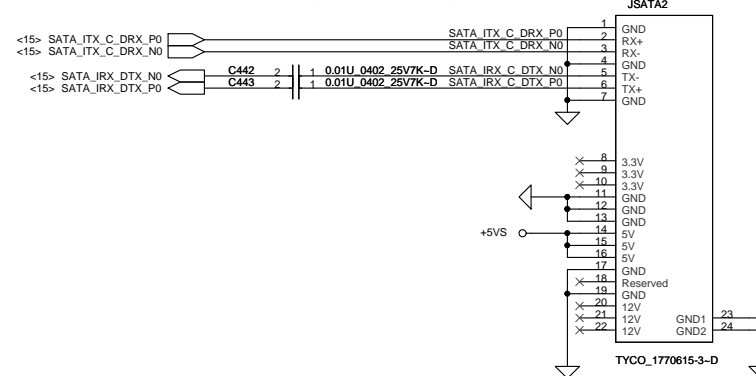
Express Card Power Switch

Express Card

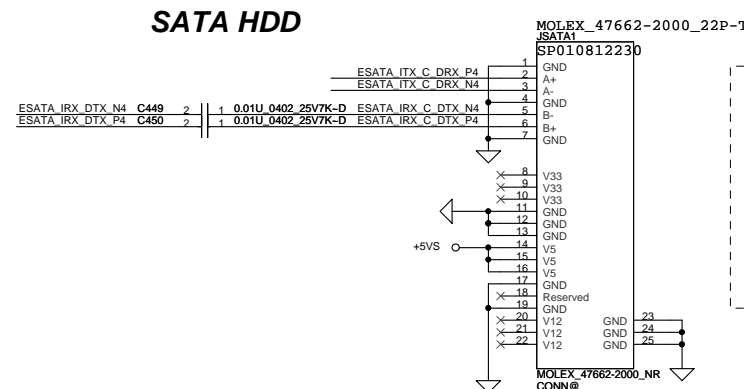
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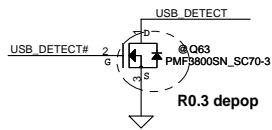
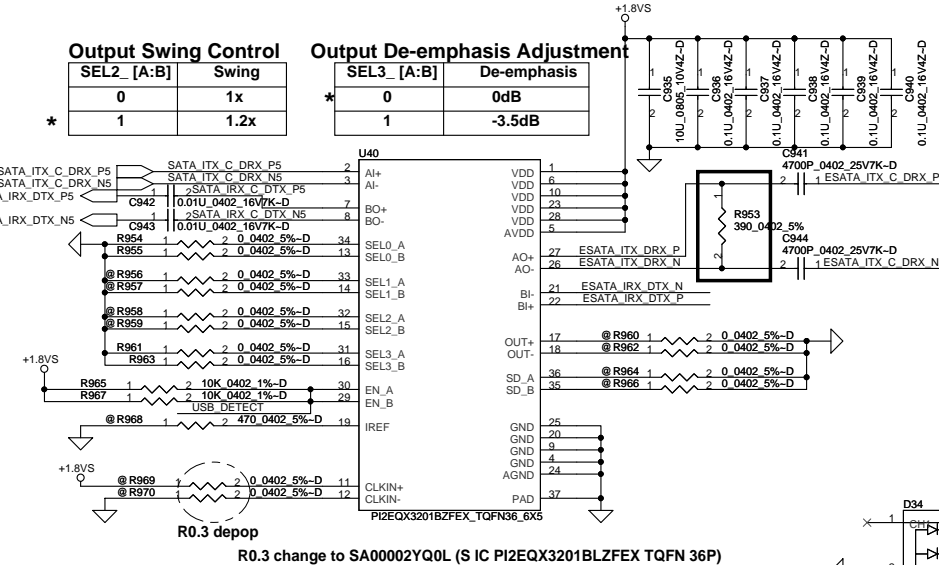
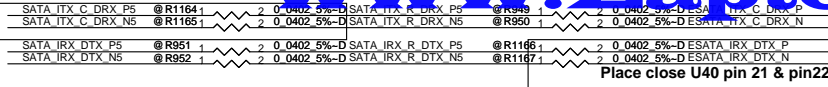
SATA HDD (On board)



SATA HDD

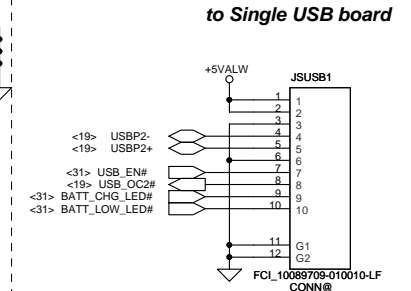
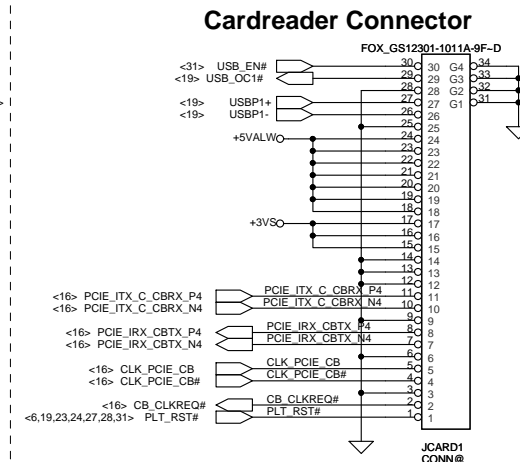
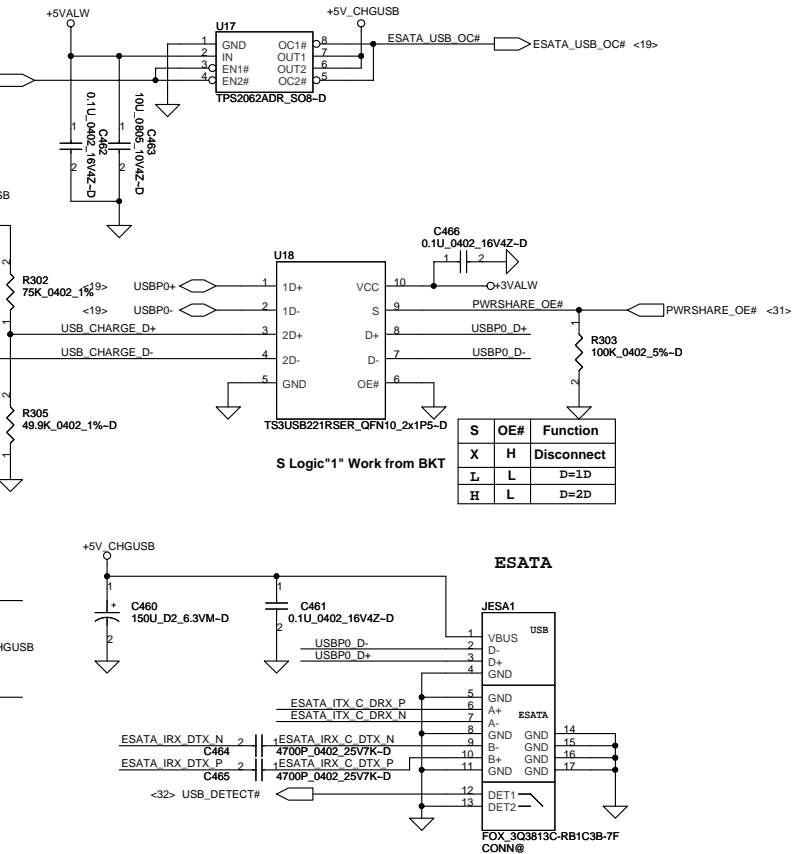
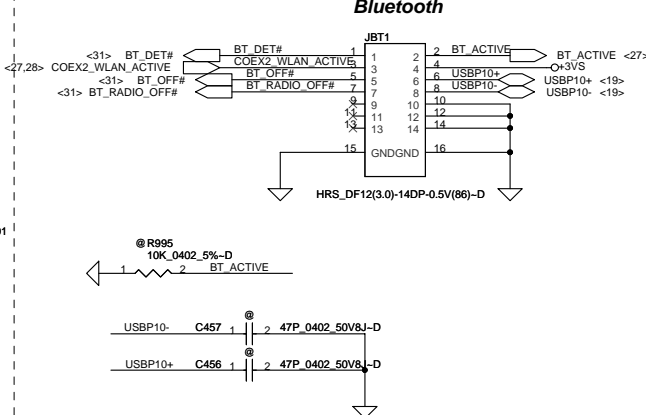
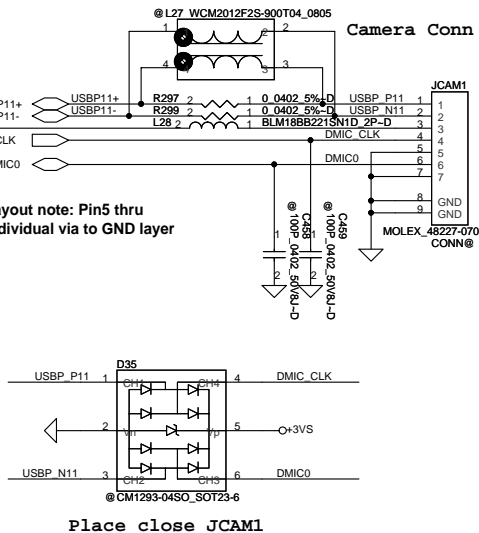


Place close U40 pin 2 & pin3

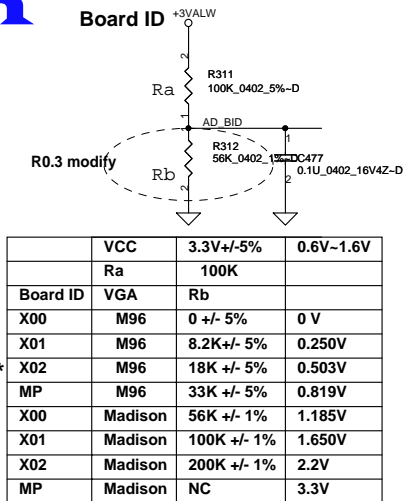
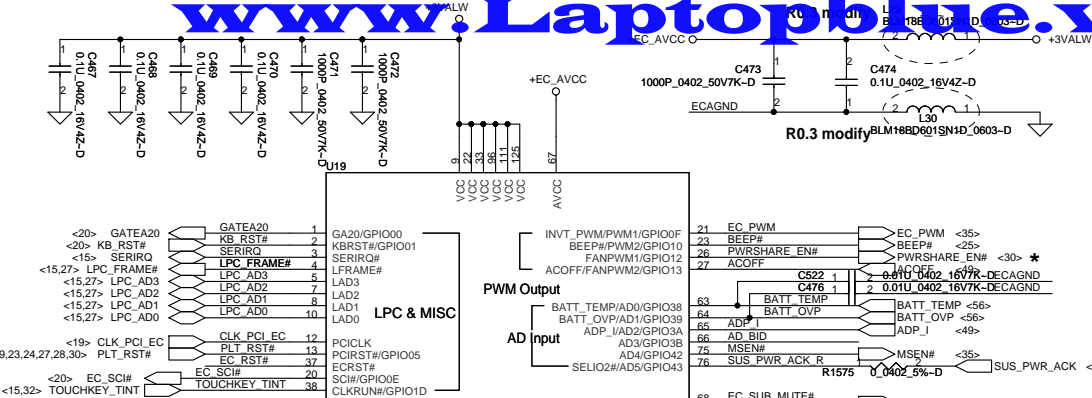
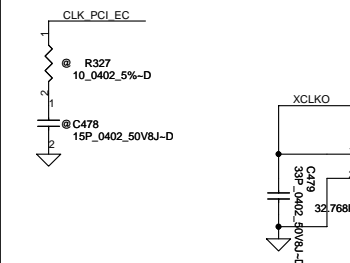
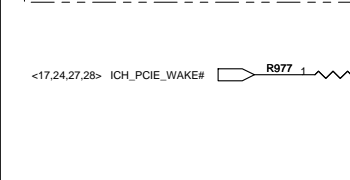
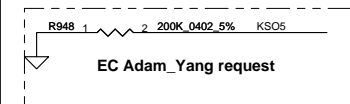
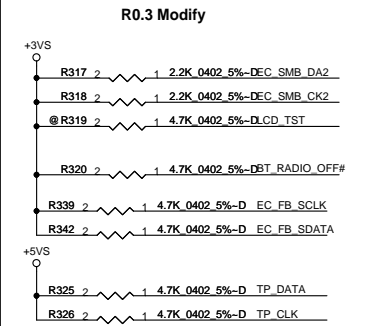
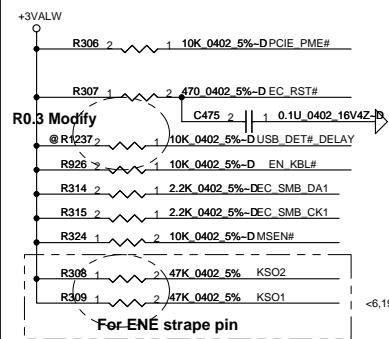


R0.3 depop

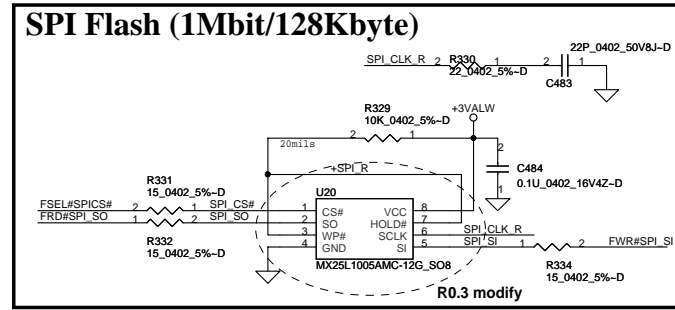
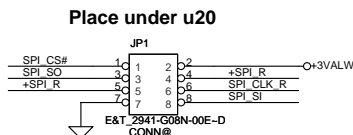
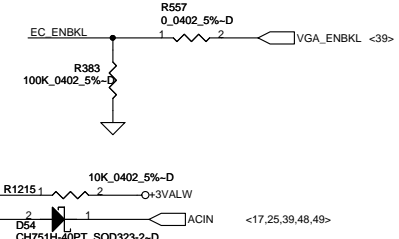
R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)



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Follow the suggestion of EC team to follow JAT10 setting.

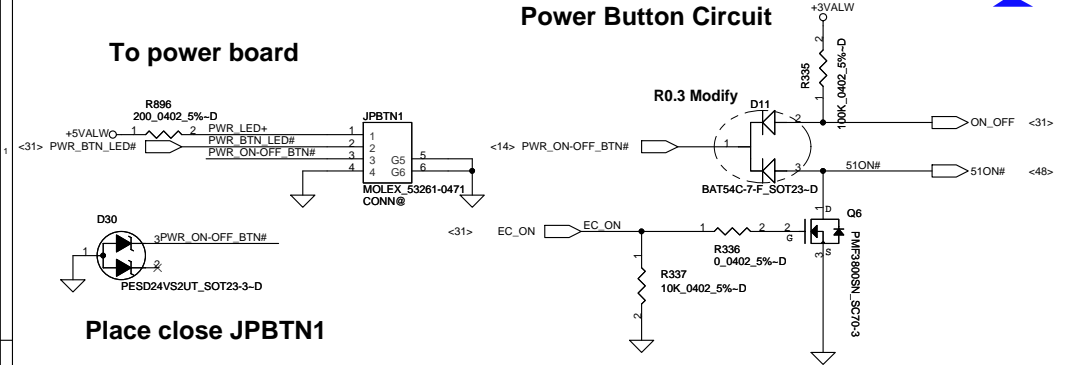


D3 Version : P/N : SA00001J580

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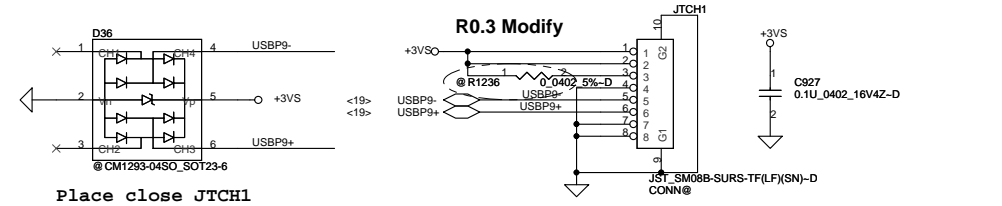
To power board

Power Button Circuit

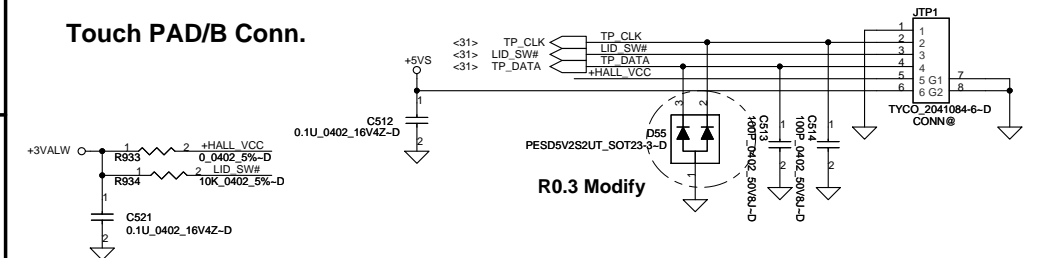


Place close JPBTN1

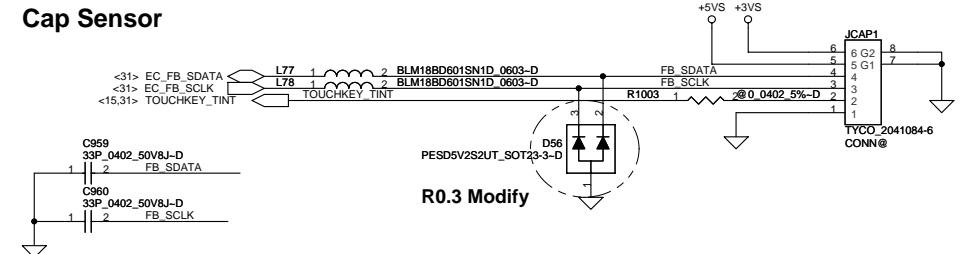
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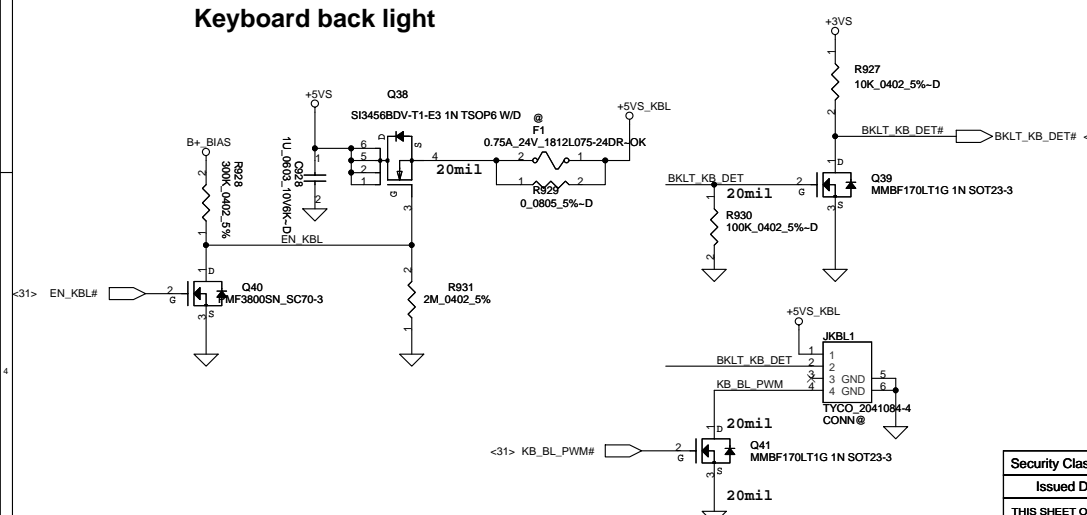
Touch PAD/B Conn.



Cap Sensor

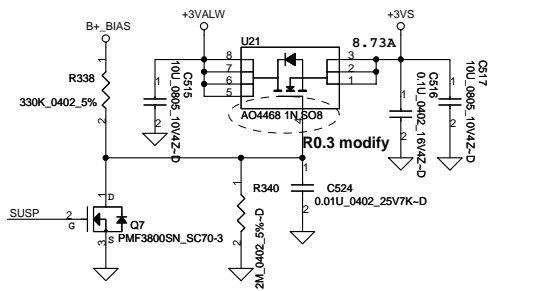


Keyboard back light

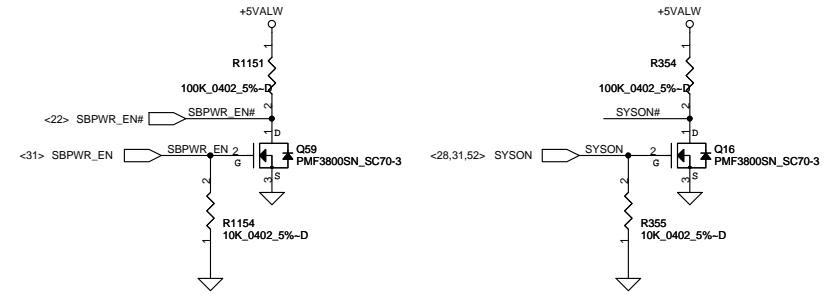
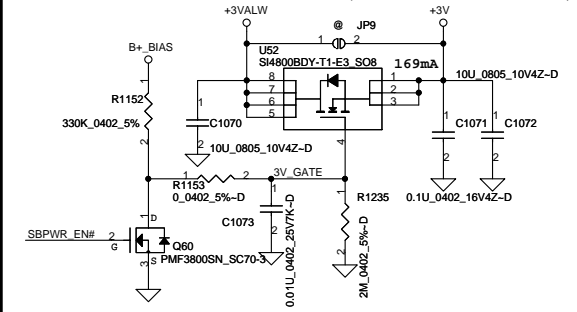


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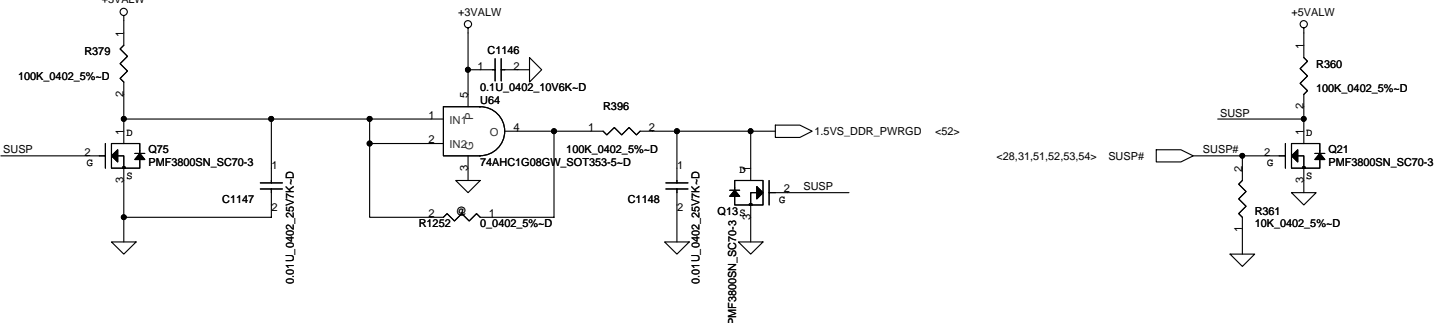
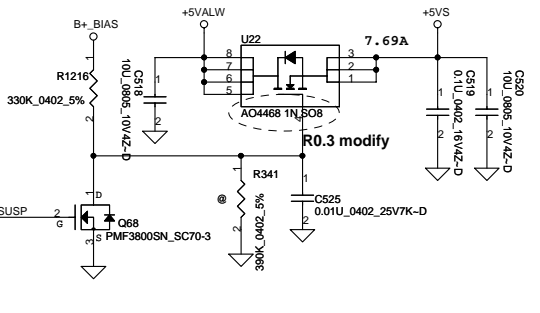
+3VALW to +3VS Transfer



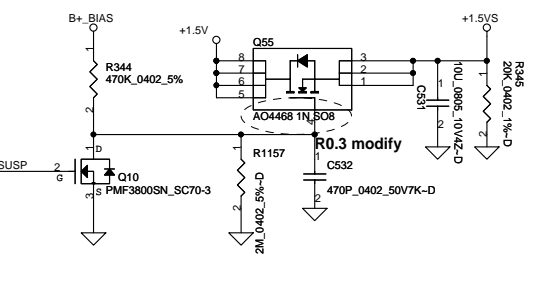
+3VALW to +3V Transfer (I/O AUX LOW)



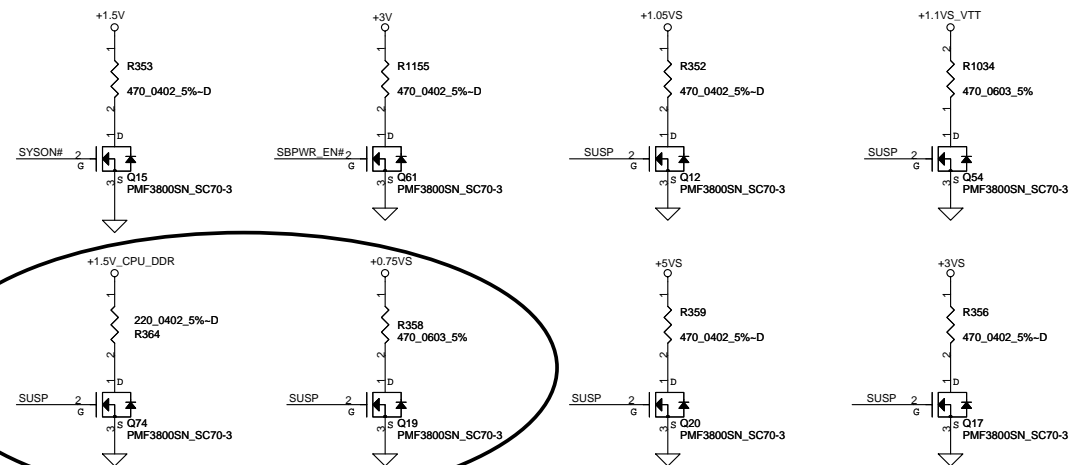
+5VALW to +5VS Transfer



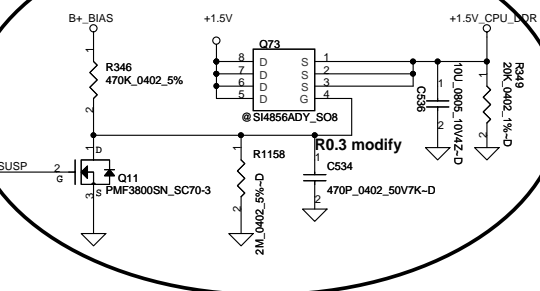
+1.5V to +1.5VS Transfer



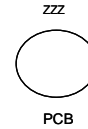
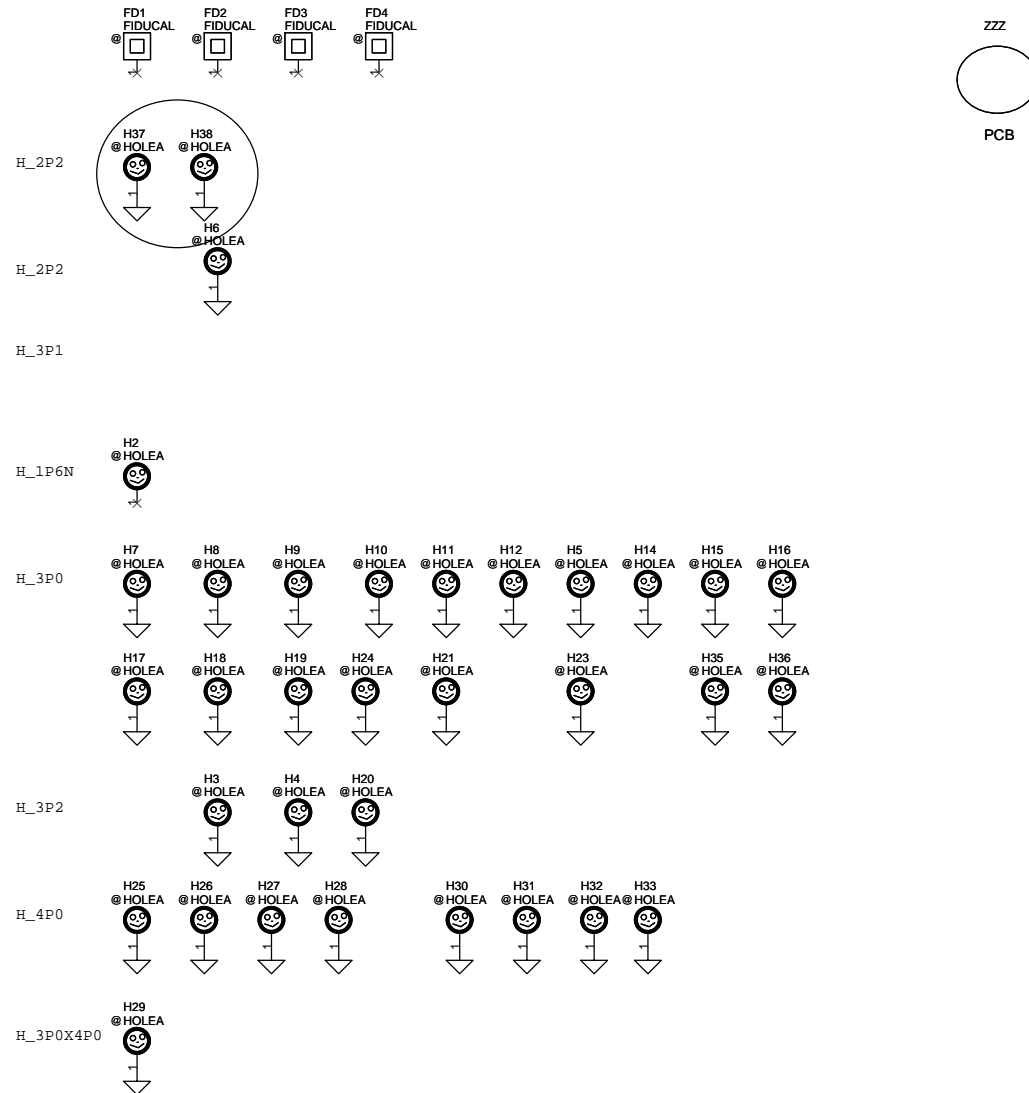
Discharge Circuit



+1.5V to +1.5VS_DDR Transfer



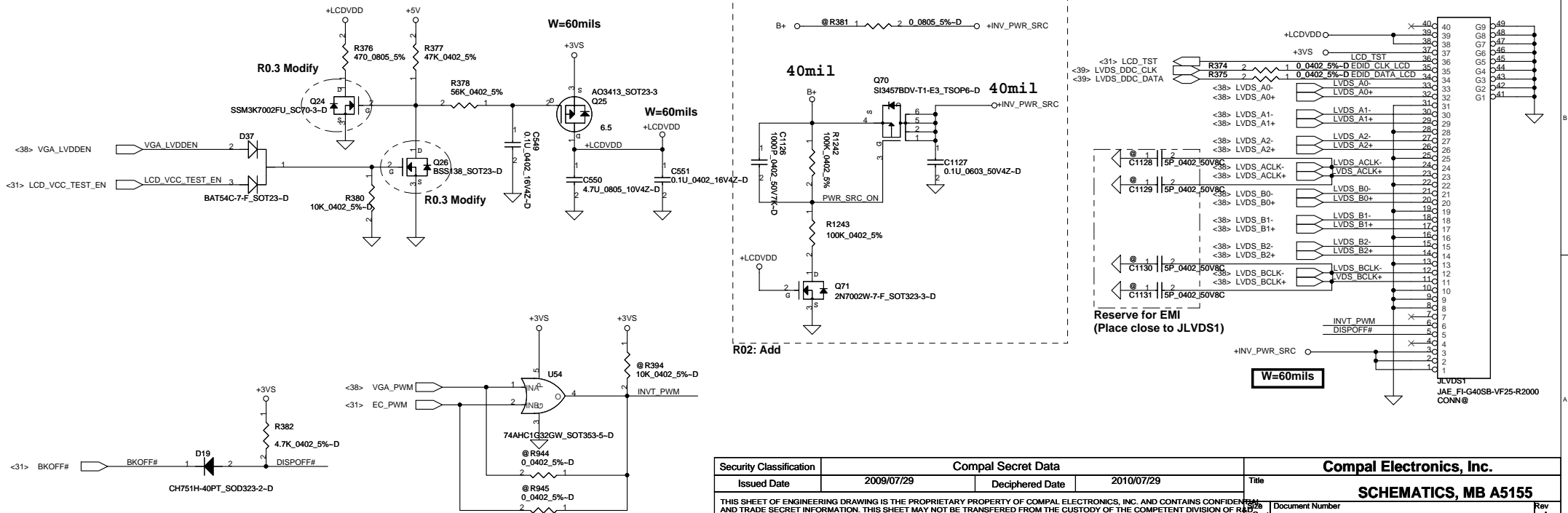
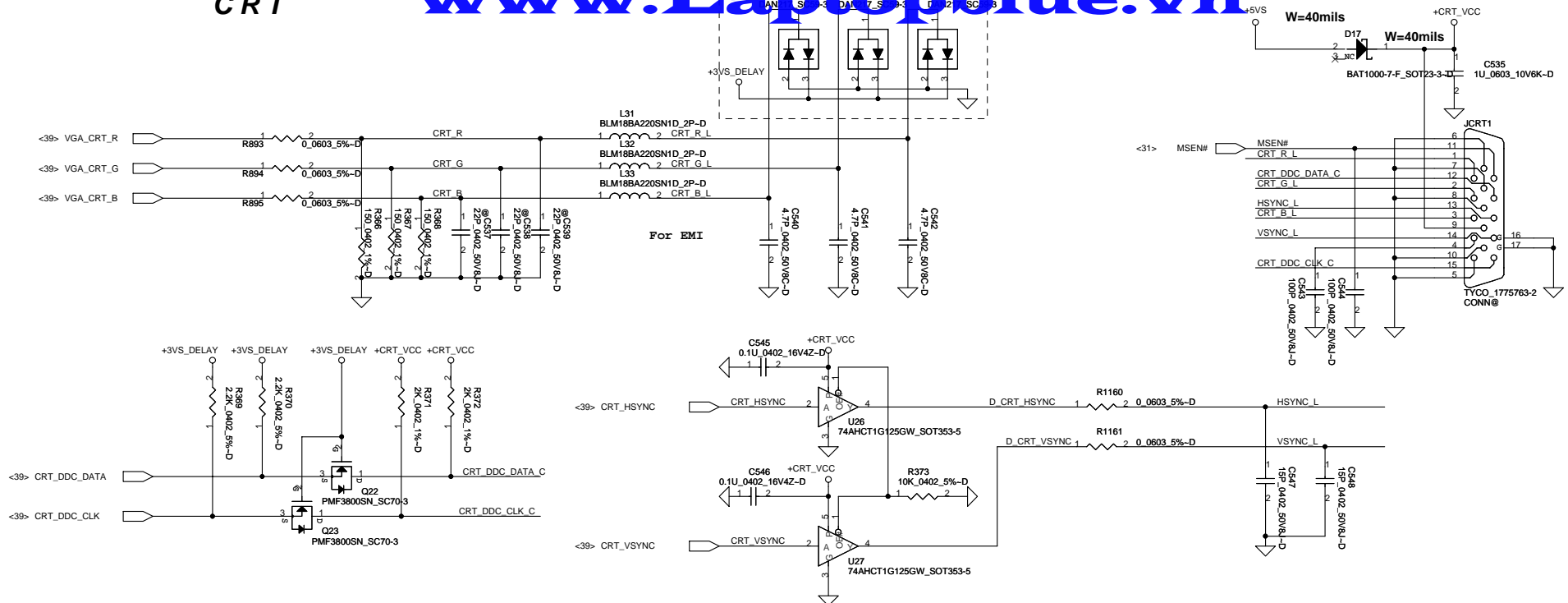
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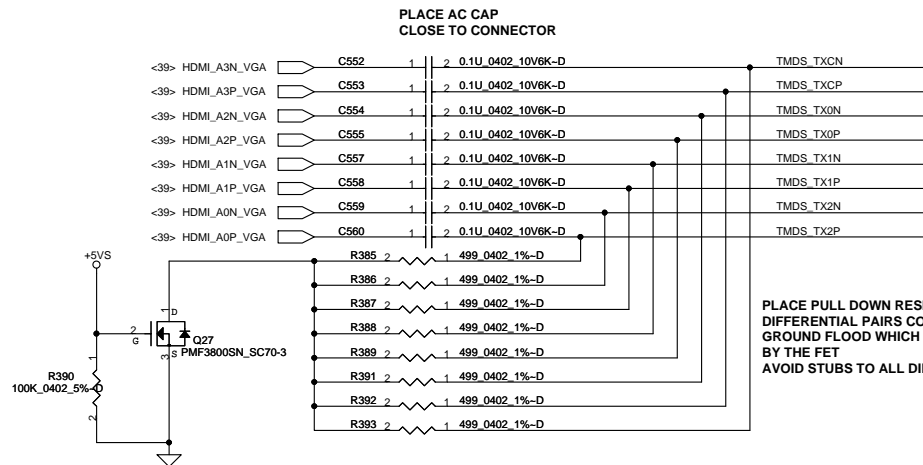
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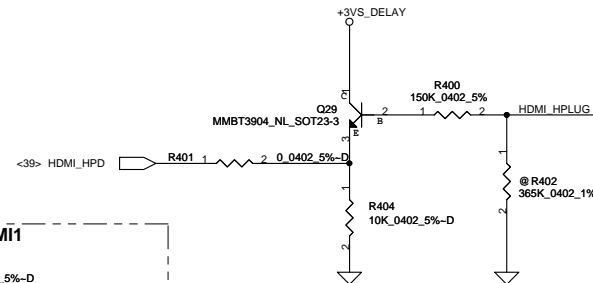
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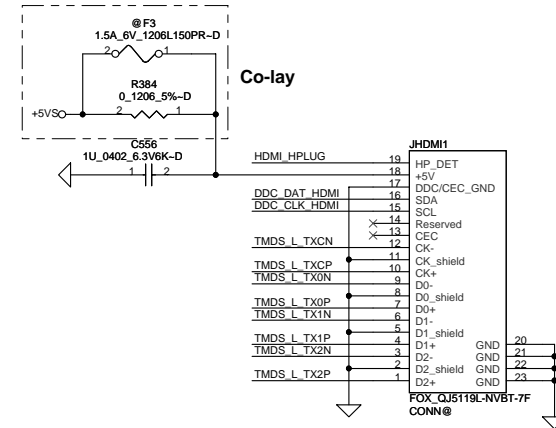
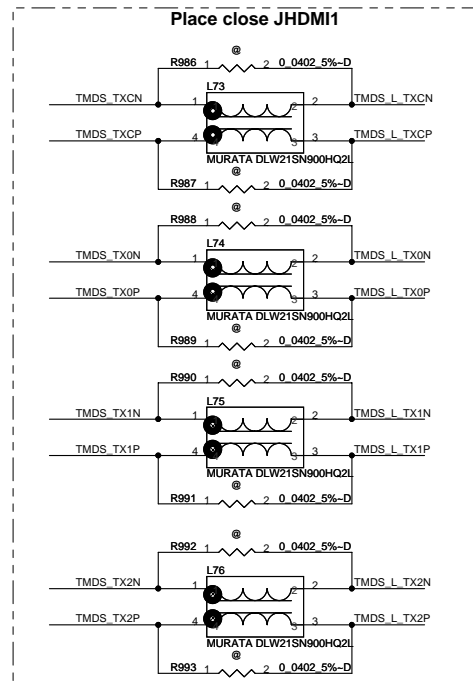
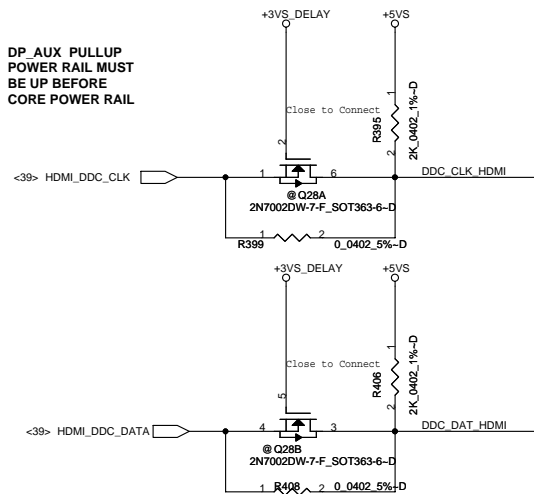
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PLACE PULL DOWN RESISTORS CLOSE TO
DIFFERENTIAL PAIRS CONNECTED TO SOLID
GROUND FLOOD WHICH IS CONTROLLED
BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

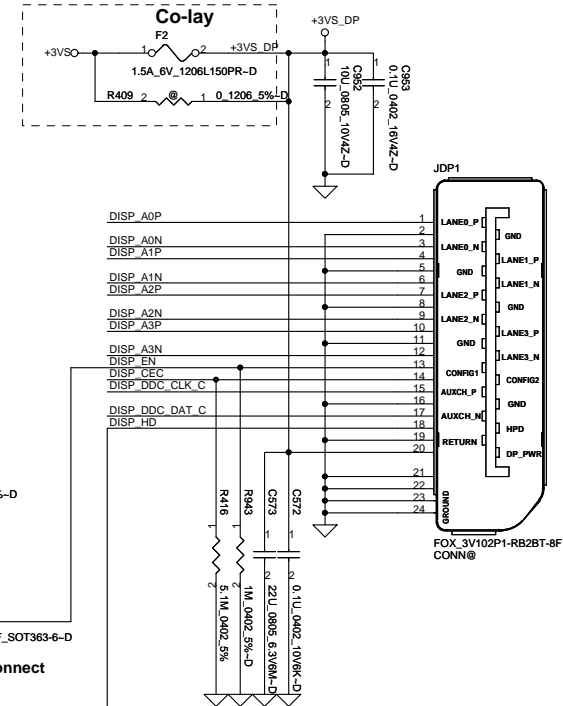
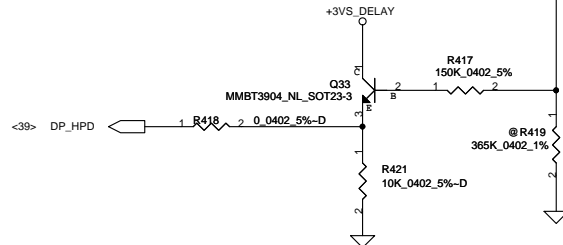
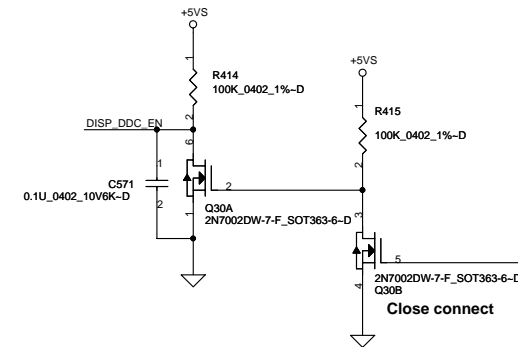
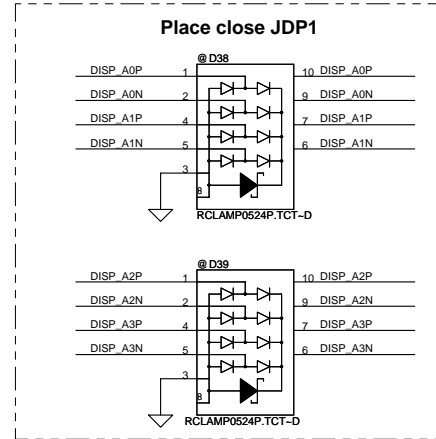
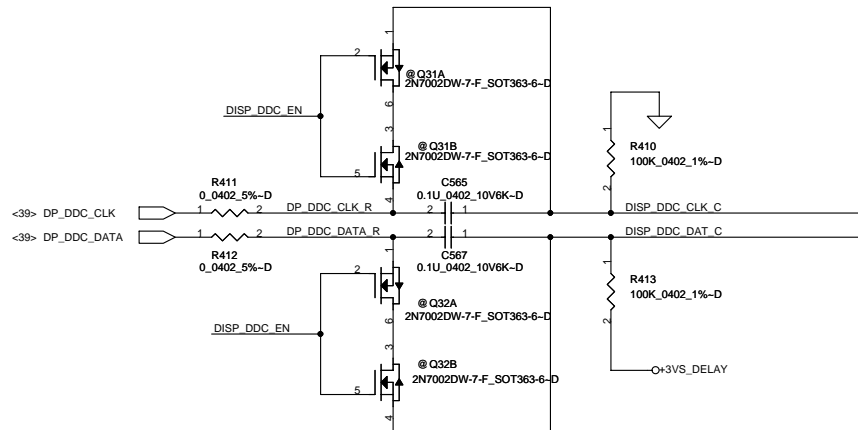


DP_AUX PULLUP
POWER RAIL MUST
BE UP BEFORE
CORE POWER RAIL



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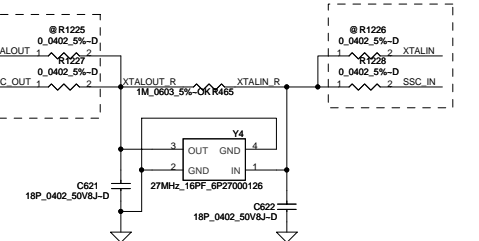
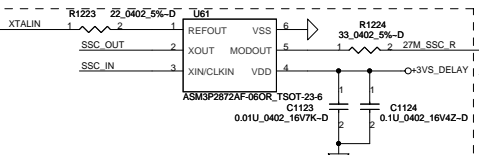
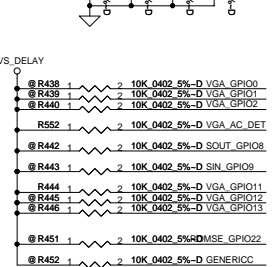
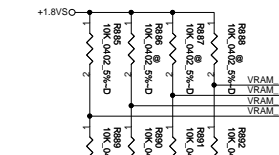
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<39> DISP_A2N_VGA	C565	2	1	0.1U_0402_10V6K-D	DISP_A2N
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<39> DISP_A3N_VGA	C569	2	1	0.1U_0402_10V6K-D	DISP_A3N
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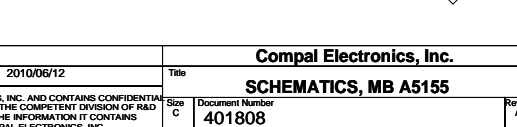
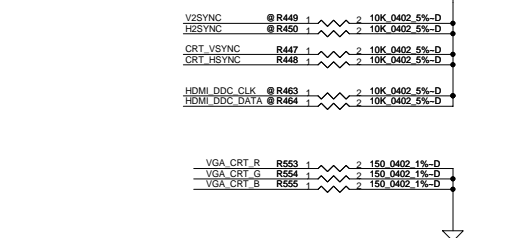
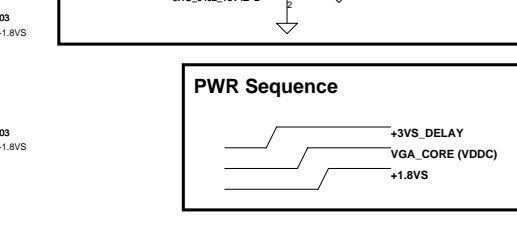
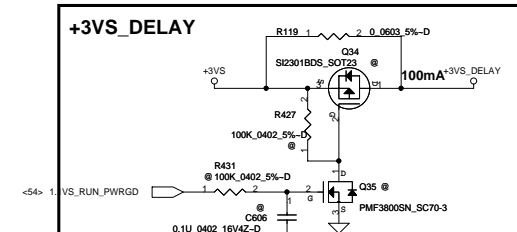
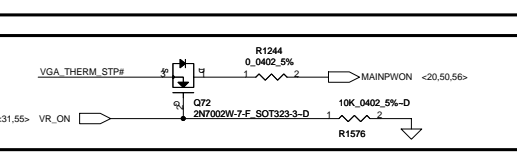
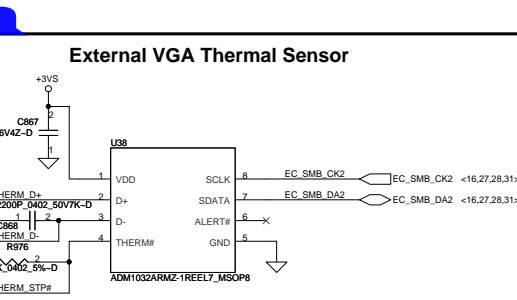
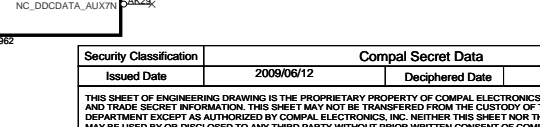
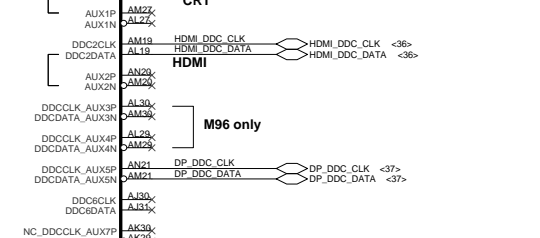
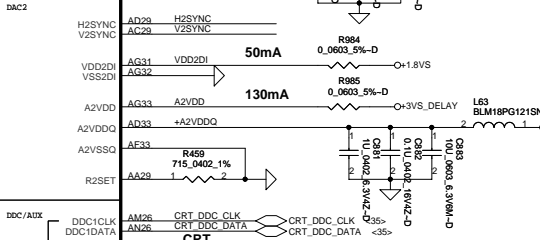
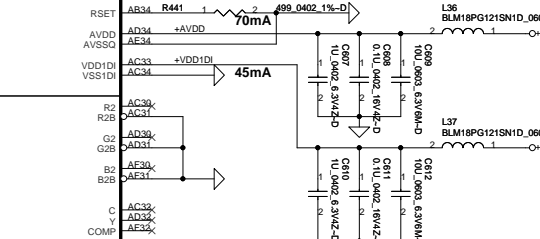
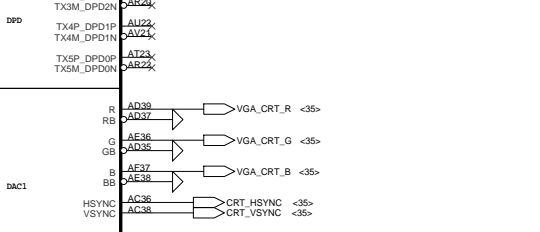
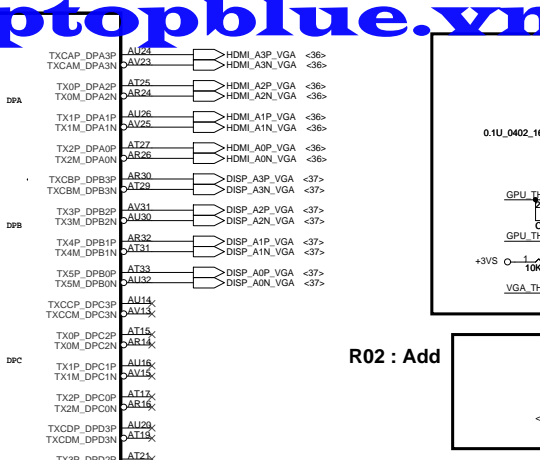
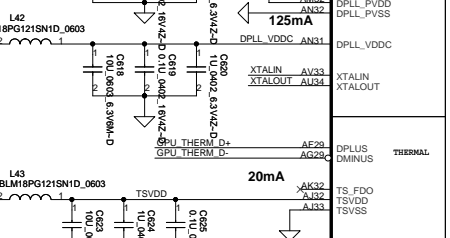
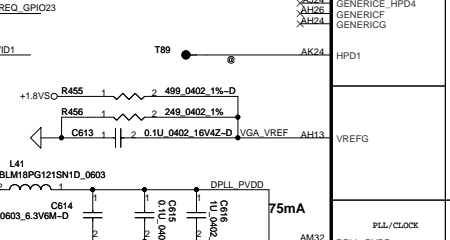
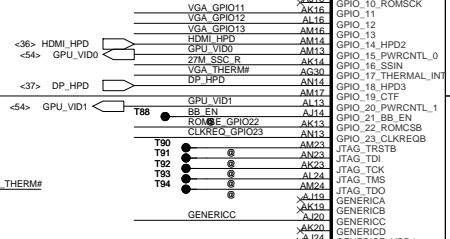
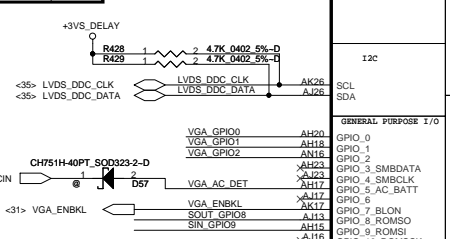
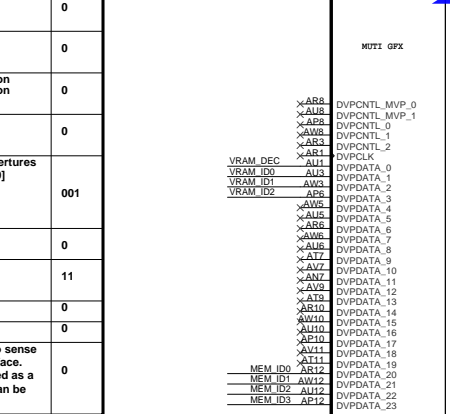
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Strap Name		Pin Straps description	
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF_CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 256 MB 001 512 MB 010 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

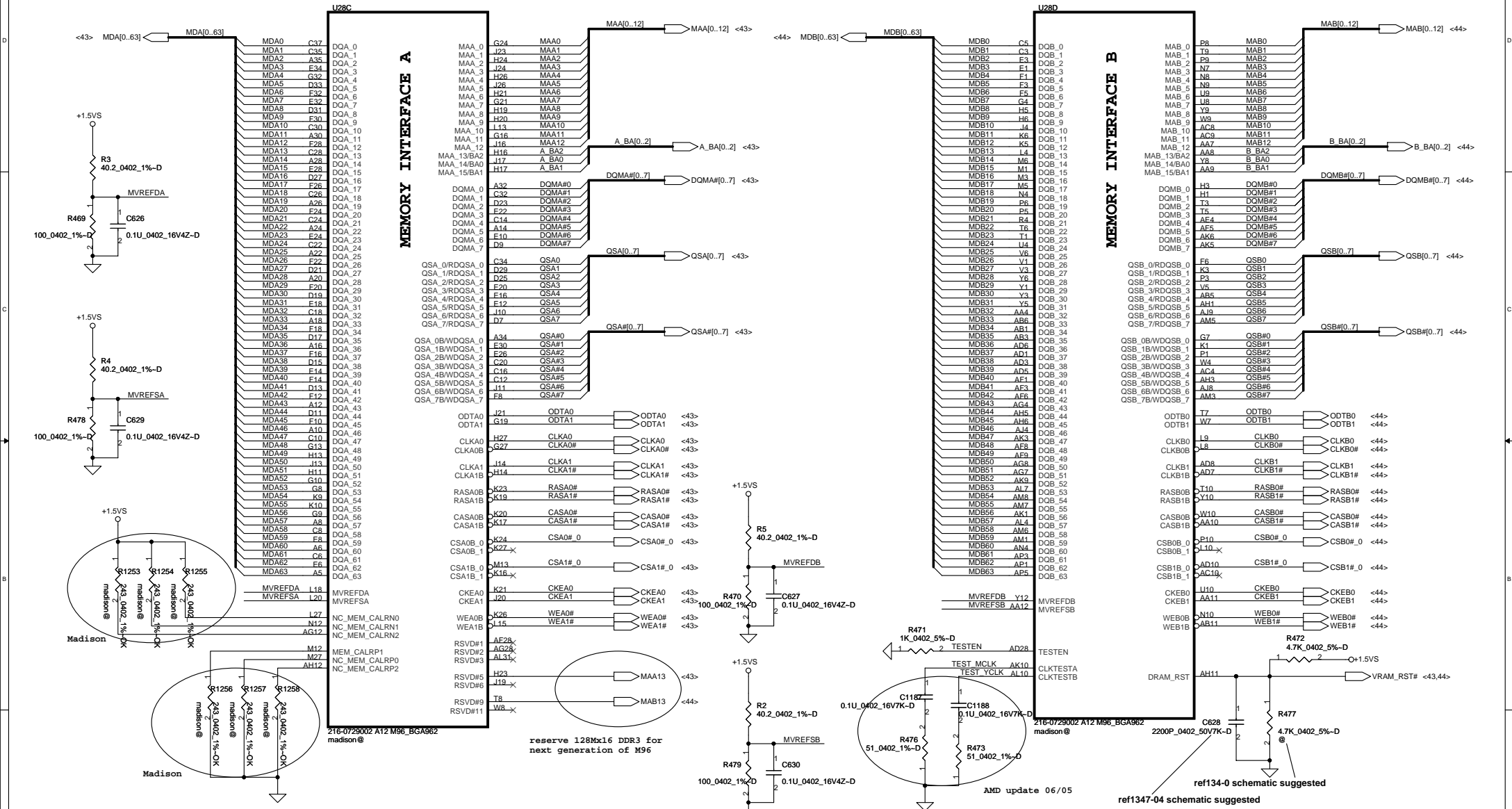
Location	MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3
VRAM				
Samsung	0	0	0	0
HYNIX	1	0	0	0



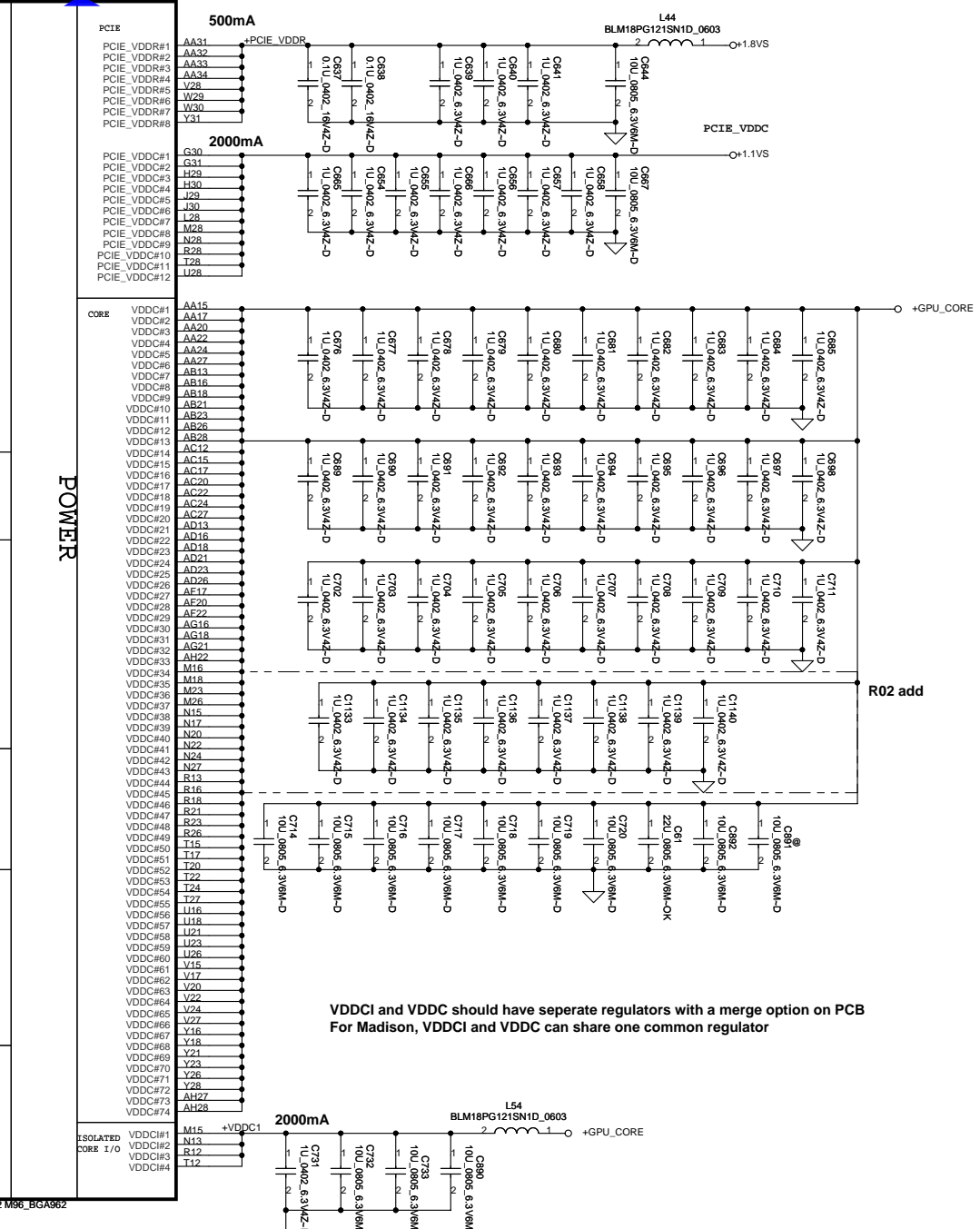
www.Laptopblue.vn



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Title		
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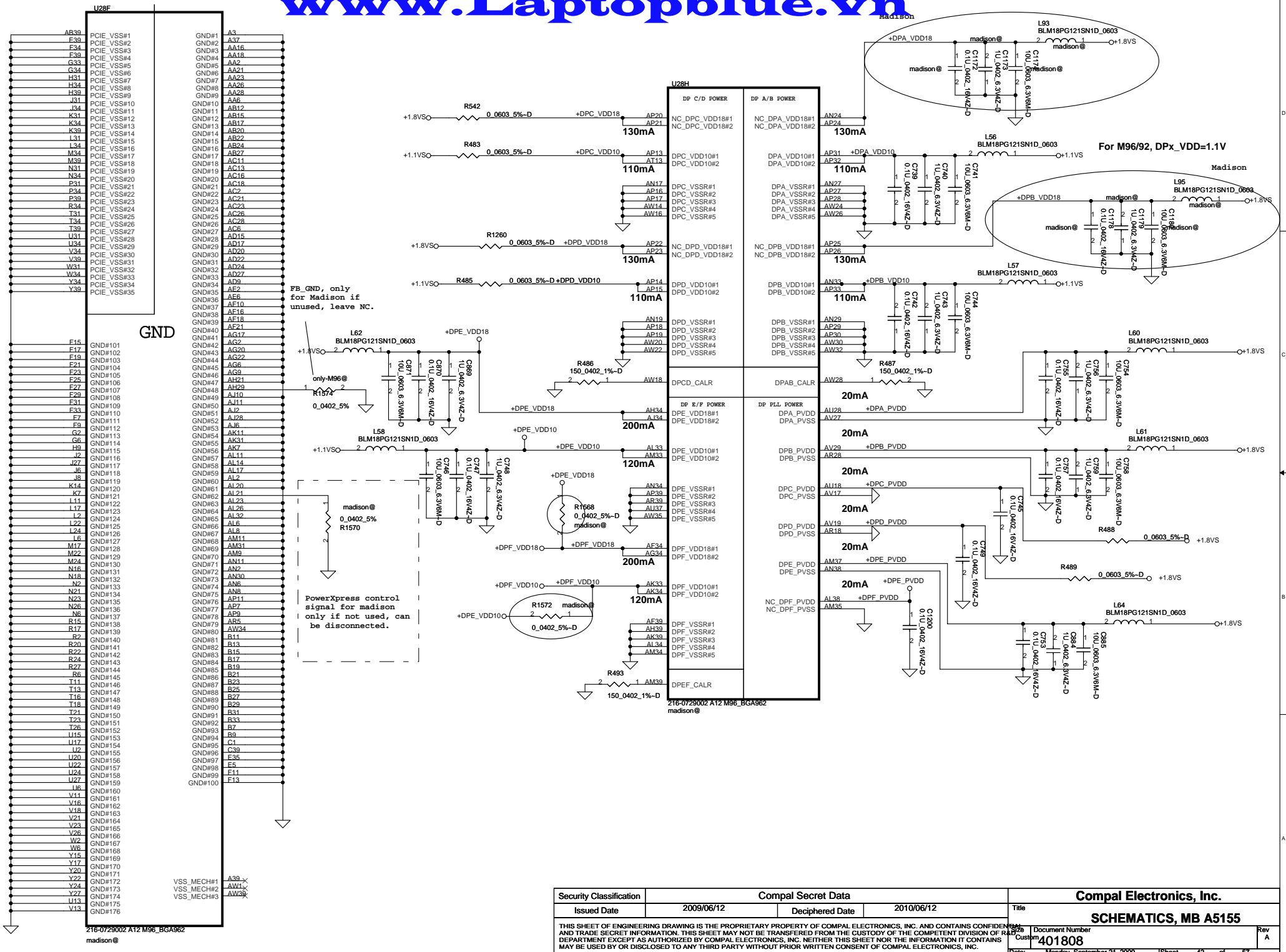


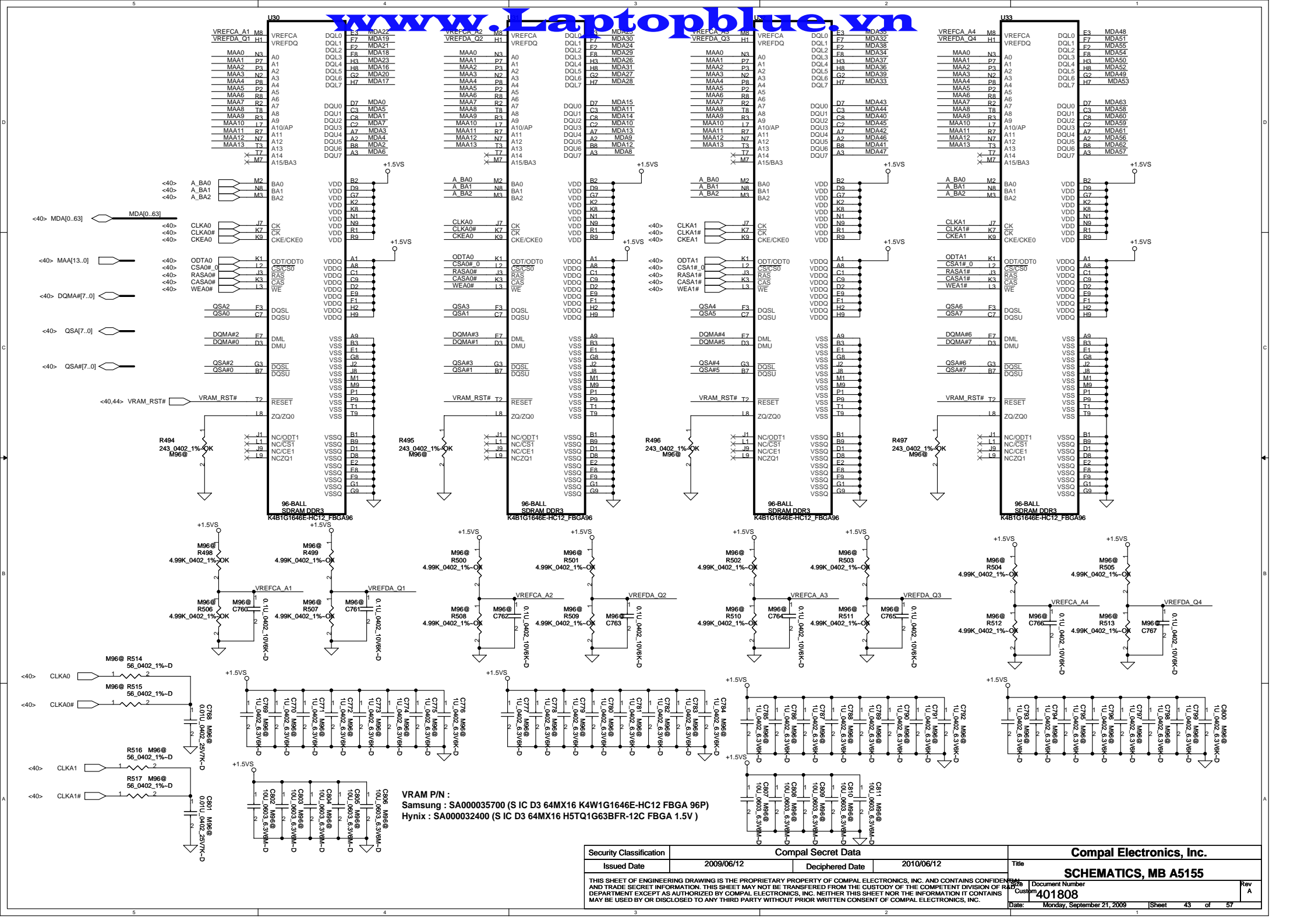
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VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, VDDCI and VDDC can share one common regulator

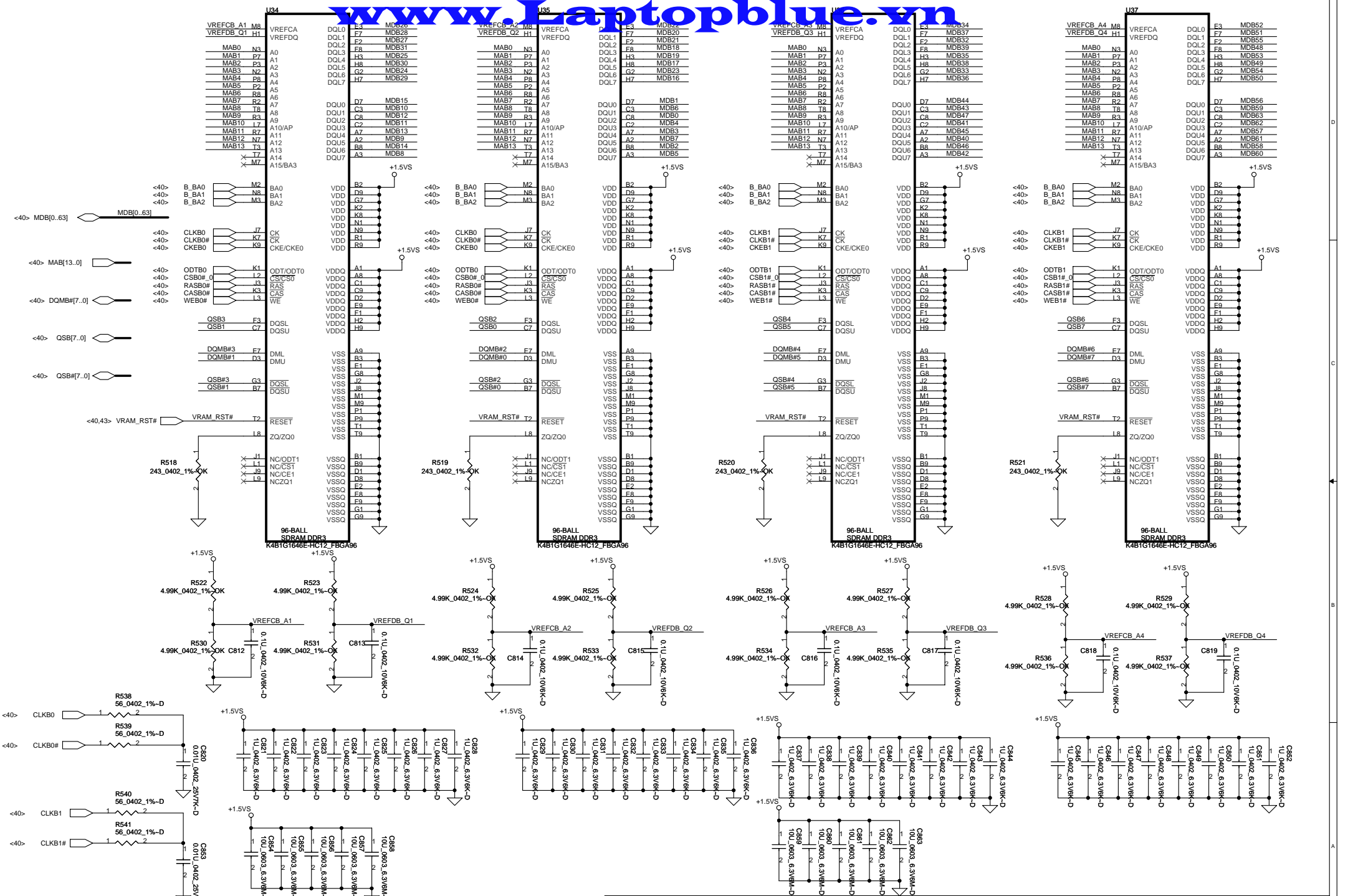
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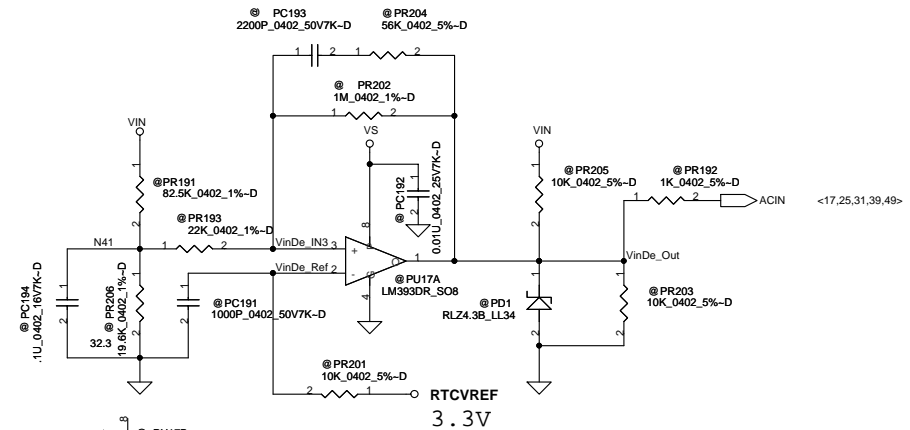
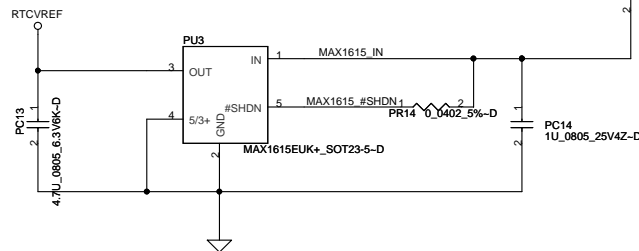
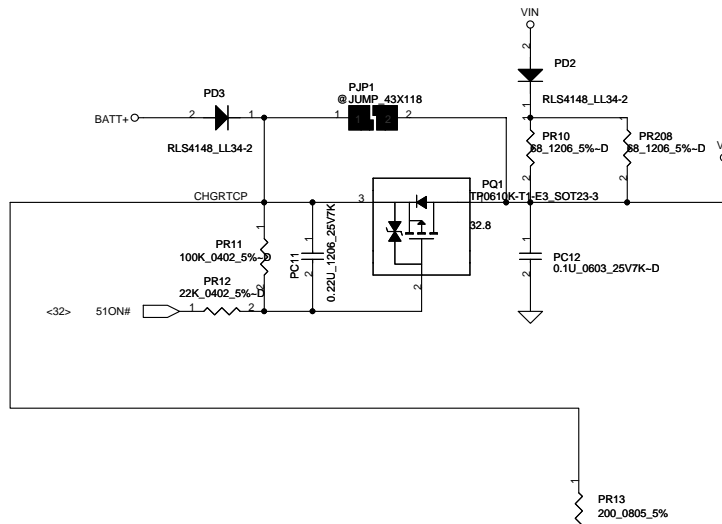
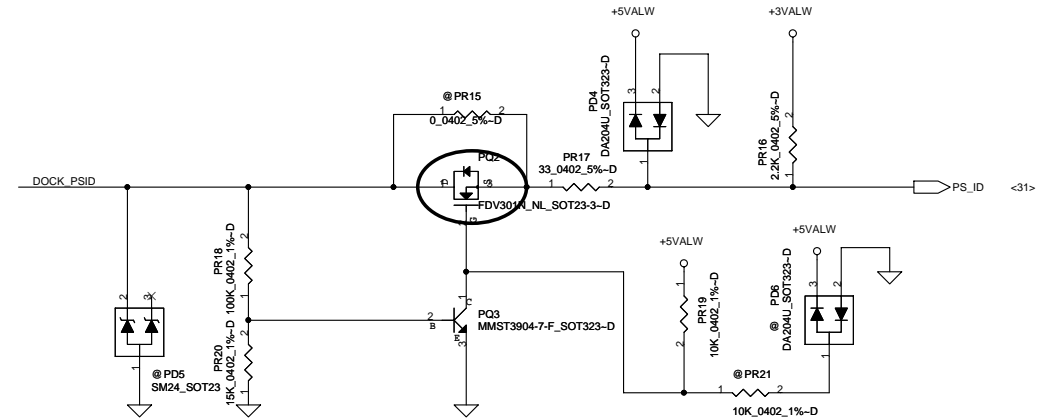
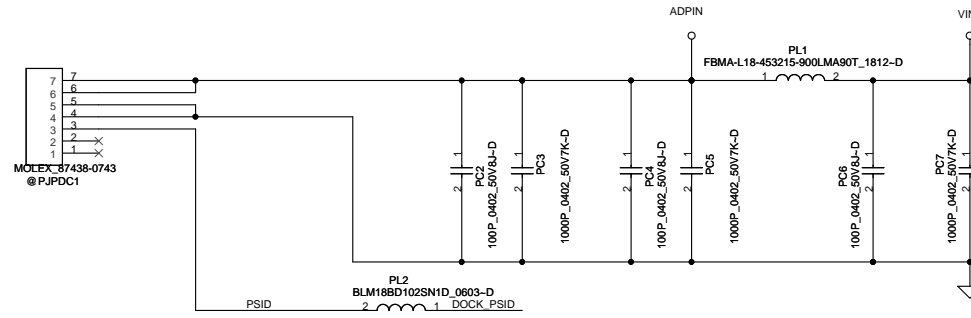


VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

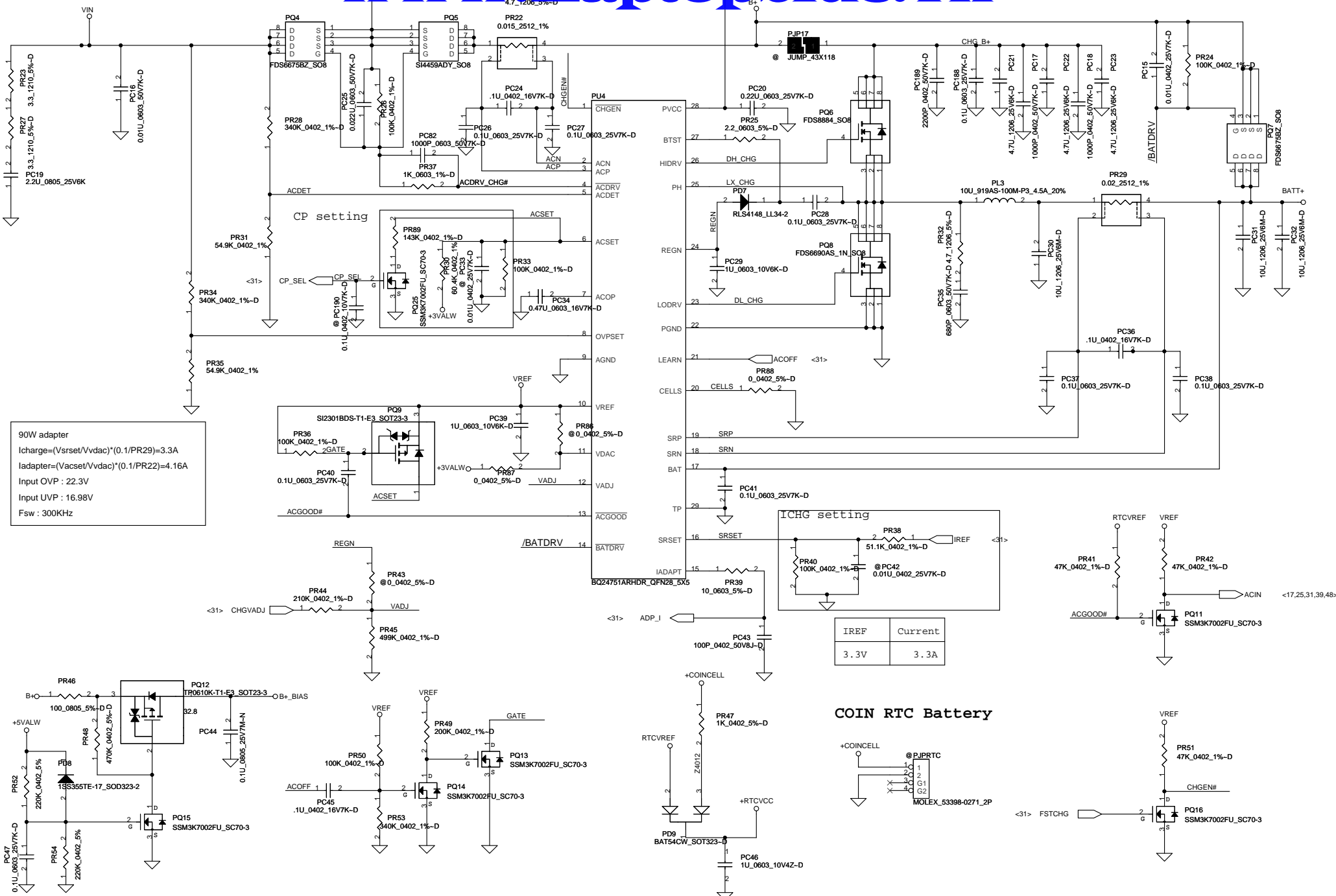
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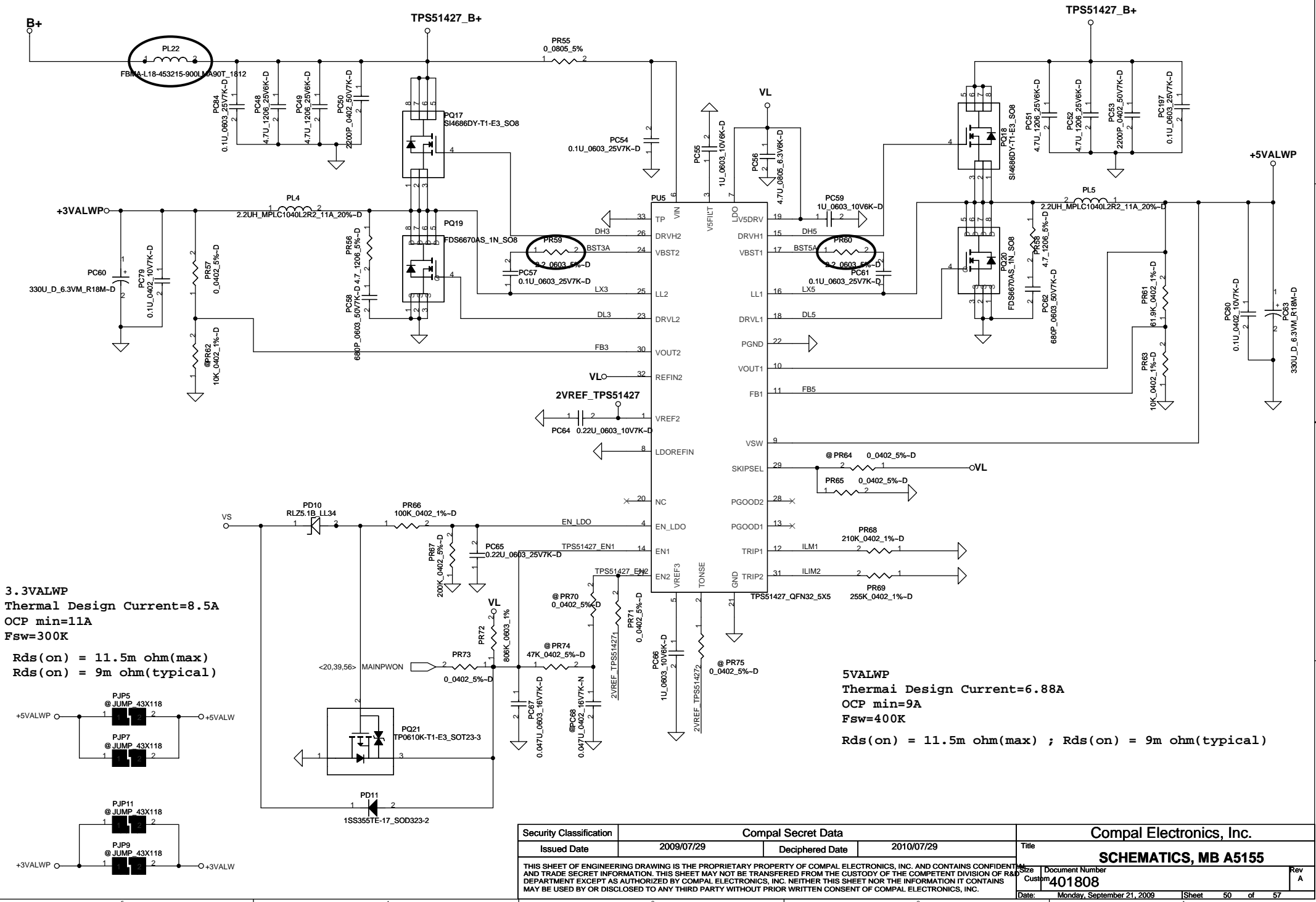


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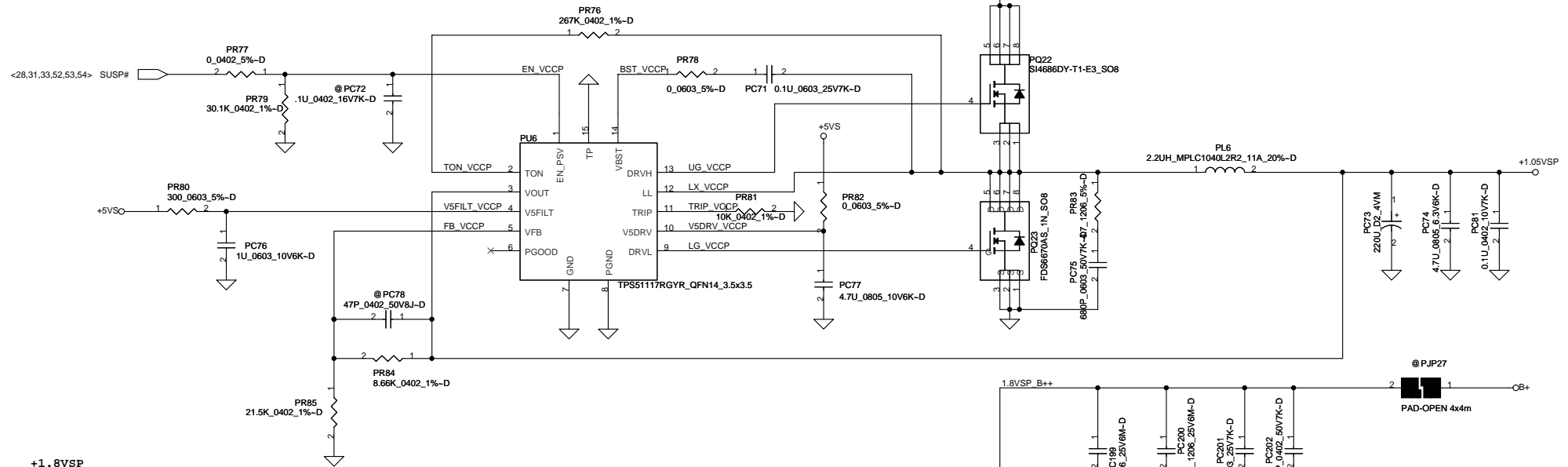
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H-->L	17.597	17.210	16.813



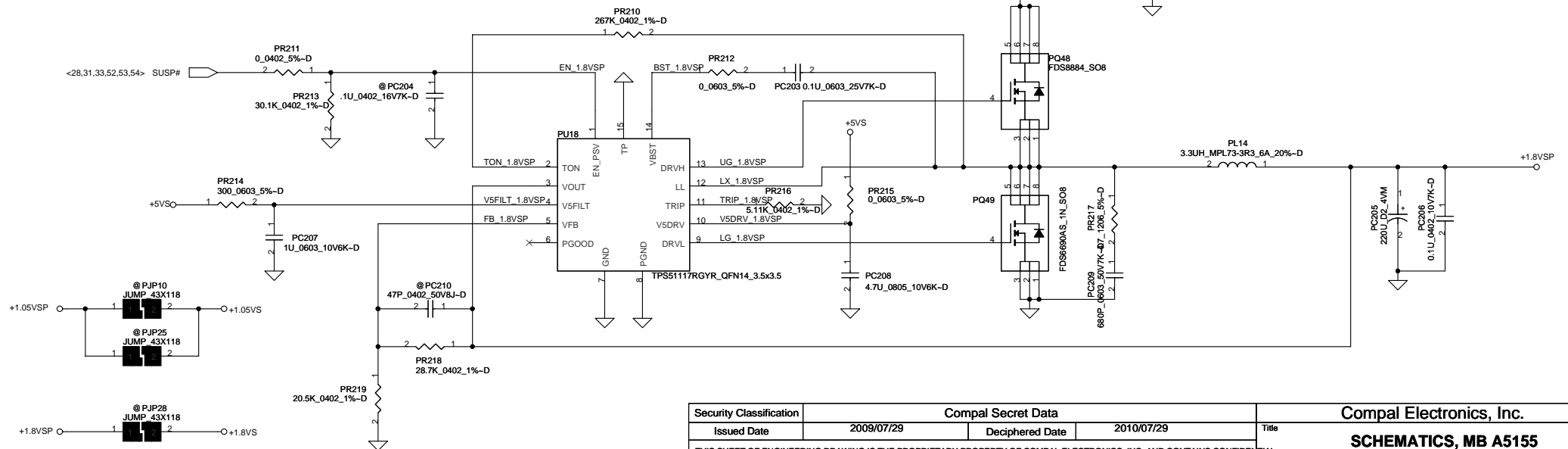


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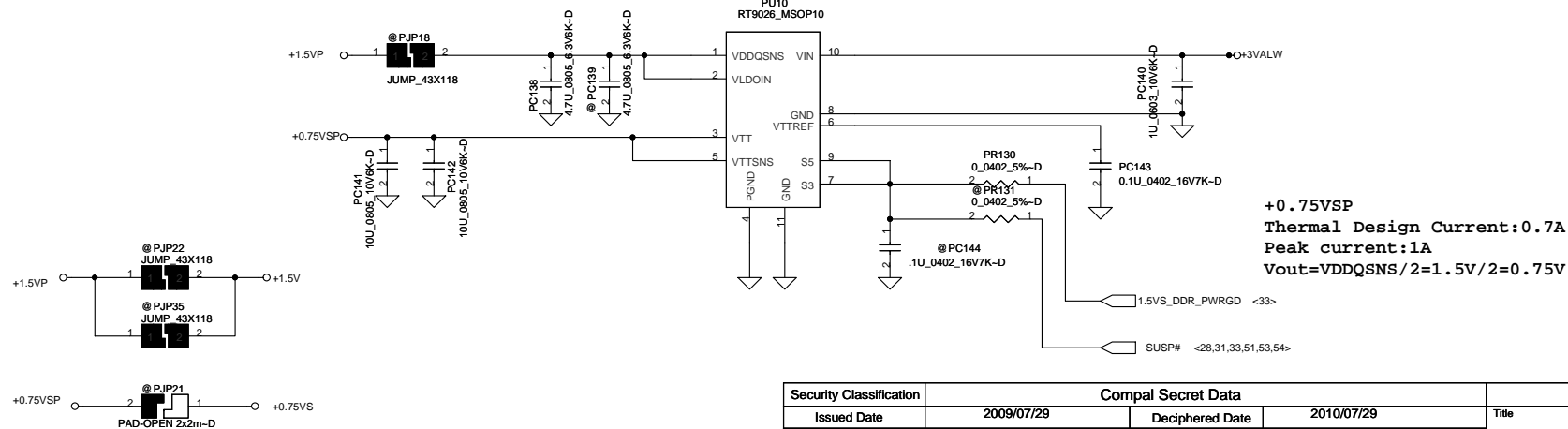
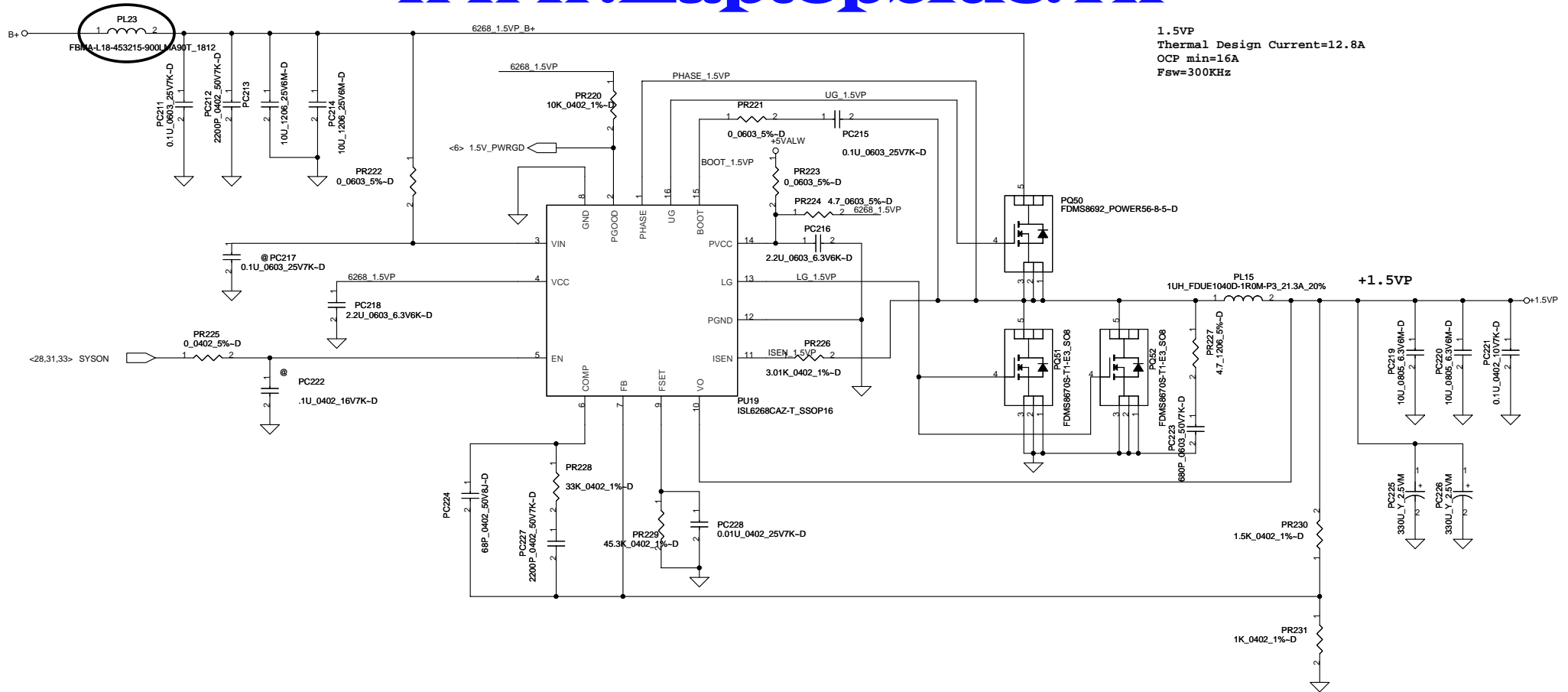
+1.05VSP
Thermal Desig Current=5.7A
OCP min=7.5A
Fsw=300KHz



+1.8VSP
Thermal Desig Current=2.5A
OCP min=3.3A
Fsw=300KHz

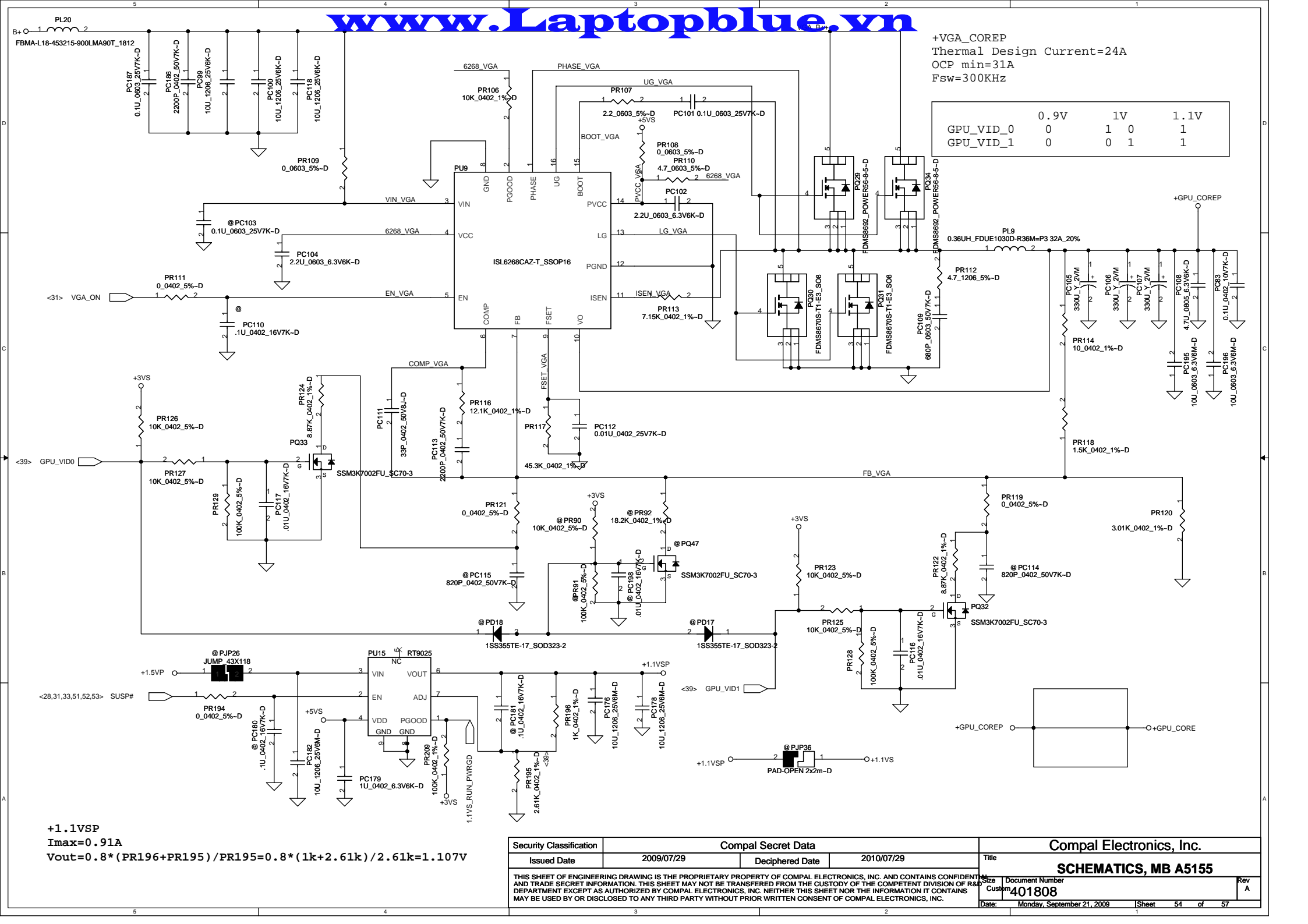


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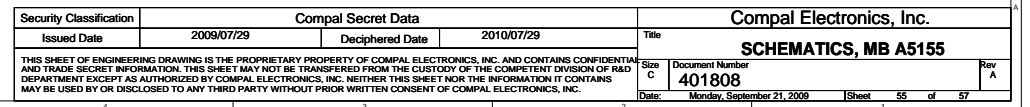


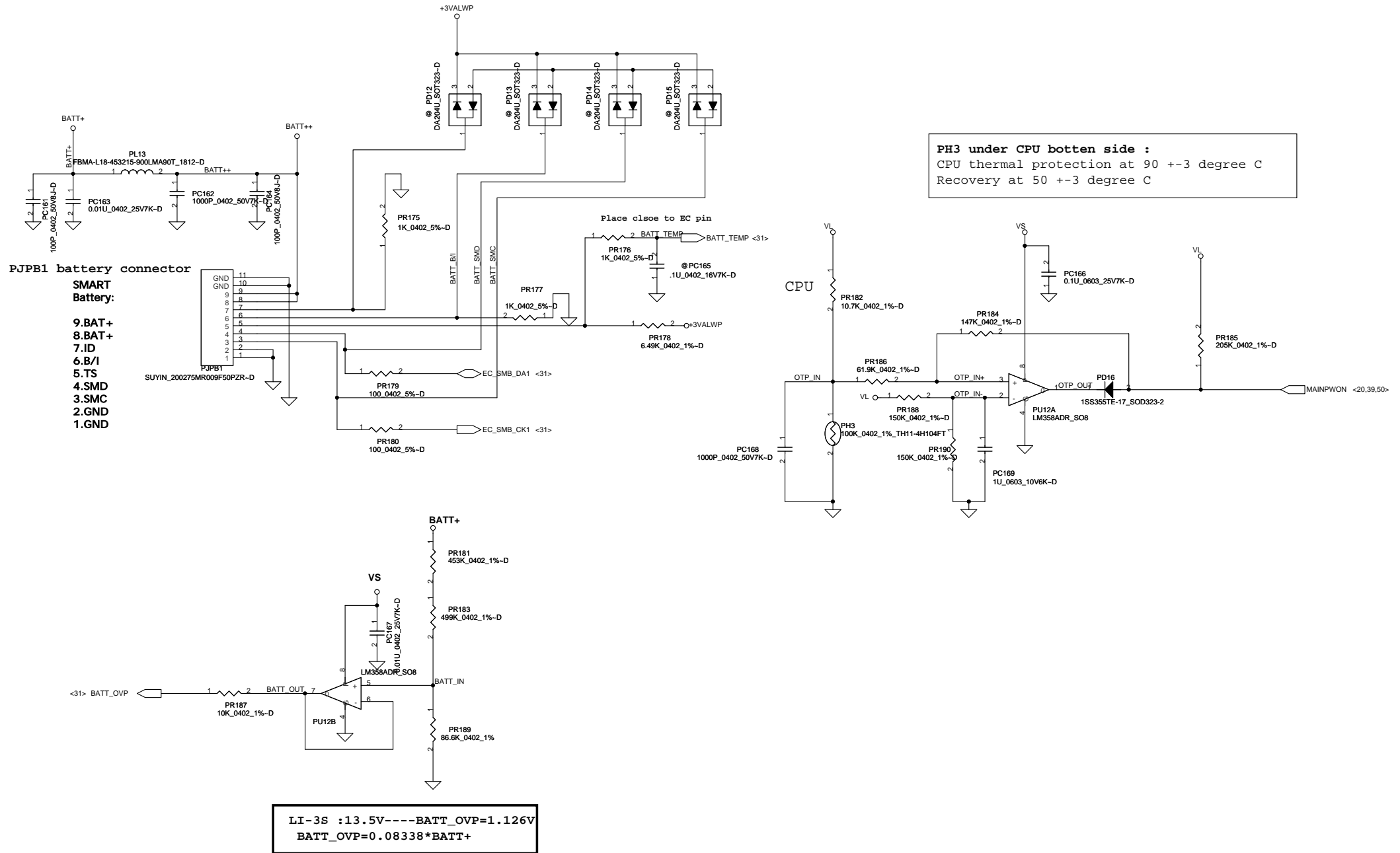
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	0.9V	1V	1.1V
GPU_VID_0	0	1 0	1
GPU_VID_1	0	0 1	1



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