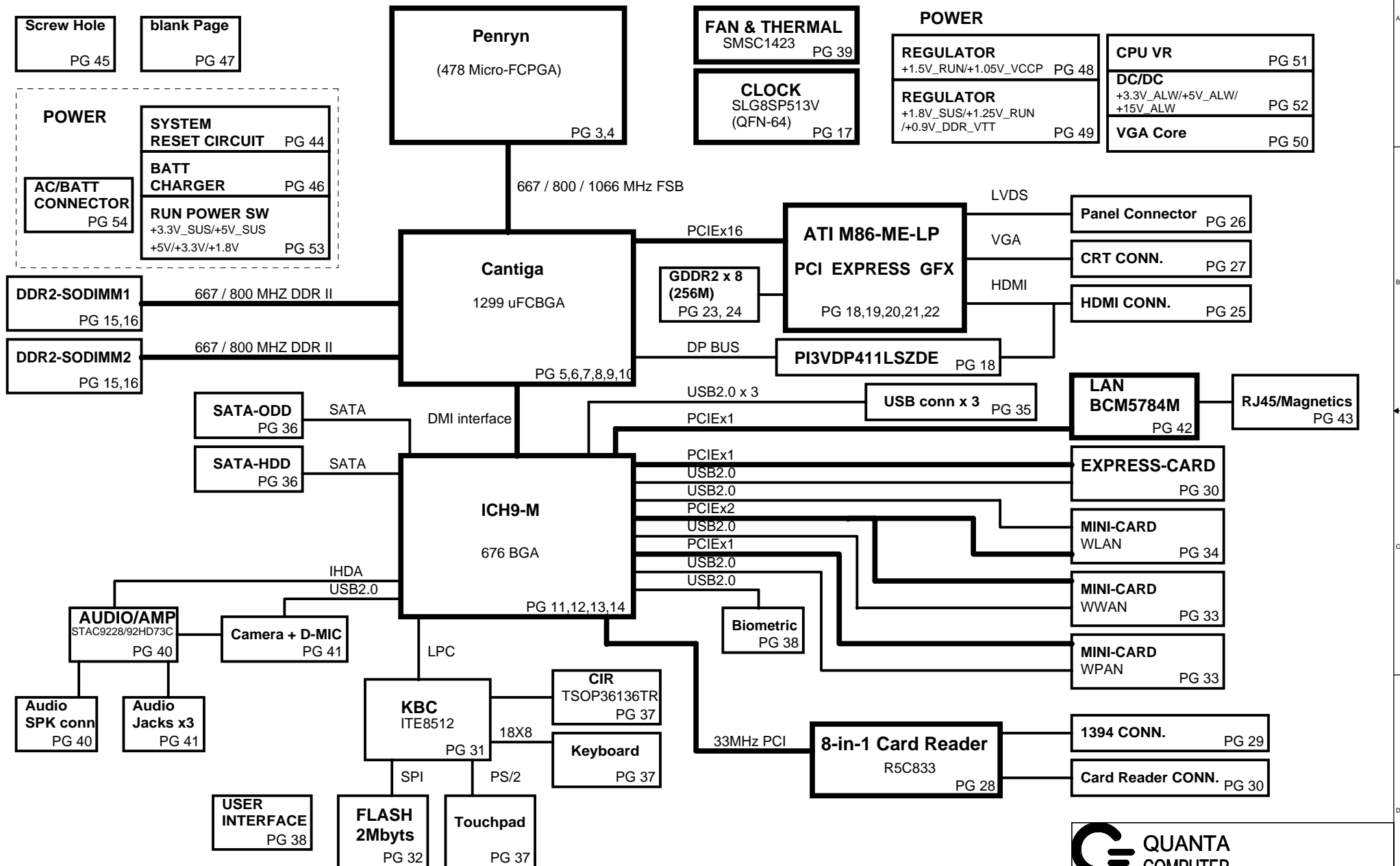


# GM5(B) Pacino Intel Discrete & UMA Block Diagram








VER : B2A



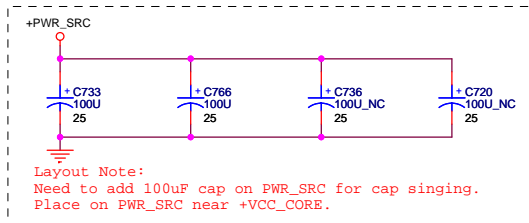
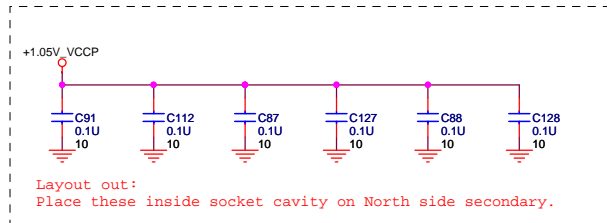
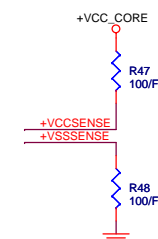
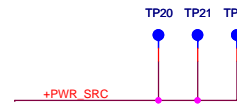
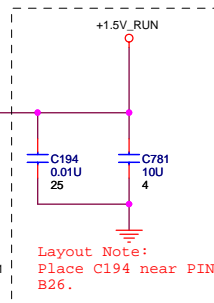
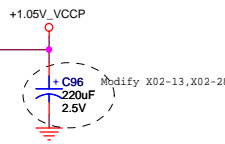
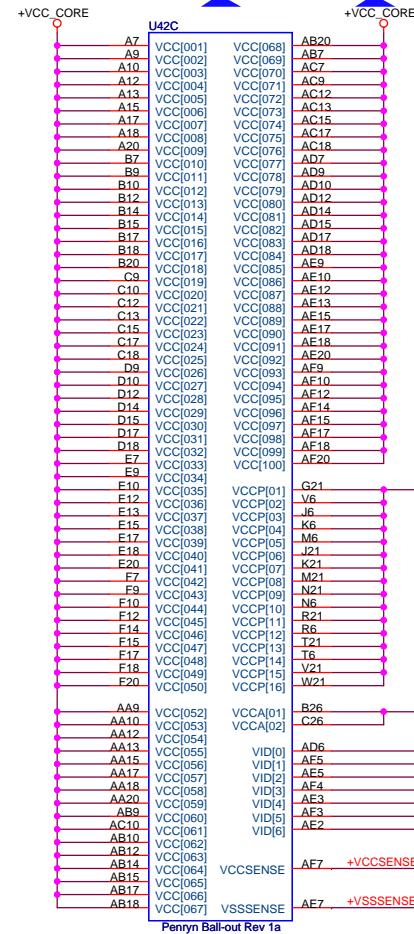
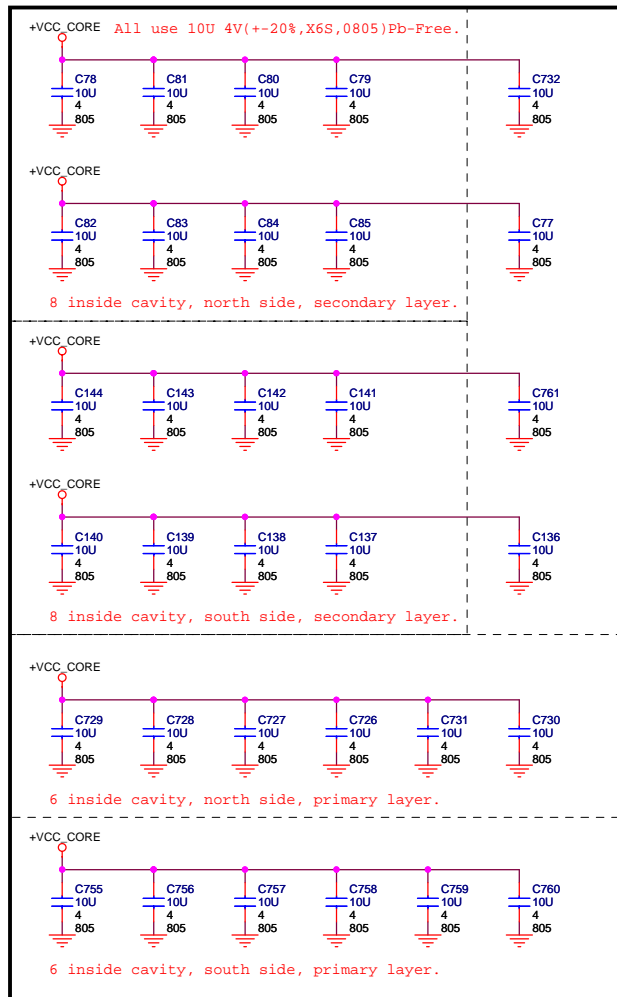
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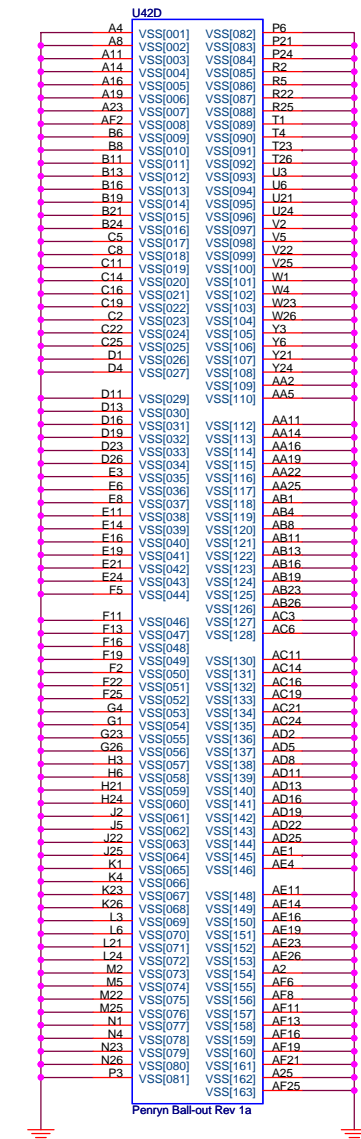
| POWER PLANE   | VOLTAGE     | PAGE  | DESCRIPTION            | CONTROL SIGNAL        | ACTIVE IN |
|---------------|-------------|---|------------------------|-----------------------|-----------|
| +PWR_SRC      | 10V~+19V    | 4,26,32,34,48,49,50,51,52,55  | MAIN POWER             |                       | S0~S5     |
| +RTC_CELL     | +3.0V~+3.3V | 11,14,31,32   | RTC                    |                       | S0~S5     |
| +3.3V_ALW     | +3.3V       | 3,13,26,31,32,34,36,37,38,44,46,49,52,53,54                                   | 8051 POWER             | ALWON                 | S0~S5     |
| +5V_ALW       | +5V         | 35,36,46,48,49,52,53,54   | LCD/CHARGE POWER       | ALWON                 | S0~S5     |
| +15V_ALW      | +15V        | 26,36,37,52,53  | LARGE POWER            | +5V_ALW               | S0~S5     |
| +3.3V_LAN     | +3.3V       | 42,43   | LAN POWER              | AUX_ON                |           |
| +5V_SUS       | +5V         | 14,38,50,51,53  | SLP_S5# CTRLD POWER    | SUS_ON                |           |
| +3.3V_SUS     | +3.3V       | 3,11,12,13,14,20,30,37,38,43,48,49,50,51,53                                   | SLP_S5# CTRLD POWER    | 3.3V_SUS_ON           |           |
| +1.8V_SUS     | +1.8V       | 6,8,9,15,48,49,50,53,55   | SODIMM POWER           | DDR_ON                |           |
| +0.9V_DDR_VTT | +0.9V       | 16,49,53  | SODIMM POWER           | 0.9V_DDR_VTT_ON       |           |
| +5V_RUN       | +5V         | 14,20,25,27,36,37,38,39,40,41,53  | SLP_S3# CTRLD POWER    | RUN_ON                |           |
| +3.3V_RUN     | +3.3V       | 6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55 | SLP_S3# CTRLD POWER    | 3.3V_RUN_ON           |           |
| +1.8V_RUN     | +1.8V       | 19,20,21,22,23,24,25,38,53  | SDVO POWER             | RUN_ON                |           |
| +1.5V_RUN     | +1.5V       | 4,9,14,30,33,34,48,,53,55   | CANTIGA/ICH8 POWER     | 1.5V_RUN_ON           |           |
| +1.05V_VCCP   | +1.05V      | 3,4,5,6,8,9,11,14,37,48,55  | CPU/CANTIGA/ICH8 POWER | 1.05V_RUN_ON          |           |
| +VCC_CORE     | +0.7V~+1.5V | 4,51  | CPU CORE POWER         | IMVP_VR_ON            |           |
| +LCDVCC       | +3.3V       | 26  | LCD Power              | LCDVCC_TST_EN & ENVDD |           |
| +5V_MOD       | +5V         | 36  | Module Power           | MODC_EN#              |           |
| +5V_HDD       | +5V         | 36  | HDD Power              | HDDC_EN#              |           |
| +5V_ALW2      | +5V         | 37,38,52,53   | LED power source       | LDO output            |           |
|               |             |   |                        |                       |           |
|               |             |   |                        |                       |           |

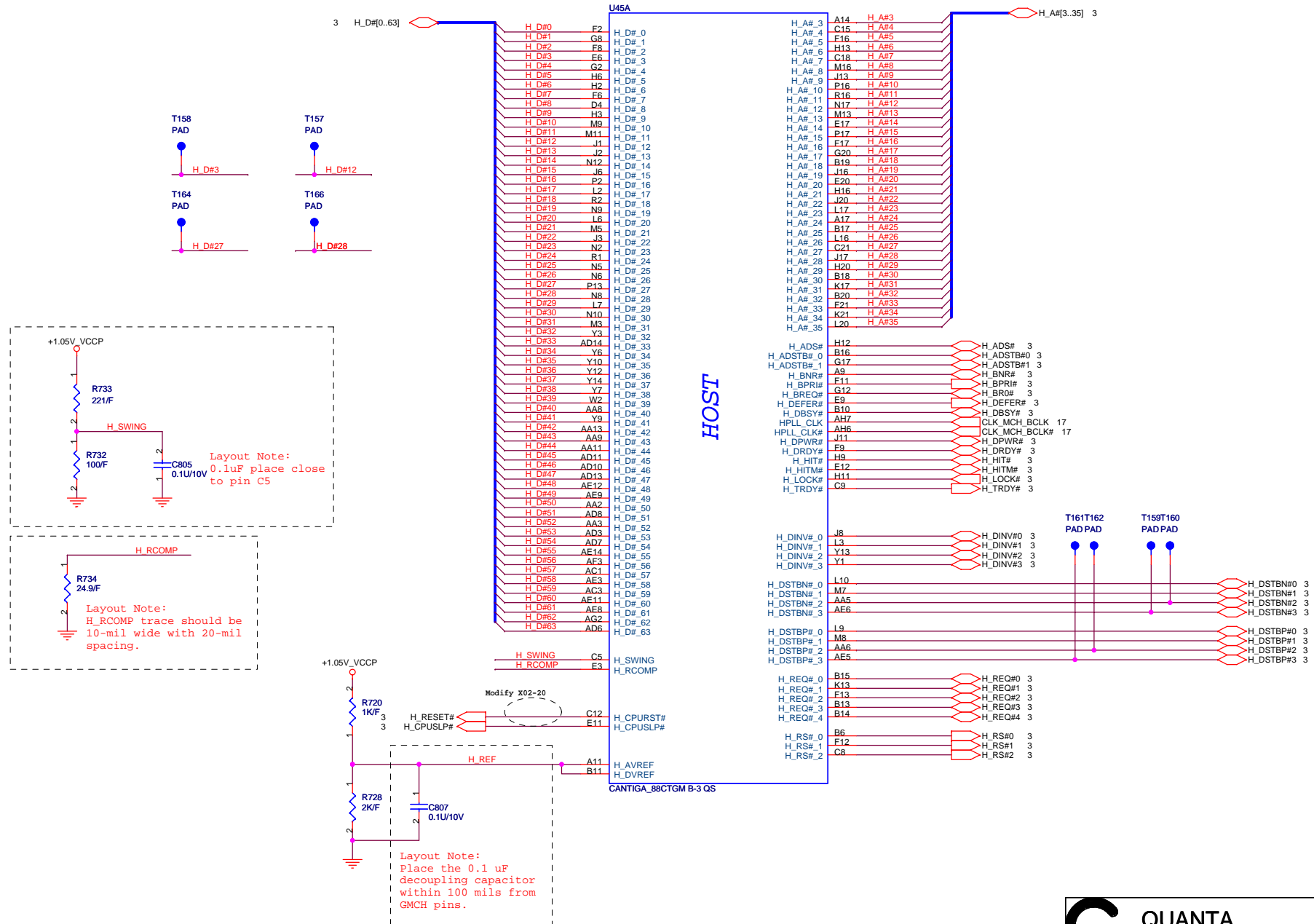
| GND PLANE  | PAGE | DESCRIPTION |
|--|------|-------------|
|  8731AGND     | 46   |             |
|  AGND_0.9V    | 49   |             |
|  AGND_DC/DC   | 52   |             |
|  AGND_DC2     | 48   |             |
|  AGND_DDR     | 49   |             |
|  AGND_ISL6260 | 51   |             |
|  GND          | ALL  |             |

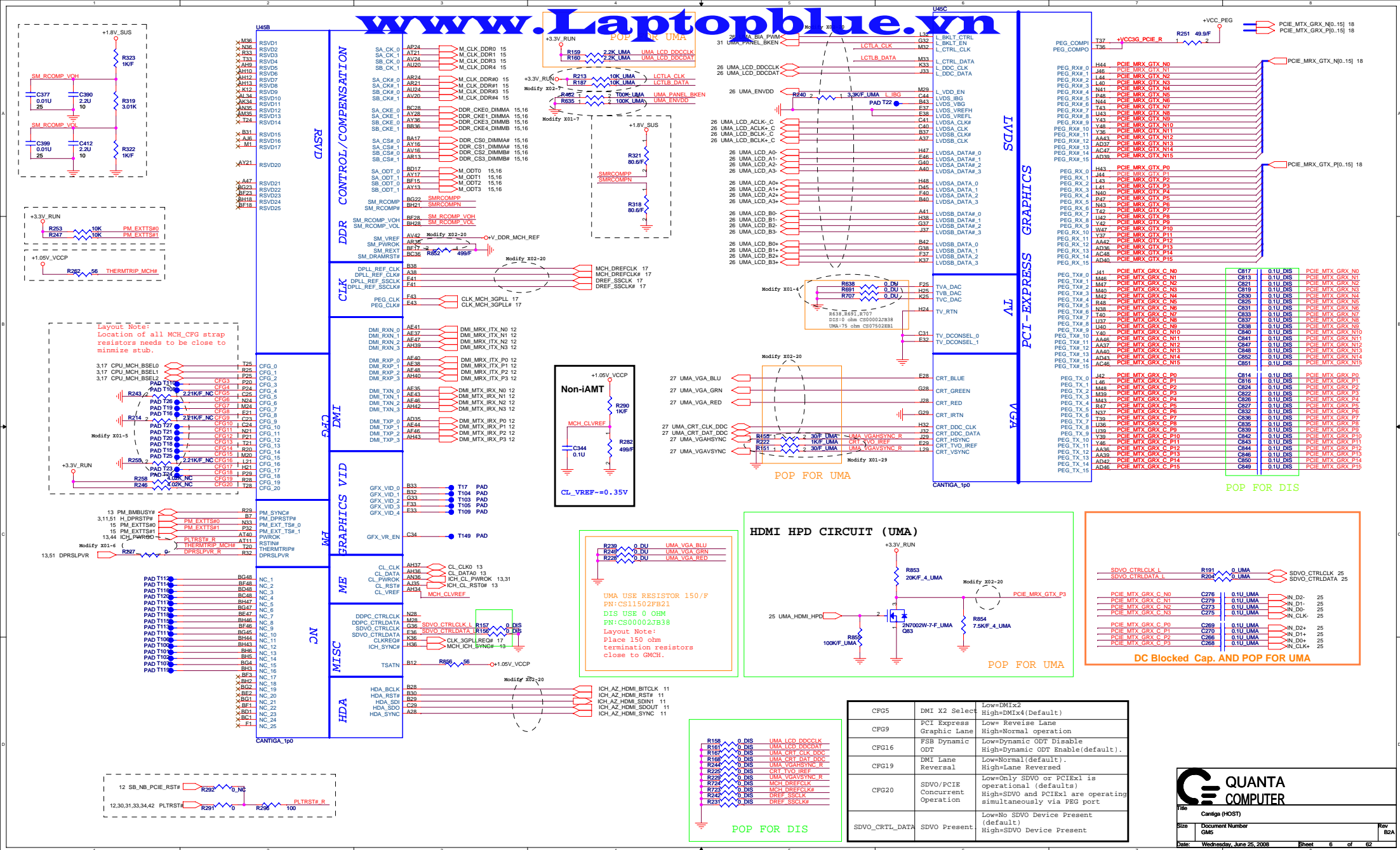


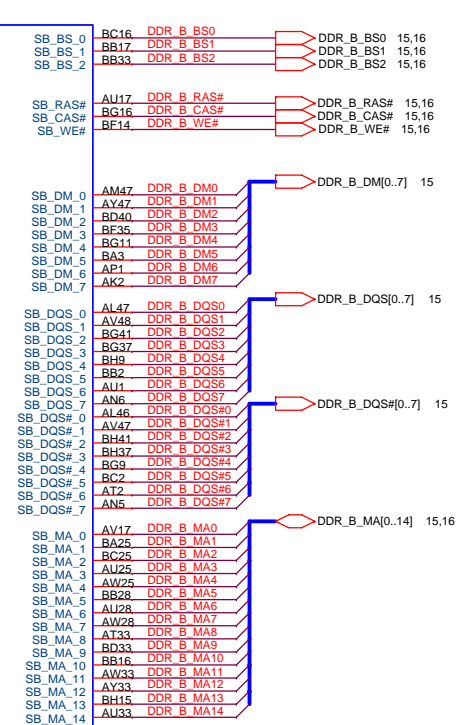
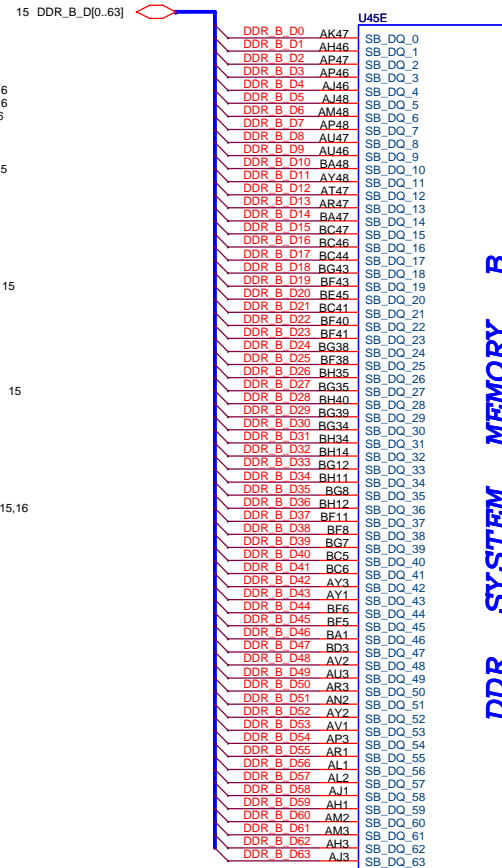
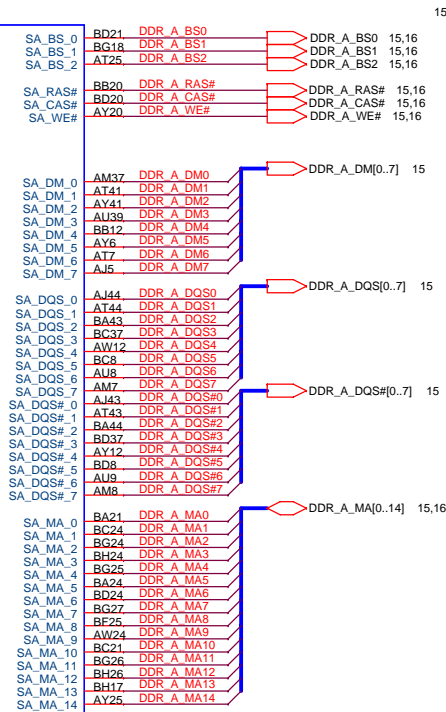
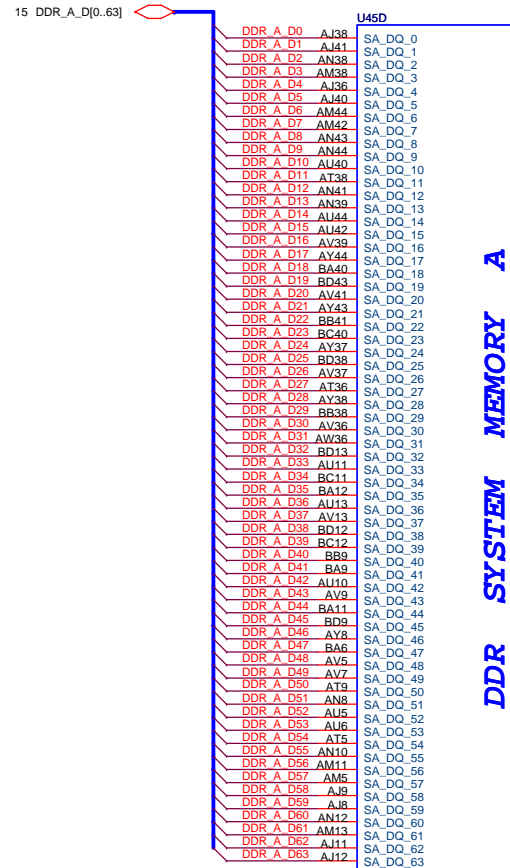
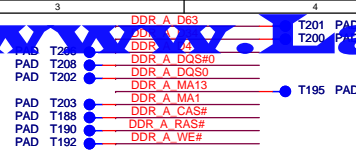


Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.





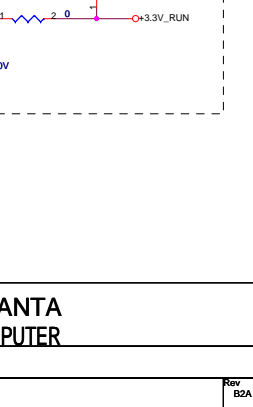
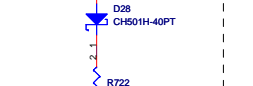
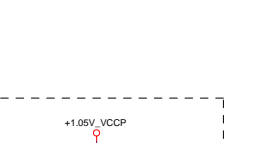
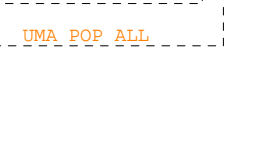
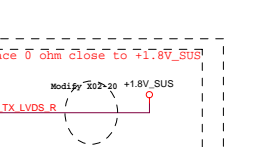
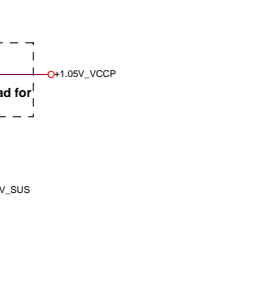
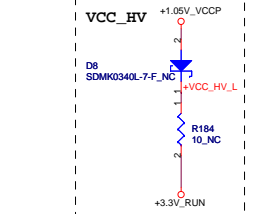
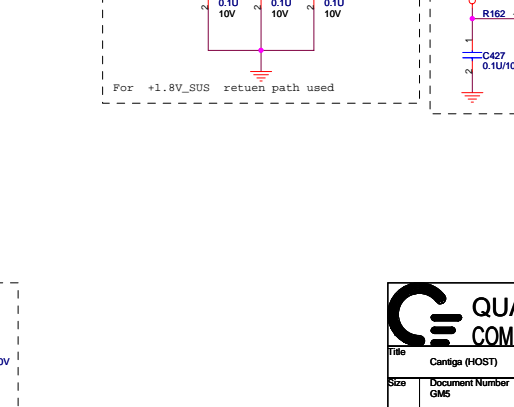
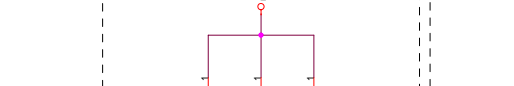
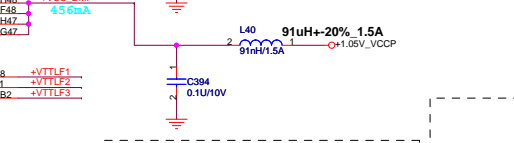
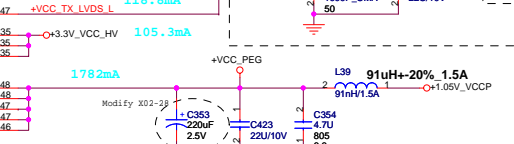
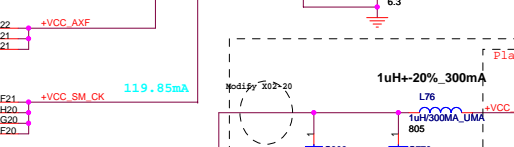
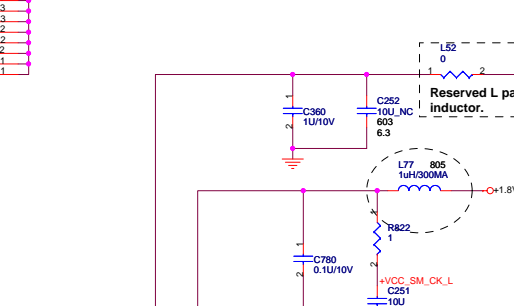
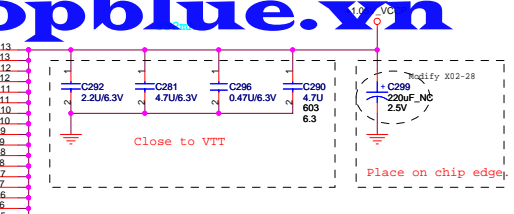
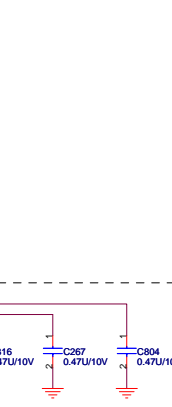
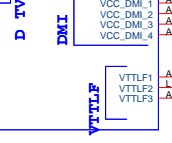
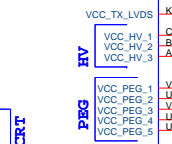
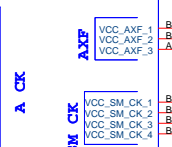
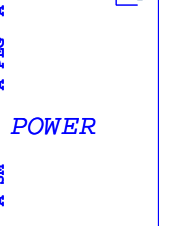
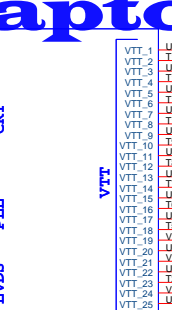
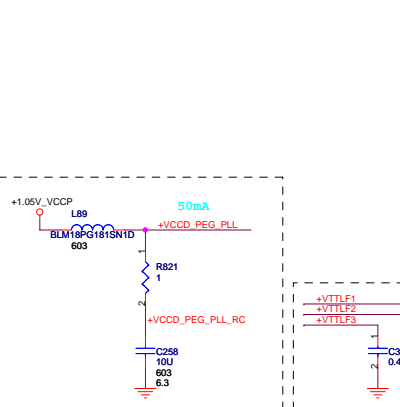
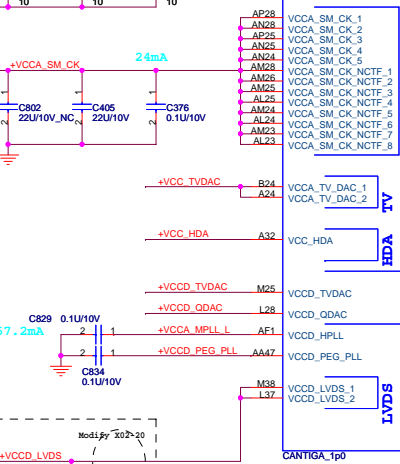
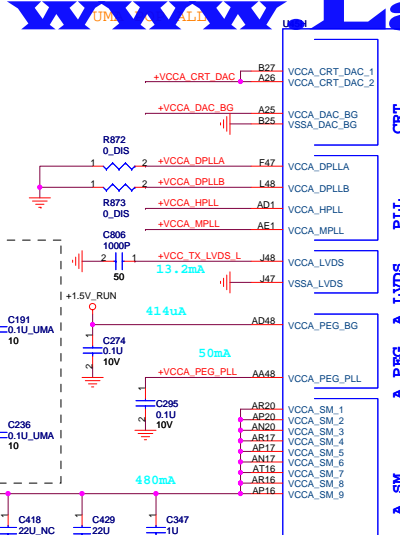
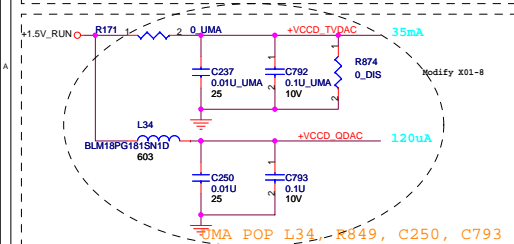
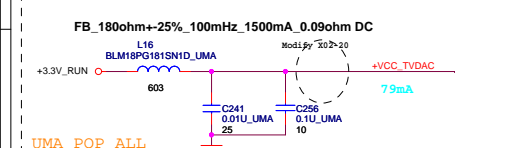
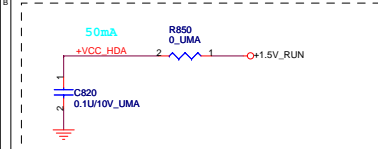
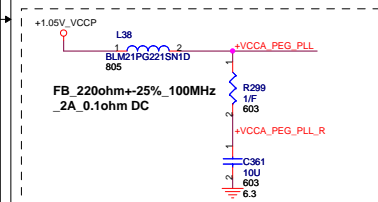
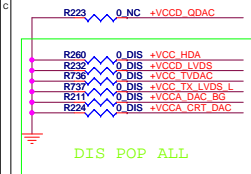
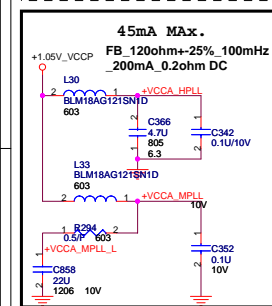
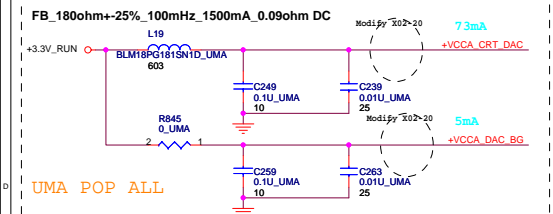


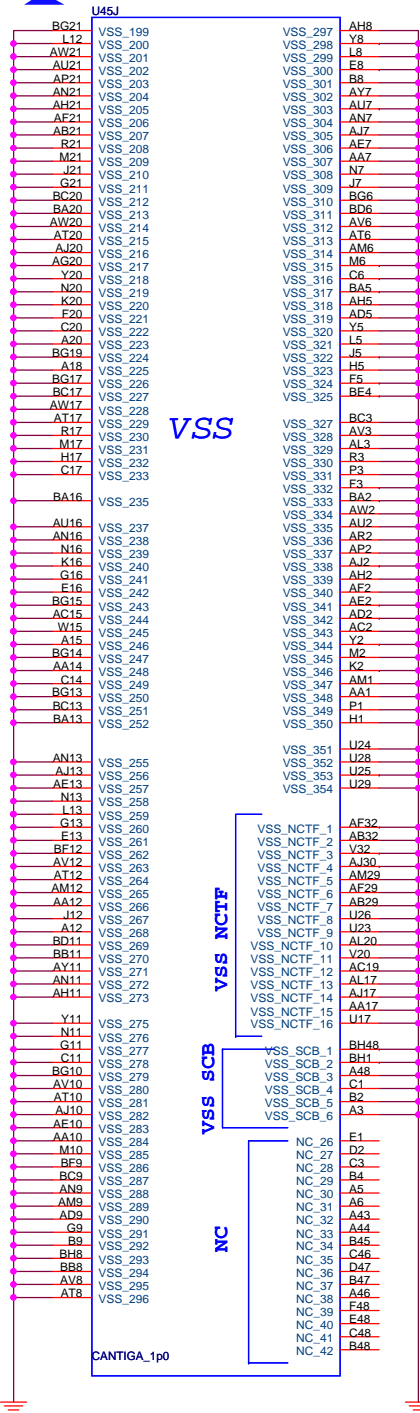
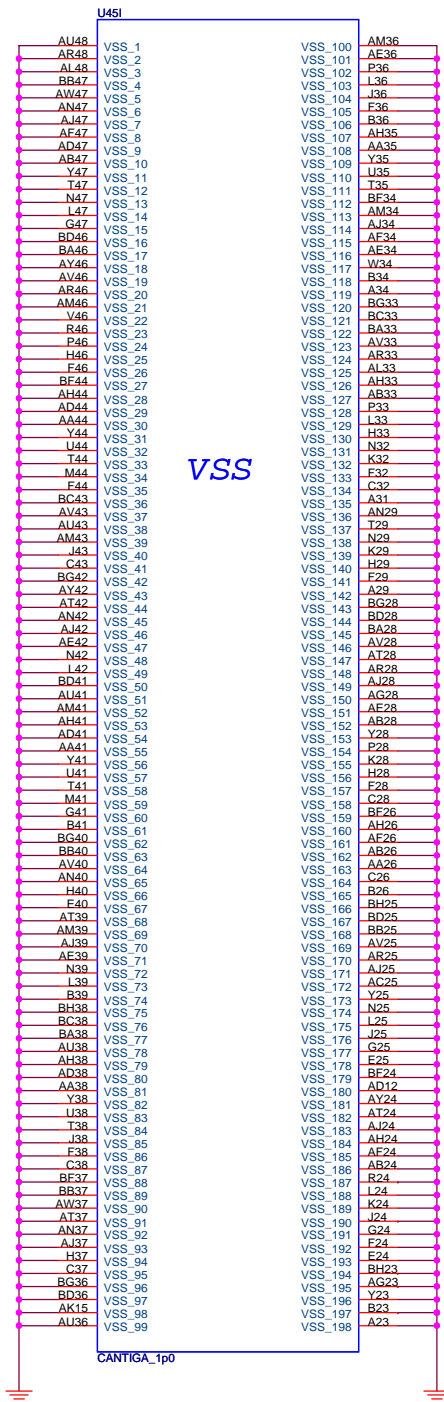


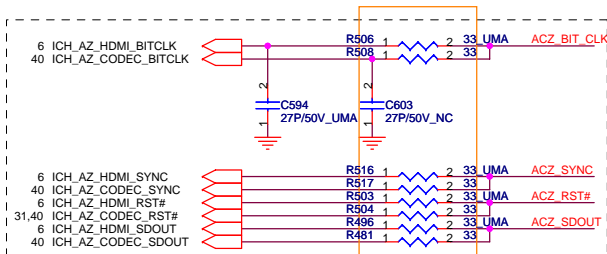
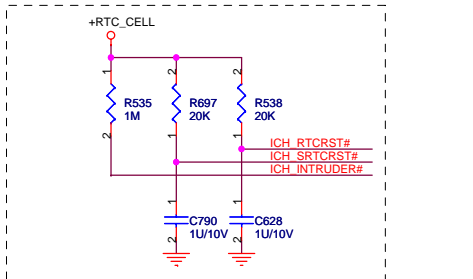
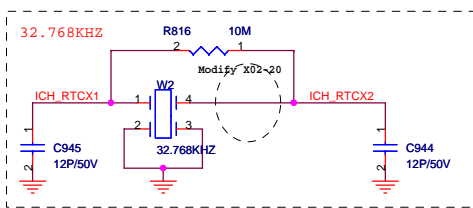
CANTIGA\_1p0

CANTIGA\_1p0

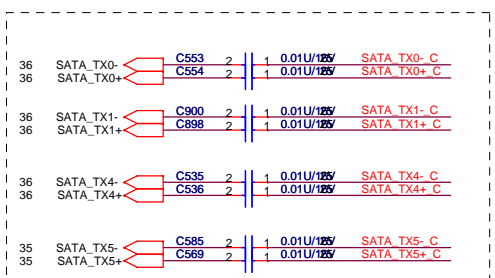




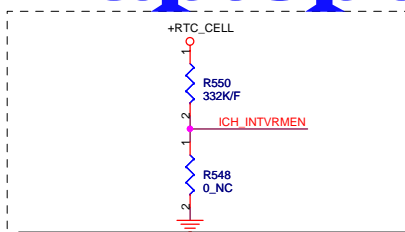




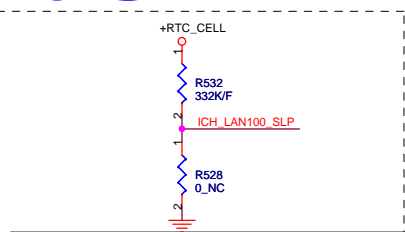
Place all series termination resistors close to IC9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



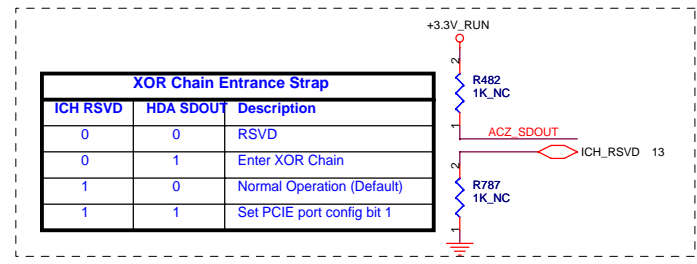
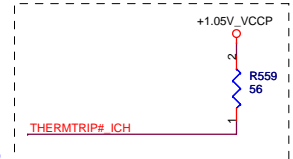
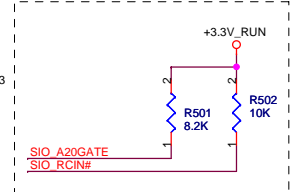
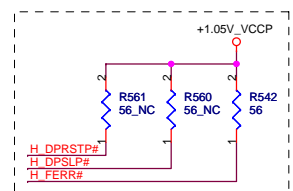
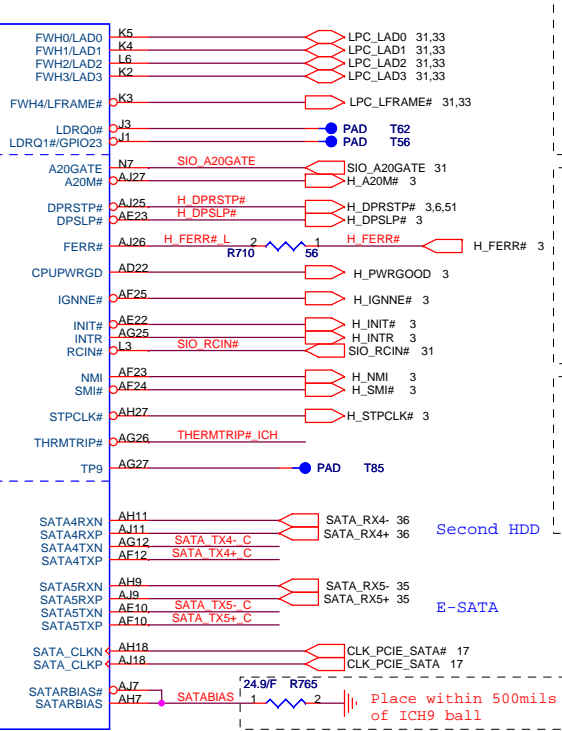
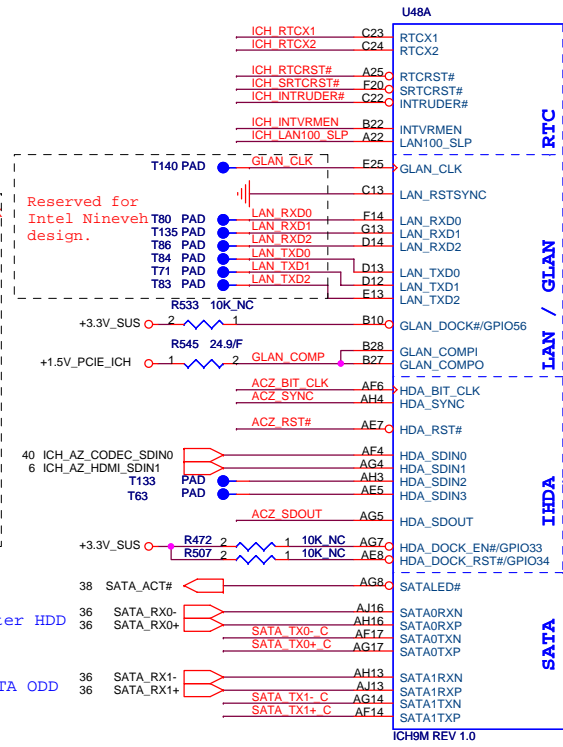
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

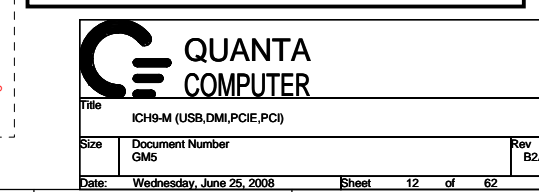
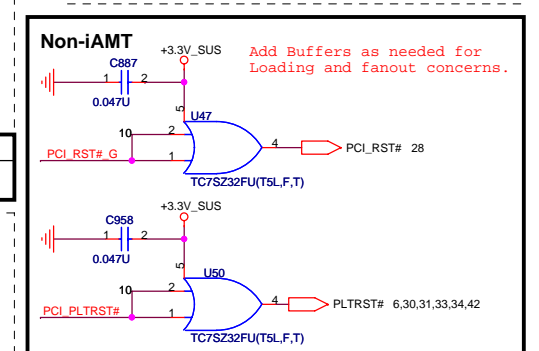
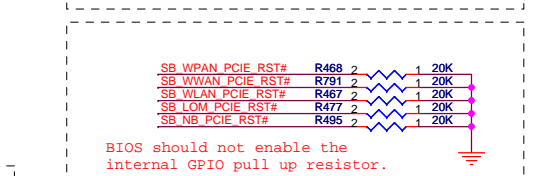
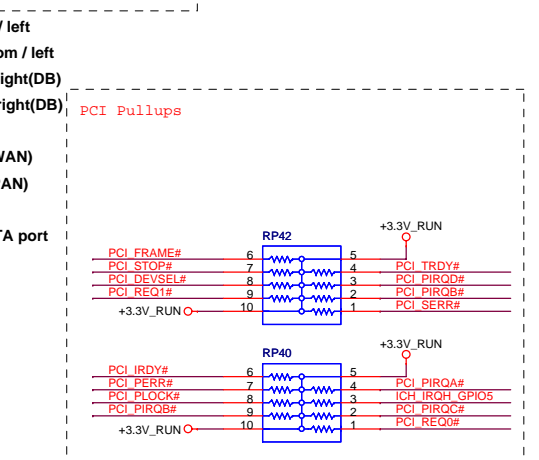
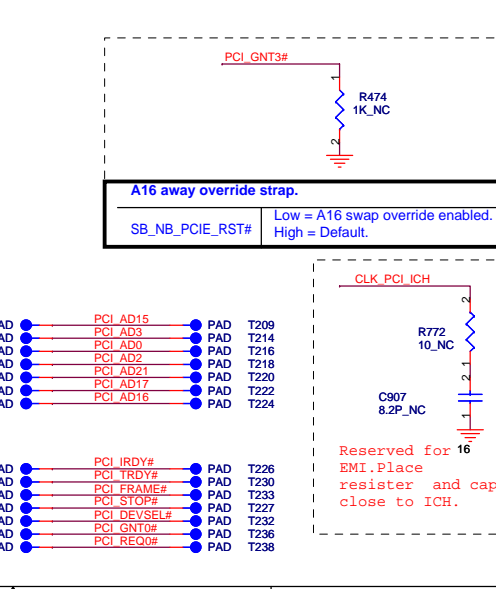
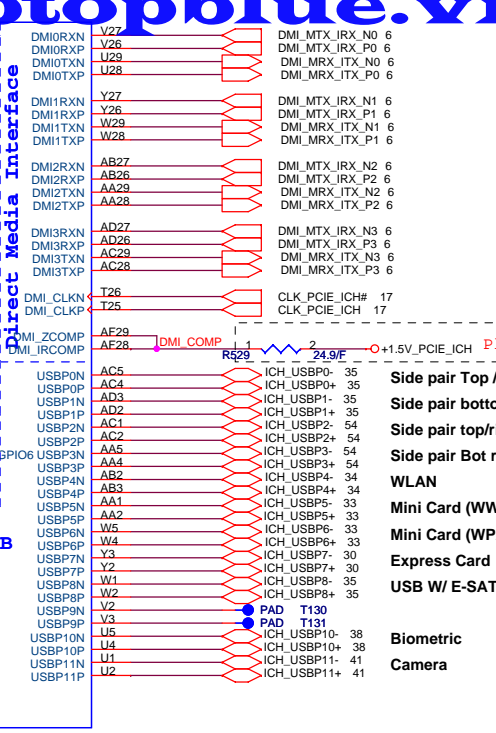
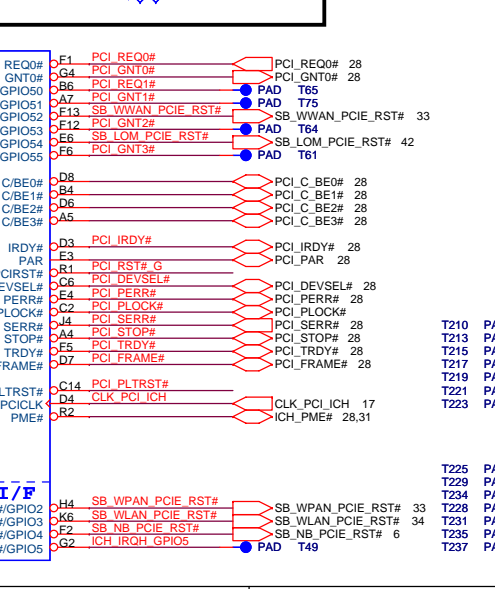
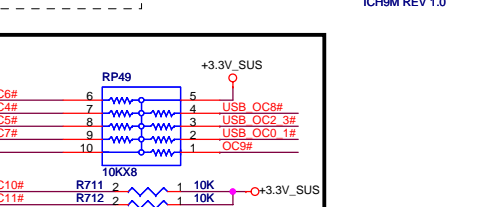
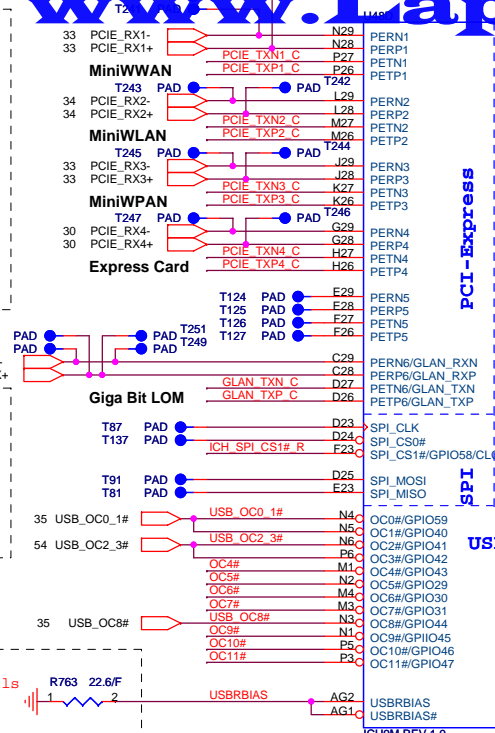
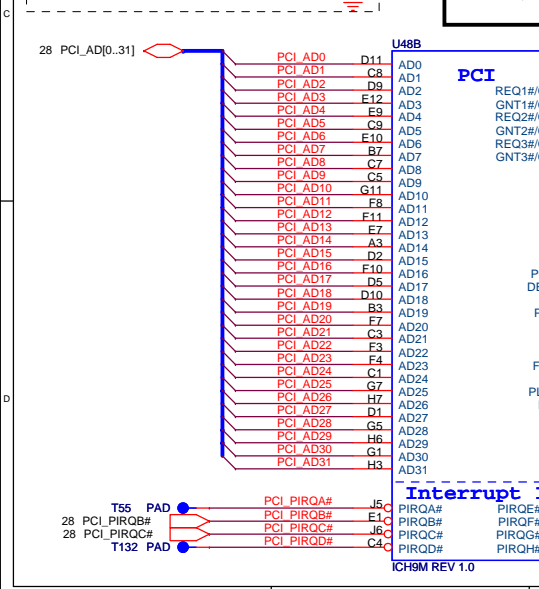
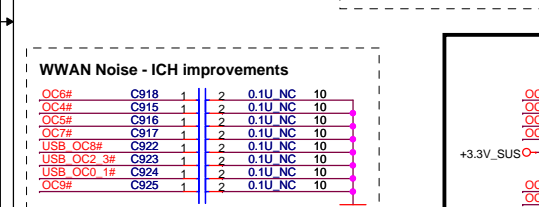
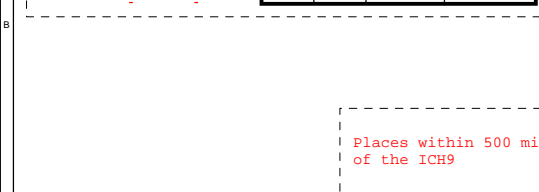
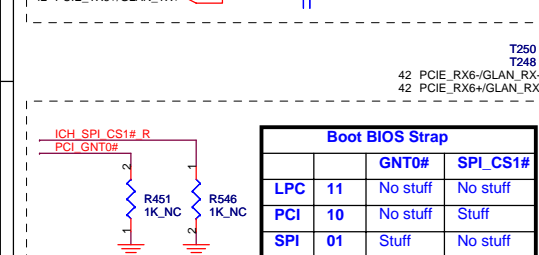
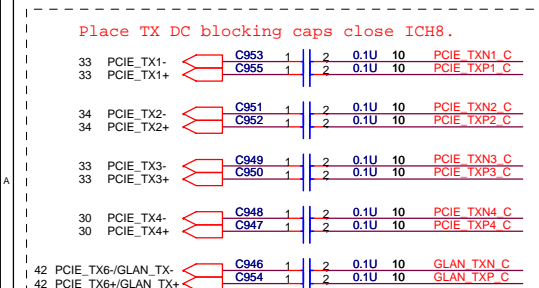


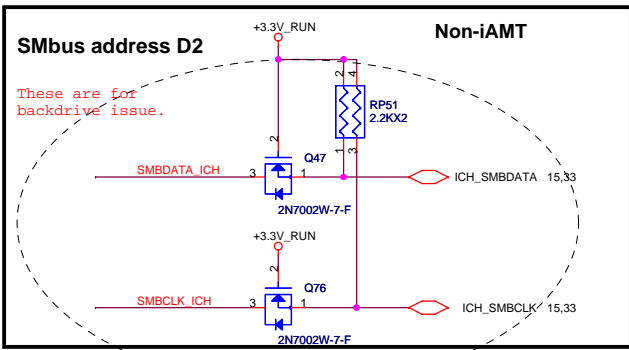
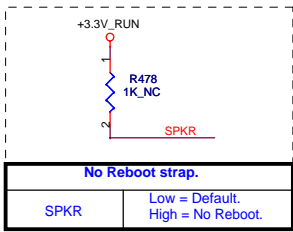
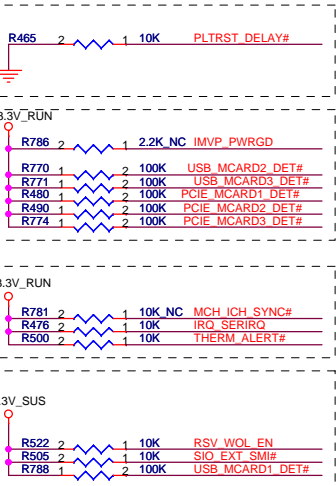
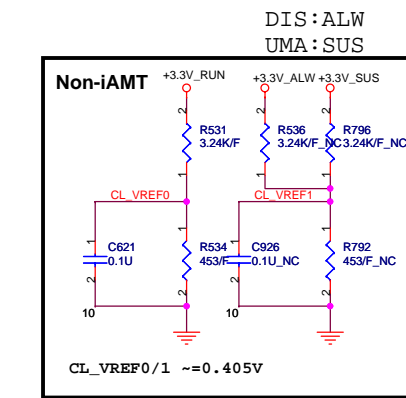
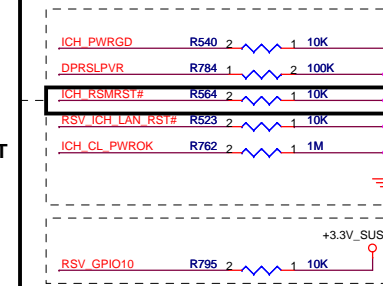
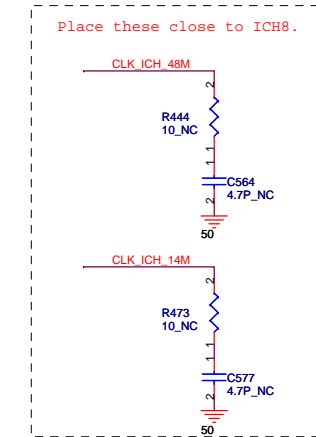
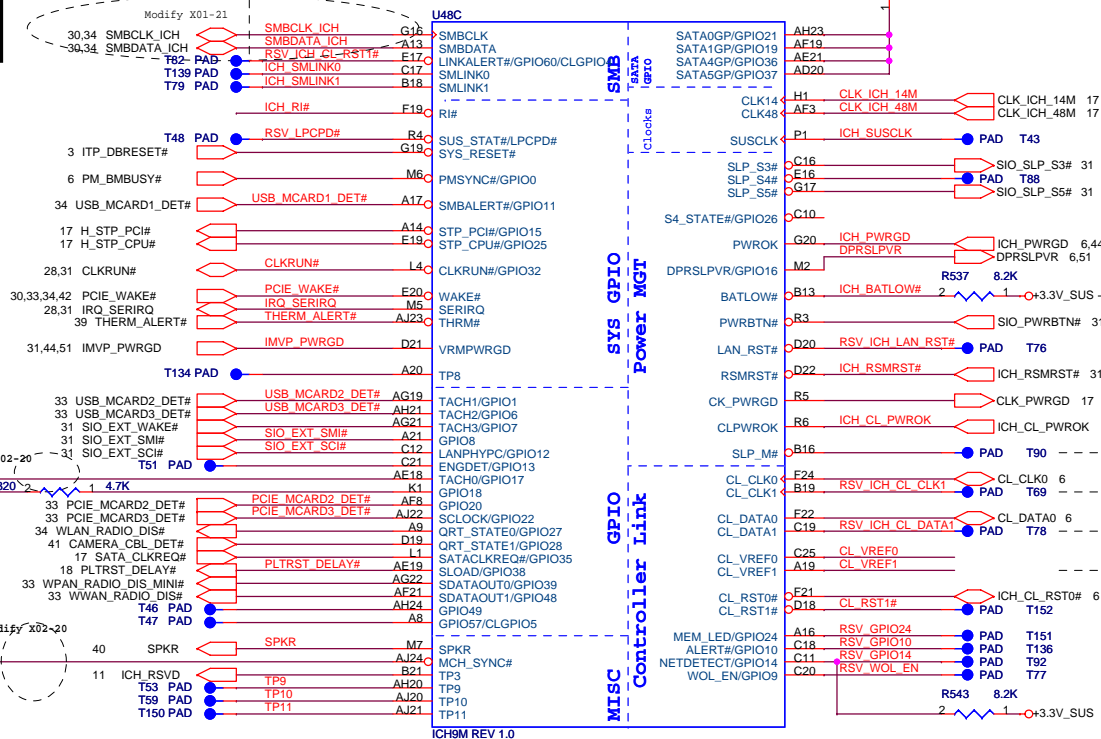
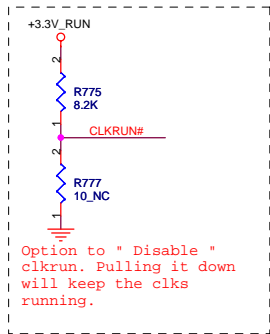
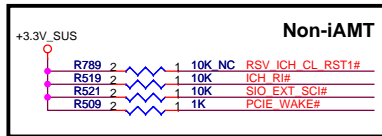
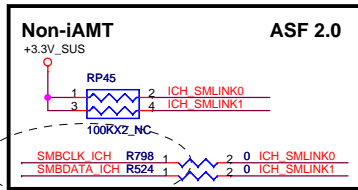
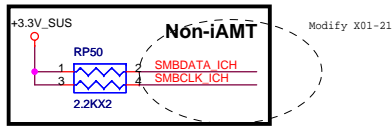
|   |   |
|---|---|
| <b>ICH9M Internal VR Enable Strap</b><br><b>(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)</b> |   |
| ICH_INTVRMEN  | Low = Internal VR Disabled<br>High = Internal VR Enabled(Default) |

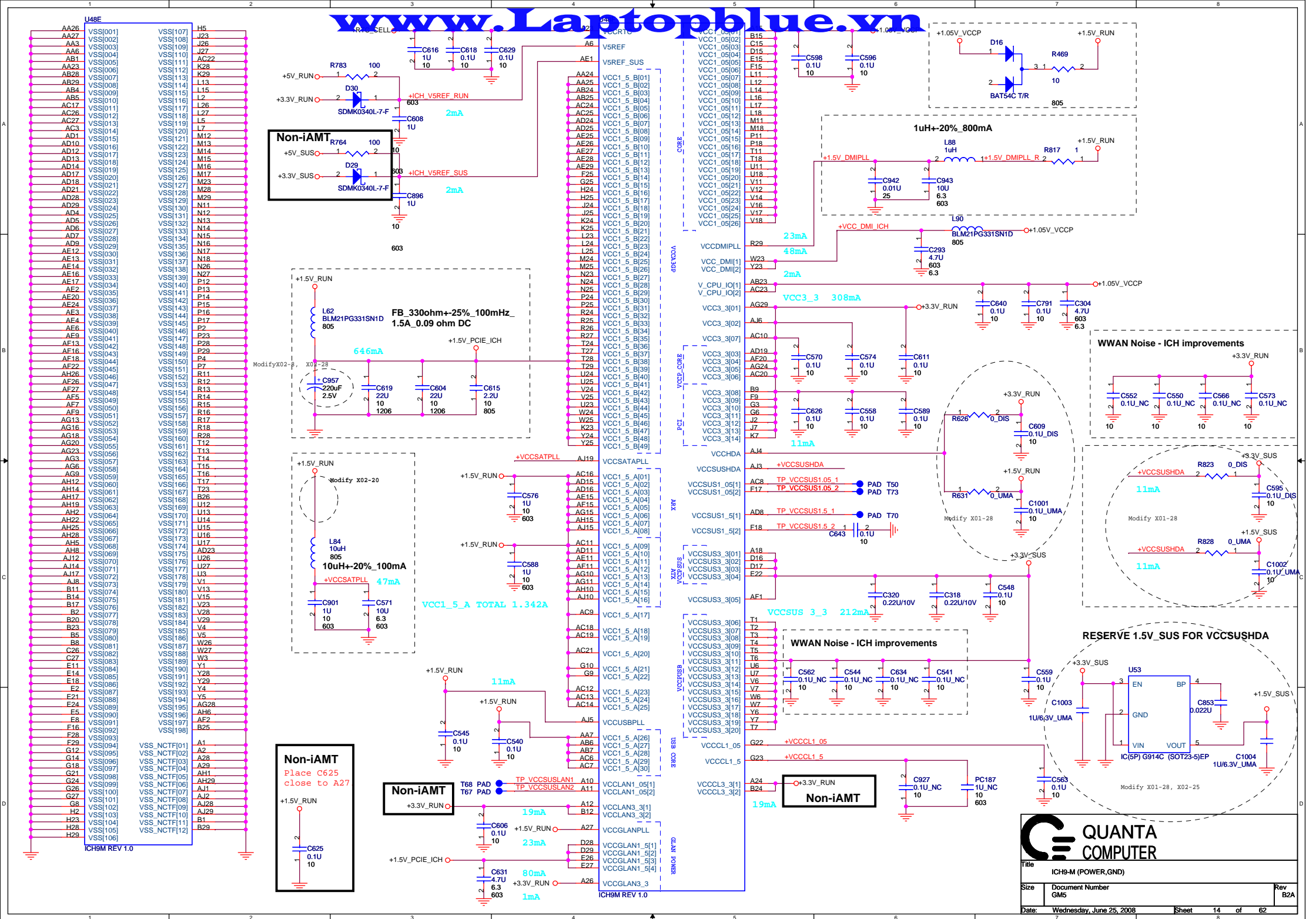


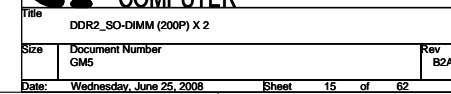
|  |   |
|--|---|
| <b>ICH9M LAN100 SLP Strap</b><br><b>(Internal VR for VccLAN1.05 and VccCL1.05)</b> |   |
| <b>ICH_LAN100_SLP</b>  | Low = Internal VR Disabled<br>High = Internal VR Enabled(Default) |

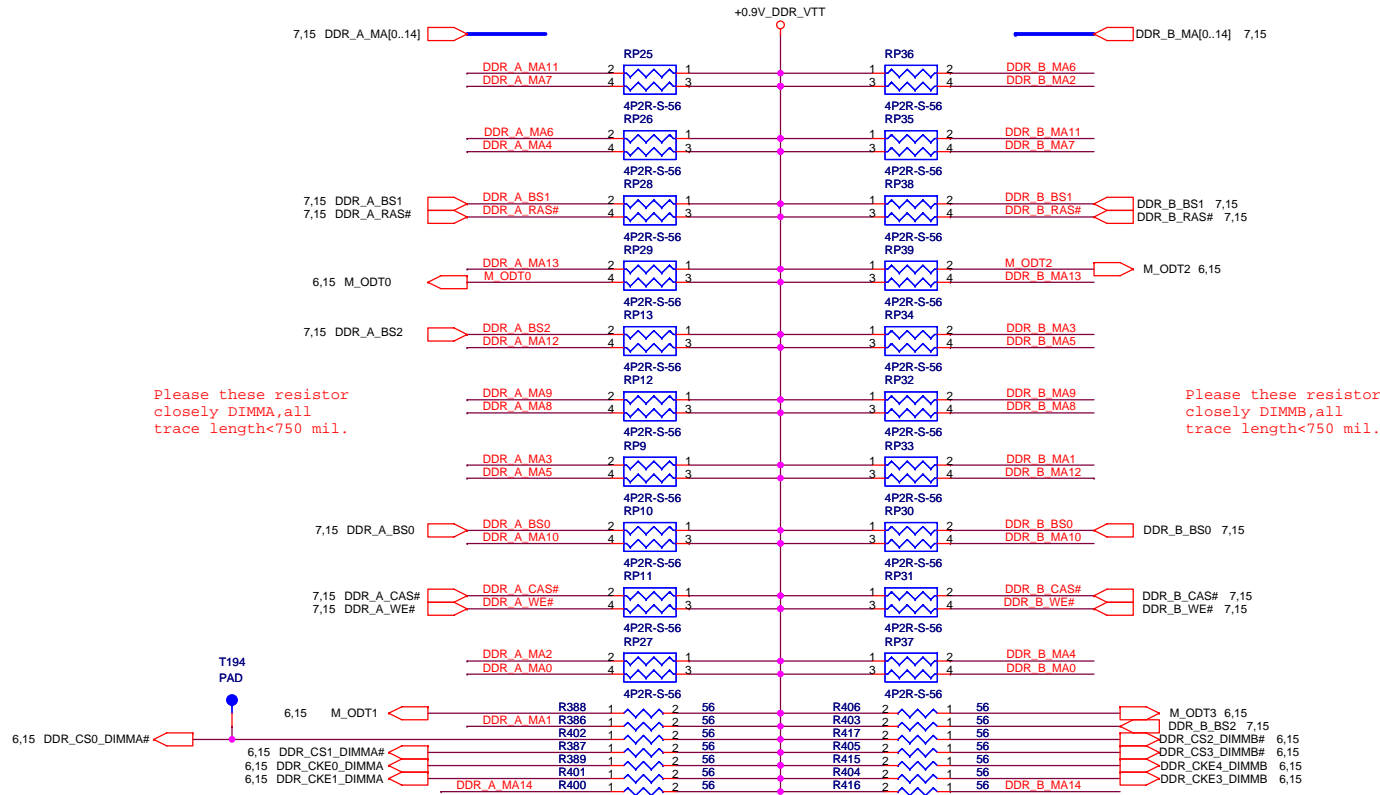
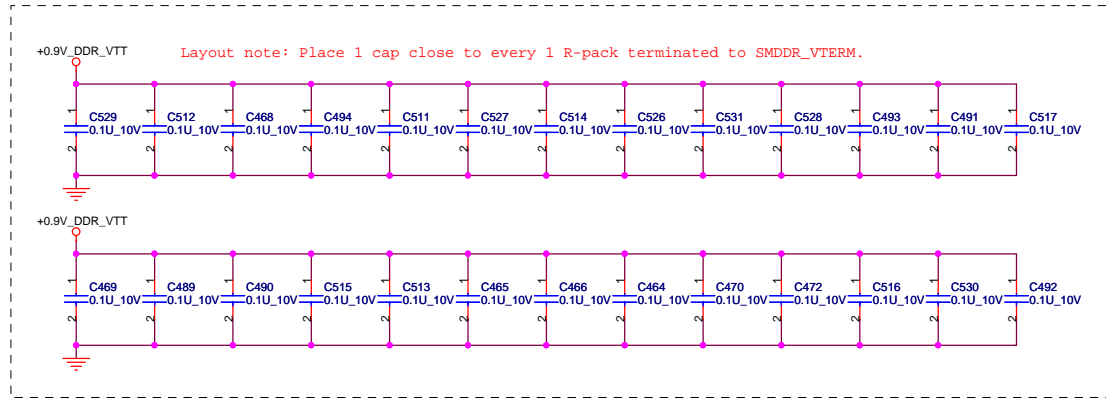




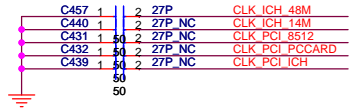




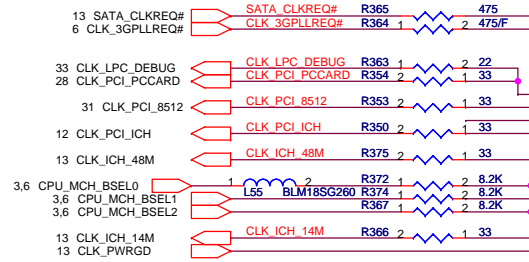




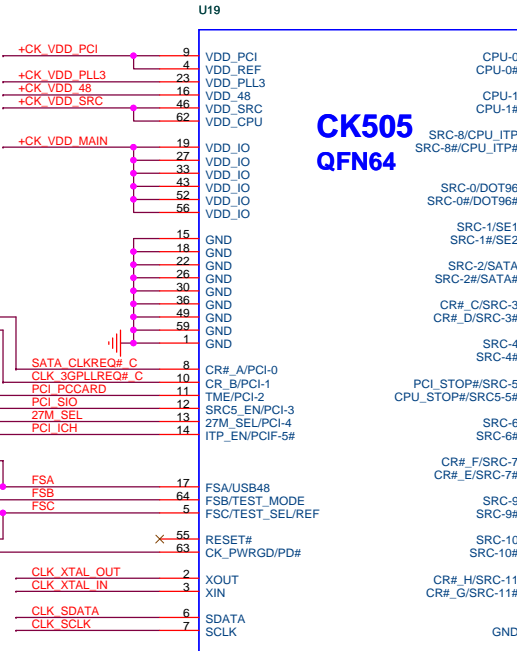
Add capacitor pads for improving WWAN.



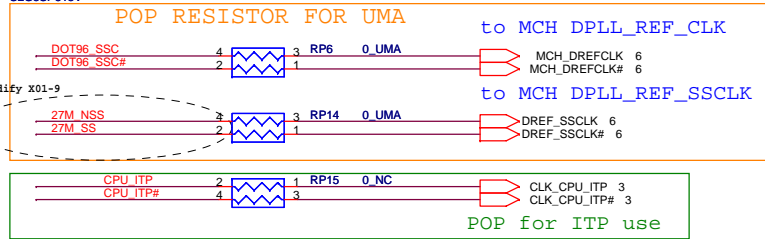
14.318MHz



CLK\_LPC\_DEBUG FOR DEBUG  
NEED POP RESISTOR

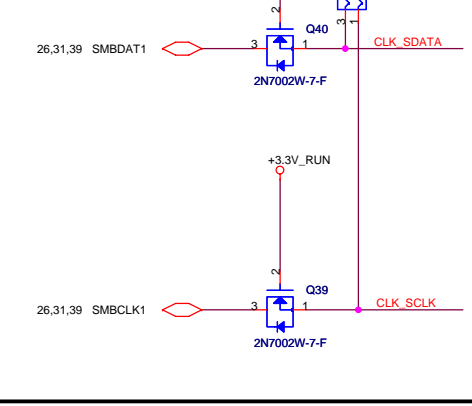


CK505  
QFN64



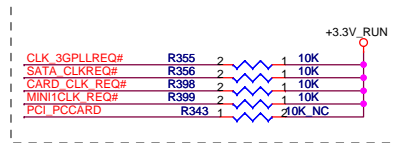
SMbus address D2

These are for  
backdrive issue.



Non-iAMT

to ATI VGA

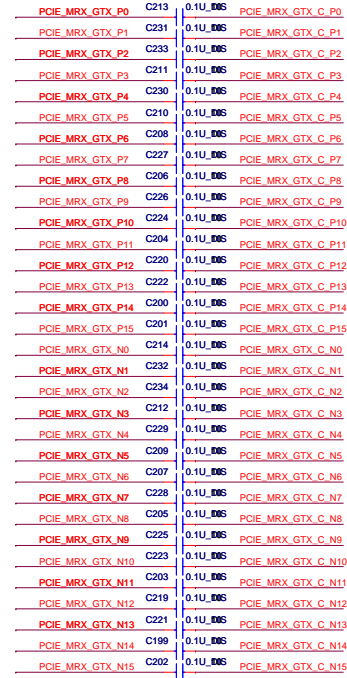


| FSC | FSB | FSA | CPU  | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1   | 0   | 1   | 100  | 100 | 33  |
| 0   | 0   | 1   | 133  | 100 | 33  |
| 0   | 1   | 1   | 166  | 100 | 33  |
| 0   | 1   | 0   | 200  | 100 | 33  |
| 0   | 0   | 0   | 266  | 100 | 33  |
| 1   | 0   | 0   | 333  | 100 | 33  |
| 1   | 1   | 0   | 400  | 100 | 33  |
| 1   | 1   | 1   | RSVD | 100 | 33  |

27M\_SEL

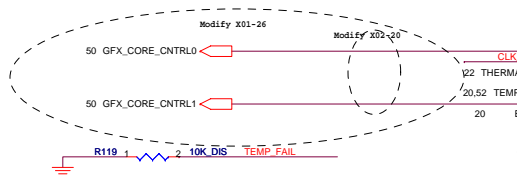
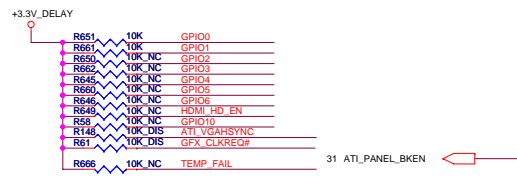
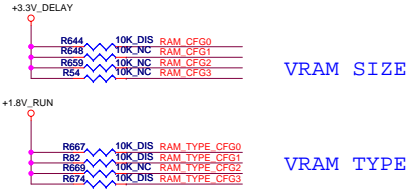
| 27M_SEL (PIN13)     | PIN20  | PIN21  | PIN24     | PIN25     |
|---------------------|--------|--------|-----------|-----------|
| 0=UMA               | DOT96T | DOT96C | 96/100M_T | 96/100M_C |
| 1 = Disc. GRFX down | SRCT0  | SRCC0  | 27Mout    | 27MSSout  |



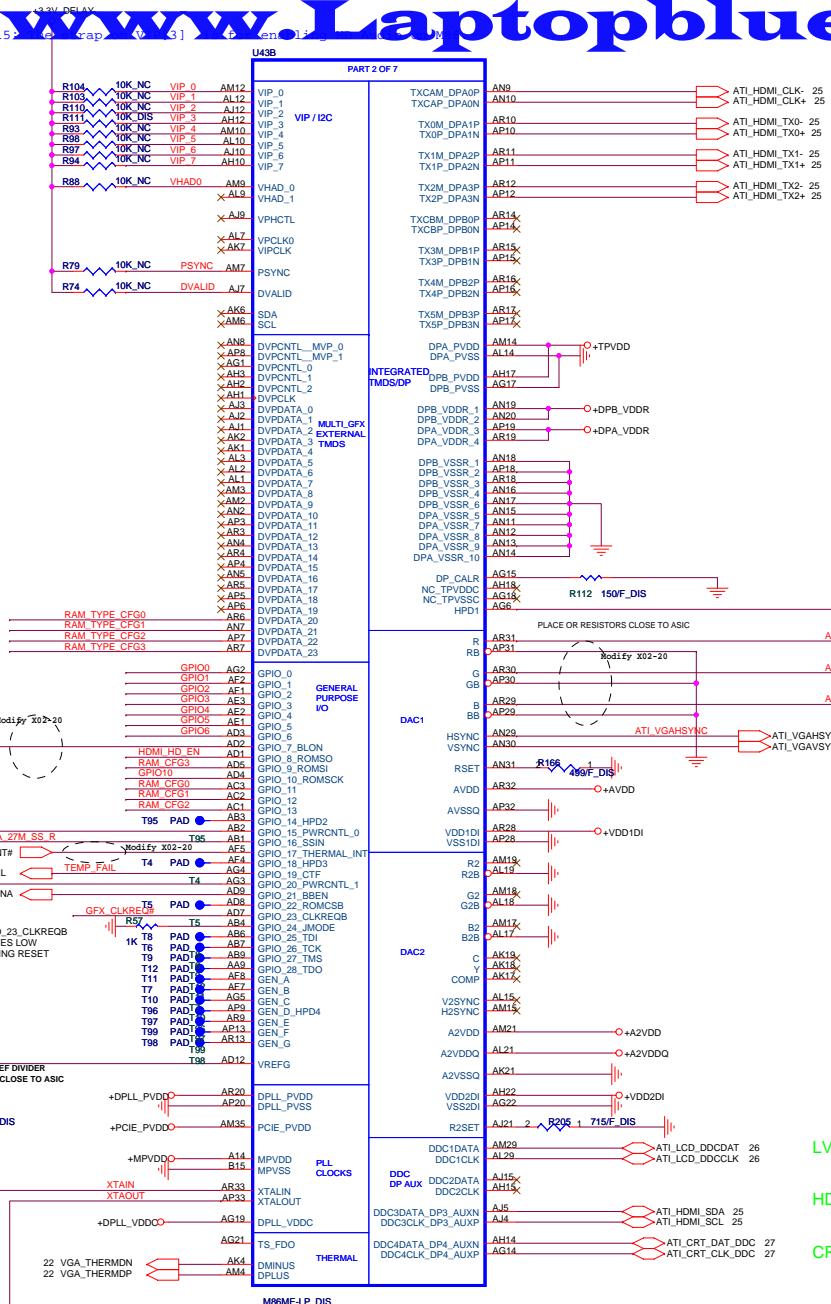
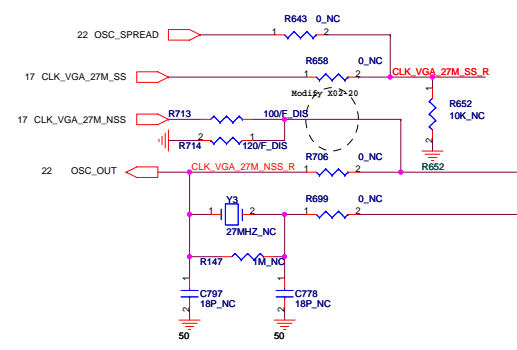


| MEMORY APERTURE SIZE SELECT |            |             |             |             |
|-----------------------------|------------|-------------|-------------|-------------|
| MEMORY SIZE                 | CFG3 GPIO9 | CFG2 GPIO13 | CFG1 GPIO12 | CFG0 GPIO11 |
| 128MB                       | X          | 0           | 0           | 0           |
| 256MB                       | X          | 0           | 0           | 1           |
| 64MB                        | X          | 0           | 1           | 0           |
| 512MB                       | X          | 1           | 0           | 0           |

| Memory Straps                 | RAM TYPE_CFG3 | RAM TYPE_CFG2 | RAM TYPE_CFG1 | RAM TYPE_CFG0 |
|-------------------------------|---------------|---------------|---------------|---------------|
| 400 MHz 256MB(16M*16) Hynix   | 1             | 1             | 1             | 1             |
| 400 MHz 256MB(16M*16) Qimonda | 1             | 1             | 1             | 0             |
| 500 MHz 256MB(16M*16) Hynix   | 1             | 1             | 0             | 1             |
| 500 MHz 256MB(16M*16) Qimonda | 1             | 1             | 0             | 0             |
| 500 MHz 256MB(16M*16) Samsung | 1             | 0             | 1             | 1             |



| GFX_CORE_CNTRL_TABLE |                 |               |
|----------------------|-----------------|---------------|
| GFX_CORE_CNTRL0      | GFX_CORE_CNTRL1 | +VCC_GFX_CORE |
| LOW                  | LOW             | 0.9V          |
| HIGH                 | LOW             | 0.95V         |
| HIGH                 | HIGH            | 1.1V          |



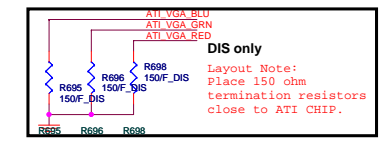
HDMI CONN

ATI VGA\_RED

ATI VGA\_GRN

ATI VGA\_BLU

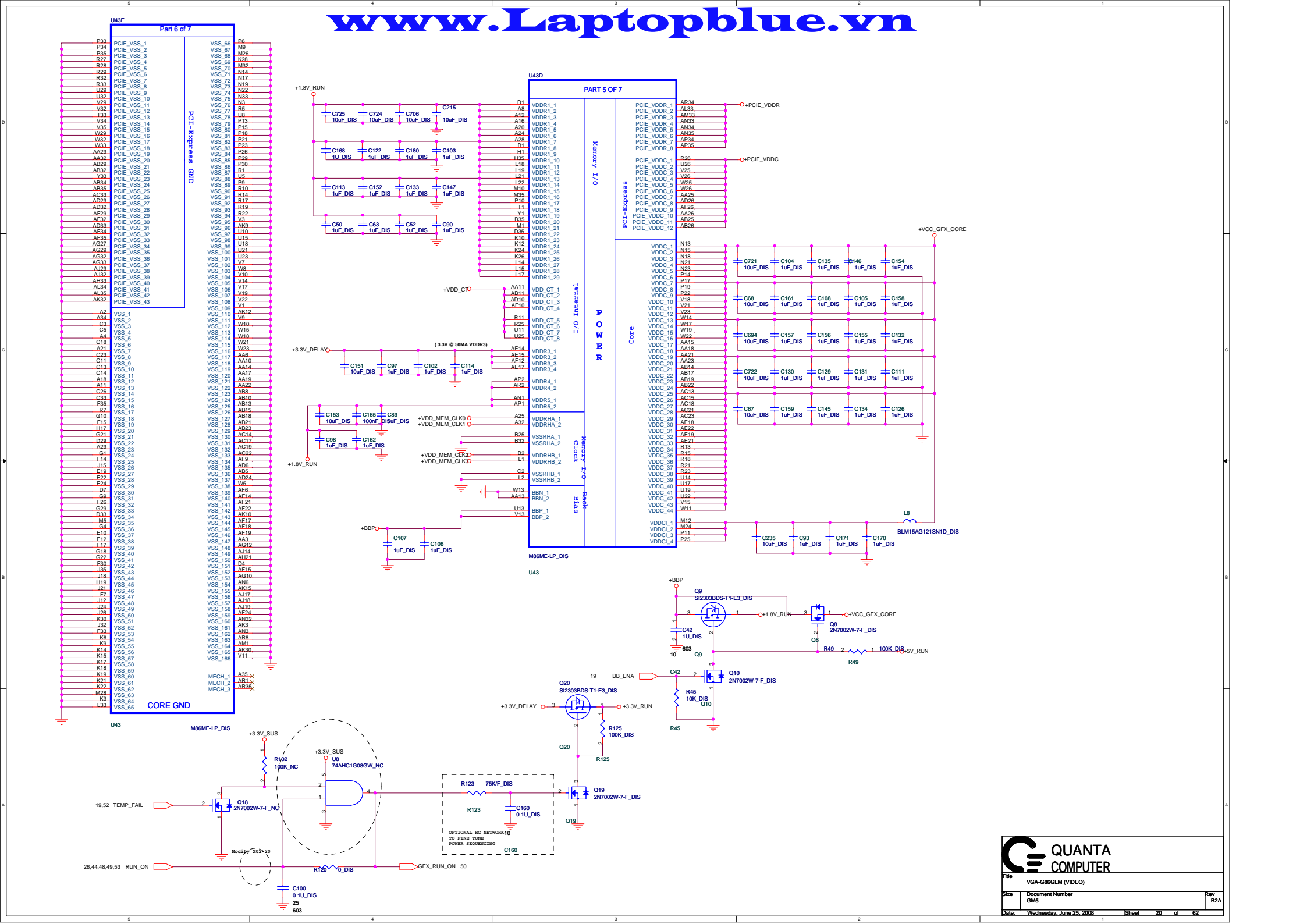
ATI VGA\_SYNC



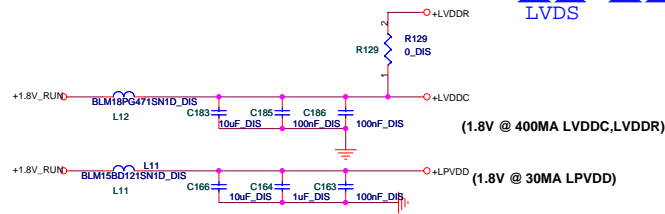
LVDS

HDMI

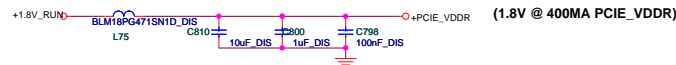
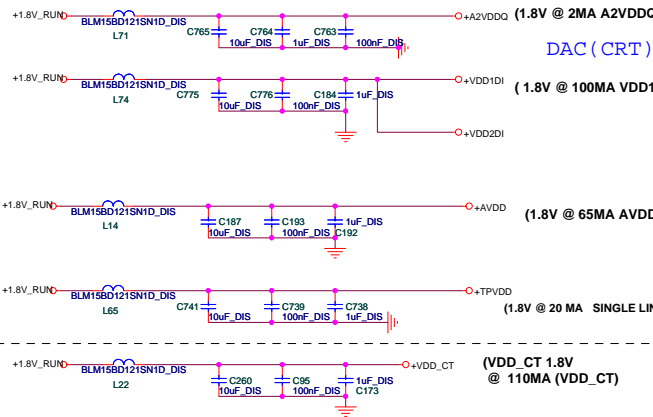
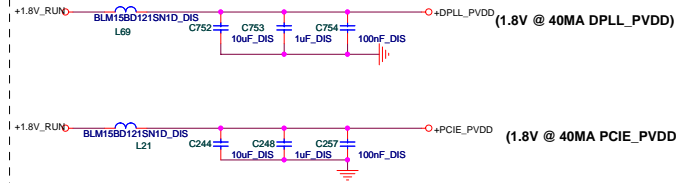
CRT



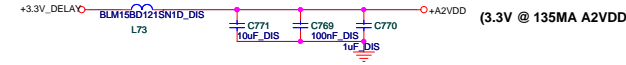
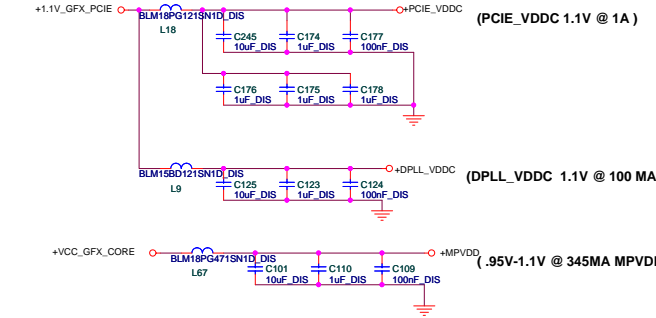
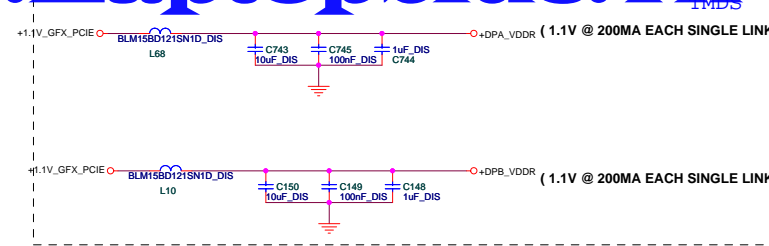
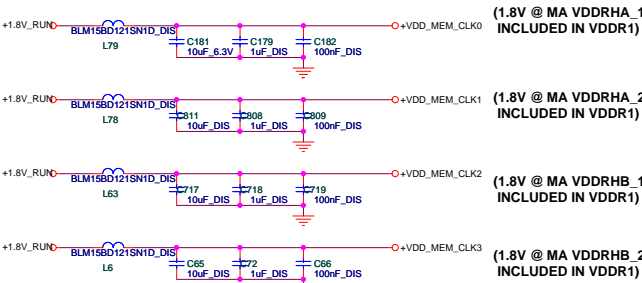
## LVDS



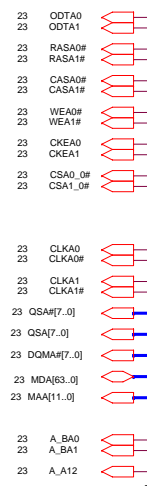
## PLL\_CLK



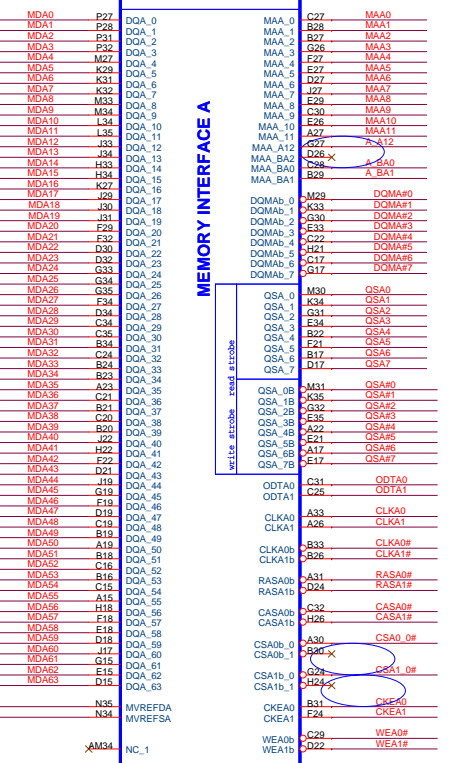
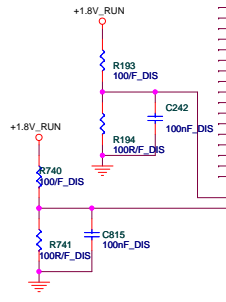
## MEM IO CLK



PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



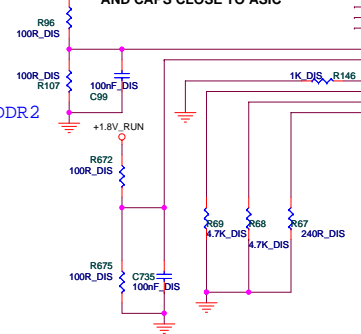
PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC



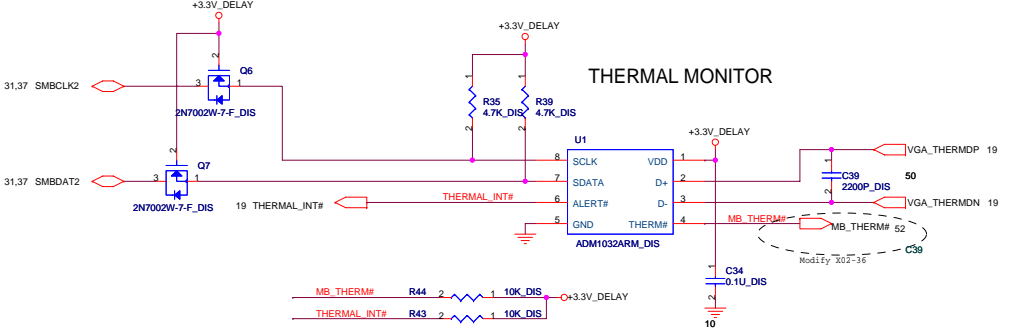
NC for 16M x16 DDR2

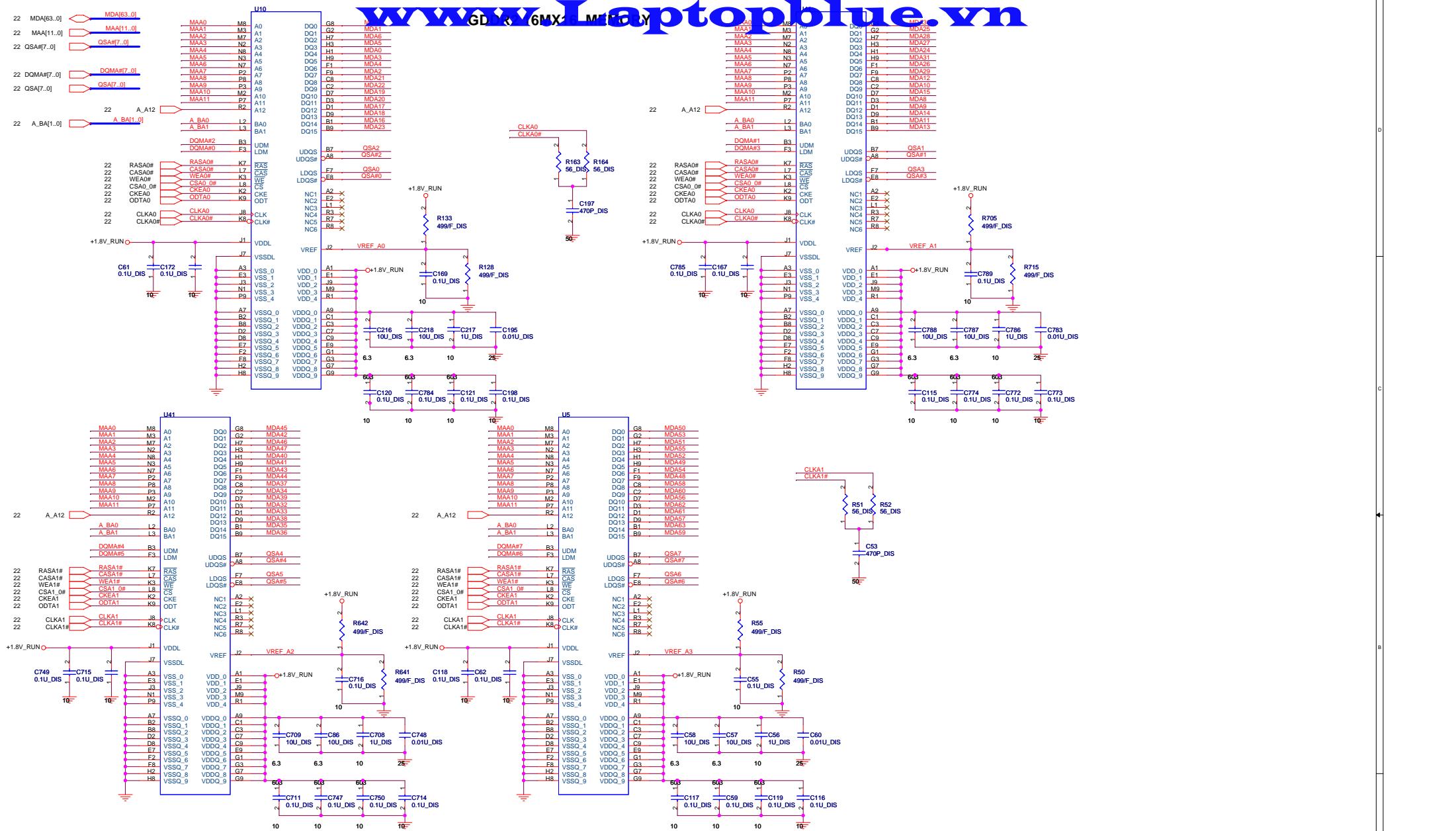
NC for 16M x16 DDR2

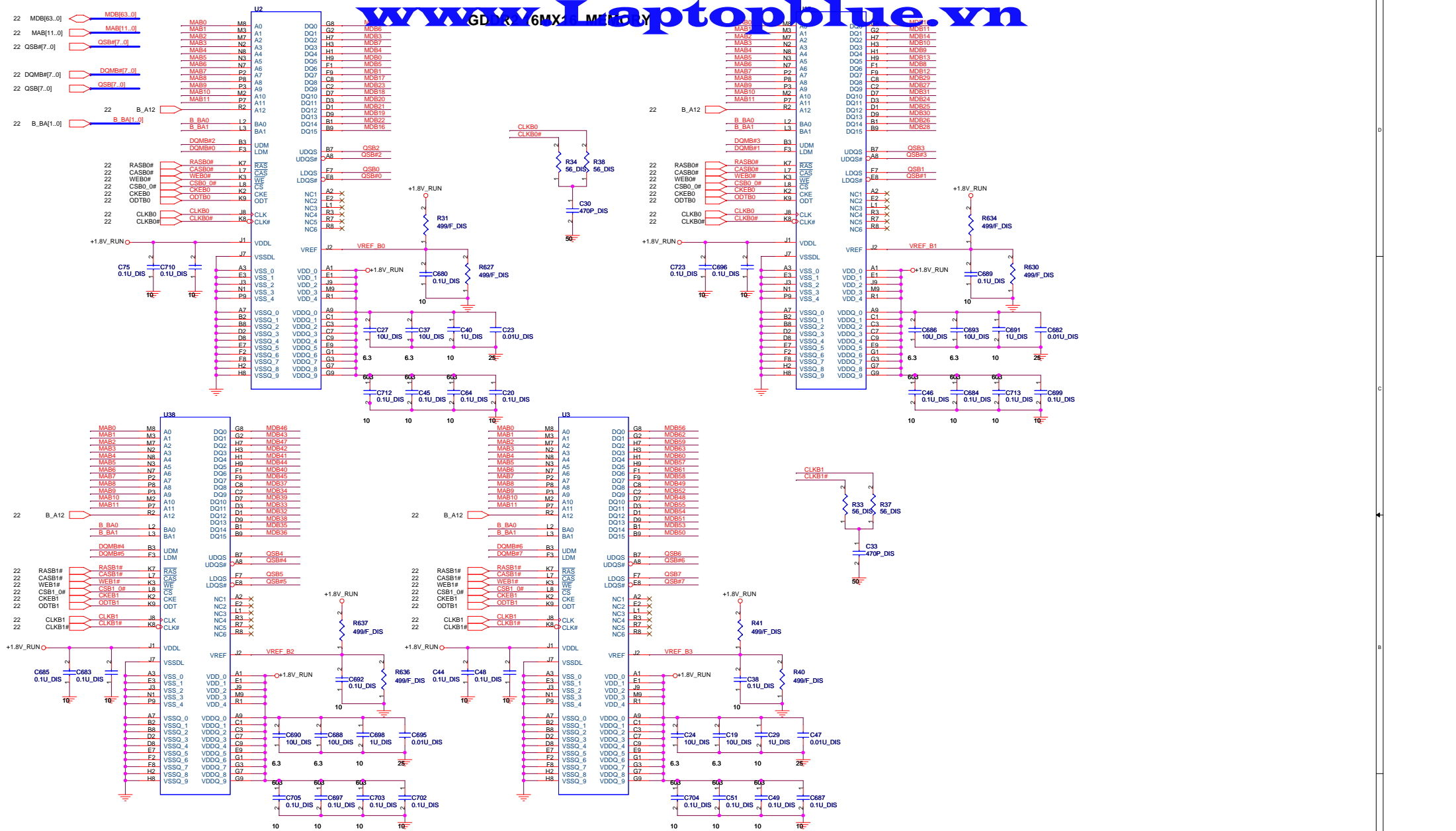
PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC

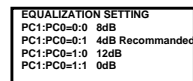


THERMAL MONITOR

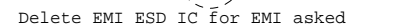
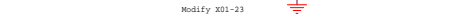
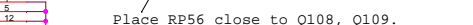
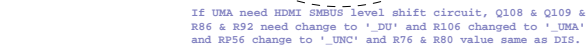




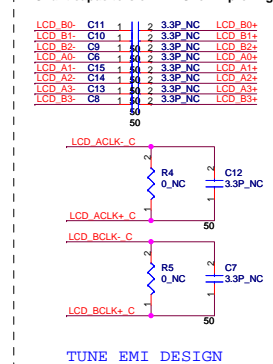
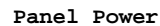
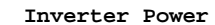
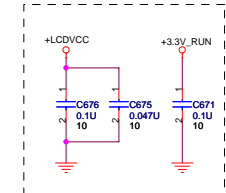


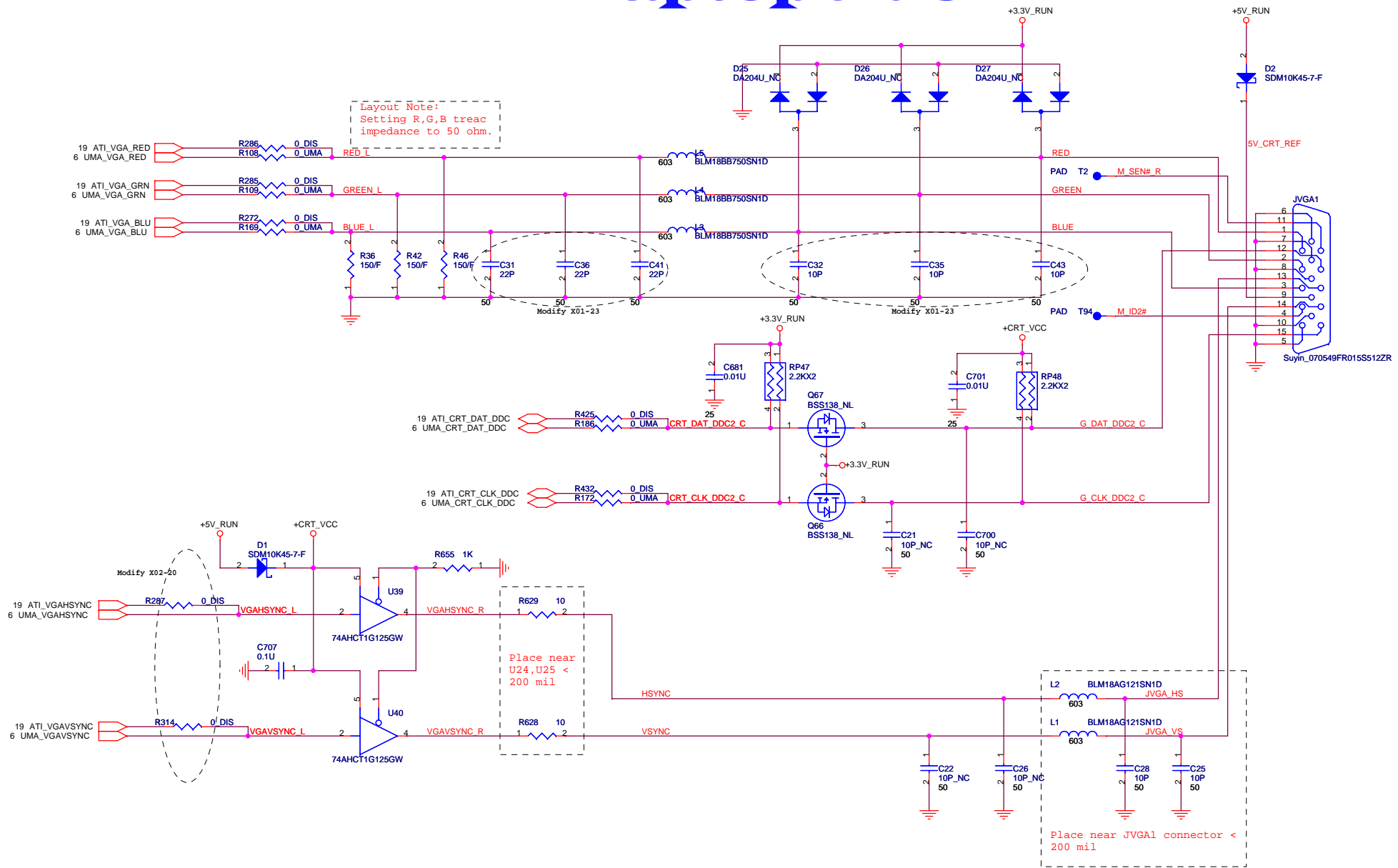


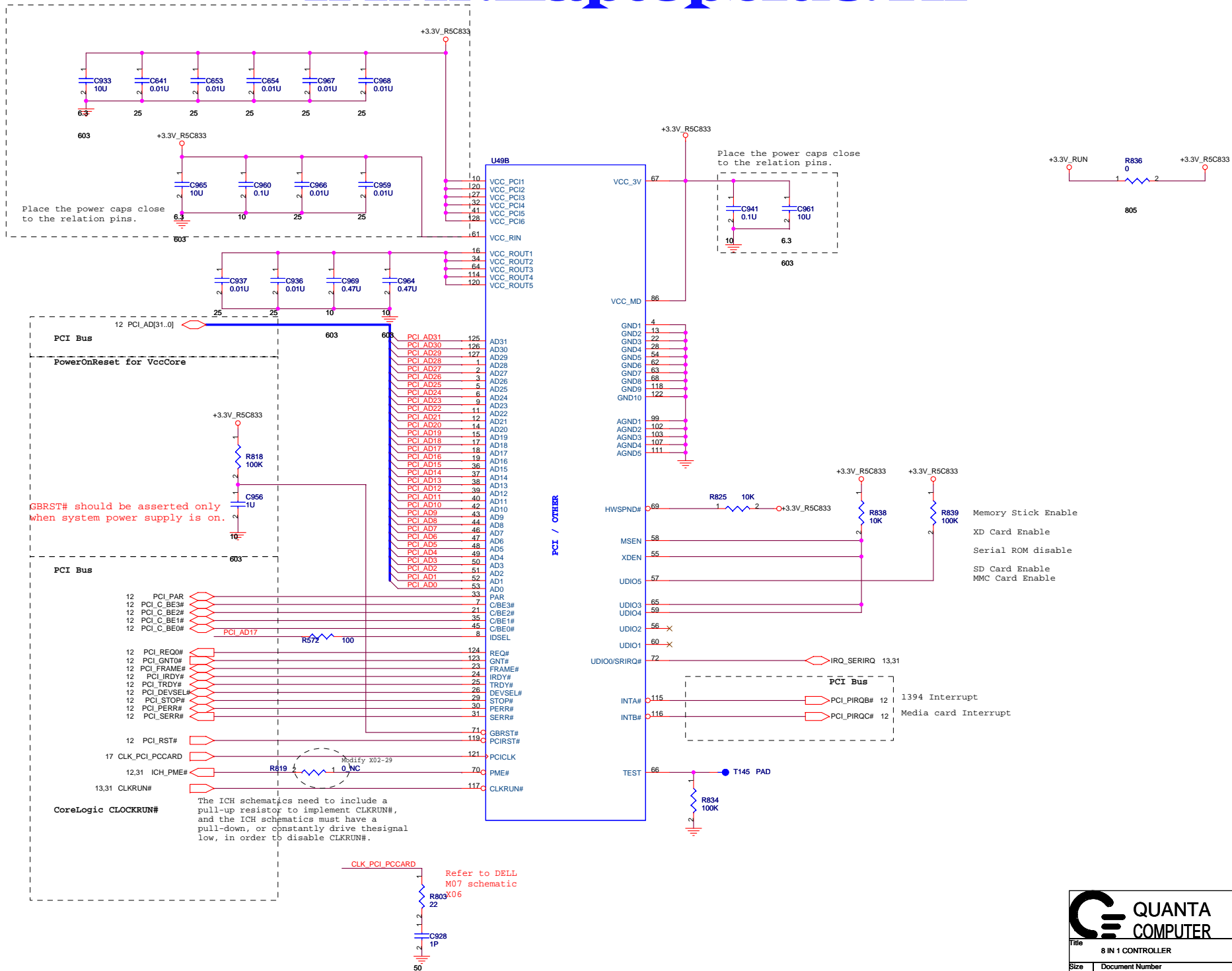
|   |                              |
|---|------------------------------|
| <b>SLC2/SDAZ Low-level input/output Voltage</b> |                              |
| CFG1:CFG0=0:0                                   | VIL:<0.4V VOL:0.6V (Default) |
| CFG1:CFG0=0:1                                   | VIL:<0.36V VOL:0.55V         |
| CFG1:CFG0=1:0                                   | VIL:<0.44V VOL:0.65V         |
| CFG1:CFG0=1:1                                   | VIL:<0.36V VOL:0.6V          |

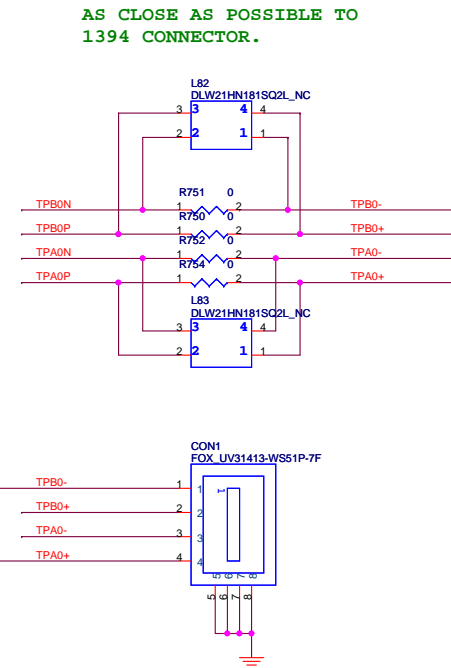
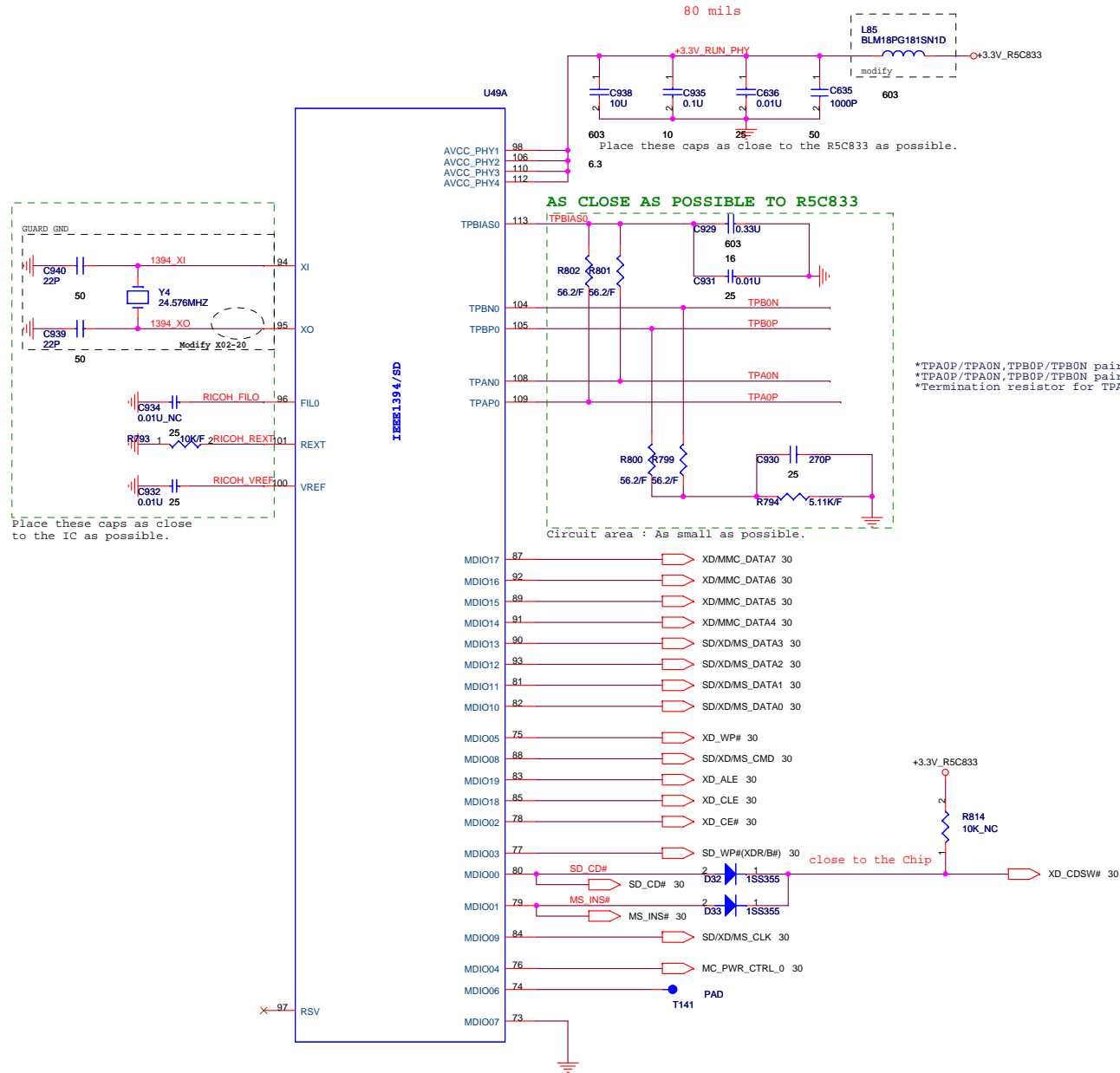


Delete EMI ESD IC for EMI asked  
HDMI signals link to CONN directly





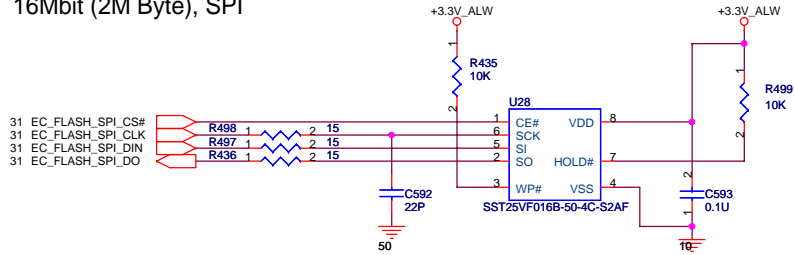




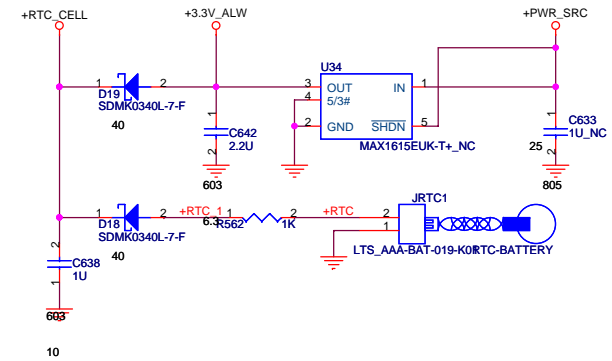




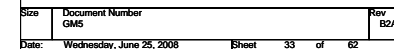
# 16Mbit (2M Byte), SPI



# RTC BATTERY

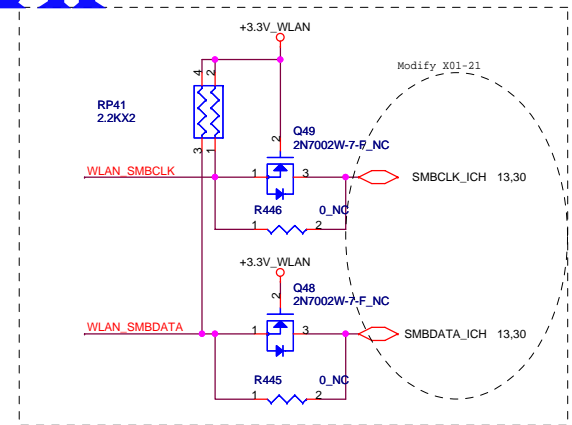
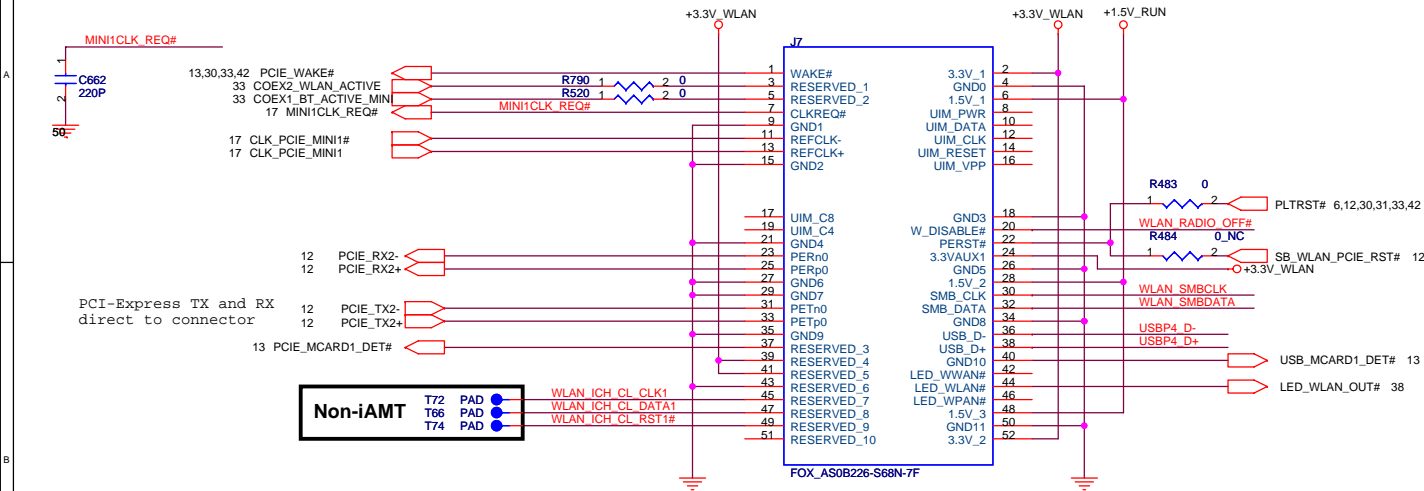


|       |            |
|-------|------------|
| Title | WWAN, WPAN |
|-------|------------|

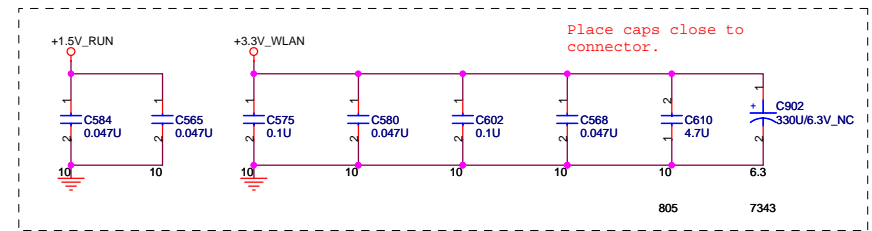
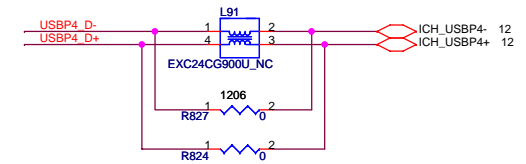
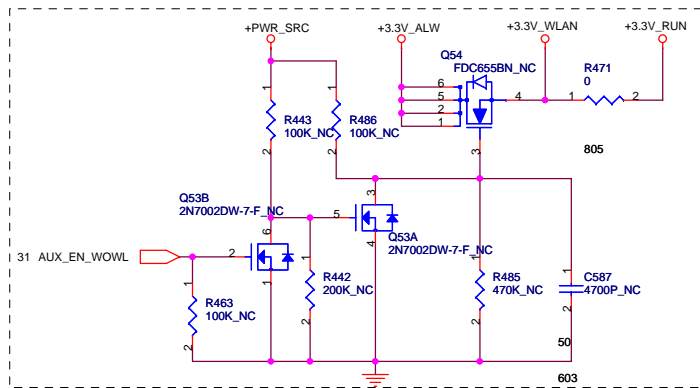
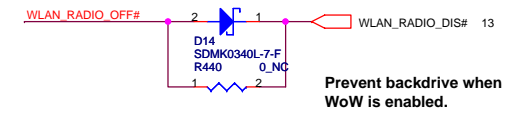


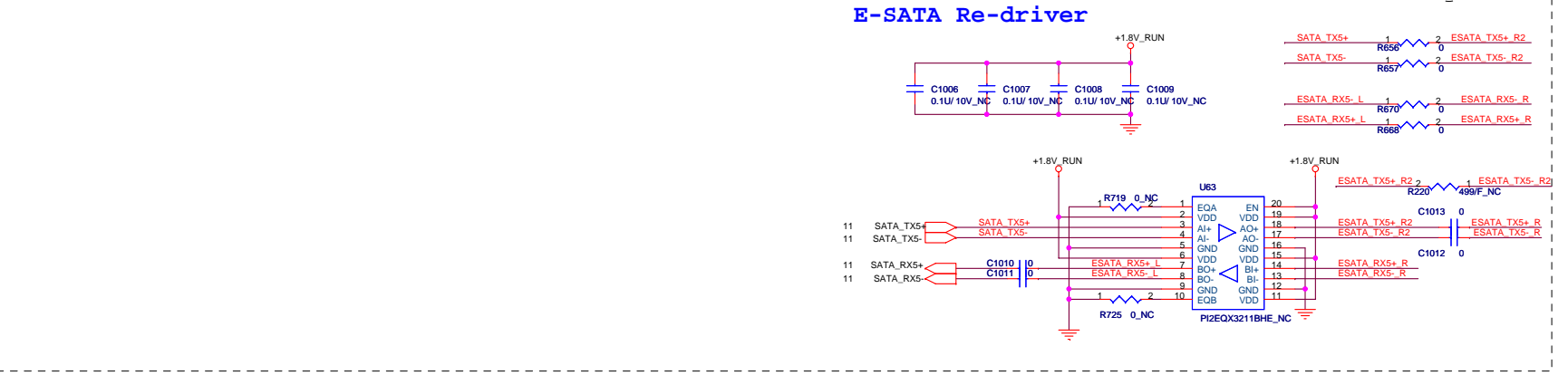
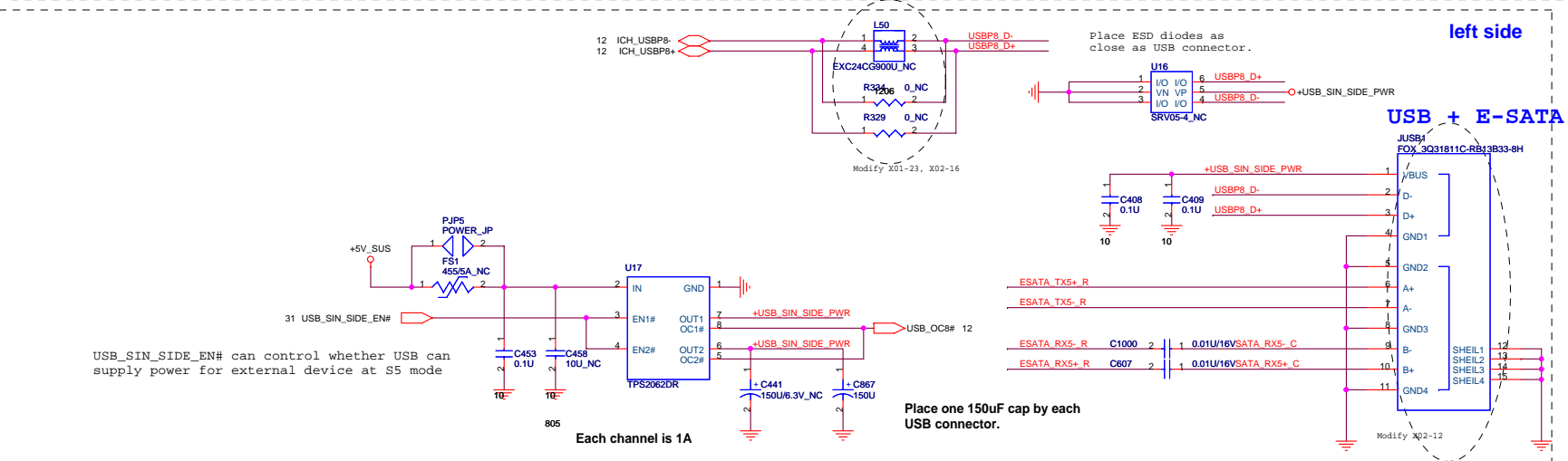
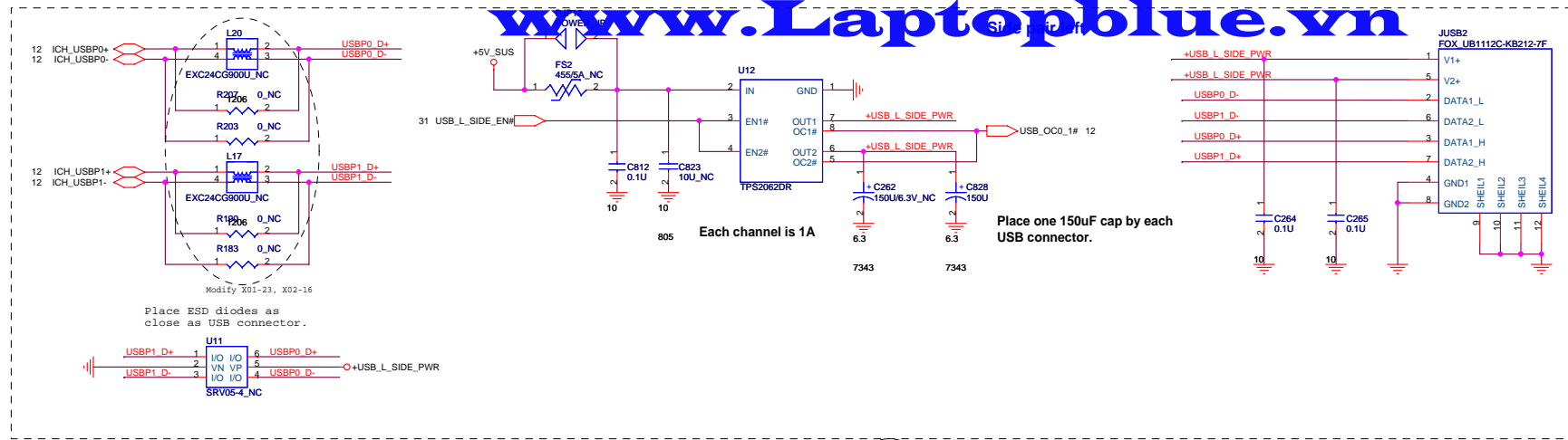
|   |
|---|
| 7 |
|---|

## MiniCard WLAN connector



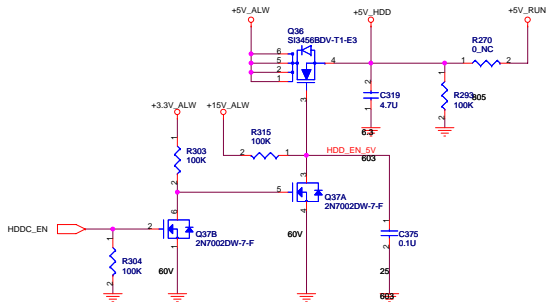
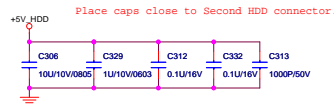
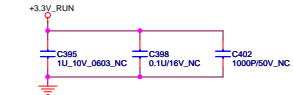
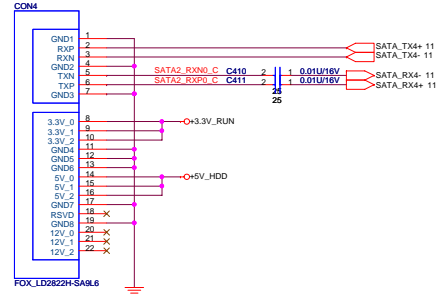
### Support for WoW



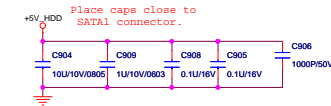
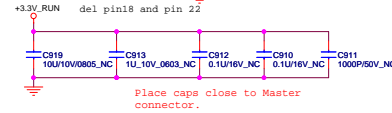
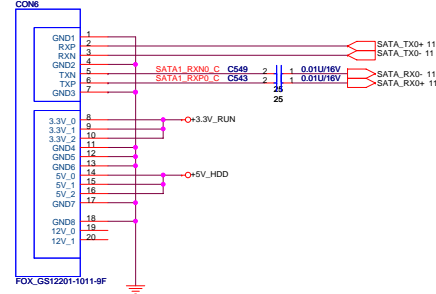


SATA Connector.

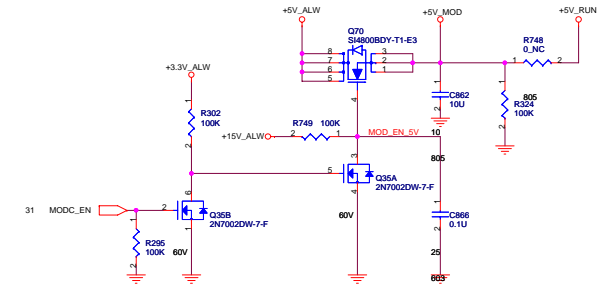
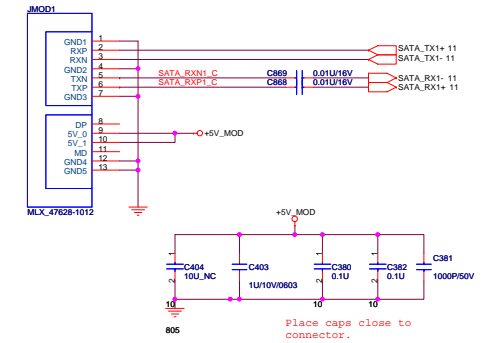
Second HDD



Master

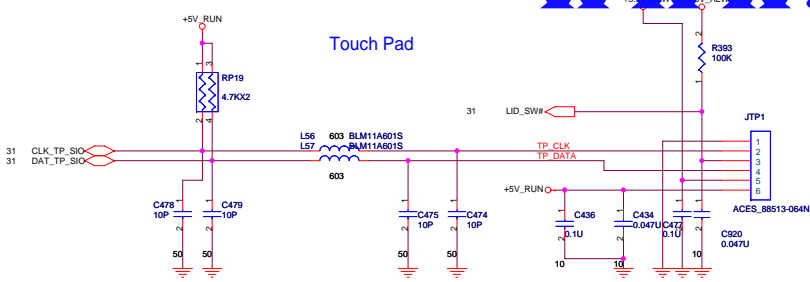


ODD Connector

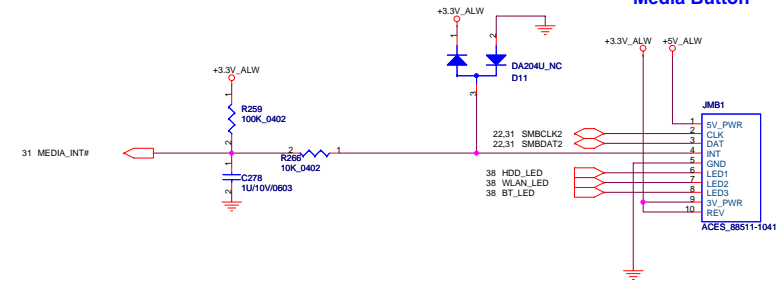


|      |                          |       |          |
|------|--------------------------|-------|----------|
| File | SATA (HDD&CD_ROM)        | Rev   | B2A      |
| Size | Document Number          |       |          |
|      | GMS                      |       |          |
| Date | Wednesday, June 25, 2008 | Sheet | 38 of 62 |

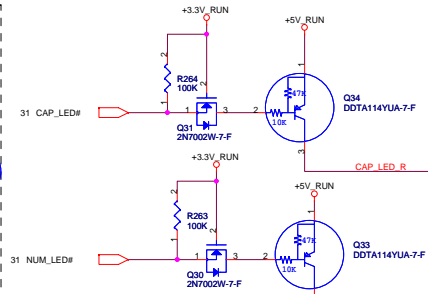
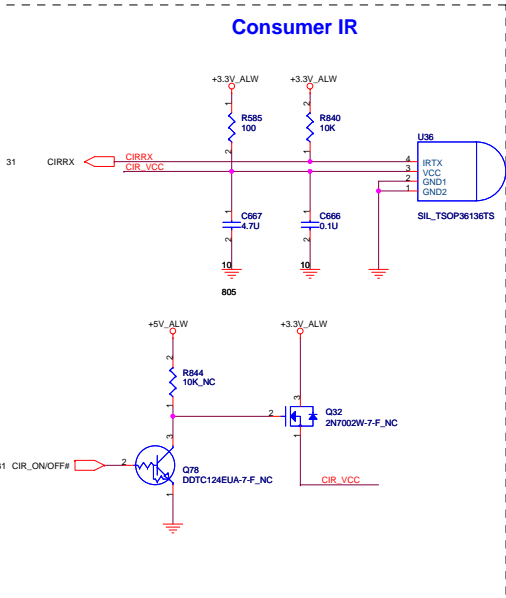
### Touch Pad



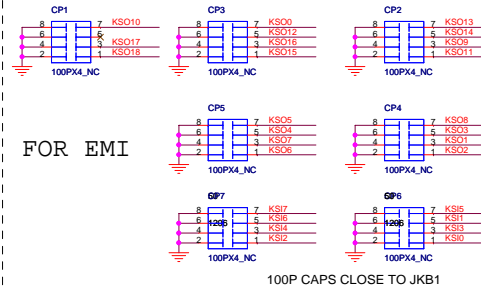
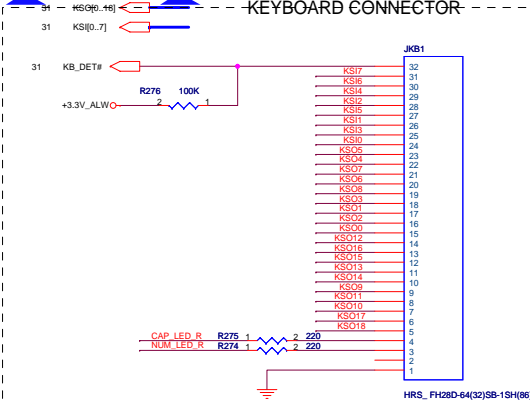
### Media Button



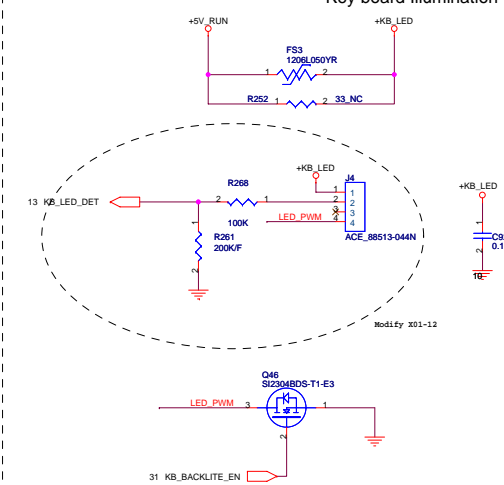
### Consumer IR



### KEYBOARD CONNECTOR



### Key board Illumination



TOUCH PAD, BLUE TOOTH & FIR

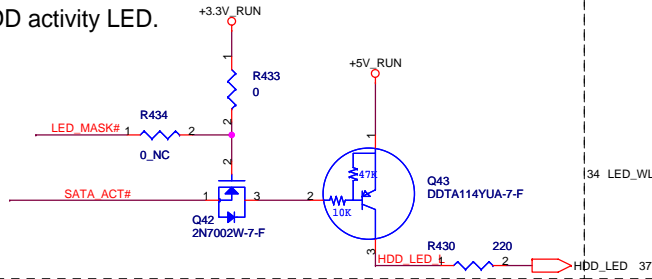
Document Number  
GM5

Date: Wednesday, June 25, 2008

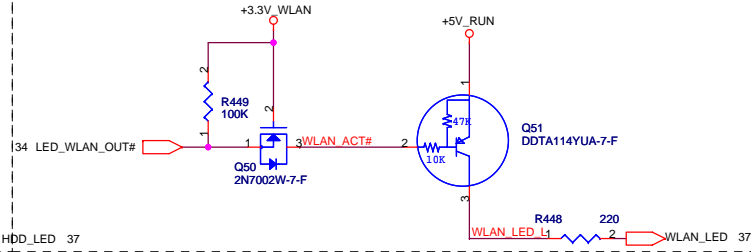
Sheet 37 of 82

Rev B2A

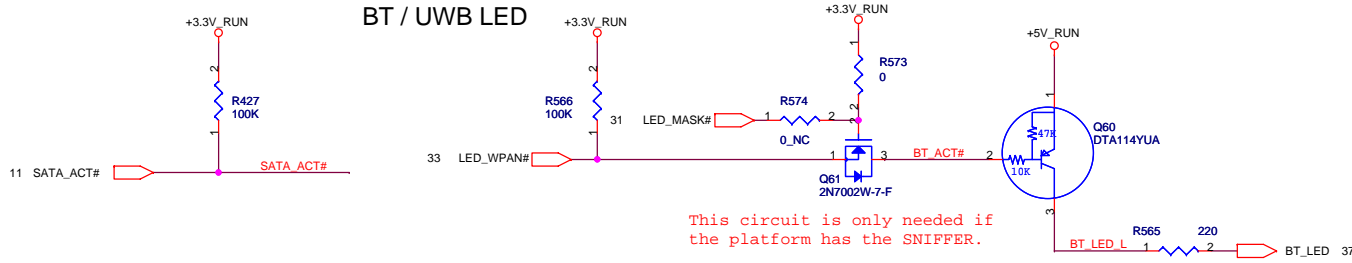
### HDD activity LED.



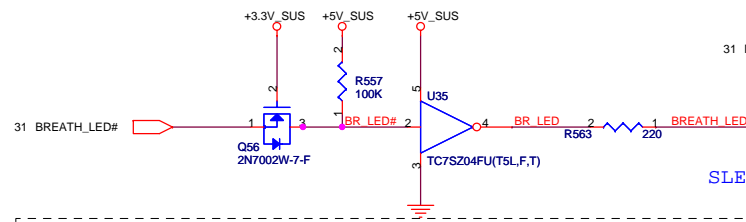
### WLAN



### BT / UWB LED

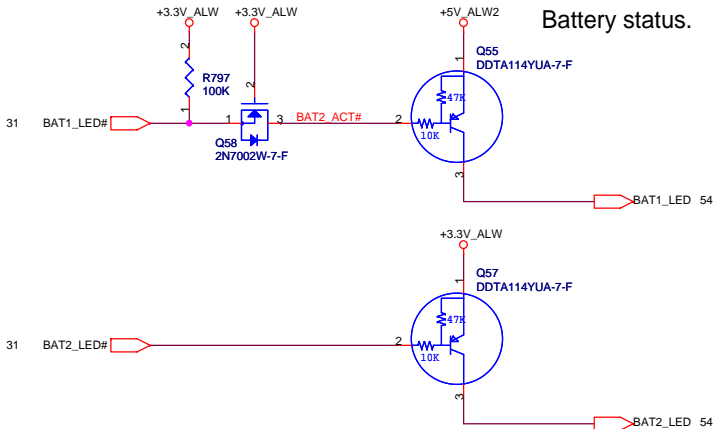


### Power & Suspend.

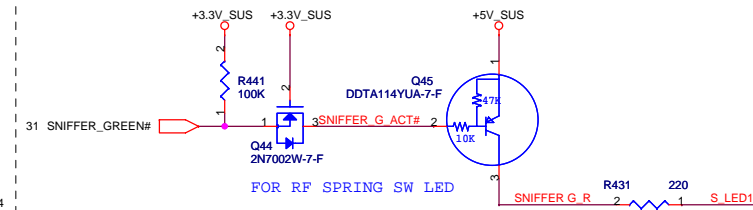


SLED2:AP detection

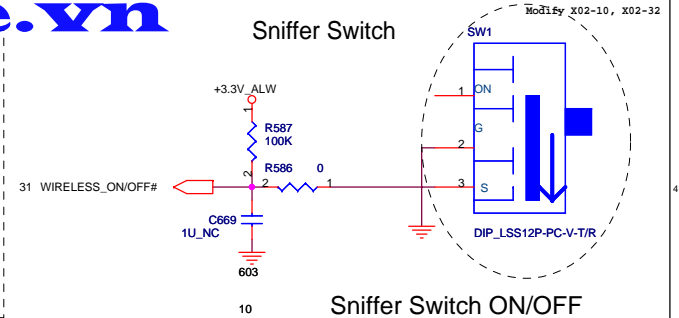
### Battery status.



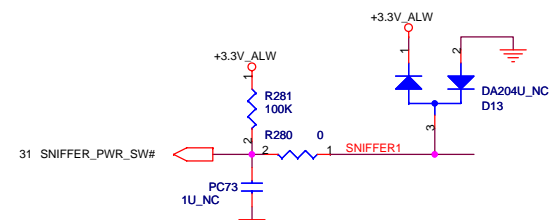
### Sniffer LED



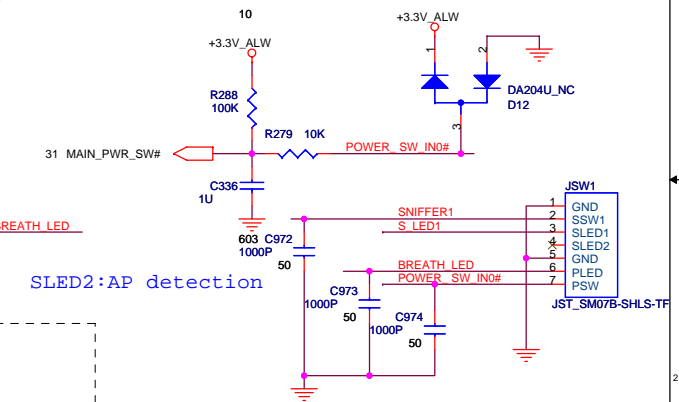
### Sniffer Switch



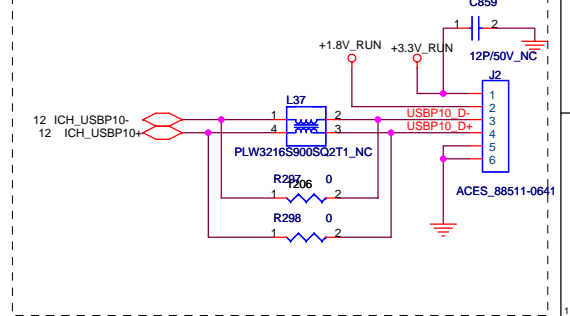
### Sniffer Switch ON/OFF



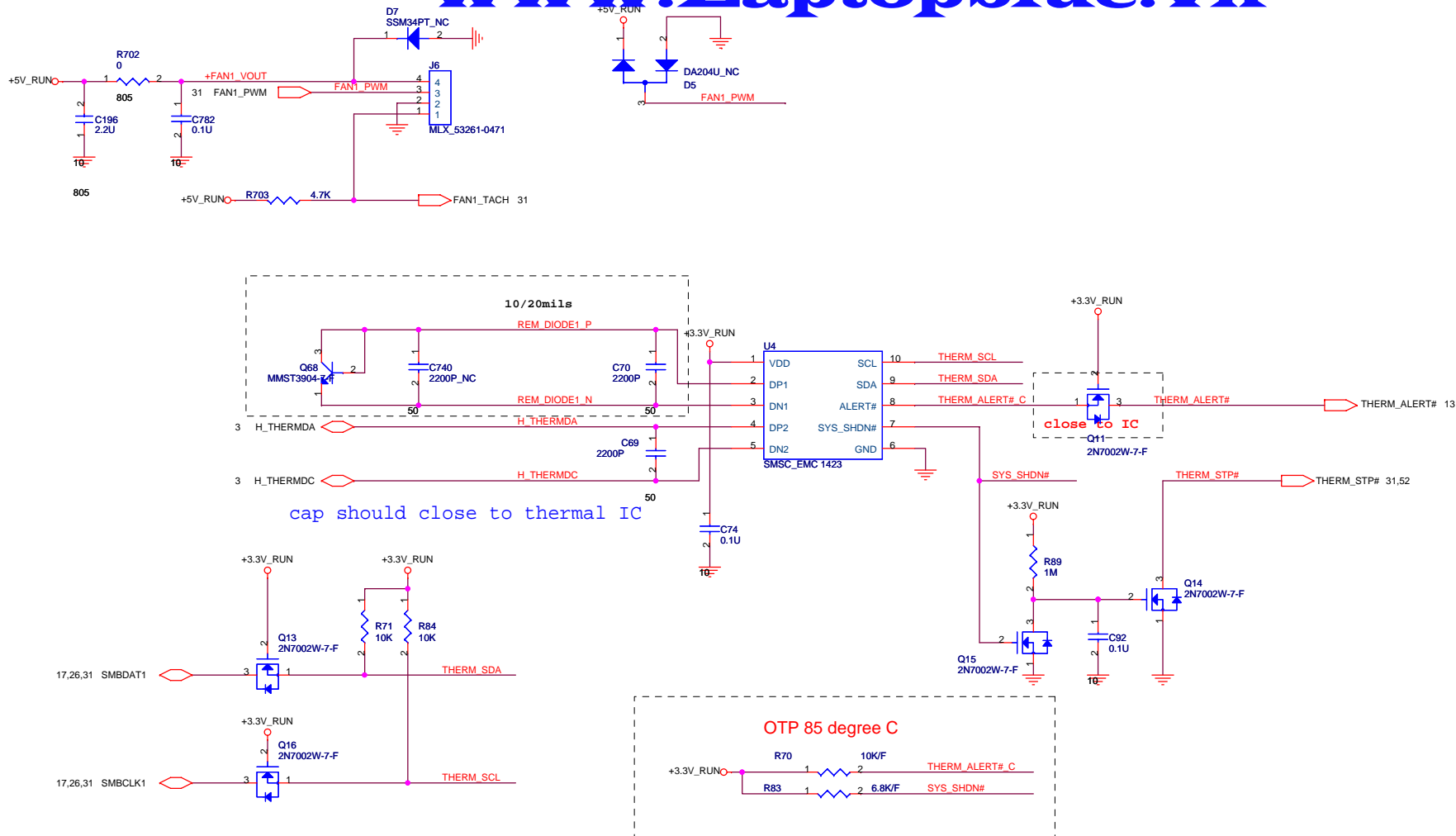
### Power Switch



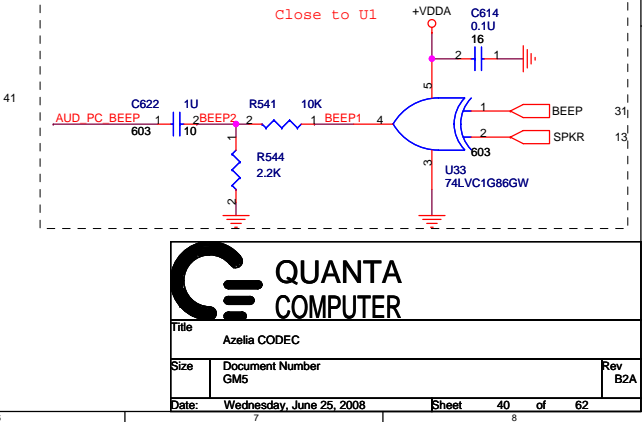
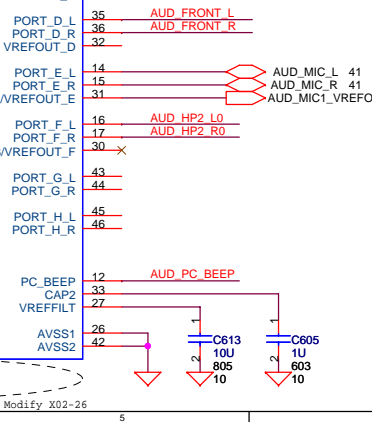
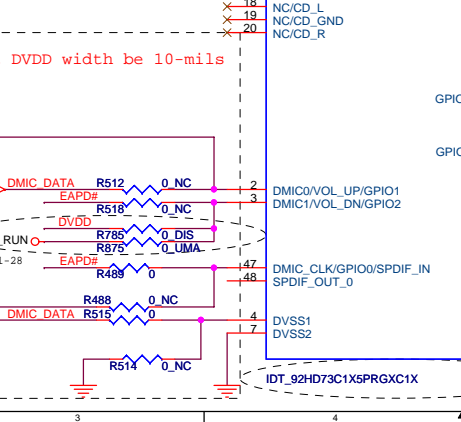
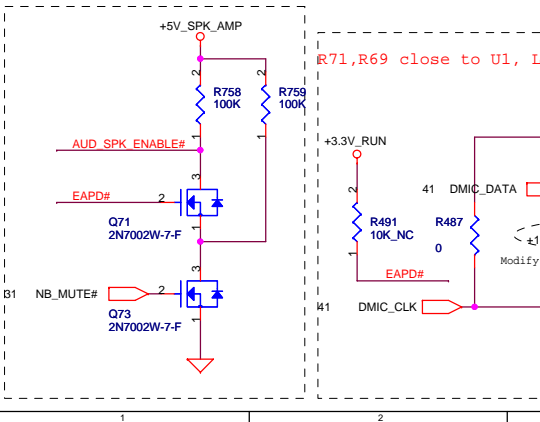
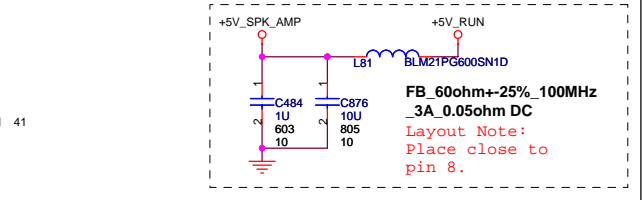
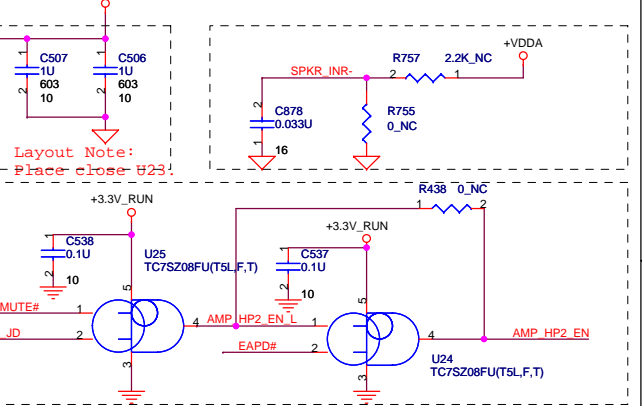
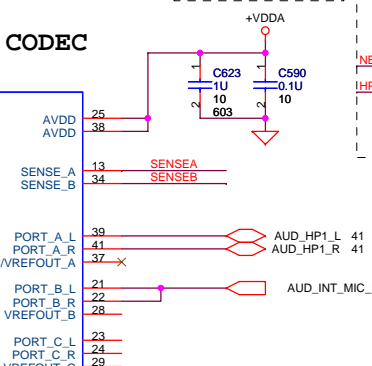
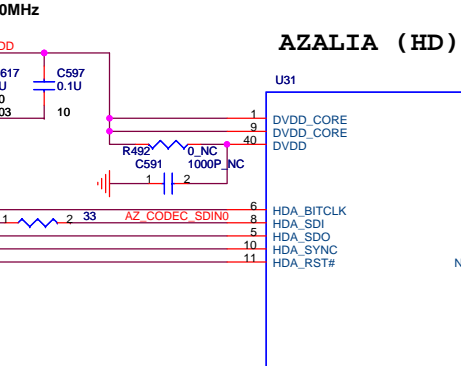
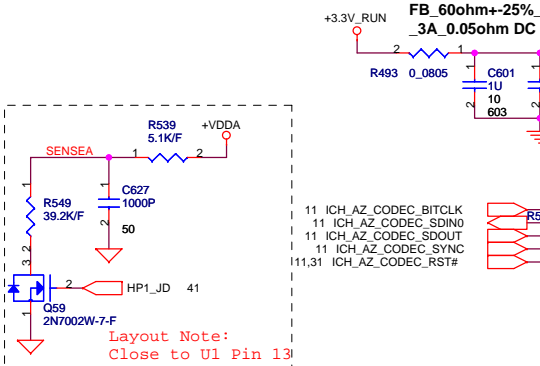
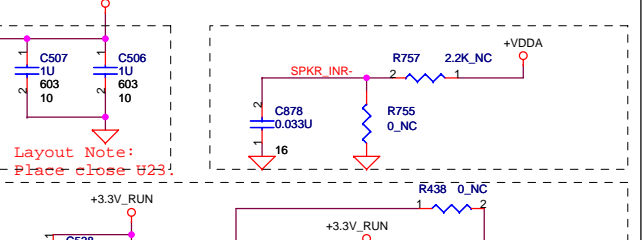
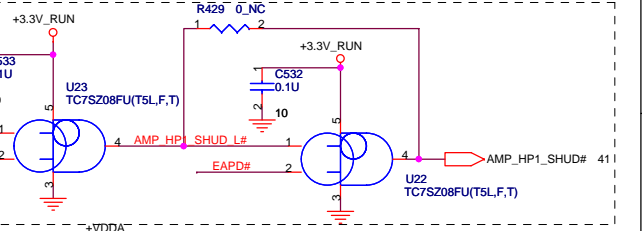
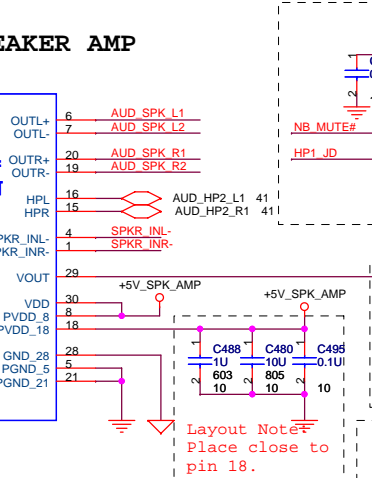
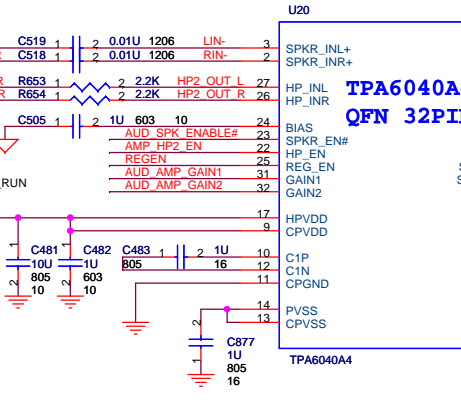
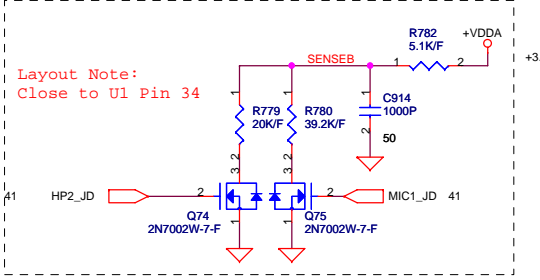
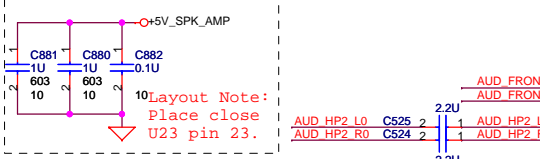
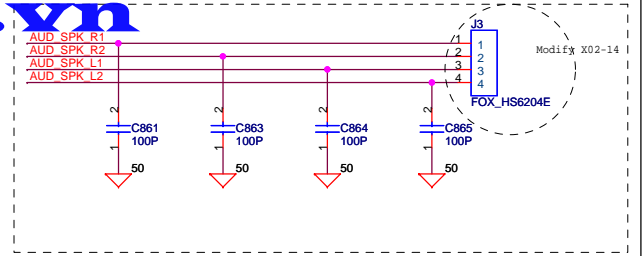
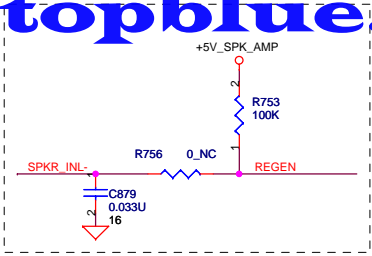
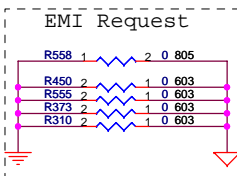
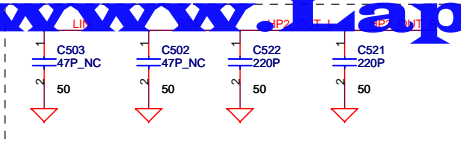
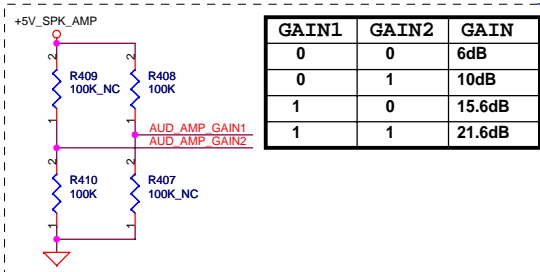
### Biometric



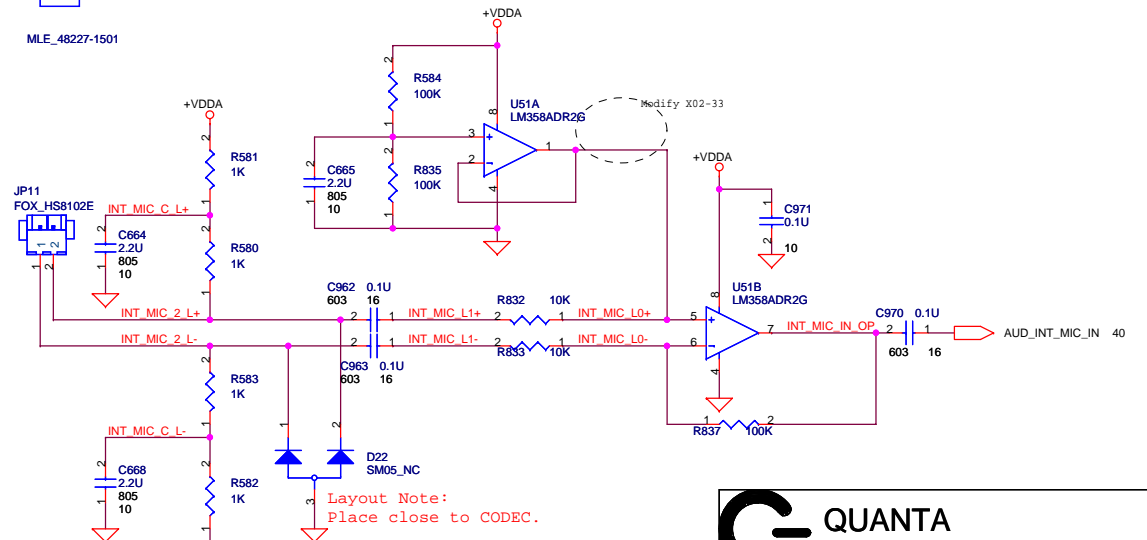
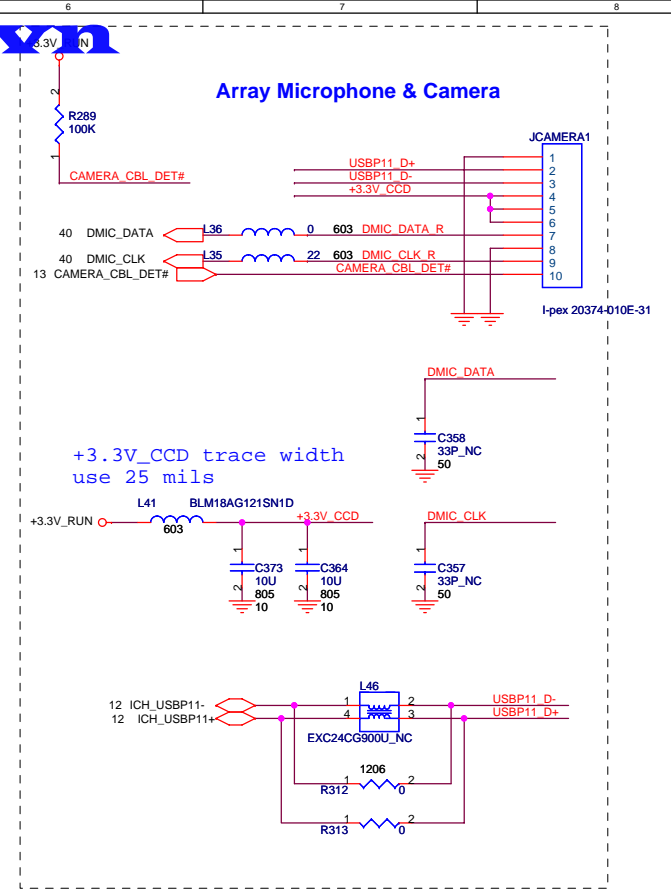
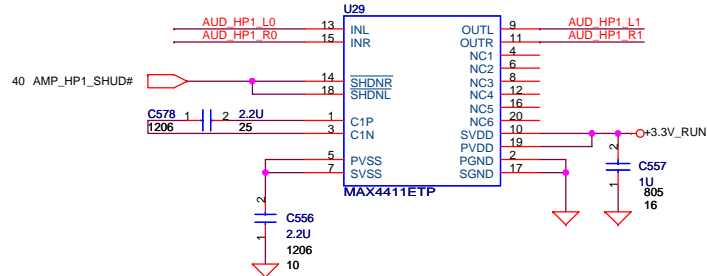
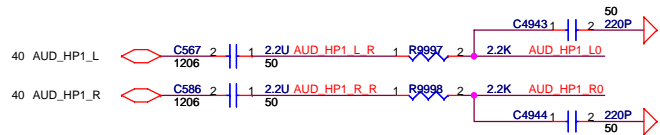
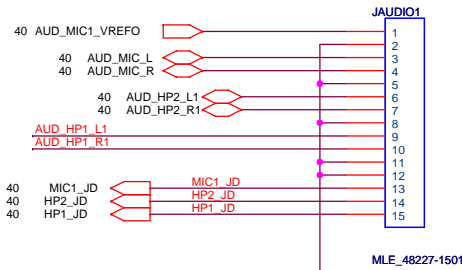
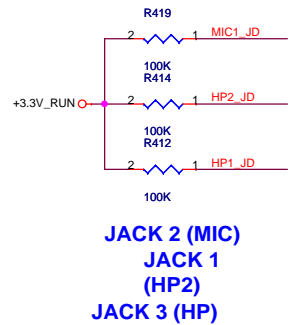
|       |                          |       |                        |
|-------|--------------------------|-------|------------------------|
| Title |                          |       | SWITCH, KEYBOARD & LED |
| Size  | Document Number          | Rev   |                        |
|       | GM5                      | B2A   |                        |
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| GAIN1 | GAIN2 | GAIN   |
|-------|-------|--------|
| 0     | 0     | 6dB    |
| 0     | 1     | 10dB   |
| 1     | 0     | 15.6dB |
| 1     | 1     | 21.6dB |

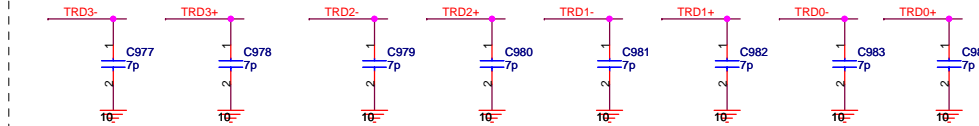
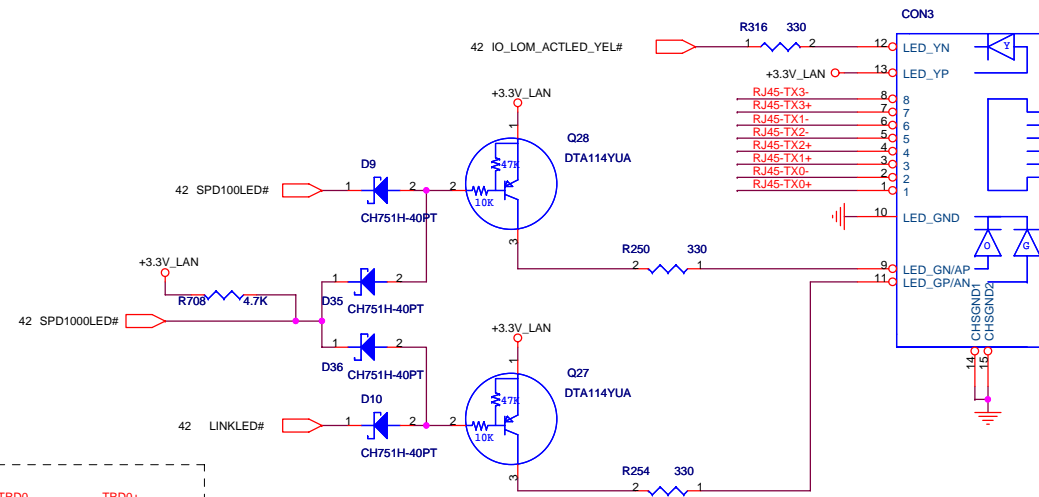


# Headphone Jack Stereo MIC Jack

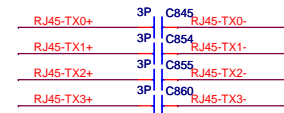


|  |                          |       |          |
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| Title: LAN   |                          |       |          |
| Size:  | Document Number          | Rev   |          |
|  | GMS                      | B2A   |          |
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## RJ-45 Connector

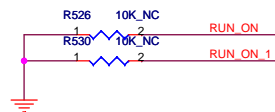
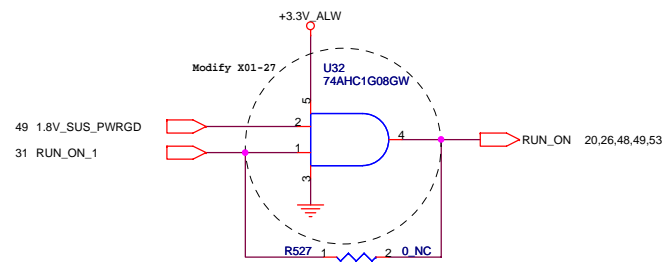
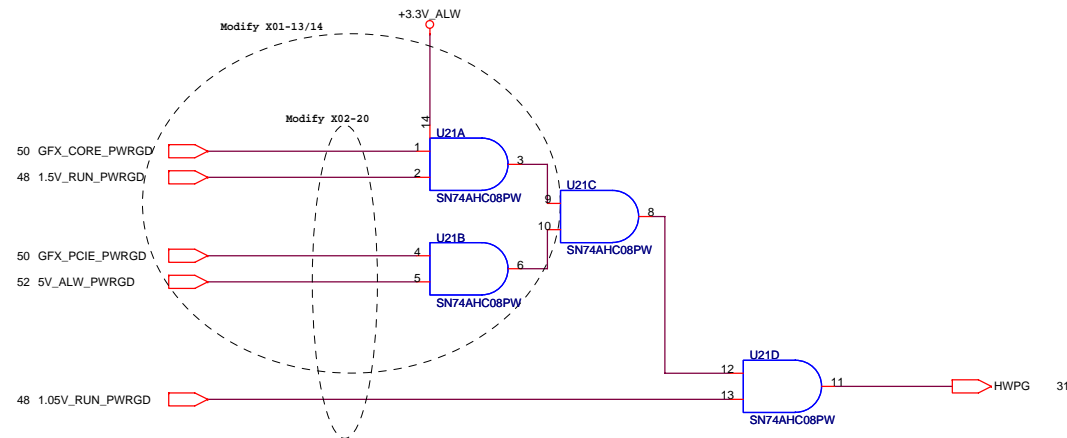
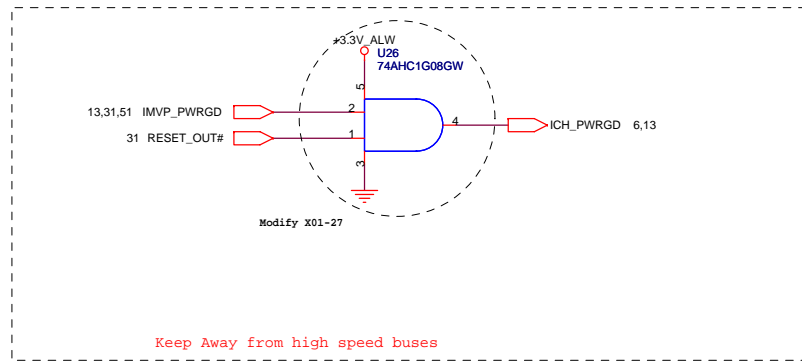


FOR EMI requirement and should close to L80



layout note:  
cap should close to CONN

Reserved for EMI.





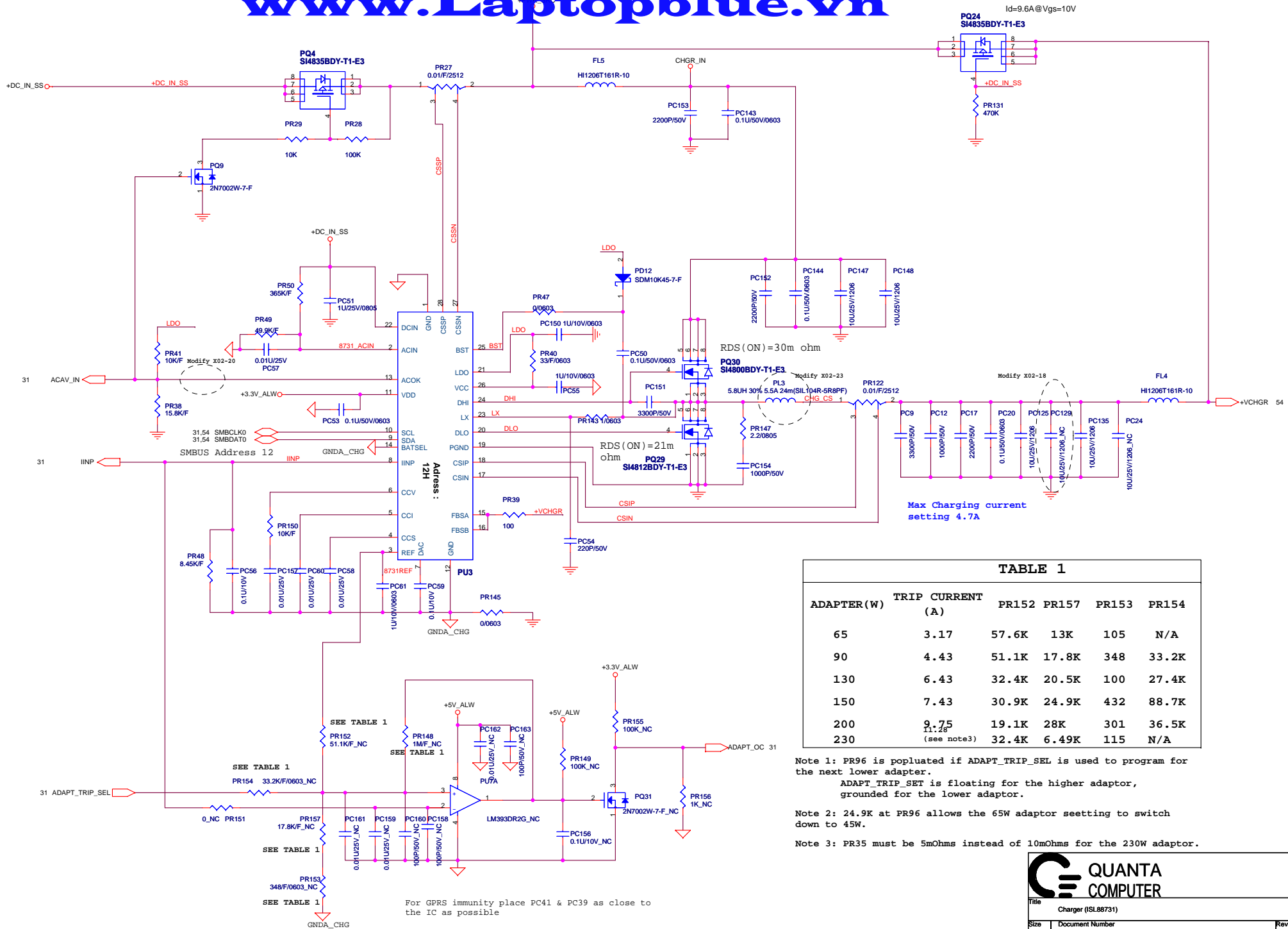


TABLE 1

| ADAPTER (W) | TRIP CURRENT (A) | PR152 | PR157 | PR153 | PR154 |
|-------------|------------------|-------|-------|-------|-------|
| 65          | 3.17             | 57.6K | 13K   | 105   | N/A   |
| 90          | 4.43             | 51.1K | 17.8K | 348   | 33.2K |
| 130         | 6.43             | 32.4K | 20.5K | 100   | 27.4K |
| 150         | 7.43             | 30.9K | 24.9K | 432   | 88.7K |
| 200         | 9.75             | 19.1K | 28K   | 301   | 36.5K |
| 230         | (see note3)      | 32.4K | 6.49K | 115   | N/A   |

Note 1: PR96 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adaptor.

ADAPT\_TRIP\_SET is floating for the higher adaptor, grounded for the lower adaptor.


Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

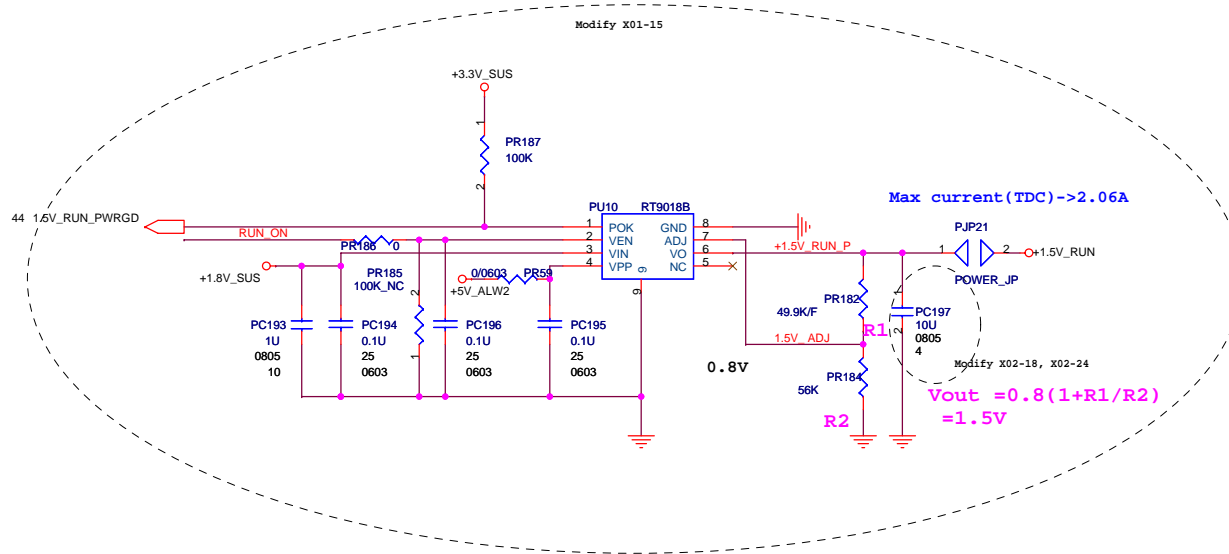
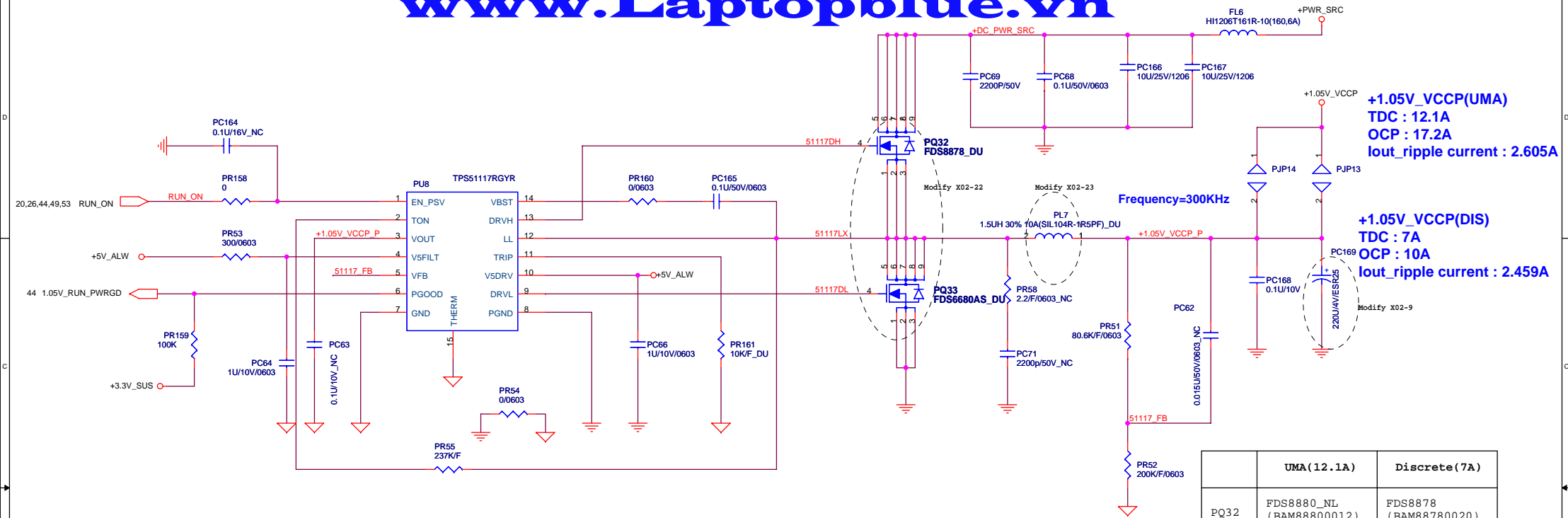
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.



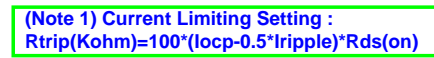
Charger (ISL88731)

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NUMBER SAME AS DISCRETE

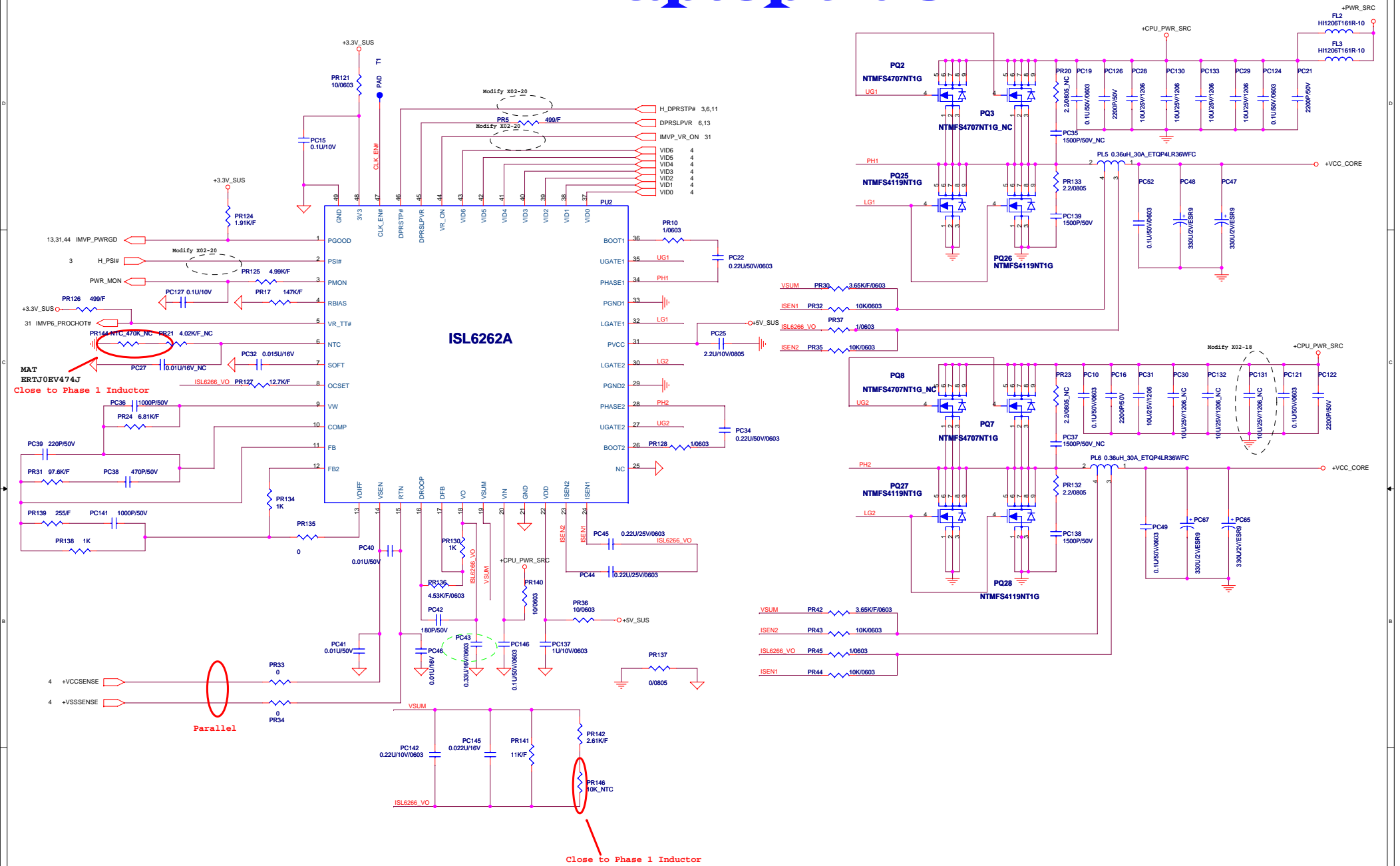
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| Title  |                          |                |
| Size   | Document Number          | Rev            |
|  | GM5                      | B2A            |
| Date:  | Wednesday, June 25, 2008 | Sheet 47 of 62 |

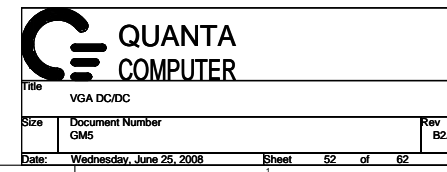


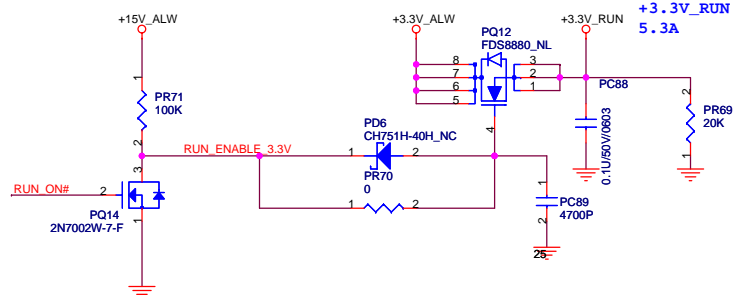
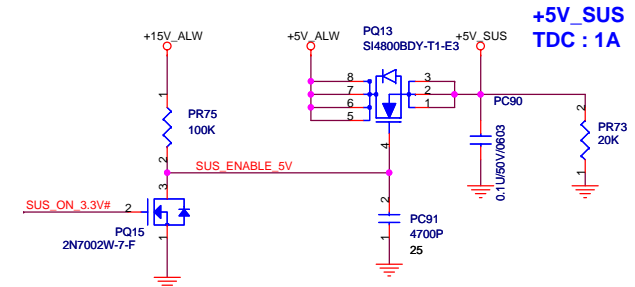
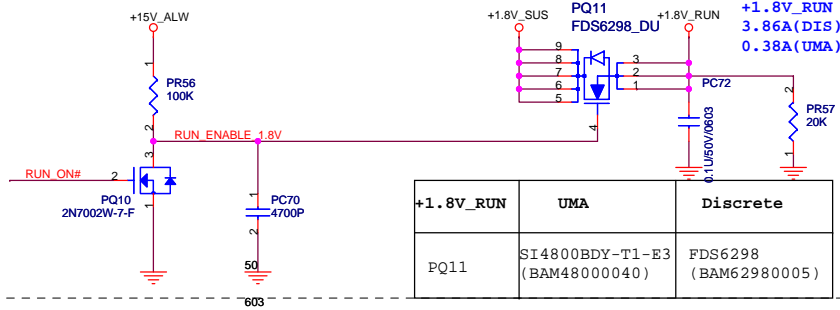
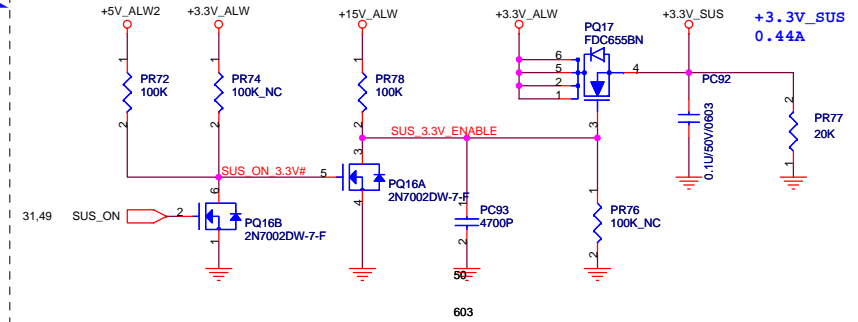
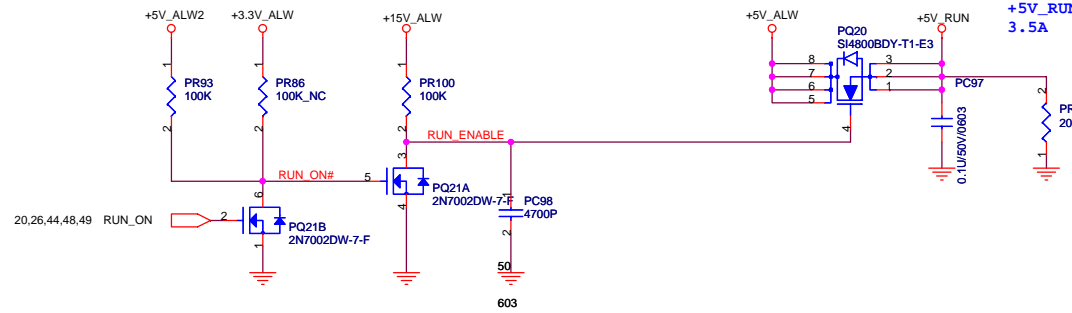
+1.8V\_SUS(UMA)  
TDC : 10.25A  
OCP : 14.9A  
Iout\_ripple current : 4.868A



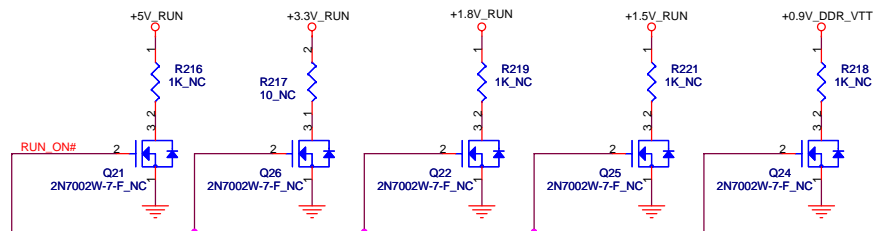




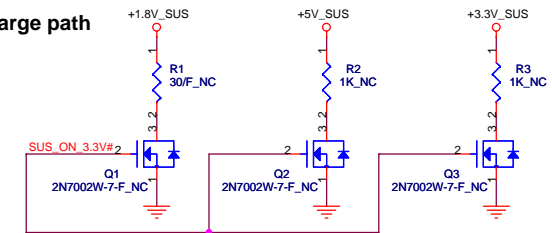


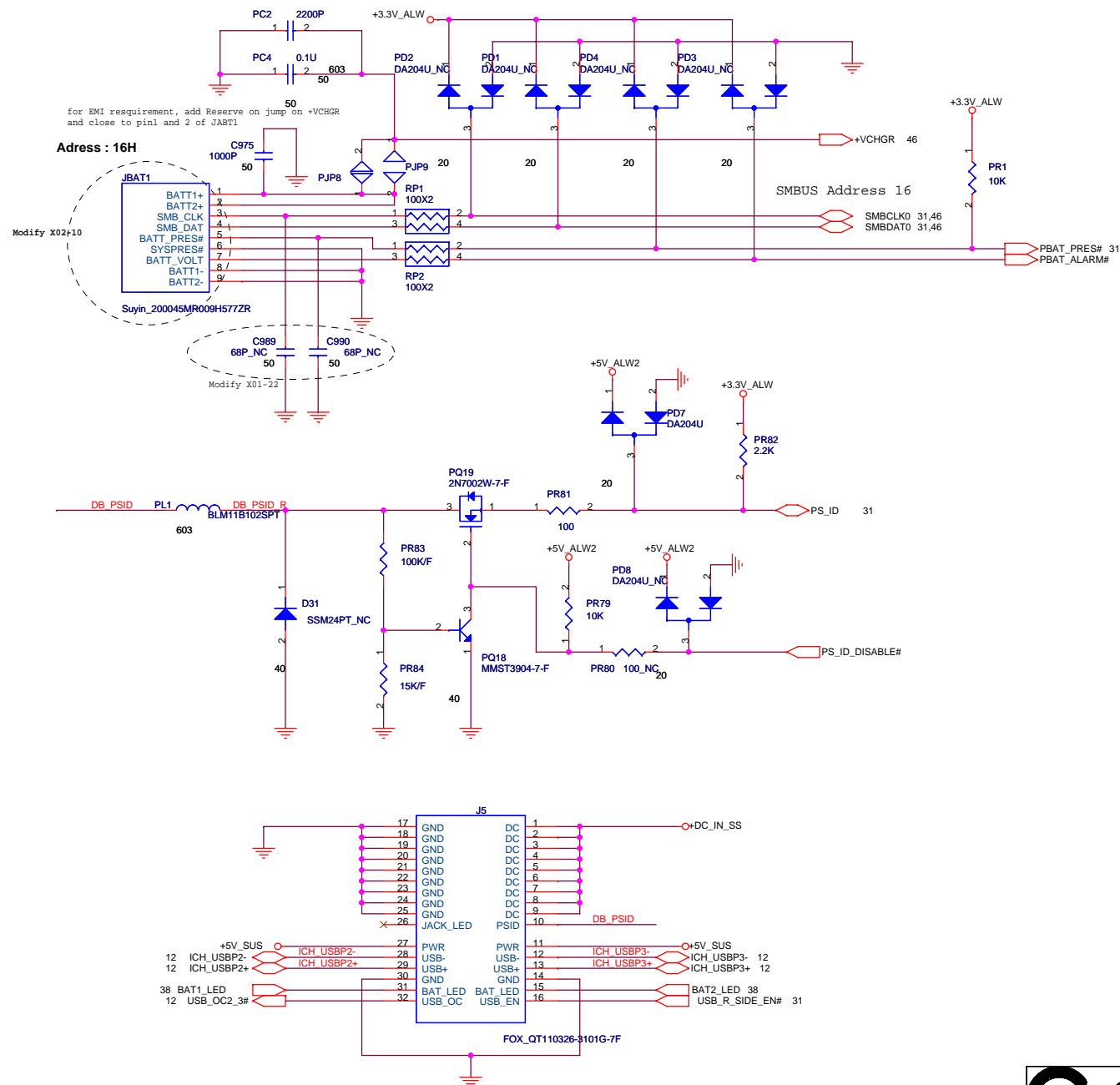


### Reserve discharge path



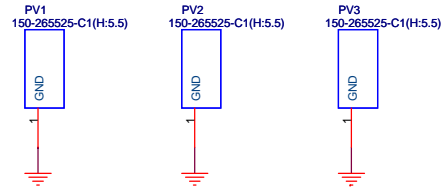
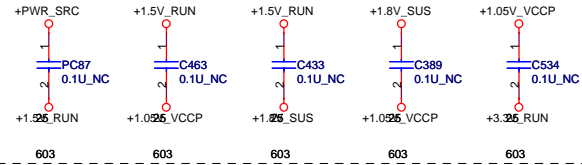
### Reserve discharge path





Reserved for EMI.

Stitching caps



Page 26  
SATA (HDD&CD\_ROM)

Page 27  
PCCARD /CONN

Page 31  
SIO(MEC5025)

Page 38  
Azelia CODEC

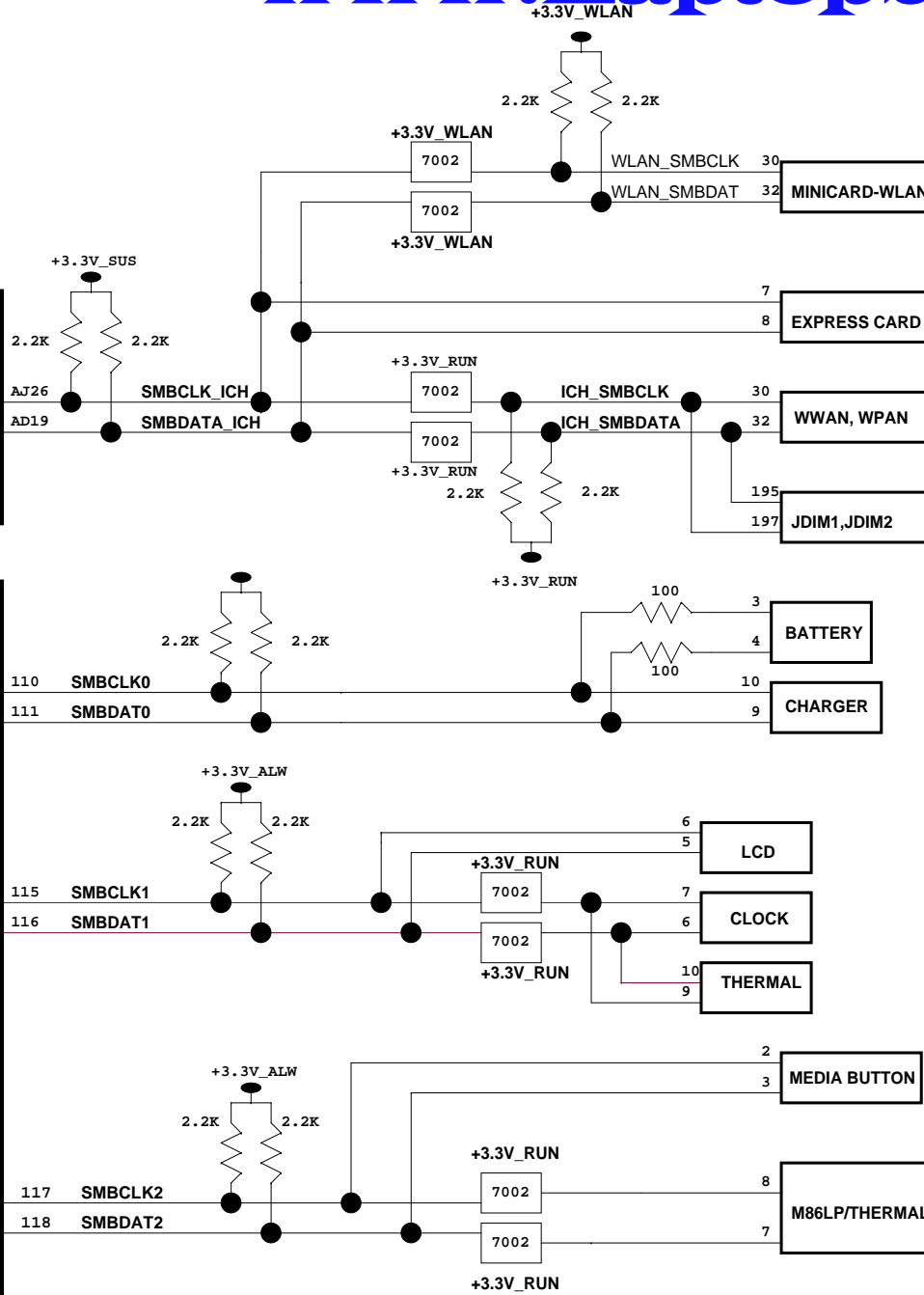
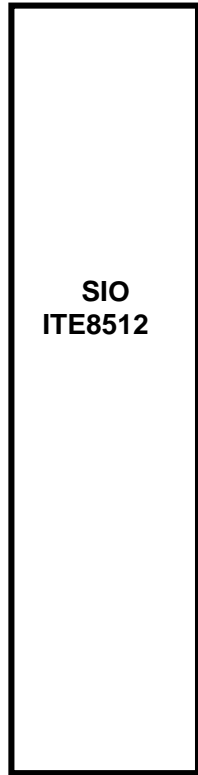
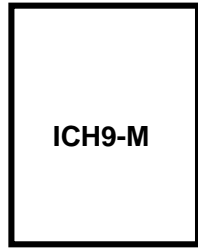
Page 40  
LAN(BCM5755M)

Page 48  
1.5VRUN,1.05V(VTT)

Page 49  
1.25V,1.8V,0.9V

Page 51  
CPU\_MAX8786(3phase)

Page 52  
D/D Power



## POWER STATES

| State \ Signal               | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | ALWAYS PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|---------|---------|---------|-----------|--------------|-----------|-----------|--------|
| S0 (Full ON) / M0            | HIGH    | HIGH    | HIGH    |           |              |           |           |        |
| S3 (Suspend to RAM) / M1     | LOW     | HIGH    | HIGH    |           |              |           |           |        |
| S4 (Suspend to DISK) / M1    | LOW     | HIGH    | HIGH    |           |              |           |           |        |
| S5 (SOFT OFF) / M1           | LOW     | HIGH    | LOW     |           |              |           |           |        |
| S3 (Suspend to RAM) / M-OFF  | LOW     | HIGH    | HIGH    |           |              |           |           |        |
| S4 (Suspend to DISK) / M-OFF | LOW     | LOW     | HIGH    |           |              |           |           |        |
| S5 (SOFT OFF) / M-OFF        | LOW     | LOW     | LOW     |           |              |           |           |        |

## PM TABLE

| State \ power plane  | +3.3V_ALW<br>+3.3V_RTC_LDO<br>+3.3V_WLAN<br>+5V_ALW<br>+15V_ALW | +1.8V_SUS<br>+1.8V_LOM<br>+3.3V_LAN<br>+3.3V_SUS<br>+5V_SUS | +0.9V_DDR_VTT<br>+1.05V_VCCP<br>+1.25V_RUN<br>+1.5V_CARD<br>+1.5V_RUN<br>+3.3V_CARD<br>+3.3V_CARDAUX<br>+3.3V_R5C832<br>+3.3V_RUN | +3.3V_RUN_CARD<br>+2.5V_RUN<br>+5V_MOD<br>+5V_RUN<br>+5V_SPK_AMP<br>+CPU_PWR_SRC<br>+VCC_CORE<br>+VDDA | +DC_IN<br>+DC_IN_SS<br>+PWR_SRC<br>+RTC_CELL |
|----------------------|---|---|---|--|--|
| S0                   | ON  | ON  | ON  | ON   | ON   |
| S3                   | ON  | ON  | OFF   | OFF  | ON   |
| S5 S4/AC             | ON  | OFF   | OFF   | OFF  | ON   |
| S5 S4/AC don't exist | OFF   | OFF   | OFF   | OFF  | ON   |

## PCI TABLE

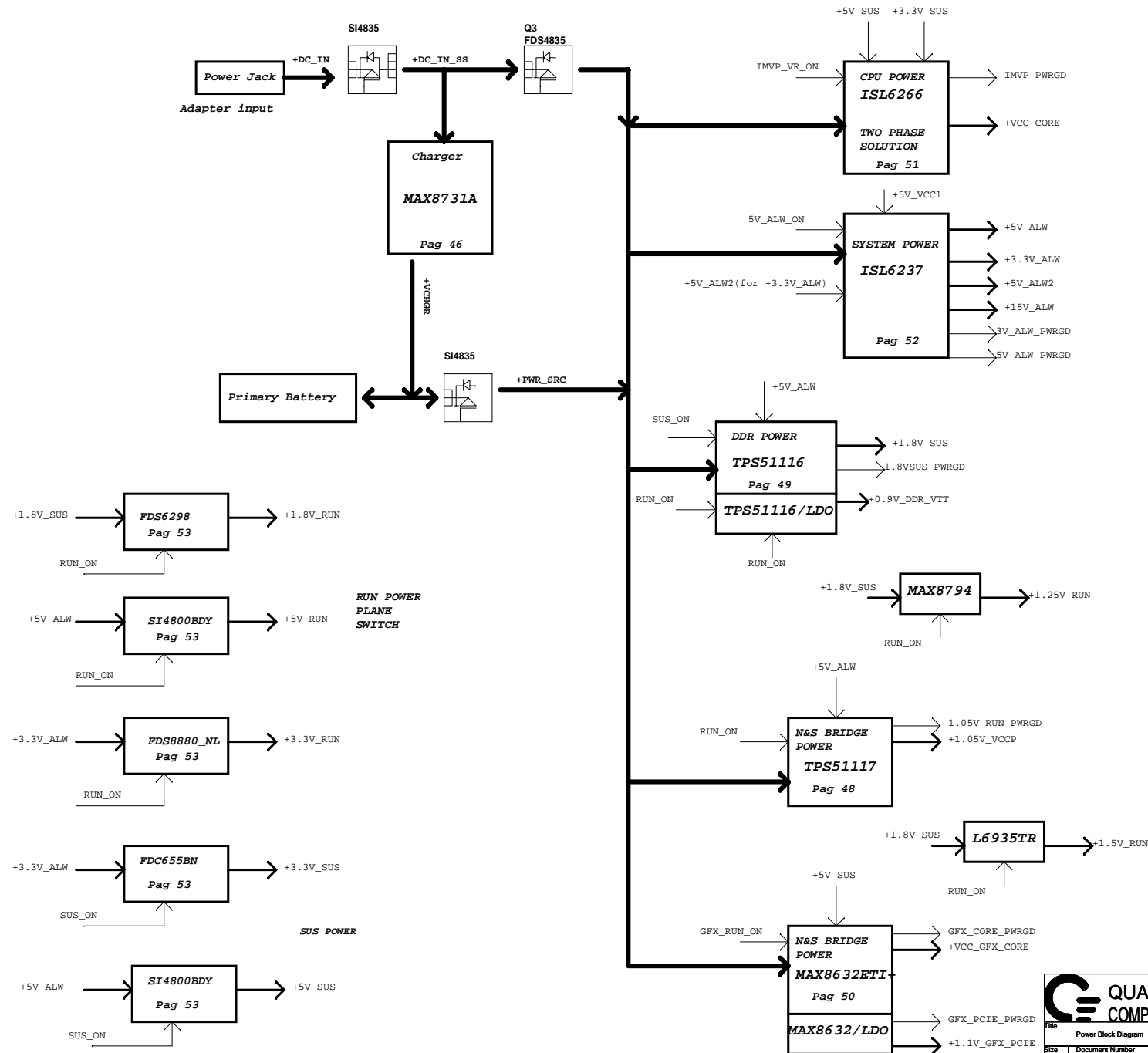
| PCI DEVICE | IDSEL | REQ#/GNT#     | PIRQ                              |
|------------|-------|---------------|-----------------------------------|
| R5C833     | AD17  | REQ#0 / GNT#0 | PIRQB: 1394<br>PIEQD: Card reader |
|            |       |               |                                   |

| ICH9-M   | USB PORT# | DESTINATION             |
|----------|-----------|-------------------------|
|          | 0         | Side pair Top / left    |
|          | 1         | Side pair bottom / left |
|          | 2         | Side pair top/right(DB) |
|          | 3         | Side pair Bot right(DB) |
|          | 4         | WLAN                    |
|          | 5         | Mini Card (WWAN)        |
|          | 6         | Mini Card (WPAN)        |
|          | 7         | Express Card            |
|          | 8         | USB W/ E-SATA port      |
|          | 9         | Reserved                |
| ECE 5011 | 10        | Biometric               |
|          | 11        | Camera                  |
|          | 1         | None                    |
|          | 2         | None                    |
|          | 3         | None                    |
|          | 4         | None                    |

| PCI EXPRESS | DESTINATION      |
|-------------|------------------|
| Lane 1      | MINI CARD-1 WWAN |
| Lane 2      | MINI CARD-2 WLAN |
| Lane 3      | MINI CARD-3 WPAN |
| Lane 4      | Express Card     |
| Lane 5      | None             |
| Lane 6      | None             |

# GM3 Power Design Block Diagram

2007/09/06

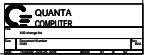


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| Model                    | Item | Page            | Date         | Rev. | Description   |
|--------------------------|------|-----------------|--------------|------|---|
| Pacino<br>M7<br>of Intel | 1    | 25              | 6/6<br>2008  |      | Change L54, L56, L70, L72 to CXCG90U000.  |
|                          | 2    | 43              | 6/6<br>2008  |      | Change L80 to DB9FXLAN01.   |
|                          | 3    | 09              | 6/6<br>2008  |      | Change D28 to BC01GKA5004.  |
|                          | 4    | 46              | 6/6<br>2008  |      | Change PQ4, PQ24 to BAMA48350001.   |
|                          | 5    | 53              | 6/6<br>2008  |      | Change PQ17 to BAMA4660102.   |
|                          | 6    | 25              | 6/11<br>2008 |      | Reserve R9999, R10000, R10001, R10002, C4945, C4946, C4947, C4948 for EMI solution.   |
|                          | 7    | 6               | 6/11<br>2008 |      | Change R187, R213 pull high to +3.3V_RUN to solve backdrive in S3.  |
|                          | 8    | 14              | 6/11<br>2008 |      | Change C957 from CH2220KMJ1 to CH71001MB82  |
|                          | 9    | 48              | 6/11<br>2008 |      | Change PC169 from CH733KM826 to CH722KM7B00   |
|                          | 10   | 54              | 6/11<br>2008 |      | Change JBA71 from DFHD09MR013 to DFHD09MR019  |
|                          | 11   | 11-14           | 6/11<br>2008 |      | Change U48 from AJQP220T05 to AJQ2T100T01   |
|                          | 12   | 35              | 6/11<br>2008 |      | Change JUSB1 from DFHD04FR126 to DFH511FR016  |
|                          | 13   | 4,8,9           | 6/11<br>2008 |      | Change C96, C188, C243, C438 to CH71001MB82   |
|                          | 14   | 40              | 6/11<br>2008 |      | Change J3 from DFHD04MR040 to DFVWF04FR001  |
|                          | 15   | 38              | 6/11<br>2008 |      | Change SW1 from DHLLS12P03 to DHLLS12P01  |
|                          | 16   | 35              | 6/11<br>2008 |      | Change L17, L20, L50 from CXSGQ2T1001 to DC0900A014   |
|                          | 17   | 50              | 6/11<br>2008 |      | Change PQ1 from BAMA00350000 to BAMA48350024  |
|                          | 18   | 51,48,<br>46,49 | 6/11<br>2008 |      | NC PC131, PC129, PC197, PC94 depended on internal notice.   |
|                          | 19   | 25              | 6/11<br>2008 |      | Change U13 to UMA part.   |
|                          | 20   |                 | 6/11<br>2008 |      | Delete reserved 0-ohm resistors: R192, R139, R226, R144, R145, R181, R248, R197, R198, R198, R188, R173, R195, R177, R209, R174, R196, R178, R215, R201, R176, R200, R179, R202, R175, R199, R180, R153, R152, R154, R140, R105, R228, R857, R717, R716, R241, R220, R206, R209, R210, R212, R245, R546, R847, R140, R848, R730, R842, R815, R871, R778, R769, R718, R664, R847, R865, R663, R705, R701, R700, R694, R106, R142, R77, R81, R75, R162, R195, R804, R767, R768, R683, R437, R547, R576, R575, R578, R428, R424, R422, R420, R423, R646, RPR14, PR4, PR6, PR97 |
|                          | 21   | 42              | 6/12<br>2008 |      | Change R325 to 39K-ohm and R311 to 20K-ohm for LAN chip, BCM5794M.  |
|                          | 22   | 48              | 6/12<br>2008 |      | Change PQ32 & PQ33 subsystem ID to PWR.Plane.Regulator_1p05v1p0v.   |
|                          | 23   | 46, 48          | 6/12<br>2008 |      | Change PL3 to CV-5855T204 & PL7 to DC-15A00002.   |
|                          | 24   | 48              | 6/12<br>2008 |      | Populate PC187 by power's request.  |
|                          | 25   | 14              | 6/12<br>2008 |      | Change U53 to DELL PSL LDO part and schematic.  |
|                          | 26   | 40              | 6/13<br>2009 |      | Change Audio codec U91 to revision C1, AL79C1X0803 for ST built.  |
|                          | 27   | 25              | 6/13<br>2009 |      | For HDMI pre-amp item, DCCCEFC Capacitance, add low-Capacitance MOSs on SMBUS between HDMI connector and PIVDPH11LS2DE.   |
|                          | 28   |                 | 6/13<br>2009 |      | Change C96, C98, C987, C438, C188, C243, C435, C595, C353, C957 to 220uF CAP2.0; CH722AM816.  |
|                          | 29   | 28              | 6/13<br>2009 |      | Depopulate R819, because R5C833 don't need PME#.  |
|                          | 30   | 31              | 6/13<br>2009 |      | Change the B0D to ST stage.   |
|                          | 31   |                 | 6/13<br>2009 |      | Change L87, L86, L91, L20, L17, L50, L46 to CXCG90U000.   |
|                          | 32   | 38              | 6/13<br>2009 |      | Change SW1 to DHLLS12P03  |
|                          | 33   | 41, 52          | 6/13<br>2009 |      | Delete reserved 0-ohm resistors R826 and PR92.  |
|                          | 34   | 52              | 6/13<br>2009 |      | Reserve a CAP PC200 for girth reducing of TEMP_FAIL.  |
|                          | 35   | 33              | 6/17<br>2009 |      | Change C655 to 100uF CAP, CH7101MB800.  |
|                          | 36   | 19, 52          | 6/18<br>2010 |      | DELL's request on thermal detect pin  |
|                          | 37   | 50              | 6/19<br>2010 |      | Change PR119 to CS32433P915(0603), PR116 to CS38662F90A(0603), PR118 to CS48372F90B(0402), R120 to CS16805F910(0603), PR185 to CS41152F90B(0402), PR188 to CS20022F901(0402) to meet GPU core voltage step: 0.9V, 0.95V and 1.1V.   |
|                          | 38   | 3,4             | 6/23<br>2009 |      | Change CPU socket(L42) PIN to DGT*6000001(Foxconn)  |
|                          | 39   | 3               | 6/23<br>2009 |      | NC R116 for H_RESET# glitch.  |
|                          | 40   | 25              | 6/24<br>2009 |      | Fine-tune the emphasis and the equalization of HDMI.<br>1. Pull OC1, OC2 to high and Pull OC1, OC3 to low.<br>2. Pull EQ1 to low and pull EQ2 to high.  |
|                          | 41   | 15              | 6/24<br>2009 |      | Change JDM1 to Hx5.6mm connector, DGMK0000015 and JDM2 to H=10.1mm connector, DGMK0000016.  |
|                          | 42   | 31              | 6/26<br>2009 |      | NC R601, R704 and populate R593 for activating platform reset signal.   |

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***Pacino  
MV  
of Intel***



|       |                 |
|-------|-----------------|
| Title | A00 change list |
|-------|-----------------|

|      |                        |
|------|------------------------|
| Size | Document Number<br>GM3 |
|------|------------------------|

|     |  |
|-----|--|
| Rev |  |
| B2A |  |

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