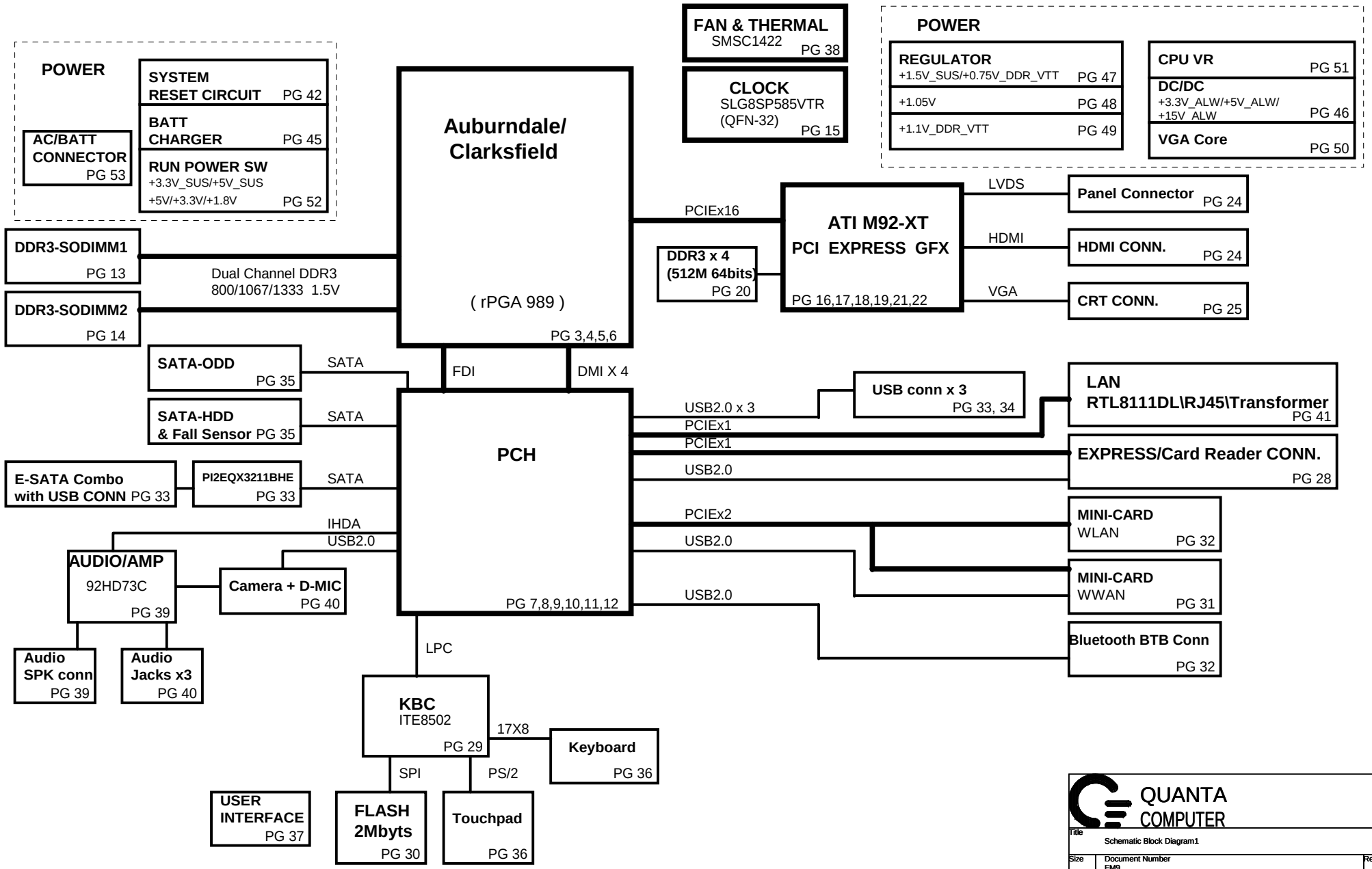
FM9 XXXX Intel Discrete GFX

VER : 1A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power State

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44 ,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
GND_CHG	46	
GND_1.05V	47	
GND_VGA	50	
GND_SIGNAL	51	
AGND_DC/DC	52	
GND	ALL	

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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Ω ±1% resistor, pulled-down to GND on the board.

U3031A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

Clarksfield/Auburndale

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3

DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3] DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]

DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3] DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

FDI_TX#[0] FDI_TX#[1] FDI_TX#[2] FDI_TX#[3] FDI_TX#[4] FDI_TX#[5] FDI_TX#[6] FDI_TX#[7]

FDI_TX[0] FDI_TX[1] FDI_TX[2] FDI_TX[3] FDI_TX[4] FDI_TX[5] FDI_TX[6] FDI_TX[7]

FDI_FSYNC[0] FDI_FSYNC[1] FDI_INT FDI_LSYNC[0] FDI_LSYNC[1]

R762 1K 0214

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor.

PEG_ICOMPI R742 49.9/F

PEG_ICOMPO PEG_RCOMPO PEG_RBIAS R744 750/F

PCIE_MRX_GTX_N[0..15] 16

PCIE_MRX_GTX_P[0..15] 16

PEG_RX#[0..15] PEG_RX[0..15]

PEG_TX#[0..15] PEG_TX[0..15]

SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

VTTPWRGOOD SC(V1.0)P18: VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.

1 +1.5V_SUS R778 4.75K/F R779 12K/F PM_DRAM_PWRGD

RSTIN#: DG(V1.11)(Doc.# 414044),P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)

R776 1.5K/F R777 750/F 0214

SM_DRAMPWROK: DG(V1.0) P311&SC(V1.0) P18:recommend 4.75-kΩ pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12-kΩ pull-down to ground to convert to processor's VTT level. CRB(V1.0) P11:CRB uses a 3.3V (always ON) rail with 2K and 1K combination. CRB Implementation is different for the Calpella Platform Design Guide. Customers to follow the latest Calpella Platform Design Guide for DRAMPWROK Implementation.

SC(V1.0),P17: SKTOCC# Can be left No Connect or tied to GND

U3031B

MISC THERMAL DDR3 MISC PWR MANAGEMENT CLOCKS JTAG & BPM

H_COMP3 H_COMP2 H_COMP1 H_COMP0 T182 TP_SKTOCC# H_CATERR# R751 0 H_PECI H_PECI_ISO H_PROCHOT#_D R755 0 H_THERM H_CPURST# PM_SYNC H_PWRGOOD PM_DRAM_PWRGD H_VTTPWRGD H_PWRGD_XDP PLTRST#

COMP3 COMP2 COMP1 COMP0 SKTOCC# CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGOOD RSTIN#

Clarksfield/Auburndale

BCLK BCLK# BCLK_ITP BCLK_ITP# PEG_CLK PEG_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#

CLK_CPU_BCLK CLK_CPU_BCLK# BCLK_ITP BCLK_ITP# CLK_PCIE_3GPLL CLK_PCIE_3GPLL#

DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Auburndale directly if motherboard only supports discrete graphics.

SM_DRAMRST# SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] PM_EXT_TS#[0] PM_EXT_TS#[1]

DDR3_DRAMRST# SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2

+1.1V_VTT R752 10K/F R753 10K/F R754 0 R756 0 PM_EXTTS#0 PM_EXTTS#1

CRB(v0.71) P.11 R1065 *12.4K/F_NC

PRDY# PREQ# TCK TMS TRST# TDI TDO TDI_M TDO_M DBR#

XDP_PRDY# XDP_PREQ# XDP_TCLK XDP_TMS XDP_TRST# T186 T168 T169 XDP_TDI_R XDP_TDO_R XDP_TDI_M XDP_TDO_M

DBR#: SC(V1.0) P22:Connected to the DBR# pin of the Processor.50-Ω to 5-kΩ pull-up to 3.3VS CRB(V1.0) P11,P71:CRB uses a 1-kΩ pull-up to 3.3VS. On the CRB this signal is ANDed with Master Reset to generate SYS_RESET.

DBR#:(Intell feedback) Nothing wrong w/ CRB design. If you want to connect it to PCH directly, make sure pull high to 3.3V (S0) main power.

2 XDP_DBRESET# 7,60 XDP_OBS[0:7] 60

BPM#[0] BPM#[1] BPM#[2] BPM#[3] BPM#[4] BPM#[5] BPM#[6] BPM#[7]

XDP_OBS0_R XDP_OBS1_R XDP_OBS2_R XDP_OBS3_R XDP_OBS4_R XDP_OBS5_R XDP_OBS6_R XDP_OBS7_R

R758 R760 R761 R763 R764 R766 R767 R769 0 XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7

+3.3V_RUN R28 10M Q6 2N7002W-7-F H_THERM Q7 MMST3904-7-F C24 0.1U 10 PM_THRMTRIP# 46

PCIE_MTX_GRX_C_N[0..15] PCIE_MTX_GRX_N[0..15] 16

PCIE_MTX_GRX_C_P[0..15] PCIE_MTX_GRX_P[0..15] 16

C1175 C1177 C1179 C1181 C1183 C1185 C1187 C1189 C1191 C1193 C1195 C1197 C1199 C1201 C1203 C1205 C1176 C1178 C1180 C1182 C1184 C1186 C1188 C1190 C1192 C1194 C1196 C1198 C1200 C1202 C1204 C1206 10 0.1U

SM_DRAMPWROK:(Intell Feedback) Either way works.

T188 T187 XDP_TMS XDP_TDI_R XDP_TCK +1.1V_VTT R787 R788 R789 R790 *51_NC

CRB(V1.0) P11: is it necessary

JTAG MAPPING

XDP_TDI_R XDP_TDO_M XDP_TDI_M XDP_TDO_R R780 R781 R783 R785 R786 0 0_NC XDP_TDI XDP_TDO XDP_TRST# R784 51

Scan Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

DG(v1.0) table 27

TRSI# SC(V1.0)P22: should be routed as a single daisy chain to all loads and terminated at the end of the trace. 51 Ω ± 5% pull down resistor. CRB()V1.0)P11

Processor Pullups

+1.1V_VTT R793 49.9/F R794 49.9/F R795 *68_NC H_CATERR# H_PROCHOT# D H_CPURST#

SC(1.0V),P17: H_PROCHOT#D use: pull to 68 ohm if it isn'tt used: pull to 50 ohm

SC(1.0V),P17: H_CATERR# 49.9-Ω ±1% Pull-Up to the VTT rail (+V1.1S_VTT)

Processor Compensation Signals

H_COMP0 H_COMP1 H_COMP2 H_COMP3 R796 49.9/F R797 49.9/F R798 20/F R799 20/F

DG(V1.0),P17: COMP[0.1] 49.9-Ω ±1% pull-down to GND COMP[2.3] 20-Ω ±1% pull-down to GND

DDR3 Compensation Signals

SM_RCOMP_2 SM_RCOMP_1 SM_RCOMP_0 R800 130/F R801 24.9/F R802 100/F

Layout Note: Place these resistors near Processor

DG(V1.0),P83: SM_RCOMP[0] 100-Ω ±1% pull-down to GND SM_RCOMP[1] 24.9-Ω ±1% pull-down to GND SM_RCOMP[2] 130-Ω ±1% pull-down to GND

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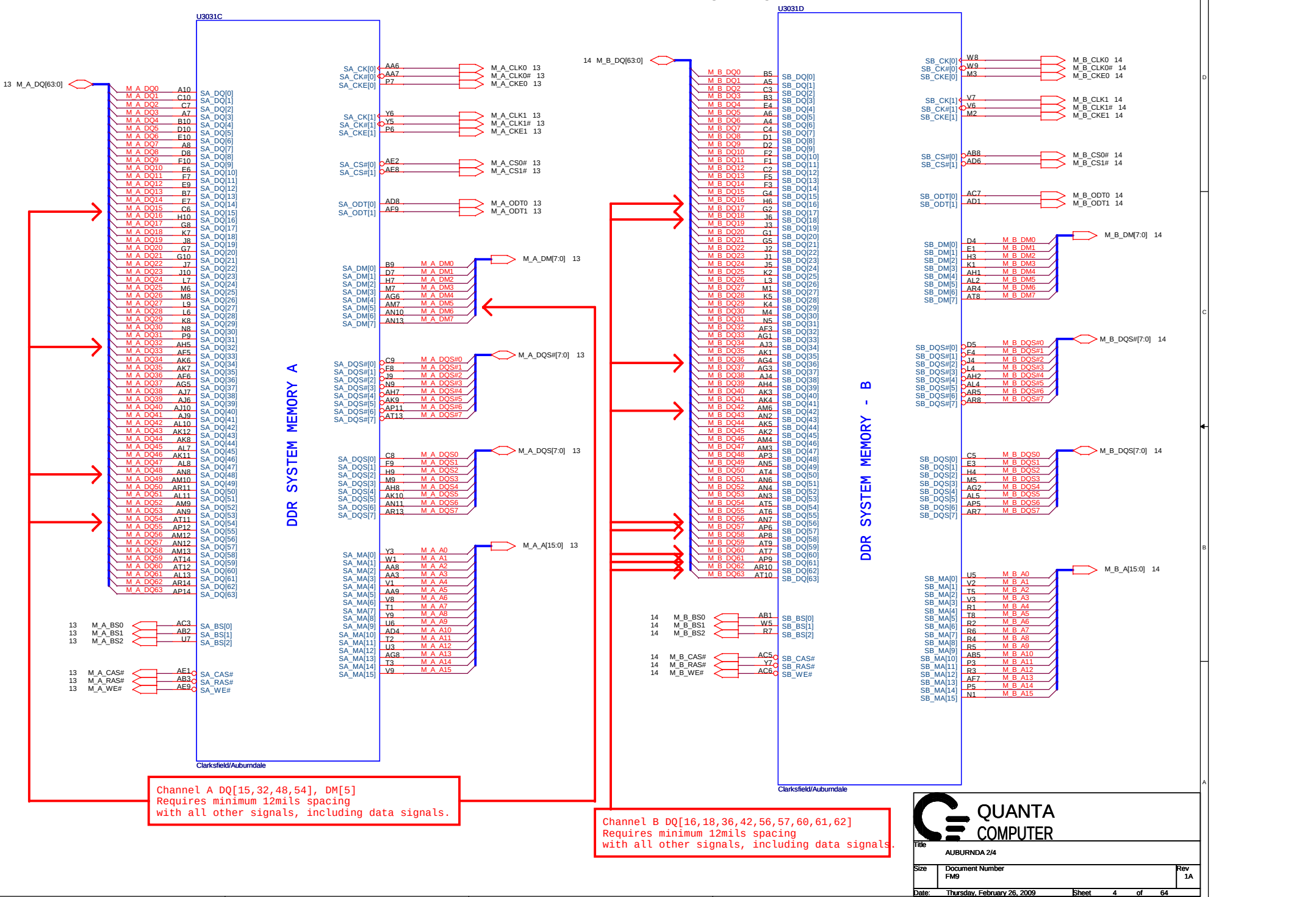
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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CPU Core Power

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

U3031F

+VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

C1207 10U C1208 10U C1209 10U C1210 10U C1211 10U C1212 10U C1213 10U C1214 *10U_NC C1215 *10U_NC

+1.1V_VTT

C1217 22U C1222 22U C1223 22U

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 +VTT_43 J15 +VTT_44

C1234 22U C1235 22U

3

VTT0_43,VTT0_44:
CRB(V1.0)P13
Why add 0ohm?? Is it trace width control??

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

C1237 22U C1238 22U

C1269 22U C1270 22U C1273 22U C1274 22U

U3031G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

GRAPHICS

VTT1_45 VTT1_46 VTT1_47

J24 J23 H25

PCI

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 F25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

PEG & DMI

POWER

Clarksfield/Auburndale

SENSE LINES

VAXG_SENSE VSSAXG_SENSE

AR22 AT22

GRAPHICS VIDS

GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6]

AM22 AP22 AN22 AP23 AM23 AP24 AN24

GFX_VR_EN GFX_DPRSLPVR GFX_IMON

AR25 AT25 AM24

R803 *1K/F_NC

4

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:
Could this be left unconnected when not in use?

GFX_VID[0..6],GFX_VR_EN,GFX_DPRSLPVR,GFX_IMON:(Intel feedback)
Yes, see DG rev1.5

DDR3 - 1.5V RAILS

+1.5V_SUS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

C1216 1U C1218 1U C1219 1U C1220 1U C1221 1U

+C1224 330U 7343 2.5

C1225 22U C1226 22U

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62

P10 N10 L10 K10

C1247 10U C1248 10U

+C1258 *330U_NC 7343 2.5

+1.1V_VTT

VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

J22 J20 J18 H21 H20 H19

C1271 22U C1272 22U

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C1275 1U C1276 1U C1277 2.2U C1278 4.7U C1279 22U

+VCC_CORE

C1227 22U C1228 22U C1229 22U C1230 22U C1231 22U C1232 22U

C1239 22U C1240 22U C1241 22U C1242 22U C1243 22U C1244 22U

C1249 10U C1250 10U C1251 10U C1252 10U C1253 10U C1254 10U C1255 10U C1256 10U

C1261 10U C1262 10U C1263 10U C1264 10U C1265 10U C1266 10U C1267 10U C1268 10U

+C1507 *470U_NC +C1508 *470U_NC

POWER

CPU VIDS

PSI# AN33 H_PSI# 51

VID[0] AK35 VID0 VID0 51
VID[1] AK33 VID1 VID1 51
VID[2] AK34 VID2 VID2 51
VID[3] AL35 VID3 VID3 51
VID[4] AL33 VID4 VID4 51
VID[5] AM33 VID5 VID5 51
VID[6] AM35 VID6 VID6 51
PROC_DPRSLPVR AM34 DPRSLPVR DPRSLPVR 51

VTT_SELECT G15 H_VTTVID1 49

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

SENSE LINES

ISENSE AN35 I_MON 51

VCC_SENSE AJ34 VCCSENSE 51
VSS_SENSE AJ35 VSSSENSE 51

VTT_SENSE B15 VTT_SENSE 49
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT T196

+VCC_CORE

R807 100/F

R819 100/F

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

+1.1V_VTT

R810 1K R811 1K R812 1K R813 *1K_NC R814 *1K_NC R815 1K R816 *1K_NC R817 1K R818 *1K_NC

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR H_PSI#

R820 *1K_NC R821 *1K_NC R822 *1K_NC R823 1K R824 1K R825 *1K_NC R826 1K R827 *1K_NC R828 1K

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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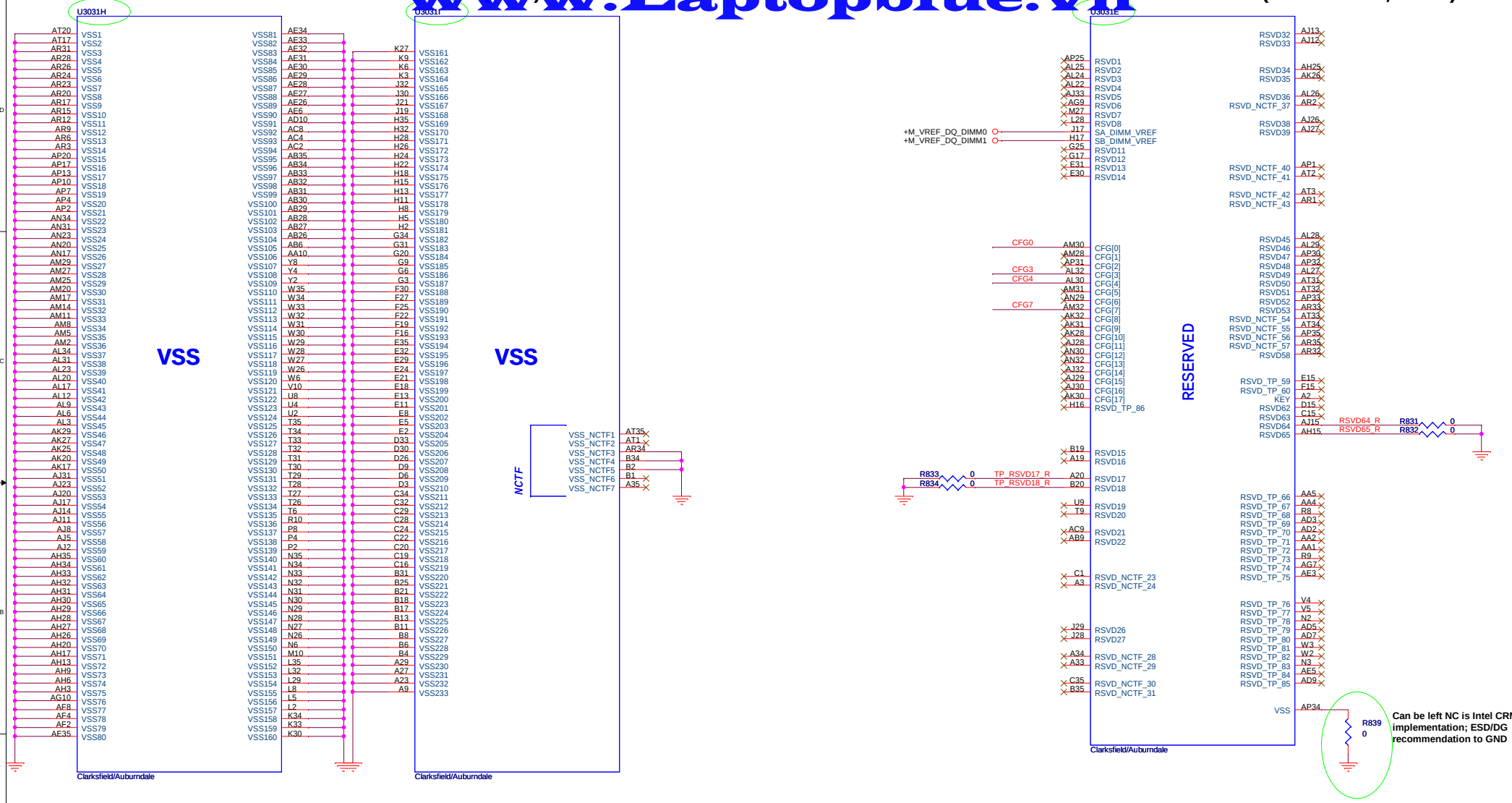
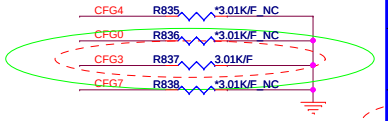
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



PCIE LANE is Lane Numbers Reversed

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

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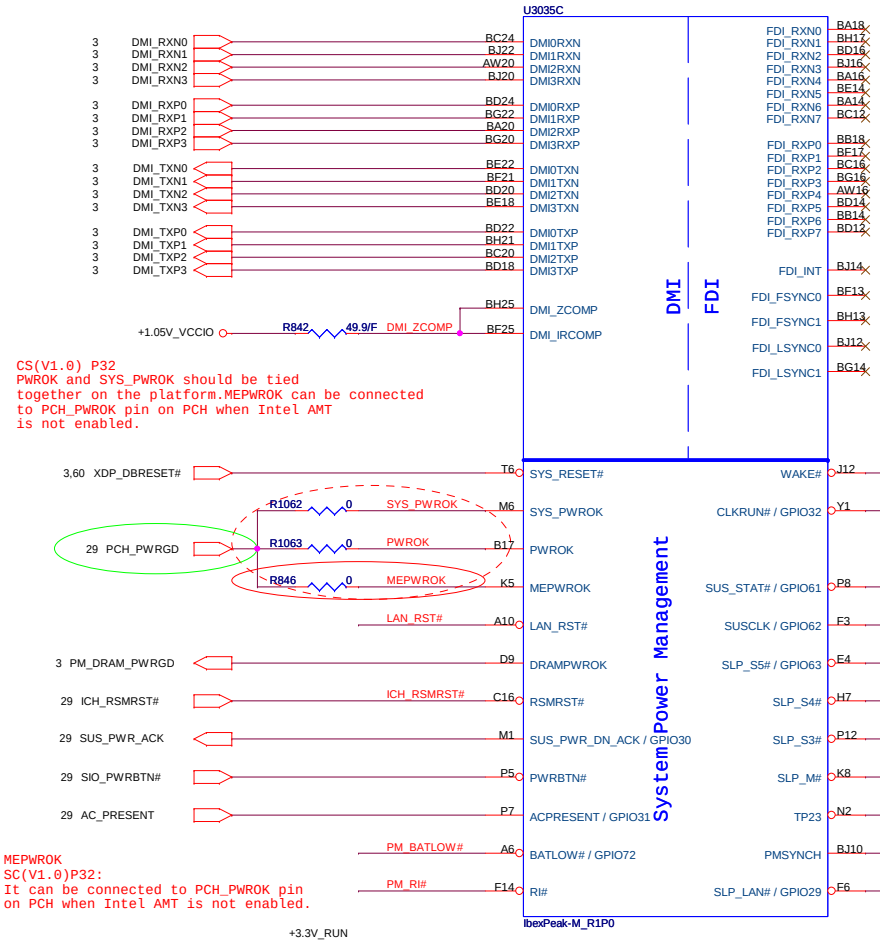
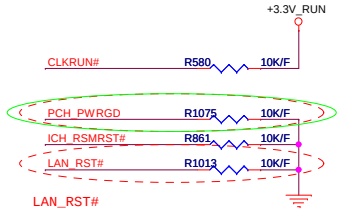
IBEX PEAK-M (DMI,FDI,GPIO)



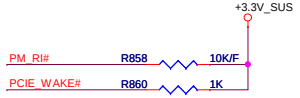
DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83:FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform.MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

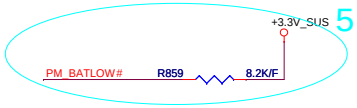
MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



LAN_RST#
DG(V1.0) P311
If integrated LAN is not used, recommend to connect LAN_RST# to GND via an 8.2-kΩ to 10-kΩ pull-down resistor.
EDS(V1.0)P64
must be grounded if Intel LAN is disabled.



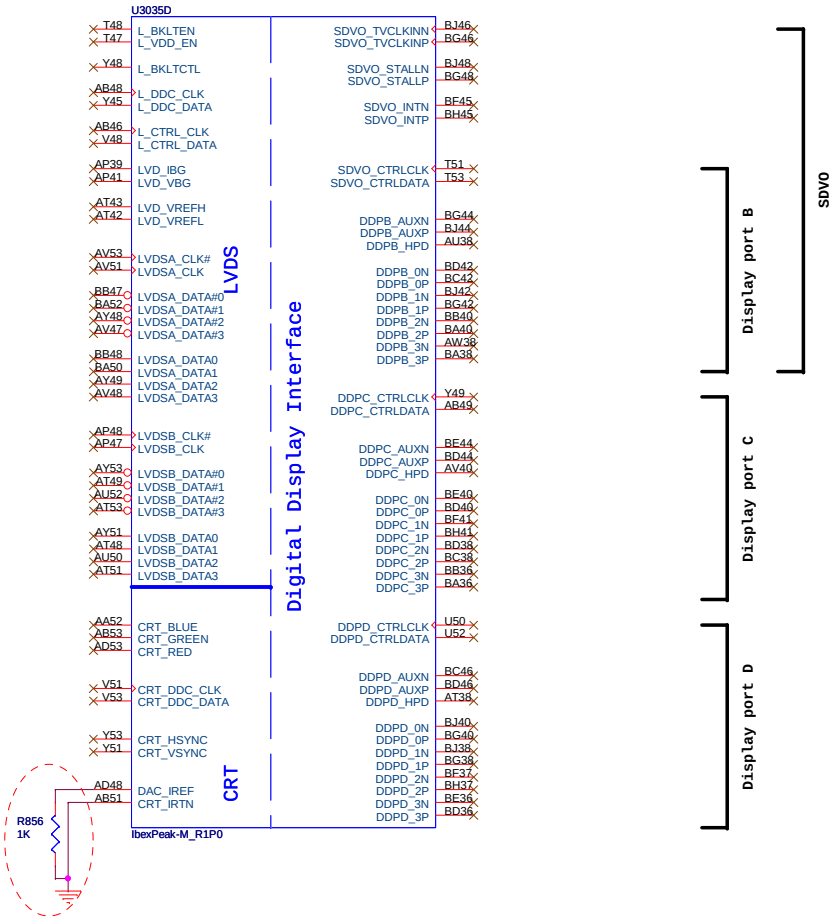
PWROK
SC(V1.0)P32:
8.2 kΩ to 10 kΩ pull-down resistor to GND.
PWROK and SYS_PWROK should be tied together on the platform.



PM_BATLOW#:
EDS(V1.0)P95: 15K~40K (+3.3V_SUS)
CRB(V1.0)P25: 8.2K (+3.3V_ALW)

PM_BATLOW#:(Intel feedback)
15K ~ 40K is a simulation result, the expected value should be 20K internal pull high in PCH.
8.2K is external pull high.

IBEX PEAK-M (LVDS,DDI)



DG(V1.0)P189:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k ±0.5% pull-down resistor

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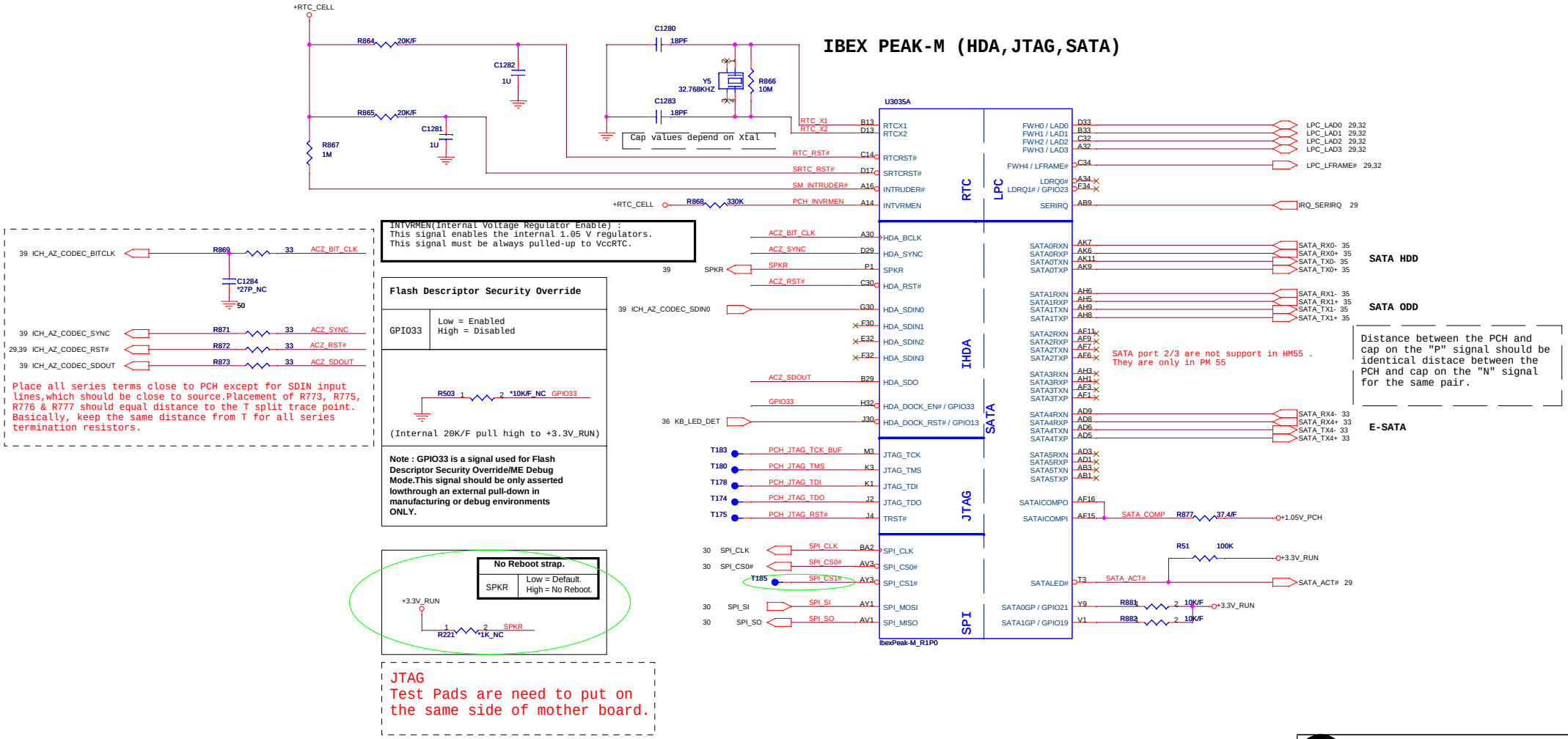
IBEX PEAK-M (HDA,JTAG,SATA)



Title	IBEX PEAK-M 1/6		
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QUANTA COMPUTER

IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

U3035E

PCI

NVRAM

USB

Left Side pair Top

Left Side pair bottom

Right Side pair top (Cable)

Mini Card (WLAN)

Mini Card (WWAN)

USB port 6/7 are not support in HM55
They are only in PM 55

Mini Card (WPAN)

Express Card

Camera

Touch Screen Module

Note : place these resistors near to PCIe Slots

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend (single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214
Pin Default Port Mapping
OC0# Port0,Port1
OC1# Port2,Port3

IbexPeak-M_R1P0

MiniWWAN

MiniWLAN

Express Card

Card Reader

Giga Bit LOM

PCI-E port 7/8 are not support in HM55 .
They are only in PM 55

U3035B

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IbexPeak-M_R1P0

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

CLKOUTFLEX3 :
EDS(V1.0) :support 48MHz 33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

U56

TC7SZ32FU(T5L,F,T)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

QUANTA COMPUTER

Title: IBEX PEAK-M 3/6

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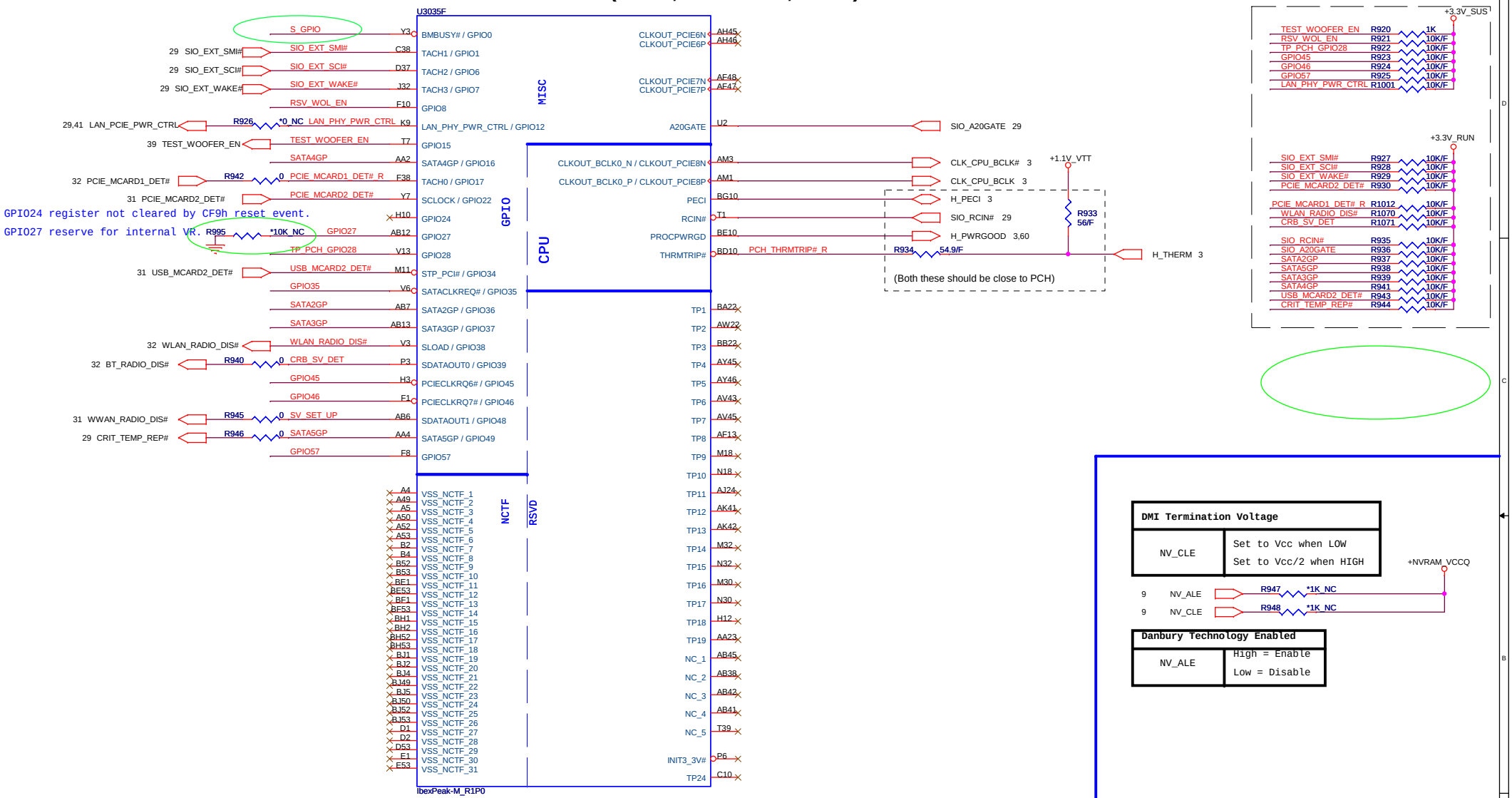
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+NVRAM_VCCQ

9 NV_ALE R947 *1K_NC

9 NV_CLE R948 *1K_NC

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

R1072 10K/F GPIO35

R950 *1K/F_NC GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

+3.3V_RUN

S_GPIO R530 10K/F

SV_SET_UP R951 10K/F

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

SV_SET_UP	1-X High = Strong (Default)

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QUANTA COMPUTER

Title	IBEX PEAK-M 4/6	
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IBEX PEAK-M (POWER)

VCCCORE=1.524A max

VCC CORE | CRT | LVDS | HVCMOS | DMI | PCI E* | SPI | NAND | FDI

VCCAPLLEXP = 100mA max

VCCAPLLEXP:
This pin can be left as no connect in
On-Die VR enabled mode (default).

VCCIO = 3.208A max

VCC3_3 = 0.357A max

VCCVRM = 0.035A max

VCCFDIPLL = 100mA max

VCCADPLLA = 0.072A max

VCCADPLLB = 0.073A max

VCCPNAND = 0.156A max

VCCME3_3 = 0.086A max

VCCME3_3:
EDS(V1.0)P84:supply for the Intel Management Engine.This is a separate power plane
that may or may not be powered in S3-S5 states.
This plane must be on in S0
and other times the Intel Management Engine is used.

PCH EDS(V1.0) P84
+NVRAM_VCCQ:
1.8 V supply for Dual Channel NAND interface.
This power is supplied by core
well. If unused, this pin should
be connected to Vcc3_3.

VCCACLK = 100mA max

VCCME = 1.998A max

VCCSUS3_3 = 0.163A max

V_CPU>1mA

VCCRTC = 2mA max

VCCSUSHDA = 6mA max

U3035J

POWER

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

ibexPeak-M_R1P0

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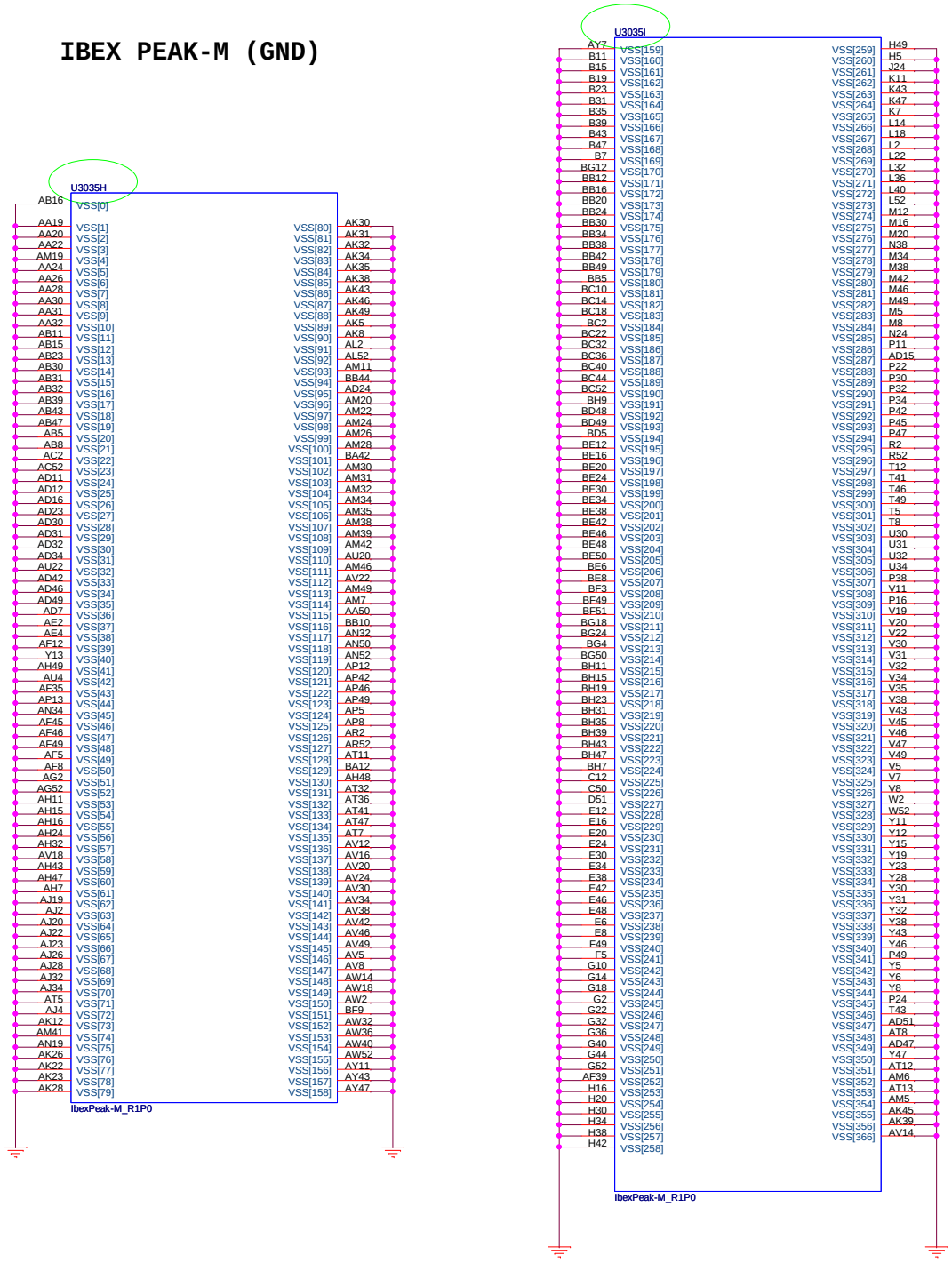
QUANTA COMPUTER

IBEX PEAK-M (GND)



QUANTA COMPUTER

Title	IBEX PEAK-M 6/6	
Size	Document Number FM9	Rev 1A
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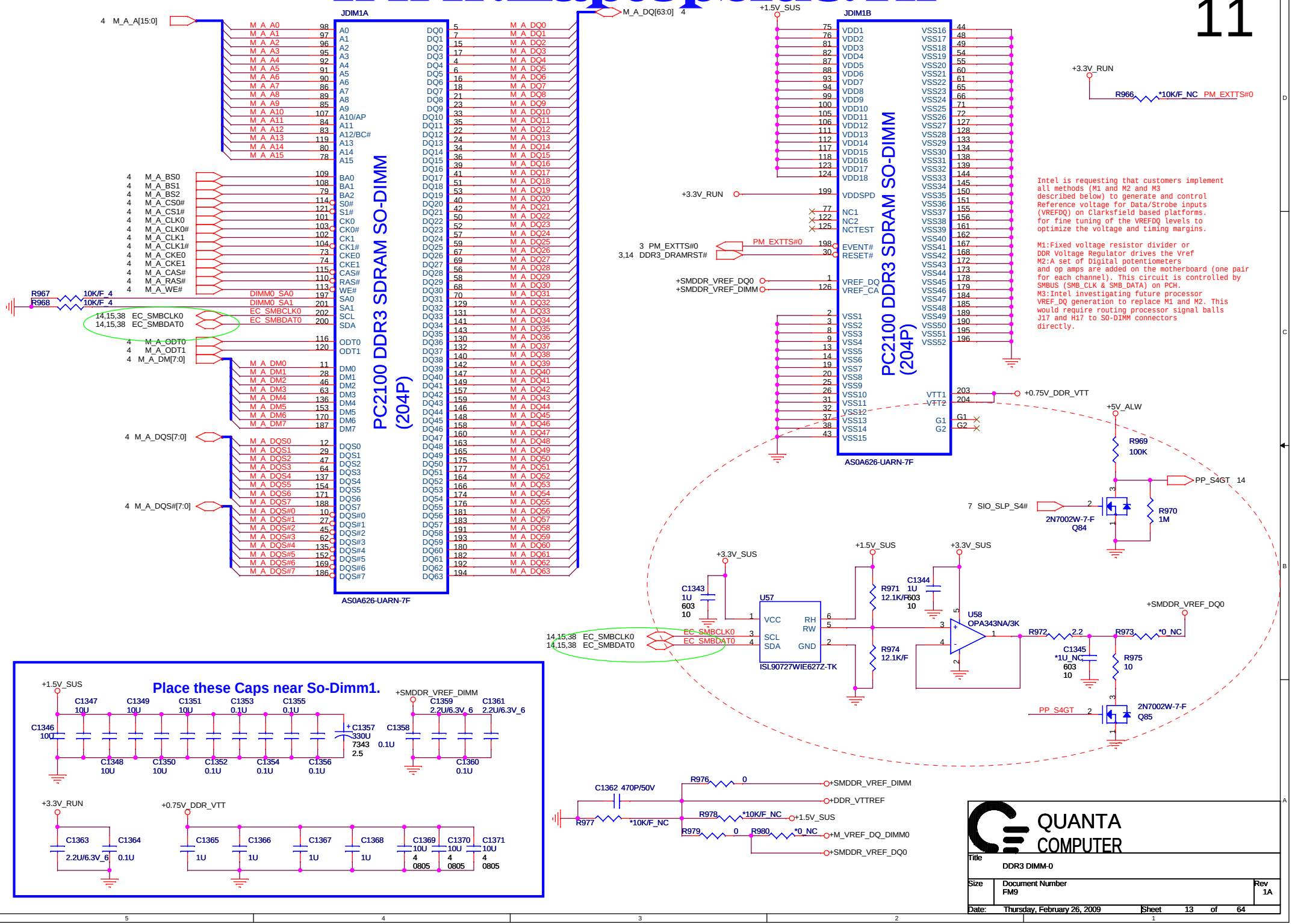

QUANTA COMPUTER

Title	DDR3 DIMM-0	
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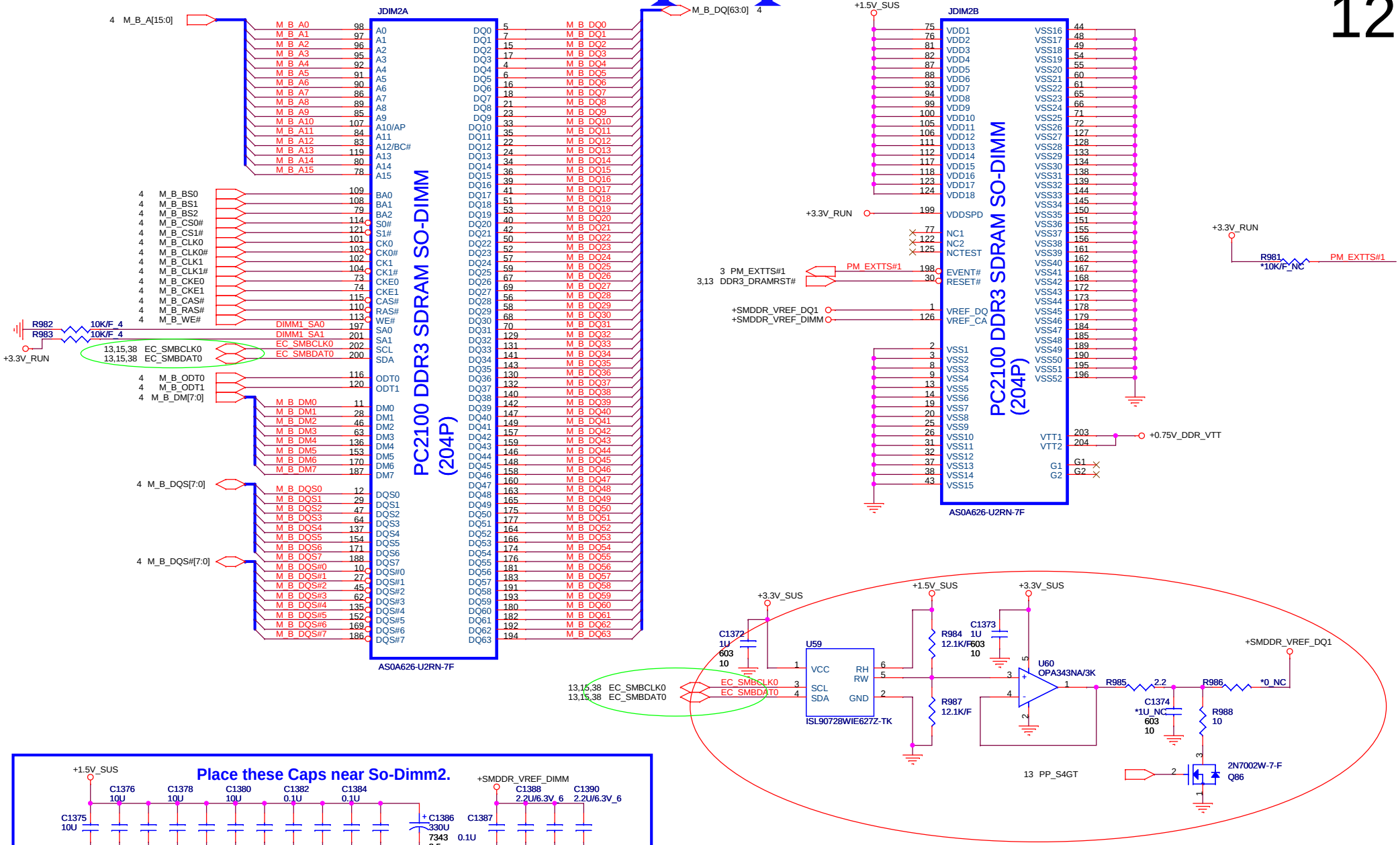

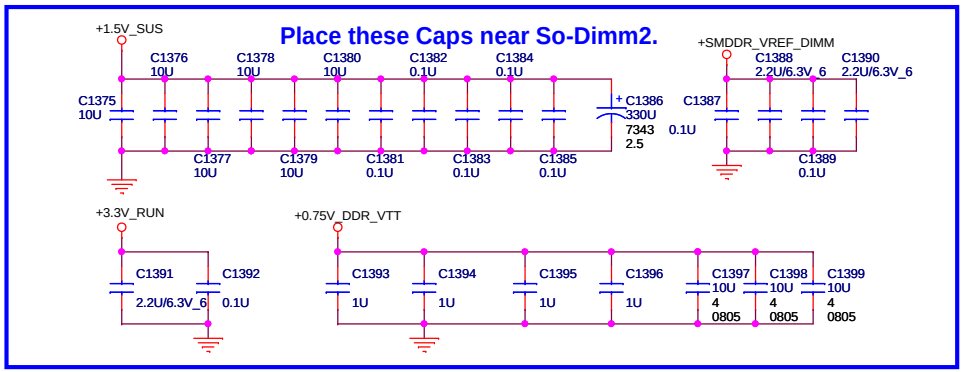

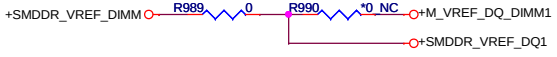

QUANTA COMPUTER

Title	DDR3 DIMM-1	
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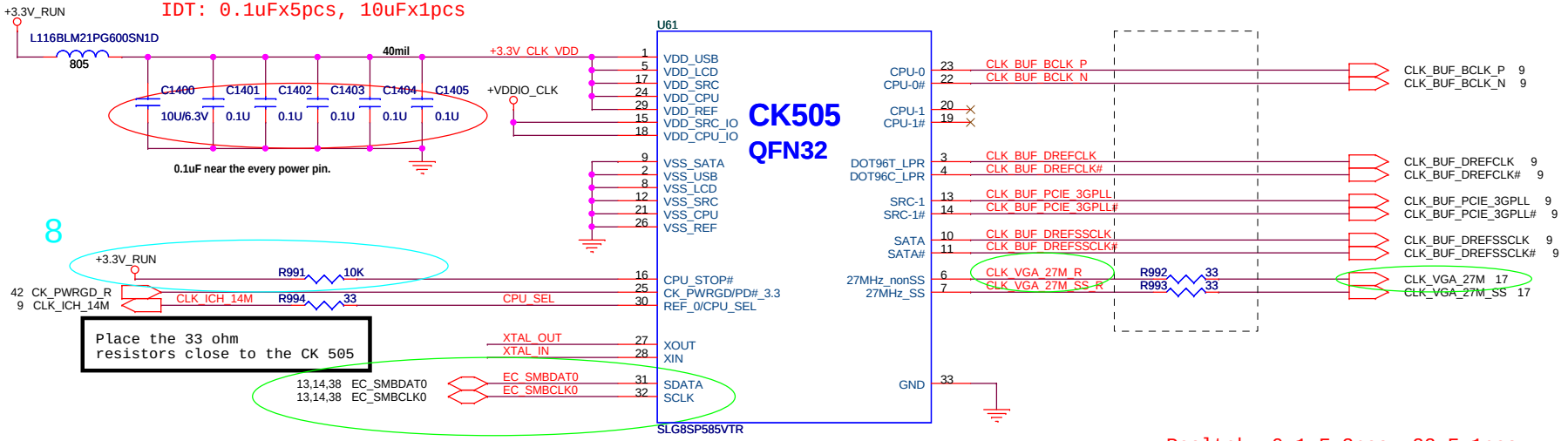
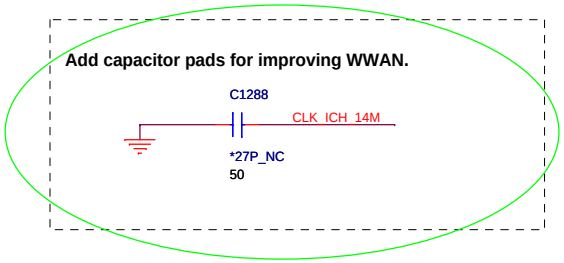
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

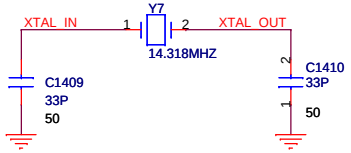
Place within 0.5" of CLKGEN



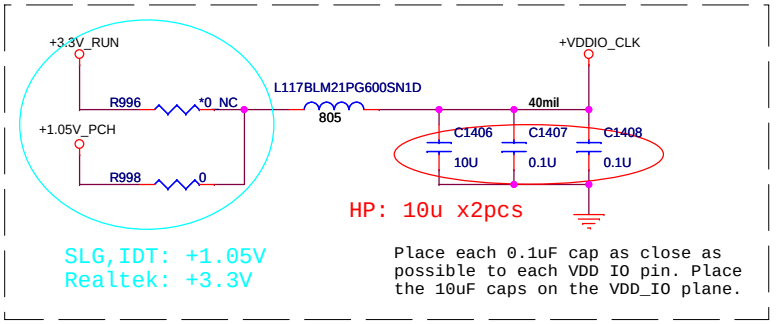
8

Place the 33 ohm resistors close to the CK 505



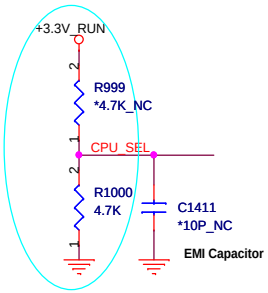


Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

7



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

QUANTA COMPUTER

Title	Clock Generator	
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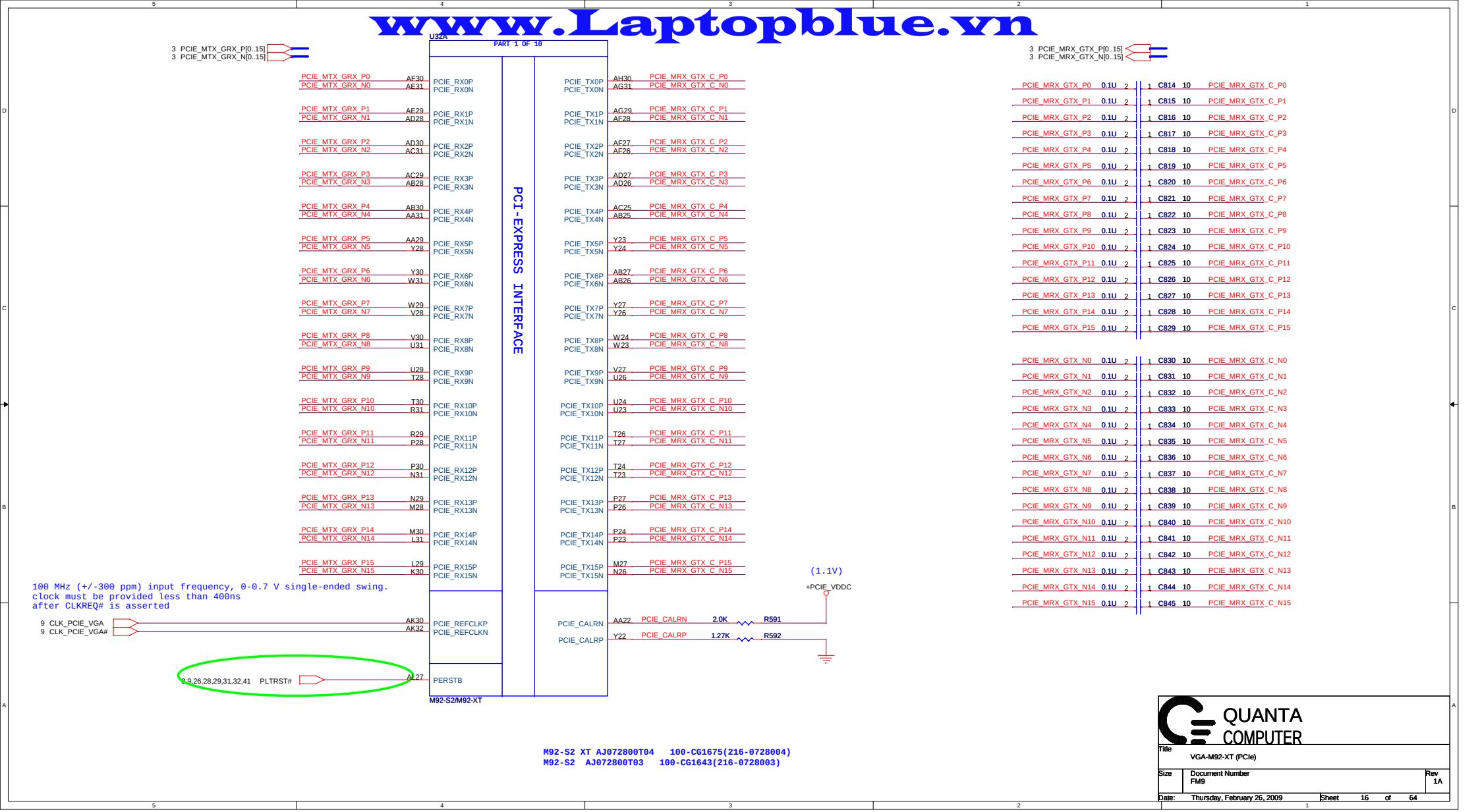

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
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MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	

For Park S3:
Install All components in this Box
L86,C960,C905,C898,L84,
C959,C891,C890,R142,
R143,R144,R145

DPC_VDD18#1 and DPC_VDD18#2 are for Future ASIC
For M92-S2: DO NOT Install any Component in this Box.

As M82 design, for GPIO use

Spread Spectrum
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

	S0
-1.75% (DOWN)	0

DIS only
Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

AVDD=70mA max
VDD1DI=45mA max
A2VDD=65mA max
A2VDDQ=1mA max
VDD2DI=40mA max
Keep A2VSSQ away from noisy ground.
Place very close to ASIC balls

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)
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(PCIE_VDDC 1.0~1.1V +/- 5%@ 2A)

layout note: close to VDDR1#[1:17]

+1.5V_RUN

C869 10nF, C870 10nF, C871 10nF, C872 10nF, C873 10nF, C874 100nF, C875 100nF, C877 100nF, C878 100nF

C879 1U, C880 1U, C881 1U, C882 1U, C883 1U, C886 100nF

+1.5V_RUN

C895 10U, C896 10U, C897 10U

+1.5V_RUN

U32D

PART 4 OF 10

POWER

VDDR1#1 H13, VDDR1#2 H16, VDDR1#3 H19, VDDR1#4 J10, VDDR1#5 J23, VDDR1#6 J24, VDDR1#7 J9, VDDR1#8 K10, VDDR1#9 K23, VDDR1#10 K24, VDDR1#11 K9, VDDR1#12 L11, VDDR1#13 L12, VDDR1#14 L13, VDDR1#15 L20, VDDR1#16 L21, VDDR1#17 L22

PCIE_VDDR#[1..8]=500mA max

+1.8V_RUN_GFX

C888 1U, C892 100nF, C889 1U, C893 10nF, C894 10U

PCIE_VDDR#1 AB23, PCIE_VDDR#2 AC23, PCIE_VDDR#3 AD24, PCIE_VDDR#4 AE24, PCIE_VDDR#5 AE25, PCIE_VDDR#6 AE26, PCIE_VDDR#7 AF25, PCIE_VDDR#8 AG26

(1.1V)

+PCIE_VDDC

PCIE_VDDC#[1..12]=2A max

C899 1U, C900 1U, C901 1U, C902 1U, C903 1U, C904 1U, C906 1U, C907 10U

PCIE_VDDC#1 L23, PCIE_VDDC#2 L24, PCIE_VDDC#3 L25, PCIE_VDDC#4 L26, PCIE_VDDC#5 M22, PCIE_VDDC#6 N22, PCIE_VDDC#7 N23, PCIE_VDDC#8 N24, PCIE_VDDC#9 P22, PCIE_VDDC#10 T22, PCIE_VDDC#11 U22, PCIE_VDDC#12 V22

+1.8V_RUN_GFX

VDD_CT#[1..4]=110mA max

L87 BLM15BD121SN1D

+VDD_CT

C909 10U, C910 100nF, C911 1U, C912 1U, C913 100nF

VDD_CT#1 AA20, VDD_CT#2 AA21, VDD_CT#3 AB20, VDD_CT#4 AB21

+3.3V_DELAY

VDDR3#[1..4]=50mA max

C914 1U, C915 1U, C916 100nF, C908 100nF

VDDR3#1 AA17, VDDR3#2 AA18, VDDR3#3 AB17, VDDR3#4 AB18

+1.8V_RUN_GFX

R45 2 *150/F_NC 1

VDDR4#[1..4] & VDDR5#[1..4]=340mA max

R150 0 2 1, R147 0 2 1

VDDR4#1 AA11, VDDR4#2 AA12, VDDR4#3 Y11, VDDR4#4 Y12

C919 1U, C920 100nF, C921 1U, C922 100nF

R148 0 2 1, R149 0 2 1

VDDR5#1 U11, VDDR5#2 U12, VDDR5#3 V11, VDDR5#4 V12

For M92-S2: Install R147,R148,R149
Use R150 0R to VDDR4
M93-S3 and Park: Remove R147,R148,R149
Use R45 150 Ohms Pull Down

+1.5V_RUN

L88 BLM15BD121SN1D +VDDRH1

C923 1U, C924 1U

VDDRHA L17

VSSRHA L16

(0.9~1.2V)

+VCC_GFX_CORE

VDDC#[2..3]=120mA max

+BBP

C917 100nF, C918 1U

VDDC#1 AA15, VDDC#2 M11, VDDC#3 M12, VDDC#4 N15, VDDC#5 N17, VDDC#6 R13, VDDC#7 R16, VDDC#8 R18, VDDC#9 R21, VDDC#10 T12, VDDC#11 T15, VDDC#12 T17, VDDC#13 T20, VDDC#14 U13, VDDC#15 U16, VDDC#16 U18, VDDC#17 U21, VDDC#18 V15, VDDC#19 V17, VDDC#20 V20, VDDC#21 V21, VDDC#22 Y13, VDDC#23 Y16, VDDC#24 Y18, VDDC#25 Y21

DDCI=2A max

+VDDCI

(0.9~1.2V)

VDDCI#1 M13, VDDCI#2 M15, VDDCI#3 M16, VDDCI#4 M17, VDDCI#5 M18, VDDCI#6 M20, VDDCI#7 M21, VDDCI#8 N20

M92-S2/M92-XT

U32E

PART 5 OF 10

GND

PCIE_VSS#1 AA27, PCIE_VSS#2 AB24, PCIE_VSS#3 AB32, PCIE_VSS#4 AC24, PCIE_VSS#5 AC26, PCIE_VSS#6 AC27, PCIE_VSS#7 AD25, PCIE_VSS#8 AD32, PCIE_VSS#9 AE27, PCIE_VSS#10 AF32, PCIE_VSS#11 AG27, PCIE_VSS#12 AH32, PCIE_VSS#13 K28, PCIE_VSS#14 K32, PCIE_VSS#15 L27, PCIE_VSS#16 M32, PCIE_VSS#17 N25, PCIE_VSS#18 N27, PCIE_VSS#19 P25, PCIE_VSS#20 P32, PCIE_VSS#21 R27, PCIE_VSS#22 T25, PCIE_VSS#23 T32, PCIE_VSS#24 U25, PCIE_VSS#25 U27, PCIE_VSS#26 V32, PCIE_VSS#27 W25, PCIE_VSS#28 W26, PCIE_VSS#29 W27, PCIE_VSS#30 Y25, PCIE_VSS#31 Y32

GND#1 A3, GND#2 A30, GND#3 AA13, GND#4 AA16, GND#5 AB10, GND#6 AB15, GND#7 AB6, GND#8 AC9, GND#9 AD6, GND#10 AD8, GND#11 AE7, GND#12 AG12, GND#13 AH10, GND#14 AH28, GND#15 B10, GND#16 B12, GND#17 B14, GND#18 B16, GND#19 B18, GND#20 B20, GND#21 B22, GND#22 B24, GND#23 B26, GND#24 B6, GND#25 B8, GND#26 C1, GND#27 C32, GND#28 E28, GND#29 F10, GND#30 F12, GND#31 F14, GND#32 F16

GND#33 F18, GND#34 F2, GND#35 F20, GND#36 F22, GND#37 F24, GND#38 F26, GND#39 F6, GND#40 F8, GND#41 G10, GND#42 G27, GND#43 G31, GND#44 G8, GND#45 H14, GND#46 H17, GND#47 H2, GND#48 H20, GND#49 H6, GND#50 J27, GND#51 J31, GND#52 K11, GND#53 K2, GND#54 K22, GND#55 K6, GND#56 M6, GND#57 N11, GND#58 N12, GND#59 N13, GND#60 N16, GND#61 N18, GND#62 N21, GND#63 P6, GND#64 P9, GND#65 R12, GND#66 R15, GND#67 R17, GND#68 R20, GND#69 T13, GND#70 T16, GND#71 T18, GND#72 T21, GND#73 T6, GND#74 U15, GND#75 U17, GND#76 U20, GND#77 U3, GND#78 U9, GND#79 V13, GND#80 V16, GND#81 V18, GND#82 V6, GND#83 Y10, GND#84 Y15, GND#85 Y17, GND#86 Y20, GND#87 Y6, GND#88 T11, GND#89 R11

VSS_MECH#1 A32, VSS_MECH#2 AM1, VSS_MECH#3 AM32

M92-S2/M92-XT

+BBP

Q71 SI2301BDS-T-GE3

C866 1U 402 6.3

+1.8V_RUN_GFX

Q70 2N7002W-7-F

(0.9~1.2V)

+VCC_GFX_CORE

R652 100K

+5V_RUN

17 BB_ENA

Q74 2N7002W-7-F

R653 10K

layout note: close to VDDC#[1:25]

(0.9~1.2V)

+VCC_GFX_CORE

C925 1U, C926 1U, C927 1U, C929 1U, C930 1U

C931 1U, C932 1U, C933 1U, C934 1U, C935 1U, C936 1U, C937 1U, C939 1U

(0.9~1.2V)

+VCC_GFX_CORE

C947 10U, C946 10U, C948 10U

L12 BLM18PG121SN1D

+1.1V_GFX_PCIE

(1.1V)

+PCIE_VDDC

C168 10U 603 6.3, C183 1U 402 6.3, C211 0.1U 10

C68 10U 603 6.3, C74 1U 402 6.3, C196 0.1U 10

(0.9~1.2V)

+VCC_GFX_CORE

(0.9~1.2V)

+VDDCI

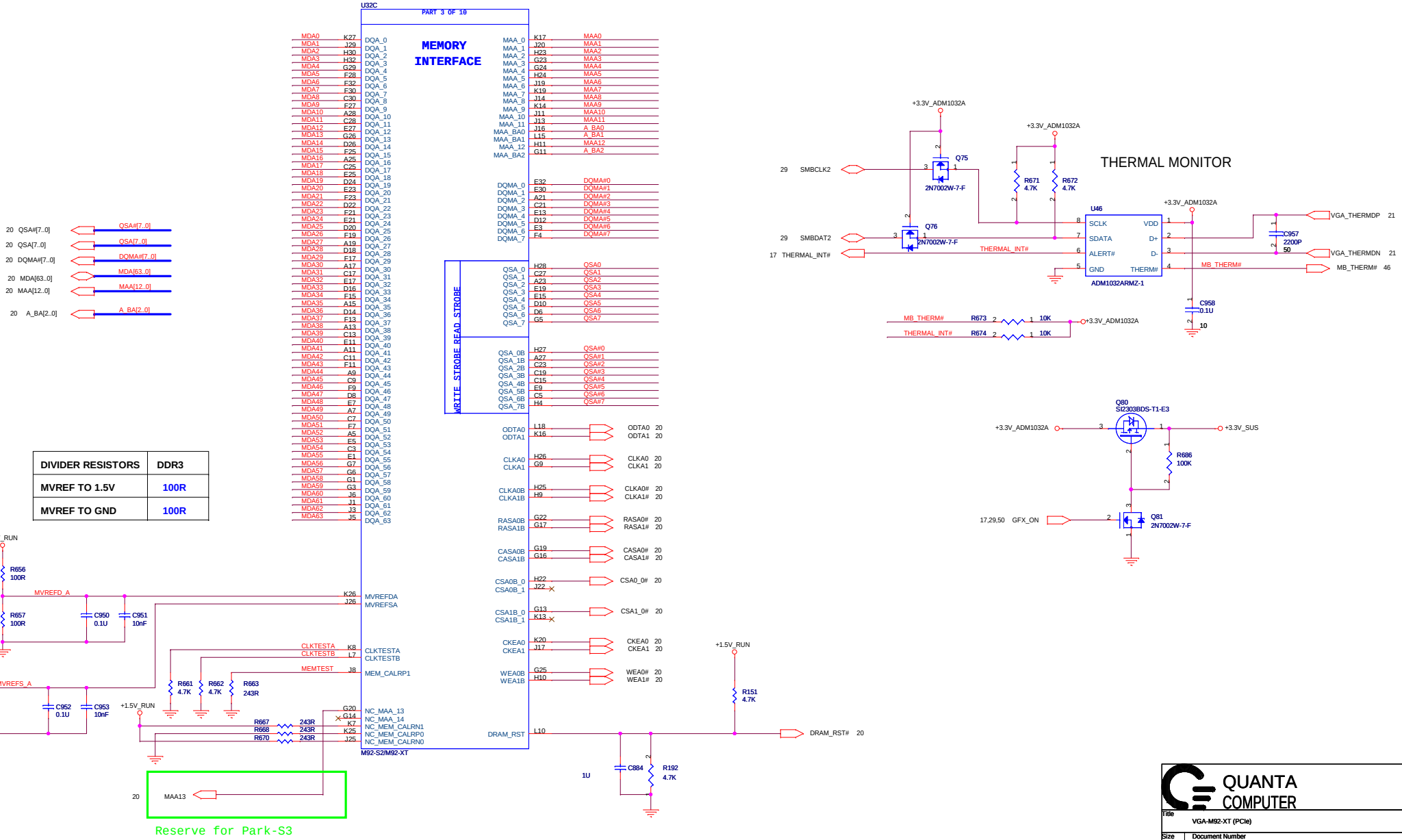
L89 BLM18EG221SN1D

C941 100nF, C942 100nF, C943 1U, C944 1U, C945 10U

QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 18 of 64	

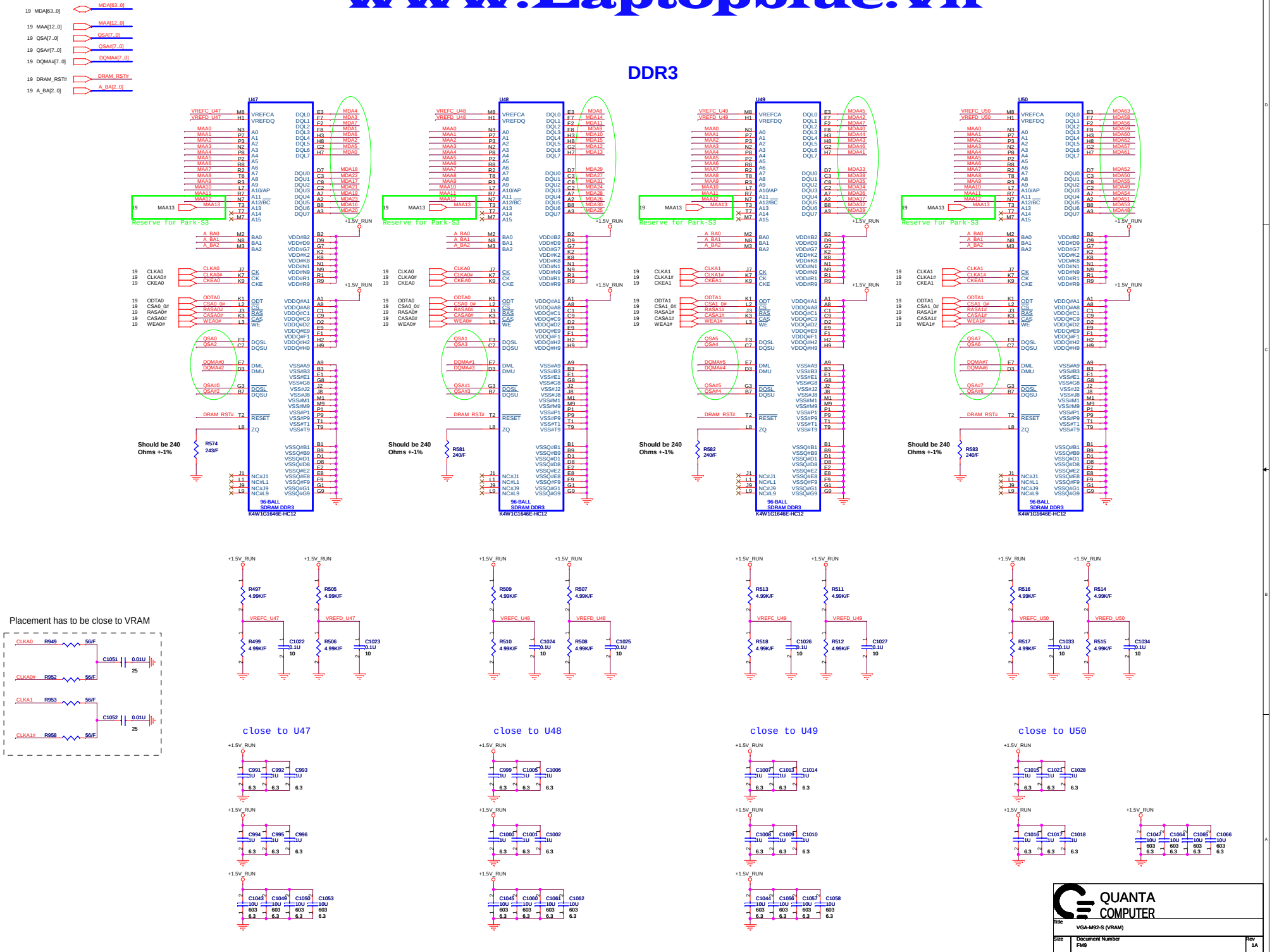
MEMORY INTERFACE



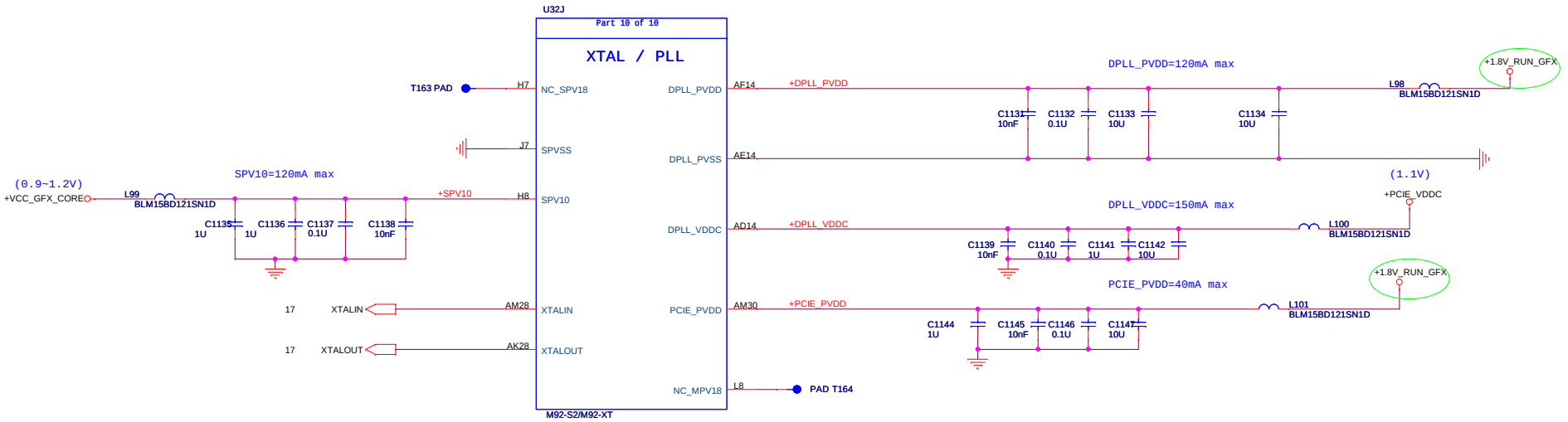
Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 19 of 64	

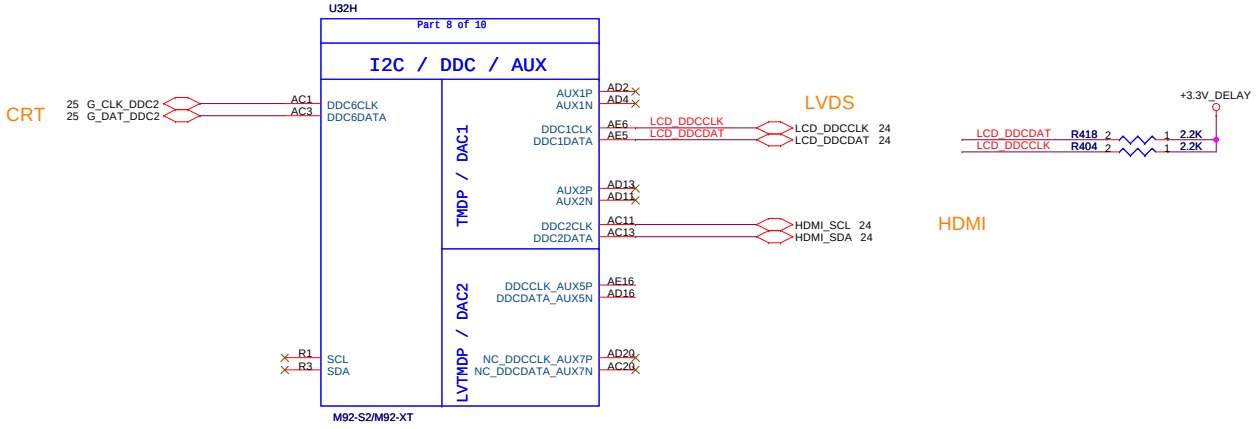
QUANTA COMPUTER

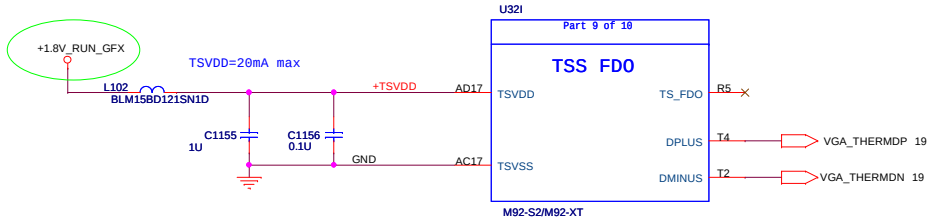
DDR3



Title	VGA-M92-S (VRAM)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 20 of 64	







QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 1A
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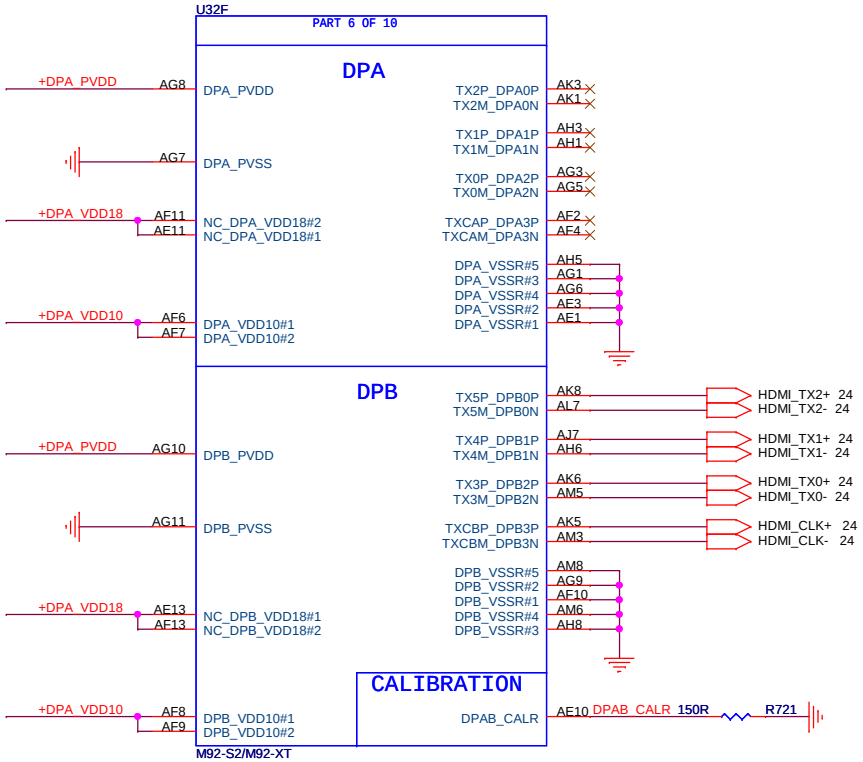
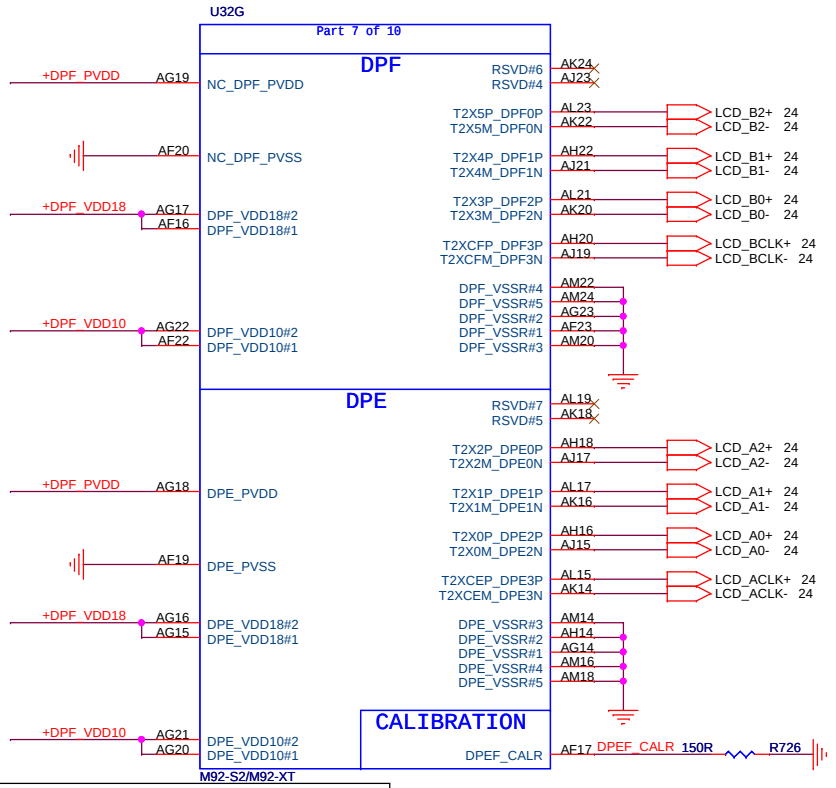
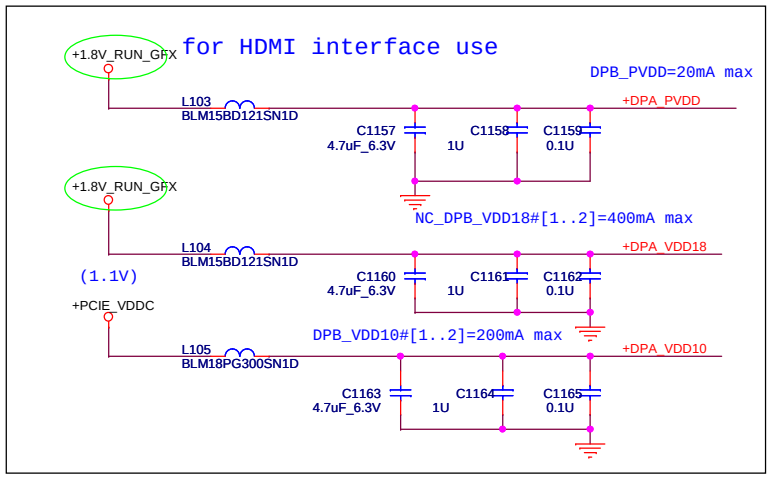
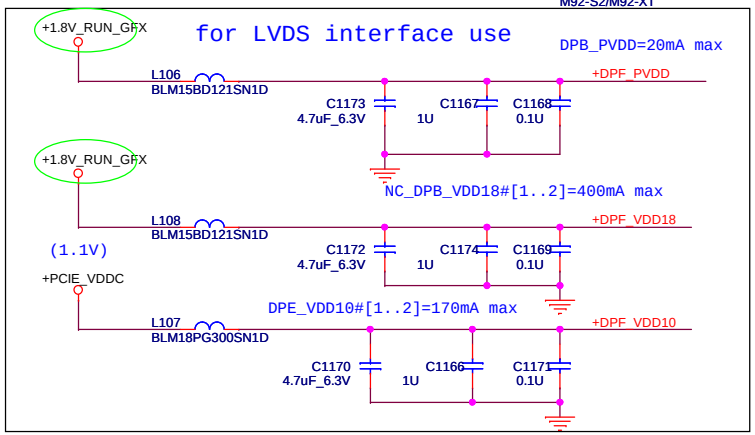
TMDP(HDMI) INTERFACE



LVDS INTERFACE







QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number FM9	Rev 1A
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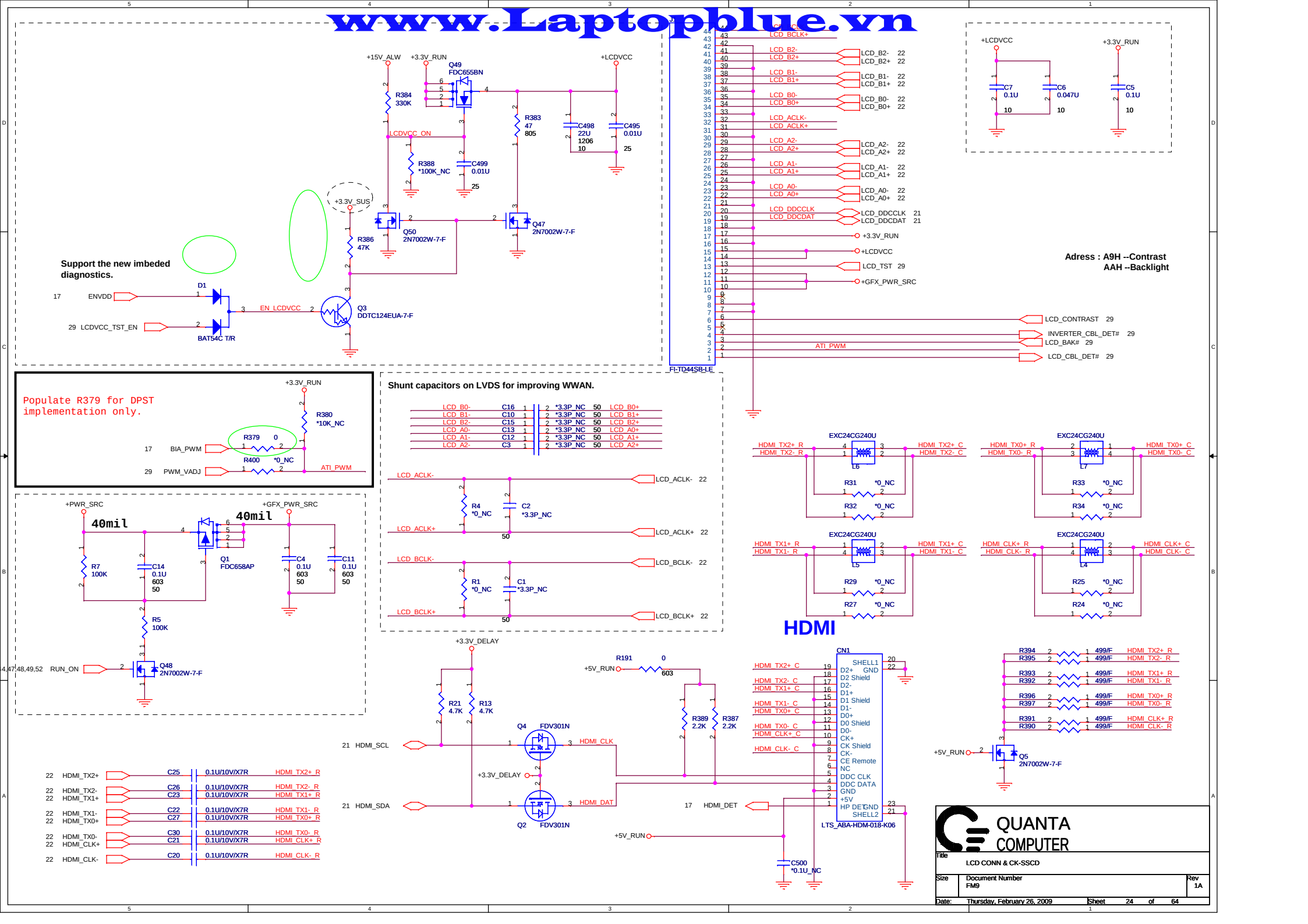
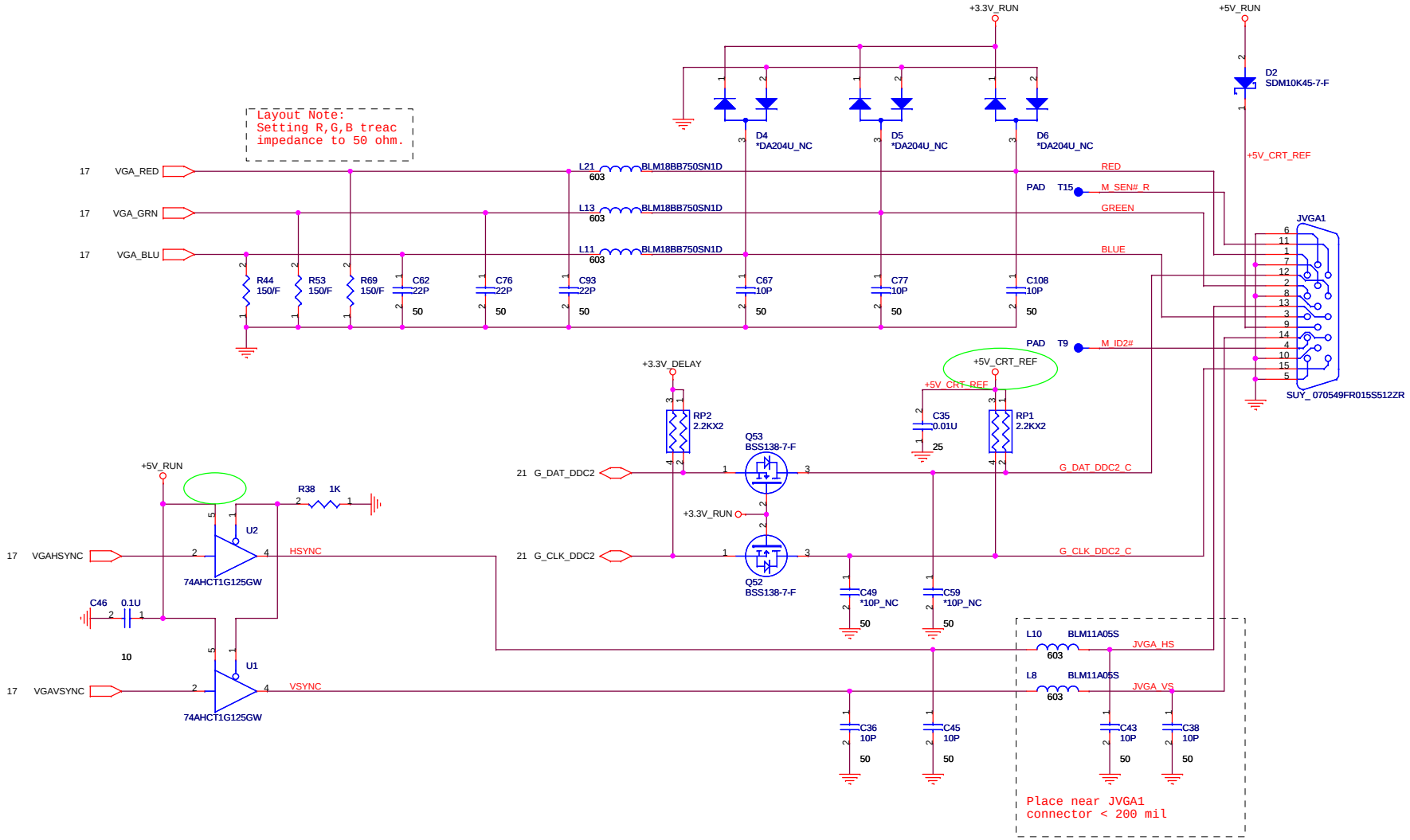
QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 23 of 64	



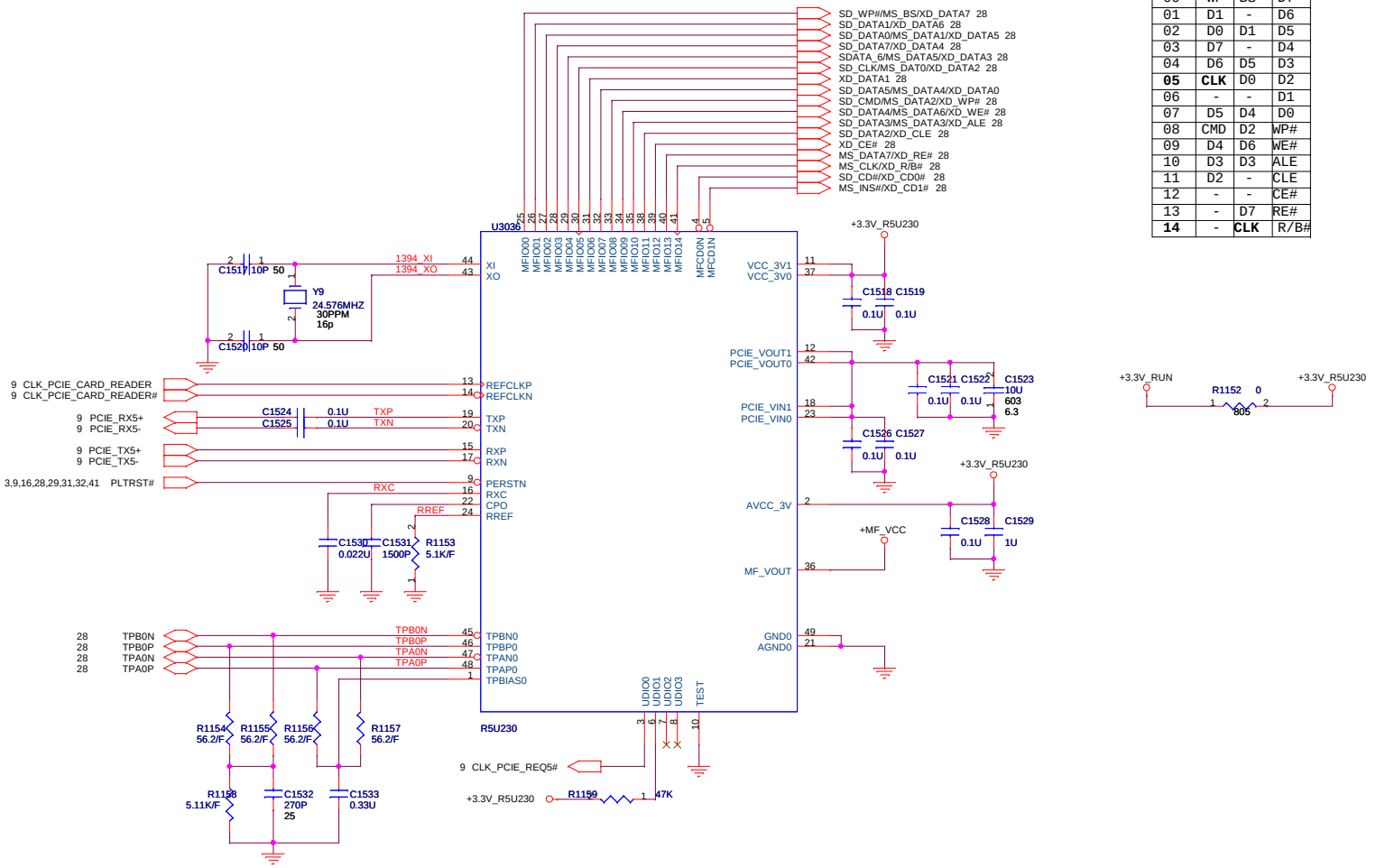


QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 25 of 64	

MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	**CLK**	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	**CLK**	R/B#



QUANTA COMPUTER

Title	5 IN 1 CONTROLLER	
Size	Document Number FM9	Rev 1A
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QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number FM9	Rev 1A
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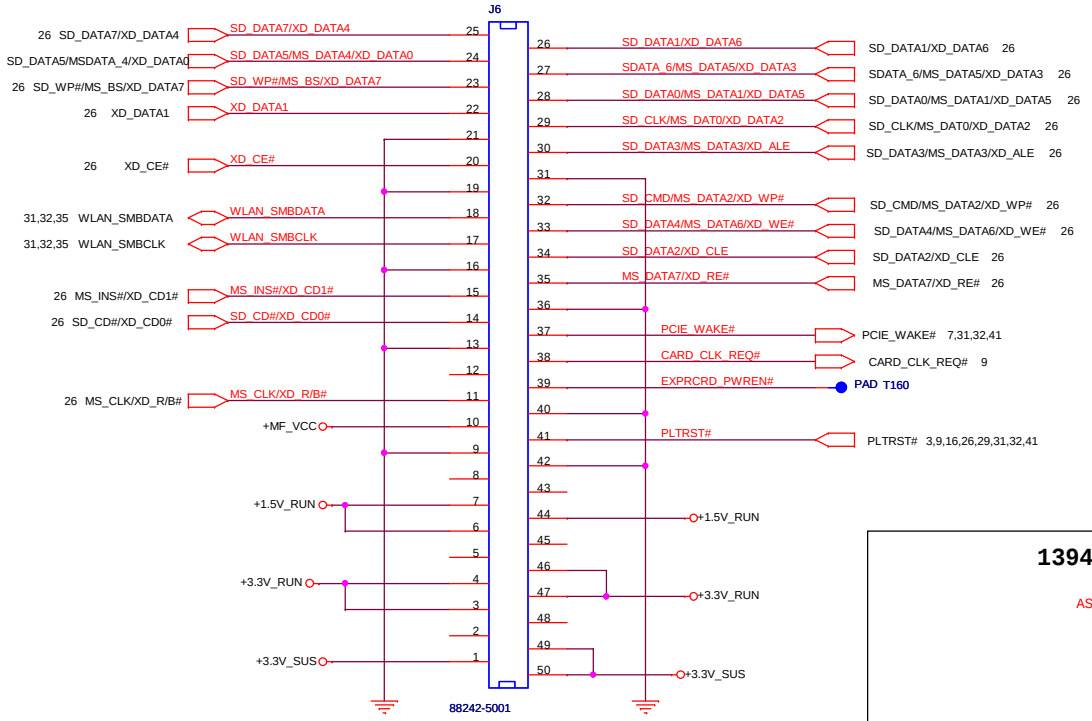
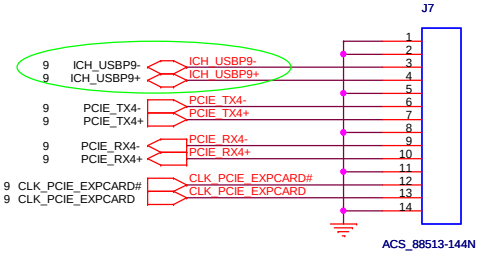
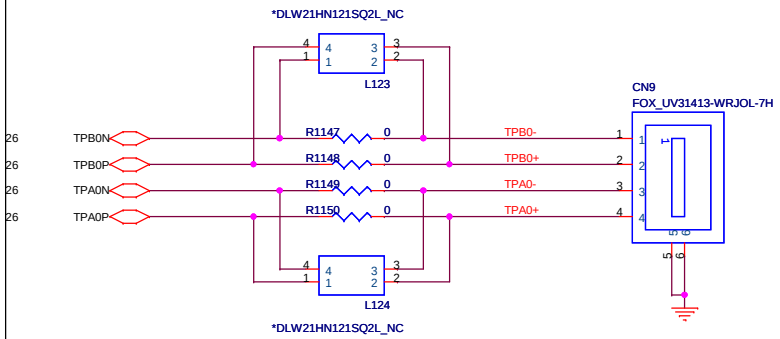
Express Card/CARD READER





1394 CONNECTOR

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
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ITE8502E
LQFP-128L

Place these caps close to ITE8502.

Charge and BAT

CLK, LCD and Thermal

G_Thermal and Media button

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

32KHz Clock.

Board ID Straps

VGA_IDENTIFY

BID0

CHIPSET_ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		

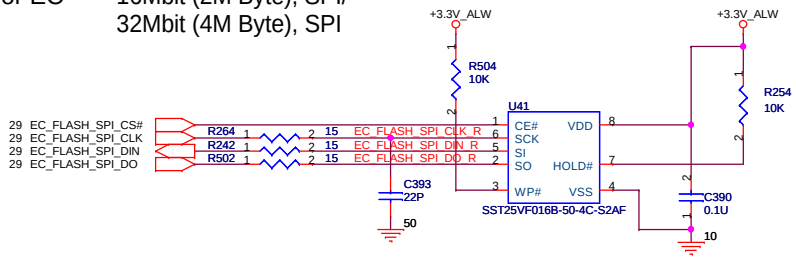
QUANTA COMPUTER

Title: Ultra I/O Controller ECE5028

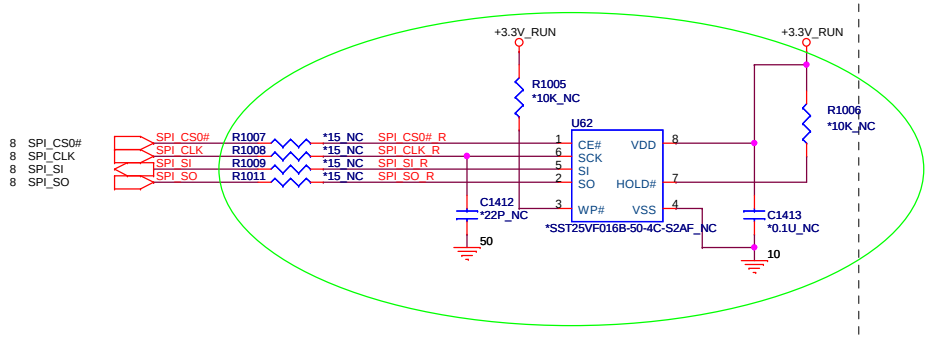
Size: | Document Number: FM9 | Rev: 1A

Date: Thursday, February 26, 2009 | Sheet 29 of 64

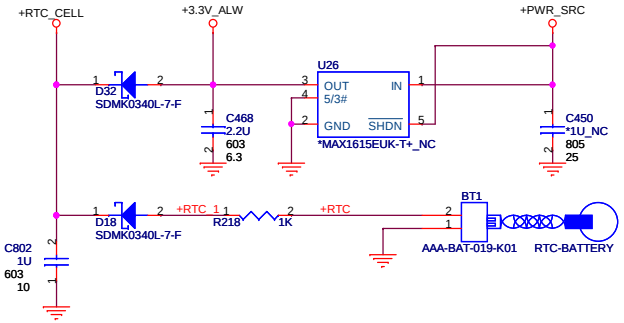
For EC 16Mbit (2M Byte), SPI/ 32Mbit (4M Byte), SPI



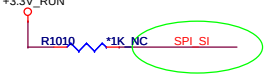
For PCH 16Mbit (2M Byte), SPI/ 32Mbit (4M Byte), SPI



RTC BATTERY



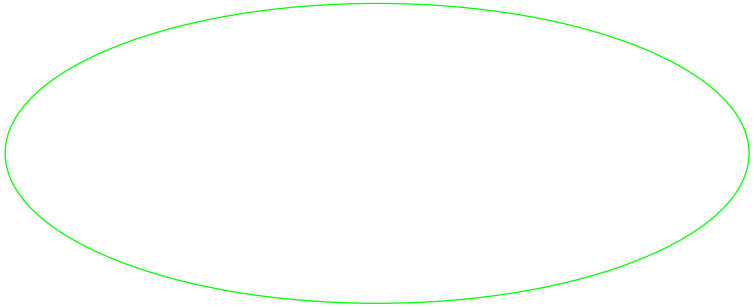
iTPM ENABLE/DISABLE



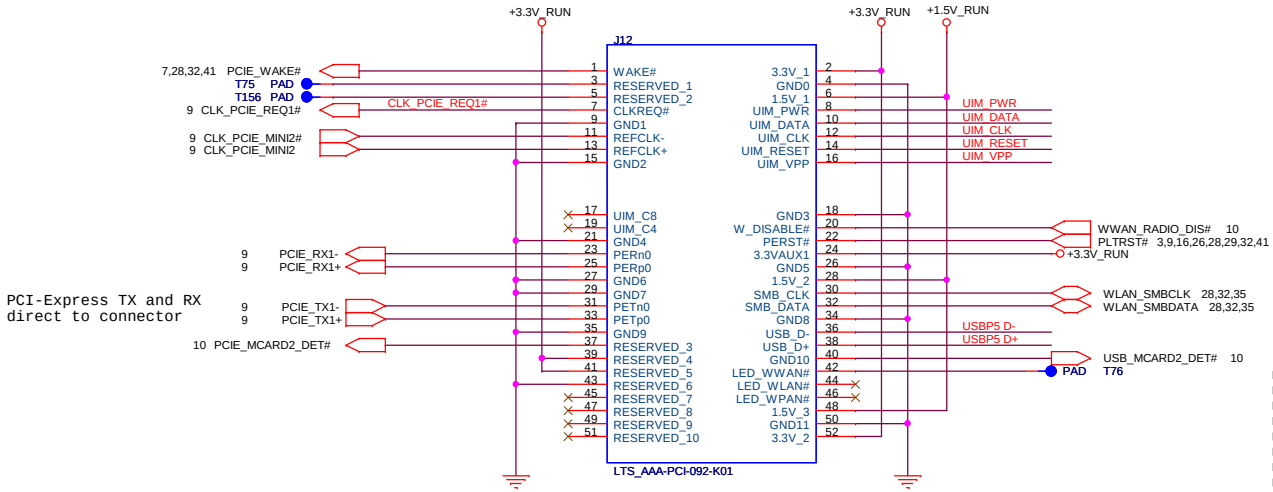
TPM Function	R712
Enable	Mount
Disable	NC (Default)

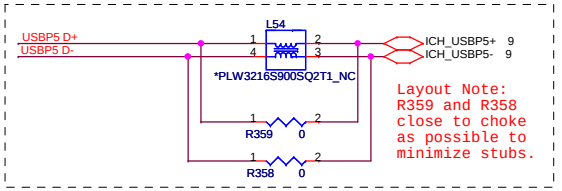
QUANTA COMPUTER

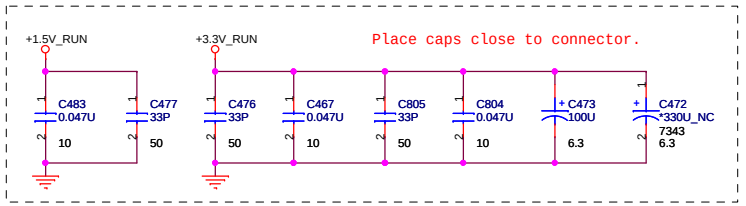
Title	Ultra I/O Controller ECE5028	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 30 of 64	

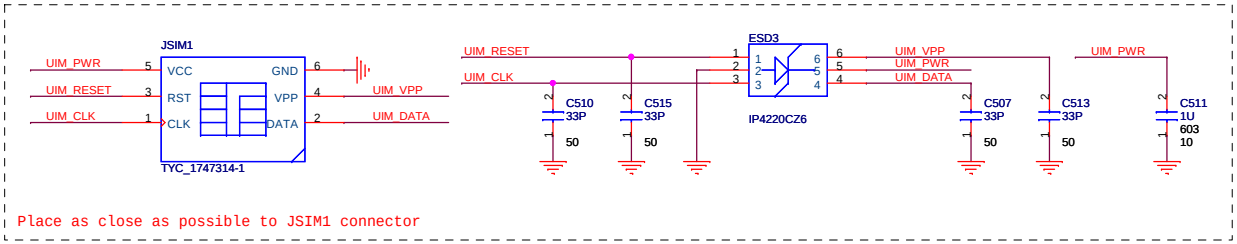


MiniCard WWAN connector









QUANTA COMPUTER		
Title: MINI-PCI		
Size	Document Number: FM9	Rev: 1A
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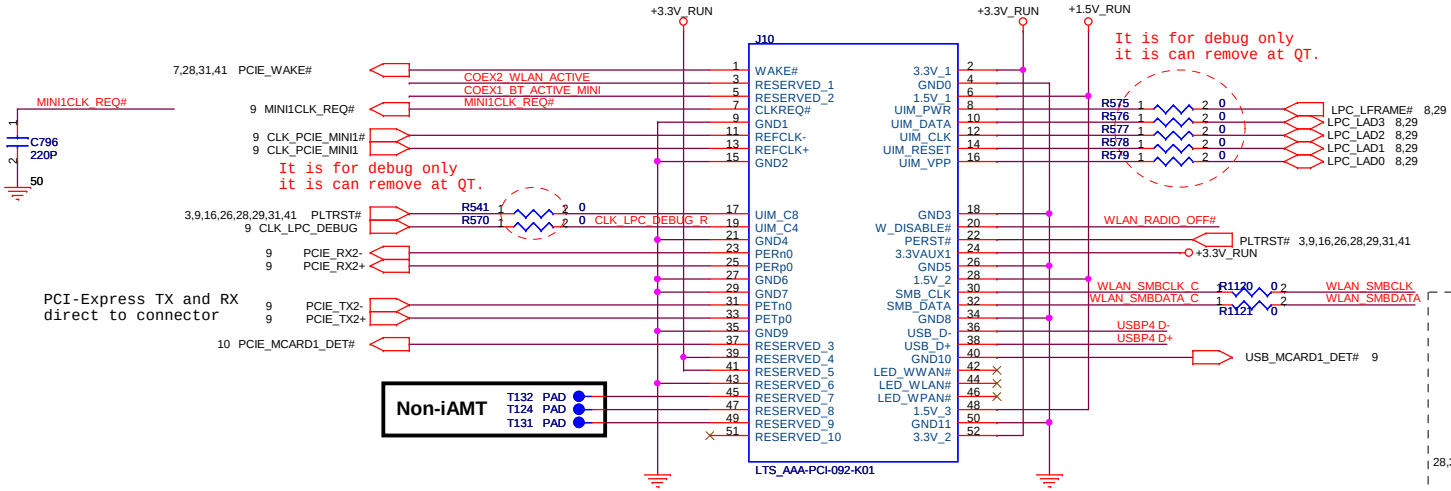
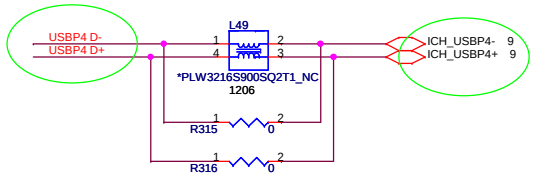
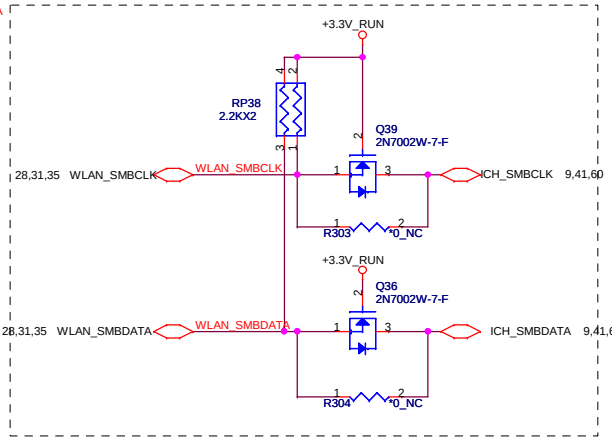
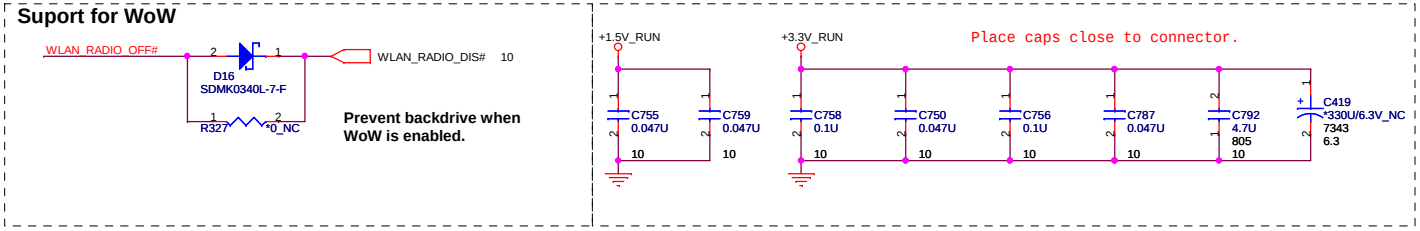
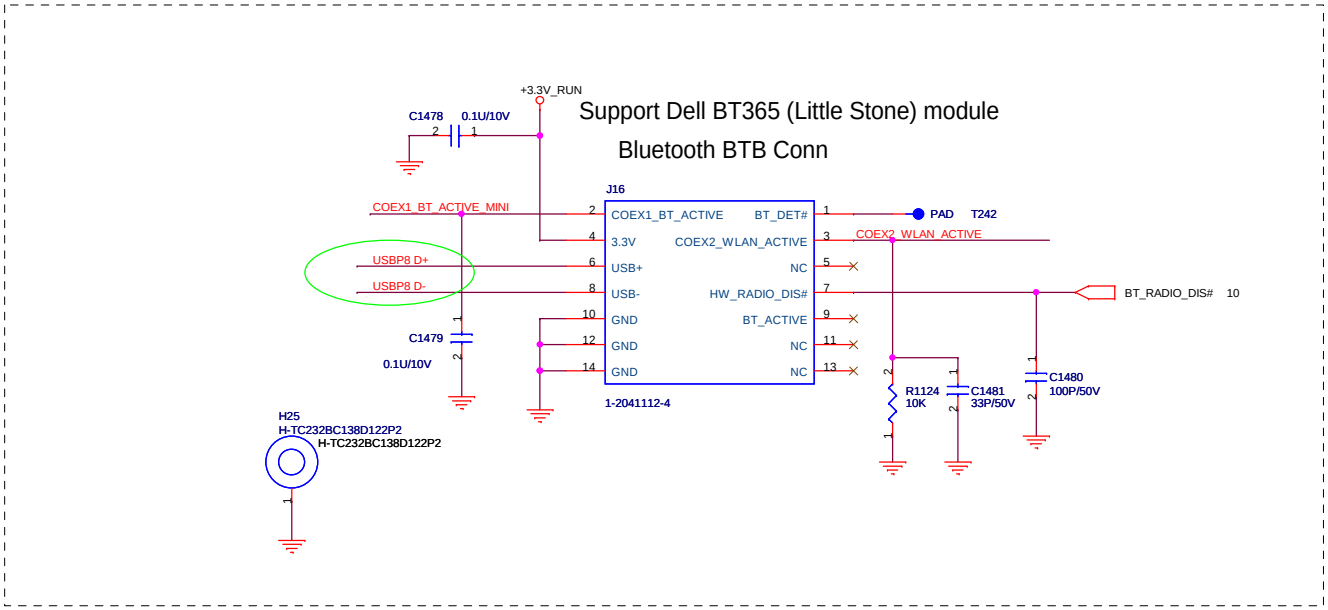
MiniCard WLAN connector

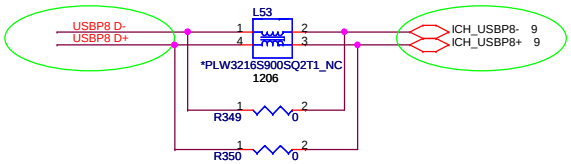












QUANTA COMPUTER		
Title: MDC CONN.		
Size	Document Number: FM9	Rev: 1A
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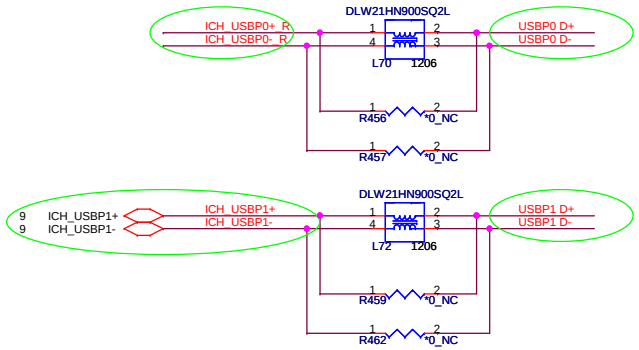
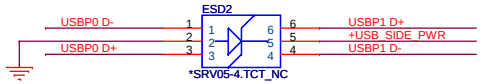
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



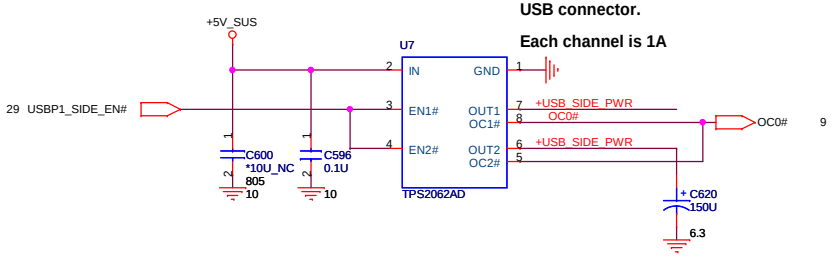
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

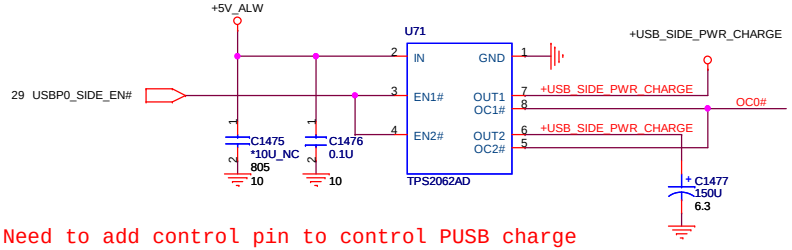
Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A



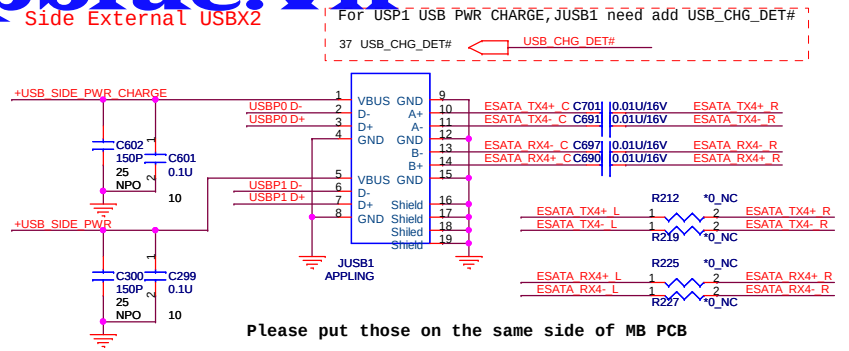


Need to add control pin to control PUSB charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

Side External USBX2

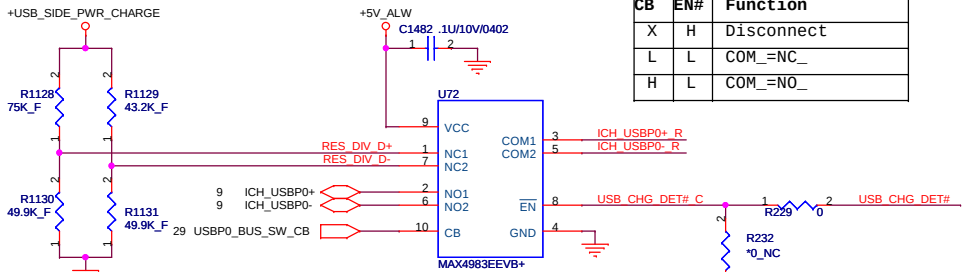
For USP1 USB PWR CHARGE,JUSB1 need add USB_CHG_DET#



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

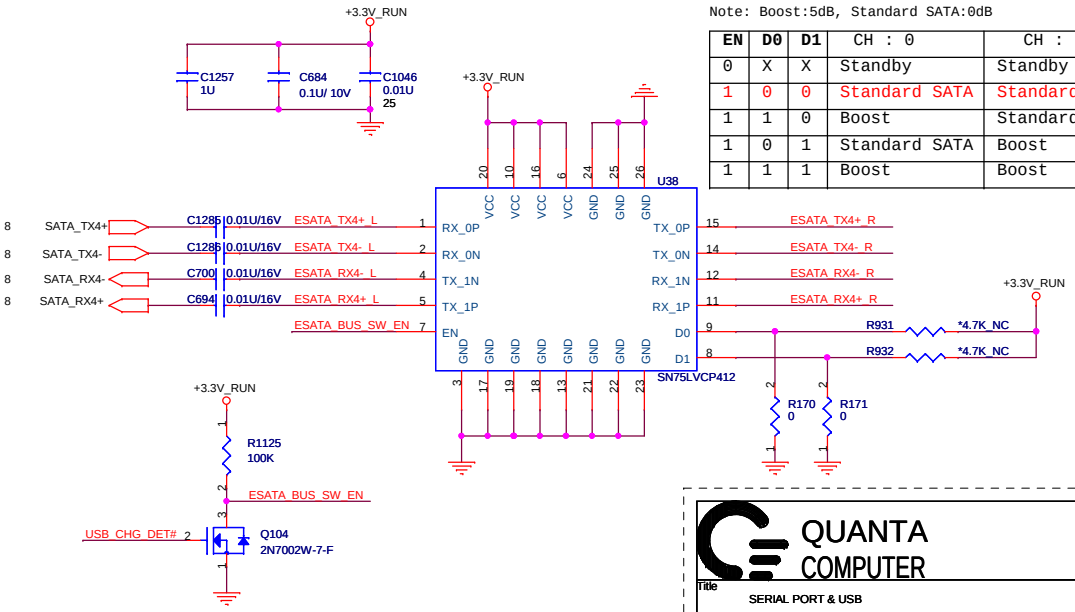
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Please put those on the same side of MB PCB

Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



Title	SERIAL PORT & USB
Size	Document Number FM9
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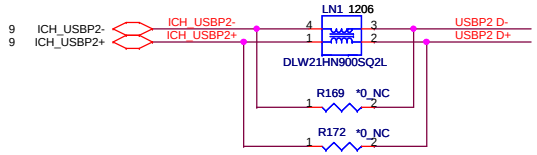
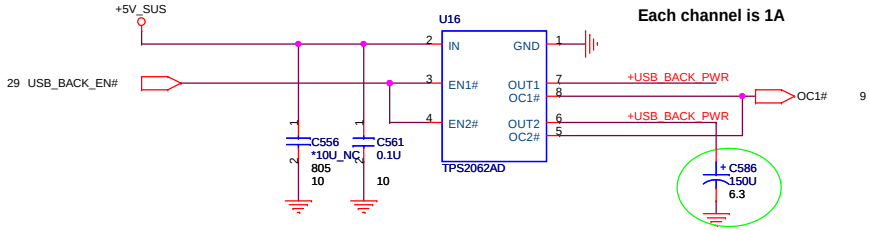
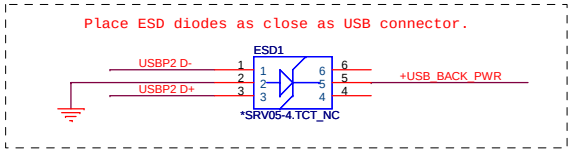
QUANTA COMPUTER

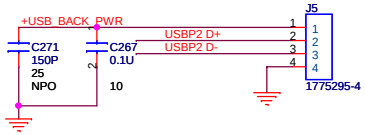


Place one 150uF cap by each USB connector.

Each channel is 1A







QUANTA COMPUTER

Title	Right USB	
Size	Document Number FM9	Rev 1A
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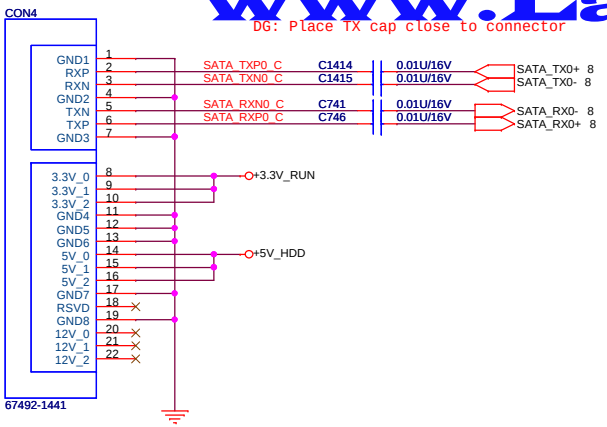
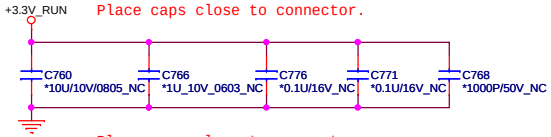
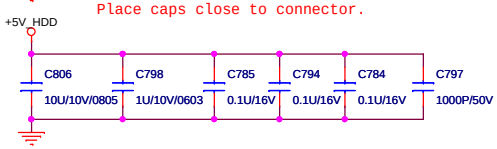
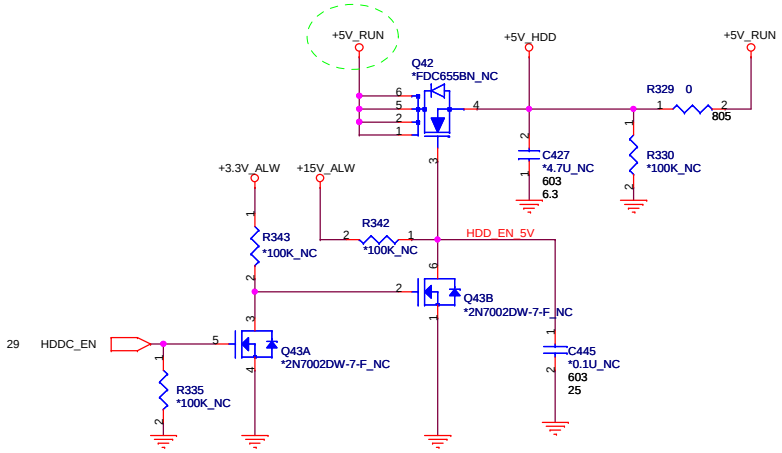
SATA Connector.

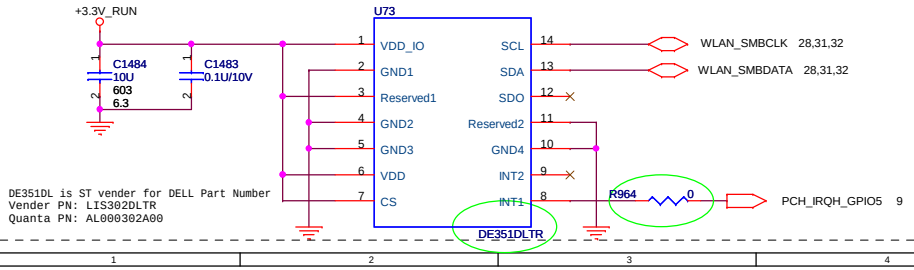




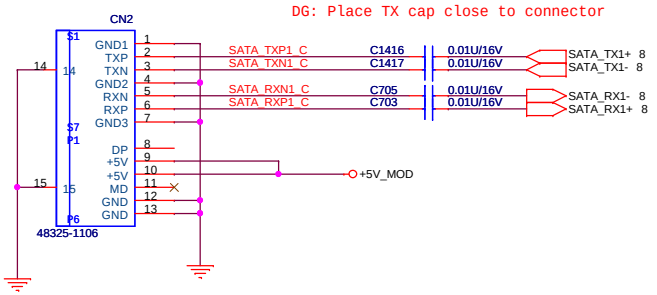


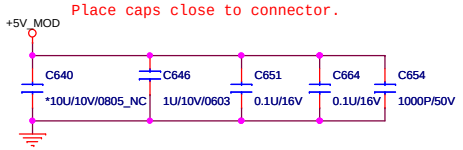


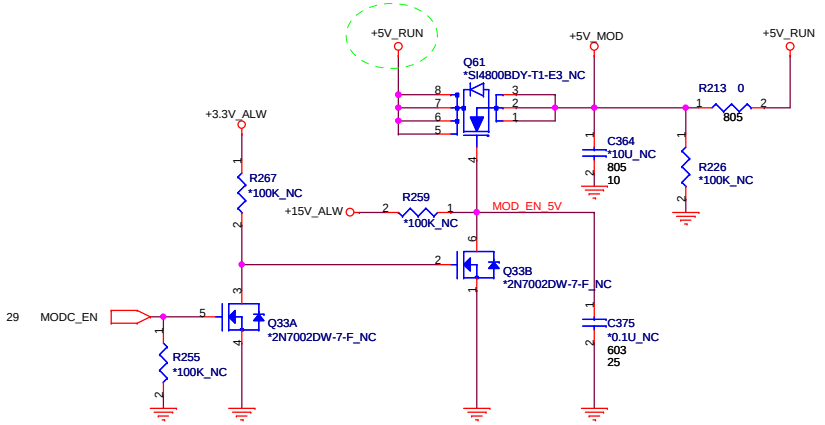
3-axis Fall Sensor (HDD data protector)



ODD Connector







QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number: FM9	Rev: 1A
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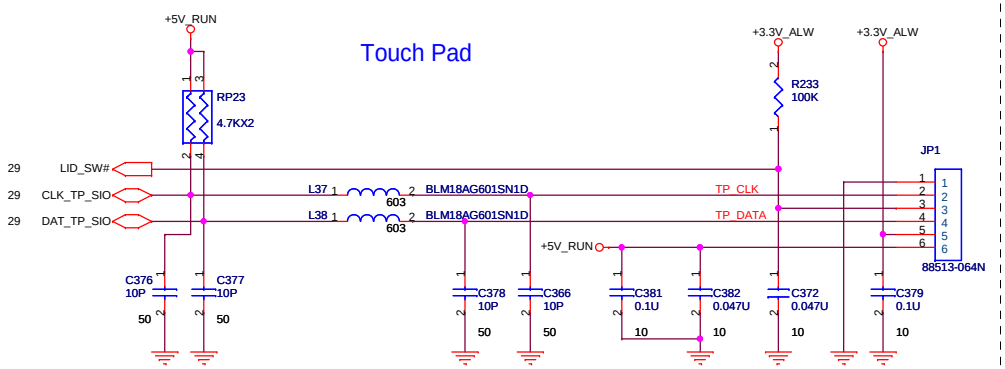
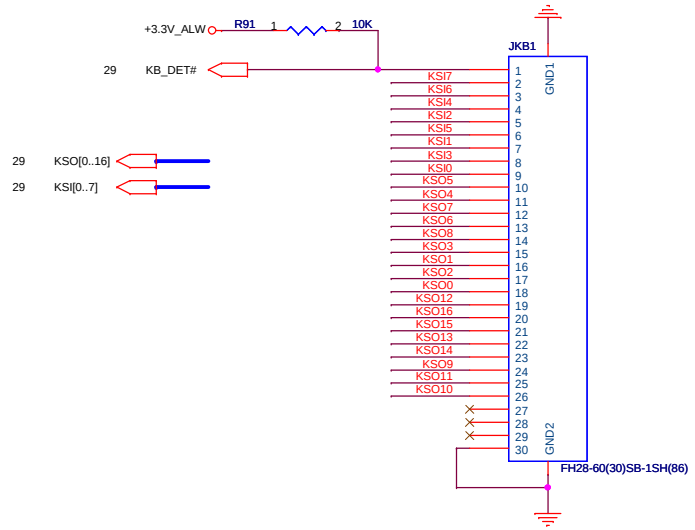
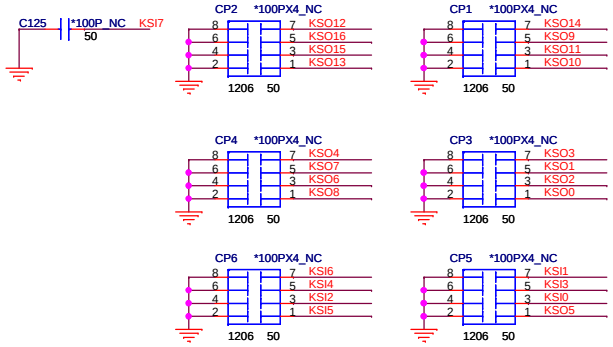
Touch Pad



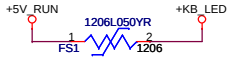


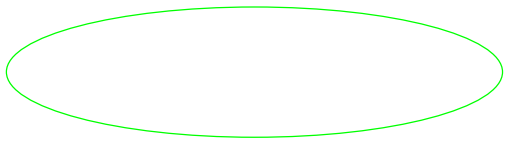


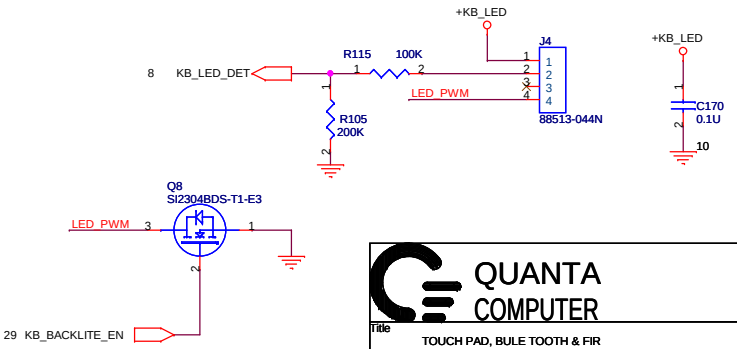
100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil







QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number FM9	Rev 1A
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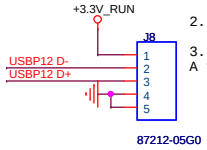
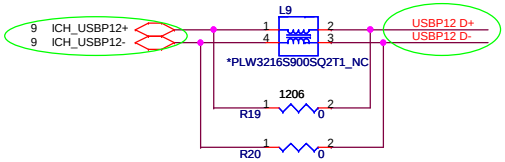
Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

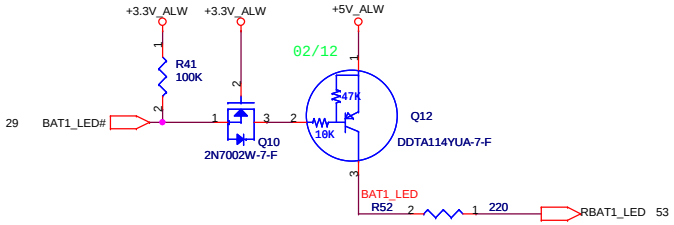


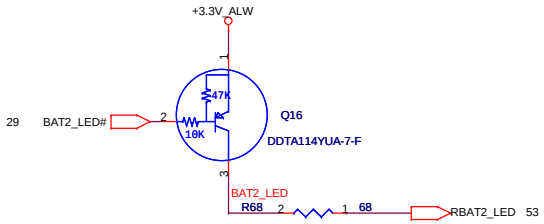
Need check the connector footprint and symble.



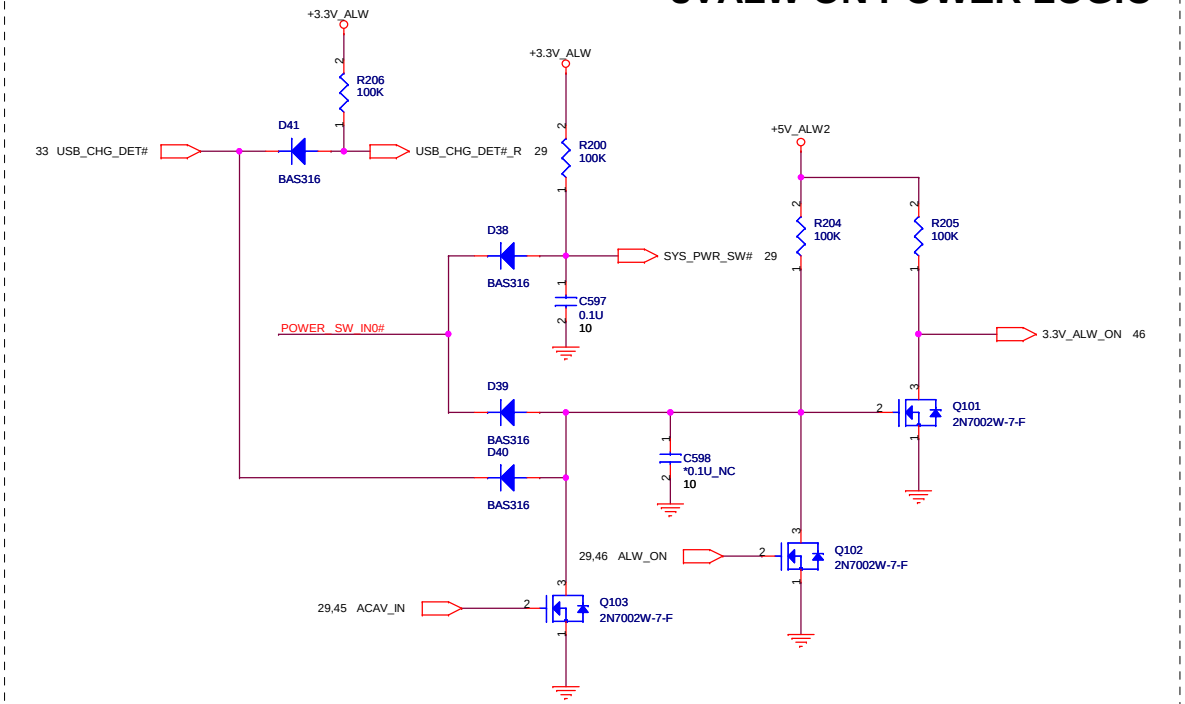
Power button Cable

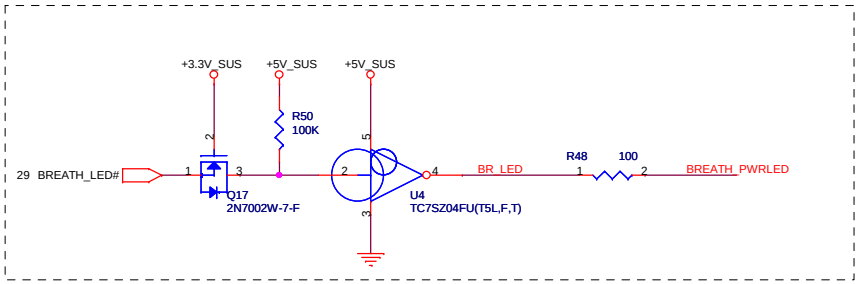
Battery status.

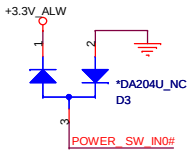


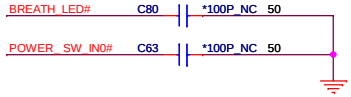


3VALW ON POWER LOGIC



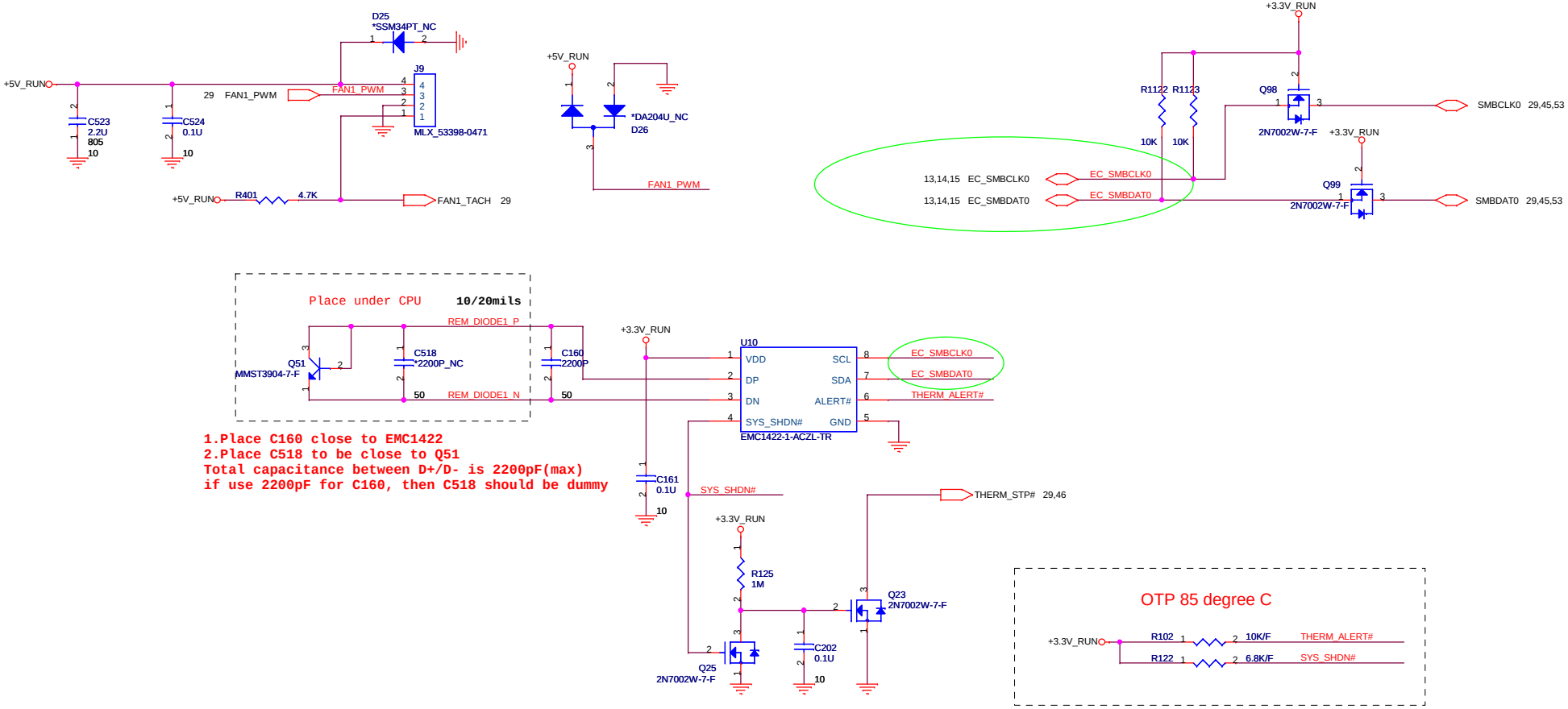






QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED&Touch Screen Module	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 37 of 64	



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 38 of 64	

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK ENABLE#	WOOFER_EN
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofer)
1	1	0	L (Test SPK)	L (Disable Woofer)
1	1	1	L	H

INTERNAL SPEAKER AMP

TPA6040A4
QFN 32PIN

Layout Note: Place close U18 pin 23.

Layout Note: Close to U18 Pin 34

Layout Note: Place close to pin 18.

Layout Note: Place close U18.

AZALIA (HD) CODEC

U19

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Depop R479,C699 for using 92HD73C

Depop R477,R478,R484,R473
Pop R476,R480,R483,R475
for using 92HD73C
R476,R483 close to U19, Let DVDD width be 10-mils

Layout Note: Close to U19 Pin 13

Layout Note: Place close to pin 8.

Close to U19

Check it is ok at ST, if it is ok then remove it.

92HD73C

Company	QUANTA COMPUTER
Title	Azelia CODEC
Size	Document Number: FM9
Rev	1A
Date	Thursday, February 26, 2009
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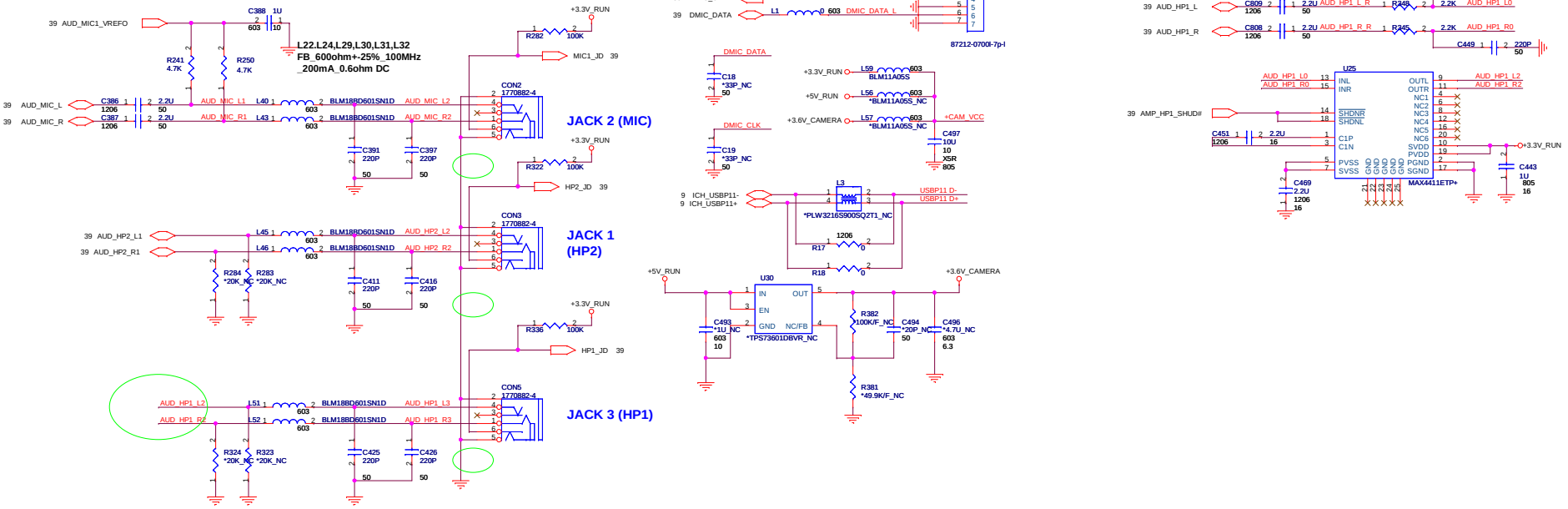
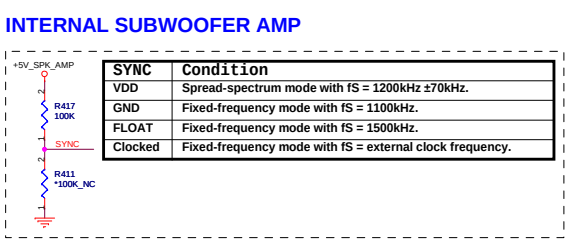
Headphone Jack
Stereo MIC Jack

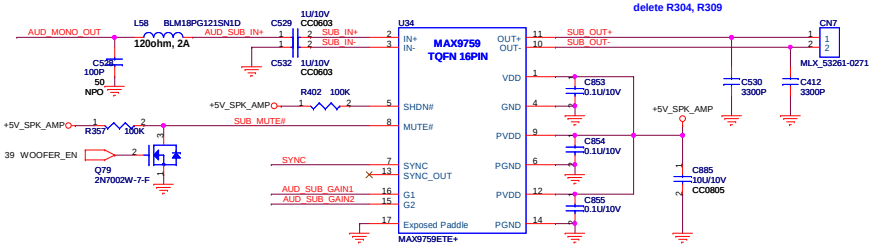


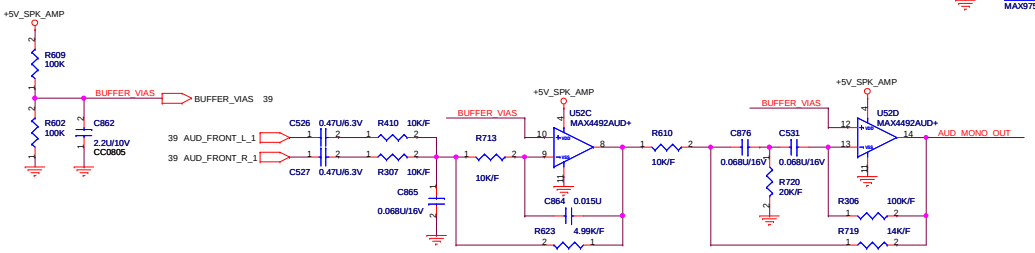
INTERNAL SUBWOOFER AMP

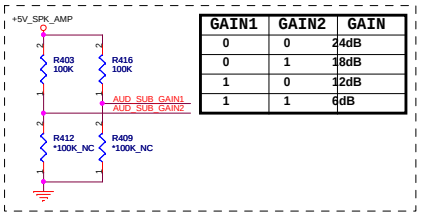
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



Gur_0808: 0 ohm removal, delete R304, R309



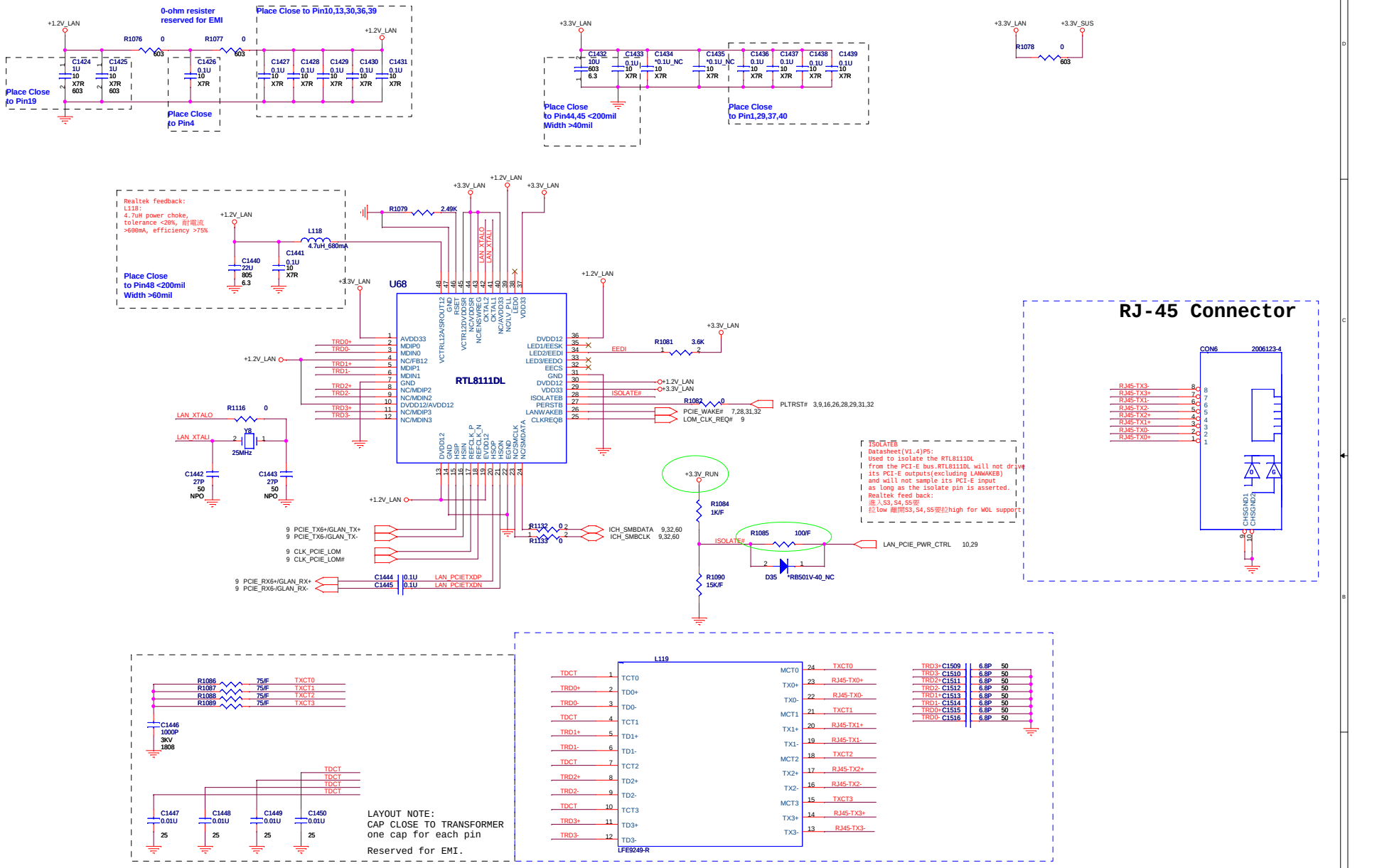




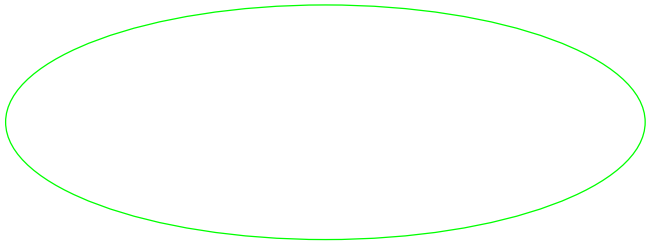
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

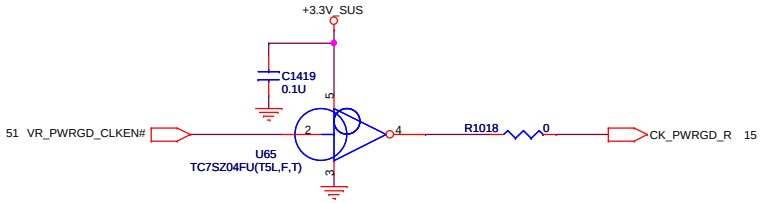
QUANTA COMPUTER

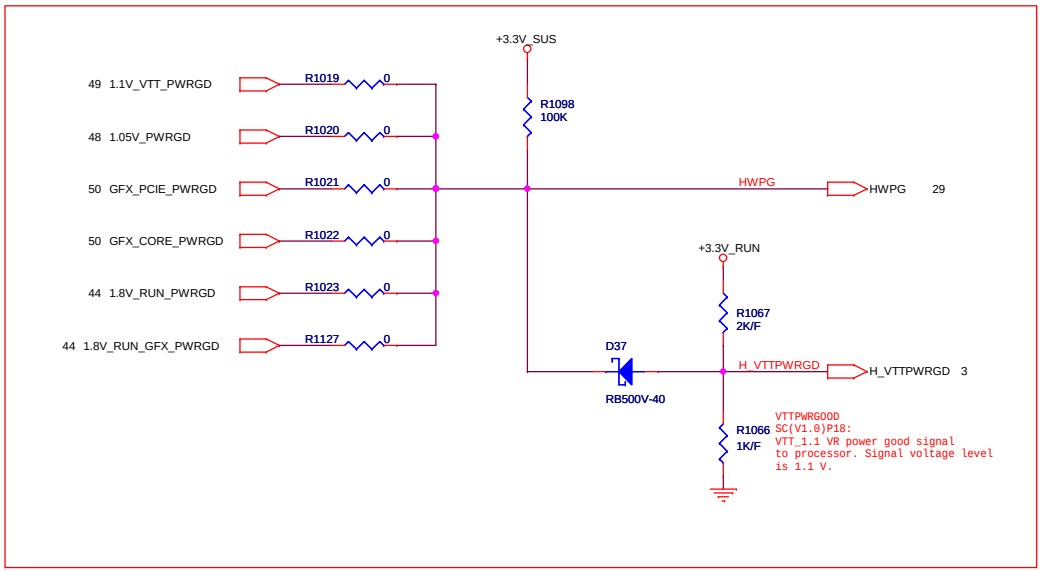
Title	AUDIO CONN	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 40 of 64	

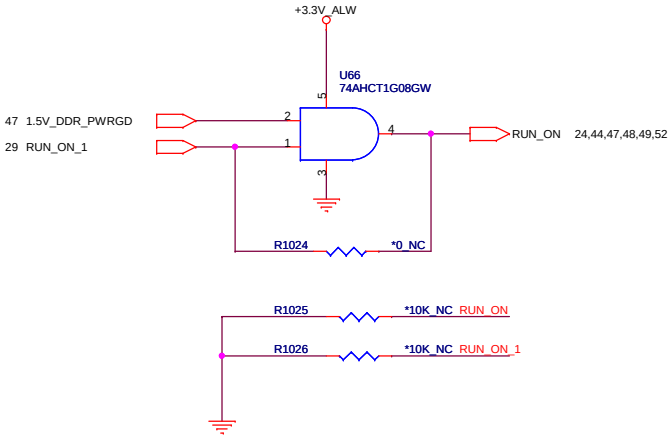


QUANTA COMPUTER			
Title	LAN		
Size	Document Number FM9		Rev 1A
Date:	Thursday, February 26, 2009	Sheet 41 of 64	







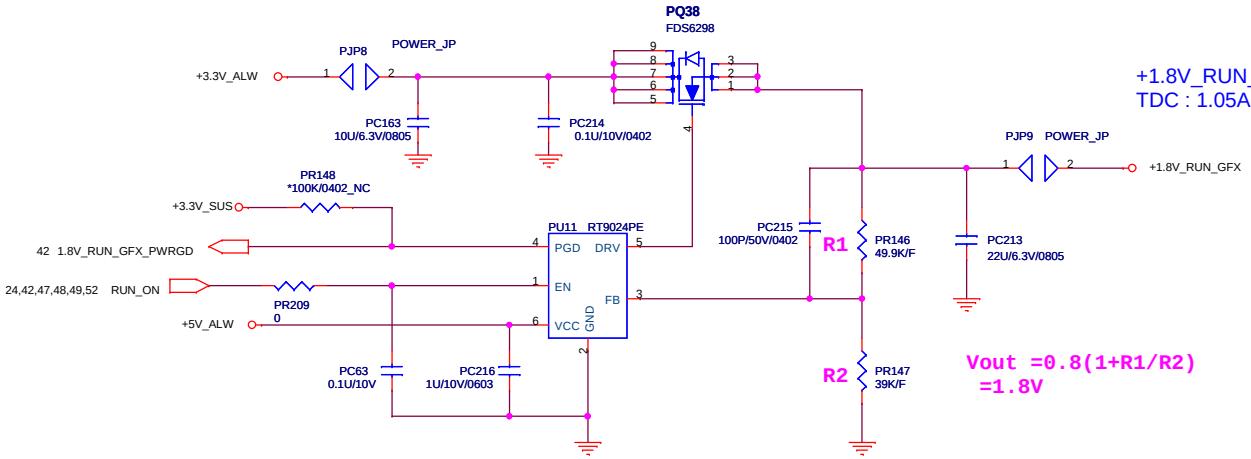


QUANTA COMPUTER

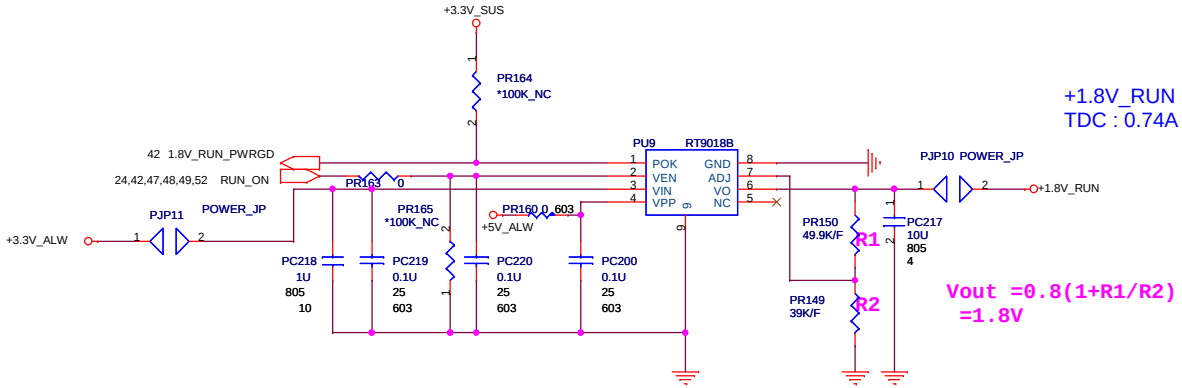
Title	System Reset Circuit	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 42 of 64	

QUANTA COMPUTER

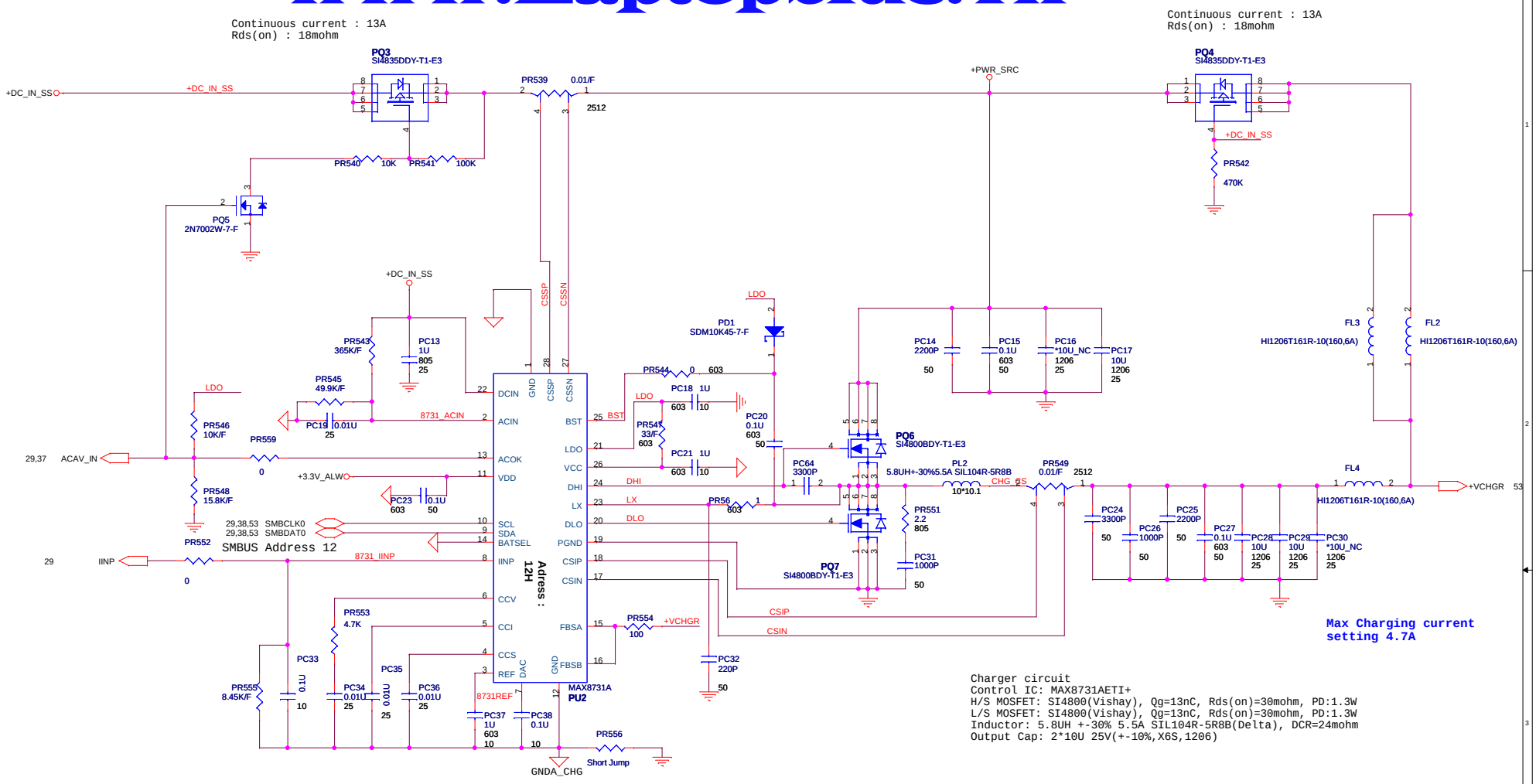
Title	Battery Selector	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 43 of 64	



+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title	+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 44 of 64	



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 45 of 64	

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDS8878(Fairchild), Qg=14nC, Rds(on)=17mohm, PD:2.5W
L/S MOSFET: FDS6680AS(Fairchild), Qg=16nC, Rds(on)=10.5mohm, PD:2.5W
Inductor: 3.3UH +-20% 12.3A FDVE1040-H-3R3M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*220U 10V(+-20%,ESR25,7343)H2.8,ripple current 2449mA

+5V_ALW
Fs=400K
TDC : 5.83A
OCP : 8.33A

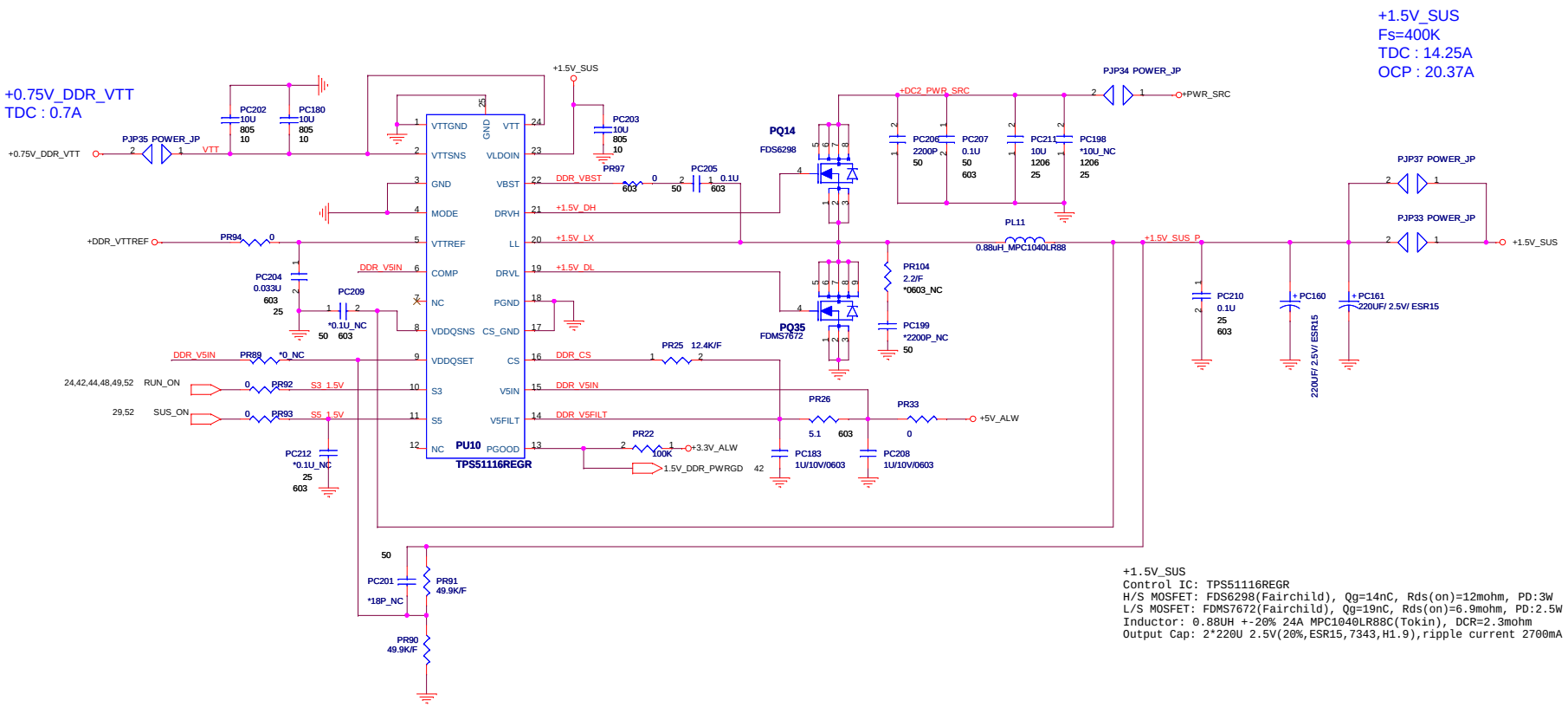
+3.3V_ALW
Fs=300K
TDC : 8.23A
OCP : 11.77A

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: SI4800BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
L/S MOSFET: SI4812BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
Inductor: 3.3UH +-30% 9A SIL1045R-3R3(Delta), DCR=21mohm
Output Cap: 1*220U 10V(+-20%,ESR25,7343)H2.8,ripple current 2449mA

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

QUANTA COMPUTER

Title	3.3V_ALW / 5V_ALW(TPS51427A)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 46 of 64	



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

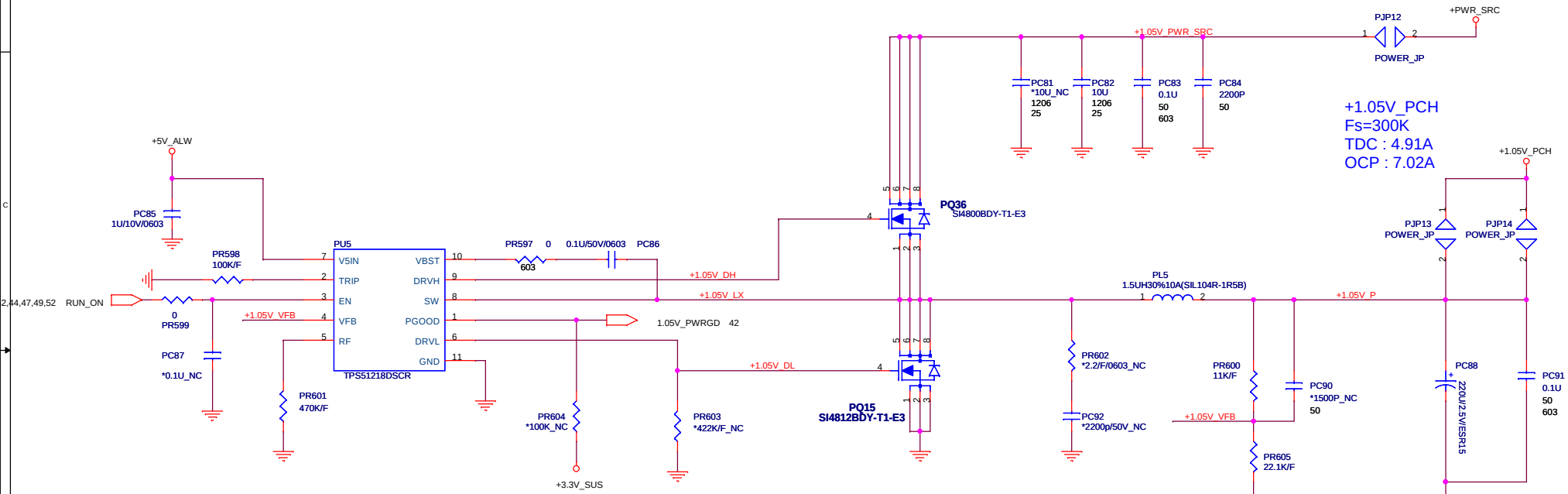
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(TPS51116)		
Size	Document Number FM9		Rev 1A
Date: Thursday, February 26, 2009	Sheet 47 of 64		

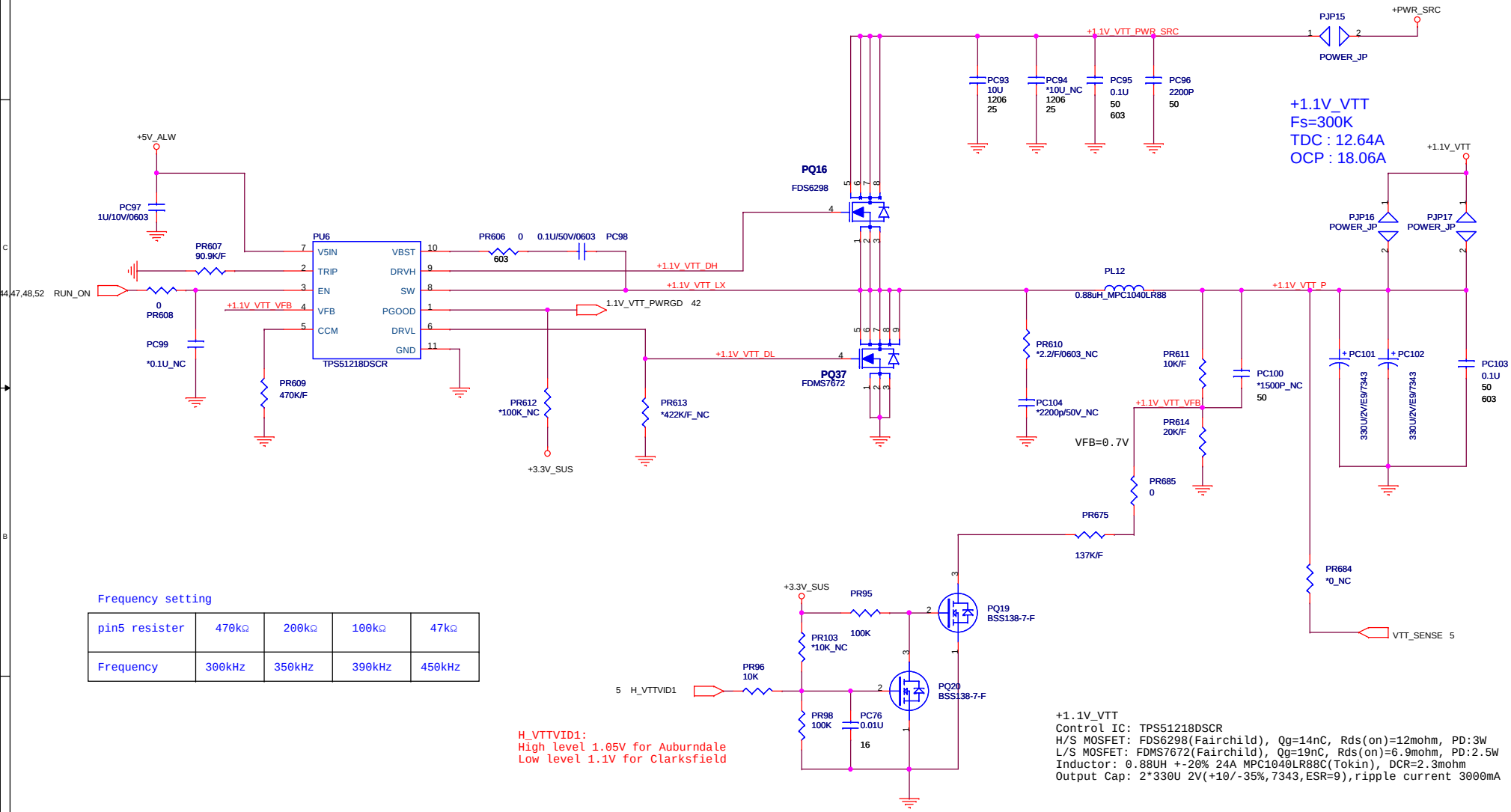


Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: SI4800BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
L/S MOSFET: SI4812BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*220U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	+1.05V_PCH(TPS51218)	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 48 of 64	



Frequency setting

pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

H_VTTVID1:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

+1.1V_VTT
Control IC: TPS51218DSCR
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDMS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.88UH +-20% 24A MPC1040LR88C(Tokin), DCR=2.3mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

Title	+1.1V_VTT(TPS51218)	
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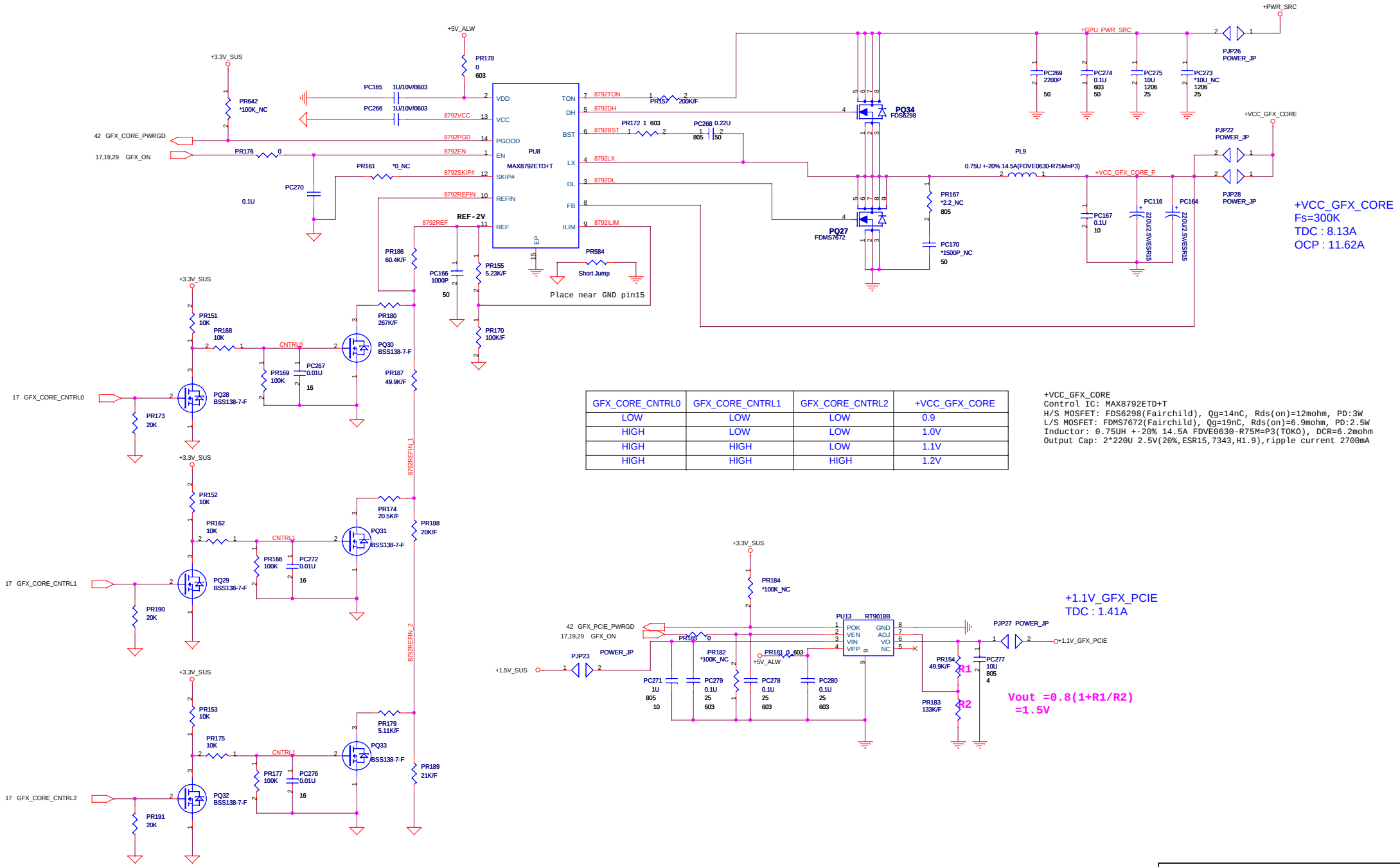

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	0.9
HIGH	LOW	LOW	1.0V
HIGH	HIGH	LOW	1.1V
HIGH	HIGH	HIGH	1.2V

+VCC_GFX_CORE
Control IC: MAX8792ETD+T
H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
L/S MOSFET: FDMS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
Inductor: 0.75UH +-20% 14.5A FDVE0630-R75M=P3(TOKO), DCR=6.2mohm
Output Cap: 2*220U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title	VGA power (MAX8792 & RT9018B)		
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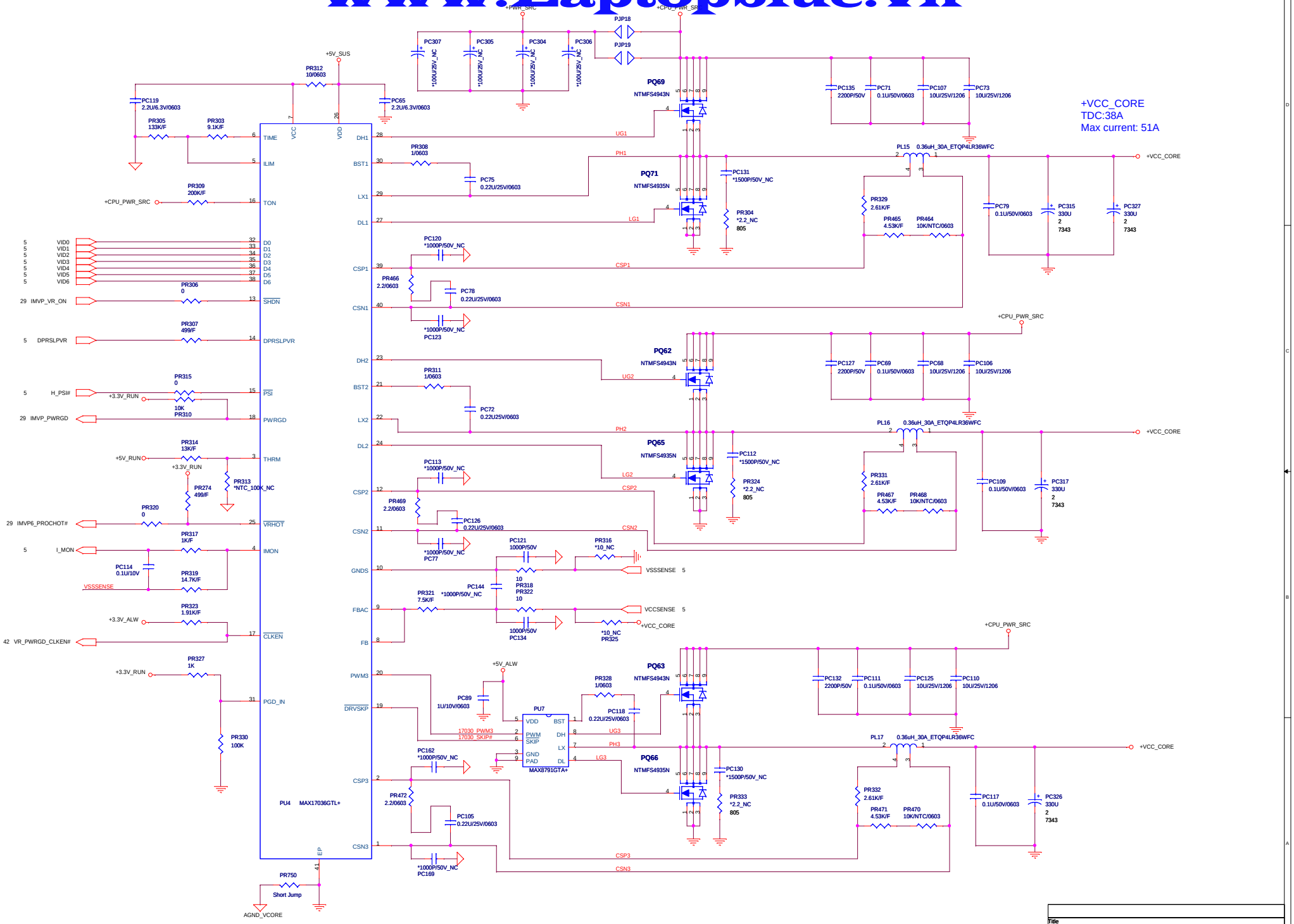
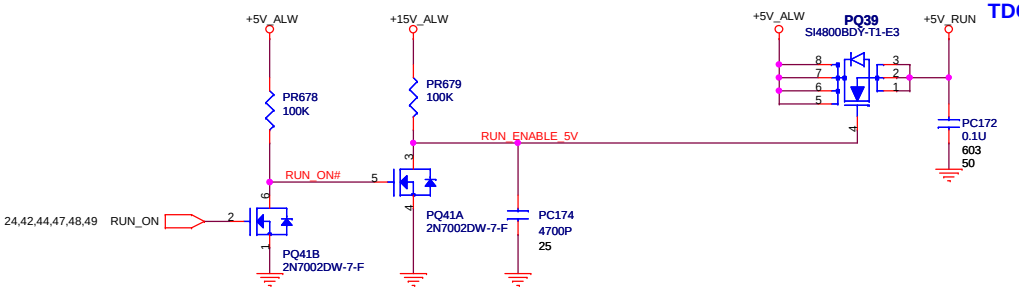
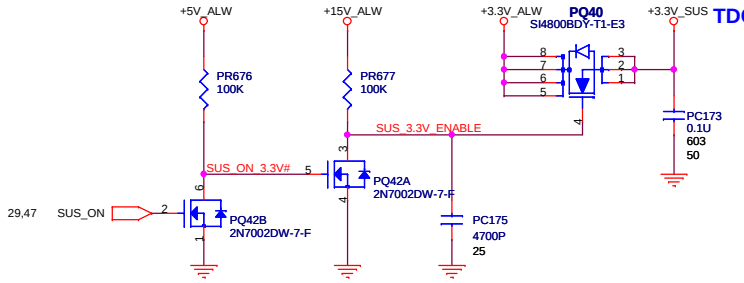


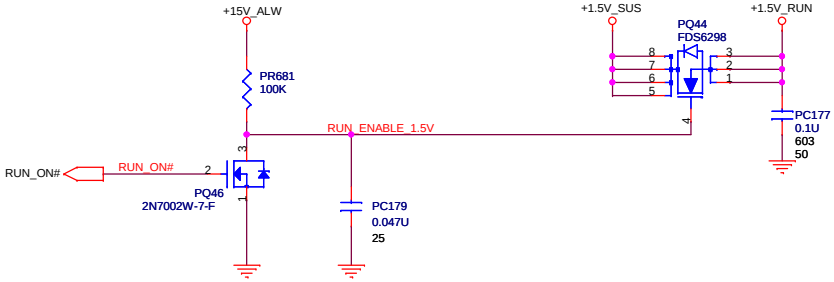
+5V_RUN
TDC : 2.67A



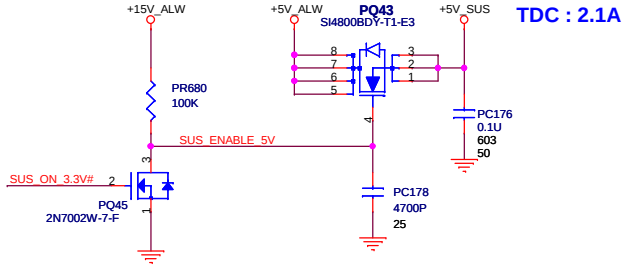
+3.3V_SUS
TDC : 0.46A



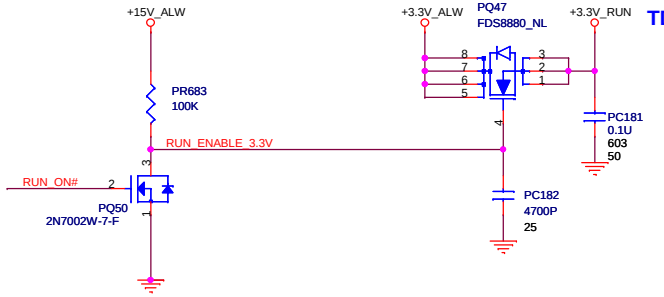
+1.5V_RUN
TDC : 3.74A



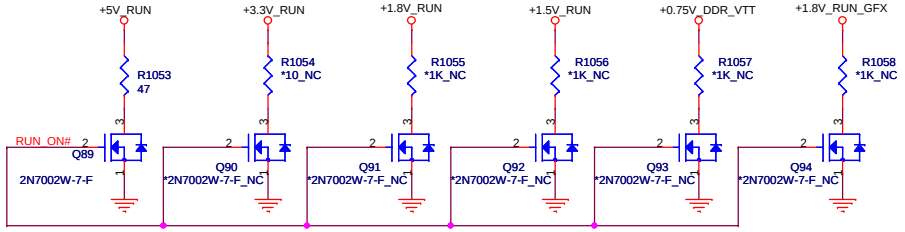
+5V_SUS
TDC : 2.1A

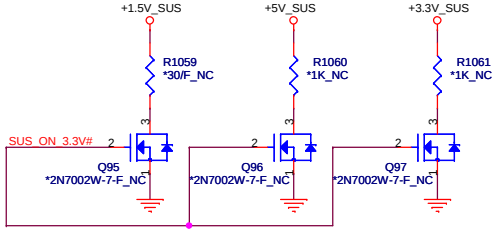


+3.3V_RUN
TDC : 5.93A



Reserve discharge path





QUANTA COMPUTER

Title	RUN / SUS POWER SW	
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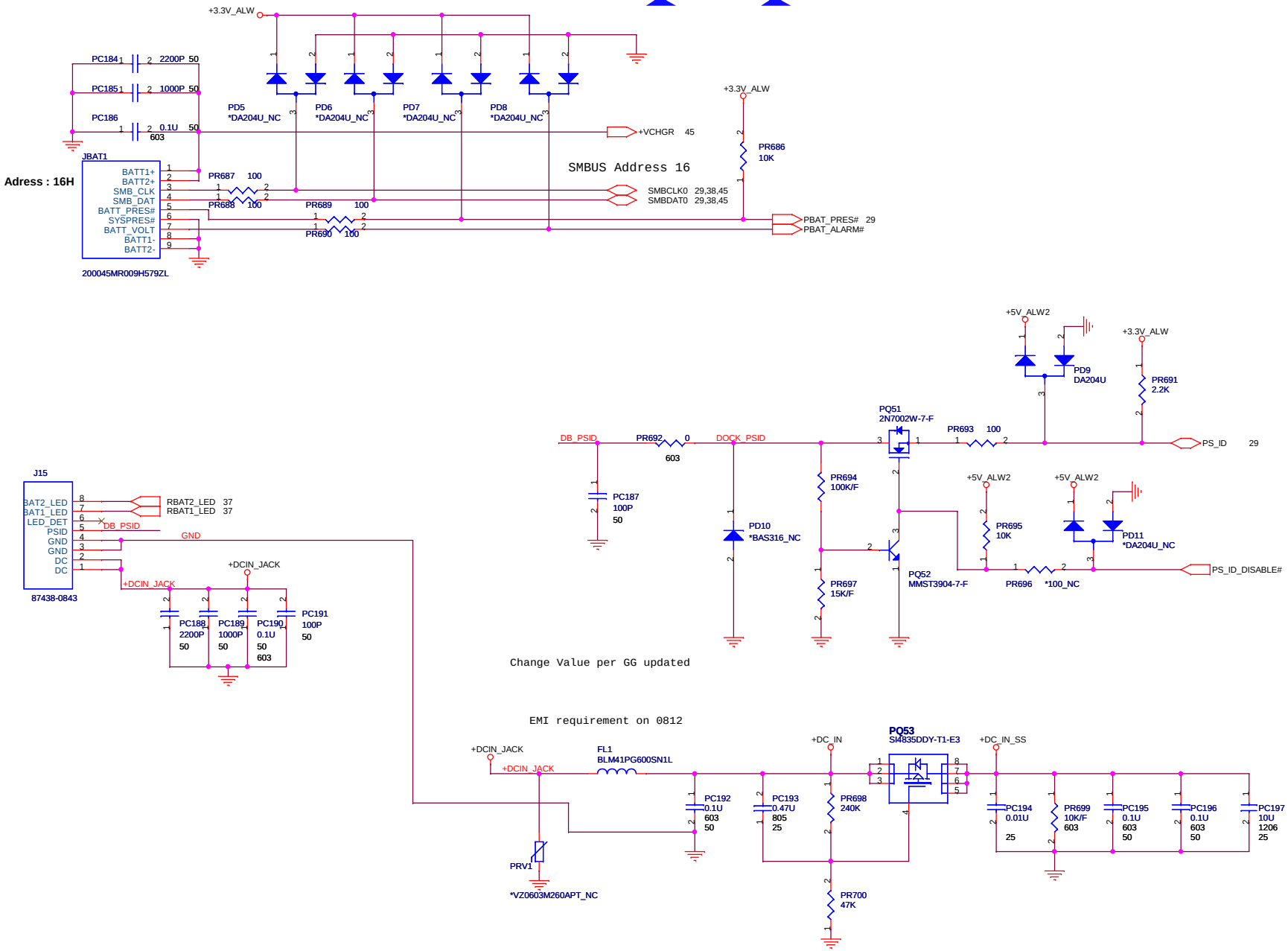
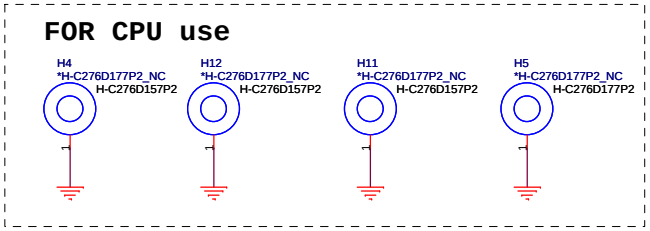
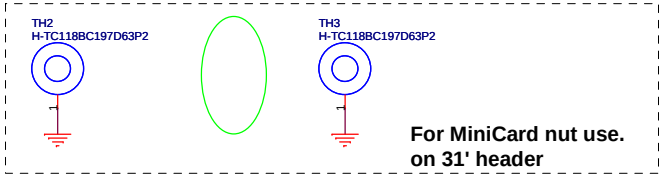
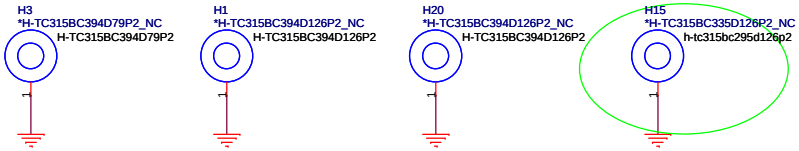


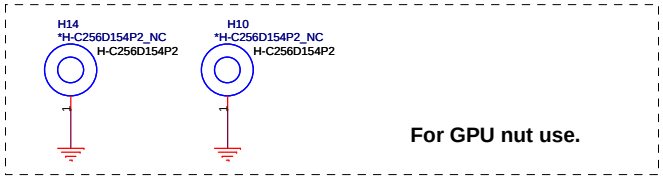
QUANTA COMPUTER

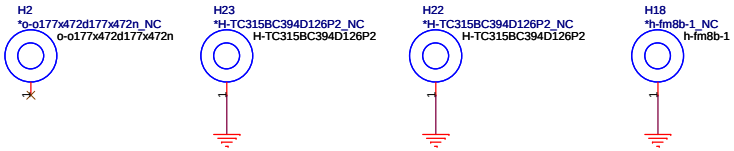
Title	DCIN,BATT CONNECTOR	
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009	Sheet 53 of 64	

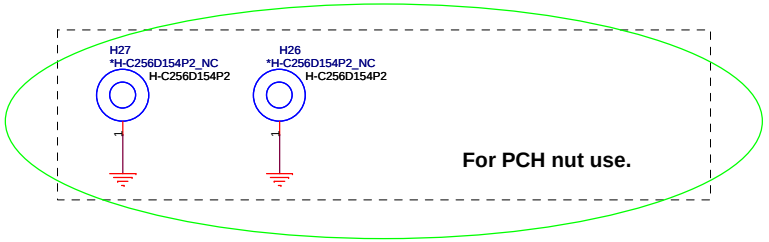


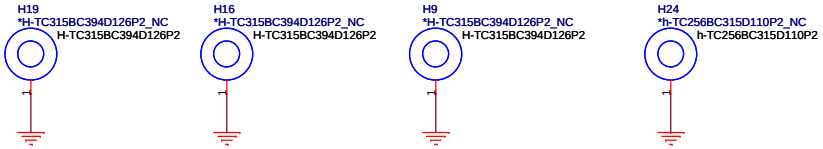


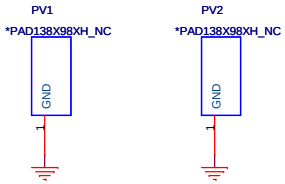


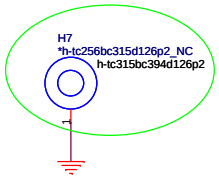


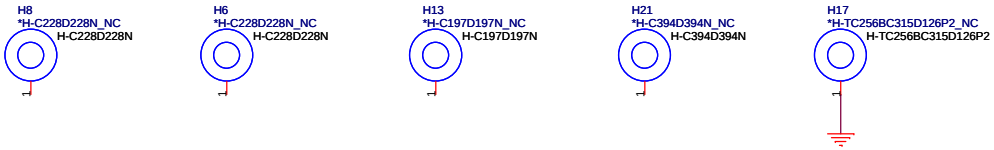












QUANTA COMPUTER

Title	SCREW PAD	
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Reserved for EMI.

QUANTA COMPUTER

Title	EMI CAP	
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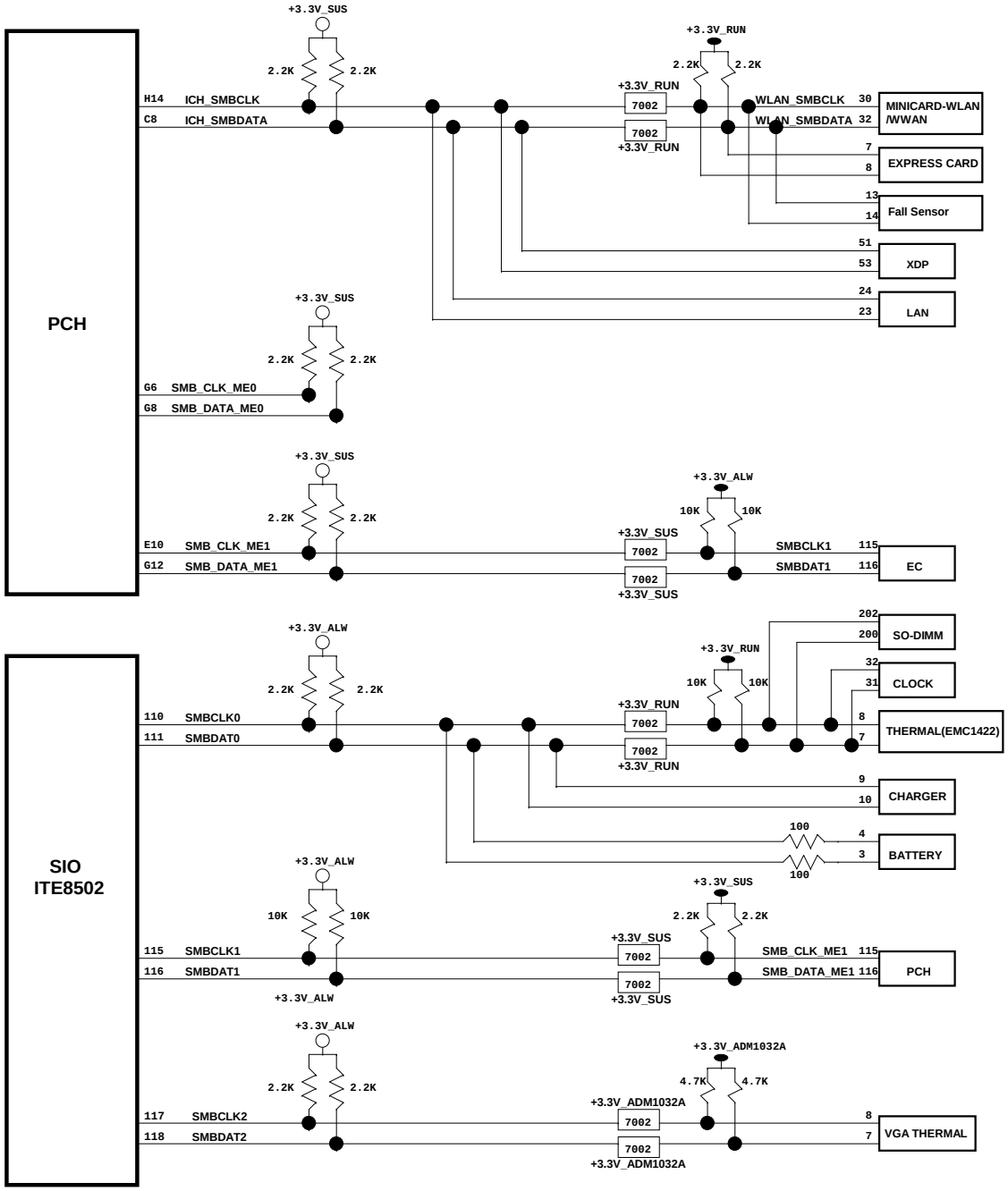

QUANTA COMPUTER

Title	SMBUS BLOCK	
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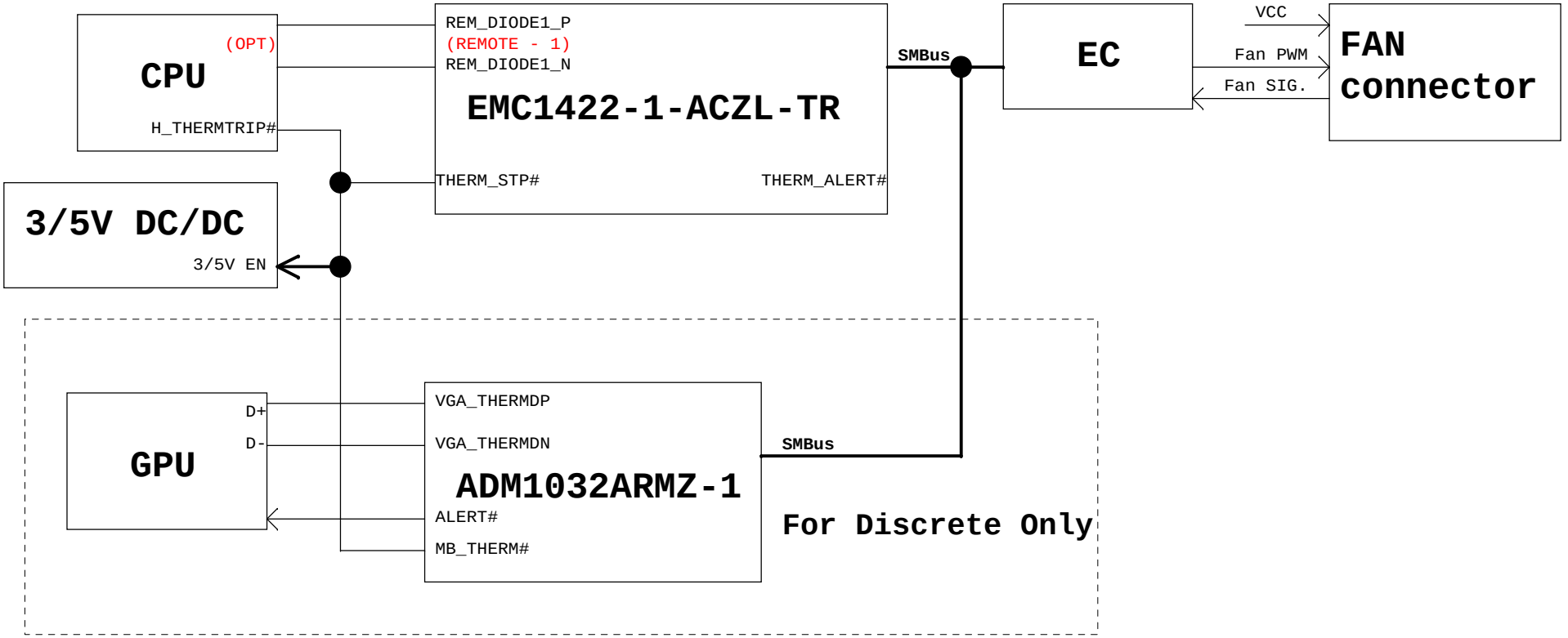

QUANTA COMPUTER

Title	Thermal Map	
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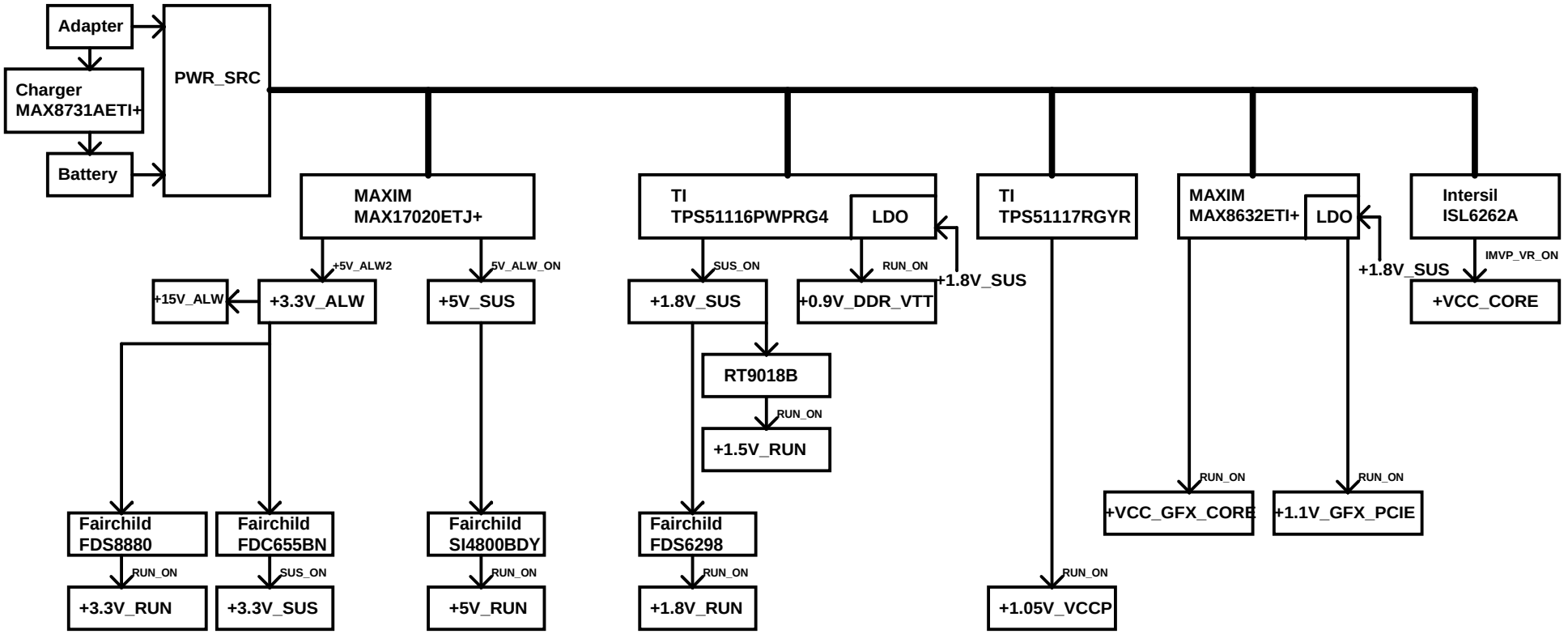
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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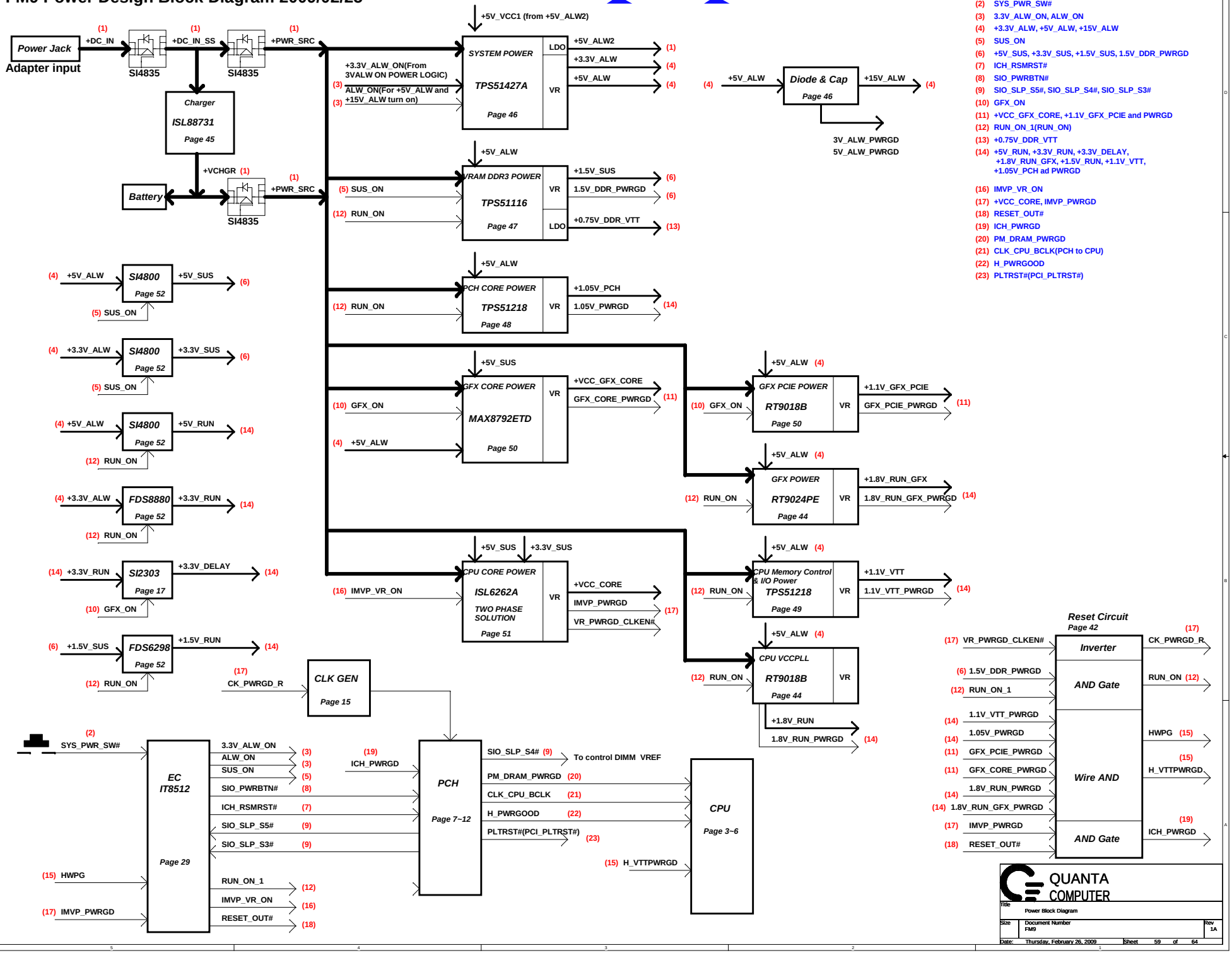
FM9 Power Design Block Diagram 2009/02/25



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

QUANTA COMPUTER

Title	Power Block Diagram	
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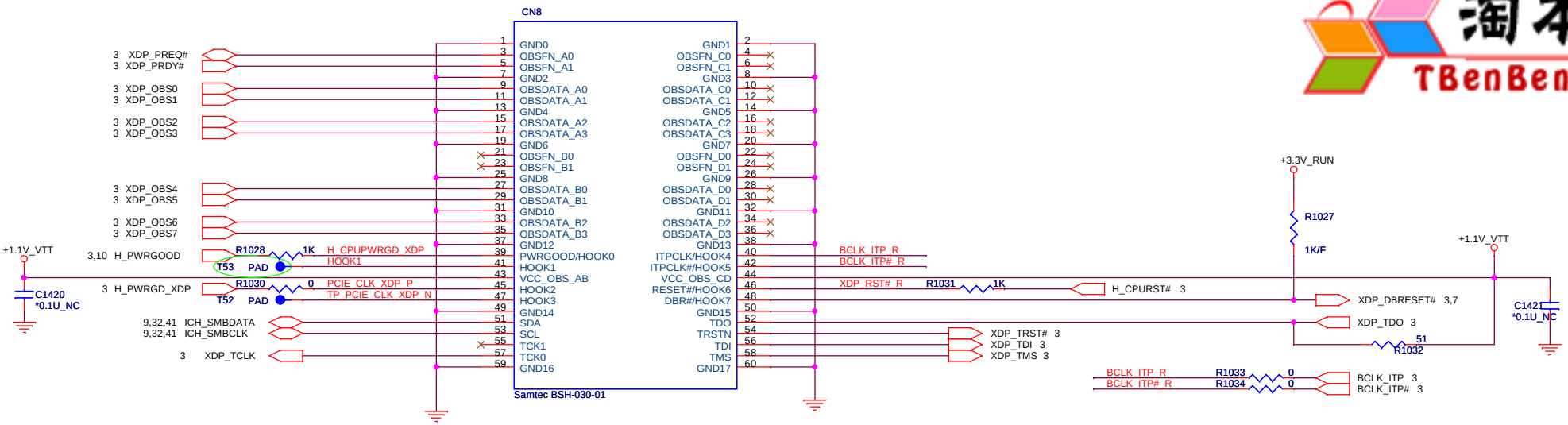

QUANTA COMPUTER		
Title: SMBUS BLOCK		
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