

*FM7B M/B PCB



QUANTA
COMPUTER

Title Schematic Block Diagram

Size	Document Number FM7B
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Rev	1A
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Date: Monday, July 21, 2008

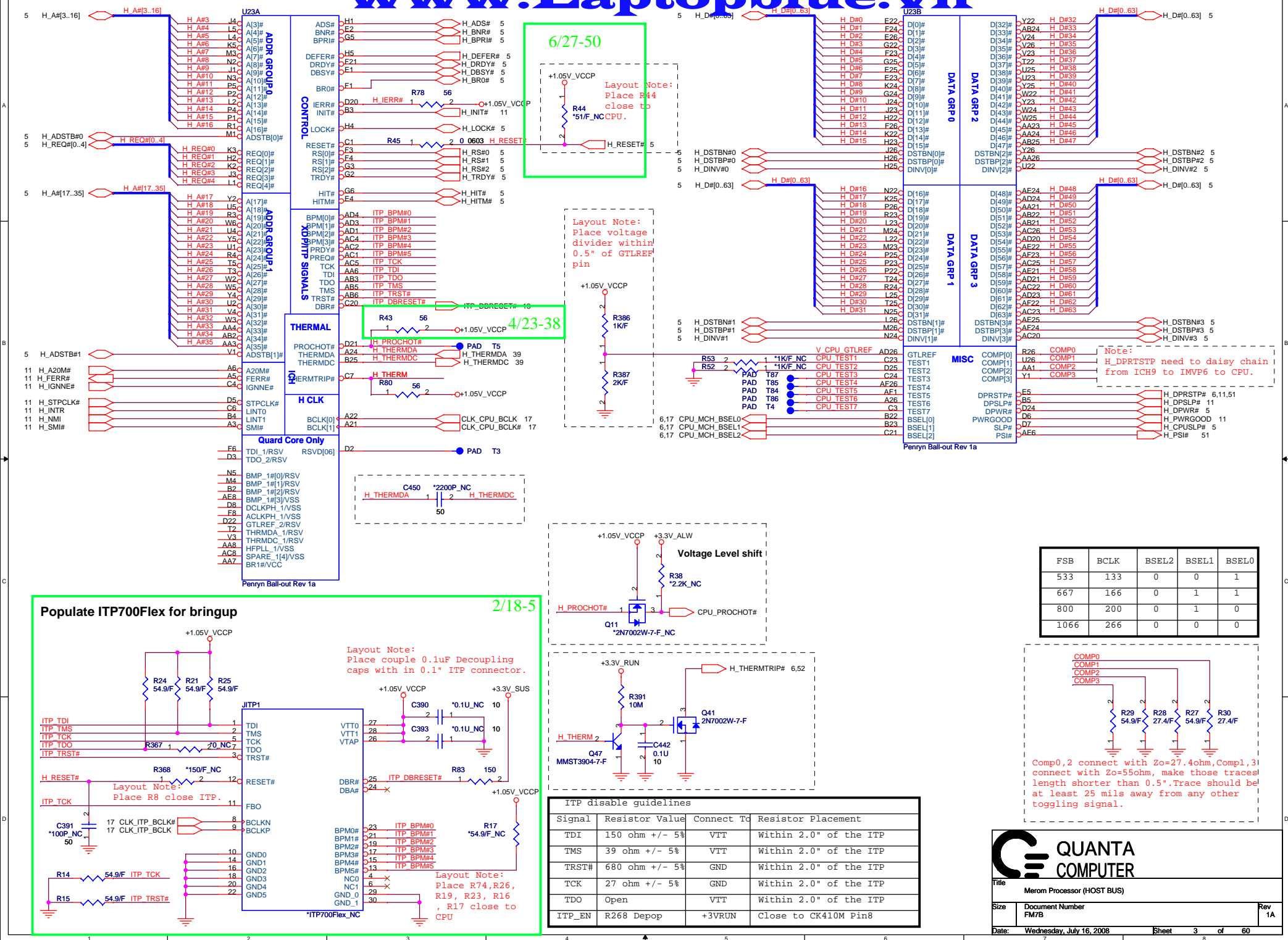
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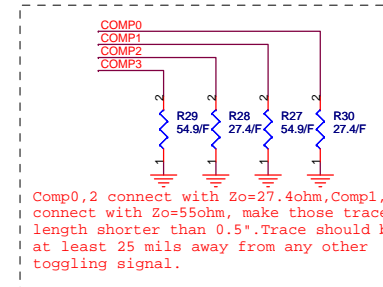
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
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15-16	DDRII SO-DIMM(200P)
17	Clock Generator
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24	CRT Conn
25	SATA Conn
26-27	CARD READER/Conn & 1394
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POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54,56	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

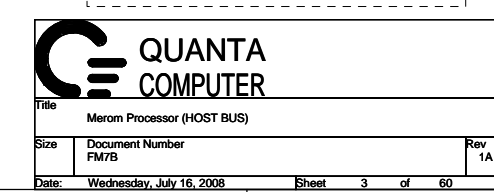
GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

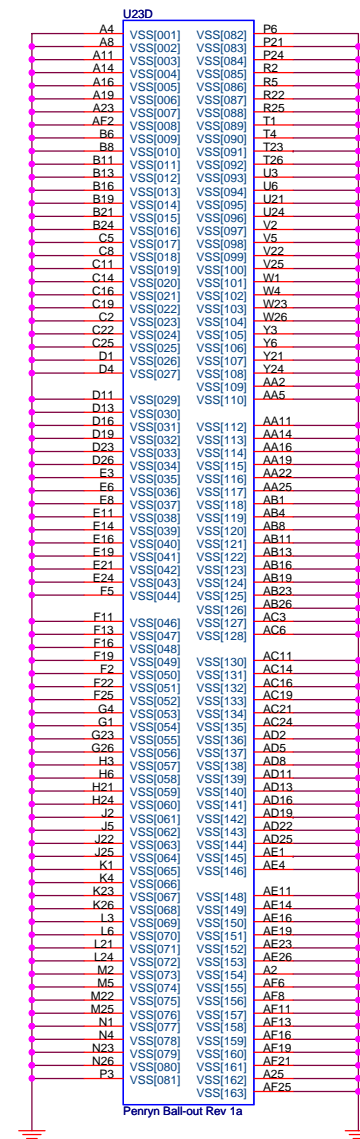
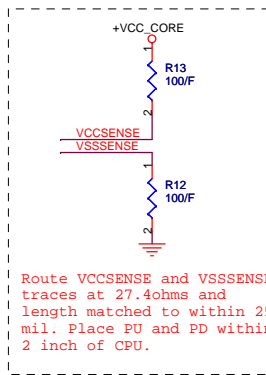
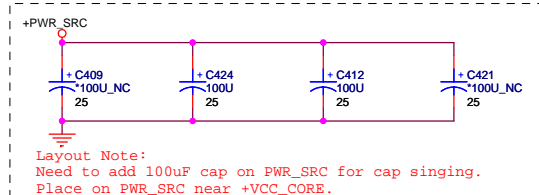
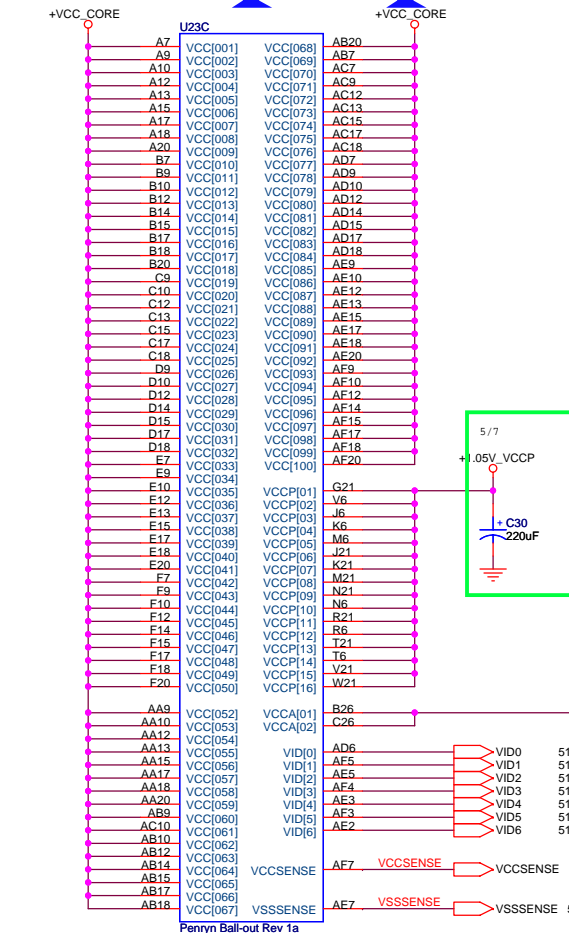
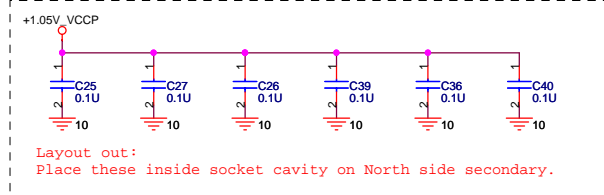
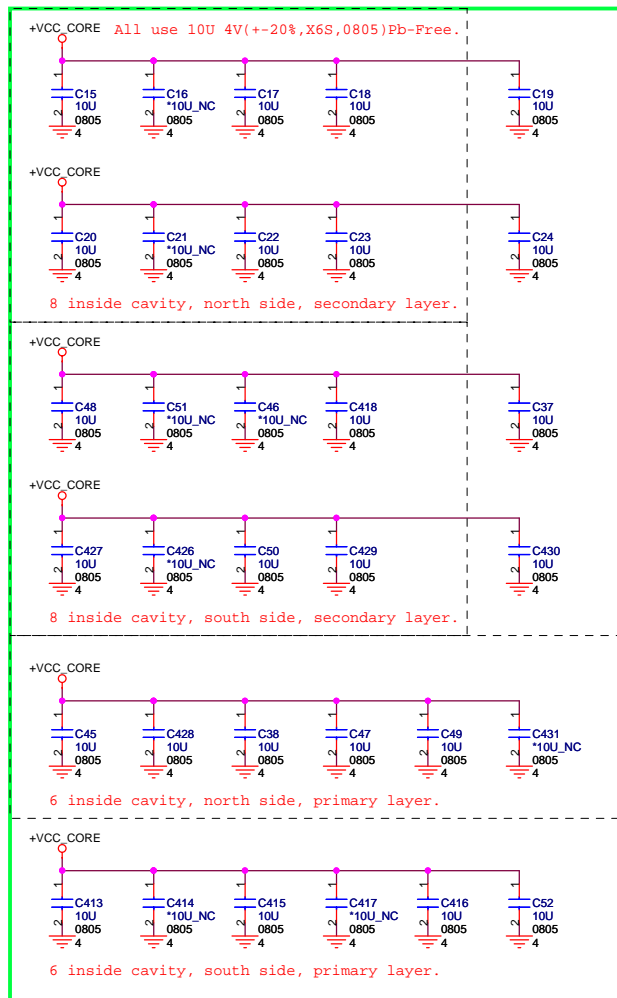


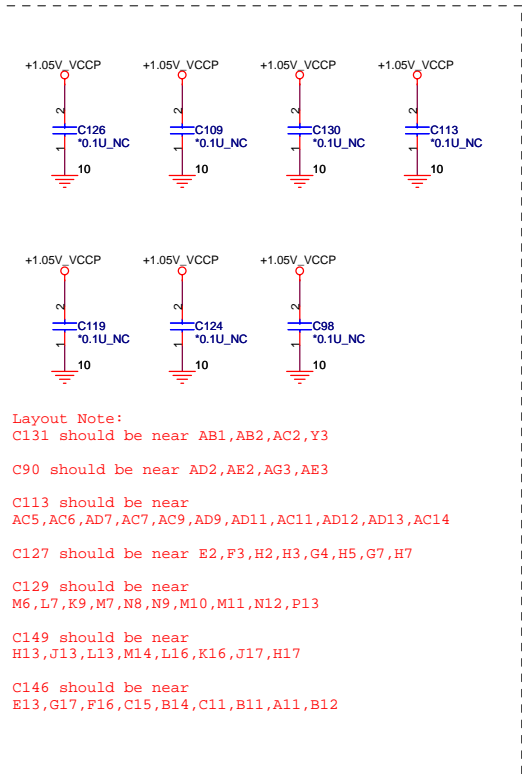
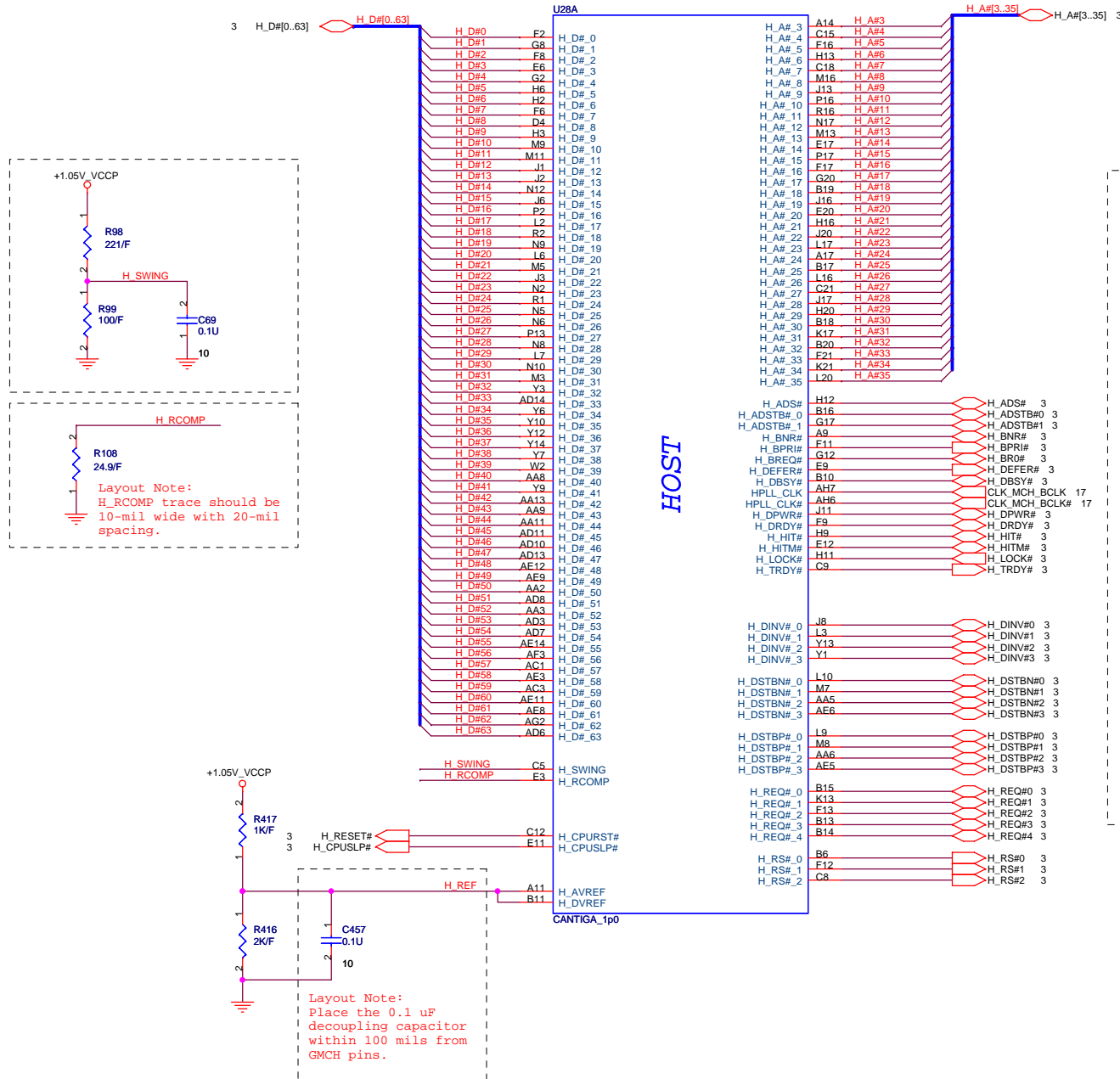
FSB	BCLK	BSEL2	BSEL1	BSEL
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

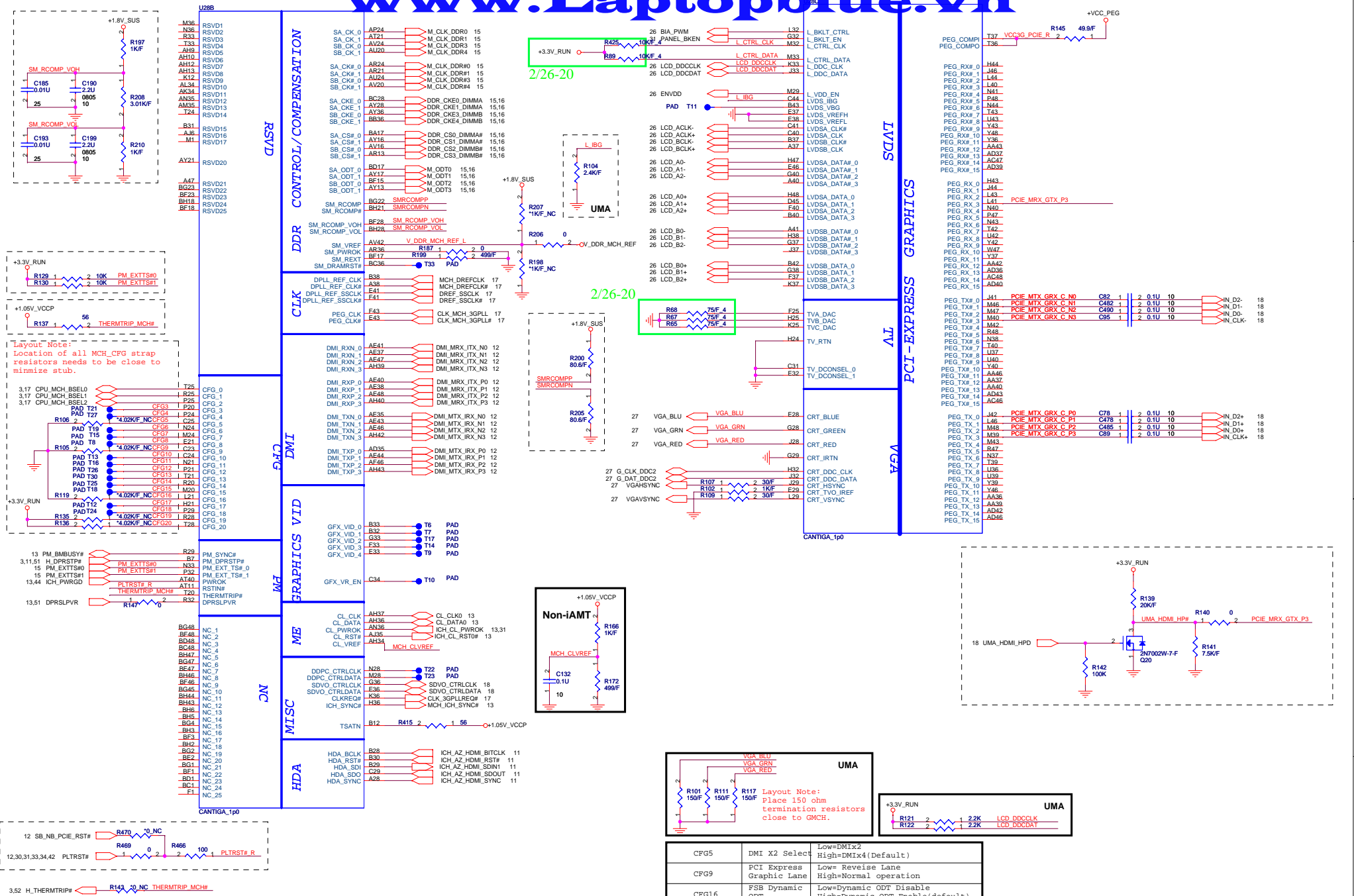


ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8









CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIex1 is operational (defaults) High=SDVO and PCIex1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

15 DDR_A_D[0..63]

DDR A D0	AJ38	SA_DQ_0
DDR A D1	AJ41	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	AJ36	SA_DQ_4
DDR A D5	AJ40	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AJ40	SA_DQ_10
DDR A D11	AT38	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AJ44	SA_DQ_14
DDR A D15	AJ42	SA_DQ_15
DDR A D16	AY39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BD41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AY38	SA_DQ_28
DDR A D29	BD36	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AU11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AU13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BD9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AU10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AU5	SA_DQ_52
DDR A D53	AU6	SA_DQ_53
DDR A D54	AT5	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	AJ9	SA_DQ_58
DDR A D59	AJ8	SA_DQ_59
DDR A D60	AN12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

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DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2

SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21. DDR A BS0
BG18. DDR A BS1
AT25. DDR A BS2

BB20. DDR A RAS#
BD20. DDR A CAS#
AY20. DDR A WE#

AM37. DDR A DM0
AT41. DDR A DM1
AY41. DDR A DM2
AU39. DDR A DM3
BB12. DDR A DM4
AY6. DDR A DM5
AT7. DDR A DM6
AJ5. DDR A DM7

AJ44. DDR A DQS0
AT44. DDR A DQS1
BA43. DDR A DQS2
BC37. DDR A DQS3
AW12. DDR A DQS4
BC8. DDR A DQS5
AU8. DDR A DQS6
AM7. DDR A DQS7

AJ43. DDR A DQS#0
AT43. DDR A DQS#1
BA44. DDR A DQS#2
BD37. DDR A DQS#3
AY12. DDR A DQS#4
BD8. DDR A DQS#5
AU9. DDR A DQS#6
AM8. DDR A DQS#7

BA21. DDR A MA0
BC24. DDR A MA1
BG24. DDR A MA2
BH24. DDR A MA3
BG25. DDR A MA4
BA24. DDR A MA5
BD24. DDR A MA6
BG27. DDR A MA7
BF25. DDR A MA8
AW24. DDR A MA9
BC21. DDR A MA10
BG26. DDR A MA11
BH26. DDR A MA12
BH17. DDR A MA13
AY25. DDR A MA14

15 DDR_B_D[0..63]

DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	AJ48	SB_DQ_5
DDR B D6	AM49	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AU47	SB_DQ_8
DDR B D9	AJ46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	BA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	BC46	SB_DQ_16
DDR B D17	BC44	SB_DQ_17
DDR B D18	BG43	SB_DQ_18
DDR B D19	BF43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BF40	SB_DQ_22
DDR B D23	BF41	SB_DQ_23
DDR B D24	BG38	SB_DQ_24
DDR B D25	BF38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BG39	SB_DQ_29
DDR B D30	BG34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BG8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BF11	SB_DQ_37
DDR B D38	BF8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BF6	SB_DQ_44
DDR B D45	BF5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AU3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	AJ1	SB_DQ_58
DDR B D59	AH1	SB_DQ_59
DDR B D60	AM2	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	AJ3	SB_DQ_63

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DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2

SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16. DDR B BS0
BB17. DDR B BS1
BB33. DDR B BS2

AU17. DDR B RAS#
BG16. DDR B CAS#
BF14. DDR B WE#

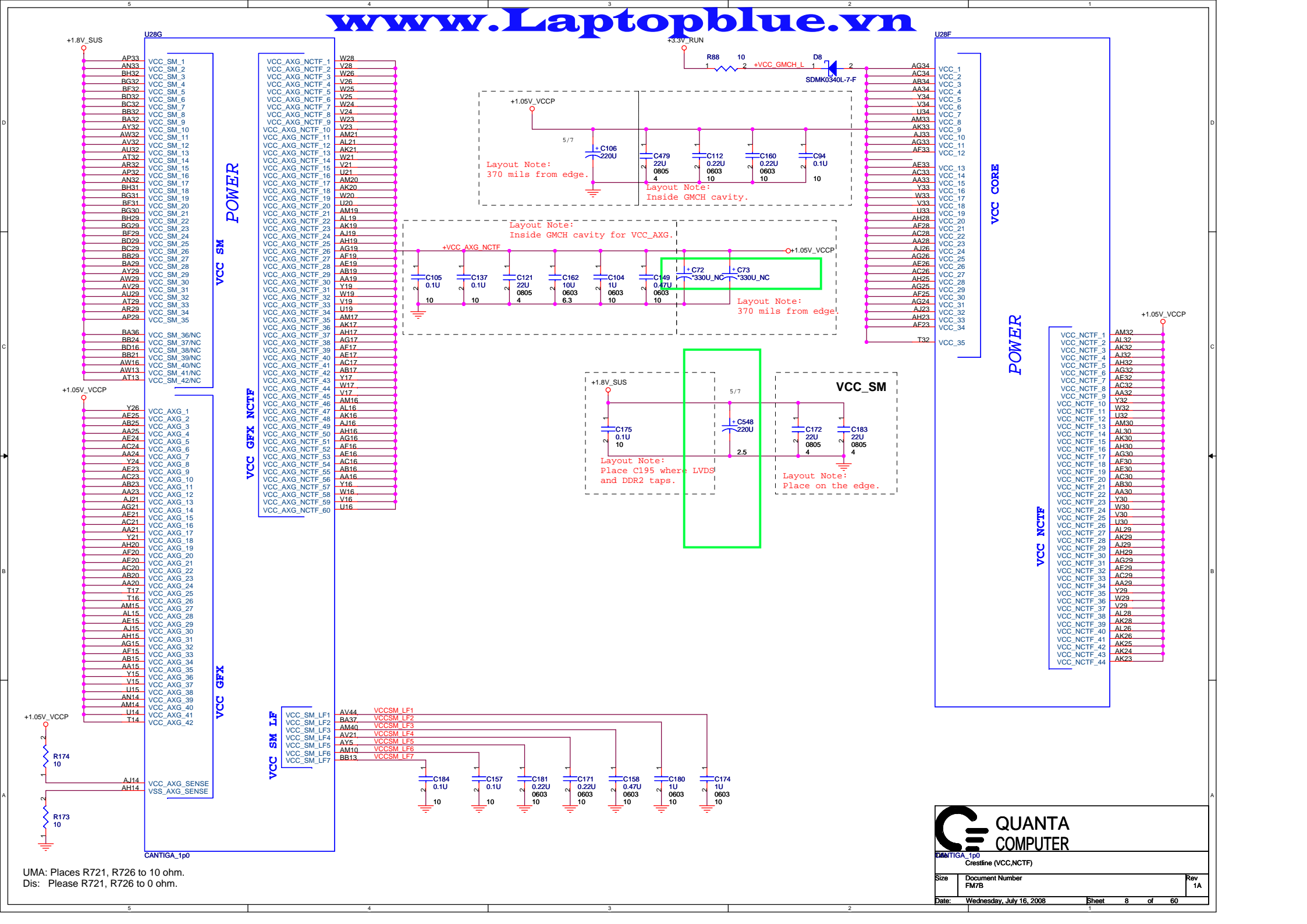
AM47. DDR B DM0
AY47. DDR B DM1
BD40. DDR B DM2
BF35. DDR B DM3
BG11. DDR B DM4
BA3. DDR B DM5
AP1. DDR B DM6
AK2. DDR B DM7

AL47. DDR B DQS0
AY48. DDR B DQS1
BG41. DDR B DQS2
BG37. DDR B DQS3
BH9. DDR B DQS4
BH2. DDR B DQS5
AU1. DDR B DQS6

AN6. DDR B DQS7
AL46. DDR B DQS#0
AY47. DDR B DQS#1
BH41. DDR B DQS#2
BH37. DDR B DQS#3
BG9. DDR B DQS#4
BC2. DDR B DQS#5
AT2. DDR B DQS#6
AN5. DDR B DQS#7

AV17. DDR B MA0
BA25. DDR B MA1
BC25. DDR B MA2
AU25. DDR B MA3
AW25. DDR B MA4
BB28. DDR B MA5
AU28. DDR B MA6
AW28. DDR B MA7
AT33. DDR B MA8
BD33. DDR B MA9
BB16. DDR B MA10
AW33. DDR B MA11
AY33. DDR B MA12
BH15. DDR B MA13
AU33. DDR B MA14



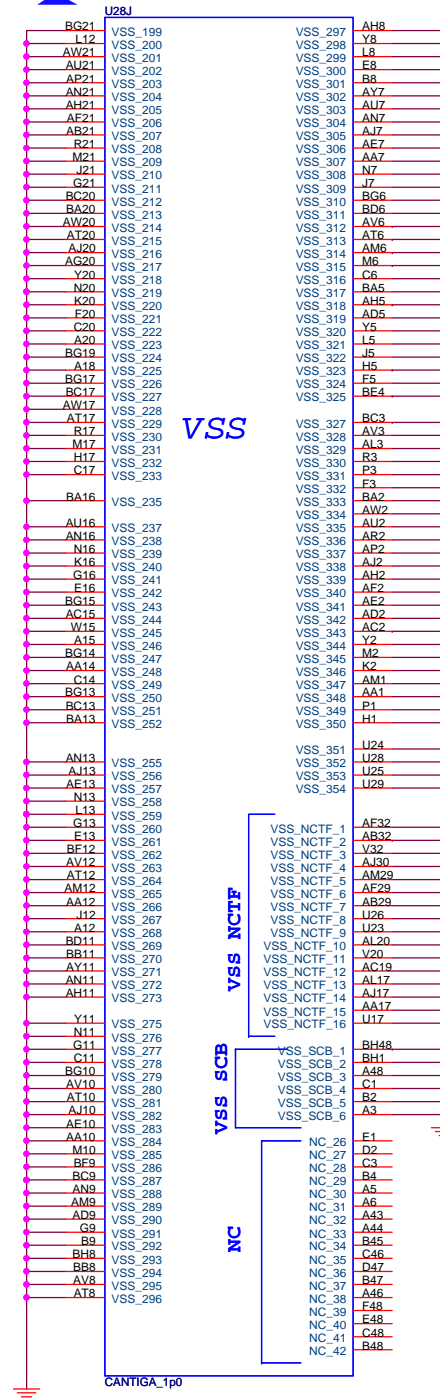
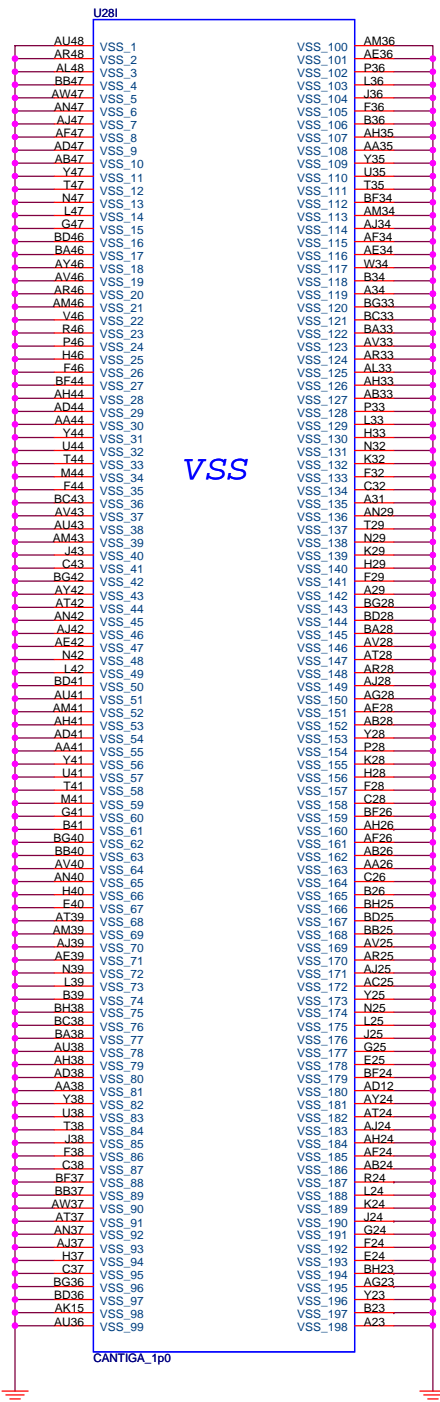


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UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.

QUANTA COMPUTER

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VSS

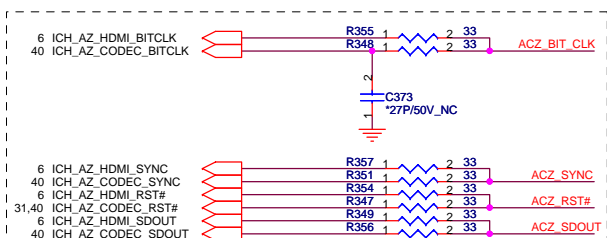
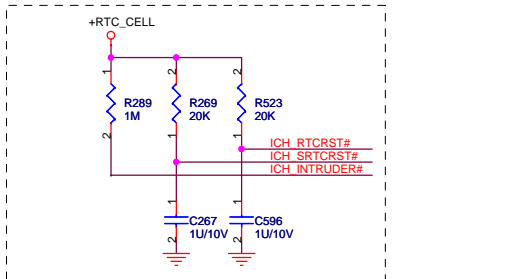
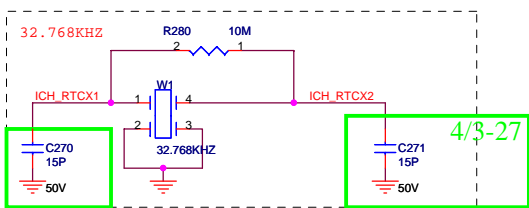
VSS NCTF

VSS SCB

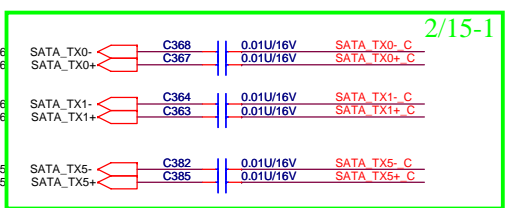
NC



Title			
Crestline (VSS)			
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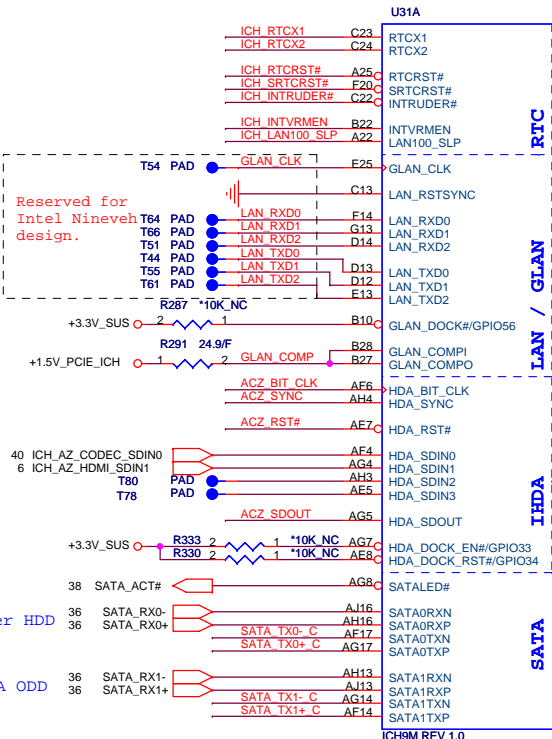


Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



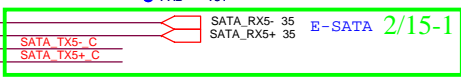
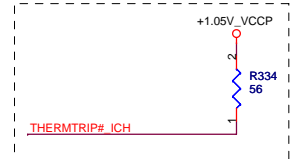
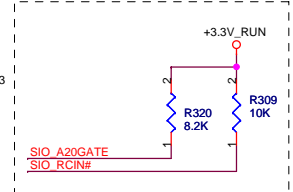
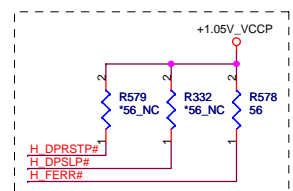
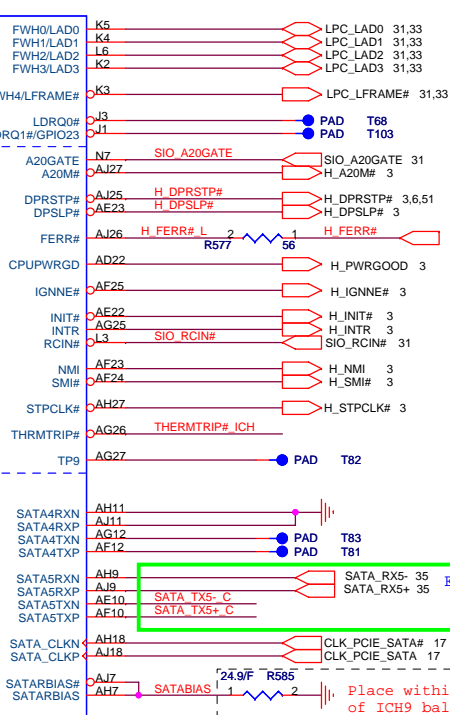
Master HDD

SATA ODD

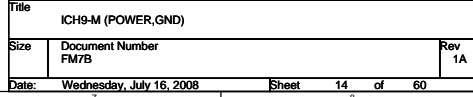


ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)	

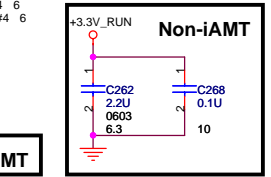
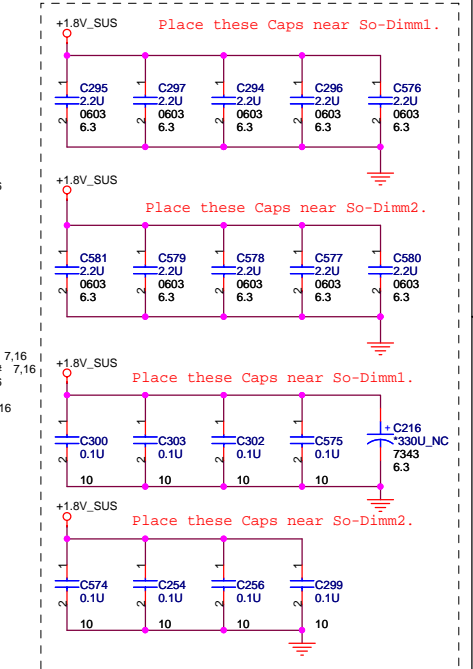
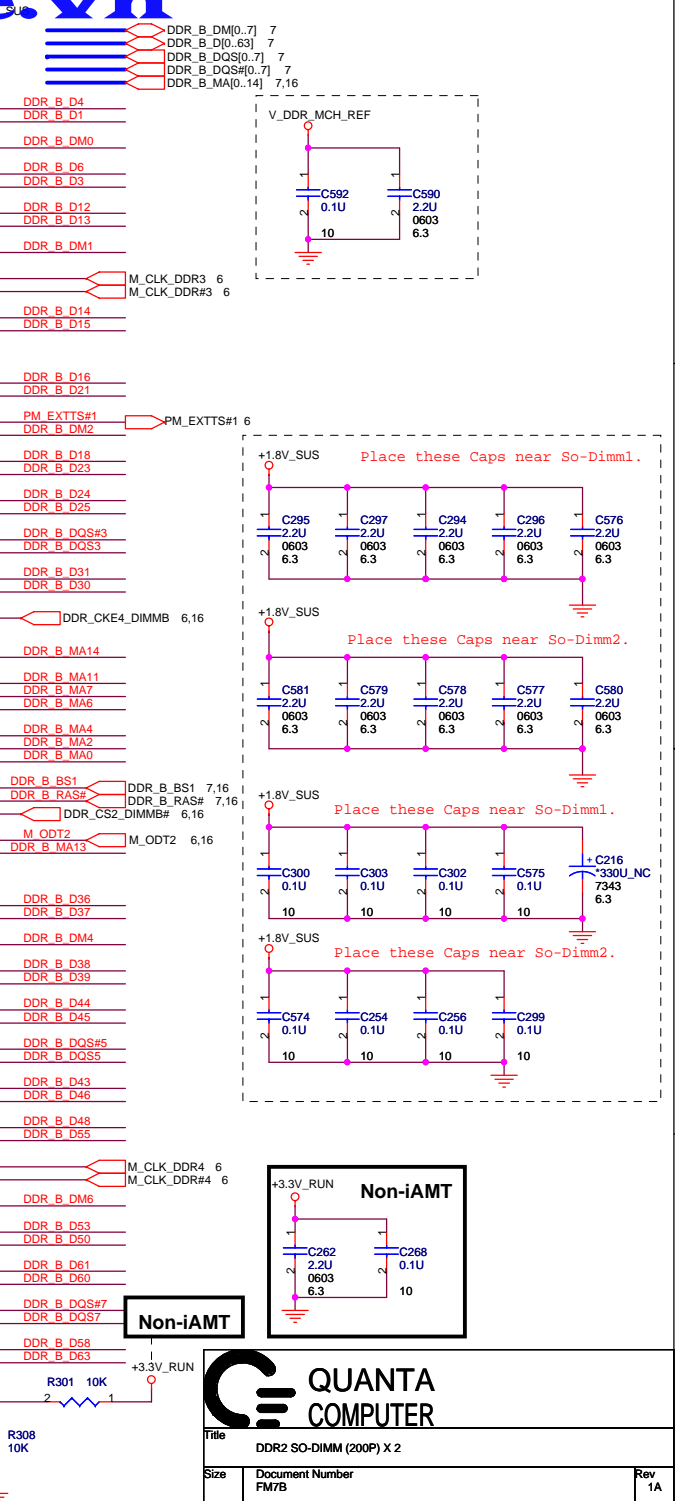
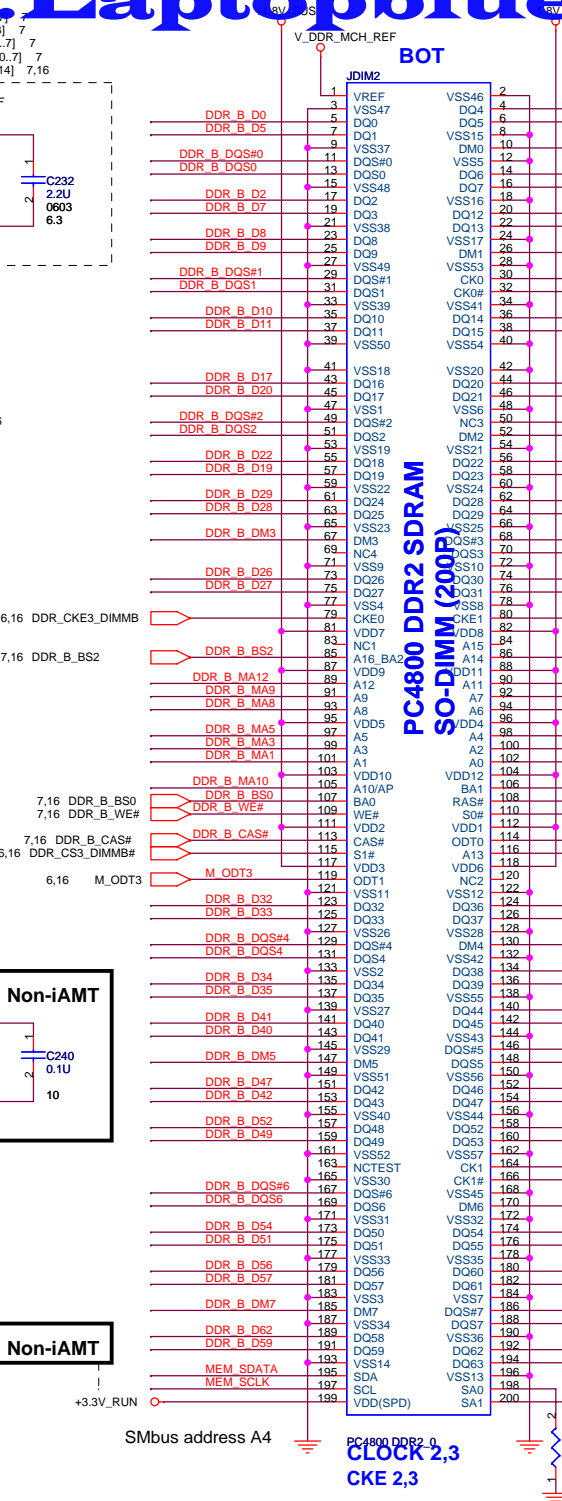
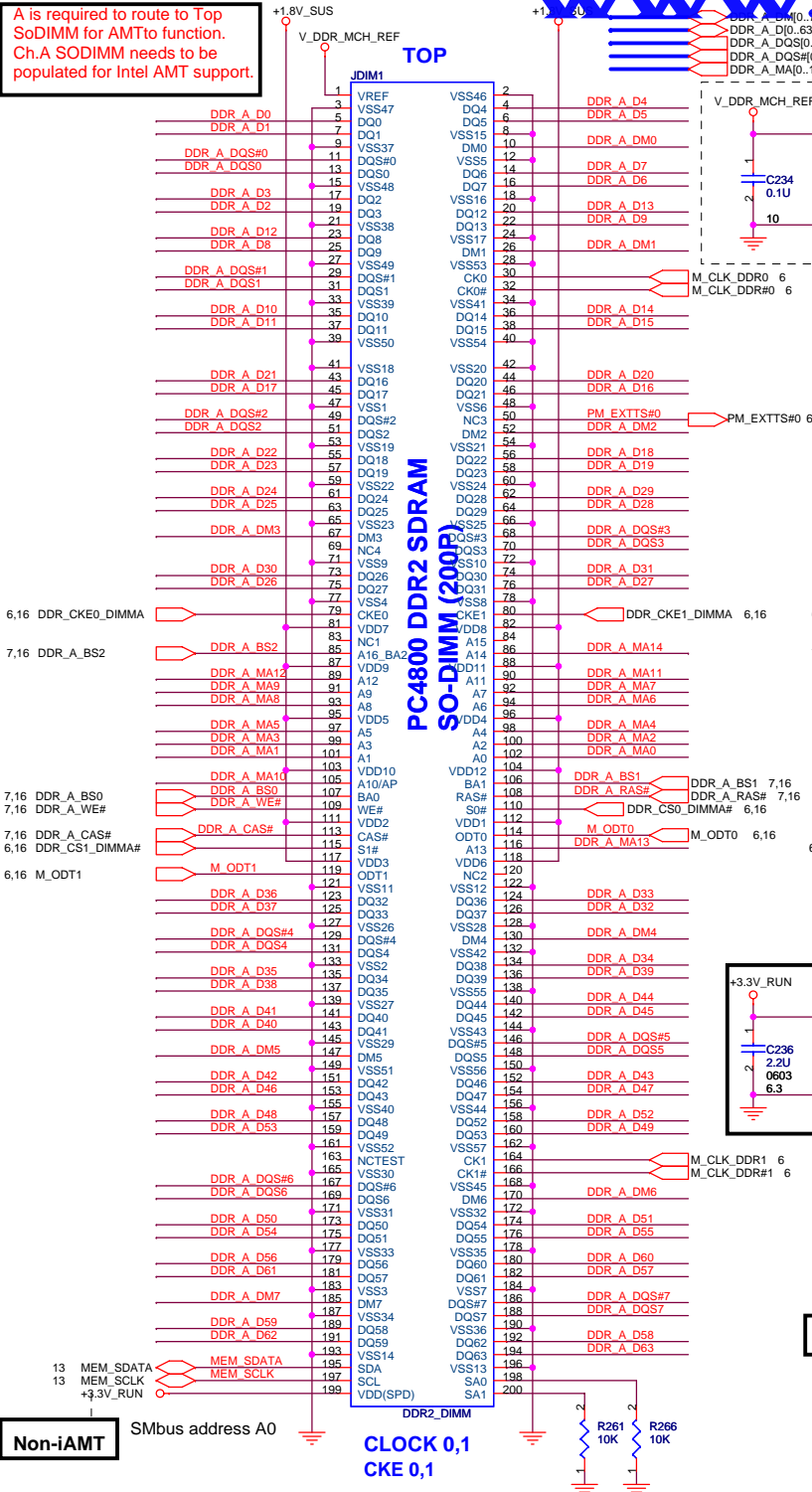
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)	



XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



QUANTA COMPUTER

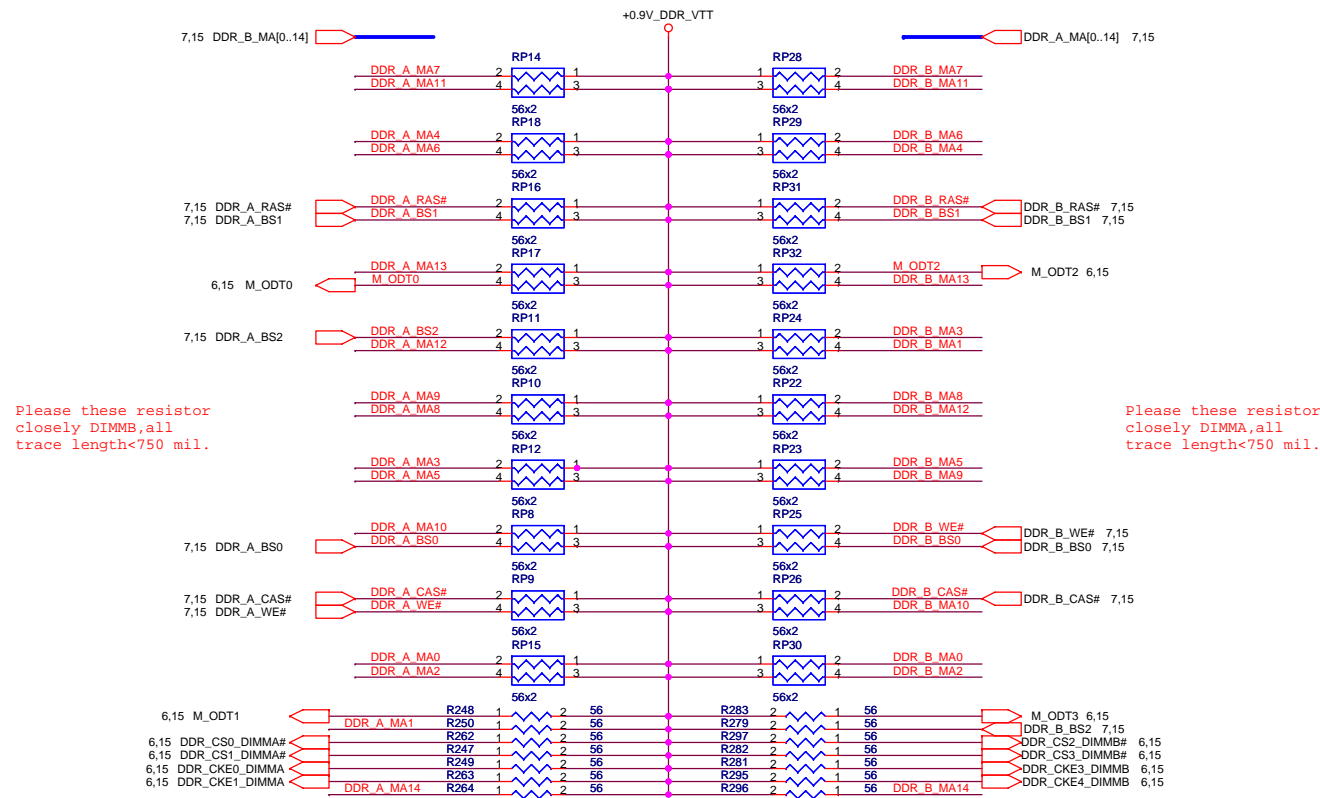
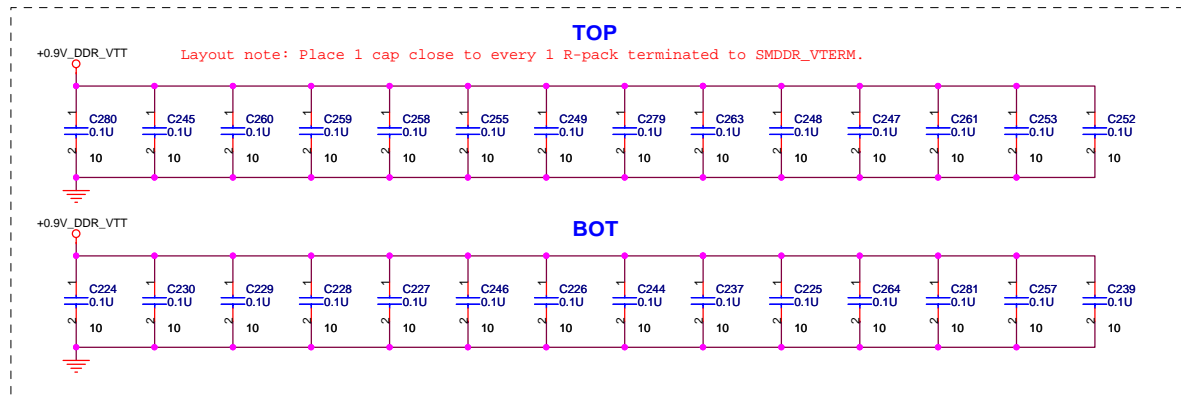
Title: DDR2 SO-DIMM (200P) X 2

Size: Document Number FM7B

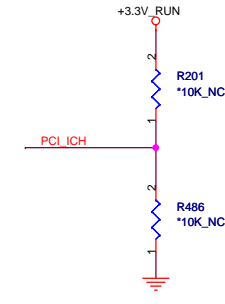
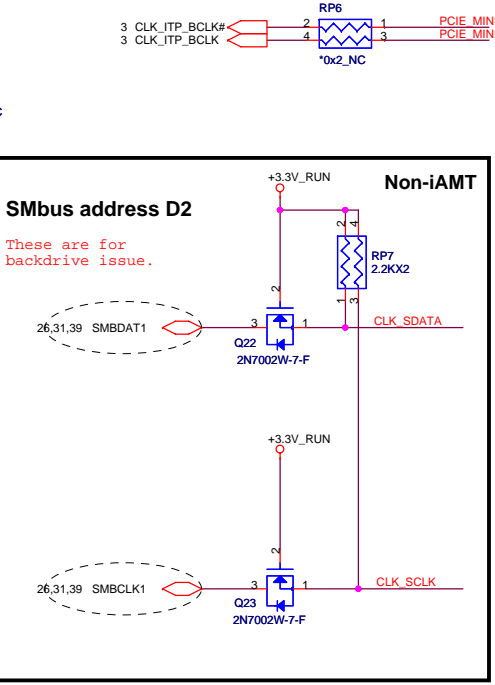
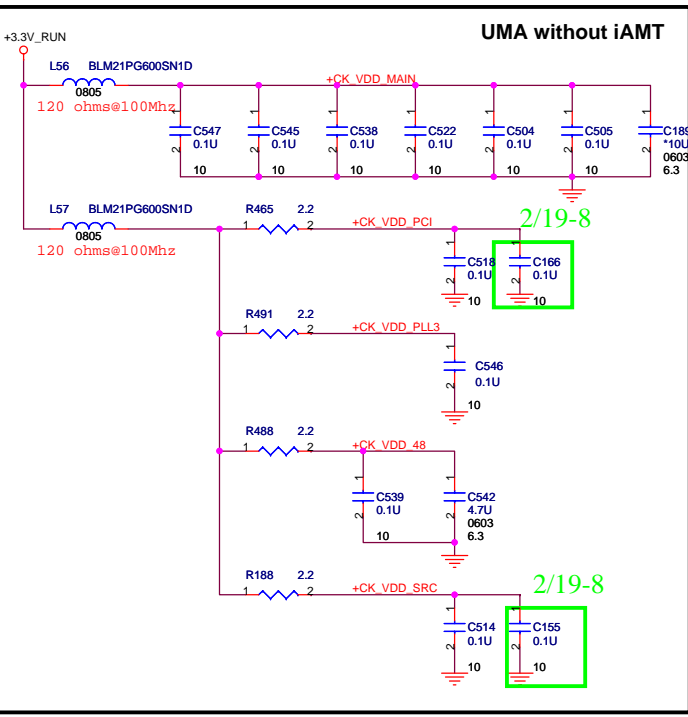
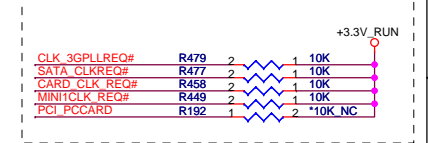
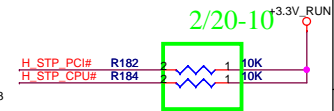
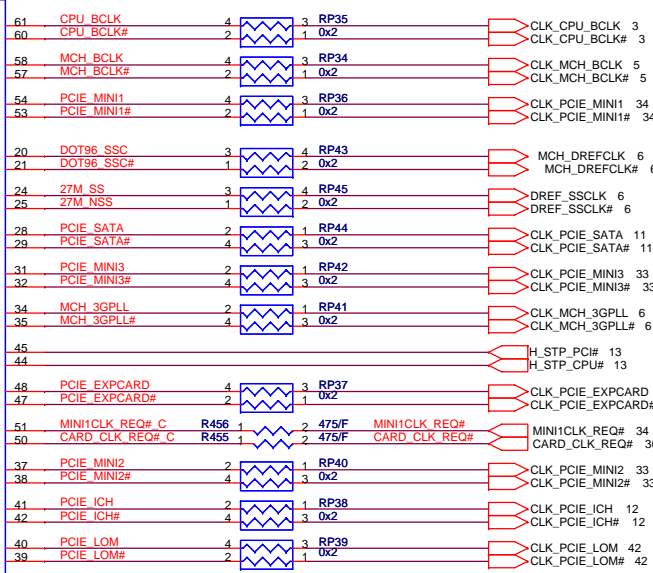
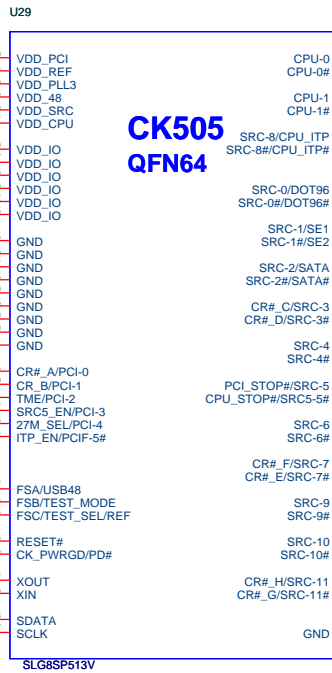
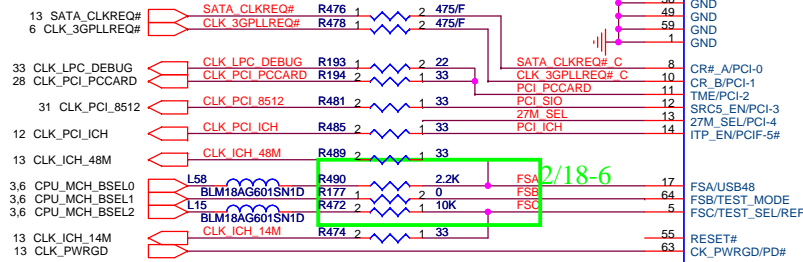
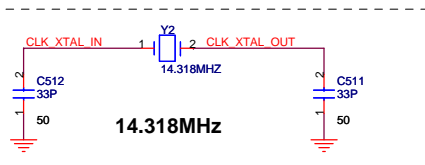
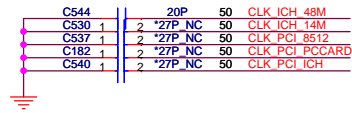
Date: Monday, June 30, 2008

Sheet: 15 of 60

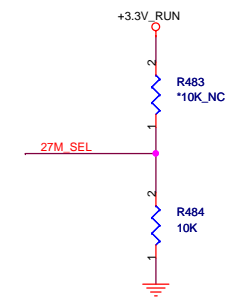
Rev: 1A



Add capacitor pads for improving WWAN.



R185 POP: For Internal pull-low.
R439 POP: For internal pull-high.

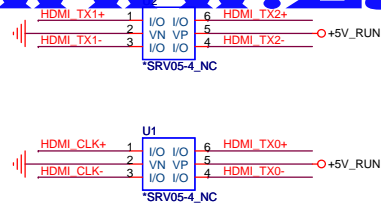


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

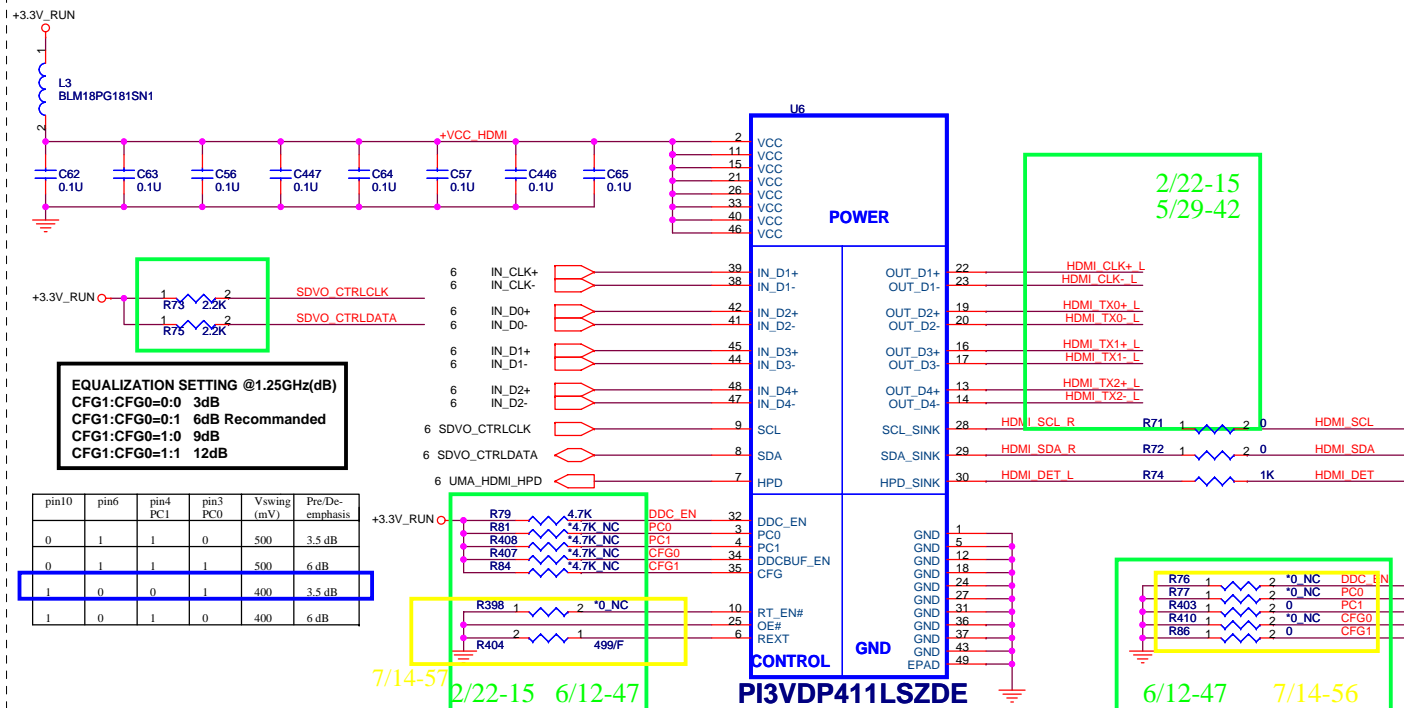
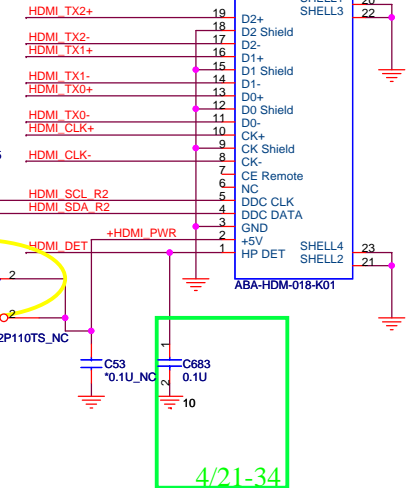
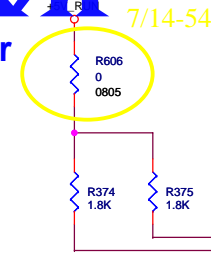
27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout







Reserve for EMI and close to HDMI CONN




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 QUANTA COMPUTER		
Title		
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 QUANTA COMPUTER		
Title		
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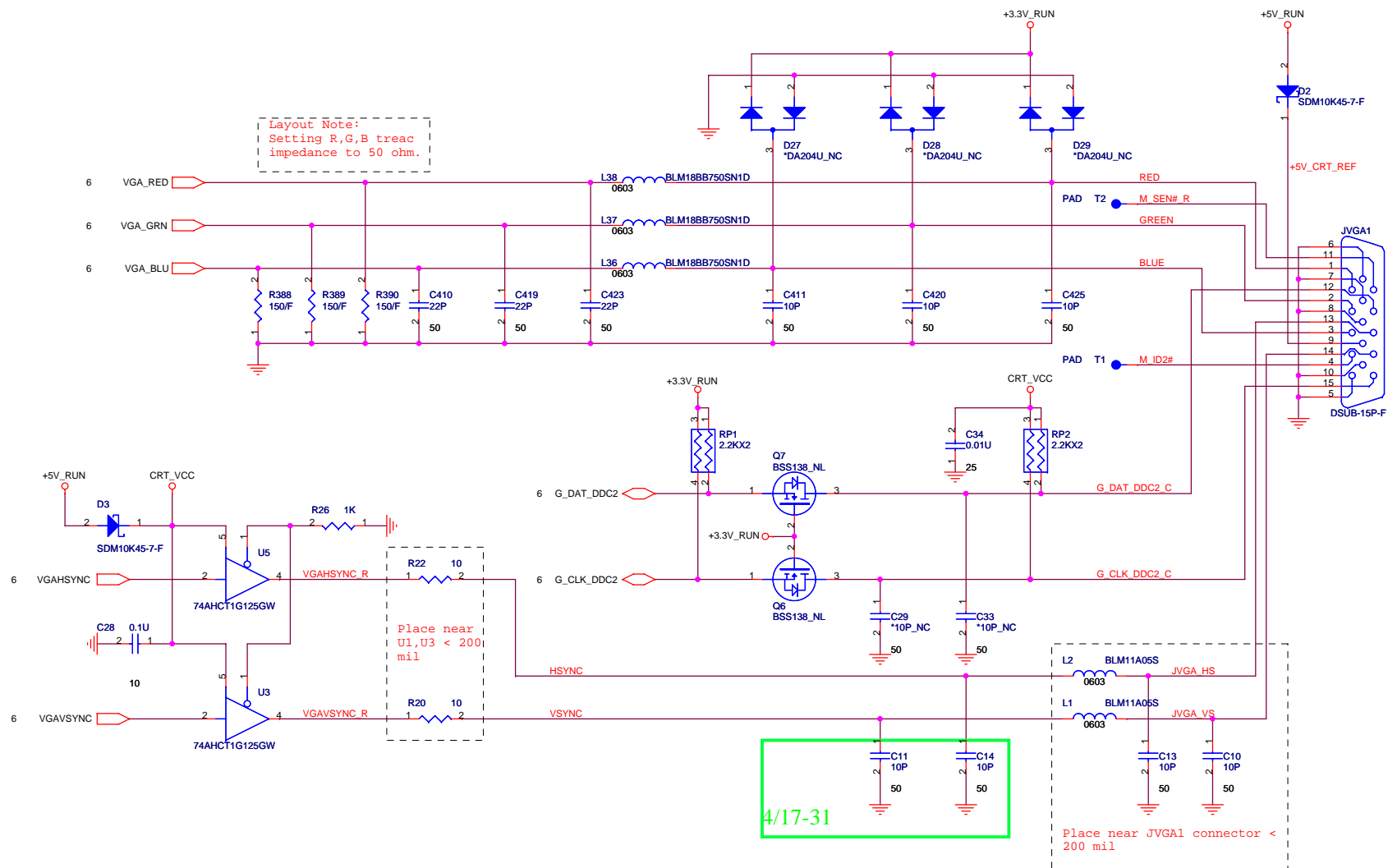
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

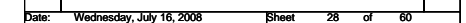
 QUANTA COMPUTER		
Title		
Size	Document Number	Rev
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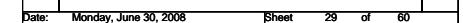
 QUANTA COMPUTER		
Title FLASH, RTC & KC		
Size FM6B	Document Number	Rev 1A
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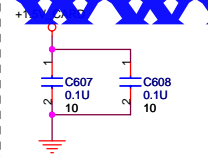
 QUANTA COMPUTER		
Title Battery Selector		
Size	Document Number FM6B	Rev 1A
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 QUANTA COMPUTER		
Title Docking Station CONN.		
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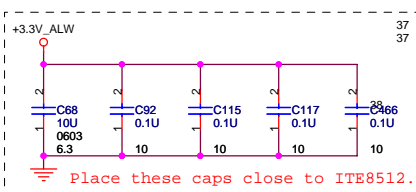








Title		ExpressCard/SmartCard	
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Place these caps close to ITE8512.

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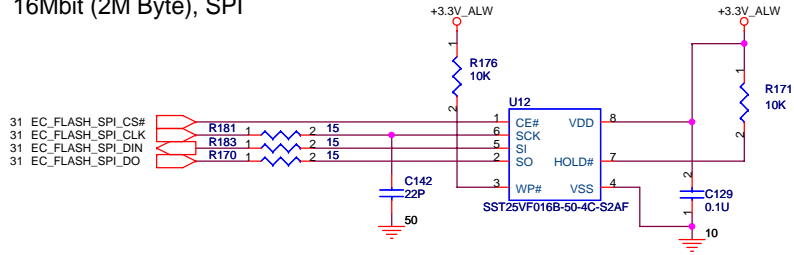
37

37

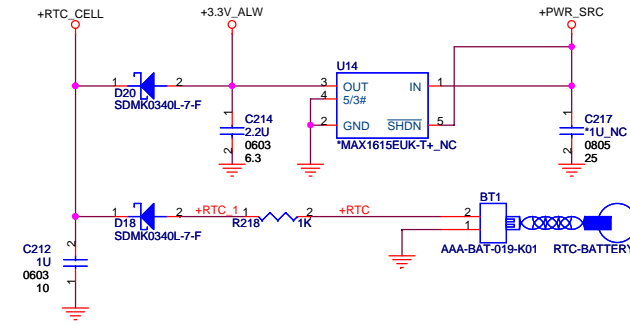
37

37

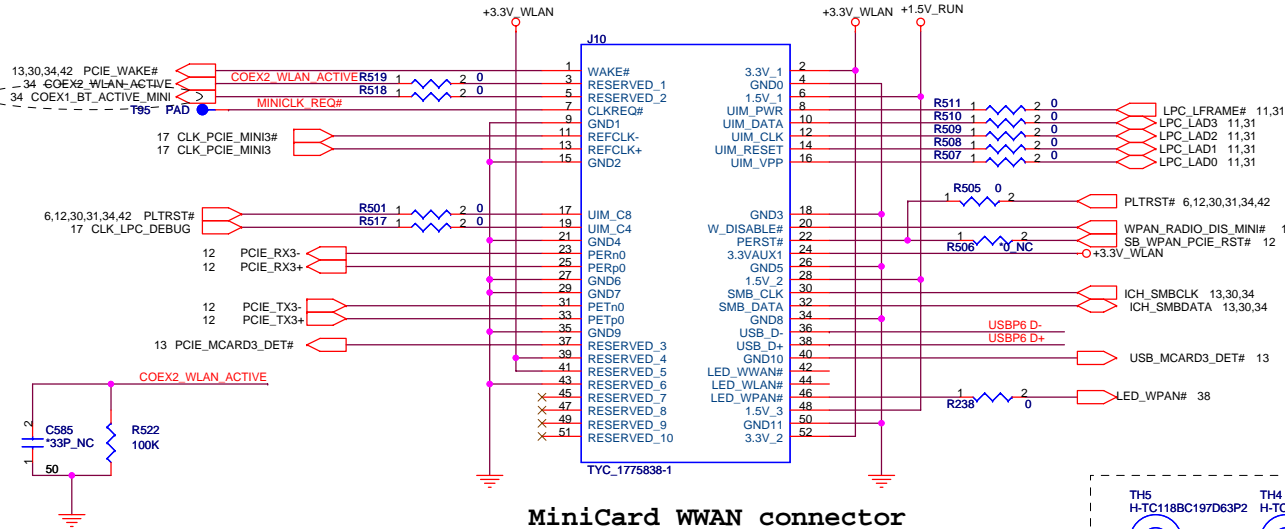
16Mbit (2M Byte), SPI



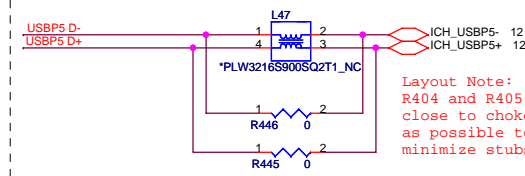
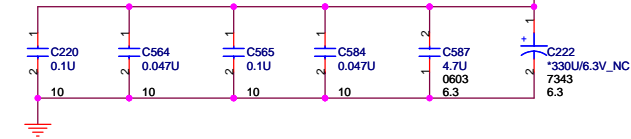
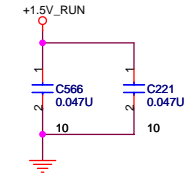
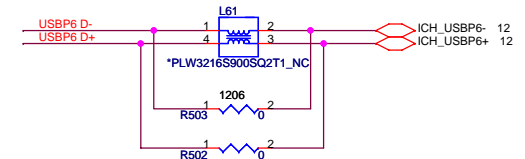
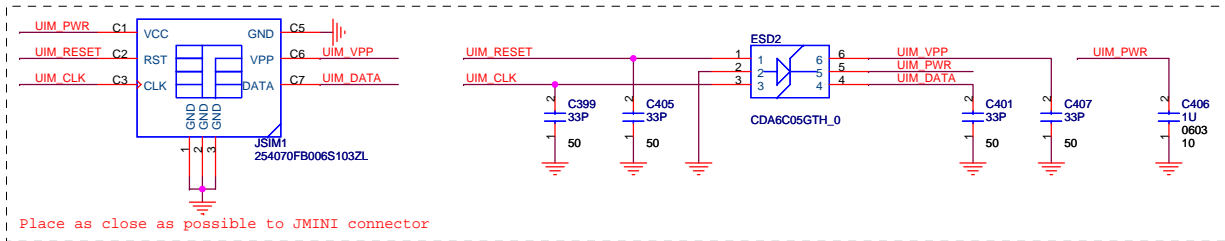
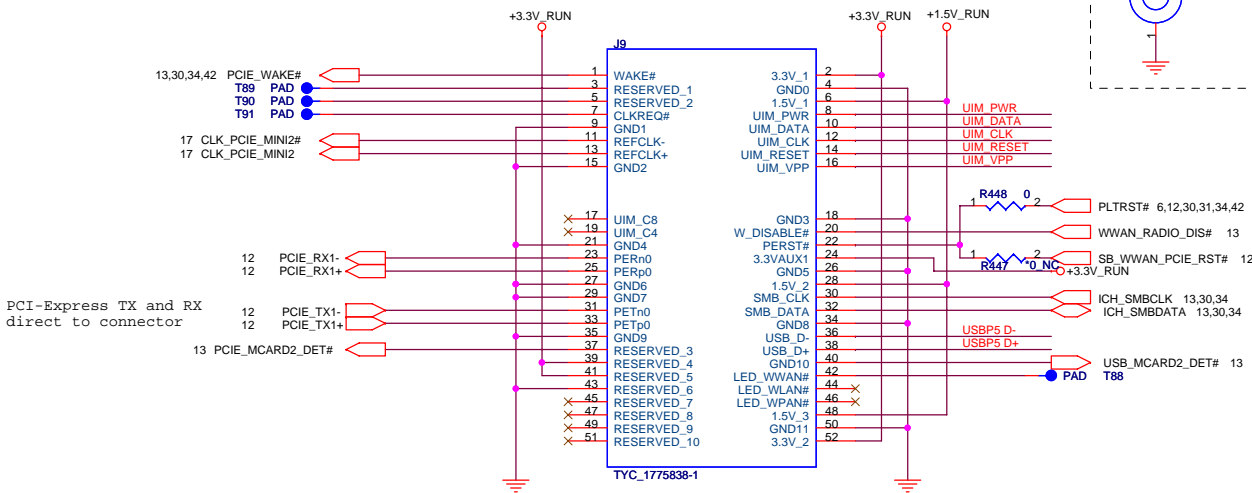
RTC BATTERY



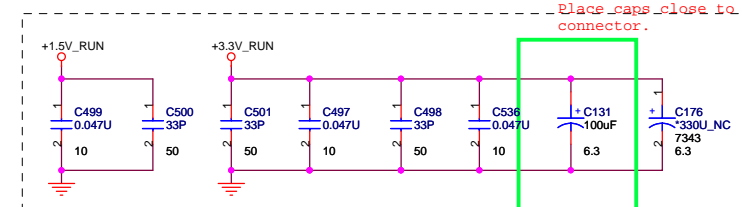
MiniCard Robson, BT. UWB connector



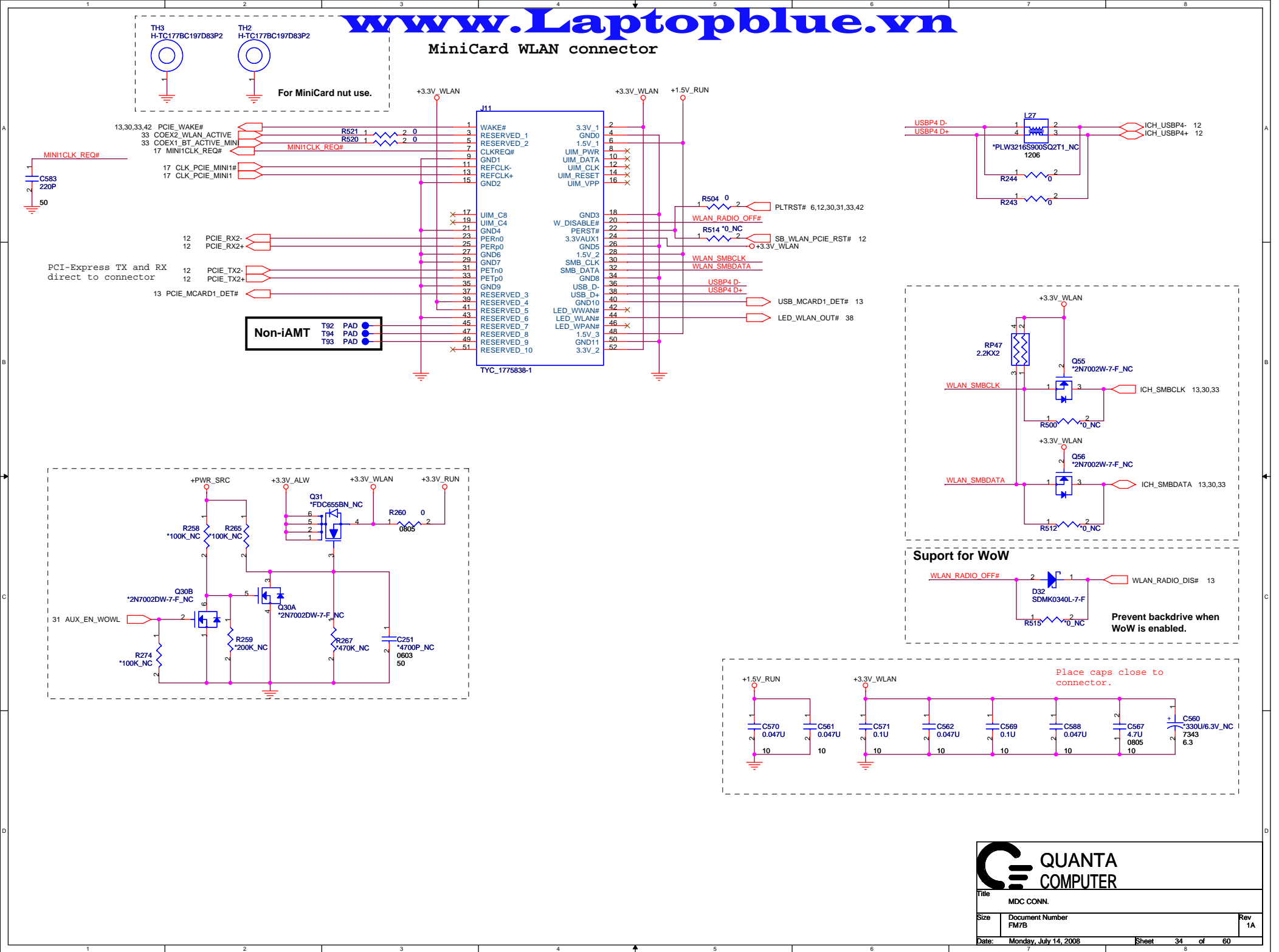
MiniCard WWAN connector



Layout Note:
R404 and R405
close to choke
as possible to
minimize stubs.



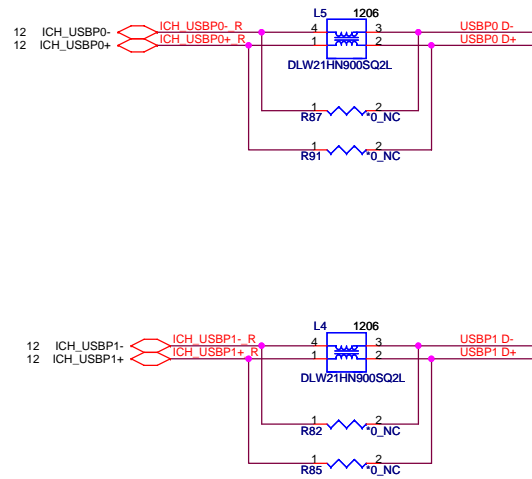
MiniCard WLAN connector



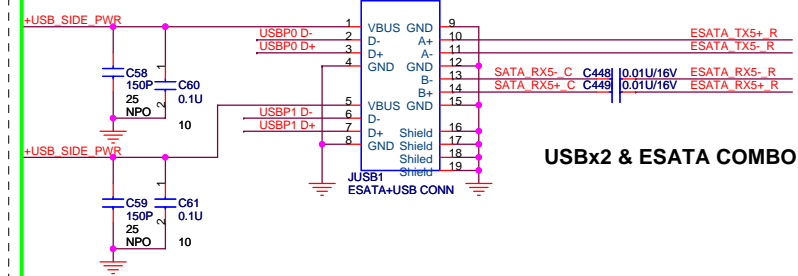
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

2/22-14

4/17-31



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

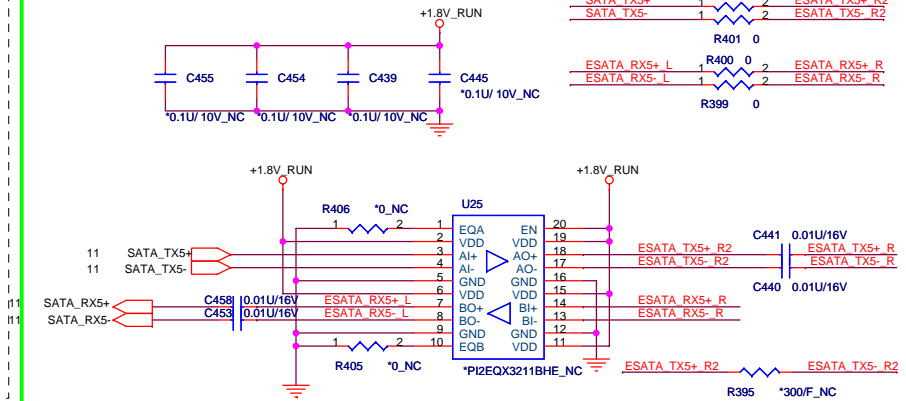


USBx2 & ESATA COMBO

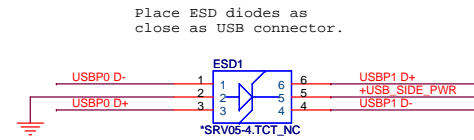
2/20-11

5/29-41

E-SATA Re-driver

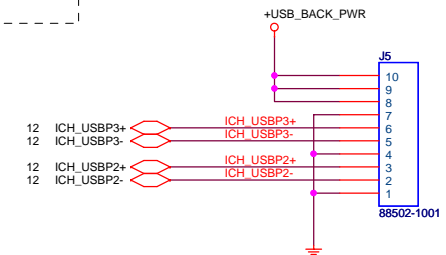


Place one 150uF cap by each USB connector.



Place ESD diodes as close as USB connector.

MB side

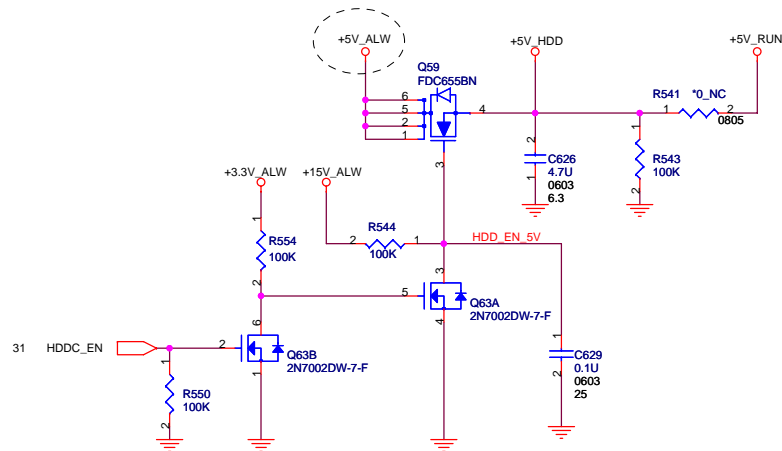
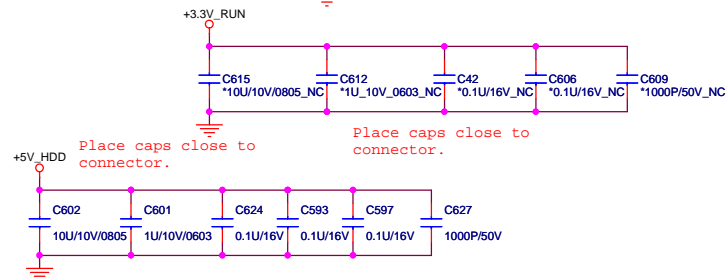
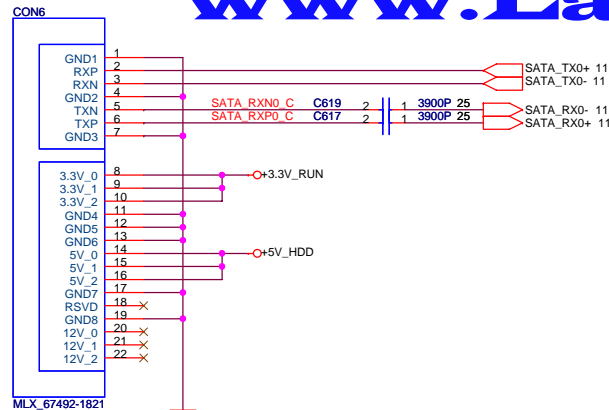


Each channel is 1A

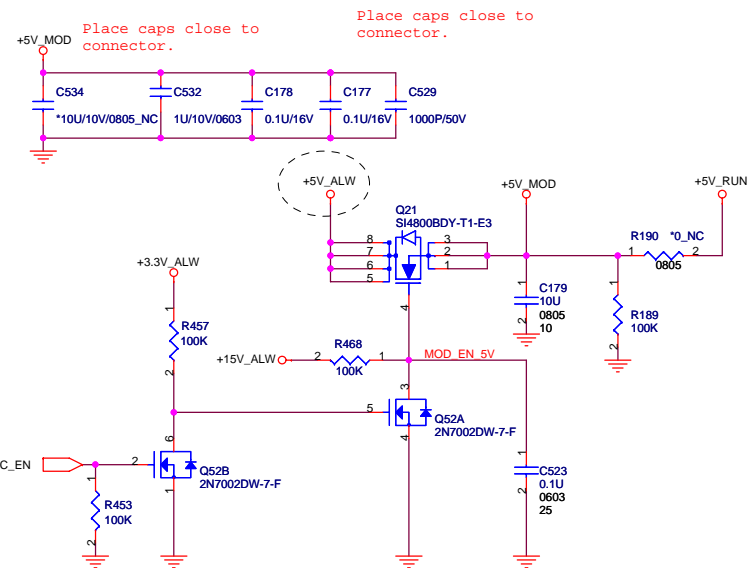
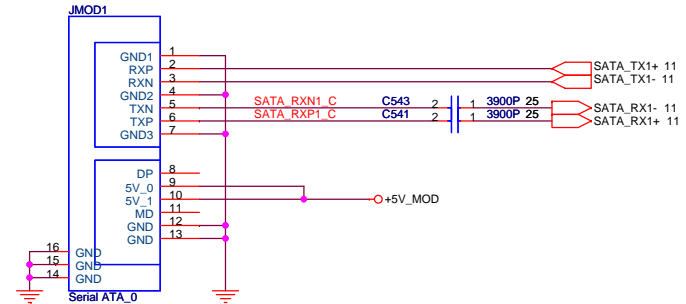


Title			SERIAL PORT & USB
Size	Document Number	Rev	
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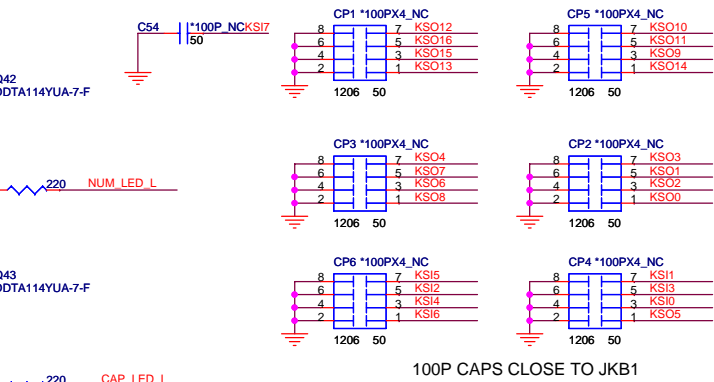
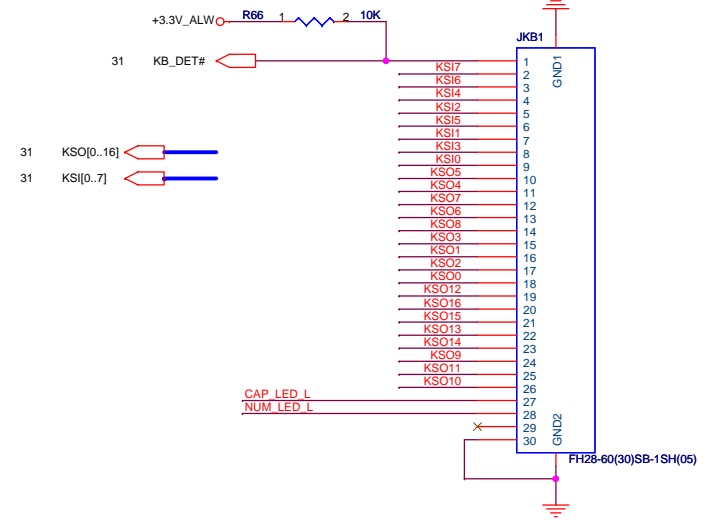
SATA Connector.



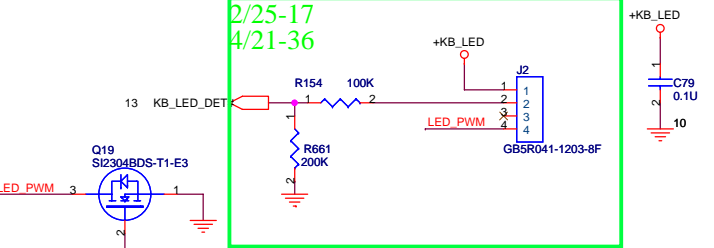
SDD Connector



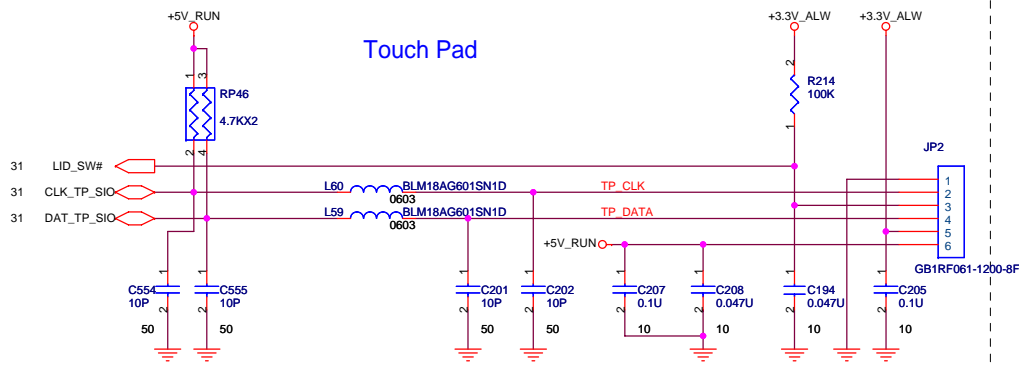
KEYBOARD CONNECTOR



Key board Illumination

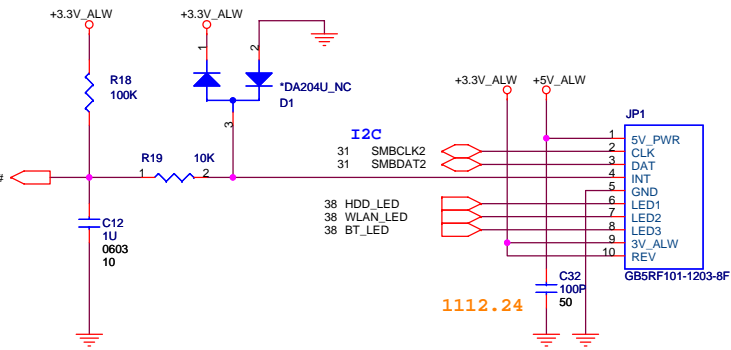


Touch Pad

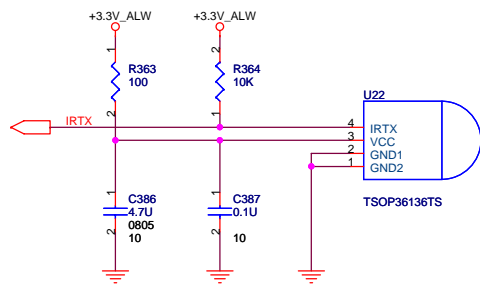


Media Button

Change to P/N:DFFC10FR138
F/T:88501-1001-10P-L(0816)



Consumer IR



Title TOUCH PAD, BULE TOOTH & FIR

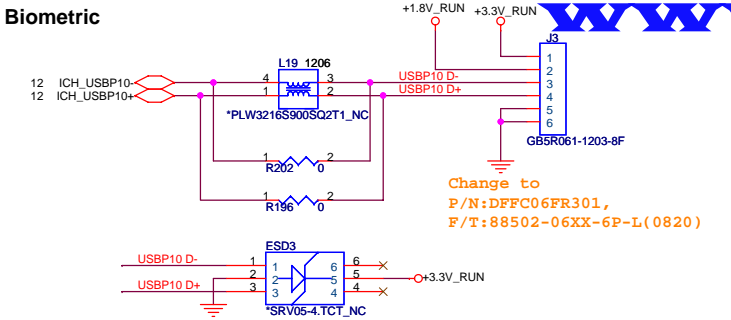
Size Document Number FM7B

Date: Monday, June 30, 2008

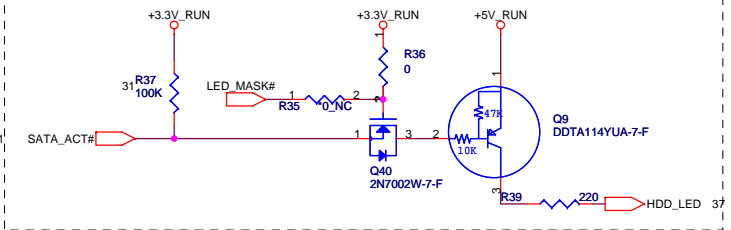
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Rev 1A

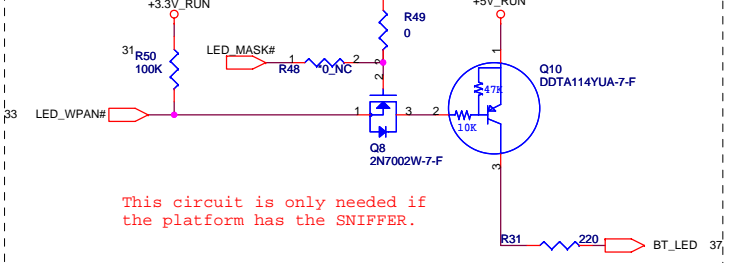
Biometric



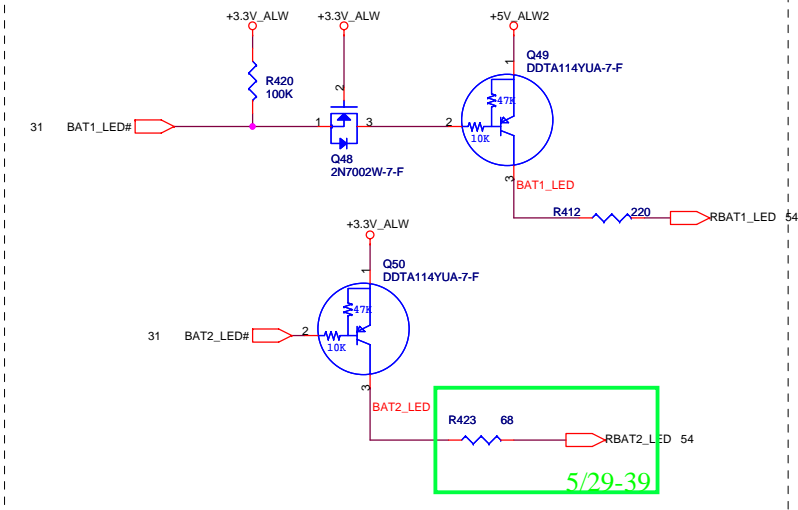
HDD activity LED.



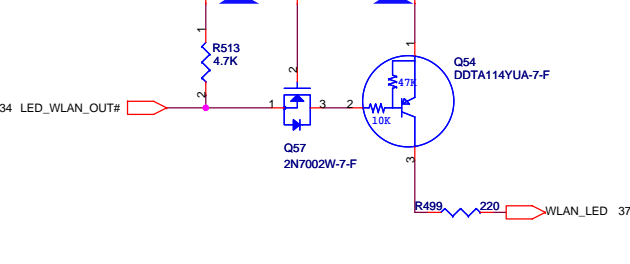
BT / UWB LED



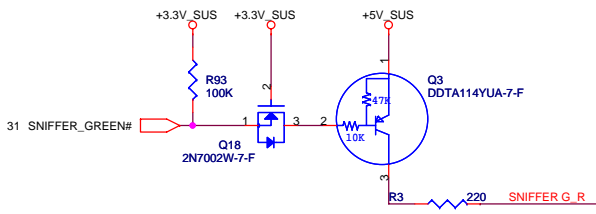
Battery status.



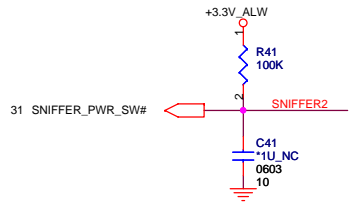
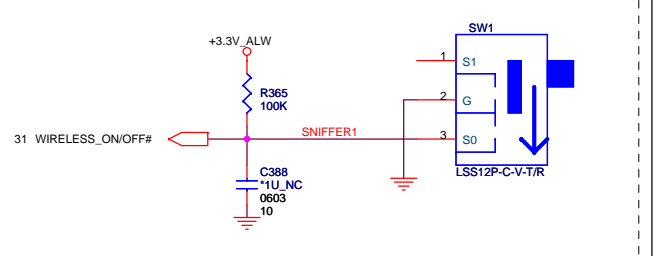
WLAN



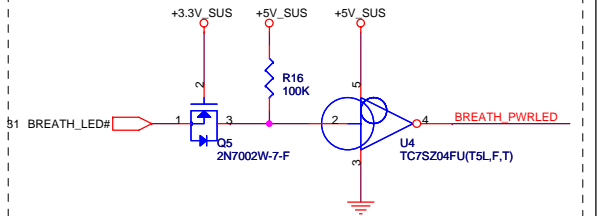
Sniffer Bottom



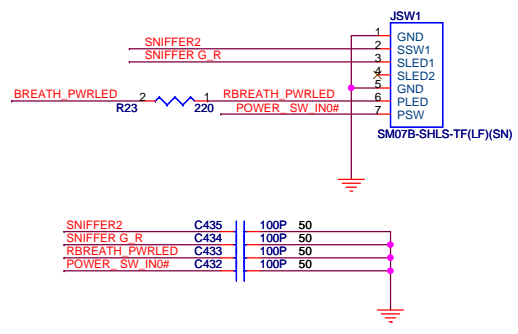
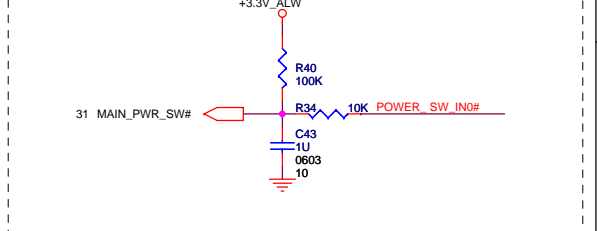
Sniffer Switch ON/OFF Sniffer Switch



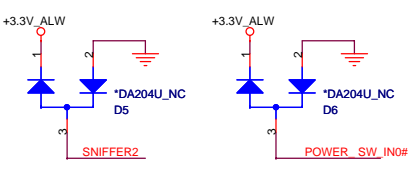
Power & Suspend.

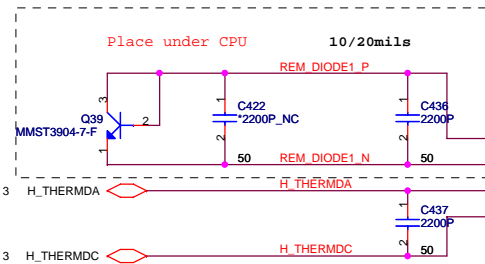
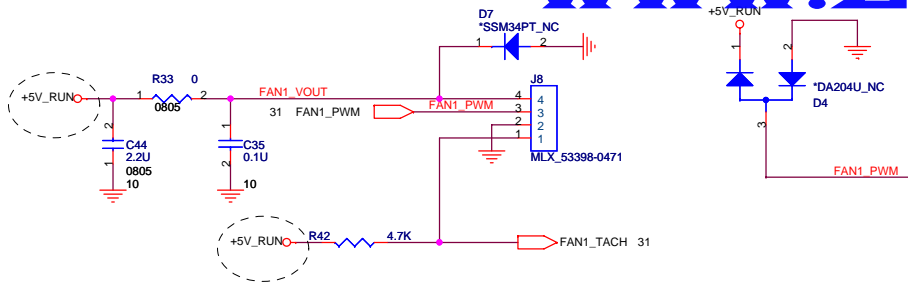


Power Switch

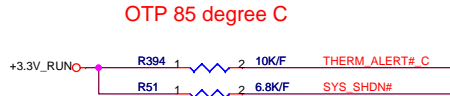
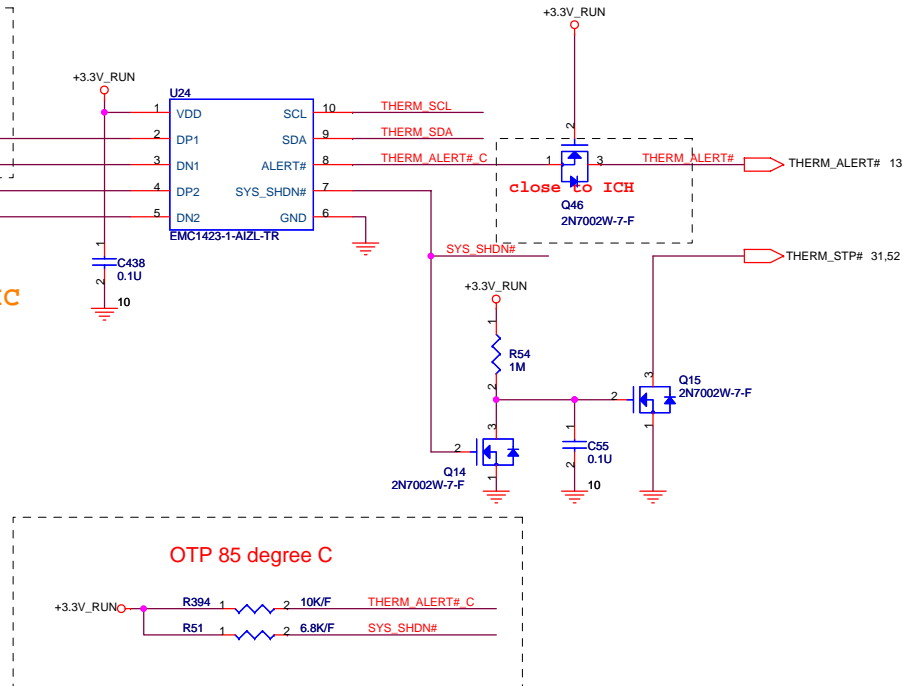
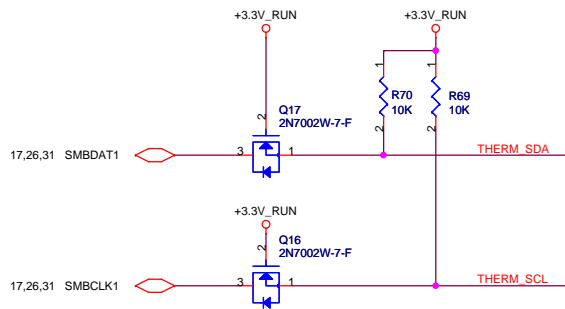


SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection

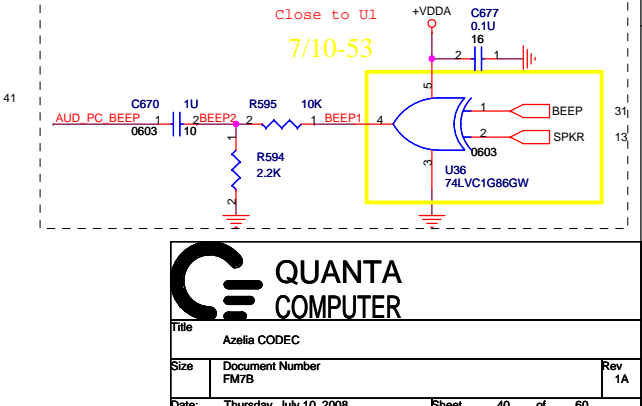
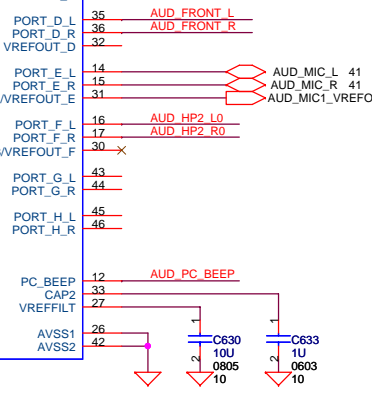
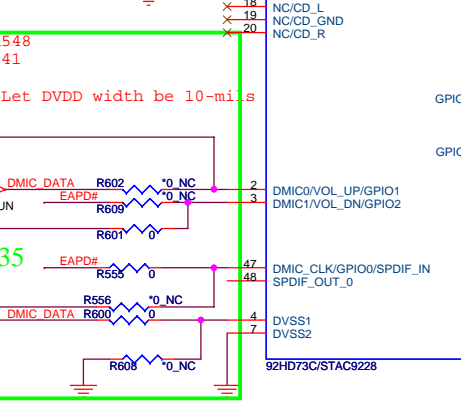
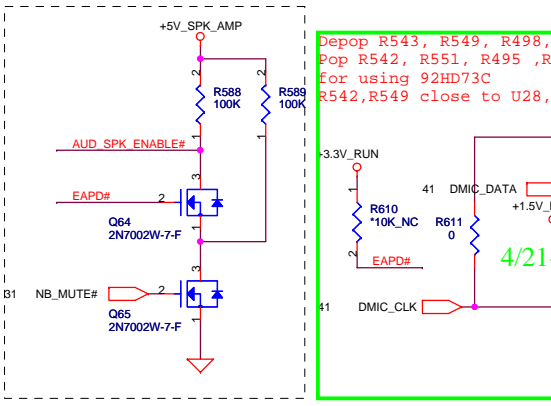
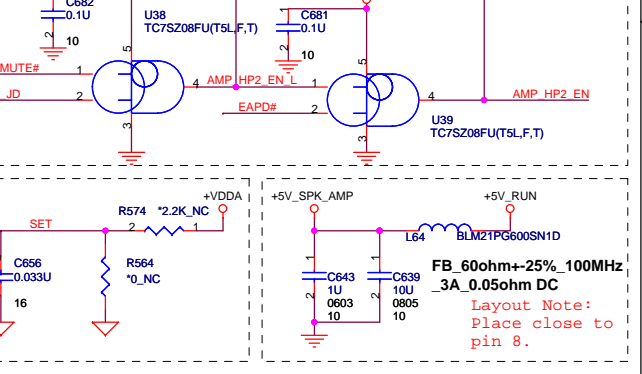
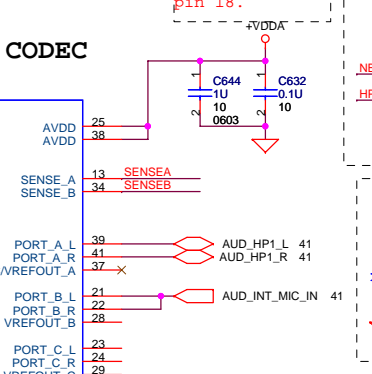
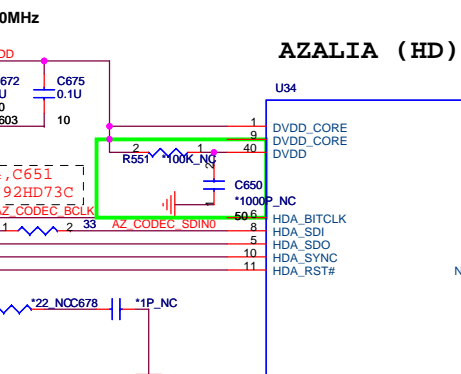
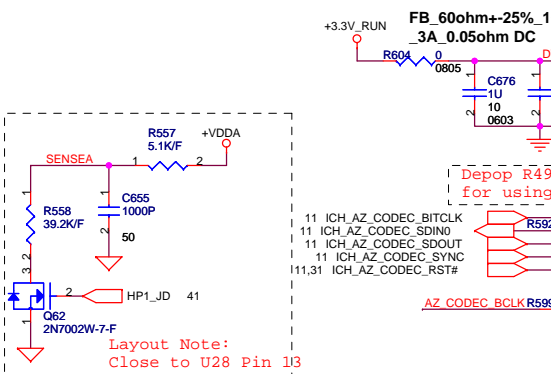
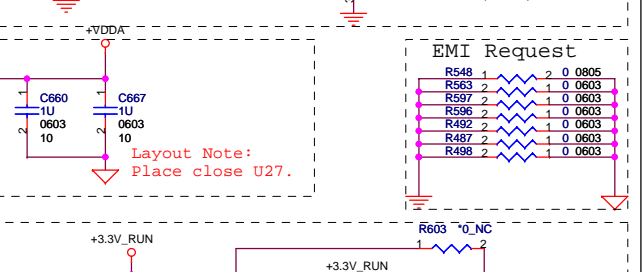
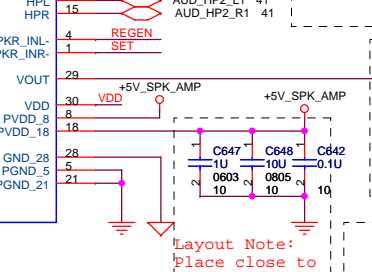
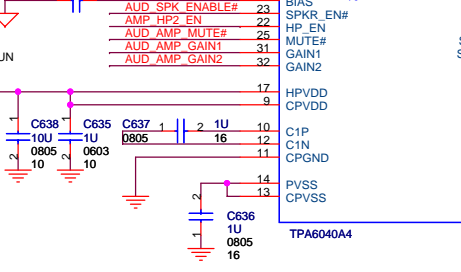
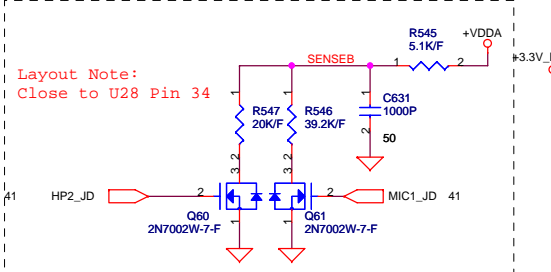
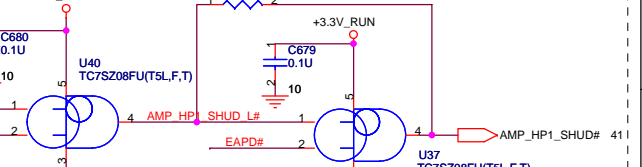
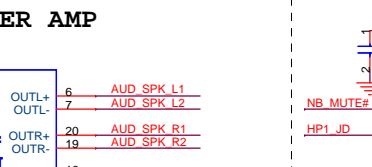
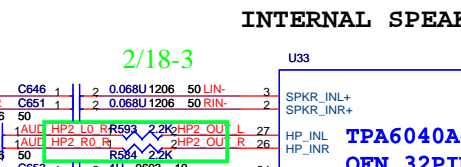
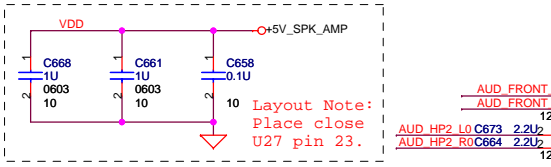
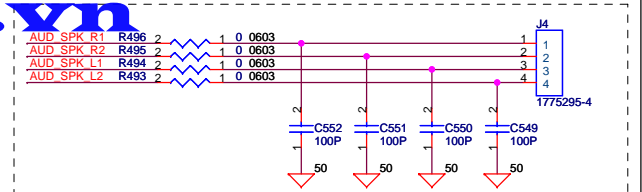
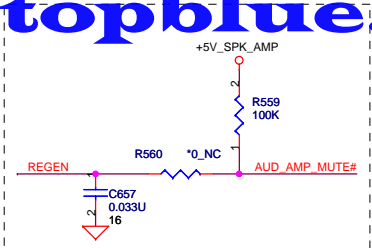
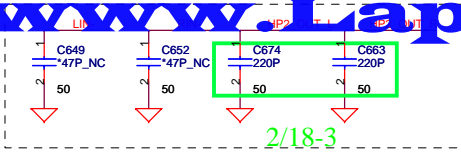
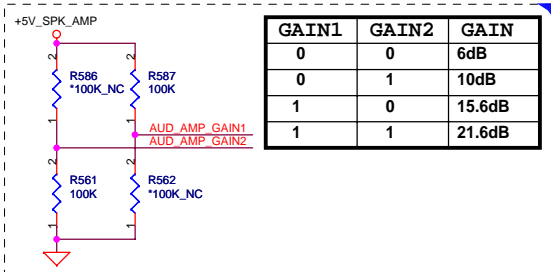


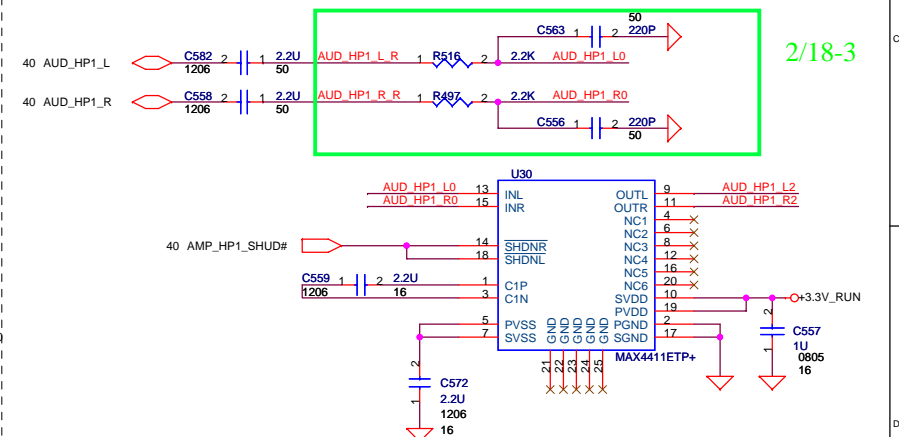


C458, C459 should close to thermal IC



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

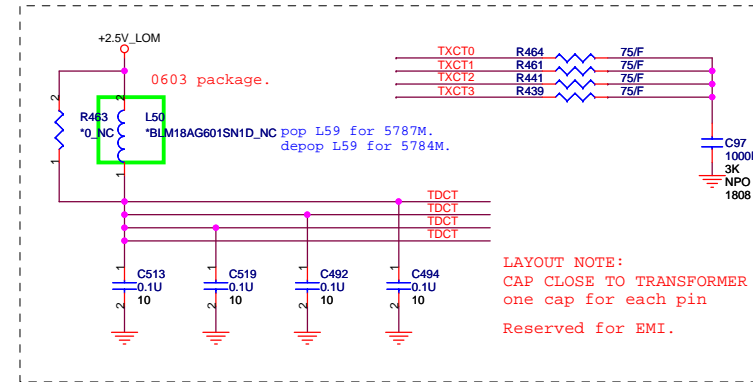
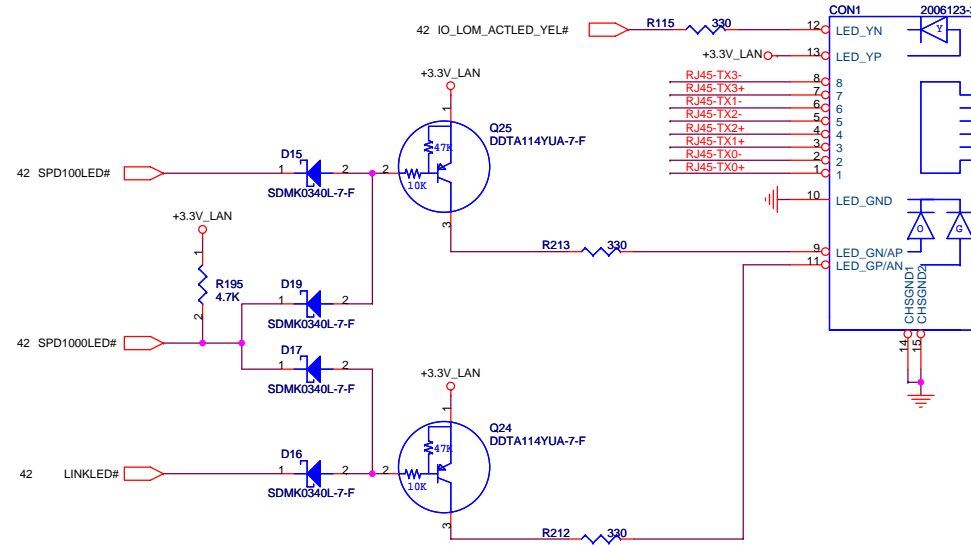
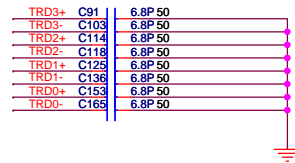
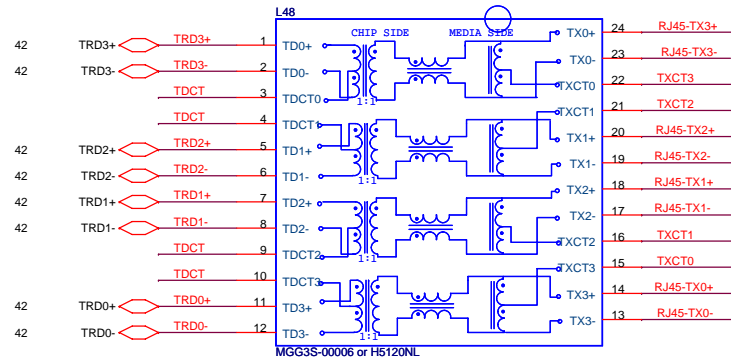


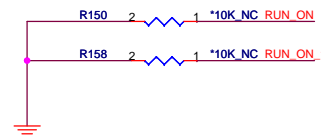
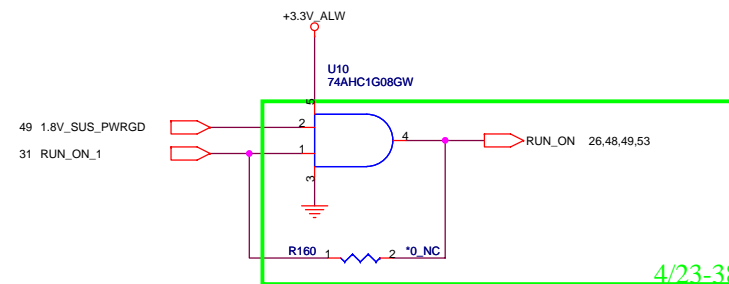
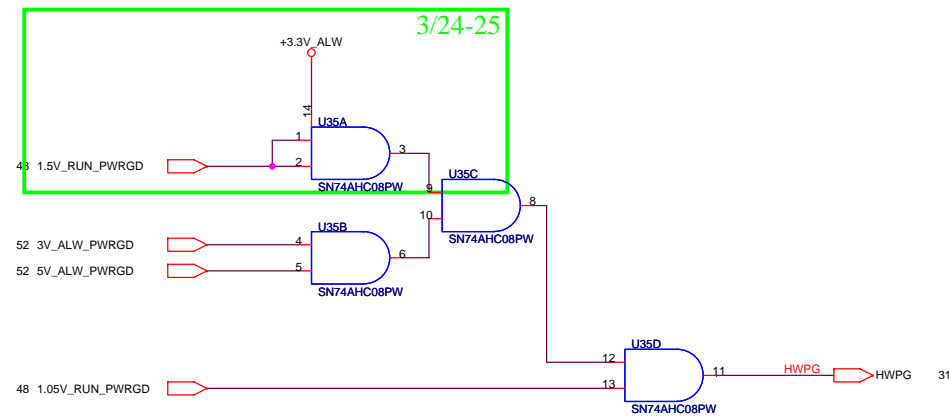
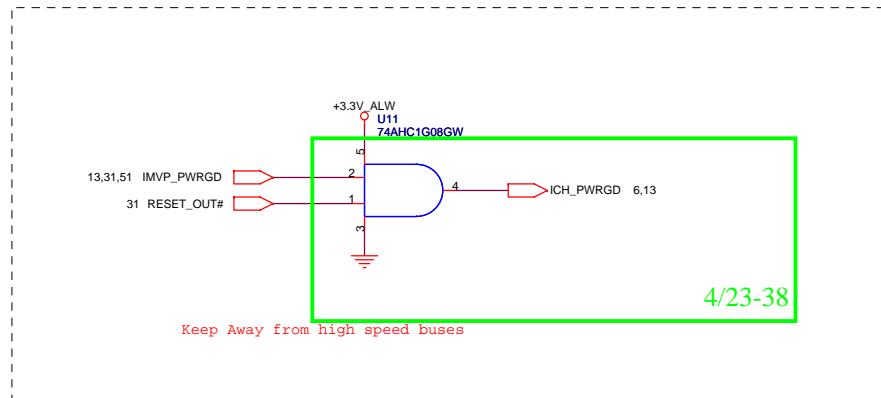



Title			
AUDIO CONN			
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TRANSFORM

TRANSFORM





 QUANTA COMPUTER		
Title Docking Q-SWITCH		
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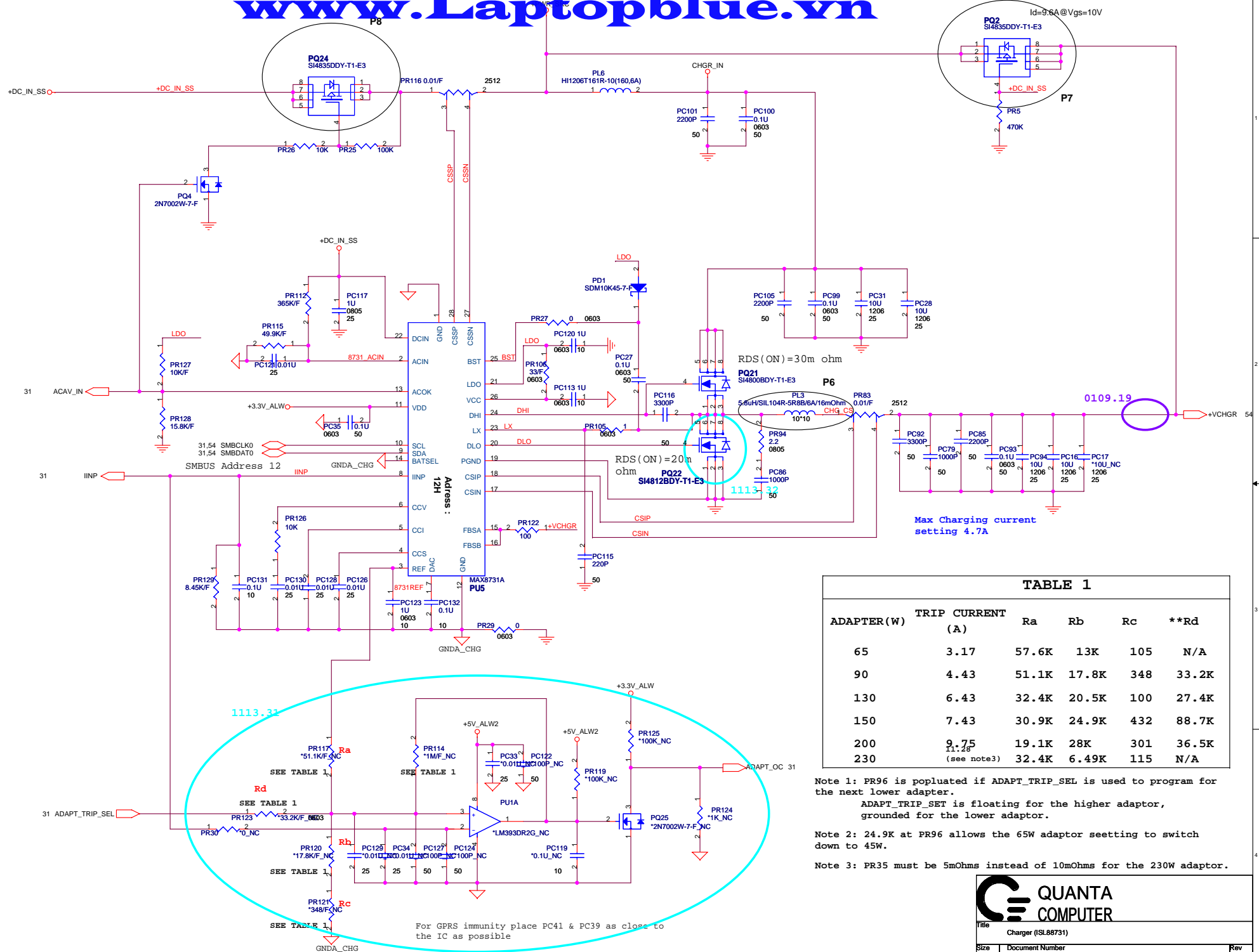


TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	(see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

ADAPT_TRIP_SET is floating for the higher adaptor,
grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.




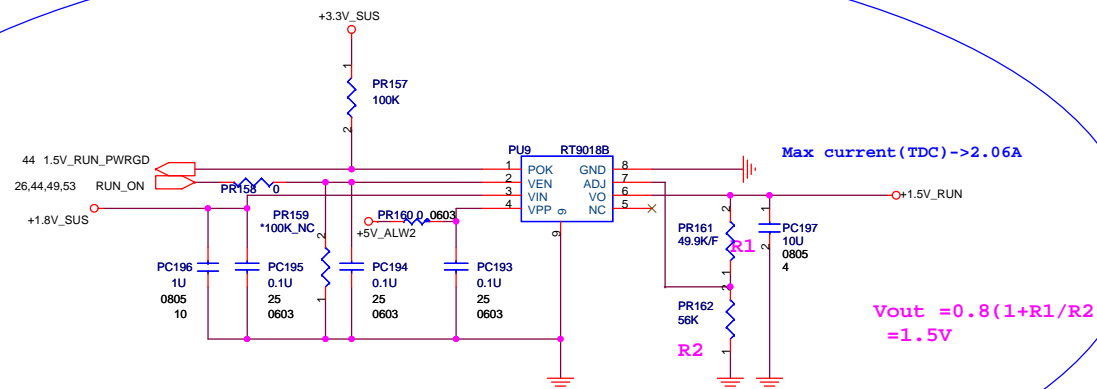
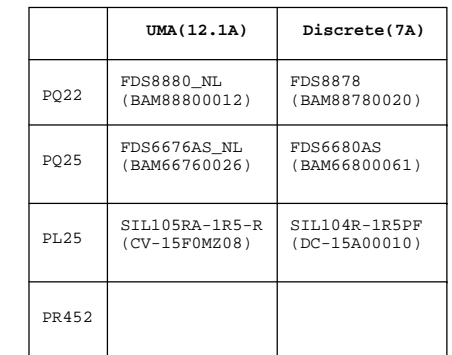
Title **Charger (ISL88731)**

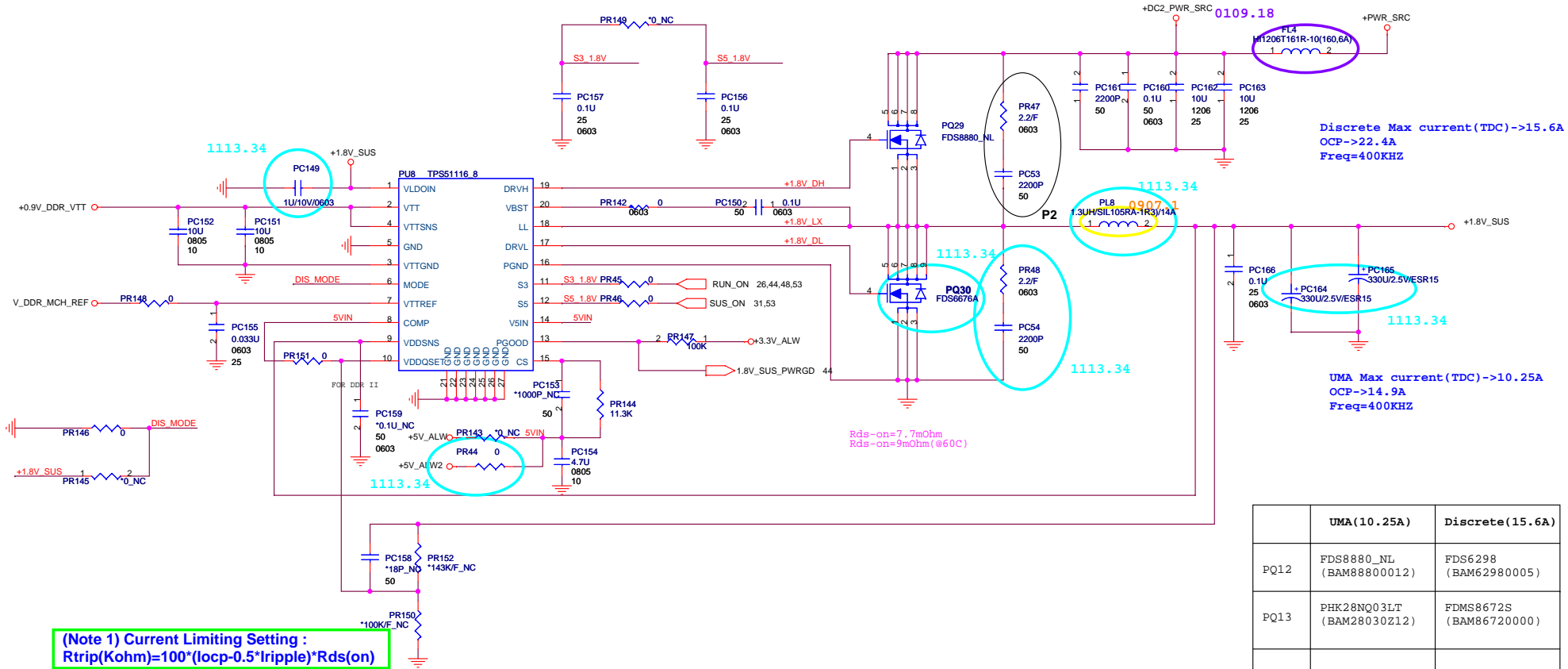
Size	Document Number	Rev
	FM6B	1A

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BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE


 QUANTA COMPUTER		
Title		
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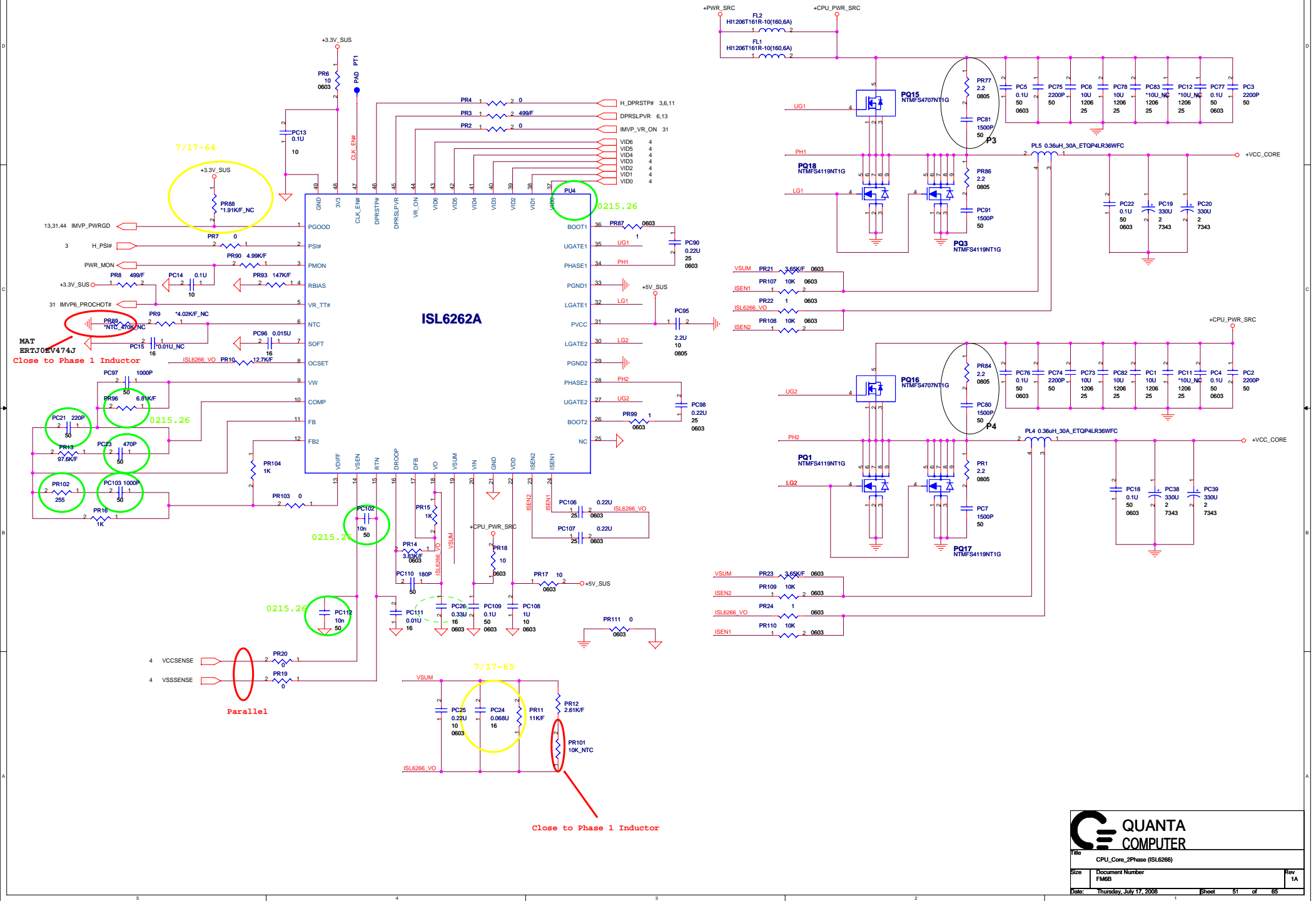




	UMA (10.25A)	Discrete (15.6A)
PQ12	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ13	PHK28NQ03LT (BAM28030212)	FDMS8672S (BAM86720000)
PR83		

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Title		
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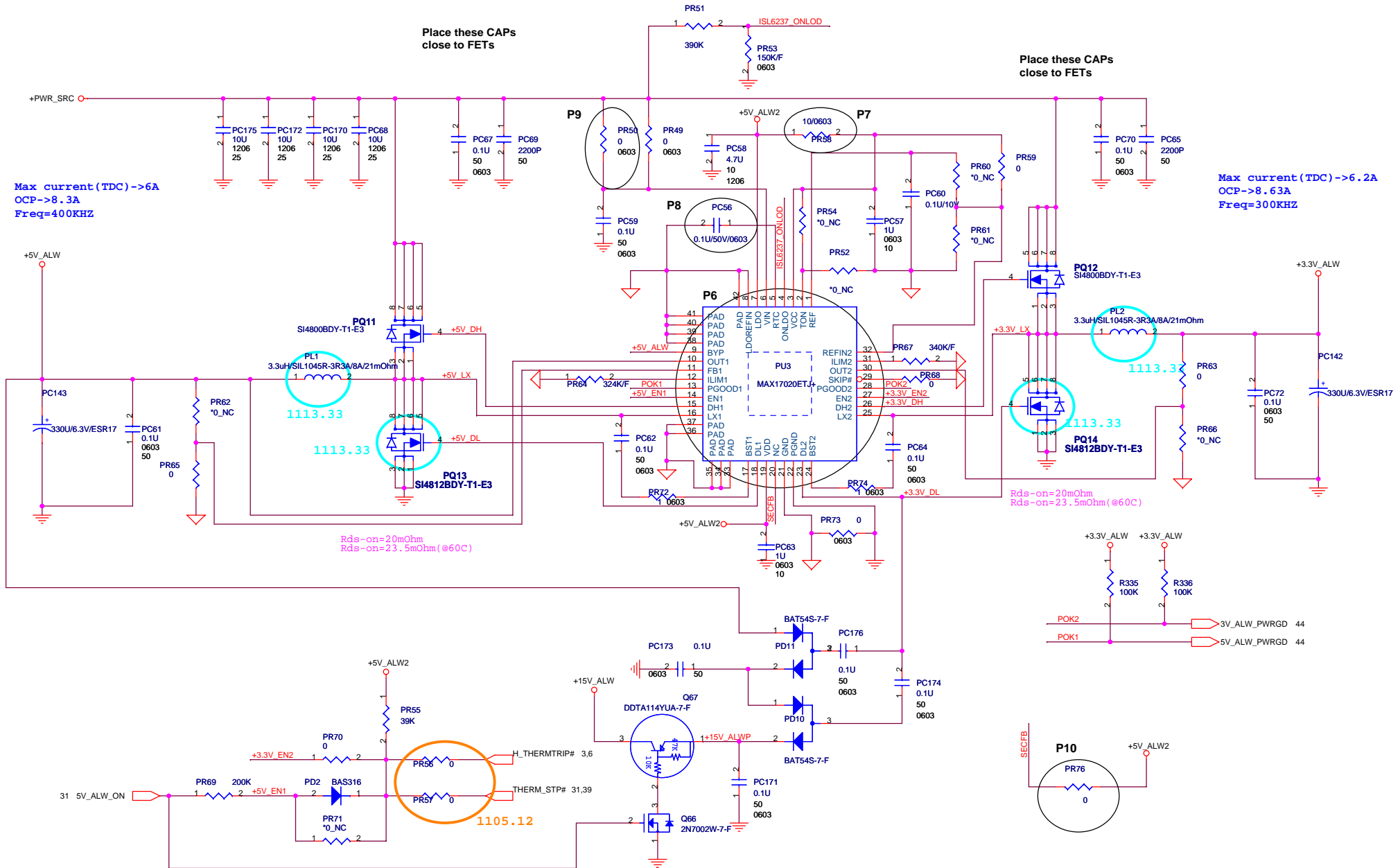


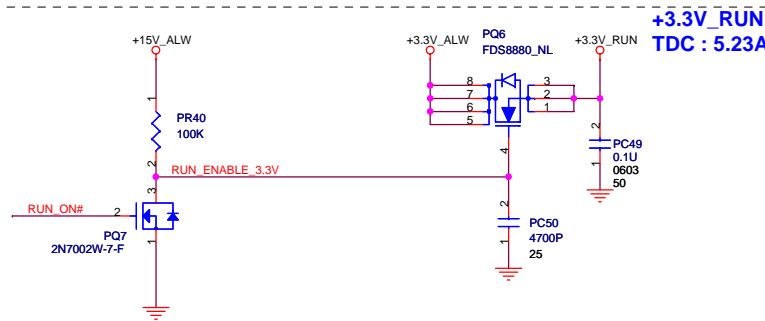
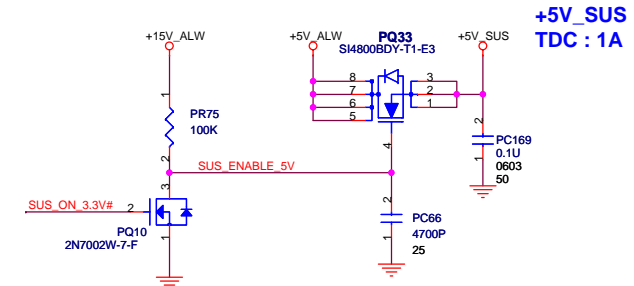
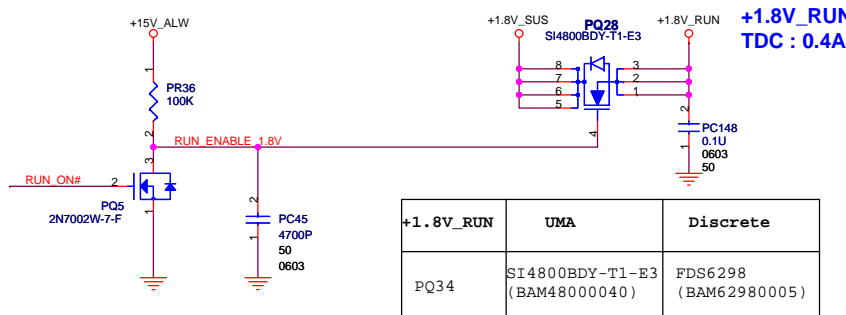
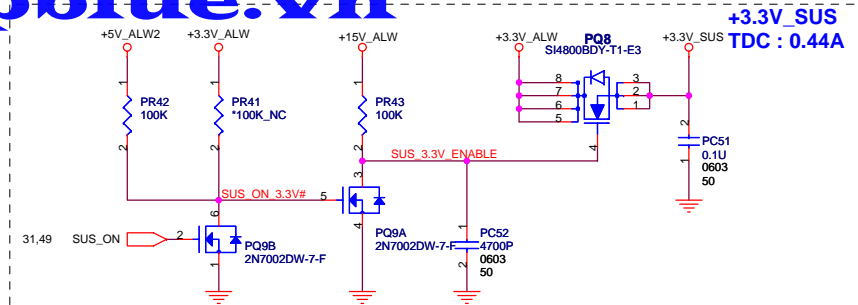
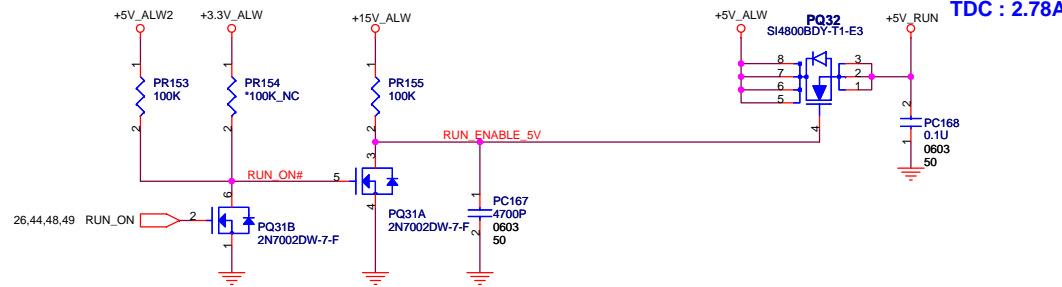
Place these CAPS
close to FETs

Place these CAPS
close to FETs

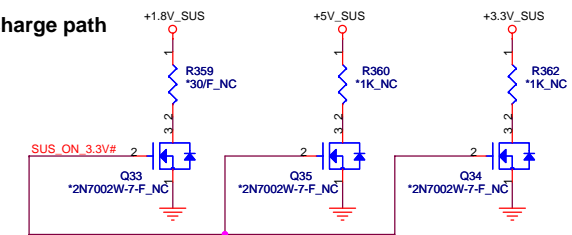
Max current (TDC) -> 6A
OCP -> 8.3A
Freq = 400KHZ

Max current (TDC) -> 6.2A
OCP -> 8.63A
Freq = 300KHZ

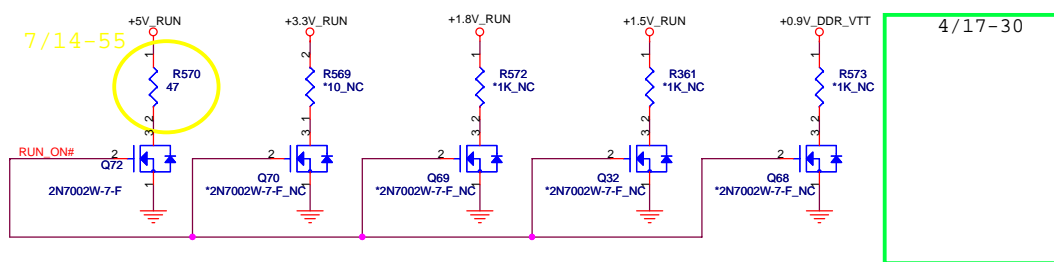


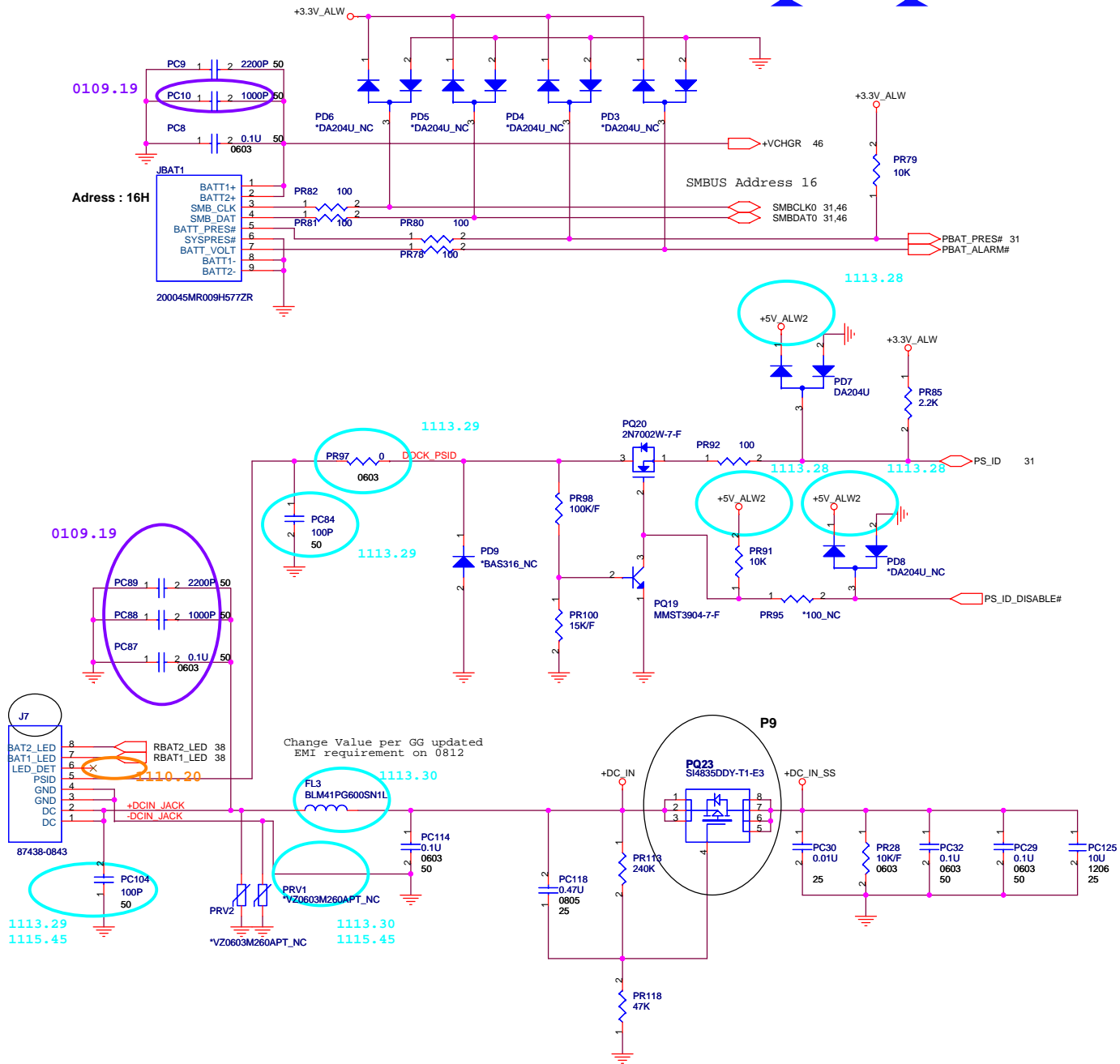


Reserve discharge path



Reserve discharge path





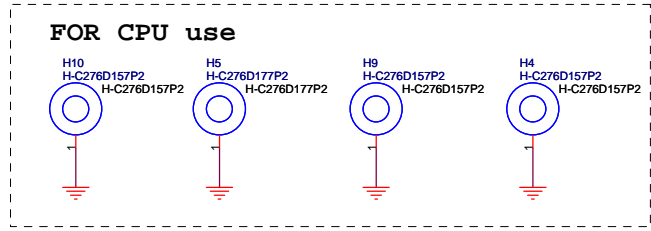
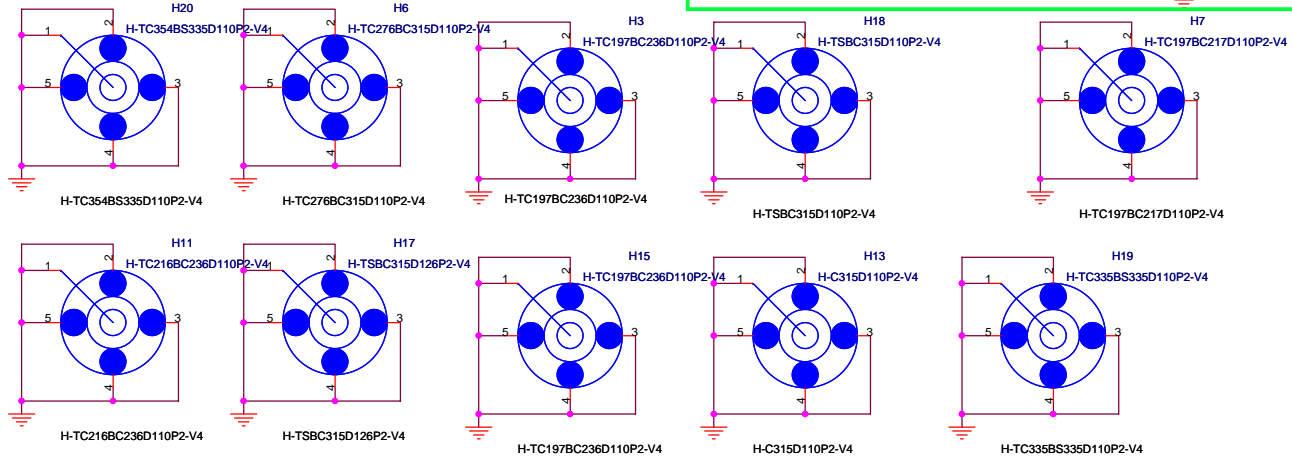
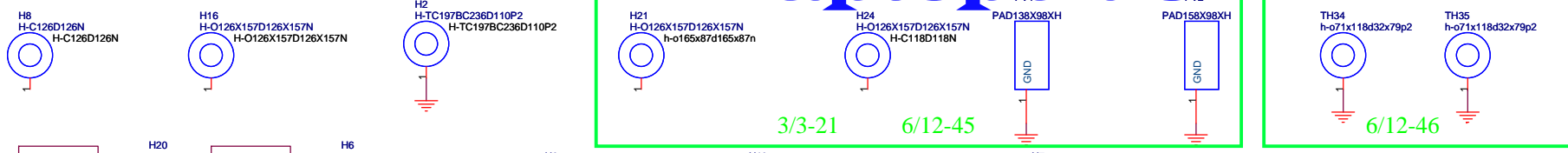
Title DCIN,BATT CONNECTOR

Size Document Number FM6B

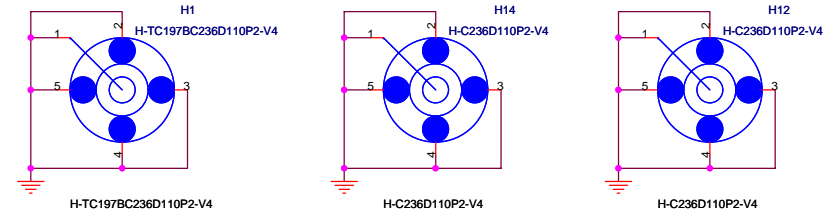
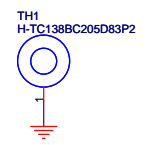
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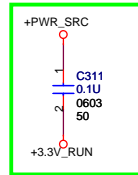
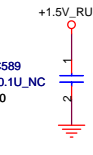
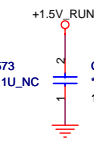
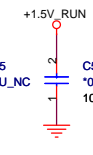
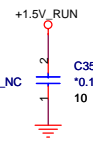
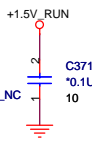
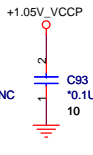
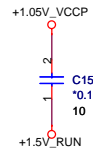
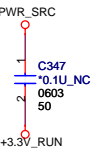
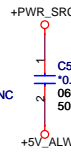
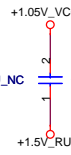
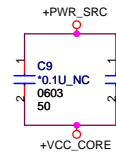
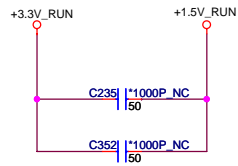


For FAN nut use.

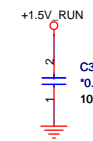
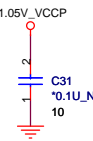
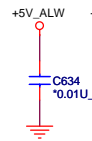


Reserved for EMI.

Stitching caps.



2/19-9



ICH8-M

SIO
ITE8512

