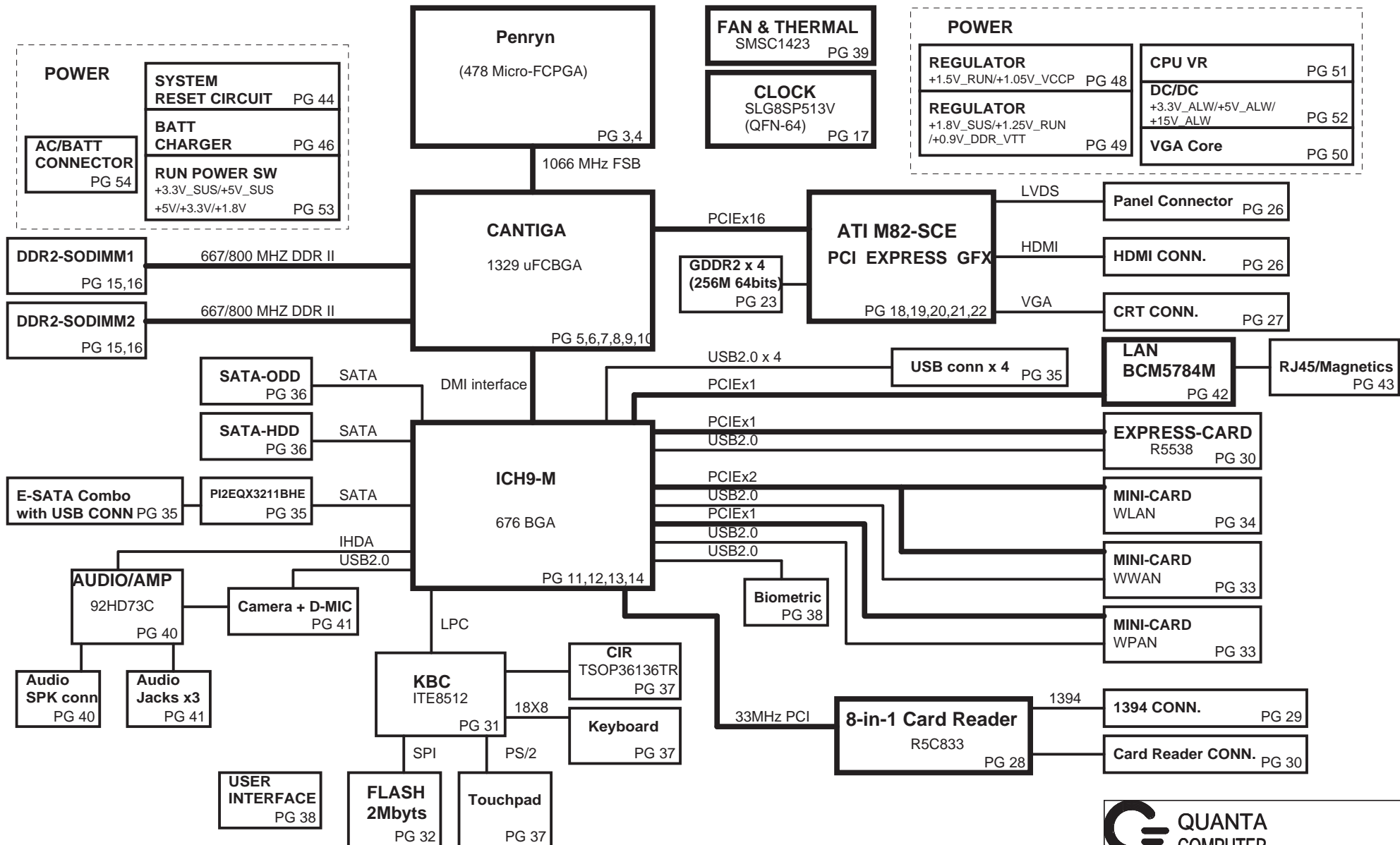









FM7 Hepburn Intel Discrete GFX


VER : D3B

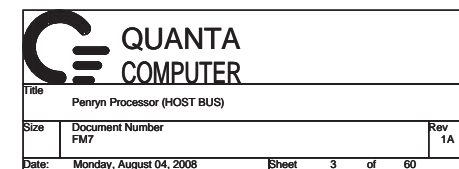


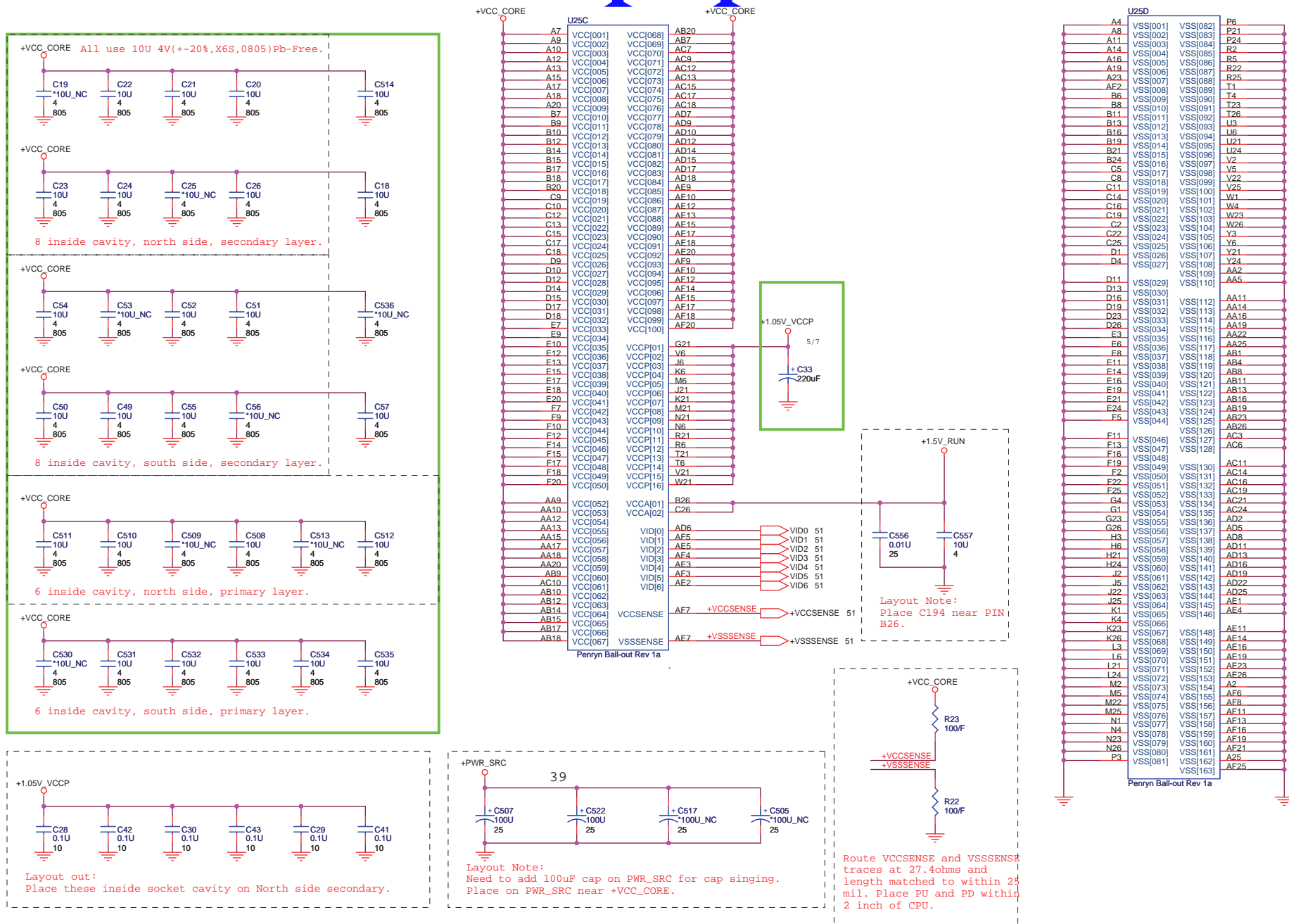
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-23	M82S
24	BLANK PAGE
25	BLANK PAGE
26	LCD CONN / HDMI CONN
27	CRT CONN
28	5C833/PCI
29	IEEE1394
30	Express/Card Reader
31	SIO (ITE8512)
32	FLASH / RTC
33	MINI-Card (WPAN, WWAN)
34	MINI-Card (WLAN)
35	USB
36	SATA (HDD & CD_ROM)
37	TP / KEYBOARD
38	SWITCH / LED
39	FAN / THERMAL
40	Azelia CODEC
41	AUDIO CONN
42	LAN (RTL8111B/8111C)
43	LAN RJ-45 / TRANSFORM
44	System Reset Circuit
45	Blank Page
46	Changer (MAX8731A)
47	Blank Page
48	1.05VCCP & 1.5VRUN
49	1.8VSUS & 0.9VTT
50	VGA_M82
51	CPU_ISL6266 (2PHASE)
52	MAX8744 (+5V,3.3V)
53	Run Power Switch
54	DCin & Batt
55	PAD & SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Diagram

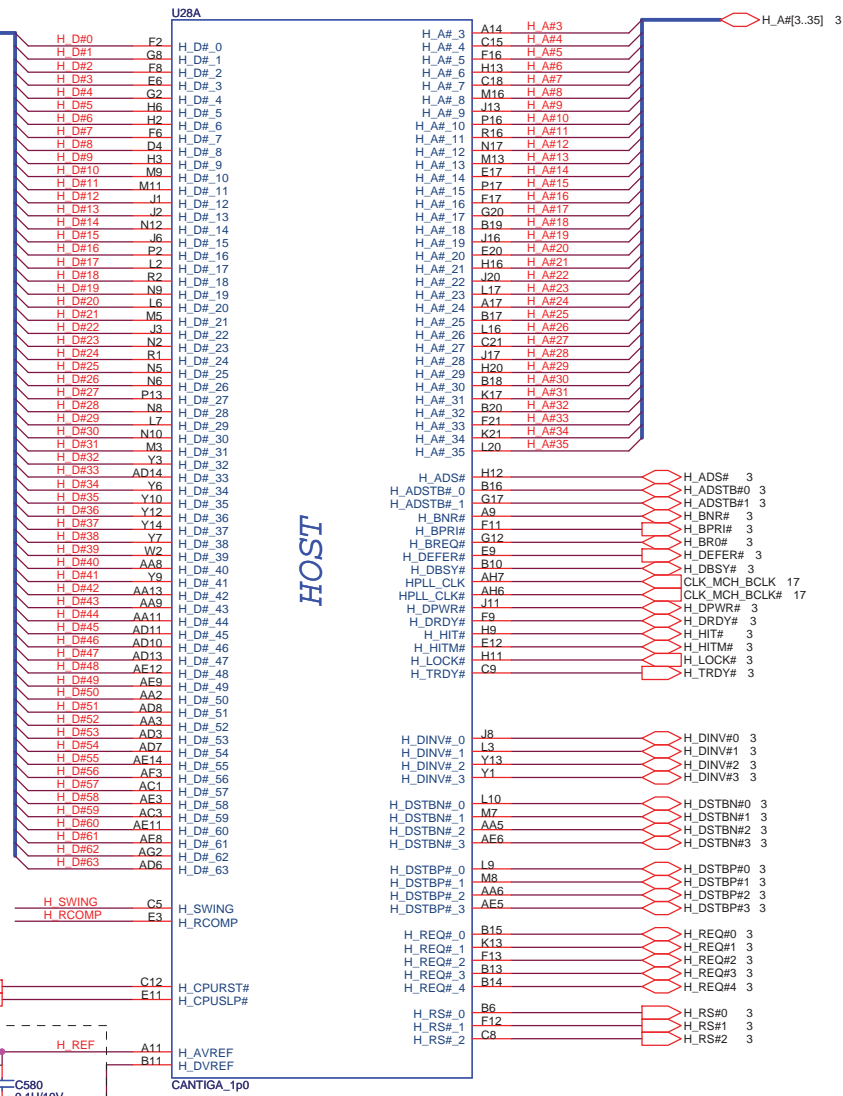
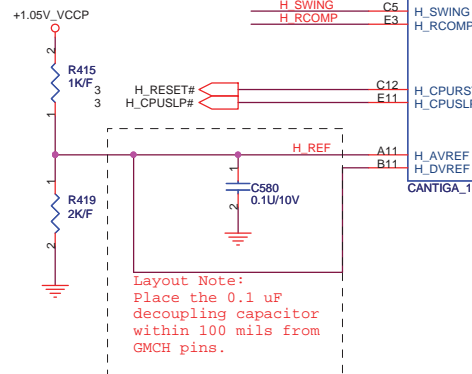
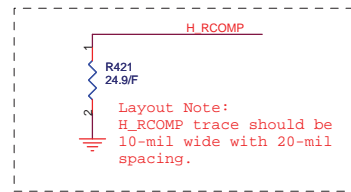
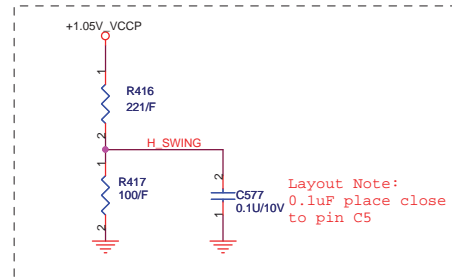
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,26,27,36,37,38,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,26,27,28,30,31,33,34,36,38,39,40,41,42,53,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.2V_LOM	+1.25V	42	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	

GND PLANE	PAGE	DESCRIPTION
 8731AGND	46	
 AGND_0.9V	49	
 AGND_DC/DC	52	
 AGND_DC2	48	
 AGND_DDR	49	
 AGND_ISL6260	51	
 GND	ALL	

 QUANTA COMPUTER		
Title: Index & Power Status		
Size:	Document Number: FM6	Rev: 1A
Date: Monday, June 30, 2008	Sheet: 2	of 58





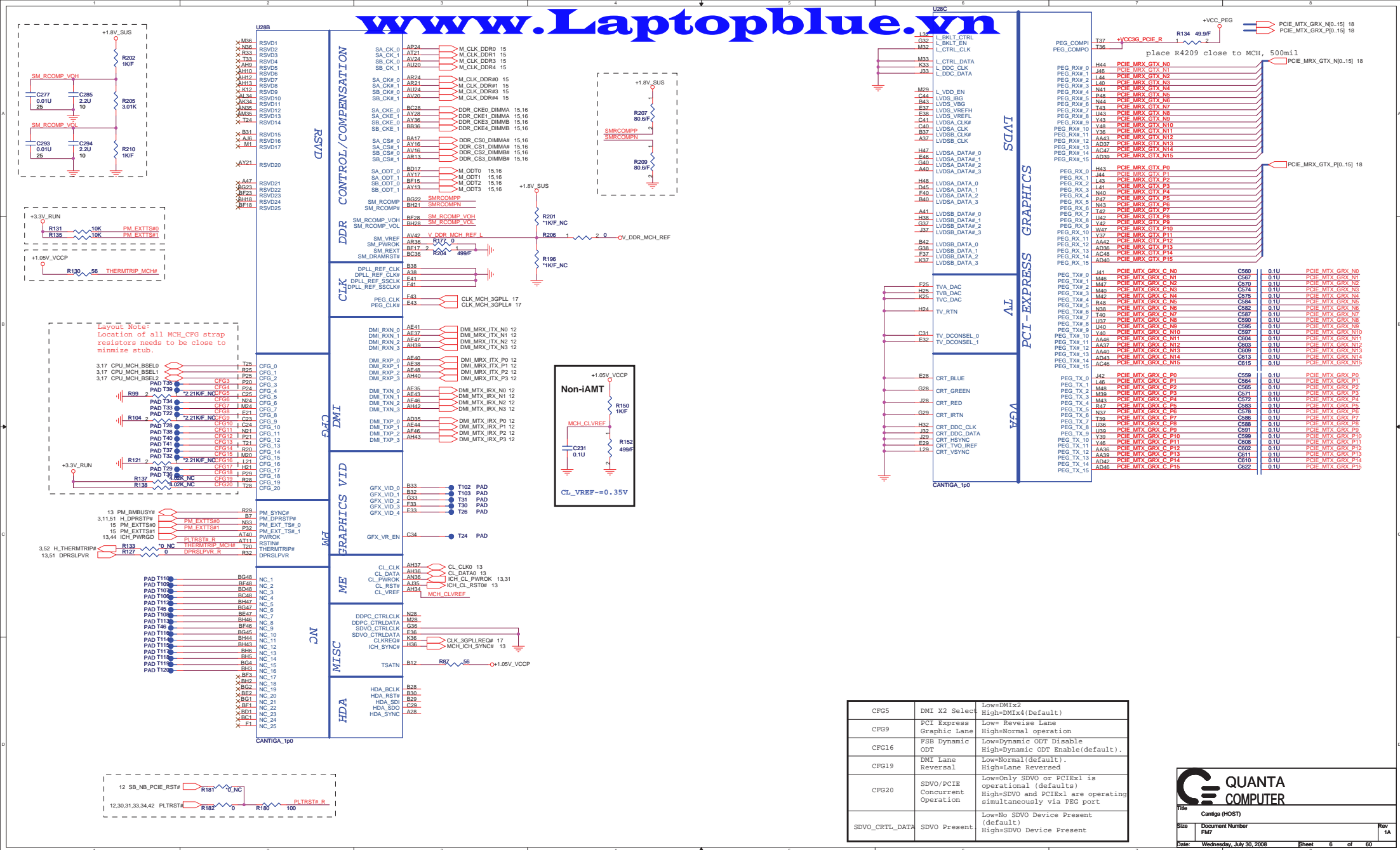


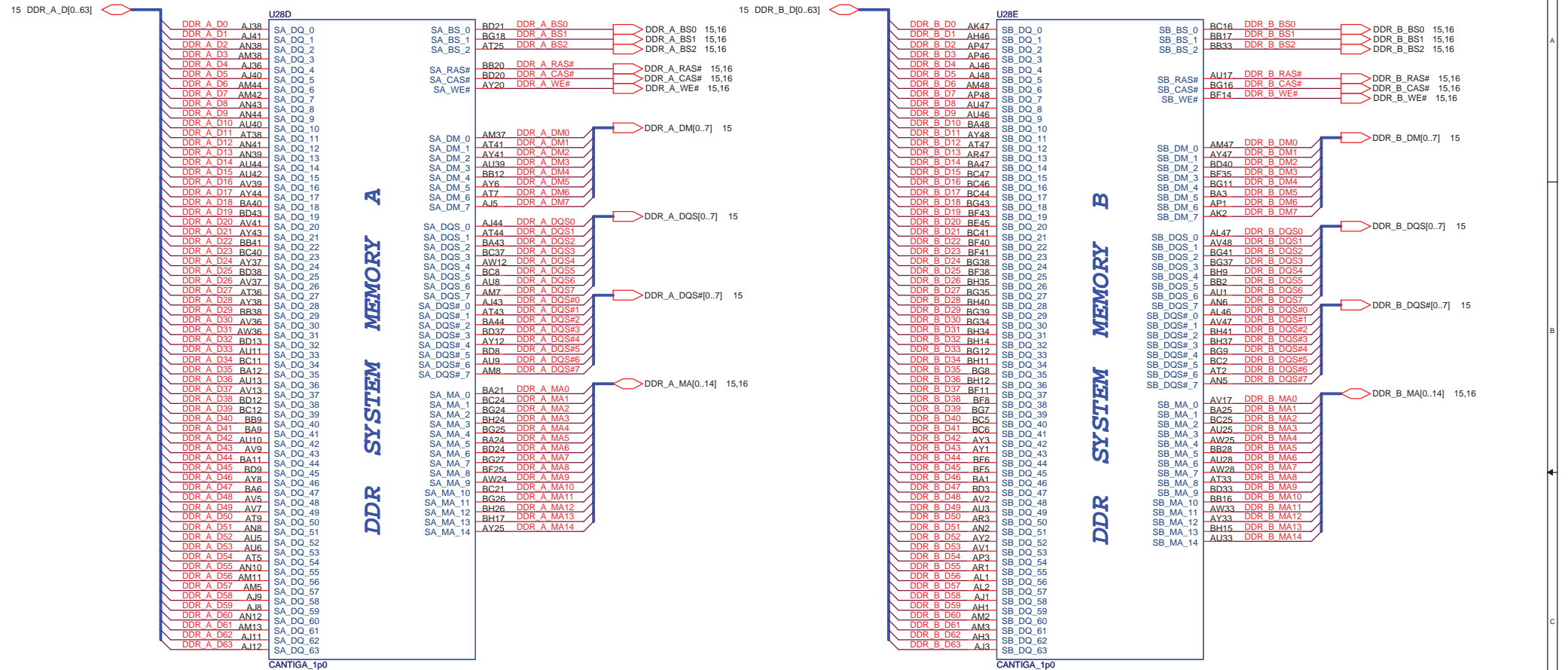
QUANTA COMPUTER

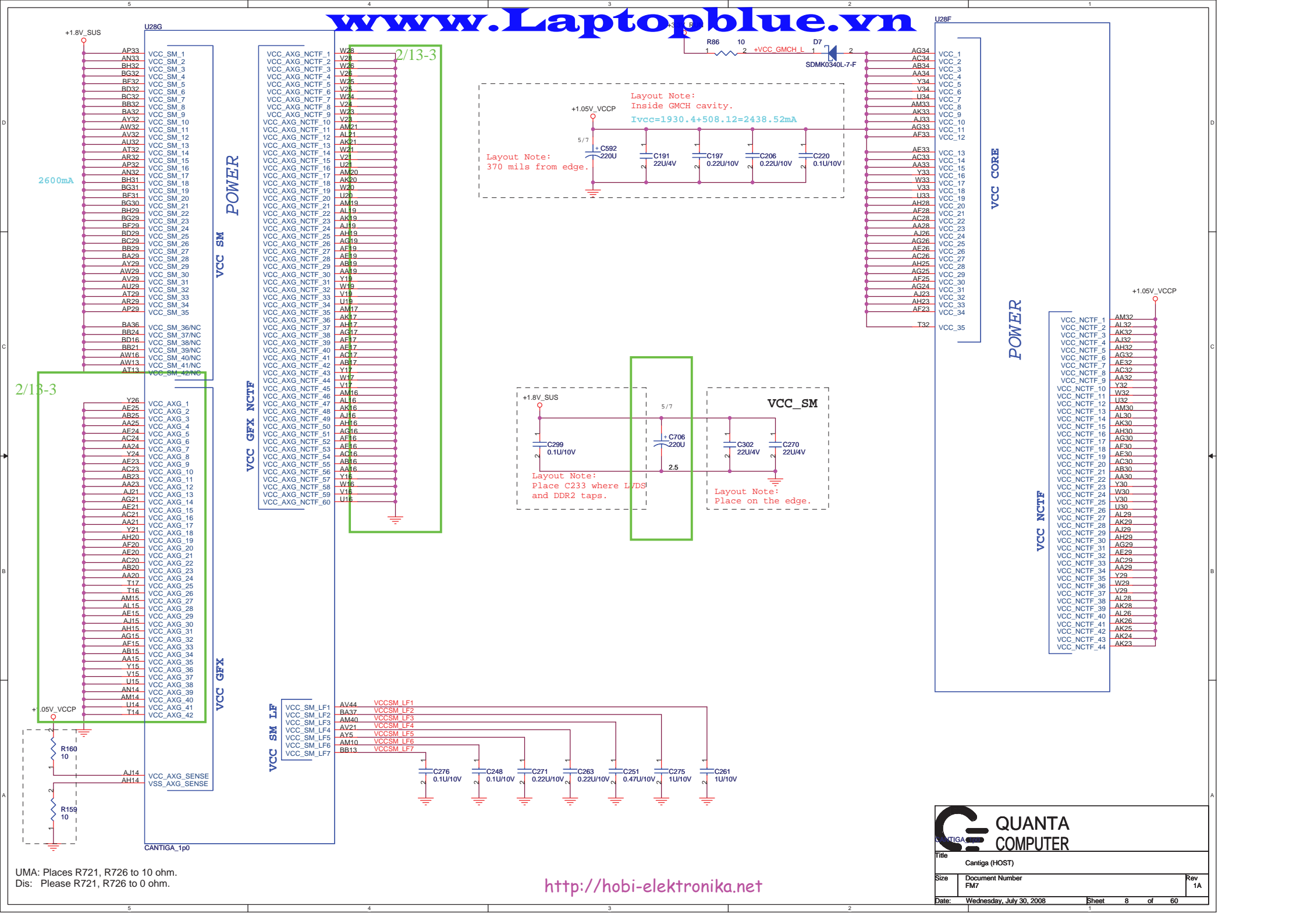
Title: Cantiga (HOST)

Size: Document Number: Rev 1A

Date: Wednesday, July 30, 2008 Sheet 5 of 60







The image displays a detailed PCB layout for the Cantiga (HOST) board. The layout is organized into several functional areas, each with a corresponding component list and pinout information.

POWER

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

VCC CORE

VCC NCTF

Component Lists:

- VCC SM:** AP33, AN33, BH32, BG32, BF32, BD32, BC32, BB32, BA32, AX32, AW32, AV32, AU32, AT32, AR32, AP32, AN32, BH31, BG31, BF31, BD31, BC31, BB31, BA31, AX31, AW31, AV31, AU31, AT31, AR31, AP31, BA36, BB34, BD16, BB21, AW16, AW13, AT13, Y26, AE25, AB25, AA25, AE24, AC24, AA24, Y24, AE23, AC23, AB23, AA23, AJ21, AG21, AE21, AC21, AA21, Y21, AH20, AE20, AC20, AB20, AA20, T17, T16, AM15, AL15, AE15, AJ15, AH15, AG15, AE15, AB15, AA15, Y15, U15, AN14, AM14, U14, T14.
- VCC GFX NCTF:** VCC_AXG_NCTF_1, VCC_AXG_NCTF_2, VCC_AXG_NCTF_3, VCC_AXG_NCTF_4, VCC_AXG_NCTF_5, VCC_AXG_NCTF_6, VCC_AXG_NCTF_7, VCC_AXG_NCTF_8, VCC_AXG_NCTF_9, VCC_AXG_NCTF_10, VCC_AXG_NCTF_11, VCC_AXG_NCTF_12, VCC_AXG_NCTF_13, VCC_AXG_NCTF_14, VCC_AXG_NCTF_15, VCC_AXG_NCTF_16, VCC_AXG_NCTF_17, VCC_AXG_NCTF_18, VCC_AXG_NCTF_19, VCC_AXG_NCTF_20, VCC_AXG_NCTF_21, VCC_AXG_NCTF_22, VCC_AXG_NCTF_23, VCC_AXG_NCTF_24, VCC_AXG_NCTF_25, VCC_AXG_NCTF_26, VCC_AXG_NCTF_27, VCC_AXG_NCTF_28, VCC_AXG_NCTF_29, VCC_AXG_NCTF_30, VCC_AXG_NCTF_31, VCC_AXG_NCTF_32, VCC_AXG_NCTF_33, VCC_AXG_NCTF_34, VCC_AXG_NCTF_35, VCC_AXG_NCTF_36, VCC_AXG_NCTF_37, VCC_AXG_NCTF_38, VCC_AXG_NCTF_39, VCC_AXG_NCTF_40, VCC_AXG_NCTF_41, VCC_AXG_NCTF_42, VCC_AXG_NCTF_43, VCC_AXG_NCTF_44, VCC_AXG_NCTF_45, VCC_AXG_NCTF_46, VCC_AXG_NCTF_47, VCC_AXG_NCTF_48, VCC_AXG_NCTF_49, VCC_AXG_NCTF_50, VCC_AXG_NCTF_51, VCC_AXG_NCTF_52, VCC_AXG_NCTF_53, VCC_AXG_NCTF_54, VCC_AXG_NCTF_55, VCC_AXG_NCTF_56, VCC_AXG_NCTF_57, VCC_AXG_NCTF_58, VCC_AXG_NCTF_59, VCC_AXG_NCTF_60.
- VCC GFX:** Y26, AE25, AB25, AA25, AE24, AC24, AA24, Y24, AE23, AC23, AB23, AA23, AJ21, AG21, AE21, AC21, AA21, Y21, AH20, AE20, AC20, AB20, AA20, T17, T16, AM15, AL15, AE15, AJ15, AH15, AG15, AE15, AB15, AA15, Y15, U15, AN14, AM14, U14, T14.
- VCC SM LF:** VCC_SM_LF1, VCC_SM_LF2, VCC_SM_LF3, VCC_SM_LF4, VCC_SM_LF5, VCC_SM_LF6, VCC_SM_LF7.
- VCC CORE:** VCC_1, VCC_2, VCC_3, VCC_4, VCC_5, VCC_6, VCC_7, VCC_8, VCC_9, VCC_10, VCC_11, VCC_12, VCC_13, VCC_14, VCC_15, VCC_16, VCC_17, VCC_18, VCC_19, VCC_20, VCC_21, VCC_22, VCC_23, VCC_24, VCC_25, VCC_26, VCC_27, VCC_28, VCC_29, VCC_30, VCC_31, VCC_32, VCC_33, VCC_34, VCC_35.
- VCC NCTF:** VCC_NCTF_1, VCC_NCTF_2, VCC_NCTF_3, VCC_NCTF_4, VCC_NCTF_5, VCC_NCTF_6, VCC_NCTF_7, VCC_NCTF_8, VCC_NCTF_9, VCC_NCTF_10, VCC_NCTF_11, VCC_NCTF_12, VCC_NCTF_13, VCC_NCTF_14, VCC_NCTF_15, VCC_NCTF_16, VCC_NCTF_17, VCC_NCTF_18, VCC_NCTF_19, VCC_NCTF_20, VCC_NCTF_21, VCC_NCTF_22, VCC_NCTF_23, VCC_NCTF_24, VCC_NCTF_25, VCC_NCTF_26, VCC_NCTF_27, VCC_NCTF_28, VCC_NCTF_29, VCC_NCTF_30, VCC_NCTF_31, VCC_NCTF_32, VCC_NCTF_33, VCC_NCTF_34, VCC_NCTF_35, VCC_NCTF_36, VCC_NCTF_37, VCC_NCTF_38, VCC_NCTF_39, VCC_NCTF_40, VCC_NCTF_41, VCC_NCTF_42, VCC_NCTF_43, VCC_NCTF_44.

Layout Notes:

- Layout Note: Inside GMCH cavity. $I_{vcc} = 1930.4 + 508.12 = 2438.52 \text{mA}$
- Layout Note: 370 mils from edge.
- Layout Note: Place C233 where L/VDS and DDR2 taps.
- Layout Note: Place on the edge.

UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.

QUANTA COMPUTER

Title: Cantiga (HOST)

Size: FM7

Date: Wednesday, July 30, 2008

Sheet: 8 of 60

Rev: 1A

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POWER

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

VCC CORE

VCC NCTF

UMA: Places R721, R726 to 10 ohm.

Dis: Please R721, R726 to 0 ohm.

http://hobi-elektronika.net

QUANTA COMPUTER

Cantiga (HOST)

Size: FM7

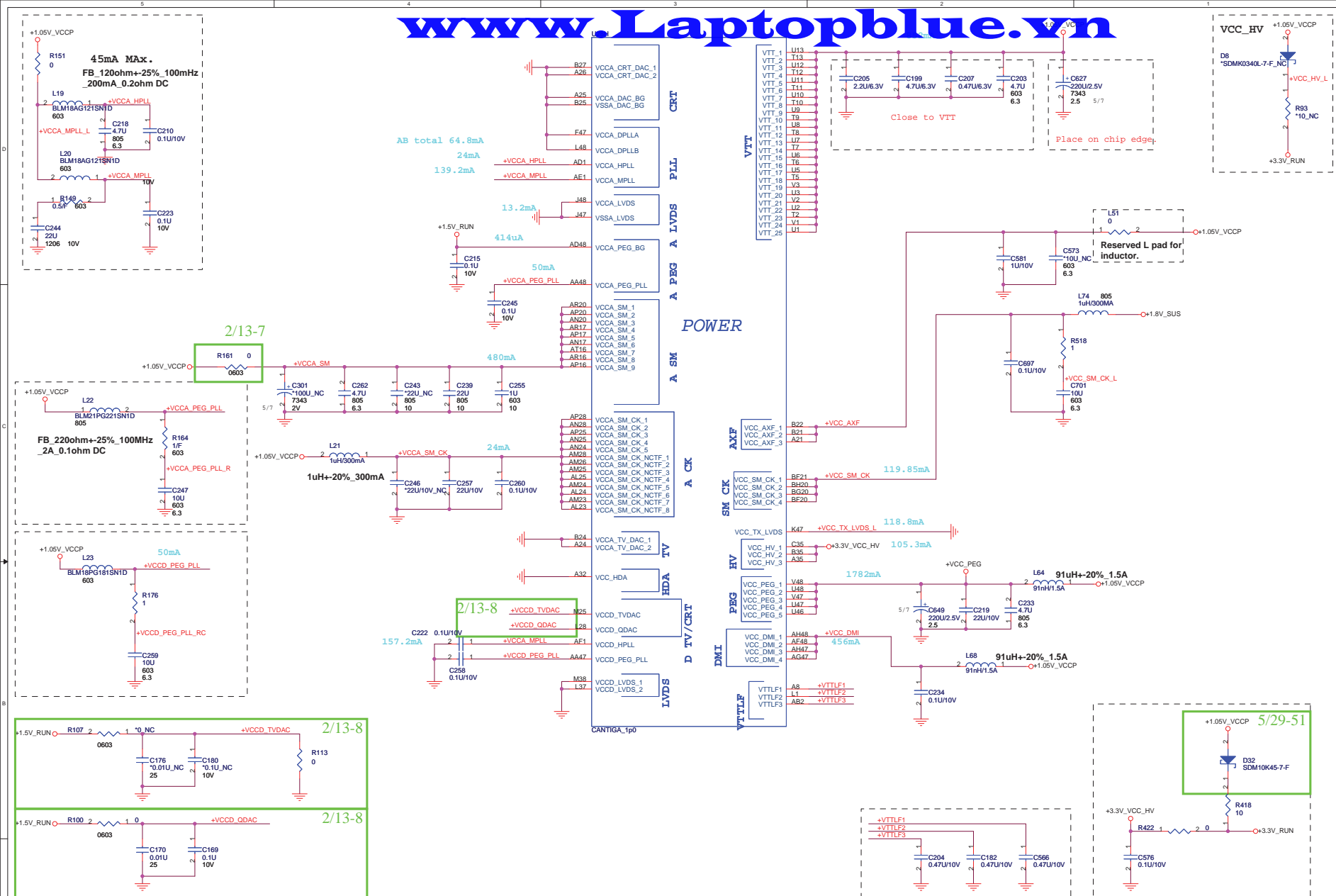
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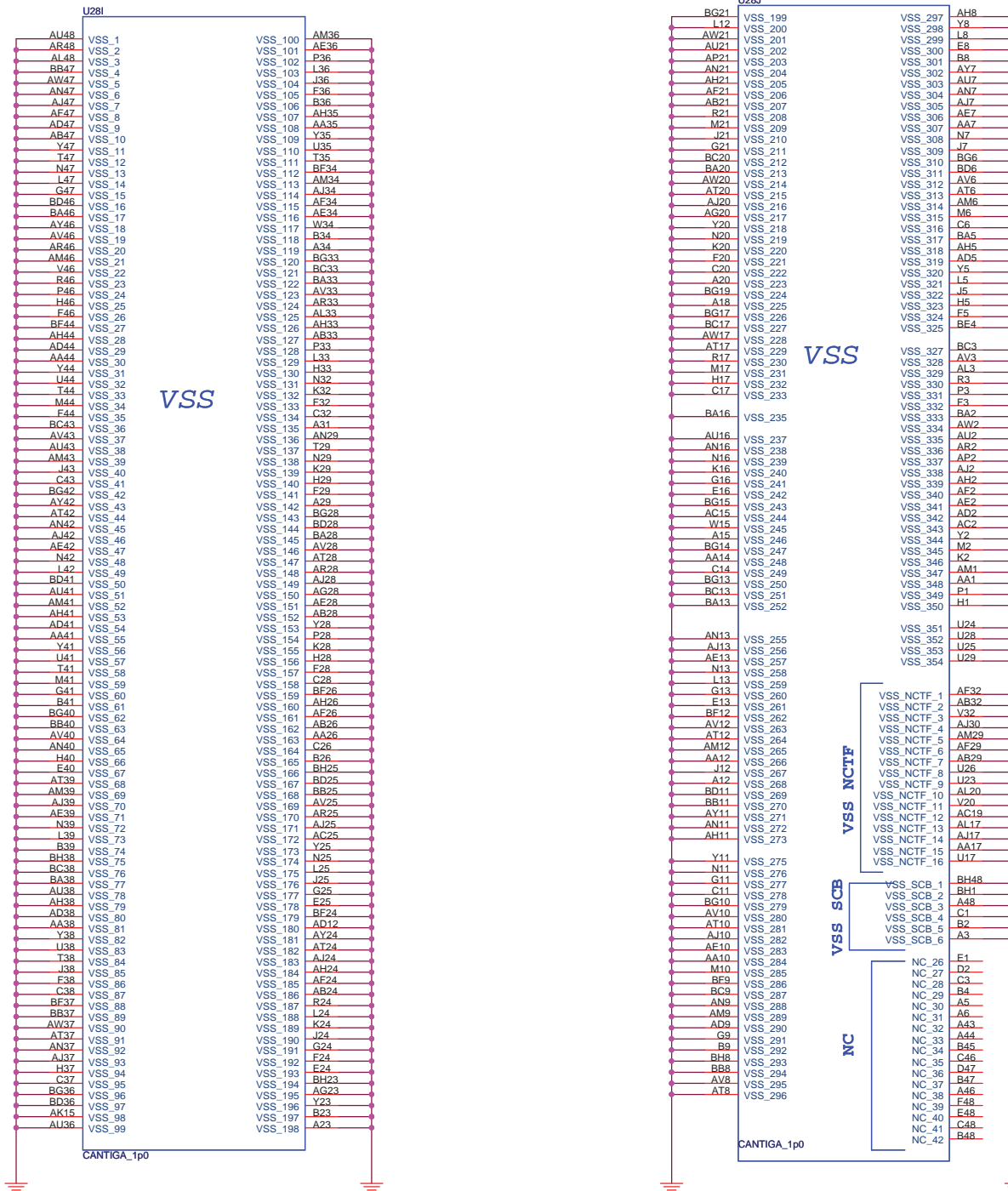
Sheet 8 of 60

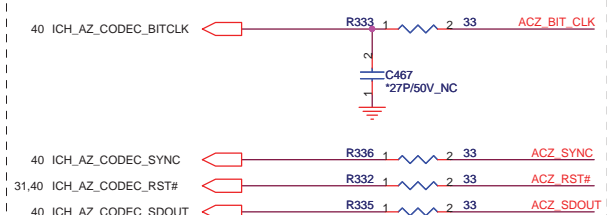
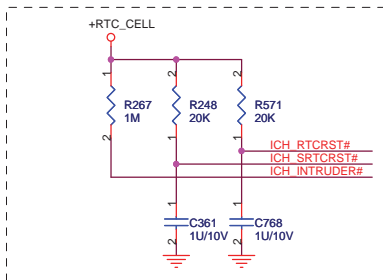
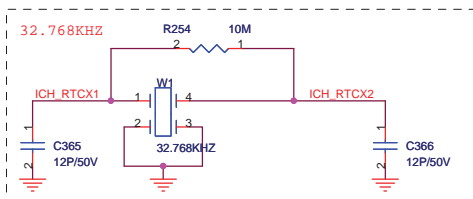
Rev 1A

The image displays a detailed PCB layout for the Cantiga (HOST) board. The layout is organized into several functional areas, each with a corresponding component list and specific design notes.

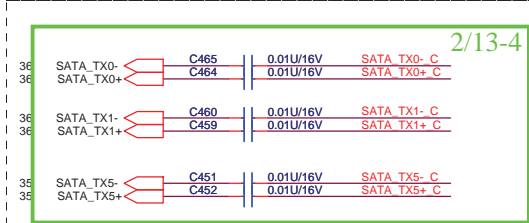
POWER PLANE: The top section shows the power plane layout, including the +1.8V_SUS and +1.05V_VCCP rails. It features a large green area for the power plane and a blue area for the ground plane. The component list for this section includes various capacitors (C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000, C1001, C1002, C1003, C1004, C1005, C1006, C1007, C1008, C1009, C1010, C1011, C1012, C1013, C1014, C1015, C1016, C1017, C1018, C1019, C1020, C1021, C1022, C1023, C1024, C1025, C1026, C1027, C1028, C1029, C1030, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038, C1039, C1040, C1041, C



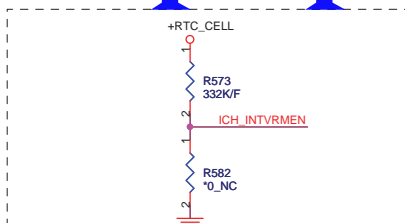




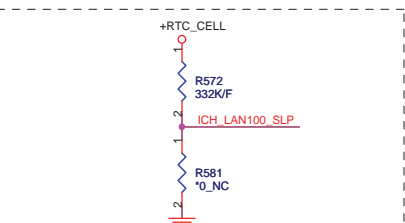
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically, keep the same distance from T for all series termination resistors.



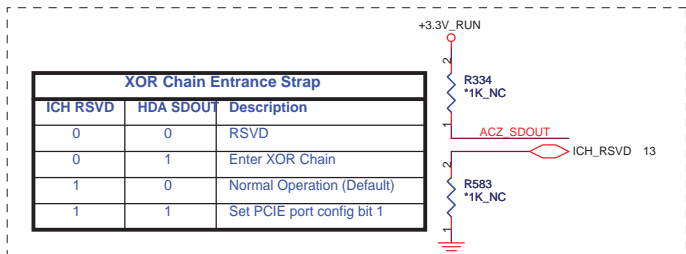
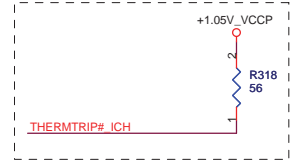
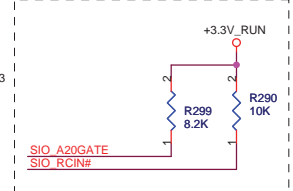
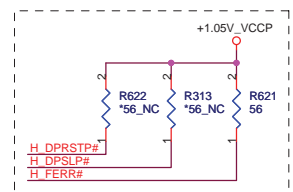
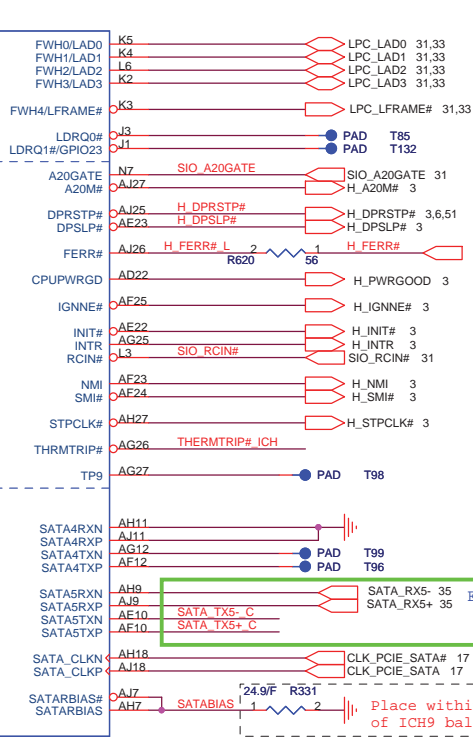
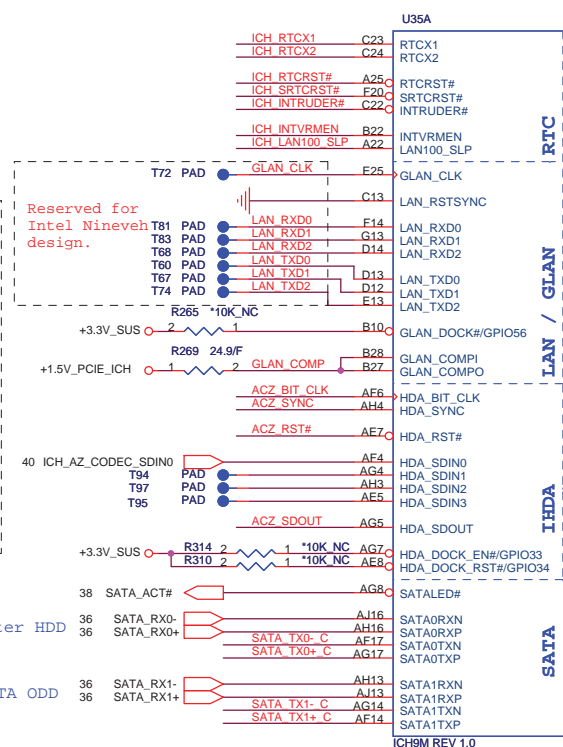
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.



ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



Title	ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)
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Size	
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Document Number
FM7

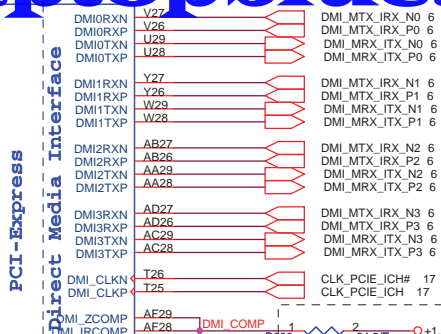
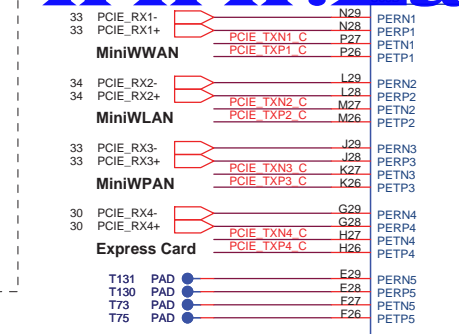
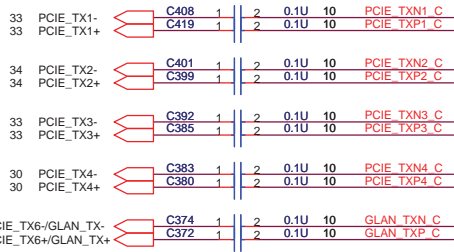
Rev	1A
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Date: Wednesday, July 30, 2008

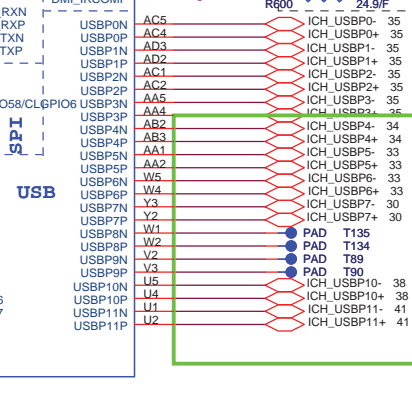
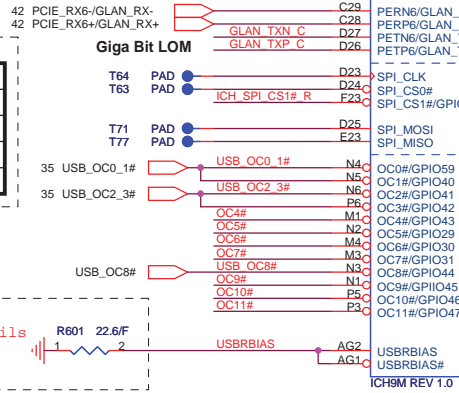
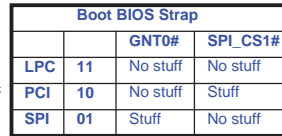
Sheet 11 of 60

<http://hobi-elektronika.net>

Place TX DC blocking caps close ICH8.



Place within 500mils of ICH8



- Side pair Top / left
- Side pair bottom / left
- Side pair top/right(DB)
- Side pair Bot right(DB)
- Mini Card (WLAN)
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card

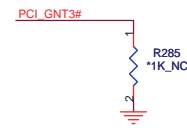
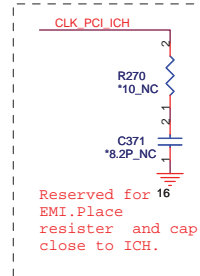
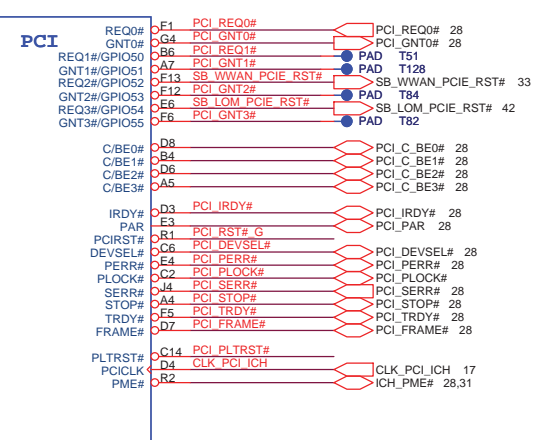
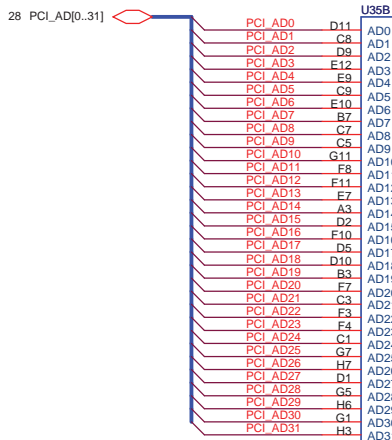
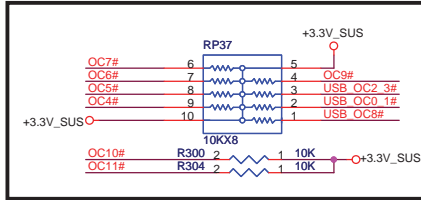
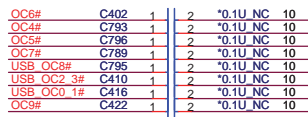
Biometric
Camera

2/25-27

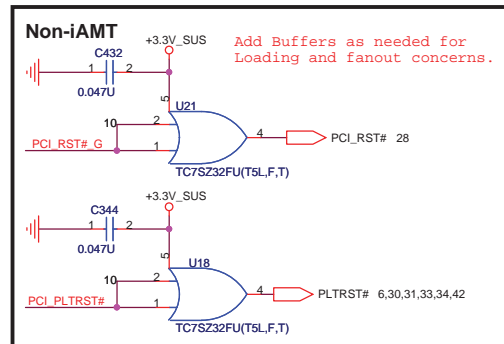
Places within 500 mils
of the ICH9



WWAN Noise - ICH improvements



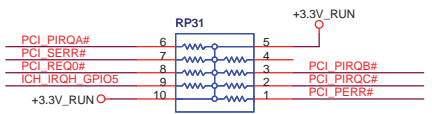
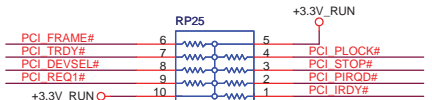
```
16 swap override enabled.  
default.
```



BIOS should not enable the internal GPIO pull up resistor.



PCI Pullups



SB WPAN PCIE RST#	R286	2	1	20K
SB WWAN PCIE RST#	R281	2	1	20K
SB WLAN PCIE RST#	R292	2	1	20K
SB LOM PCIE RST#	R266	2	1	20K
SB NB PCIE RST#	R276	2	1	20K

BIOS should not enable the internal GPIO pull up resistor.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

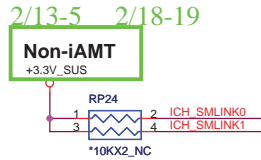
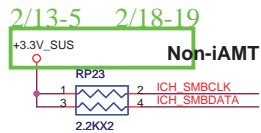


Title	ICH9-M (USB,DMI,PCIE,PCI)
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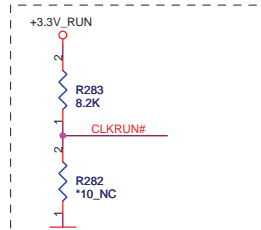
Size	Document Number
	FM7

Date: Wednesday, July 30, 2008 Sheet 12 of 60

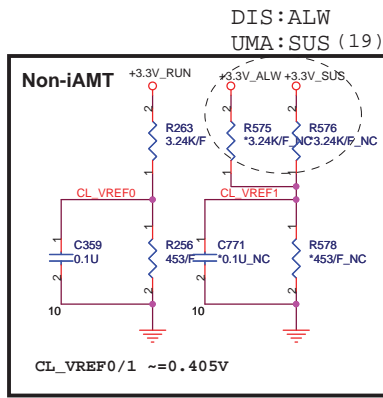
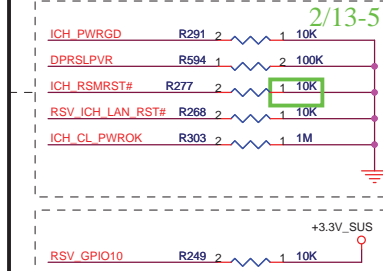
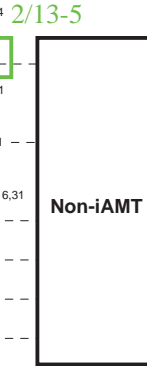
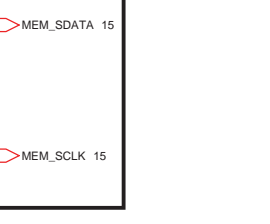
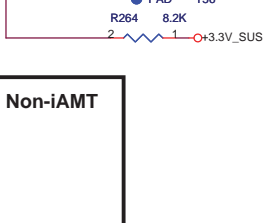
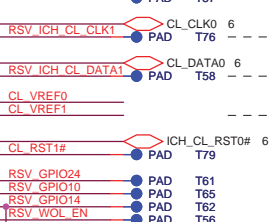
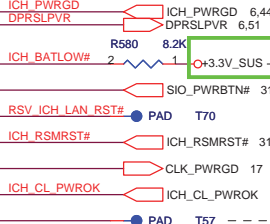
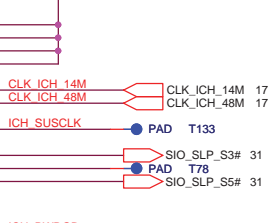
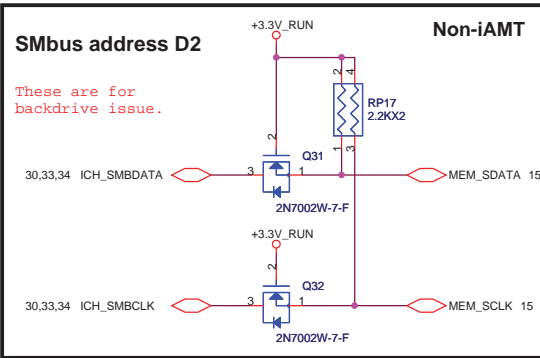
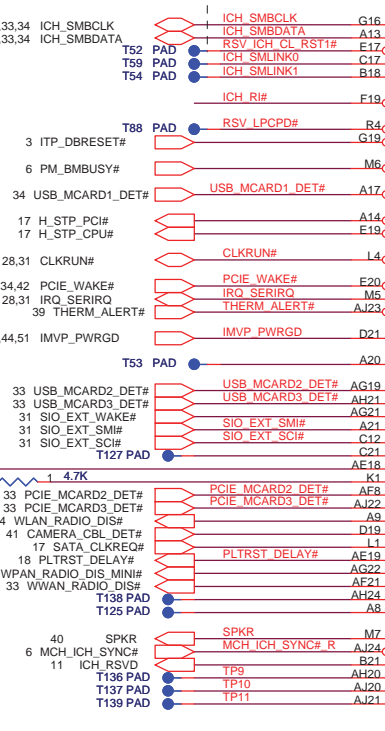
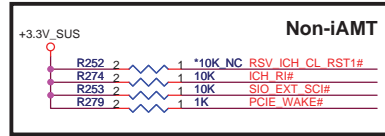
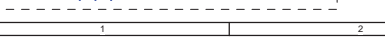
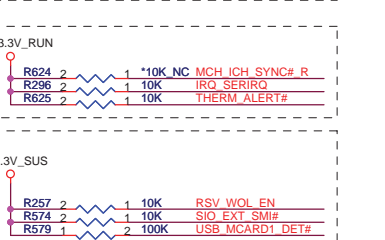
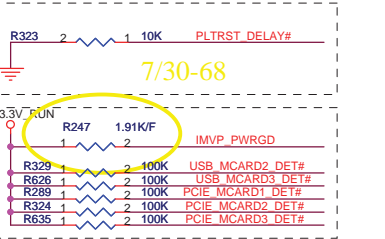
PCI_IRDY#



ASF 2.0



Option to "Disable" clkrun. Pulling it down will keep the clks running.



QUANTA COMPUTER

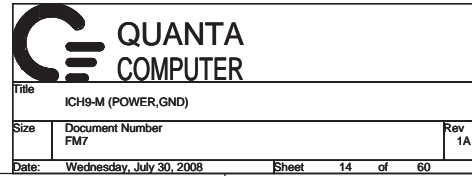
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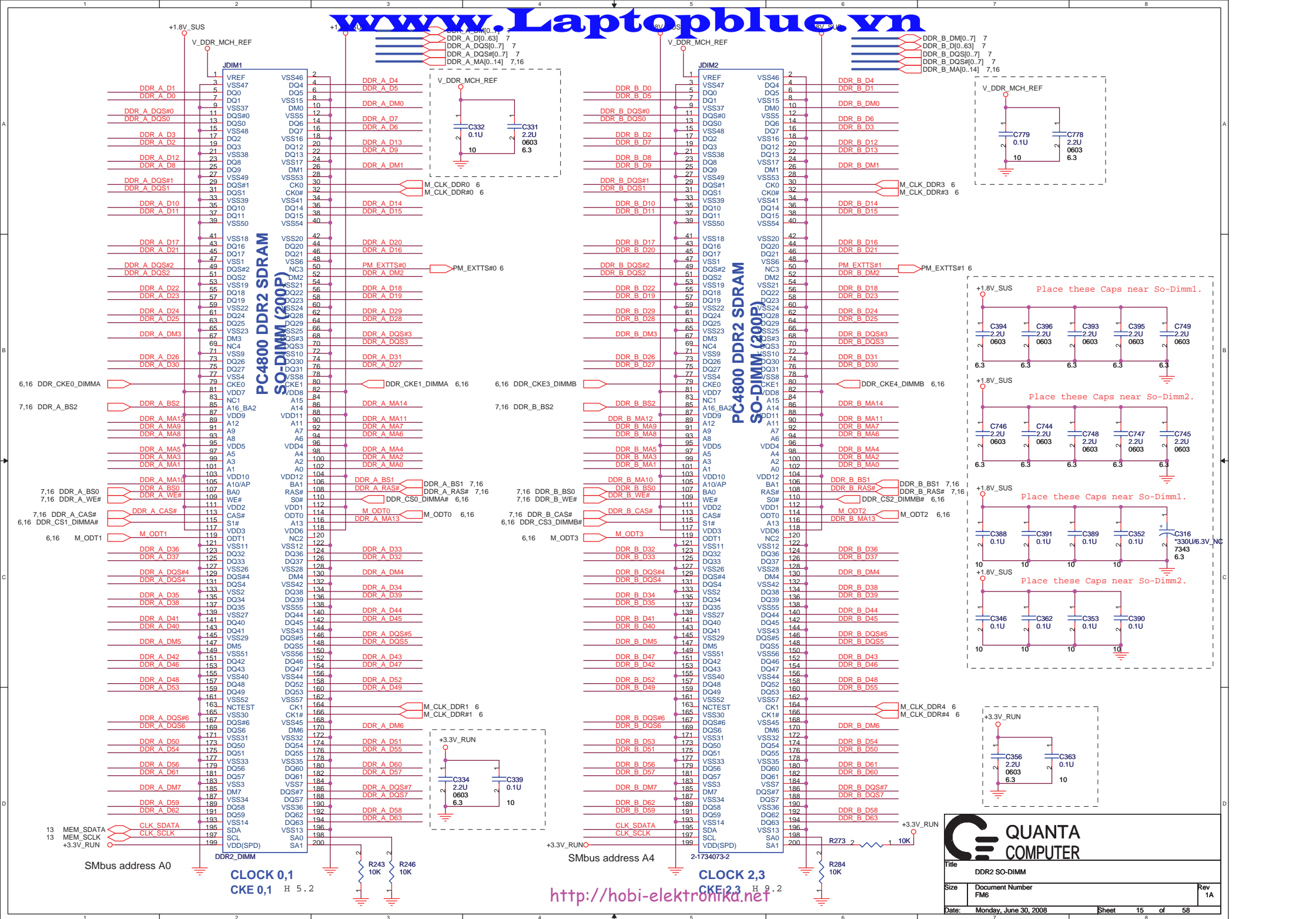
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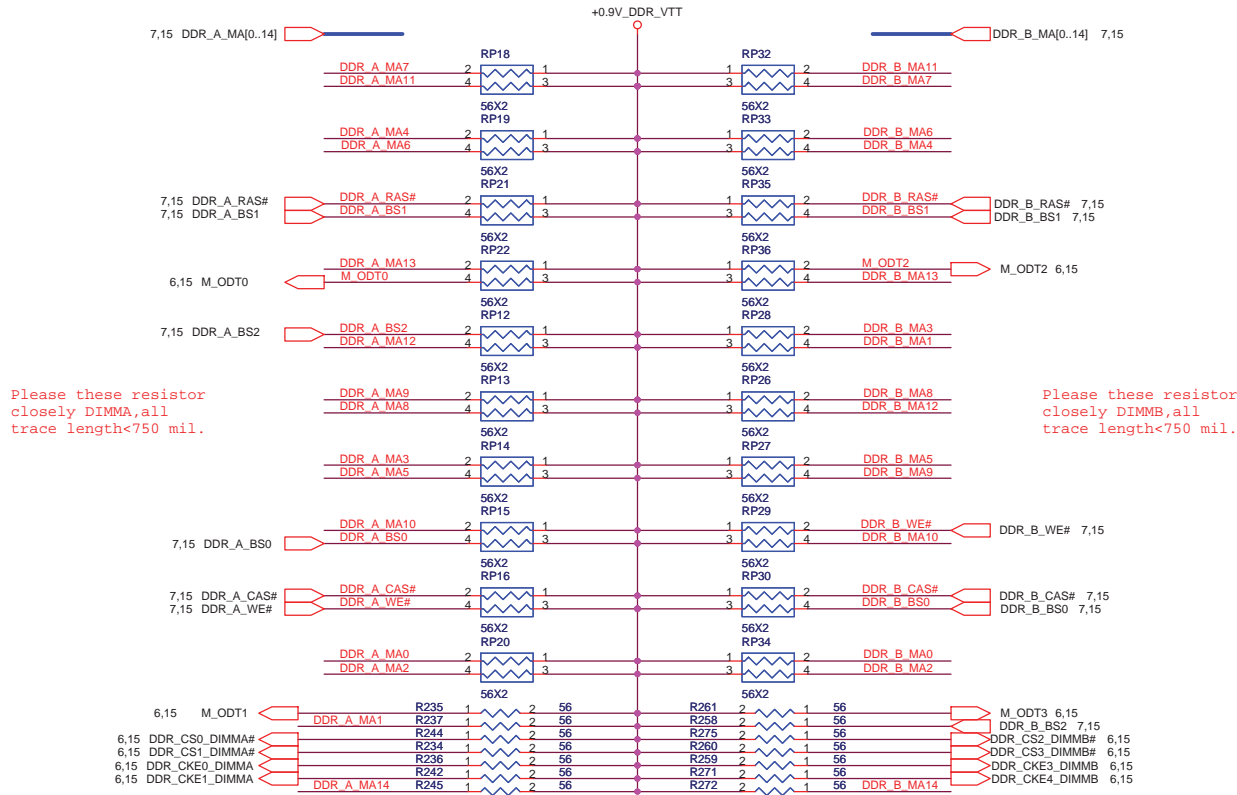
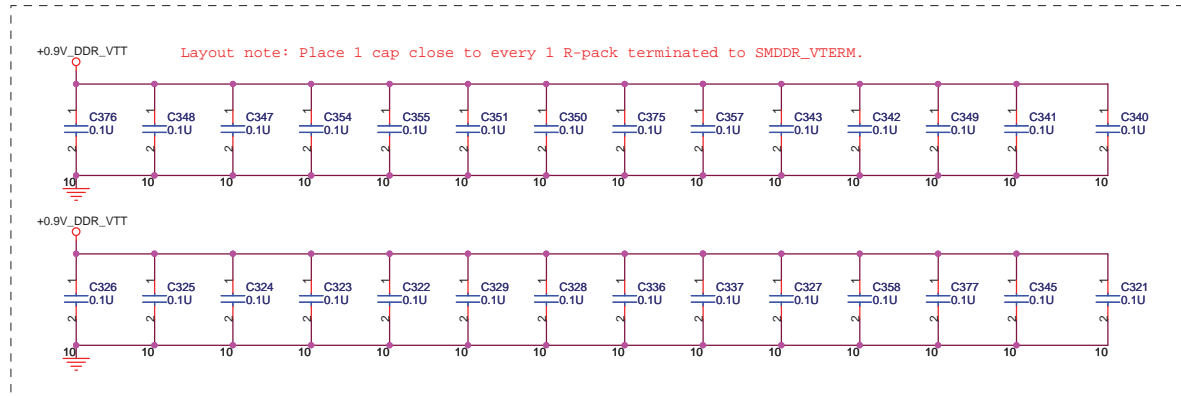
Date: Wednesday, July 30, 2008

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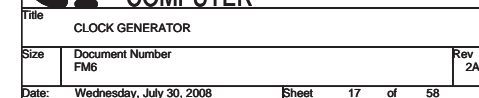
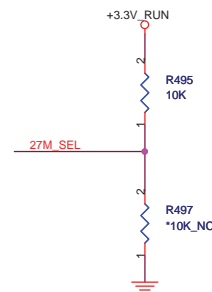
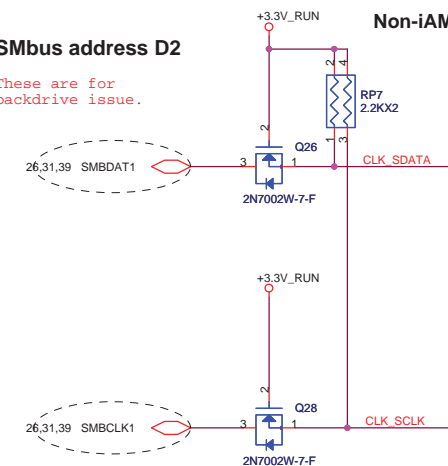
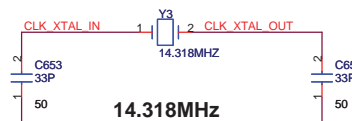
Rev: 1A





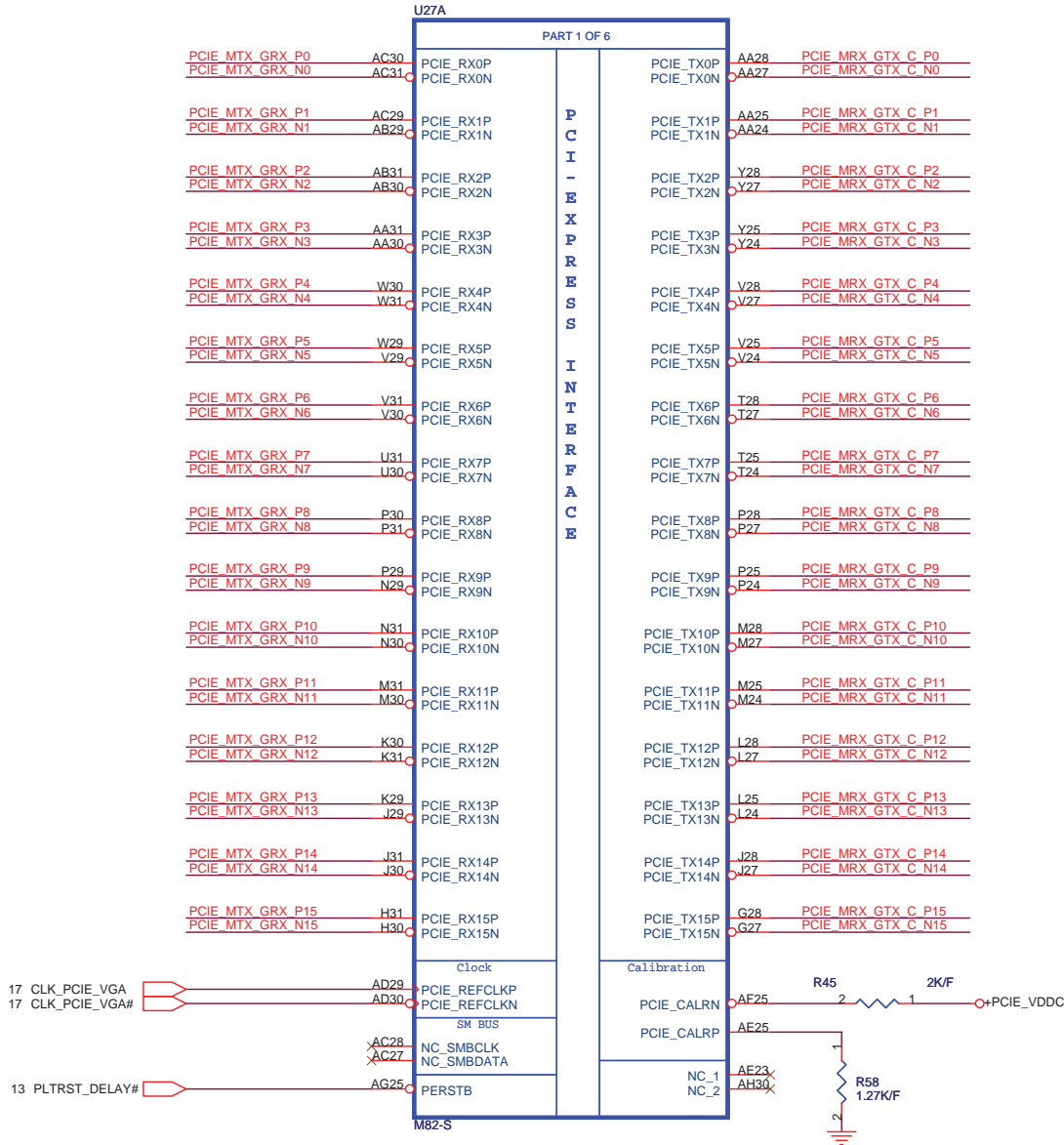


Title: DDR2 RES. ARRAY		
Size: FM6	Document Number: Monday, June 30, 2008	Rev: 1A
Date: Monday, June 30, 2008	Sheet: 16	of 58



6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]



PCIE_MRX_GTX_P0	0.1U	2	1	C83	10	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	0.1U	2	1	C80	10	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	0.1U	2	1	C88	10	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	0.1U	2	1	C84	10	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	0.1U	2	1	C90	10	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	0.1U	2	1	C89	10	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	0.1U	2	1	C107	10	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	0.1U	2	1	C95	10	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	0.1U	2	1	C116	10	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	0.1U	2	1	C108	10	PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10	0.1U	2	1	C128	10	PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11	0.1U	2	1	C120	10	PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12	0.1U	2	1	C150	10	PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13	0.1U	2	1	C130	10	PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14	0.1U	2	1	C157	10	PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15	0.1U	2	1	C151	10	PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0	0.1U	2	1	C81	10	PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1	0.1U	2	1	C82	10	PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2	0.1U	2	1	C86	10	PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3	0.1U	2	1	C87	10	PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4	0.1U	2	1	C94	10	PCIE_MRX_GTX_C_N4
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PCIE_MRX_GTX_N6	0.1U	2	1	C102	10	PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7	0.1U	2	1	C103	10	PCIE_MRX_GTX_C_N7
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PCIE_MRX_GTX_N9	0.1U	2	1	C111	10	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	0.1U	2	1	C125	10	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	0.1U	2	1	C126	10	PCIE_MRX_GTX_C_N11
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PCIE_MRX_GTX_N13	0.1U	2	1	C135	10	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	0.1U	2	1	C156	10	PCIE_MRX_GTX_C_N14
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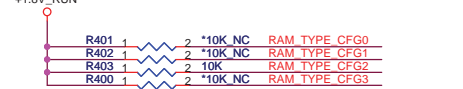
Title			VGA-M82-S (PCIe)
Size	Document Number	Rev	
	FM7	1A	
Date:	Wednesday, July 30, 2008	Sheet	18 of 58

+3.3V_DELAY

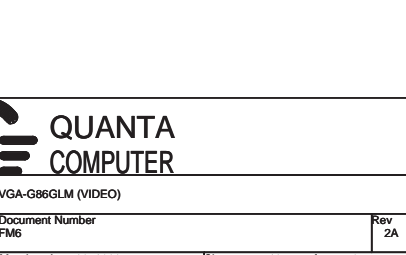
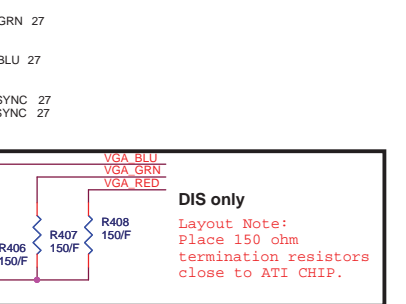
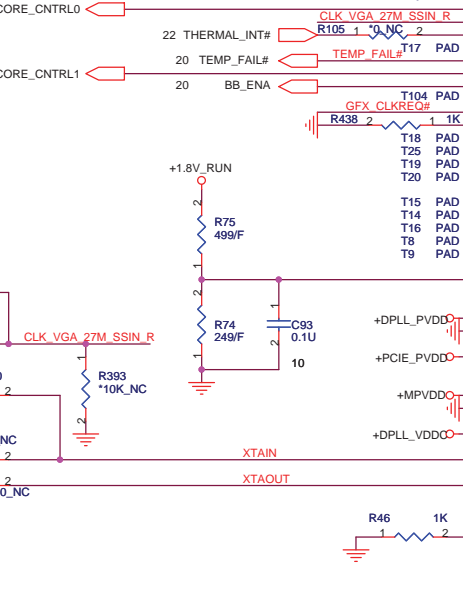
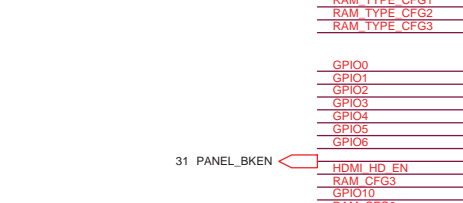
Component	Pin 1	Pin 2	Value	Function
R431	1	2	10K	RAM_CFG0
R432	1	2	*10K_NC	RAM_CFG1
R433	1	2	*10K_NC	RAM_CFG2
R96	1	2	*10K_NC	RAM_CFG3

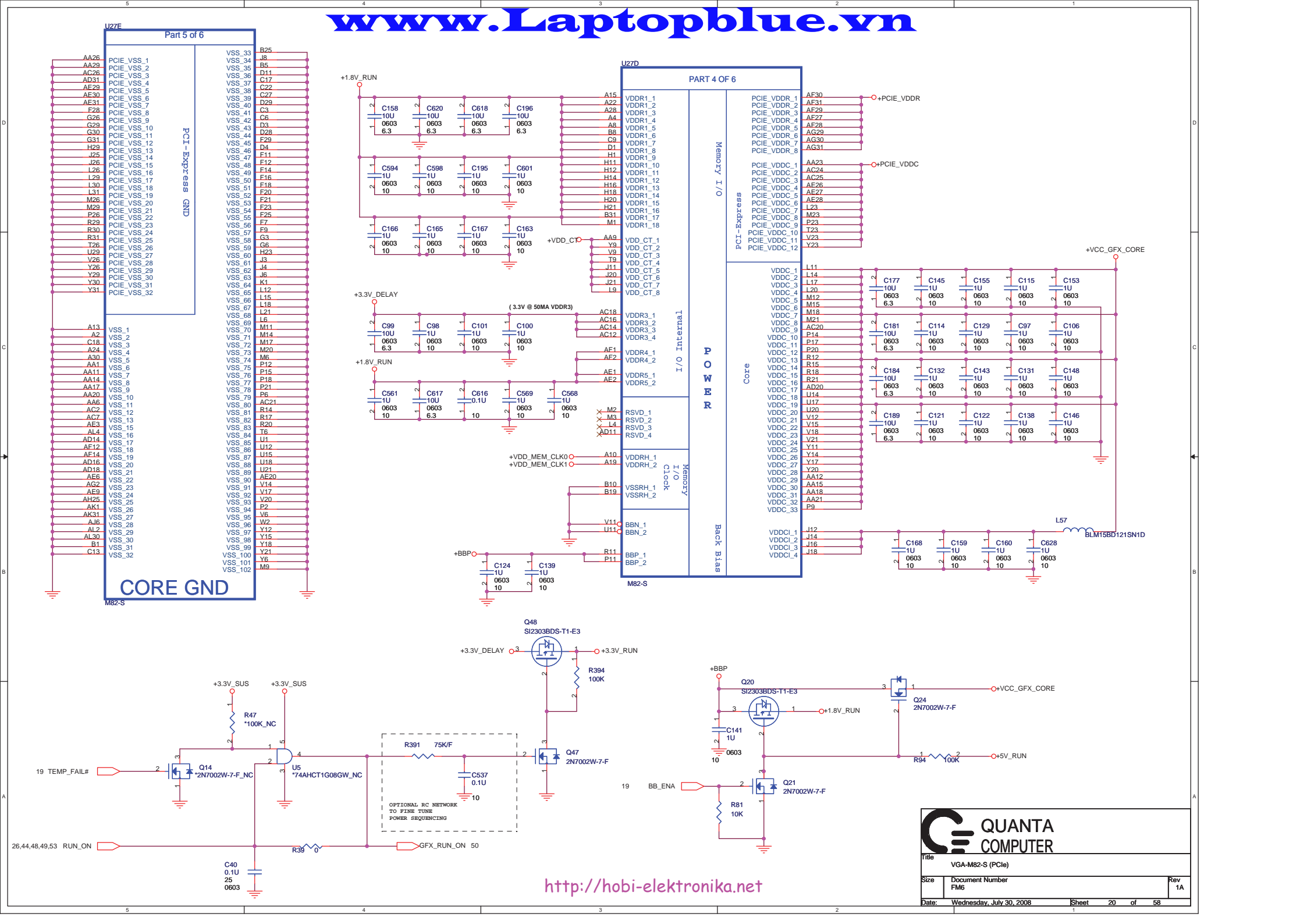
+1.8V_RUN

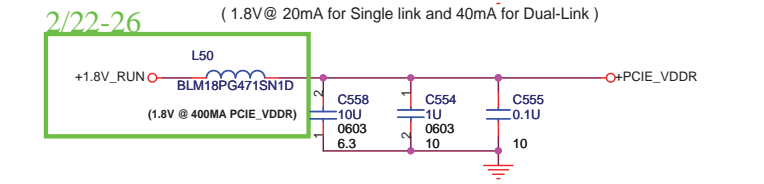
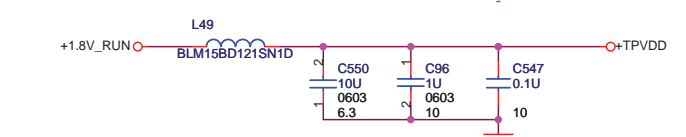
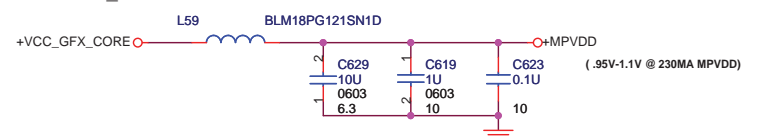
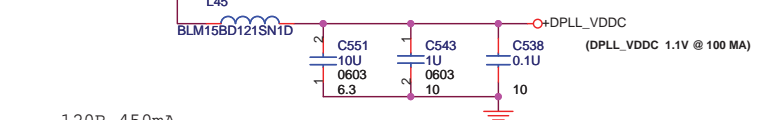
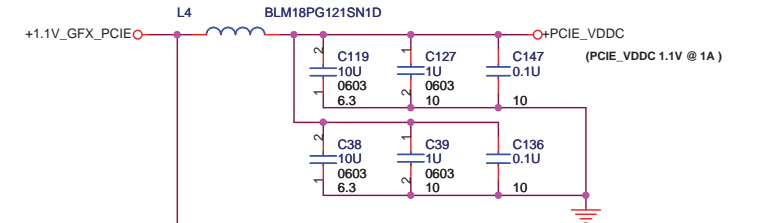
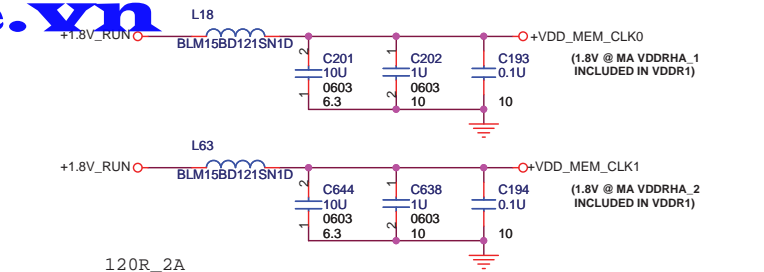
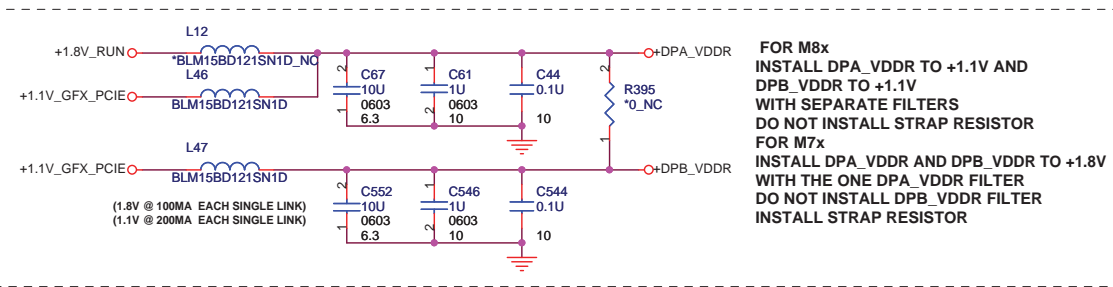
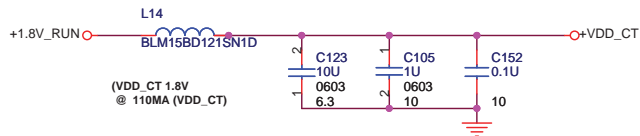
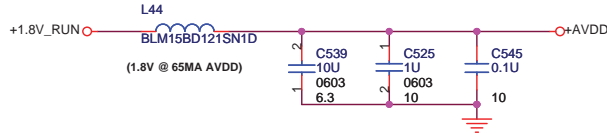
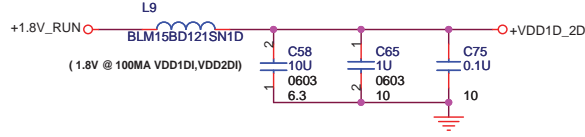
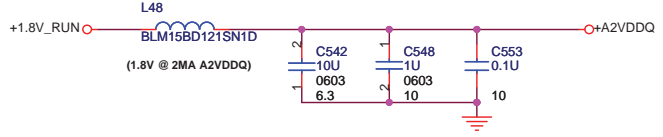
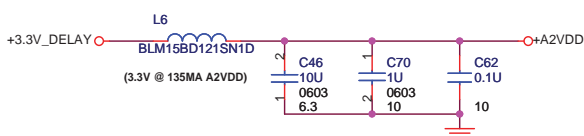
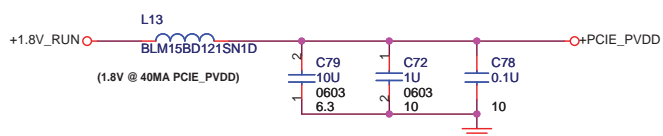
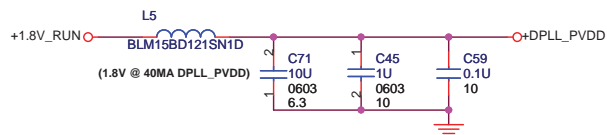
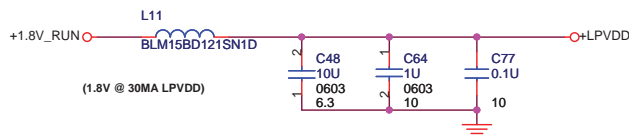
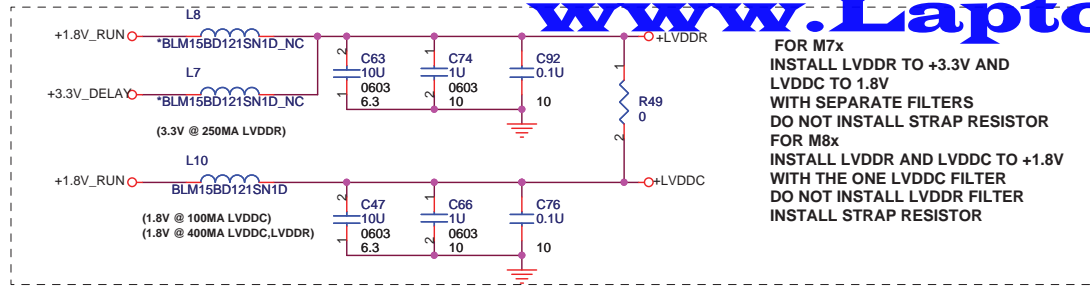
Component	Pin 1	Pin 2	Value	Function
R401	1	2	*10K NC	RAM TYPE CFG0
R402	1	2	*10K NC	RAM TYPE CFG1
R403	1	2	10K	RAM TYPE CFG2
R400	1	2	*10K NC	RAM TYPE CFG3



ATI Usage recommended settings	0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)
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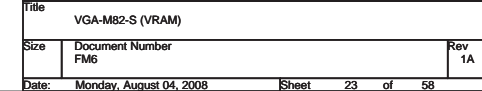





PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

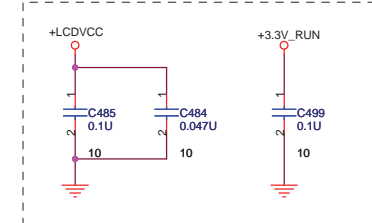
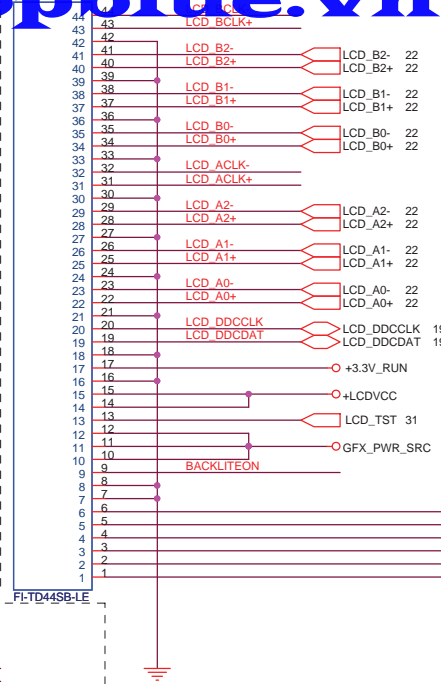
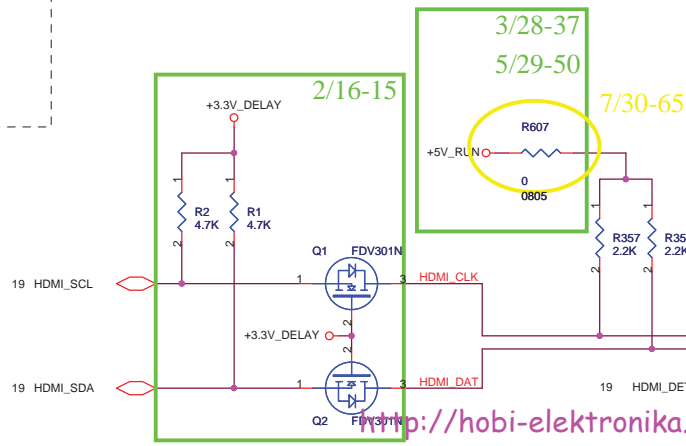
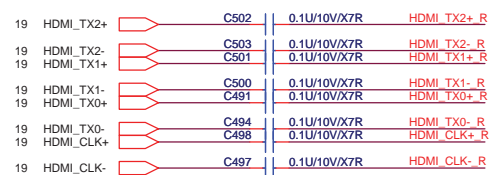
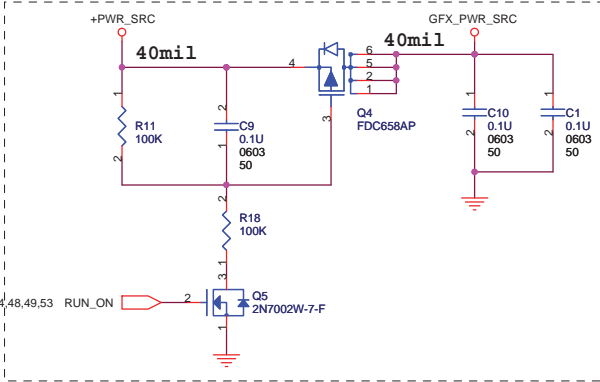
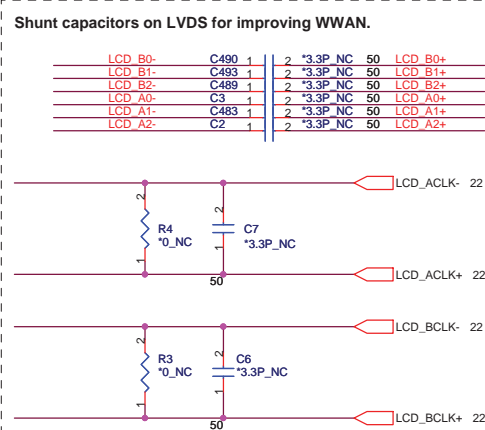
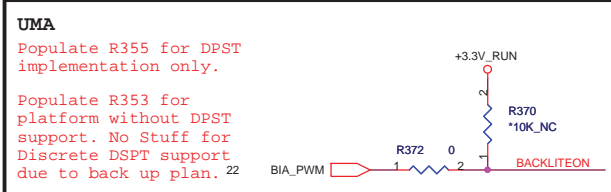
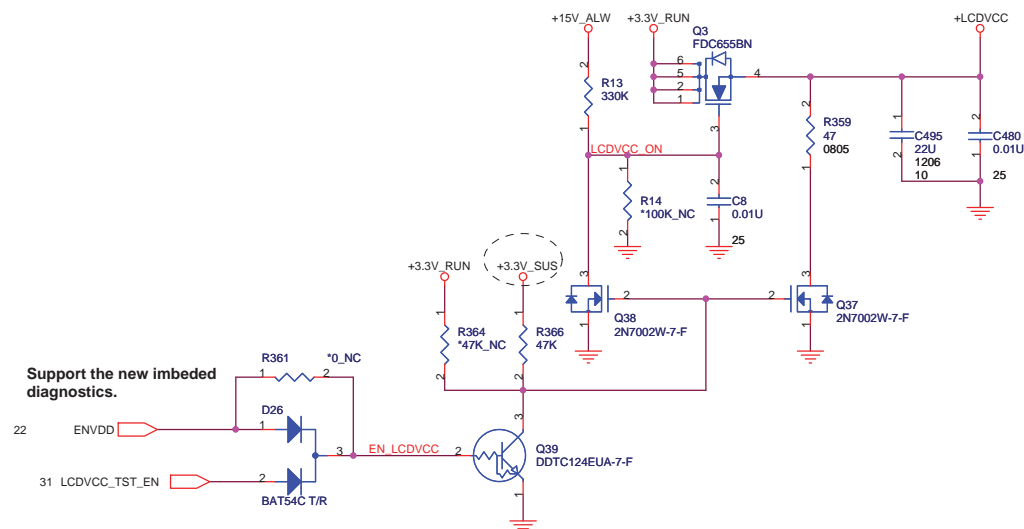
Title	VGA-M82-S (PCIe)	
Size	Document Number FM6	Rev 1A
Date:	Monday, June 30, 2008	Sheet 21 of 58



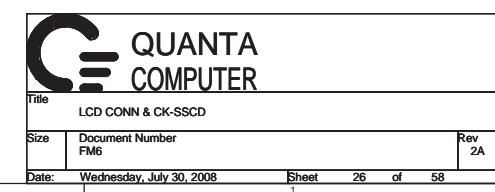
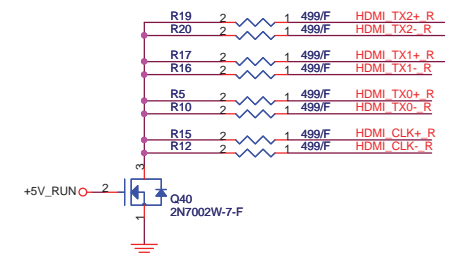
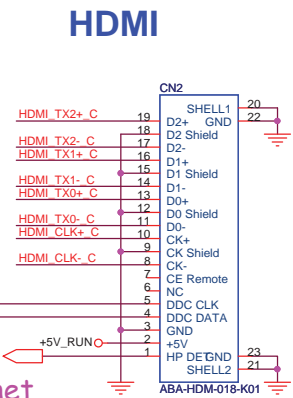
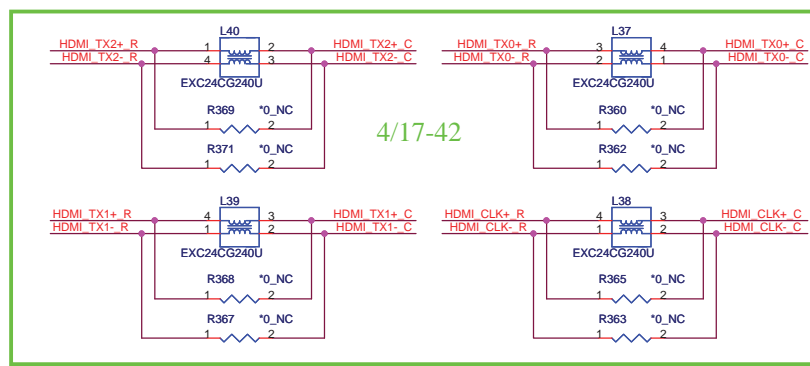


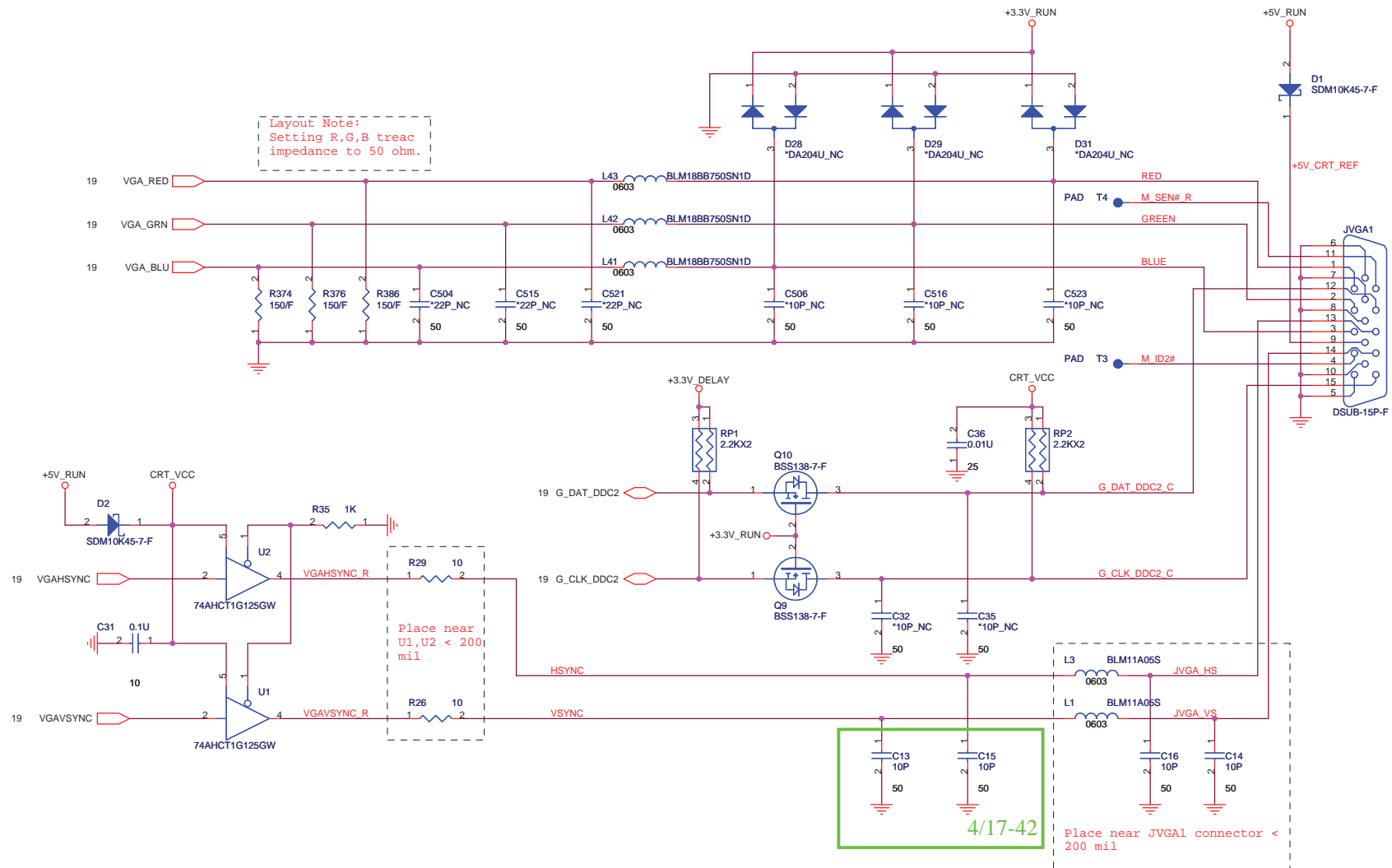
GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings		0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)	

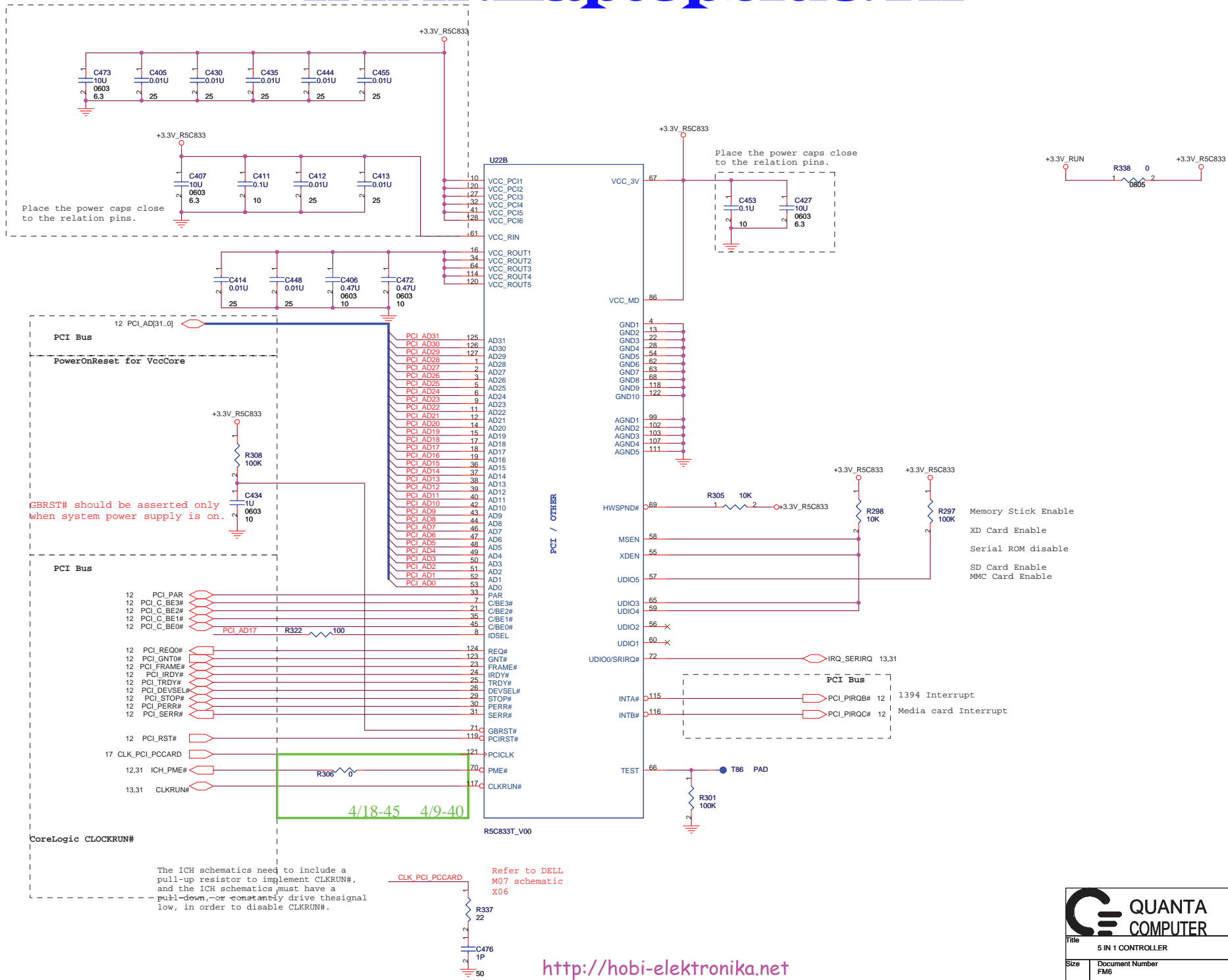
		QUANTA COMPUTER	
Title		VGA-M82-S (PCIe)	
Size	Document Number		Rev
FM6			1A
Date: Monday, June 30, 2008		Sheet	25 of 58

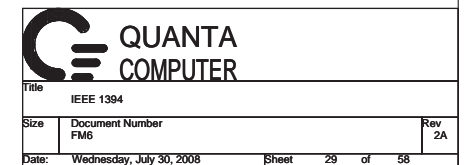


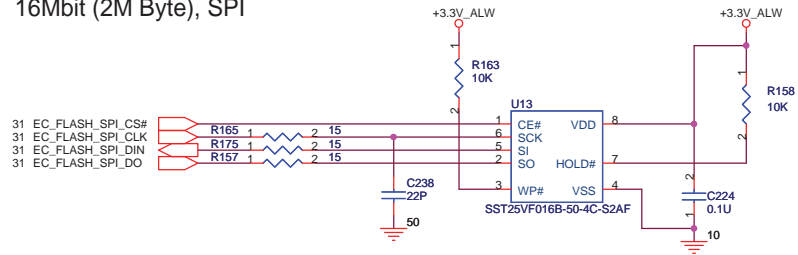
Adress : A9H --Contrast
AAH --Backlight



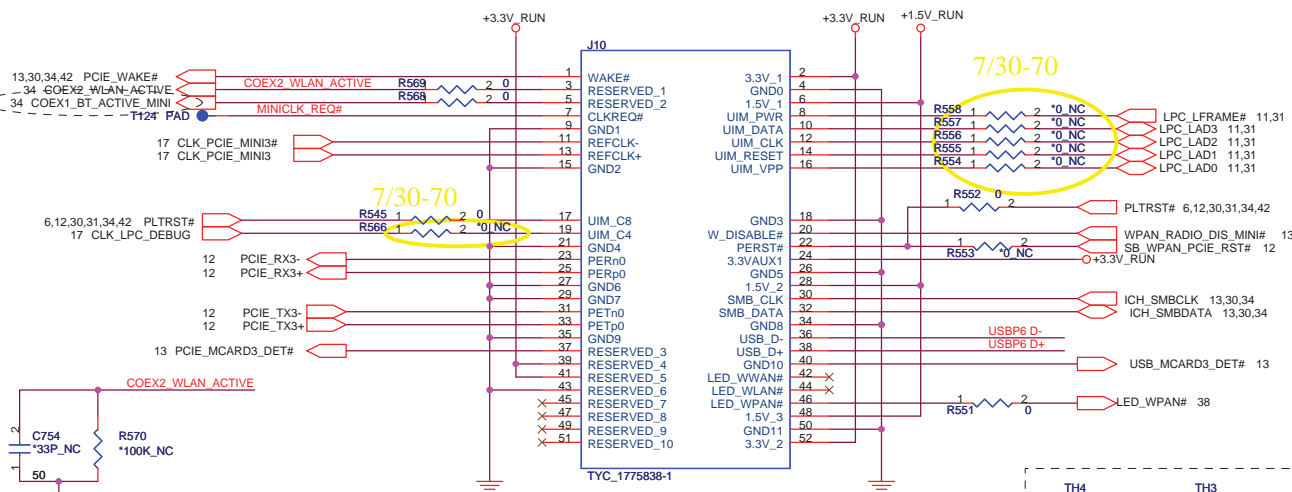




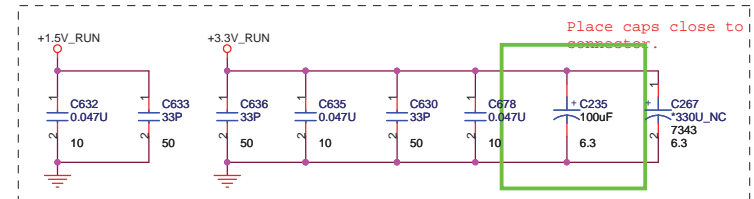
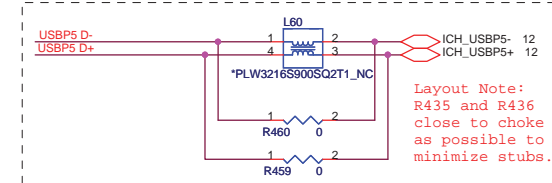
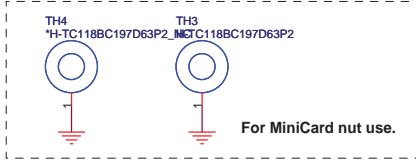
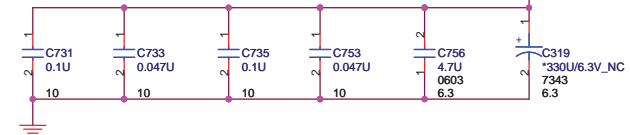
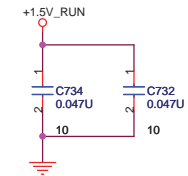
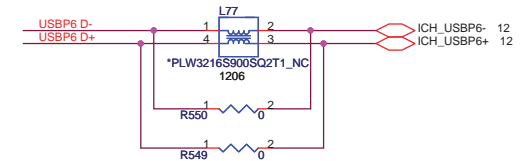
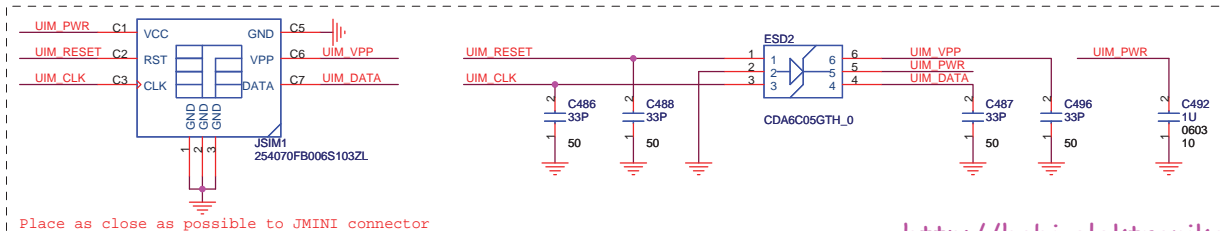
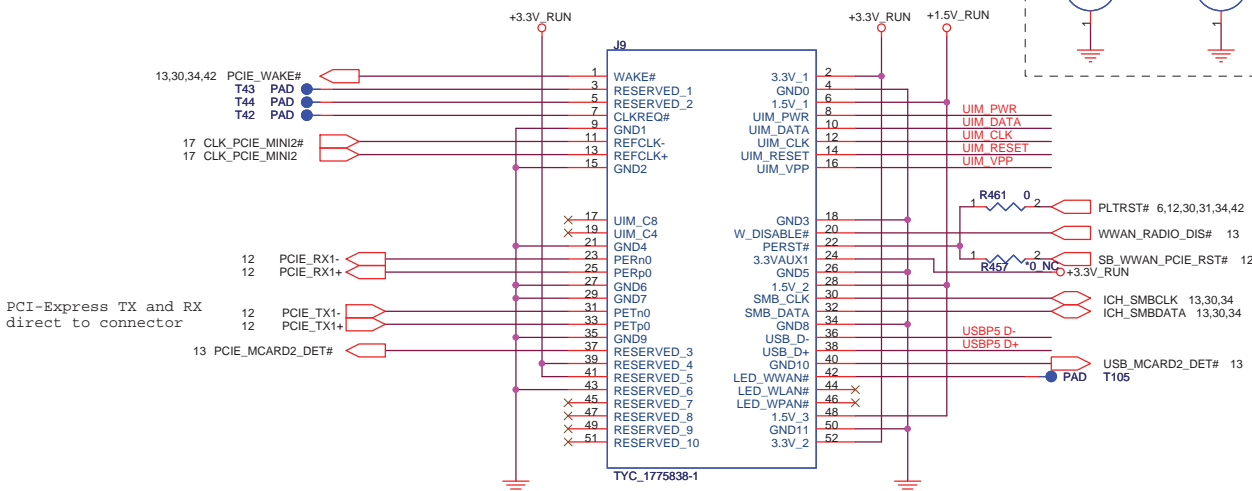




MiniCard Robson, BT. UWB connector



MiniCard WWAN connector

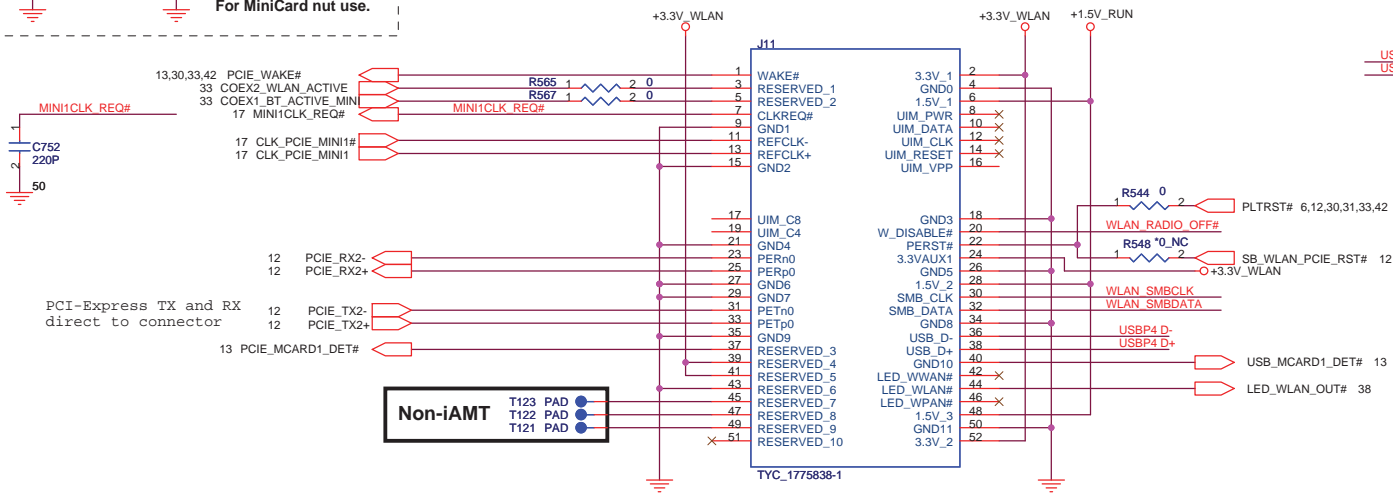


TH2
*H-TC177BC197D83P2_NCH-TC177BC197D83P2

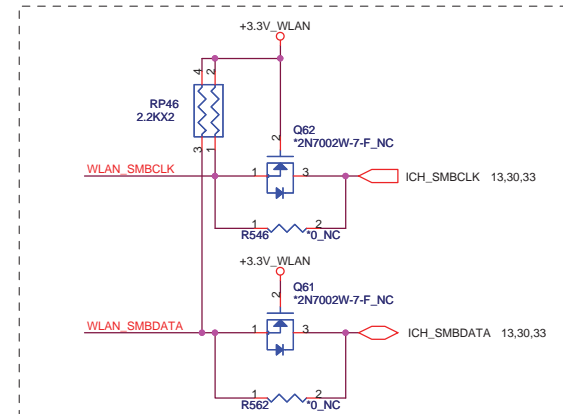
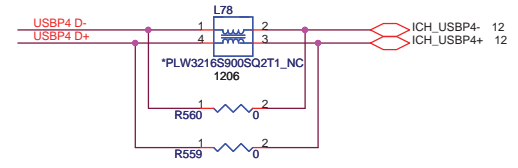


For MiniCard nut use.

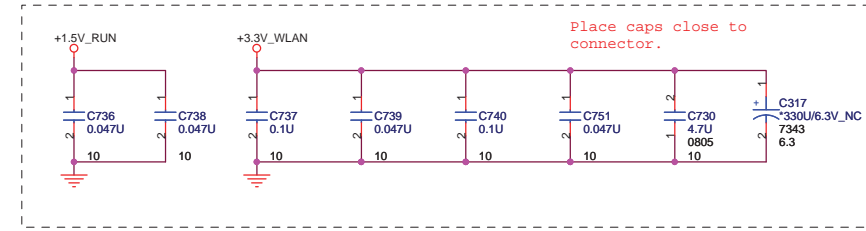
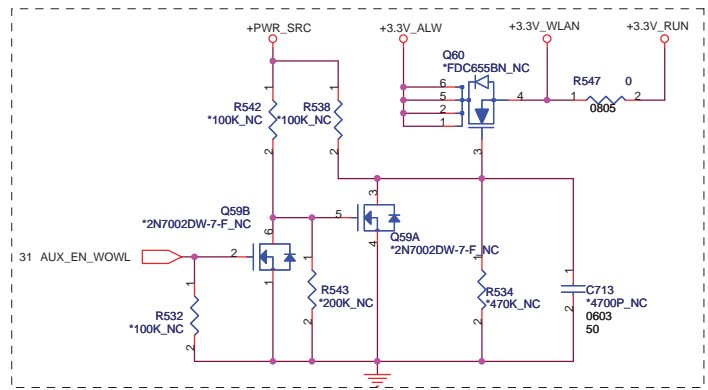
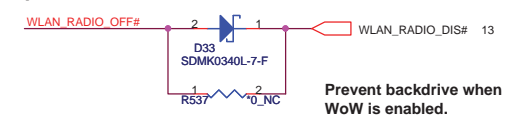
MiniCard WLAN connector




Non-iAMT
T123 PAD
T122 PAD
T121 PAD



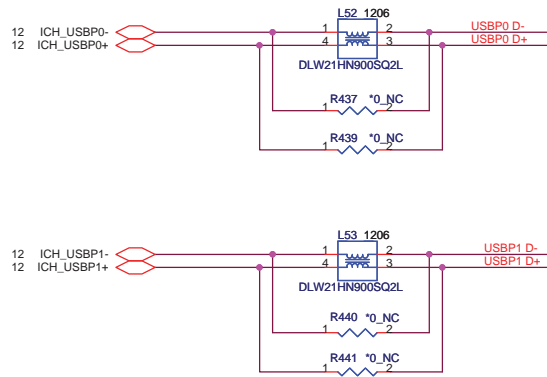
Support for WoW



**QUANTA
COMPUTER**

Title MDC CONN.		
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Date:	Friday, August 01, 2008	Sheet 34 of 58

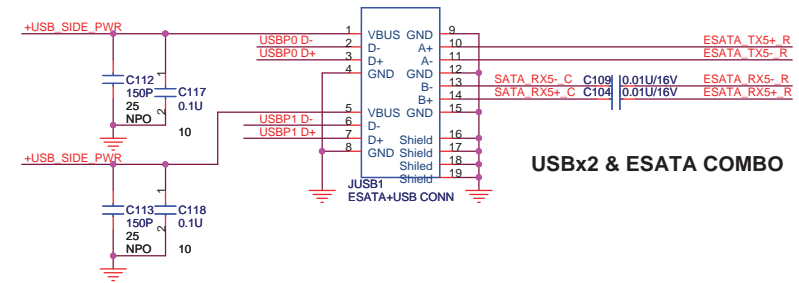
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



2/22-25
4/17-42

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Side External USBX2

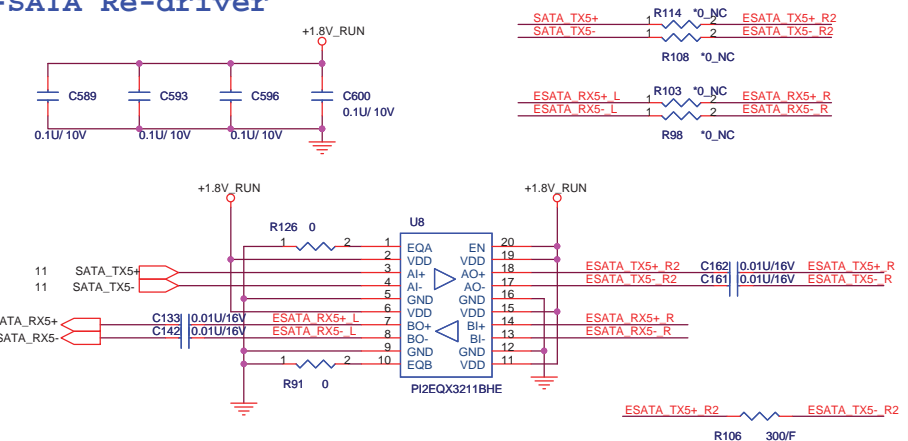


USBx2 & ESATA COMBO

5/29-52

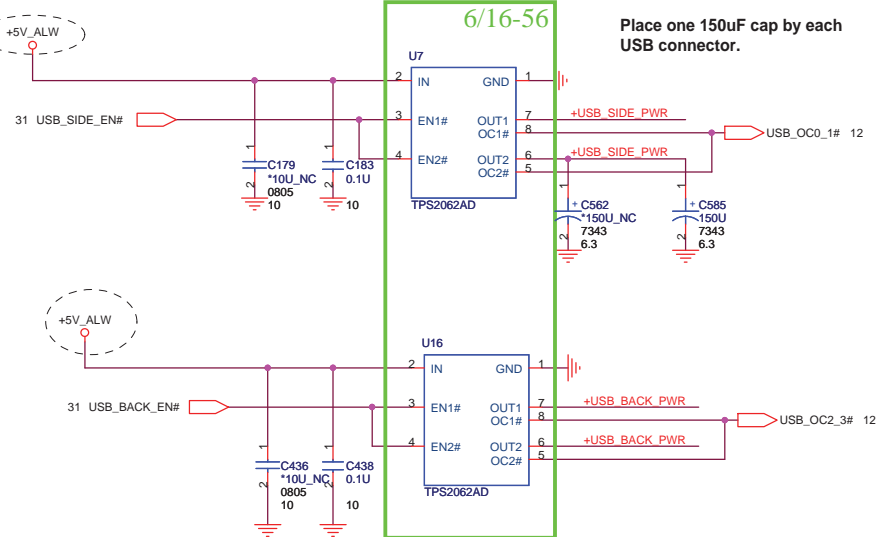
2/20-22

E-SATA Re-driver



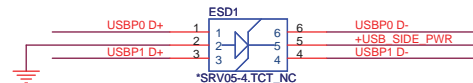
6/16-56

Place one 150uF cap by each USB connector.

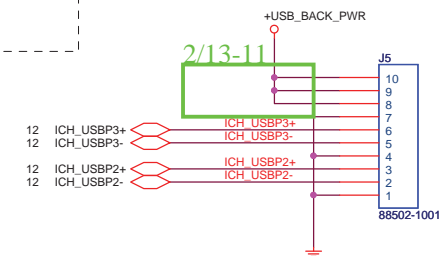


Each channel is 1A

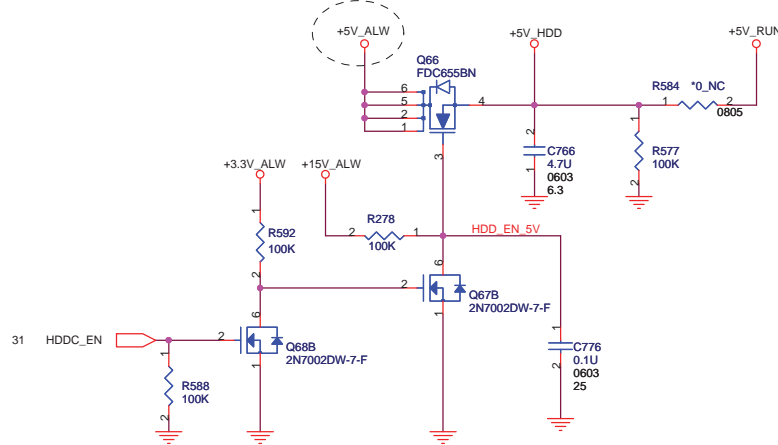
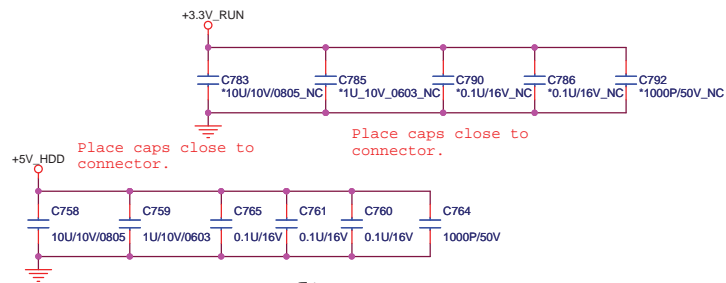
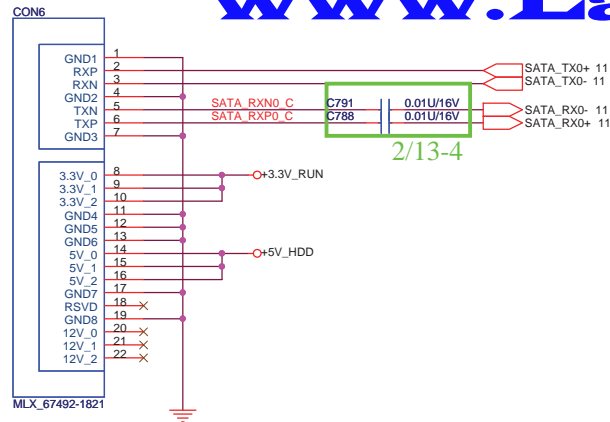
Place ESD diodes as close as USB connector.



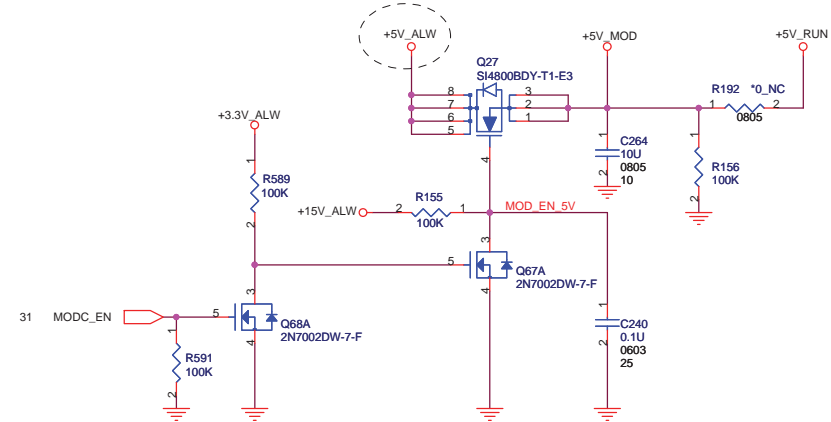
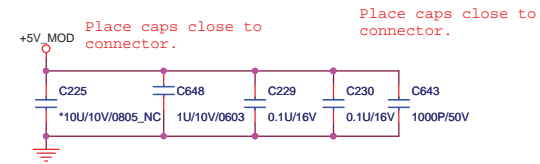
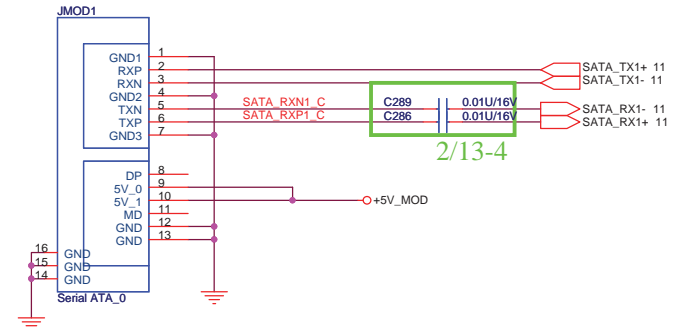
MB side



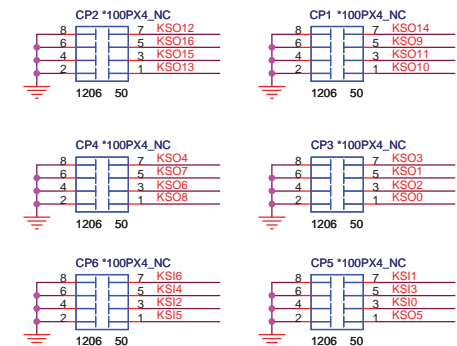
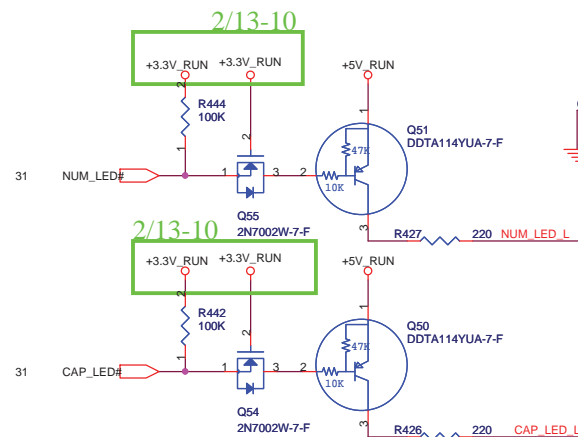
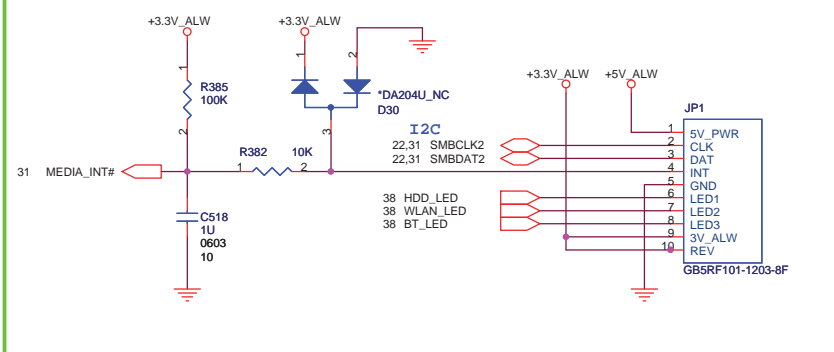
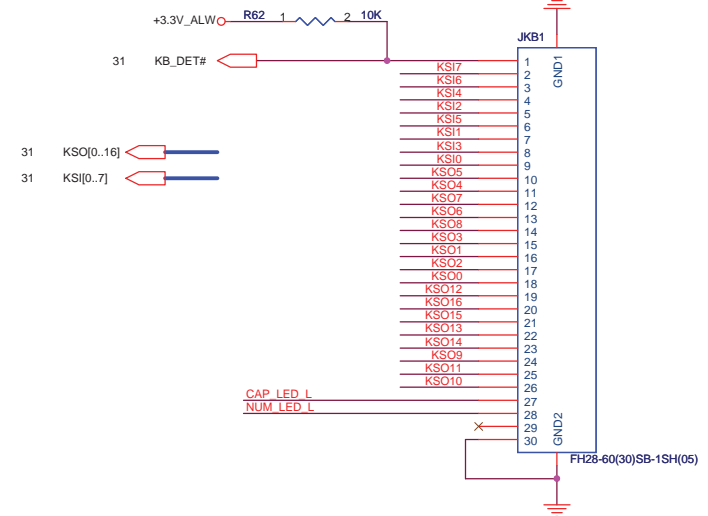
SATA Connector.



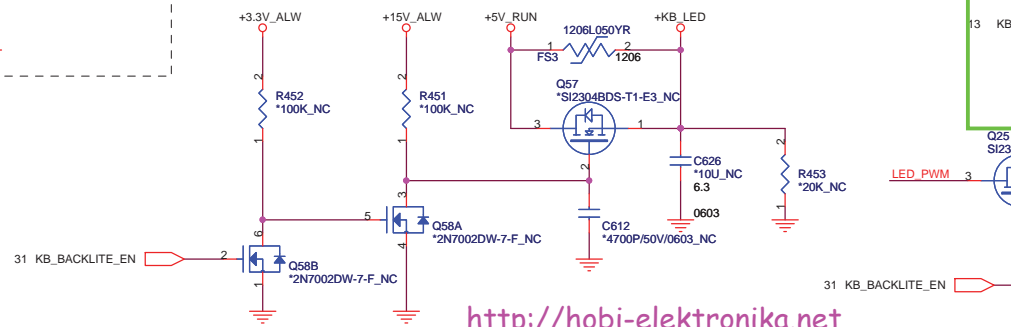
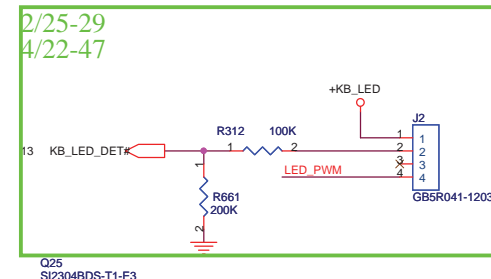
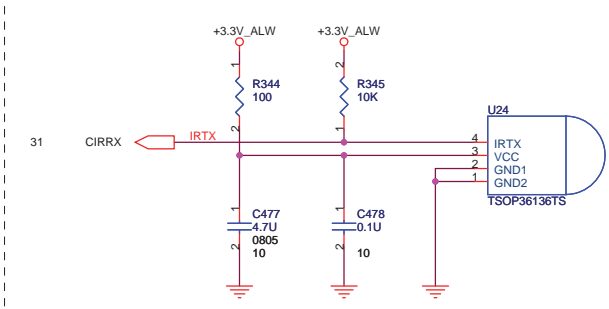
ODD Connector



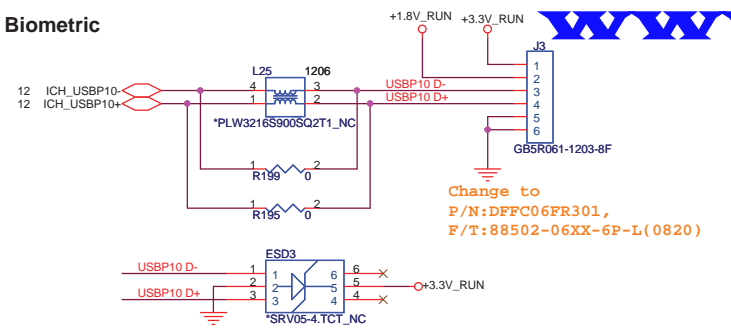
Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
	FM6	2A	
Date:	Wednesday, July 30, 2008	Sheet	36 of 58



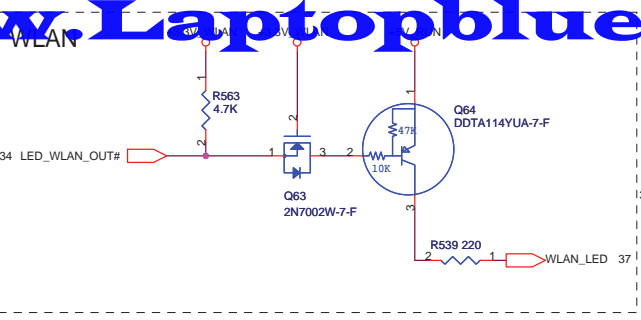
100P CAPS CLOSE TO JKB1



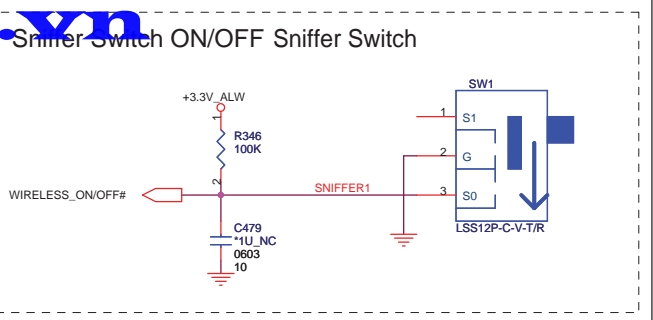
Biometric



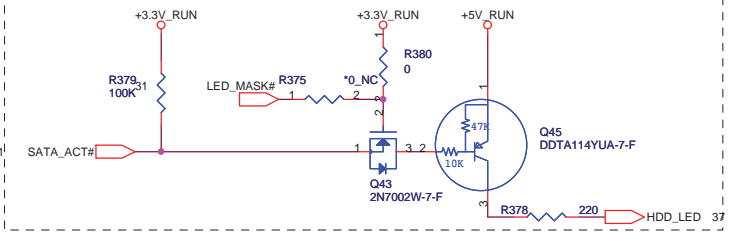
WLAN



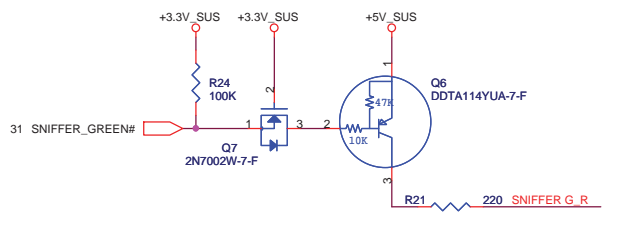
Sniffer Switch ON/OFF Sniffer Switch



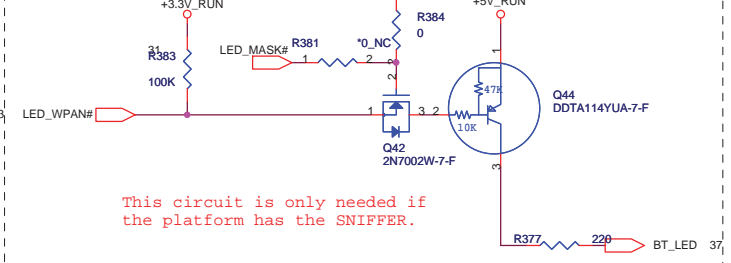
HDD activity LED.



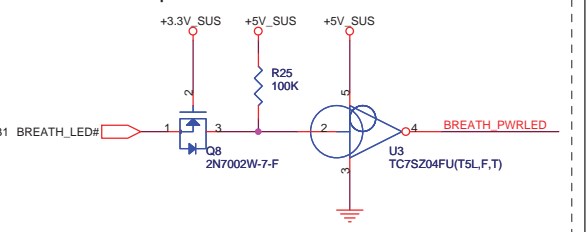
Sniffer Bottom



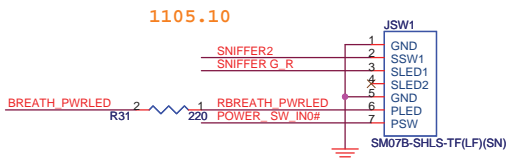
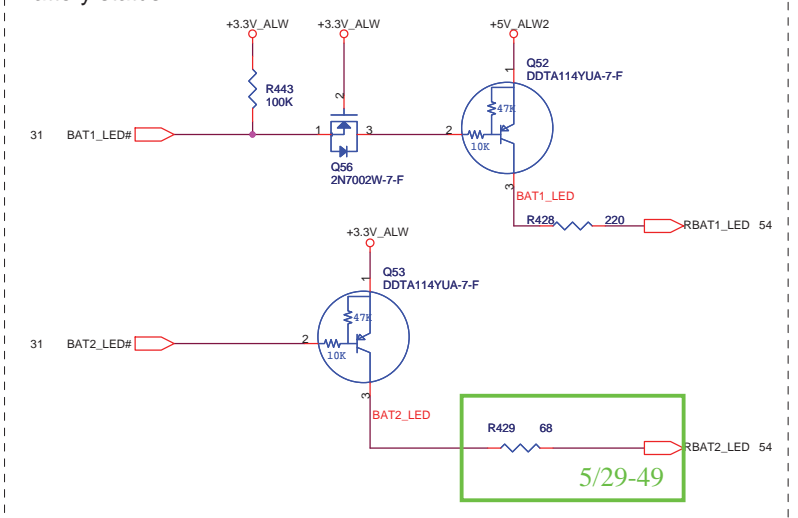
BT / UWB LED



Power & Suspend.

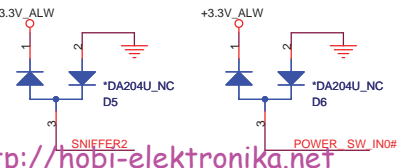


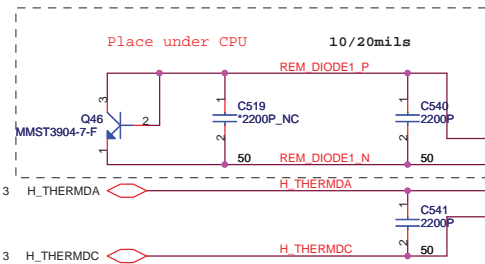
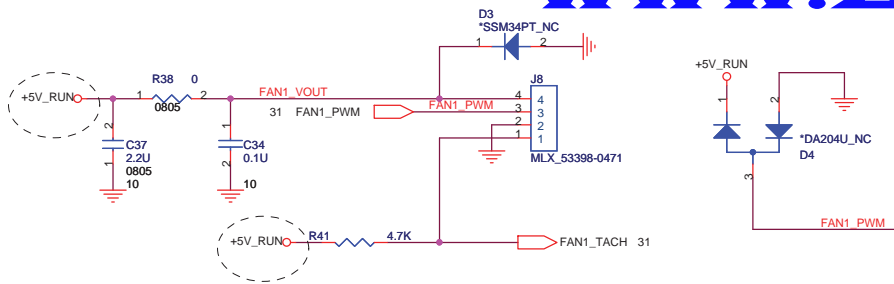
Battery status.



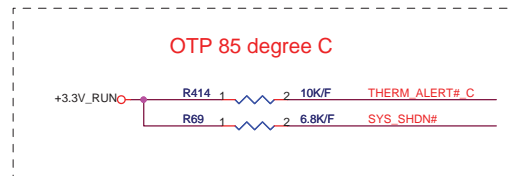
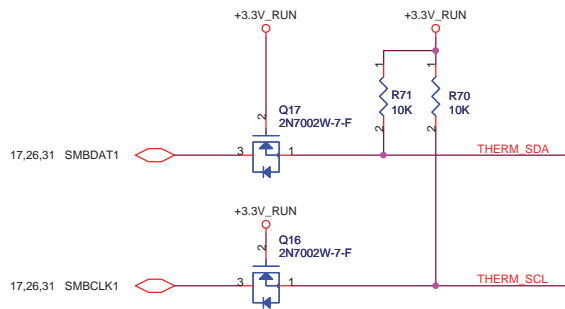
SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection

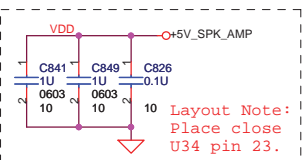
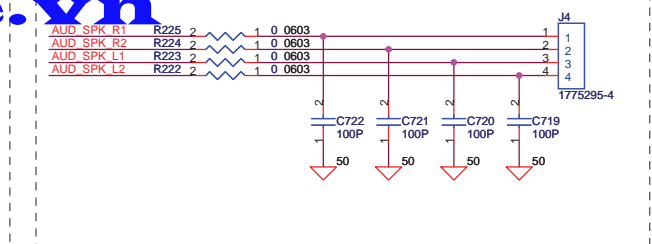
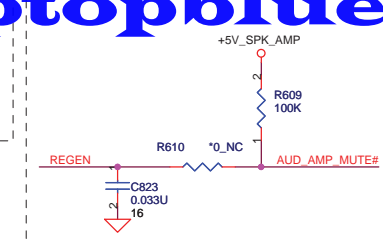
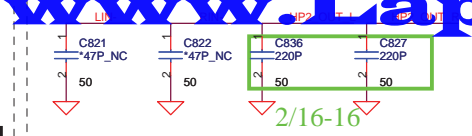
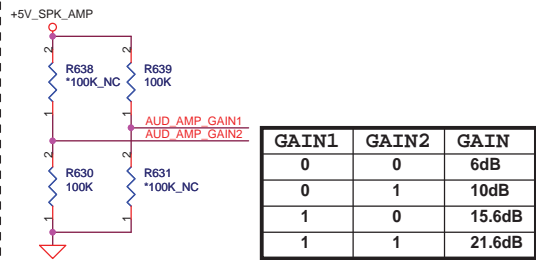
SNIFFER2	C526	100P	50
SNIFFER G_R	C527	100P	50
RBREATH_PWRLED	C528	100P	50
POWER_SW_IN0#	C529	100P	50



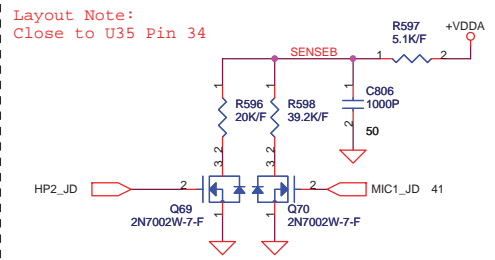


C523, C524 should close to thermal IC





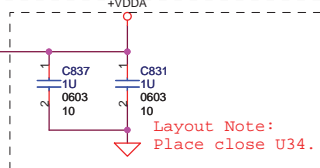
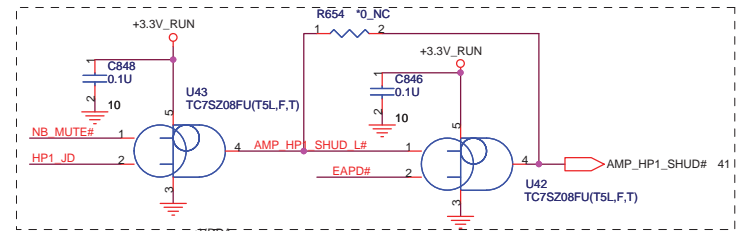
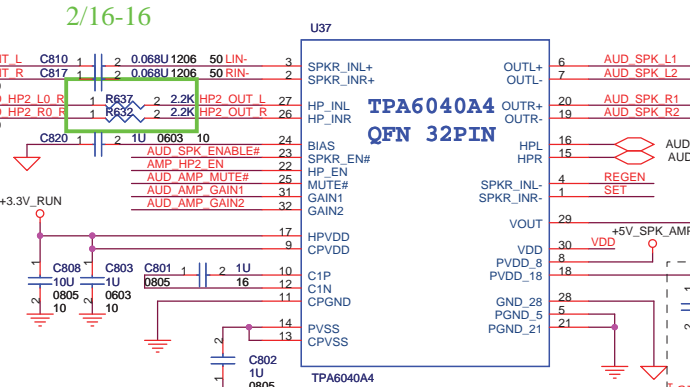
Layout Note:
Place close
U34 pin 23.



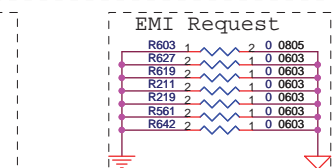
Layout Note:
Close to U35 Pin 34

2/16-16

INTERNAL SPEAKER AMP



Layout Note:
Place close U34.



Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

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Layout Note:
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Layout Note:
Close to U35 Pin 34

Layout Note:
Close to U35 Pin 34

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

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Place close to pin 18.

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Place close to pin 18.

Layout Note:
Place close to pin 18.

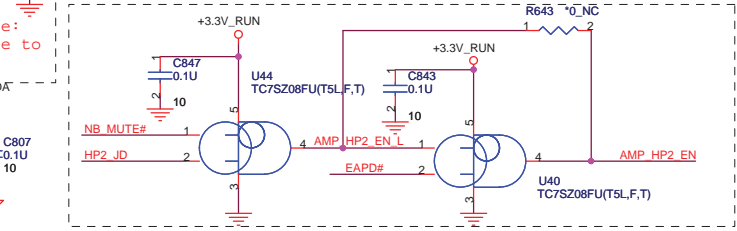
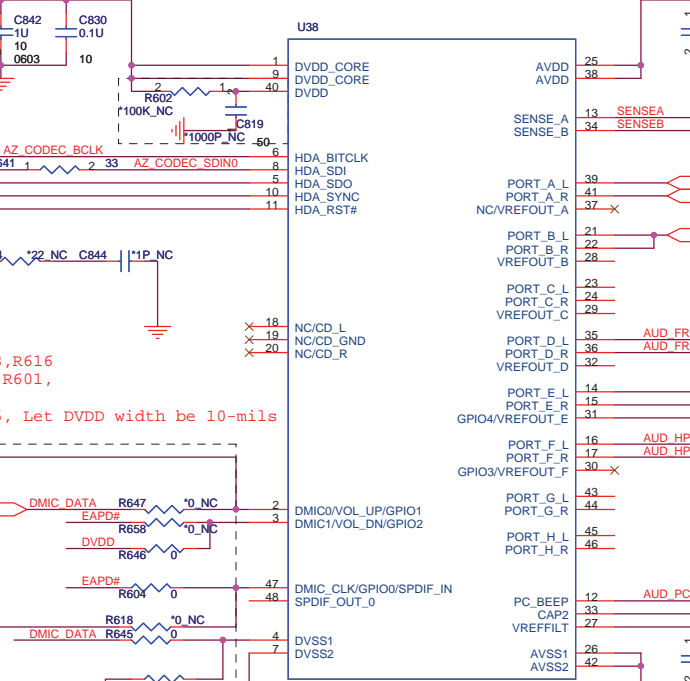
Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

Layout Note:
Place close to pin 18.

AZALIA (HD) CODEC



Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

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Layout Note:
Place close to pin 8.

Layout Note:
Place close to pin 8.

QUANTA COMPUTER

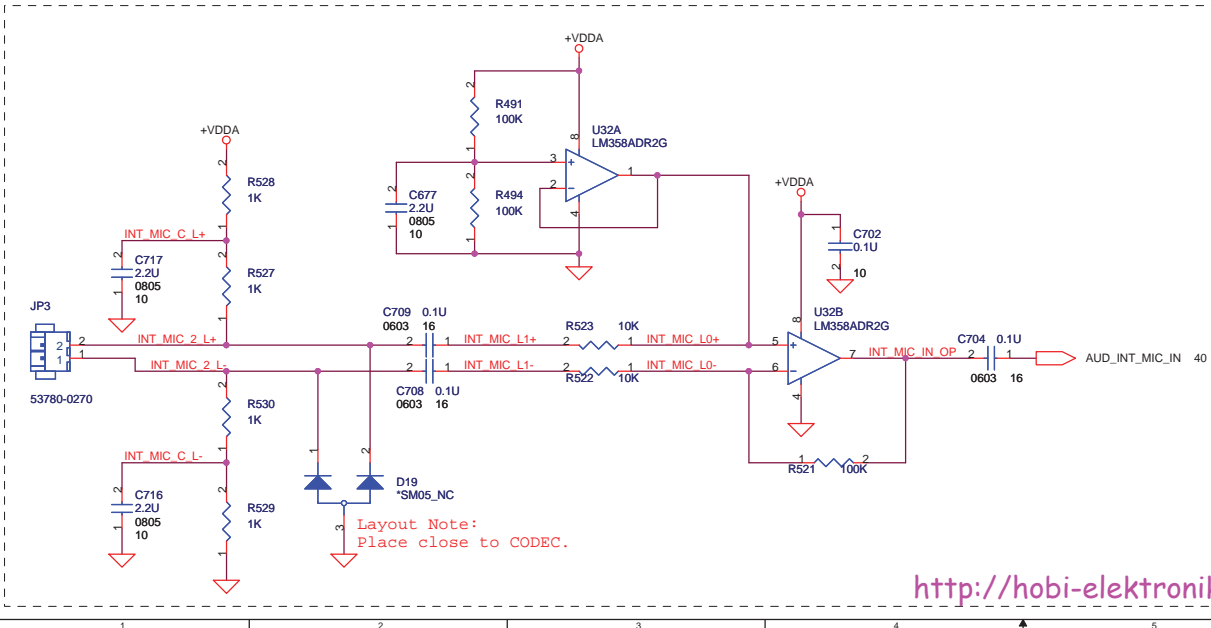
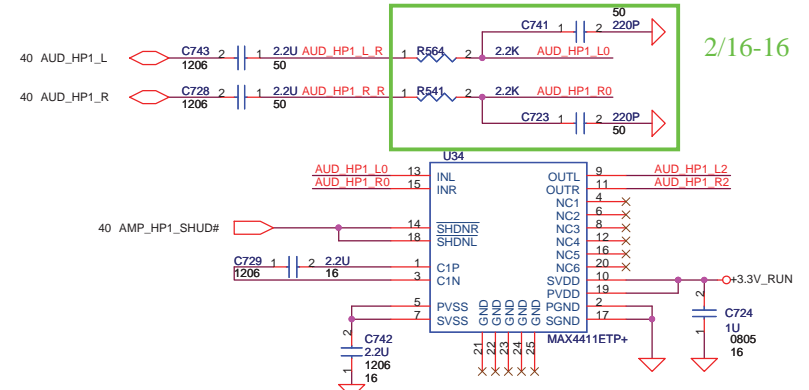
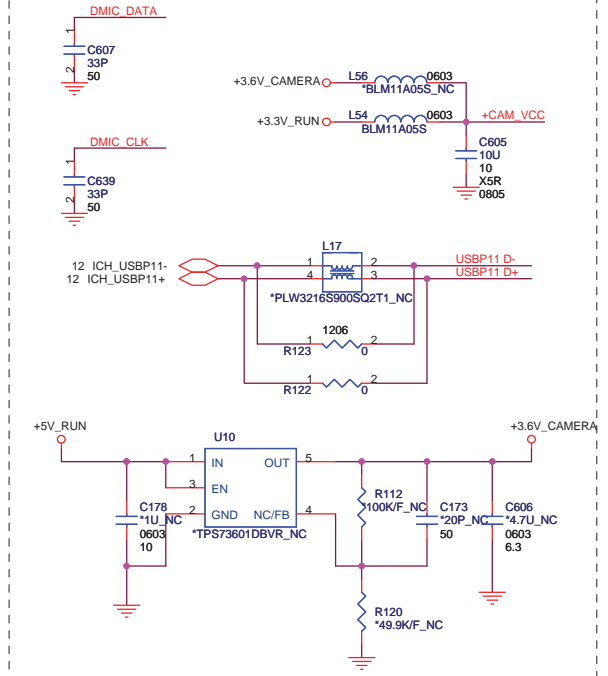
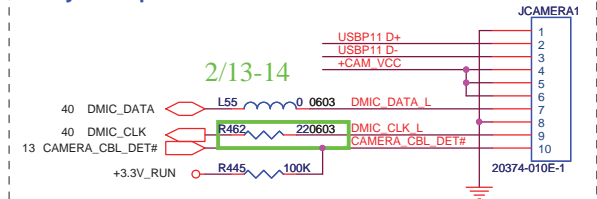
Title: Azelia CODEC

Size: Document Number FM6

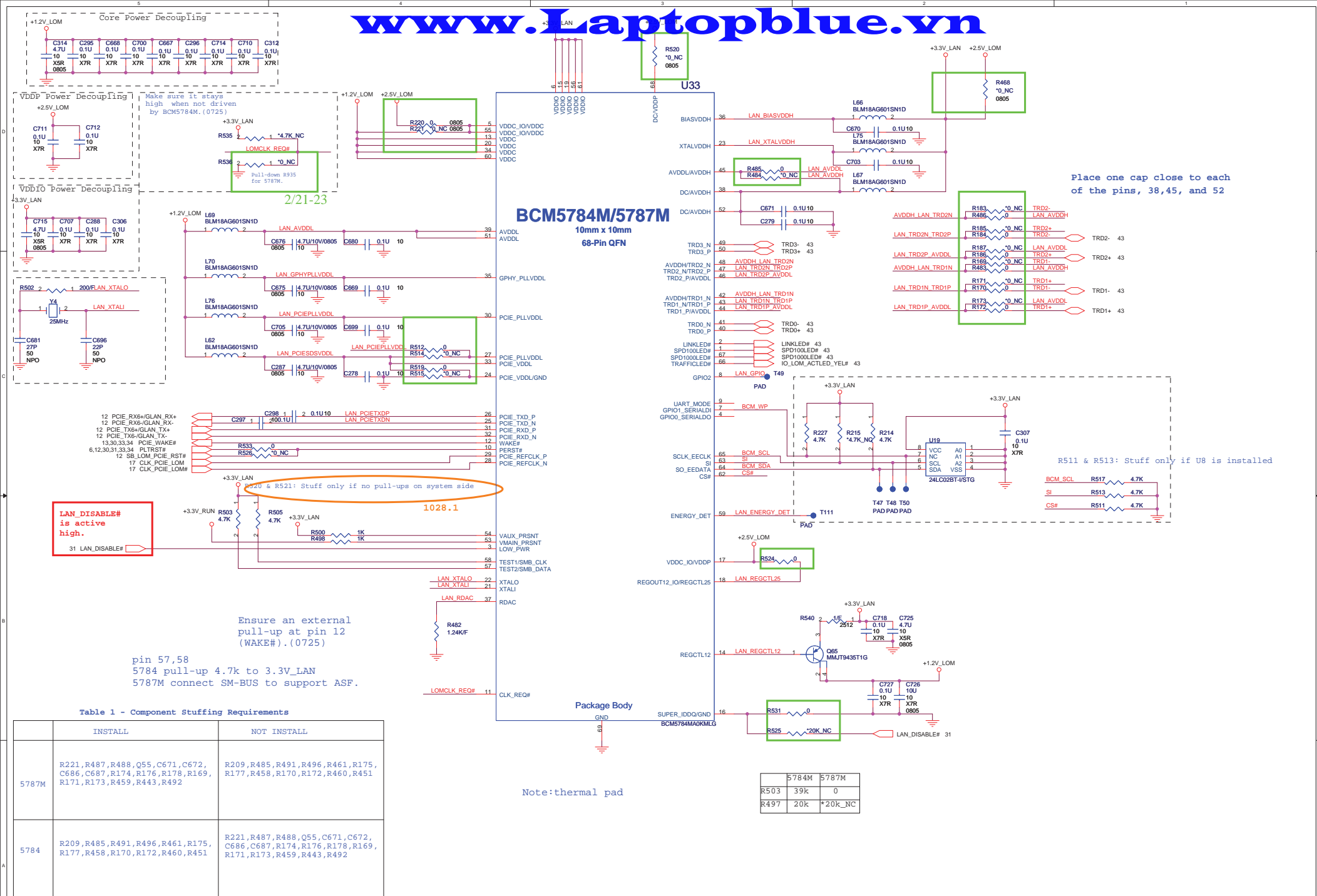
Date: Wednesday, July 30, 2008

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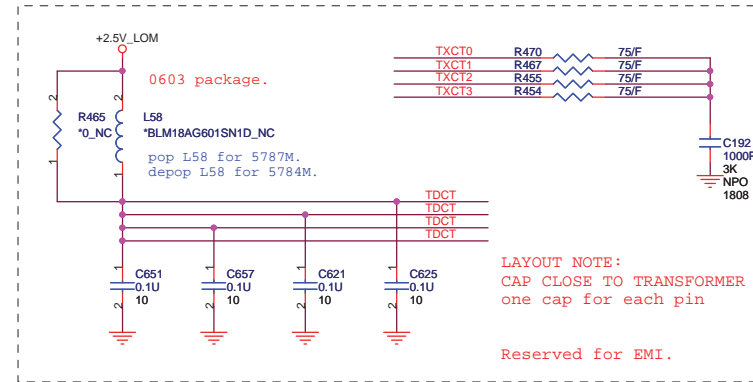
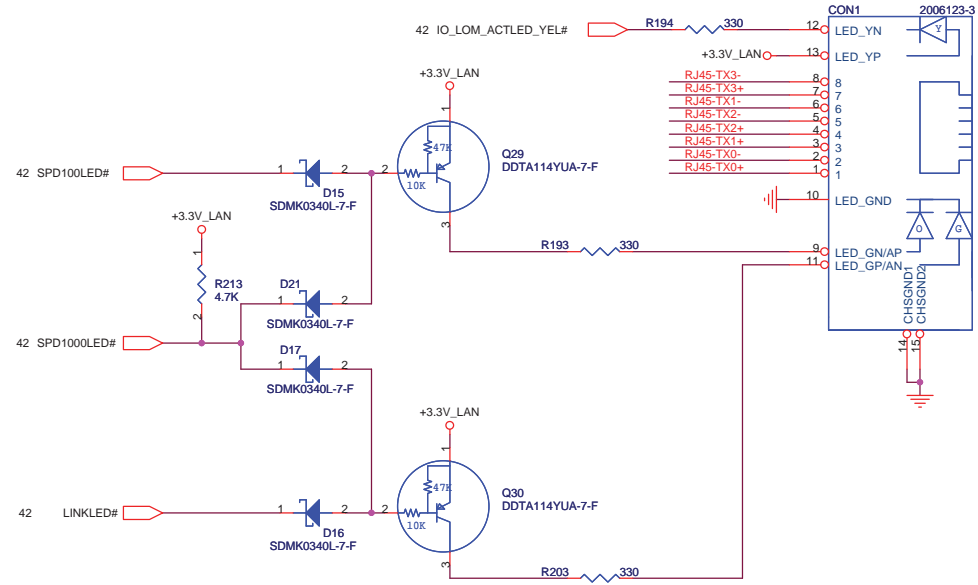
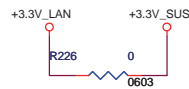
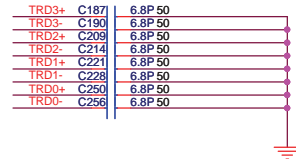
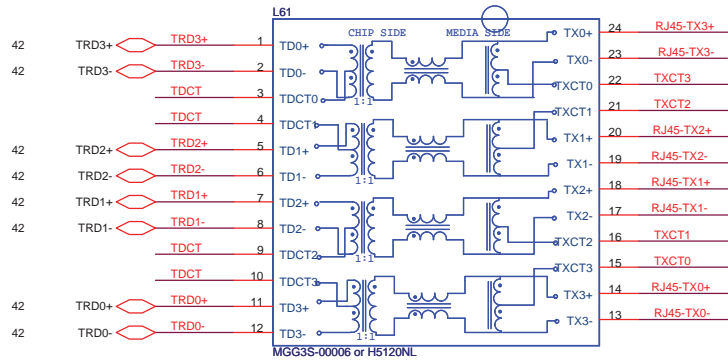


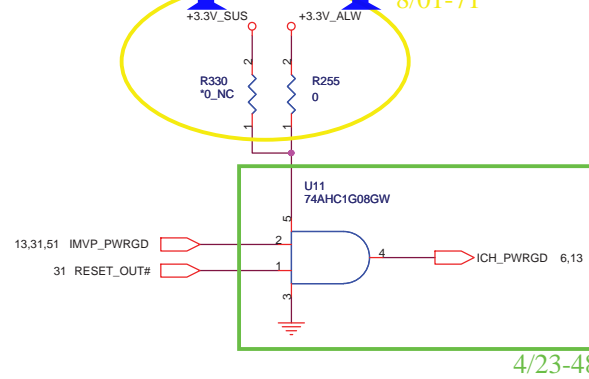
Layout Note:
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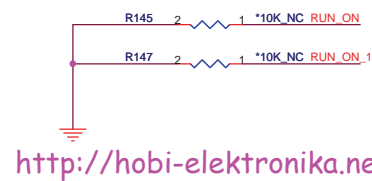
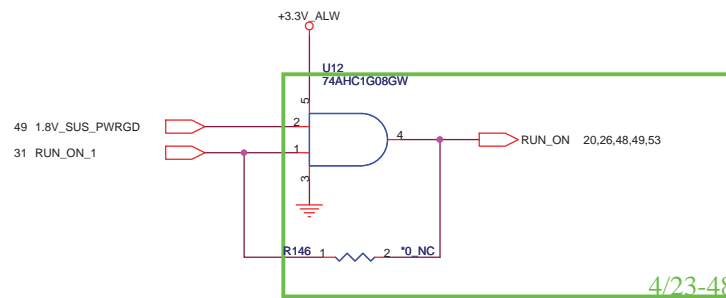
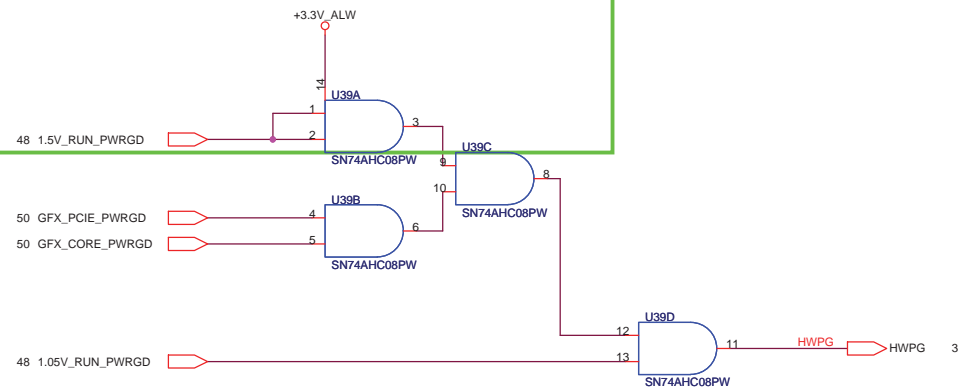
TRANSFORM


TRANSFORM





Keep Away from high speed buses



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Size	Document Number FM6	Rev 1A
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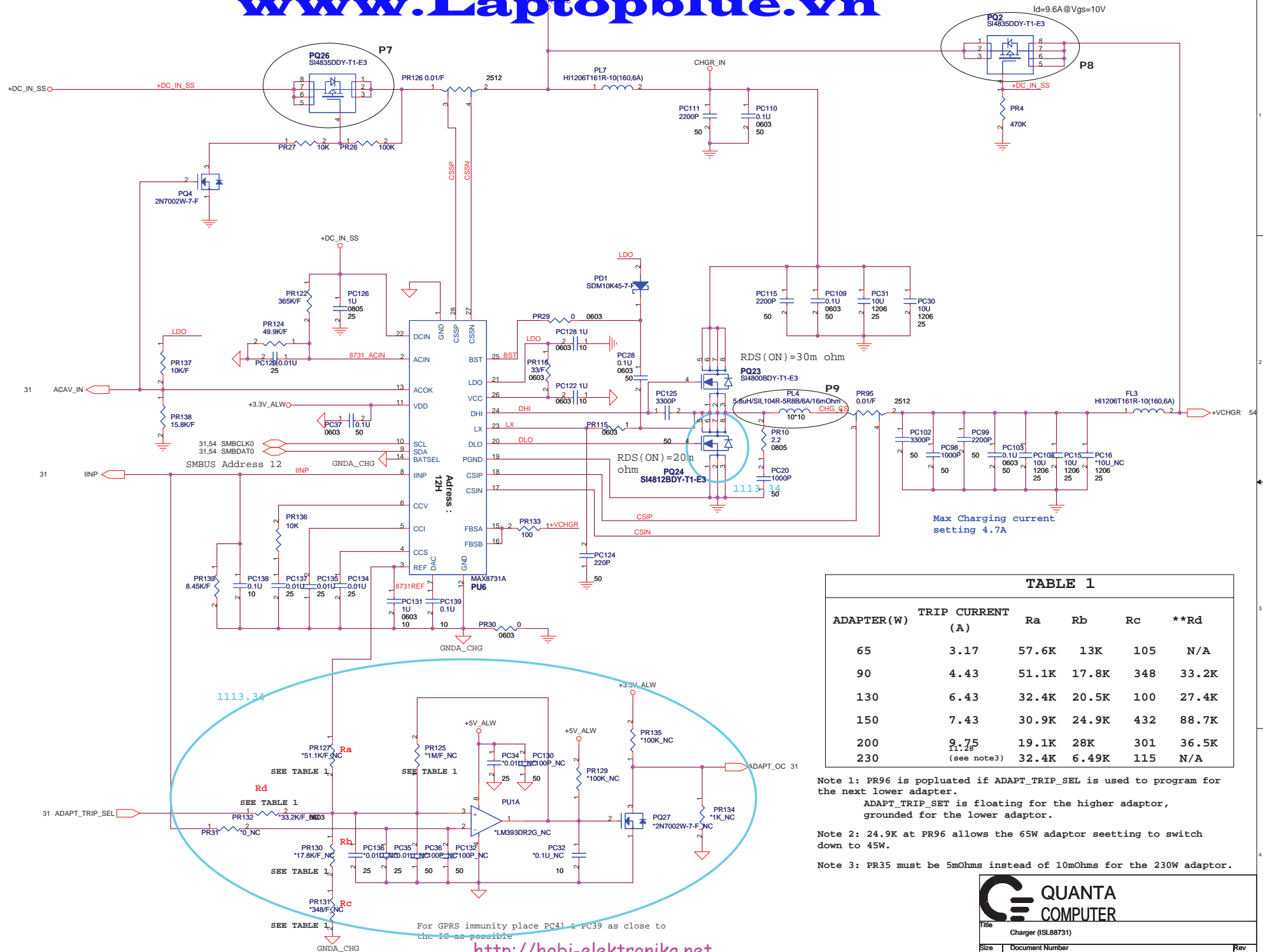


TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	(see note3)	32.4K	6.49K	115	N/A


Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

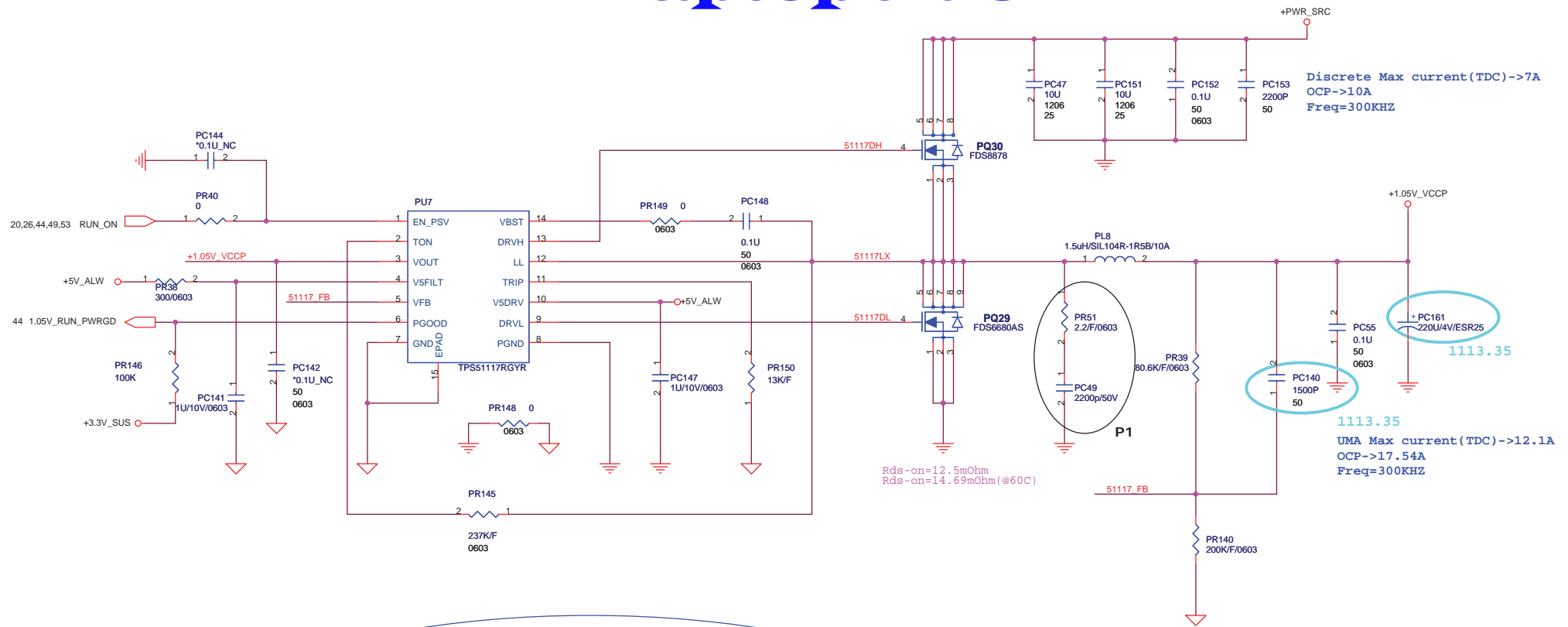
ADAPT_TRIP_SET is floating for the higher adaptor,
grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

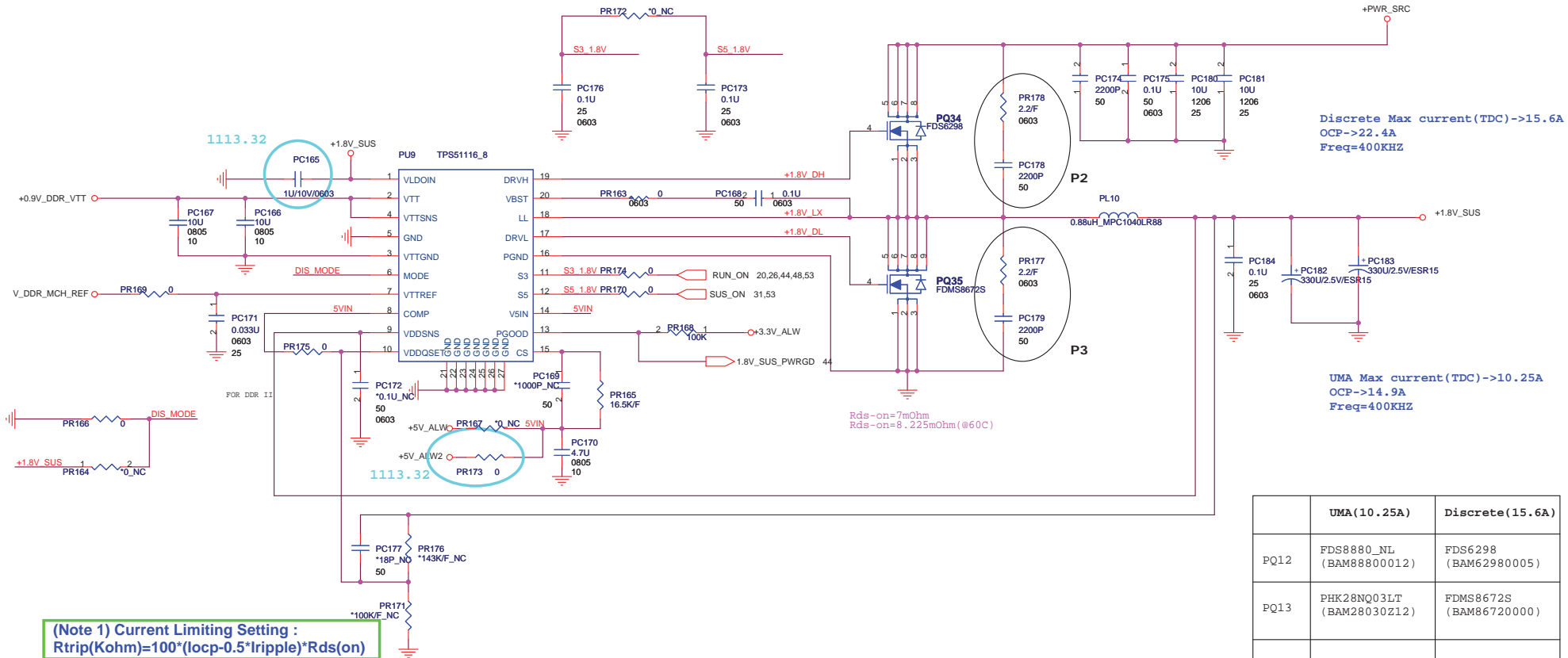
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

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NUMBER SAME AS DISCRETE

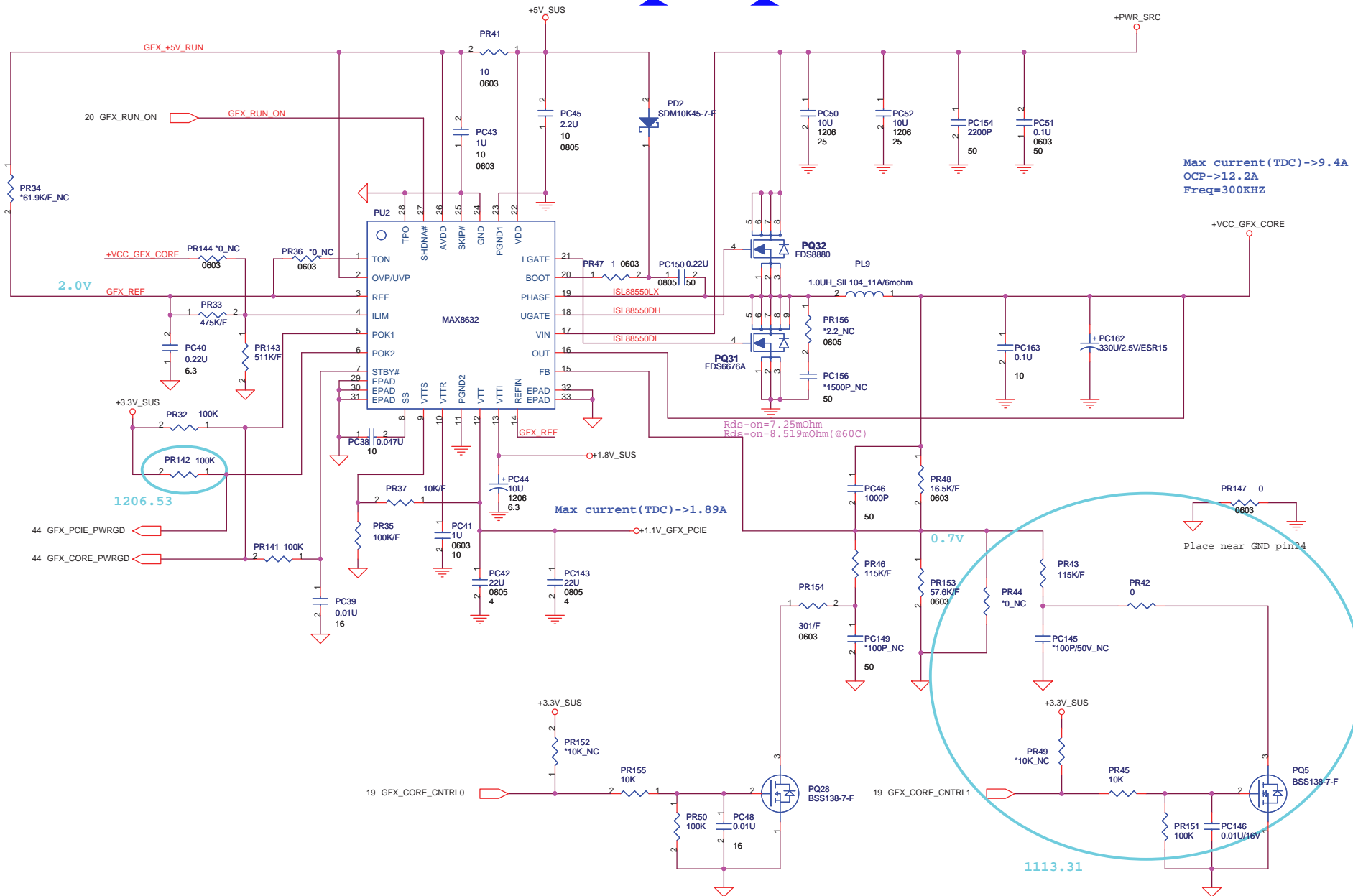
		QUANTA COMPUTER	
Title			
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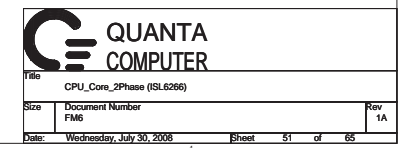
	UMA (12.1A)	Discrete (7A)
PQ22	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ25	FDS6676AS_NL (BAM66760026)	FDS6680AS (BAM66800061)
PL25	SIL105RA-1R5-R (CV-15F0MZ08)	SIL104R-1R5PF (DC-15A00010)
PR452	9.09K/F (CS29092FB27)	10K/F (CS31002FB26)



	UMA (10.25A)	Discrete (15.6A)
PQ12	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ13	PHK28NQ03LT (BAM28030212)	FDMS8672S (BAM86720000)
PR83		



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9
HIGH	LOW	1.0V
HIGH	HIGH	1.1V

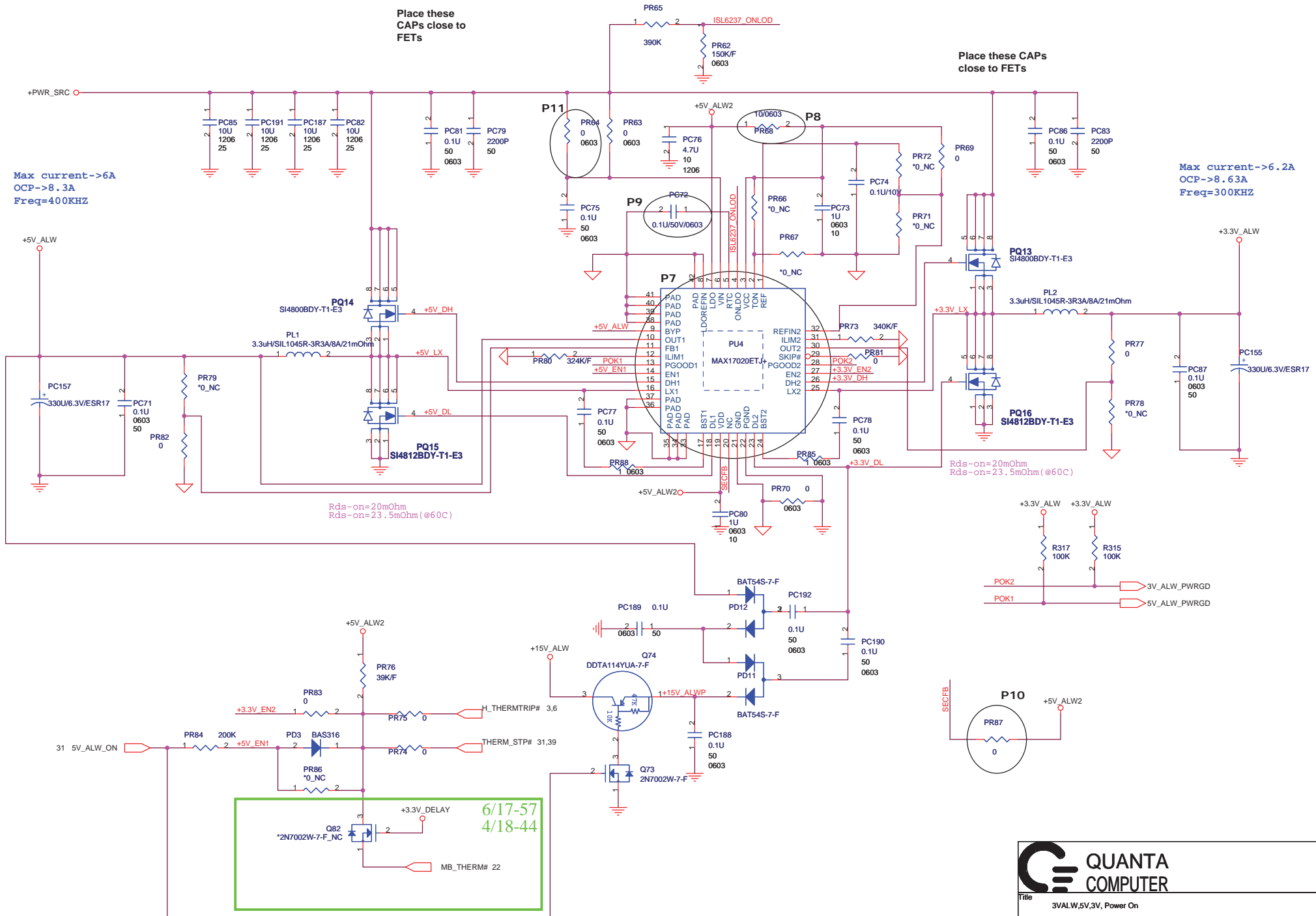


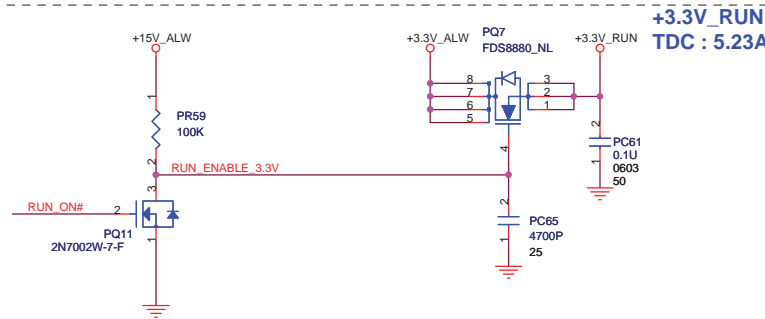
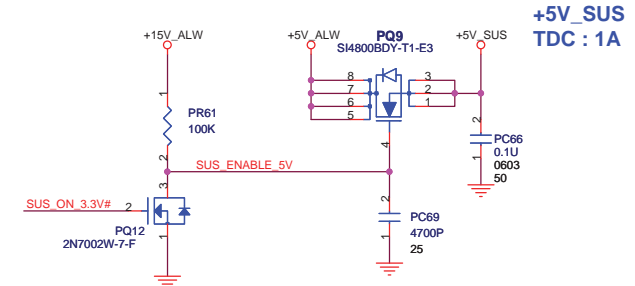
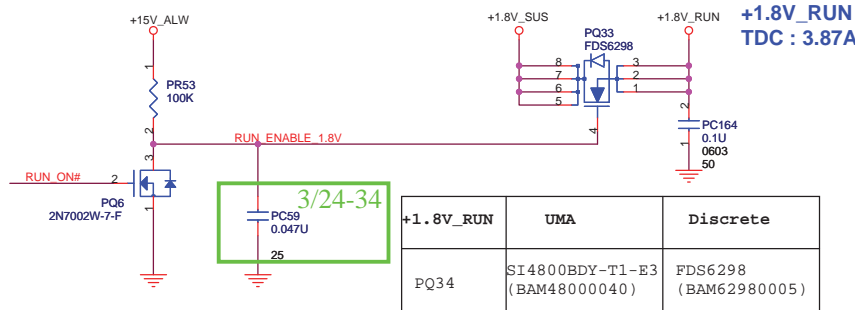
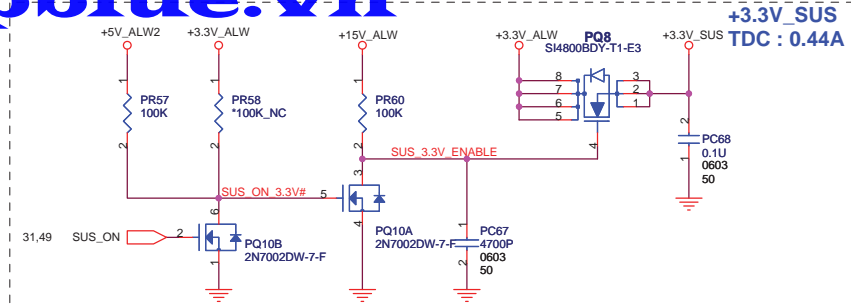
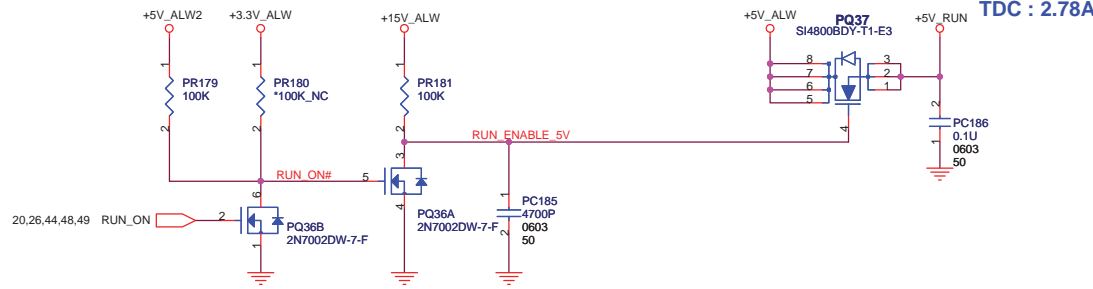
Place these
CAPs close to
FETs

Place these CAPs
close to FETs

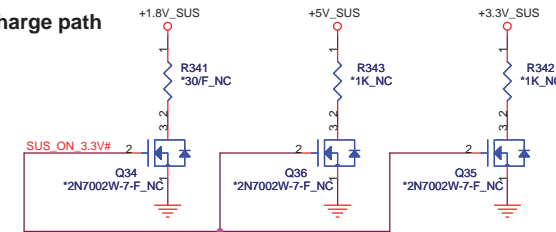
Max current->6A
OCP->8.3A
Freq=400KHZ

Max current->6.2A
OCP->8.63A
Freq=300KHZ

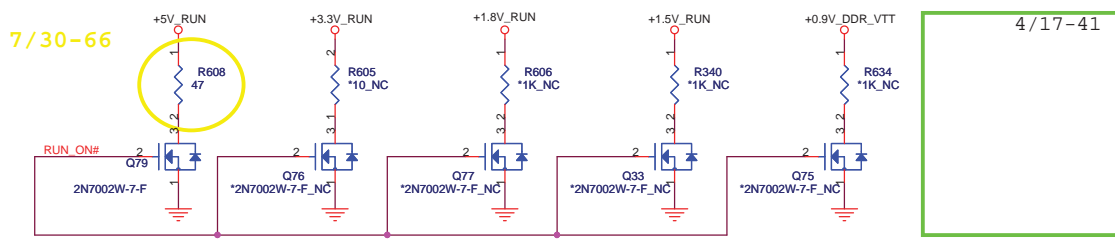


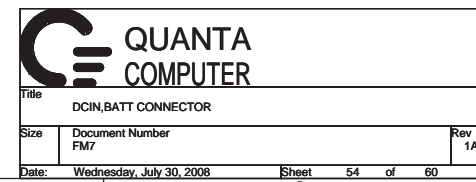


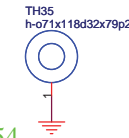
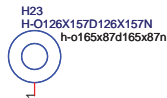
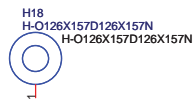
Reserve discharge path



Reserve discharge path

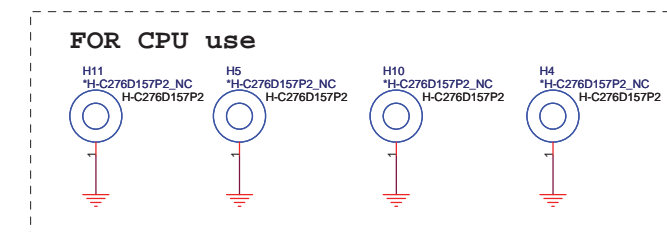
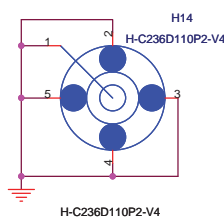
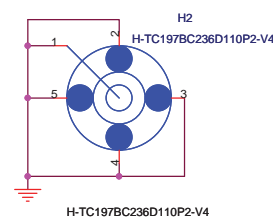
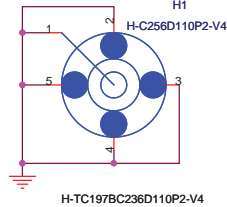
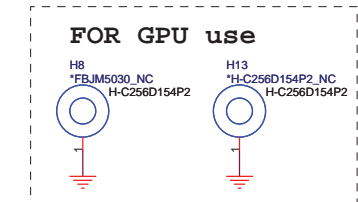
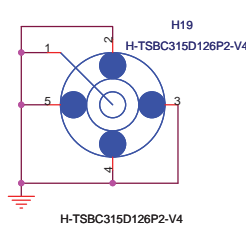
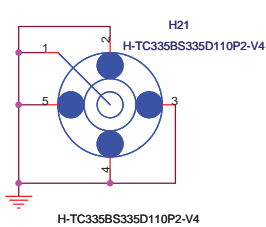
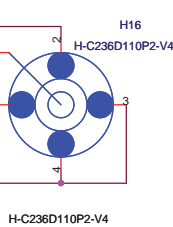
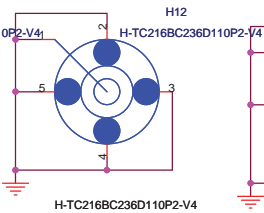
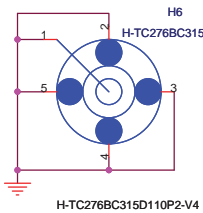
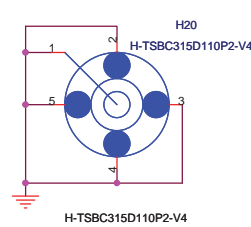
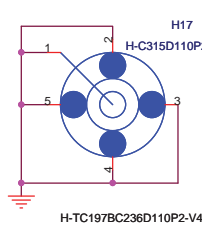
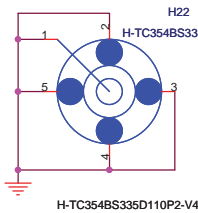
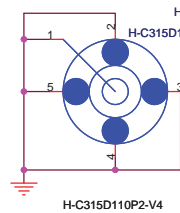
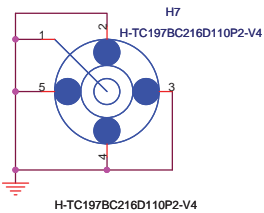
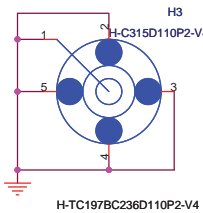






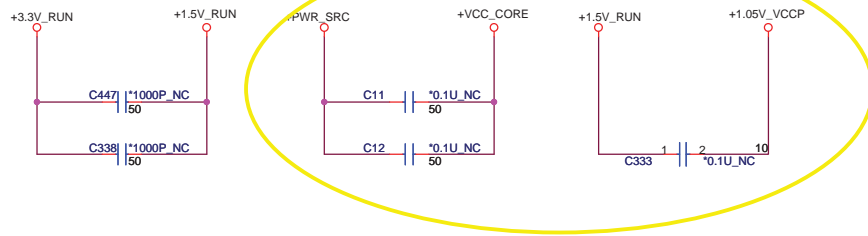
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6/12-54




Reserved for EMI.

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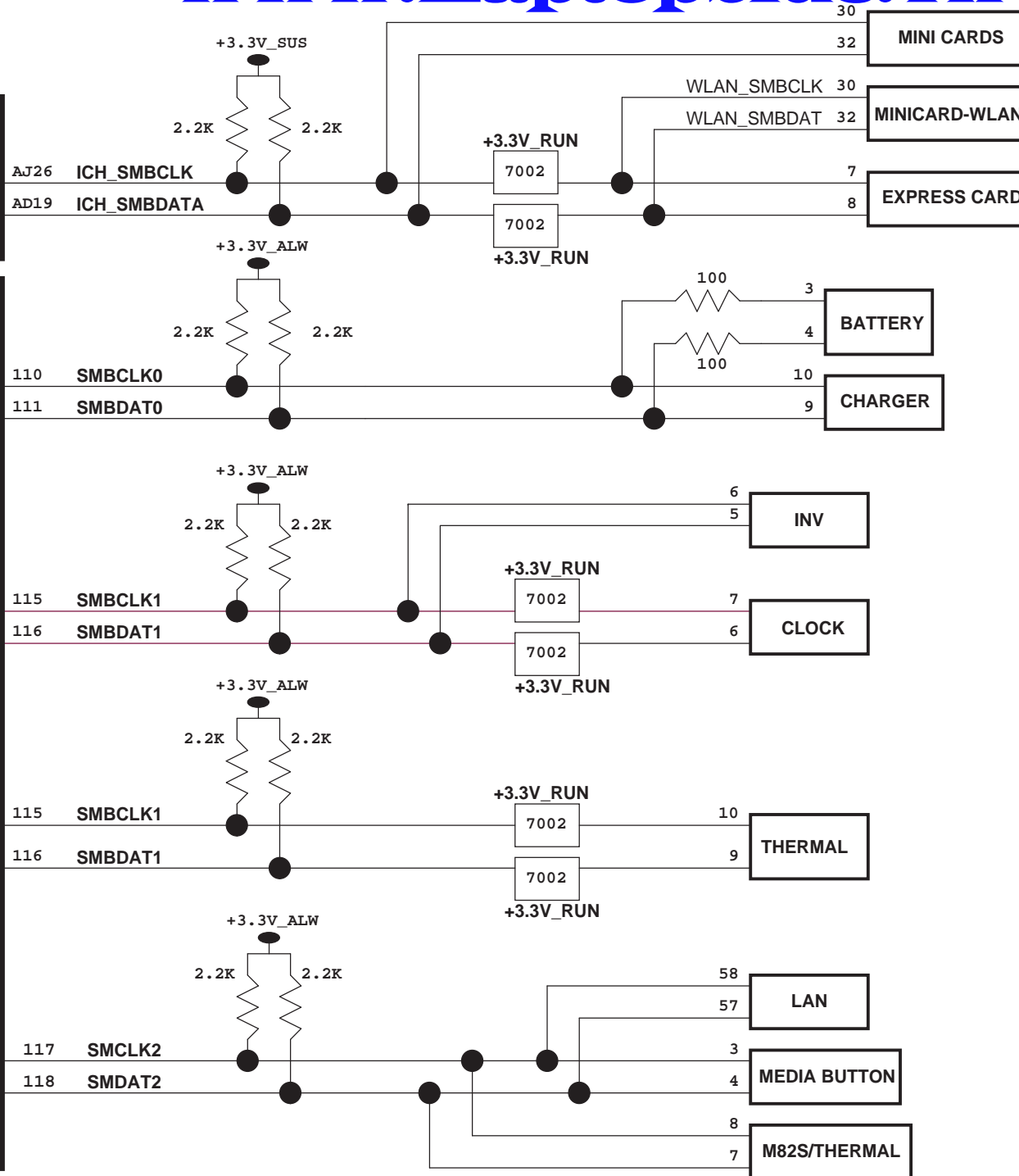


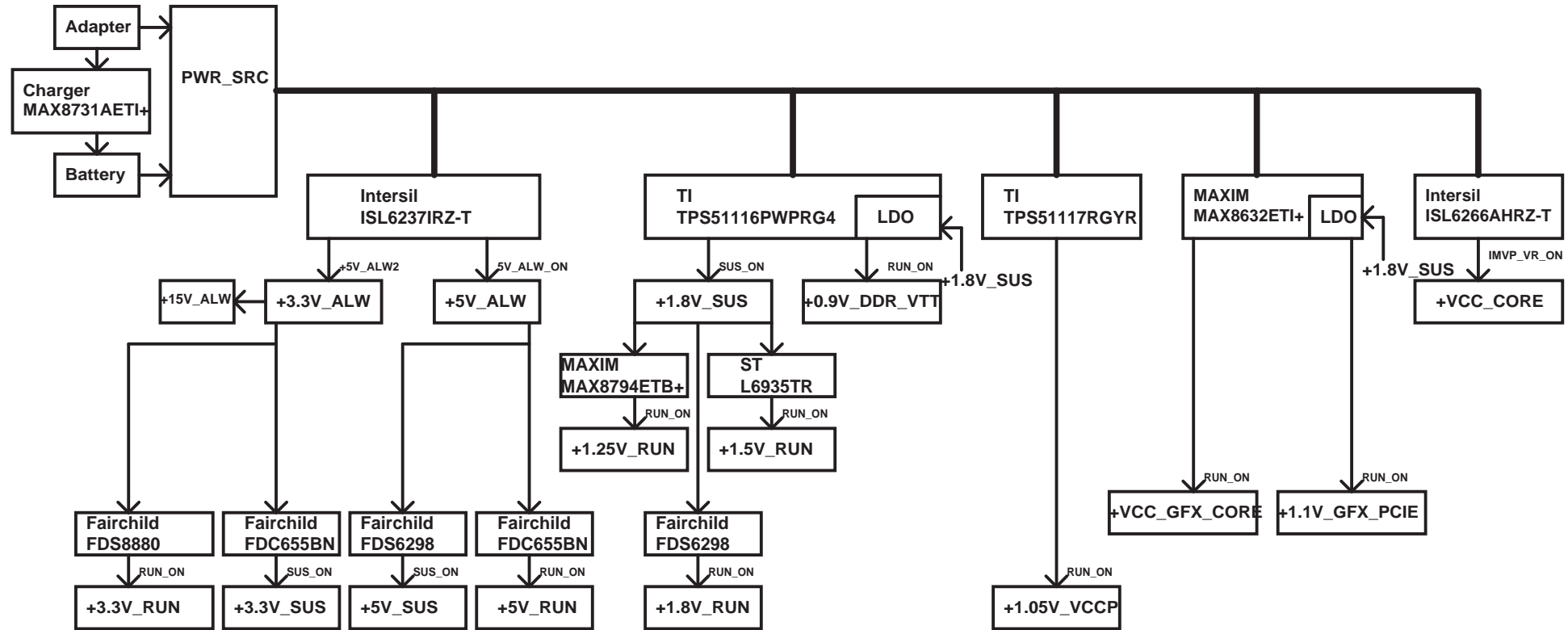
<http://hobi-elektronika.net>

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Size	Document Number FM6
Date: Monday, June 30, 2008	Rev 1A
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ICH8-M

SIO
ITE8512





Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	1	3	2-13-08				Debug port needs to be updated for MV	Change the BOM, and add a pull high circuit on ITP_BPM#5
	2	3	2-13-08				H_THERM circuit has risk	Change the BOM in order to make it same with FM6
	3	8	2-13-08				VCC_AXG and VCC_AXG_NCTF are different with MV DG	Change VCC_AXG, and VCC_AXG_NCTF to ground
	4	11, 35	2-13-08				Add E-SATA function	Refer to page 11 and 35
	5	13	2-13-08				Some power rails don't mach with DG	Refer to page 13
	6	17	2-13-08				BSEL0, BSEL1, and BSEL2's seris resisters don't mach with DG	Refer to page 17
	7	9	2-13-08				VCCA_SM doesn't mach with DG	Add 0-ohm in order to make it same with other project
	8	9	2-13-08				VCCD_TVDAC and VCCD_QDAC are different with DG	Grond VCCD_TVDAC and update another circuit for VCCD_QDAC
	9	19,22	2-13-08				Change the power rail for avoiding leakage during power up	Change +3.3V_RUN to +3.3V_DELAY
	10	37	2-13-08				MMB vender changed it's F/W to fix the LED flash issue. Change Num/Cap LED circuit for avoiding leakage voltage	Change the circuit, refer to page 37
	11	35	2-13-08				Fulfill reliability's request	Add one more power pin on connector
	12	31	2-13-08				New chip version for ITE	Change the circuit
	13	40,42	2-13-08				Change chip version for Codec and LOM	Done
	14	41	2-13-08				Approve DMIC'S performance according to IDT's recommendation	Change o-ohm to 22-ohm
	15	26	2-16-08				DDC BUS for HDMI Certificate	Add Level Shift on DDC BUS of HDMI
	16	40,41	2-16-08				Need to meet WLP4.0	Refer to page 40 and 41
	17	31	2-16-08				Add audio solution for PO noise issue when loading driver	Connect ICH_AZ_CODEC_RST# to SIO.22
	18	14	2-18-08				Reserve +1.5V_SUS for VCCSUSHDA	Add a LDO and reserve 0-ohm for +1.5V_SUS
	19	13	2-18-08				Avoid leakage voltage	Follow the SR FM6 design
	20	17	2-19-08				After FAE review, modify circuit in order to let wave form smooth	Add two 0.1u cap
	21	17	2-20-08				After FAE review, modify circuit for single end nets	change 0-ohm to 33-ohm, add pull high resister
	22	35	2-20-08				Add E-SATA redriver function	Refer to page 35
	23	42	2-21-08				According to FAE, stub a resister	Refer to page 42
	24	17	2-21-08				In order to meet spec, we need to swap two signals	Refer to page 17
	25	35	2-22-08				Co-work with GM3 team and decide to take USB charger function off	Refer to page 35
	26	21	2-22-08				According to realiability team request, change BOM	Change L51
	27	12	2-25-08				Need to meet Dell USB port requirement	Refer to page 12
	28	19	2-25-08				FAE's suggestion is add ground	Refer to page 19
	29	13,37	2-25-08				Add one pin for LCD inventer det	Refer to pages
	30	30	3-03-08				Footprint is wrong for express card	Refer to FM6 footprint
	31	32 35	3-24-08				Change locations for USB and Coin Battery for safty requirement	Refer to those pages
	32	26 35	3-24-08				Change BOM for HDMI and E-sata	Refer to those pages
	33	49	3-24-08				Del 1.25V power rail	Refer to page 49
	34	53	3-24-08				Change BOM for correcting power sequence	Refer to page 53
								 <div> <div>QUANTA</div> <div>COMPUTER</div> </div> <div> <div>Title</div> <div>Change List</div> </div> <div> <div>Size</div> <div>Document Number</div> <div>FM7</div> <div>Rev</div> <div>1A</div> </div> <div> <div>Date:</div> <div>Wednesday, June 18, 2008</div> <div>Sheet</div> <div>1</div> <div>of</div> <div>6</div> </div>

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