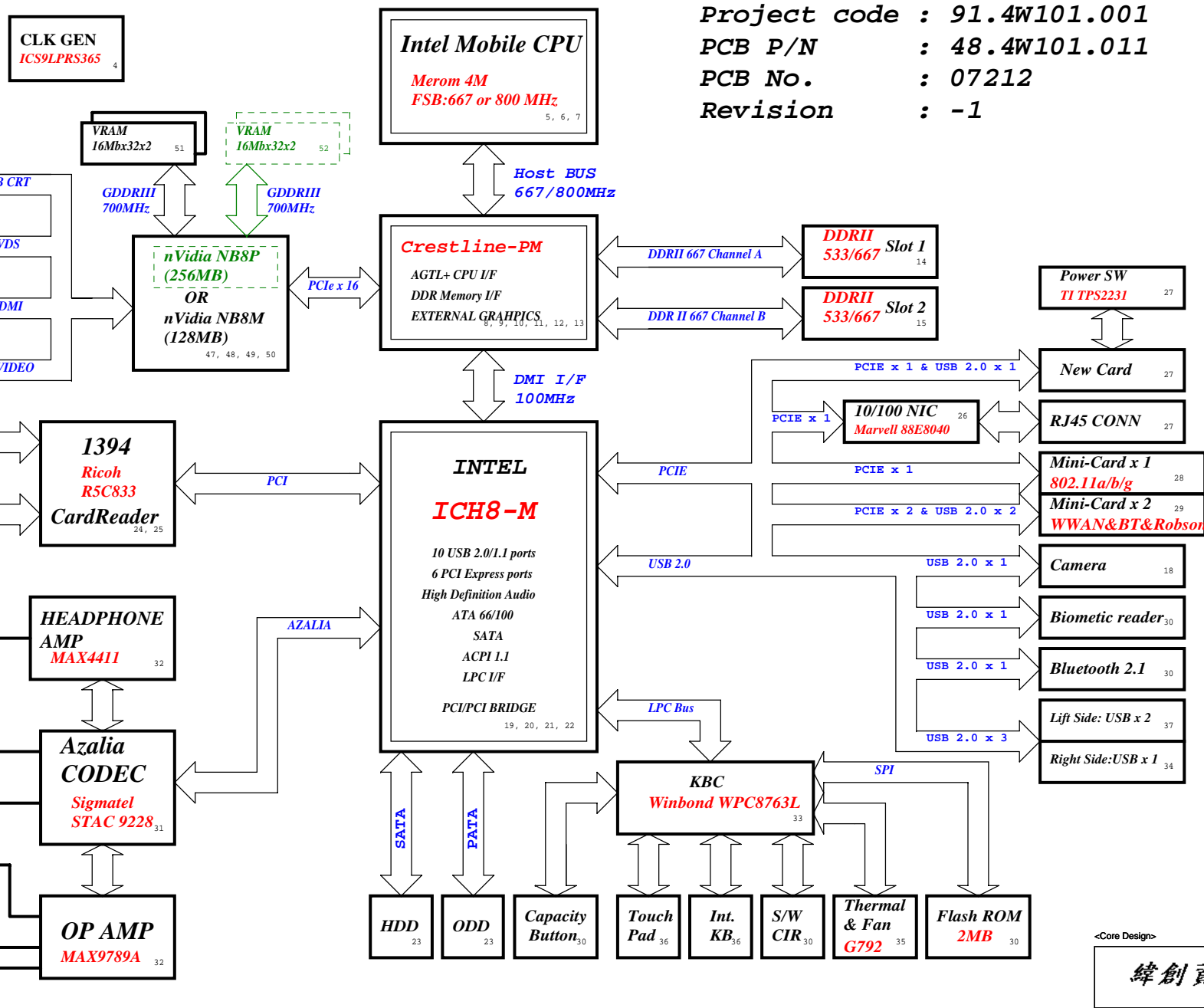


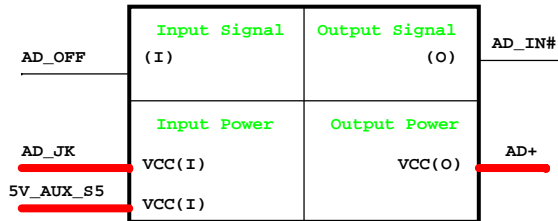
Hawke Intel Discrete Block Diagram



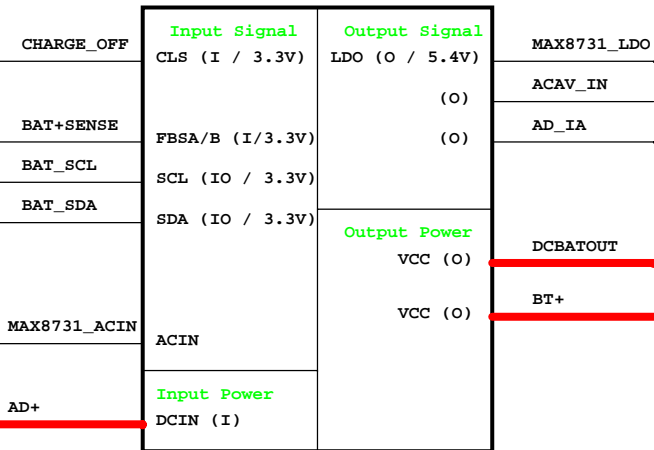
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PCB P/N : 48.4W101.011
PCB No. : 07212
Revision : -1

BATTERY CHARGER MAX8731A		38
INPUTS	OUTPUTS	
AD+ BAT+	DCBATOUT	
SYSTEM DC/DC TPS51120		39
INPUTS	OUTPUTS	
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	
SYSTEM DC/DC TPS5117		42, 43
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0 1D8V_S3	
SYSTEM DC/DC TPS51100		44
INPUTS	OUTPUTS	
1D8V_S3	0D9V_S3	
SYSTEM DC/DC RT9018		44
INPUTS	OUTPUTS	
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0	
VGA DC/DC TPS5117		53
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFX_CORE_S0	
CPU DC/DC ISL6262A		40
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
PCB LAYER		
L1:TOP		
L2:GND		
L3:Signal		
L4:Signal		
L5:VCC		
L6:Singal		
L7:GND		
L8:BOT		

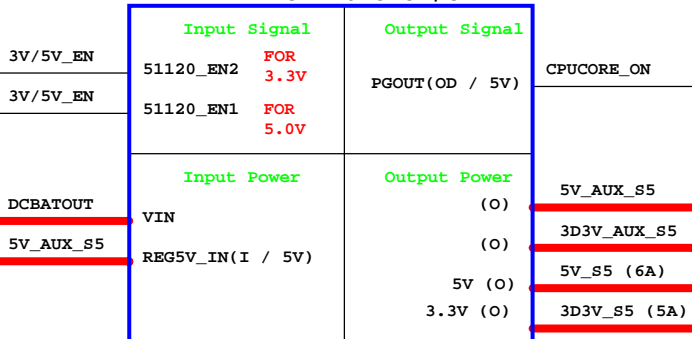
Adapter



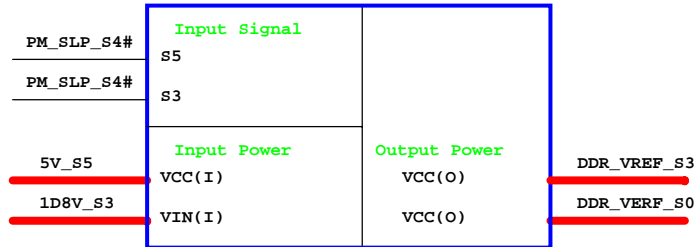
Charger MAX8731A



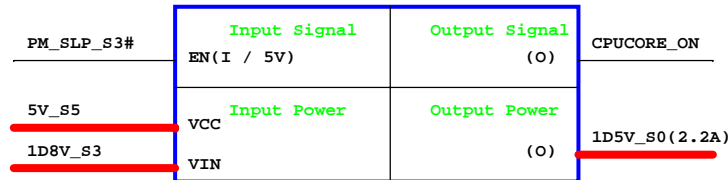
TI TPS51120 3D3V/5V



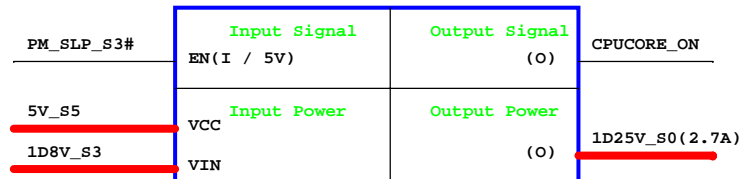
TI TPS51100 0.9V/DDR_VREF_S3



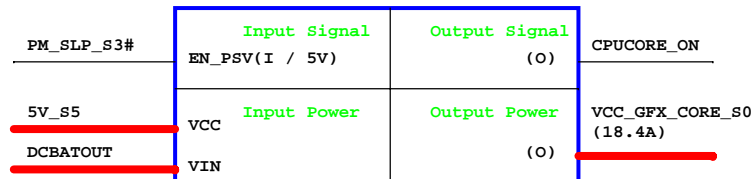
RT9018A 1D5V



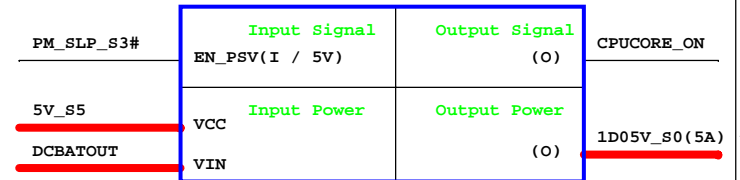
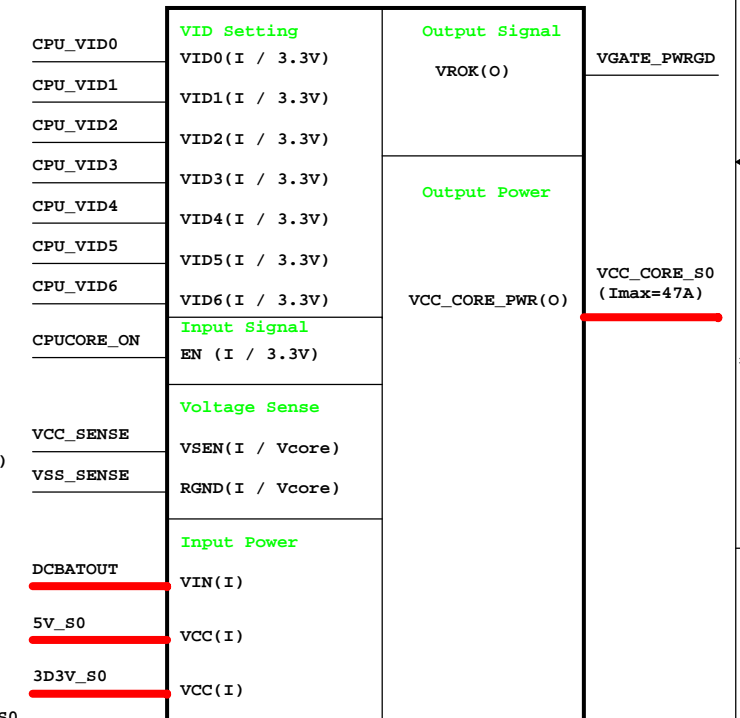
RT9018A 1D25V



TPS51117 VGA_CORE



TPS51117 1D05V

ISL6262A
CPU_CORE

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP	TP3	AZ	DOUT ICH
0	0	1	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable

Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

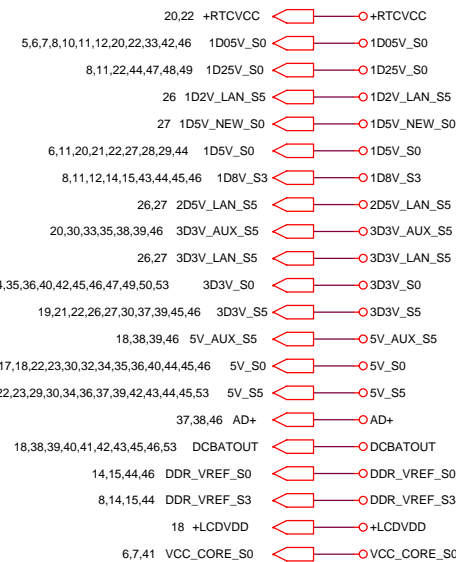
INTEL ICH8-M INTEGRATED
PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation



PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

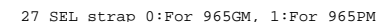
PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Table of Content	
Size A3	Document Number	Hawke-Intel		Rev -1
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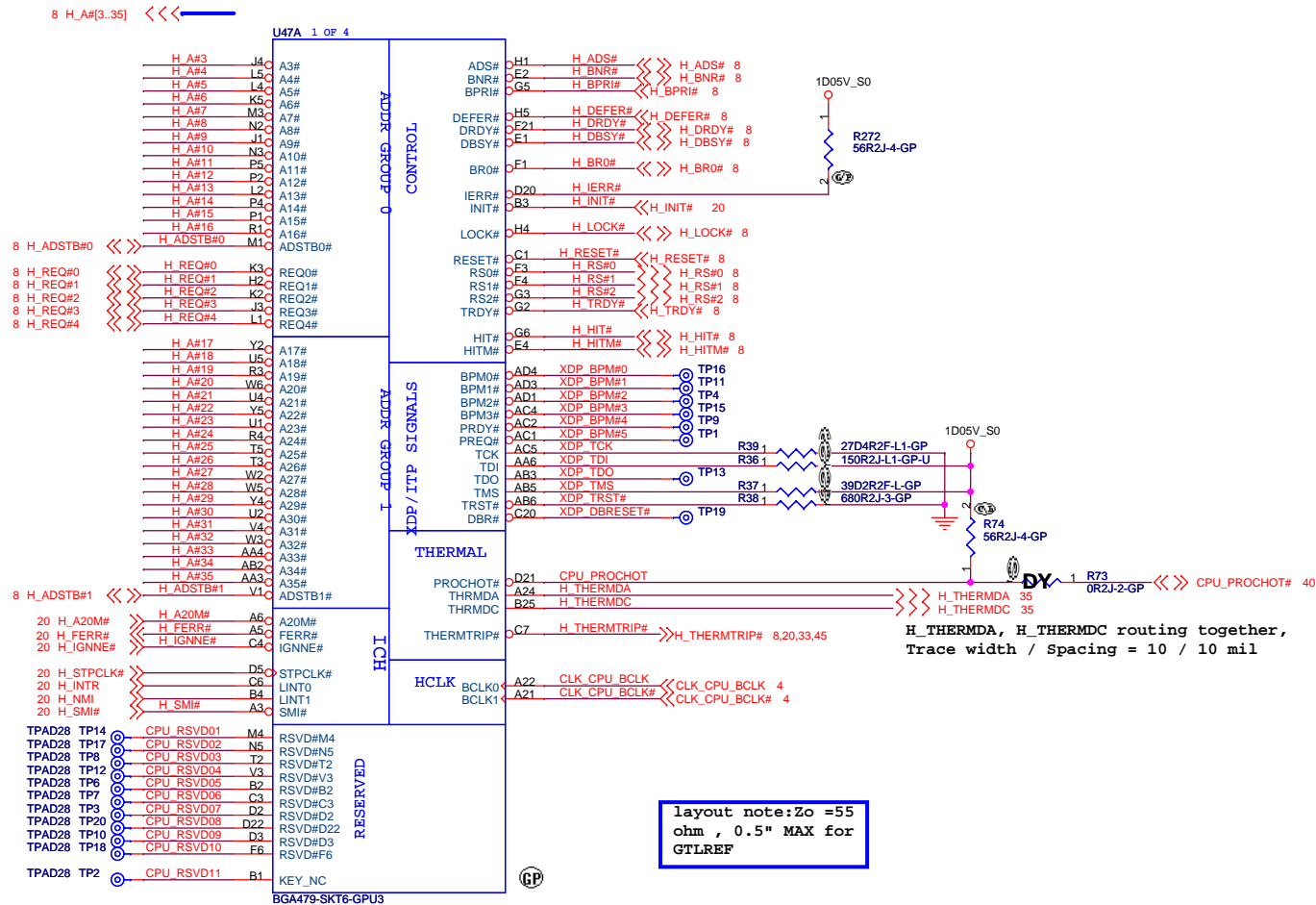


27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM

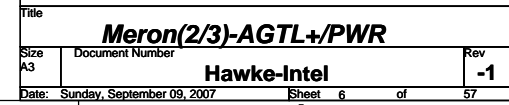
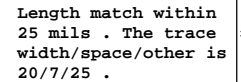
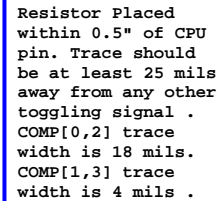
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Size A3	Document Number Hawke-Intel	Rev -1
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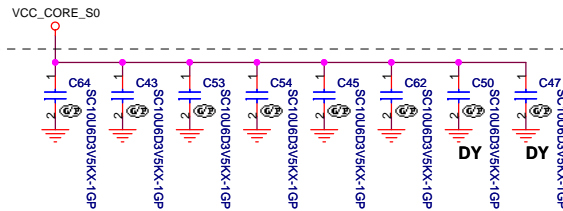
Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41



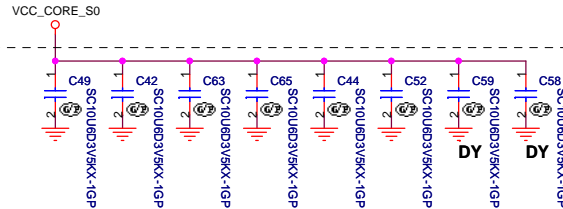
U47D 4 OF 4		
A4	VSS	P6
A8	VSS	P21
A11	VSS	P24
A14	VSS	R2
A16	VSS	R5
A19	VSS	R22
A23	VSS	R25
AF2	VSS	T1
B6	VSS	T4
B8	VSS	T23
B11	VSS	T26
B13	VSS	U3
B16	VSS	U6
B19	VSS	U21
B21	VSS	U24
B24	VSS	V2
C5	VSS	V5
C8	VSS	V22
C11	VSS	V25
C14	VSS	W1
C16	VSS	W4
C19	VSS	W23
C2	VSS	W26
C22	VSS	Y3
C25	VSS	Y6
D1	VSS	Y21
D4	VSS	Y24
D8	VSS	AA2
D11	VSS	AA5
D13	VSS	AA8
D16	VSS	AA11
D19	VSS	AA14
D23	VSS	AA16
D26	VSS	AA19
E3	VSS	AA22
E8	VSS	AA25
E8	VSS	AB1
E11	VSS	AB4
E14	VSS	AB8
E16	VSS	AB11
E19	VSS	AB13
E21	VSS	AB16
E24	VSS	AB19
F5	VSS	AB23
F8	VSS	AB26
F11	VSS	AC3
F13	VSS	AC6
F16	VSS	AC8
F19	VSS	AC11
F2	VSS	AC14
F22	VSS	AC16
F25	VSS	AC19
G4	VSS	AC21
G1	VSS	AC24
G23	VSS	AD2
G26	VSS	AD5
H3	VSS	AD8
H6	VSS	AD11
H21	VSS	AD13
H24	VSS	AD16
J2	VSS	AD19
J5	VSS	AD22
J22	VSS	AD25
J25	VSS	AE1
K1	VSS	AE4
K4	VSS	AE8
K23	VSS	AE11
K26	VSS	AE14
L3	VSS	AE16
L6	VSS	AE19
L21	VSS	AE23
L24	VSS	AE26
M2	VSS	A2
M5	VSS	AF6
M22	VSS	AF8
M25	VSS	AF11
N1	VSS	AF13
N4	VSS	AF16
N23	VSS	AF19
N26	VSS	AF21
P3	VSS	A25
	VSS	AF25

BGA479-SKT6-GPU3

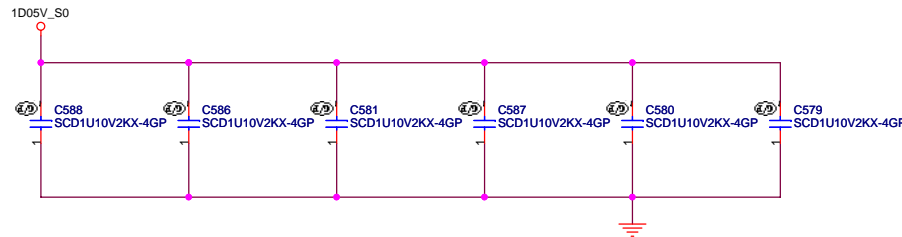
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequenced
Decoupling

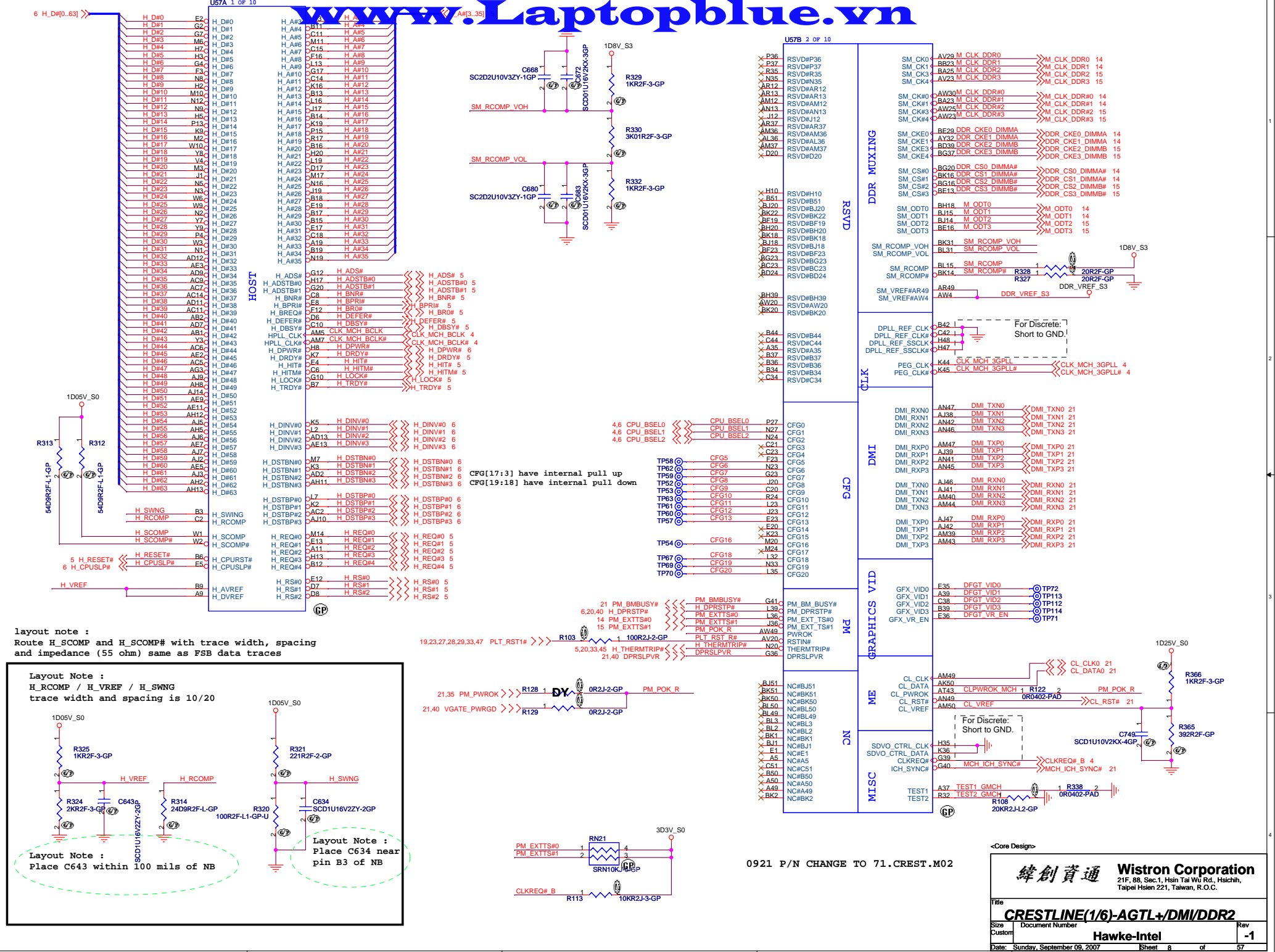


Place these
inside socket
cavity on L1
(North side
Secondary)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Meron(3/3)-GND&Bypass		
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DDR_A_D[0..63] 14
DDR_A_BS[0..2] 14
DDR_A_DM[0..7] 14
DDR_A_DQS[0..7] 14
DDR_A_DQS#[0..7] 14
DDR_A_MA[0..14] 14

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BE40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AW15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#
DDR A D50	AT5	SA_DQ50			
DDR A D51	AT7	SA_DQ51	SA_WE#	BA19	DDR A WE#
DDR A D52	AY6	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR5	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

DDR SYSTEM MEMORY A



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DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BE50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AI50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BE25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BL5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BK5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BE4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN#
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BJ2	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

DDR SYSTEM MEMORY B



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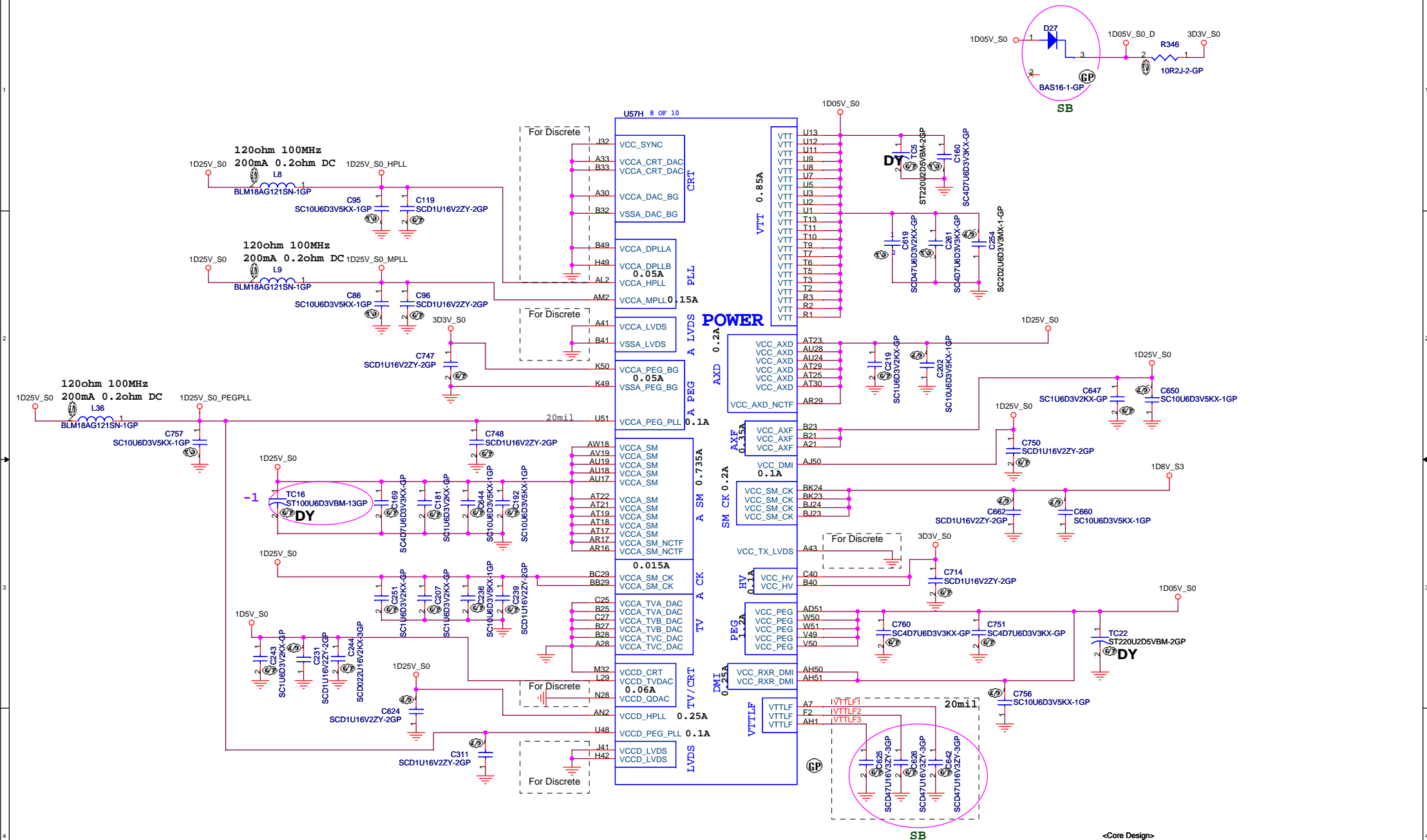
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(2/6)-DDR2 A/B CH
Size A3 Document Number
Date: Sunday, September 09, 2007 Sheet 9 of 57
Hawke-Intel
Rev -1



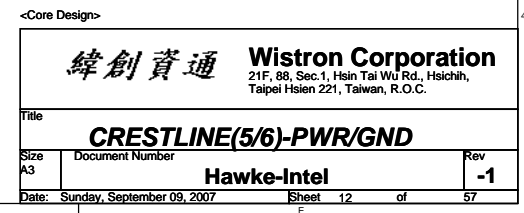
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Title			
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Size A3	Document Number		Rev
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Date: Sunday, September 09, 2007		Sheet 10 of 57	

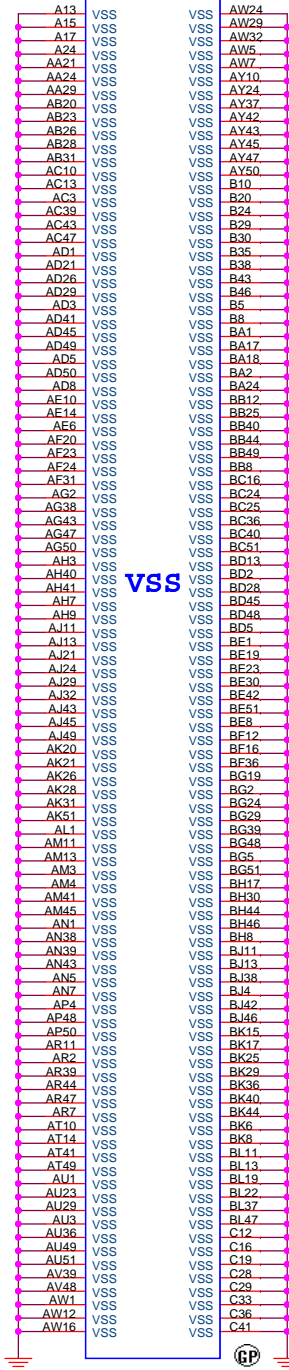


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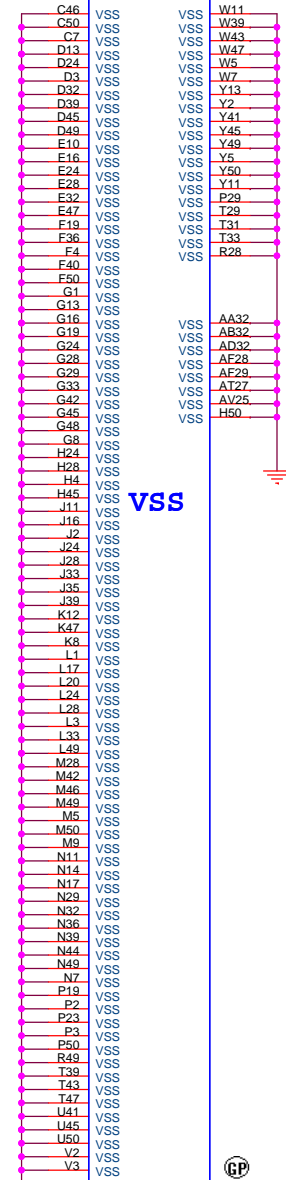
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



U57I 9 OF 10



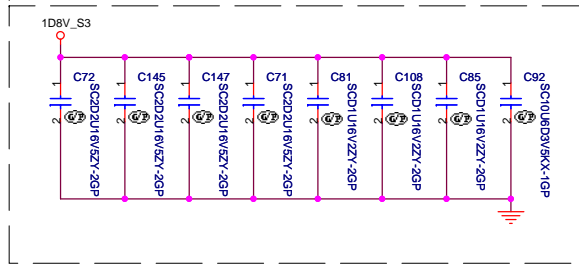
U57J10 OF 10



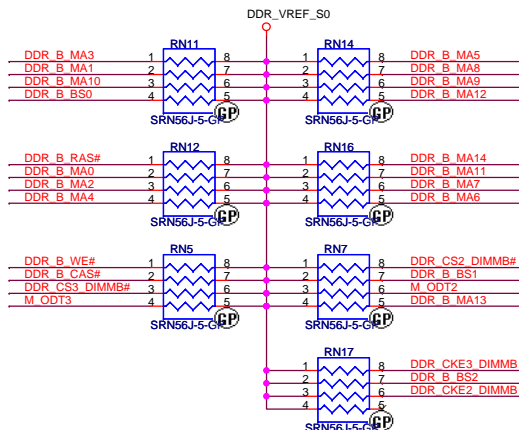
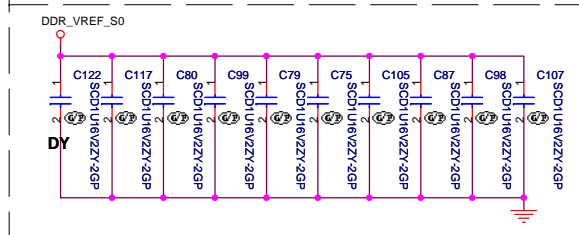
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緯創資通				Wistron Corporation			
				21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title							
DDRII-SODIMM SLOT1							
Size A3		Document Number				Rev -1	
Hawke-Intel							
Date: Sunday, September 09, 2007				Sheet 14		of 57	

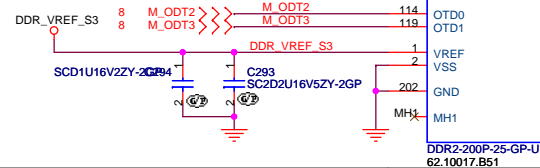
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

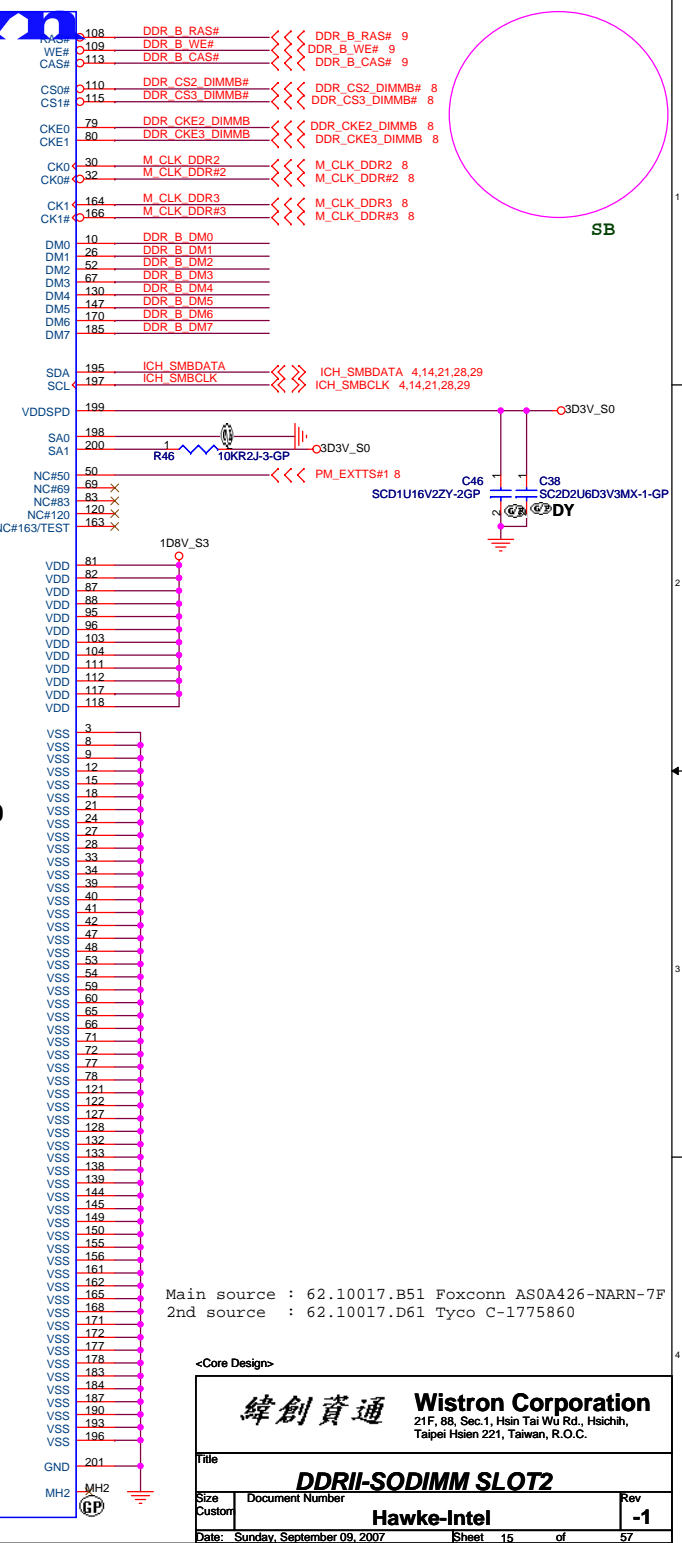


Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"



polu		DM1
DDR B MA1	101	A0
DDR B MA2	100	A1
DDR B MA3	99	A2
DDR B MA4	98	A3
DDR B MA5	97	A4
DDR B MA6	96	A5
DDR B MA7	92	A6
DDR B MA8	93	A7
DDR B MA9	91	A8
DDR B MA10	105	A9
DDR B MA11	89	A10/AP
DDR B MA12	89	A11
DDR B MA13	116	A12
DDR B MA14	116	A13
DDR B MA15	85	A14
DDR B BS2	85	A15/BA
DDR B BS0	107	BA0
DDR B BS1	106	BA1
DDR B D0	5	D00
DDR B D1	7	D01
DDR B D2	17	D02
DDR B D3	19	D03
DDR B D4	6	D04
DDR B D5	6	D05
DDR B D6	14	D06
DDR B D7	16	D07
DDR B D8	23	D08
DDR B D9	25	D09
DDR B D10	35	D10
DDR B D11	20	D11
DDR B D12	20	D12
DDR B D13	22	D13
DDR B D14	36	D14
DDR B D15	38	D15
DDR B D16	44	D16
DDR B D17	45	D17
DDR B D18	55	D18
DDR B D19	57	D19
DDR B D20	44	D20
DDR B D21	46	D21
DDR B D22	56	D22
DDR B D23	58	D23
DDR B D24	61	D24
DDR B D25	63	D25
DDR B D26	73	D26
DDR B D27	73	D27
DDR B D28	61	D28
DDR B D29	64	D29
DDR B D30	74	D30
DDR B D31	76	D31
DDR B D32	123	D32
DDR B D33	125	D33
DDR B D34	135	D34
DDR B D35	137	D35
DDR B D36	124	D36
DDR B D37	126	D37
DDR B D38	134	D38
DDR B D39	136	D39
DDR B D40	141	D40
DDR B D41	143	D41
DDR B D42	143	D42
DDR B D43	153	D43
DDR B D44	140	D44
DDR B D45	142	D45
DDR B D46	152	D46
DDR B D47	154	D47
DDR B D48	157	D48
DDR B D49	159	D49
DDR B D50	173	D50
DDR B D51	175	D51
DDR B D52	158	D52
DDR B D53	163	D53
DDR B D54	174	D54
DDR B D55	176	D55
DDR B D56	179	D56
DDR B D57	181	D57
DDR B D58	189	D58
DDR B D59	189	D59
DDR B D60	180	D60
DDR B D61	182	D61
DDR B D62	192	D62
DDR B D63	194	D63
DDR B DQS#0	11	DQS0#
DDR B DQS#1	29	DQS1#
DDR B DQS#2	49	DQS2#
DDR B DQS#3	68	DQS3#
DDR B DQS#4	124	DQS4#
DDR B DQS#5	142	DQS5#
DDR B DQS#6	167	DQS6#
DDR B DQS#7	186	DQS7#
DDR B DQ#0	13	DQ0
DDR B DQ#1	31	DQ1
DDR B DQ#2	51	DQ2
DDR B DQ#3	70	DQ3
DDR B DQ#4	131	DQ4
DDR B DQ#5	148	DQ5
DDR B DQ#6	168	DQ6
DDR B DQ#7	188	DQ7

REVERSE TYPE High 9.2 mm



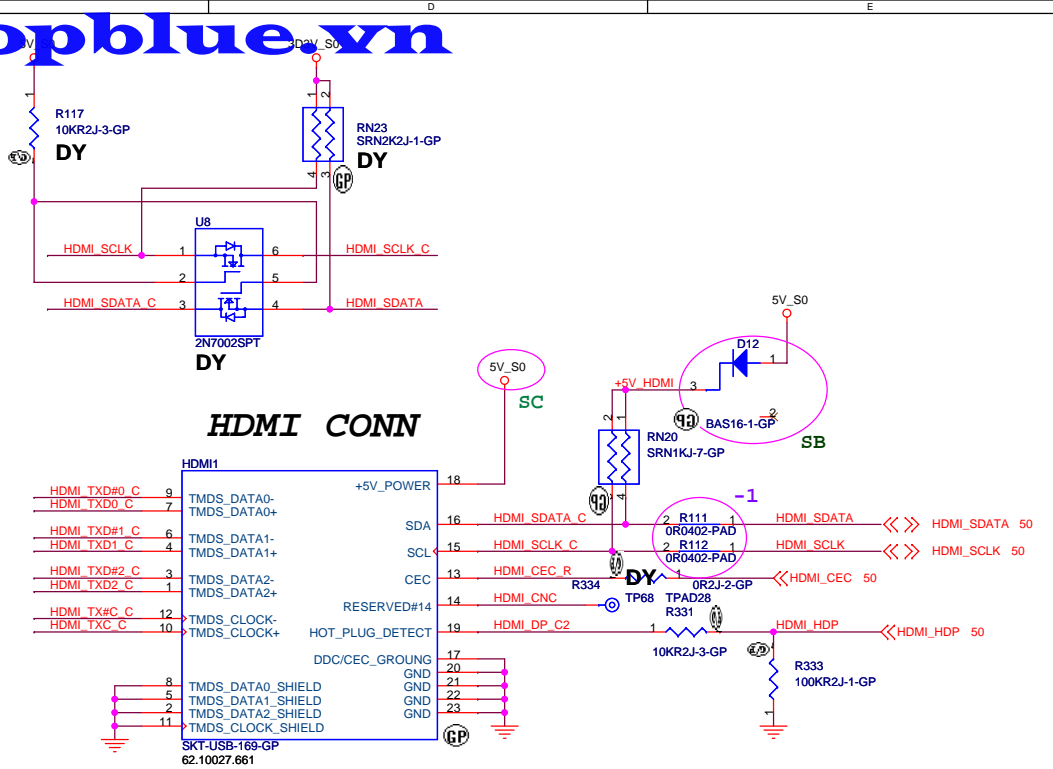
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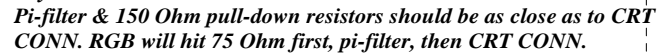
緯創資通

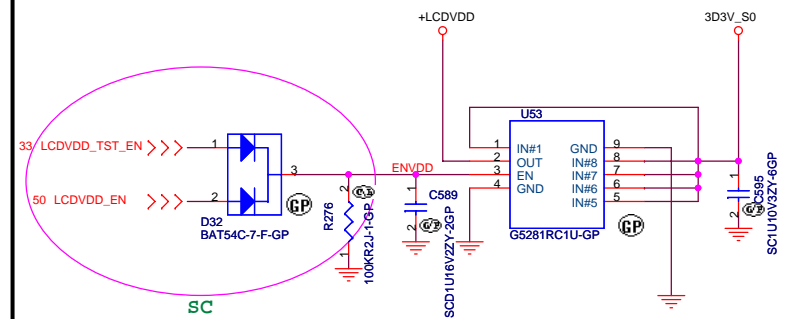
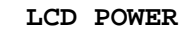
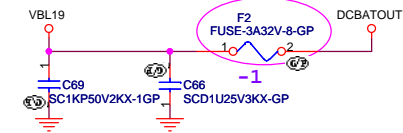
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DDRII-SODIMM SLOT2			
Size Custom	Document Number		Rev
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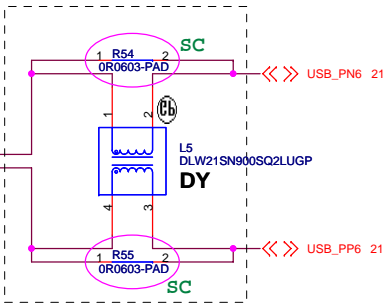


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Place near connector CAMERA1.



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD

LCD/Inverter/Camera

Size
A3

Document Number

Hawke-Intel

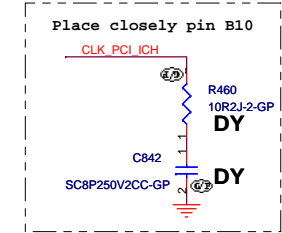
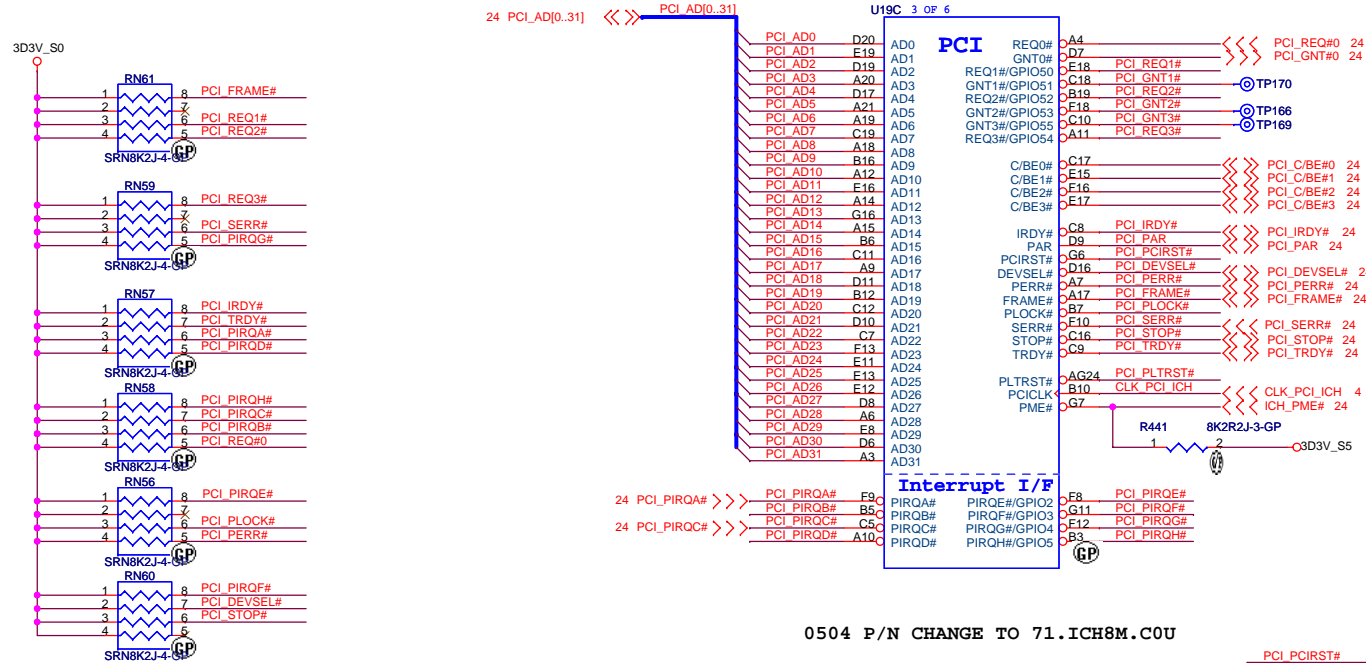
Rev
1

Date: Sunday, September 09, 2007

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PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

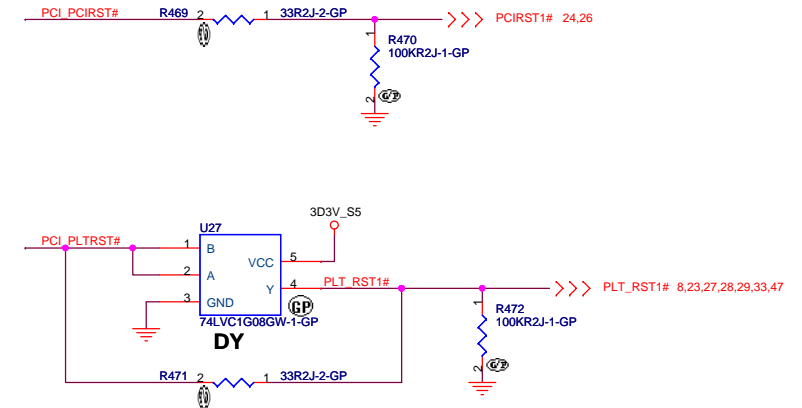
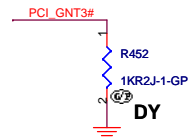


0504 P/N CHANGE TO 71.ICH8M.C0U

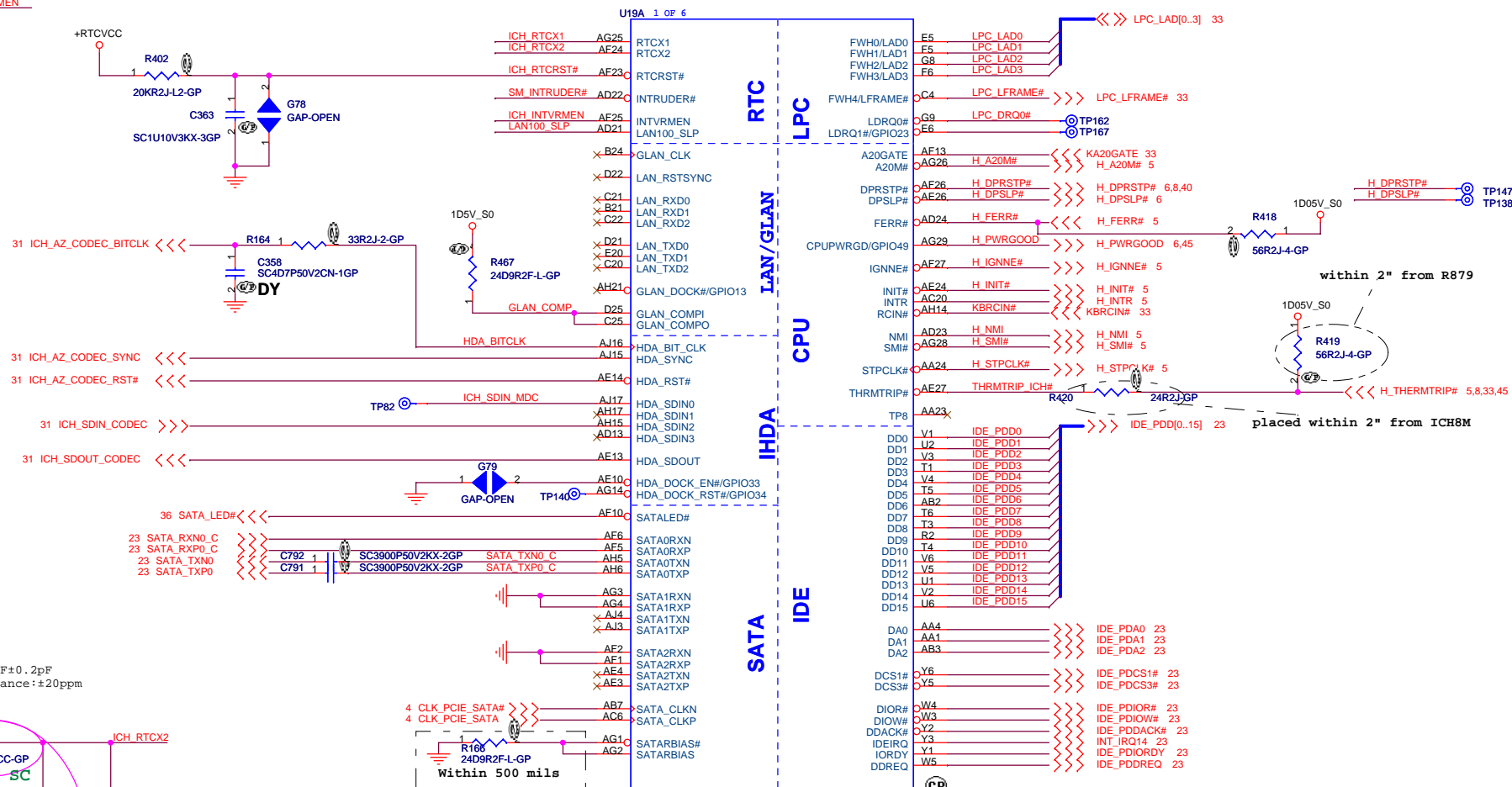
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



<Core Design>



X1 CL=12.5pF±0.2pF
Freq. Tolerance:±20ppm

SB

SC

SC

ICH_RTCX2

RESO-32D768KHZ-HP X1

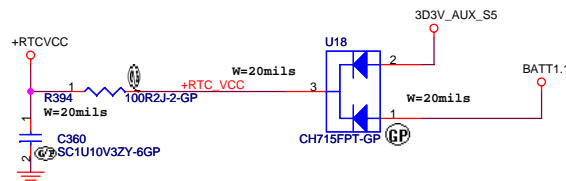
3 4

R165
10MR2JL-GP

ICH_RTCX1

C354
SC8P250V2CC-GP

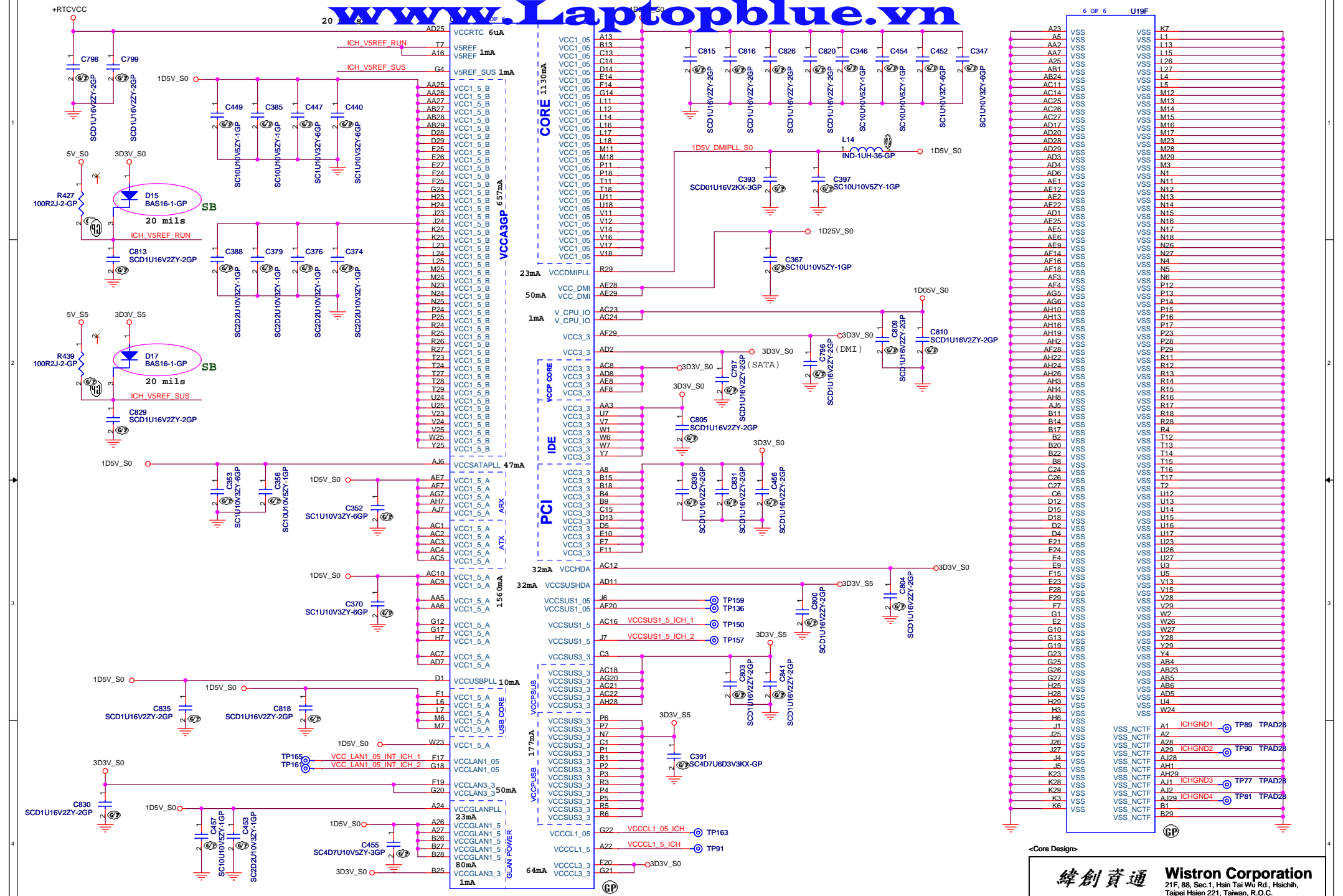
C355
SC8P250V2CC-GP



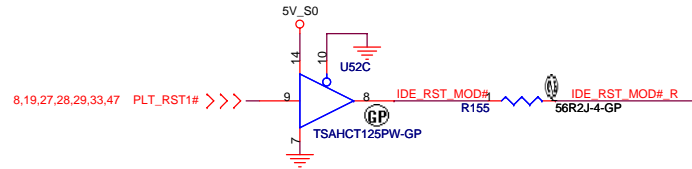
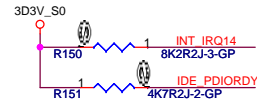
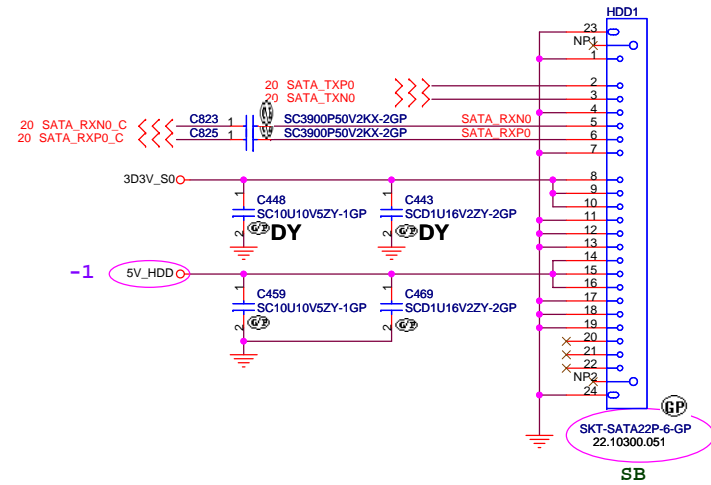
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
ICH8(2/4) LAN,HD,IDE,LPC			
Size A3	Document Number		Rev
	Hawke-Intel		-1
Date: Sunday, September 09, 2007	Sheet 20	of	57

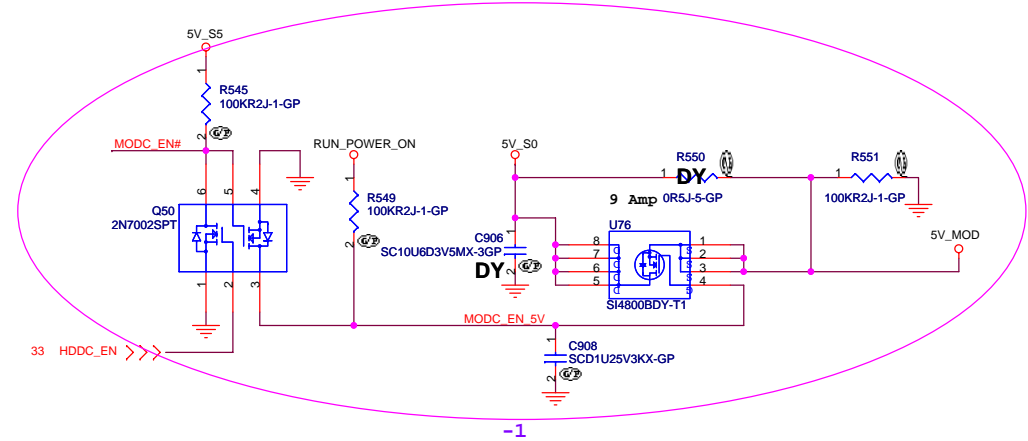
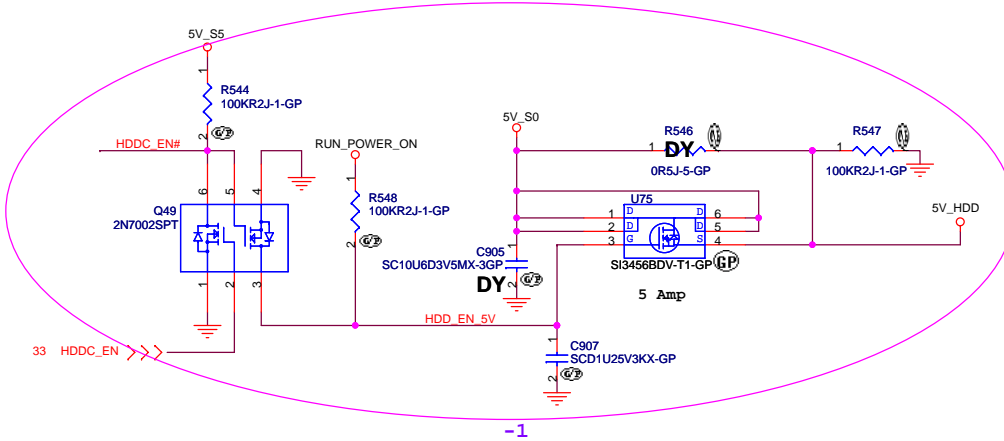
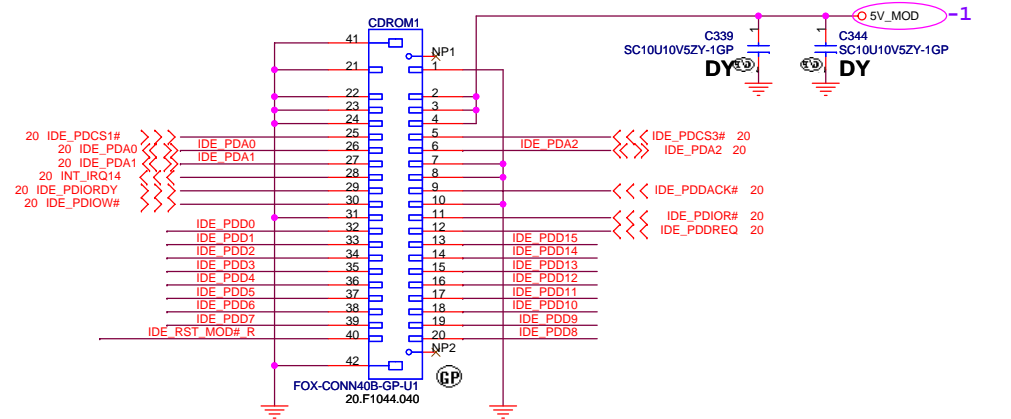




SATA HDD Connector

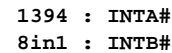


ODD Connector

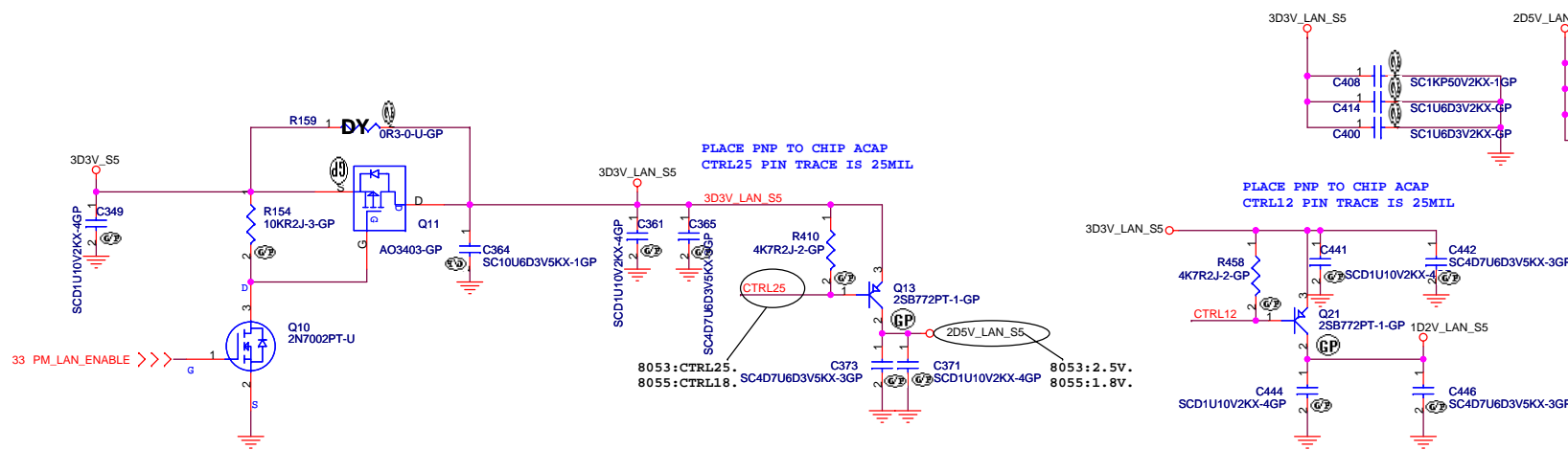
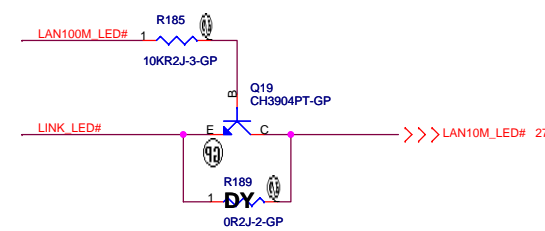
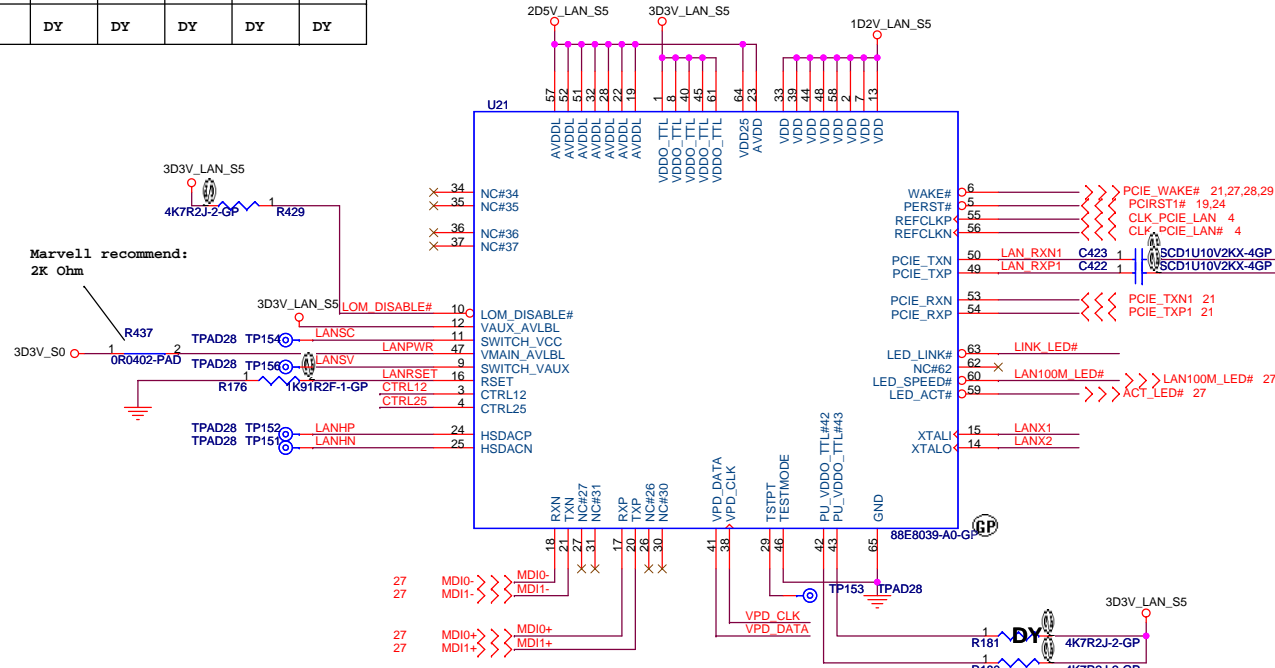


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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size		
A3		
Document Number		
HDD/ODD		
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-1		

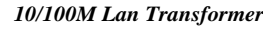




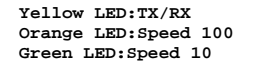
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Title			
LAN MARVELL			
Size A3	Document Number		Rev
	Hawke-Intel		-1
Date: Sunday, September 09, 2007		Sheet 26 of	57

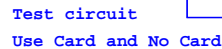


SC

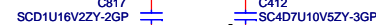


SE

Place them Near to Chip

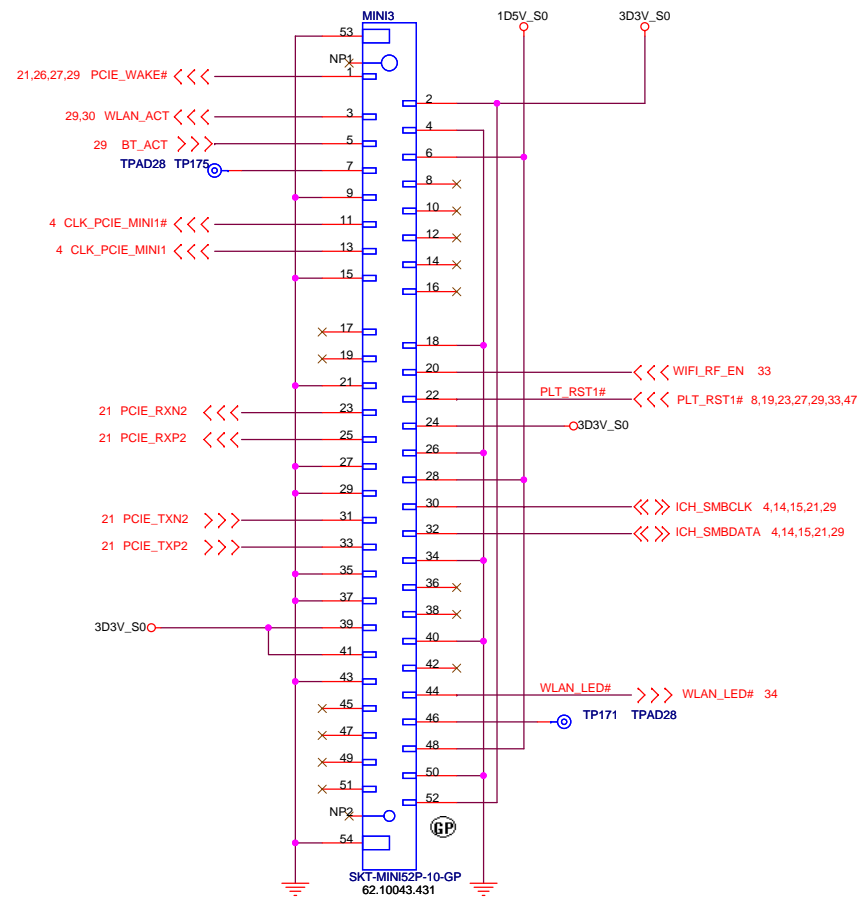


DY

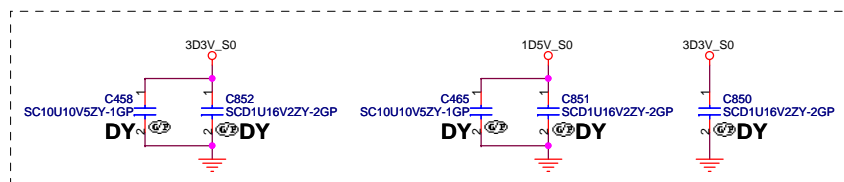


Title			
LAN connector/NEW CARD			
Size A3	Document Number	Rev	
	Hawke-Intel	-1	
Date:	Sunday, September 09, 2007	Sheet	27 of 57

Mini Card Connector 1(802.11a/b/g)

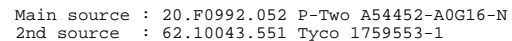


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2nd source : 62.10043.551 Tyco 1759553-1



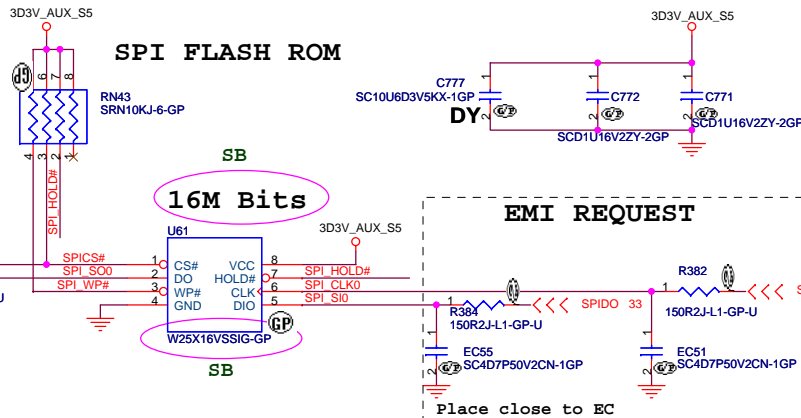
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Title		
MINI CARD CONN 1		
Size	Document Number	Rev
A3	Hawke-Intel	-1
Date: Sunday, September 09, 2007		
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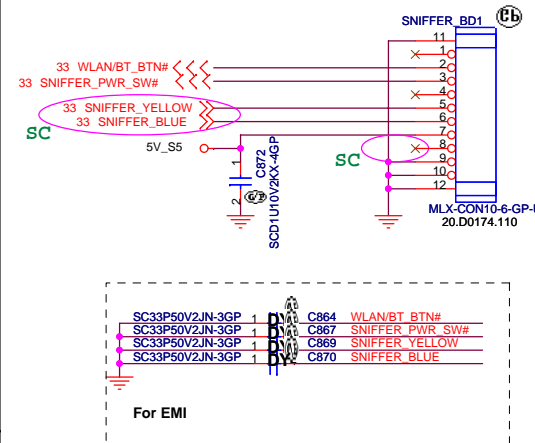


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Taipei Hsien 221, Taiwan, R.O.C.

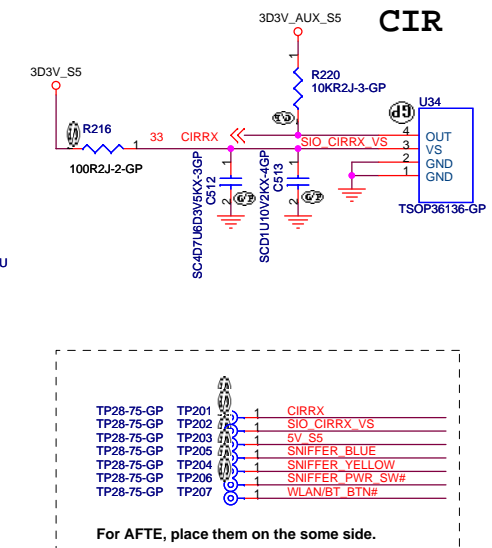
Title			
MINI CARD CONN 2 & 3			
Size A3	Document Number	Rev	
	Hawke-Intel	-1	
Date:	Sunday, September 09, 2007	Sheet	29 of 57



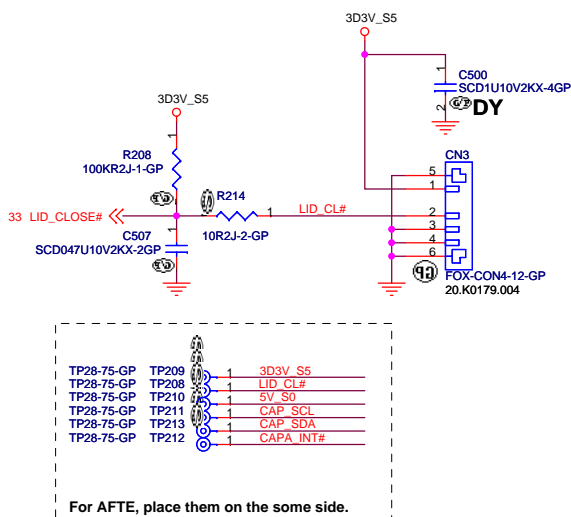
Switch Board



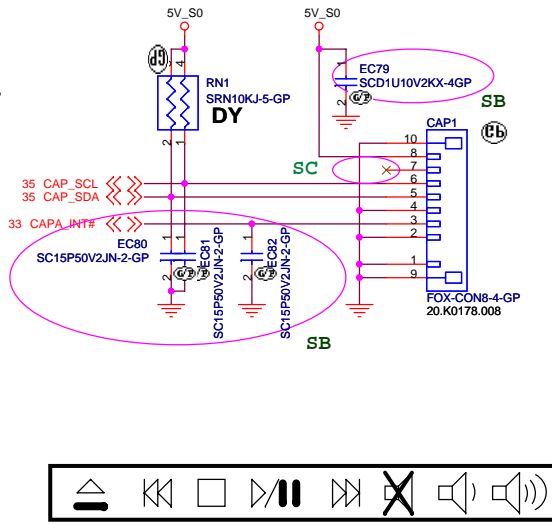
CIR



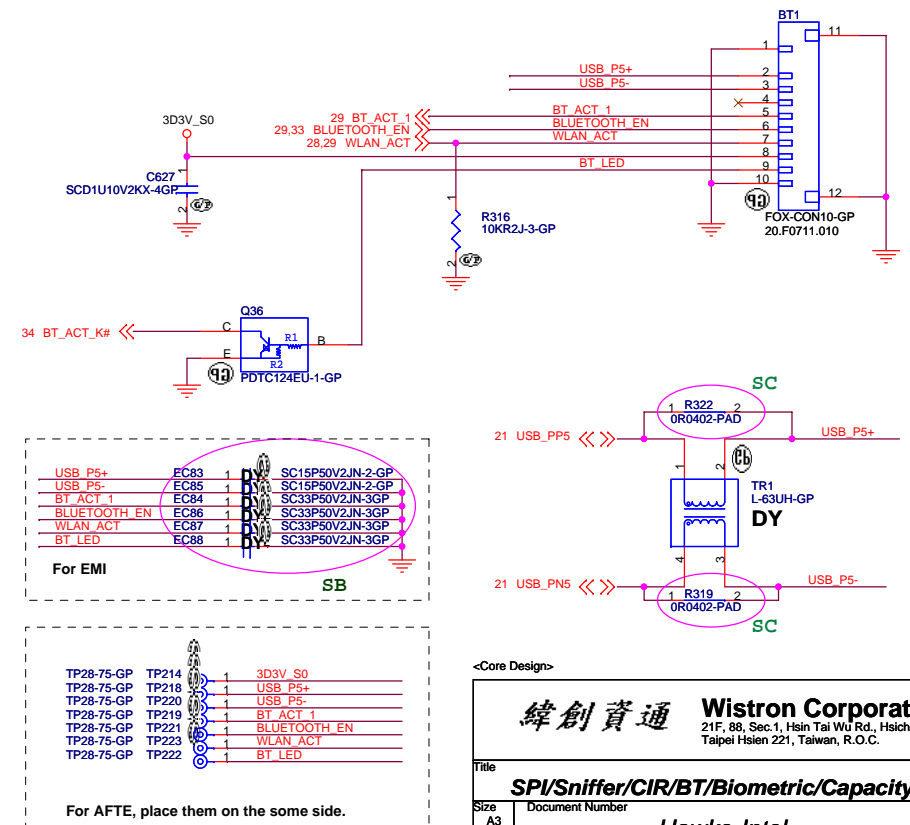
Hall Switch conn.



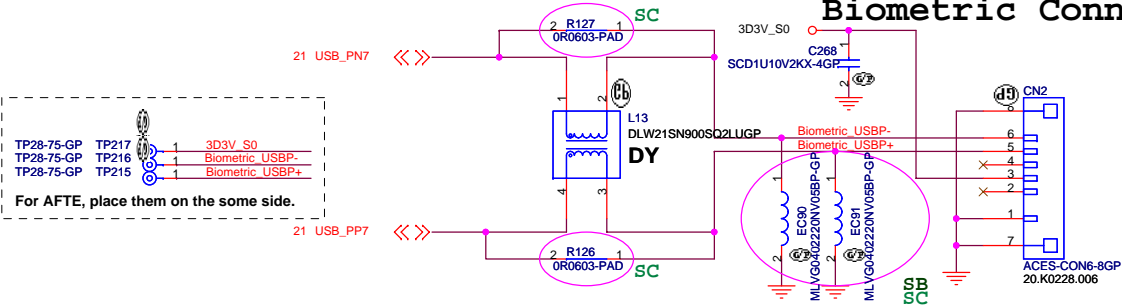
Capacity Button conn.



Bluetooth Module conn.



Biometric Conn.



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.



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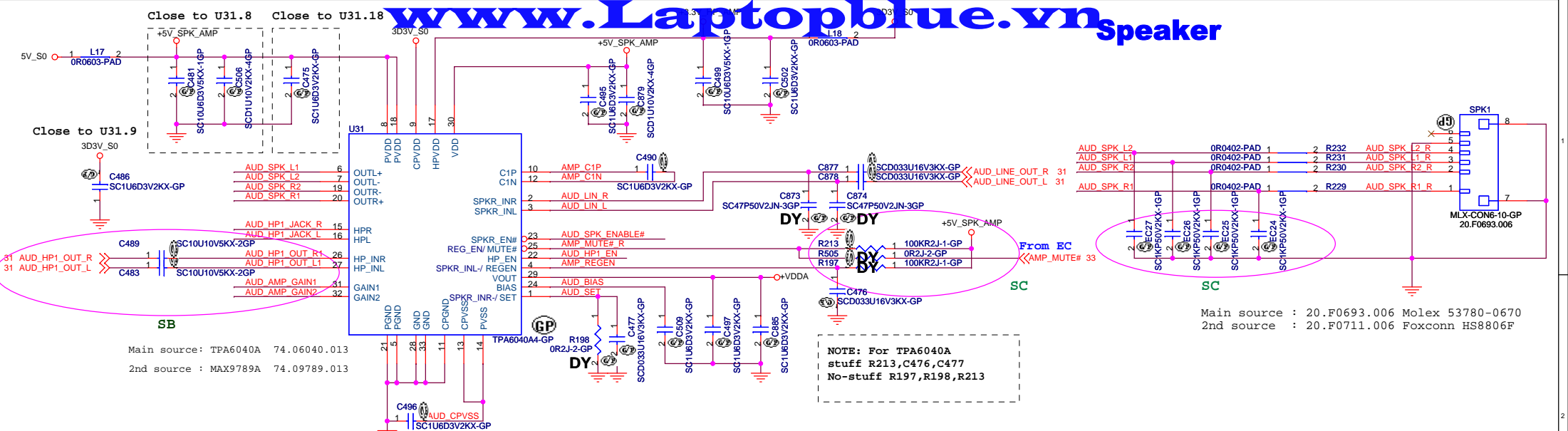
Sheet 31

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Sheet :

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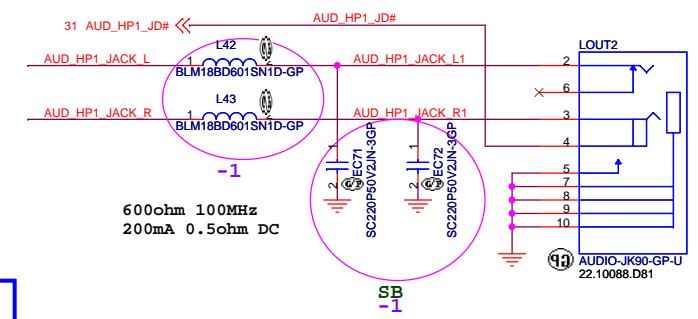


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2nd source : MAX9789A 74.09789.013

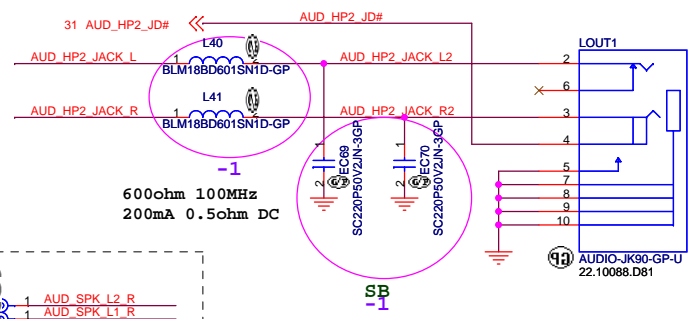
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NOTE: For TPA6040A
stuff R213, C476, C477
No-stuff R197, R198, R213

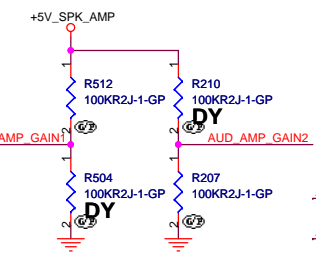
LINE1 OUT



LINE2 OUT

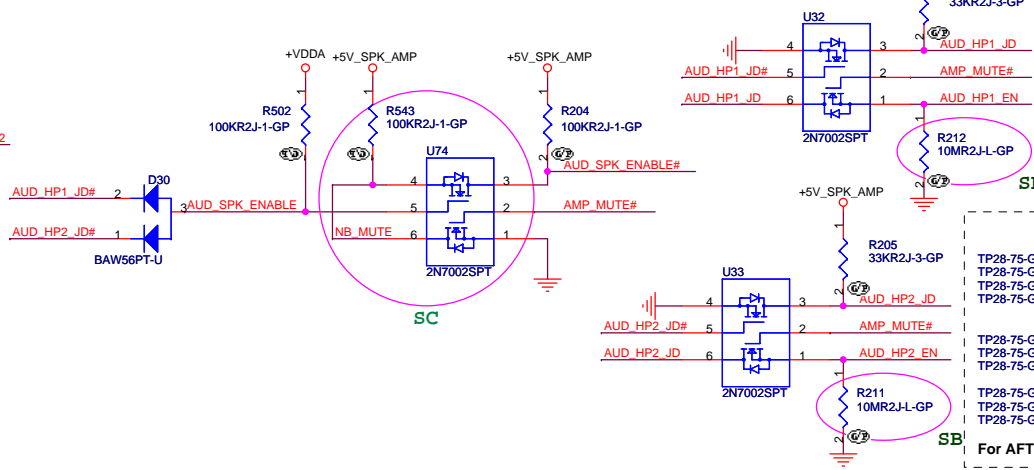


GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



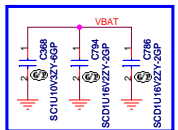
TP28-75-GP	TP227	1	AUD SPK L2 R
TP28-75-GP	TP228	1	AUD SPK L1 R
TP28-75-GP	TP230	1	AUD SPK R2 R
TP28-75-GP	TP229	1	AUD SPK R1 R
TP28-75-GP	TP232	1	AUD HP1 JD#
TP28-75-GP	TP231	1	AUD HP1 JACK L1
TP28-75-GP	TP233	1	AUD HP1 JACK R1
TP28-75-GP	TP234	1	AUD HP2 JD#
TP28-75-GP	TP235	1	AUD HP2 JACK L2
TP28-75-GP	TP236	1	AUD HP2 JACK R2

For AFTE, place them on the some side.

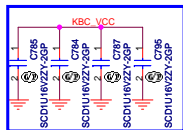
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

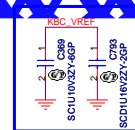
Title		
AUDIO AMP/SPEAKER		
Size A3	Document Number	Rev
	Hawke-Intel	-1
Date: Sunday, September 09, 2007	Sheet 32	of 57



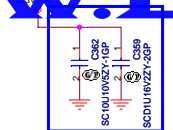
PLACE CAP NEAR PIN80 AND PIN102



PLACE CAP NEAR PIN46,19,115,76,88



PLACE CAP NEAR PIN104



PLACE CAP Close to Pin 4

WPC8763L STRAP PIN

JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

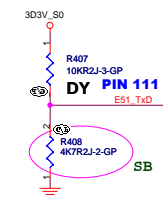
TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins, if an external 10 KΩ pull-down resistor is connected.

BADDR1-0 (PIN 111, 112) I/O Base Address.

10KΩ external pull-down

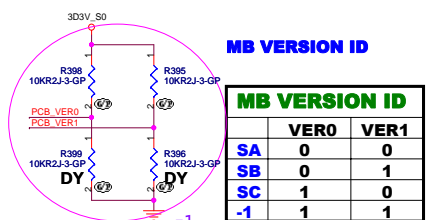
resistor on BADDR1: Core defined



SHBM PIPN83 Shared Host BIOS Memory.

HIGH:NO SHARED(internal resistor)

LOW:SHARED BIOS memory.

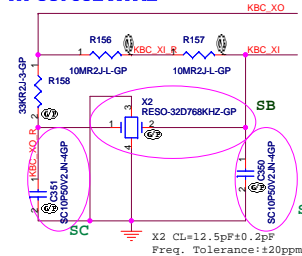


MB VERSION ID

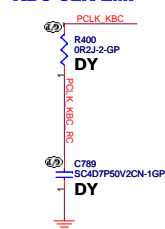
MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

WPC8763L XTAL



KBC CLK EMI



For Thermal and Capacity button module

21,39,42,44,45,53 PM_SLP_S3#

34 POWER_SW#

18 LCD_CBL_DET#

38 AC_IN#

30 LID_CLOSE#

34 INSTANT_BTN#

21,24 PM_CLKRUN#

37 BAT_IN#

18 BRIGHTNESS

30 CHRG#

36 BATFULL_LED

37 ACDC_ID

36 PWLED

21 PM_PWRBTN#

34-SKRLK-LED

29 WLAN_EN

23 HBBG_EN

53 GFX_CORE_ON

34 NUM_LED

34 CAP_LED

34,36 LED_MASK#

30 SNIFFER_BLUE

18 LCD_TST

48 SL_ENABLE

21 KSMRST# KBC

37 AD_OFF

26 PM_LAN_ENABLE

36 CHARGE_LED

30 CAPA_INT#

34-WLAN-TEST

TPAD28 TP301

37 PSID_DISABLE#

30 WLANBT_BTNR#

SC-18 LCDVDD_TST_EN

50 PANEL_BKEN

24 GB_RST#

GPIO01

GPIO03

GPIO05

GPIO06

GPIO07

GPIO10

GPIO11

GPIO12

GPIO13

GPIO14

GPIO15

GPIO16

GPIO17

GPIO18

GPIO19

GPIO20

GPIO21

GPIO22

GPIO23

GPIO24

GPIO25

GPIO26

GPIO27

GPIO28

GPIO29

GPIO30

GPIO31

GPIO32

GPIO33

GPIO34

GPIO35

GPIO36

GPIO37

GPIO38

GPIO39

GPIO40

GPIO41

GPIO42

GPIO43

GPIO44

GPIO45

GPIO46

GPIO47

GPIO48

GPIO49

GPIO50

GPIO51

GPIO52

GPIO53

GPIO54

GPIO55

GPIO56

GPIO57

GPIO58

GPIO59

GPIO60

GPIO61

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GPIO64

GPIO65

GPIO66

GPIO67

GPIO68

GPIO69

GPIO70

GPIO71

GPIO72

GPIO73

GPIO74

GPIO75

GPIO76

GPIO77

GPIO78

GPIO79

GPIO80

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GPIO84

GPIO85

GPIO86

GPIO87

GPIO88

GPIO89

GPIO90

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GPIO93

GPIO94

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GPIO96

GPIO97

GPIO98

GPIO99

GPIO100

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GPIO102

GPIO103

GPIO104

GPIO105

GPIO106

GPIO107

GPIO108

GPIO109

GPIO110

GPIO111

GPIO112

GPIO113

GPIO114

GPIO115

GPIO116

GPIO117

GPIO118

GPIO119

GPIO120

GPIO121

GPIO122

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GPIO124

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GPIO126

GPIO127

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GPIO146

GPIO147

GPIO148

GPIO149

GPIO150

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GPIO159

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GPIO163

GPIO164

GPIO165

GPIO166

GPIO167

GPIO168

GPIO169

GPIO170

GPIO171

GPIO172

GPIO173

GPIO174

GPIO175

GPIO176

GPIO177

GPIO178

GPIO179

GPIO180

GPIO181

GPIO182

GPIO183

GPIO184

GPIO185

GPIO186

GPIO187

GPIO188

GPIO189

GPIO190

GPIO191

GPIO192

GPIO193

GPIO194

GPIO195

GPIO196

GPIO197

GPIO198

GPIO199

GPIO200

GPIO201

GPIO202

GPIO203

GPIO204

GPIO205

GPIO206

GPIO207

GPIO208

GPIO209

GPIO210

GPIO211

GPIO212

GPIO213

GPIO214

GPIO215

GPIO216

GPIO217

GPIO218

GPIO219

GPIO220

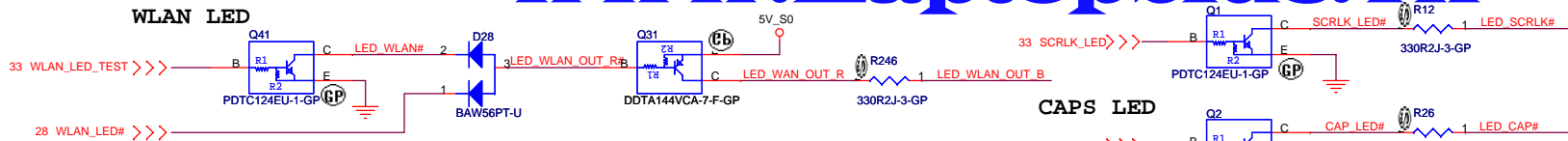
GPIO221

GPIO222

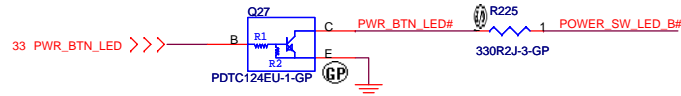
GPIO223



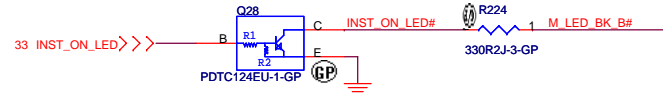
WLAN LED



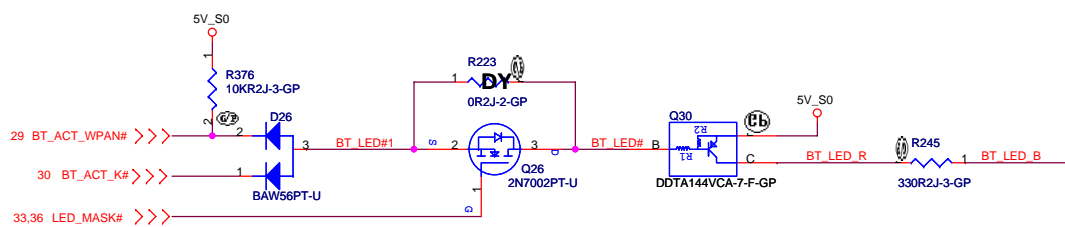
Power Button LED



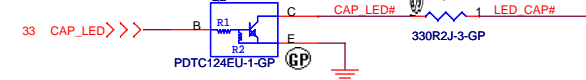
Instant Power Button LED



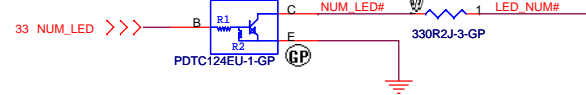
Bluetooth LED



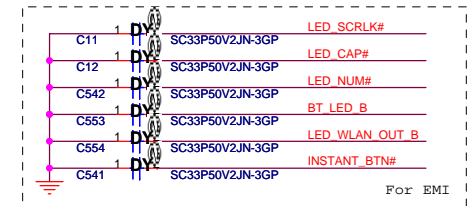
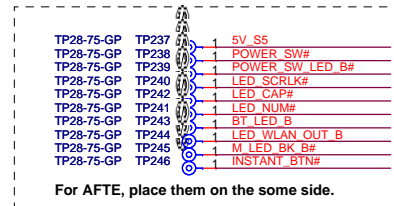
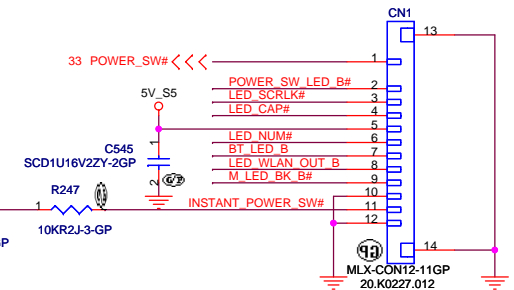
CAPS LED



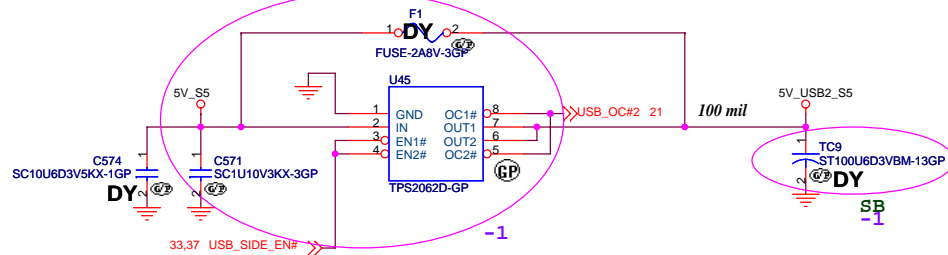
NUM LED



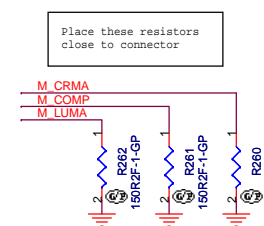
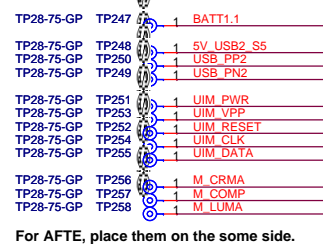
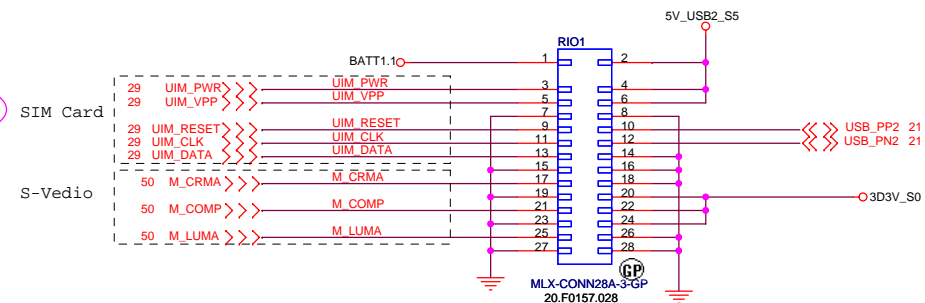
To LED Board



USB POWER

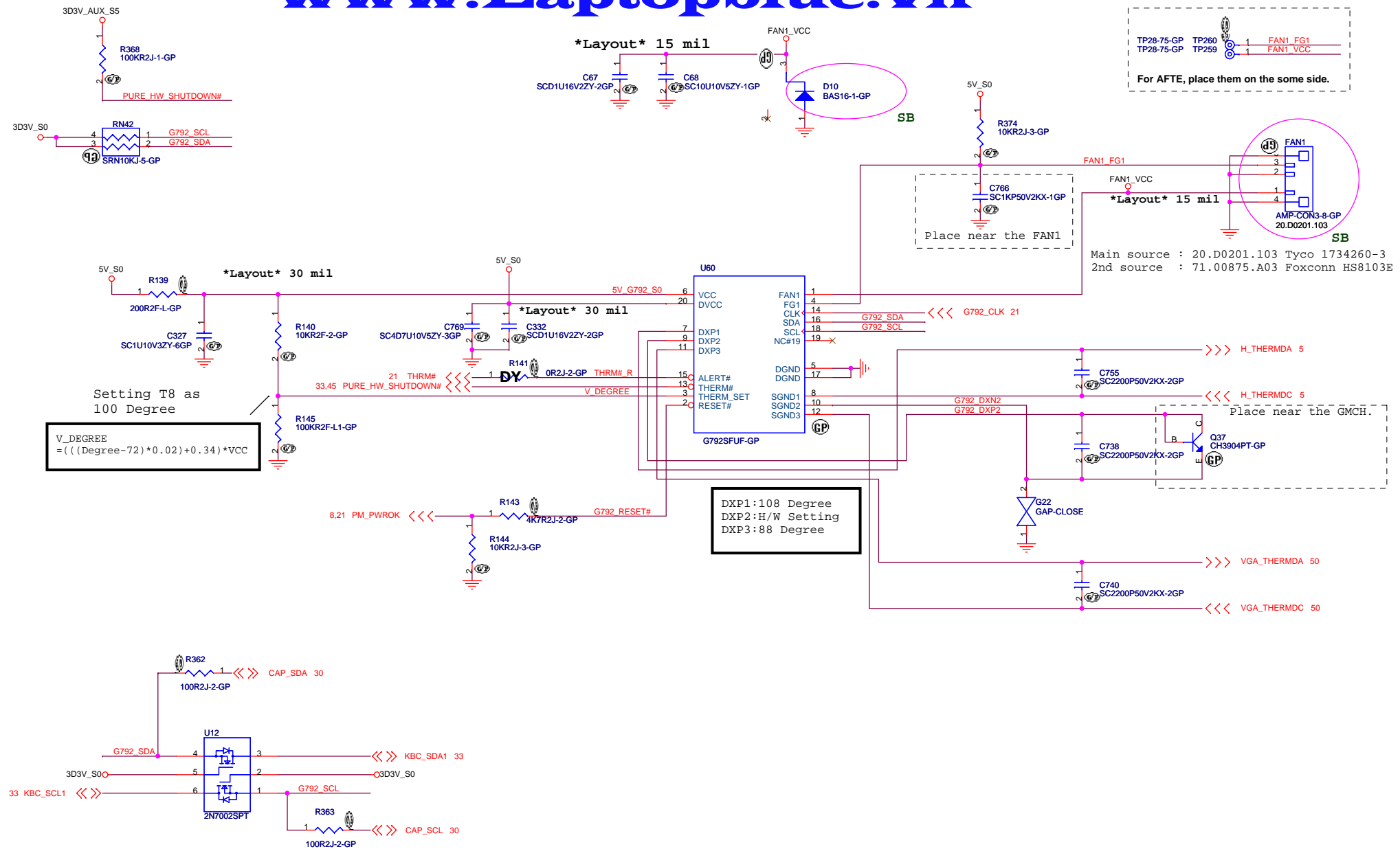


To Right I/O Board



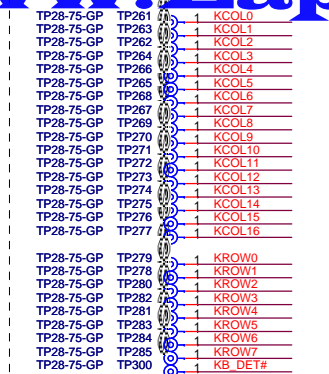
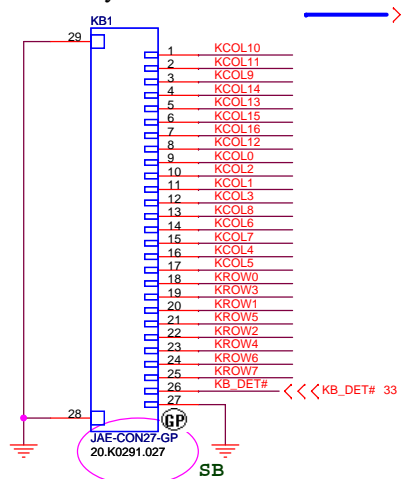
<Core Design>

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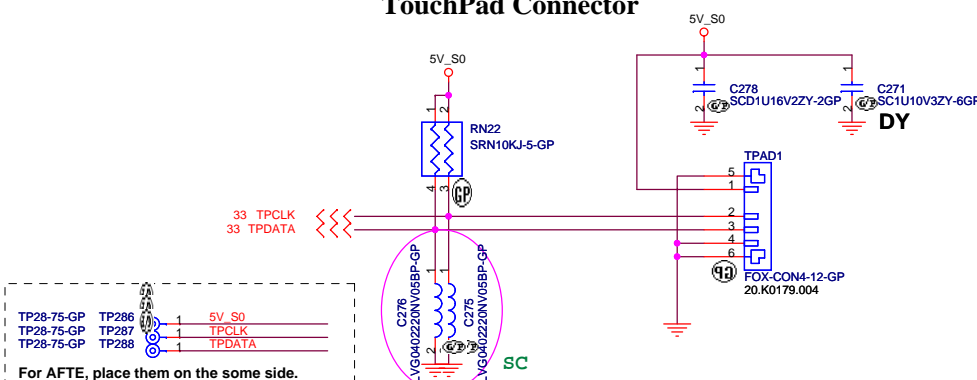
<Core Design>

Internal KeyBoard Connector



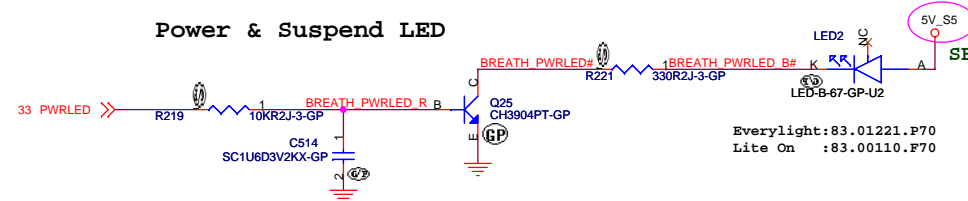
For AFTE, place them on the same side.

TouchPad Connector



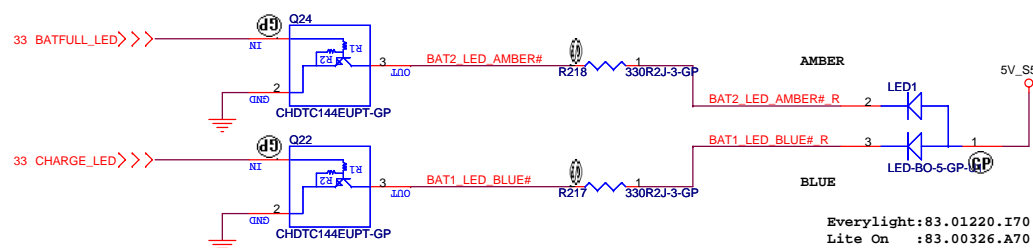
For AFTE, place them on the same side.

Power & Suspend LED



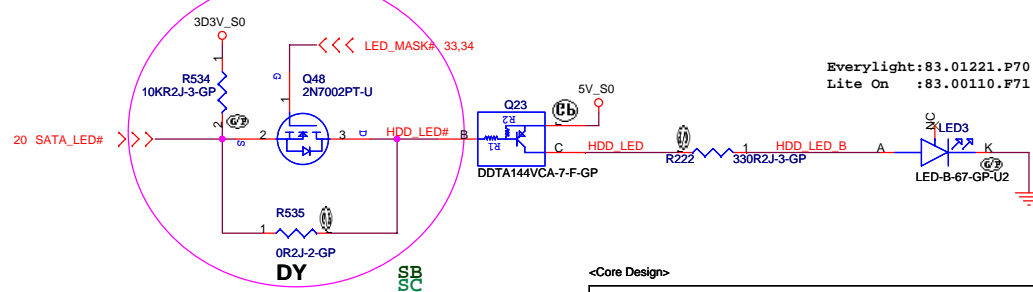
Everylight:83.01221.P70
Lite On :83.00110.F70

Battery LED



Everylight:83.01220.I70
Lite On :83.00326.A70

HDD LED



Everylight:83.01221.P70
Lite On :83.00110.F71

LED Board

LED NAME	ACTIVE SIGNAL
Power Button LED	PWR_BTN_LED
Instant Power Button LED	INST_ON_LED
WLAN LED	WLAN_LED_TEST (from KBC)
Bluetooth LED	BT_ACT_WPAN# (from Mini)
NUM LED	BT_ACT_K# (from BT)
SCRLK LED	NUM_LED (from KBC)
CAPS LED	SCRLK_LED (from KBC)
	CAP_LED (from KBC)

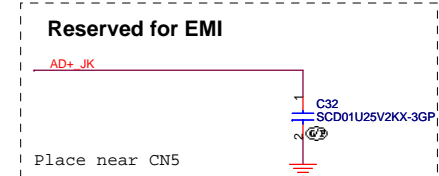
Main Board

Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC)
	CHARGE_LED (from KBC)

<Core Design>

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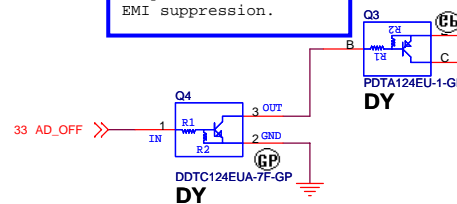
Title	KeyBoard/Touchpad	Rev
Size	Document Number	A3
Date:	Sunday, September 09, 2007	Sheet 36 of 57
	Hawke-Intel	-1



For AFTE, place them on the same side.

This cap should be used only as last resort for EMI suppression.

Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm



Batt Connector

The diagram illustrates the electrical connections for the Batt Connector (CN4). The connector pins are numbered 1 through 11. The connections are as follows:

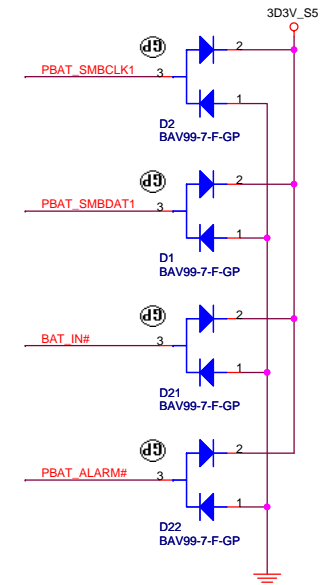
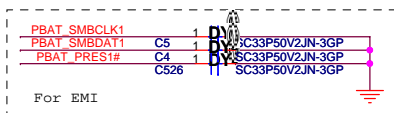
- Pin 1:** BATT1+ (connected to BT+)
- Pin 2:** BATT2+ (connected to BT+)
- Pin 3:** CLK_SMB (connected to R6)
- Pin 4:** DAT_SMB (connected to R5)
- Pin 5:** BATT_PRES# (connected to R241)
- Pin 6:** SYS_PRES# (connected to R241)
- Pin 7:** BAT_ALERT (connected to TP96)
- Pin 8:** GND1 (connected to GND)
- Pin 9:** GND2 (connected to GND)
- Pin 10:** GND (connected to GND)
- Pin 11:** GND (connected to GND)

Other components and connections shown include:

- Resistors:** R2 (0R0603-PAD), R6 (100R2J-2-GP), R5 (100R2J-2-GP), R241 (100R2J-2-GP), R244 (100KR2J-1-GP).
- Capacitors:** C6 (SCD1U25V3KX-GP), C3 (SC2200P50V2KX-2GP).
- Microcontroller (U1):** SYN-C0N9-1-GP-U1.
- Temperature Sensor (TP96):** Connected to Pin 7.
- Battery Management System (BT+):** Connected to Pin 1.
- Other Labels:** BAT_SCL 18,33,38, BAT_SDA 18,33,38, BAT_IN# 33, OD3V_S5.

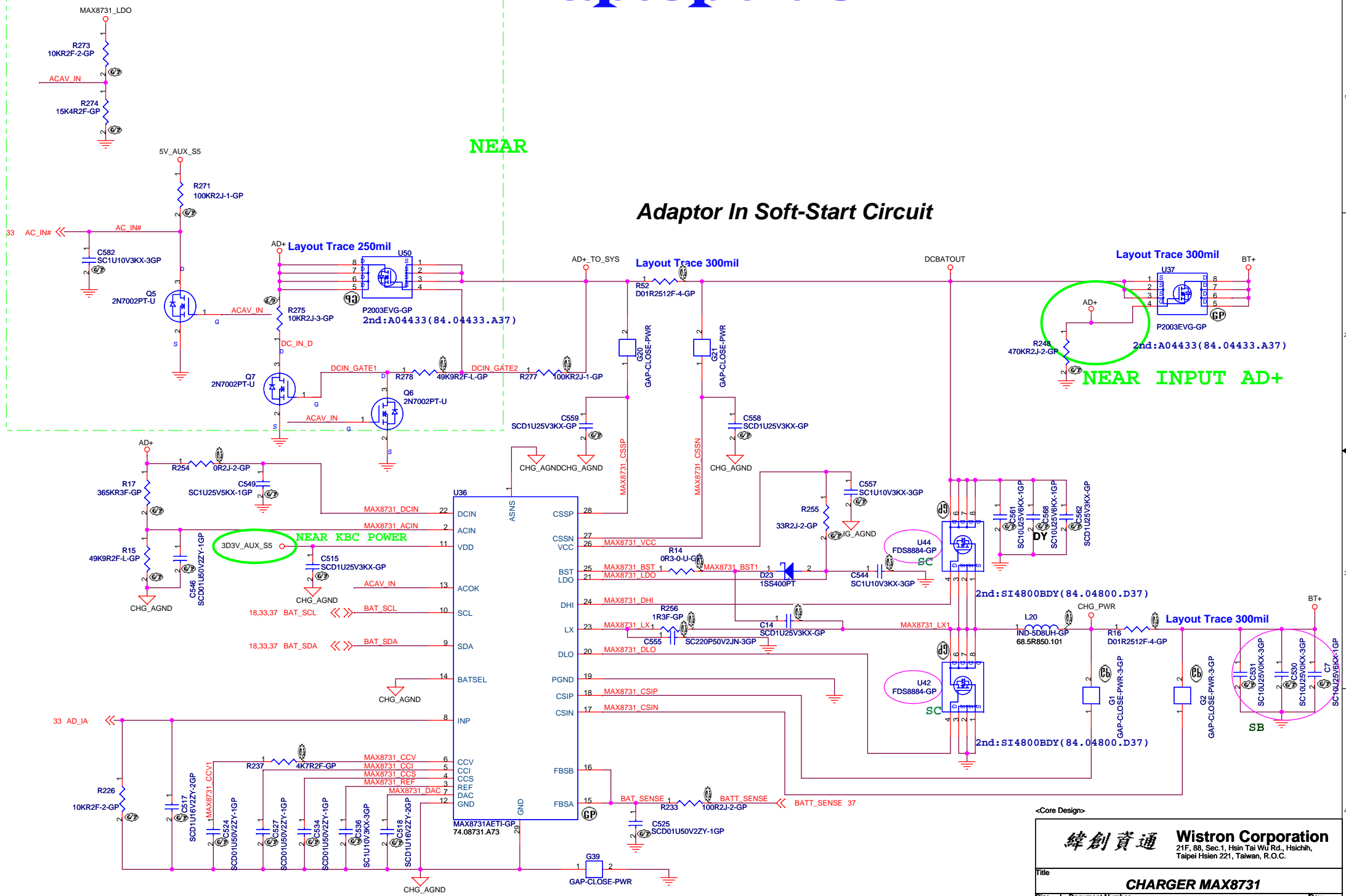
TP28-75-GP	TP296	1	BT+
TP28-75-GP	TP297	1	PBAT SMBCLK1
TP28-75-GP	TP298	1	PBAT SMBDAT1
TP28-75-GP	TP299	1	PBAT PRES1#

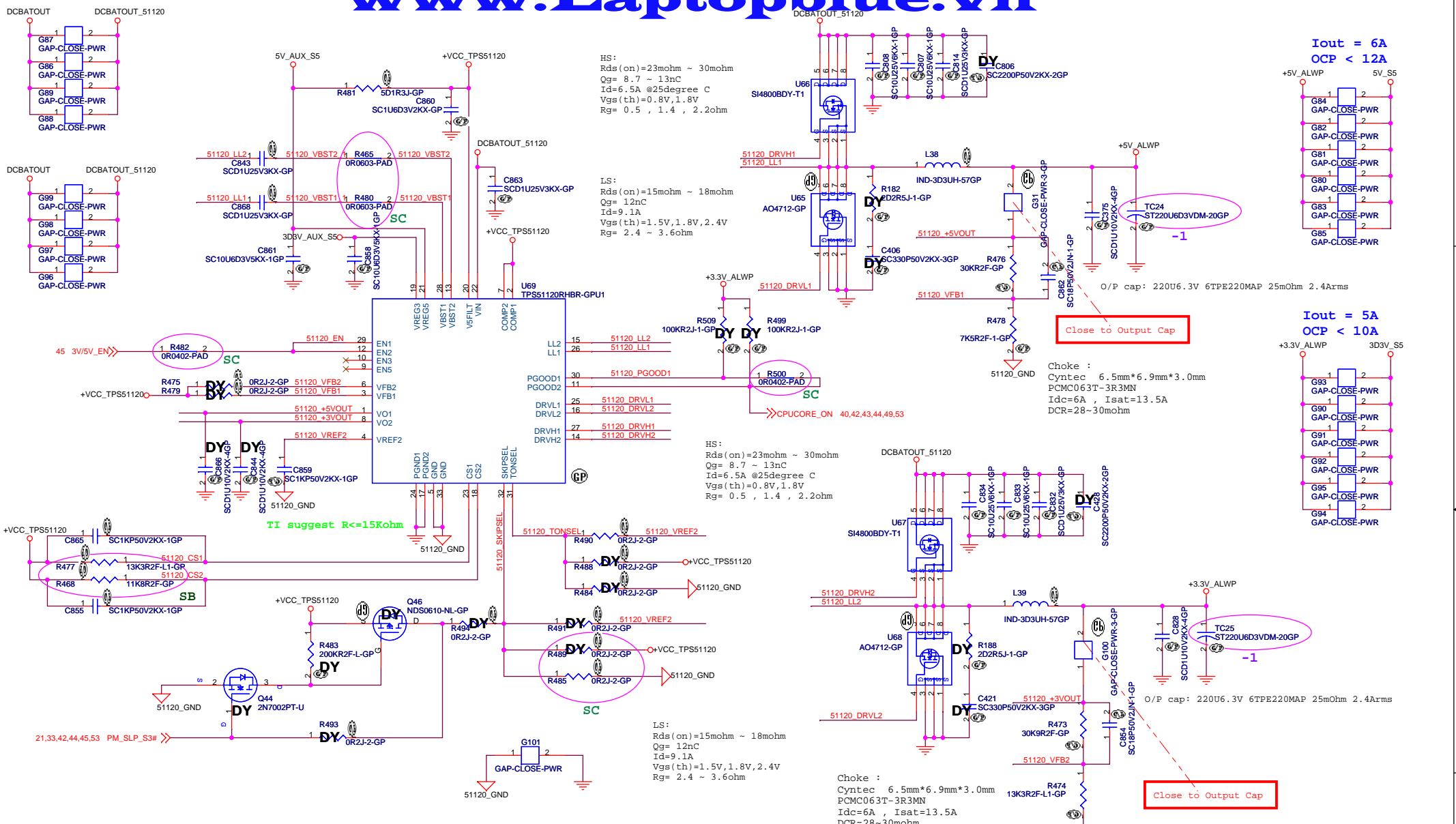
For AFTE, place them on the same side.



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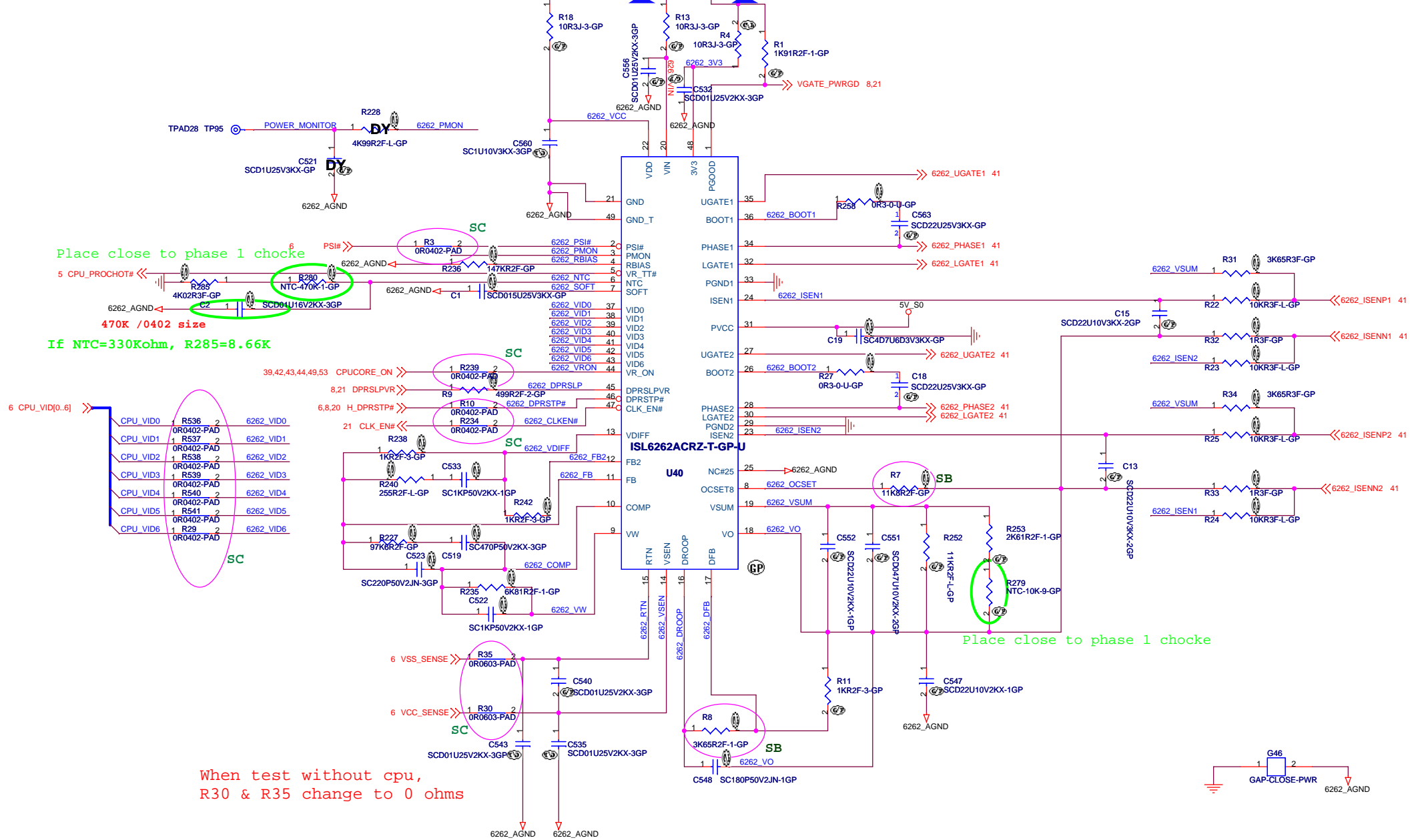
Title			
AD/BATT CONN			
Size	Document Number	Rev	
A3	Hawke-Intel	-1	
Date:	Sunday, September 09, 2007	Sheet	37 of 57





$$V_{out} = 1V \cdot (R1 + R2) / R2$$

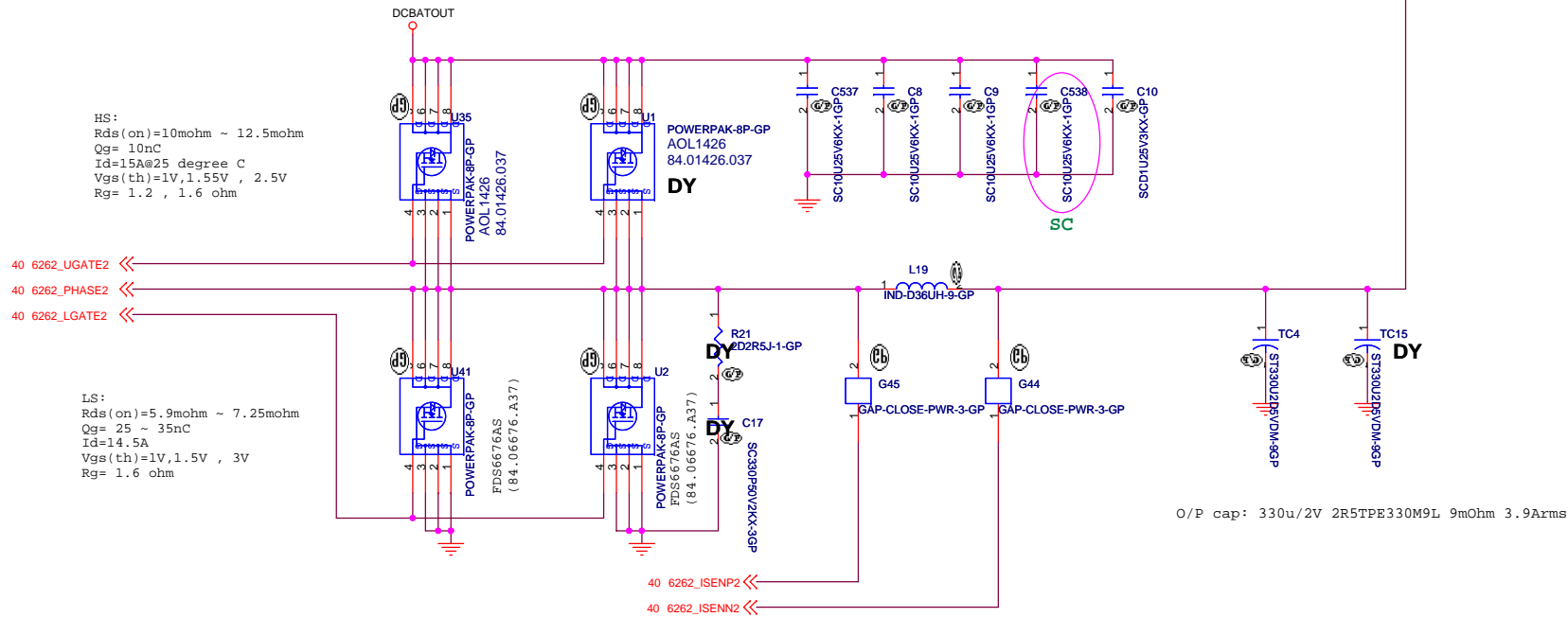
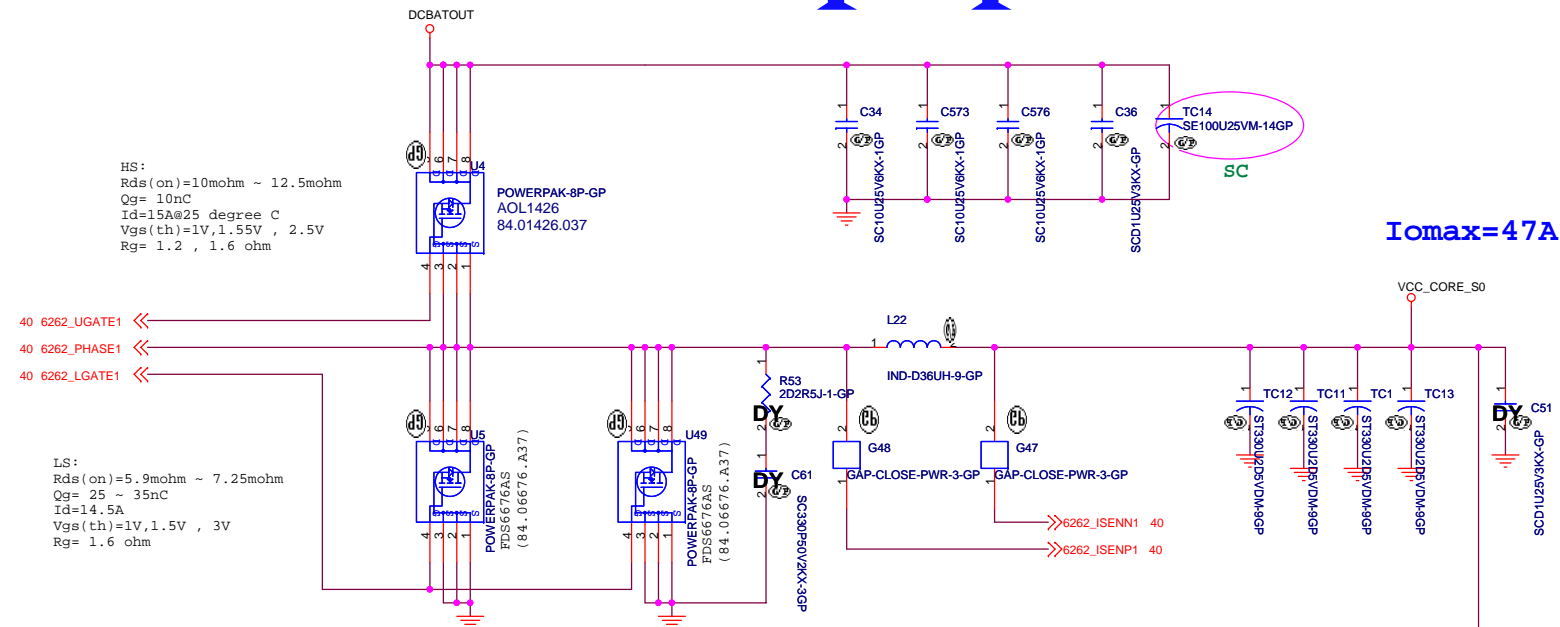
	GROUND	VREF2	FLDLY	VSPILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



<Core Design>

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Title			DC-DC VCCCPUCORE 1/2
Size	Document Number	Rev	
A3		-1	
Date: Sunday, September 09, 2007		Sheet	40 of 57

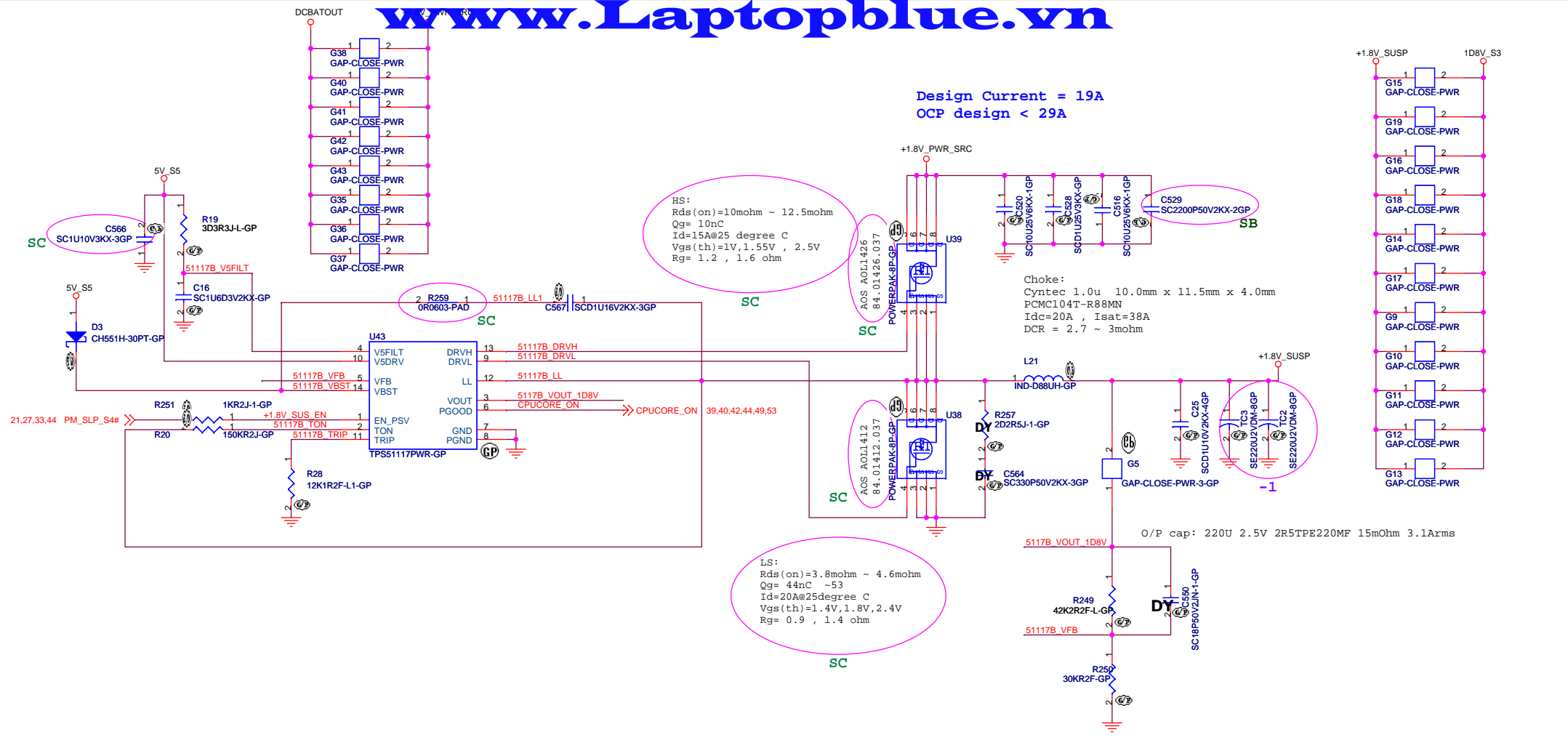


If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R44/R45/R46/R47.

<Core Design>

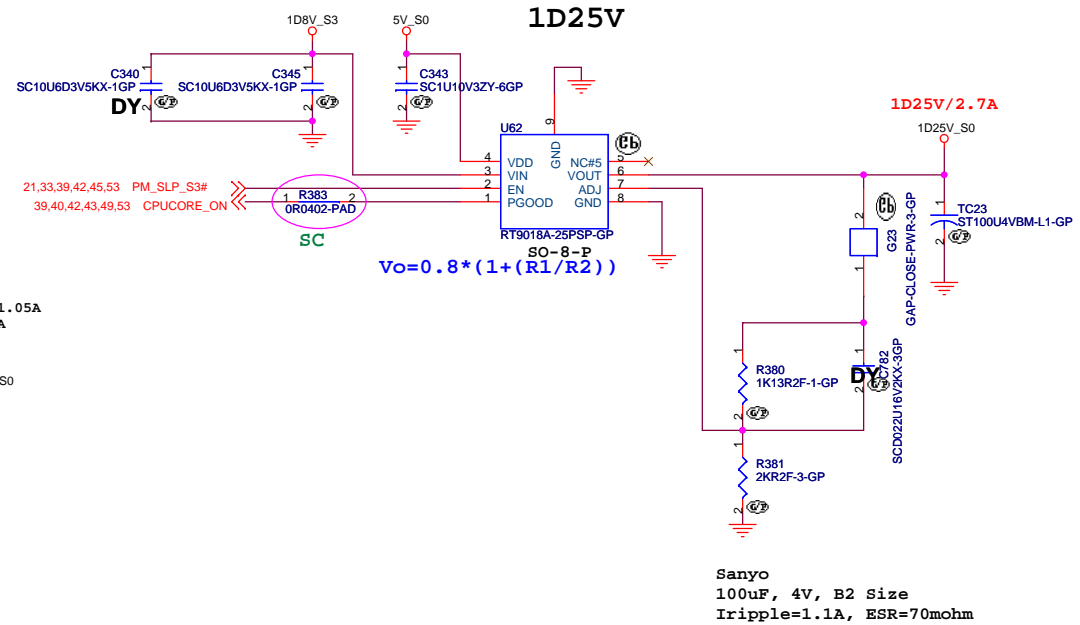
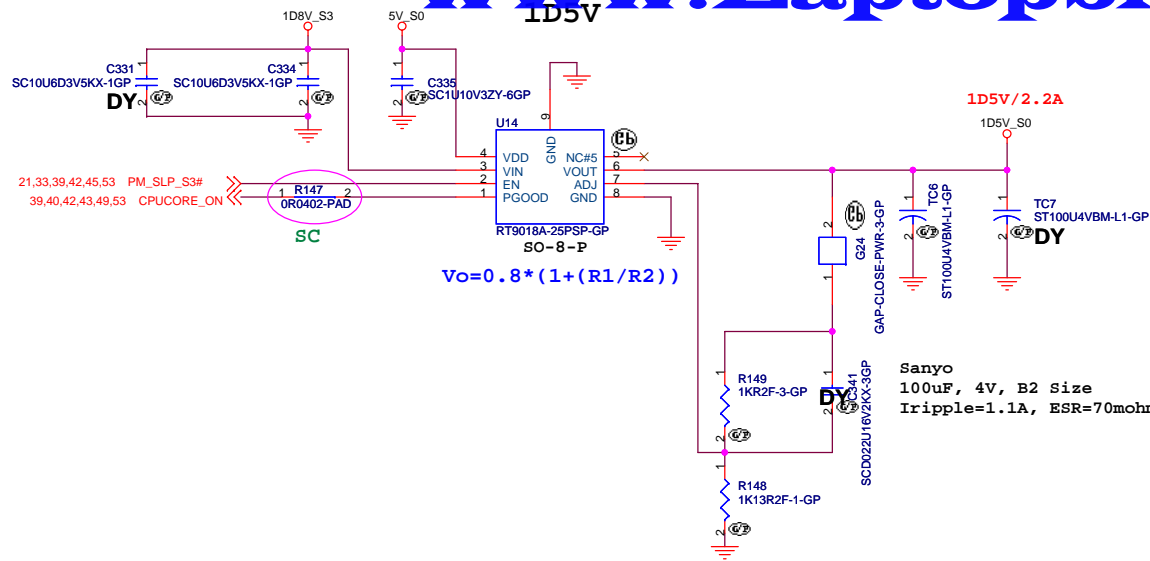


Title			
DCDC 1.05V			
Size A3	Document Number		Rev -1
Hawke-Intel			
Date:	Sunday, September 09, 2007	Sheet	42 of 57

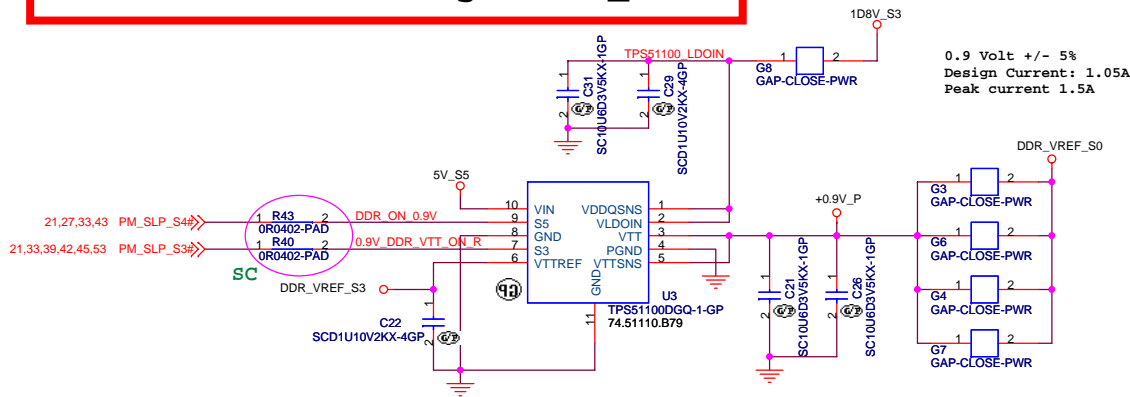


$$V_{out} = 0.75V * (R1 + R2) / R2$$

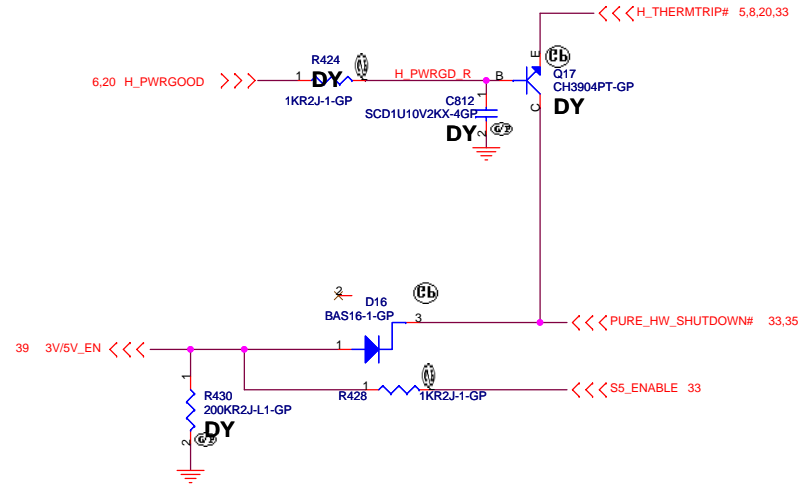
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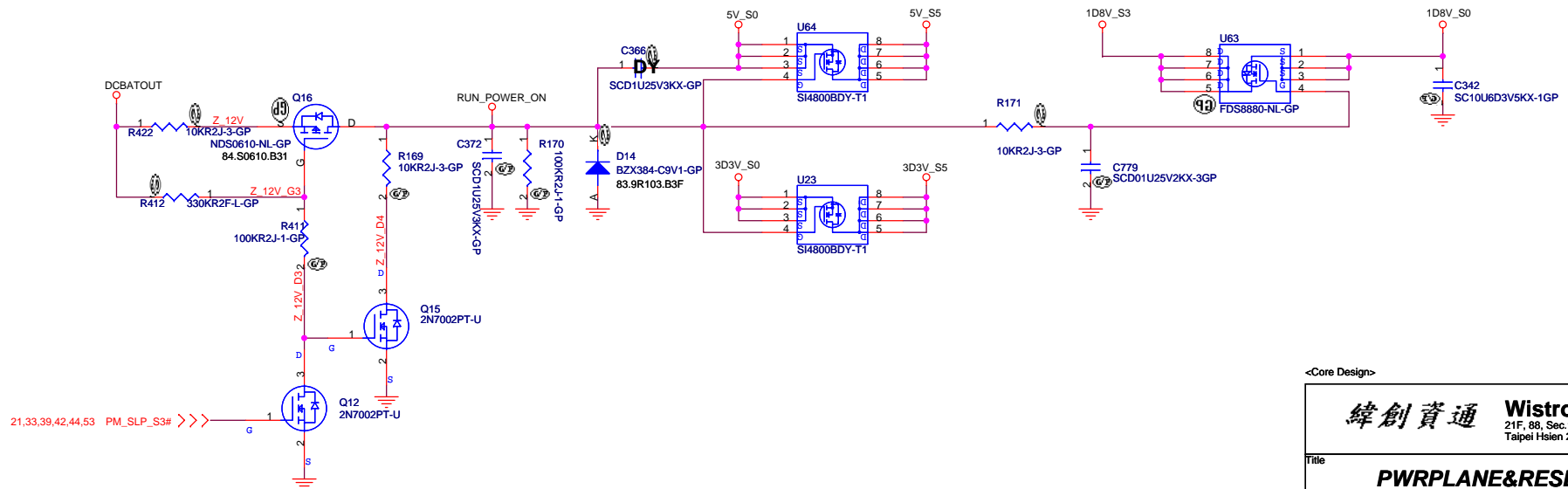
SSID = PWR.Plane.Regulator_0.9V



<Core Design>



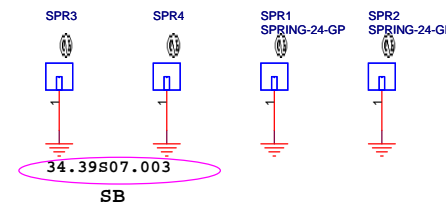
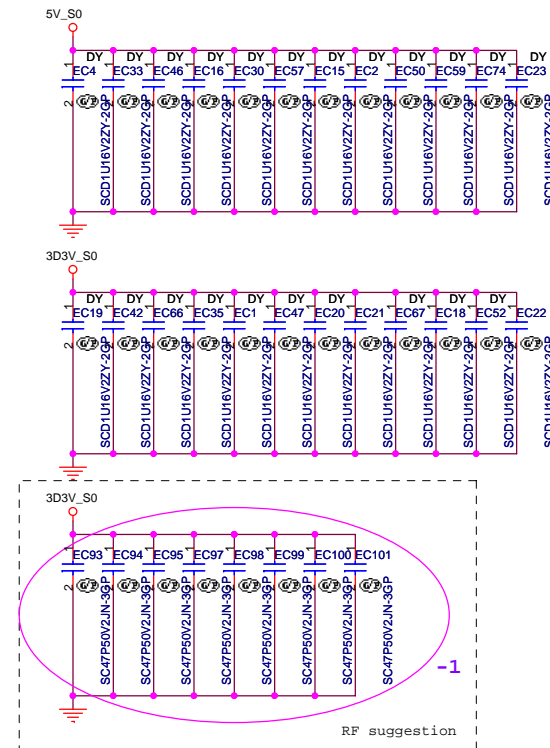
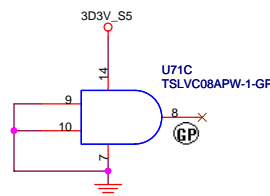
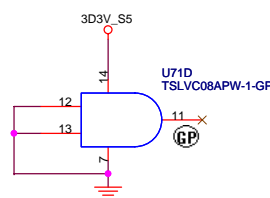
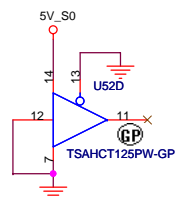
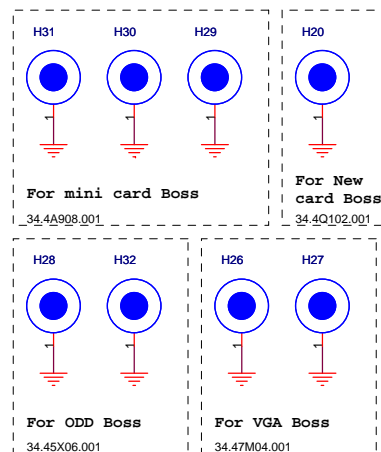
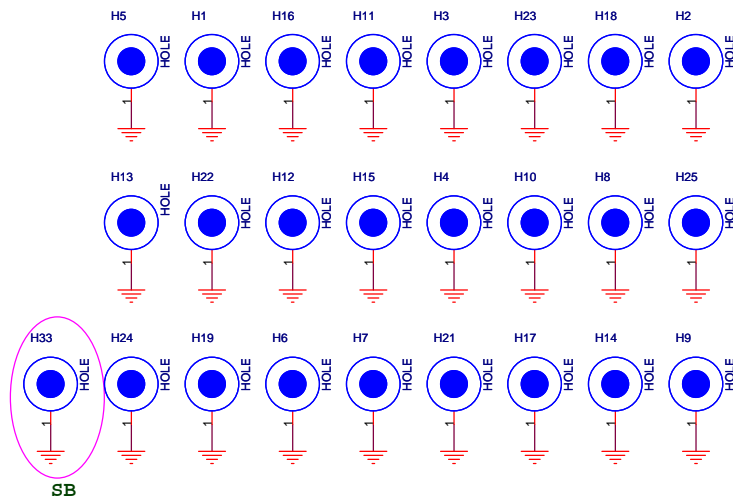
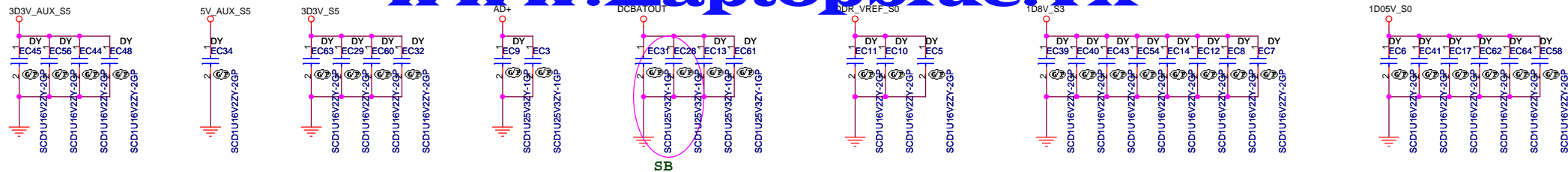
Run Power



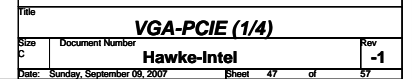
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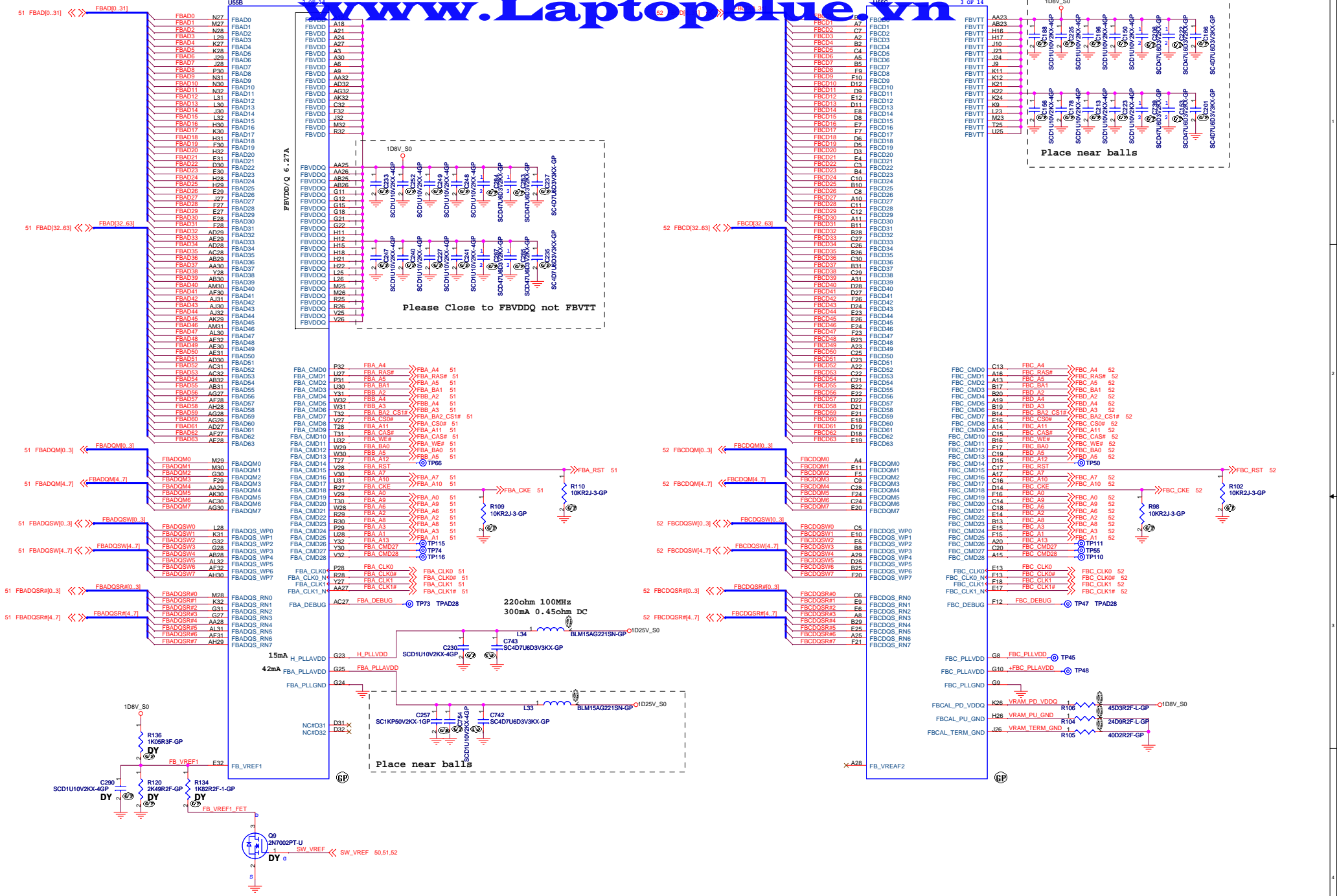
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

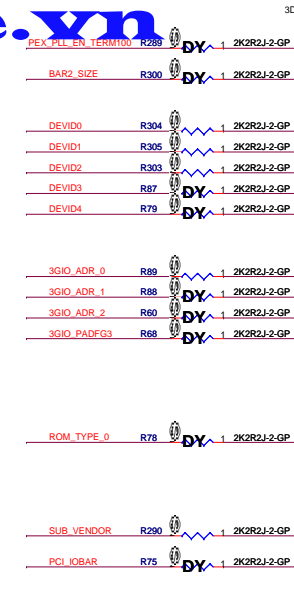
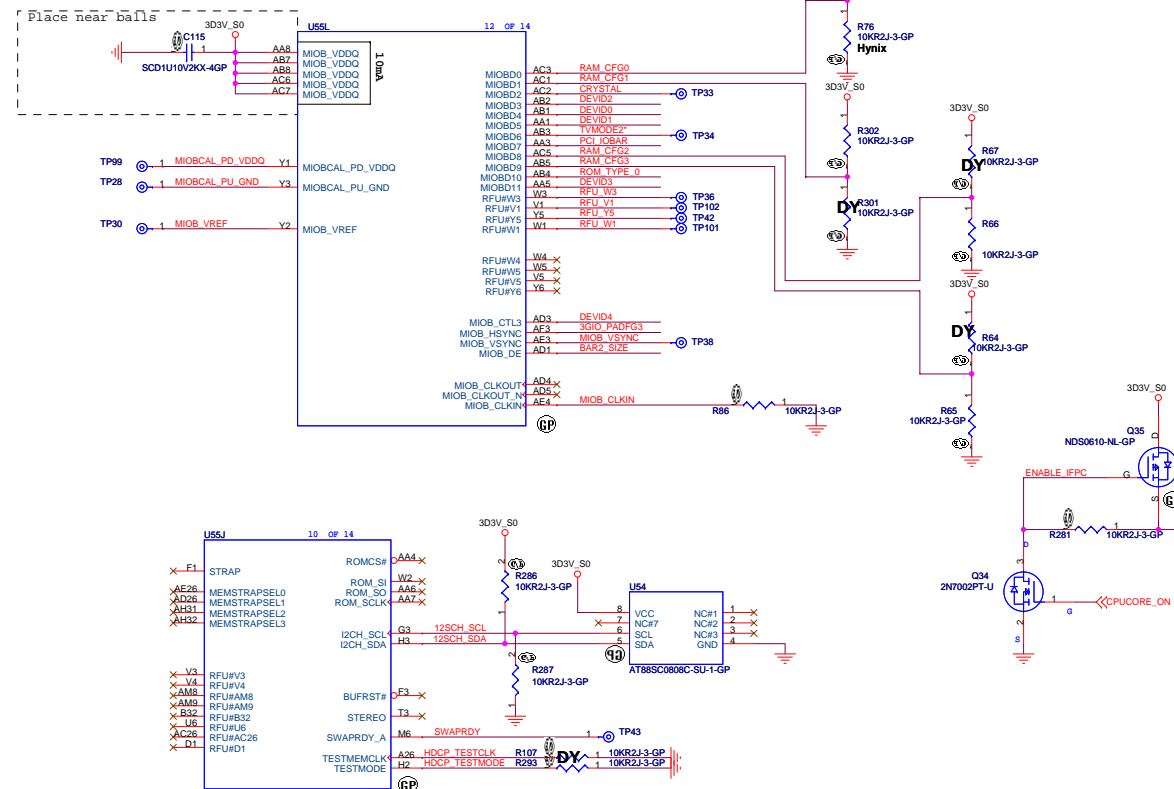
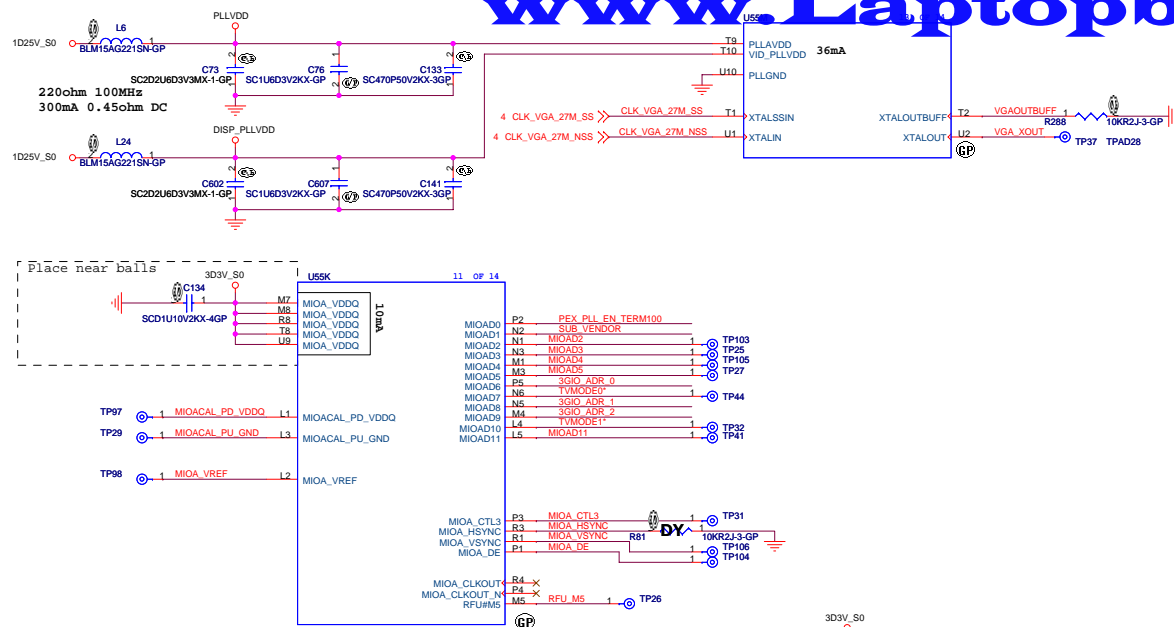
Title		PWRPLANE&RESETLOGIC	
Size	Document Number	Rev	
A3		-1	
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<Core Design>







PEX_PLL_EN_TERM		BAR2_SIZE	
0	Enable	0	32 Mb
1	Disable	1	16 Mb

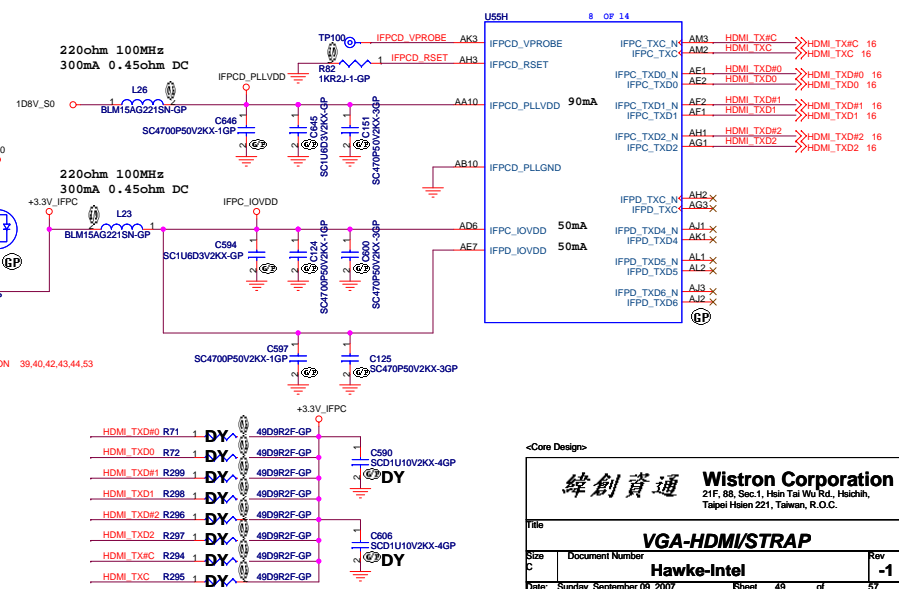
DEVICE	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	1	0	0
G72M	1	1	0	0	0
G72MV	1	0	1	1	1
G86-GS	0	0	1	1	1
G84-GS					

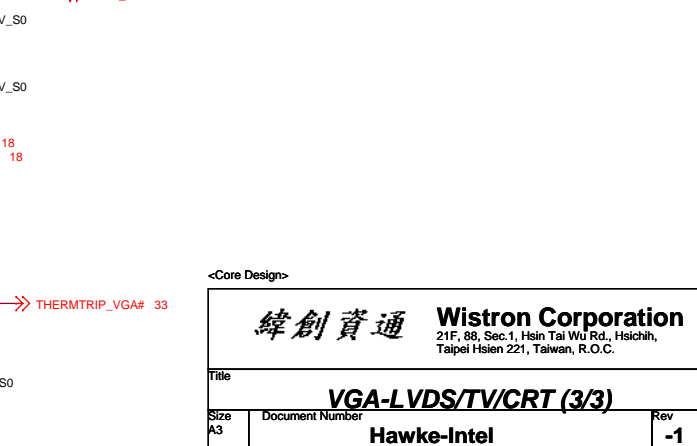
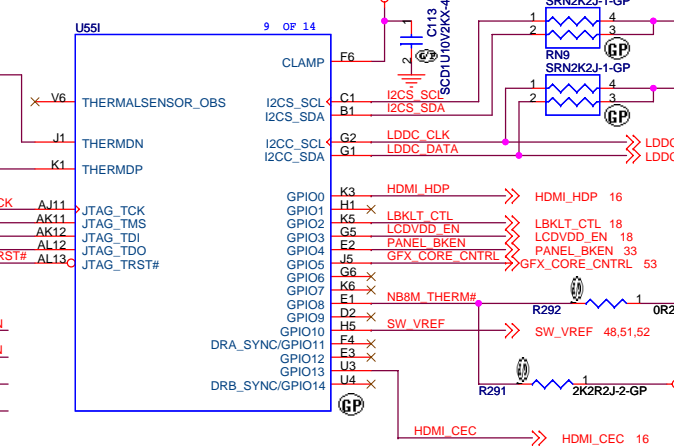
3GIO_PADCFG[3:0]	Notes
0000	Desktop (Default)
0001	Mobile1 Recommended for NV43/NV44/G/x
0010	Mobile2 NV42
0011	Mobile3
0100	Reserved
0101...1110	Reserved
1111	Reserved

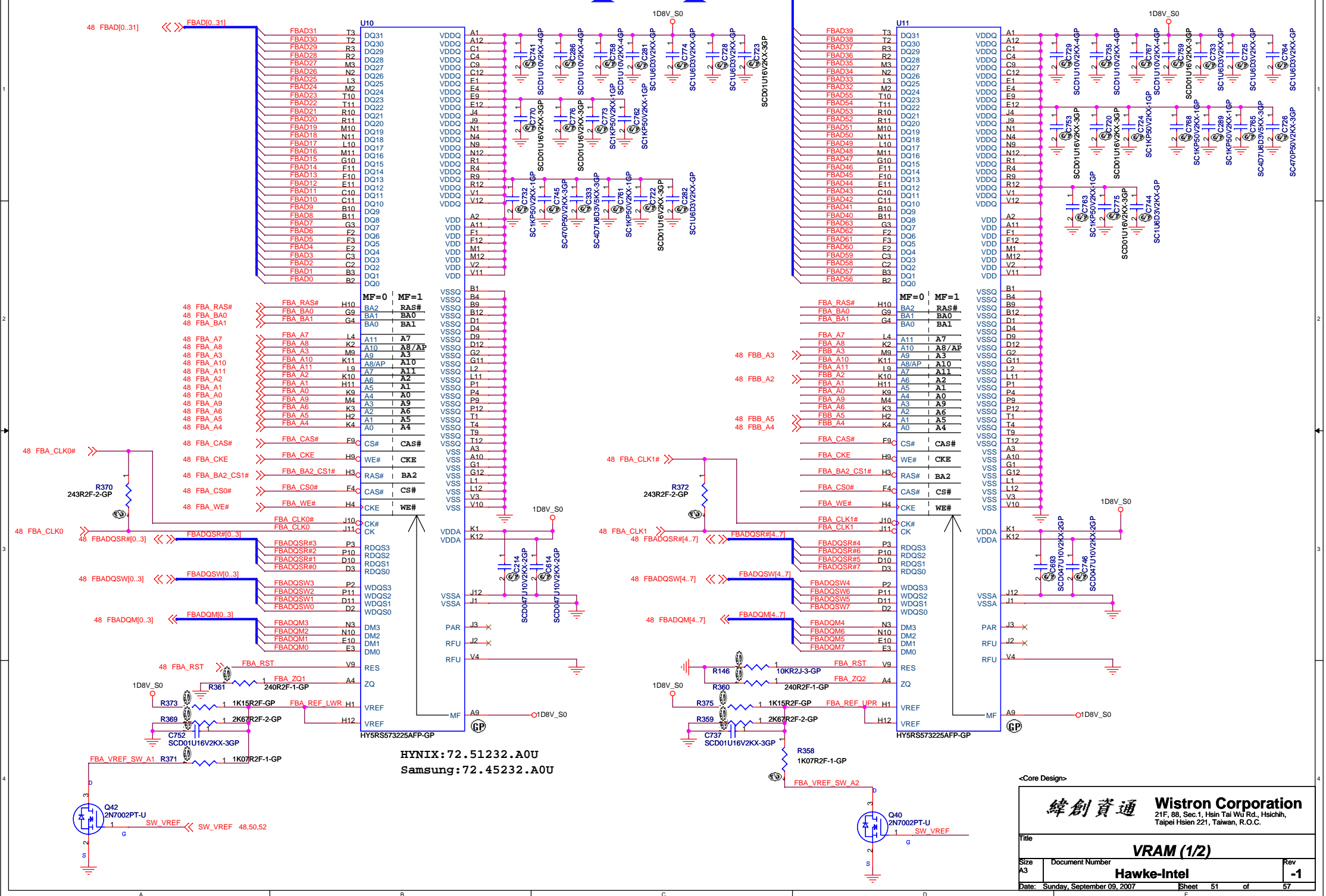
ROMTYPE[1:0]	
00	Parallel
01	Serial
10	Reserved
11	LPC

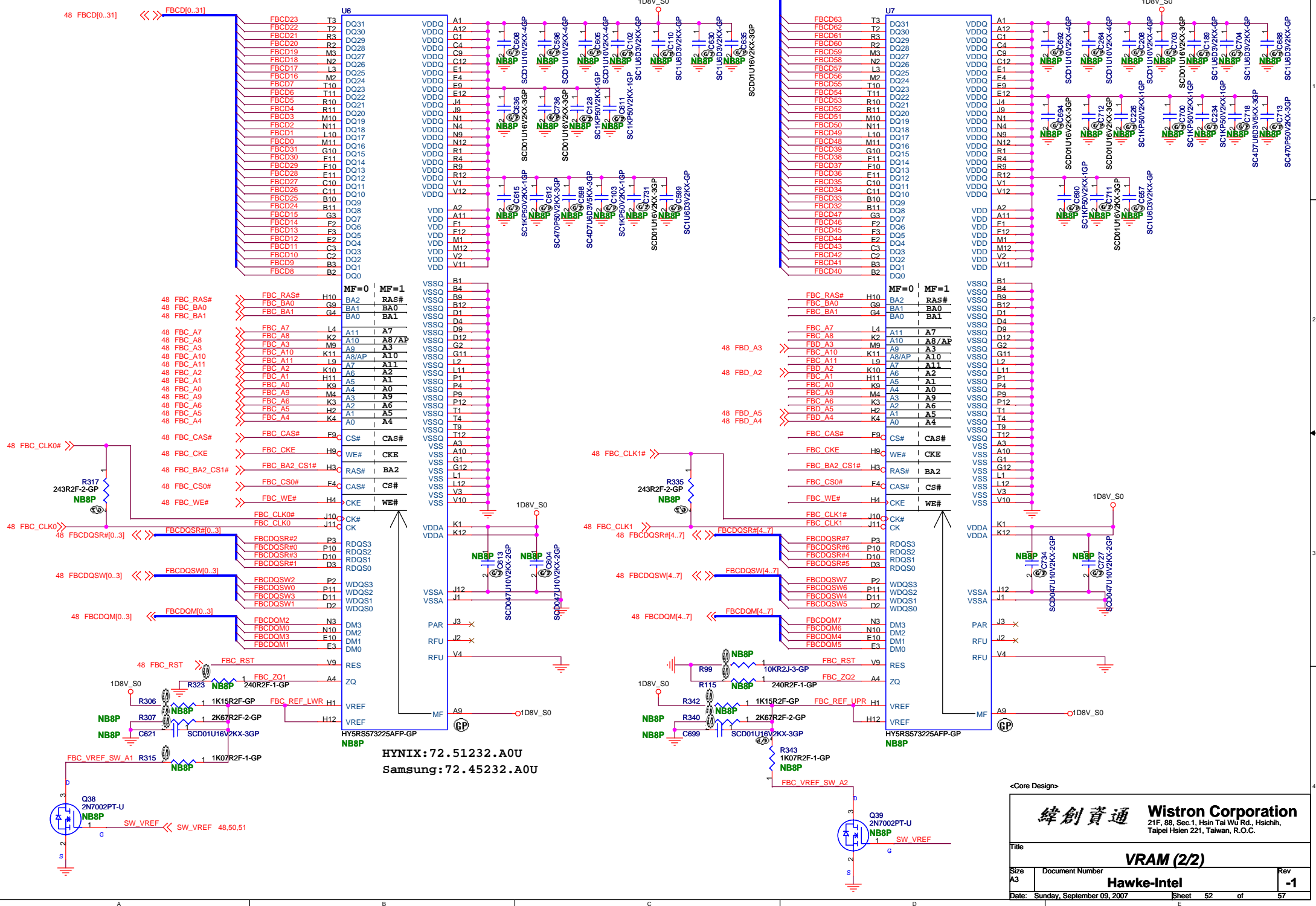
SUB_VENDOR		PCI_IOBAR	
0	No vedio BIOS ROM	0	Disabled
1	BIOS ROM is present	1	Enabled

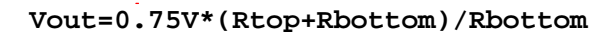
RAM_CFG[3:0]	MIOB0D MIOB1D MIOB8D MIOB9D	Infincon 8MX32	0101
		DDR3 1.8V	
		Hynix 8MX32	0111
		DDR3 1.8V	
		Samsung 8MX32	0110
		DDR3 1.8V	
		Infincon 16MX32	0001
		DDR3 1.8V	
		Hynix 16MX32	0010
		DDR3 1.8V	
		Samsung 16MX32	0011
		DDR3 1.8V	









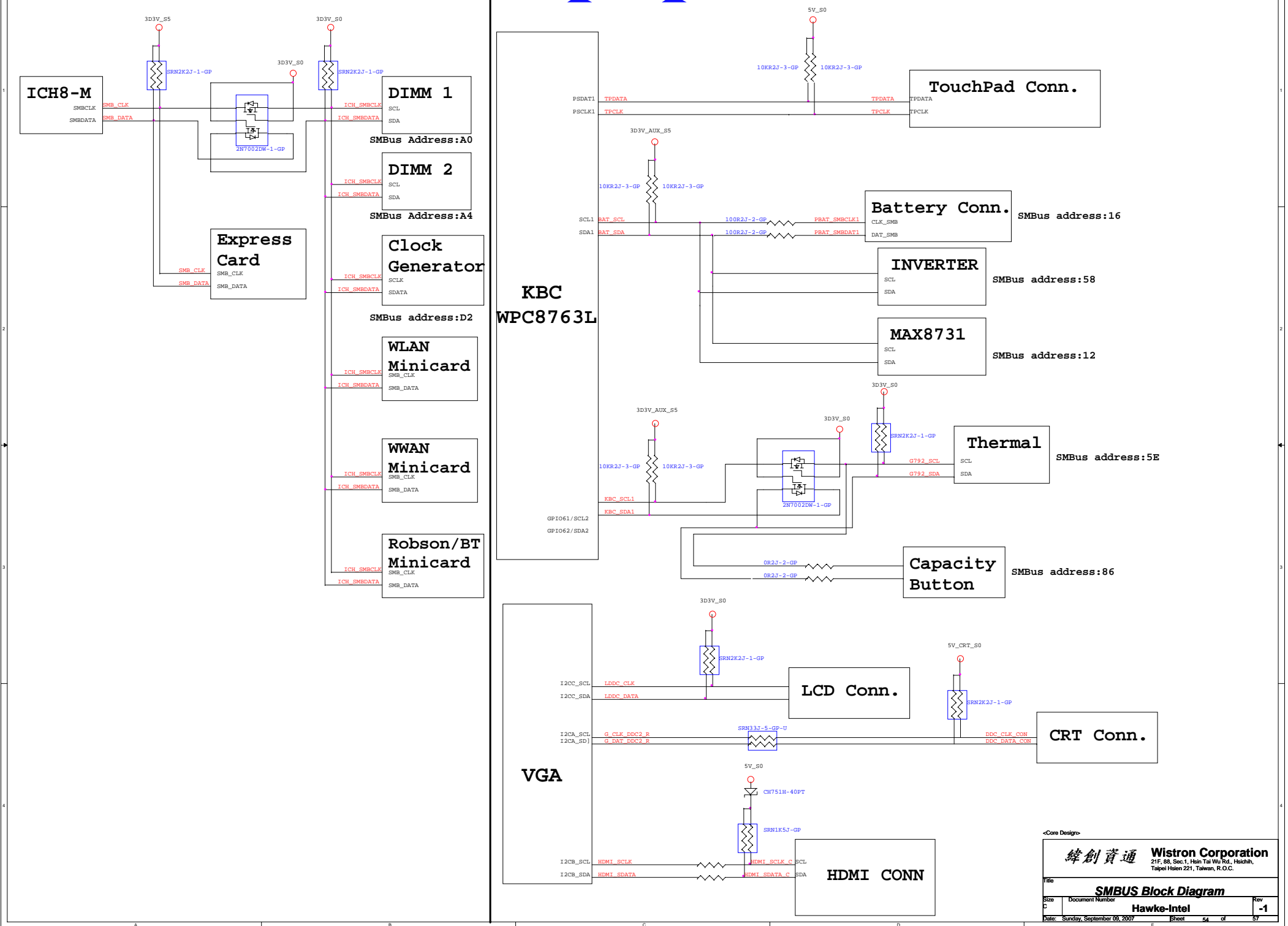


	R1	R2	R3	R4	Vout(V)
GFX_CORE_CNTRL NA	DY	DY	DY	18.7K	1.15V
GFX_CORE_CNTRL Low	8.45K	10K	40.2K to FET	DY	1.15V
GFX_CORE_CNTRL High	8.45K	10K	40.2K to GND	DY	1.2V

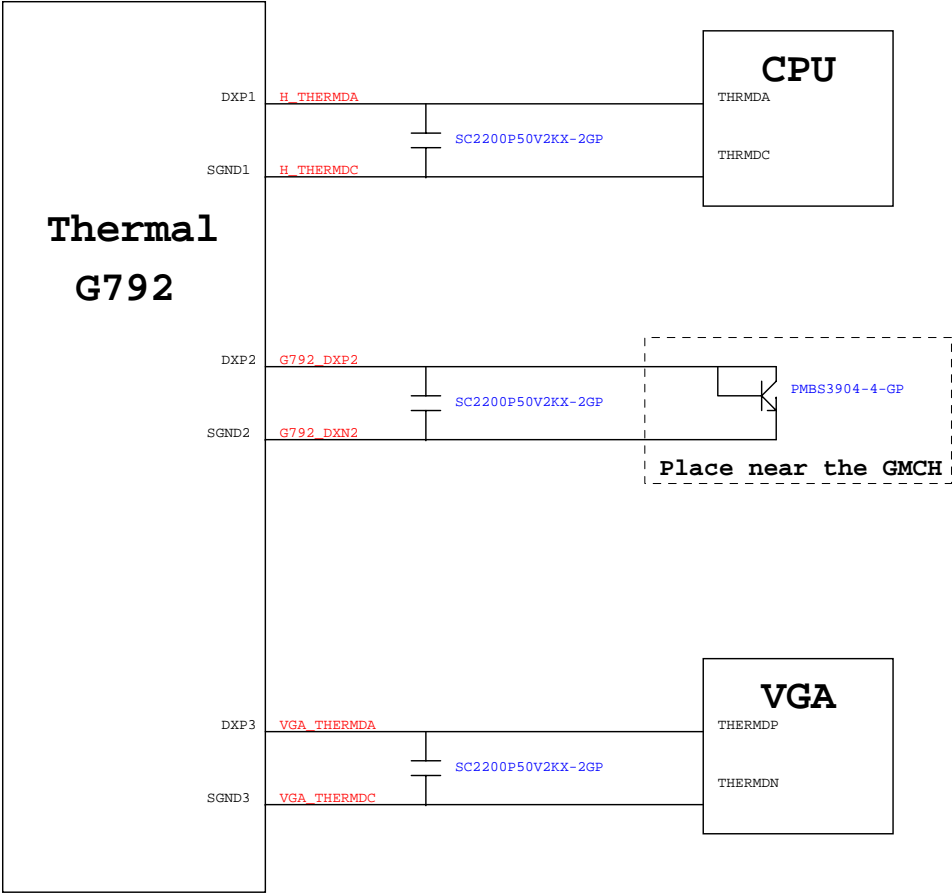
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DCDC VGA Core			
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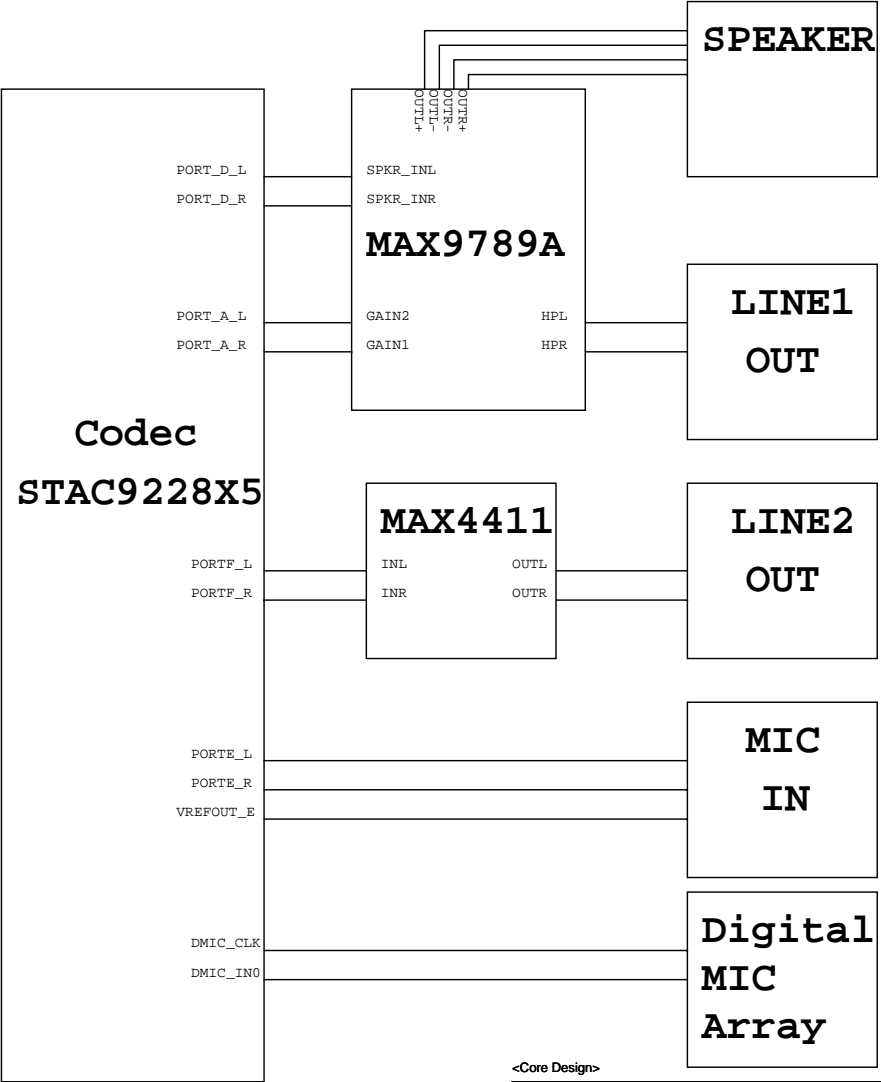
ICH8 SMBus Block Diagram Laptop SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/06	X00 to X01	1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
		15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY from X00 to X01

Size A3

Document Number

Hawke-Intel

Rev -1

Date: Sunday, September 09, 2007

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<Core Design>

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/08/17	X01 to X02	1	4	Changed U22 from ICS 9LPRS365BKLF to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLF to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB signal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconncted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconncted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
		14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE