

PWA : P835D  
PWB : R983D  
SCH : M854D

# RM2 Paltrow Intel Discrete Block Diagram

VER : 3A

## POWER

AC/BATT CONNECTOR	PG 54
BATT CHARGER	PG 47

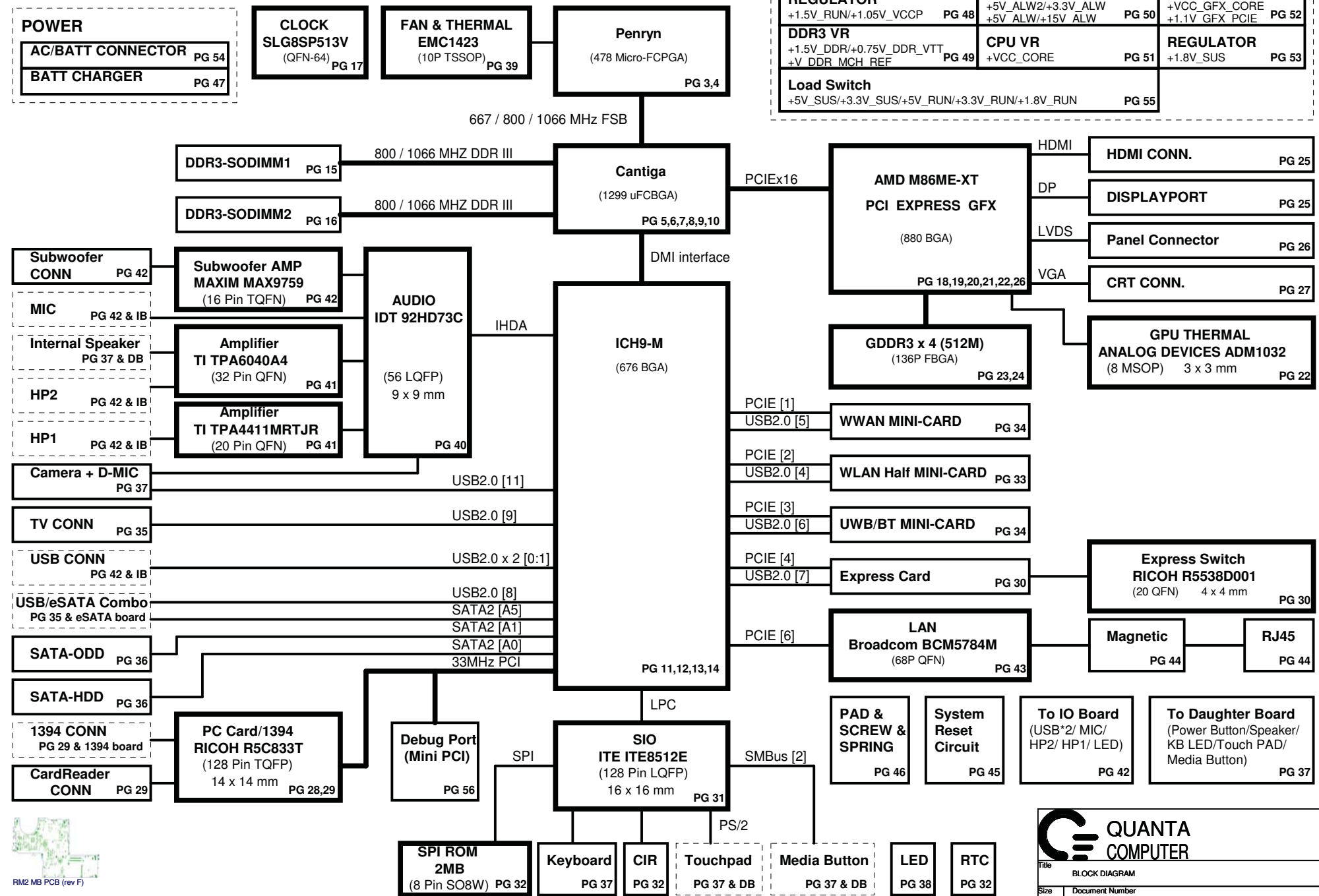
CLOCK SLG8SP513V (QFN-64)	PG 17
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FAN & THERMAL EMC1423 (10P TSSOP)	PG 39
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Penryn (478 Micro-FCPGA)	PG 3,4
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## SYSTEM POWER

REGULATOR +1.5V_RUN/+1.05V_VCCP	PG 48	SYS VR +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW	PG 50	VGA Core +VCC_GFX_CORE +1.1V_GFX_PCIE	PG 52
DDR3 VR +1.5V_DDR/+0.75V_DDR_VTT +V_DDR_MCH_REF	PG 49	CPU VR +VCC_CORE	PG 51	REGULATOR +1.8V_SUS	PG 53
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/+3.3V_RUN/+1.8V_RUN		PG 55			



Title: BLOCK DIAGRAM

Size: Document Number: RM2 Rev: 3A

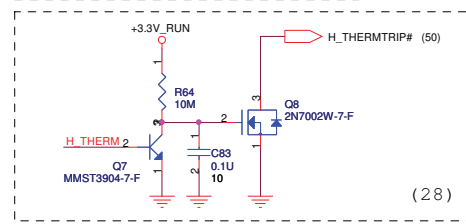
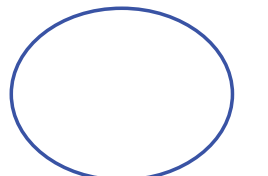
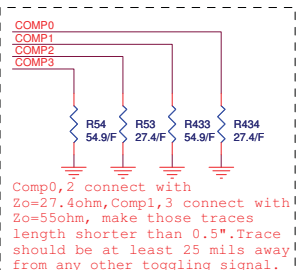
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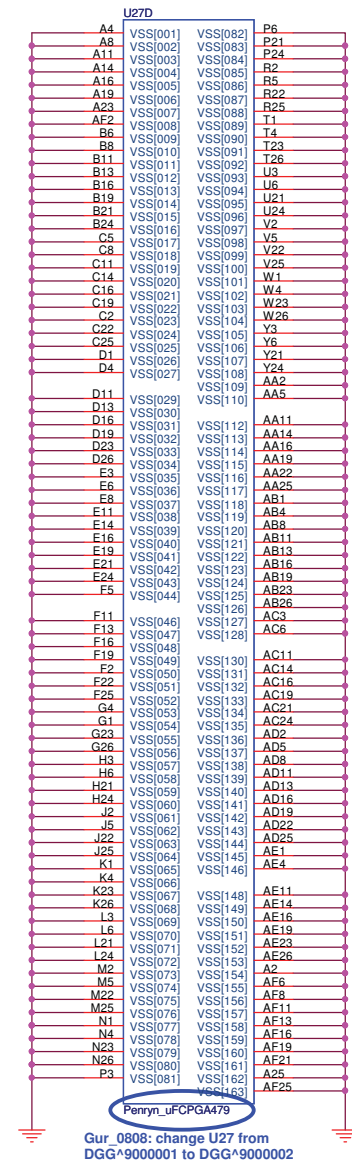
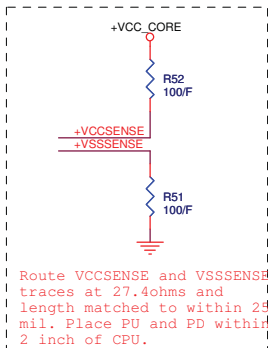
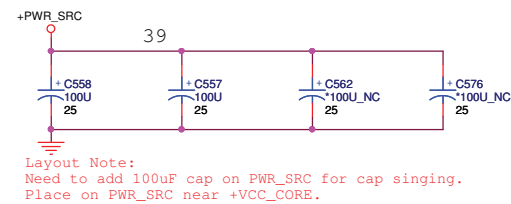
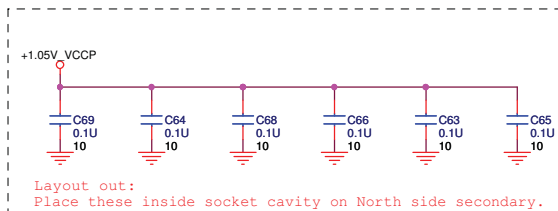
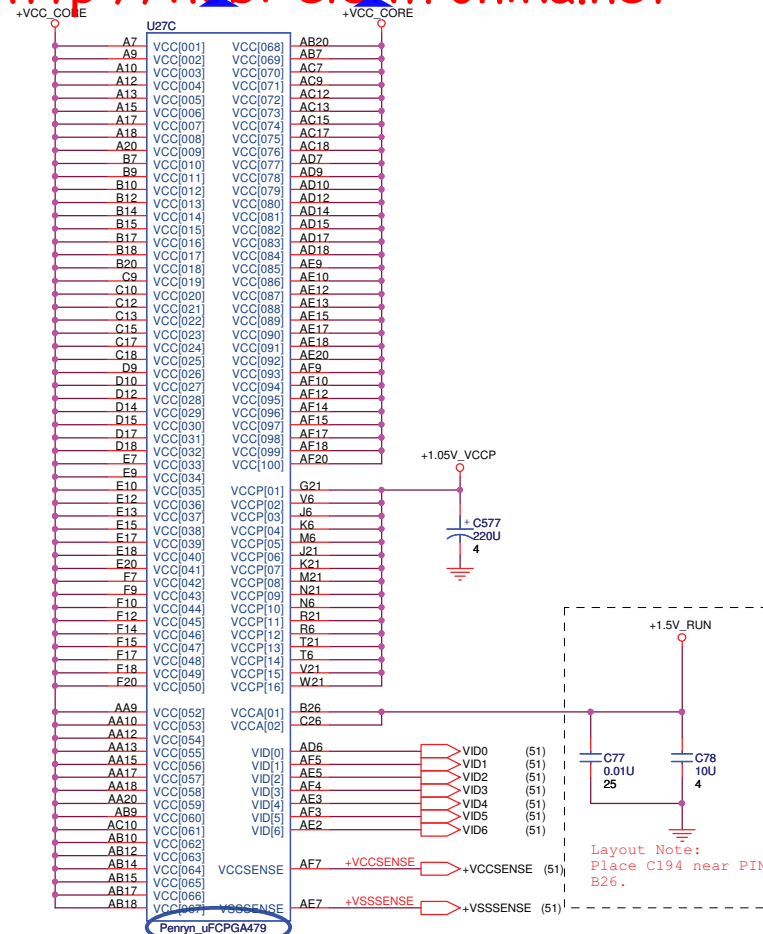
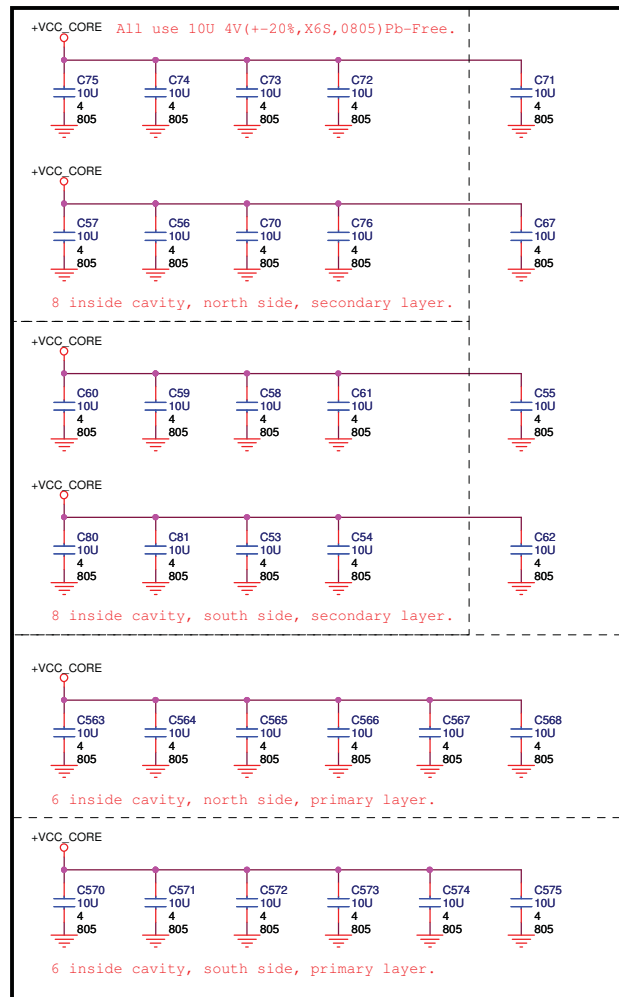
PAGE	DESCRIPTION
1	Block Diagram
2	Front Page
3-4	CPU (Penryn)
5-10	NB (Cantiga)
11-14	SB (ICH9-M)
15-16	DDR3 SO-DIMM(204P)
17	Clock Generator
18-24	GPU (M86XT)
25	HDMI & DP
26	LCD connector
27	CRT
28	Card reader PCI interface
29	Card reader & 1394 CONN
30	Express card
31	SIO (IT8512)
32	Flash/RTC/CIR
33	WLAN
34	WWAN/WPAN
35	USB & eSATA & TV
36	SATA HDD & ODD
37	KB/CCD/UI
38	LED
39	FAN/Thermal
40-42	Audio/CONN/Subwoofer (92HD73C).
43-44	LAN/RJ45 (BCM5784M)
45	System Reset Circuit
46	PAD & SCREW & SPRING
47	CHARGER (MAX8731A)
48	1.05VCCP & 1.5VRUN
49	1.5_DDR/0.75(TPS51116)
50	3.3V/5V/15V (MAX17020)
51	CPU_POWER (ISL6262A) - 2 phase
52	VGA_M86 (MAX8632)
53	1.8V_SUS (TPS51117)
54	DCIN & Batt
55	Load Switch
56	Debug Port (Mini PCI)
57	SMBUS BLOCK
58	Power statu
59	Power Block Diagram

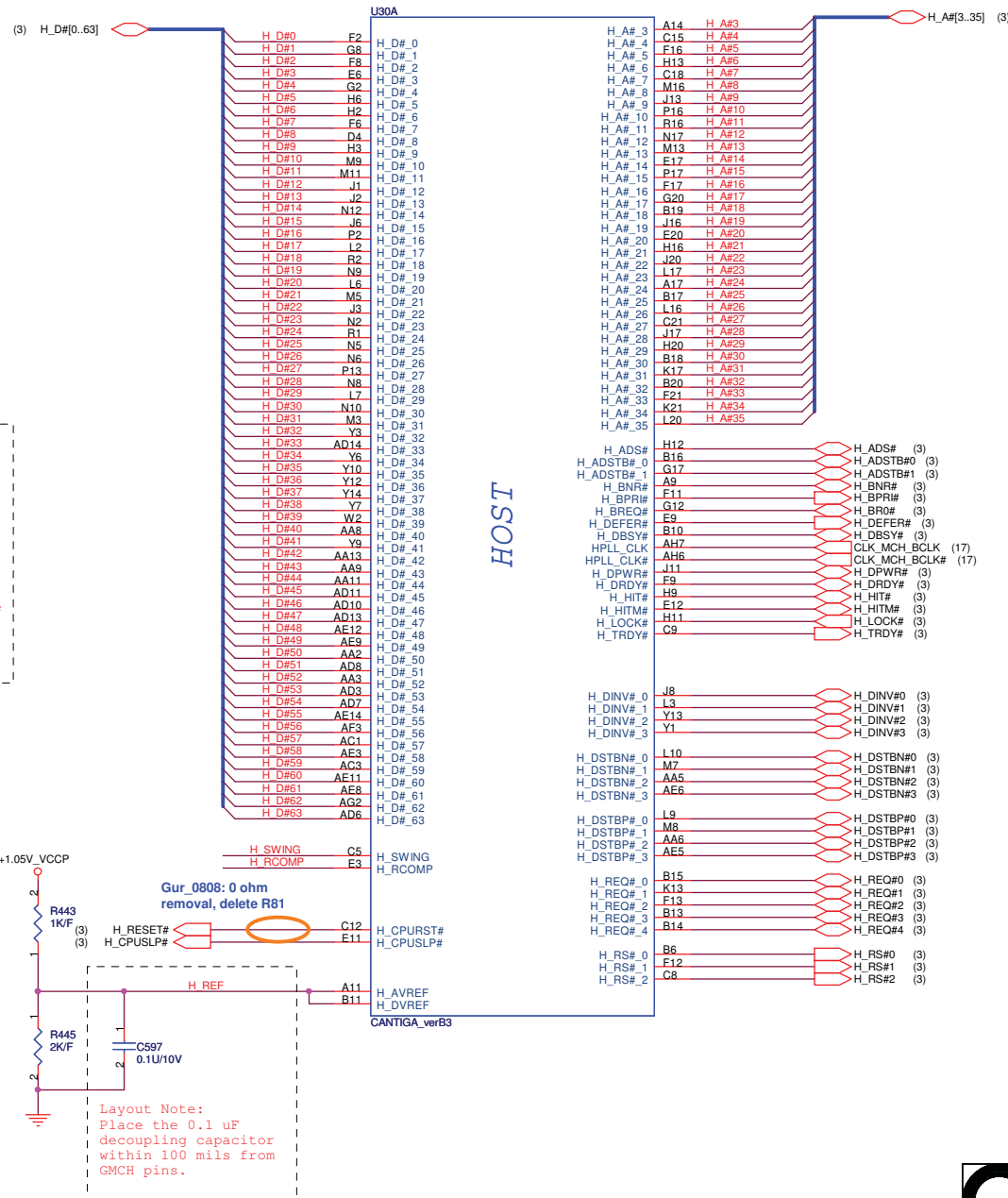
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

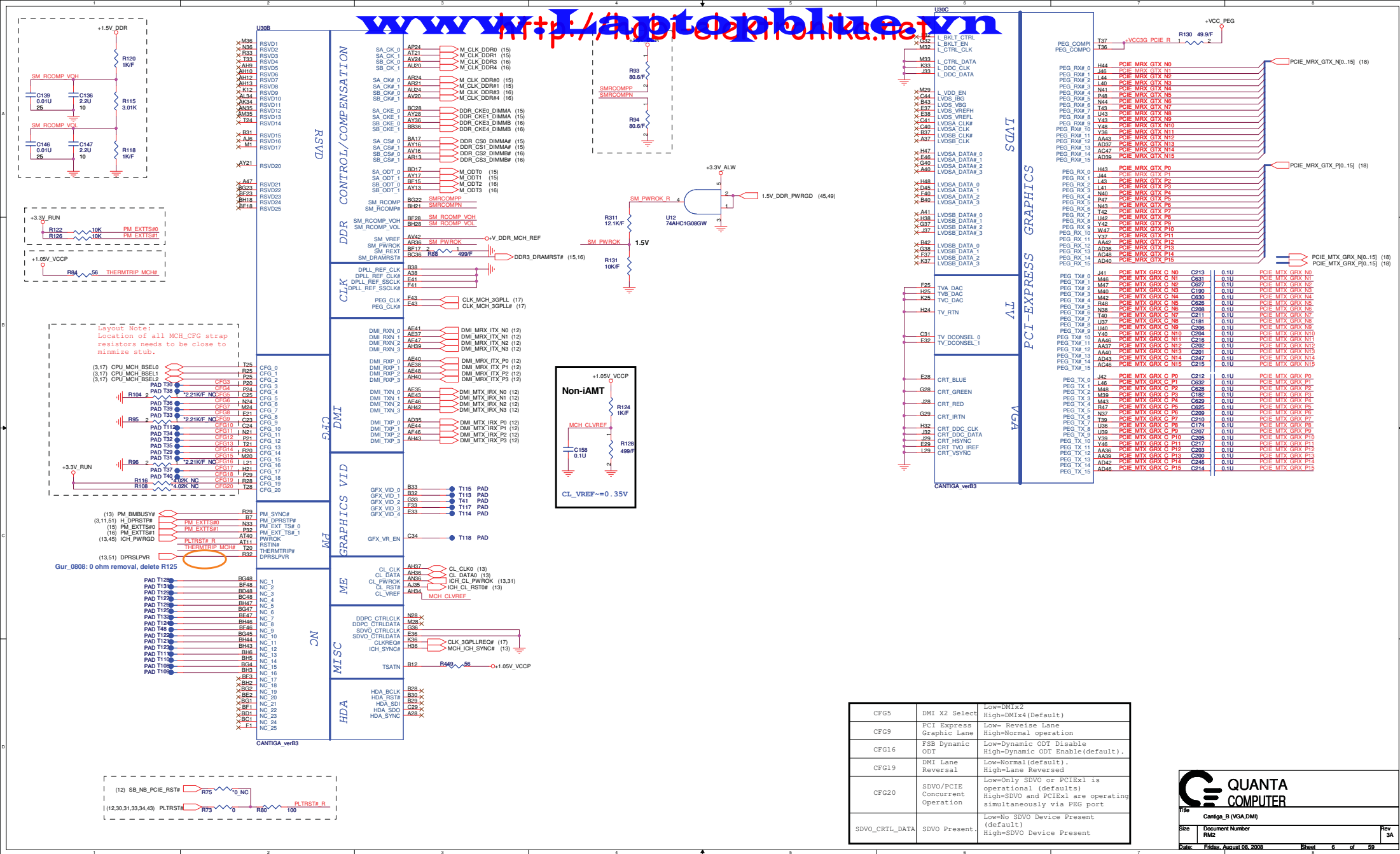


FSB	BCLK	BSEL2	BSEL1	BSEL0
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0









(15) DDR\_A\_D[0..63]



DDR SYSTEM MEMORY A

SA\_BS\_0  
SA\_BS\_1  
SA\_BS\_2  
SA\_RAS#  
SA\_CAS#  
SA\_WE#

SA\_DM\_0  
SA\_DM\_1  
SA\_DM\_2  
SA\_DM\_3  
SA\_DM\_4  
SA\_DM\_5  
SA\_DM\_6  
SA\_DM\_7

SA\_DQS\_0  
SA\_DQS\_1  
SA\_DQS\_2  
SA\_DQS\_3  
SA\_DQS\_4  
SA\_DQS\_5  
SA\_DQS\_6  
SA\_DQS\_7  
SA\_DQS#\_0  
SA\_DQS#\_1  
SA\_DQS#\_2  
SA\_DQS#\_3  
SA\_DQS#\_4  
SA\_DQS#\_5  
SA\_DQS#\_6  
SA\_DQS#\_7

SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

BD21 DDR A BS0  
BG18 DDR A BS1  
AT25 DDR A BS2  
BB20 DDR A RAS#  
BD20 DDR A CAS#  
AY20 DDR A WE#

AM37 DDR A DM0  
AT41 DDR A DM1  
AY41 DDR A DM2  
AU39 DDR A DM3  
BB12 DDR A DM4  
AY6 DDR A DM5  
AT7 DDR A DM6  
AJ5 DDR A DM7

AJ44 DDR A DQS0  
AT44 DDR A DQS1  
BA43 DDR A DQS2  
BC37 DDR A DQS3  
AW12 DDR A DQS4  
BC8 DDR A DQS5  
AU8 DDR A DQS6  
AM7 DDR A DQS7

AJ43 DDR A DQS#0  
AT43 DDR A DQS#1  
BA44 DDR A DQS#2  
BD37 DDR A DQS#3  
AY12 DDR A DQS#4  
BD8 DDR A DQS#5  
AU9 DDR A DQS#6  
AM8 DDR A DQS#7

BA21 DDR A MA0  
BC24 DDR A MA1  
BG24 DDR A MA2  
BH24 DDR A MA3  
BG25 DDR A MA4  
BA24 DDR A MA5  
BD24 DDR A MA6  
BG27 DDR A MA7  
BF25 DDR A MA8  
AW24 DDR A MA9  
BC21 DDR A MA10  
BG26 DDR A MA11  
BH26 DDR A MA12  
BH17 DDR A MA13  
AY25 DDR A MA14

(16) DDR\_B\_D[0..63]



DDR SYSTEM MEMORY B

SB\_BS\_0  
SB\_BS\_1  
SB\_BS\_2  
SB\_RAS#  
SB\_CAS#  
SB\_WE#

SB\_DM\_0  
SB\_DM\_1  
SB\_DM\_2  
SB\_DM\_3  
SB\_DM\_4  
SB\_DM\_5  
SB\_DM\_6  
SB\_DM\_7

SB\_DQS\_0  
SB\_DQS\_1  
SB\_DQS\_2  
SB\_DQS\_3  
SB\_DQS\_4  
SB\_DQS\_5  
SB\_DQS\_6  
SB\_DQS\_7  
SB\_DQS#\_0  
SB\_DQS#\_1  
SB\_DQS#\_2  
SB\_DQS#\_3  
SB\_DQS#\_4  
SB\_DQS#\_5  
SB\_DQS#\_6  
SB\_DQS#\_7

SB\_MA\_0  
SB\_MA\_1  
SB\_MA\_2  
SB\_MA\_3  
SB\_MA\_4  
SB\_MA\_5  
SB\_MA\_6  
SB\_MA\_7  
SB\_MA\_8  
SB\_MA\_9  
SB\_MA\_10  
SB\_MA\_11  
SB\_MA\_12  
SB\_MA\_13  
SB\_MA\_14

BC16 DDR B BS0  
BB17 DDR B BS1  
BB33 DDR B BS2

AU17 DDR B RAS#  
BG16 DDR B CAS#  
BF14 DDR B WE#

AM47 DDR B DM0  
AY47 DDR B DM1  
BD40 DDR B DM2  
BF35 DDR B DM3  
BG11 DDR B DM4  
BA3 DDR B DM5  
AP1 DDR B DM6  
AK2 DDR B DM7

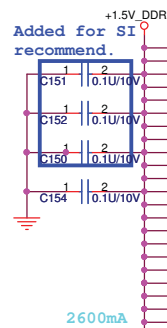
AL47 DDR B DQS0  
AV48 DDR B DQS1  
BG41 DDR B DQS2  
BG37 DDR B DQS3  
BH9 DDR B DQS4  
BB2 DDR B DQS5  
AU1 DDR B DQS6  
AN6 DDR B DQS7

AL46 DDR B DQS#0  
AV47 DDR B DQS#1  
BH41 DDR B DQS#2  
BH37 DDR B DQS#3  
BG9 DDR B DQS#4  
BC2 DDR B DQS#5  
AT2 DDR B DQS#6  
AN5 DDR B DQS#7

AV17 DDR B MA0  
BA25 DDR B MA1  
BC25 DDR B MA2  
AU25 DDR B MA3  
AW25 DDR B MA4  
BB28 DDR B MA5  
AU28 DDR B MA6  
AW28 DDR B MA7  
AT33 DDR B MA8  
BD33 DDR B MA9  
BB16 DDR B MA10  
AW33 DDR B MA11  
AY33 DDR B MA12  
BH15 DDR B MA13  
AU33 DDR B MA14

CANTIGA\_verB3

CANTIGA\_verB3



U30G

VCC\_SM\_1  
VCC\_SM\_2  
VCC\_SM\_3  
VCC\_SM\_4  
VCC\_SM\_5  
VCC\_SM\_6  
VCC\_SM\_7  
VCC\_SM\_8  
VCC\_SM\_9  
VCC\_SM\_10  
VCC\_SM\_11  
VCC\_SM\_12  
VCC\_SM\_13  
VCC\_SM\_14  
VCC\_SM\_15  
VCC\_SM\_16  
VCC\_SM\_17  
VCC\_SM\_18  
VCC\_SM\_19  
VCC\_SM\_20  
VCC\_SM\_21  
VCC\_SM\_22  
VCC\_SM\_23  
VCC\_SM\_24  
VCC\_SM\_25  
VCC\_SM\_26  
VCC\_SM\_27  
VCC\_SM\_28  
VCC\_SM\_29  
VCC\_SM\_30  
VCC\_SM\_31  
VCC\_SM\_32  
VCC\_SM\_33  
VCC\_SM\_34  
VCC\_SM\_35  
VCC\_SM\_36/NC  
VCC\_SM\_37/NC  
VCC\_SM\_38/NC  
VCC\_SM\_39/NC  
VCC\_SM\_40/NC  
VCC\_SM\_41/NC  
VCC\_SM\_42/NC

VCC SM

POWER

Y26  
AE25  
AB25  
AA25  
AE24  
AC24  
AA24  
Y24  
AE23  
AC23  
AB23  
AA23  
AJ21  
AG21  
AE21  
AC21  
AA21  
Y21  
AH20  
AF20  
AE20  
AC20  
AB20  
AA20  
TI17  
TI16  
AM15  
AL15  
AE15  
AJ15  
AH15  
AG15  
AF15  
AB15  
AA15  
Y15  
V15  
U15  
AM14  
U14  
TI14

VCC GFX

AI14  
AH14

CANTIGA\_verB3

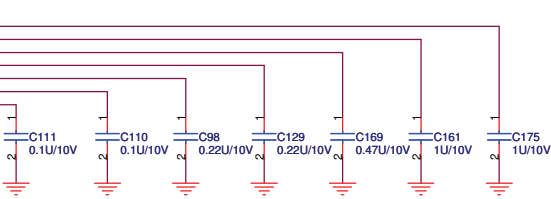
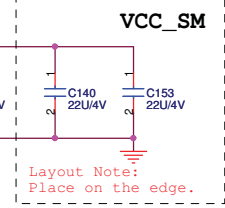
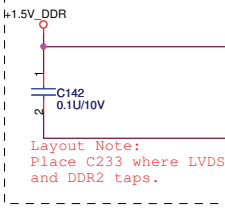
VCC\_AXG\_NCTF\_1  
VCC\_AXG\_NCTF\_2  
VCC\_AXG\_NCTF\_3  
VCC\_AXG\_NCTF\_4  
VCC\_AXG\_NCTF\_5  
VCC\_AXG\_NCTF\_6  
VCC\_AXG\_NCTF\_7  
VCC\_AXG\_NCTF\_8  
VCC\_AXG\_NCTF\_9  
VCC\_AXG\_NCTF\_10  
VCC\_AXG\_NCTF\_11  
VCC\_AXG\_NCTF\_12  
VCC\_AXG\_NCTF\_13  
VCC\_AXG\_NCTF\_14  
VCC\_AXG\_NCTF\_15  
VCC\_AXG\_NCTF\_16  
VCC\_AXG\_NCTF\_17  
VCC\_AXG\_NCTF\_18  
VCC\_AXG\_NCTF\_19  
VCC\_AXG\_NCTF\_20  
VCC\_AXG\_NCTF\_21  
VCC\_AXG\_NCTF\_22  
VCC\_AXG\_NCTF\_23  
VCC\_AXG\_NCTF\_24  
VCC\_AXG\_NCTF\_25  
VCC\_AXG\_NCTF\_26  
VCC\_AXG\_NCTF\_27  
VCC\_AXG\_NCTF\_28  
VCC\_AXG\_NCTF\_29  
VCC\_AXG\_NCTF\_30  
VCC\_AXG\_NCTF\_31  
VCC\_AXG\_NCTF\_32  
VCC\_AXG\_NCTF\_33  
VCC\_AXG\_NCTF\_34  
VCC\_AXG\_NCTF\_35  
VCC\_AXG\_NCTF\_36  
VCC\_AXG\_NCTF\_37  
VCC\_AXG\_NCTF\_38  
VCC\_AXG\_NCTF\_39  
VCC\_AXG\_NCTF\_40  
VCC\_AXG\_NCTF\_41  
VCC\_AXG\_NCTF\_42  
VCC\_AXG\_NCTF\_43  
VCC\_AXG\_NCTF\_44  
VCC\_AXG\_NCTF\_45  
VCC\_AXG\_NCTF\_46  
VCC\_AXG\_NCTF\_47  
VCC\_AXG\_NCTF\_48  
VCC\_AXG\_NCTF\_49  
VCC\_AXG\_NCTF\_50  
VCC\_AXG\_NCTF\_51  
VCC\_AXG\_NCTF\_52  
VCC\_AXG\_NCTF\_53  
VCC\_AXG\_NCTF\_54  
VCC\_AXG\_NCTF\_55  
VCC\_AXG\_NCTF\_56  
VCC\_AXG\_NCTF\_57  
VCC\_AXG\_NCTF\_58  
VCC\_AXG\_NCTF\_59  
VCC\_AXG\_NCTF\_60

VCC GFX NCTF

VCC\_SM\_LF1  
VCC\_SM\_LF2  
VCC\_SM\_LF3  
VCC\_SM\_LF4  
VCC\_SM\_LF5  
VCC\_SM\_LF6  
VCC\_SM\_LF7

VCC SM LF

W28  
V28  
W26  
V26  
W25  
V25  
W24  
V24  
W23  
V23  
AM21  
AL21  
AK21  
W21  
V21  
U21  
AM20  
AL20  
AK20  
W20  
V20  
U20  
AM19  
AL19  
AK19  
W19  
V19  
U19  
AM17  
AL17  
AK17  
AH17  
AG17  
AF17  
AE17  
AC17  
AB17  
Y17  
W17  
V17  
AM16  
AL16  
AK16  
AJ16  
AH16  
AG16  
AF16  
AE16  
AC16  
AB16  
AA16  
Y16  
W16  
V16  
U16



+3.3V\_RUN

+1.05V\_VCCP

Layout Note:  
Inside GMCH cavity.

$$I_{vcc} = 1930.4 + 508.12 = 2438.52 \text{mA}$$

Layout Note:  
370 mils from edge.

U30F

AG34  
AC34  
AB34  
AA34  
Y34  
U34  
AM33  
Y33  
AK33  
AJ33  
AG33  
AF33  
AE33  
AC33  
Y33  
W33  
V33  
U33  
AH28  
AF28  
AC28  
AA28  
AJ26  
AG26  
AE26  
AC26  
AH25  
AG25  
AF25  
AG24  
AJ23  
AH23  
AE23  
T32

VCC CORE

POWER

VCC NCTF

VCC\_NCTF\_1  
VCC\_NCTF\_2  
VCC\_NCTF\_3  
VCC\_NCTF\_4  
VCC\_NCTF\_5  
VCC\_NCTF\_6  
VCC\_NCTF\_7  
VCC\_NCTF\_8  
VCC\_NCTF\_9  
VCC\_NCTF\_10  
VCC\_NCTF\_11  
VCC\_NCTF\_12  
VCC\_NCTF\_13  
VCC\_NCTF\_14  
VCC\_NCTF\_15  
VCC\_NCTF\_16  
VCC\_NCTF\_17  
VCC\_NCTF\_18  
VCC\_NCTF\_19  
VCC\_NCTF\_20  
VCC\_NCTF\_21  
VCC\_NCTF\_22  
VCC\_NCTF\_23  
VCC\_NCTF\_24  
VCC\_NCTF\_25  
VCC\_NCTF\_26  
VCC\_NCTF\_27  
VCC\_NCTF\_28  
VCC\_NCTF\_29  
VCC\_NCTF\_30  
VCC\_NCTF\_31  
VCC\_NCTF\_32  
VCC\_NCTF\_33  
VCC\_NCTF\_34  
VCC\_NCTF\_35  
VCC\_NCTF\_36  
VCC\_NCTF\_37  
VCC\_NCTF\_38  
VCC\_NCTF\_39  
VCC\_NCTF\_40  
VCC\_NCTF\_41  
VCC\_NCTF\_42  
VCC\_NCTF\_43  
VCC\_NCTF\_44

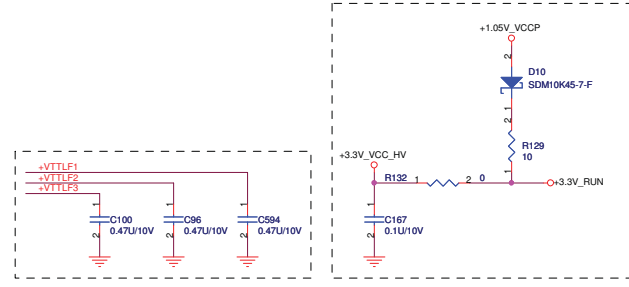
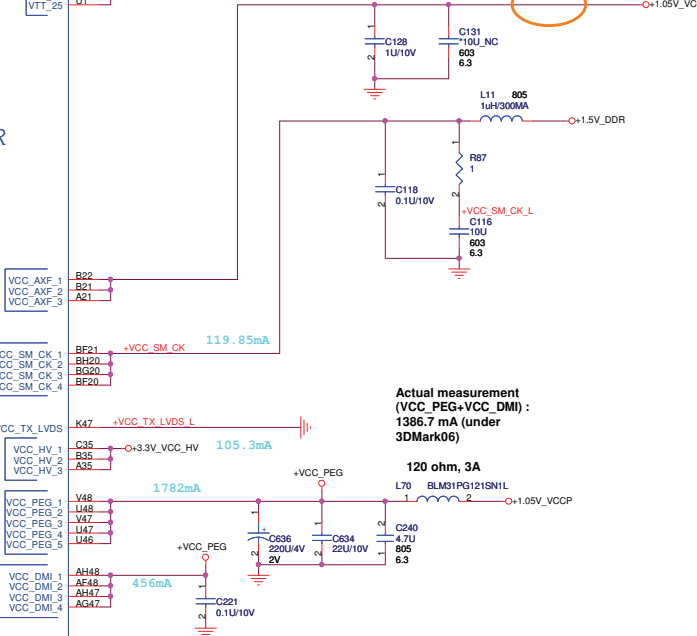
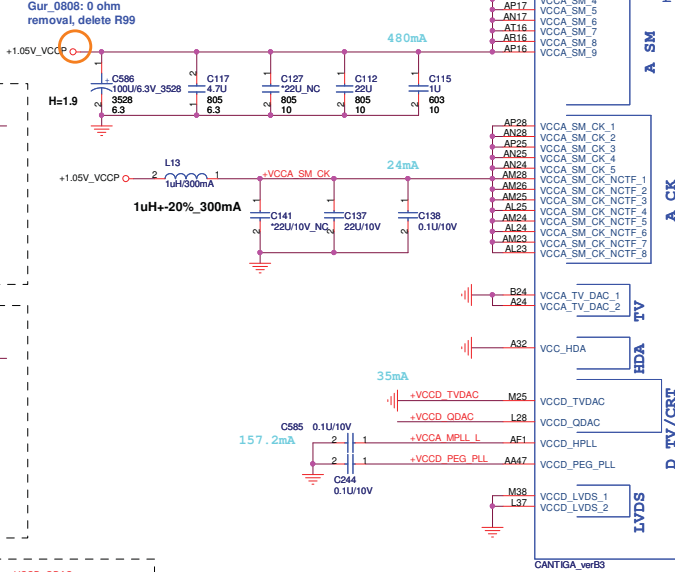
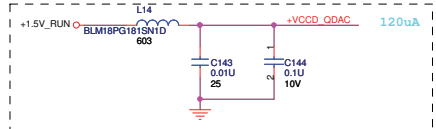
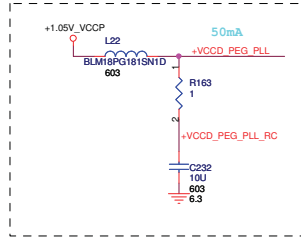
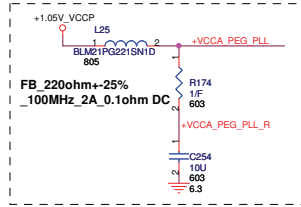
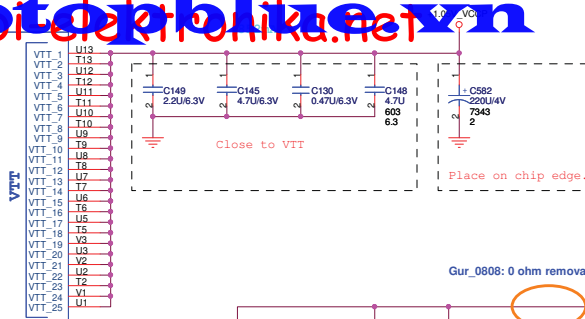
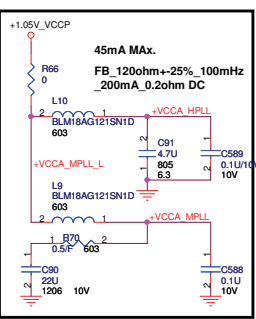
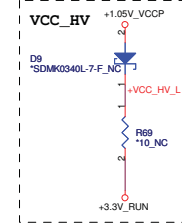
+1.05V\_VCCP

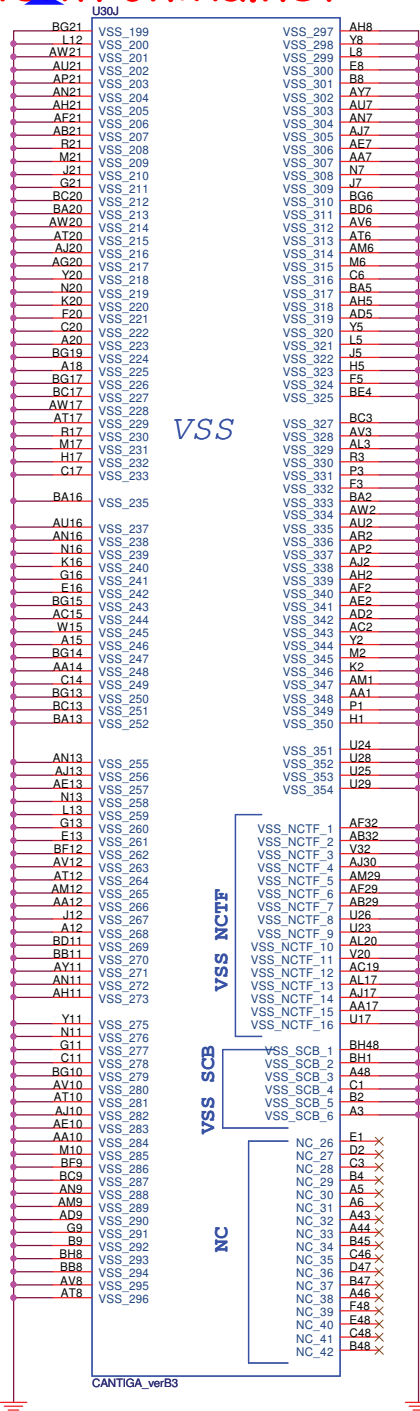
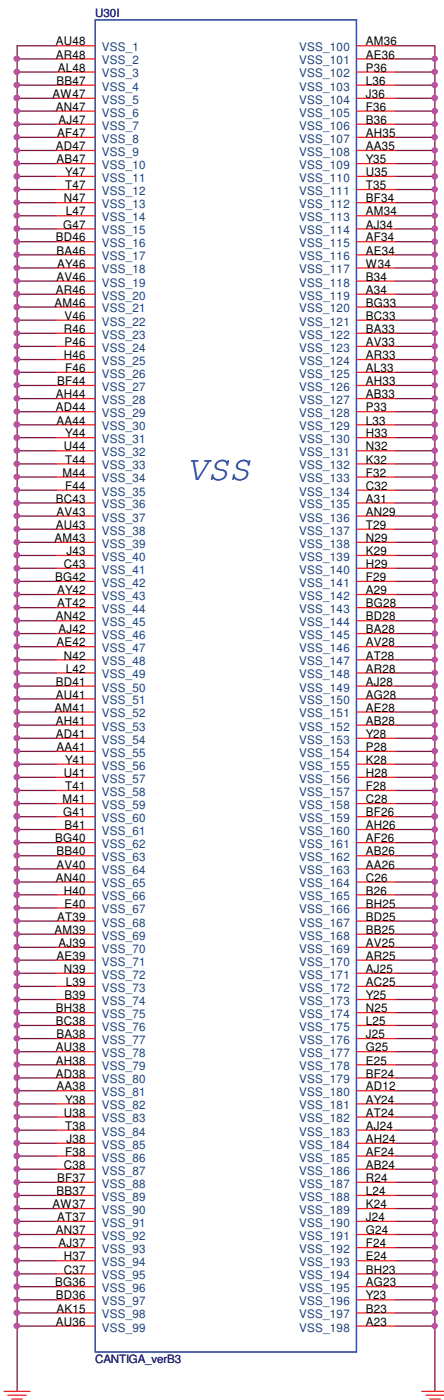
AM32  
AL32  
AK32  
AJ32  
AH32  
AG32  
AE32  
AC32  
AA32  
Y32  
W32  
U32  
AM30  
AL30  
AK30  
AJ30  
AH30  
AG30  
AF30  
AE30  
AC30  
AB30  
AA30  
Y30  
W30  
V30  
U30  
AL29  
AK29  
AJ29  
AH29  
AG29  
AE29  
AC29  
AA29  
Y29  
W29  
V29  
U29  
AL28  
AK28  
AJ28  
AH28  
AG28  
AE28  
AC28  
AA28  
Y28  
W28  
V28  
U28

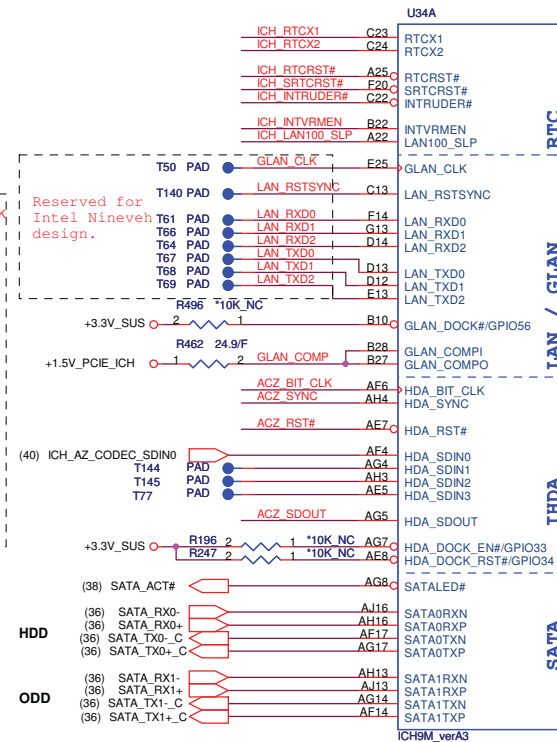
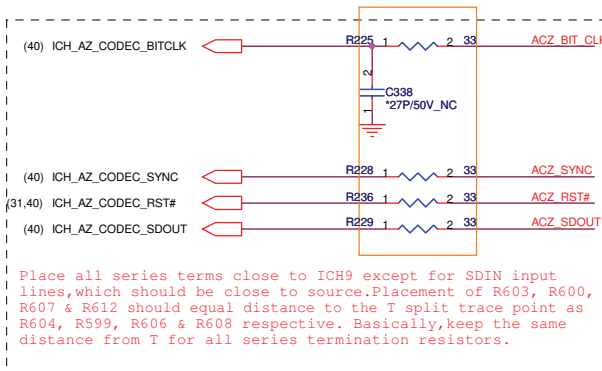
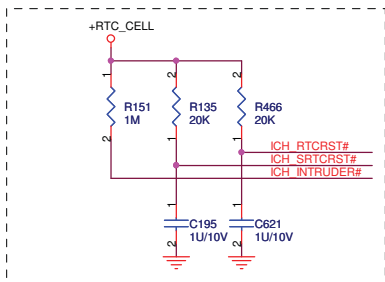
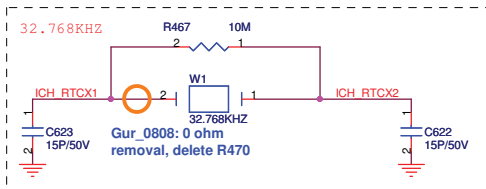
CANTIGA\_verB3





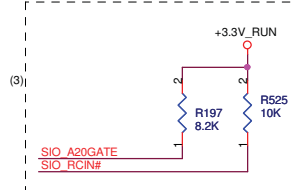
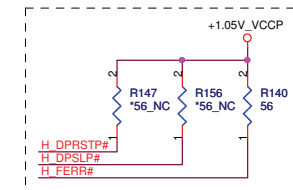
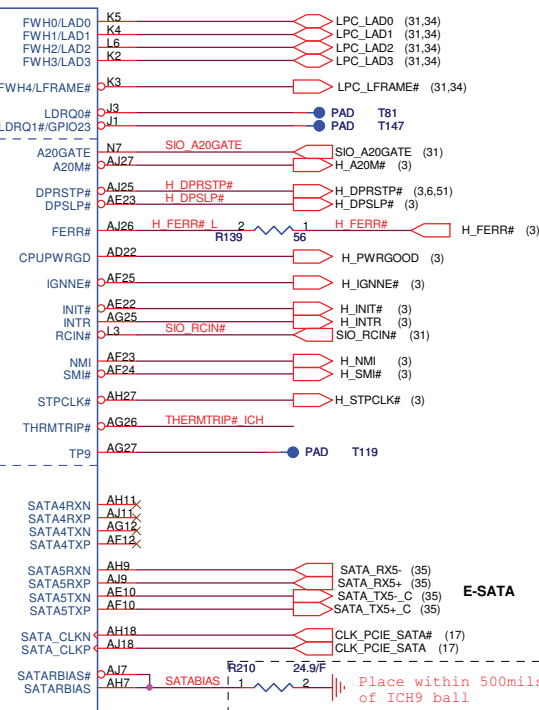
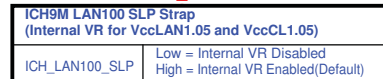
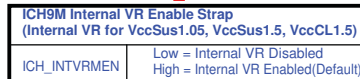


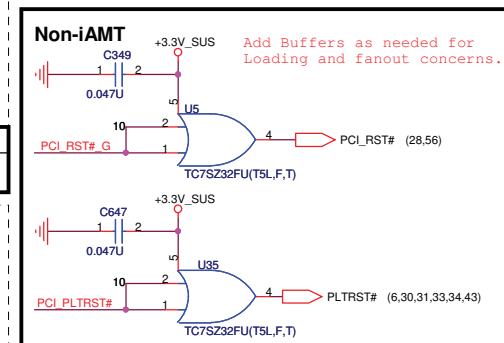
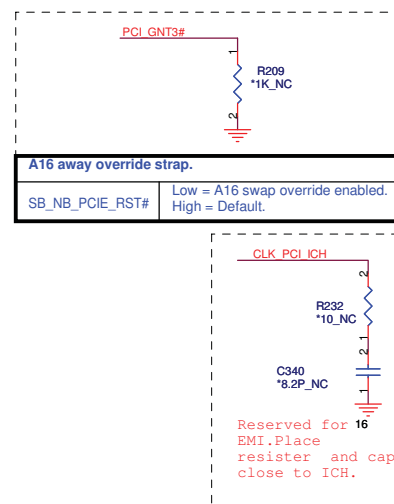
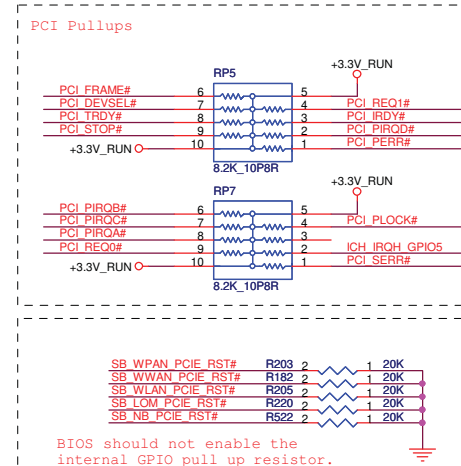
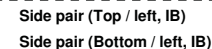
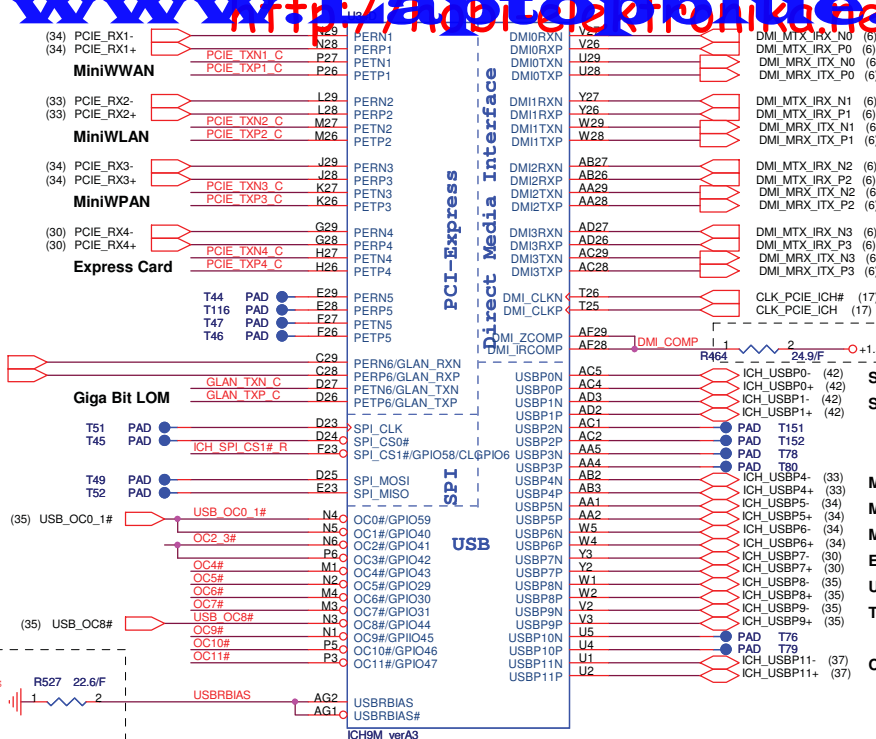
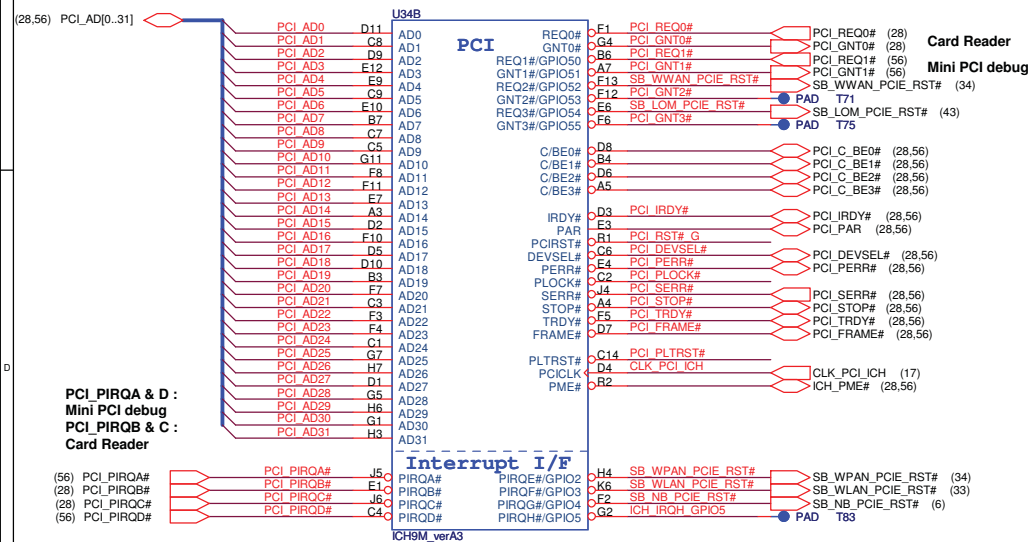
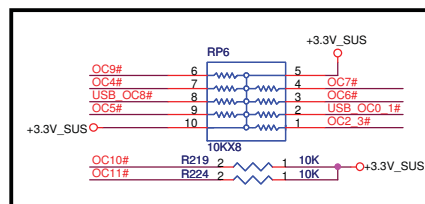
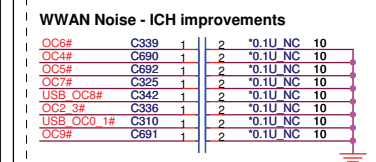
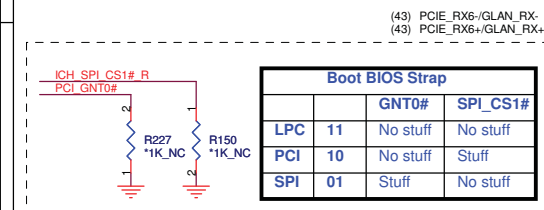
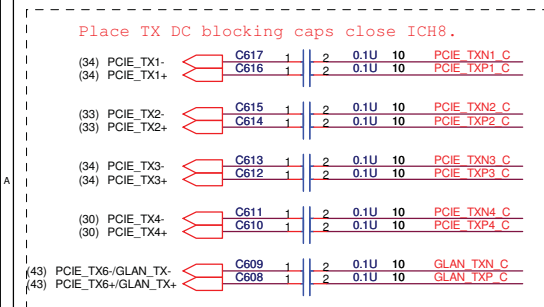


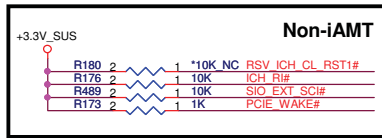
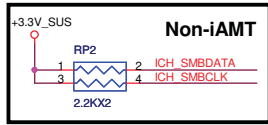


XOR Chain Entrance Strap

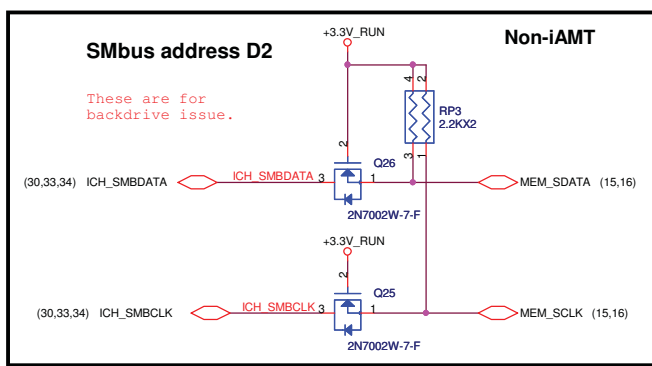
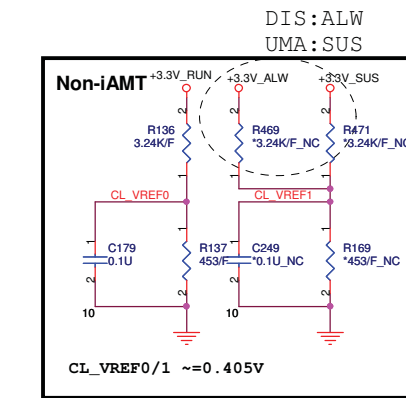
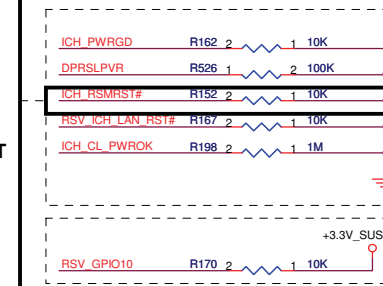
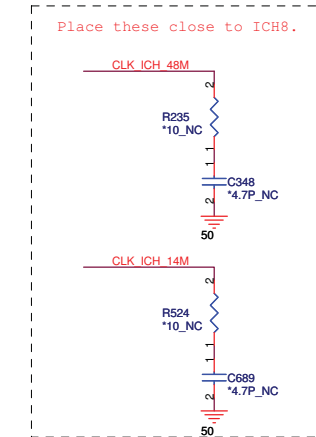
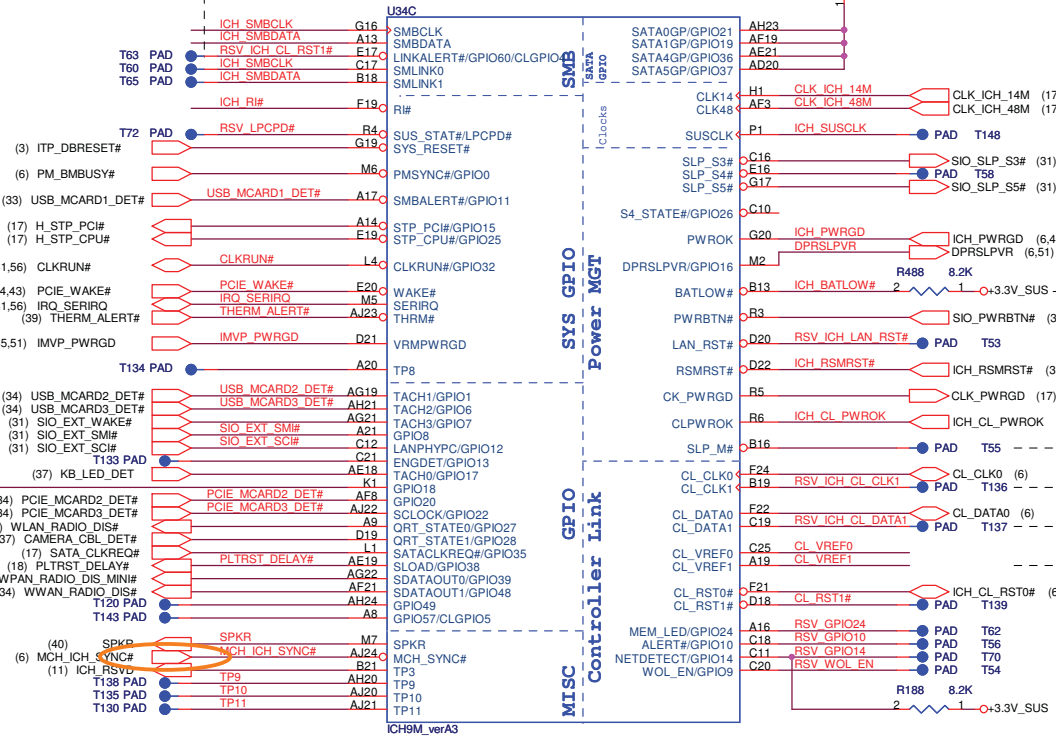
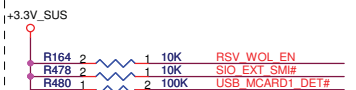
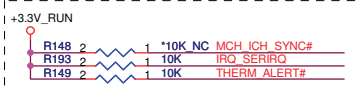
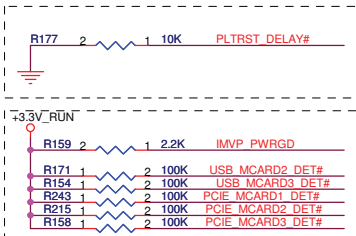
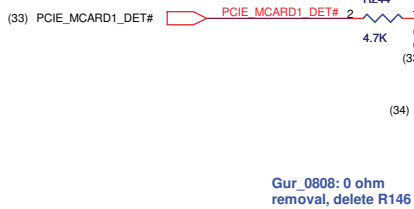
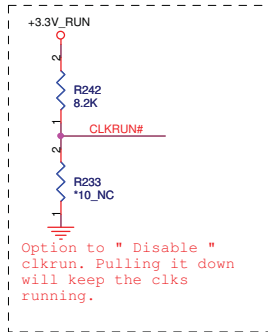
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



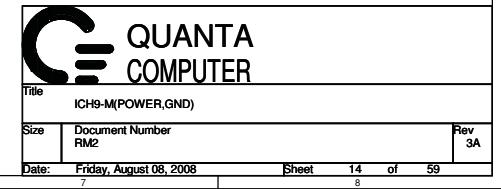


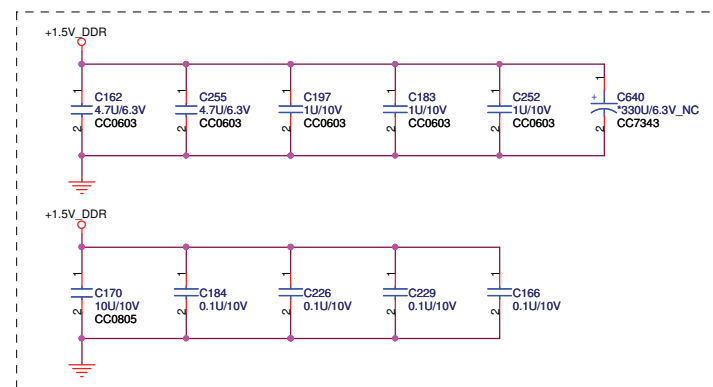
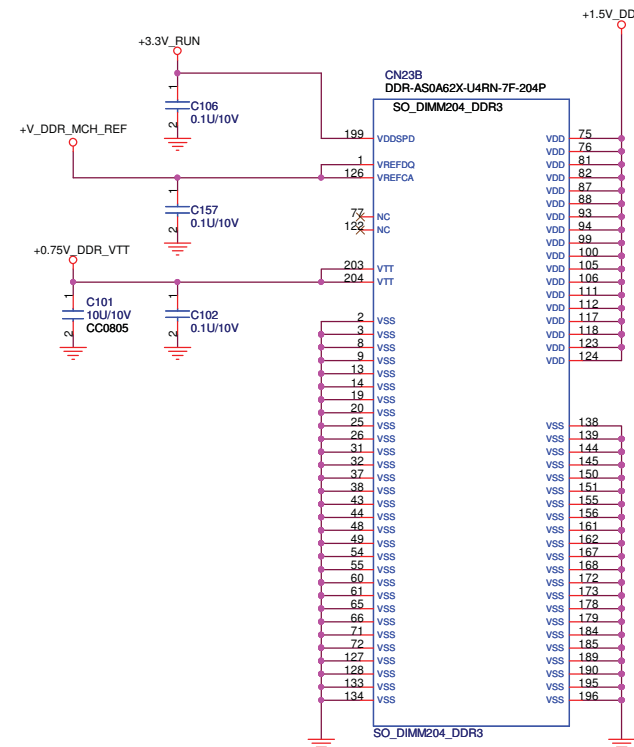
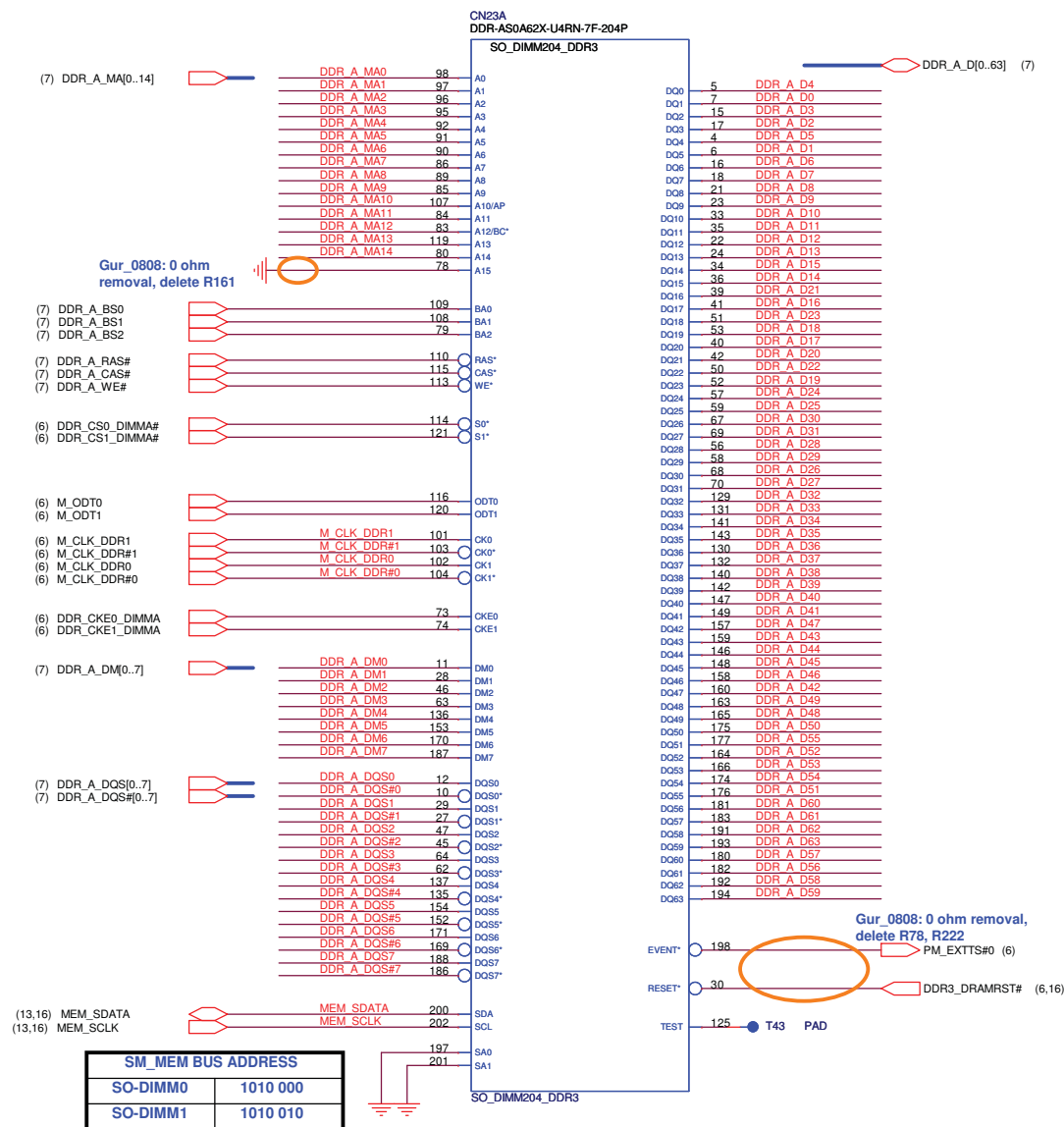


Gur\_0808: 0 ohm removal,  
delete R178, R186, RP14





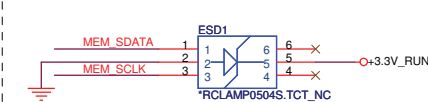


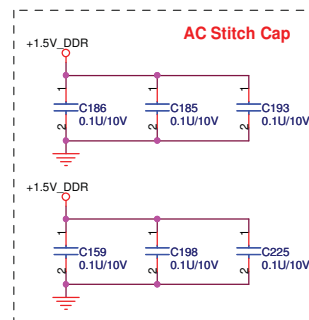
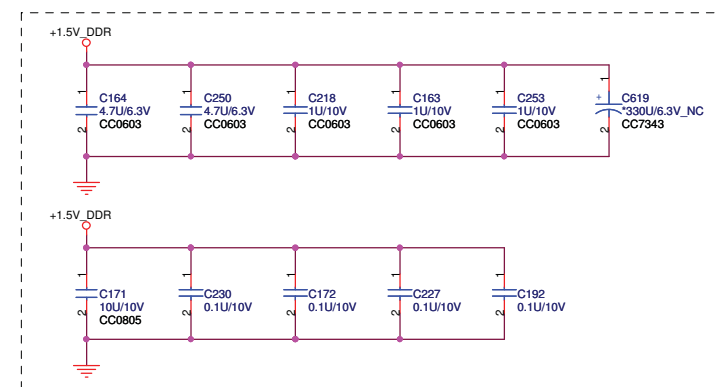
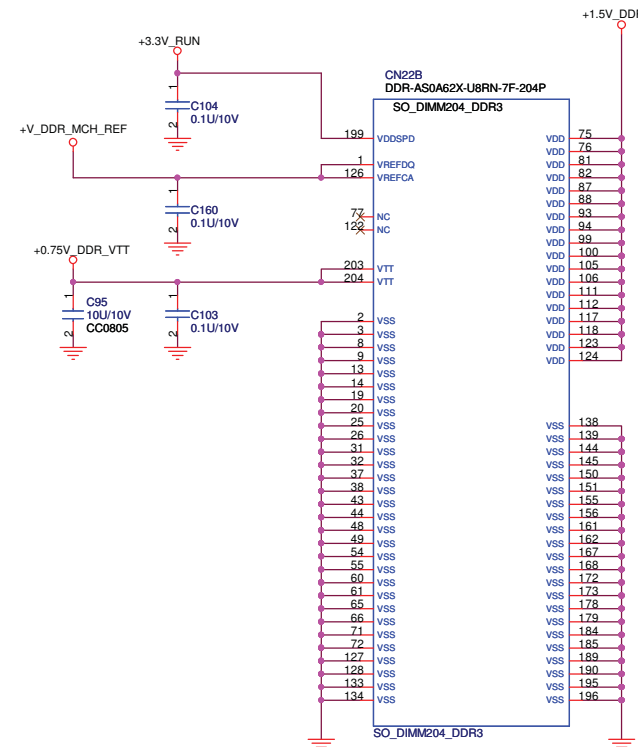
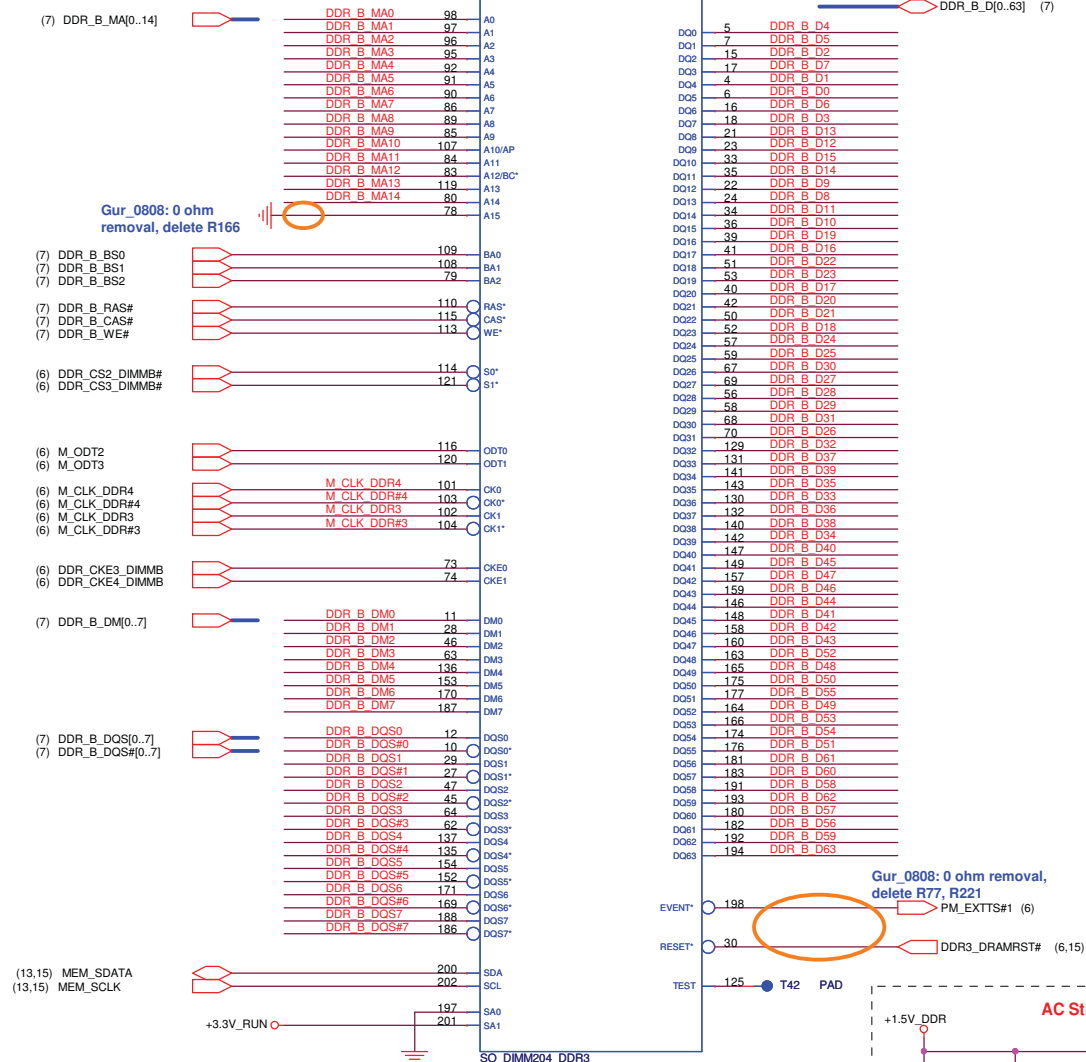


**For EMI Reserved**



**Place ESD Protection diodes.**





**For EMI Reserved**

M CLK DDR4	R138	1	2	*200/F NC	M CLK DDR4
M CLK DDR3	R142	1	2	*200/F NC	M CLK DDR3



Title	DDR3 SO-DIMM2 (204P)
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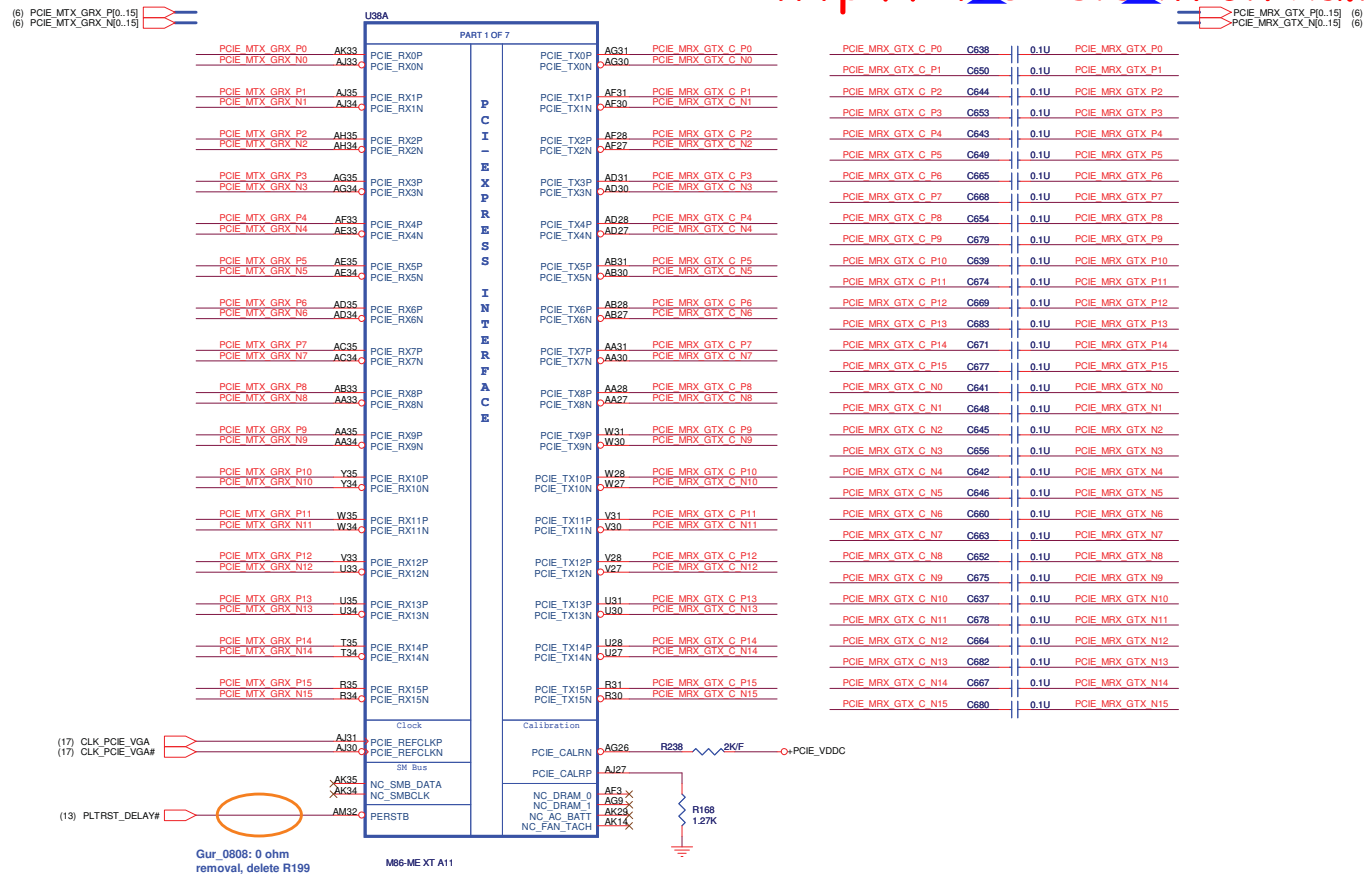
Size

Document Number	RM2
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Date: Thursday, August 14, 2008

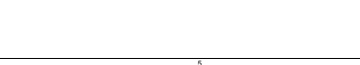
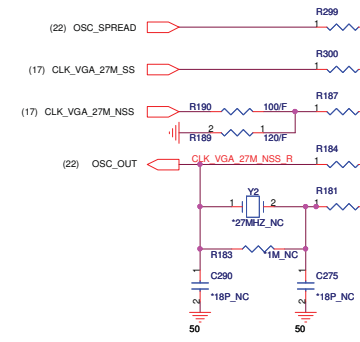
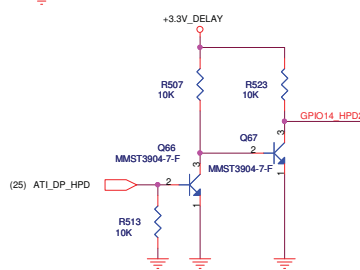
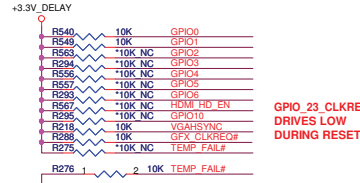
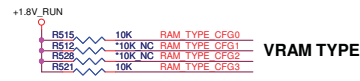
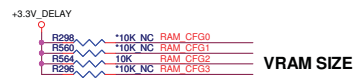
Sheet 16 of 59







MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

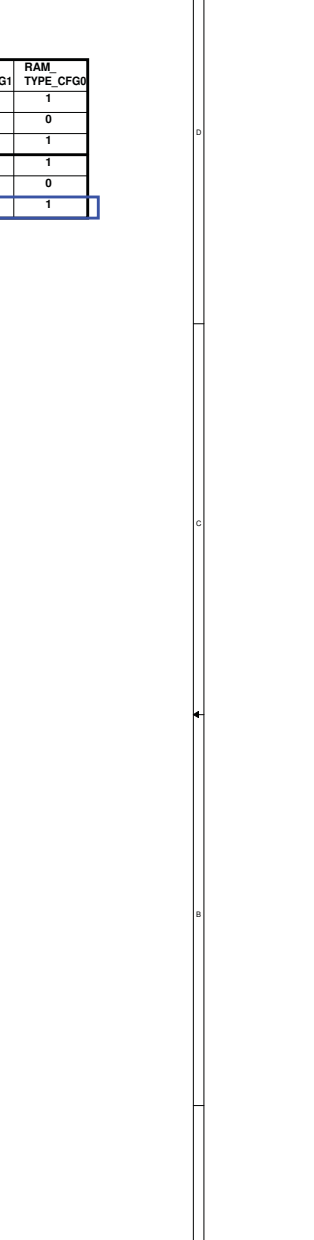
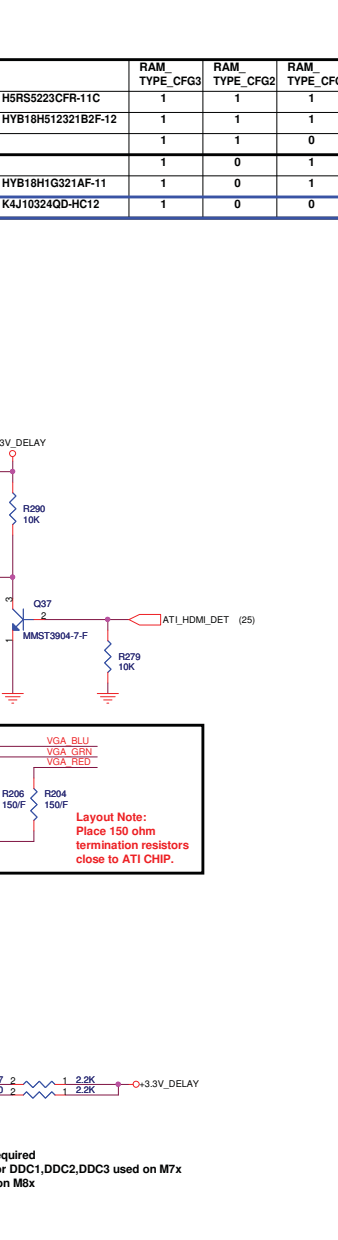
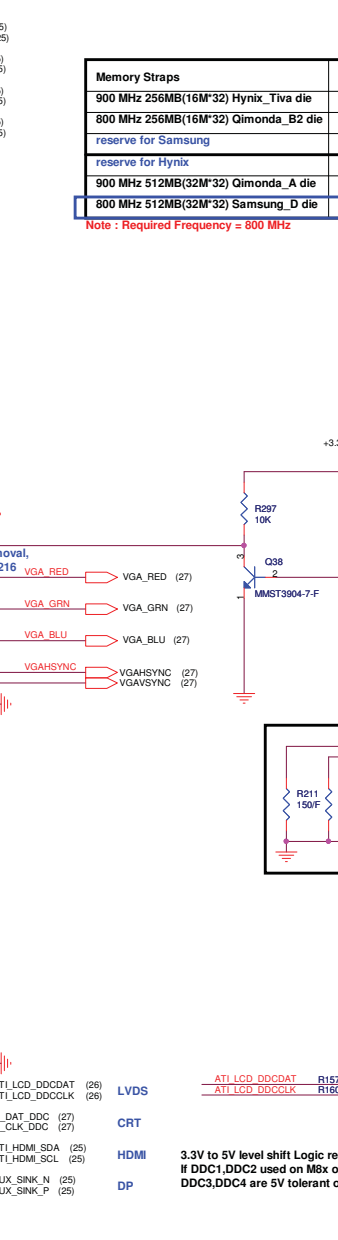
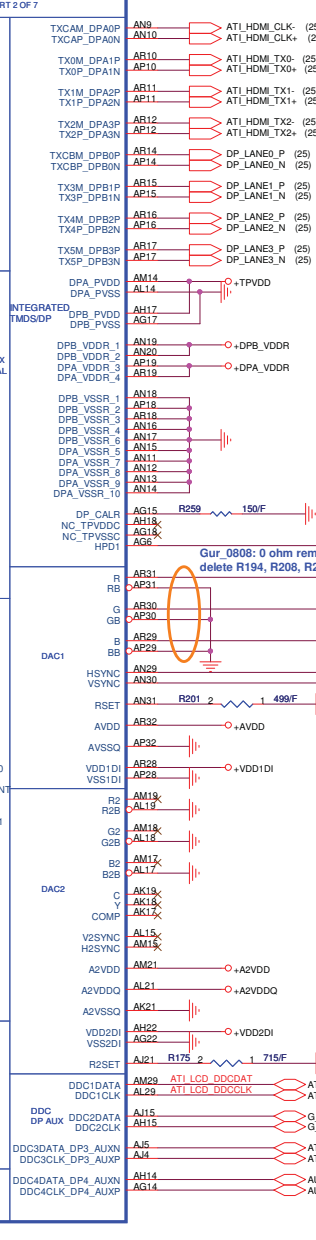
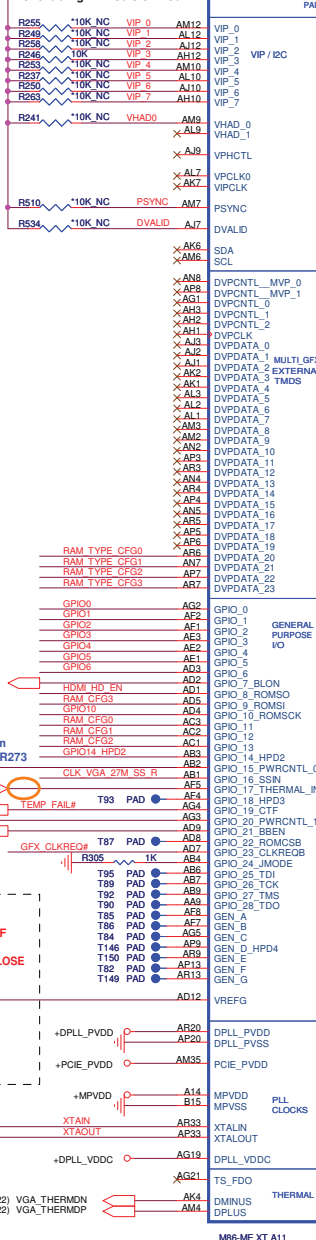


VRAM SIZE

VRAM TYPE

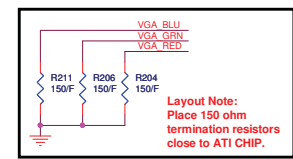
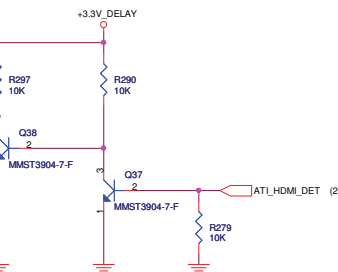
GPIO\_23\_CLKREQB DRIVES LOW DURING RESET

8/15: The strap on VIP[3] is for enabling HD Audio on M86.



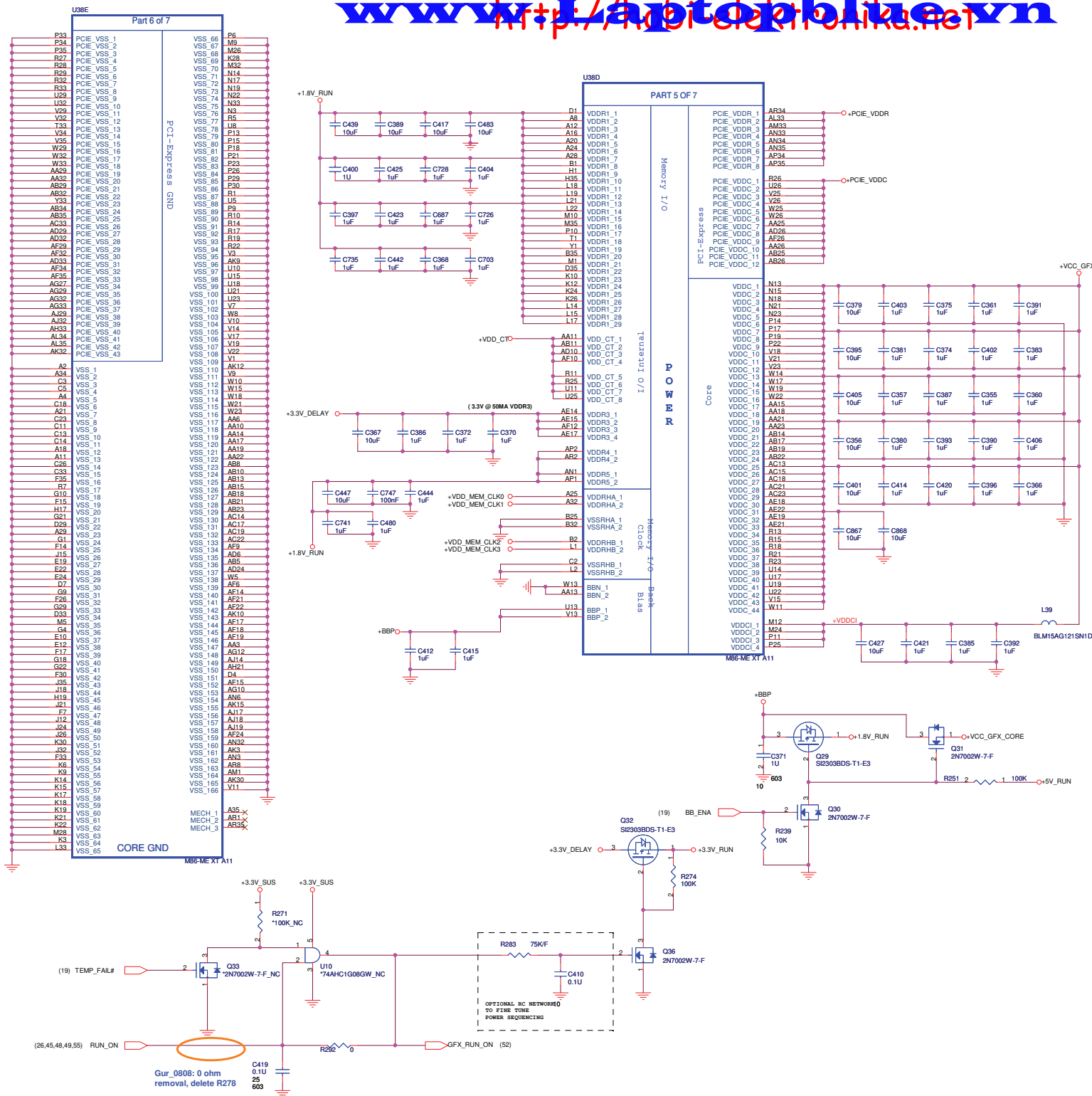
Memory Straps		RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
900 MHz 256MB(16M*32) Hynix_Tiva die	H5RS5223CFR-11C	1	1	1	1
800 MHz 256MB(16M*32) Qimonda_B2 die	HYB18H512321B2F-12	1	1	1	0
reserve for Samsung		1	1	0	1
reserve for Hynix		1	0	1	1
900 MHz 512MB(32M*32) Qimonda_A die	HYB18H1G321AF-11	1	0	1	0
800 MHz 512MB(32M*32) Samsung_D die	K4J10324QD-HC12	1	0	0	1

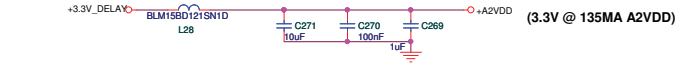
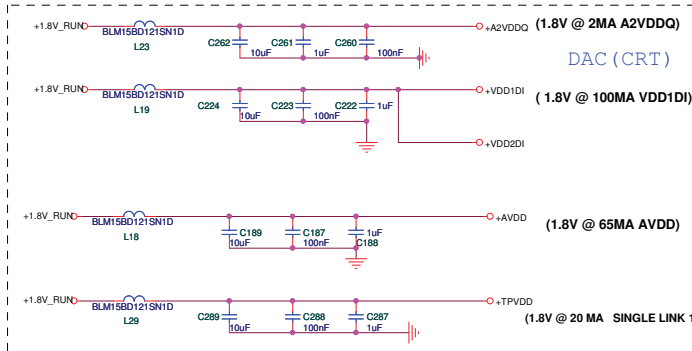
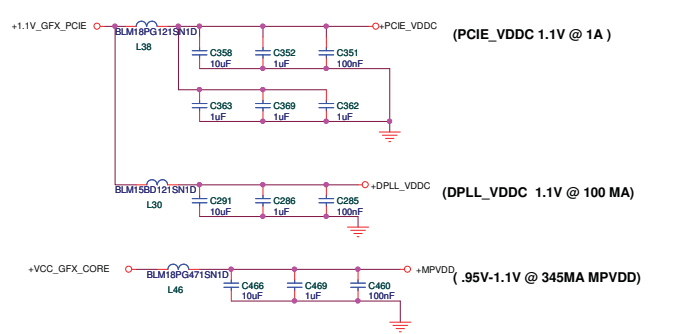
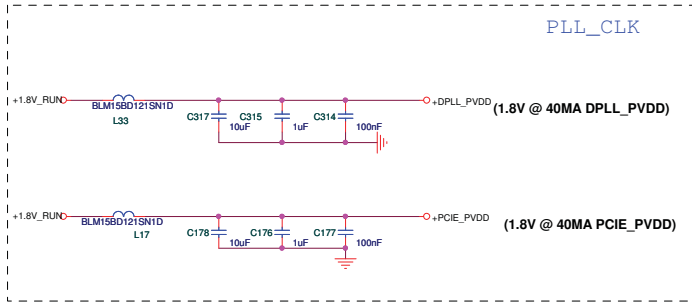
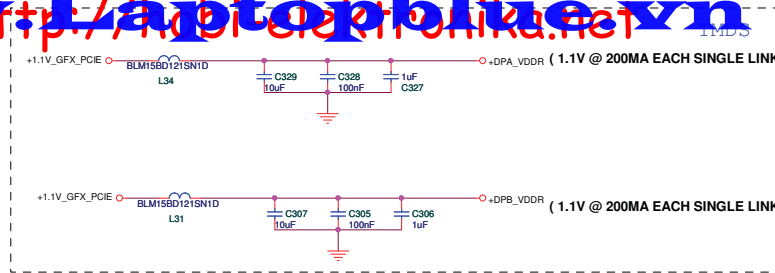
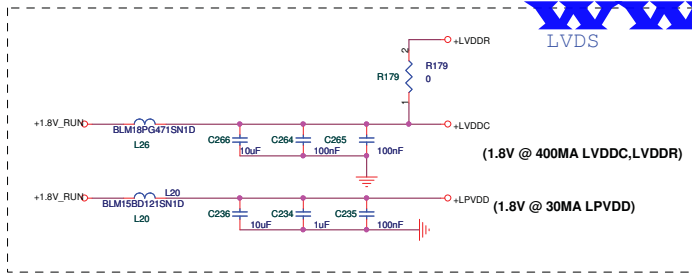
Note : Required Frequency = 800 MHz



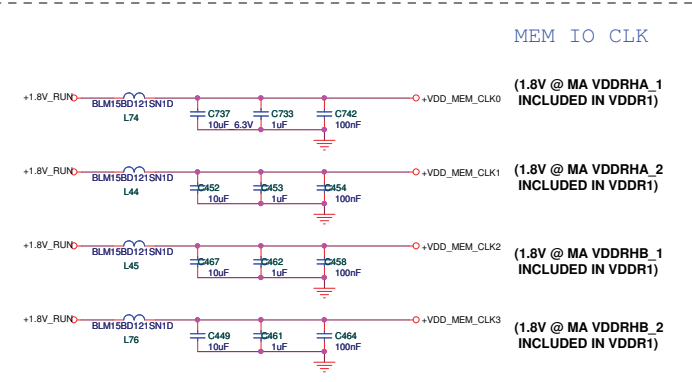
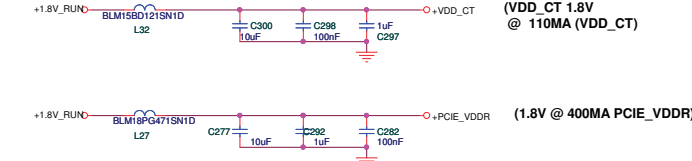
Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

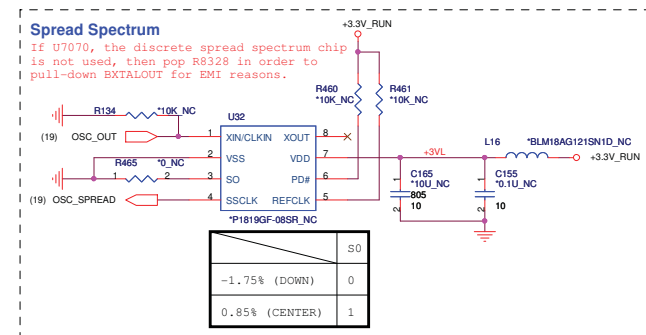
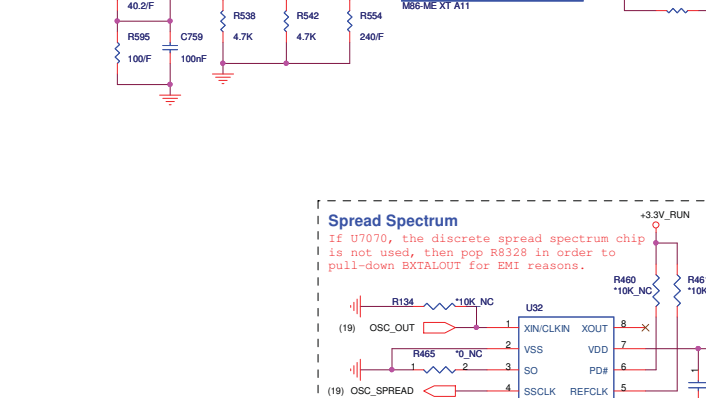
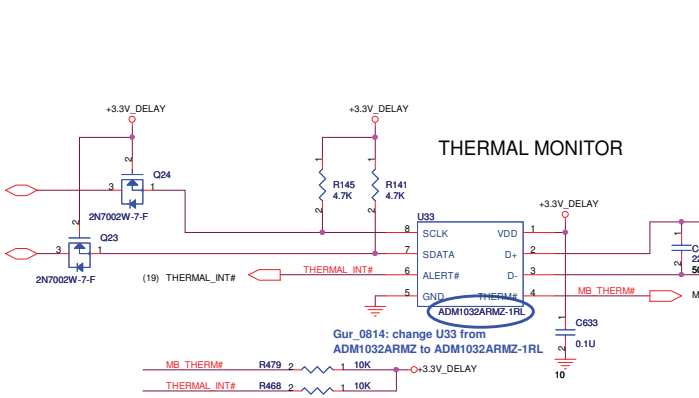
3.3V to 5V level shift Logic required If DDC1,DDC2 used on M8x or DDC1,DDC2,DDC3 used on M7x DDC3,DDC4 are 5V tolerant on M8x

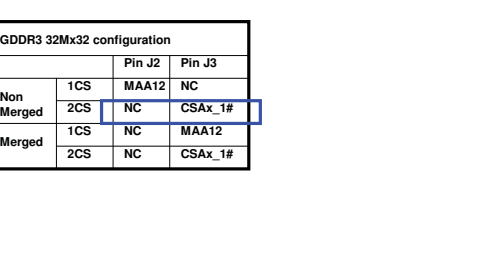
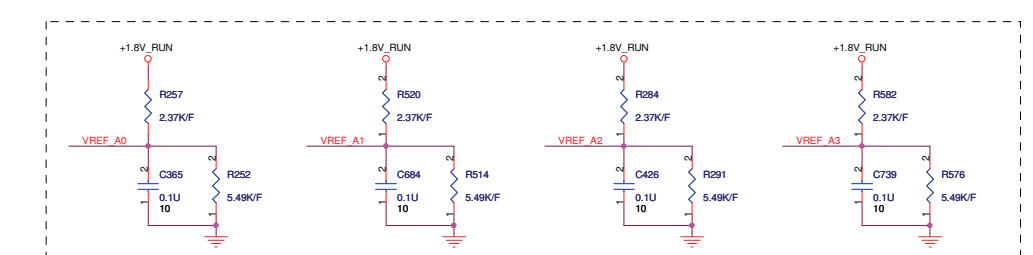
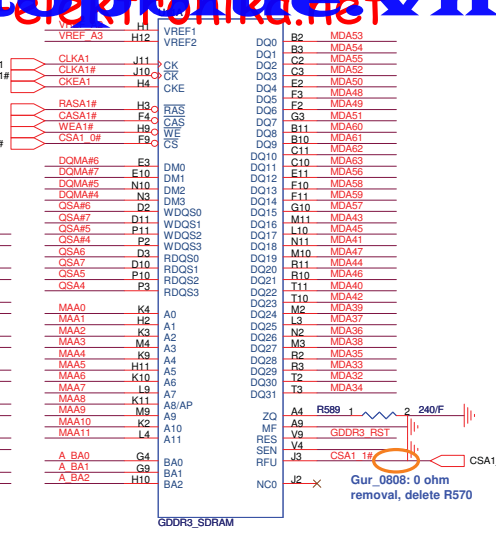
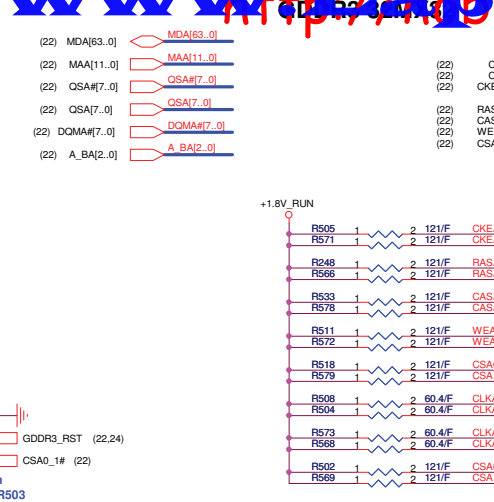




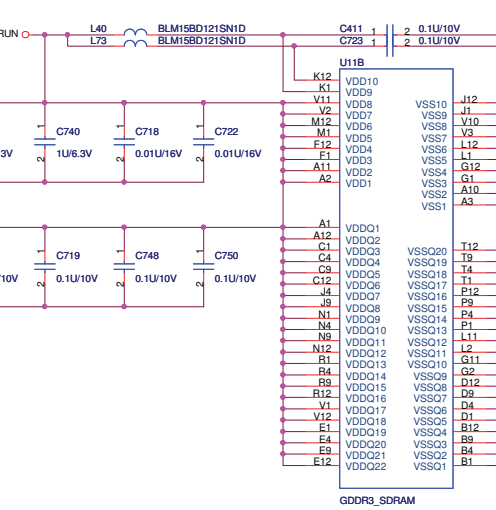
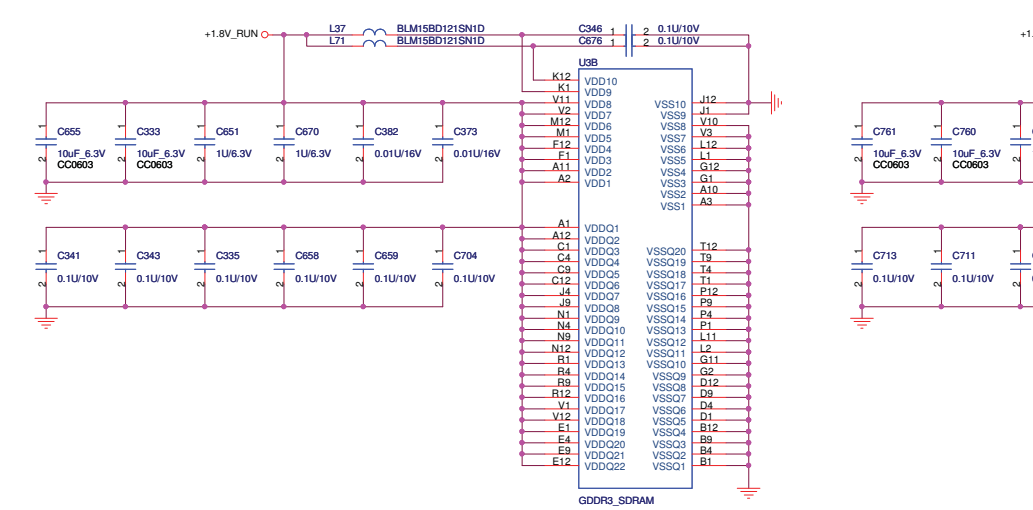
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



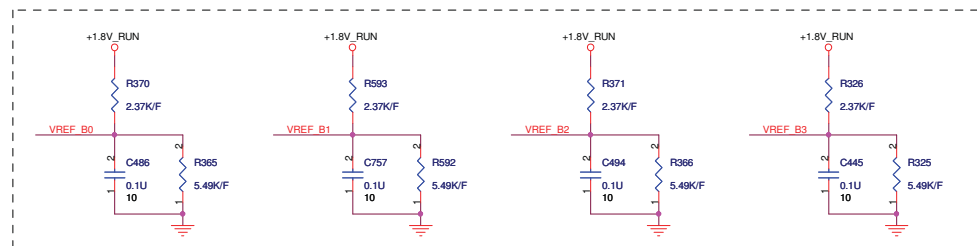
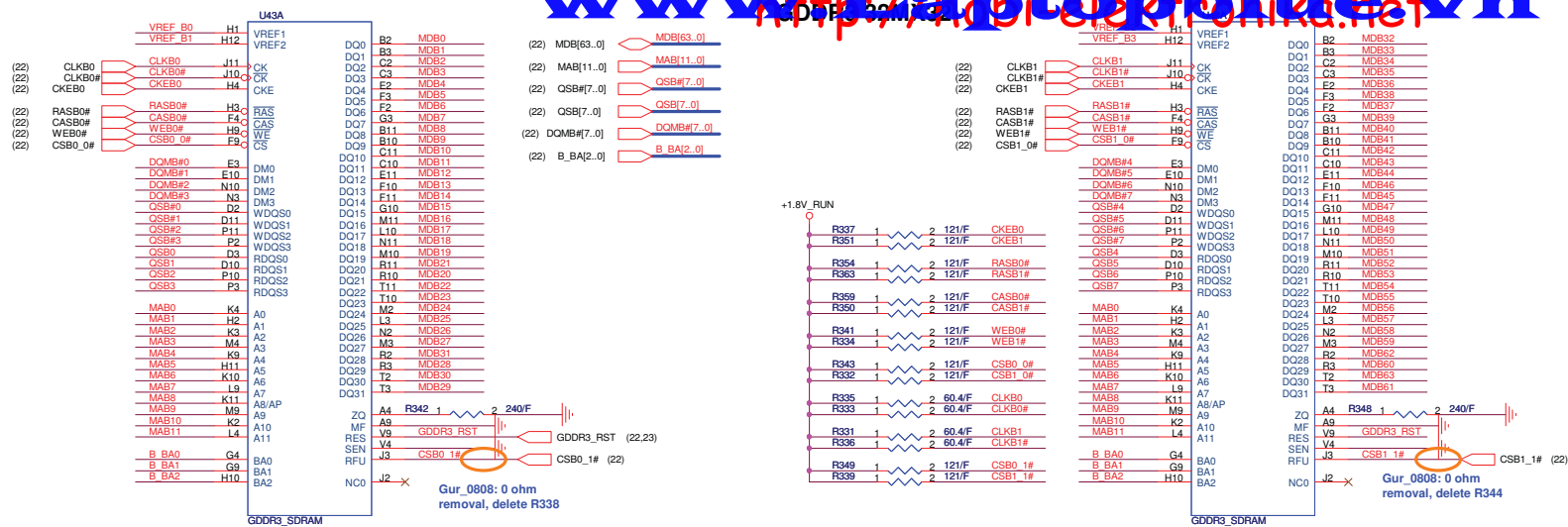




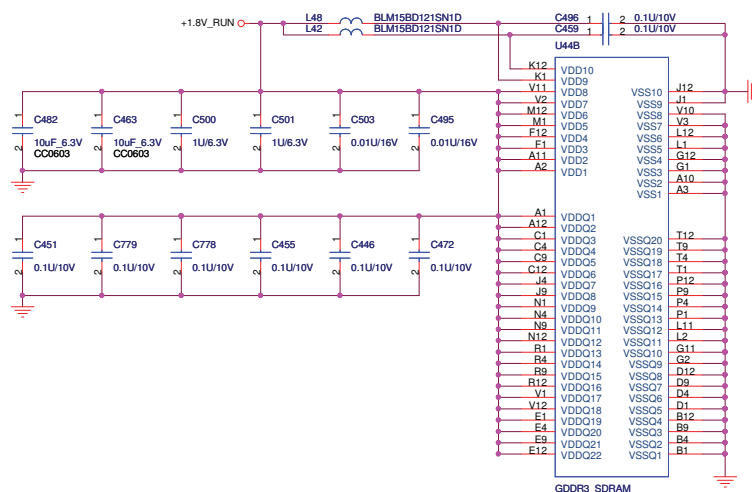
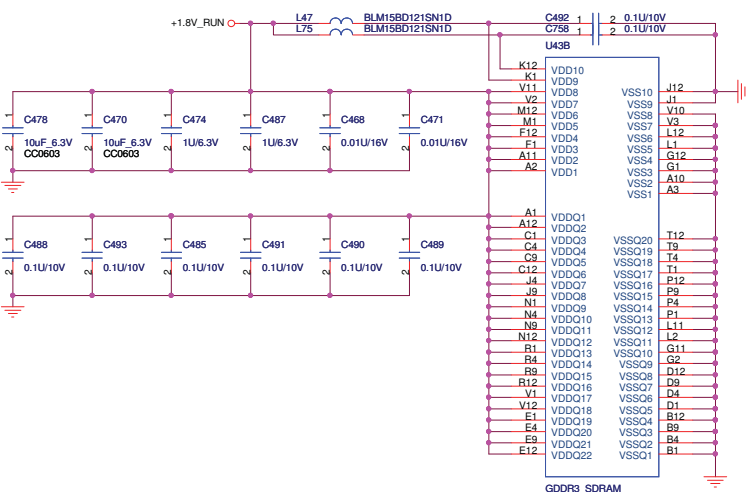
GDDR3 32Mx32 configuration			
	Pin J2	Pin J3	
Non Merged	1CS	MAA12	NC
Merged	2CS	NC	CSAx_1#

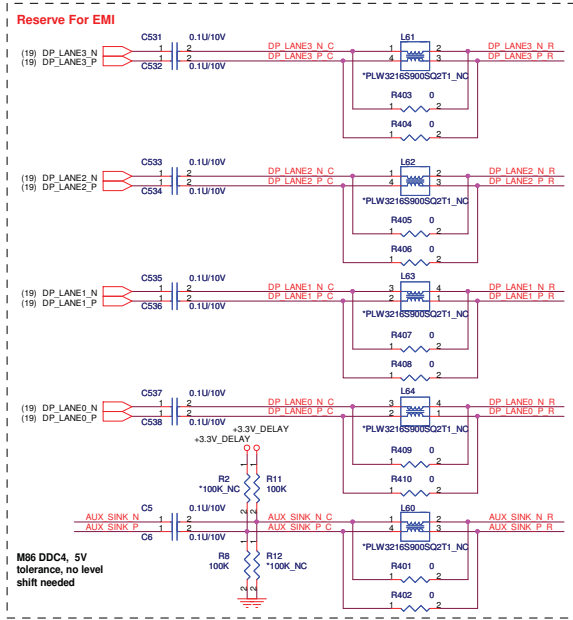
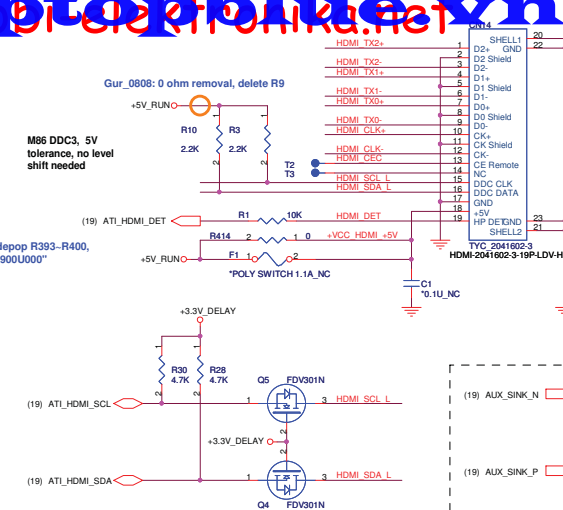
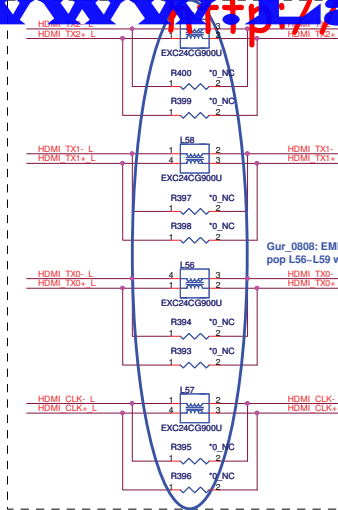
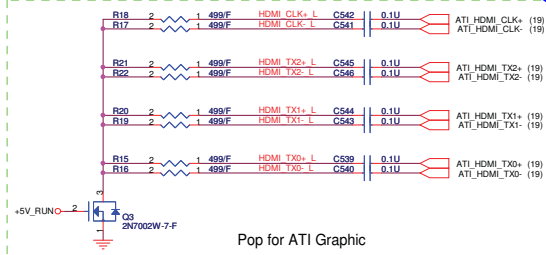




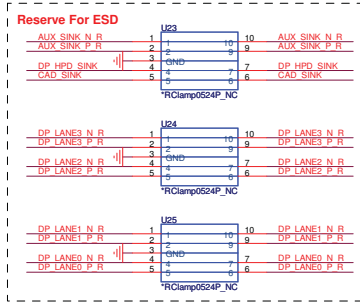
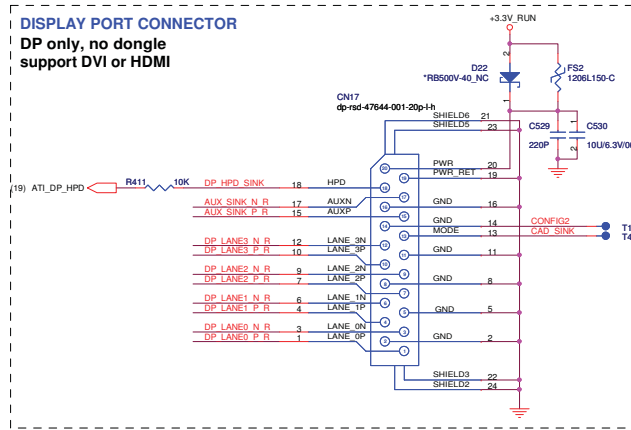
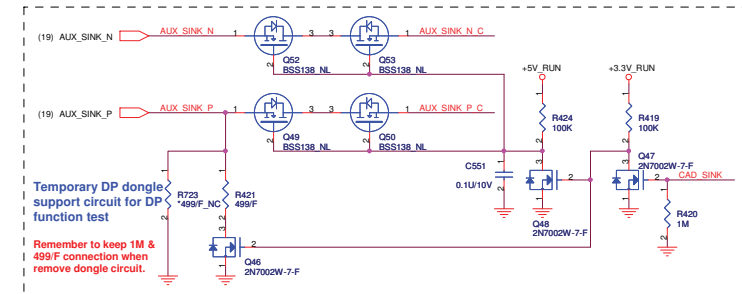


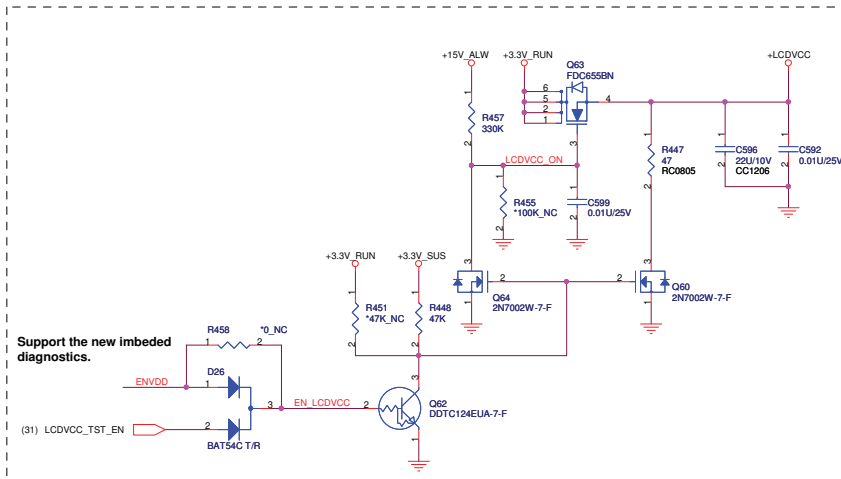
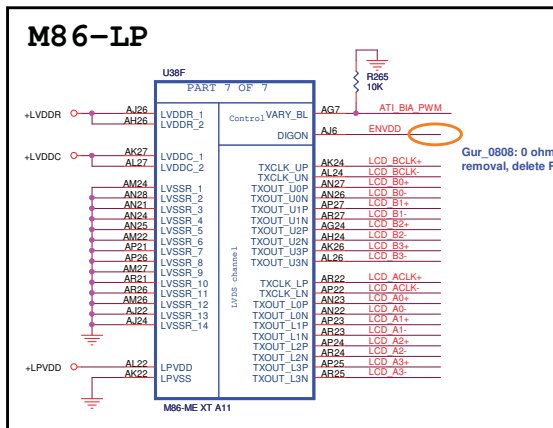
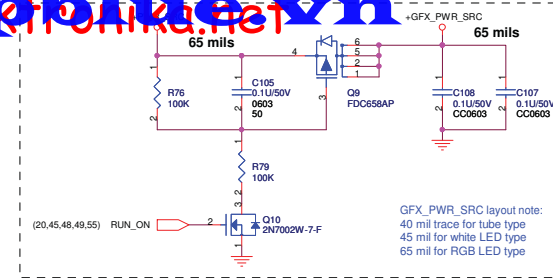
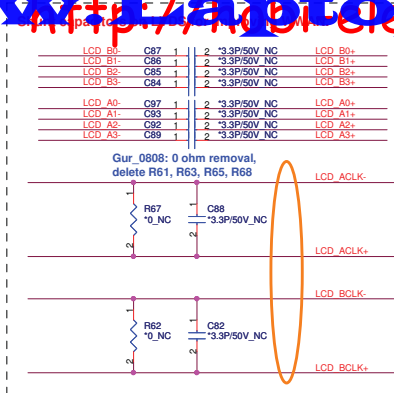
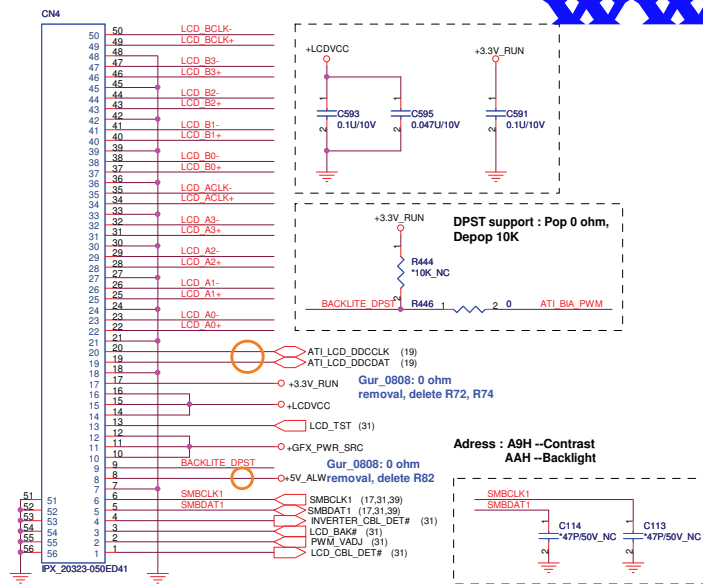
GDDR3 32Mx32 configuration			
		Pin J2	Pin J3
Non Merged	1CS	MAB12	NC
	2CS	NC	CSBx_1#
Merged	1CS	NC	MAB12
	2CS	NC	CSBx_1#

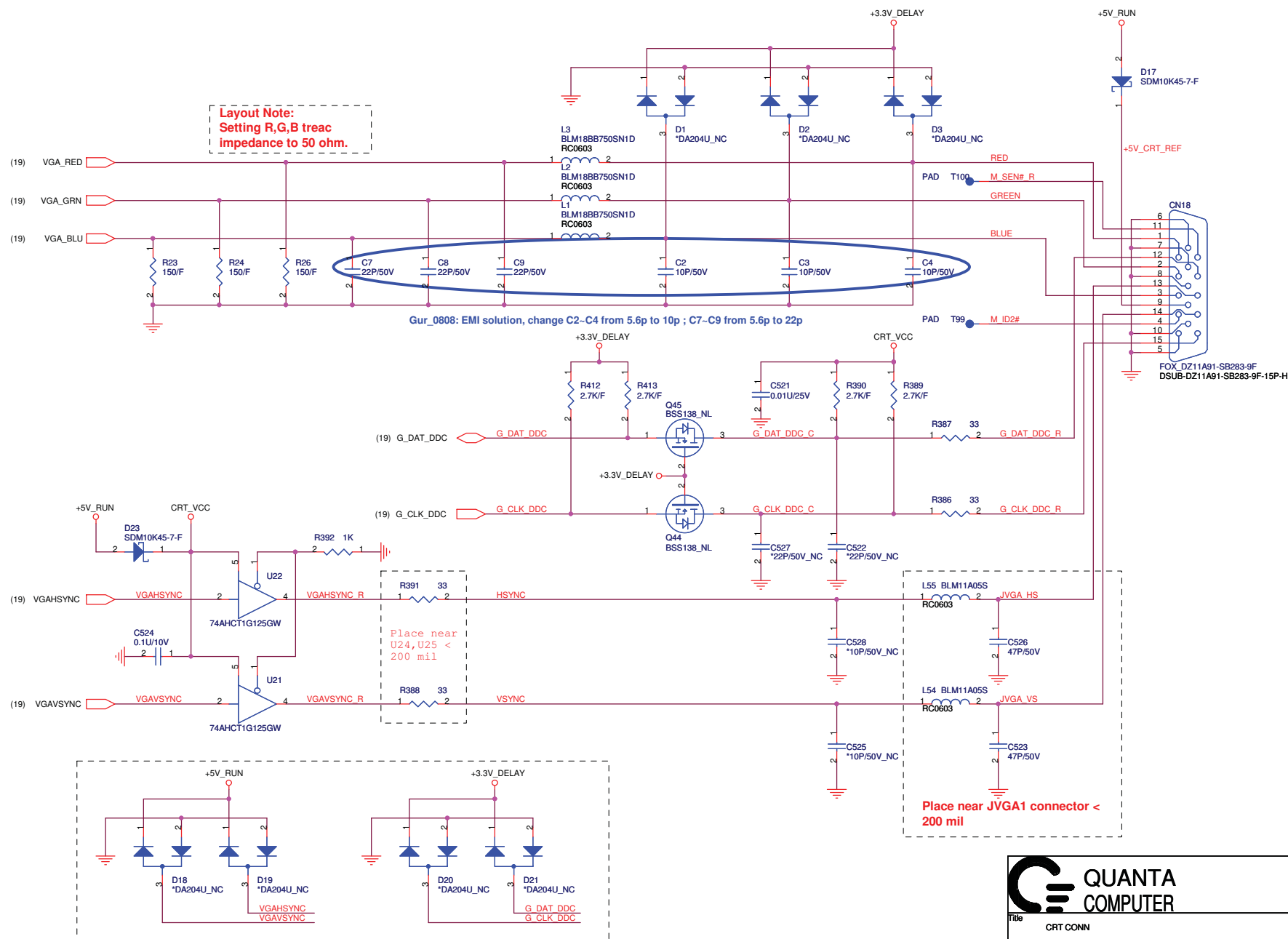




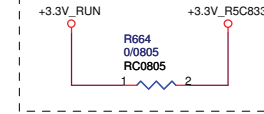
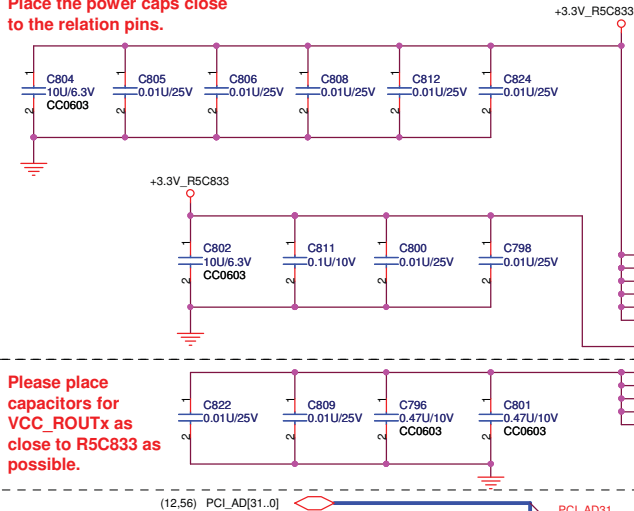
**Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.**



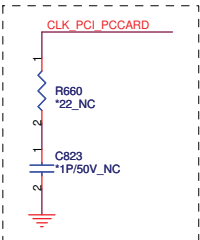
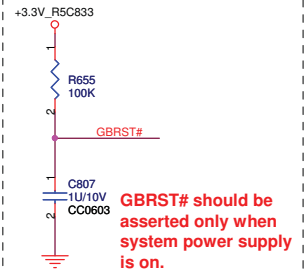
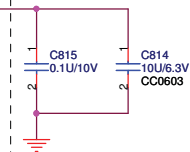




Place the power caps close to the relation pins.



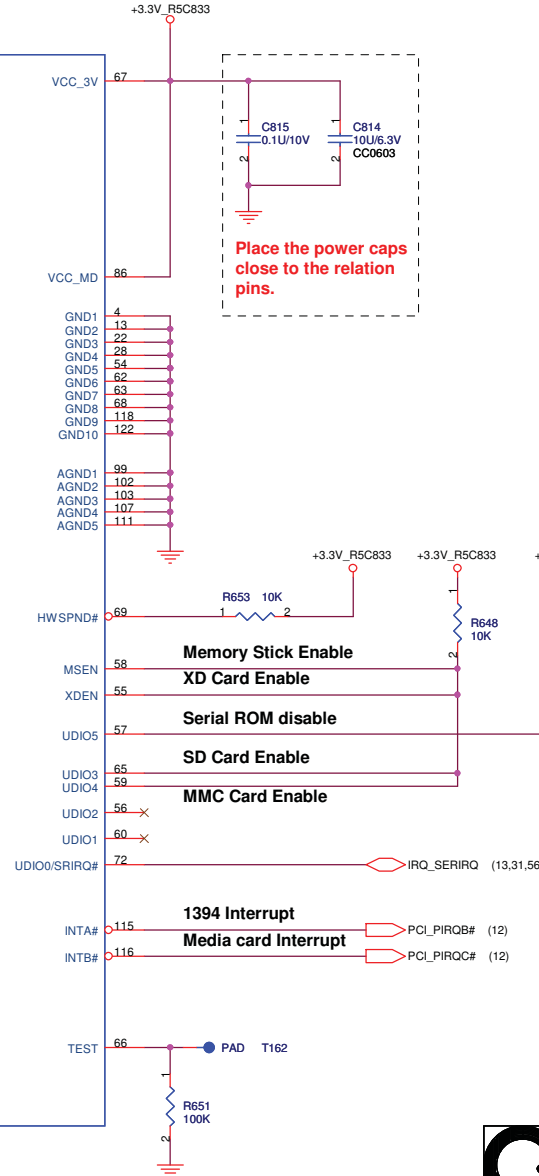
Place the power caps close to the relation pins.



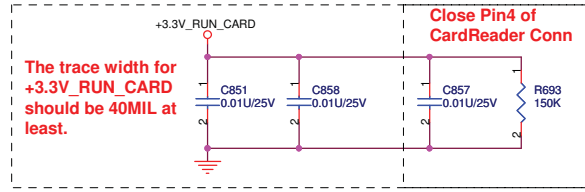
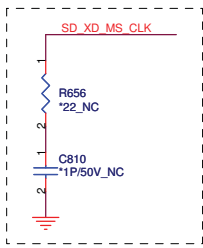
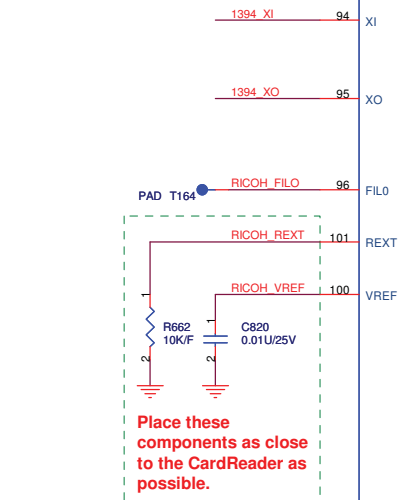
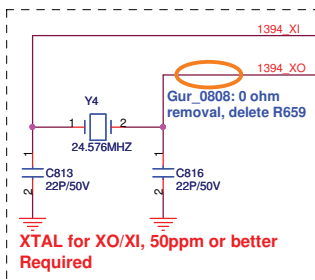
(12,56) PCI\_PAR  
(12,56) PCI\_C\_BE3#  
(12,56) PCI\_C\_BE2#  
(12,56) PCI\_C\_BE1#  
(12,56) PCI\_C\_BE0#  
  
(12) PCI\_REQ0#  
(12) PCI\_GNT0#  
(12,56) PCI\_FRAME#  
(12,56) PCI\_IRDY#  
(12,56) PCI\_TRDY#  
(12,56) PCI\_DEVSEL#  
(12,56) PCI\_STOP#  
(12,56) PCI\_PERR#  
(12,56) PCI\_SERR#  
  
(12,56) PCI\_RST#  
(17) CLK\_PCI\_PCCARD  
(12,56) ICH\_PME#  
(13,31,56) CLKRUN#

PCI AD31  
PCI AD30  
PCI AD29  
PCI AD28  
PCI AD27  
PCI AD26  
PCI AD25  
PCI AD24  
PCI AD23  
PCI AD22  
PCI AD21  
PCI AD20  
PCI AD19  
PCI AD18  
PCI AD17  
PCI AD16  
PCI AD15  
PCI AD14  
PCI AD13  
PCI AD12  
PCI AD11  
PCI AD10  
PCI AD9  
PCI AD8  
PCI AD7  
PCI AD6  
PCI AD5  
PCI AD4  
PCI AD3  
PCI AD2  
PCI AD1  
PCI AD0  
  
AD31  
AD30  
AD29  
AD28  
AD27  
AD26  
AD25  
AD24  
AD23  
AD22  
AD21  
AD20  
AD19  
AD18  
AD17  
AD16  
AD15  
AD14  
AD13  
AD12  
AD11  
AD10  
AD9  
AD8  
AD7  
AD6  
AD5  
AD4  
AD3  
AD2  
AD1  
AD0  
  
PAR  
C/BE3#  
C/BE2#  
C/BE1#  
C/BE0#  
IDSEL  
  
REQ#  
GNT#  
FRAME#  
IRDY#  
TRDY#  
DEVSEL#  
STOP#  
PERR#  
SERR#  
  
GBRST#  
PCIRST#  
PCICLK  
PME#  
CLKRUN#

PCI / OTHER

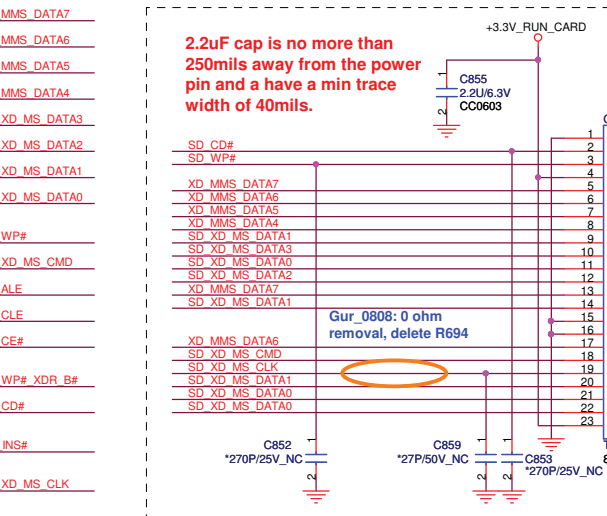
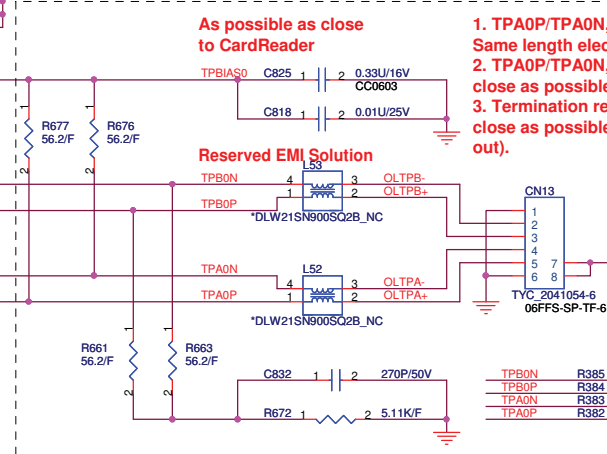
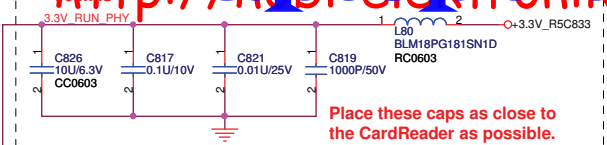




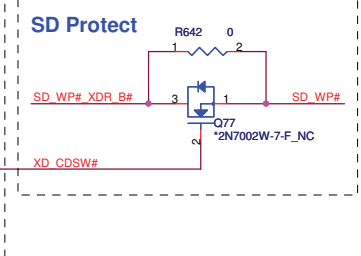
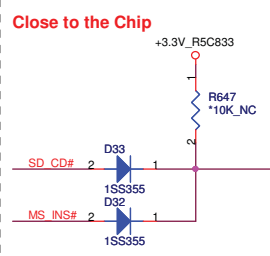
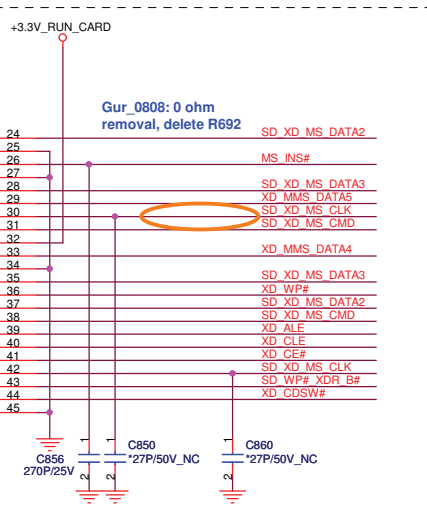
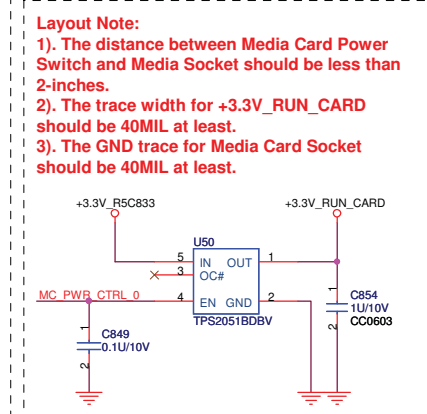
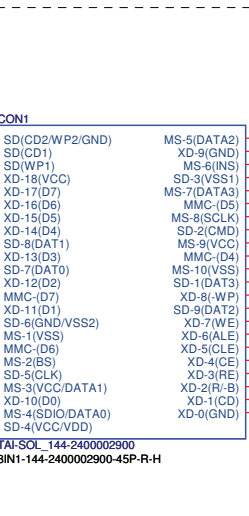


AVCC\_PHY1  
AVCC\_PHY2  
AVCC\_PHY3  
AVCC\_PHY4

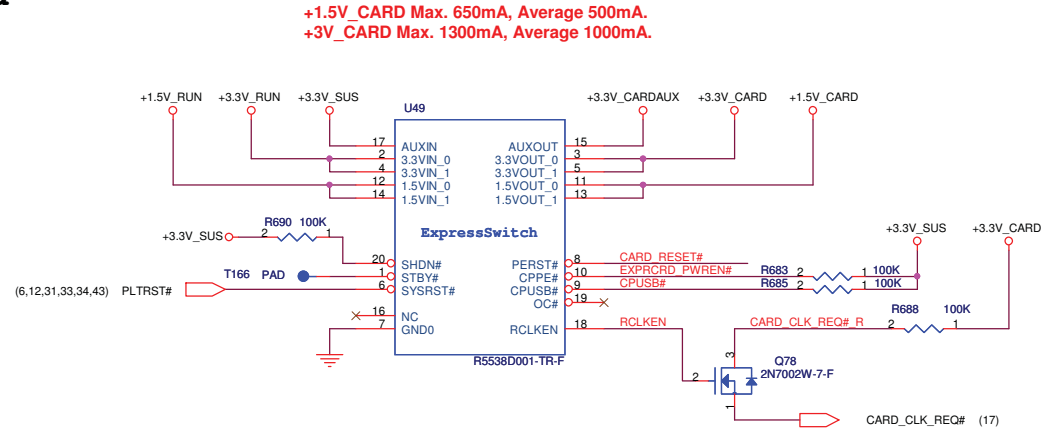
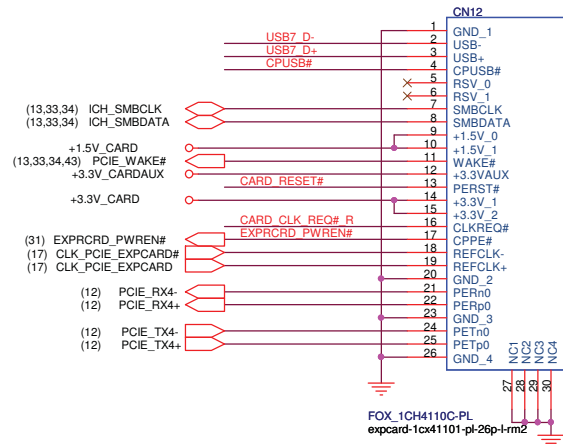
TPBIAS0  
TPB0N  
TPB0P  
TPA0N  
TPA0P  
MDIO17  
MDIO16  
MDIO15  
MDIO14  
MDIO13  
MDIO12  
MDIO11  
MDIO10  
MDIO05  
MDIO08  
MDIO19  
MDIO18  
MDIO02  
MDIO03  
MDIO00  
MDIO01  
MDIO09  
MDIO04  
MDIO06  
MDIO07



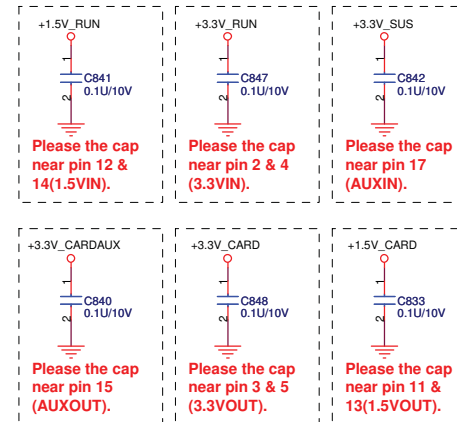
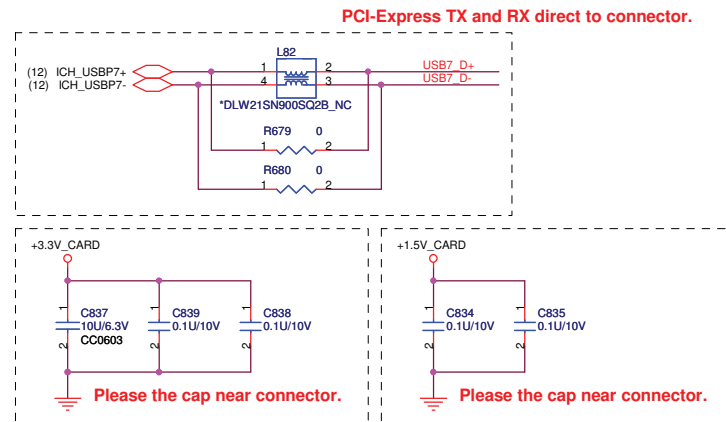
TPB0N	R385	2	0	OLTPB-
TPB0P	R384	2	0	OLTPB+
TPA0N	R383	2	0	OLTPA-
TPA0P	R382	2	0	OLTPA+

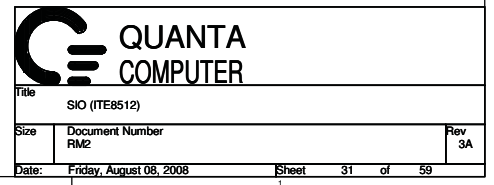


## Express Card

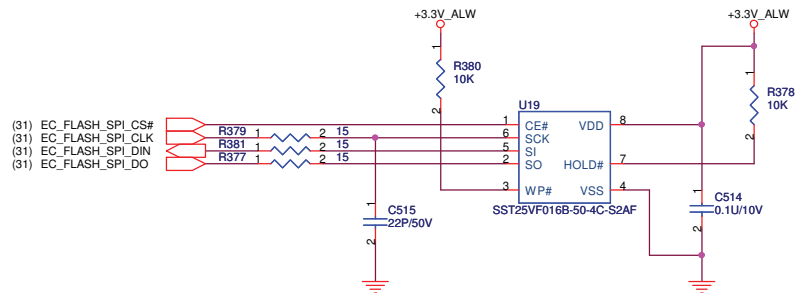


+1.5V\_CARD Max. 650mA, Average 500mA.  
+3V\_CARD Max. 1300mA, Average 1000mA.

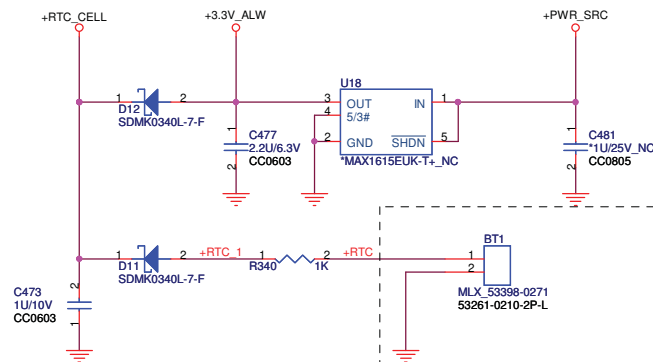




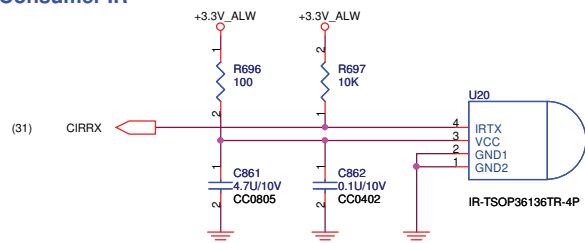
# 16Mbit (2M Byte), SPI



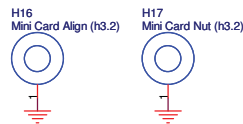
## RTC BATTERY



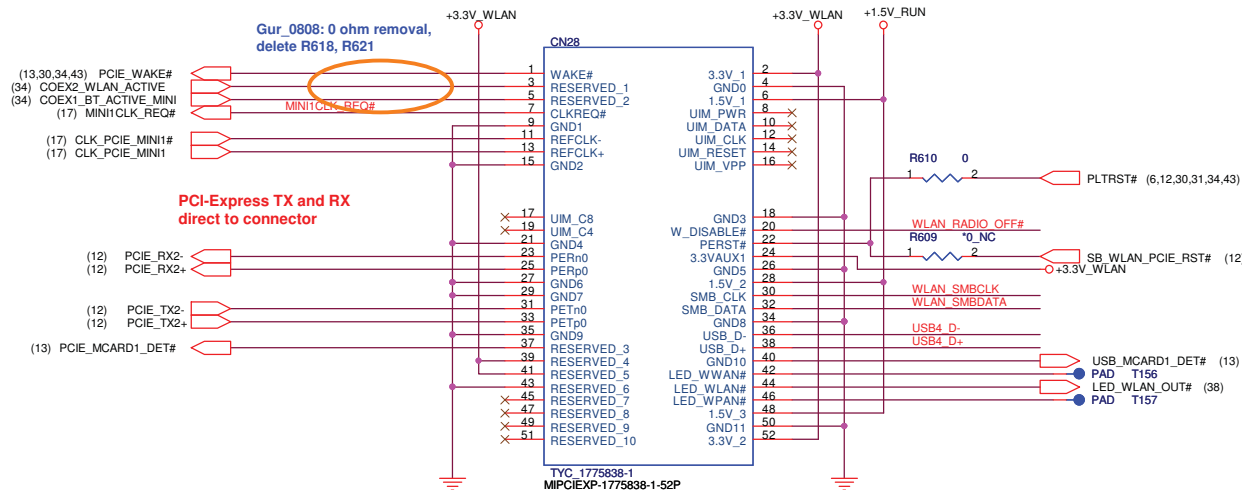
## Consumer IR



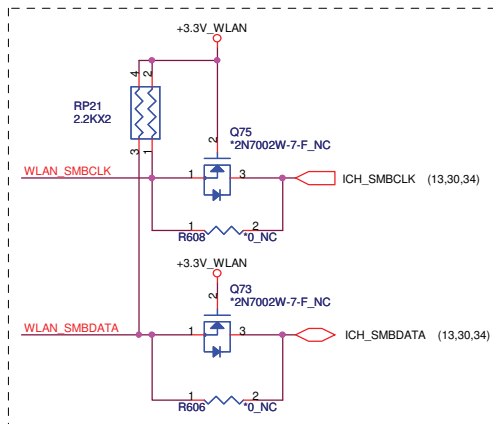
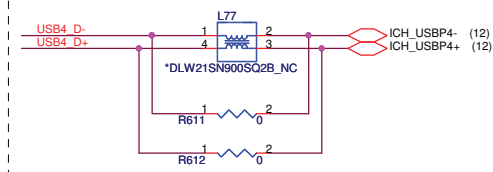
# Mini Card Nut



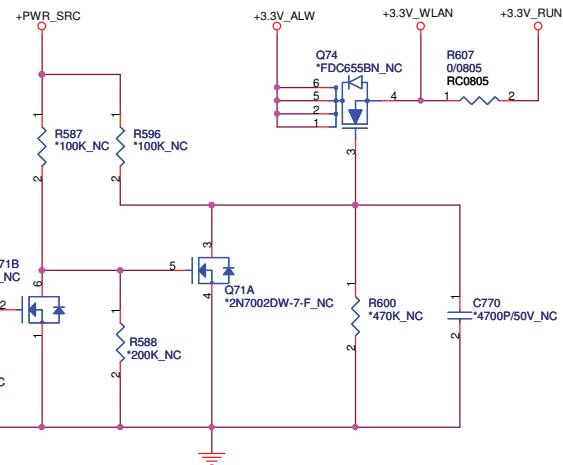
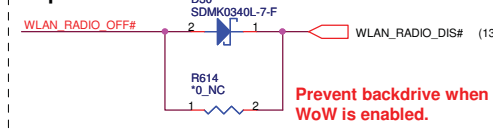
## MiniCard WLAN Connector



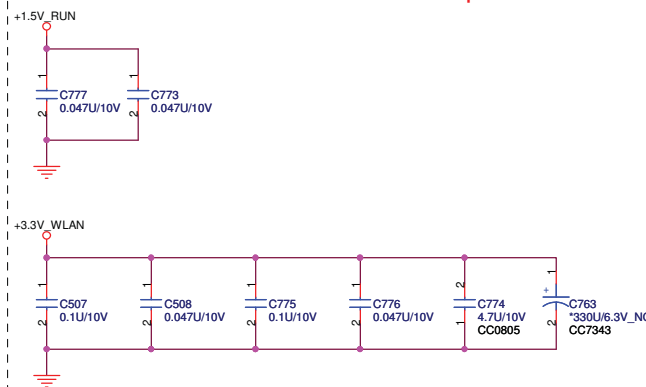
### Reserved PAD for EMI



### Support for WoW

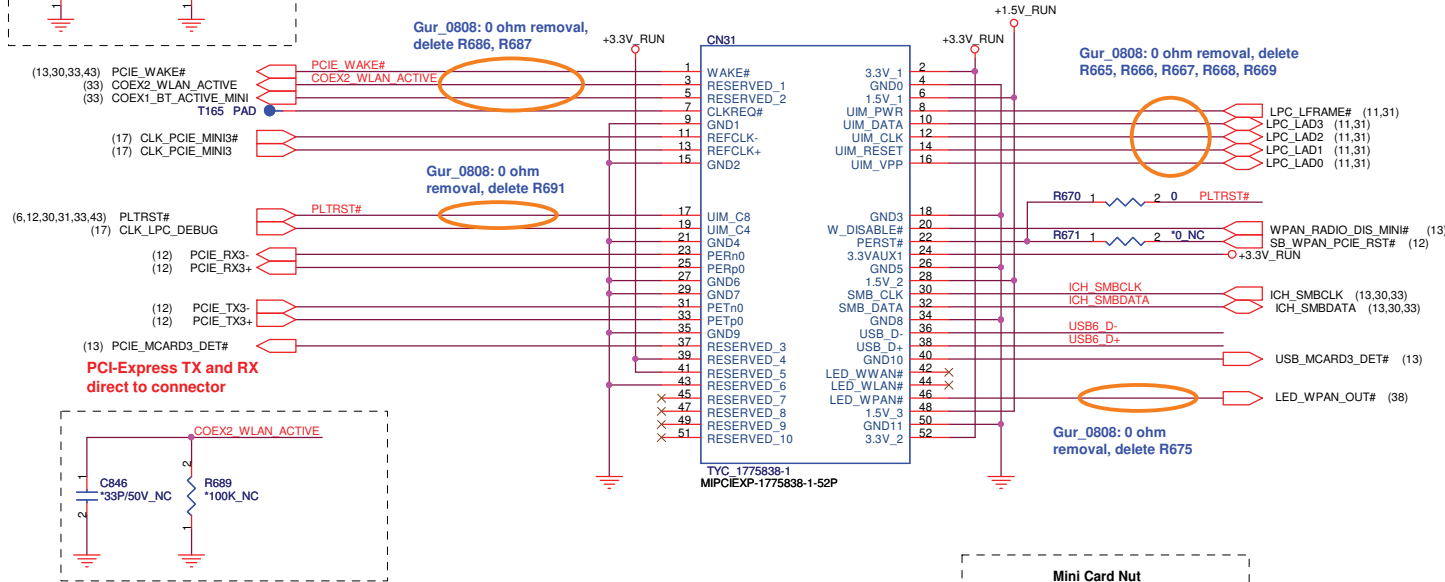
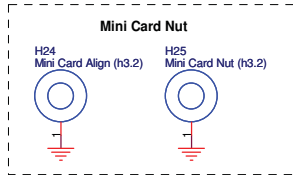


### Place caps close to connector.

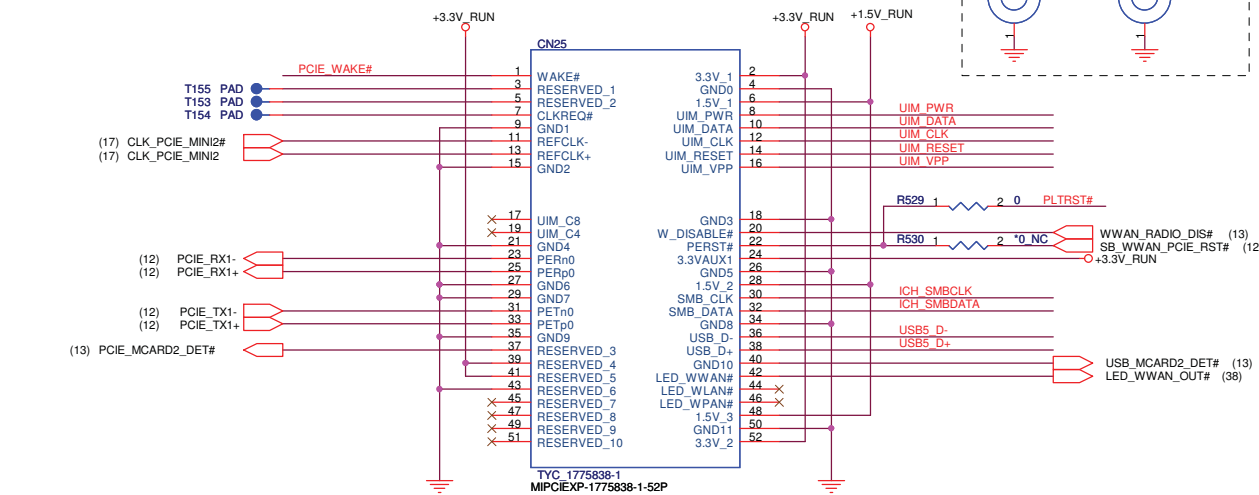
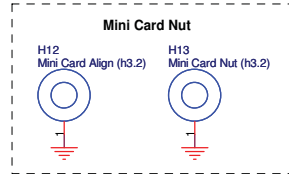


Title MINI-CARD (WLAN)		
Size RM2	Document Number	Rev 3A
Date: Friday, August 08, 2008	Sheet 33	of 59

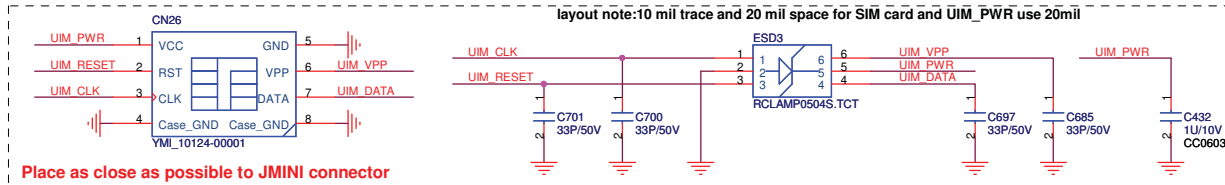
## MiniCard Robson, BT. UWB Connector



## MiniCard WWAN Connector

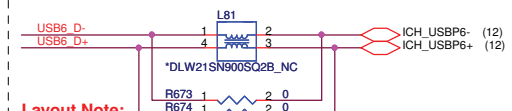


layout note: 10 mil trace and 20 mil space for SIM card and UIM\_PWR use 20mil



Place as close as possible to JMINI connector

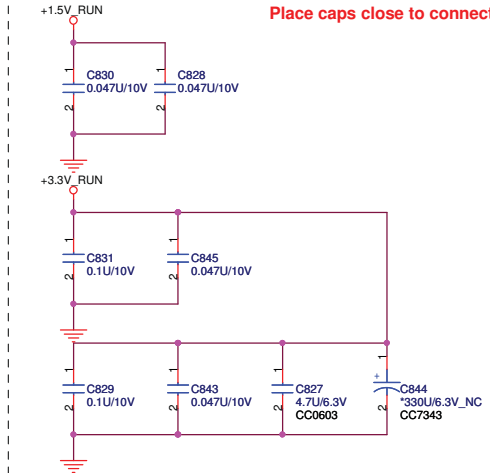
Reserve For EMI



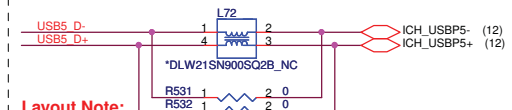
Layout Note:

R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.



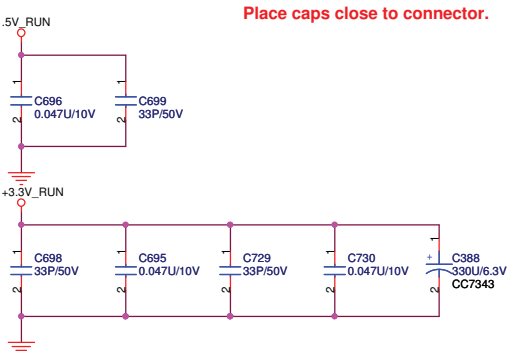
Reserve For EMI



Layout Note:

R240 and R244 close to choke as possible to minimize stubs.

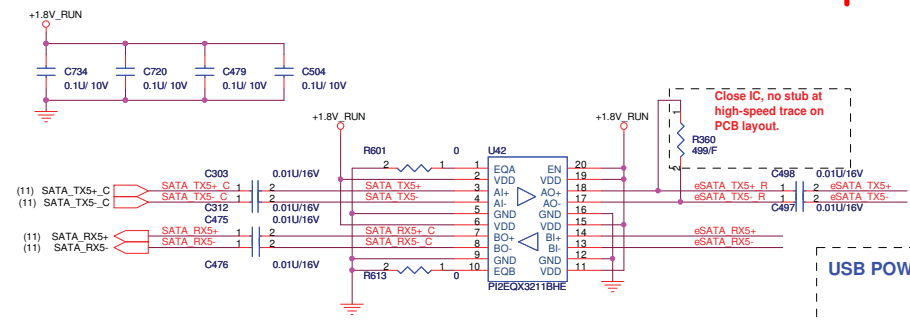
Place caps close to connector.



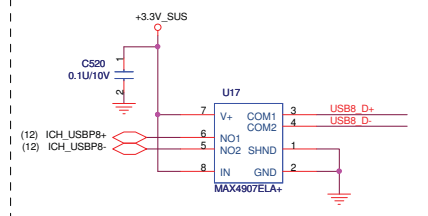
Title		
MINI-CARD (WPAN,WWAN)		
Size	Document Number	Rev
RM2		3A
Date:	Friday, August 08, 2008	Sheet 34 of 59



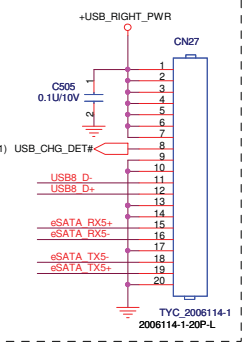
eSATA Re-driver IC



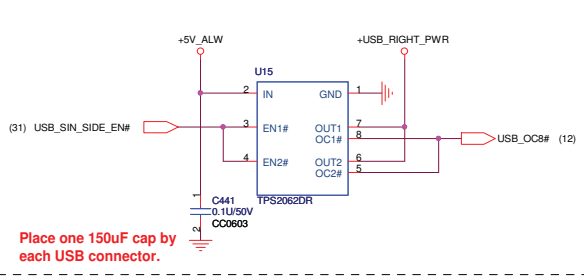
USB BUS SW



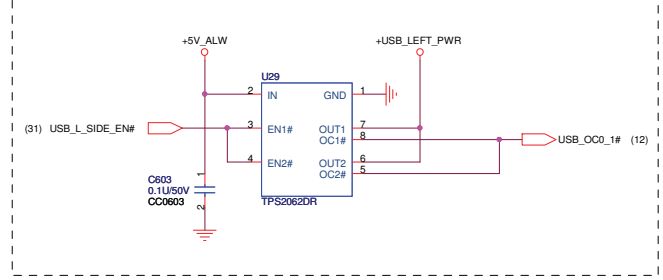
eSATA CONN



USB POWER SW



USB POWER SW





## To Daughter Board connector

Solid White = System On, Normal Activity  
Off= System off (system off or hibernate);  
"Breathing White" = System in Standby (S3);

### Power Button

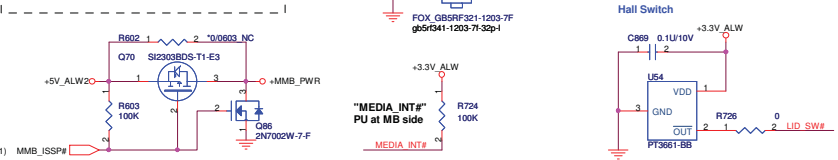
### Speaker

Gur\_0614: change  
R722 to connect to  
R721 from pin1 to pin2

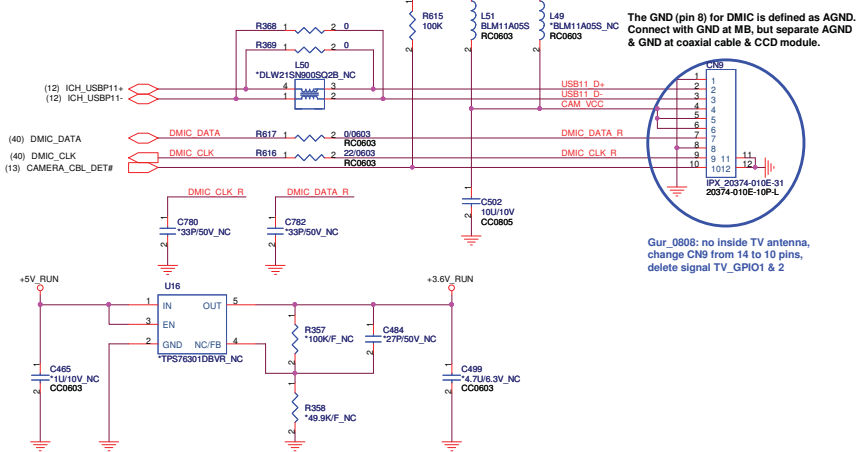
### KB LED

### Touch Pad

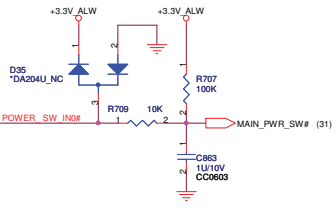
### Media Button



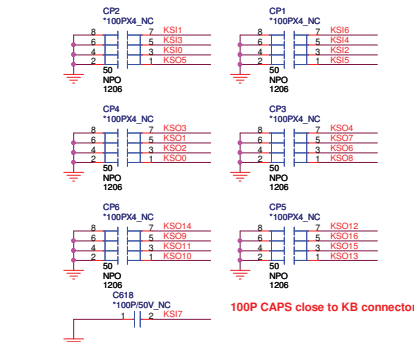
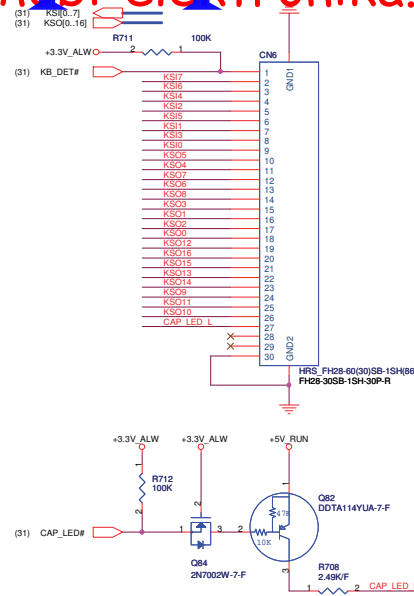
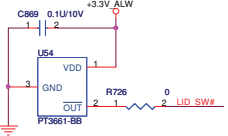
## Array Microphone & Camera



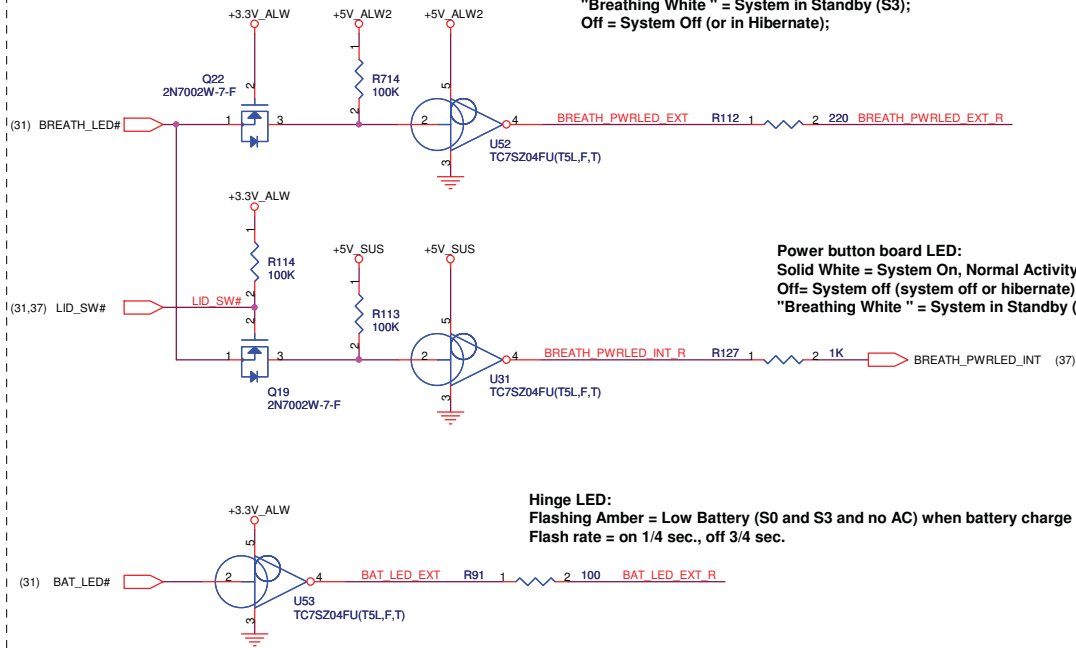
### Power Button



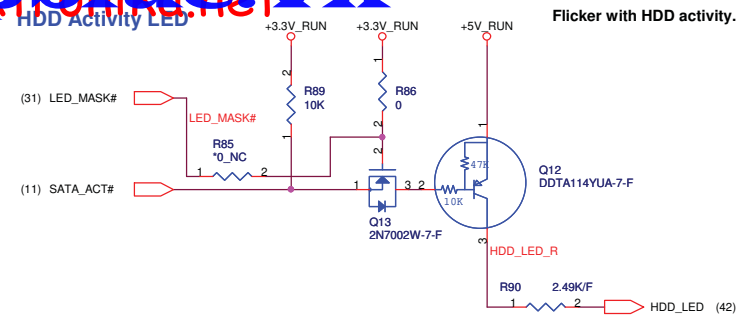
### Hall Switch



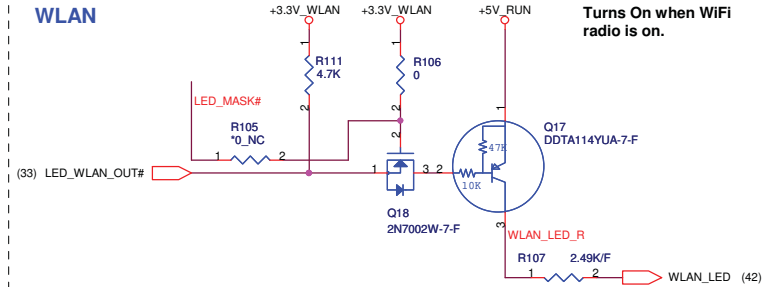
# Hinge & Power Button board LED (PWR/Battery indicator)



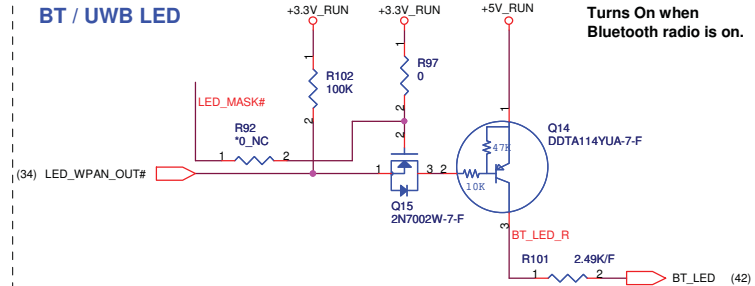
## HDD Activity LED



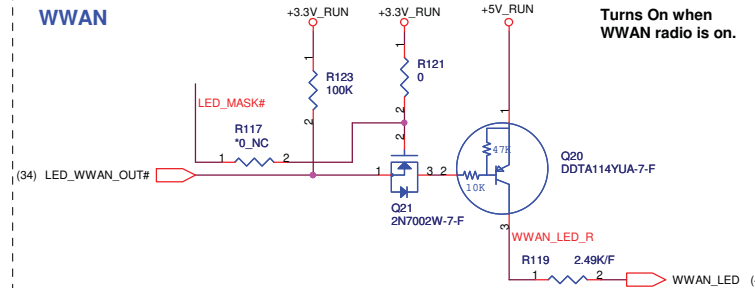
## WLAN



## BT / UWB LED

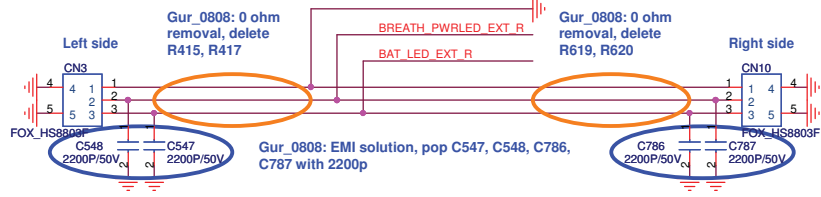


## WWAN



## Hinge LED (PWR/Battery indicator)

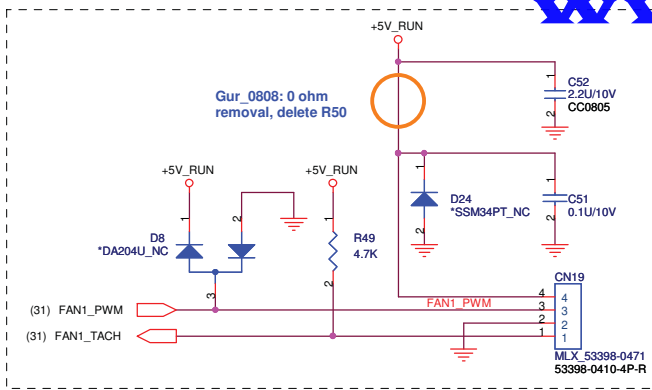
L-C filter (reserve R-C) for EMI



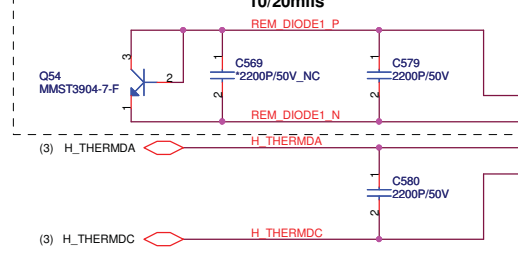
Solid White= System On, Normal Activity  
Solid White= Charging (system on);  
Solid White= Charging (system off or hibernate and battery charge <90%);  
Off= Charging (system off or hibernate and battery charge > 90%);  
"Breathing White" = System in Standby (S3);  
Off = System Off (or in Hibernate);

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%  
Flash rate = on 1/4 sec., off 3/4 sec.

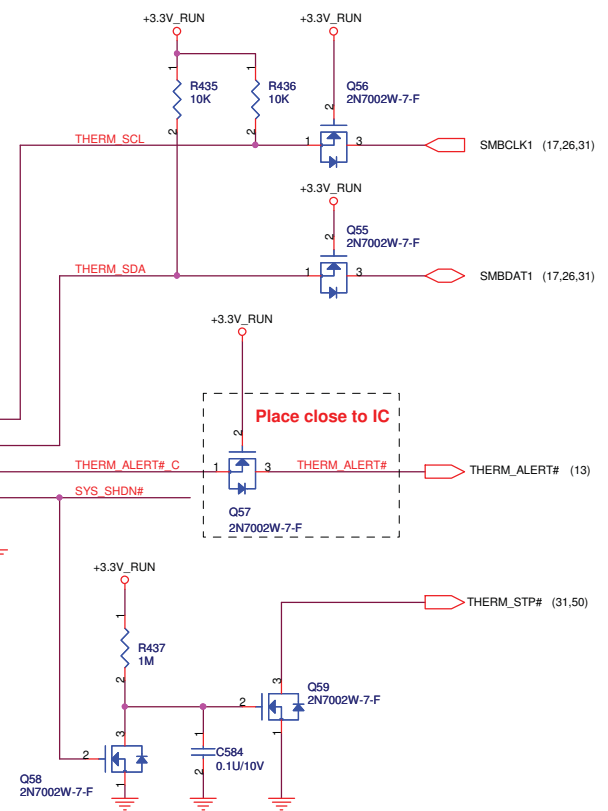
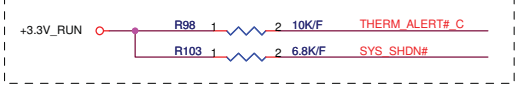


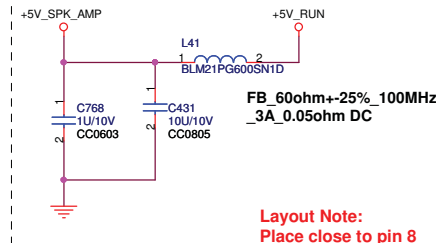
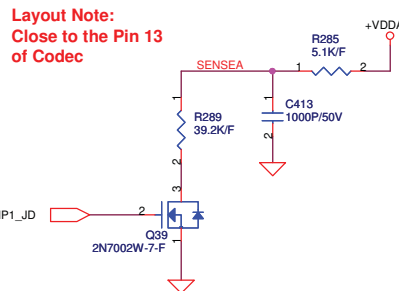
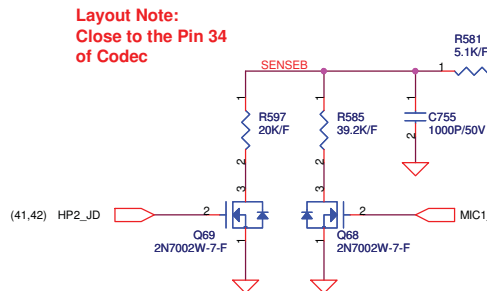


Place these under CPU

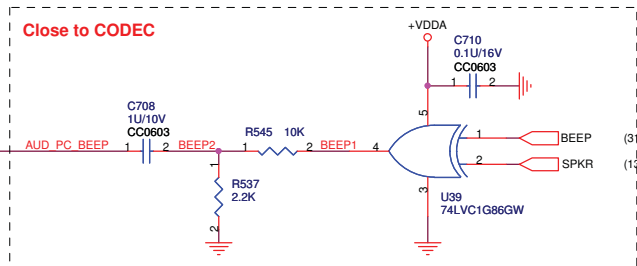
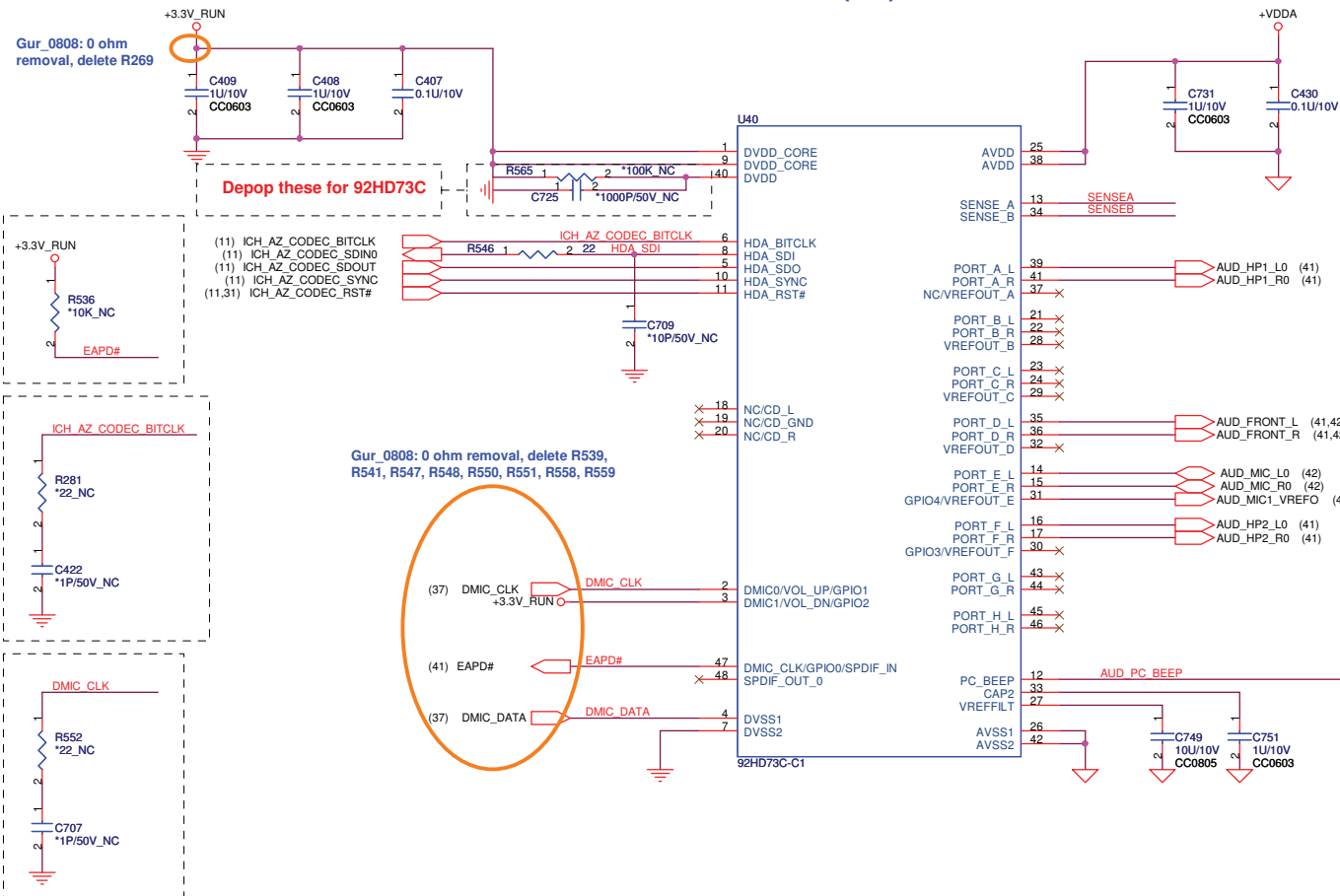


OTP 85 degree C

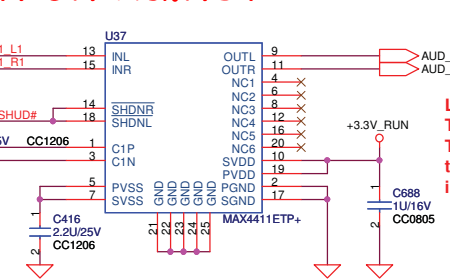
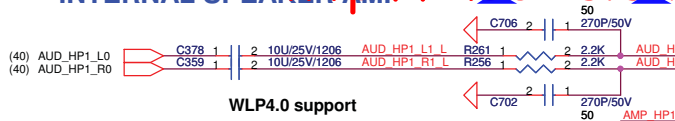
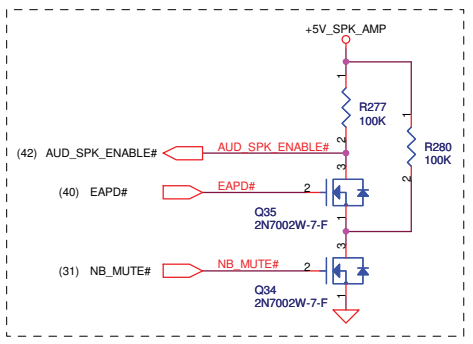




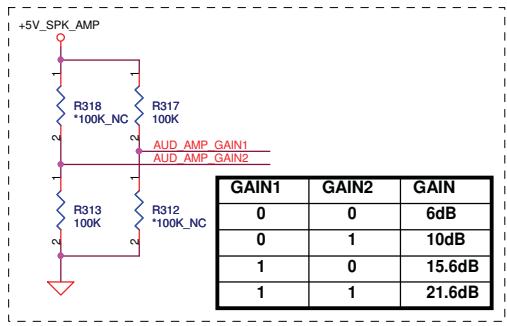
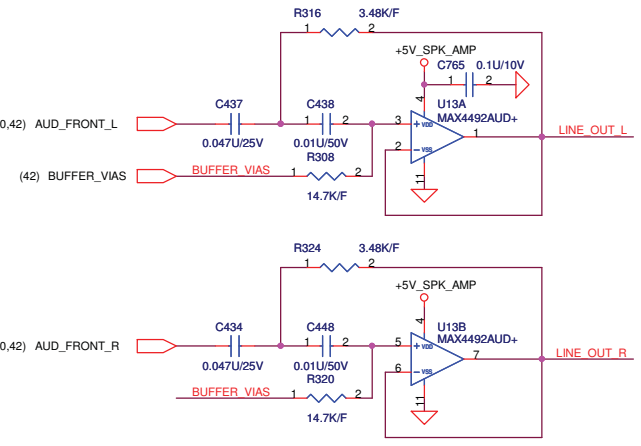
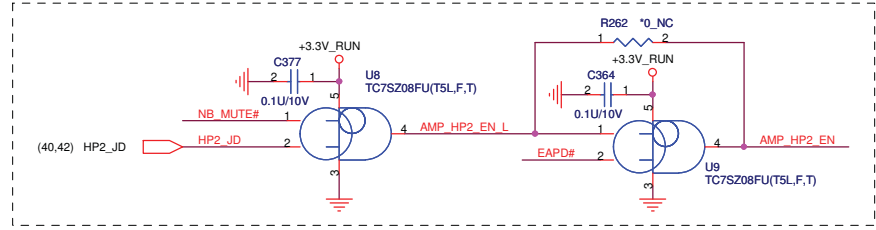
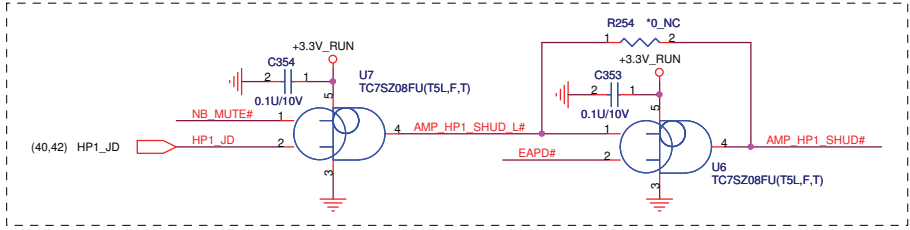
## AZALIA (HD) CODEC



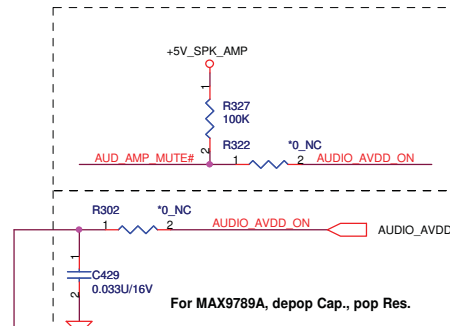




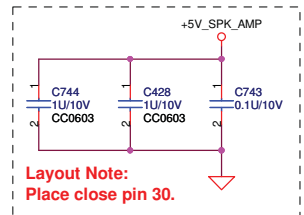
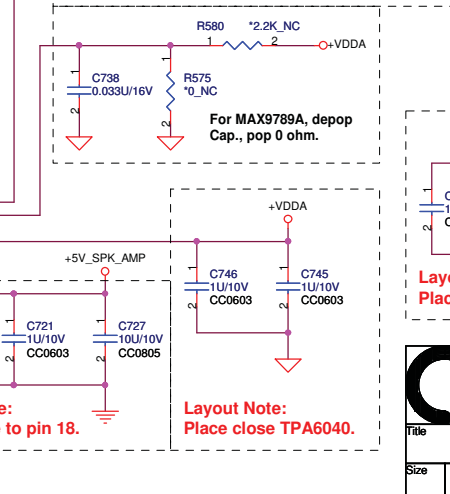
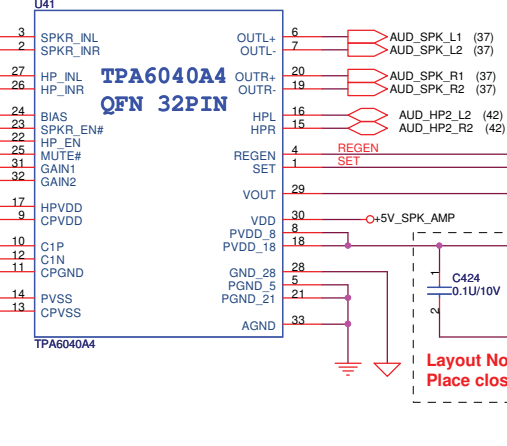
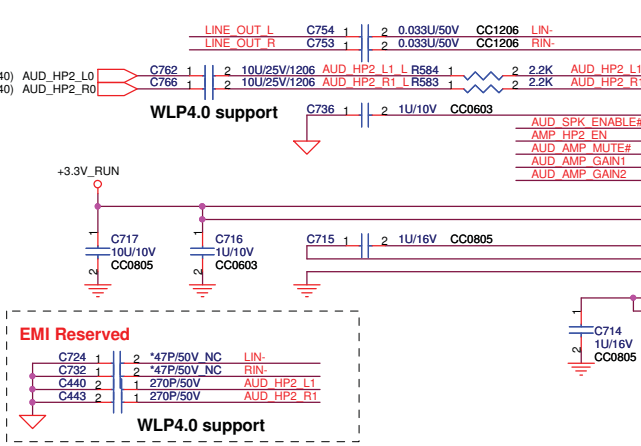
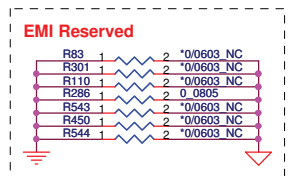
Layout Note:  
TPA 4411 : cannot connect EP to GND.  
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



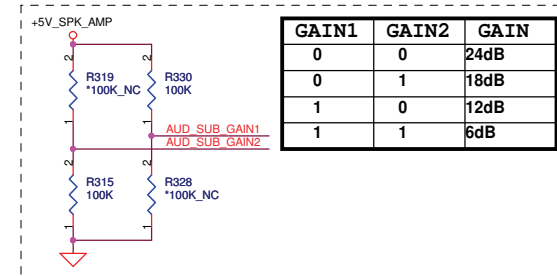
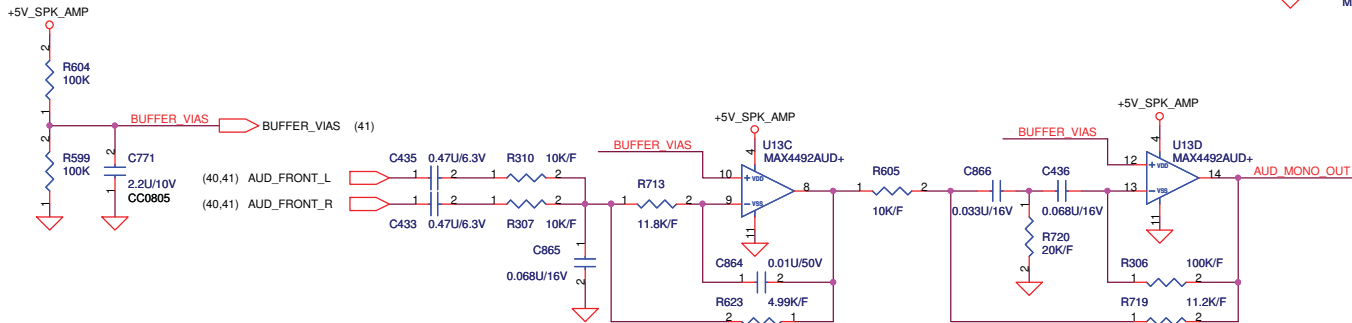
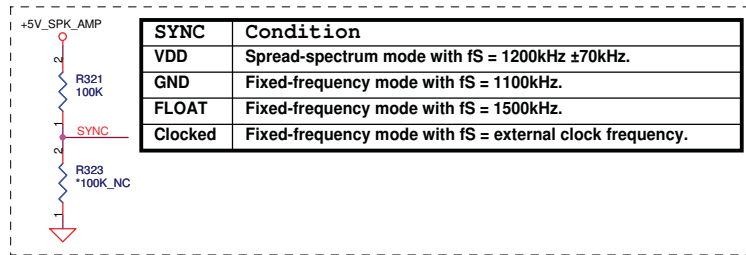
Layout Note:  
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.  
TPA 4411 : cannot connect EP to GND.  
MAX 4411 : can connect EP to GND.



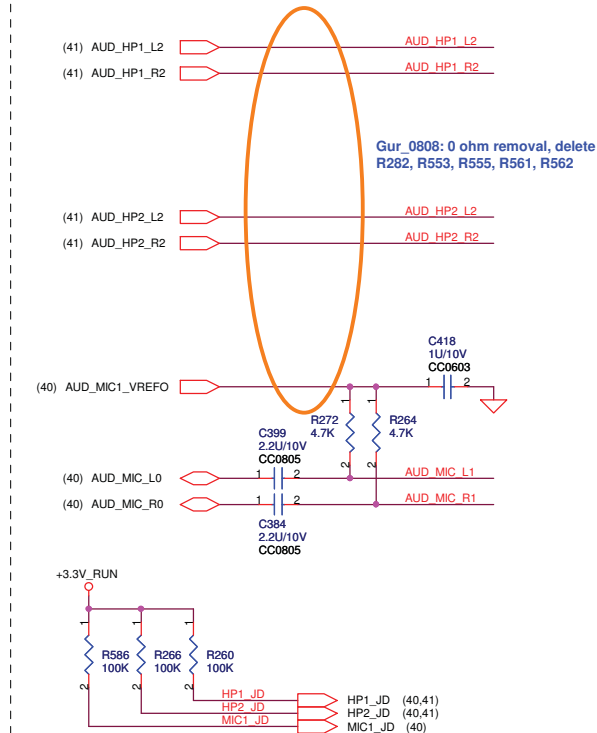
Layout Note:  
Place close pin 30.



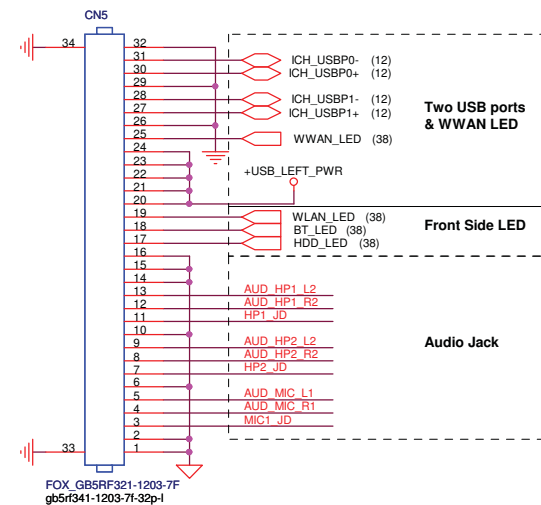
## INTERNAL SUBWOOFER AMP



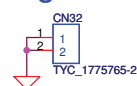
## Ambient Parts of Headphone & MIC Jack



## To IB(IO Board) connector



## Adding additional AGND



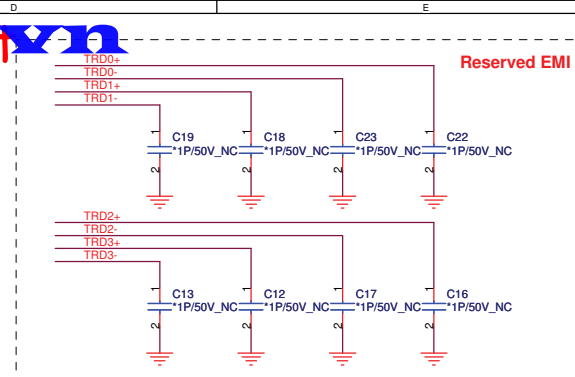
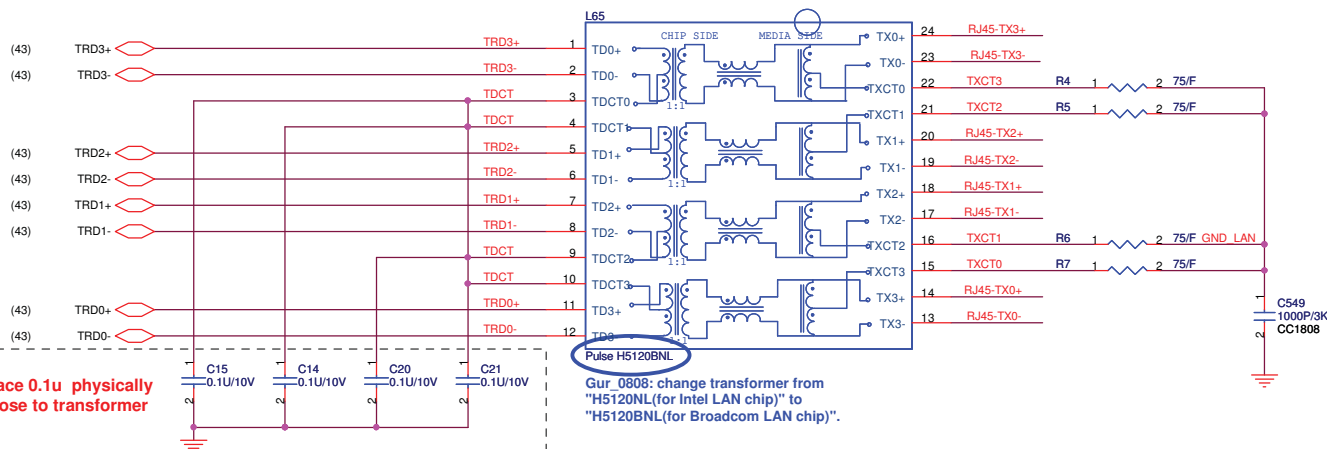
Title			IB CONN & SUBWOOFER
Size	Document Number	Rev	
	RM2	3A	
Date:	Friday, August 08, 2008	Sheet	42 of 59



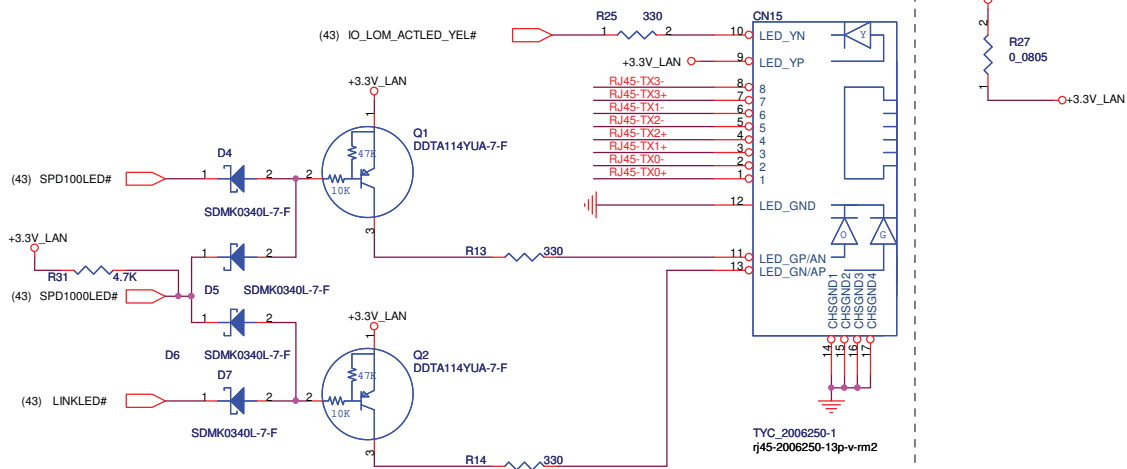
Note:thermal pad

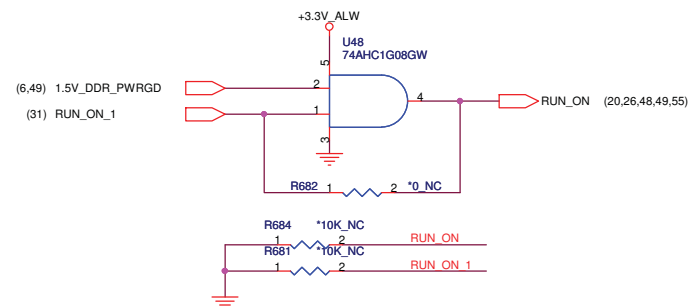
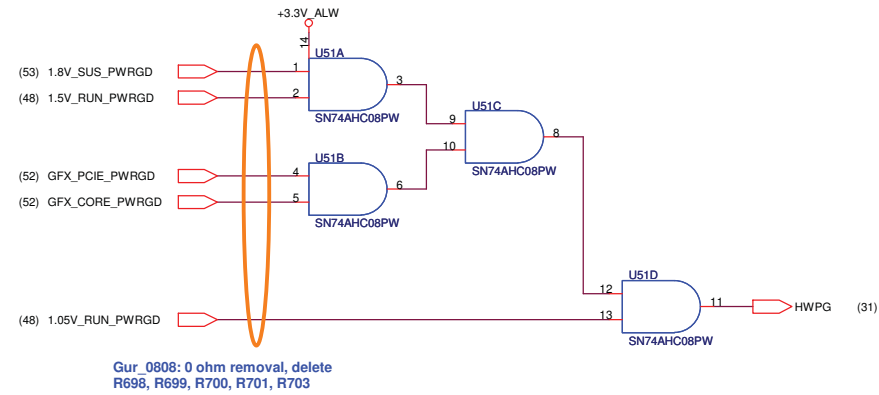
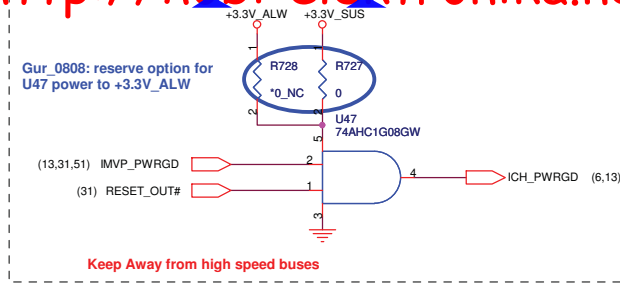
## TRANSFORMER

**Layout Note:**  
Route TRD+/- pairs with 100 ohm differential trace impedance.

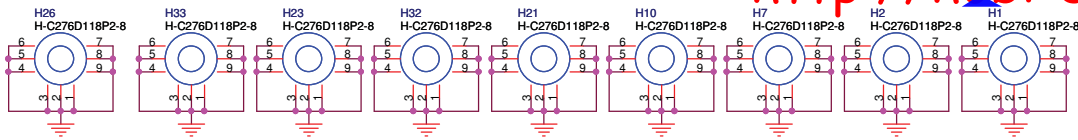


## RJ-45 Connector

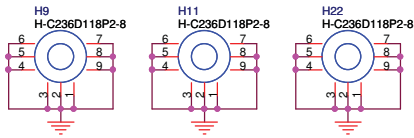




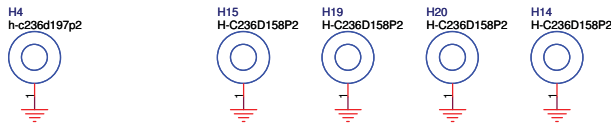
H-C276D118P2-8 \* 9



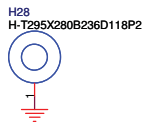
H-C236D118P2-8 \* 3



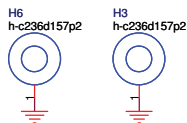
h-c236d197p2 \* 1



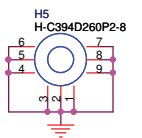
H-T295X280B236D118P2 \* 1



h-c236d157p2 \* 2



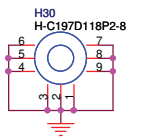
h-c394d260p2 \* 1



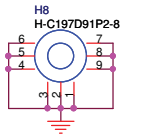
h-c236d236n \* 2



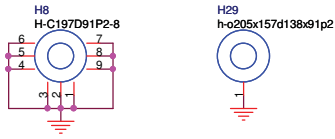
H-C197D118P2-8 \* 1



H-C197D91P2-8 \* 1

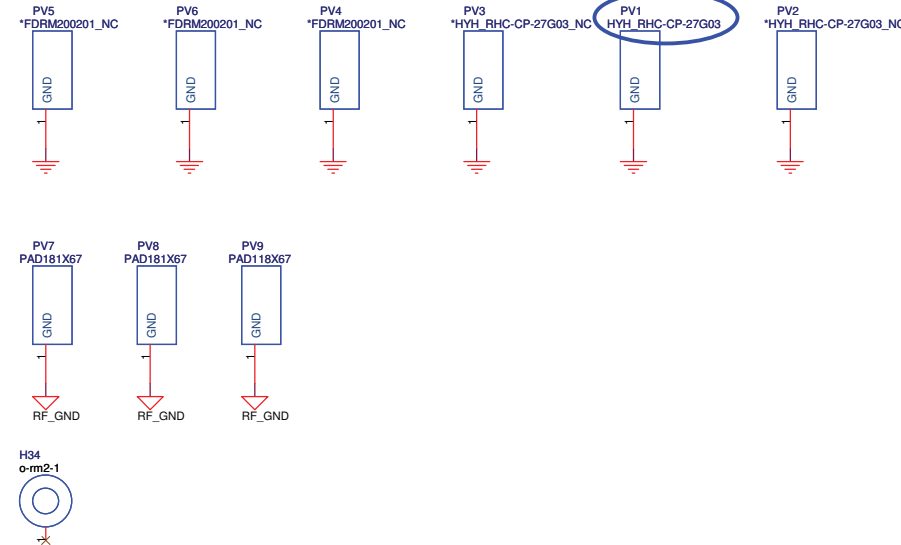


h-o205x157d138x91p2 \* 1



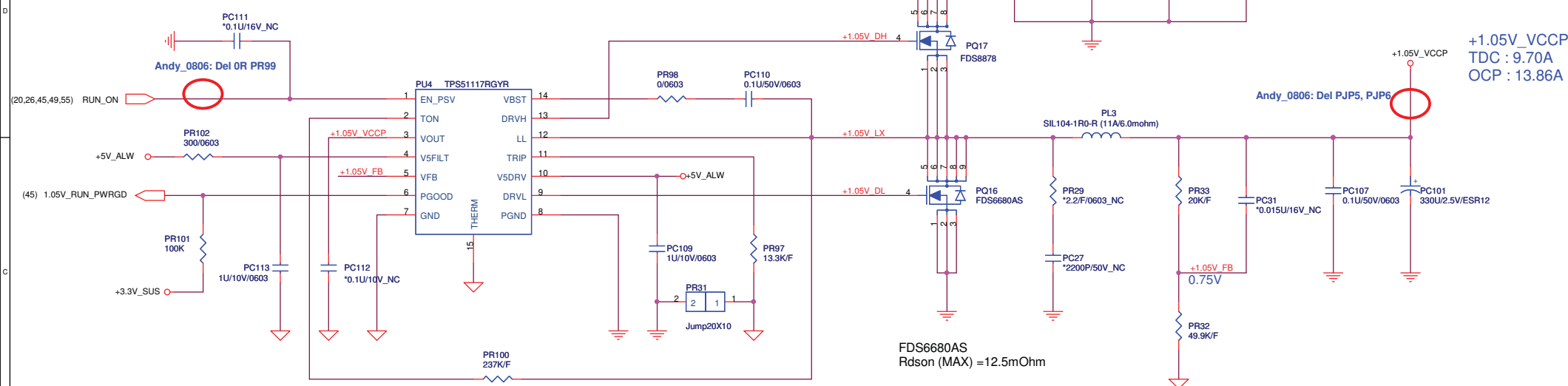
www.Laptopblue.vn

Gur\_0808: change PV1 from  
FDZD3002010 to FDEF3001015



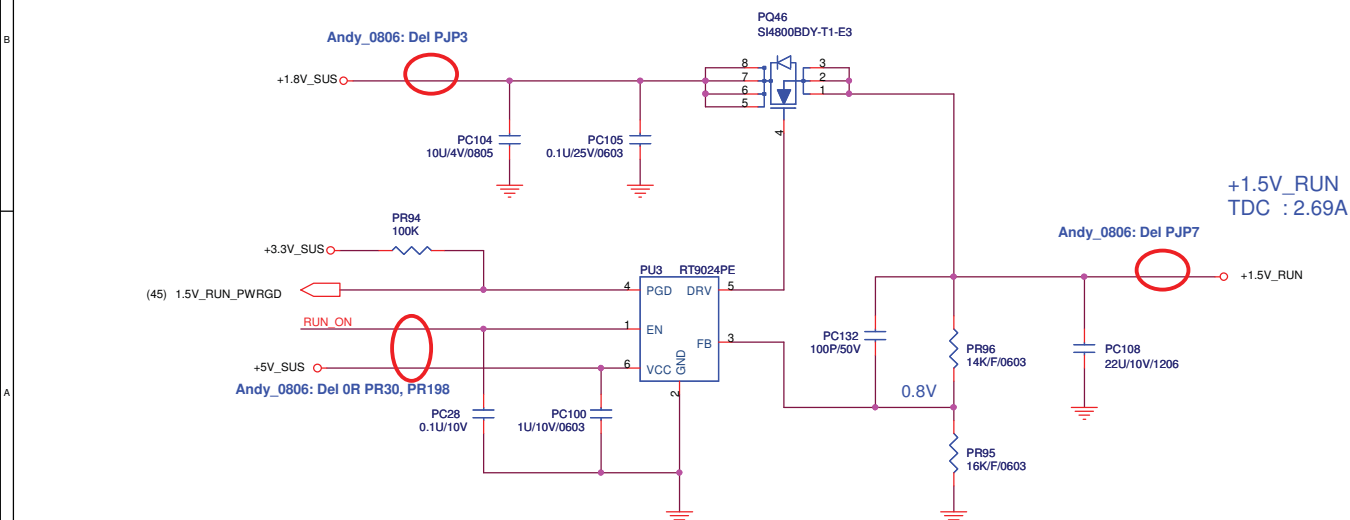




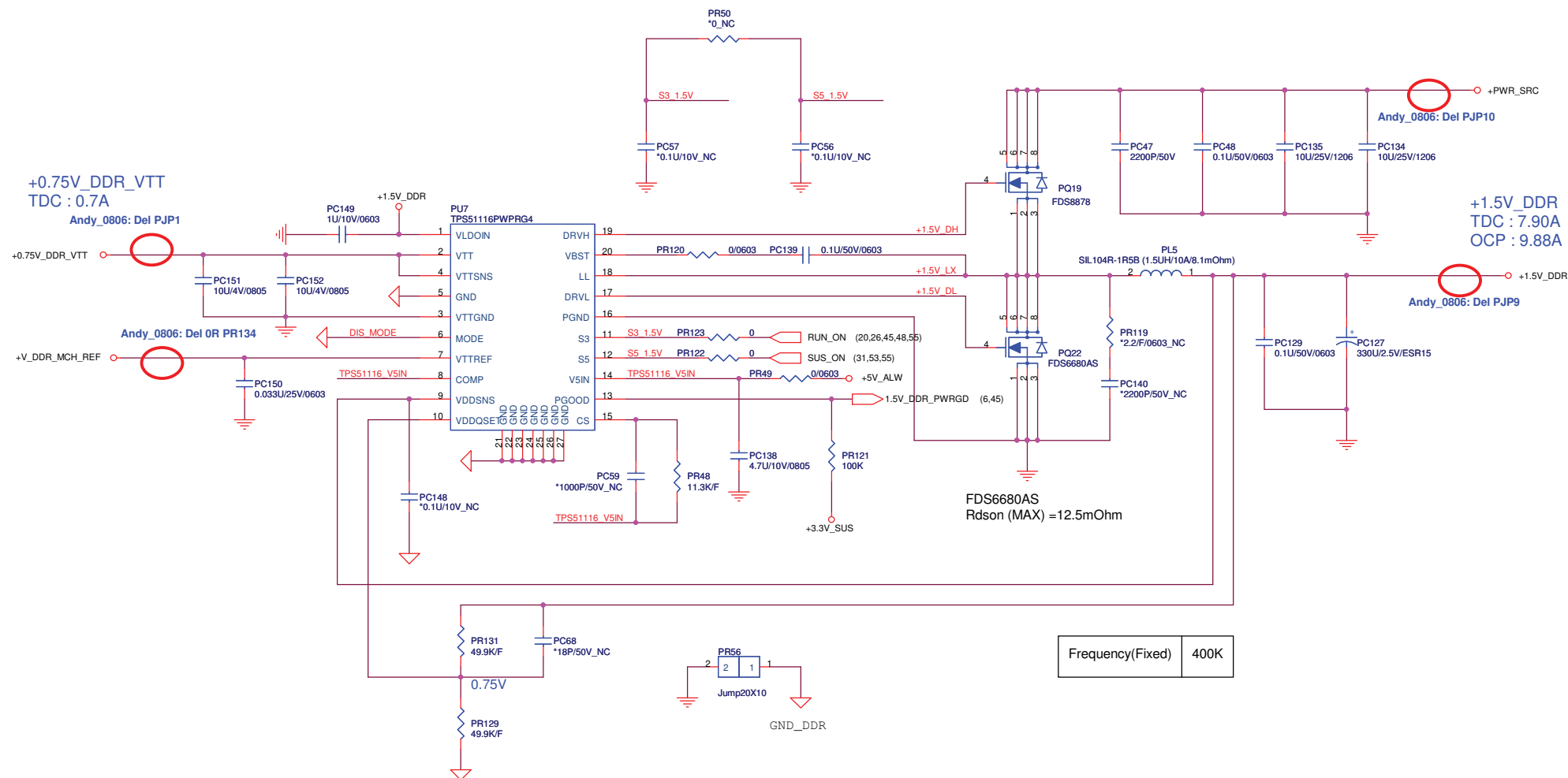


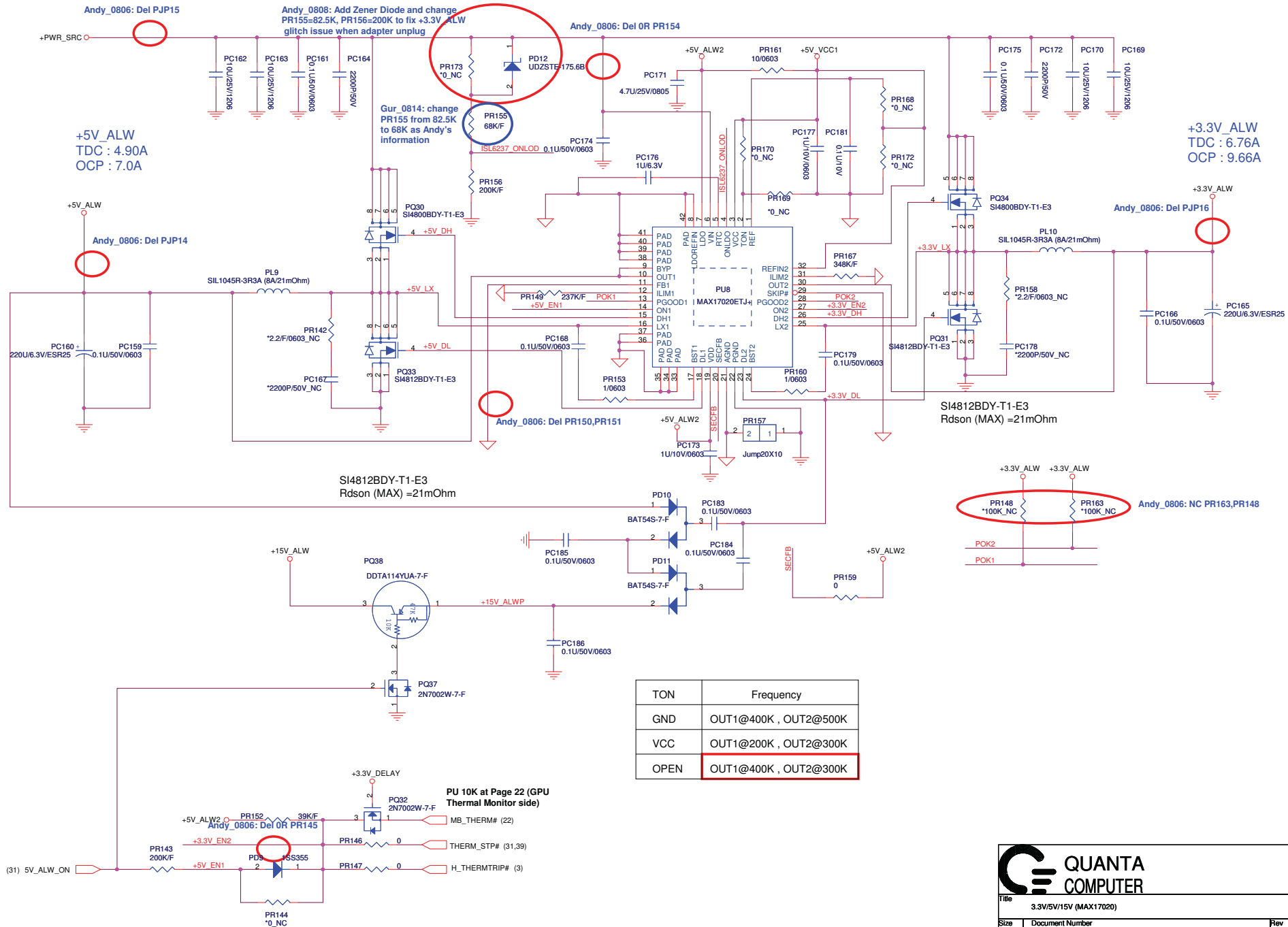
TON	PR3=237K
Frequency	300K

FDS6680AS  
Rdson (MAX) =12.5mOhm

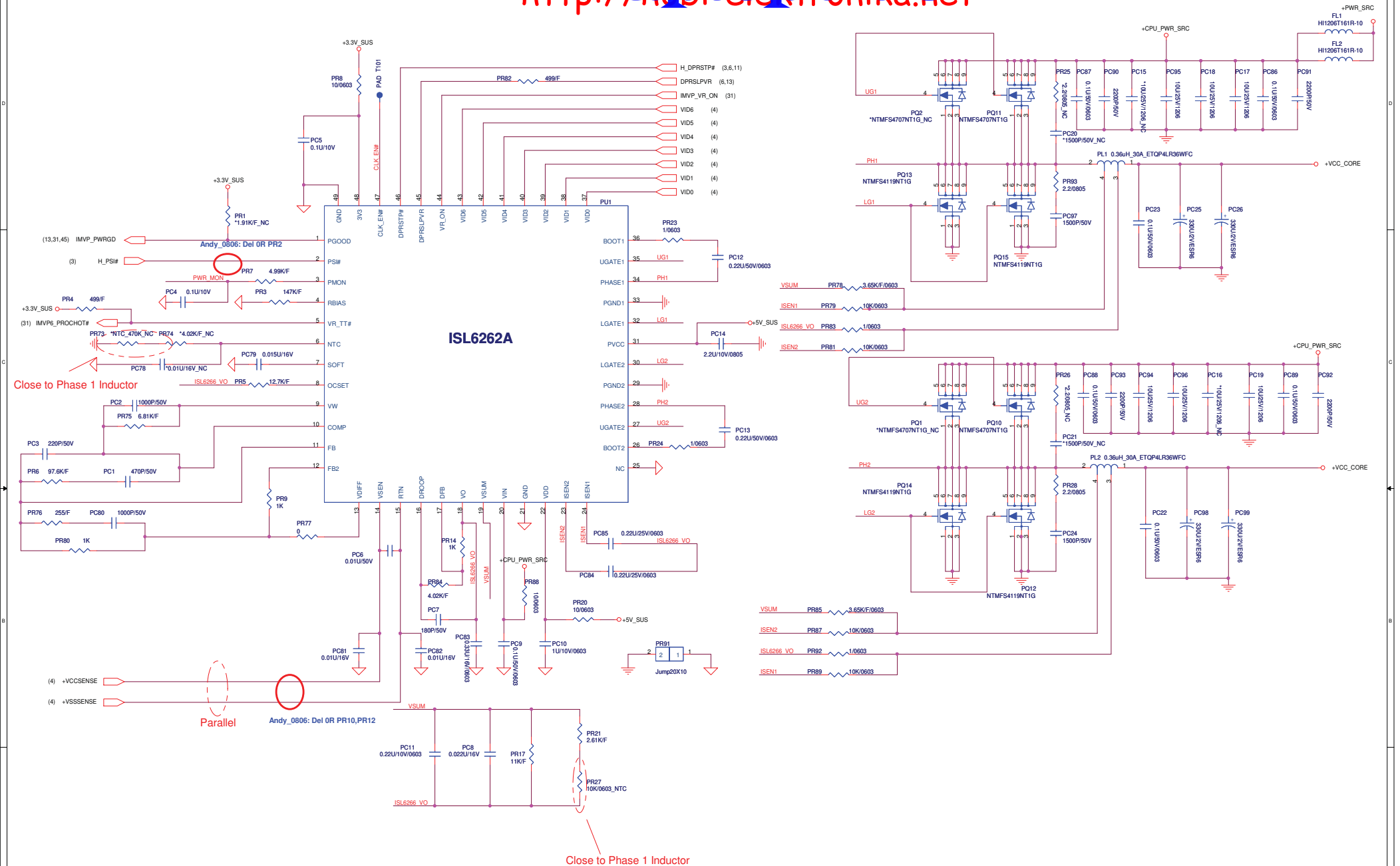


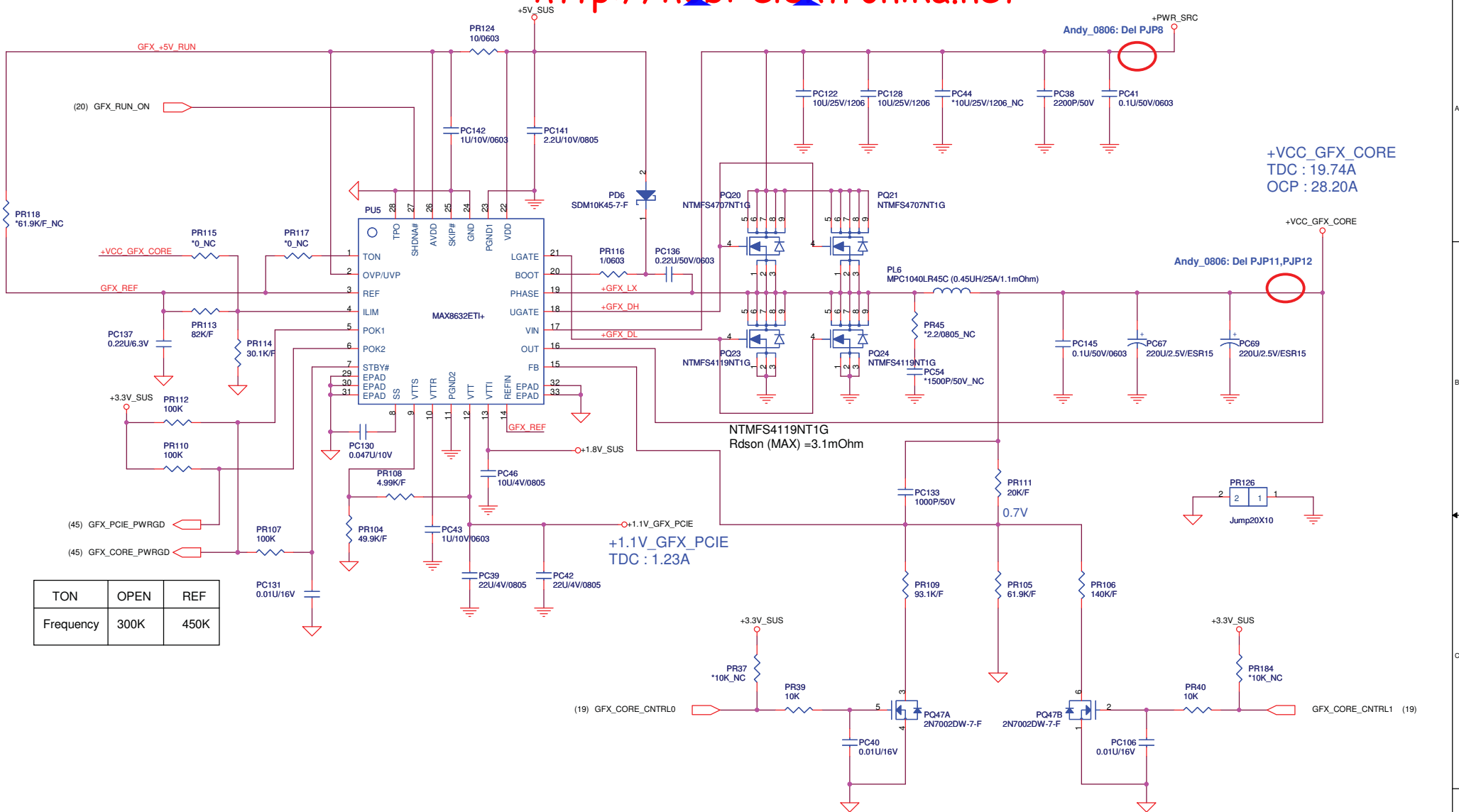
Title 1.05VCCP & 1.5VRUN		
Size RM2	Document Number	Rev 3A
Date Thursday, August 07, 2008	Sheet 48	of 59





TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K



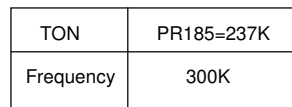


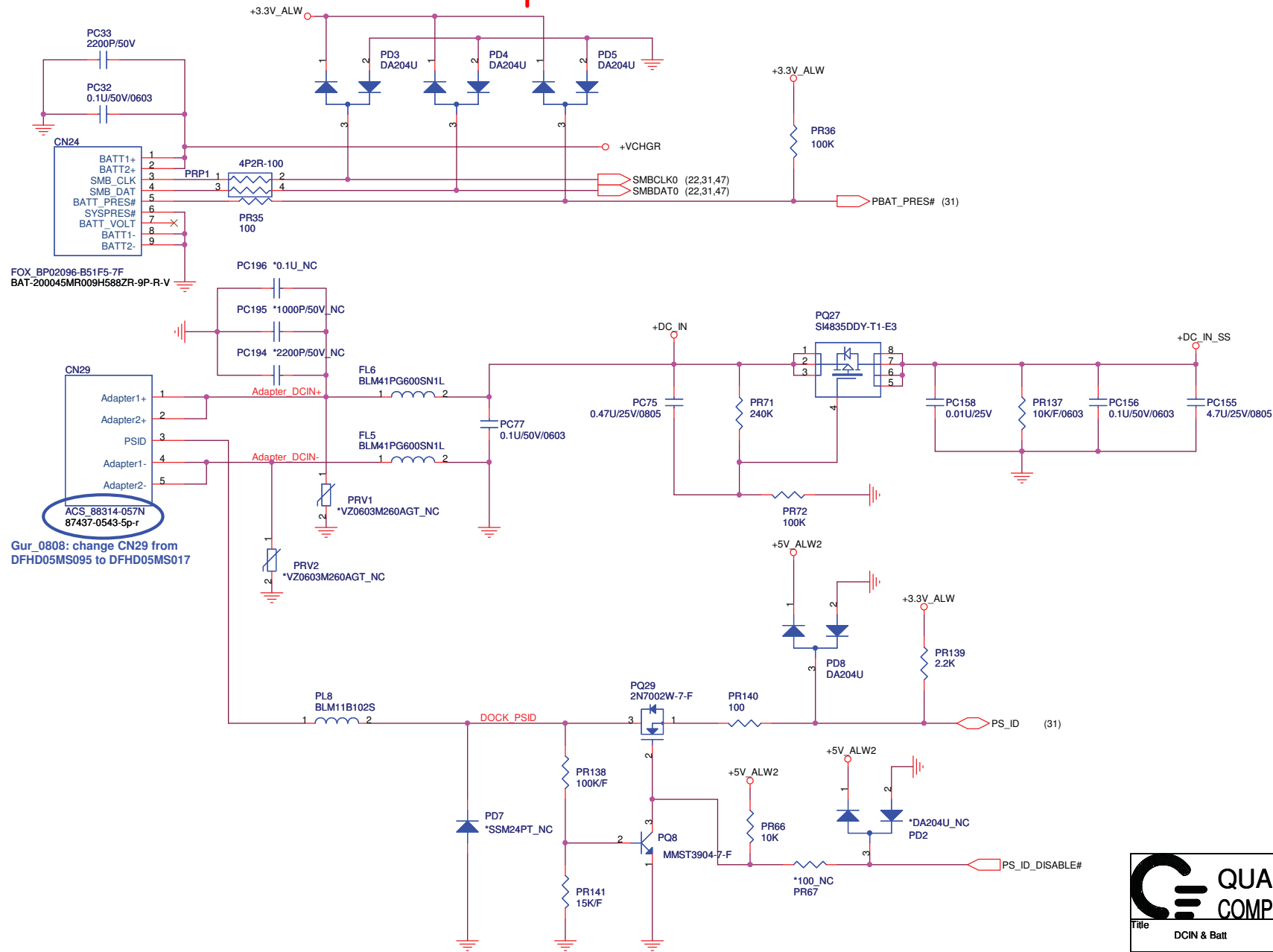
TON	OPEN	REF
Frequency	300K	450K

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.95
HIGH	LOW	1.1V
HIGH	HIGH	1.2V

ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.





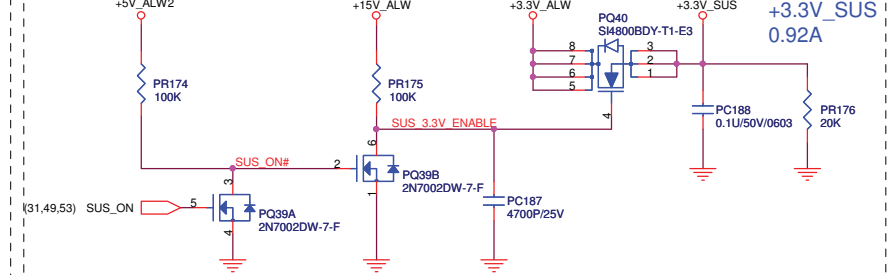
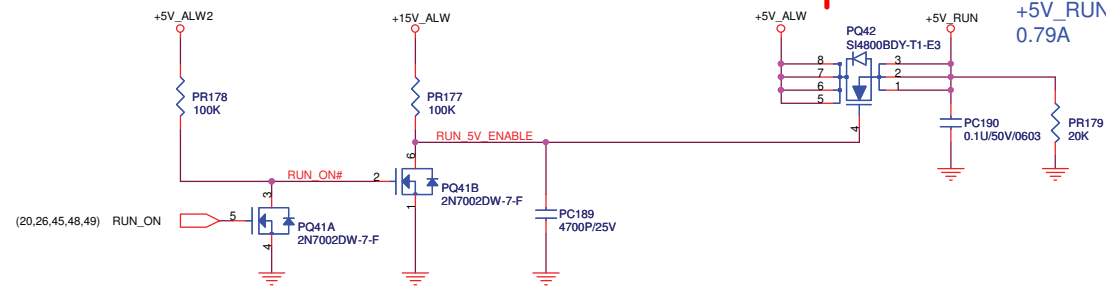


FOX\_BP02096-B51F5-7F  
BAT-200045MR009H588ZR-9P-R-V

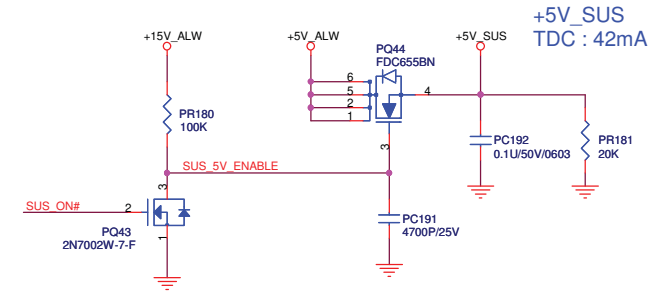
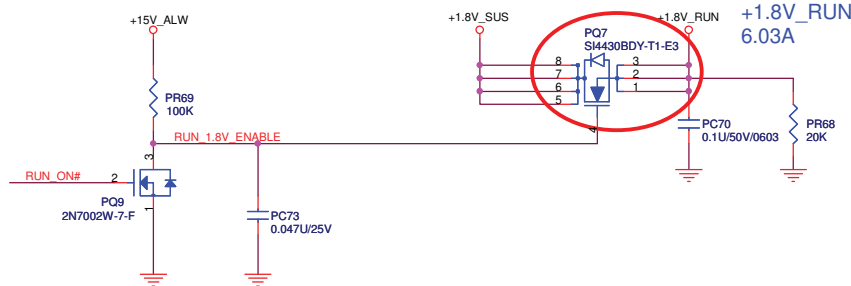
CN29  
Adapter1+  
Adapter2+  
PSID  
Adapter1-  
Adapter2-  
ACS\_88314-057N  
87437-0543-5p-r

Gur\_0808: change CN29 from  
DFHD05MS095 to DFHD05MS017

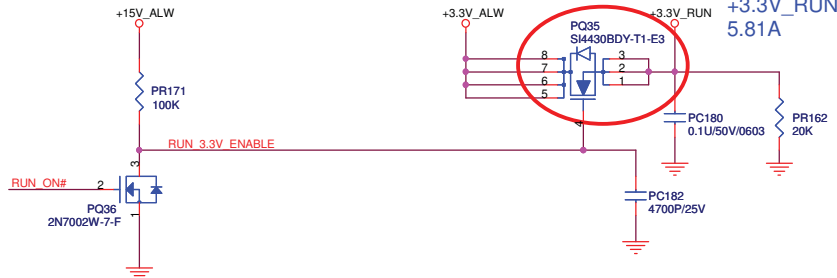
Title		
DCIN & Batt		
Size	Document Number	Rev
RM2		3A
Date:	Friday, August 08, 2008	Sheet 54 of 59



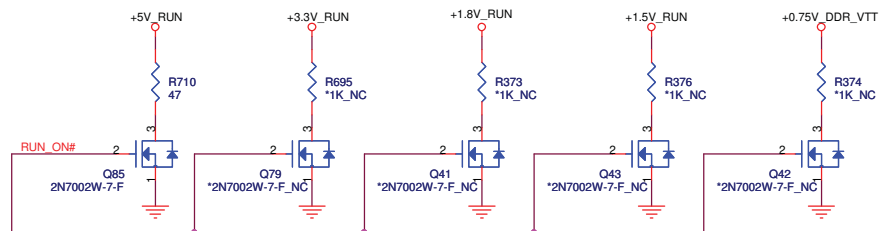
Andy\_0807: Change to SI4430BDY-T1-E3  
due to SI4336DY-T1-E3 EOL



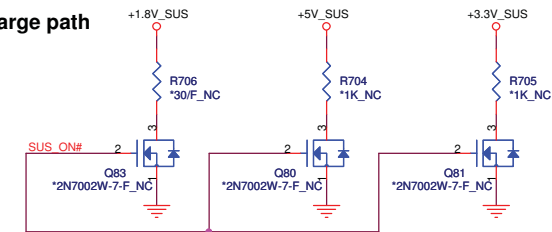
Andy\_0807: Change to SI4430BDY-T1-E3  
due to SI4336DY-T1-E3 EOL

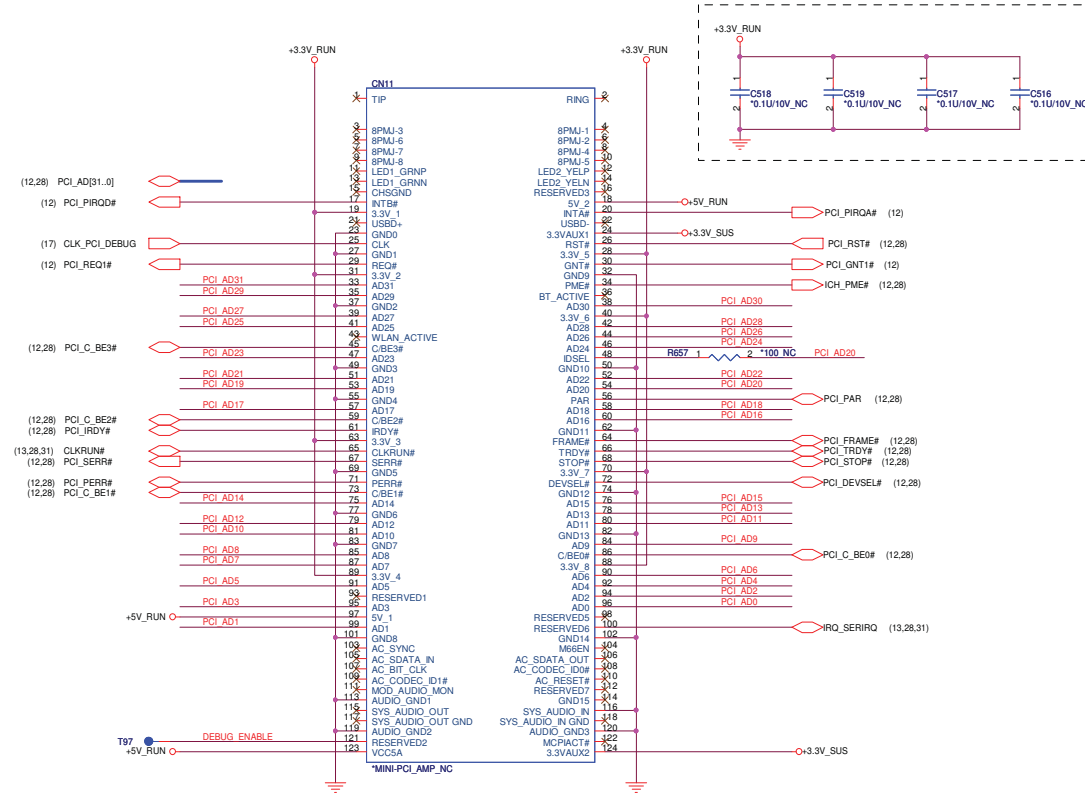


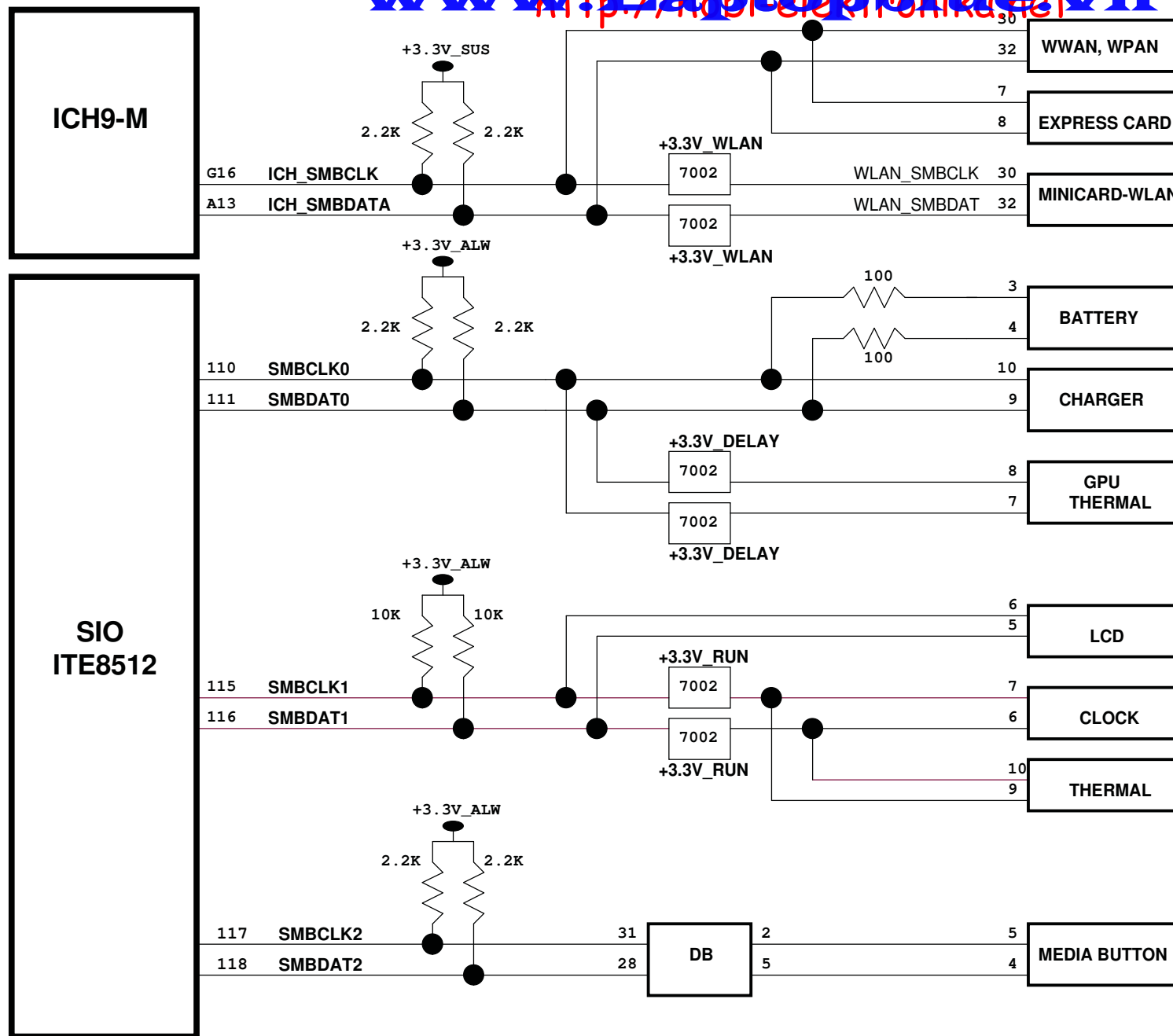
### Reserve discharge path



### Reserve discharge path







## POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

## PM TABLE

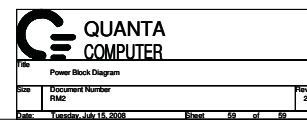
State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

## PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD23	REQ#0 / GNT#0	PIRQB: 1394 PIEQC: Card reader

ICH9-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair bottom / left
	2	Reserved
	3	Reserved
	4	WLAN
	5	Mini Card (WWAN)
	6	Mini Card (WPAN)
	7	Express Card
	8	USB W/ E-SATA port
	9	TV
	10	Reserved
ECE 5011	11	Camera
	1	None
	2	None
	3	None
ECE 5011	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	LOM






E			
Page	Model	RM2 MB with MV	
		FROM	TO
1	2A		
2	2A		
3	2A		
4	2A		
5	2A		
6	2A		
7	2A		
8	2A		
9	2A		
10	2A		
11	2A		
12	2A		
13	2A		
14	2A		
15	2A		
16	2A		
17	2A		
18	2A		
19	2A		
20	2A		
21	2A		
22	2A		
23	2A		
24	2A		
25	2A		
26	2A		
27	2A		
28	2A		
29	2A		
30	2A		
31	2A		
32	2A		
33	2A		
34	2A		
35	2A		
36	2A		
37	2A		
38	2A		
39	2A		
40	2A		
41	2A		
42	2A		
43	2A		
44	2A		
45	2A		
46	2A		
47	2A		
48	2A		
49	2A		
50	2A		
51	2A		
52	2A		
53	2A		
54	2A		
55	2A		
56	2A		
57	2A		
58	2A		
59	2A		

1      OF      4



MODEL		REV	DATE	DESCRIPTION	Page	Model	RM2 MB with MV	
							FROM	TO
RM2 MB with MV	Pre	2008/04/16	P17, remove bead of BSEL0 & 2 for layout space concern	1	2E			
		2008/04/17	P1, update Block Diagram	2	2A			
			P29, update library of CON1 to delete pin 48 & 49 (to GND)	3	2D			
			P51 (alter rename), pop PQ10 & PQ11, depop PQ1 & PQ2	4	2B			
			Rename	5	2D			
	2008/04/18	P48, update power circuit as "RM2MB_M86_A1A_0417 FOR 512MB_1.DSN" P31, BOM change for RP23 from "CJ310042N02" to "CJ310042N11" P32, delete RTC battery "UBM2" for assembly process change	6	2D				
	2A(PT)	2008/04/18	First Release pages, change revision form 1A to 2A for RM2 start from PT stage P44, change footprint of RJ45 from "rj45-2006250-13p-v-rm2" to "rj45-2006250-13p-h-rm2."	7	2D			
	2B(PT)	2008/04/23	P01, change Ver. from 2A to 2B; adding Dell PWA, PWB, SCH P/N P26, delete Pin 57, 58 of CN4 for new footprint Update for AMD PowerPlay P52, update power circuit as "RM2MB_M86_A1A_0418A FOR 512MB_1.DSN" P19, pop R287 and separate "GFX_CORE_CNTRL" to "GFX_CORE_CNTRL0" & "GFX_CORE_CNTRL1"	8	2D			
		2008/04/24	P48, update power circuit as "RM2MB_M86_B2B_0423 FOR 512MB_1.DSN" P20, change reserved U10 from "74AHCT1G08GW" to "74AHCT1G08GW" for logic power level issue	9	2D			
		2008/04/28	P4, pop C558 & depop C562 for mechanical interference concern	10	2D			
2008/05/02		Badge LED don't light enough issue P38, change R112 from 100K (CS41002JB20) to 220 (CS12202JB24) ; change R91 from 100K (CS41002JB20) to 150 (CS11502JB22) ; change R416 & R418 from 220 (CS12202JB24) to 0 ohm (CS00002JB38)	11	2D				
2C(PT)	2008/05/14	P1, change ver. from 2B to 2C P14, change L15 from "CV-1008MZ14" to "CV-1001TN09" P38, delete bypass Res. of eSATA MMB ISSP backdrive issue P37, reserve a MOS for +MMB_PWR backdrive when ISSP LAN 10M & 100M LED reversed and LAN footprint update P46, exchchange CN15 pin 11 & 13 for LAN 10M & 100M LED reversed; change RJ45 footprint from "rj45-2006250-13p-h-rm2" to "rj45-2006250-13p-v-rm2."	12	2D				
	2008/05/29	P44, change H14, H15, H19, H20 from "h-c236d197p2" to "H-C236D158P2"; change from "h-tc197bc236d118p2" to "H-T295X280B236D118P2"; change H30 from "h-c157d157n" to "H-C197D118P2" for IB cable cost down from coaxial to FFC type P42, change CN5 from 30 to 32 pin for cable cost down from coaxial to FFC type	13	2E				
		2008/06/16	P1, change ver. from 2C to 2D P31, pop R637 & depop R640 for BID update from 1000 to 1001 P11, change C622 & C623 from 10pF to 15pF as TXC's validation. P40, change U40 from AL73C1X5B02 to AL73C1X5B03 for Rev. from B2 to C1. P43, change +2.5V_LCM to +2V_VDDC_IO & LAN_REGO125 to LAN_REGOUT12_IO to avoid confusion. P46, change PV4~PV6 from FDZ23002010 to FDRM2002010 as ME's request S3/S5 leakage P28, R31, depop R654 for S3 leakage issue, and supplier indicate it's no need for R5C833; pop R652 as GM5, no leakage concern as test P49, change PR121 PU from +3.3V_ALW to +3.3V_SUS for S5 leakage issue P38, change design, add U52, R714 & U53, delete Q11, R416 & R418 Derating issue P9, change L70(91nH, 1.5A) to 0_0805	14	2D			
		2008/06/19	P42, change CN5 from 32 FFC to 32 coaxial connector for IB cable change P38, del JF1, F31, JP2, F53, for direct USB SW power P38, del C520 & add R711~R718 & change GND to RF_GND for TV layout ; del CN2 to disable internal antenna support P46, depop PV2 & PV4 as ME request XPS Premium LED colors behavior v3 3.xls P38, depop Q16, R100, U2, R109 of Power button board Amber LED as "XPS_Premium_LED_colors_behavior v3 3.xls" MMB ISSP fail P31, change RP22 from 2.2K to 10K for ISSP fail Power issue (update as "RM2MB_M86_D2D_0616 FOR 512MB_1.DSN") P47, change R018 P025 to S4835BDY-T1-E3 due to S4835BDY-T1-E3 EOL; Change PL4 to SIL104R-SR8B due to SIL104R-SR8PF EOL; Change PR47 to short jumper; Remove 0R PR58 P48, Change PR97 from 15.8K to 13.3K for WCEPTA; Remove PR65 and PR64, directly connect pin6 to GND; Change PR31 to short jumper P49, Remove PR65 and PR64, directly connect pin6 to GND; Depop PC56, PC57; Change PR48 from 15.4K to 11.32K for WCEPTA; Change PR56 to short jumper; Change PL5 to SIL104R-1R5B due to SIL104R-1R5PF EOL P50, Remove 0R PR173; Change PR157 to short jumper; Remove 0R PR164; Remove 0R PR165 and PR166 P51, Remove 0R PR11, PR13, PR15, PR68, PR16, PR18, PR19, PR22, PR90; Change PR84 to 4.02K; Change PR91 to short jumper; Andy_0617: Depop PC15, PC16 P52, Remove 0R PR125; Change PR113 to 82K; Change PR105 to 61.9K; Change PR126 to short jumper P53, Change PR61 to short jumper; Change PL7 to SIL104R-1R5B due to SIL104R-1R5PF EOL P54, Change to S4835DDY-T1-E3 due to S4835BDY-T1-E3 EOL	15	2E			
		2008/06/20	EMI Solution for Power as "RM2MB_M86_D2D_0619 FOR 512MB_1.DSN" P47, Add FL5 for EMI solution P50, Change PC176 from 0.1u to 1u by FEA suggestion P54, Add PC194, PC195, PC196 for EMI solution Derating issue P9, as EMI request, change from R713 0_0805 to L70 "CX3P121001(120 ohm, 3A)"	16	2A			
	2008/06/24	P31, del R623 & "ICH_PME#" to connect "PLTRST#" to R652; add PD 1K for RESET_OUT# P47, depop PV3, P45 & PV6 as ME request; add PAD PV7, PV8 & PV9 & hole H34; change screw hole from " " to " " for H26, H33, G23, H32, H21, H10, H7, H2, H1, H9, H22, H11, H18, H30 & H8 P41, change R286 from 0_0803 to 0_0805, depop R83, R301, R110, R543, R450 & R544 P38, add pin 4 & 5 for CN3 & CN10 to connect to GND P42, change CN5 from 32 to 30 pin & change pin assignment for cable manufacture P30, change CN12 from "EXPCARD-1CX41101-p1-26P-1" to "expcard-tox41101-p1-26p-1-rm2" P54, change CN24 from "DFHD09MR017(SUYIN)" to "DFHD09MR024(FOXCONN)" as ME's information P9, P11, P13, P20, change footprint from RC0402-C to RC0402 or CC0402-C to CC0402 for R247, R496, R489, R524, R525, C726, C728, C741, C624, C689 P3, depop R56 for abnormal H_RESET# Combo USB EA fail - change USB Bus SW P35, change U17 from "ALDUSB31003" to "AL004907000"; del R345 & add C520 for support item NB(Cantiga) & SB(ICH9M) P/N change P5~P14, change NB from "AJQ01720708" to "AJSLB970T13(ver B3)"; change SB from "AJQ07090T06" to "AJSLB8Q0T16(ver A3)" For 2nd source BOM creation problem P9, P26, P27, P38, P44, change Q63 from "BAM34560102" to "BAM06550025"; change D17 from "BCR8500VZ02" to "BC010K45004"; change D10 from "BC000501Z09" to "BC010K45004"; change D4 & D7 from "BC000751Z05" to "BC000340033"; change Q20 from "BA0011420Z08" to "BA001140001"	17	2D				
	2D(ST)	2008/06/16	P1, change ver. from 2C to 2D P31, pop R637 & depop R640 for BID update from 1000 to 1001 P11, change C622 & C623 from 10pF to 15pF as TXC's validation. P40, change U40 from AL73C1X5B02 to AL73C1X5B03 for Rev. from B2 to C1. P43, change +2.5V_LCM to +2V_VDDC_IO & LAN_REGO125 to LAN_REGOUT12_IO to avoid confusion. P46, change PV4~PV6 from FDZ23002010 to FDRM2002010 as ME's request S3/S5 leakage P28, R31, depop R654 for S3 leakage issue, and supplier indicate it's no need for R5C833; pop R652 as GM5, no leakage concern as test P49, change PR121 PU from +3.3V_ALW to +3.3V_SUS for S5 leakage issue P38, change design, add U52, R714 & U53, delete Q11, R416 & R418 Derating issue P9, change L70(91nH, 1.5A) to 0_0805	18	2A			
		2008/06/19	P42, change CN5 from 32 FFC to 32 coaxial connector for IB cable change P38, del JF1, F31, JP2, F53, for direct USB SW power P38, del C520 & add R711~R718 & change GND to RF_GND for TV layout ; del CN2 to disable internal antenna support P46, depop PV2 & PV4 as ME request XPS Premium LED colors behavior v3 3.xls P38, depop Q16, R100, U2, R109 of Power button board Amber LED as "XPS_Premium_LED_colors_behavior v3 3.xls" MMB ISSP fail P31, change RP22 from 2.2K to 10K for ISSP fail Power issue (update as "RM2MB_M86_D2D_0616 FOR 512MB_1.DSN") P47, change R018 P025 to S4835BDY-T1-E3 due to S4835BDY-T1-E3 EOL; Change PL4 to SIL104R-SR8B due to SIL104R-SR8PF EOL; Change PR47 to short jumper; Remove 0R PR58 P48, Change PR97 from 15.8K to 13.3K for WCEPTA; Remove PR65 and PR64, directly connect pin6 to GND; Change PR31 to short jumper P49, Remove PR65 and PR64, directly connect pin6 to GND; Depop PC56, PC57; Change PR48 from 15.4K to 11.32K for WCEPTA; Change PR56 to short jumper; Change PL5 to SIL104R-1R5B due to SIL104R-1R5PF EOL P50, Remove 0R PR173; Change PR157 to short jumper; Remove 0R PR164; Remove 0R PR165 and PR166 P51, Remove 0R PR11, PR13, PR15, PR68, PR16, PR18, PR19, PR22, PR90; Change PR84 to 4.02K; Change PR91 to short jumper; Andy_0617: Depop PC15, PC16 P52, Remove 0R PR125; Change PR113 to 82K; Change PR105 to 61.9K; Change PR126 to short jumper P53, Change PR61 to short jumper; Change PL7 to SIL104R-1R5B due to SIL104R-1R5PF EOL P54, Change to S4835DDY-T1-E3 due to S4835BDY-T1-E3 EOL	19	2B			
		2008/06/20	EMI Solution for Power as "RM2MB_M86_D2D_0619 FOR 512MB_1.DSN" P47, Add FL5 for EMI solution P50, Change PC176 from 0.1u to 1u by FEA suggestion P54, Add PC194, PC195, PC196 for EMI solution Derating issue P9, as EMI request, change from R713 0_0805 to L70 "CX3P121001(120 ohm, 3A)"	20	2E			
		2008/06/24	P31, del R623 & "ICH_PME#" to connect "PLTRST#" to R652; add PD 1K for RESET_OUT# P47, depop PV3, P45 & PV6 as ME request; add PAD PV7, PV8 & PV9 & hole H34; change screw hole from " " to " " for H26, H33, G23, H32, H21, H10, H7, H2, H1, H9, H22, H11, H18, H30 & H8 P41, change R286 from 0_0803 to 0_0805, depop R83, R301, R110, R543, R450 & R544 P38, add pin 4 & 5 for CN3 & CN10 to connect to GND P42, change CN5 from 32 to 30 pin & change pin assignment for cable manufacture P30, change CN12 from "EXPCARD-1CX41101-p1-26P-1" to "expcard-tox41101-p1-26p-1-rm2" P54, change CN24 from "DFHD09MR017(SUYIN)" to "DFHD09MR024(FOXCONN)" as ME's information P9, P11, P13, P20, change footprint from RC0402-C to RC0402 or CC0402-C to CC0402 for R247, R496, R489, R524, R525, C726, C728, C741, C624, C689 P3, depop R56 for abnormal H_RESET# Combo USB EA fail - change USB Bus SW P35, change U17 from "ALDUSB31003" to "AL004907000"; del R345 & add C520 for support item NB(Cantiga) & SB(ICH9M) P/N change P5~P14, change NB from "AJQ01720708" to "AJSLB970T13(ver B3)"; change SB from "AJQ07090T06" to "AJSLB8Q0T16(ver A3)" For 2nd source BOM creation problem P9, P26, P27, P38, P44, change Q63 from "BAM34560102" to "BAM06550025"; change D17 from "BCR8500VZ02" to "BC010K45004"; change D10 from "BC000501Z09" to "BC010K45004"; change D4 & D7 from "BC000751Z05" to "BC000340033"; change Q20 from "BA0011420Z08" to "BA001140001"	21	2E			
2008/07/10		P1, change ver. from 2D to 2E P47, update power circuit as "RM2MB_M86_D2D_0624 FOR 512MB_1.DSN" P47, depop PR1 & pop R159 for change IMVP_P2 PU from +3.3V_SUS & +3.3V_RUN P42, change back CN5 from 30 pin coaxial to 32 pin FFC & change pin assignment for FFC implement; add CN32 for additional AGND P20, add two more 10uF for +VCC_GFX_CORE ripple P15, P34, P35, change ESD1~3 from ALSRV054011 to AL000504000 for EOL concern P34, change SIM card connector to push-push type, CN56 from DSG06001404 to DSG060000020 P25, reserve R723 for option when remove DP dongle support ST Internal Doc. 0703-1 update P48, change PU3 from AL009194000 to AL009024000. P38, change R127 from 220 to 1K; R90, R107, R101, R119 from 220 to 3.3K as IM3 XPS Premium LED colors behavior v3 7.xls (no Amber LED & charge indicator on power button LED) P37, del "BAT_LED_INT" as "XPS_Premium_LED_colors_behavior v3 7.xls" P38, change power of R113 & U31 from +VCC_ALW2 to +VCC_SUS; no charge indicator ; del Q16, R100, U2, R109 of Power button board Amber LED Subwoofer overload & band filter and main SPK EQ issue fix as "PALTROW EQ CIRCUIT rev 3.pptx" P41, circuit change for main SPK EQ as "PALTROW EQ CIRCUIT rev 3.pptx" P42, circuit change for subwoofer overload & band filter issue as "PALTROW EQ CIRCUIT rev 3.pptx" add KB LED detect pin P13, del T59 & add "KB_LED_DET" P37, del +15V_ALW, add KB_LED_DET & R721, R722	22	2A				
2008/07/14		P25, change DP connector footprint from "DP-47644-0001-20P-L-H" to "dp-rsd-47644-001-20p-l-h" P20, P21, add "-C" on footprint for C867, C868, C427, C417, C405, C395, C401, C379, C367, L38, C356, C358, L39, C389 P46, update library for "8" for H26, H33, G23, H32, H21, H10, H7, H2, H1, H9, H22, H11, H18, H30 & H8 debug port code "52" issue when "MEDIA_INT#" isn't high at system boot P37, add R724, move PU of "MEDIA_INT#" to MB side reserve Hall IC on MB side for option & study P37, add U54, C869, R726 & reserve R725 for study of Hall IC on MB	23	2A				
				24	2A			
				25	2E			
				26	2D			
				27	2D			
				28	2D			
				29	2A			
				30	2D			
				31	2D			
				32	2A			
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