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Project Code & Schematics Subject:

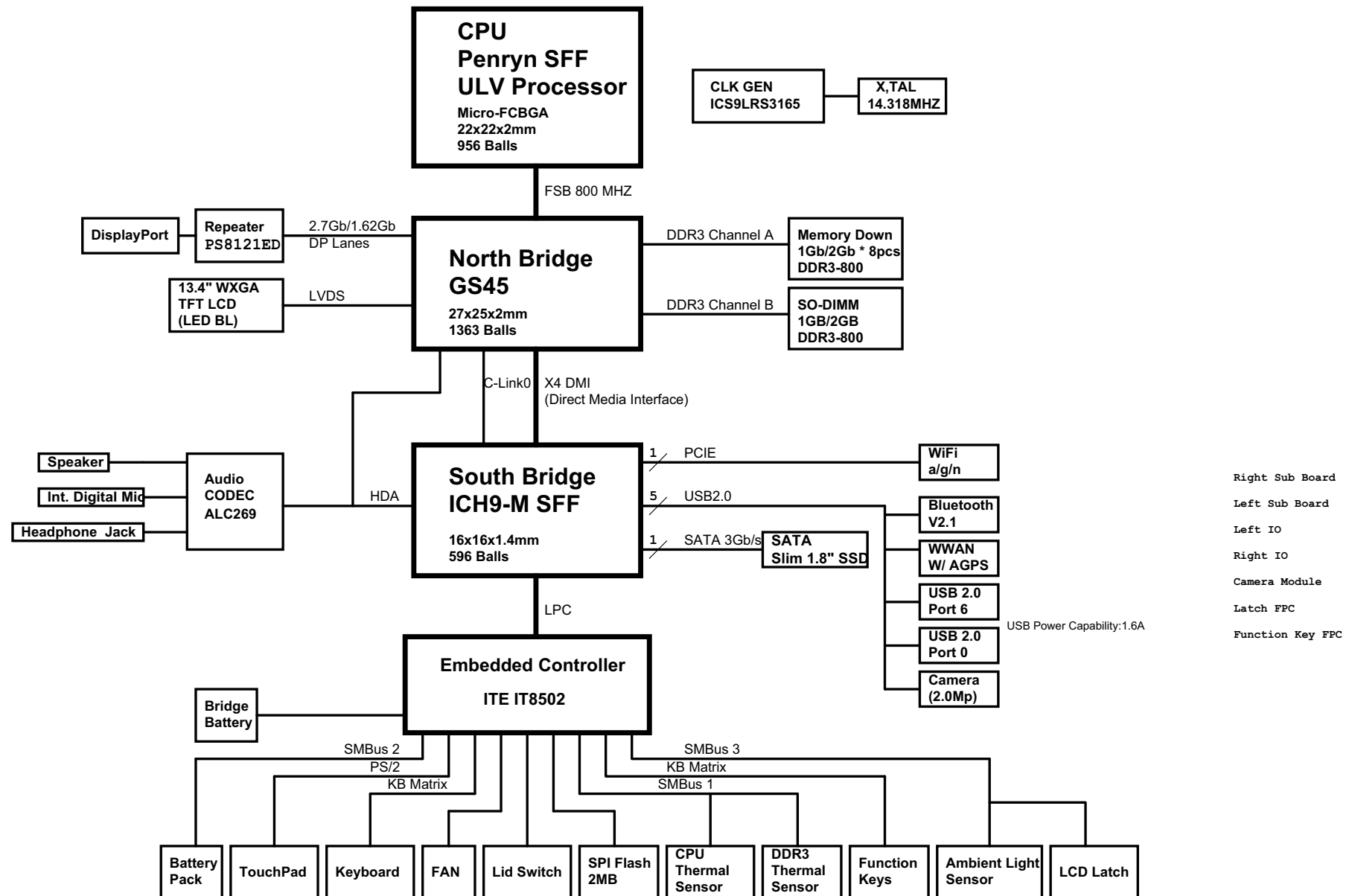
H800 Main Board1P-0099L00-A000 (COMPEQ)  
1P-0099J00-A000 (IRIS)

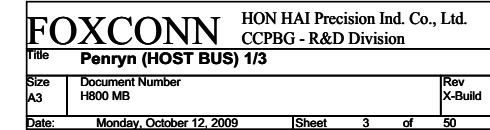
FOXCONN

HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

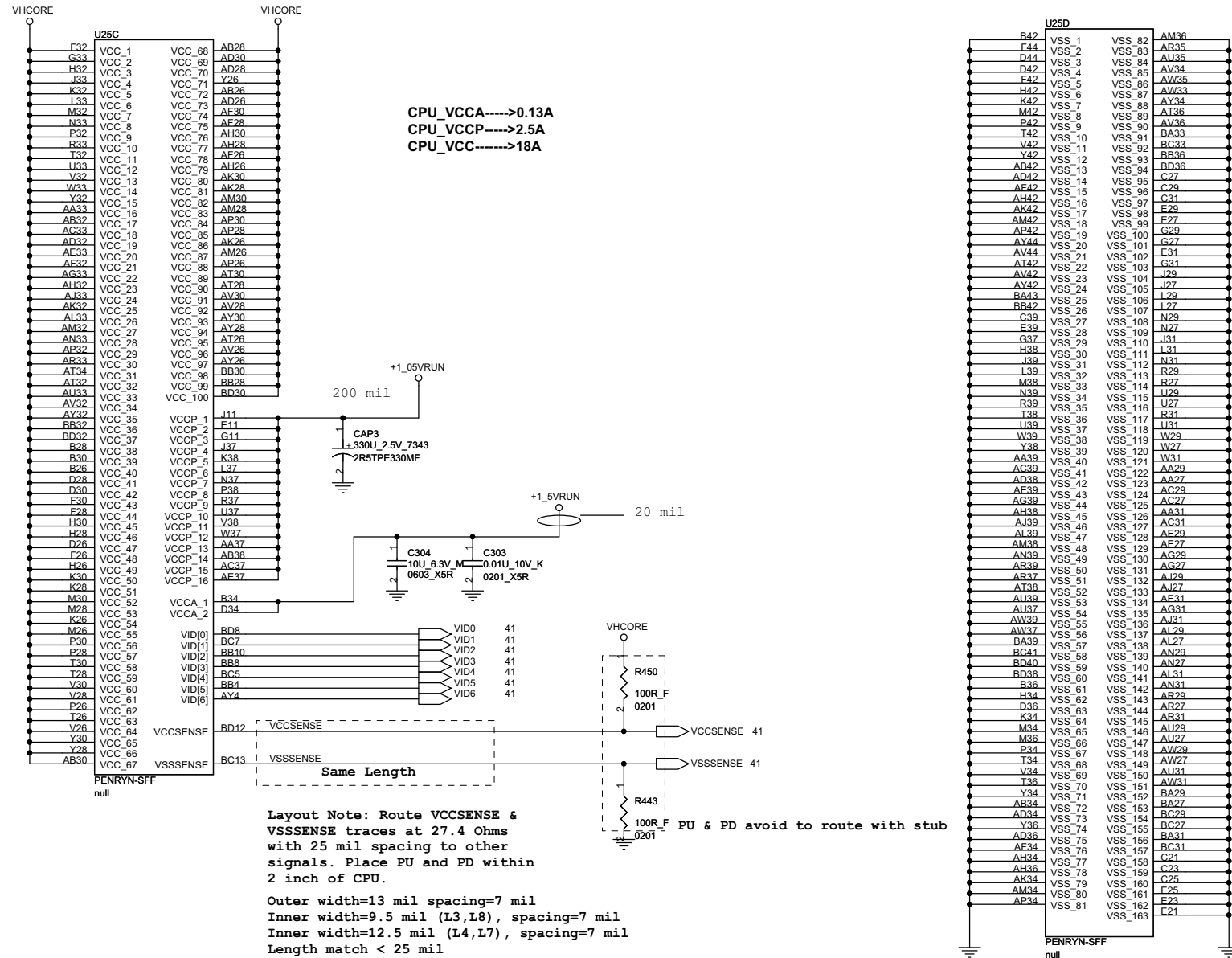
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SizeCustom	Document NumberH800 MB	RevX-Build
Date:	Wednesday, October 07, 2009	Sheet1 of 50

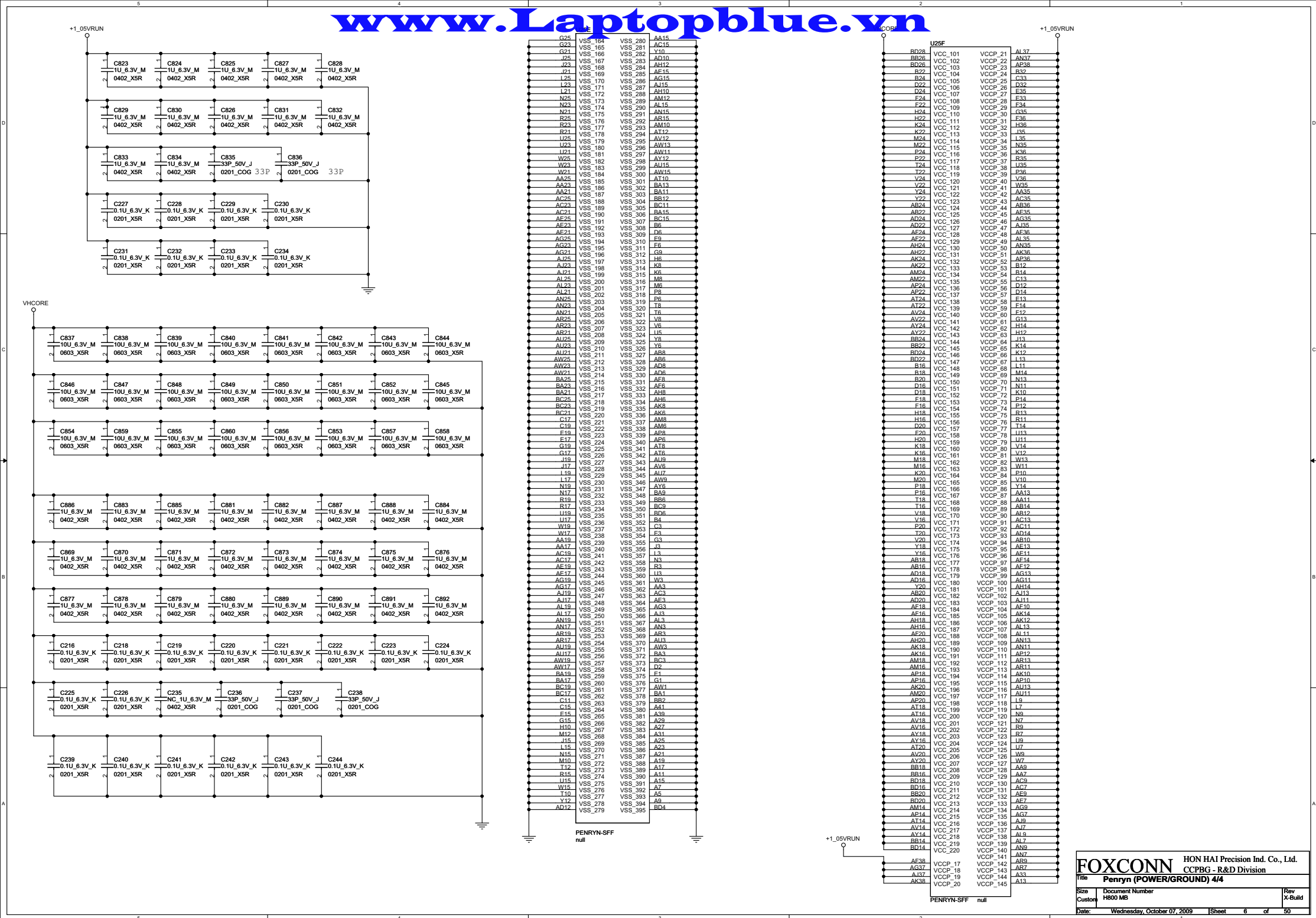
# H800 BLOCK DIAGRAM







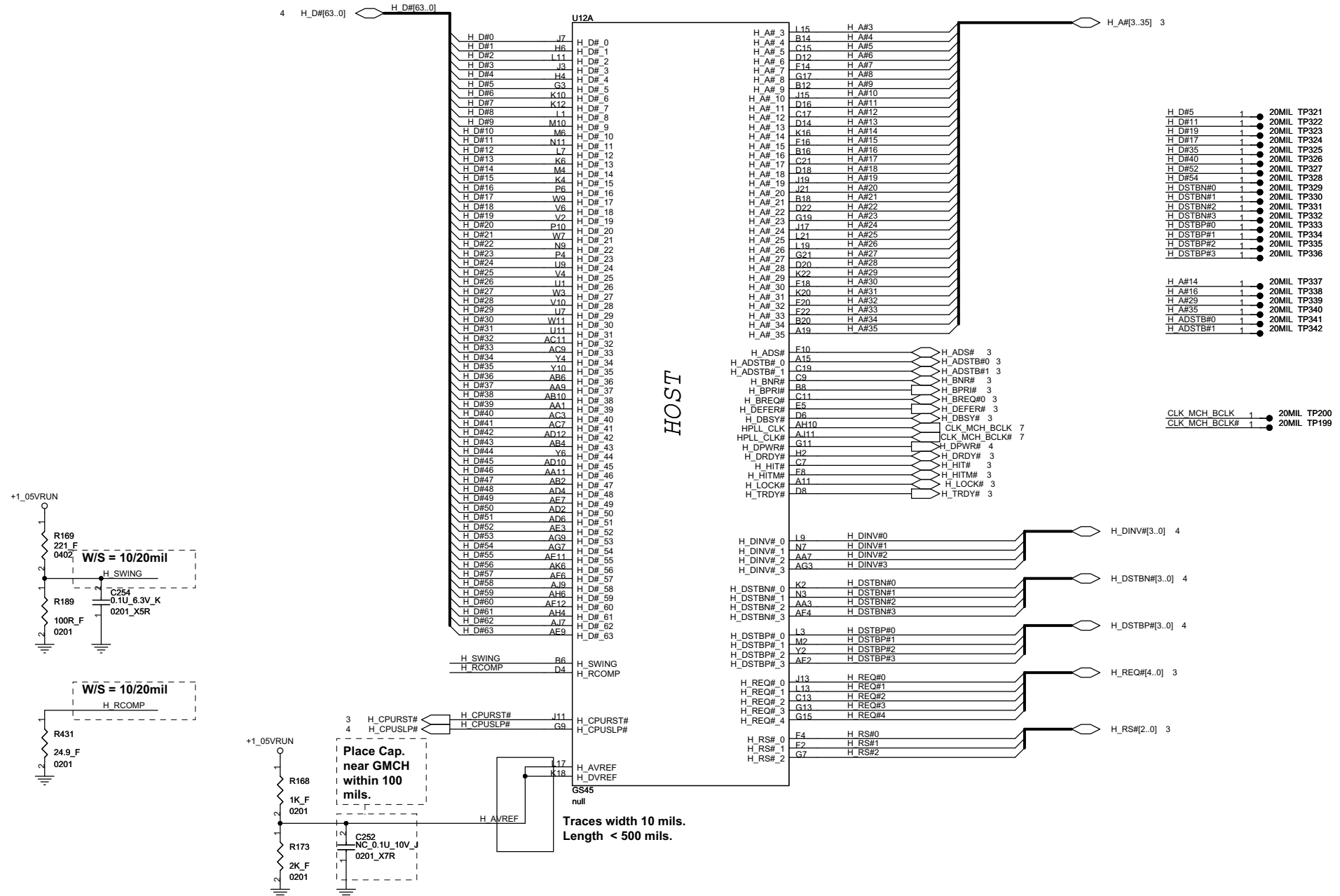




FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

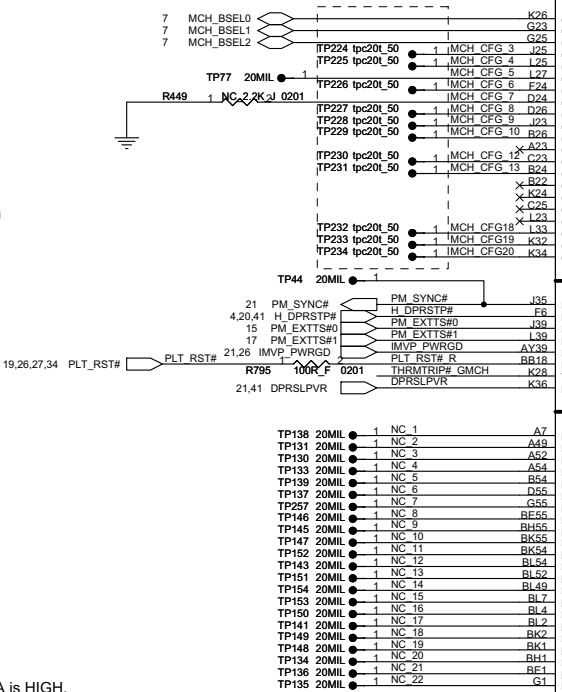
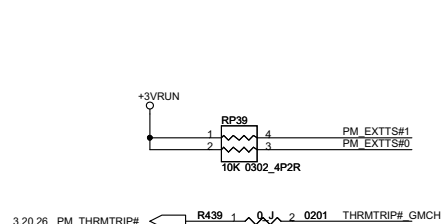
Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10





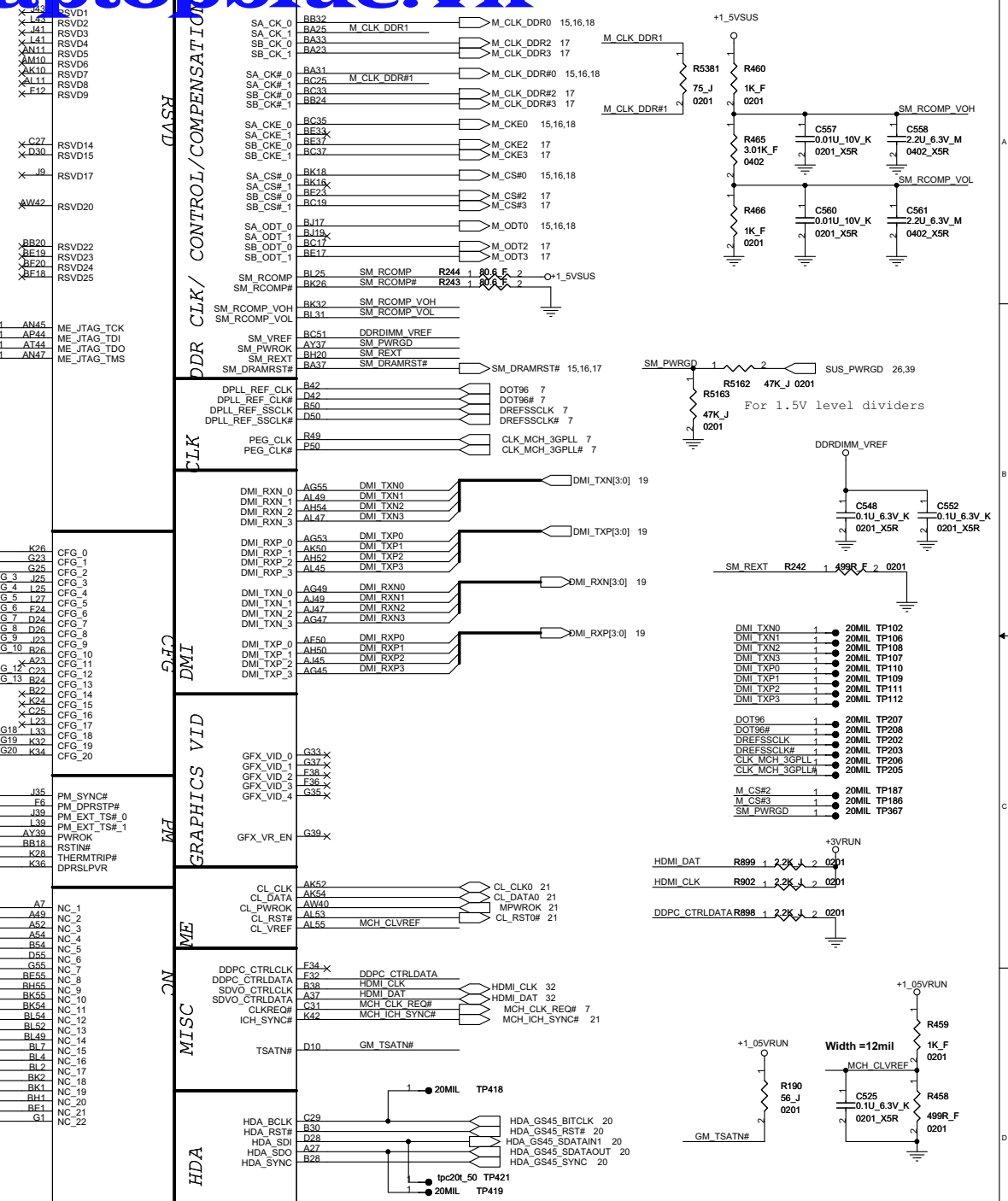


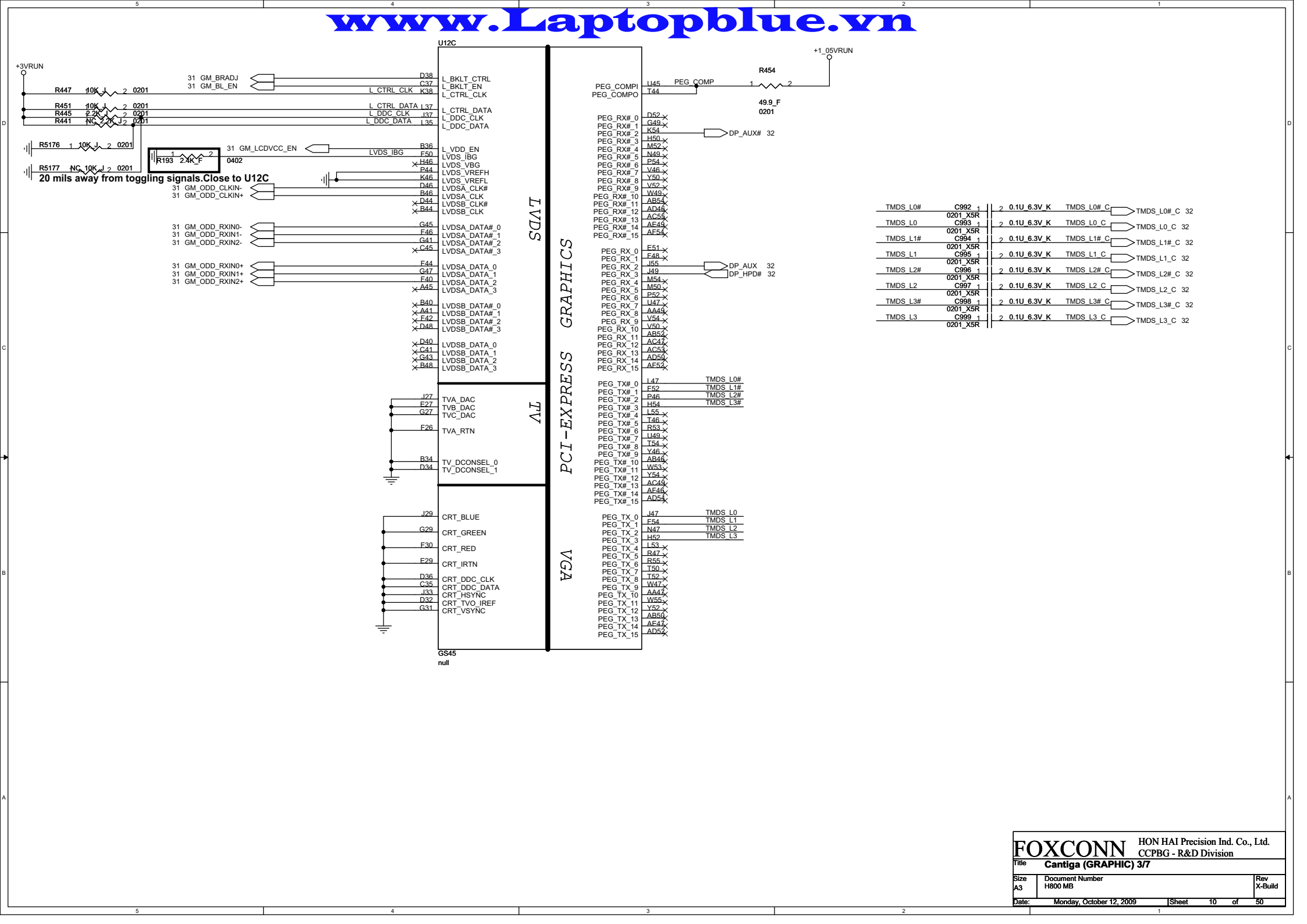
MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no Confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

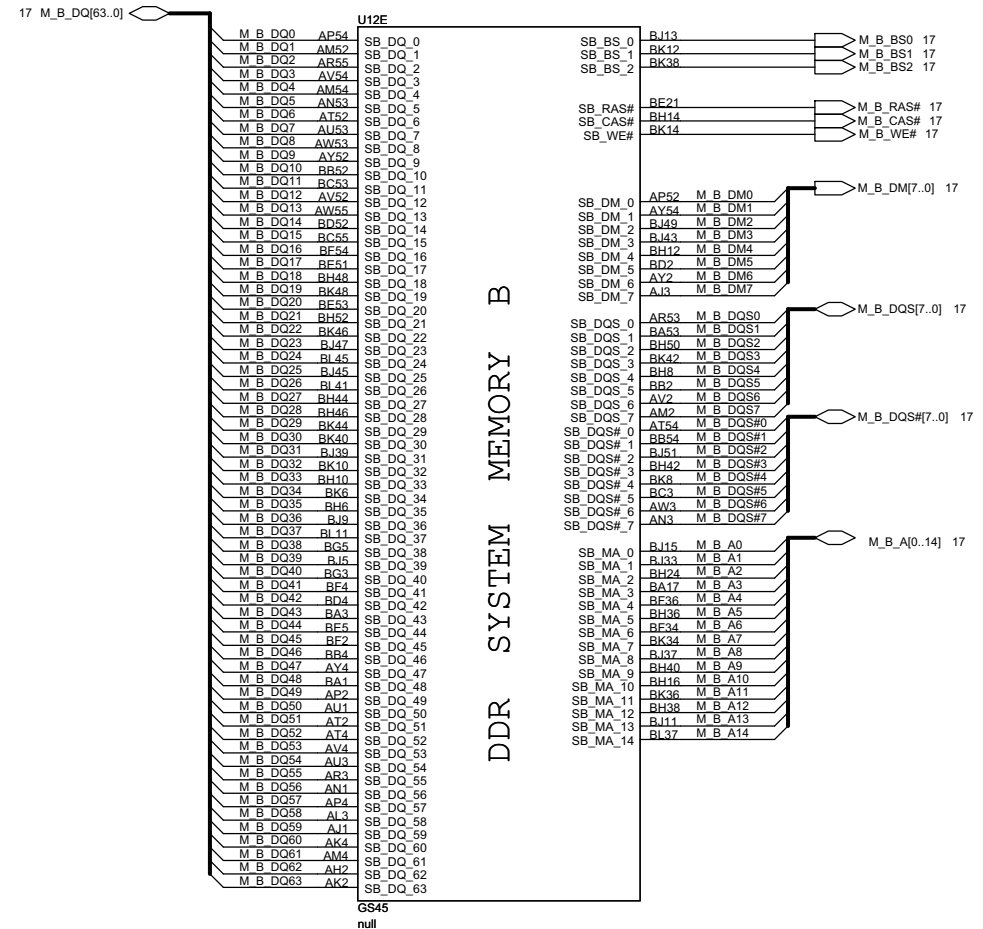
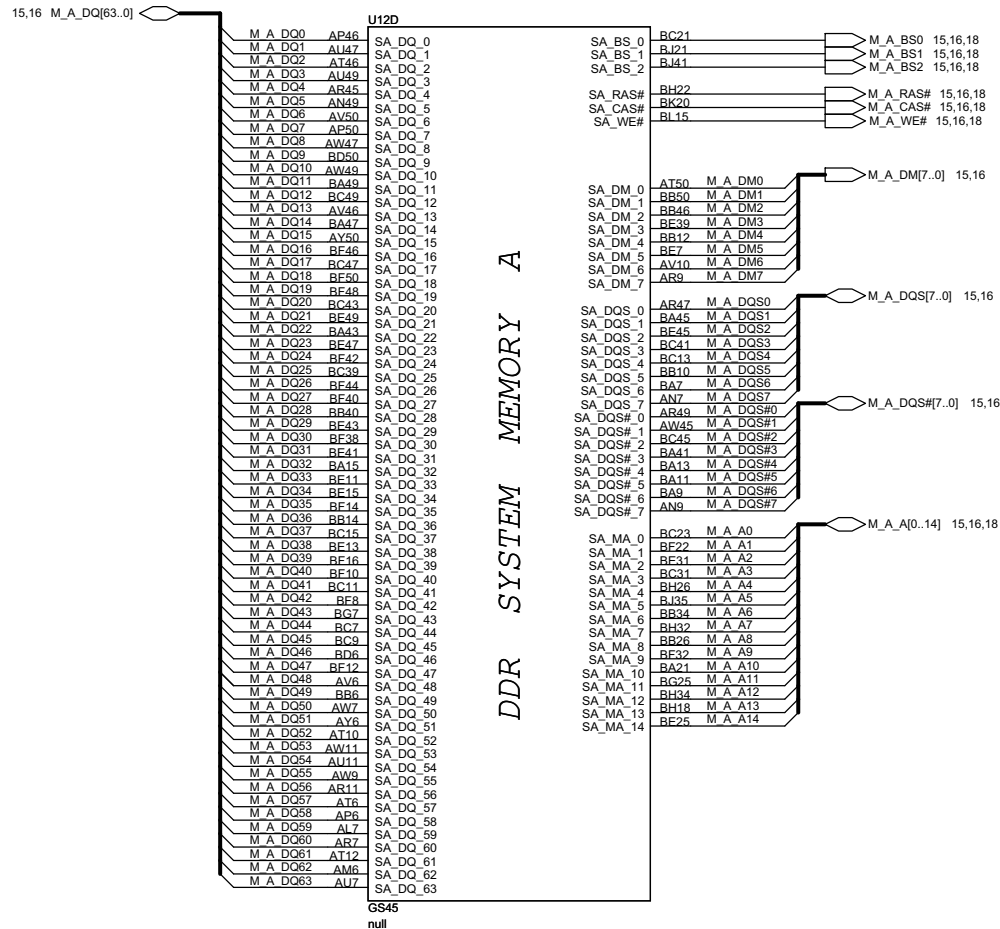


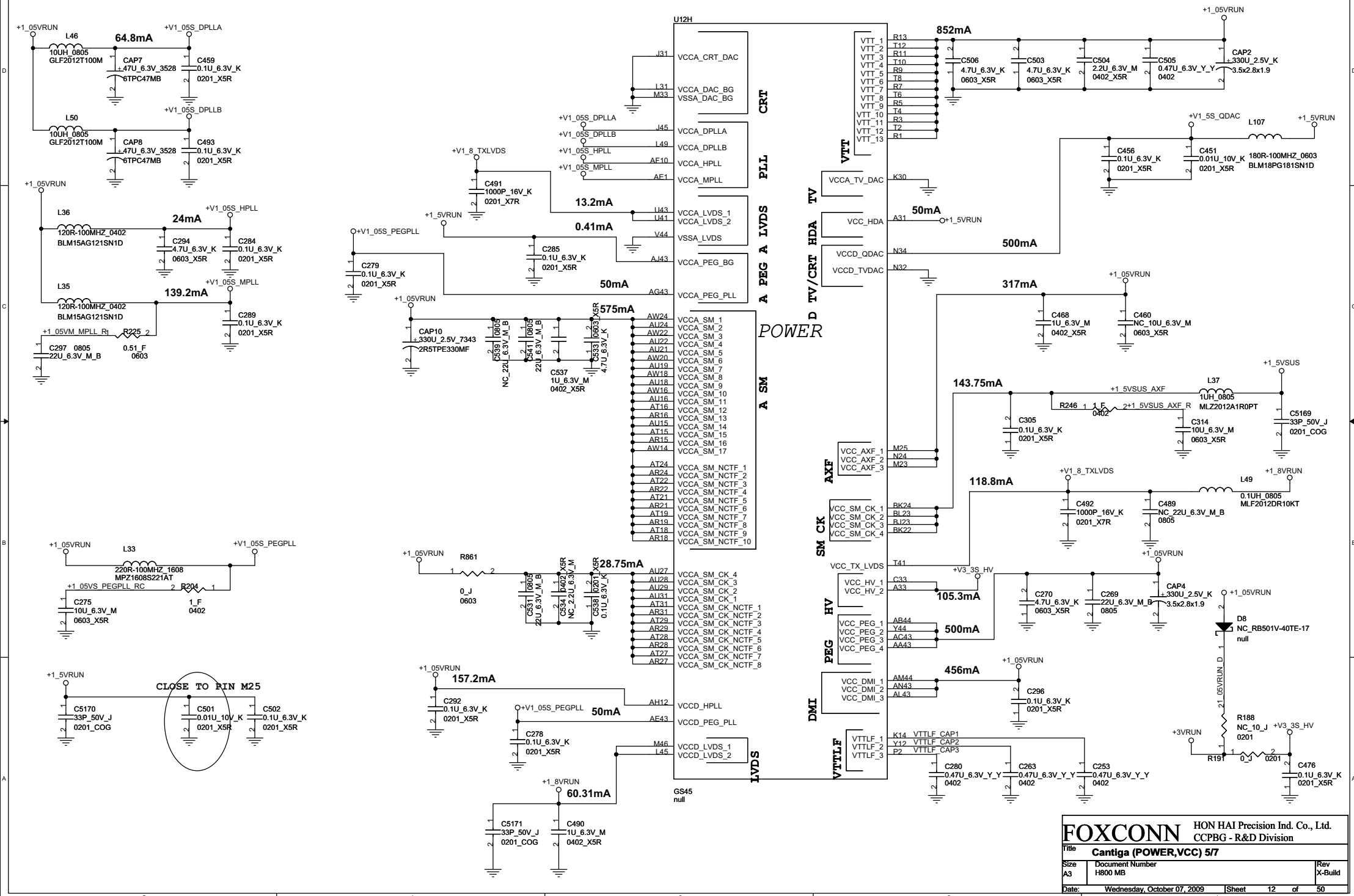
- NOTES:
1. SDVO\_CTRLCLK should be pulled up if SDVO\_CTRLDATA is HIGH.
  2. DDPC\_CTRLCLK should be pulled up if DDPC\_CTRLDATA is HIGH.
  3. L\_DDC\_CLK should be pulled up if L\_DDC\_DATA is HIGH.

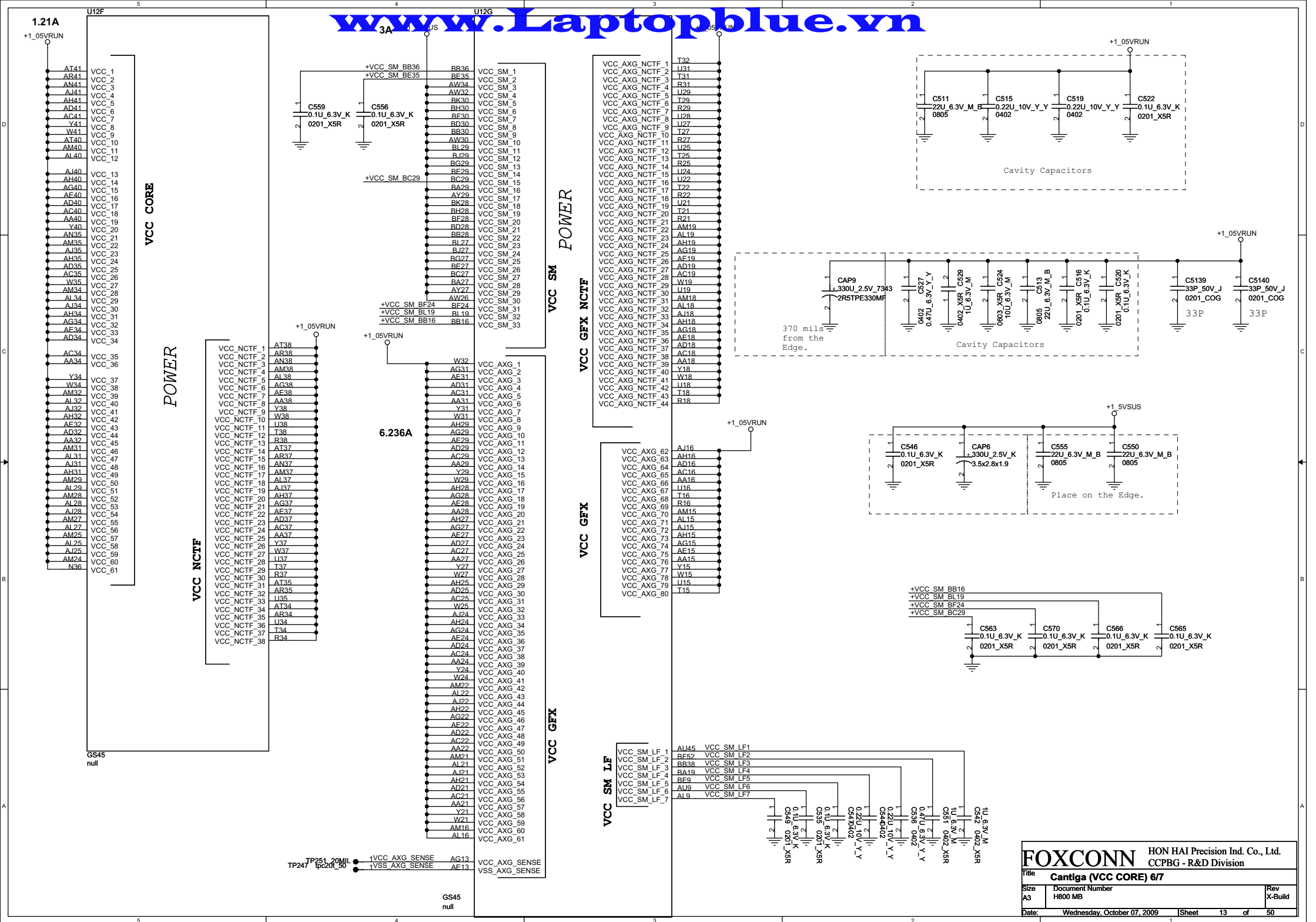
SDVO/HDMI/DP Configuration	Local Flat Panel (LFP) Present Strap L_DDC_DATA	DP/HDMI Present Strap DDPC_CTRLDATA	SDVO Present Strap SDVO_CTRLDATA	Digital Display Port/PCI Express Concurrent Strap CFG20
HDMI/DP Port B Enabled	Low	Low	High	Low

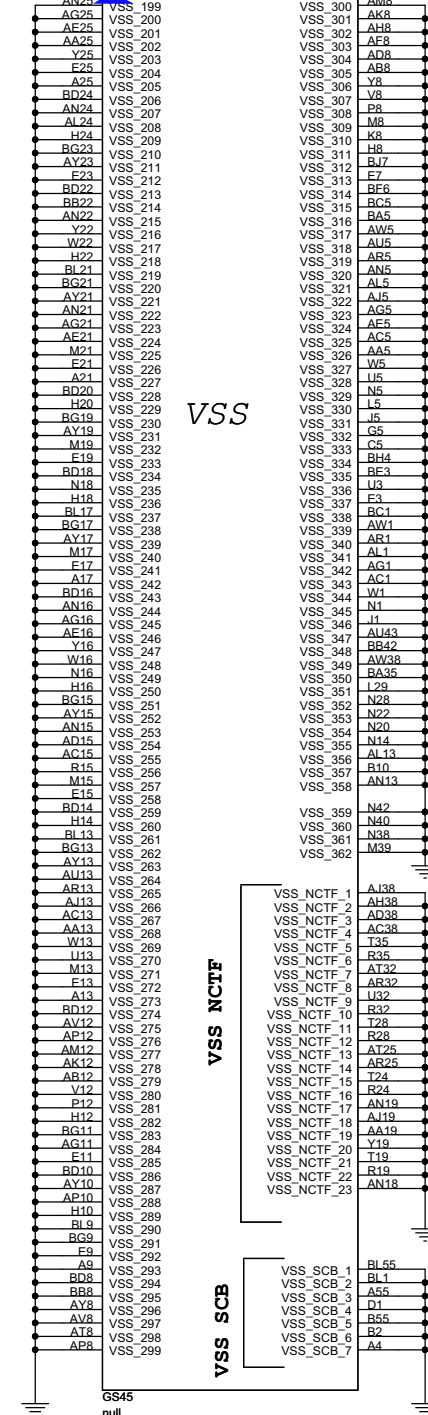
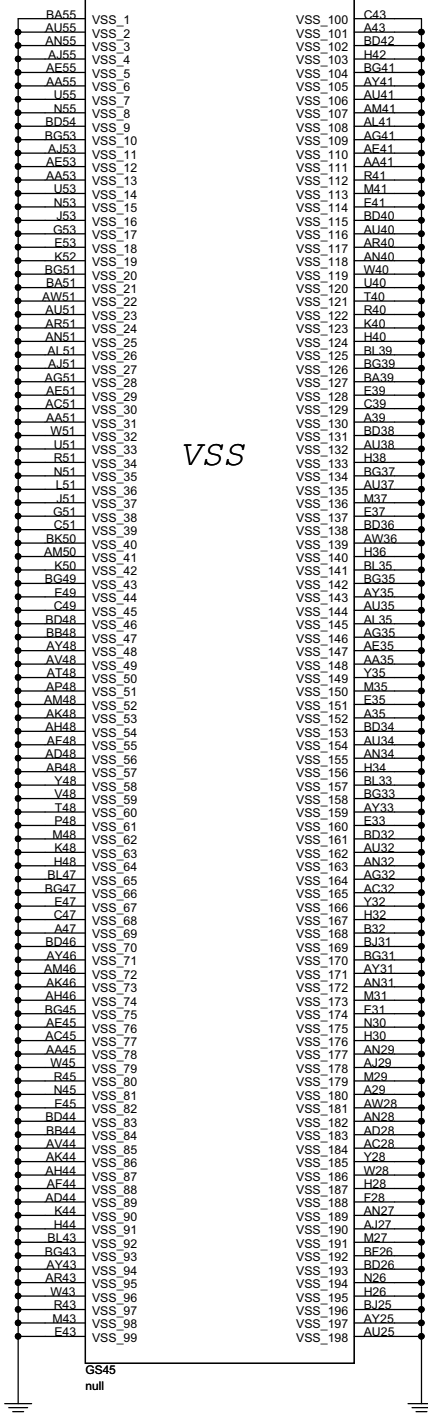








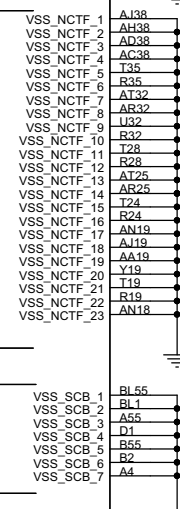




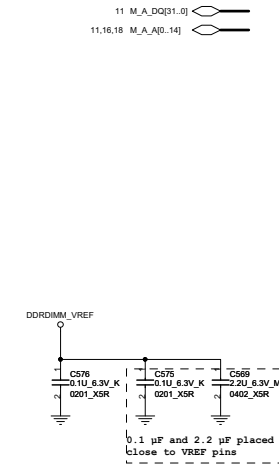
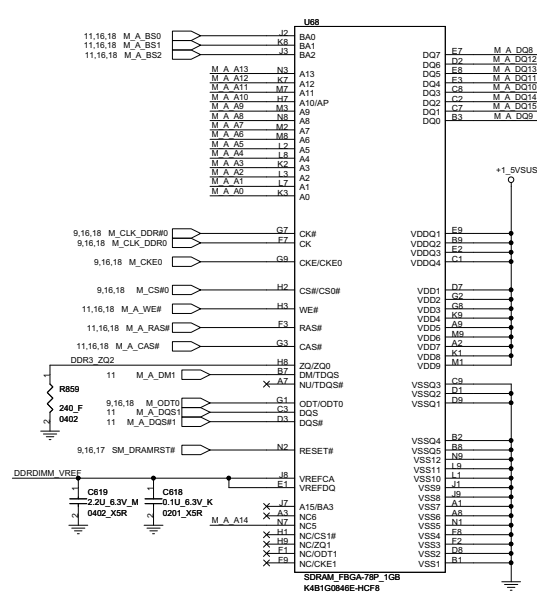
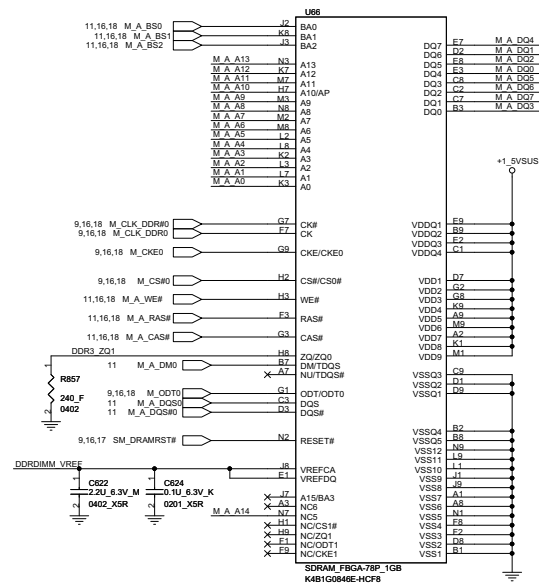
VSS

VSS NCTF

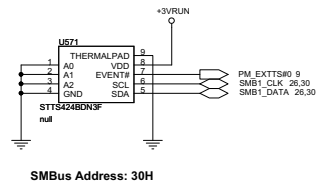
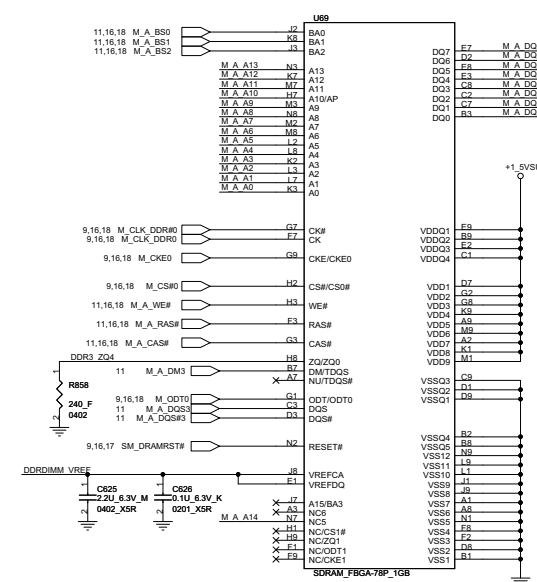
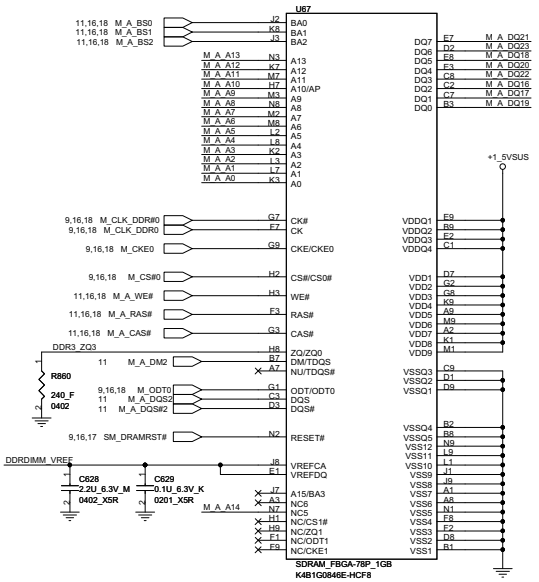
VSS SCB



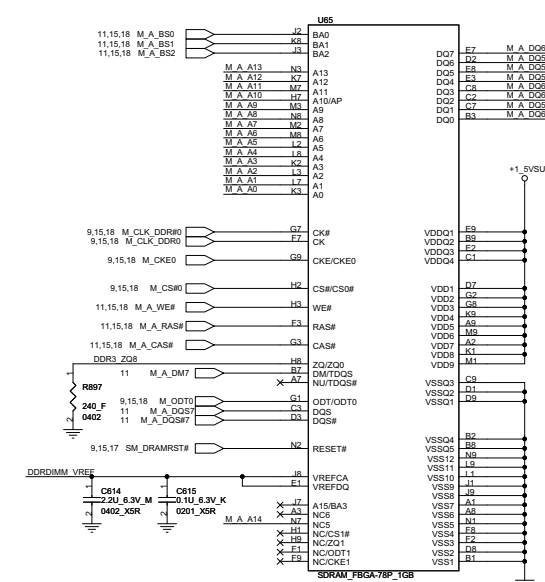
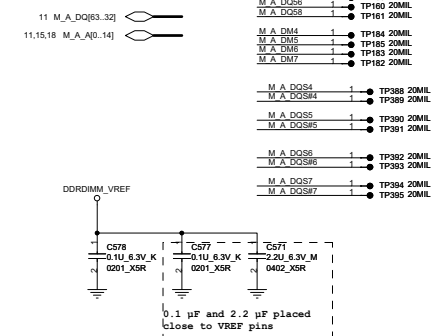
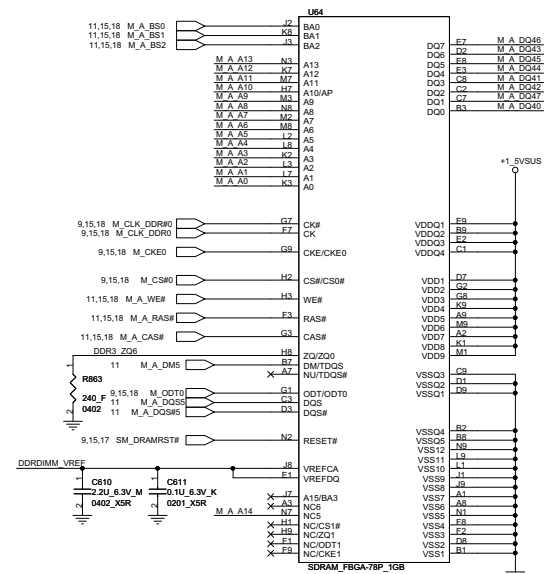


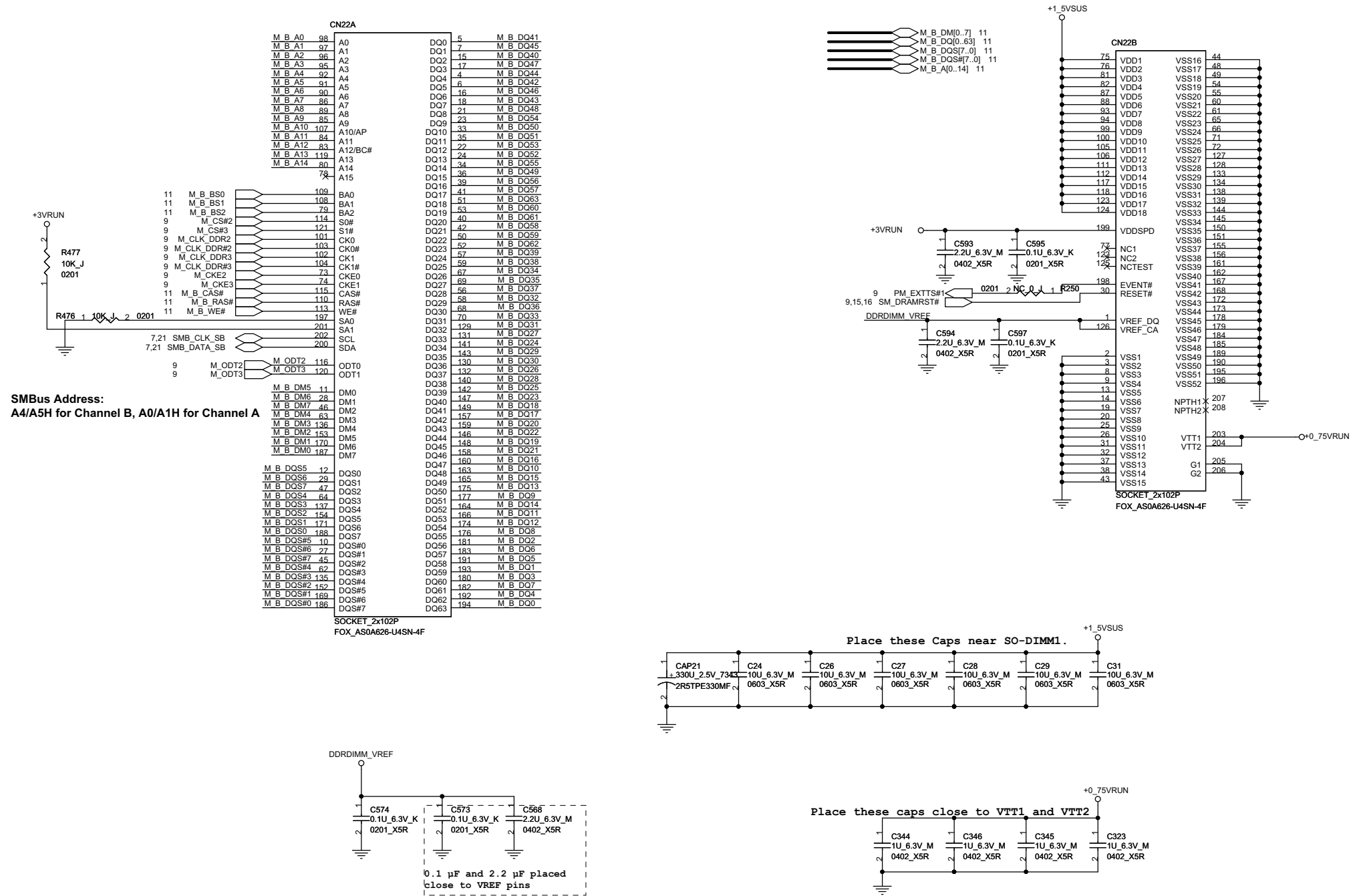


M_A A8	1	TP121 20ML
M_A A13	1	TP122 20ML
M_A DQ0	1	TP123 20ML
M_A DQ1	1	TP124 20ML
M_A DQ2	1	TP125 20ML
M_A DQ3	1	TP126 20ML
M_A DQ4	1	TP127 20ML
M_A DQ5	1	TP128 20ML
M_A DQ6	1	TP129 20ML
M_A DQ7	1	TP130 20ML
M_A DQ8	1	TP131 20ML
M_A DQ9	1	TP132 20ML
M_A DQ10	1	TP133 20ML
M_A DQ11	1	TP134 20ML
M_A DQ12	1	TP135 20ML
M_A DQ13	1	TP136 20ML
M_A DQ14	1	TP137 20ML
M_A DQ15	1	TP138 20ML
M_A DQ16	1	TP139 20ML
M_A DQ17	1	TP140 20ML
M_A DQ18	1	TP141 20ML
M_A DQ19	1	TP142 20ML
M_CKE0	1	TP164 20ML
M_CS#0	1	TP167 20ML
M_A_WE#	1	TP168 20ML
M_A_RAS#	1	TP169 20ML
M_A_CAS#	1	TP170 20ML
M_A DQ20	1	TP171 20ML
M_A DQ21	1	TP172 20ML
M_A DQ22	1	TP173 20ML
M_A DQ23	1	TP174 20ML
M_A DQ24	1	TP175 20ML
M_A DQ25	1	TP176 20ML
M_A DQ26	1	TP177 20ML
M_A DQ27	1	TP178 20ML
M_A DQ28	1	TP179 20ML
M_A DQ29	1	TP180 20ML
M_A DQ30	1	TP181 20ML
M_A DQ31	1	TP182 20ML
M_A DQ32	1	TP183 20ML
M_A DQ33	1	TP184 20ML
M_A DQ34	1	TP185 20ML
M_A DQ35	1	TP186 20ML
M_A DQ36	1	TP187 20ML
M_A DQ37	1	TP188 20ML
M_A DQ38	1	TP189 20ML
M_A DQ39	1	TP190 20ML
M_A DQ40	1	TP191 20ML
M_A DQ41	1	TP192 20ML
M_A DQ42	1	TP193 20ML
M_A DQ43	1	TP194 20ML
M_A DQ44	1	TP195 20ML
M_A DQ45	1	TP196 20ML
M_A DQ46	1	TP197 20ML
M_A DQ47	1	TP198 20ML
M_A DQ48	1	TP199 20ML
M_A DQ49	1	TP200 20ML

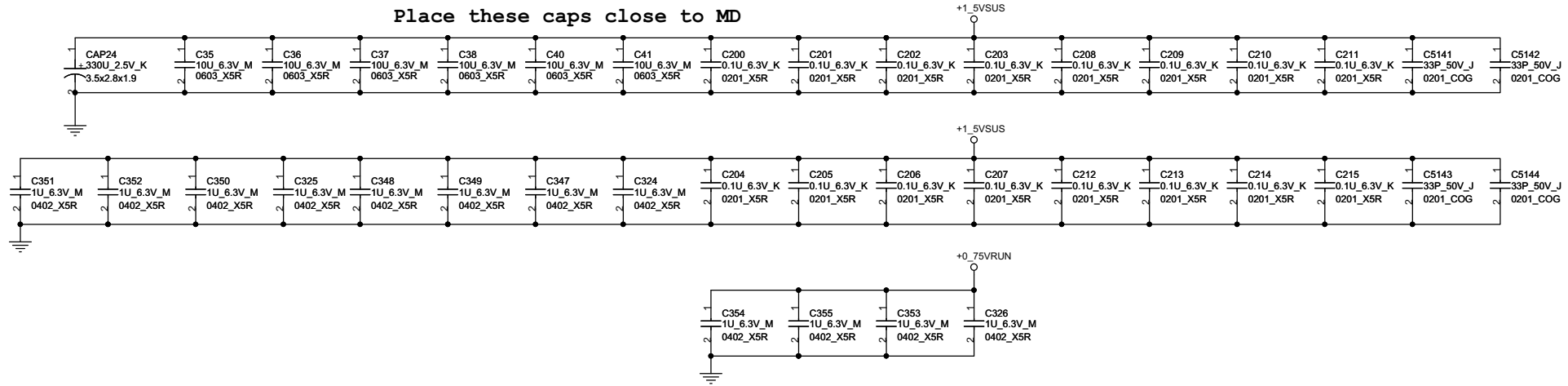




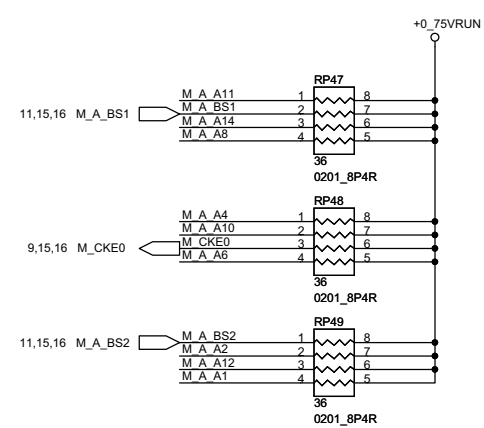
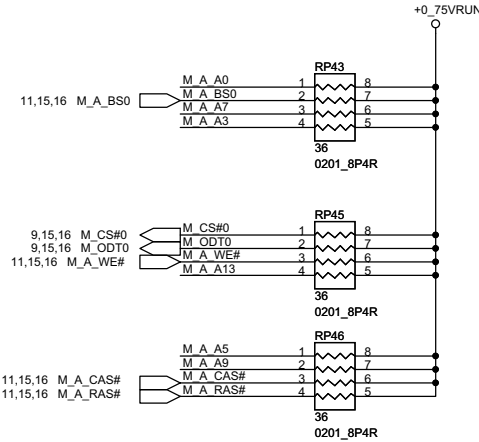
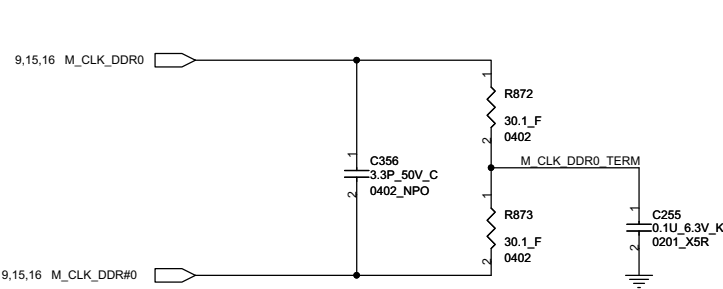


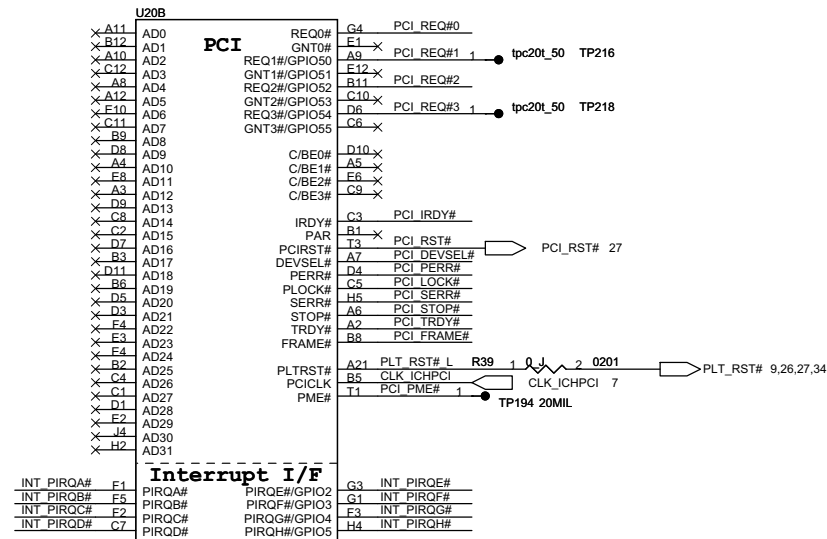
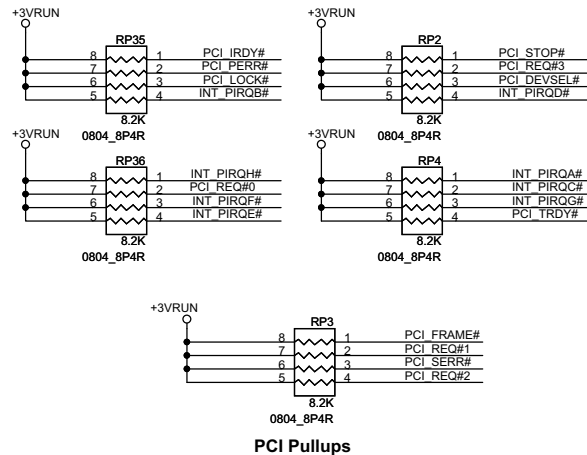


Place these caps close to MD



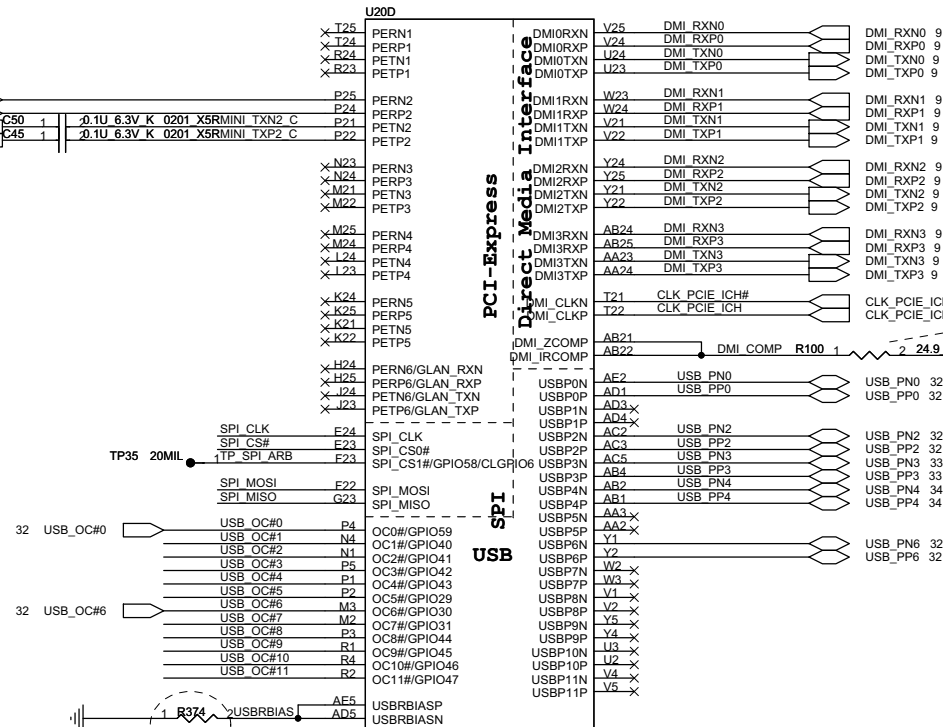
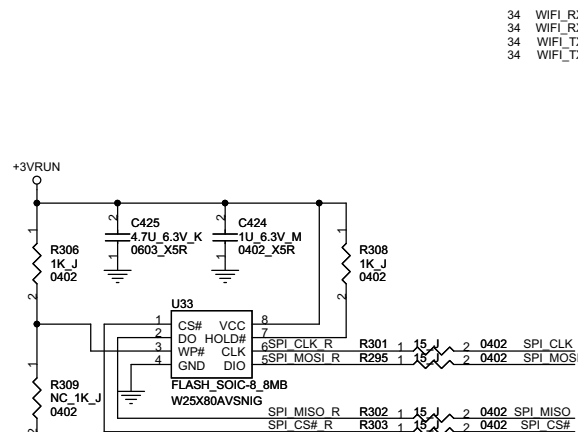
M\_A\_A[0..14] 11,15,16





## Strap for Boot-BIOS

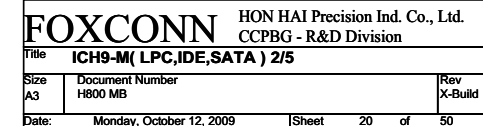
	GNT0#	SPI_CS1#
LPC(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

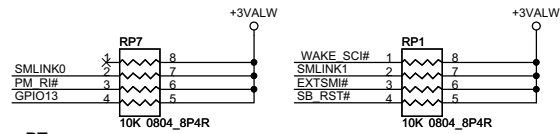


CLK ICHPCI	1	TP343 20MIL
DMI RXN0	1	TP118 20MIL
DMI RXN2	1	TP119 20MIL
DMI RXN3	1	TP120 20MIL
DMI RXP0	1	TP114 20MIL
DMI RXP2	1	TP117 20MIL
DMI RXP3	1	TP116 20MIL
CLK PCIE ICH#	1	TP209 20MIL
CLK PCIE ICH	1	TP210 20MIL

Place within 500 mils of ICH

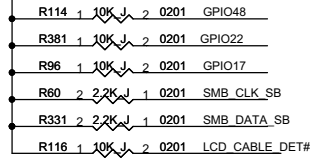
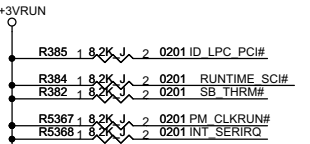
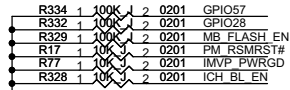
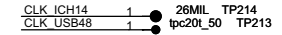
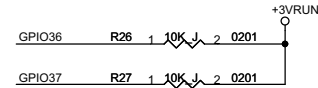
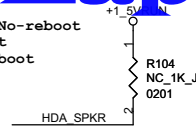
USB PORT	FUNCTION
PORT-0	Right USB
PORT-2	CAMERA
PORT-3	WWAN
PORT-4	BlueTooth
PORT-6	Left USB (USB to RJ45)





PT  
2008/12/22 Changed RP7,RP1 from 0201 array to 0402 array

Stuff for No-reboot  
Low=Default  
High=No-reboot



ID\_LPC\_PCI#  
80 Port I/F:  
H: LPC bus  
L: PCI bus

TP235 tpc20t\_50

31 ICH\_BL\_EN

7 SATACLKREQ#

24 HDA\_SPKR

9 MCH\_ICH\_SYNC#

TP215 tpc20t\_50

26,41 IMVP\_OK

R22 NC\_0\_J 0201

R21 100K\_J 0201

VRMPWRGD

ALW\_PWRGD 26,38

NC\_BAT54C-7-F

D28

PM\_RSMRST# SB

IMVP\_PWRGD SB

3

2

1

2

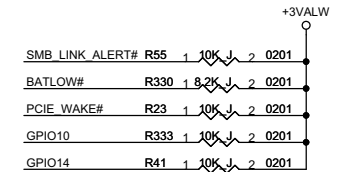
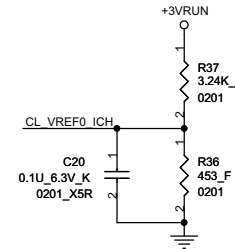
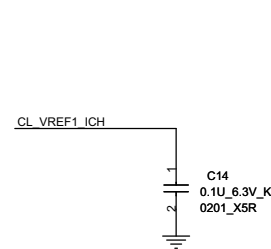
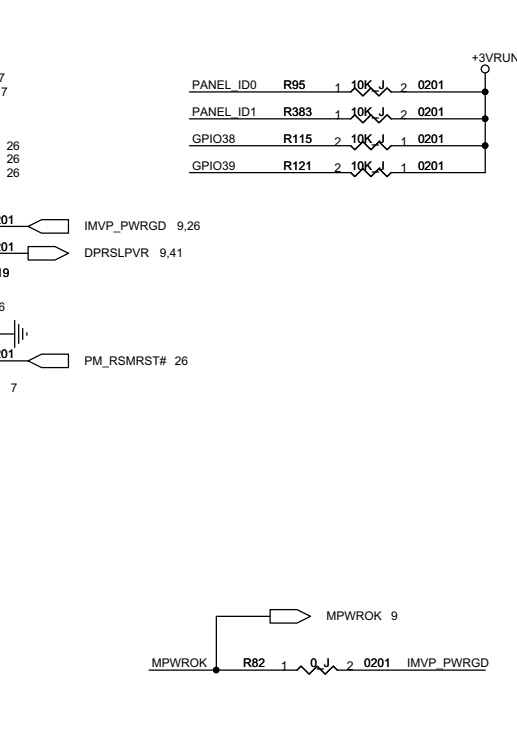
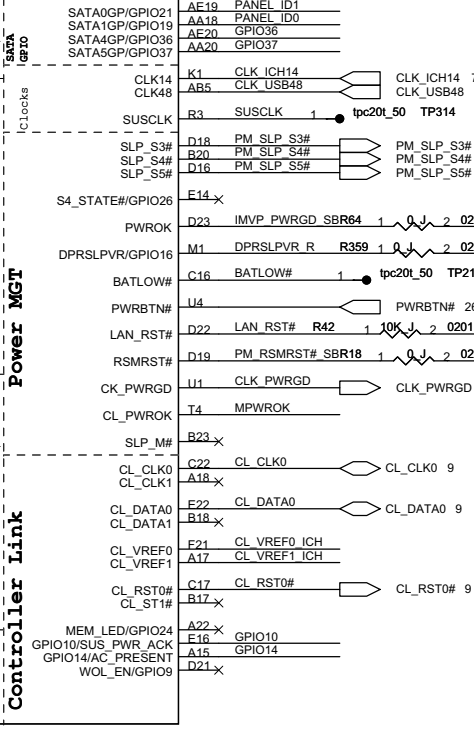
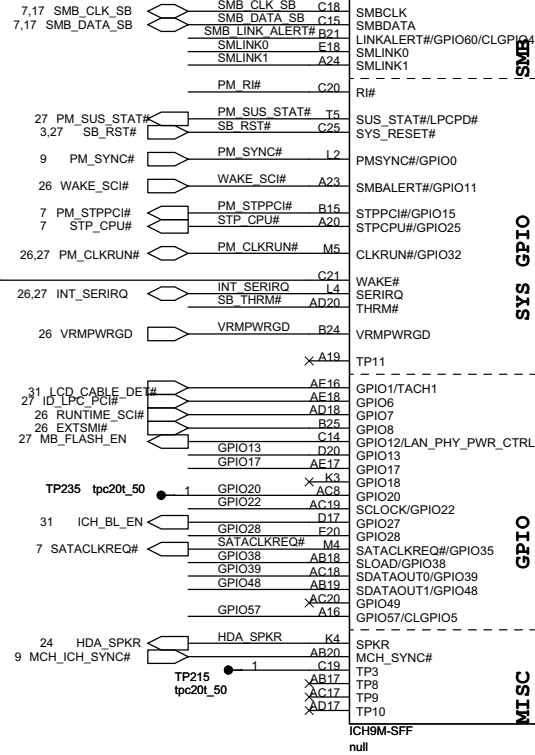
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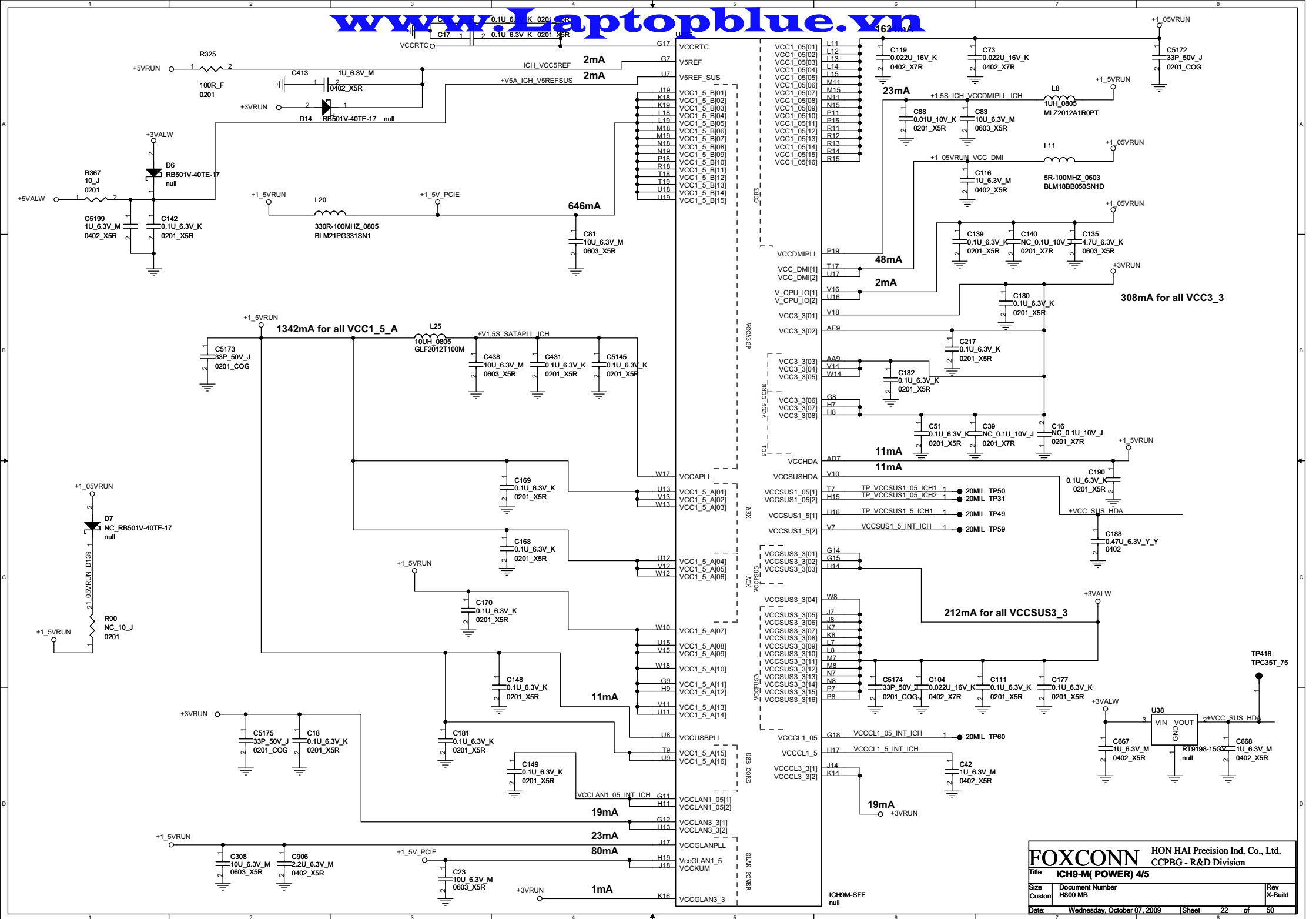
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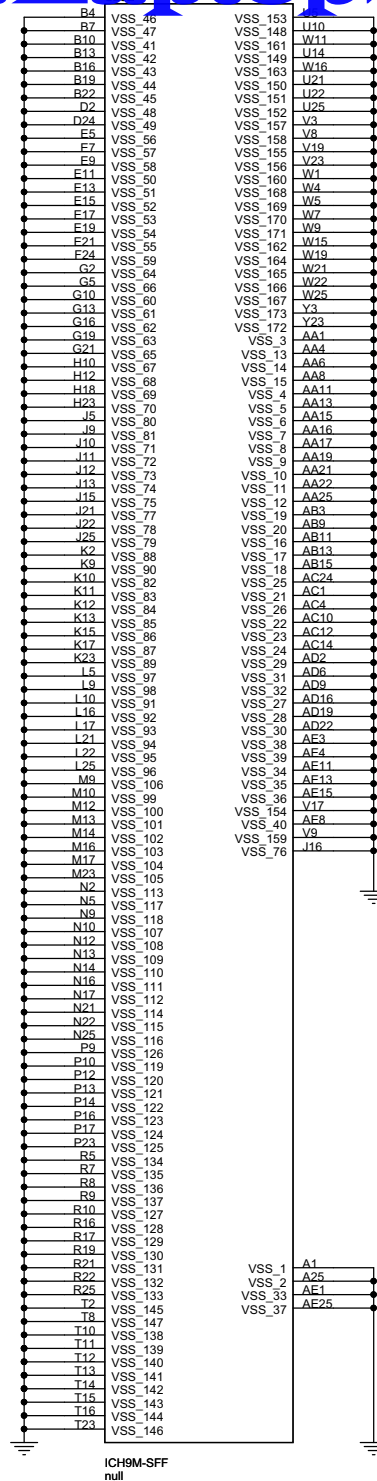
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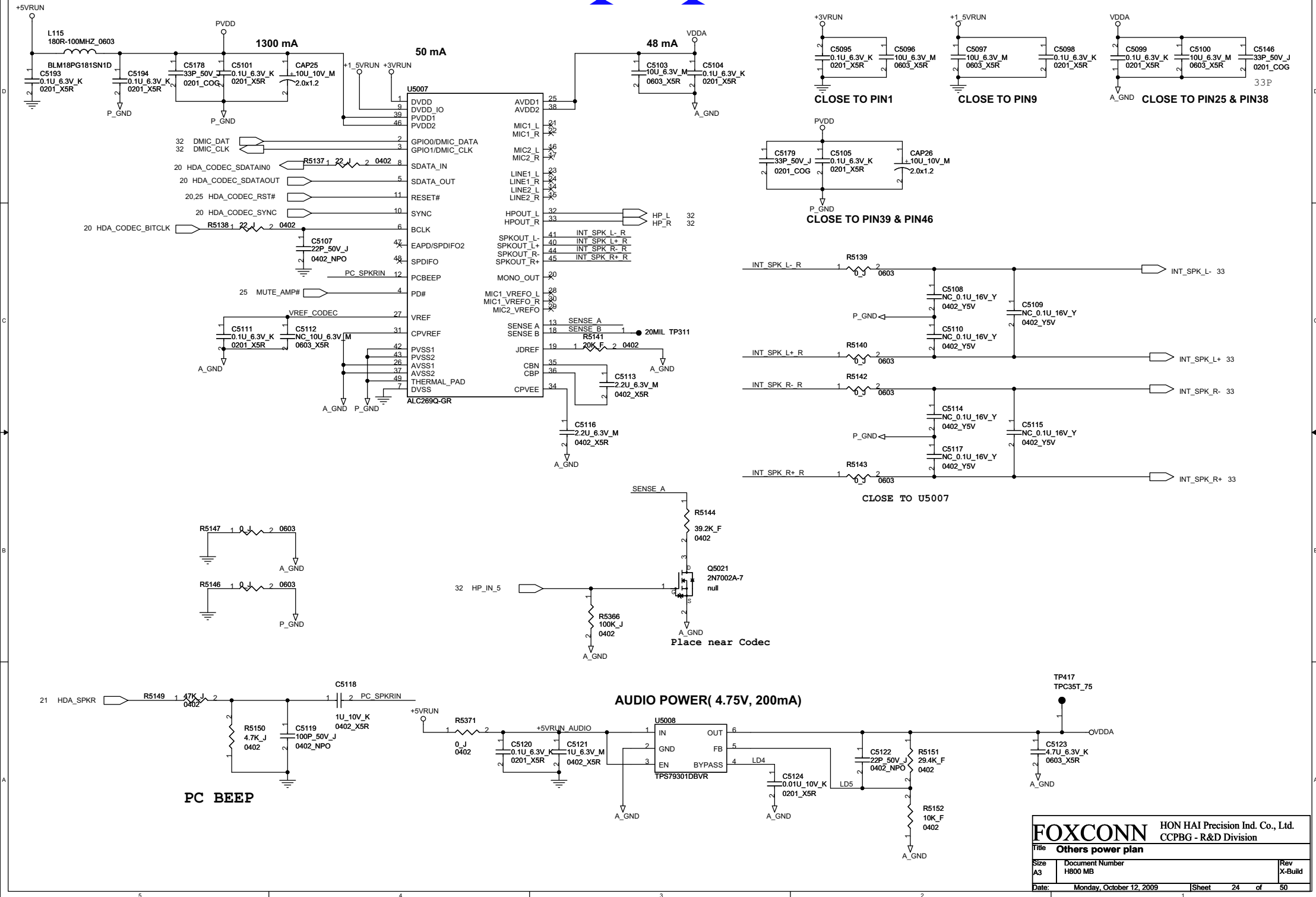
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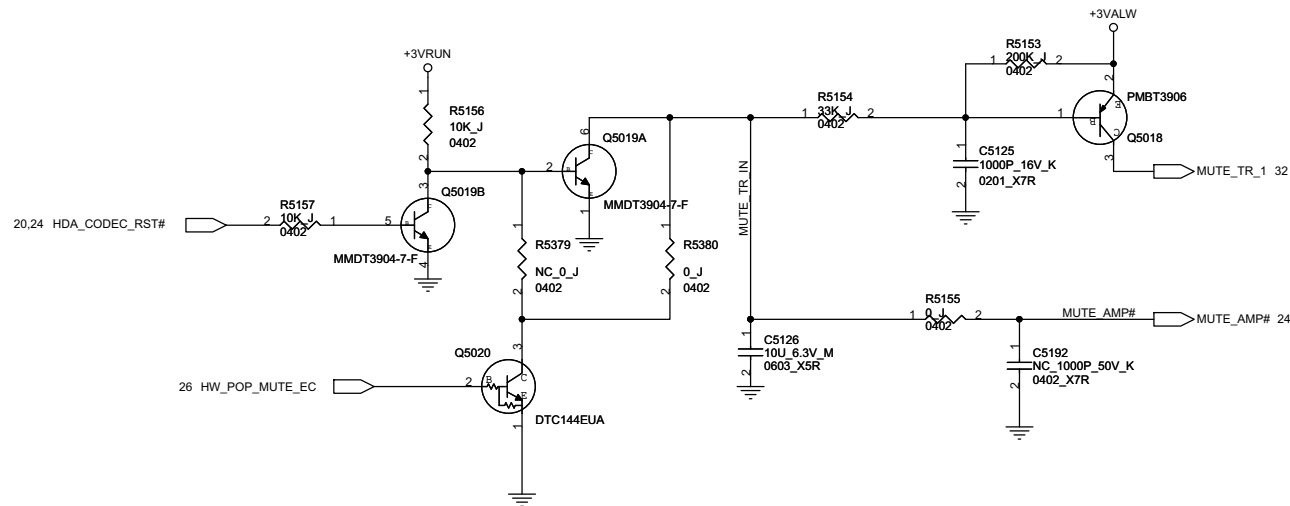


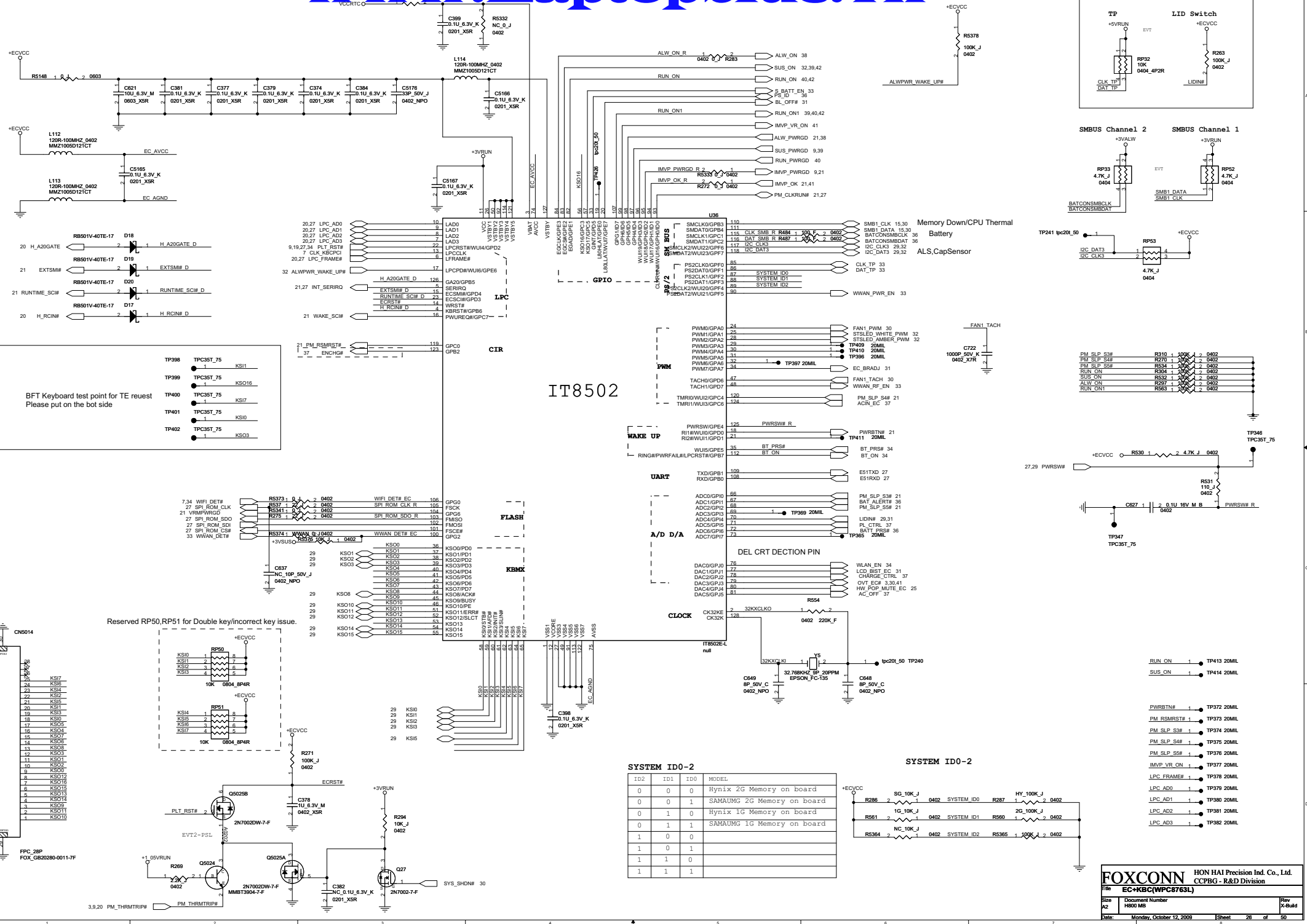


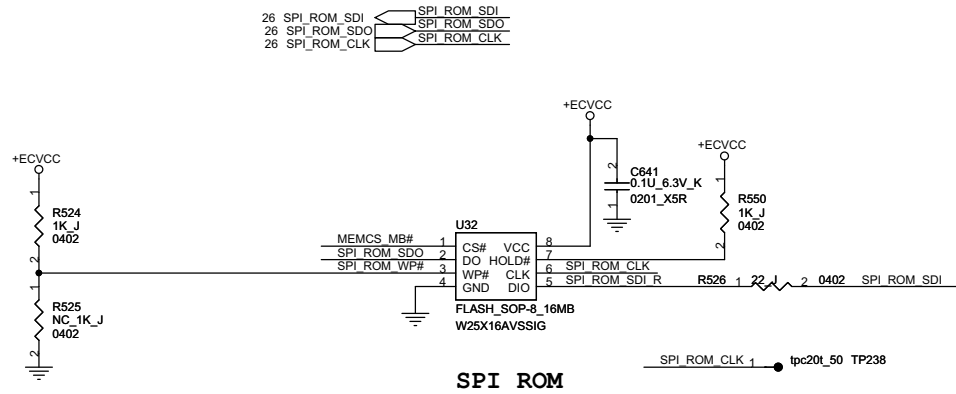






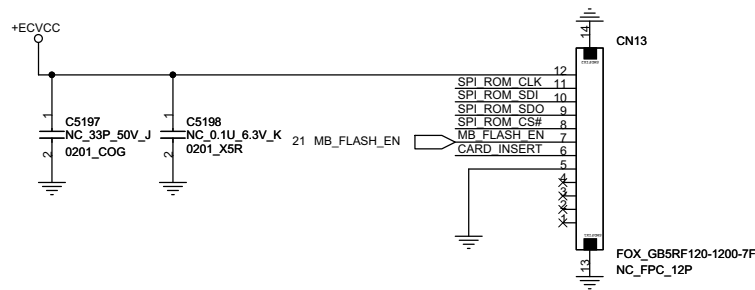




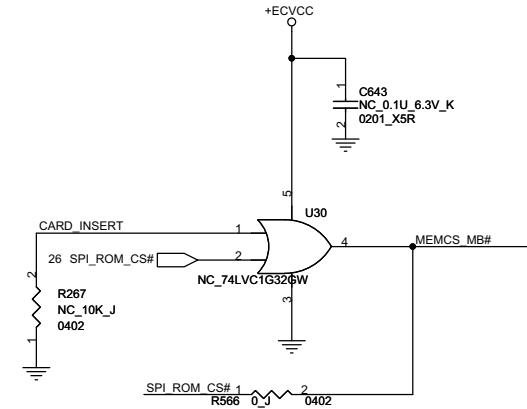


SPI ROM

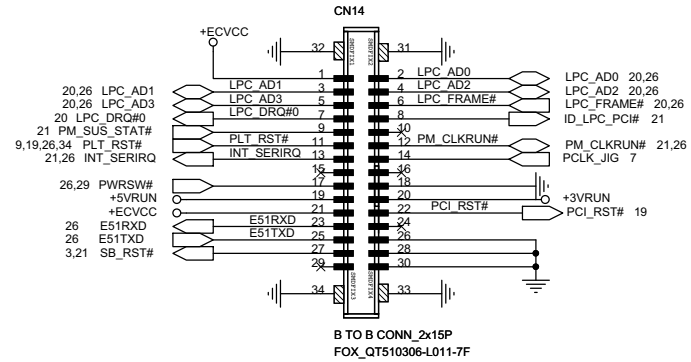
X-Build 2009.10.12  
Disabled external SPI ROM boot function and changed part value as below.  
From Mount to NC : U30,C643,R267,CN13  
From NC to Mount : R566



EXTERNAL SPI ROM INTERFACE



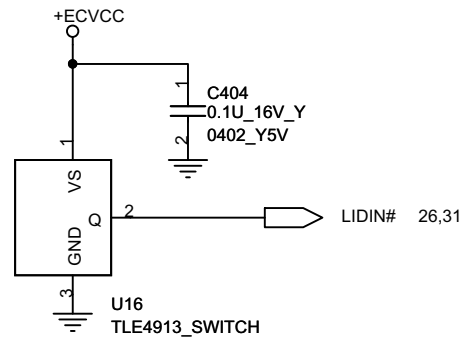
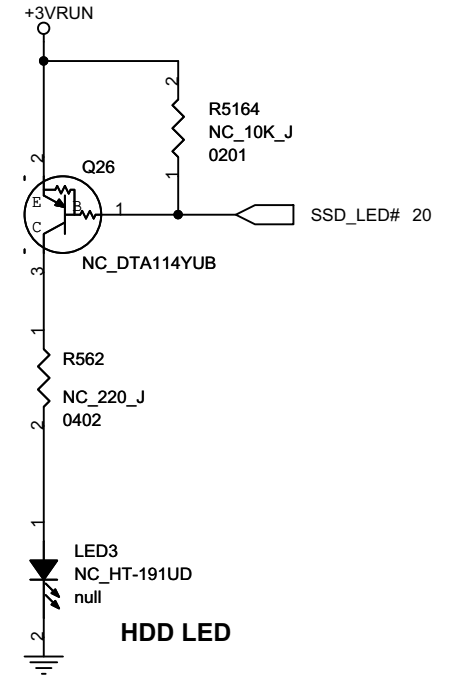
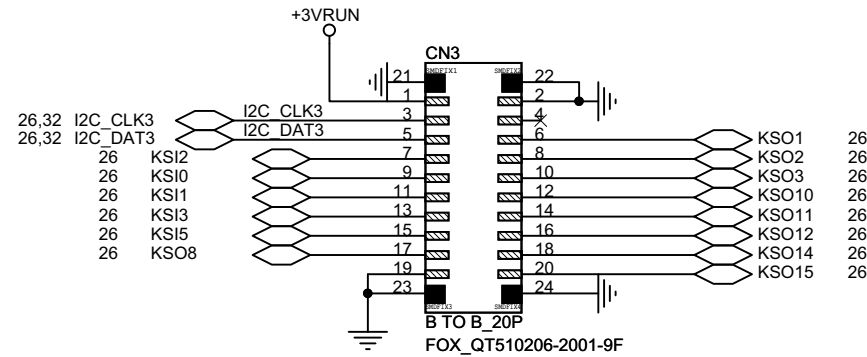
JIG-120



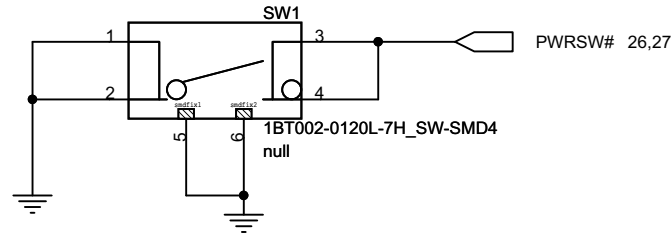
PT

Removed on board key pad design

## FUNCTION KEY CONN

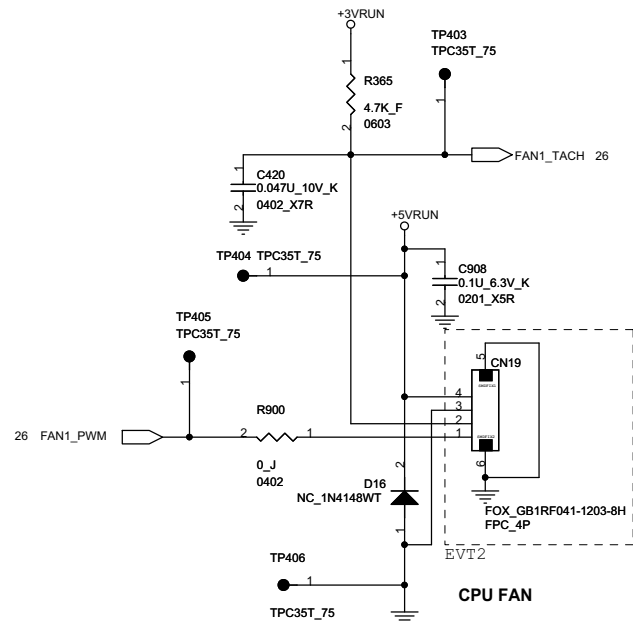
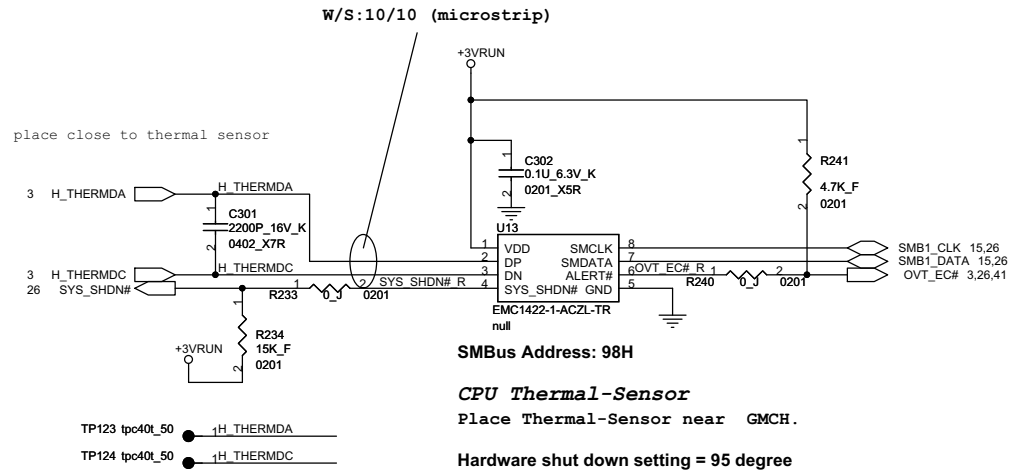


## LID SWITCH



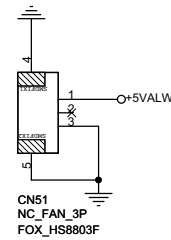
## POWER BOTTON



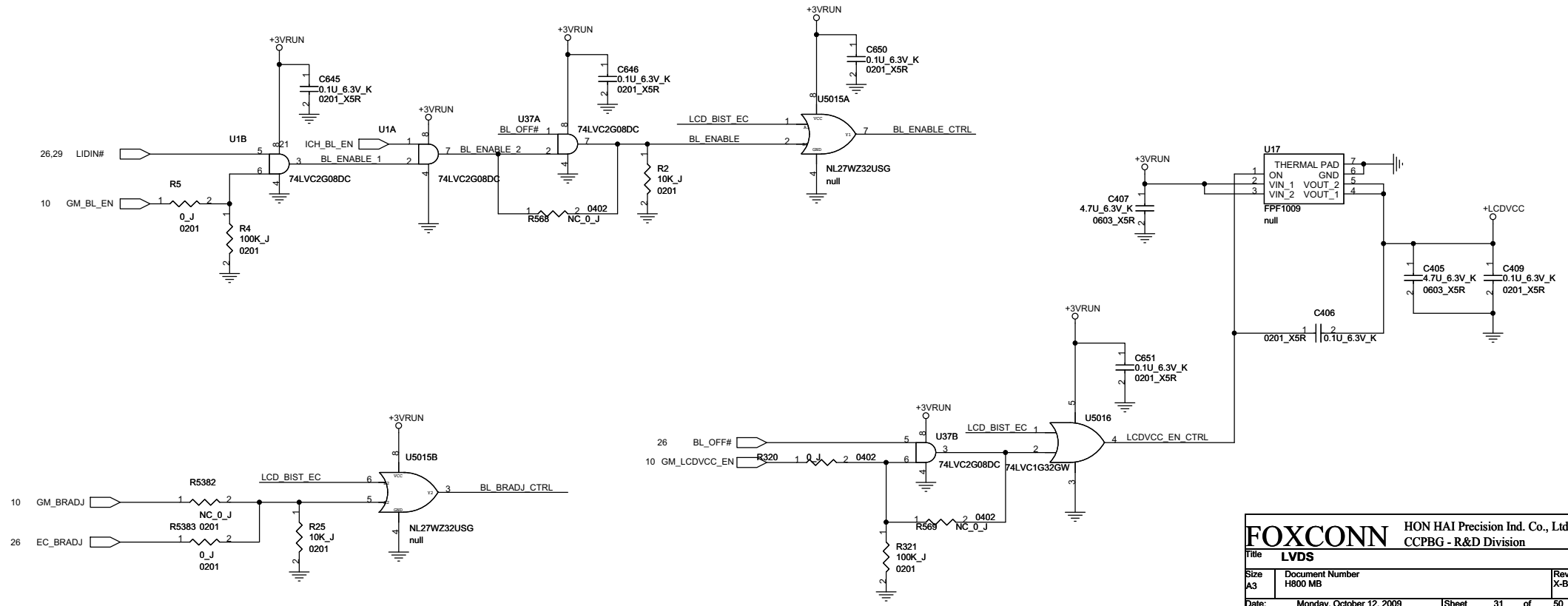
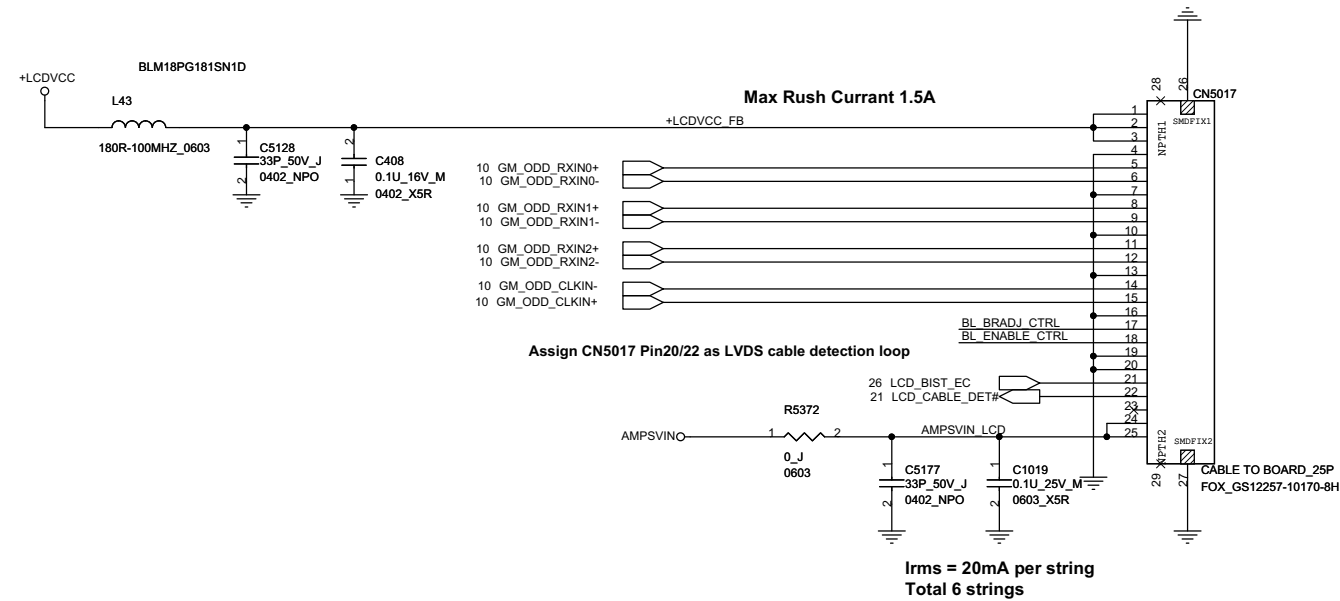


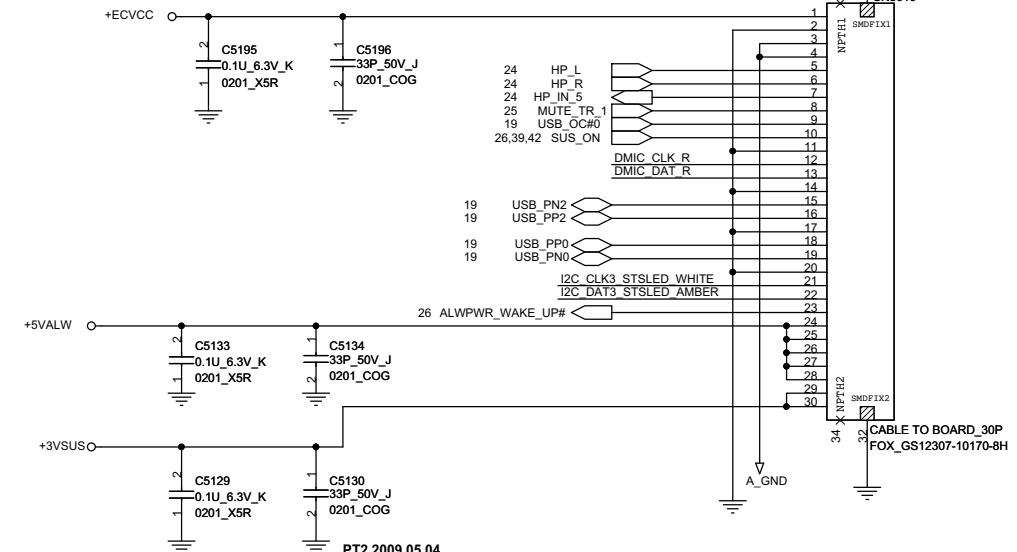
TP403~TP406 BFT FAN test point for TE request  
Please put on the bot side

CN51 for test FAN power



X-Build 2009.10.12  
Disabled test fan function and changed part value for CN51 from Mount to NC.



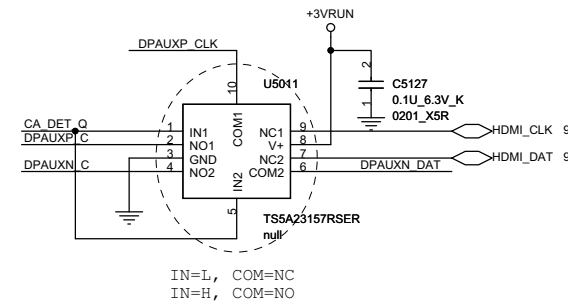


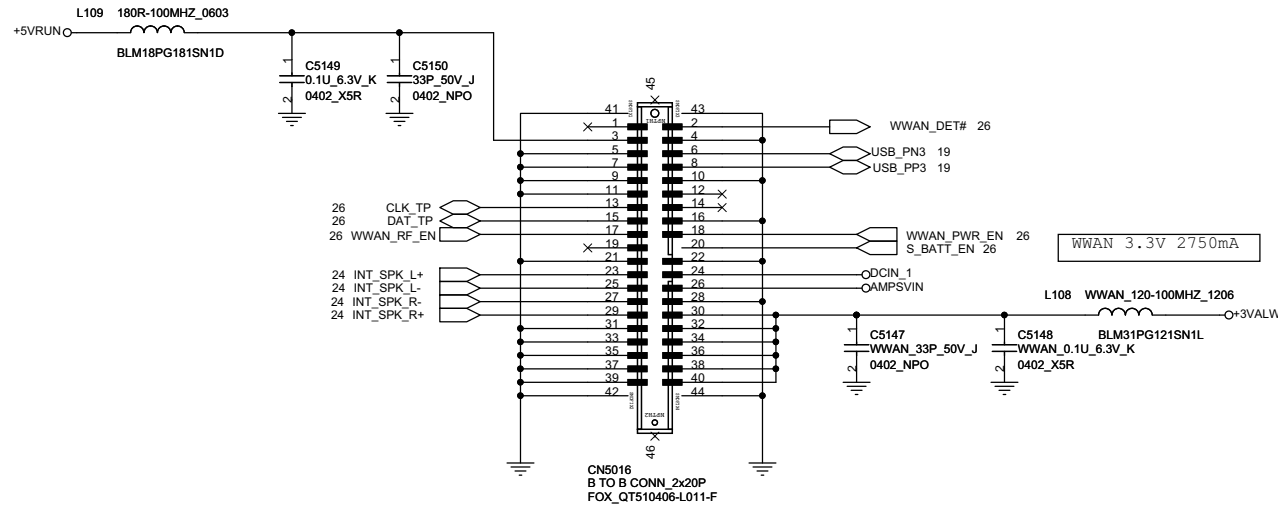
24 DMIC\_CLK R5173 1 0 2 4002 DMIC\_CLK\_R

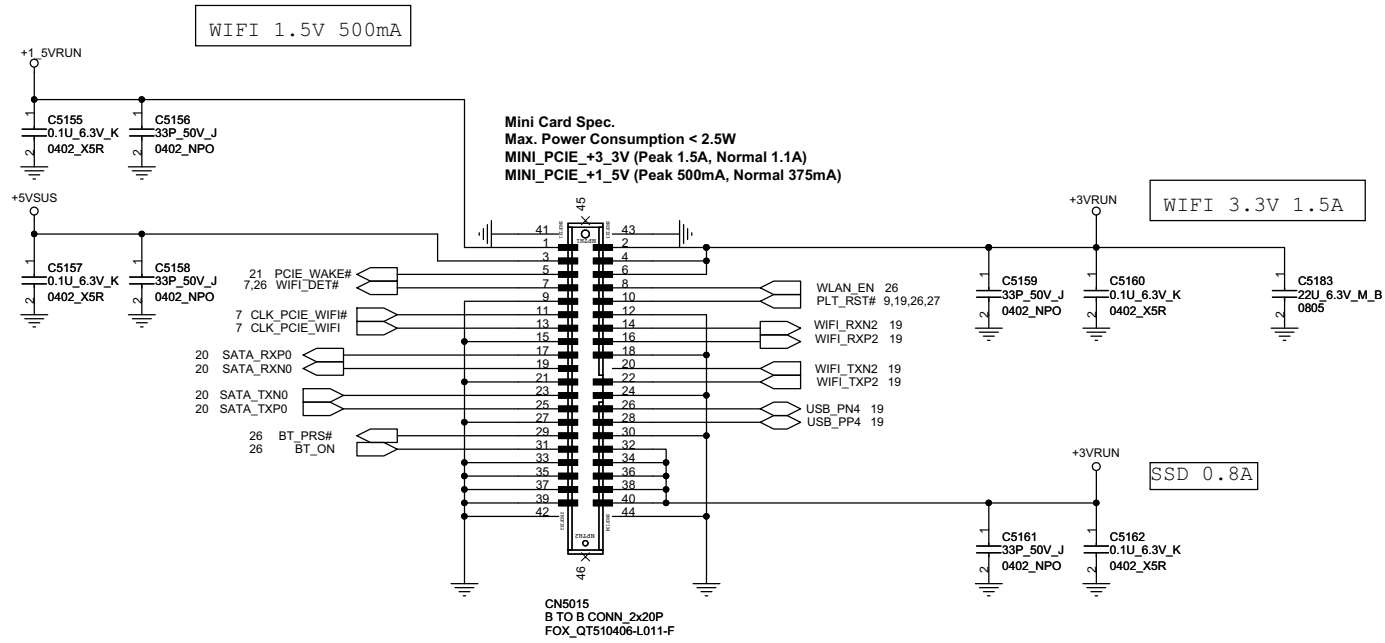
24 DMIC\_DAT R5174 1 0 2 4002 DMIC\_DAT\_R

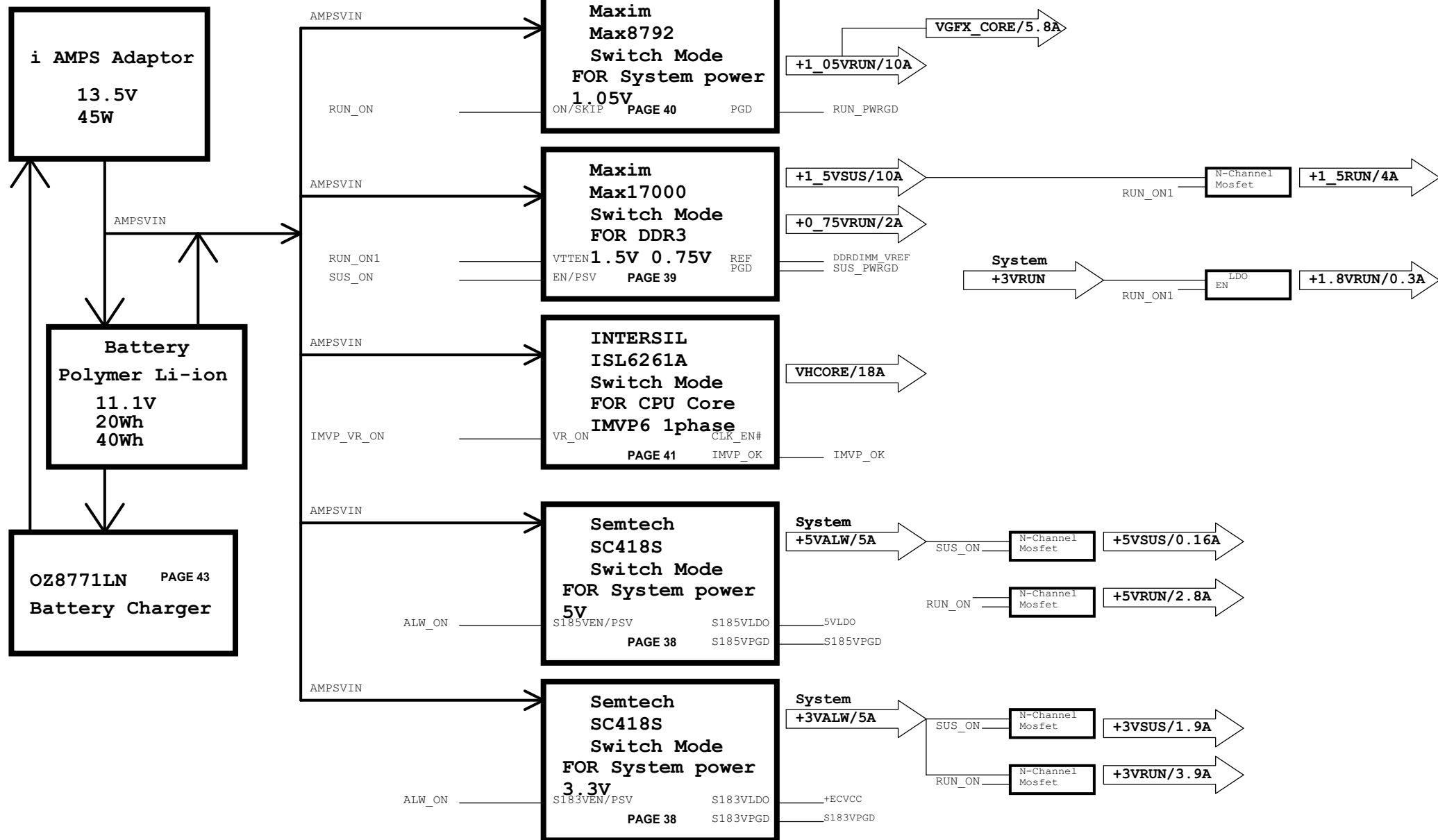
C5137 NC\_0.1U\_6.3V\_K 0201\_X5R

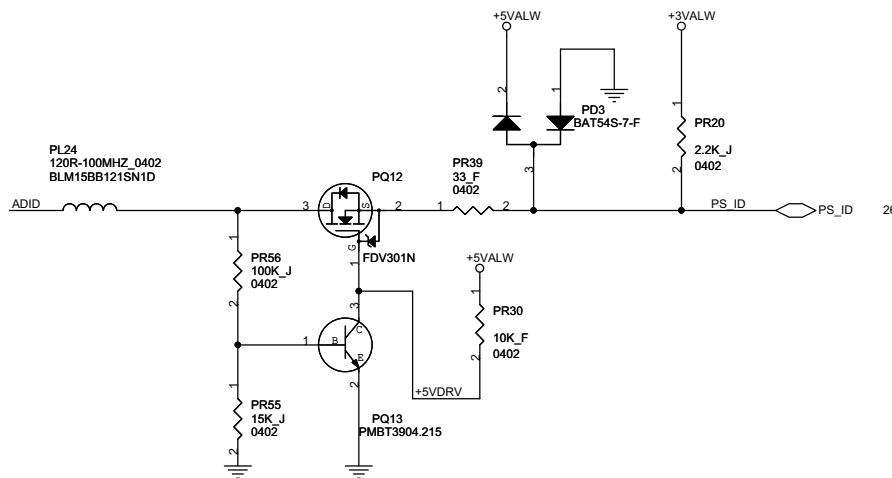
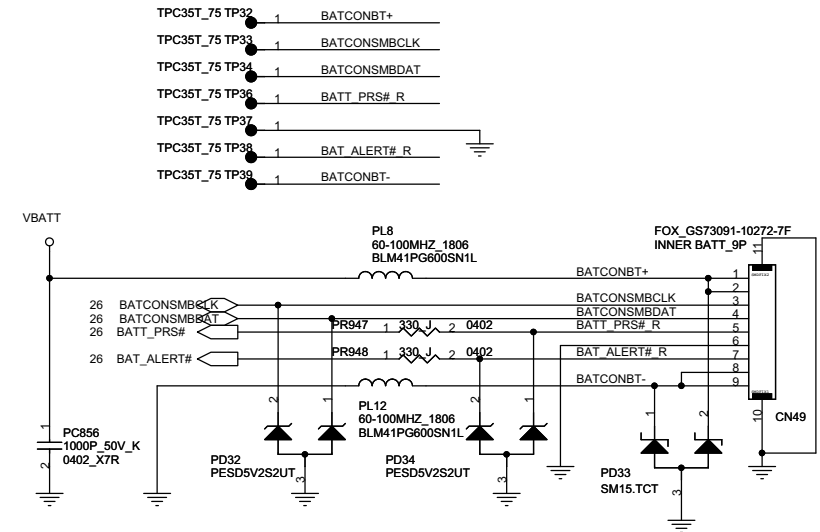
C5138 NC\_0.1U\_6.3V\_K 0201\_X5R



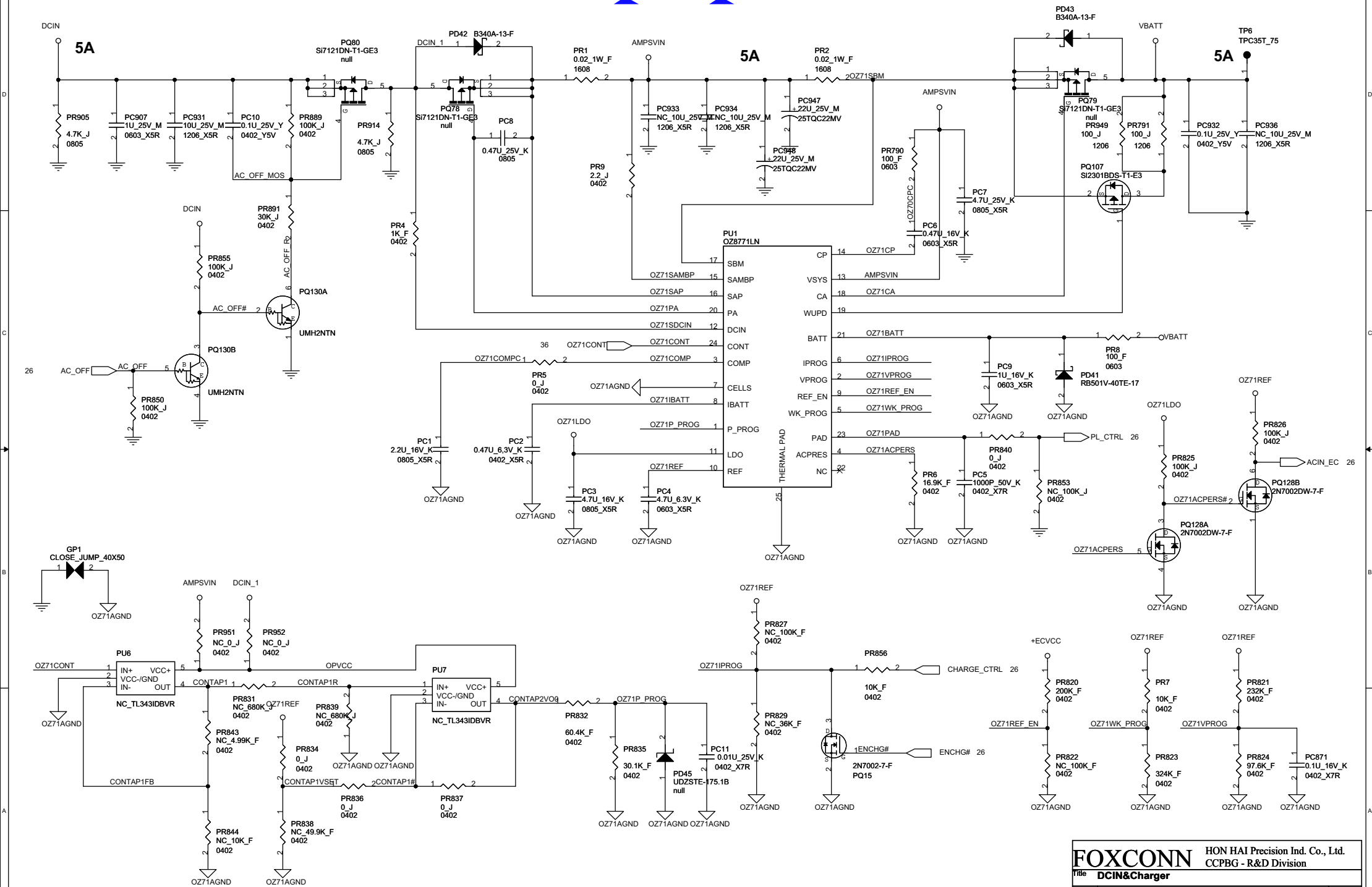


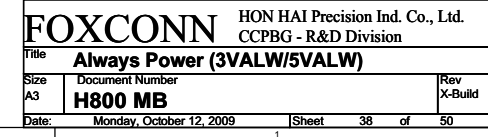


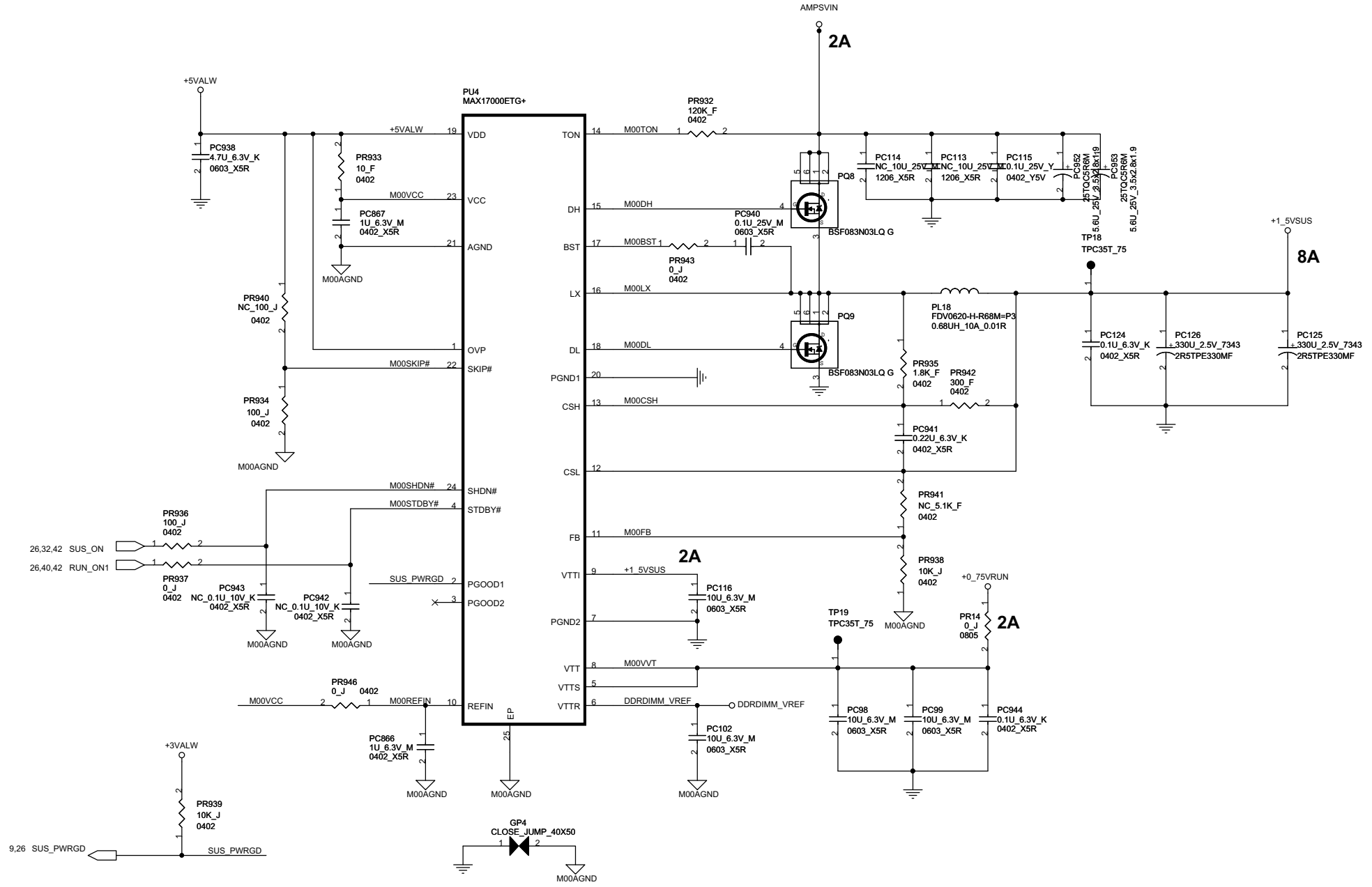




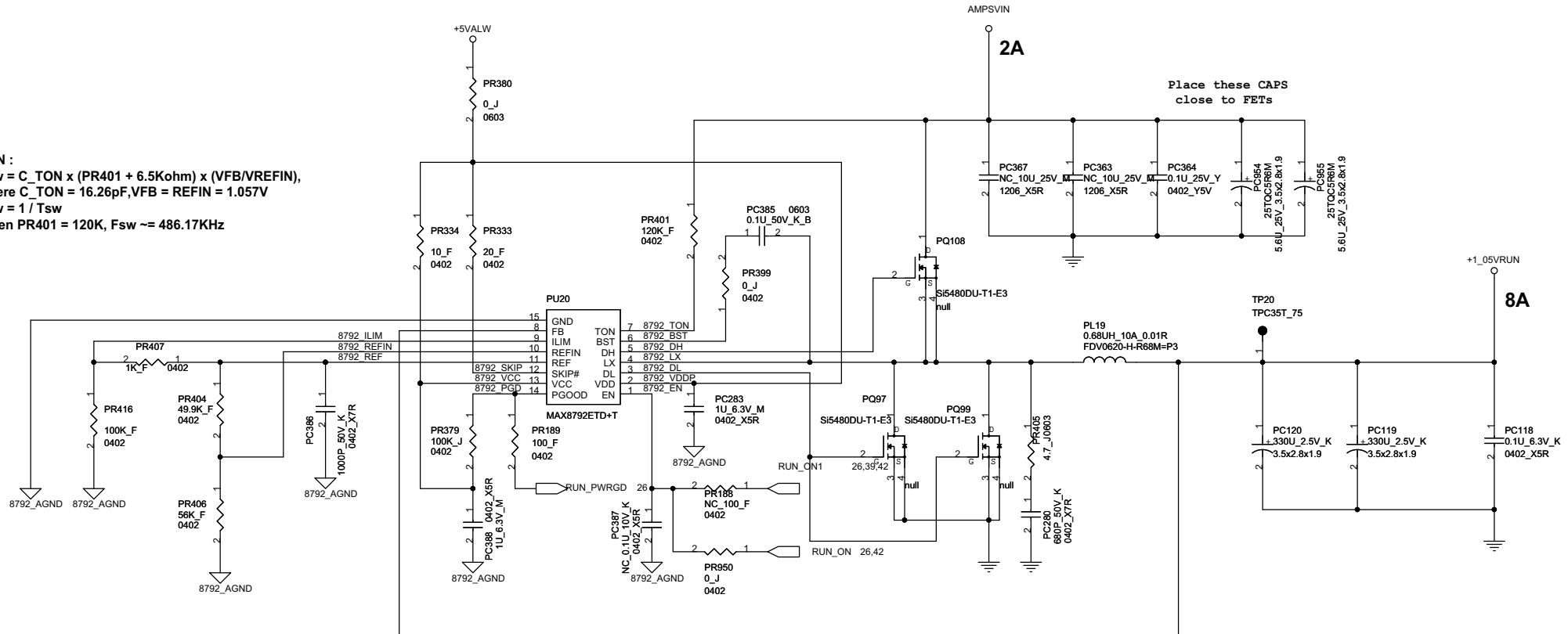








TON :  
 $T_{sw} = C_{TON} \times (PR401 + 6.5K\Omega) \times (V_{FB}/V_{REFIN})$ ,  
 where  $C_{TON} = 16.26pF$ ,  $V_{FB} = REF_{IN} = 1.057V$   
 $F_{sw} = 1 / T_{sw}$   
 When  $PR401 = 120K$ ,  $F_{sw} \approx 486.17KHz$



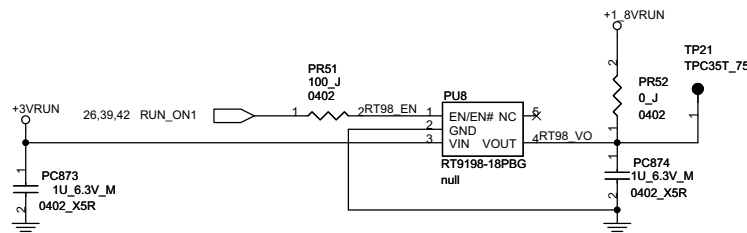
Choose  $I_{LOAD} = 10A$ . So  $I_{peak} = 11.47A$ ,  $I_{valley} = 8.53A$   
 $V_{LIM} = 8.53A \times R_{ds} = 85.3mV$ , where  $R_{ds} = 20m\Omega/2 = 10m\Omega$   
 Choose  $PR416 = 100K$ . So  $PR407 = PR416 \times ((0.1 / V_{LIM}) - 1) \approx 1K$   
 Set Valley Current Limit Threshold =  $85.3mV / 10m\Omega = 8.53A$

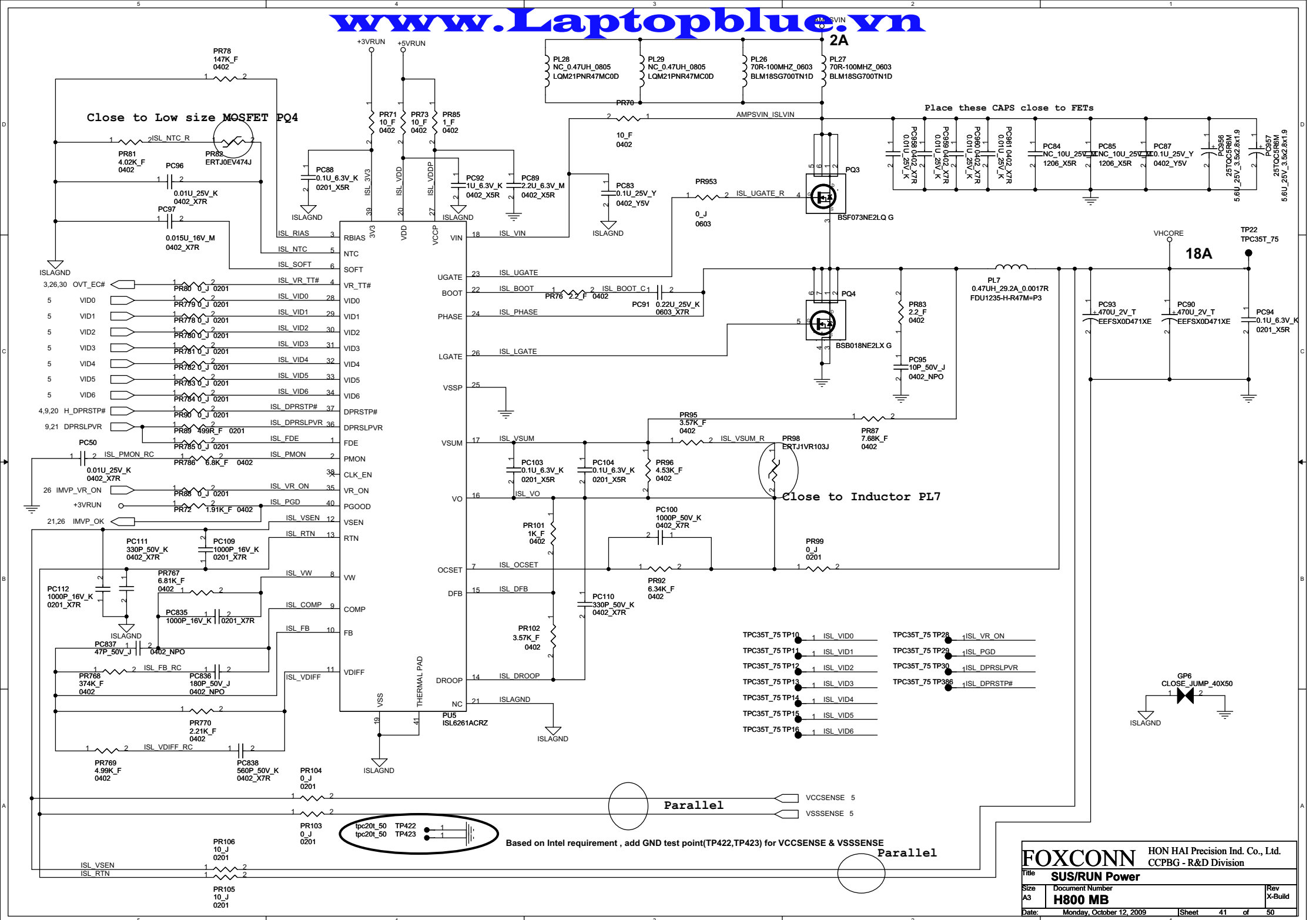
REFIN and FB :

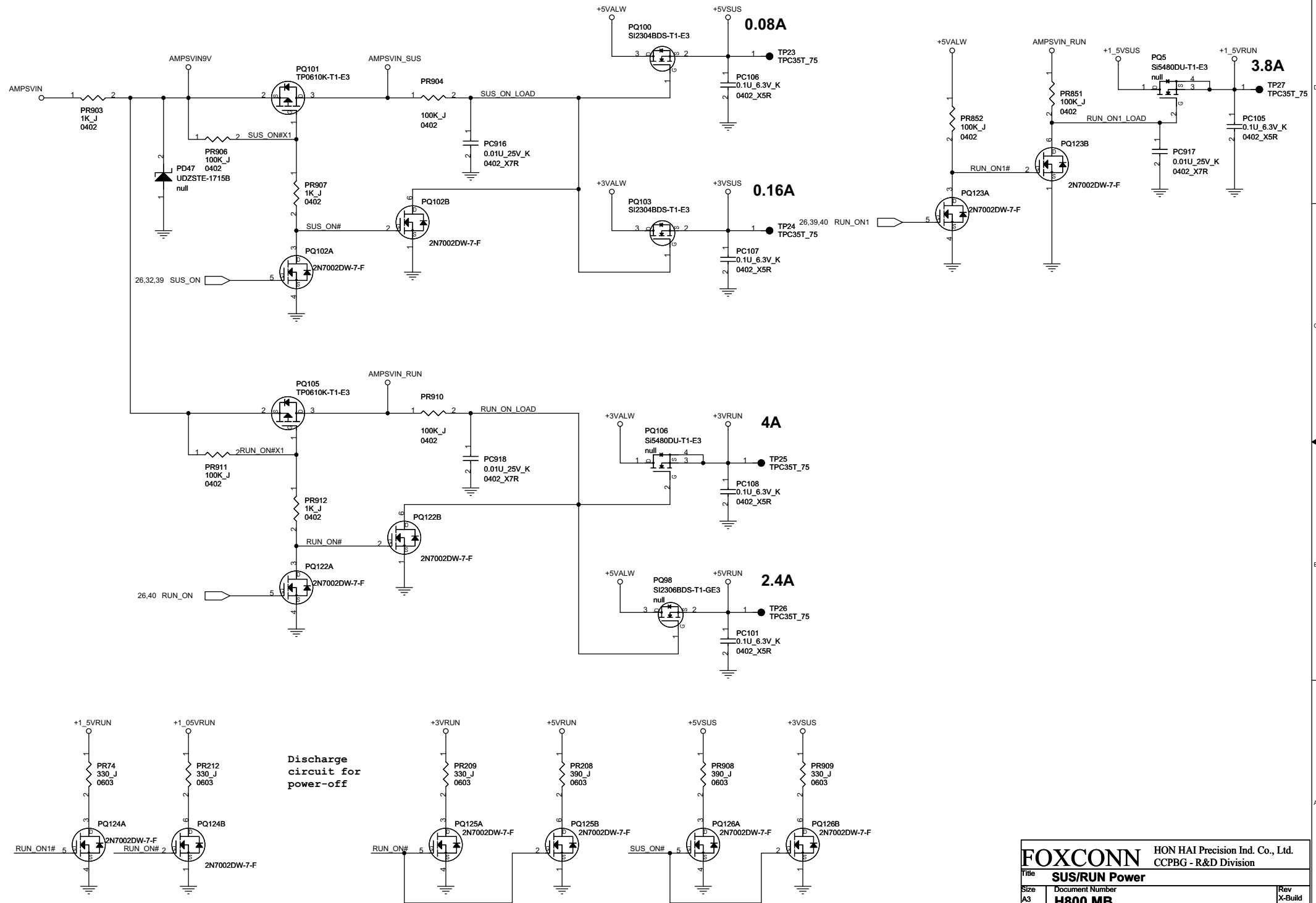
1. FB TO Output => output voltage less than 2V.
2. REFIN voltage determines SMPS output.  
 $V_{REFIN} = 2V \times PR406 / (PR406 + PR404) = 1.057V$

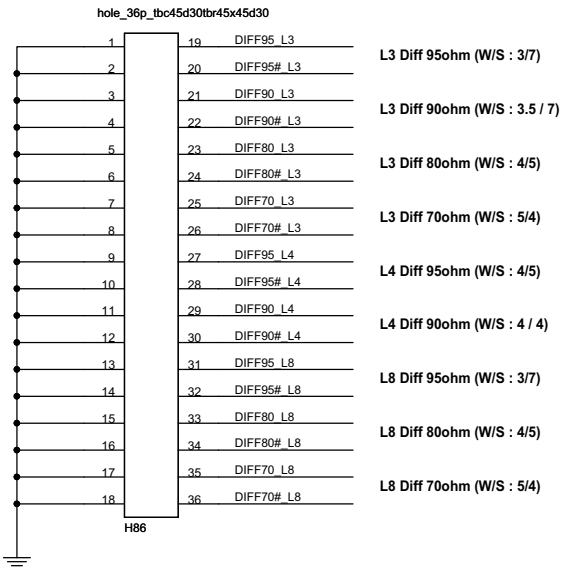
SKIP#:

- SKIP# TO VDD => forced PWM mode
- SKIP# TO REF => pulse-skipping mode with forced-PWM during transitions.
- SKIP# TO OPEN => ultrasonic mode
- SKIP# TO GND => pulse-skipping mode

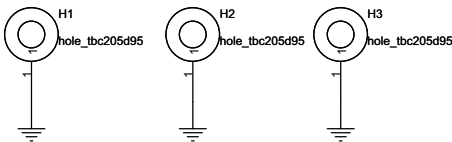




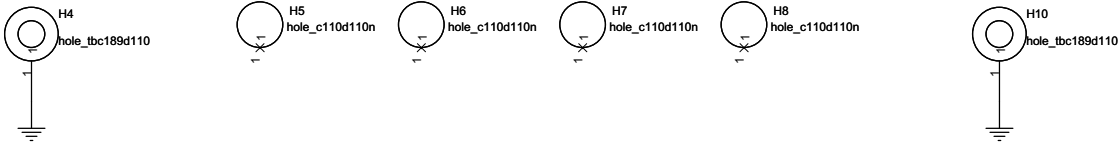




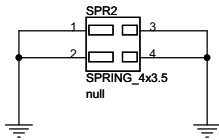
Type A\*3PCS



Type B\*6PCS



Type C\*2PCS





Page 7. Add R5159,R5160 for crystal accuracy test. Delete clocks for IAN chip Page 9. Pull down DDC_CTRLDATA for DisplayPort strapping Add R5162,R5163 for 1.5V CMOS SR_WDRG signal. Page 20. Delete SATA1 signals. Page 26. Change R292 from 10k to 470k. Page 29. Add R5164 10k PU on SATA_LED+. Page 30. Add CN13 connector for CPU fan. Page 32. Add U5011 for dual mode DP Aux/HDMI DDC switch.	2008/0905 1.Update Power schematic  2008/0908  Page9,15,16 addition ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 2 RANK Page 18 Addition RP54 for 2 RANK Page 31 Addition C5128,RP50-RP53 For RF team request Page 32 Addition C5129,C5130,C5131,C5132,C5134,C5135,C5136,C5137,C5138,C5139,R5173,R5174 for RF team request	2008/0905 1.Update Power schematic  2008/0908  Page9,15,16 addition ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 2 RANK Page 18 Addition RP54 for 2 RANK Page 31 Addition C5128,RP50-RP53 For RF team request Page 32 Addition C5129,C5130,C5131,C5132,C5134,C5135,C5136,C5137,C5138,C5139,R5173,R5174 for RF team request	2008/0905 1.Update Power schematic  2008/0908  Page9,15,16 addition ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 2 RANK Page 18 Addition RP54 for 2 RANK Page 31 Addition C5128,RP50-RP53 For RF team request Page 32 Addition C5129,C5130,C5131,C5132,C5134,C5135,C5136,C5137,C5138,C5139,R5173,R5174 for RF team request
Page 18 . DDR3 termal resistance Swap for layout RP49.4 M_CKE1 RP49.3 M_A_A1 RP49.2 M_A_A12 RP49.1 M_A_A2 RP49.4 M_A_B52 RP49.3 M_A_RAS# RP49.2 M_A_CAS# RP49.1 M_A_A9 RP49.4 M_A_A5 RP49.3 M_A_A3 RP49.2 M_A_A7 RP49.1 M_A_B50 RP49.4 M_ODT1 RP49.3M_A_A0 RP49.2M_A_A13 RP49.1M_A_MER# RP54.4 M_ODT0 RP54.3 M_CD#1 RP54.2 M_CD#0	2008/0916 Page 4 ADD TEST POINT TP320_forH_DPSP# Page 8 ADD TEST POINT TP321--TP342 Page 11 DEL TEST POINT TP188-TP192 Page 19 (1)ADD TEST POINT TP343 for CLK_ICHPCI (2)U33 change package to 13-W25X80A-7000	2008/0916 Page 4 ADD TEST POINT TP320_forH_DPSP# Page 8 ADD TEST POINT TP321--TP342 Page 11 DEL TEST POINT TP188-TP192 Page 19 (1)ADD TEST POINT TP343 for CLK_ICHPCI (2)U33 change package to 13-W25X80A-7000	2008/0916 Page 4 ADD TEST POINT TP320_forH_DPSP# Page 8 ADD TEST POINT TP321--TP342 Page 11 DEL TEST POINT TP188-TP192 Page 19 (1)ADD TEST POINT TP343 for CLK_ICHPCI (2)U33 change package to 13-W25X80A-7000
For RF suggestion Page 6 C835,C836,C236,C237,C238 change to 0201 SIZE Page 13 ADD C5139,C5140 Page 18 ADD C5141-C5144 Page 22 ADD C5145 Page 24 ADD C5146 Page 33 ADD C5147-C5154 ,ADD L109-L111 Page 34 ADD C5155-C5164	2008/0917 (1)Page 22 Change U38 from G9131-15T73UF to RT9170-15VP (2)Page 10 Add R5176-R5177	2008/0917 (1)Page 22 Change U38 from G9131-15T73UF to RT9170-15VP (2)Page 10 Add R5176-R5177	2008/0917 (1)Page 22 Change U38 from G9131-15T73UF to RT9170-15VP (2)Page 10 Add R5176-R5177
Page 33 CN5016 PIN 31_PIN33 SWAP for layout route Page 13 DEL CAP5 for layout space Page 32 CN5019 power pin 1 from +5VSUS to +3VSUS Pin2 from +5VALWS to +5VALW Page 15,16 U62-U69 Change SDRAM from Qimonda(78ball) to Sumaung 1G (82 Ball) Page 18 Addition C5165,C5166,R5175,R5176 for 2 rank	2008/0918 Page 10 R5176,R5177 Change to 10k Page 32 CN5016 Pin6 change to GND Page 24 Q5021 Change to 17-2N7002A-7000 ADD LED DEL R323,R219 Page 26 DEL R300,R277,R299,R282	2008/0918 Page 10 R5176,R5177 Change to 10k Page 32 CN5016 Pin6 change to GND Page 24 Q5021 Change to 17-2N7002A-7000 ADD LED DEL R323,R219 Page 26 DEL R300,R277,R299,R282	2008/0918 Page 10 R5176,R5177 Change to 10k Page 32 CN5016 Pin6 change to GND Page 24 Q5021 Change to 17-2N7002A-7000 ADD LED DEL R323,R219 Page 26 DEL R300,R277,R299,R282
2008/0911A 1600 Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0 Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR0 to M_CLK_DDR#1,M_CLK_DDR1	2008/0918A Page 34 Change C5156,C5158,C5164,C5159,C5161 to 0402 10p	2008/0918A Page 34 Change C5156,C5158,C5164,C5159,C5161 to 0402 10p	2008/0918A Page 34 Change C5156,C5158,C5164,C5159,C5161 to 0402 10p
2008/0911B-1700 Page 33 CN5016 change to FOX_QT510406-L011-F Page 34 CN5015 change to FOX_QT510406-L011-F	2008/0919 1.Page 26 ADD TEST POINT TP322-TP382 2.Page 7 ADD TEST POINT TP366 3.Page 9 ADD TEST POINT TP367  2008/0919A 1.Page 35-43 Update Power schematic  2008/0919B 1.Page 21 DEL U3,C21	2008/0919 1.Page 26 ADD TEST POINT TP322-TP382 2.Page 7 ADD TEST POINT TP366 3.Page 9 ADD TEST POINT TP367  2008/0919A 1.Page 35-43 Update Power schematic  2008/0919B 1.Page 21 DEL U3,C21	2008/0919 1.Page 26 ADD TEST POINT TP322-TP382 2.Page 7 ADD TEST POINT TP366 3.Page 9 ADD TEST POINT TP367  2008/0919A 1.Page 35-43 Update Power schematic  2008/0919B 1.Page 21 DEL U3,C21
2008/0912 Page 3 Change test point for FSB each group long and short trace length TP73 H_A#4 -->H_A#14 TP74 H_A#10 -->H_A#16 TP75 H_A#17 -->H_A#29 TP76 H_A#20 -->H_A#35 TP77 H_D#8 -->H_D#11 TP81 H_D#29 -->H_D#17 Page 31 ADD LVDS TEST POINT TP320-TP327	2008/0912A Page9,15,16 DEL ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 1 RANK Page 18 1.DEL RP54 for 1 RANK 2. DDR3 termal resistance Swap back for layout Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0 Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR1 to M_CLK_DDR#1,M_CLK_DDR0 Page 44 Addition H1-H23 HOLE	2008/0912A Page9,15,16 DEL ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 1 RANK Page 18 1.DEL RP54 for 1 RANK 2. DDR3 termal resistance Swap back for layout Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0 Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR1 to M_CLK_DDR#1,M_CLK_DDR0 Page 44 Addition H1-H23 HOLE	2008/0912A Page9,15,16 DEL ODT1,CS#1,CKE1,ZQ1A-ZQ8A and R5165-R5172 for 1 RANK Page 18 1.DEL RP54 for 1 RANK 2. DDR3 termal resistance Swap back for layout Page 15, Change U68,U69 CLK from M_CLK_DDR#1,M_CLK_DDR1 to M_CLK_DDR#0,M_CLK_DDR0 Page 16, Change U62,U63 CLK from M_CLK_DDR#0,M_CLK_DDR1 to M_CLK_DDR#1,M_CLK_DDR0 Page 44 Addition H1-H23 HOLE
2008/0920 1.Update Power schematic page35-43	2008/0922 1.Page 7 C339 from 0.1uf change to 33pf for RF suggestion 2.Page 7 ADD C5168 for RF suggestion  2008/0923A 1.Page 24 DEL MIC_L_MIC_R_net,MIC1_VREF0_L_MIC1_VREF0_R  2008/0924 1.Page 26 update ec schematic,Del R273,R274,ADD C5176 2.Page 9 DEL TP384 3.Page 31 ADD C5177 33pf 4.Page 12 ADD C5169-C5170 33pf 5.Page 22 ADD C5172-C5175 33 pf 6.Page 6 C835,C836,C236,C237,C238 from 0.1u change to 33pf 7.Page 18 C5141-C5144 from 0.1u change to 33pf 8.Page 24 C5146 from 0.1u change to 33pf 9.Page 33 C5147,C5151,C5153,C5150 from 0.1u change to 33pf 10.Page 31 SWAP CN5017 pin 5, 8 11.Chagne Y5 from 4 pin to 2pin for height limit<2mm 2. DEL R866,R865,R864 DEL R234 form 33k to 15k for hardware shut seating 95 degree 4.Chagne R241 form 15k to 4.7k for hardware shut seating 95 degree	2008/0922 1.Page 7 C339 from 0.1uf change to 33pf for RF suggestion 2.Page 7 ADD C5168 for RF suggestion  2008/0923A 1.Page 24 DEL MIC_L_MIC_R_net,MIC1_VREF0_L_MIC1_VREF0_R  2008/0924 1.Page 26 update ec schematic,Del R273,R274,ADD C5176 2.Page 9 DEL TP384 3.Page 31 ADD C5177 33pf 4.Page 12 ADD C5169-C5170 33pf 5.Page 22 ADD C5172-C5175 33 pf 6.Page 6 C835,C836,C236,C237,C238 from 0.1u change to 33pf 7.Page 18 C5141-C5144 from 0.1u change to 33pf 8.Page 24 C5146 from 0.1u change to 33pf 9.Page 33 C5147,C5151,C5153,C5150 from 0.1u change to 33pf 10.Page 31 SWAP CN5017 pin 5, 8 11.Chagne Y5 from 4 pin to 2pin for height limit<2mm 2. DEL R866,R865,R864 DEL R234 form 33k to 15k for hardware shut seating 95 degree 4.Chagne R241 form 15k to 4.7k for hardware shut seating 95 degree	2008/0922 1.Page 7 C339 from 0.1uf change to 33pf for RF suggestion 2.Page 7 ADD C5168 for RF suggestion  2008/0923A 1.Page 24 DEL MIC_L_MIC_R_net,MIC1_VREF0_L_MIC1_VREF0_R  2008/0924 1.Page 26 update ec schematic,Del R273,R274,ADD C5176 2.Page 9 DEL TP384 3.Page 31 ADD C5177 33pf 4.Page 12 ADD C5169-C5170 33pf 5.Page 22 ADD C5172-C5175 33 pf 6.Page 6 C835,C836,C236,C237,C238 from 0.1u change to 33pf 7.Page 18 C5141-C5144 from 0.1u change to 33pf 8.Page 24 C5146 from 0.1u change to 33pf 9.Page 33 C5147,C5151,C5153,C5150 from 0.1u change to 33pf 10.Page 31 SWAP CN5017 pin 5, 8 11.Chagne Y5 from 4 pin to 2pin for height limit<2mm 2. DEL R866,R865,R864 DEL R234 form 33k to 15k for hardware shut seating 95 degree 4.Chagne R241 form 15k to 4.7k for hardware shut seating 95 degree
2008/0925 1.Update Power schematic page35-43	2008/0925 1.Page 7 ADD R for Silago special function 2.Page 24 ADD C5178,C5179 3.Page 34 Change C5156,C5158,C5164,C5159,C5161 form 10PF(0402) to 33PF (0201) 4.Page 26 update EC schematic 5.Page 15 Change U71 STTS424E02BDN3F to STTS424CDA3F Page 31 DEL U71,ADD R5336,R5337,R5335_Q5023,Q5024	2008/0925 1.Page 7 ADD R for Silago special function 2.Page 24 ADD C5178,C5179 3.Page 34 Change C5156,C5158,C5164,C5159,C5161 form 10PF(0402) to 33PF (0201) 4.Page 26 update EC schematic 5.Page 15 Change U71 STTS424E02BDN3F to STTS424CDA3F Page 31 DEL U71,ADD R5336,R5337,R5335_Q5023,Q5024	2008/0925 1.Page 7 ADD R for Silago special function 2.Page 24 ADD C5178,C5179 3.Page 34 Change C5156,C5158,C5164,C5159,C5161 form 10PF(0402) to 33PF (0201) 4.Page 26 update EC schematic 5.Page 15 Change U71 STTS424E02BDN3F to STTS424CDA3F Page 31 DEL U71,ADD R5336,R5337,R5335_Q5023,Q5024
2008/0926 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53
2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP51,RP52,RP53	2008/0926B 1.DEL RP50,RP

2008/11/21  
Page 36  
1. Change SPI\_ROM\_SDI from U36 pin 102 to pin 103 to fix EVT2 wrong connection  
2. Change SPI\_ROM\_SDO from U36 pin 103 to pin 102 to fix EVT2 wrong connection  
3. Change  
R310, R270, R534, R304, R532, R297, R563, R286, R561, R5364, R287, R560, R5365, R867, R868, R279, R284, R294 from 0201 to 0402 for product yield  
4. DEL R5361, R5357 and remove FN\_INT#  
Page35~43 Update Power schematic  
Change PQ4 from 17-1RF6631-TR00 to 17-BSB018N-E200  
Change PQ3 from 17-1RF6638-PB00 to 17-BSF073N-E200  
Change PQ8,PQ9 from 17-1RF6638-PB00 to 17-BSF083N-0300  
Change PR905 from 1R-000015-F200 to 1R-0001271-F200  
Change PR407 from 1R-0000183-F200 to 1R-0000153-F200  
Add part PD42 (From NC to 16-B340A13-F000)  
Change PR6 from 1R-0001652-F200 to 1R-0001692-F200  
Change net name from M00OVP to +5VALW  
Change net name from M001D8VVOUT to + +1\_5VSUS\_1.  
Change PR846 From 1R-0000104-F300 to 1R-0000303-F200  
Add PD34 16-PESD5V2-S200 for EC ESD

2008/11/24  
Page 36  
1.ADD L117 for ECVCVC

2008/12/1  
1. Change EC and audio part  
R5324, R537, R5341, R275, R526, R524, R525, R550, R267, R566, R283, R5157, R5156, R5149, R5144, R5150, R5174, R5152, R5173, R5147, R5141, R5137, R5138, R5155, R5153, R5154 from 0201 to 0402 for product yield

2008/12/1A  
1. ADD TEST POINT TP398~TP406 for BFT test point  
2. Change  
R481, R480, R486, R485, R483, R490, R489, R493, R512, R513, R517, R5343, R494, R503, R501, R5352, R5353, R491, R492, R495, R502, R19, R565, R308, R309, R306 from 0201 to 0402 for product yield

2008/12/1B  
1. Change C5161, C5162, C5163, C5164, C5159, C5160, C5155, C5156, C5158, C5157, C5148, C5147, C5151, C5152, C5153, C5154, C5149, C5150 from 0201 to 0402 for product yield

2008/12/07  
1. SWAP P56 pin2 and pin5  
2. SWAP U32 pin102 and pin103

2008/12/08  
1. Update block diagram  
2. DEL on board Key pad

2008/12/22  
Page 22  
1. ADD RP50,RP51 for EC keyboard pull up  
Page19  
2. Change RP35,RP2,RP36,RP4,RP4,RP3,RP6,RP42,RP37 from 0201\_8P4R to 0804\_8P4R  
3. DEL PWR LED and Status LED circuit  
DEL Q5024,R5358, R5359, Q5023, Q54, R703, R705, Q52, R707, LED1, R5360, Q15, R317, R318, Q16, R18, R322, R319, Q17, Q20, R324, R315  
4. Remove UWB circuit  
DEL R5342, C52, C46  
5. Change R5358 from 0201 to 0402 for product yield  
6. Change L117 from 0402 to 0603 for +ECVCVC

2008/12/22A  
Page 21  
Change RP7,RP1 from 0201\_8P4R to 0804\_8P4R  
Page 12  
ADD CAP8

2008/12/23  
1. ADD Port to EC keyboard to FN key signal  
2. DEL USB Port5  
3. DEL Fujst Power solution

2008/12/24  
1. Change H4,H5,H6,H7,H8,H9,H10,H11 to 2.5mm(1X-HOLE000-0835)

2008/12/25  
1. Change CN5018 TMDs and power Pin define for layout route

Pin NET

14 TMDs\_L2#\_C  
15 TMDs\_L2\_C  
17 TMDs\_L0#\_C  
18 TMDs\_L0\_C  
20 TMDs\_L3\_C  
21 TMDs\_L3#\_C  
23 TMDs\_L1\_C  
24 TMDs\_L1#\_C

2. Remove DMA speaker function ,Del SPK\_DMA\_L,SPK\_DMA\_R signal

3. Change CN5019 pin define for layout route  
4. ADD R5366 100k pull down RES for fix HP detect floating issue  
5. ADD C5195, C5196 for +ECVCVC

2008/12/25  
1. ADD SUS\_ON and RUN\_ON test point for SI

2008/12/29  
1. Change C301 from 0201 to 0402 for material prepare issue

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1. Change CN50 from FOX\_GST73091-10272-7F to FOX\_GST73061-10272-7F,  
2. Add PL25.  
3. Add power test Pad TP32,TP33,TP34,TP36,TP37,TP38,TP39.  
4. CHANGE From 1C-2B60106-M300 to 1C-2B60106-M001 for Derating issue.  
5. Add PR18,PR19,PR21,PR23,PR24 for Derating issue

DVT 20090105A  
Change Power source for CN5019 Pin29&30 from +3VALW to +3VSUS

DVT 20090106  
(1)Follow ME request to change B type Hole from 1X-HOLE000-0835 to 1X-HOLE000-0974 (H4,H5,H6,H7,H8,H9,H10,H11)  
(2)For EMI concern , add L118 & L119 for LIO power source and add L120 & L121 for RIO power source

20090109  
Update Power schematic (Waiting for PWR change list)

20090109  
Change Net name from SMB2\_CLK/SMB2\_DATA to BATCONSMBCLK/BATCONSMBDAT

20090112  
(1)The EMI test result is PASS after SS enable , cancel L118/L119/L120/L121  
(2)Add TP415 for RTC Power  
(3)Change part for U571 from 15-STTS424-0001 to 15-STTS424-NA00  
(4)Assign CN607 Pin20/22 as LCD cable detection loop  
Implement LVDS cable detection function , delete TP365 and add LCD\_cable\_Det# input for U36-Pin73(GPI7)  
(Add RS387 to pull up for LCD\_Cable\_Det#)

2008/01/13  
1. Delete Control ACIN OCP protect, EC Include  
2. Delete PSID Circuit, follow H830 [Phelps]  
3. Change 1.05VRUN/1.5VSUS power budget 10A to 8A

DVT2009.01.14  
Follow SW suggestion to change LCD\_Cable\_Det# from U36-Pin73(GPI7) to SB GPIO1 and delete R5367 pull up resistor.

DVT 2009.01.16  
(1)For L6 DFM concern , change RP5 from 1R-1010822-JX00 to 2pcs 1R-0000822-J100(R5367&R5368).  
(2)Based on the Crystal test result , change R554 from 1R-0000000-J200(0 ohm) to 1R-0000224-F200(220K ohm)  
(3)Chaned CN5018&CN5019 from 1N-0030007-FK60 to 1N-0030009-FK60 for Halogen Free purpose.

DVT 20090116-1  
Follow ME request to delete H9  
DVT 20090119  
(1)For TE test request , add TP416 for +VCC, SUS\_HDA  
(2)For TE test request , add TP417 for VDDA  
(3)To fix BIOS timer issue , change part for C412&C416 from 1C-2N20100-J000 to 1C-2N20180-J000.

DVT 20090120  
Due to change WWAN LDO solution , cancel unnecessary +5VALW power source for CN5016

DVT 20090121  
Follow ME Connector list to change CN22 from 1N-1204002-0000 to 1N-1204009-0000

DVT 20090121A  
To fix OS timer accuracy issue change part solution as below.  
(1)Y4 from 1F-X14M318-3001 to 1F-X14M318-2001.  
(2)C592&C596 from 1C-2N20230-J000 to 1C-2N20270-J000

DVT 2009/01/22  
Change signal from A\_GND to GND for CN5019 Pin4&7

DVT2009.02.02  
To fix Pure ShutDown(SYS\_SHDN#) accuracy issue.  
-- Implement Q5023(2N7002-7-F) to instead to Q23B(MMDT3904-7-F)  
-- Implement Q5024(MMBT3904-7-F) to instead to Q23A(MMDT3904-7-F)

DVT 2009.02.05  
Follow Samsung PM680 SSD SPEC to enhance +3VRUN power and cancel +5VRUN power  
-- Changed CN5015 Pin36 from GND to +3VRUN  
-- Changed CN5015 Pin39 from +5VRUN to GND  
-- Due to cancel +5VRUN power , deleted C5163, C5164

DVT 2009.02.09  
Corect signal name for CN49 Pin3&4 from SMB2\_CLK/SMB2\_DATA to BATCONSMBCLK/BATCONSMBDAT

DVT 2009.02.12  
For ICT coverage request , change TP213,TP353,TP314,TP247 to 1X-TESTPT0-0032

DVT 2009.02.12A  
(1) Deleted P.J1,P.J3,PC846,PC847 for EMI  
(2) Change PQ107 from 17-TP610K1-E000 to 17-S12301B-DS00  
(3) Change PR791 from 0603 to 1206  
(4) Change PR7 from 1R-0002323-F200 to 1R-0000363-F200 Wake-up seting 9.4V  
(5)Added PR949 for DVT Derating  
(6)Deleted R880,R881,C1006 and canceled CLK\_PCIE\_UWB/CLK\_PCIE\_UWB#

PT 2009/02/18  
(1)To guarantee Power/Status LED can work normally when EC in Deep Sleep mode(ALW power will be off) , change the power source from +5VALW to S185VLD0 for CN5019 Pin28  
-- Added R5370 for S185VLD0 path  
-- Reserved R5369 for +5VALW path  
(2)To improve the Power sequency issue for +3VRUN/1\_1\_05VRUN , chaged the EN signal from RUN\_ON1 to RUN\_ON for +1\_05VRUN.  
-- Changed PR188,PC387 from mount to NC.  
-- Added PR950 for RUN\_ON control path.

2009.02.19  
(1)To fix battery low charge issue , changed PR2 from 1R-200500L-FB00(0.05ohm) to 1R-200200L-FB00(0.02ohm)  
(2)To reduce power consumption on battery mode , reserved DCIN\_1 power source for OPVCC  
-- Added PR951 for AMPSVIN power source select  
-- Reserved PR952 for DCIN\_1 power source select.

PT 2009.02.23  
(1)To save more layout spacing , cancelled below parts after confirm with RF team.  
(R5344~R5351 & C5184~C5191)  
(2)Reserved C5197 & C5198 for RF request.  
(3)Added R5371&R5372 for power consumption measurement

2009.02.23  
(1)Due to USB power source for P\_0 to USB\_6  
To guarantee it can work well on S5(battery only mode.)  
(2)Added TP418 & TP419 for SI request.

PT 2009.02.25  
(1)Added PC947/PC948 for acoustic issue  
(2)Due to UWB is dropped , change PQ103 from 17-S12312B-DS00 to 17-S12304B-DS00.  
(Cost down)

PT 2009.02.27  
(1)Due to USB port for RJ45 dongle has to be assigned to 2nd EHCI (port 6), and defined on left IO.  
Changed USB port on LIO from USB\_1 to USB\_6  
(2)Deleted the unnecessary R5354,(R5356 can cover the same function for path select.)  
(3)Added TP420(GND TP) for TP52. (SI request)  
(4)To meet Net name rule , changed name from LCD\_Cable\_Det# to LCD\_CABLE\_DET#.  
(5)Deleted unnecessary R5147.  
(There is 10K pull up to 3.3V on HP jack side.)  
(6)Changed head value for RP50,RP51 from Mount to NC.  
(Just reserved for debugging.)

(7)Implement RP52,RP53(Res Array to instead for R867,R868,R279,R284)  
(8)Changed part for R524,R525 from 0201 to 0402  
(9)Deleted R5369,R5370 to cancel LED power source option.  
(Just recover to original +5VLAW power source for LED.)  
(EC should turn on always power to drive LED and latch actuators when slider is activated under battery mode)  
(10)Merged U5012B to U37B  
(11)Deleted unnecessary +1\_5VRUN , +3VRUN power source for CN5016.( UWB is dropped.)  
-- Deleted L110,L111,C5151,C5152,C5153,C5154  
(12)Deleted RC for DREFSSCLK/DREFSSCLK# to optimize layout routing in inner layers.  
-- R893,R894,C1015,C1016  
(13)Deleted TP412,TP361 and assign PG0 as WIFI detection pin & GP62 as WWAN detection pin.  
-- Added R5373,R5374,R5375  
(14)Changed power source for WIFI +3V from +3VSUS to +3VRUN.(CN5015 Pin2,4,6)  
(15)Corrected the connection for PD33-Pin1 from BAT\_ALERT#\_R to BATCONBT-  
(16)Corrected head value for PR951,PR952 as below.  
PR951 ==> from Mount to NC\_  
PR952 ==> from NC\_ to Mount  
(17)Del unnecessary signal -DOPC\_CTRLCLK  
(18)Implement LCD\_BIST control function from SB/EC control.  
(19)Reserved PC945 & PC946 & PC949 & PC950 & PC951 & PC952 & PC953 & PC954 & PC955 & PC956 & PC957 for acoustic issue  
(20)Changed PR825 from 1R-0000103-J200 to 1R-0000104-J200 for power consumption improvement.

PT 2009.03.01  
(1)Correct signal connection for CN13 Pin8&10(SWAP)  
(2)Follow Realtek design guide to change C5100 from 4.7uF to 10uF.  
(3)Follow Code design guide to swap location between R5150&C5119  
(4)Changed PCP1 form close jump(X-JUMPO00-0007) to 0ohm(1R-0000000-J300)  
(5)Merge single 2N7002 Q22&Q5023(17-2N7002-F000) to Dual 2N7002 Q5025A,Q5025B(17-2N7002D-W000)  
(6)Changed L117(1L-BLLM06P-G101) to R5148 0ohm(1R-0000000-J300)  
(7)Changed U5012 from 14-74LVC1G-3200 to 14-NC7S32M-5X00  
(8)Added Decoupling Cap for logic ic power.  
-- C644 -- C450  
(9)Added test point for H\_A#25 & H\_A#17  
(10)Changed P078,PQ79,PQ80 from SI7121DN-T1-E3 to SI7121DN-T1-GE3(Halogen free)  
(11)Adjust pin assignment for CN5015 to add two +3VRUN power pin.  
(12)To enhance connector SMT reliability , implement additional GND pin for CN5016  
(13)Implement ALWPWR\_WAKE\_UP function on CN5019-Pin23 & U36-Pin

PT2009.03.02  
(1)Changed Pull up power source for WWAN\_DET# from +3VRUN to +3VSUS  
(2)To improve power consumption , changed PD47 from Mount to NC\_  
(3)Changed power source for OZ71REF\_EN from AMPSVIN9V to +ECVCVC and changed PR822 from Mount to NC\_  
(4)For layout spacing concern changed U5012 from 14-NC7S32M-5X00 to 14-74LVC1G-3200  
(5)For part consistence , changed U30 from 14-NC7S32M-5X00 to 14-74LVC1G-3200.(Same as U5012)  
(6)Merged U5013,U5014(single OR gate) to U5015(Dual OR gate)  
(7)Followed Intel suggestion to add 6pcs 0.1uF Decap for VHCORE power. (C239~C244)  
(8)To setting the suitable wake up voltage , changed PR7 from 36Kohm to 10Kohm and PR823 from 97.6Kohm to 324Kohm

PT 2009.03.02B  
To meet +3VRUN power budget , changed PQ106 from 17-S12312B-DS00 to 17-S15480D-UT00

PT 2009.03.03\_C  
Changed pin assignment for CN5019 to separate D/A

PT 2009.03.04  
Follow ME request to change H4~8,H10,H11 from 1X-HOLE000-0974 to 1X-HOLE000-1062

PT 2009.03.04\_B  
Corrected signal name for ALWPWR\_WAKE\_UP ==>ALWPWR\_WAKE\_UP#

PT 2009.03.04\_C  
(1)Changed C5162 from 33pF to 0.1uF.  
(2)Deleted C651.

PT 2009.03.05  
Changed GND for C5193 from P\_GND to GND.

PT 2009.03.06  
(1)Due to material preparation L/T issue , changed PU8 from 15-RT91981-0001 to 15-RT91981-0000.  
(2)Follow ME request to change H11 from 1X-HOLE000-1063 to 1X-HOLE000-0974  
(3)Deleted TP113,TP115 for DMI\_RXN1/DMI\_RXP1.  
(4)Deleted BIST control function from SB

PT 2009.03.09  
(1)Due to material purchase concern , changed U5015 from 14-SN74LVC-2G02 to 14-NL27W23-2U00  
(2)Backward PS\_ID Pull Up power source to +3VALW

PT 2009.03.09\_C  
(1)For layout spacing concern , c hanged R241 from 0402 to 0201  
(2)Follow ME request to add NUT1 & RING1 & RING2

PT 2009.03.11  
Add TP235(ICH9-GPIO20) for ICT request.

PT 2009.03.12  
Changed R241 from 4.7K 5% to 4.7K 1%  
PT 2009.03.16

(1)Changed D8 & R188 from Mount to NC\_.(No sequence concern.)  
(2)Changed D28 from Mount to NC\_  
(3)Changed R18 & R64 from 2.2Kohm to 0ohm.  
(4)Changed R283 from 2.2Kohm to 0ohm

2009/03/30  
For Exponent test purpose , changed PQ107&PR791&PR949 from NC\_ to Mount

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PT Changelist			
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PT2 2009.04.20  
To fix GPIO function limitation(GPE0 is no function when system in S5) ,  
changed ALWPWR\_WAKE\_UP# from GPE0 to GPE6.  
(Deleted TP353 for GPE6 & Added TP426 for GPE0)

PT2 2009.04.27  
To improve SMT reliability issue , implemented new part footprint for  
PQ5,PQ6,PQ7,PQ10,PQ11,PQ37,PQ99,PQ106,PQ108

PT2 2009.04.30  
To support Bridge Battery function , implement S\_BATT\_EN for EC GPIO GPC5(Pin57)  
(Deleted TP348)  
(2)To support Bridge Battery function , implement necessary Power/control signal for CN5016  
S\_BATT\_EN  
DCHN\_1  
AMPSVIN

PT2 2009.05.04  
(1)Follow ME DXF to deleted H11  
(2)Implement PWLED & STSLED PWM control for EC to support Power LED & Status LED control in Mech. Latch case.  
(3)Added RP55 & RP54 for the path select function.  
If RP55 Mount / RP54 NC : PWM control function by EC.  
If RP55 NC / RP54 Mount : I2C Bus connection between Cypress uC(Latch FPC) & EC.

PT2 2009.05.05  
(1)To improve the HP Crosstalk issue , changed CN5019-Pin3 from GND to A\_GND  
(2)To fix the timing issue for VCCRTC to RTCRST# , changed part value for R19 from 13Kohm to 17.8Kohm.  
(3)To reduce leakage , changed part value for PR857, PR869, PR883, PR886 from 10Kohm to 100Kohm.  
(4)Change part for PL3&PL5 from Lead free to Halogen free.  
(FDVE0630-2R2M=P3 to FDVE0630-H-2R2M=P3.)  
(5)Change part for PL7 from Lead free to Halogen free.  
(FDU1235-R47M=P3 to FDU1235-H-R47M=P3.)

PT2 2009.05.06  
(1)Added TP241 for I2C\_DAT3  
(2)For USB 5V power drop concern :  
changed part value for PR864&PR867 to rise +5VALW power level.  
PR864 : 91Kohm to 84.5Kohm  
PR867 : 10Kohm to 9.1Kohm

PT2 2009.05.07  
To fix ghost key issue , mount RP50/RP51 as external pull high.

ST 2009.05.22  
To fix sense issue for system shutdown of SMSC1422 , added Q27 to change the connection of SYS\_SHDN# from Source to Gate of MOS.

ST 2009.05.22  
To meet Dell requirement , added WWAN\_PWR\_EN control to separate the WWAN device/power control.

ST 2009.05.25  
(1)To fix power noise issue , added C5199(1uF Cap) for +5VALW .  
(2)Changed part for PD35 from 15V rating to 5V rating and follow EMI suggestion to connect PD35-1 from ADADJ to QZ71CONT.  
(3)Follow Dell requirement to implement PS\_ID circuit.  
(4)To guarantee the suitable power level output when air adapter condition(14V~19V) , added PC11,PD45.

ST 2009.5.27  
(1)Deleted close Gap PJ4,PR10,PR18,PR19 and changed net name form AMPSVINS185V to AMPSVIN  
(2)Deleted Close Gap PJ15 and change net name form S185VOUT to +5VALW.  
(3)Deleted Close Gap PJ16,PR11,PR21 and changed net name form AMPSVINS183V to AMPSVIN  
(4)Deleted Close Gap PJ7 and changed net name form S183VOUT to +3VALW.  
(5)Deleted close Gap PJ10,PR12,PR23 and change net name form AMPSVINM00 to AMPSVIN  
(6)Deleted Close Gap PJ11,PJ12 and changed net name form +1\_5VSUS\_1 to +1\_5VSUS  
(7)Deleted Close Gap PJ18,PR13,PR24 and changed net name form AMPSVINM8792 to AMPSVIN.  
(8)Deleted Close Gap PJ19,PR20 and changed net name form 8792\_FB to +1\_05VRUN.  
(9)Deleted Close Gap PJ14,PR15,PR16 and changed net name form AMPSVIN\_ISLVIN to AMPSVIN.  
(10)To fix hang up issue(Post code:0x86) ,added R5379 as termination Res.

ST 2009.06.01  
Follow the suggestion from SMSC FAE to reserve C382(0.1uF) for RC delay reuquest.

ST 2009.06.02  
Removed 75ohm termination Res.--R5379

ST 2009.06.02B  
To fix the RTCRST# timing issue ,  
changed part value for R19 from 17.8Kohm to 22Kohm and R565 from 13Kohm to 22Kohm.

ST 2009.06.02B  
To fix the Ripple /Noise issue for +5V power ,  
changed part for PC949 from TEPSLD1A227M(25)12R to TLP5LV0J227M(15)12RE.  
(Lower ESR)

ST 2009.06.02B  
To fix the Ripple /Noise issue for +5V power ,  
changed part value for PR860 from 100K to 75K

ST 2009.06.02B  
Corrected signal name as below.  
I2C\_DAT3\_STSLD ==> I2C\_DAT3\_STSLD\_AMBER  
I2C\_CLK3\_PWRLED ==> I2C\_CLK3\_STSLD\_WHITE  
PWRLED\_PWM ==> STSLED\_WHITE\_PWM  
STSLED\_PWM ==> STSLED\_AMBER\_PWM

ST 2009.06.03  
To fix timing accuracy issue , changed part value for C648&C649 from 10pF to 8pF.

ST 2009.06.09  
Follow adapter ground linear resistance to adjust part value for PR832,PR835  
PR832 : 4.87Kohm to 118Kohm  
PR835 : 31.6Kohm to 768Kohm

ST 2009.06.09B  
(1)To fix noise issue when Codec initial , changed C5112 from mounted to NC\_  
(2)Corrected signal name from WWAN\_EN to WWAN\_RF\_EN  
(3)To drop HDD\_LED function from ST , reserved below parts from mount to NC\_  
R5164,Q26,R562,LED3  
(4)Corrected signal name from HW\_POP\_MUTE\_ECG to HW\_POP\_MUTE\_EC

ST 2009.06.24  
(1)To fix derating concern for air adapter condition(14V~19V) , changed part value for PR905,PR914 from 2.2Kohm to 4.7Kohm.  
(2)To fix derating concern for air adapter condition(14V~19V) , changed part value for PC932 from 0.1uF\_16V to 0.1uF\_25V.  
(3)To improve ripple noise for +3VALW+5VALW , NC PC858&PC996  
(4)To fix derating concern , changed part value for PC885 from 0.1uF\_6.3V to 0.1uF\_25V  
(5)To control Impedance accurately , implement Impedance coupon on MB.  
(6)To fix USB 5V power drop issue , changed part value for PR864,PR867  
PR864 : from 84.5Kohm to 110Kohm  
PR867 : from 9.1Kohm to 12Kohm

ST 2009.06.29  
(1)Update Block Diagram  
(2)To fix Slew issue for DREFSSCLK/DREFSSCLK# , changed Clock Gen.(U29) from SL28541BQCJ to 9LRS3165BKLFT.  
(3)Reserved R5379/R5380 as path select for HW\_POP\_MUTE\_EC control function.

ST 2009.06.29B  
Due to Die-transfer from D to E , changed Part for U62~U69 from K4B1G0846D-HCF8 to K4B1G0846E-HCF8

ST 2009.06.30  
(1)Follow JEDEC Standard to implement 75ohm terminator(R5381) for unused M\_CLK\_DDR1/M\_CLK\_DDR#1  
(2)To fix the DP source detection issue when system in S5 , changed power source for DPAUXN\_C pull up & U5011 switch power from +3VRUN to +ECVCC

ST 2009.07.01  
(1)Implement special footprint(qfn\_65p\_20\_354x354\_th118\_H800) that set thermal pad as 3mmx3mm for U29  
(2)Implement suitable Symbol(Footprint(H86) for Impedance coupon on MB.

ST 2009.07.02  
(1)For BFT test request , changed TP size from tpc20t\_50 to TPC35T\_75 for TP52/TP420  
(2)For height limitation concern , changed part size from 0402 to 0201 for R5381

ST 2009.07.02B  
To fix the DP source detection issue when system in S5 , changed power source for CA\_DET\_Q pull up power from +3VRUN to +ECVCC

ST 2009.07.03  
For DFM concern , implemented special footprint to improve SMT quality.  
PQ5,PQ6,PQ7,PQ10,PQ11,PQ97,PQ99,PQ106,PQ108

SV 2009.07.07  
For ESD concern , changed part for Q23 from 2N7002-7-F to 2N7002-7 (with ESD diode)

ST 2009.07.07B  
(1)Deleted unnecessary P12(Open GAP for GND)  
(2)For fix EMI issue , added SPR1 & SPR2

ST 2009.07.09  
For height limitation concern , deleted SPR1

ST 2009.07.13  
To prevent the abnormal short between LCD\_CABLE\_DET#(Pin22) & AMPSVIN\_LCD(Pin23) when cable assy ,  
changed pin define for CANS017-pin23 from AMPSVIN\_LCD to NC.

ST 2009.07.21  
To fix the DP source detection issue completely when system in S5 , backward pull high power source for CA\_DET\_Q/DPAUXN\_C/U5011 VDD to +3VRUN.  
And move Pull high/Pull down Res(R891/R890) connection from switch input to switch output.

ST 2009.07.22  
To fix ESD issue , changed H5~H8 from PTH Hole to NPTH Hole.  
(Cut off the path from Keyboard to system GND.)

ST 2009.07.23  
To fix the derating issue(Vgs) , changed part for PQ98 from Si2312BDS(8V) to Si2306(20V)

ST 2009.07.27  
To fix the derating issue(Vgs) , changed part for PD47 from UDZSTE-17B.19 to UDZSTE-1715B.  
(Fix AMPSVIN9V level is 15V when air adapter input)

ST 2009.07.30  
To control BOM for option WWAN function , changed the head value for related parts from Mount to WWAN\_  
Page33 : C5147,C5146,L108  
Page26 : R5375

ST 2009.08.03  
Follow adapter ground linear resistance to adjust part value for PR832,PR835  
PR832 : 118Kohm to 143Kohm  
PR835 : 768Kohm to 931Kohm

ST 2009.08.06  
Follow adapter ground linear resistance to adjust part value for fixed adapter watt.  
NC PR952,PR831,PR843,PR844,PR838,PR839,PJ6,PU7  
PR834,PR836,PR837 Change part value to 0 ohm.

ST 2009.08.28  
(1)  
To fix USB 5V power drop issue ,  
backward part value for PR864,PR867 to enhance +5VALW level  
PR864 : from 110Kohm to 84.5Kohm

(2)(ECN:CDNRDS0908009)  
To fix maximum power limitation function , changed part value for PR832,PR835  
PR832 : from 143Kohm to 60.4Kohm  
PR835 : from 931Kohm to 30.1Kohm  
PR867 : from 12Kohm to 9.1Kohm

(3)  
To fix the rise time SI issue for Batt SMBus , changed part value for RP33.  
From 10Kohm(1R-1010103-JP00) to 4.7Kohm(1R-1010472-JP00)

ST 2009.09.10  
To support complete vendor P/N & part description , changed part for PD45 from 16-UD2551B-0001 to 16-UD2551B-0000

ST2 2009.09.16  
To fix hang up issue , implement below solution for VR design.  
(1)Reserved PR953 for H side MOS(PQ3) rise timing adjustment.  
(2)To reduce Spike for AMPSVIN\_ISLVIN , added PL28,PL27 for PQ3(VR H side MOS) VIN.  
(3)To reduce Spike for AMPSVIN\_ISLVIN , follow Intel CRB(Rev1.01) to add 4pcs 0.01uF cap(PC958-PC961)

ST2 2009.09.17  
Co-layout PL28,PL29 for Inductor solution.

ST2 2009.09.17B  
To get better brightness linearity , added EC control signal(EC\_BRADJ) and reserved R5382,R5383 for path selection.

ST2 2009.09.18B  
Follow the suggestion from PWR team , corrected part for PL28,PL29 from BLM21PG331SN1 to LQM21PNR47MC0D

ST2 2009.09.28  
To support backlight control function by EC side , changed control circuit path from GMCH to EC.  
R5382 : From Mount to NC.  
R5383 : From NC to Mount.

X-Build 2009.10.12  
Disabled external SPI ROM boot function and changed part value as below.  
From Mount to NC : U30,C643,R267,CN13  
From NC to Mount : R566

X-Build 2009.10.12  
Disabled test fan function and changed part value for CN51 from Mount to NC.

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