

COMPAL CONFIDENTIAL

MODEL NAME : IAQ20

PCB NO : LA-3751P (DA800008Y0L)

BOM P/N : 46149031L0121

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# Converse

uFCPGA Mobile Merom  
Intel Crestline + ICH8M

21-05-2007

REV : 0.1(X00)

@ : Nopop Component

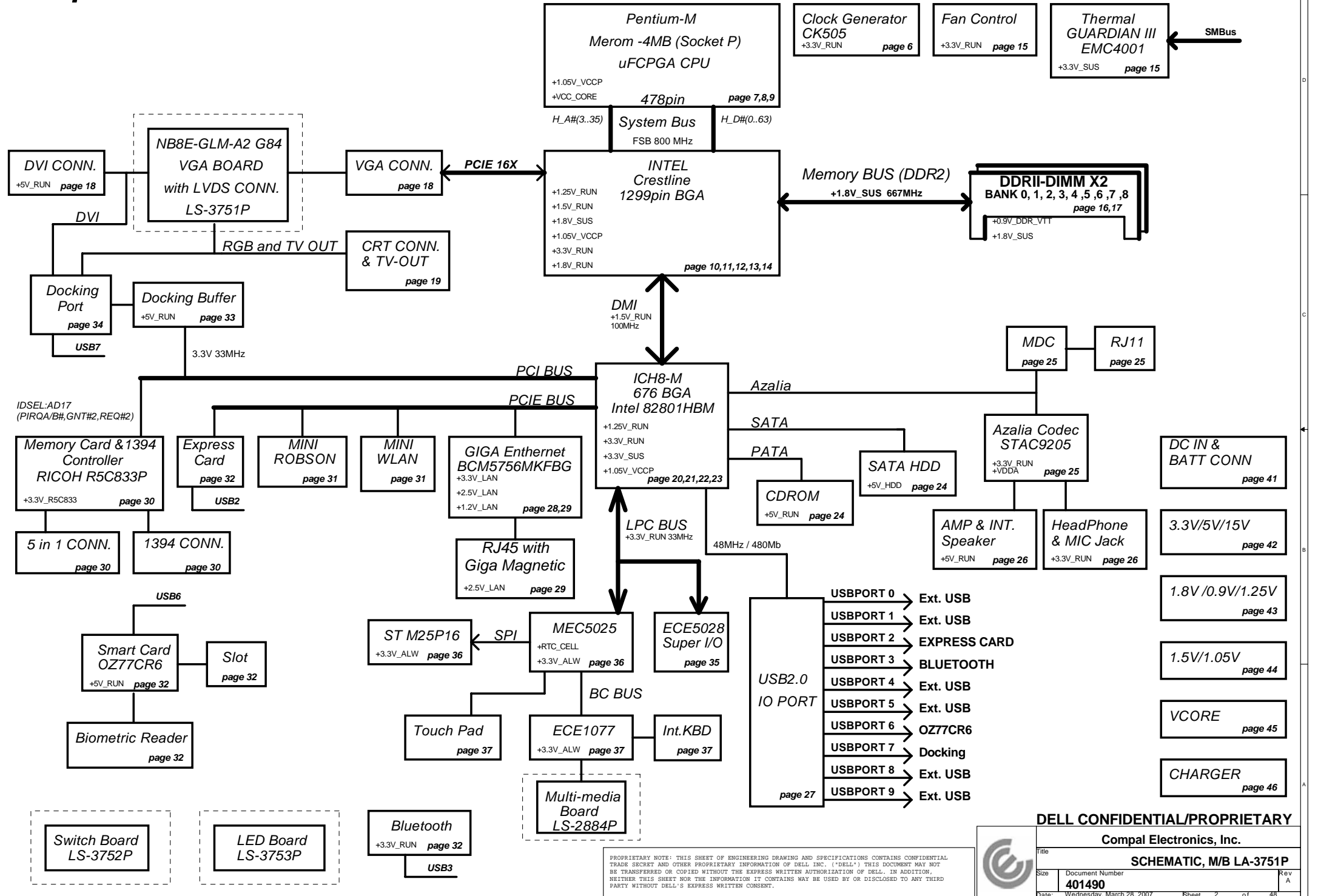
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Size	Document Number		Rev	
	401490		A	
Date:	Wednesday, March 28, 2007	Sheet	1	of 48



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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +1.25V_RUN +0.9V_DDR_VTT +1.05V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

## PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQC, D
Docking	AD24	REQ#0 / GNT#0	PIRQA

ICH8-M	USB PORT#	DESTINATION
	0	Rear Right Bottom
	1	Rear Right Top
	2	EXPRESS CARD
	3	Bluetooth
	4	Rear Left Bottom
	5	Rear Left Top
	6	OZ77CR6/Smart Card Reader
	7	Docking
	8	Side Bottom
	9	Side Top
OZ77CR6	UPD+/D-, pin 16/17	ICH8-M
	DPD+/D-, pin 18/19	Biometric Reader
	EGATED+/D-, pin 20/21	SMART CARD

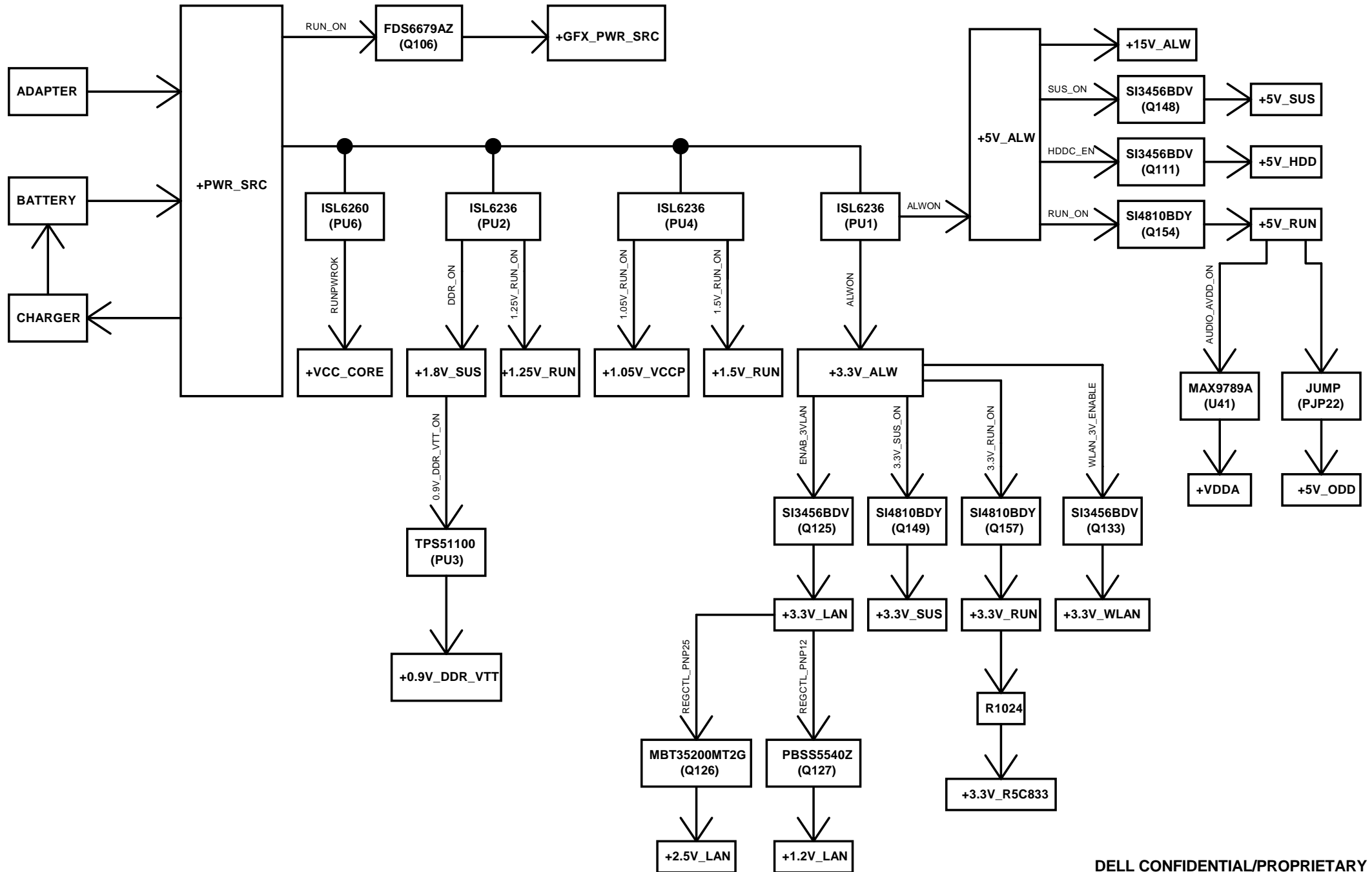
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD 1- Robson
Lane 2	MINI CARD 2- WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	GIGA LAN

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Title	SCHEMATIC, M/B LA-3751P		
Size	Document Number	Rev	A
	401490		
Date:	Wednesday, March 28, 2007	Sheet	3 of 48

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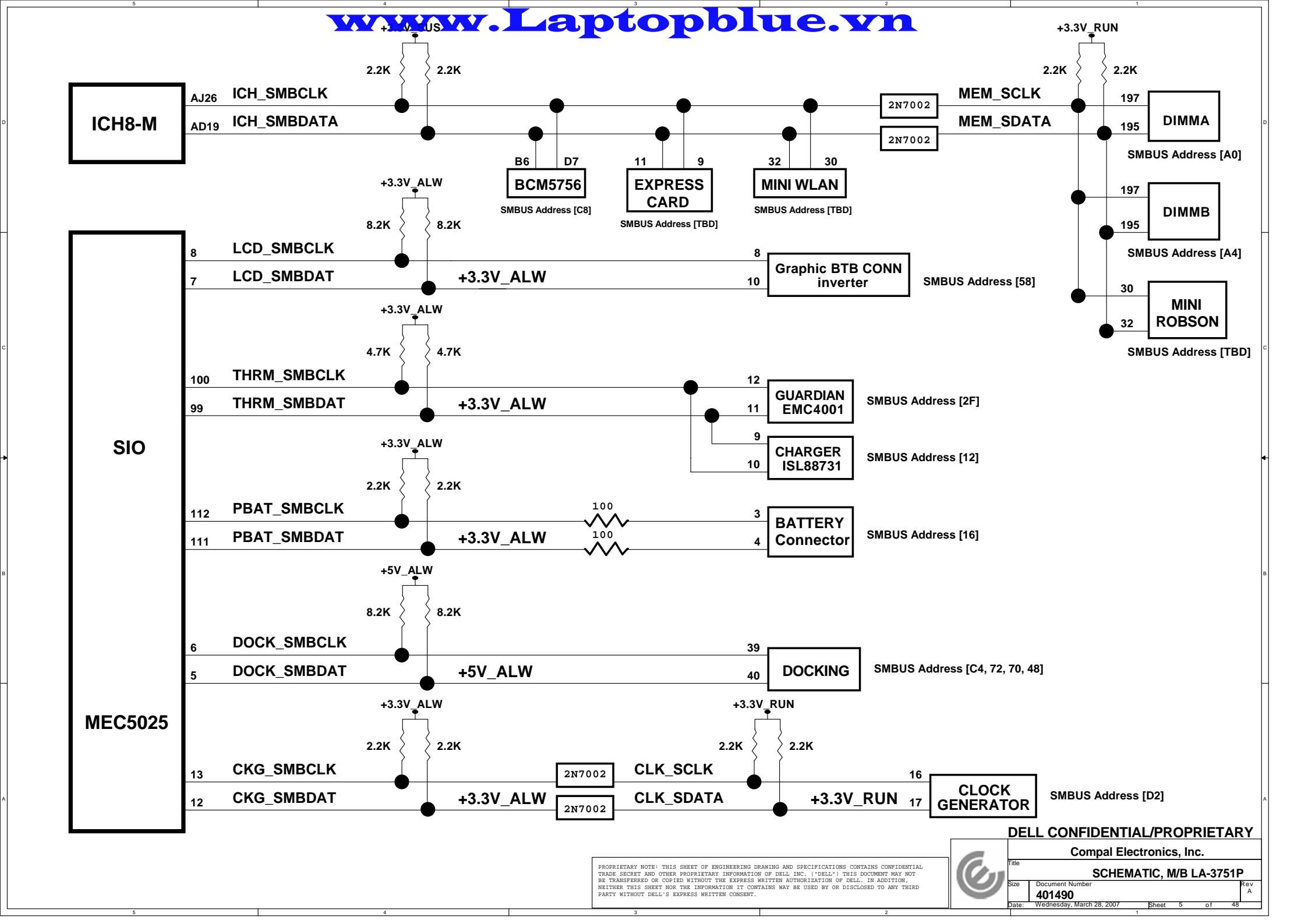
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Size	Document Number	401490		Rev	A
Date:	Wednesday, March 28, 2007	Sheet	4	of	48



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**ICH8-M**

**SIO**

**MEC5025**

**ICH8-M**

**MEM\_SCLK**

**MEM\_SDATA**

**DIMMA**

**DIMMB**

**MINI ROBSON**

**GUARDIAN EMC4001**

**CHARGER ISL88731**

**BATTERY Connector**

**DOCKING**

**CLOCK GENERATOR**

**BCM5756**

**EXPRESS CARD**

**MINI WLAN**

**Graphic BTB CONN inverter**

**CLK\_SCLK**

**CLK\_SDATA**

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**401490**

**Rev A**

**Date: Wednesday, March 28, 2007**

**Sheet 5 of 48**

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**Date: Wednesday, March 28, 2007**

**Sheet 5 of 48**

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**401490**

**Rev A**

**Date: Wednesday, March 28, 2007**

**Sheet 5 of 48**

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**401490**

**Date: Wednesday, March 28, 2007**

**Sheet 5 of 48**

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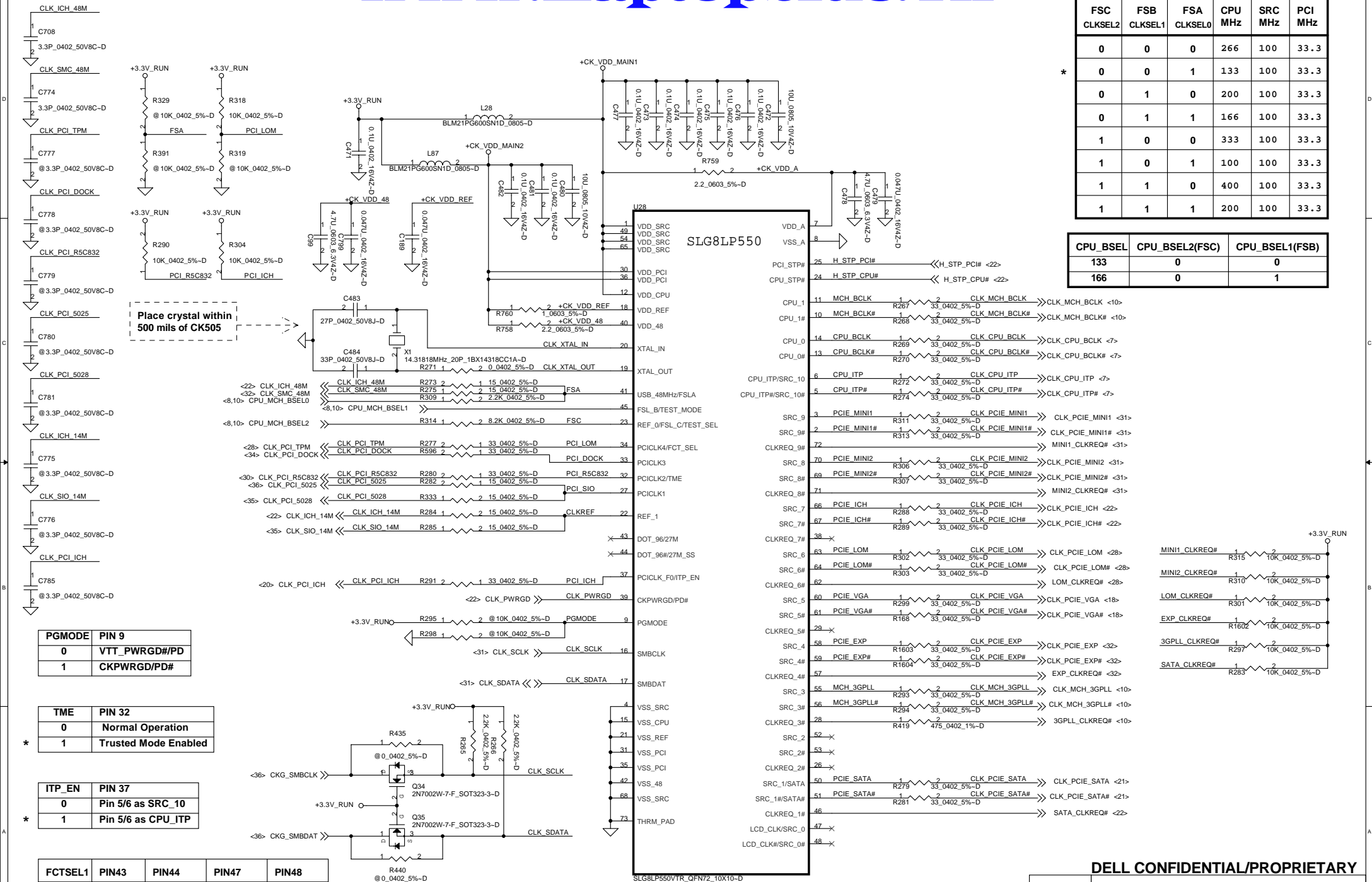
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**401490**

**Date: Wednesday, March 28, 2007**

**Sheet 5 of 48**



	FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
*	0	0	0	266	100	33.3
	0	0	1	133	100	33.3
	0	1	0	200	100	33.3
	0	1	1	166	100	33.3
	1	0	0	333	100	33.3
	1	0	1	100	100	33.3
	1	1	0	400	100	33.3
	1	1	1	200	100	33.3

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

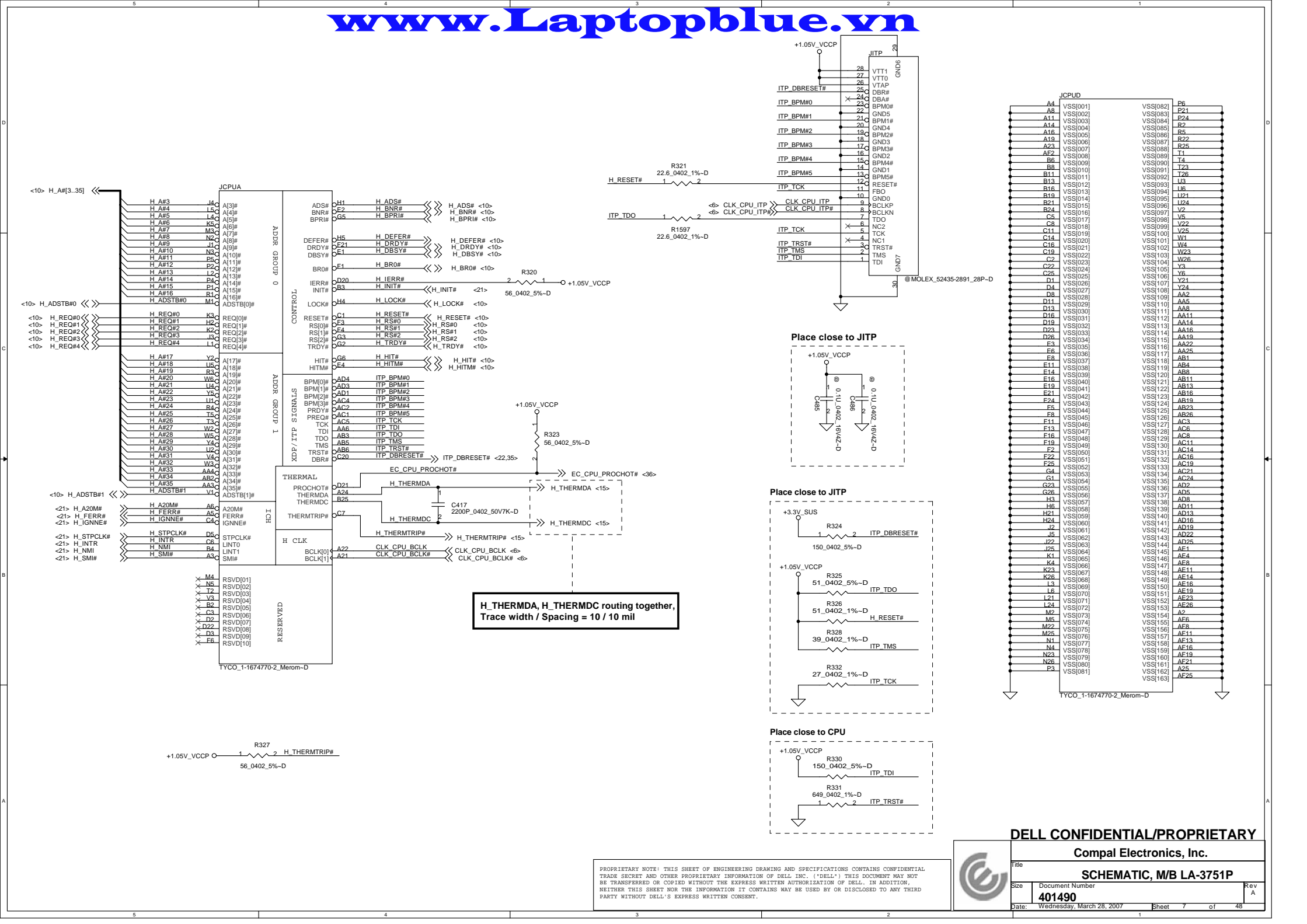
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Size	Document Number	Rev
	101-100	A

Date: Wednesday, March 28, 2007 Sheet 6 of 48



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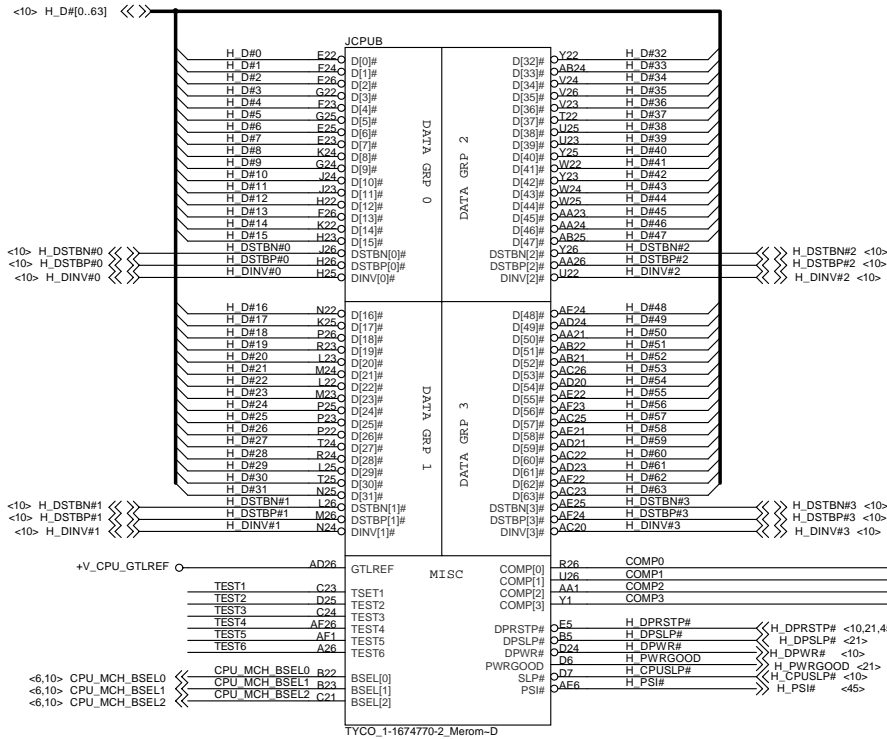
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Size	Document Number	Rev
	401490	A
Date:	Wednesday, March 28, 2007	Sheet 7 of 48

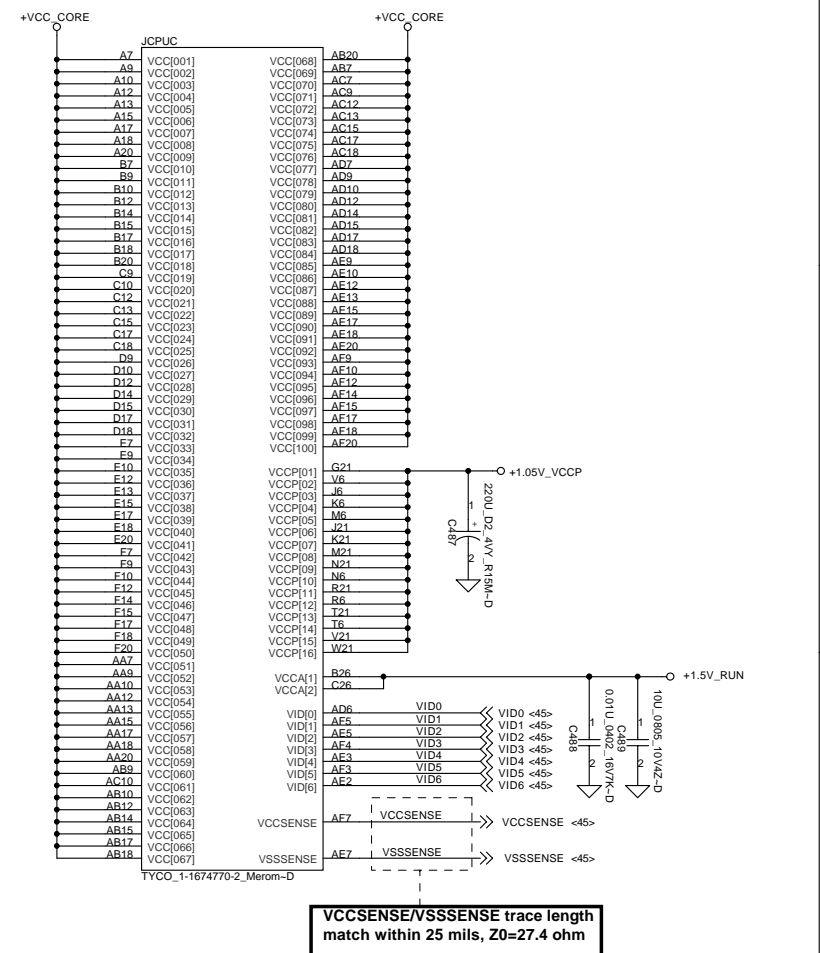
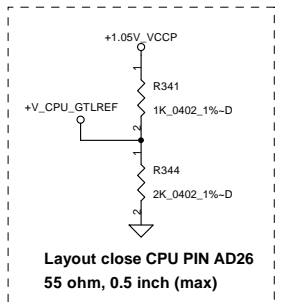
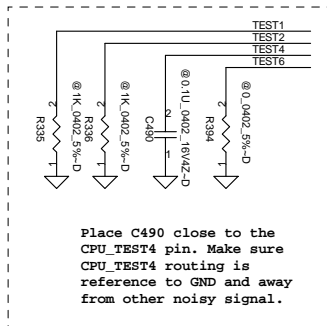




Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.

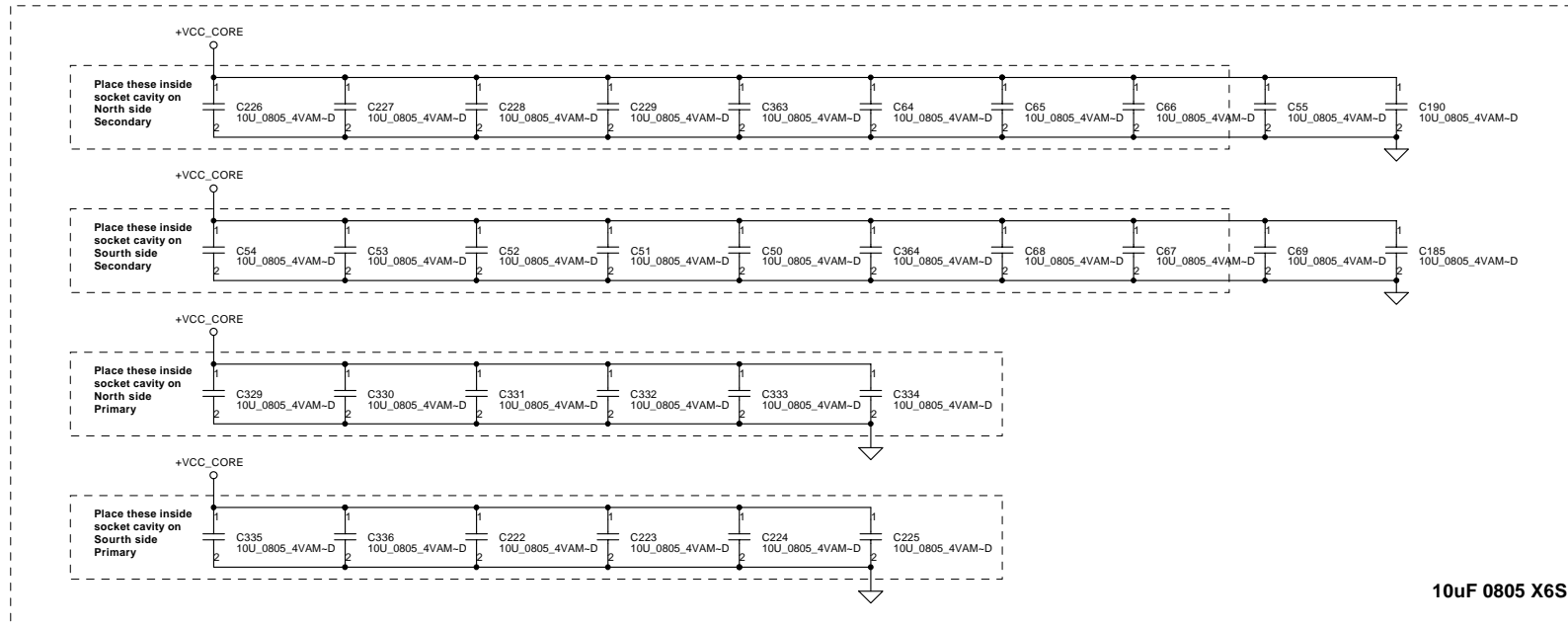
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

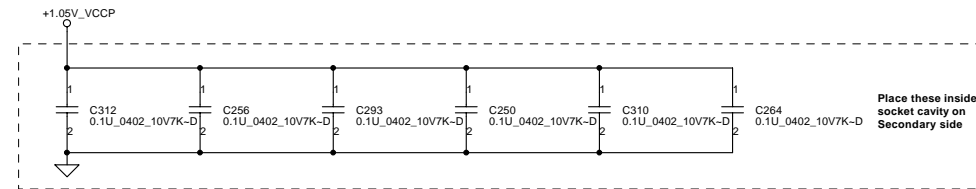
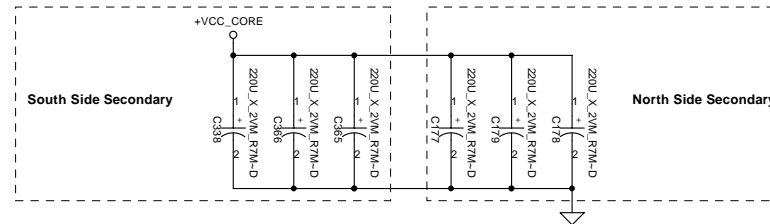




# High Frequency Decoupling



Near VCORE regulator.



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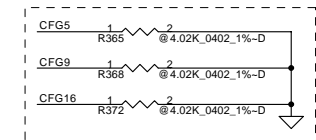
Title	SCHEMATIC, W/B LA-3751P		
Size	Document Number	Rev	A
	401490		
Date:	Wednesday, March 28, 2007	Sheet	9 of 48

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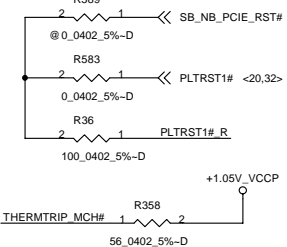
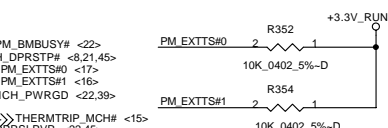
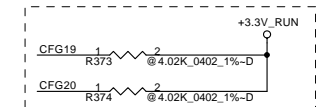
# Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation (Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present

CFG[3:17] have internal pullup



CFG[18:19] have internal pulldown

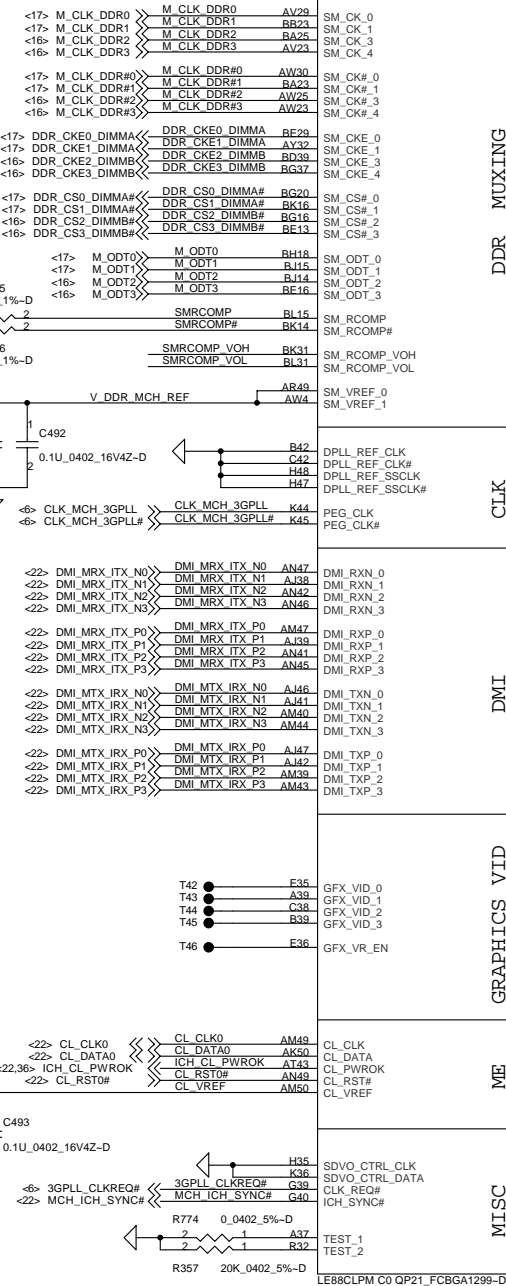


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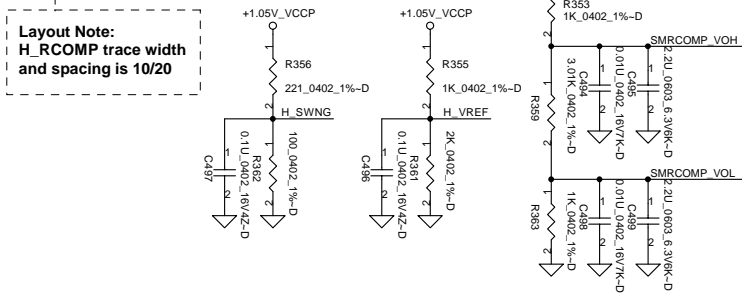
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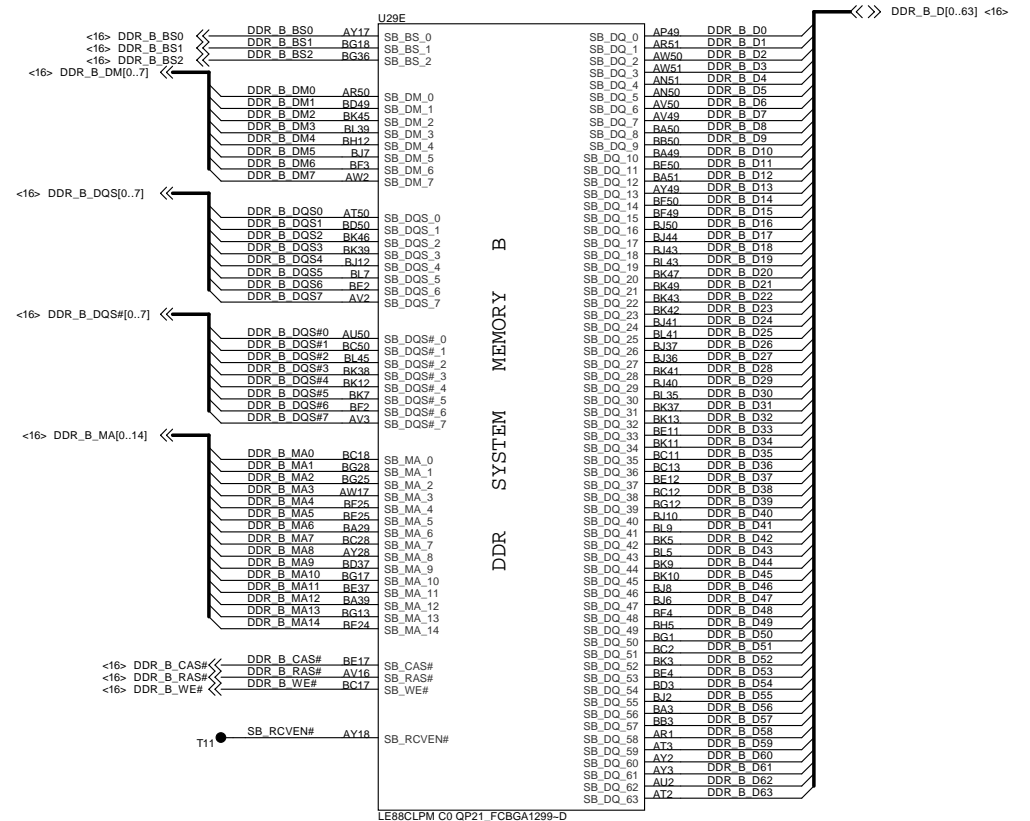
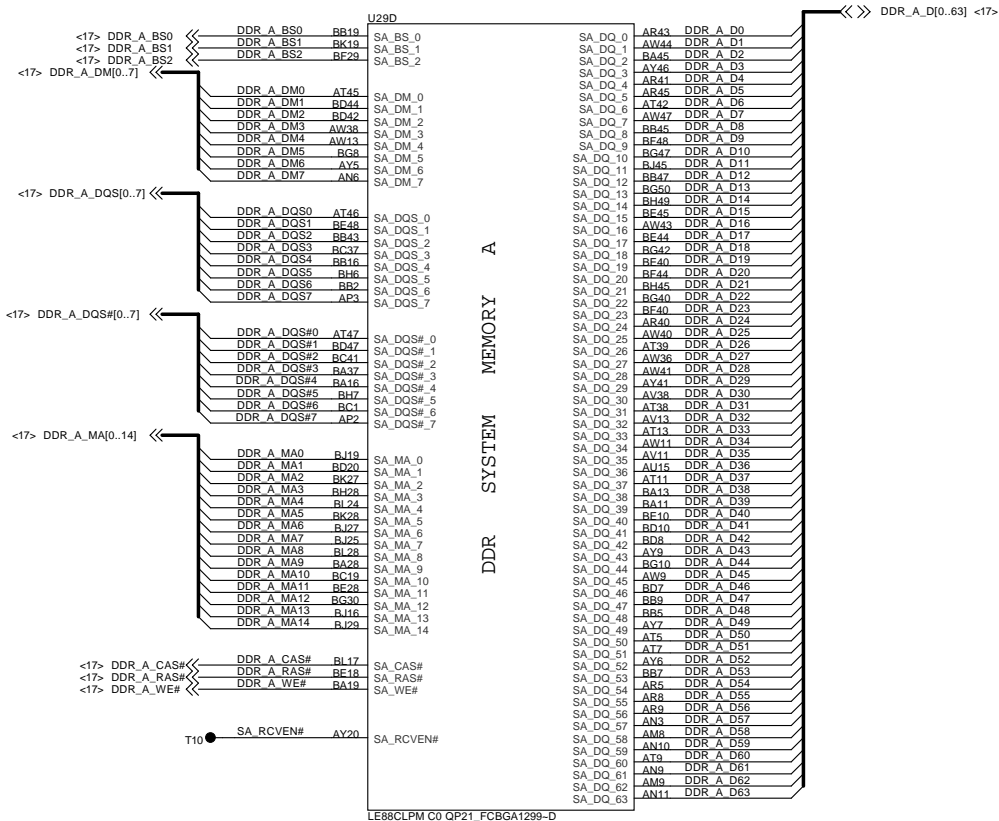
Title: 401490  
Date: Wednesday, March 28, 2007  
Sheet: 10 of 48



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Layout Note:  
H\_RCOMP trace width and spacing is 10/20





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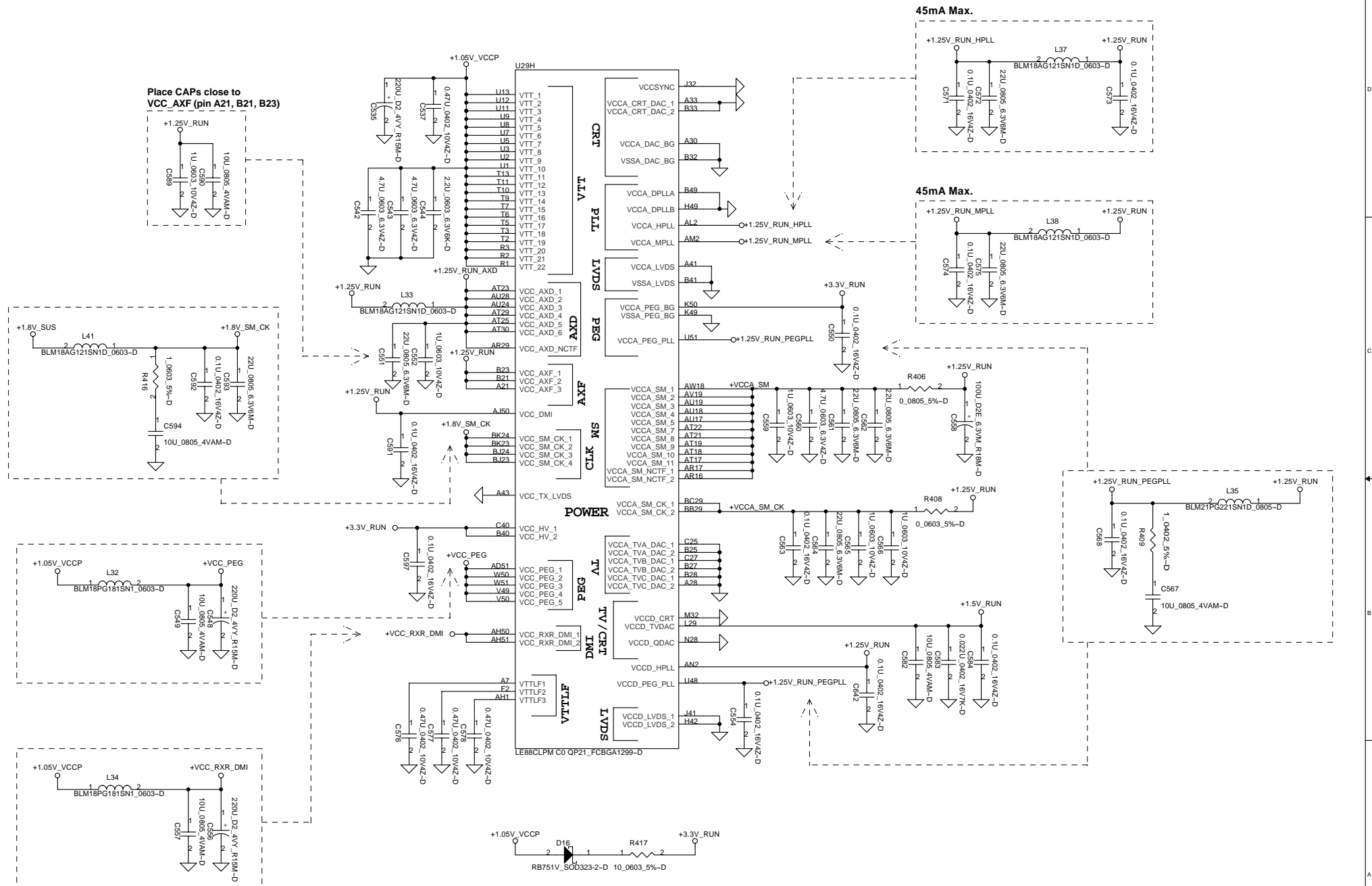
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Title		SCHEMATIC, M/B LA-3751P	
Size	Document Number	Rev A	
401490			
Date:	Wednesday, March 28, 2007	Sheet	11 of 48

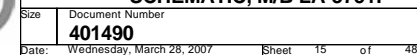
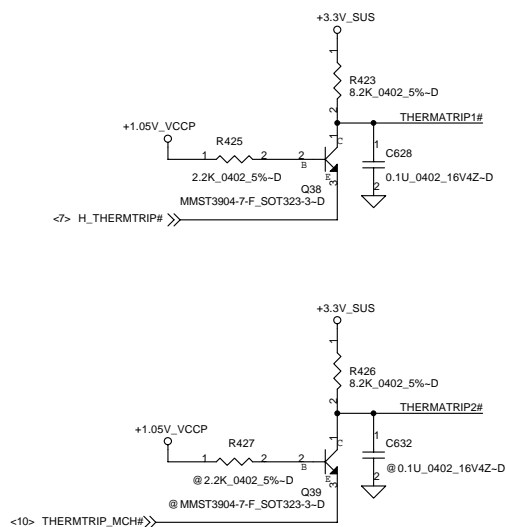
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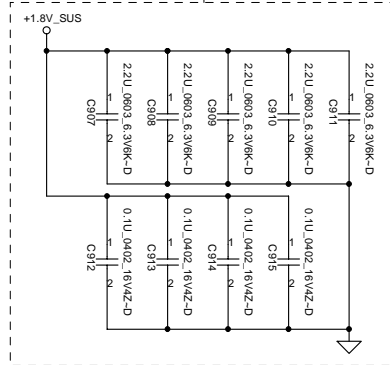




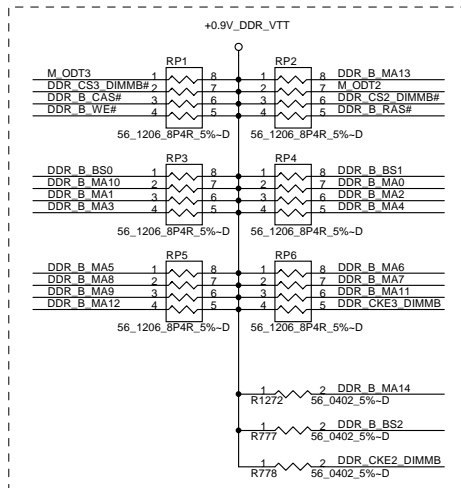
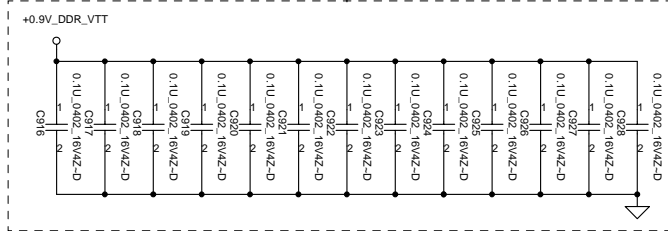




Layout Note:  
Place near JDIMB

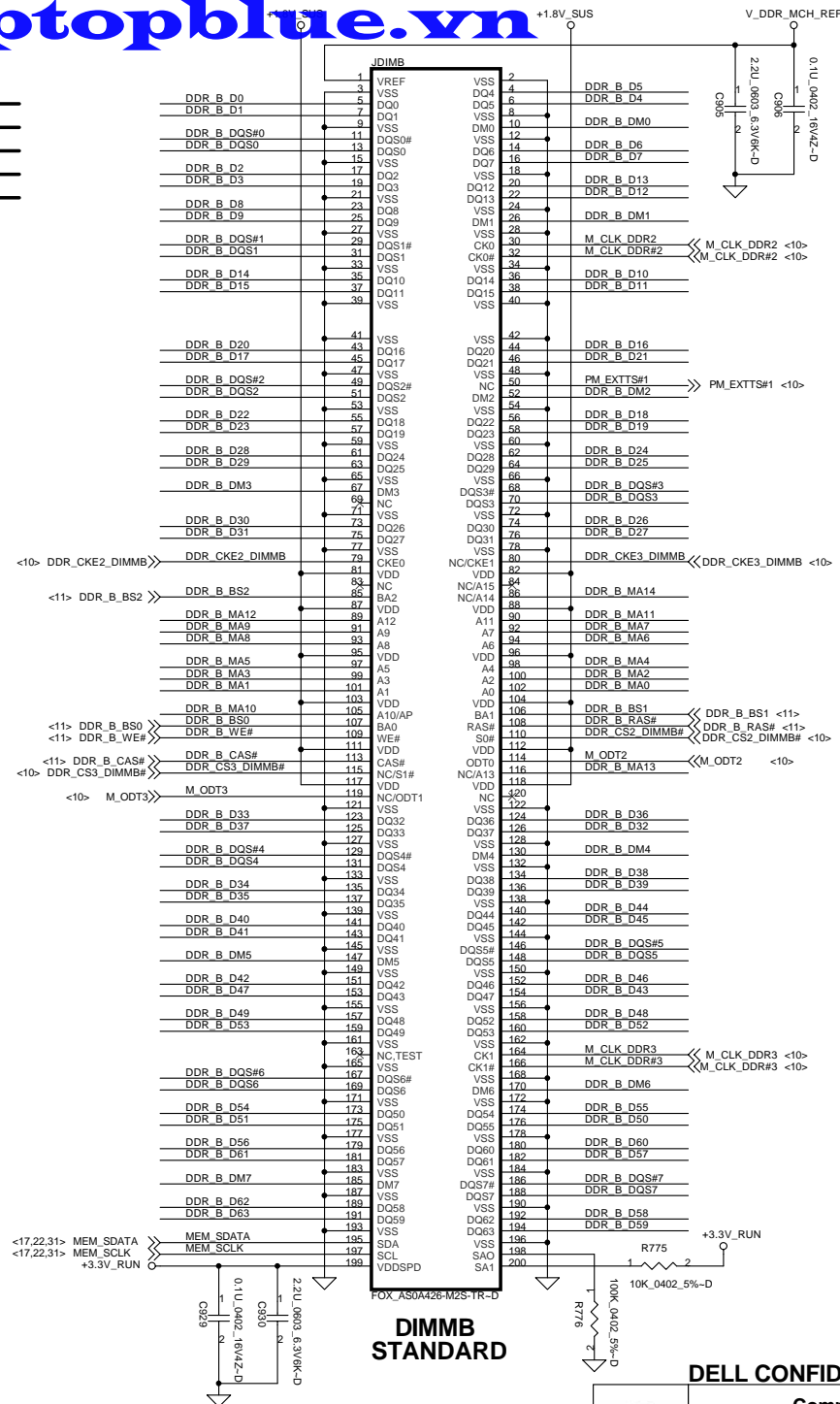


Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to +0.9V\_DDR\_VTT



Layout Note:  
Place these resistors  
close to JDIMB

<11> DDR\_B\_D[0..63] <<>>  
<11> DDR\_B\_DM[0..7] <<>>  
<11> DDR\_B\_DQS[0..7] <<>>  
<11> DDR\_B\_DQS#[0..7] <<>>  
<11> DDR\_B\_MA[0..14] <<>>



DIMB  
STANDARD

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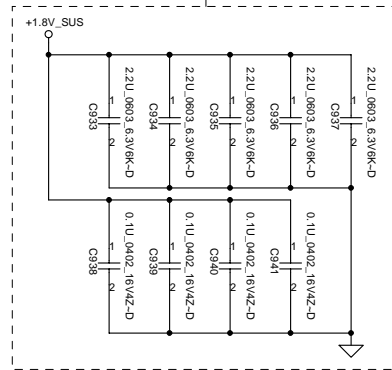
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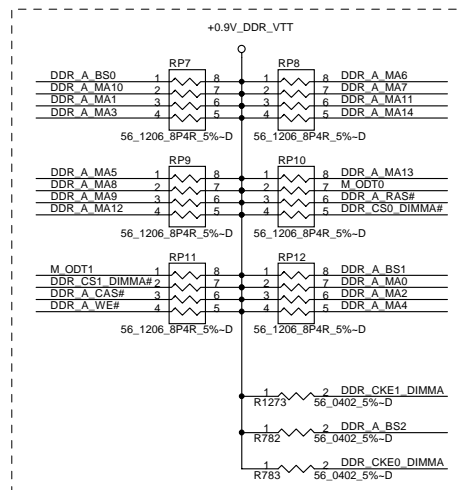
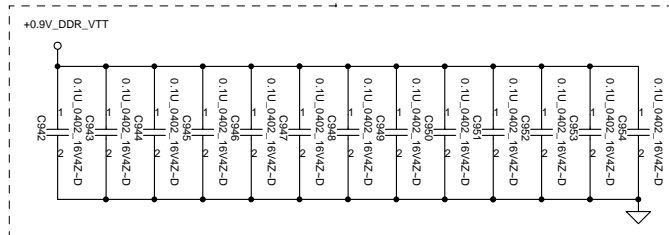
File	Document Number	Rev
401490		A
Date: Thursday, March 29, 2007	Sheet 16 of 48	

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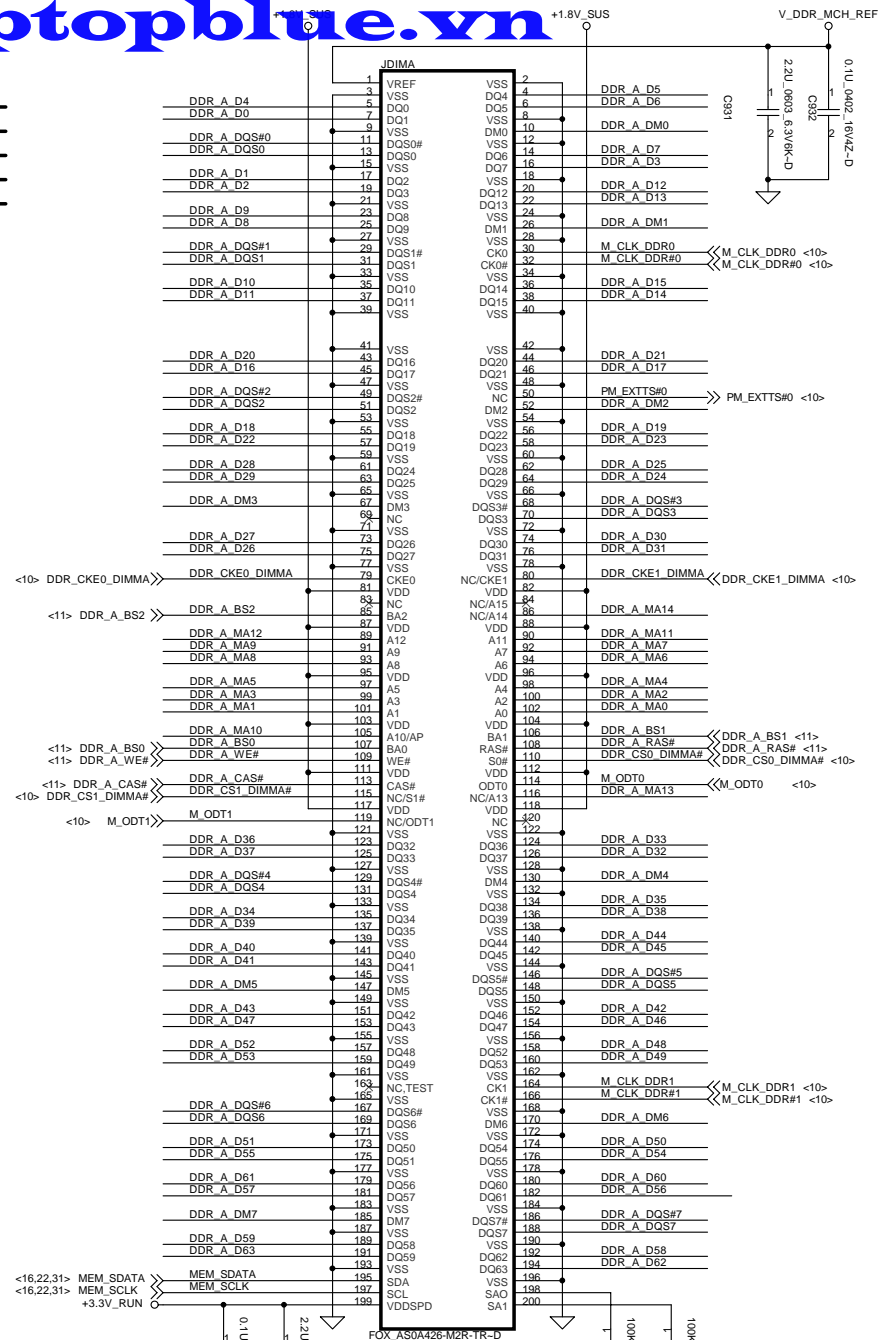


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Place one cap close to every 2 pullup  
resistors terminated to +0.9V\_DDR\_VTT



Layout Note:  
Place these resistors  
close to JDIMA

<11> DDR\_A\_D[0..63] <<>  
<11> DDR\_A\_DQS[0..7] <<>  
<11> DDR\_A\_DQS0[0..7] <<>  
<11> DDR\_A\_DM[0..7] <<>  
<11> DDR\_A\_MA[0..14] <<>



DIMMA  
REVERSE

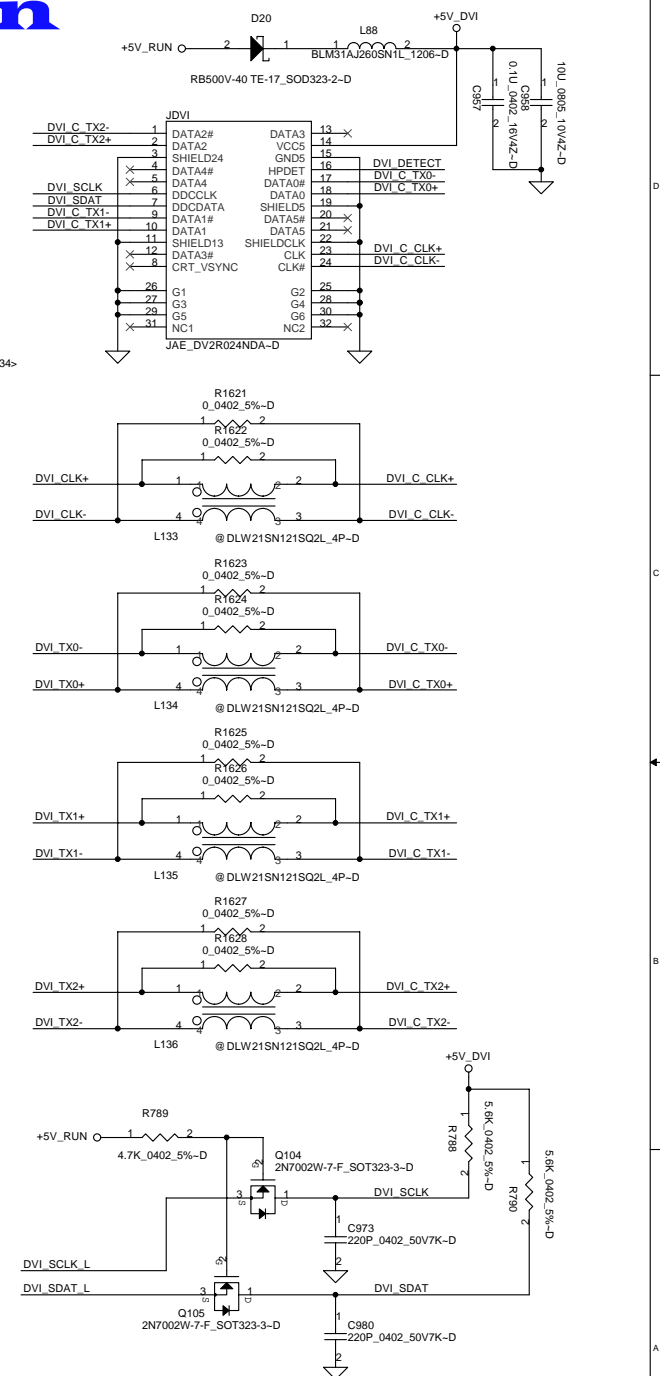
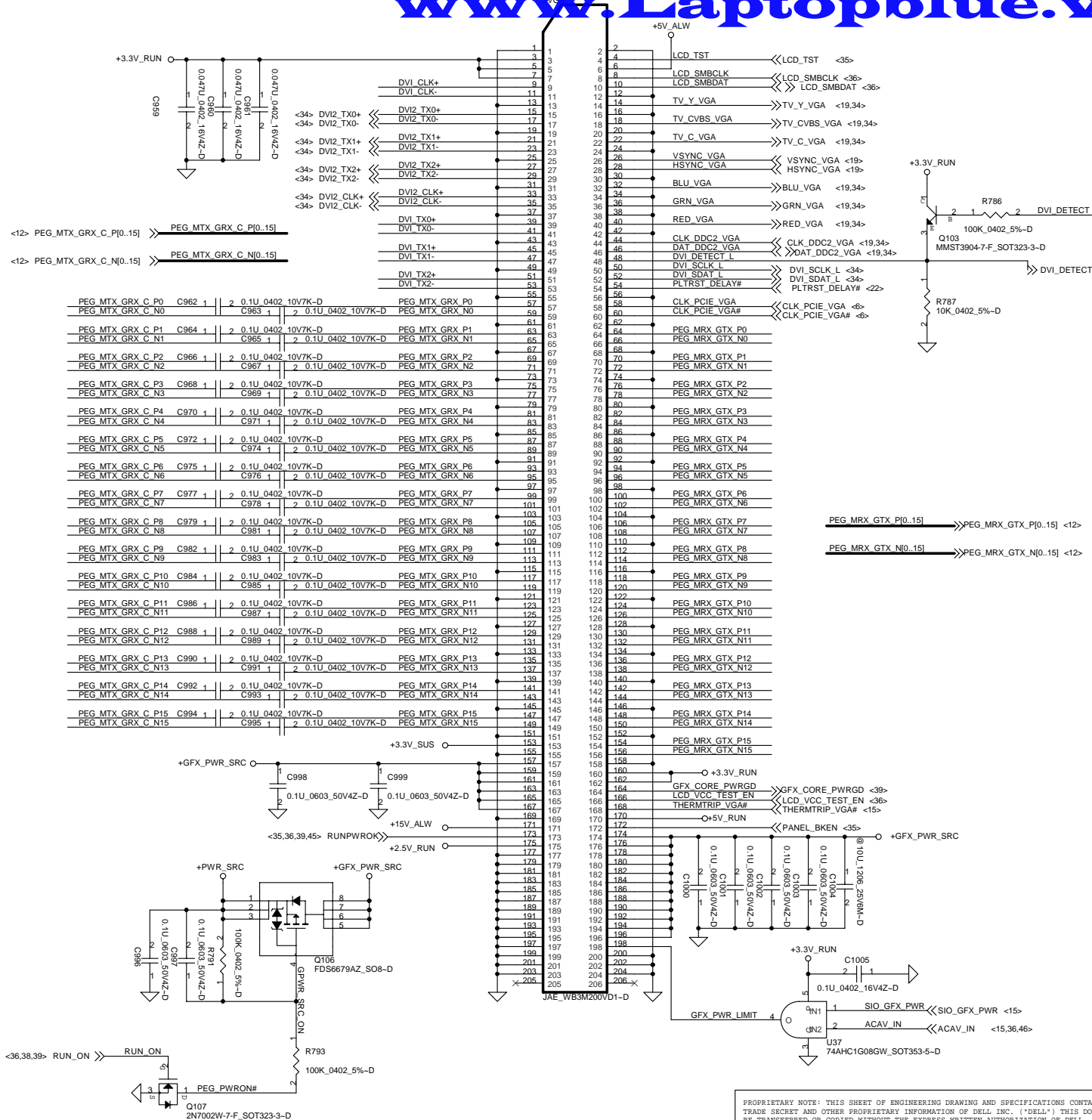
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Title		Rev A	
Size	Document Number	401490	
Date:	Thursday, March 29, 2007	Sheet	17 of 48

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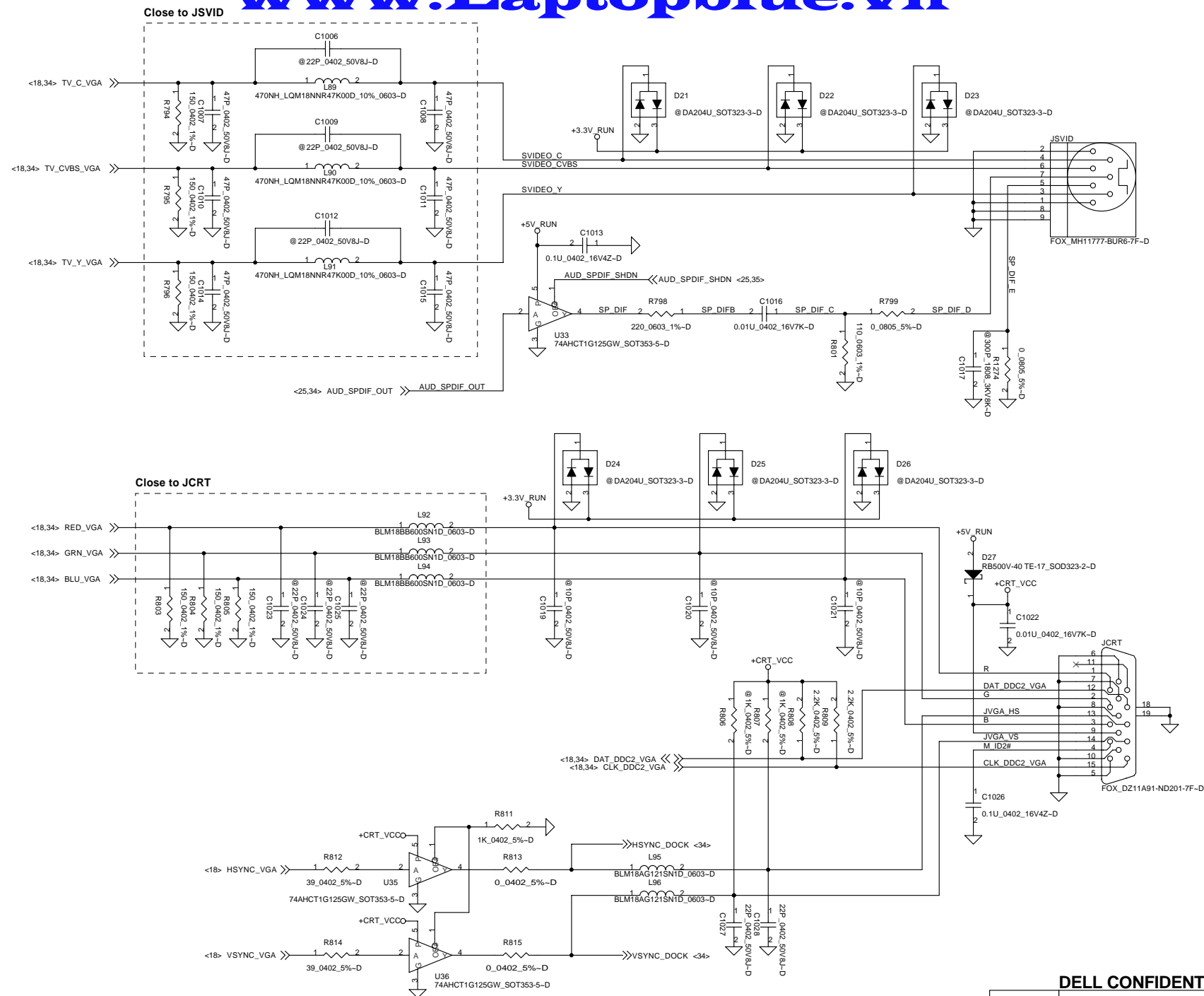
**SCHEMATIC, M/B LA-3751P**

Size	Document Number	Rev
	101400	A

Date: Wednesday, March 28, 2007		Sheet 18 of 48	
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**Place R813 near U35 and R815 near U36**

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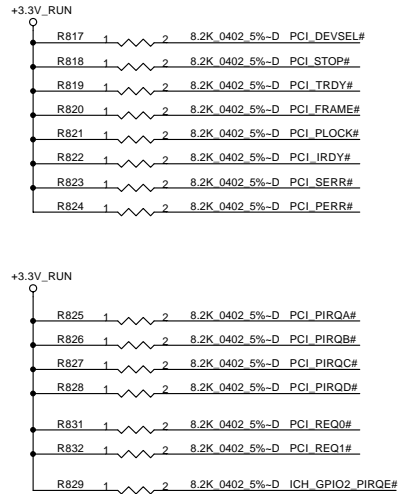
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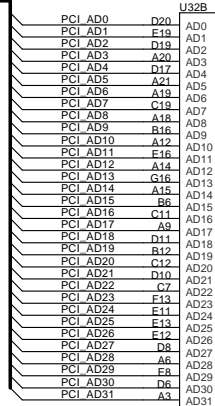
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Size	Document Number	Rev
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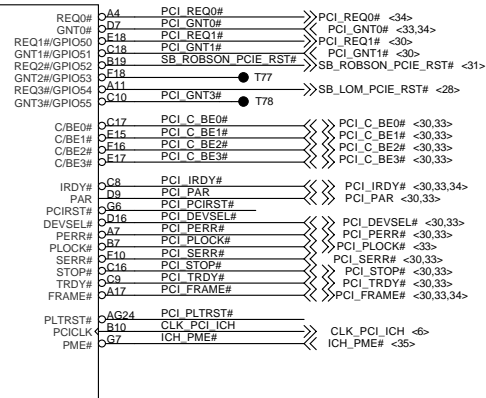
Date: Wednesday, March 28, 2007 Sheet 19 of 48



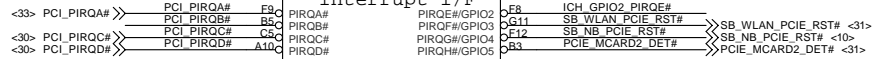
<30,33> PCI\_AD[0..31] <<>



PCI

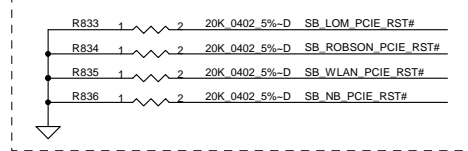


Interrupt I/F



NH82801HEM B1 QN24\_BGA676-D

BIOS should not enable the internal GPIO pull up resistor



A16 away override strap.

PCI\_GNT3#

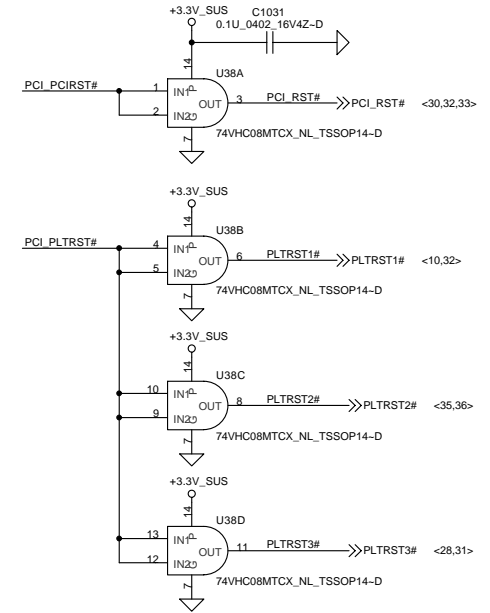
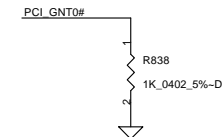
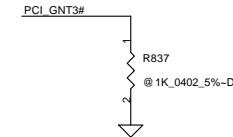
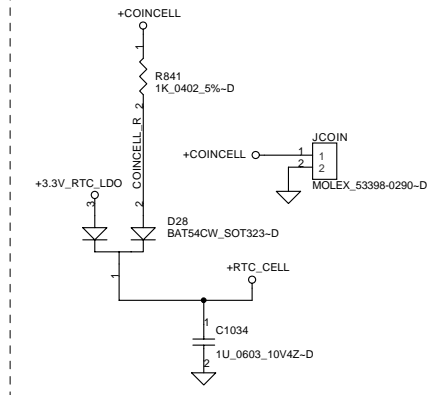
Low = A16 swap override enabled.  
High = Default.

BOOT BIOS STRAP

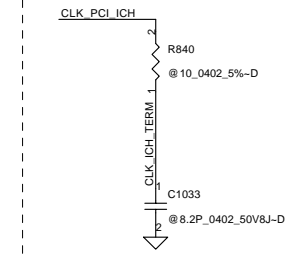
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

\*

COIN CELL RTC BATTERY



Place close to pin U32.B10



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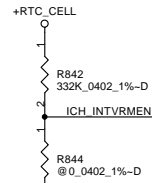
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Size	Document Number
401490	Rev A
Date: Wednesday, March 28, 2007	Sheet 20 of 48

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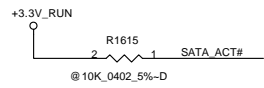
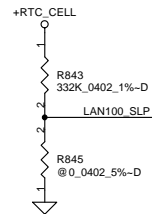
**ICH8-M Internal VR Enable Strap**  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH\_INTVRMEN Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

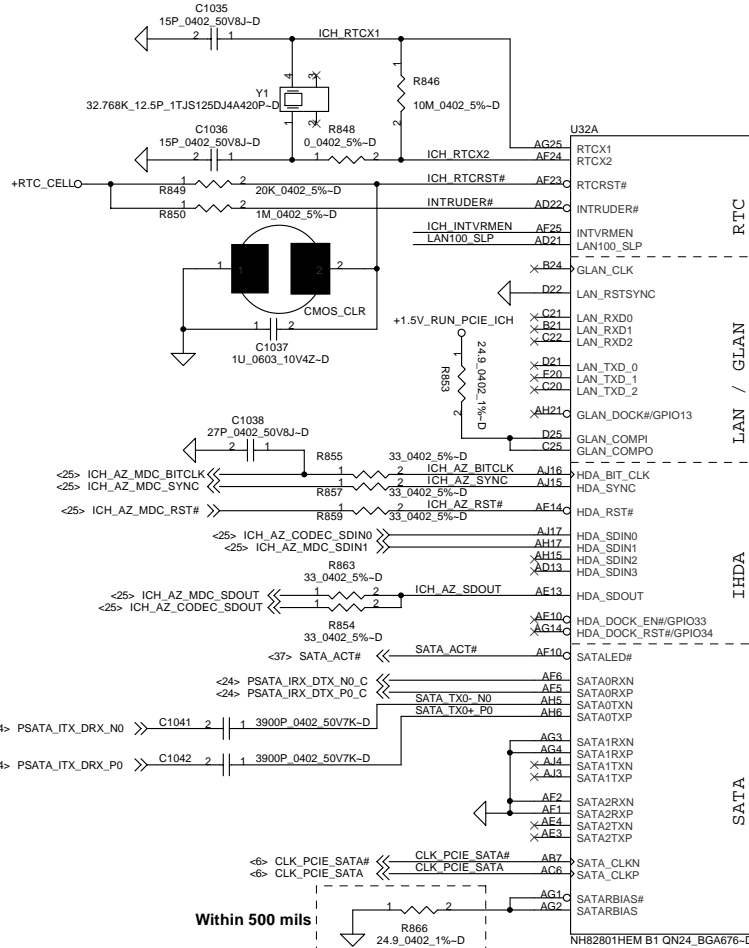
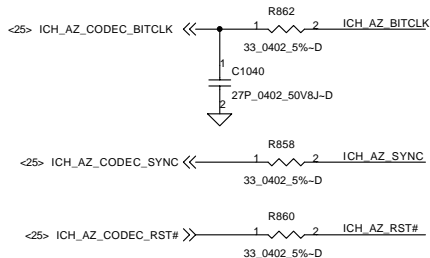


**ICH8-M LAN100 SLP Strap**  
(Internal VR for VccLAN1.05 and VccCL1.05)

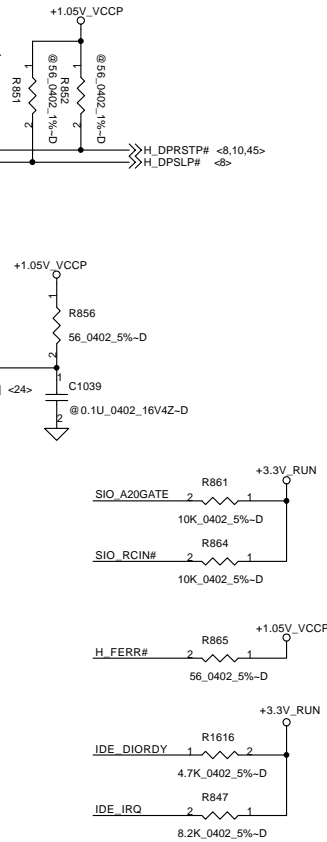
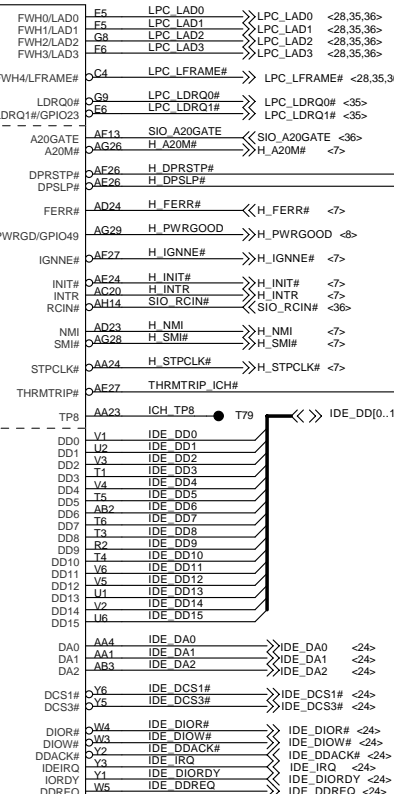
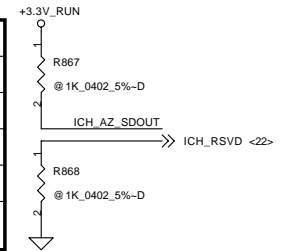
ICH\_LAN100\_SLP Low = Internal VR Disabled  
High = Internal VR Enabled(Default)



Place close to U32



XOR Chain Entrance STRAP		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

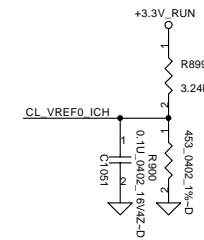
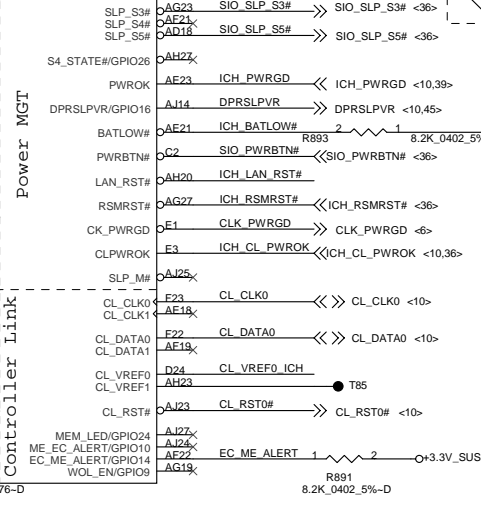
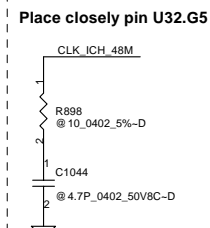
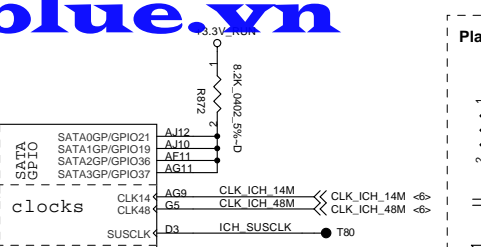


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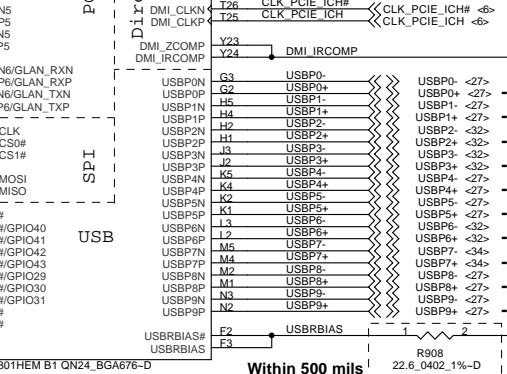
No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

**MINI WLAN (Mini Card 2)--->**

I - Express		ct Media Interface			
N1		DMIORXN	Y27	DMI MTX_IRX_N0	<10>
N1		DMIOIRXP	Y26	DMI MTX_IRX_P0	<10>
N1		DMIOITXN	U29	DMI MRX_ITX_N0	<10>
N1		DMIOITXP	U28	DMI MRX_ITX_P0	<10>
N2		DMI1RXN	Y27	DMI MTX_IRX_N1	<10>
N2		DMI1IRXP	Y26	DMI MTX_IRX_P1	<10>
N2		DMI1ITXN	U29	DMI MTX_ITX_N1	<10>
N2		DMI1ITXP	U28	DMI MTX_ITX_P1	<10>
N3		DMI2RXN	AB26	DMI MTX_IRX_N2	<10>
N3		DMI2IRXP	AB25	DMI MTX_IRX_P2	<10>
N3		DMI2ITXN	AA29	DMI MRX_ITX_N2	<10>
N3		DMI2ITXP	AA28	DMI MRX_ITX_P2	<10>
N4		DMI3RXN	AD27	DMI MTX_IRX_N3	<10>
N4		DMI3IRXP	AD26	DMI MTX_IRX_P3	<10>
N4		DMI3ITXN	AC29	DMI MRX_ITX_N3	<10>
N4		DMI3ITXP	AC28	DMI MRX_ITX_P3	<10>

PCI - Express

ICH SPI CS1#



R901  
24.9\_0402\_1%-D

- >Rear Right Bottom
- >Rear Right Top
- >Express Card
- >Bluetooth
- >Rear Left Bottom
- >Rear Left Top
- >OZ77CR6
- >Docking
- >Side Bottom
- >Side Top

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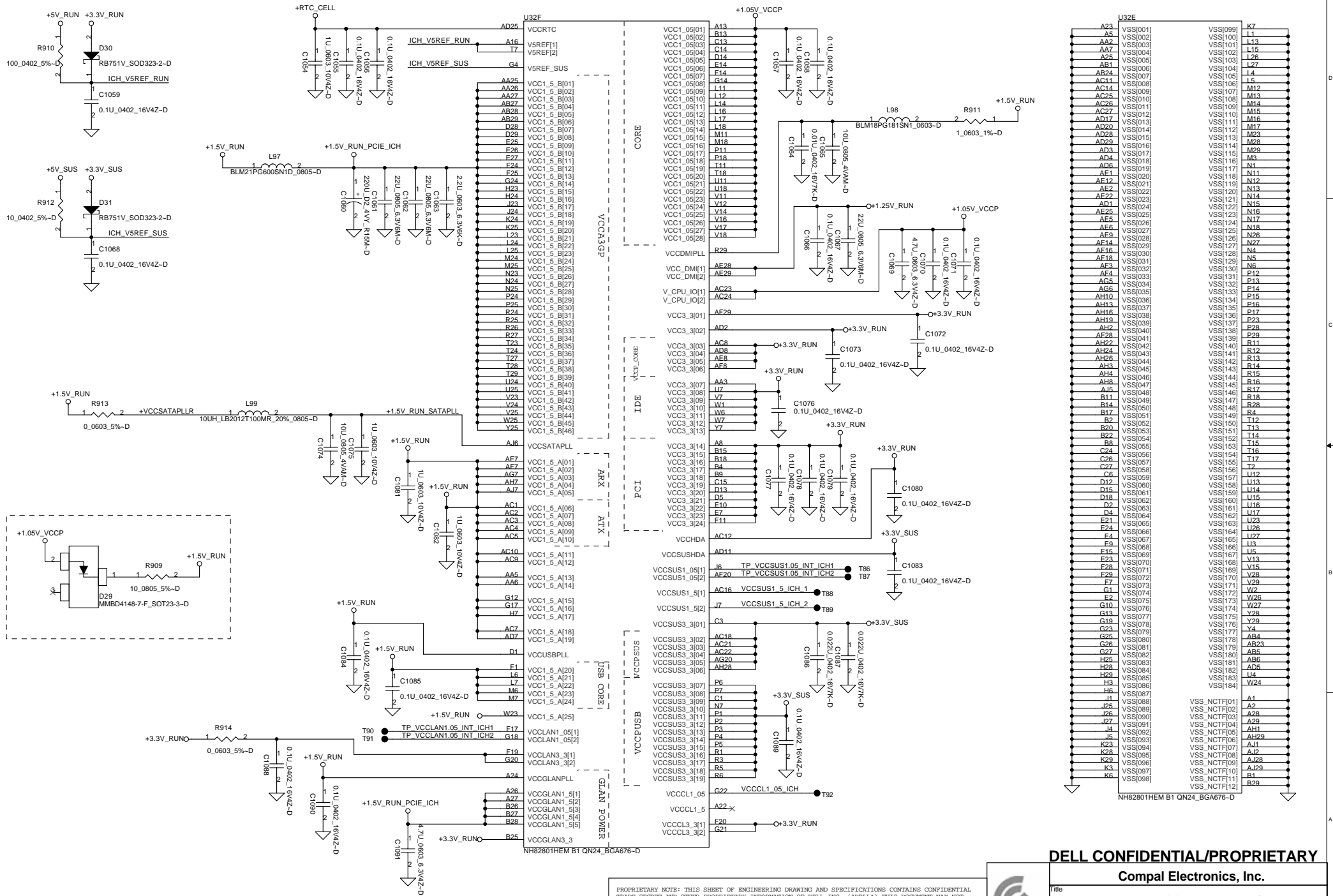
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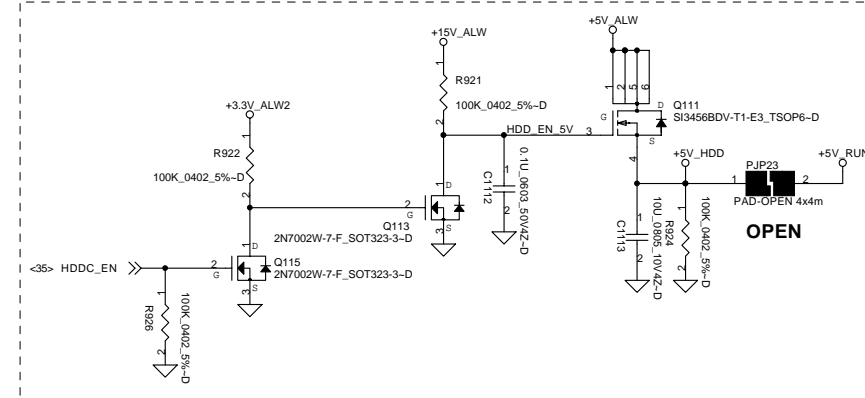
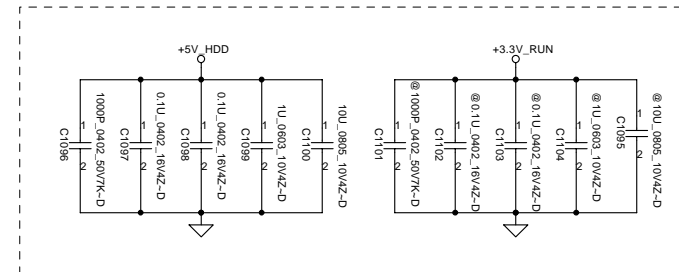
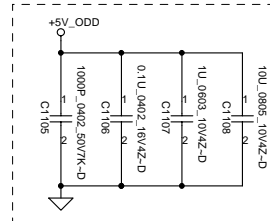
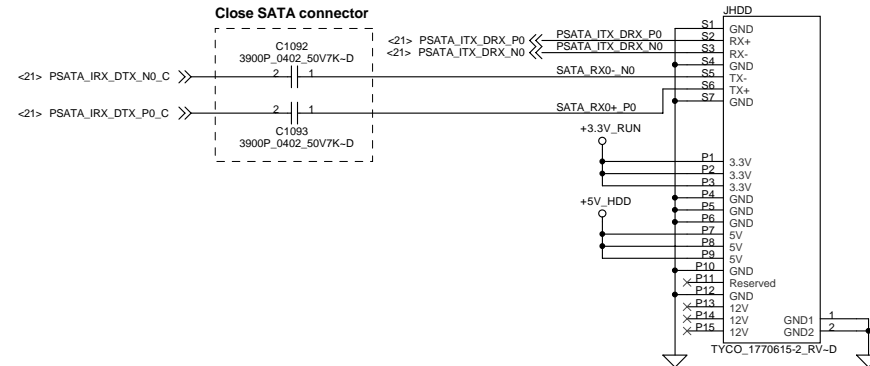
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Size	Document Number		Rev
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Date:	Wednesday, March 28, 2007	Sheet	22 of 48

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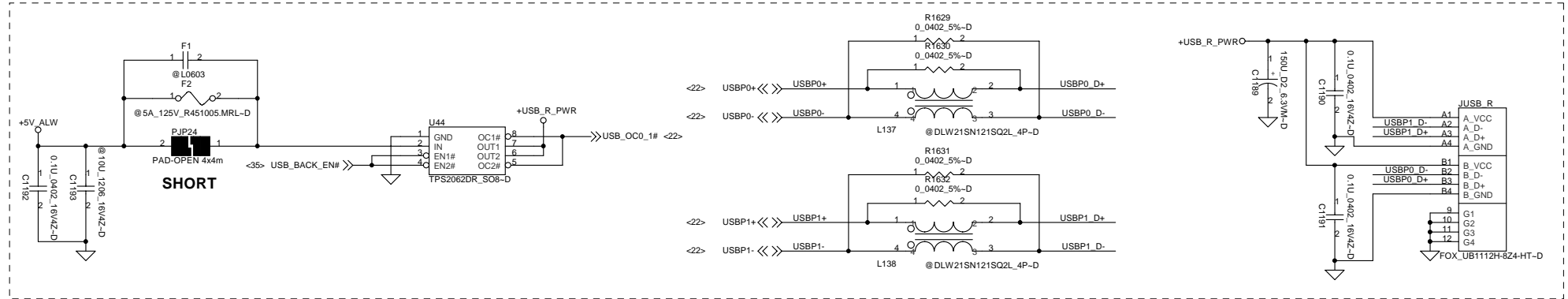


Date: Wednesday, March 28, 2007 Sheet 24 of 48

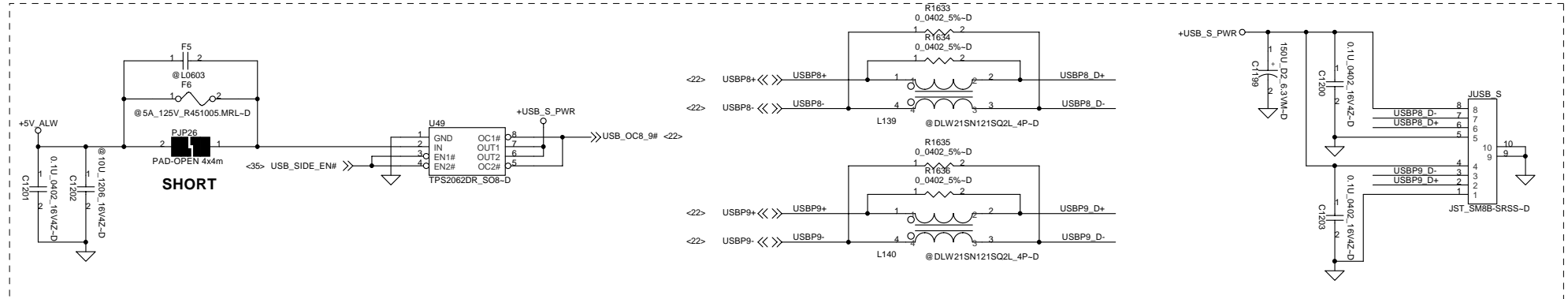




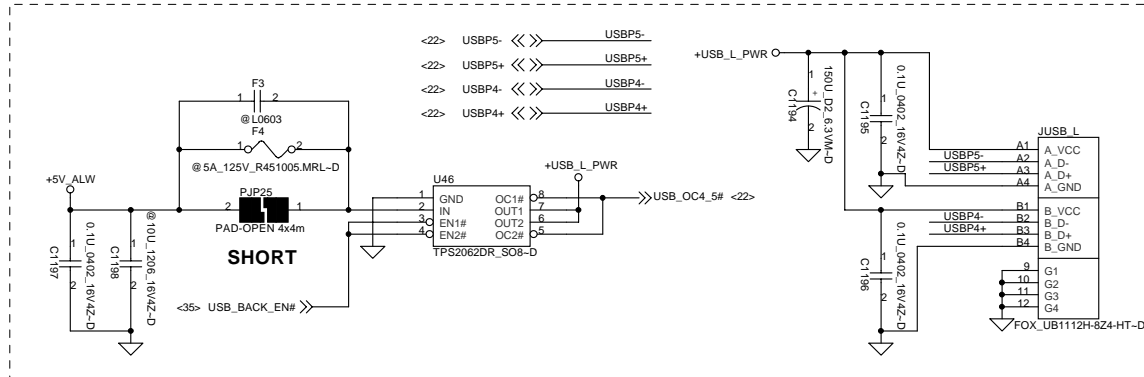
## Rear Right USB Port



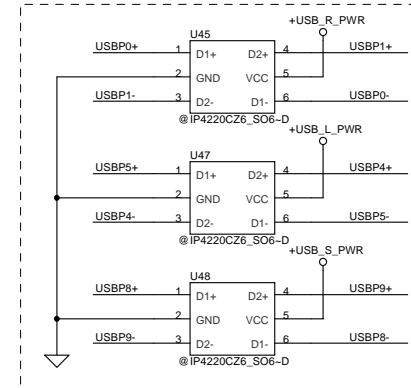
## Side USB Port



## Rear Left USB Port



Place U45, U47, U48 as close as USB connector



USB PORT#	DESTINATION
0	JUSB_R (Rear Right Bottom)
1	JUSB_R (Rear Right Top)
4	JUSB_L (Rear Left Bottom)
5	JUSB_L (Rear Left Top)
8	JUSB_S (Side Bottom)
9	JUSB_S (Side Top)

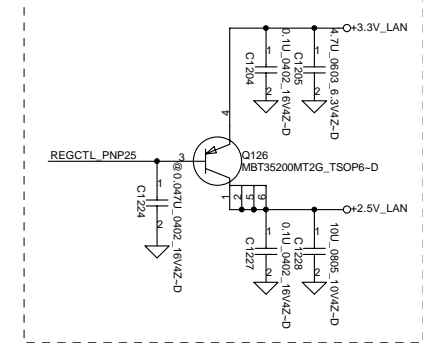
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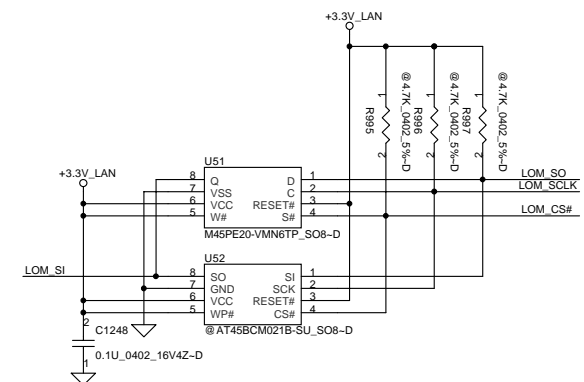
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Date:	Wednesday, March 28, 2007	Sheet	27 of 48

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### +2.5V\_LAN Regularator Control



LOM\_CABLE\_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM\_LOW\_PWR when LOM\_CABLE\_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping

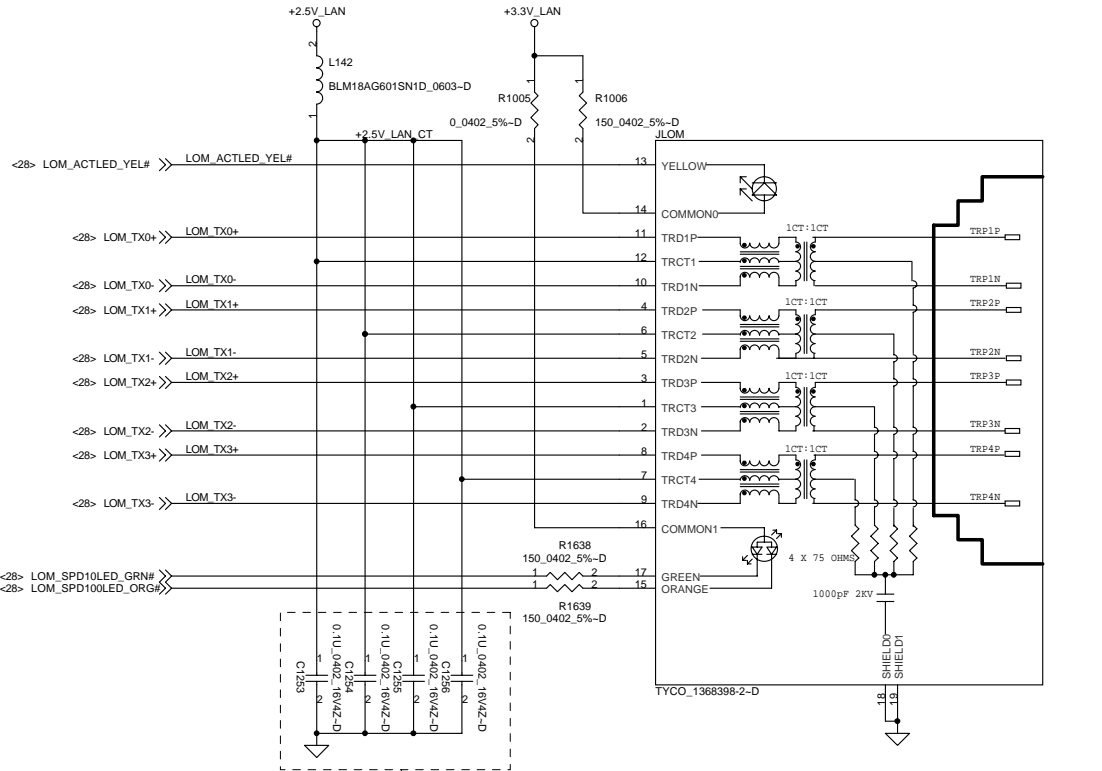
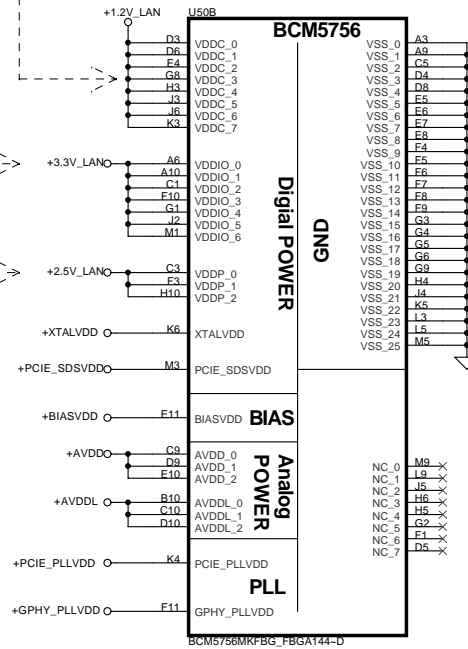
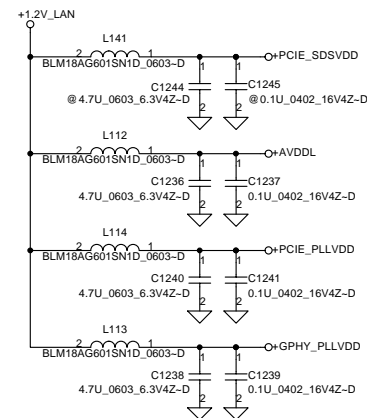
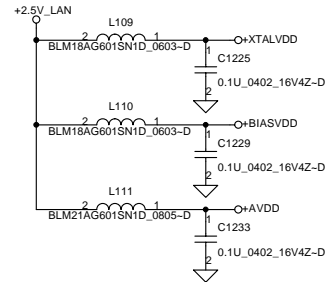
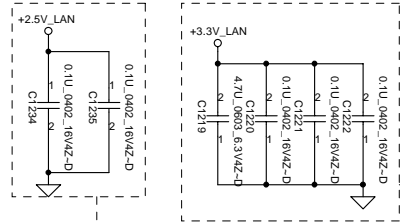
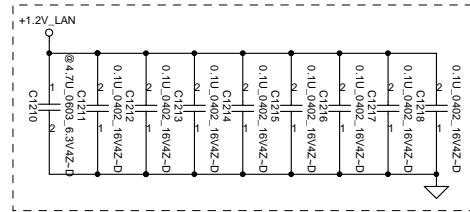


	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

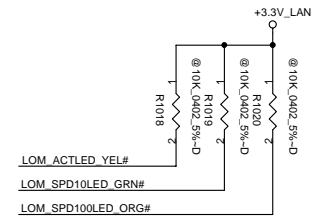
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Size	Document Number		Rev
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Date:	Wednesday, March 28, 2007	Sheet	28 of 48



Place as close as U50 as possible



Place these caps as close to the center tap pins of the mag/connector



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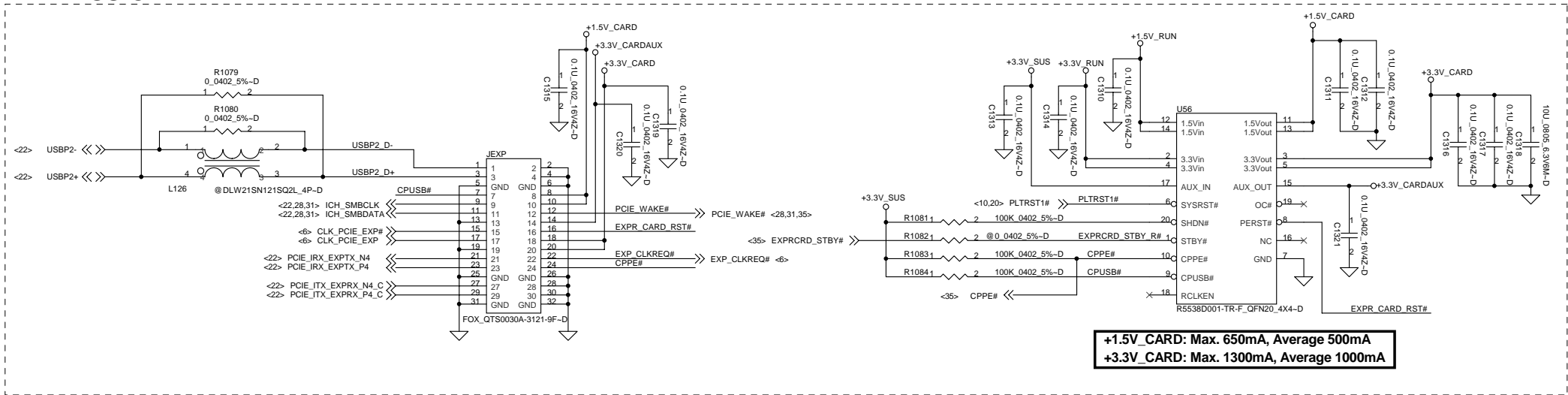
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Size	Document Number		
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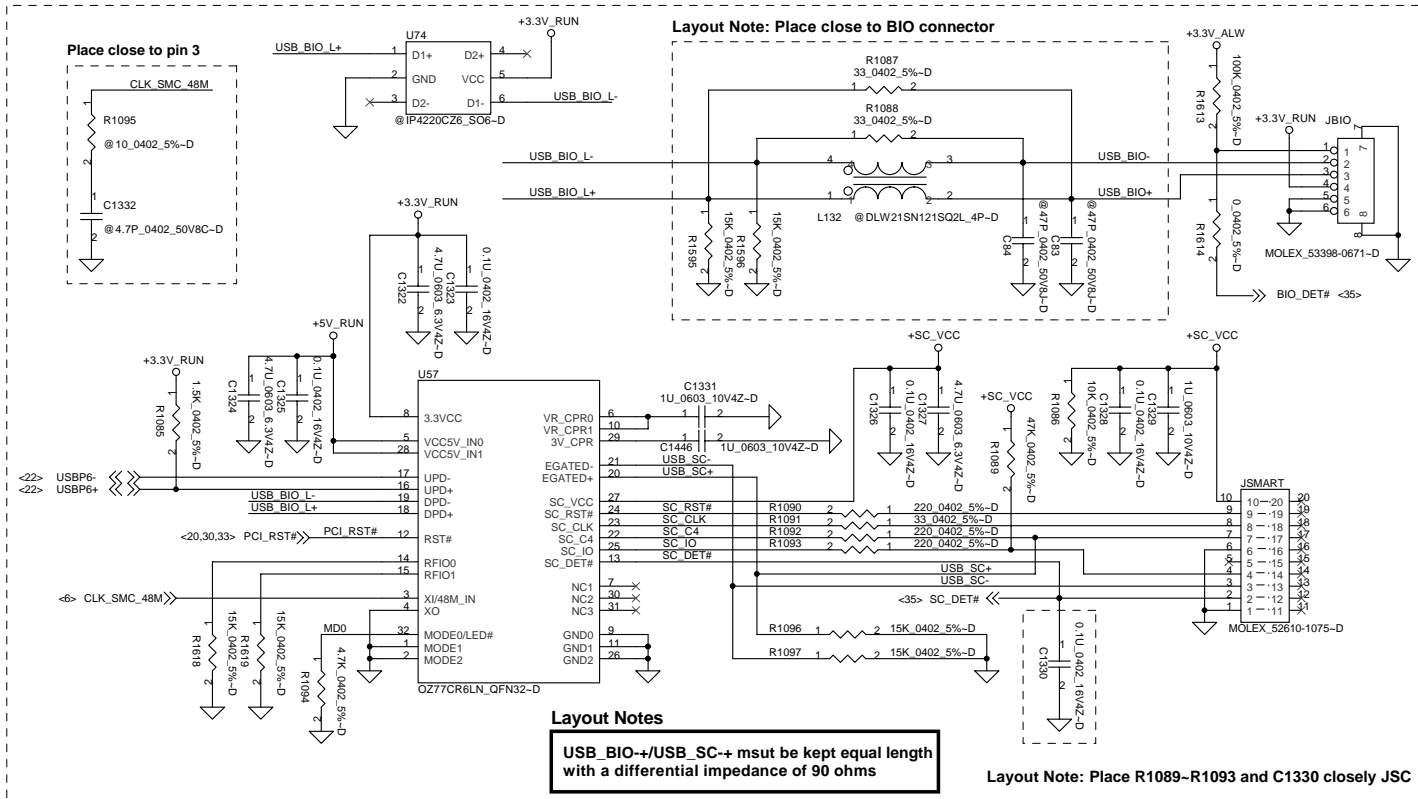




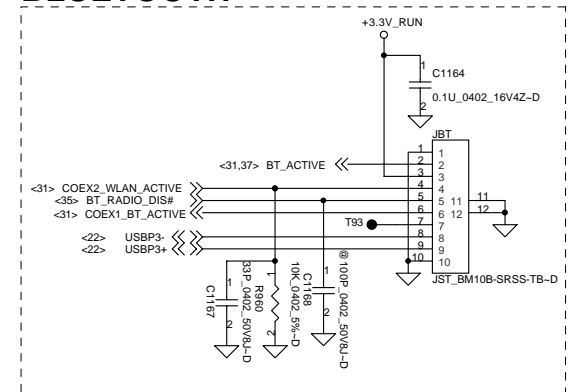
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## SMART CARD and Biometric Reader



## BLUETOOTH



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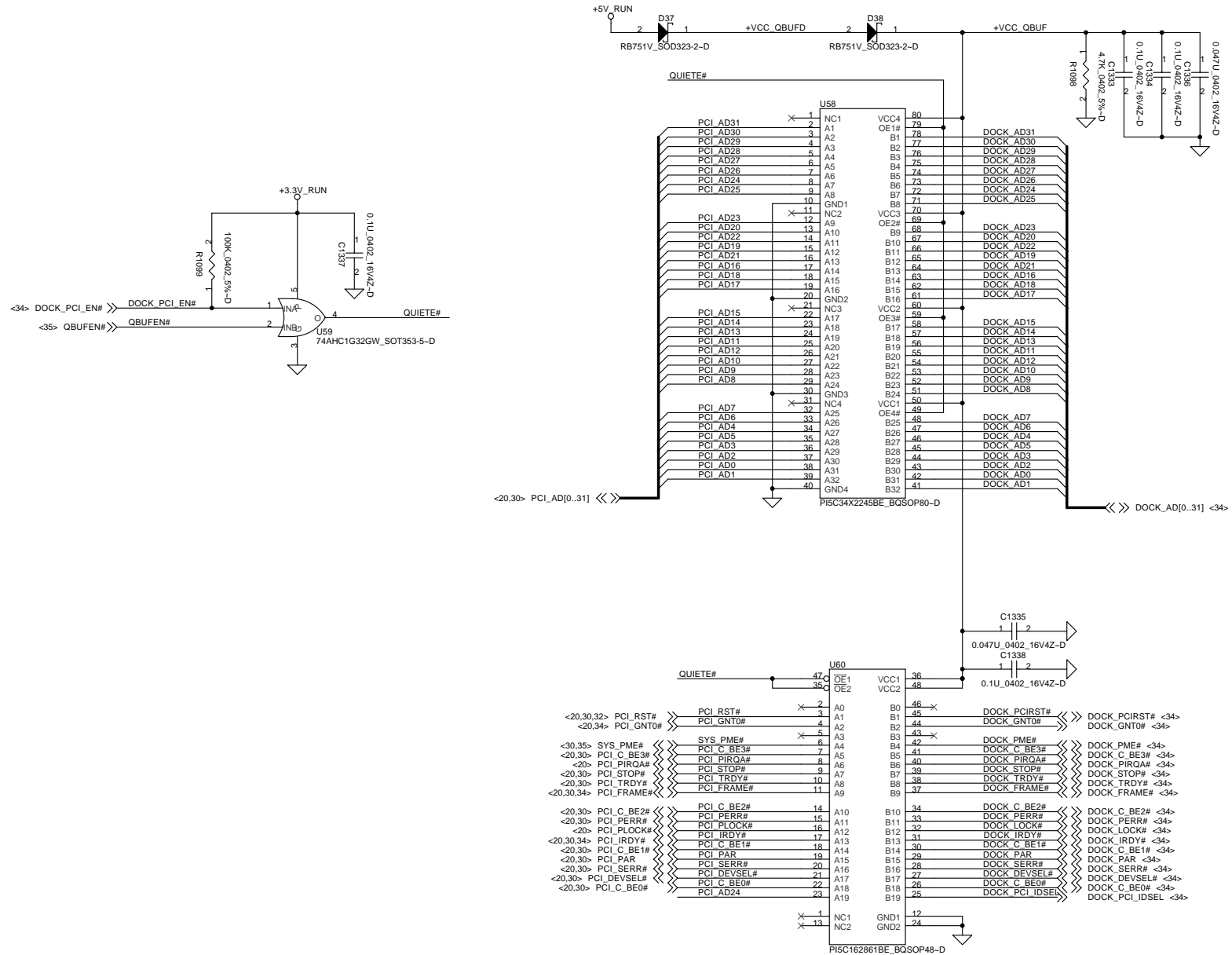
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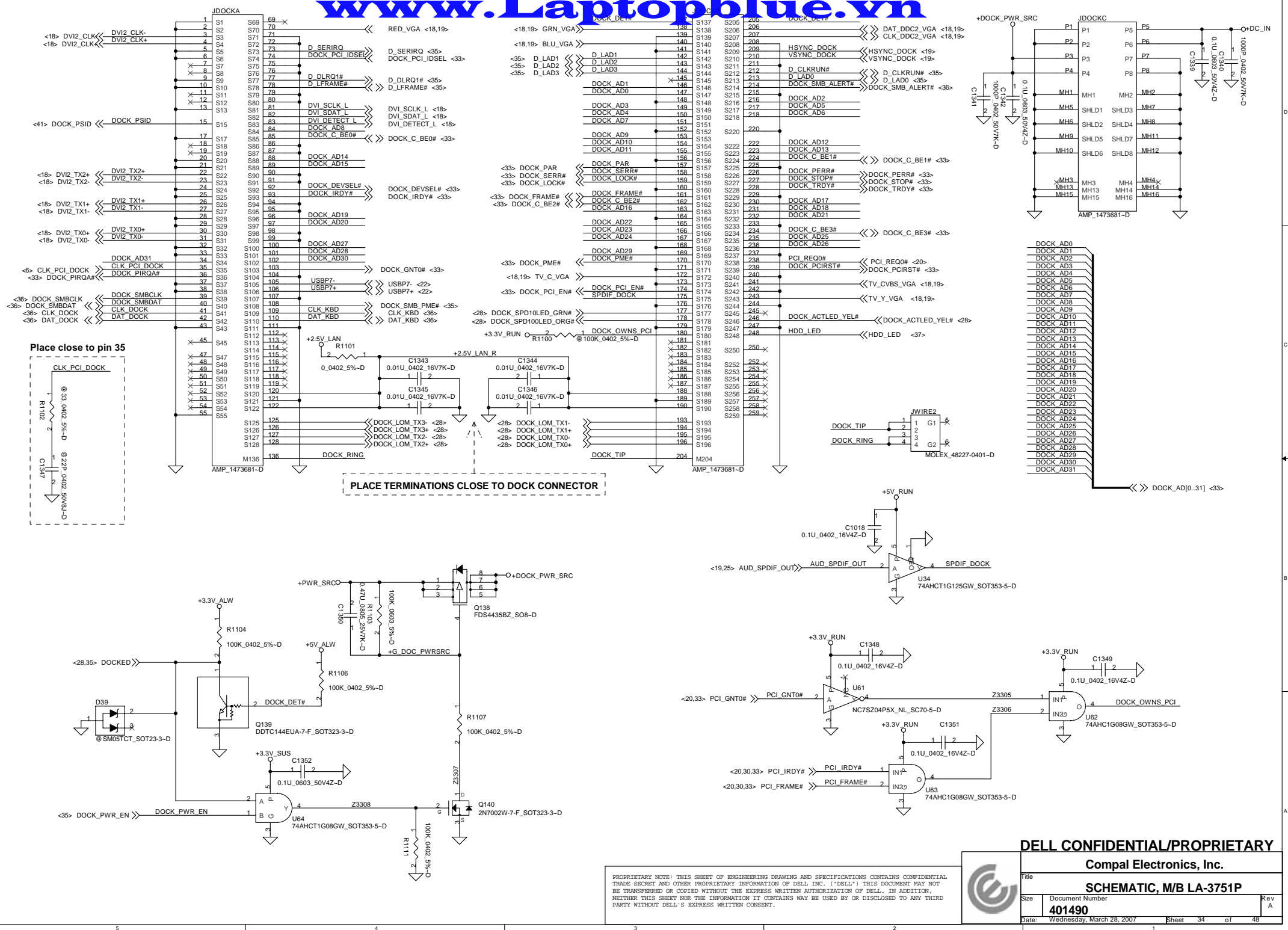
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401490

Wednesday, March 28, 2007 Sheet 33 of 48

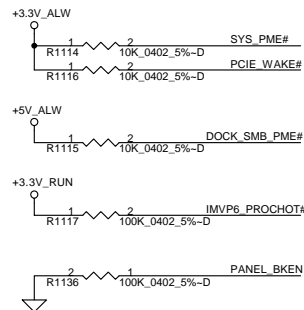
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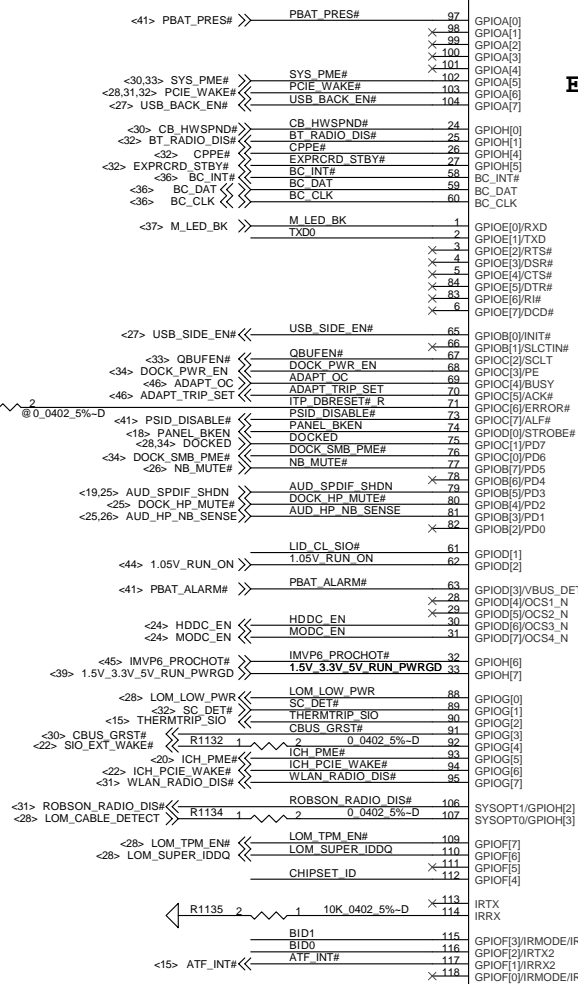
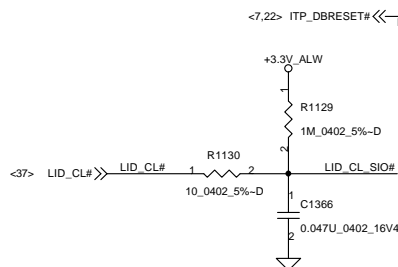
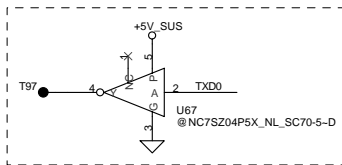
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Size Document Number  
401490  
Date: Wednesday, March 28, 2007 Sheet 34 of 48





Note: For system debug  
pin4 connect to serial port pin3



REV	BID1	BID0
X00	0	0
X01	0	1

## ECE5028-NU (ECE5018)

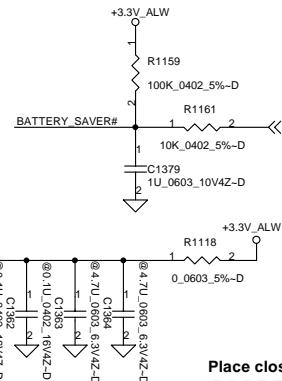
### USB

### TEST

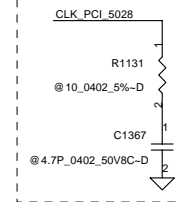
### CLK

### LPC

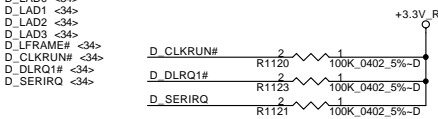
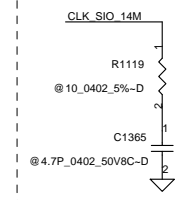
### DLPC



Place close to pin 56



Place close to pin 64



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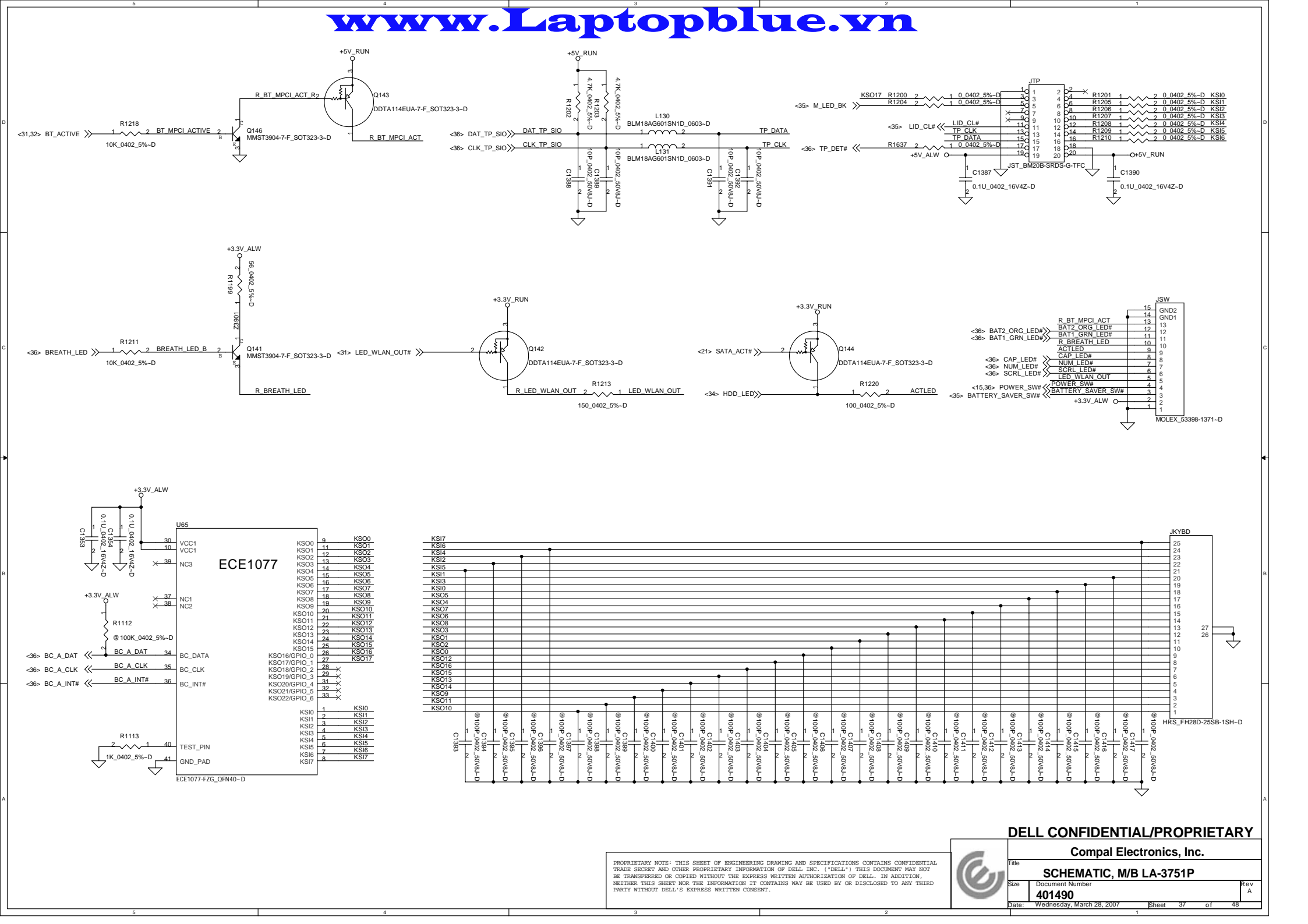
SCHEMATIC, M/B LA-3751P

Title	Document Number	Rev
	401490	A
Date	Wednesday, March 28, 2007	Sheet 35 of 48

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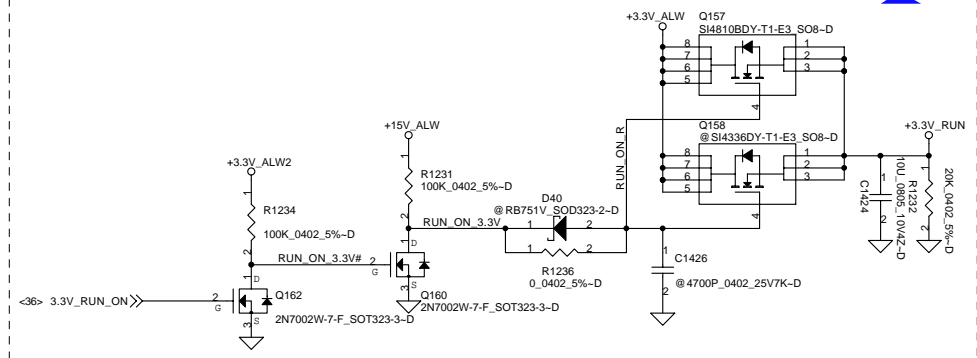


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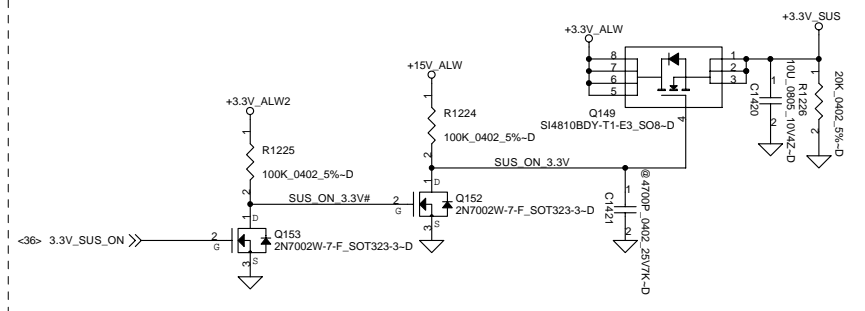
Size	Document Number	Rev
	<b>401490</b>	A

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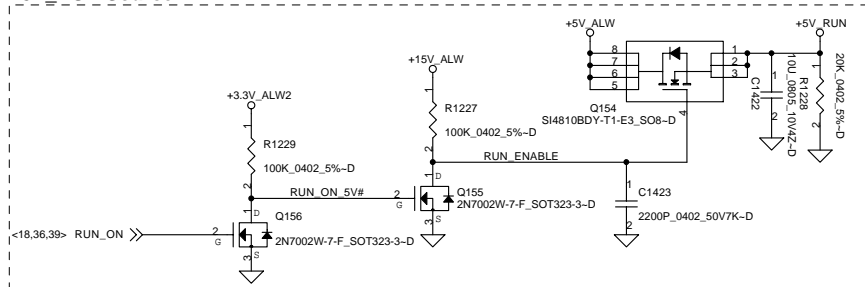
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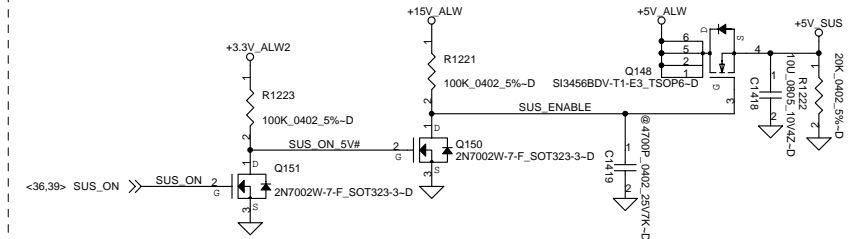
### +3.3V\_SUS Source



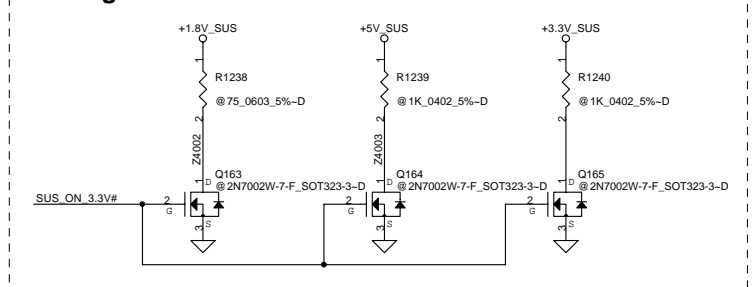
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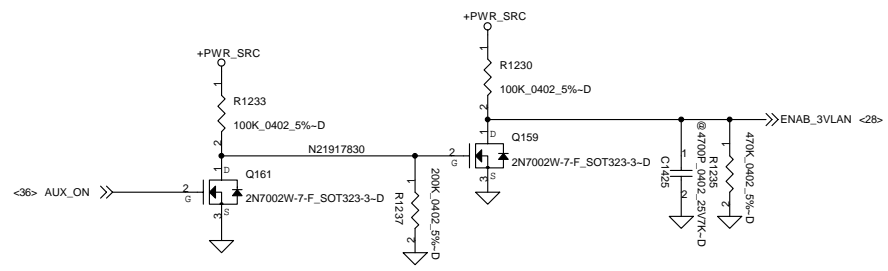
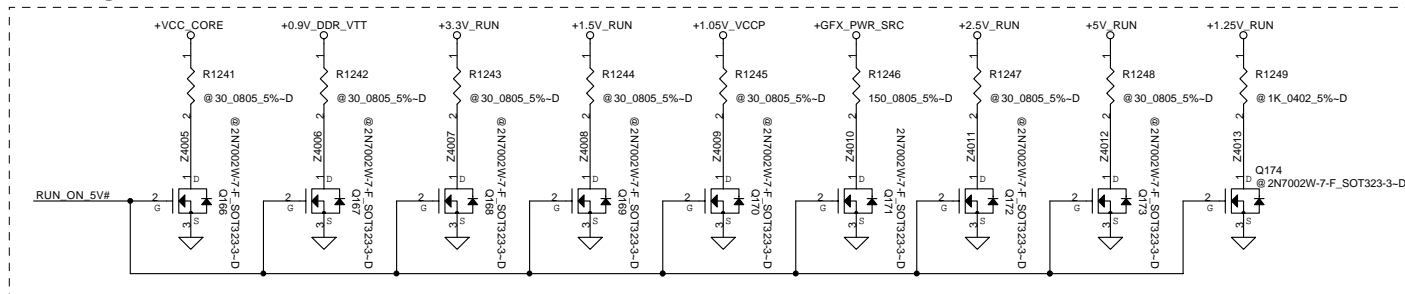
### +5V\_SUS Source



### Discharg Circuit



### Discharg Circuit



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SCHEMATIC, M/B LA-3751P			
Title	Document Number	Rev	A
Size	401490		
Date:	Wednesday, March 28, 2007	Sheet	38 of 48

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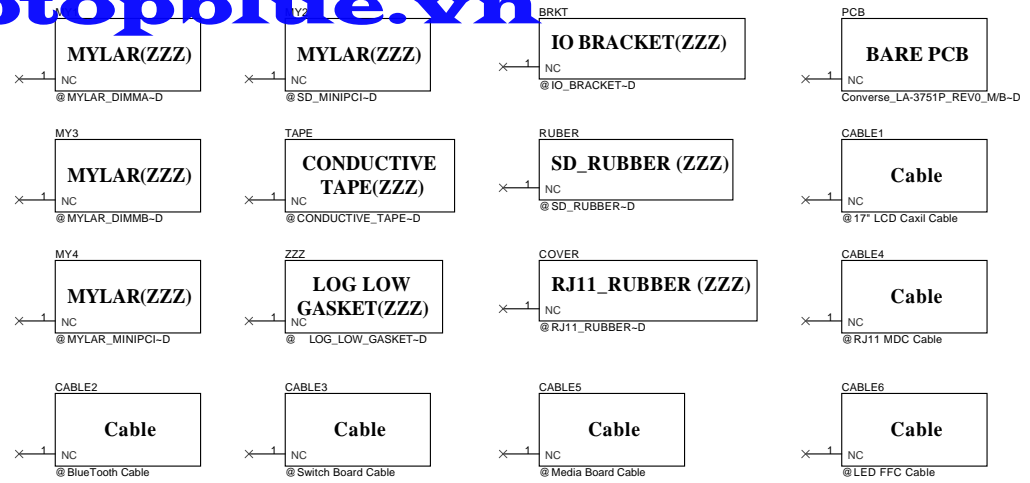
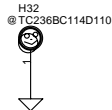
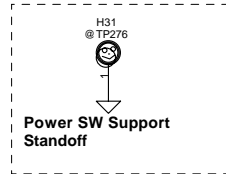
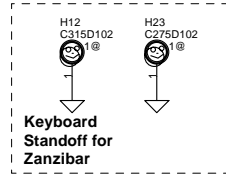
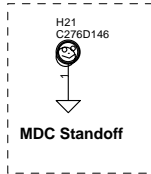
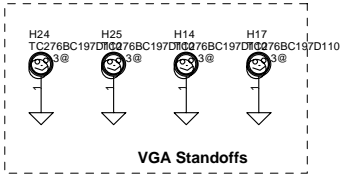
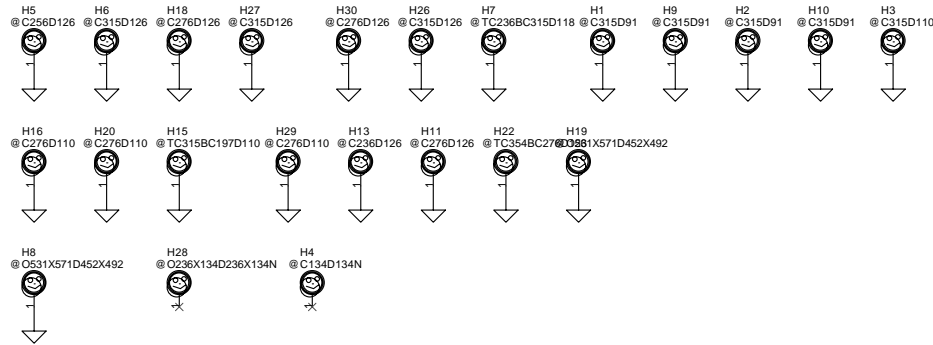
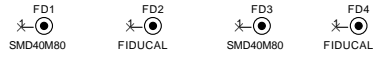


Size	Document Number	Rev
	<b>401490</b>	A
Date:	Wednesday, March 28, 2007	Sheet 39 of 48

HEX STANDOFF



Fiducial Mark



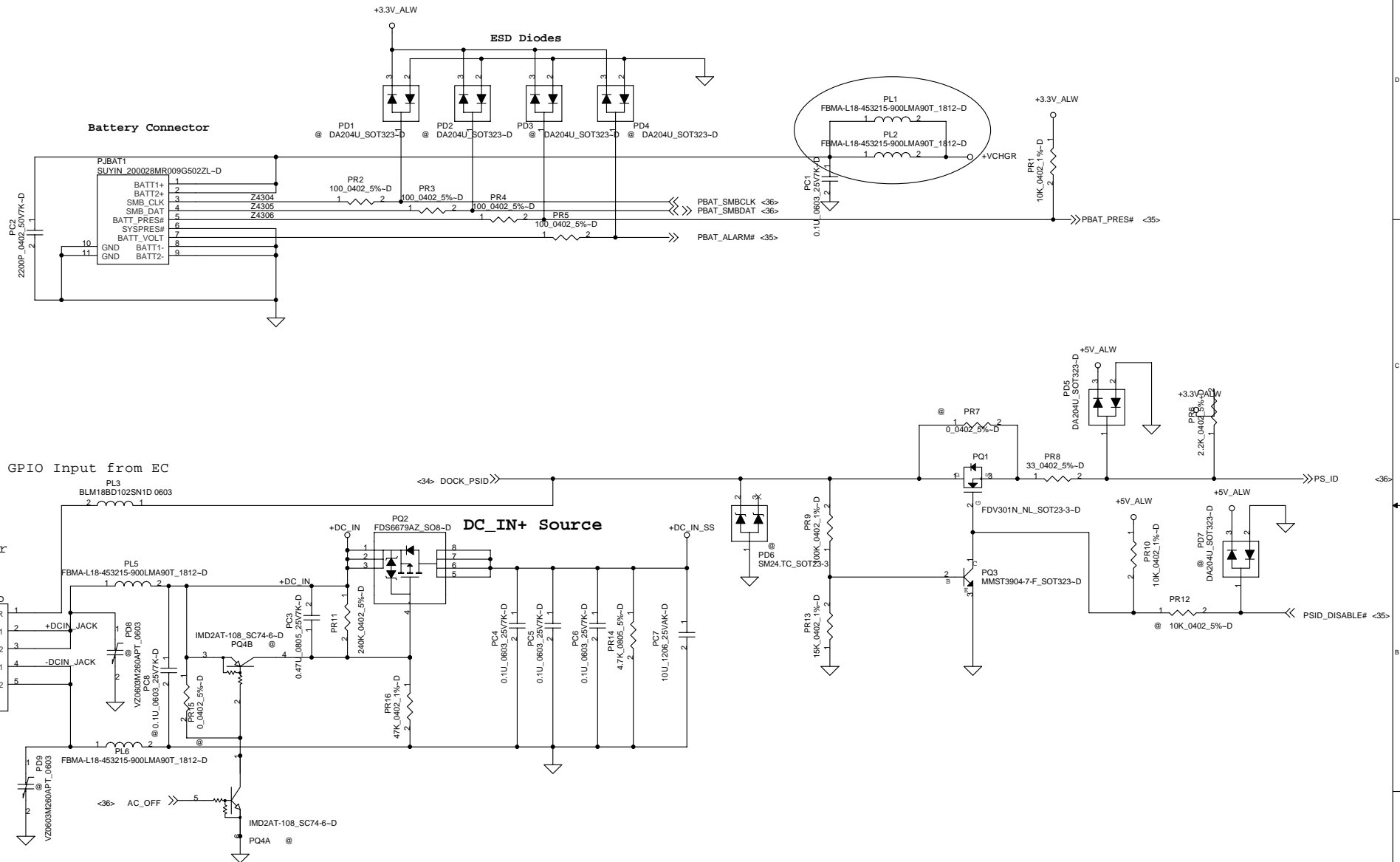
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Compal Electronics, Inc.

Title		SCHEMATIC, M/B LA-3751P	
Size	Document Number	Rev	
	401490	A	
Date:	Wednesday, March 28, 2007	Sheet	40 of 48



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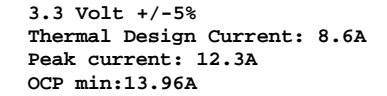
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Title SCHEMATIC, M/B LA-3751P

Size Document Number 401490

Date: Wednesday, March 28, 2007 Sheet 41 of 48

Ton=GND 400KHz/500KHz

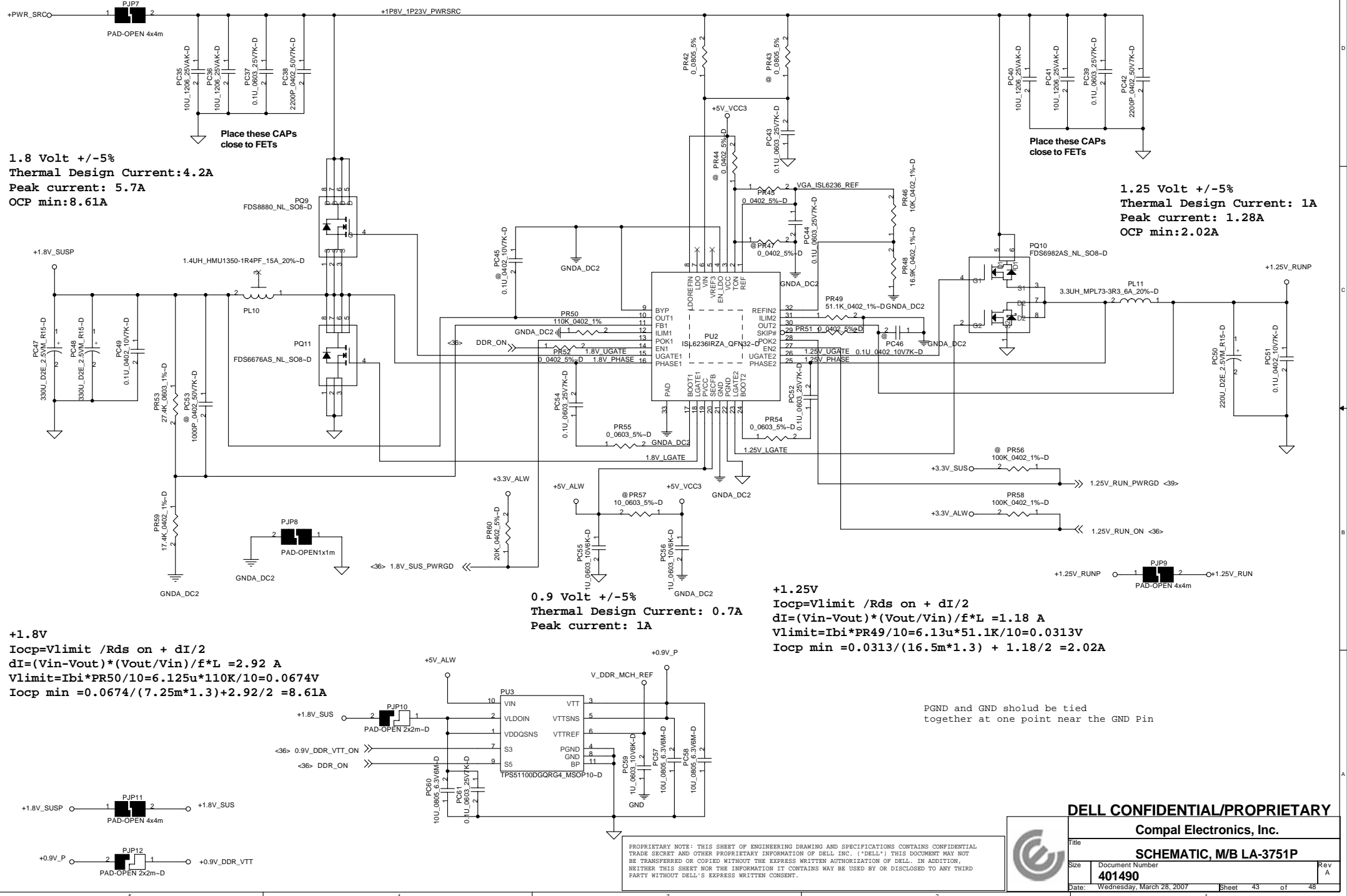


```
+3.3V_ALWP
Iocp=Vlimit /Rds on + dI/2
dI=(Vin-Vout)*(Vout/Vin)/f*L =1.82A
Vlimit=Ibi*PR25/10=6.125u*200K/10=0.123V
Iocp min =0.123/ 7.25m*1.3 + 1.82/2 =13.96A
```



Size	Document Number <b>401490</b>	Rev A
Date:	Wednesday, March 28, 2007	Sheet 42 of 48





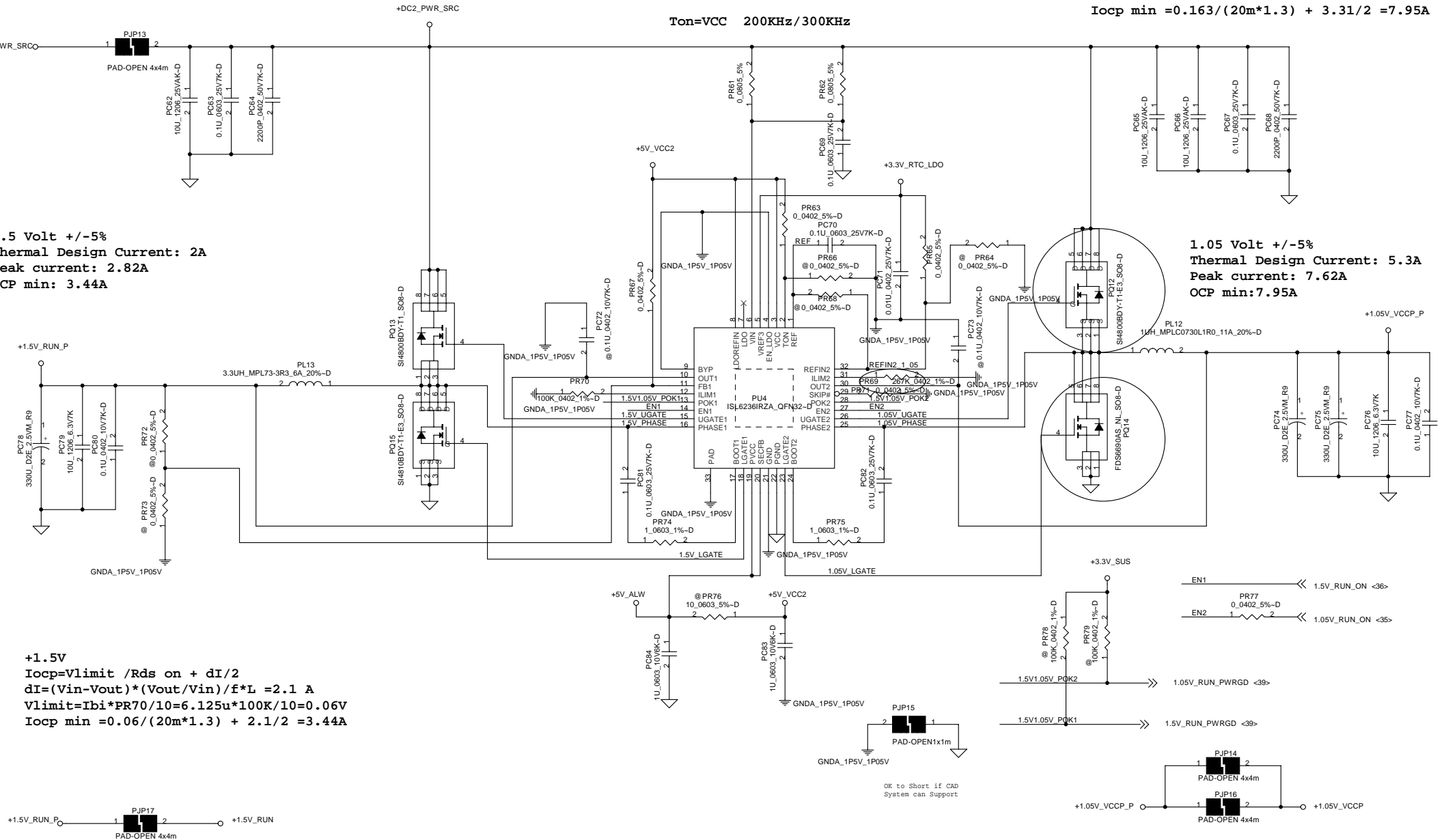
+1.5V\_RUN / +1.05V\_VCCP / +3.3V\_ALW / +3.3V\_RTC\_LDO

Ton=VCC 200KHz/300KHz

+1.05V  
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$   
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 3.31A$   
 $V_{limit} = I_{bi} * PR69 / 10 = 6.125u * 267K / 10 = 0.163V$   
 $I_{ocp\ min} = 0.163 / (20m * 1.3) + 3.31 / 2 = 7.95A$

1.5 Volt +/-5%  
 Thermal Design Current: 2A  
 Peak current: 2.82A  
 OCP min: 3.44A

1.05 Volt +/-5%  
 Thermal Design Current: 5.3A  
 Peak current: 7.62A  
 OCP min: 7.95A



+1.5V  
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$   
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 2.1 A$   
 $V_{limit} = I_{bi} * PR70 / 10 = 6.125u * 100K / 10 = 0.06V$   
 $I_{ocp\ min} = 0.06 / (20m * 1.3) + 2.1 / 2 = 3.44A$

EN1 1.5V\_RUN\_ON <36>  
 EN2 1.05V\_RUN\_ON <35>

1.5V1.05V\_POK2  
 1.5V1.05V\_POK1  
 1.05V\_RUN\_PWRGD <39>  
 1.5V\_RUN\_PWRGD <39>

+1.05V\_VCCP\_P  
 +1.05V\_VCCP

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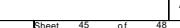
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Title  
 SCHEMATIC, M/B LA-3751P  
 Size Document Number  
 401490  
 Date Wednesday, March 28, 2007 Sheet 44 of 48 Rev A

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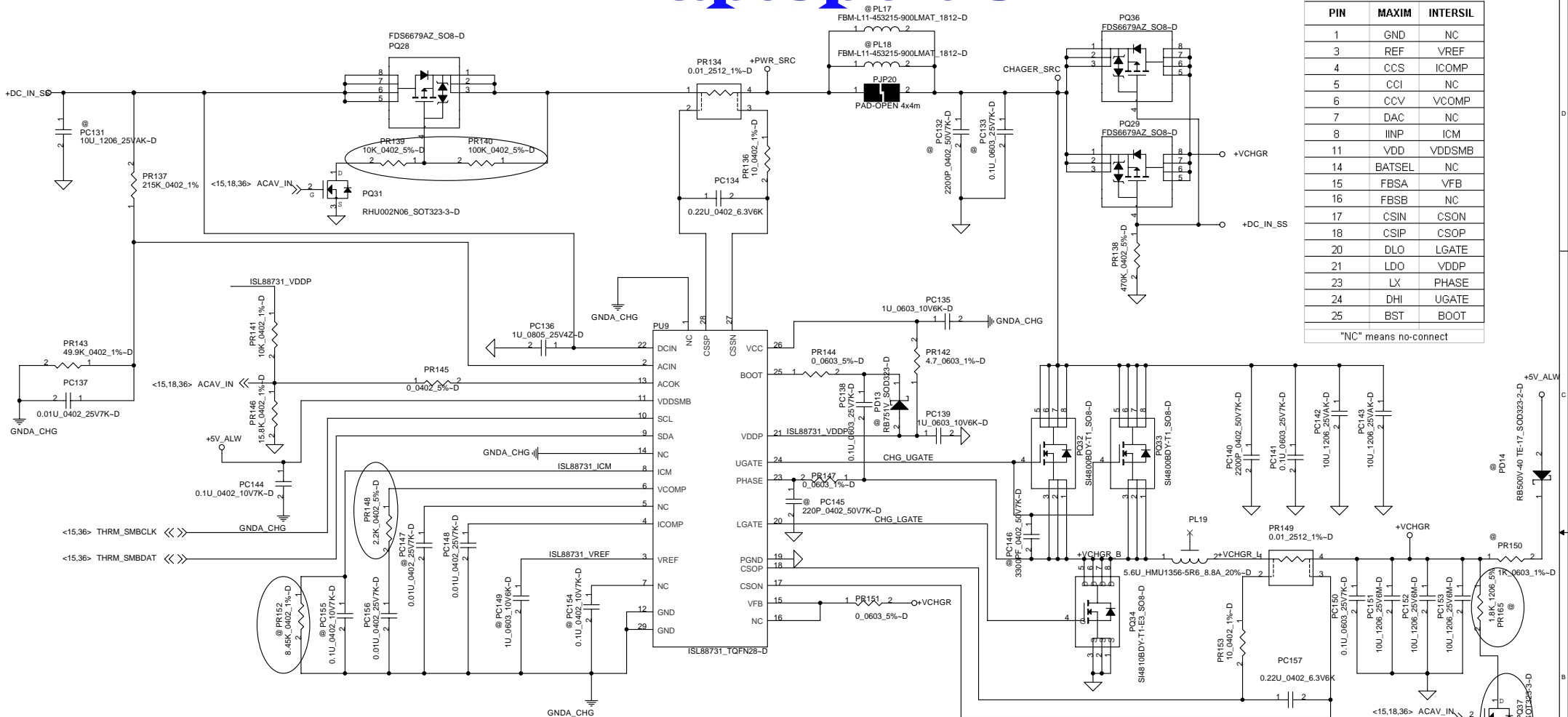
OK to Short if CAD System can Support



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TABLE 3, PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		



Version Change List ( P. I. R. List )

Item

Page#

Title

Date

Request  
Owner

Issue Description

Solution Description

Rev.

1							
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Compal Electronics, Inc.

Title

SCHEMATIC, M/B LA-3751P

Size

Document Number

401490

Rev

A

Date:

Wednesday, March 28, 2007

Sheet

47

of

48

Version Change List ( P. I. R. List )

Item

Page#

Title

Date

Request  
Owner

Issue Description

Solution Description

Rev.

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Title

SCHEMATIC, M/B LA-3751P

Size

Document Number

401490

Rev

A

Date:

Wednesday, March 28, 2007

Sheet

48

of

48