
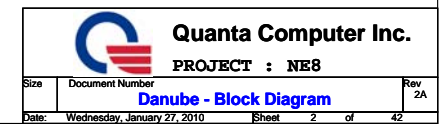


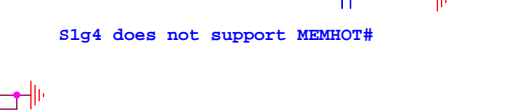
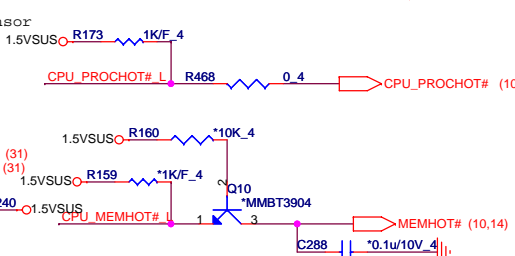
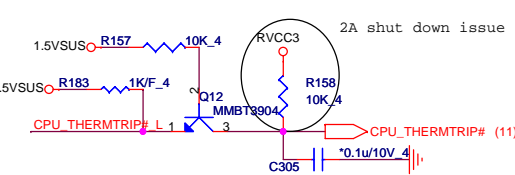
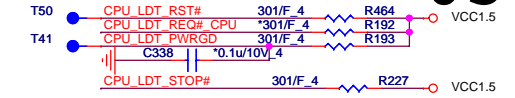
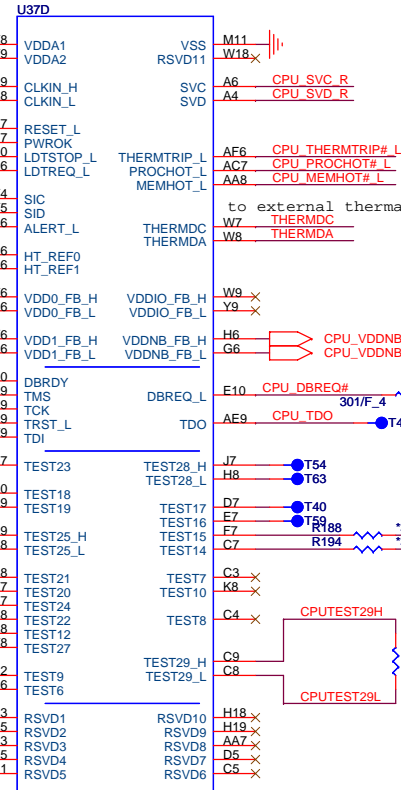
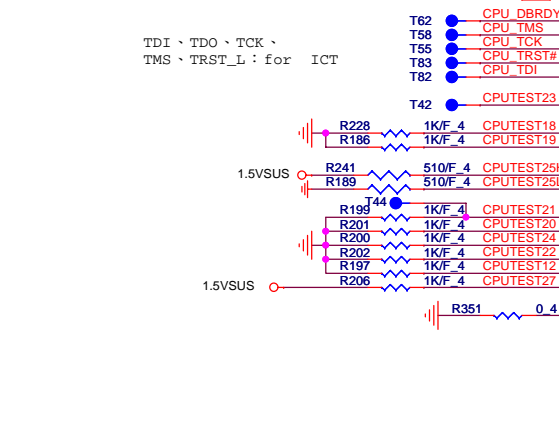
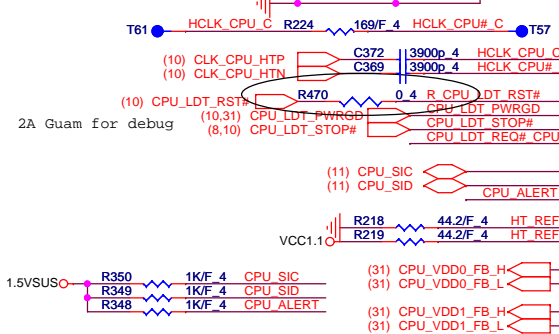
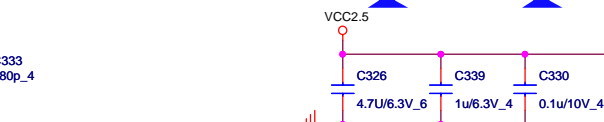
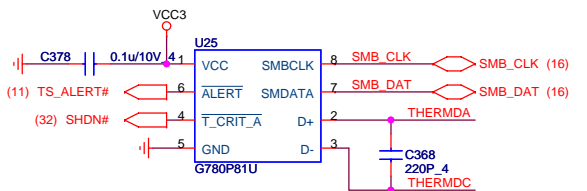
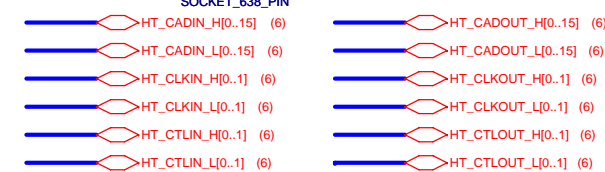
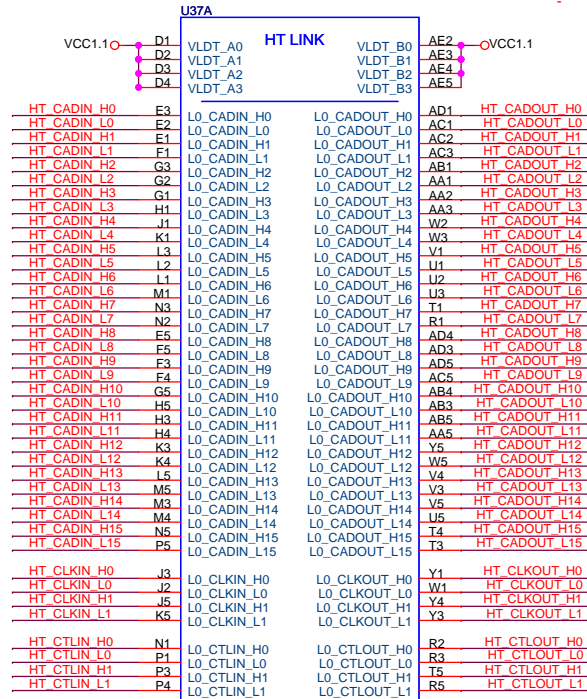
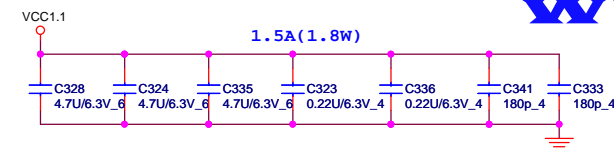
Page	Title of schematic page	Rev.	Date
01	Page List	2A	12/24
02	Block Diagram	2A	12/24
03	CPU-Champlain HT/CONTROL (1/3)	2A	01/04
04	CPU-Champlain MEMORY (2/3)	1B	12/16
05	CPU-Champlain POWER/GND (3/3)	1B	12/08
06	NB-RS880M HT/SP-MEM (1/4)	1B	12/08
07	NB-RS880M GFX/PCIE (2/4)	1A	09/24
08	NB-RS880M SYSTEM (3/4)	1A	09/24
09	NB-RS880M POWER (4/4)	1A	09/24
10	SB-SB820M PCI/CLK/LPC (1/4)	1A	09/24
11	SB-SB820M AUDIO/USB (2/4)	1A	09/24
12	SB-SB820M SATA (3/4)	1B	12/08
13	SB-SB820M POWER (4/4)	1A	09/24
14	DDR3 SODIMM* 2 (5.2mm+9.2mm)	2A	12/24
15	ATI-Madison LP PCIE/LVDS (1/5)	2A	12/24
16	ATI-Madison LP MAIN I/O (2/5)	2A	12/24
17	ATI-Madison LP POWER/GND (3/5)	2A	12/24
18	ATI-Madison LP Display POWER (4/5)	2A	12/24
19	ATI-Madison LP MEM I/F (5/5)	2A	12/24
20	ATI-Madison LP (DDR3 V-ram a)	2A	12/24
21	ATI-Madison LP (DDR3 V-ram b)	1B	12/08
22	CRT/LVDS	2A	12/24

Page	Title of schematic page	Rev.	Date
23	HDMI	1B	12/09
24	WLAN/HDD/ODD	1B	12/08
25	Card Reader RTS5186	1B	12/08
26	Express Card/BT/LED	1B	12/08
27	Codec-ALC269Q VB5 GR	1B	12/08
28	LAN RTL8111E	1B	12/08
29	NPCE781	1B	12/08
30	KB/USB/FAN/PS	1B	12/09
31	VCORE(ISL6265A)	1A	09/24
32	3VPCU&5VPCU(PM6686)	1A	09/24
33	1.5VSUS/VTT_MEM	1A	09/24
34	DYN_VCC1.1(OZ8116LN)	1A	09/24
35	VCC1.1(OZ8116LN)-7A	1A	09/24
36	VGA_CORE(OZ8116)-16A	1A	09/24
37	VCC1.8/0.9/2.5/1.0	1A	09/24
38	POWER(BAT IN / ADA IN/ UL)	1A	09/24
39	CHARGER (ISL6252A)	1A	09/24
40	Small board connector	1A	09/24
41	Power Sequence		
42	CHANGE LIST		

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

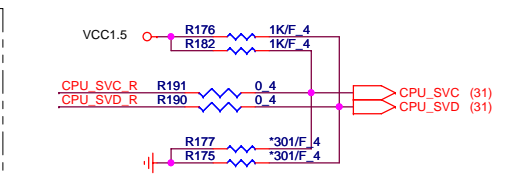
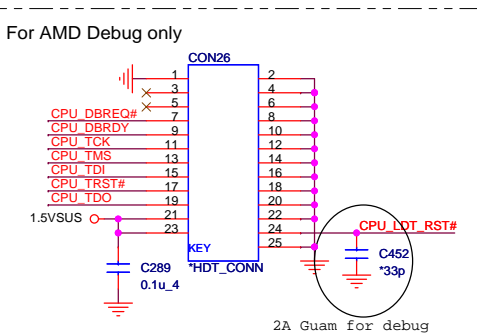
 Quanta Computer Inc. PROJECT : NE8		Rev 2A
AMD Danube		
Date:	Wednesday, January 27, 2010	Sheet 1 of 42





VFIX MODE VID Override Circuit

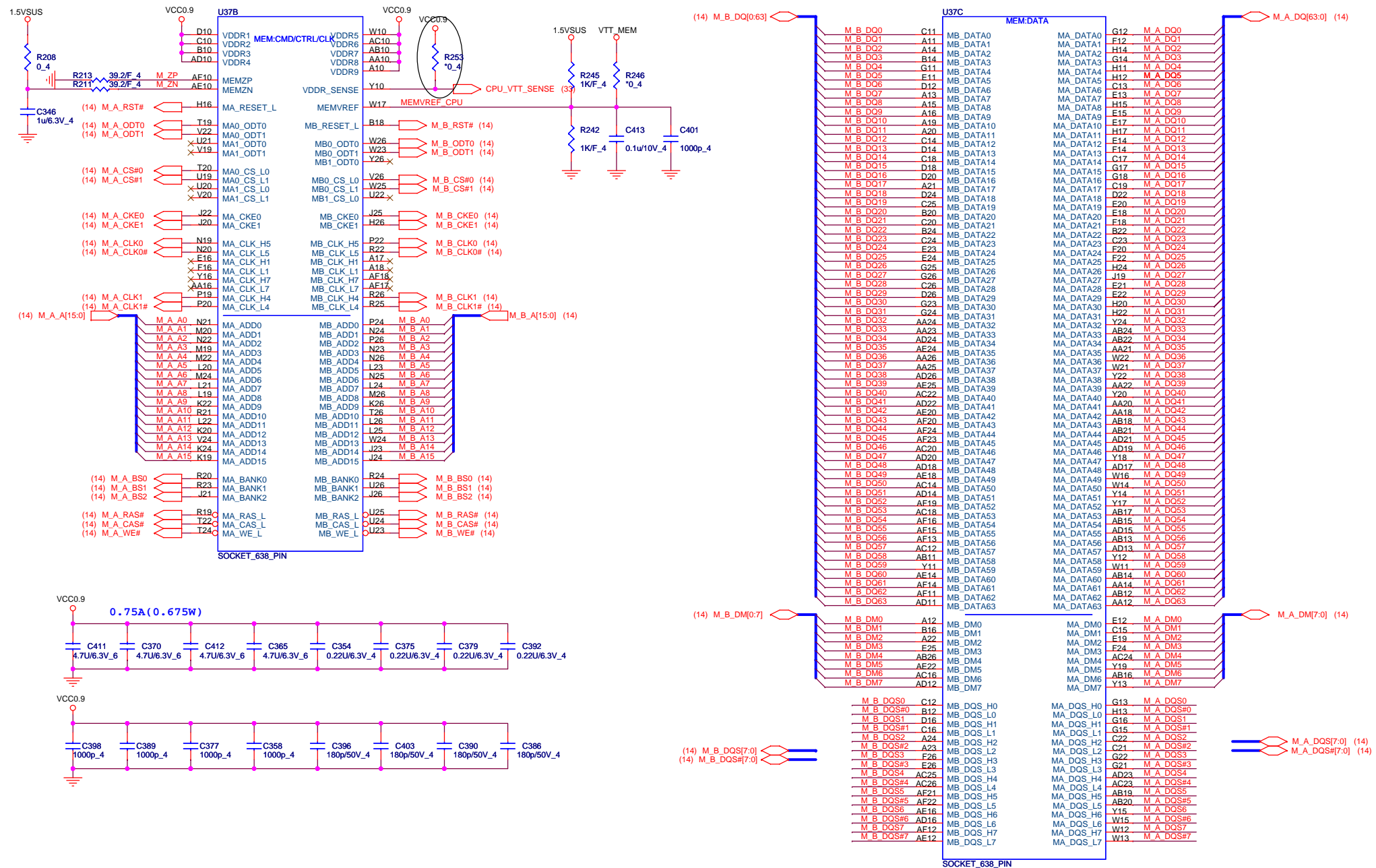
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



Quanta Computer Inc.
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Size	Document Number	Rev
	CPU HT/CONTROL(1/3)	2A
Date:	Wednesday, January 27, 2010	Sheet 3 of 42

1.Level 1 Environment-related Substances Should NEVER be Used.
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Quanta Computer Inc.

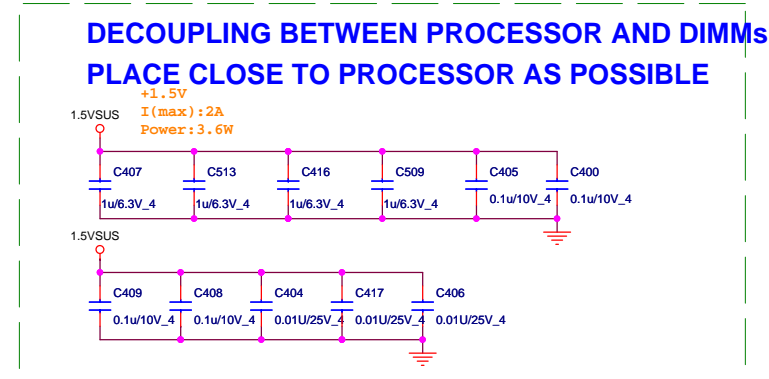
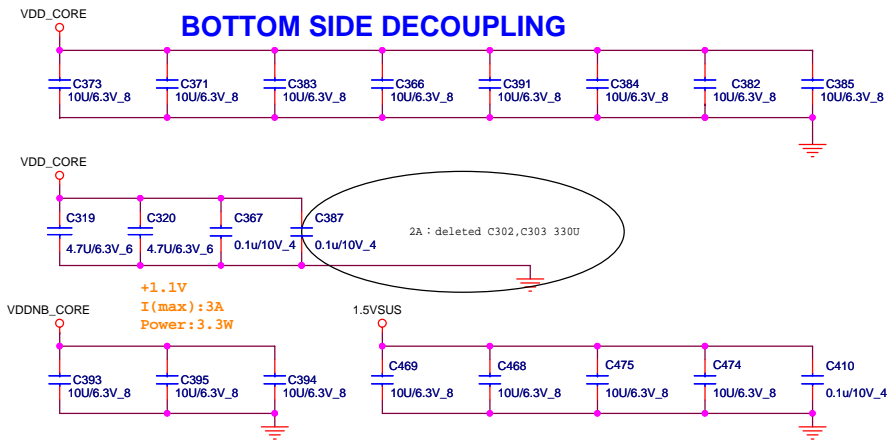
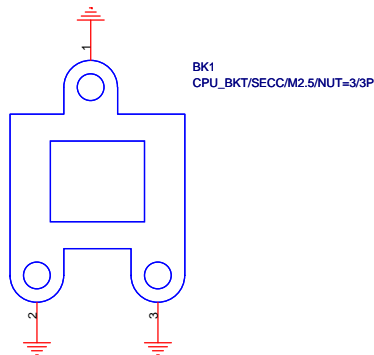
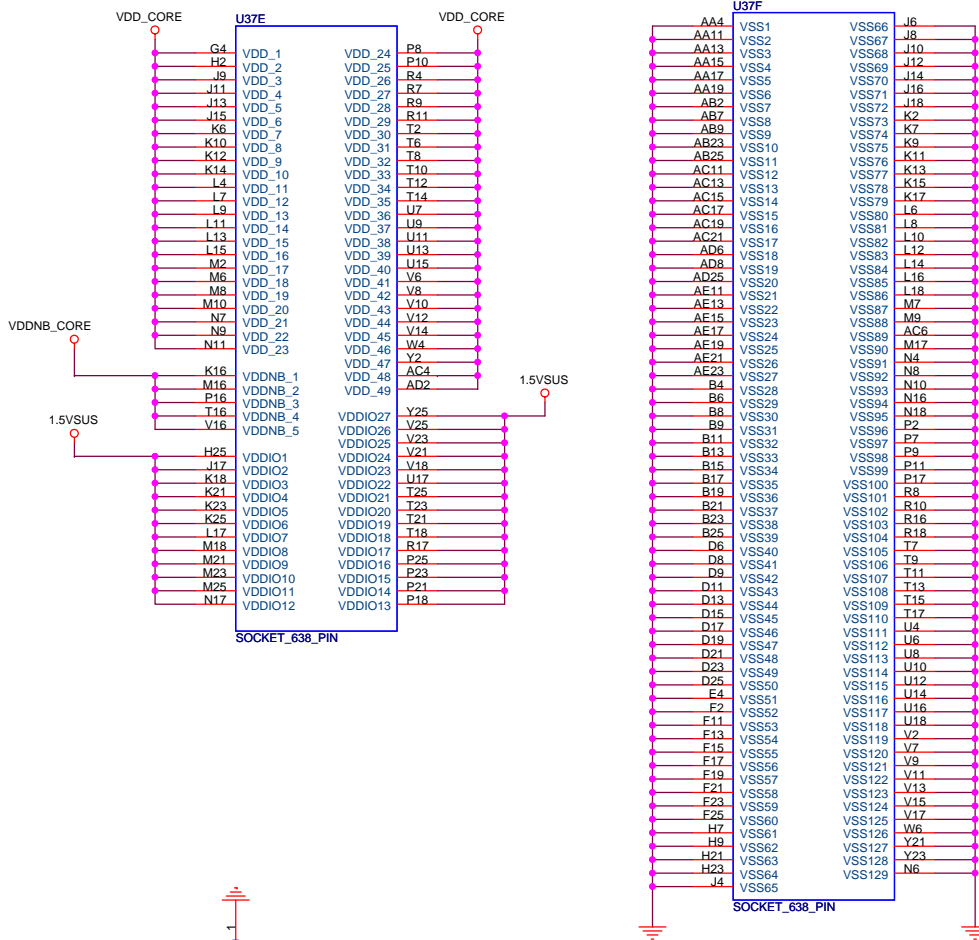
PROJECT : NE8

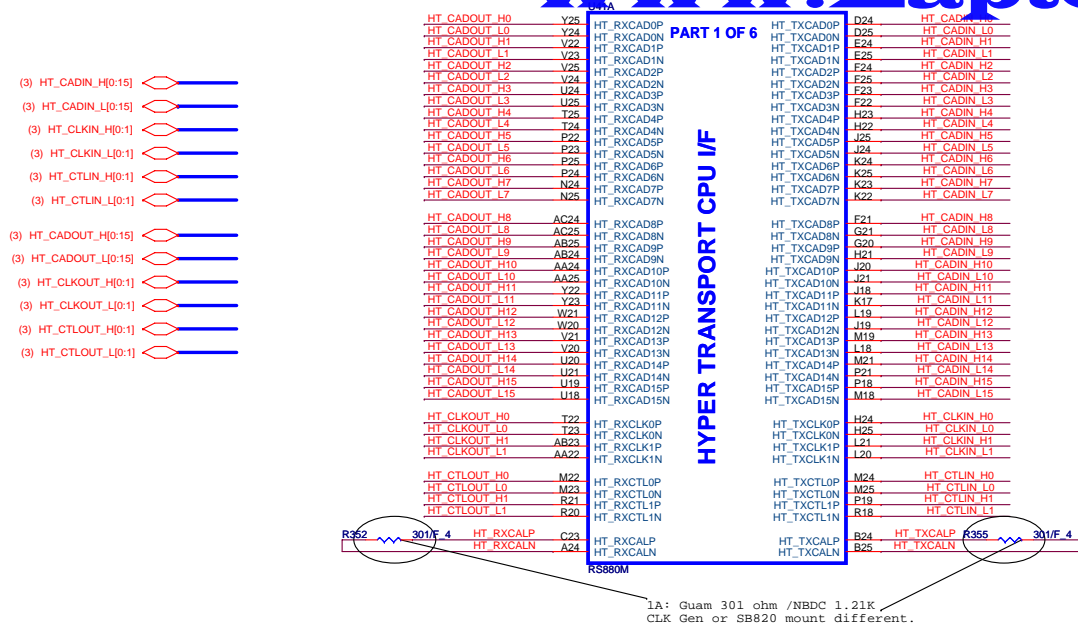
CPU MEMORY(2/3)

Size	Document Number	Rev
		2A
Date:	Wednesday, January 27, 2010	Sheet 4 of 42

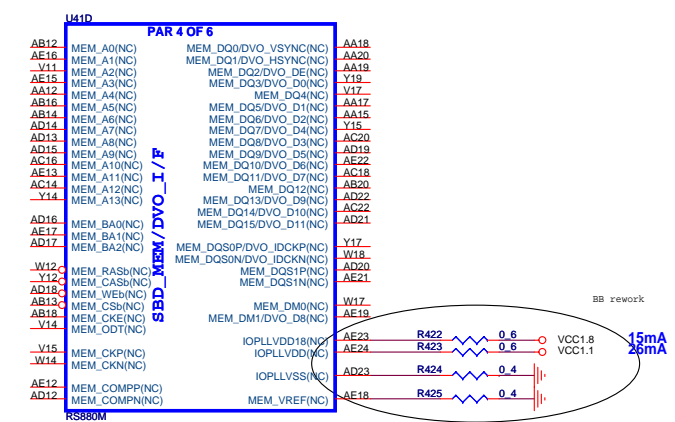
1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

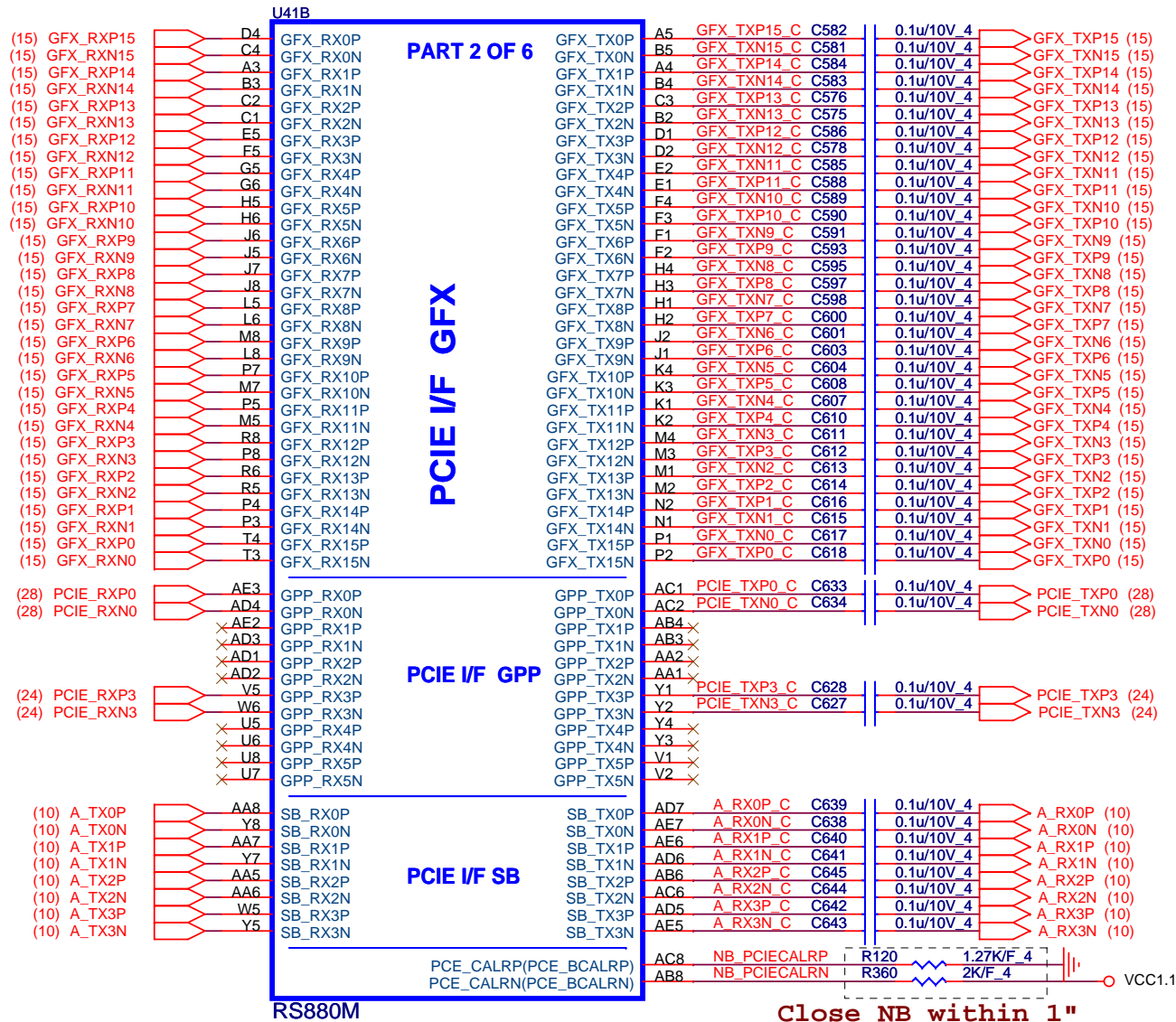
Socket Type	QCI P/N
Normal	DG0^8000018
90 degree	DG0^8000023





This block is for Side Port only , others can remove some components





Layout Swap
TX11, TX10, TX9,
TX8, TX7, TX6, TX5,
TX4, TX3, TX2, TX0

GLAN

WLAN

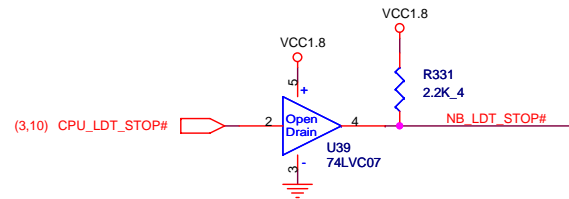
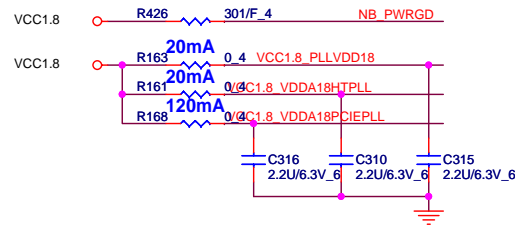
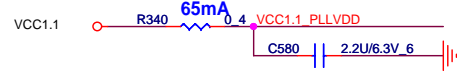
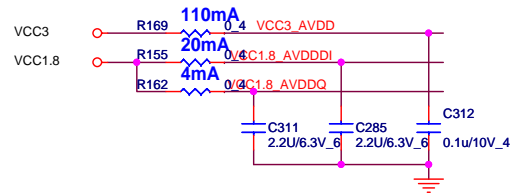


Quanta Computer Inc.

PROJECT : NE8

Size	Document Number	Rev
	RS880M GFX/PCIE(2/4)	2A
Date:	Wednesday, January 27, 2010	Sheet 7 of 42

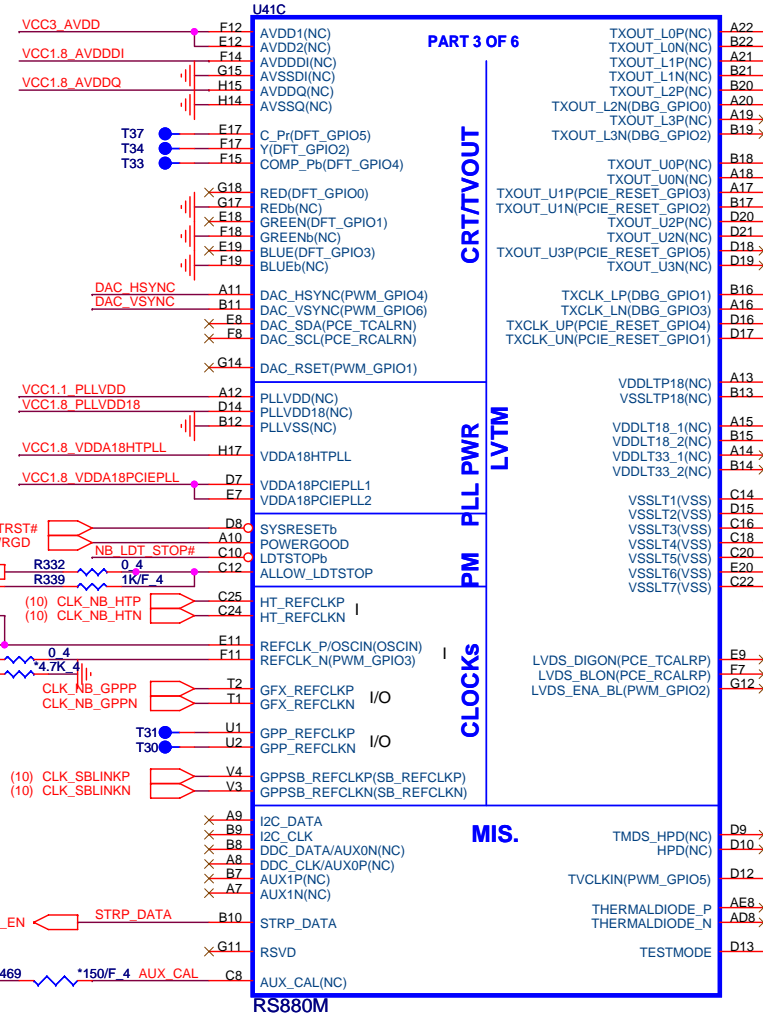
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



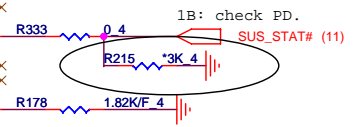
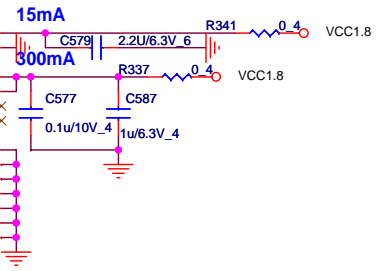
Enables Debug Bus access through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M

Discrete : Connect All, B11

Indicates if memory Side port is available or not
1: Disable side port memory
0: Enable side port memory



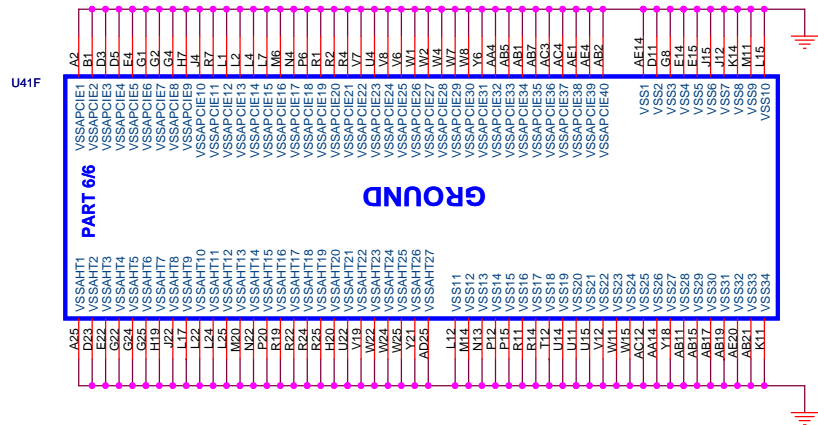
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



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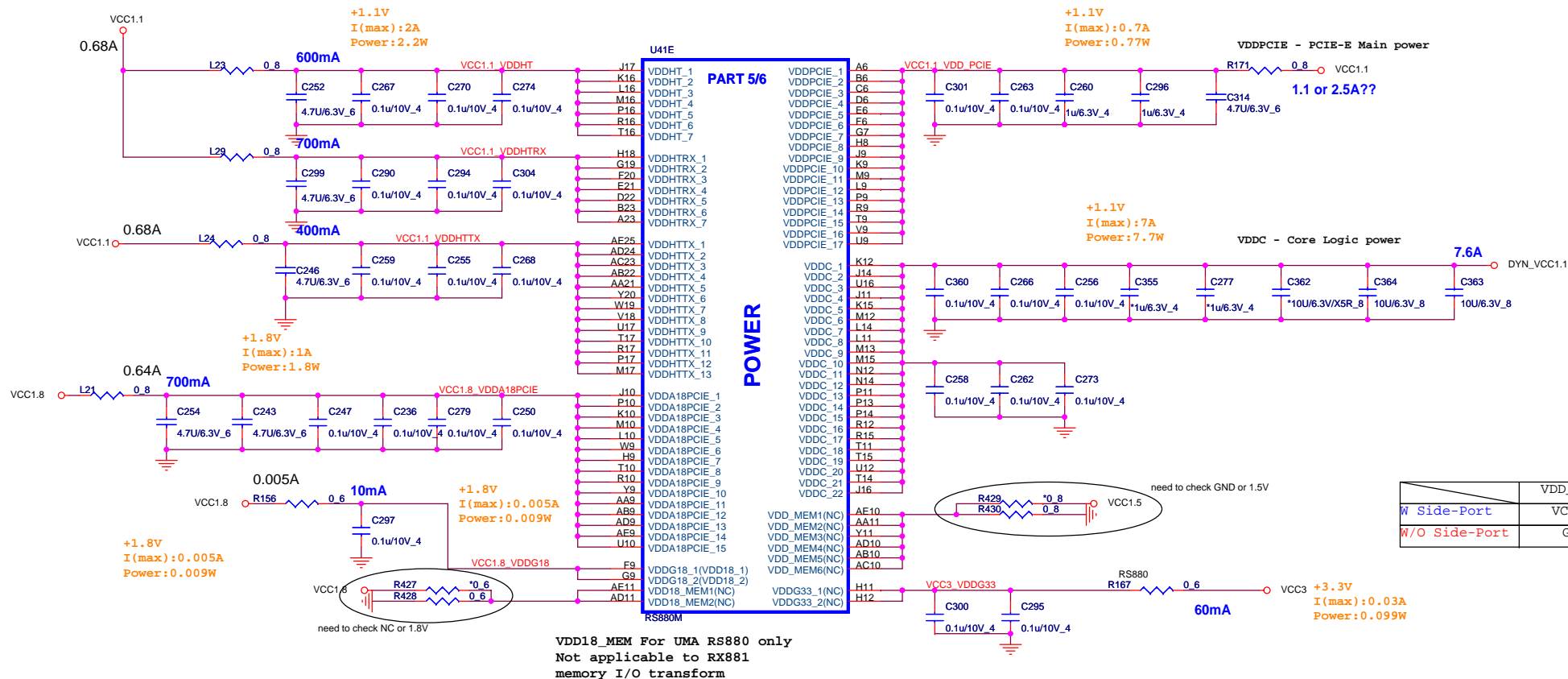
PROJECT : NE8

Size	Document Number	Rev
	RS880M SYSTEM(3/4)	2A
Date:	Wednesday, January 27, 2010	Sheet 8 of 42



RS880M/RX881 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880M	PIN NAME	RX881	RS880M
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.1V	+1.1V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL18	NC	NC



	VDD18_MEM
W Side-Port	VCC1.8
W/O Side-Port	GND

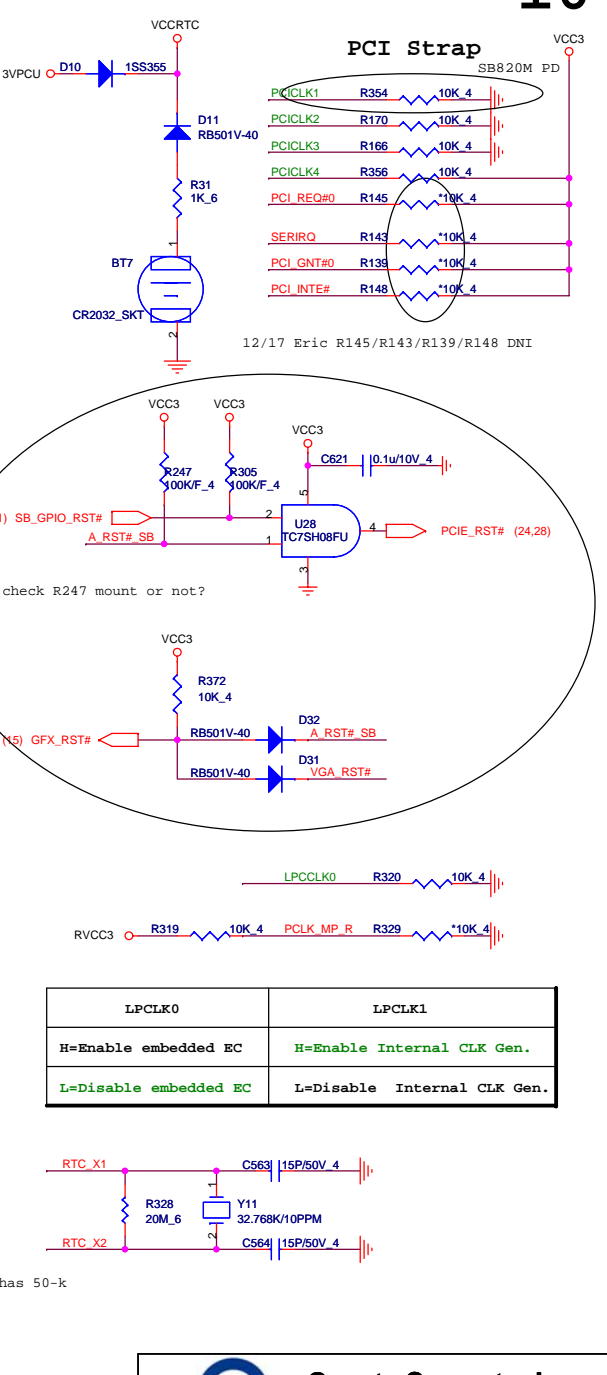
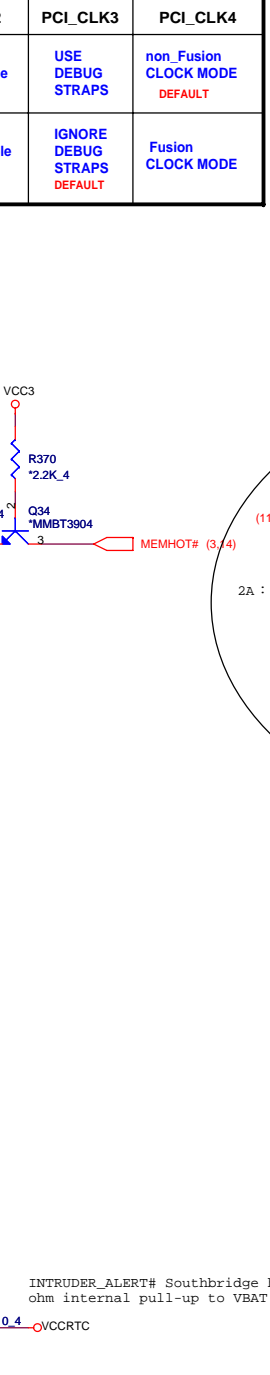
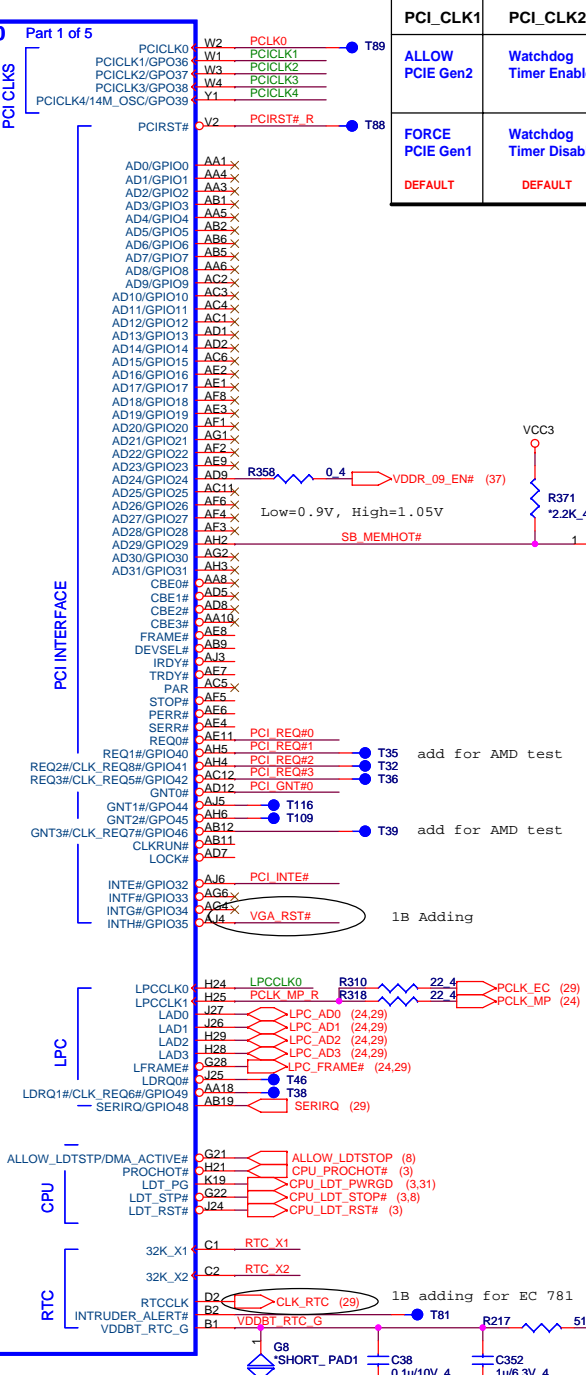
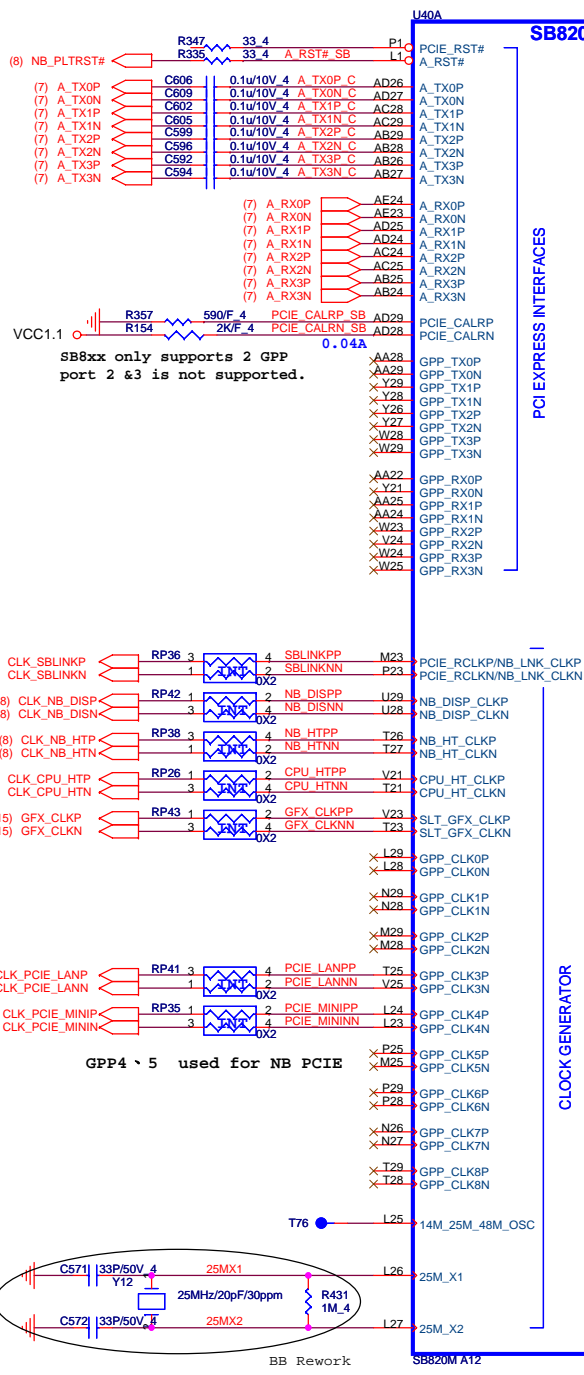
VDD18_MEM For UMA RS880 only
Not applicable to RX881
memory I/O transform

	VDD_MEM
W Side-Port	VCC1.5
W/O Side-Port	GND

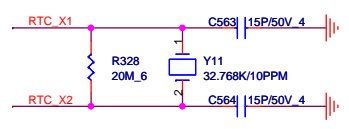


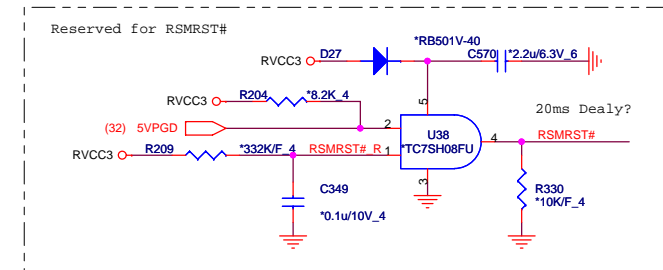
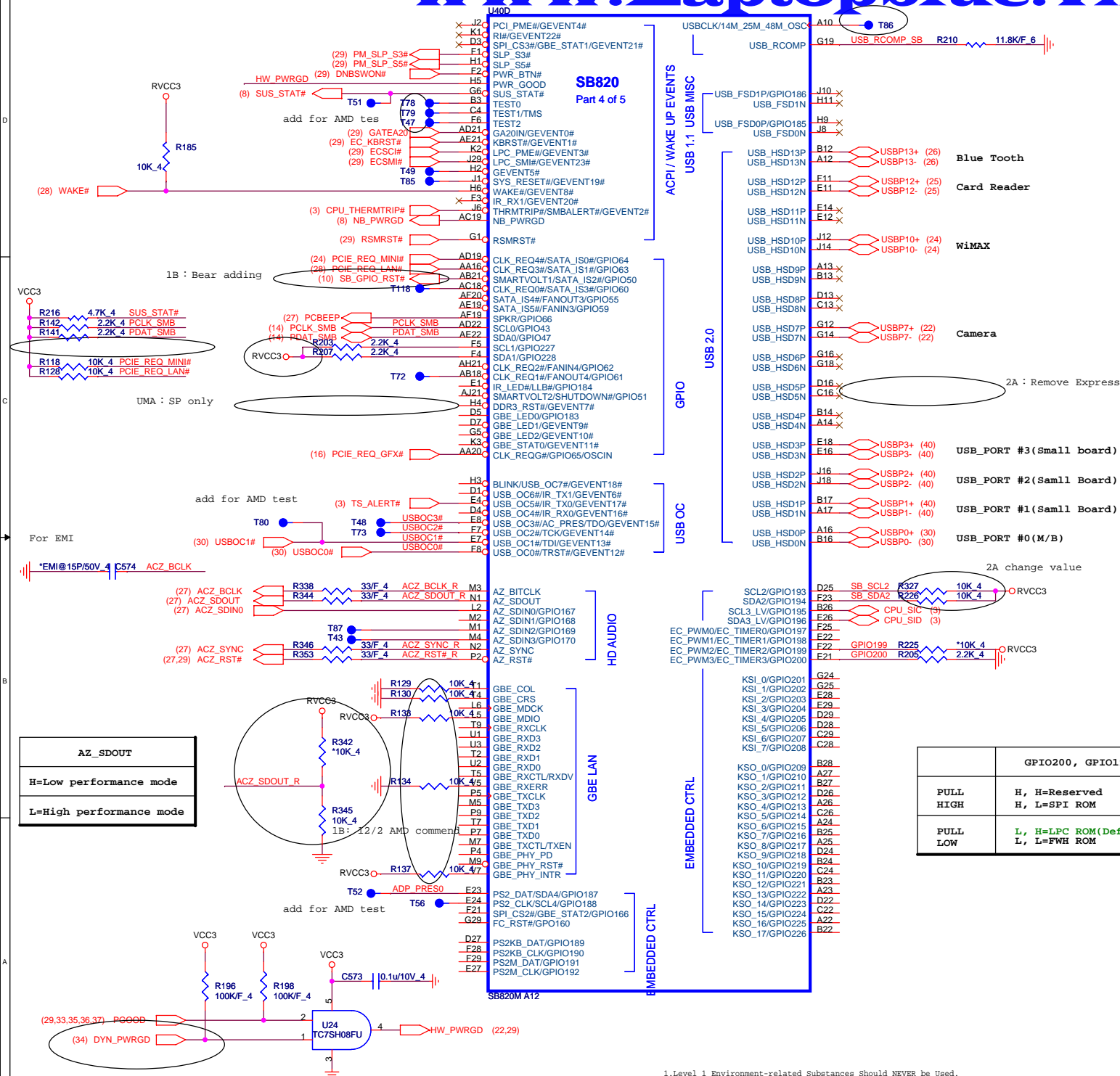
Quanta Computer Inc.
PROJECT : NE8

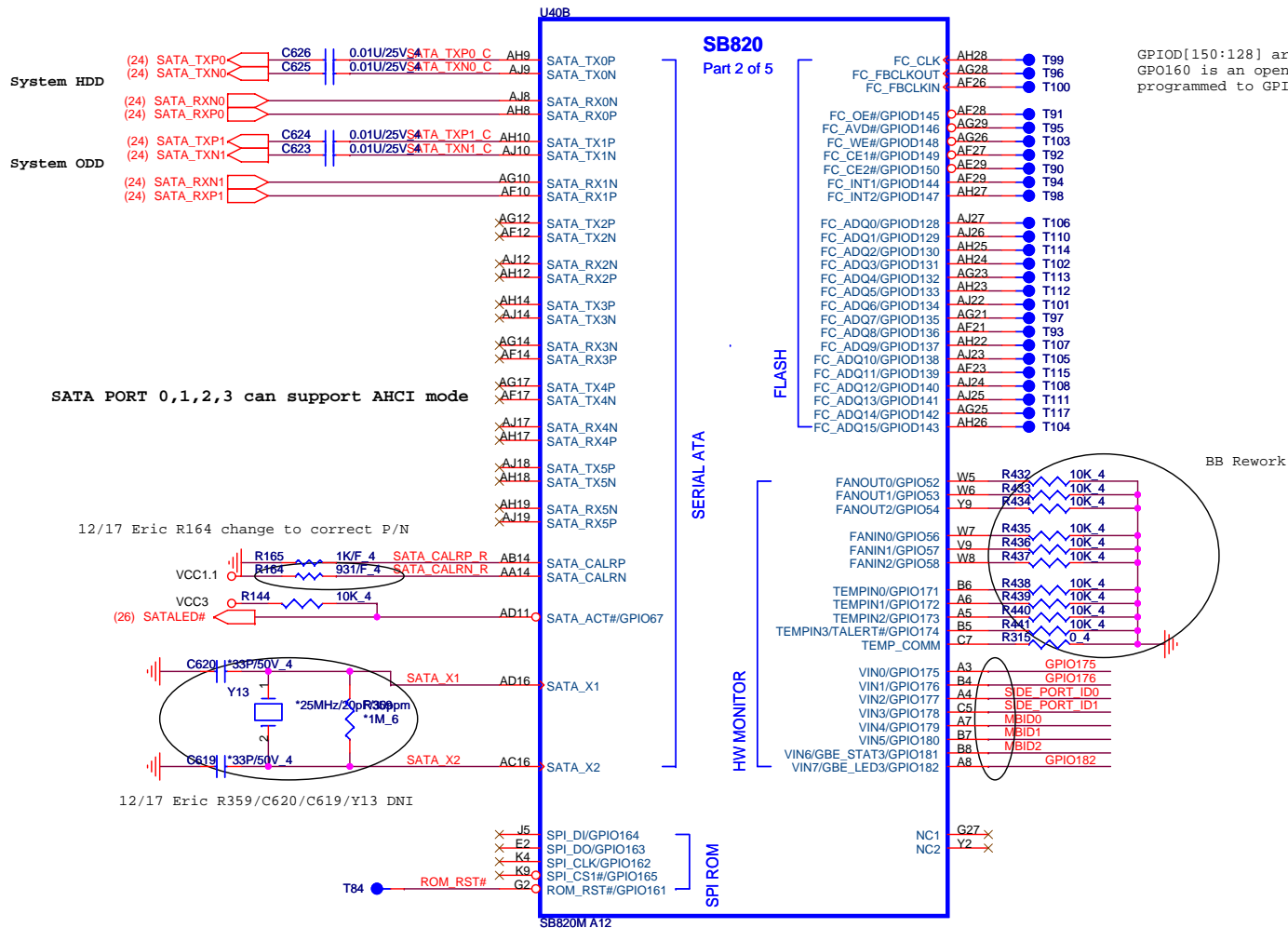
Size	Document Number	Rev
		2A
RS880M POWER(4/4)		
Date	Wednesday, January 27, 2010	Sheet 9 of 42



LPCLK0	LPCLK1
H=Enable embedded EC	H=Enable Internal CLK Gen.
L=Disable embedded EC	L=Disable Internal CLK Gen.



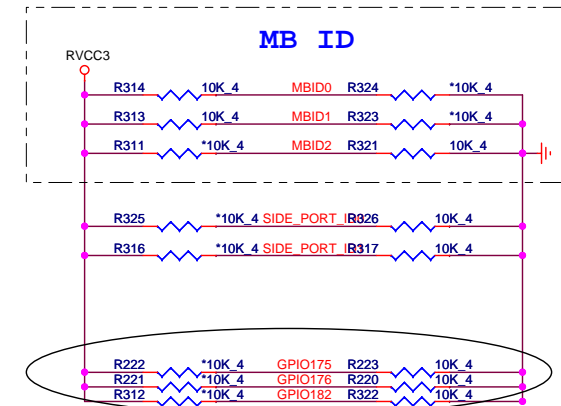




GPIO[150:128] are open drain GPIO pins where as GP0160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

ID2	ID1	ID0	
0	0	0	Danube UMA
0	0	1	Danube UMA+Side port
0	1	0	Danube+Park XT
0	1	1	Danube+Madison LP
1	0	0	Danube+M92 XTX
1	0	1	
1	1	0	
1	1	1	

	NON	SAMSUNG	HYNIX	
SP ID0	0	1	0	1
SP ID1	0	0	1	1



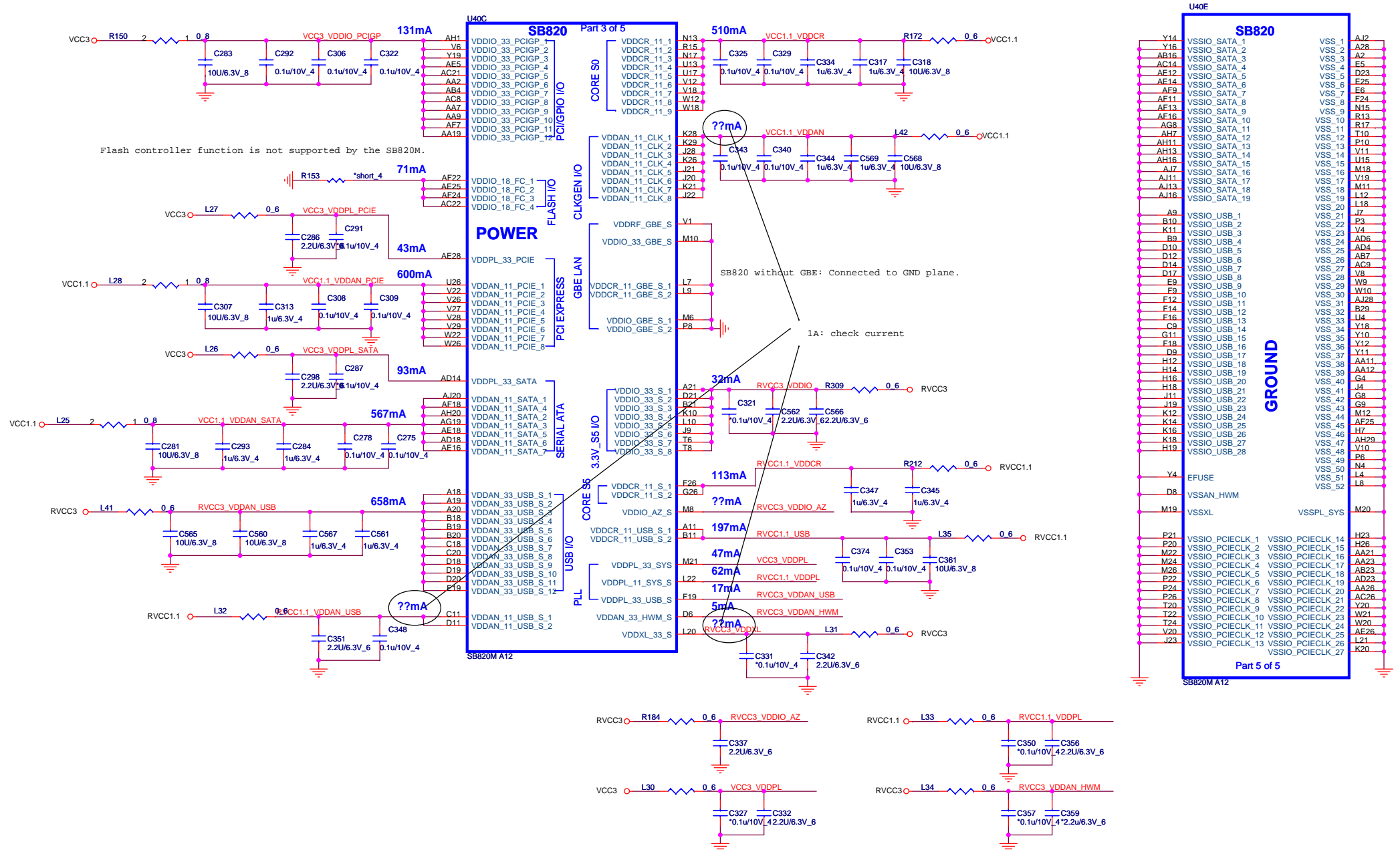
- 1.Level 1 Environment-related Substances should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

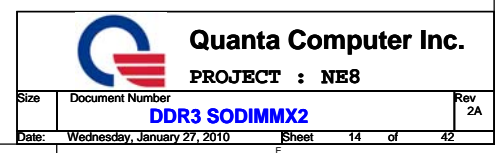


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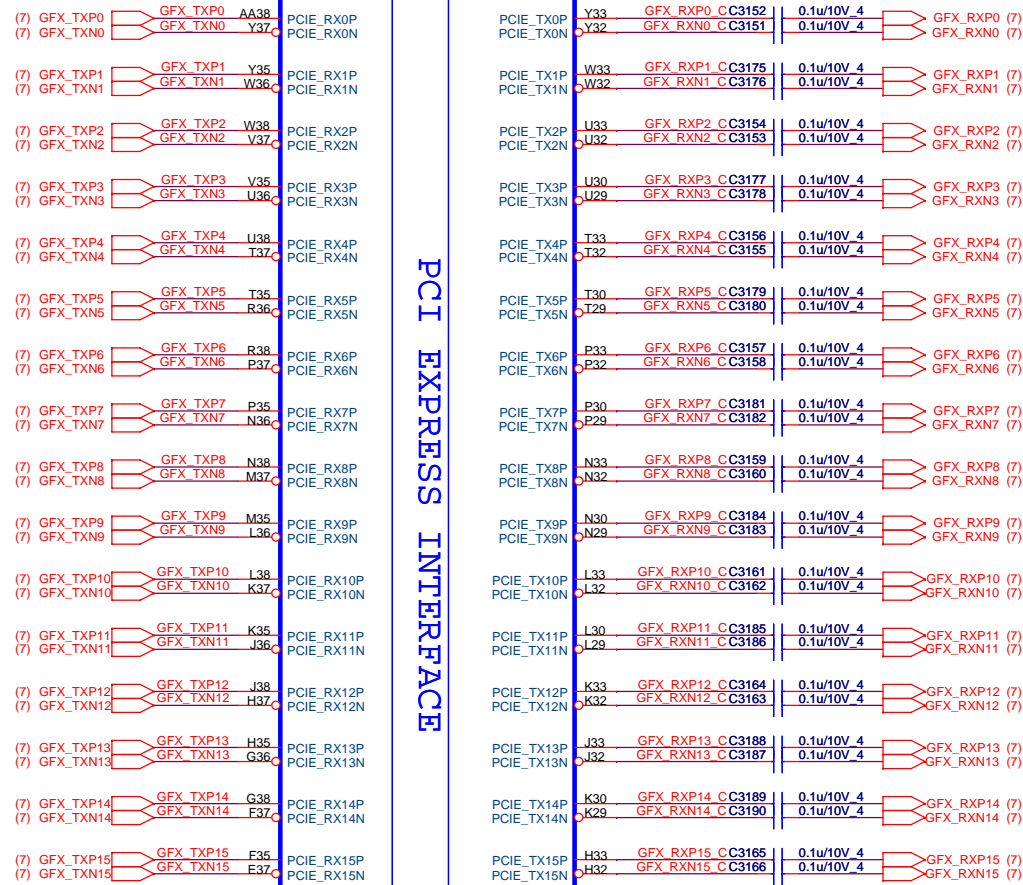
PROJECT : NE8

Size	Document Number	Rev
	SB820 SATA(2/4)	2A
Date:	Wednesday, January 27, 2010	Sheet 12 of 42

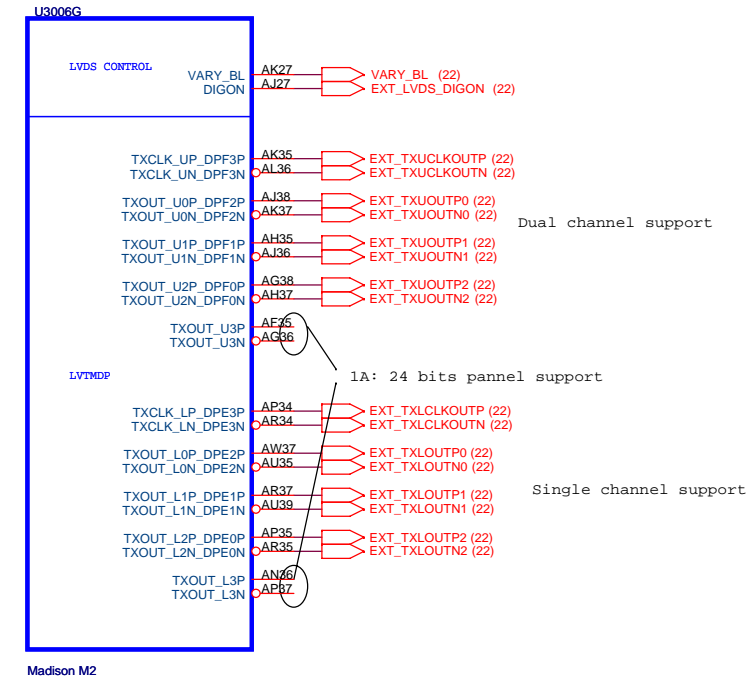




1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



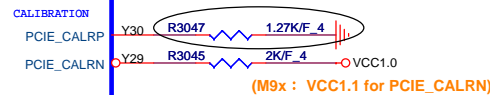
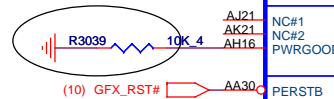
PCI EXPRESS INTERFACE



Dual channel support

Single channel support

M9x : R3039 -> NC



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PROJECT : NE8

Size	Document Number	Rev
	ATI PCIE/LVDS	2A
Date:	Wednesday, January 27, 2010	Sheet 15 of 42

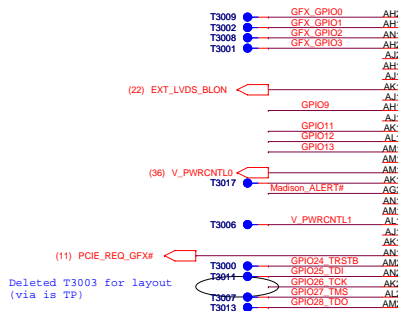
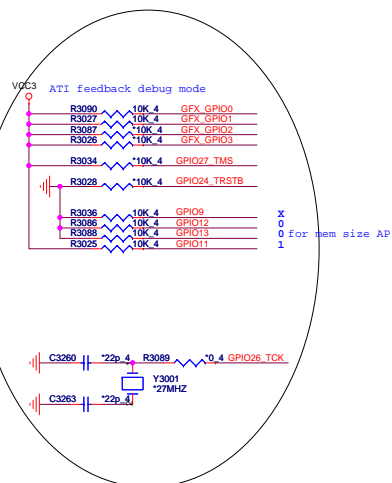
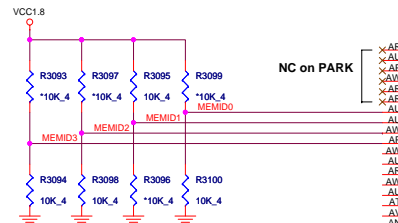
AKD5LZGTW00
AKD5LGGT502
AKD5LGGT701

Samsung 64*16-900MHZ K4W1G1646E-HC11

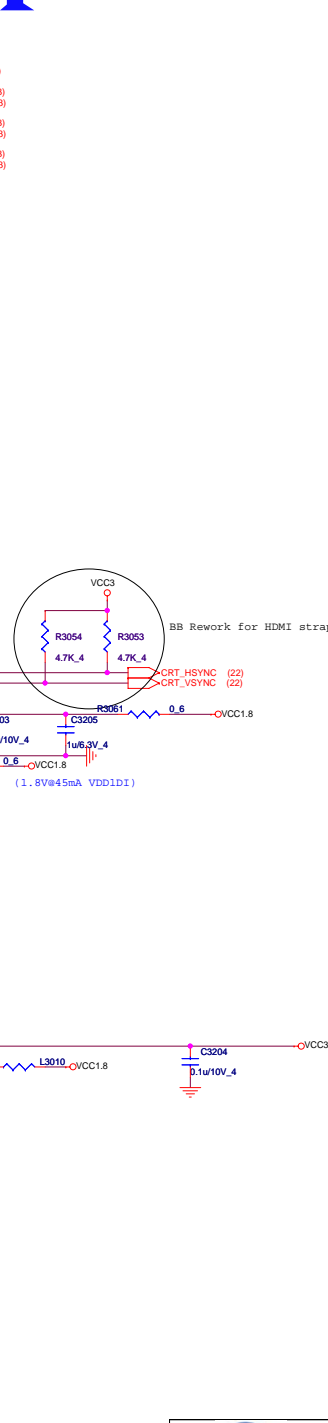
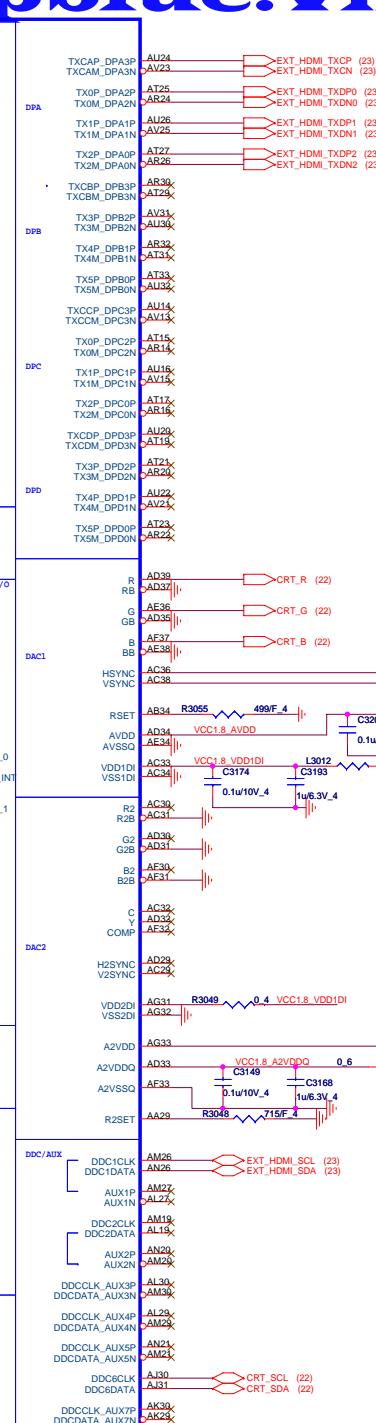
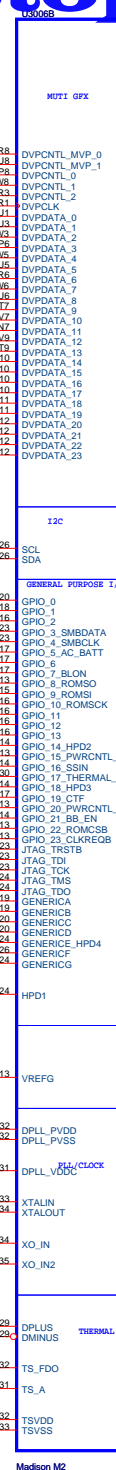
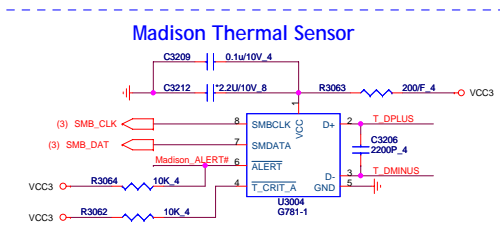
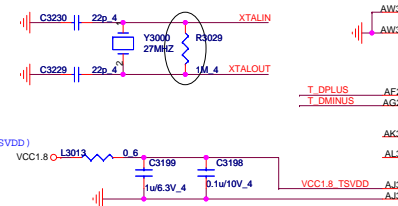
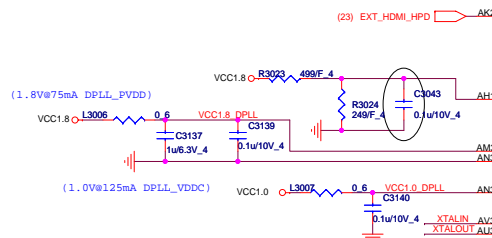
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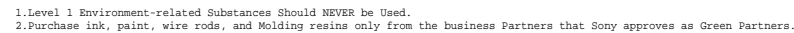
GPIO0 : PCIE FULL TX OUTPUT SWING
GPIO1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO2 : BIF_GEN2_EN_A
GPIO8 : RESERVED
GPIO9 : VGA ENABLED
GPIO[13:11] : SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT
V2SYNC : IGNORE VIP DEVICE STRAPS
HS2SYNC : 0
GENERIC# : 0
HSYNC : 1 (AUDIO FOR BOTH DP AND HDMI)
VSYNC : 1 (AUDIO FOR BOTH DP AND HDMI)


```



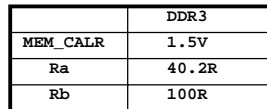
Deleted T3003 for layout
(via is TP)





 <div> Quanta Computer Inc. PROJECT : NE8 </div>		
Size	Document Number	Rev
	ATI MEM/IF/DP	2A
Date:	Wednesday, January 27, 2010	Sheet 18 of 42

**Park Use Channel B
Memory Interface Only**



```
route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DN
```

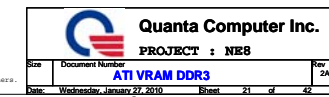


TI MEM IF

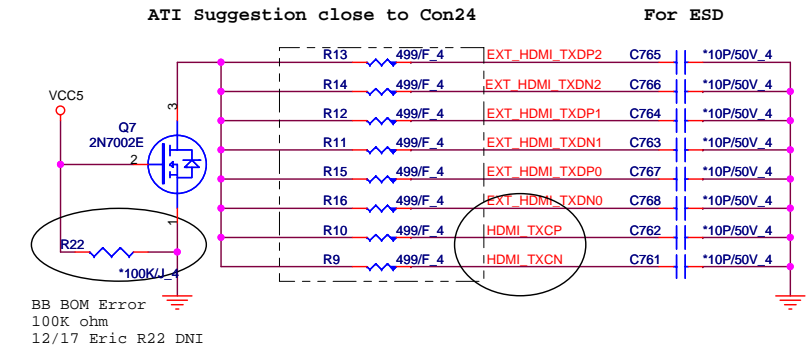
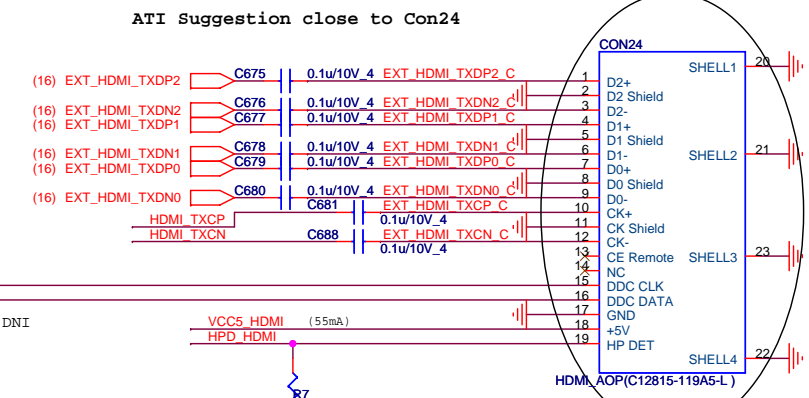
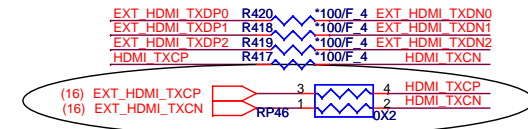
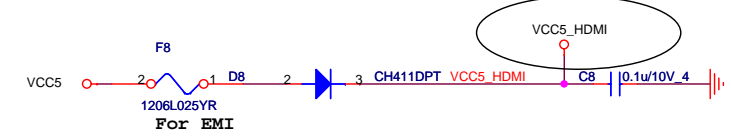
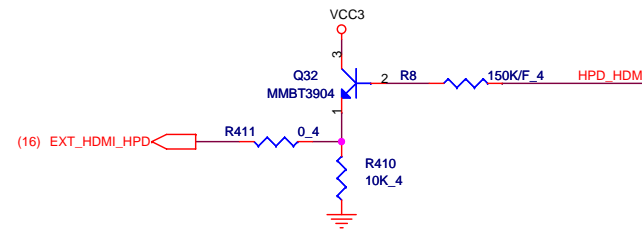
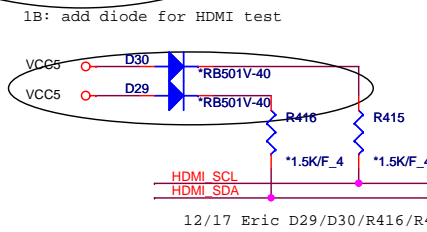
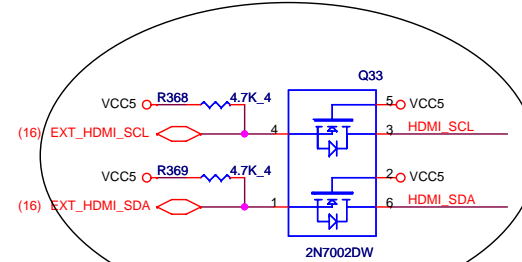
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Use this option ONLY
for Park-S3

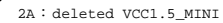
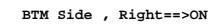
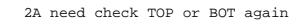
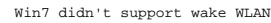




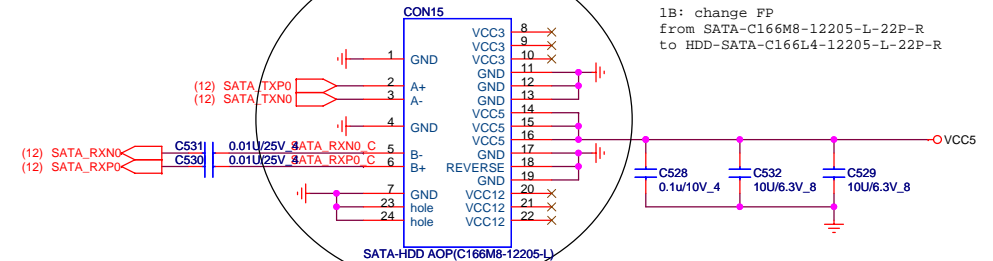


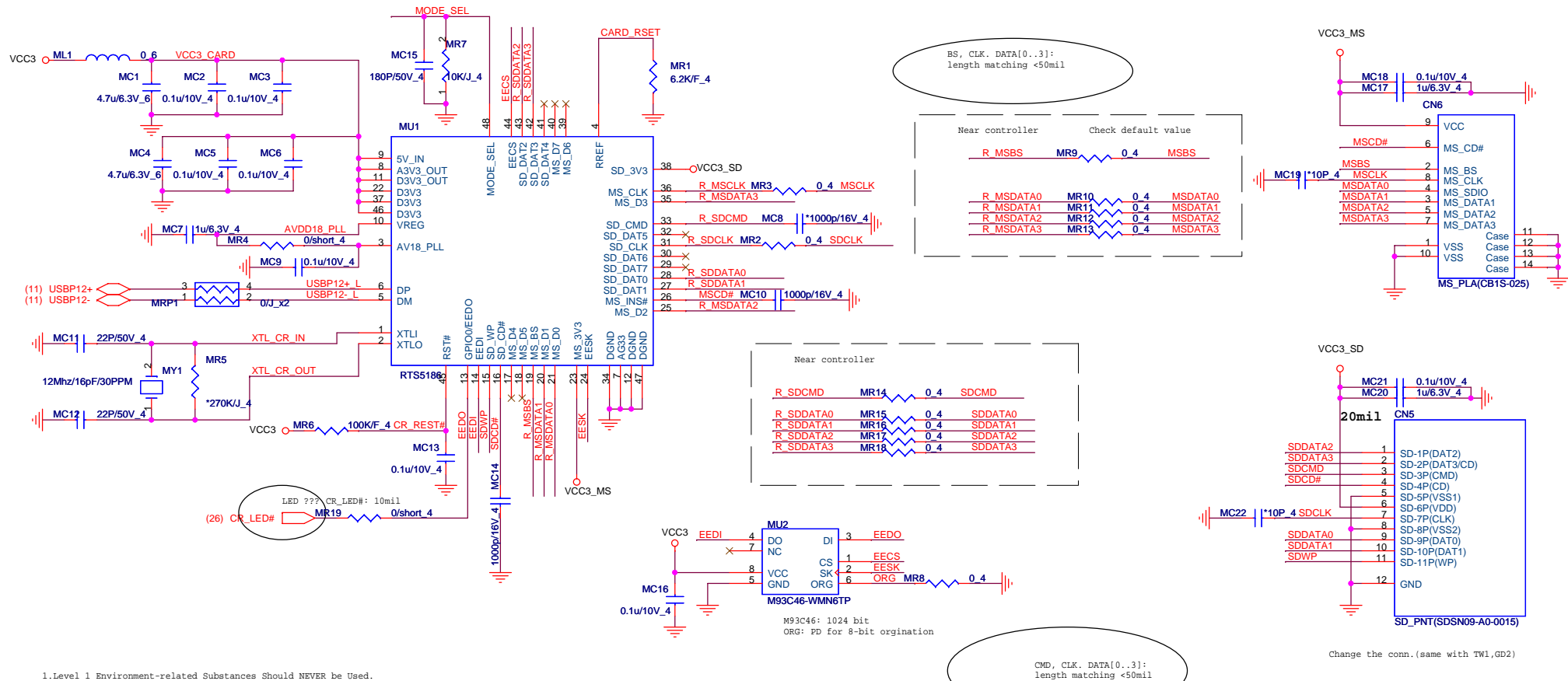


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```
1B: change FP
from SATA-C166M8-12205-L-22P-R
to HDD-SATA-C166L4-12205-L-22P-R
```



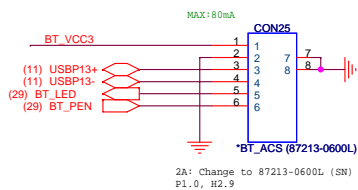
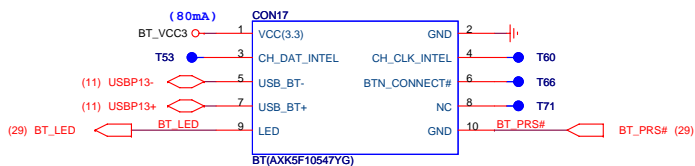
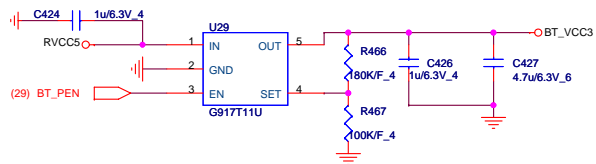


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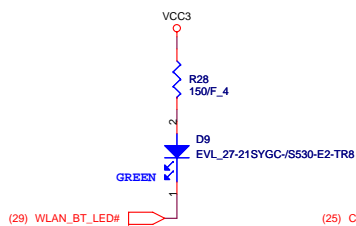
2A: Remove Express card

Bluetooth

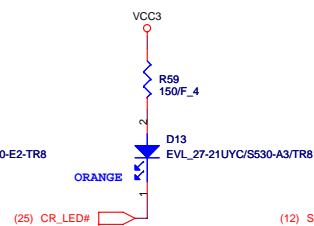


020M--BC2070 (wire)
1. 3.3V
2. GND
3. USB D+
4. USB D-
5. BT_LED
6. BT_ON

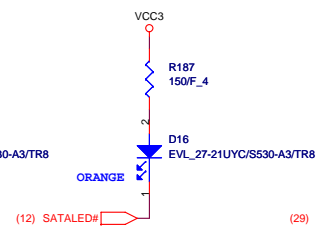
RF LED



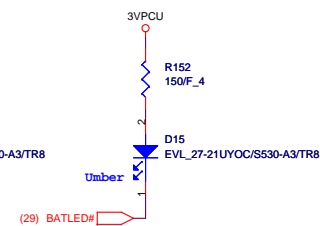
Card LED

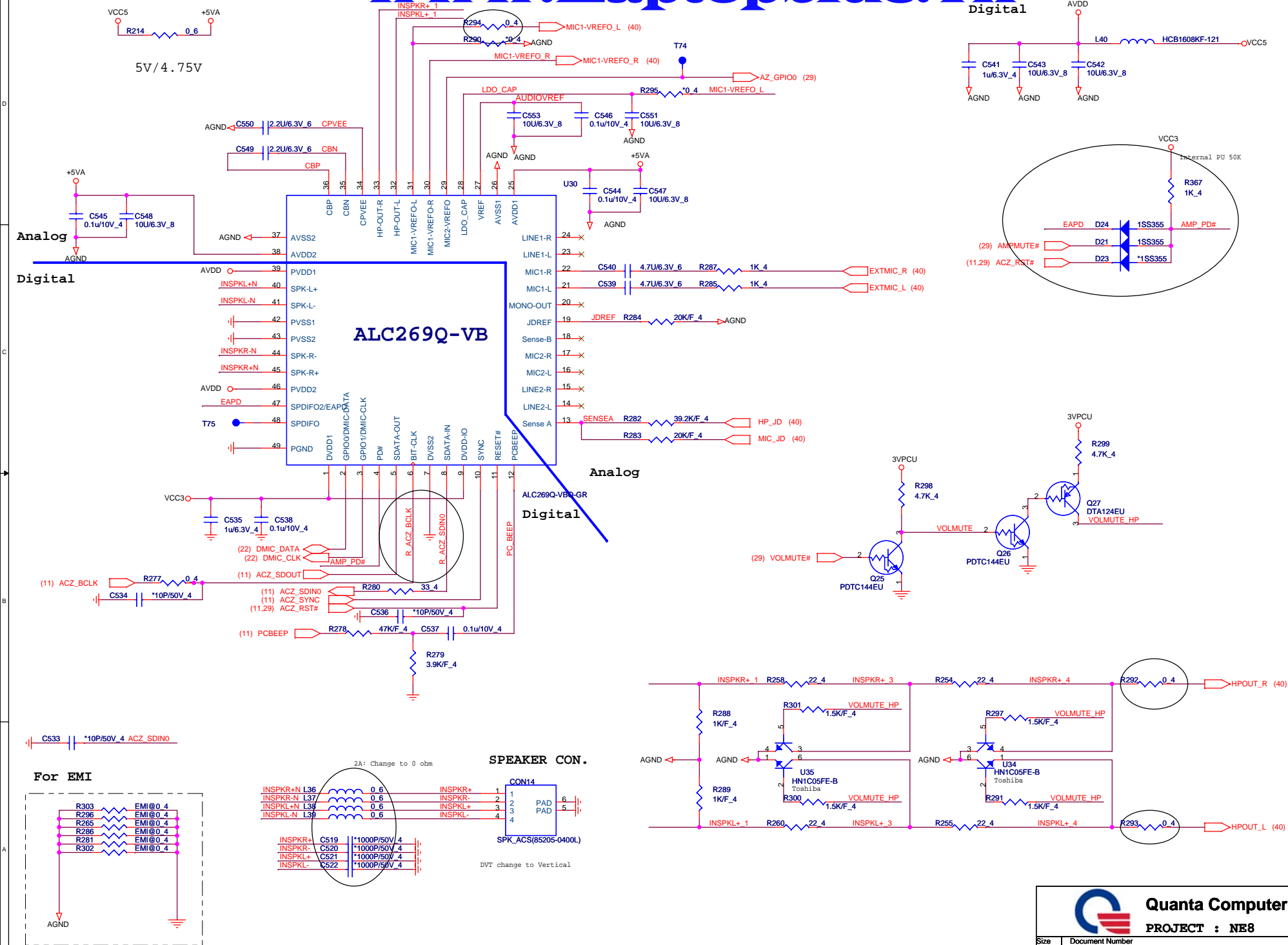


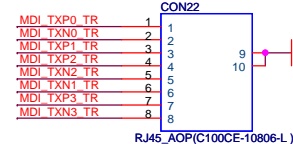
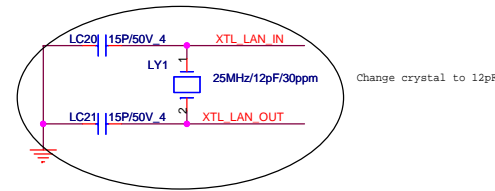
HDD LED



Battery LED



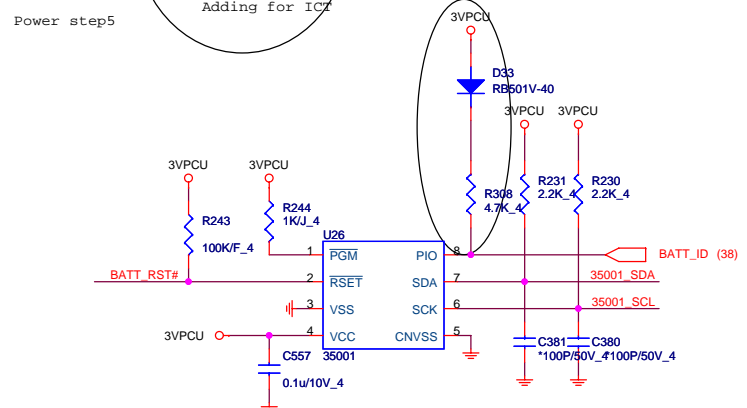
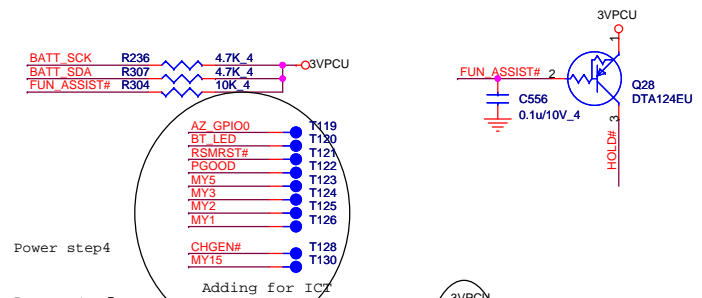
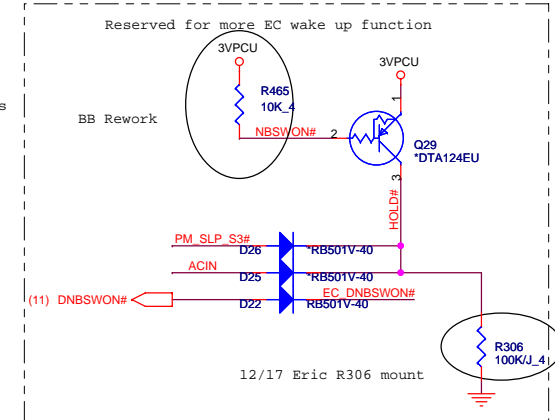




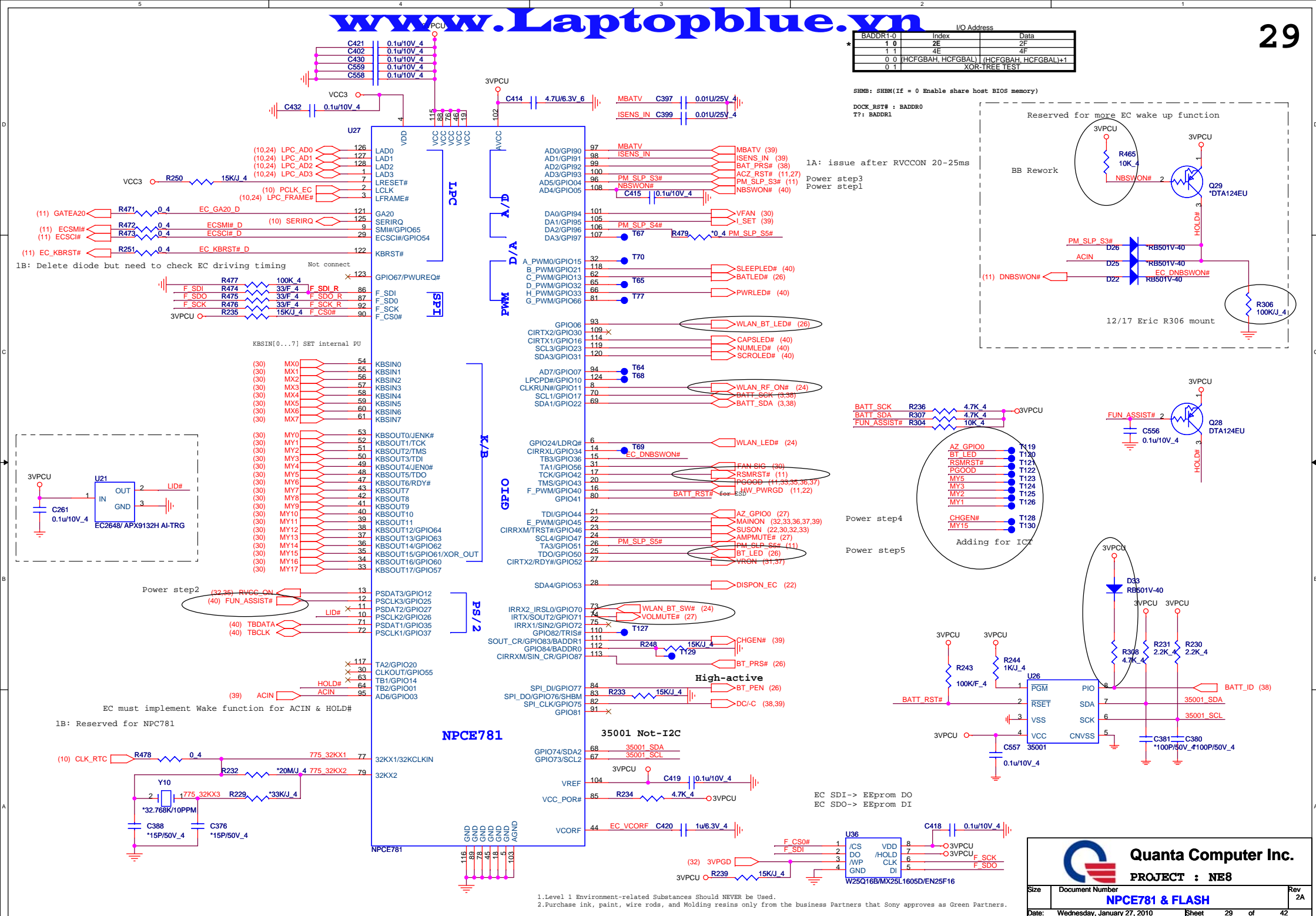
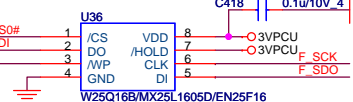
I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+
0 1	XOR-TREE TEST	

SHMB: SHBM(If = 0 Enable share host BIOS memory)

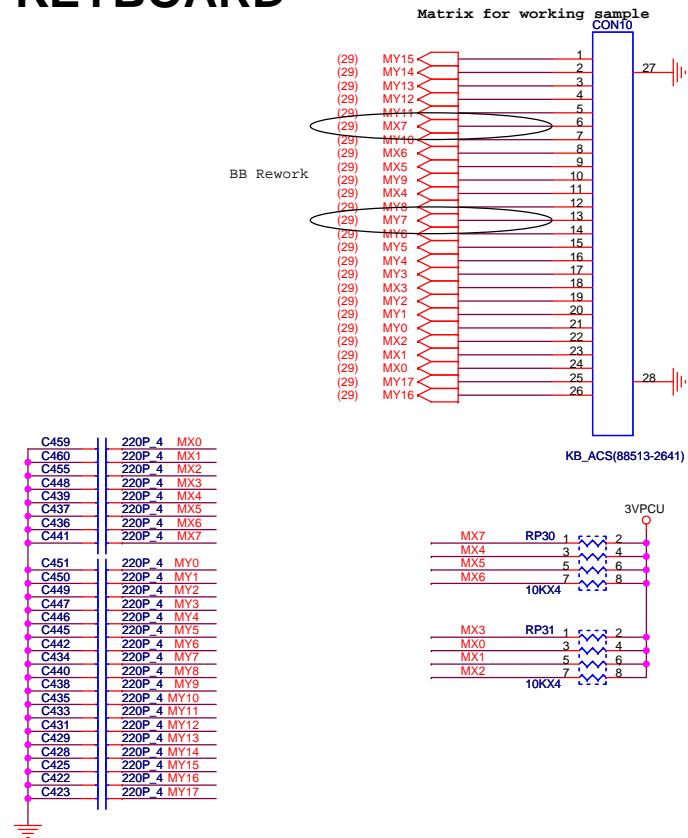
```
DOCK_RST# : BADDR0
T?: BADDR1
```



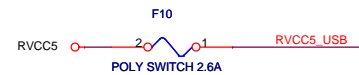
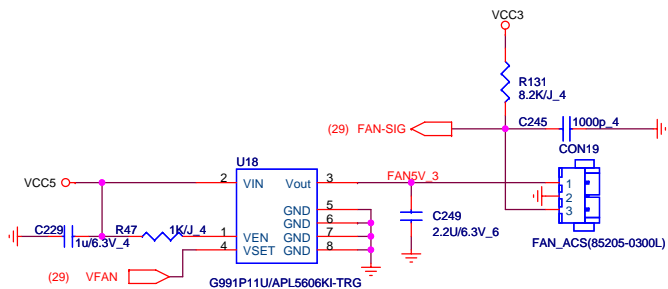
```
EC SDI-> EEprom DC
EC SDO-> EEprom DI
```



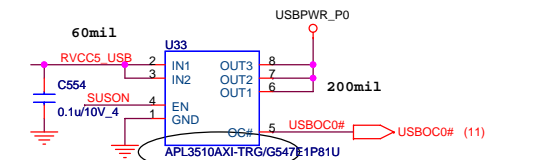
KEYBOARD



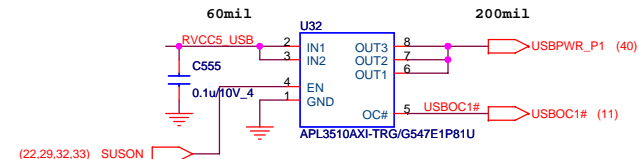
FAN



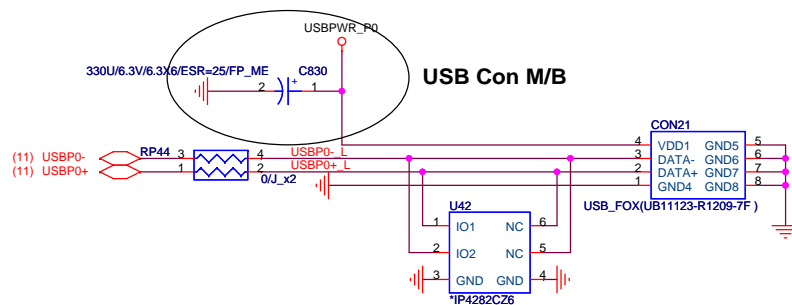
Current limit need to check



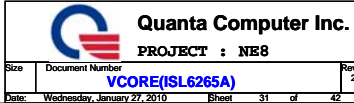
Current limit = ~1.5A
(For port0 and Camera)



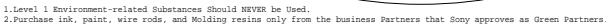
Current limit = ~3A



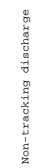
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



3.0A 6



1.2A



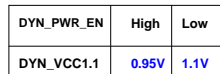
MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

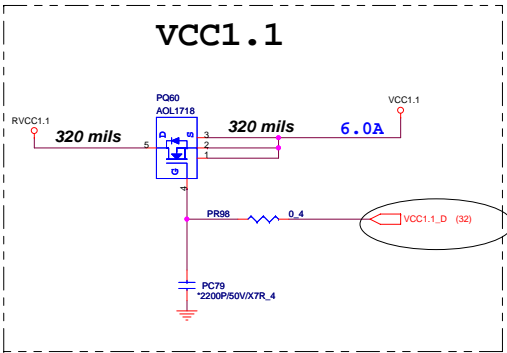
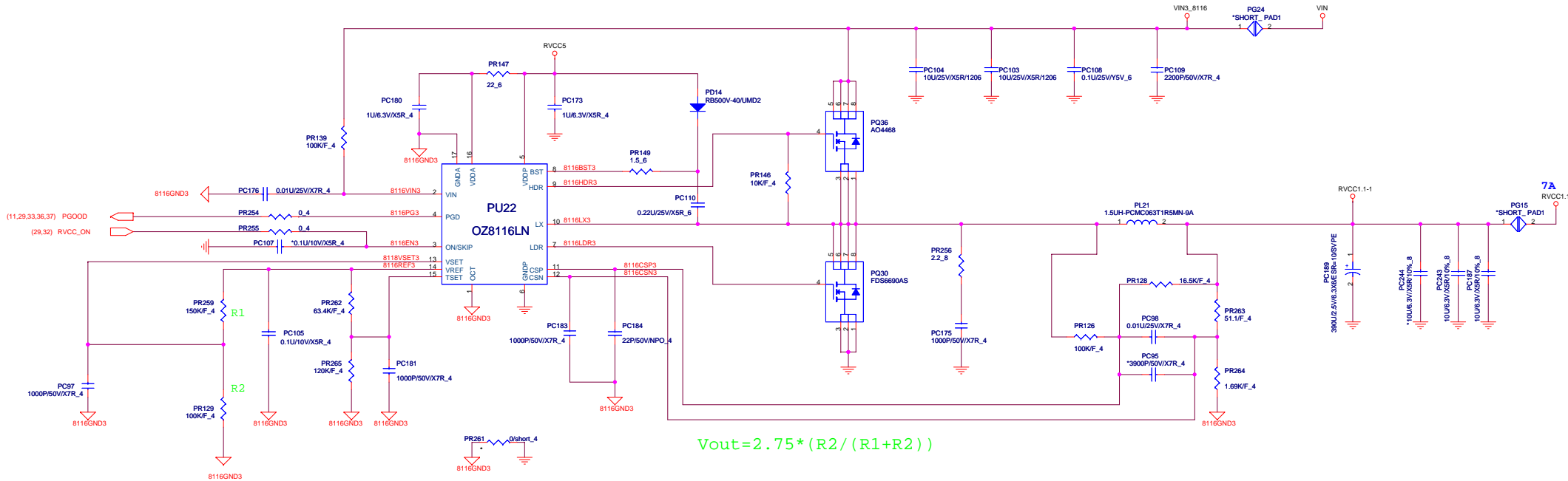
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.75V$$

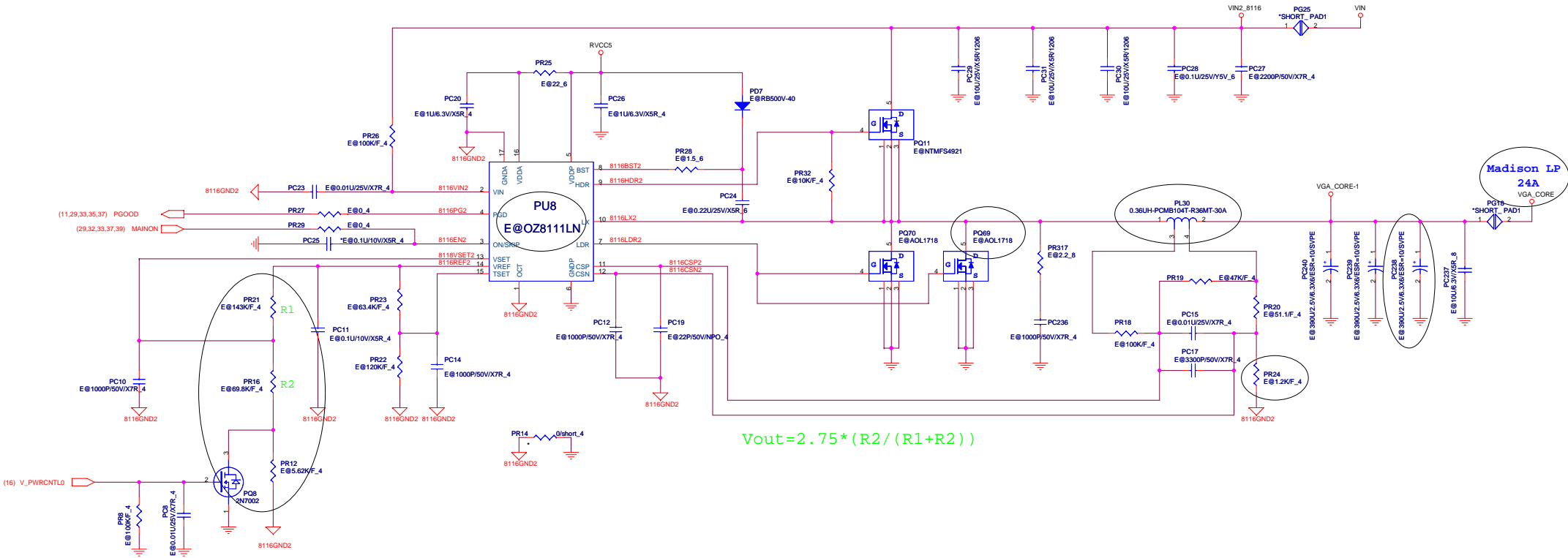
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

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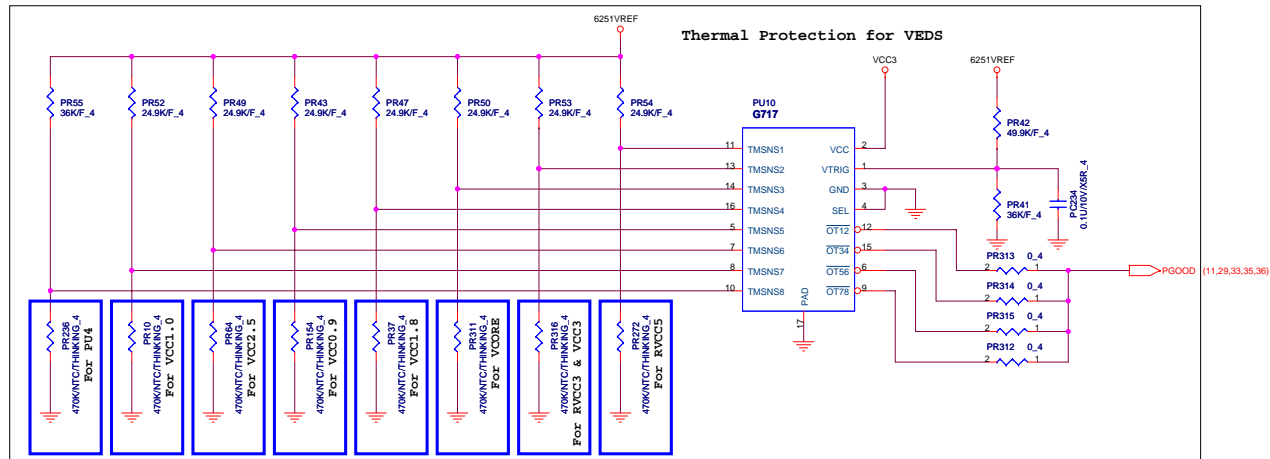
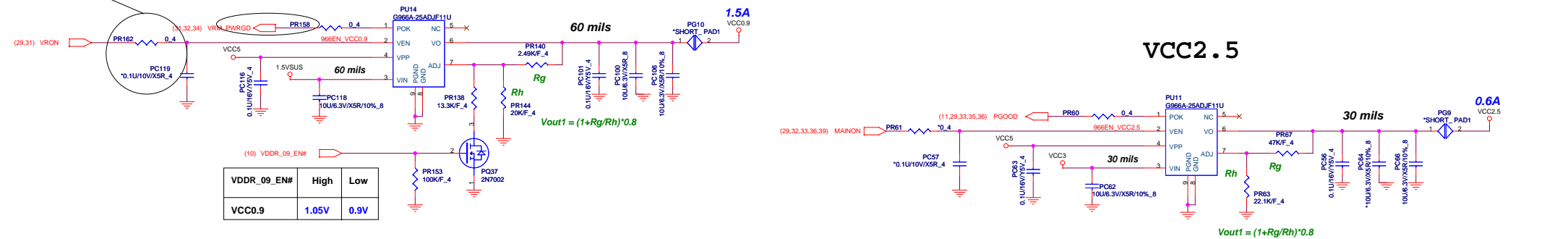
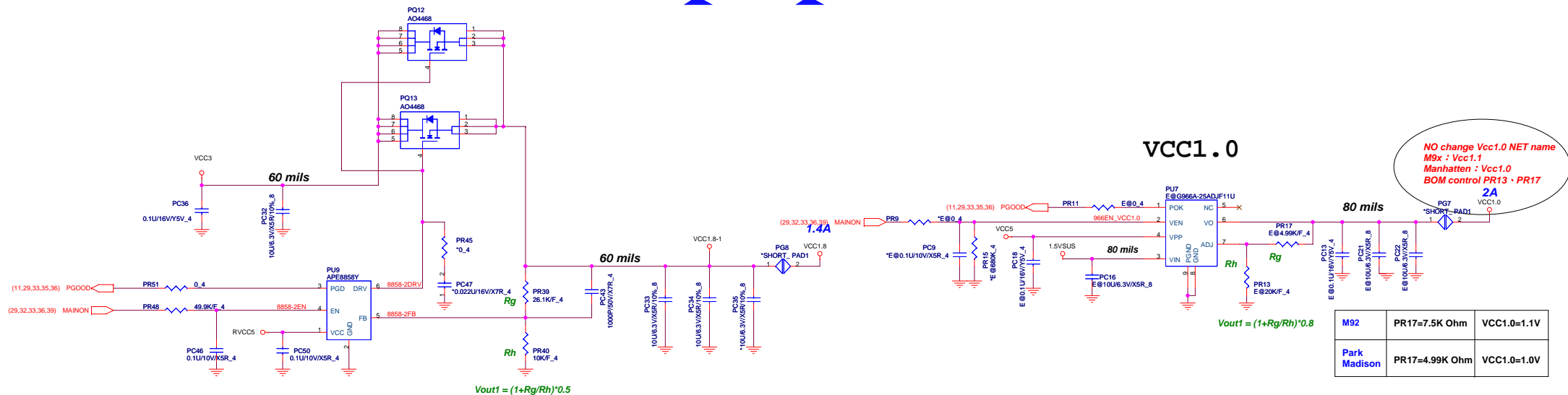


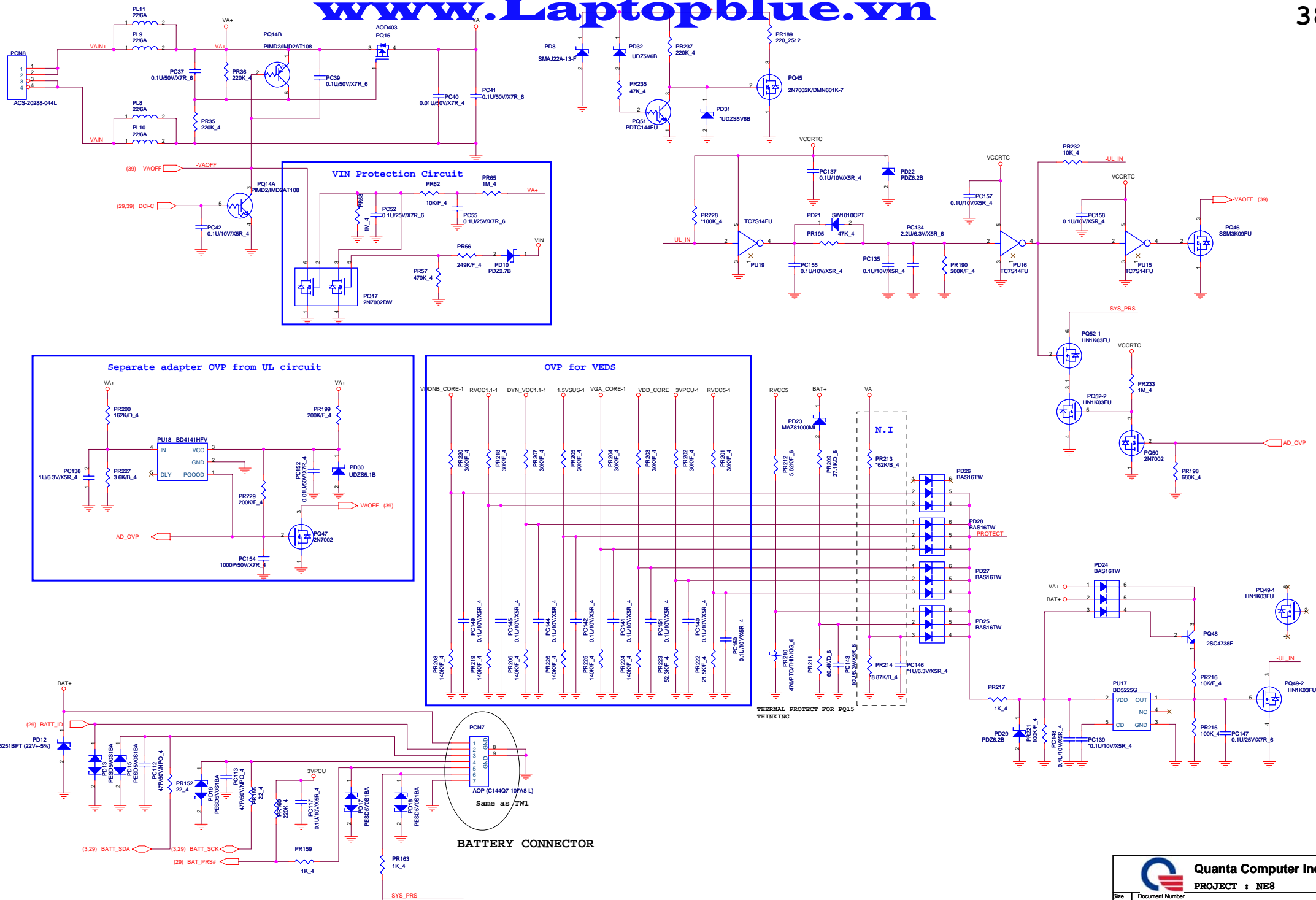
Madison LP

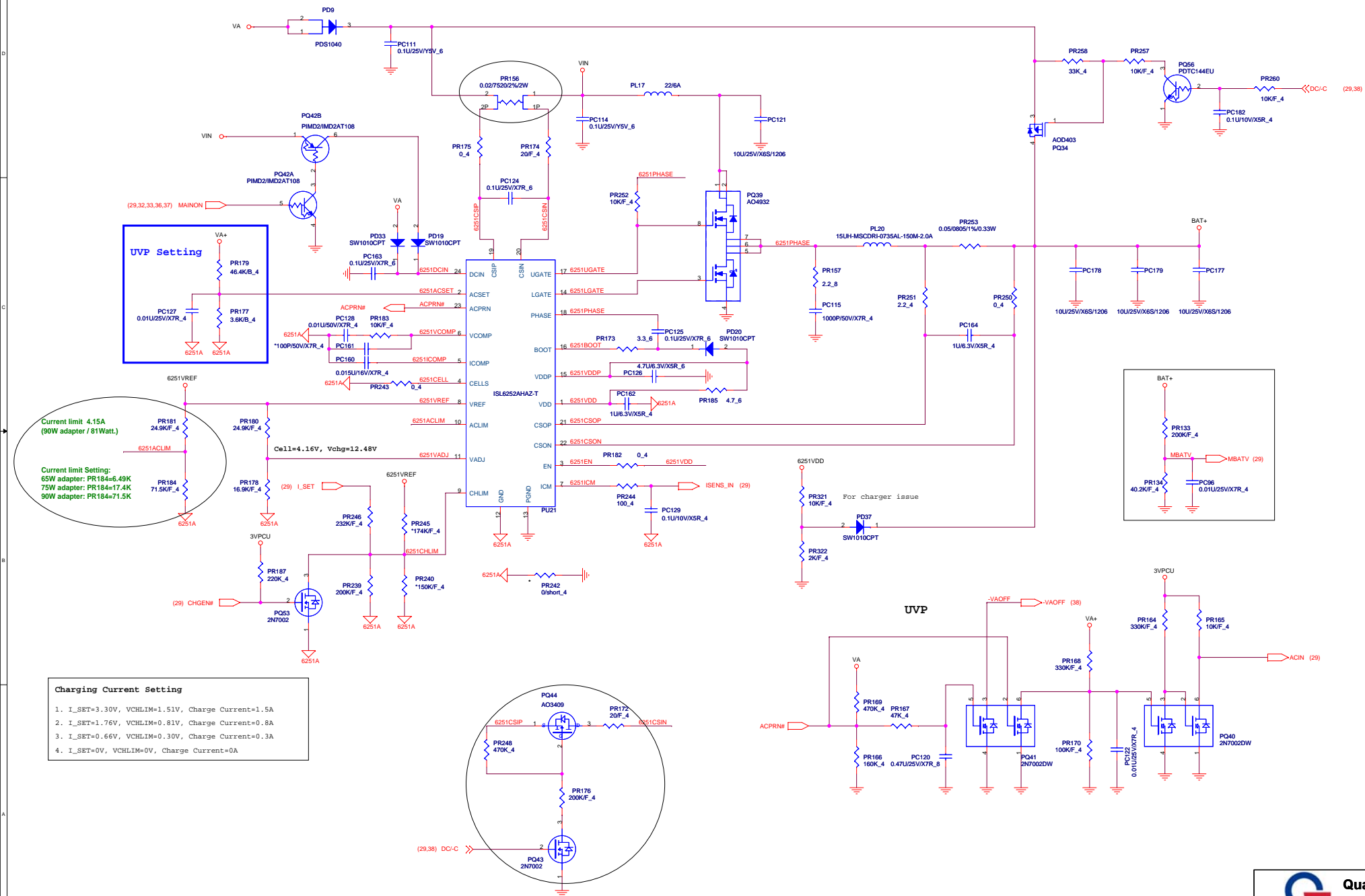
External VGA_CORE Voltage Setting:

V_PWRCNTL0	VGA_CORE
0	0.95V
1	0.90V

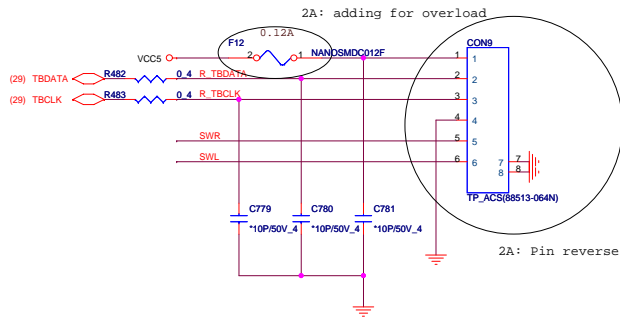
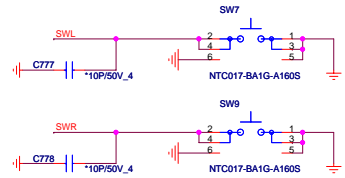
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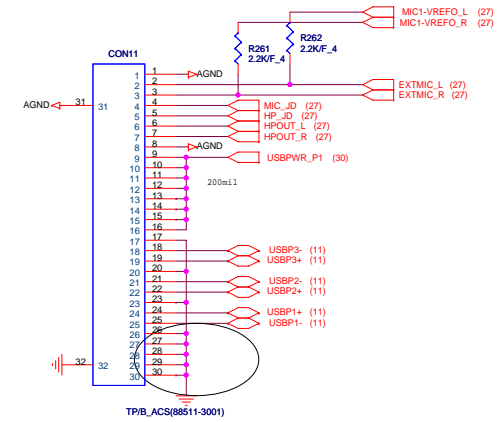
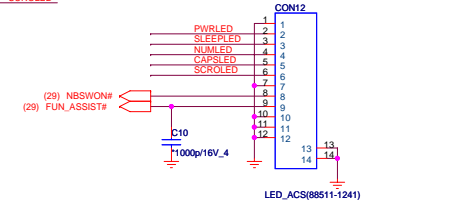
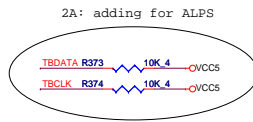




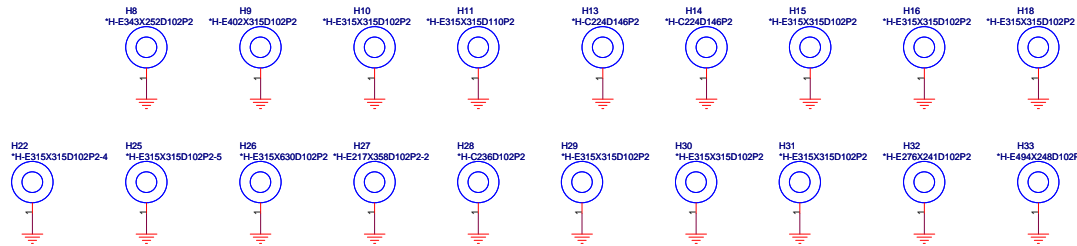
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2A: Pin reverse

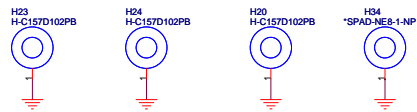


2A: change CON11 form 26pin to 30pin.



WLAN

BT



Power on Sequence required:

SB800:
 1, +3.3VDUAL ramp before +1.1VDUAL
 2, +3.3V ramp before +1.8v
 3, +1.8V ramp before +1.1v
 4, +3.3v ramp before +1.1v
 5, +3.3VALW_R ramping down time > 300us
 6, 50uS <= All power rails except +3.3VALW_R <= 40mS
 7, 100uS <= +3.3VALW_R <= 40mS

RS880:
 1, 0 <(+3.3V) - (+1.8v) < 2.1
 2, +1.8V ramp before +1.1v
 3, +1.1V ramp before VCC_NB

CPU_LDT_RST#
 (SB TO CPU)

CPU_LDT_PWRGD
 (SB TO CPU)

CPU_CLKP/N

SB OUTPUT - - - - -NB_PWRGD
 NB_PWRGD_IN
 SB INPUT - - - - -SB_PWRGD

GROUP B

GROUP A

PGOOD(DYN)

DYN_VCC1.1

VLDT(VCC1.1)

VCC1.1

VRM_PWRGD

VCC0.9

VDD_CORE

(VRON)

VDDNB_CORE

PGOOD(2.5)

VCC2.5

(CPU_VDDA_2.5_RUN)

VCC1.5

PGOOD(1.8)

VCC1.8

VCC3, VCC5

MAINON

SUSON

PM_SLP_S3#

PGOOD(1.5)

MEM_VTT

1.5VSUS

PM_SLP_S5#

EC_DNBSWON#

RSMRST#

PGOOD(1.1)

RVCC5, RVCC3, RVCC1.1

VDD_DUAL_EN

RVCC_ON

EC_DNBSWON#

DNBSWON#

AC_OK

(ACIN detect)

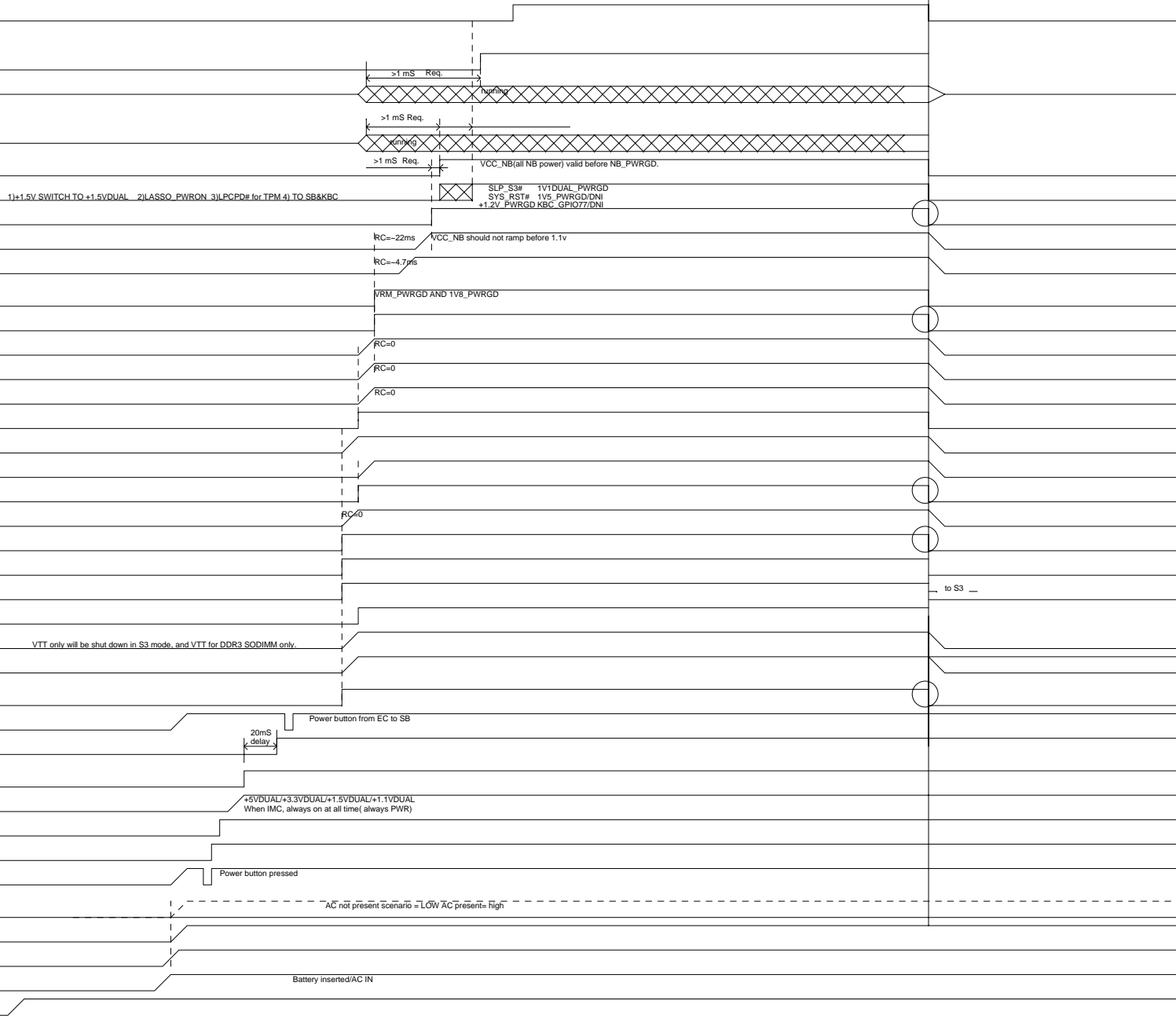
3VPCU

LDO:5.4V

(from DCIN)

+VIN/+12V_HD

A_VBAT



1)+1.5V SWITCH TO +1.5VDUAL 2)IASSO_PWRON_3)I_LPCPD# for TPM 4) TO SB&KBC

RC=22ms

RC=4.7ms

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

RC=0

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RC=0

RC=0

RC=0

RC=0


RC=0

RC=0

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2A Adding R159 (10K) for shut down issue.

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Quanta Computer Inc.

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