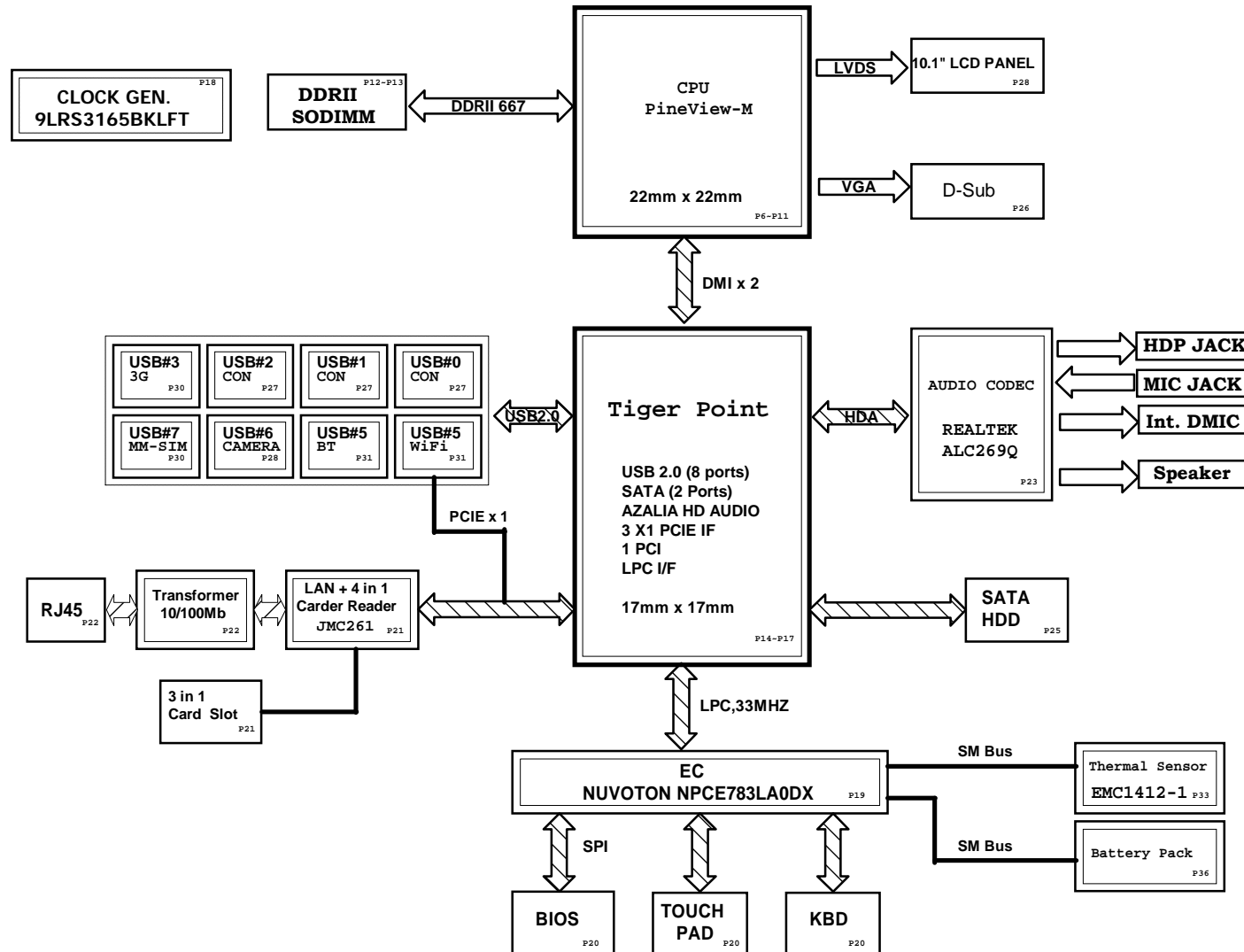


M9F1 Block Diagram R1.0



TI Charger BQ24753ARHBR P.36	
Inputs	Outputs
DC_IN	DCBATOUT BT+

System DC/DC TPS51125RGER P.37	
Inputs	Outputs
DCBATOUT	+3VALW +5VALW +5VALW_LDO +5CVCC

System DC/DC TPS51124RGER P.38	
Inputs	Outputs
DCBATOUT	+1_8VSUS VCCGFX

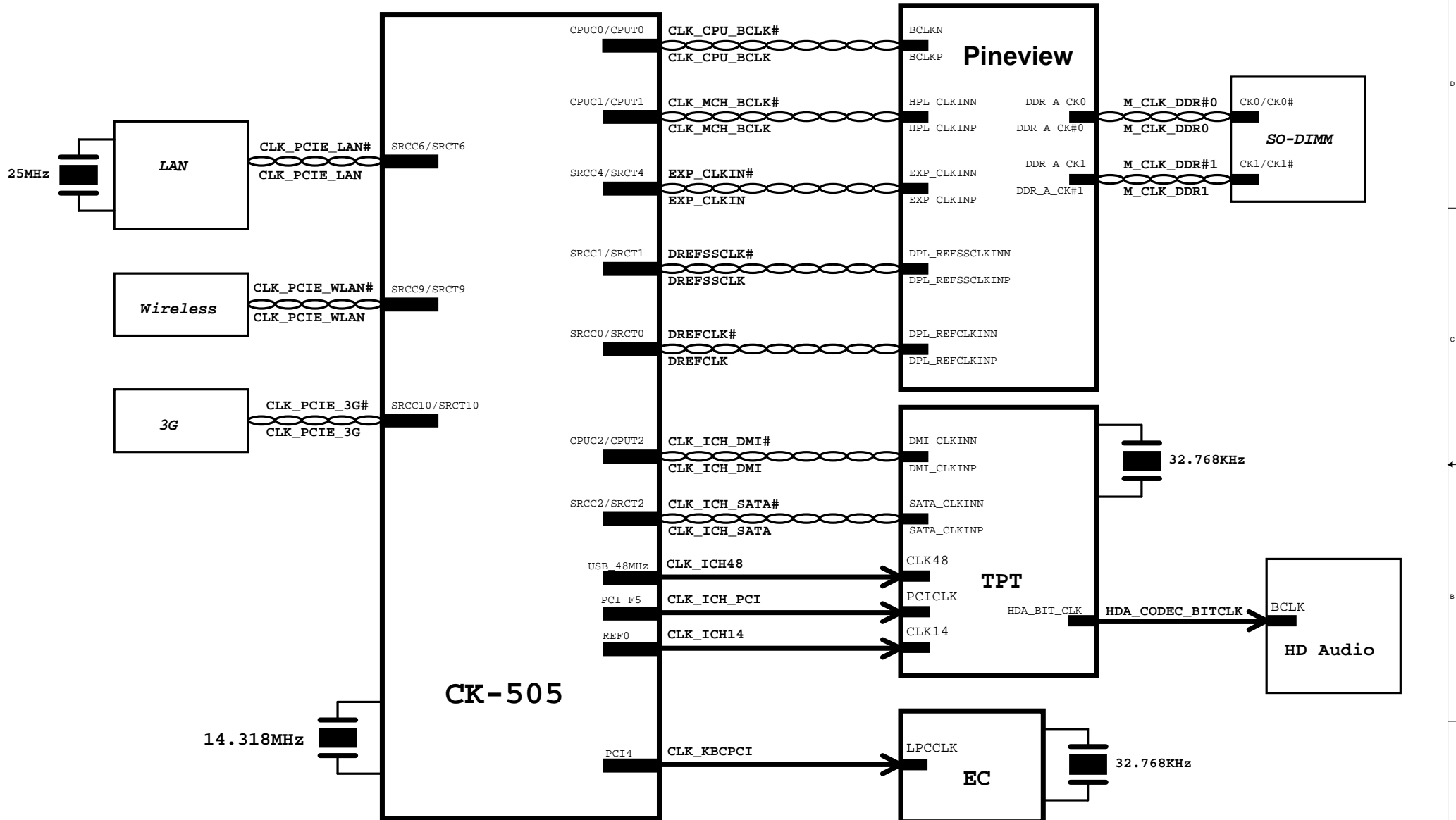
CPU DC/DC MAX8796GTJ+ P.39	
INPUTS	OUTPUT
DCBATOUT	VHCORE

System DC/DC G2998BP11U P.40	
Inputs	Outputs
+1_8VSUS	+0_9VRUN

System DC/DC G9731P11U P.40	
Inputs	Outputs
+1_8VSUS	+1_5VRUN

System DC/DC G9731P11U P.40	
Inputs	Outputs
+1_8VSUS	+1_05VRUN

CCPBG			
Block Diagram			
Rev	Document Number	Rev	
M9F1	M9F1	6.1	
Date:	Wednesday, March 17, 2010	Sheet	1 of 44



<div style="background-color: black; width: 100px; height: 15px; margin: 0 auto;"></div> <p align="center">CCPBG</p>		
<p align="center">Clock distribution</p>		
<p>Size A3</p>	<p>Document Number M9F1</p>	<p>Rev 0.1</p>
<p>Date: Wednesday, March 17, 2010 Sheet 2 of 44</p>		

Pine Trail Power Flowchart for M9F1

Voltage Rails

O MEANS ON
X MEANS OFF

<div>power plane</div> <div>State</div>	+5VALW_LDO +ECVCC	+5VALW +3VALW	+3VSUS +1_8VSUS	+5VRUN +3VRUN +1_8VRUN +1_5VRUN +1_05VRUN +0_9VRUN VCCGFX VHCORE
S0	O	O	O	O
S3	O	O	O	X
S5/AC, S4	O	O	X	X
S5 Battery only	O	X	X	X
S5 S4/AC & Battery don't exist (G3)	X	X	X	X

S3 : STR

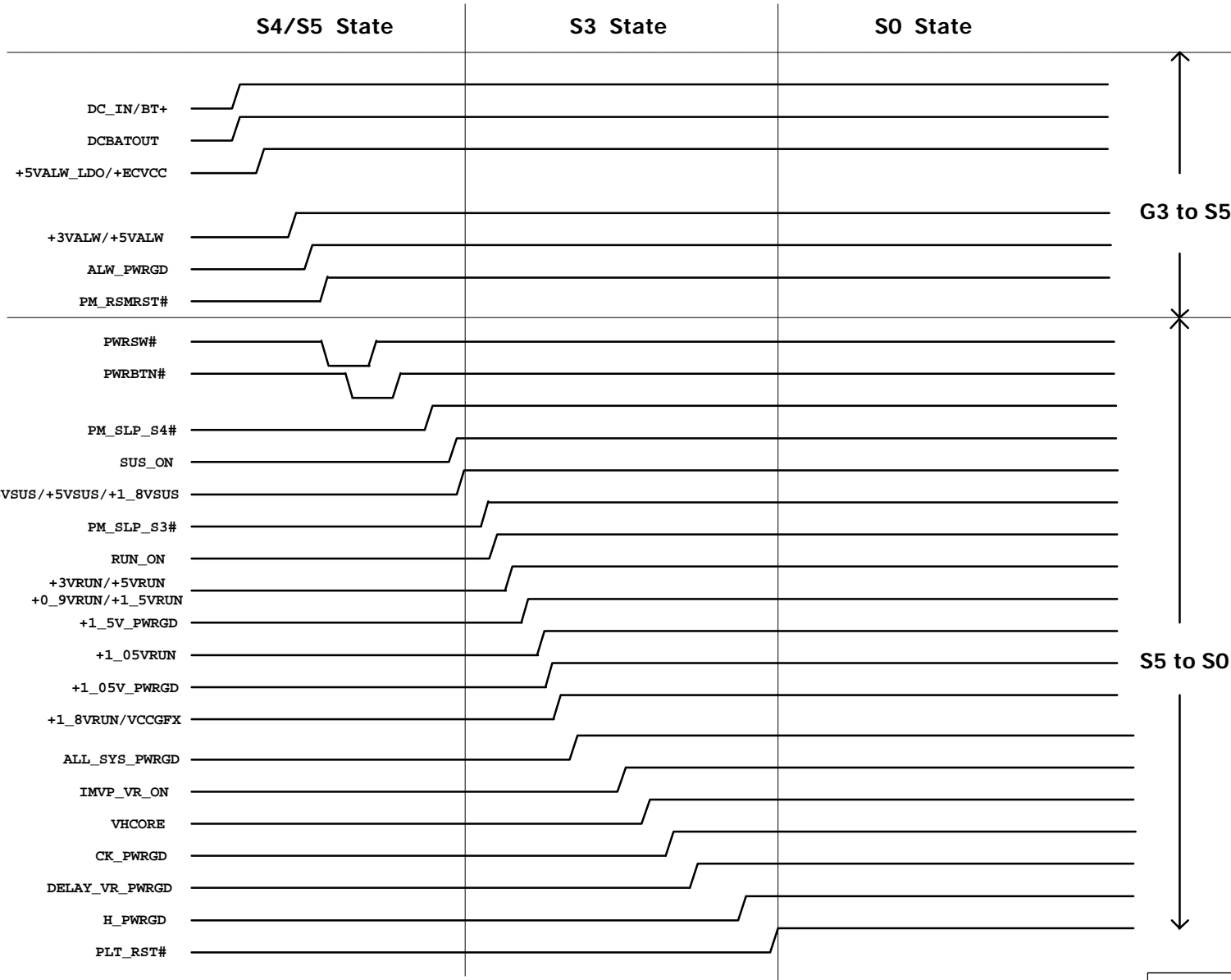
S4 : STD

S5 : SOFT OFF

G3 : ME OFF

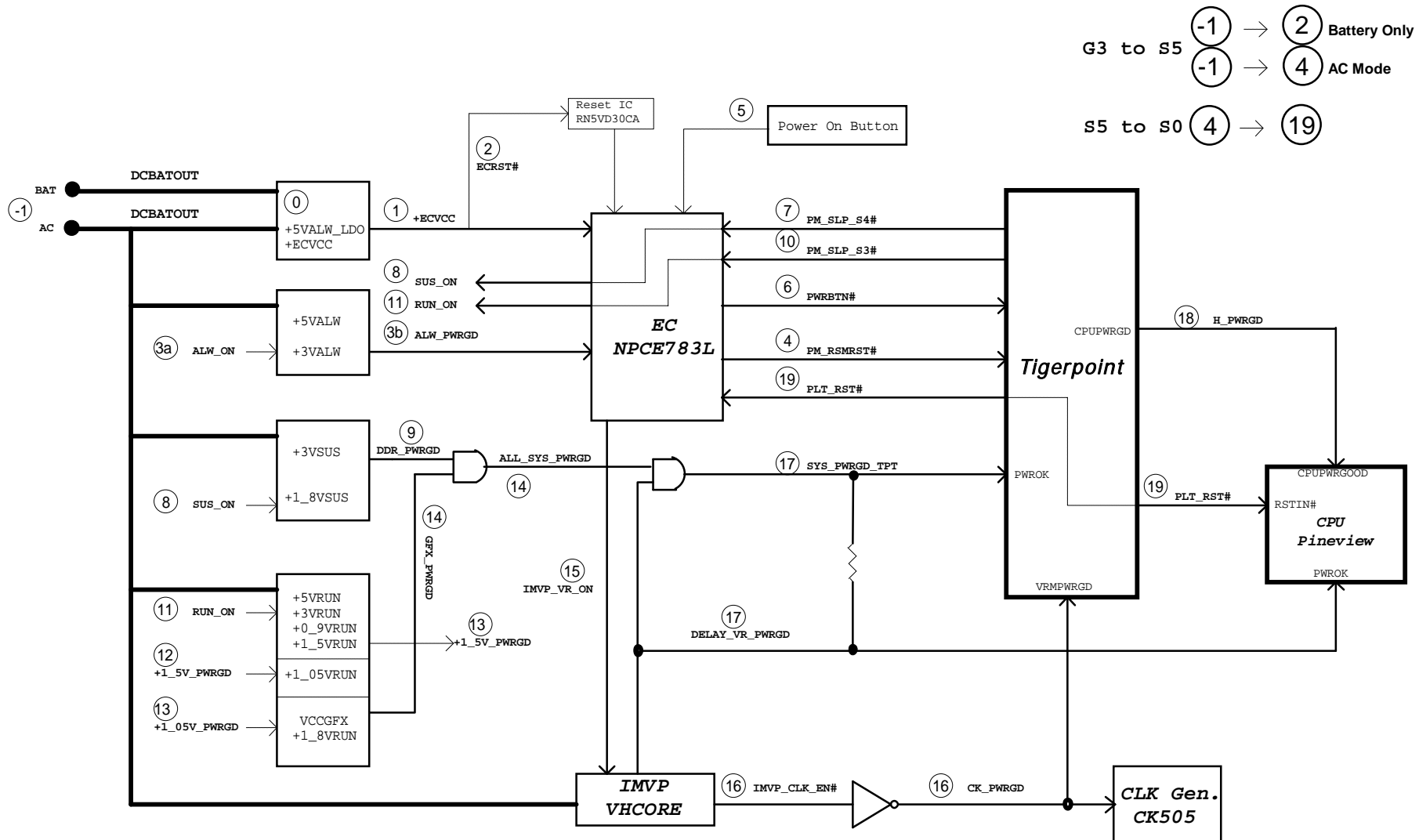
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CCPBG		
Title		
Power Flowchart		
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010		
Sheet 3 of 44		

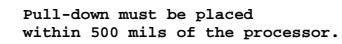
Pine Trail Power On Sequence



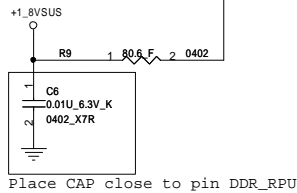
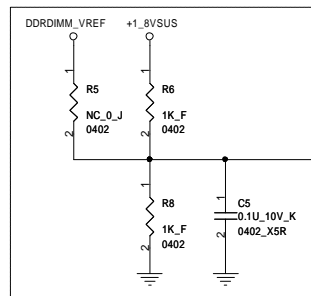
CCPBG		
Power On Sequence(1)		
Size	Document Number	Rev
Custom	M9F1	0.1
Date:	Wednesday, March 17, 2010	Sheet 4 of 44

Pine Trail Power On Sequence

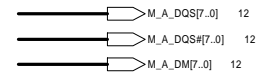
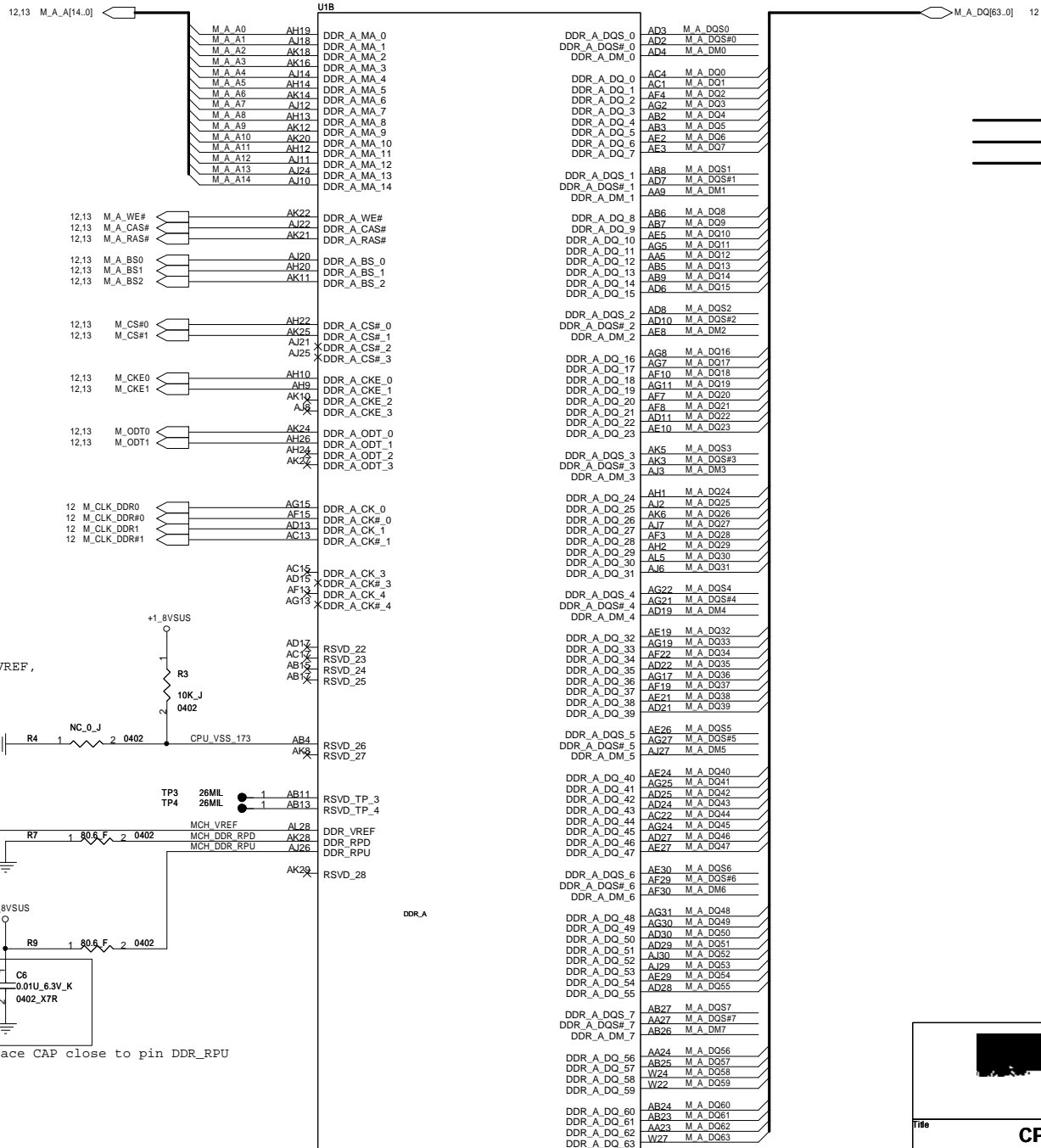




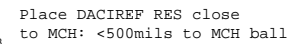
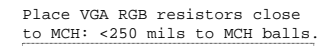
Place resistors close to MCH PINS ON MCH_VREF,
Place 0.1uF CAP close to MCH.

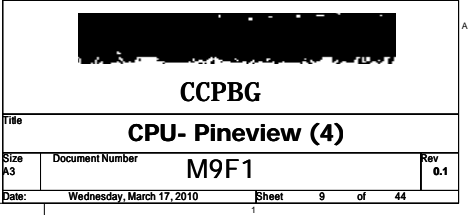


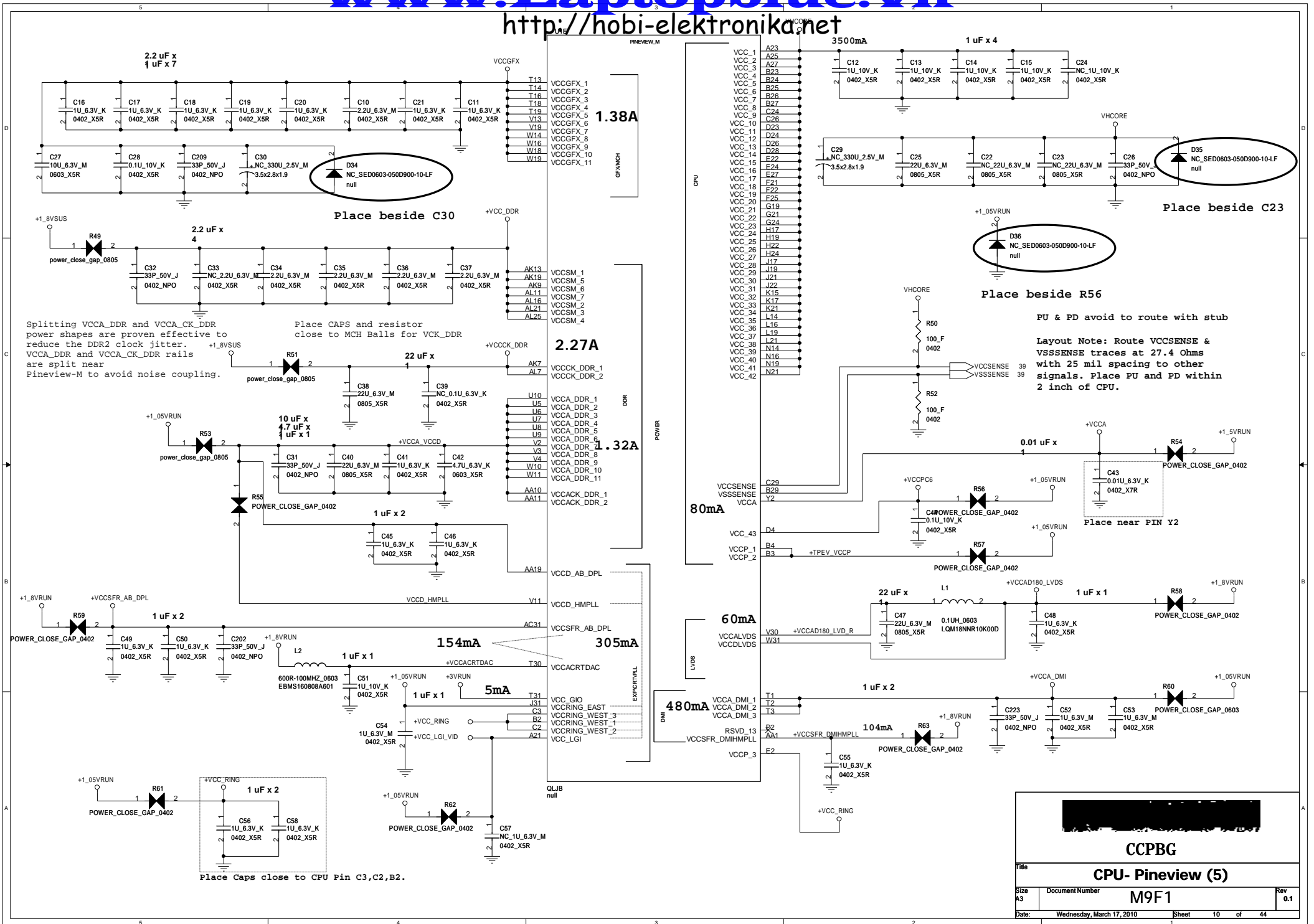
Place CAP close to pin DDR_RPU

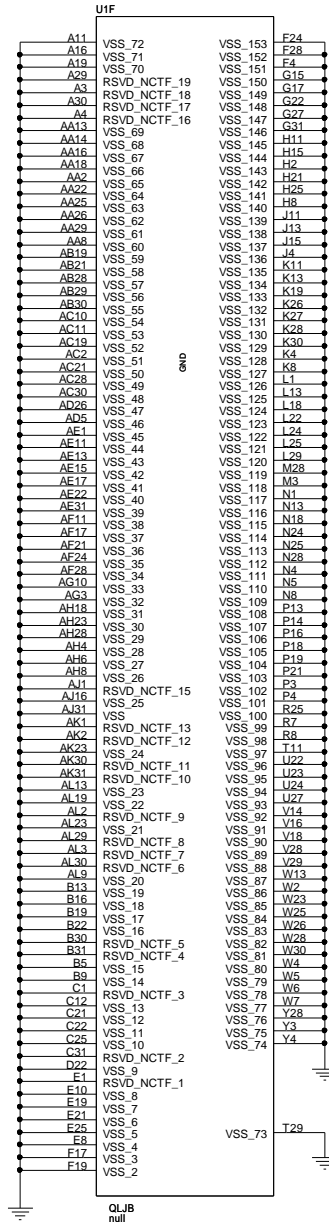


CCPBG		
CPU- Pineview (2)		
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010	Sheet 7 of 44	

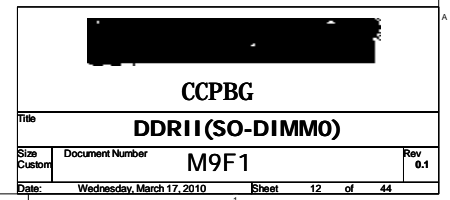


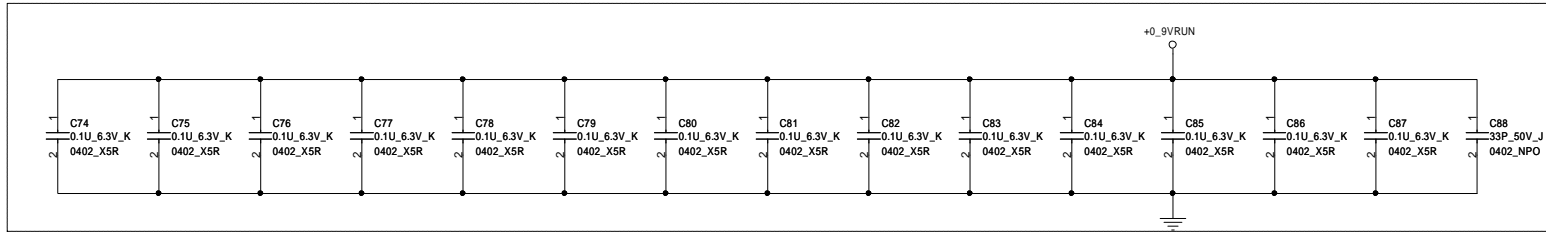




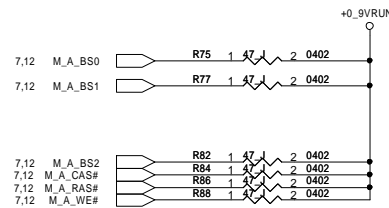
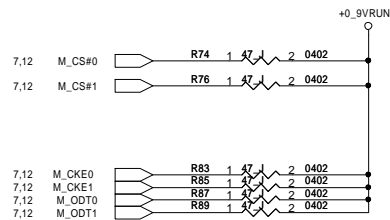


CCPBG		
Title		
CPU- Pineview (6)		
Size A3	Document Number M9F1	Rev 0.1
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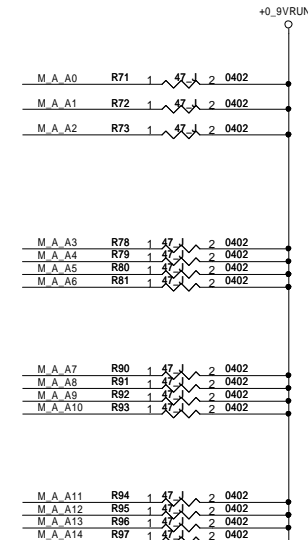





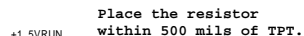
Place one cap close to every two pull-up resistors terminated to +0.9V_RUN.



7,12 M_A_A[14..0]

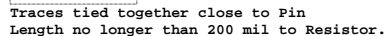
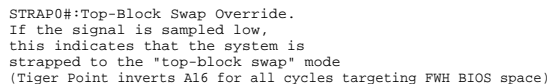


		
CCPBG		
Title		
DDRII (Termination)		
Size	Document Number	Rev
A3	M9F1	0.1
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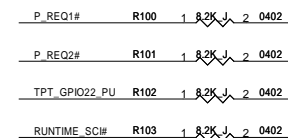
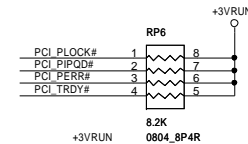
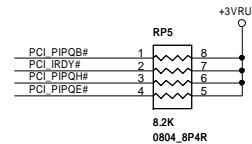
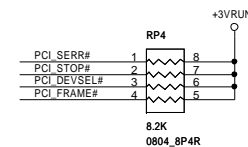
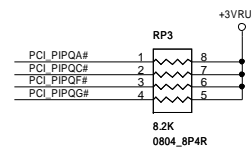
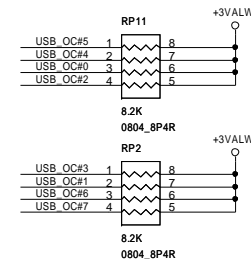


STRAP2#/ GPIO17	STRAP1#/ GPIO48	Routing
0	1	SPI
1	0	PCI
1	1	LPC

STRAP2#/GPIO17 and STRAP1#/GPIO48
have weak internal pull-ups



Port0	External USB1
Port1	External USB2
Port2	External USB3
Port3	WWAN (3G/GPS)
Port4	WLAN(WIFI)
Port5	Bluetooth
Port6	Camera module
Port7	MM-SIM



TPT Strap Pin

Strap Pin	Internal PU/PD	External PU/PD
STRAP0#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP1#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP2#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)



CCPBG

Tiger Point (1)

Size

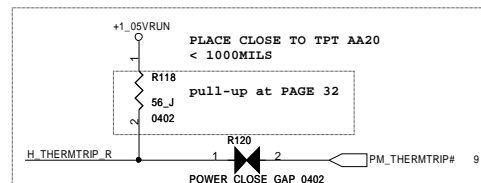
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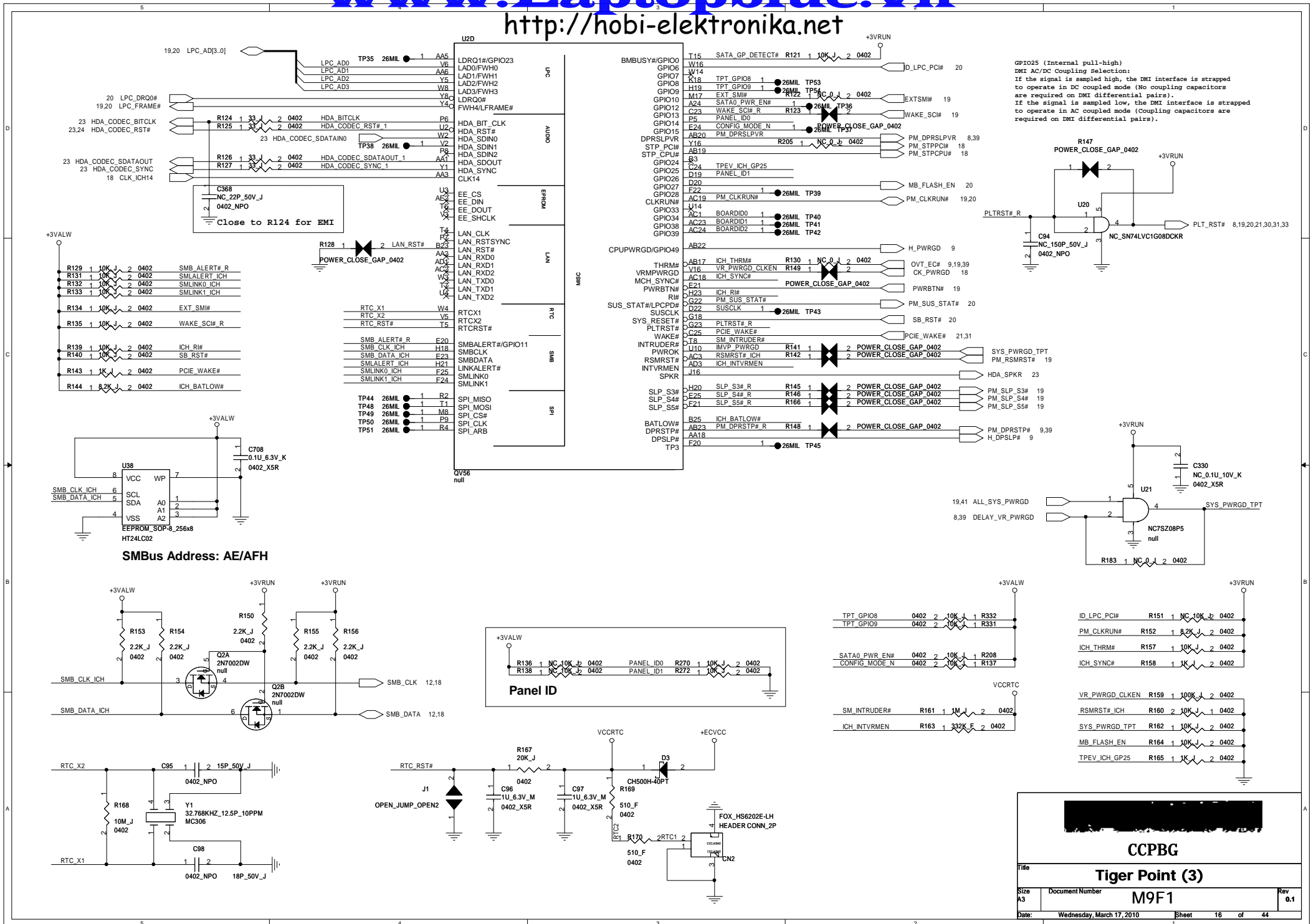
M9F1

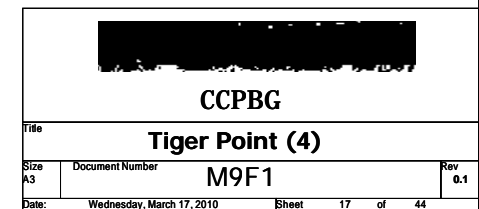
Rev	
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9LRS3165BKLFT
pull

9LRS3165BKLFT
pull

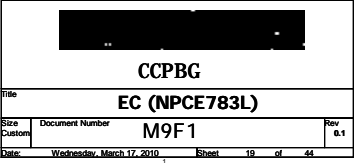
9LRS3165BKLFT
pull

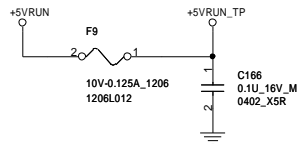
9LRS3165BKLFT
pull

9LRS3165BKLFT
pull

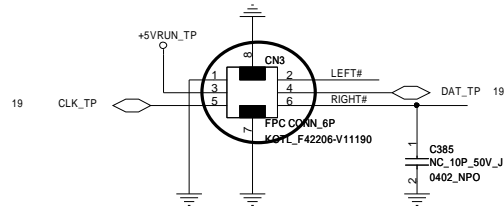
Stuff
C720, C721, R233, R359, PR144, PR145, PR146

NC
R357, PR139, PU9, PC115, PC116, PR118, PR123, PR124





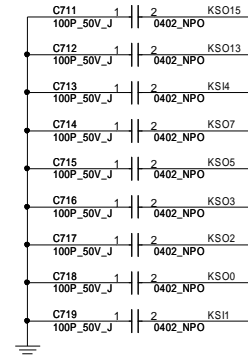
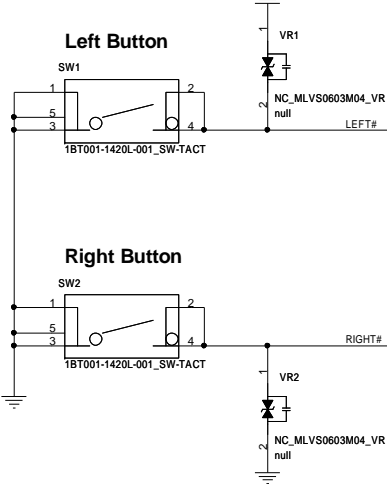
Touch Pad CONN.



BFT Test Point for Touch Pad (BOTTOM side)

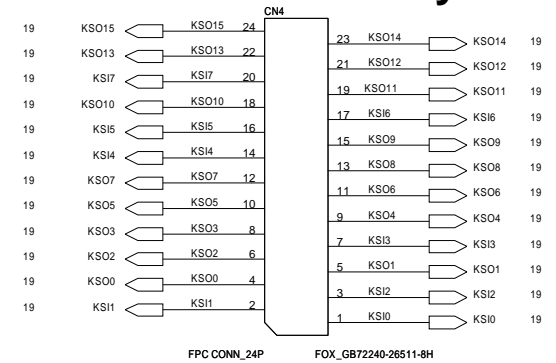
tpc60b_100	TP100	1	GND
tpc60b_100	TP109	1	LEFT#
tpc60b_100	TP110	1	RIGHT#
tpc60b_100	TP111	1	DAT TP
tpc60b_100	TP112	1	CLK TP
tpc60b_100	TP113	1	+5VRUN_TP

Touch Pad



Place these caps close to CN4.

Keyboard

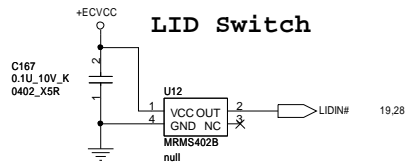


BFT Test Point for Keyboard (BOTTOM side)

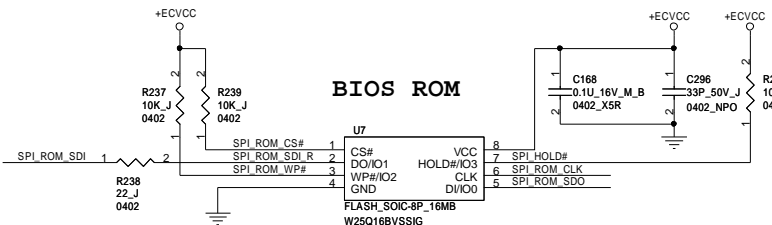
tpc60b_100	TP96	1	KSI4
tpc60b_100	TP97	1	KSO7
tpc60b_100	TP98	1	KSO5
tpc60b_100	TP99	1	KSI2

tpc40L_75	TP101	1	SPI_ROM_CS#
tpc40L_75	TP102	1	SPI_ROM_SDI_R
tpc40L_75	TP103	1	SPI_ROM_WP#
tpc40L_75	TP104	1	GND
tpc40L_75	TP105	1	+ECVCC
tpc40L_75	TP106	1	SPI_HOLD#
tpc40L_75	TP107	1	SPI_ROM_CLK
tpc40L_75	TP108	1	SPI_ROM_SDO

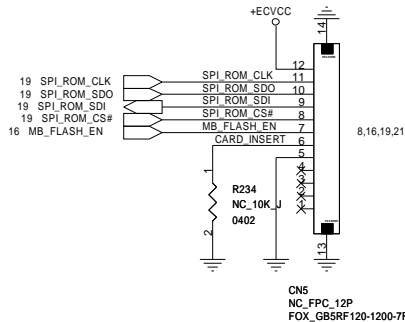
LID Switch



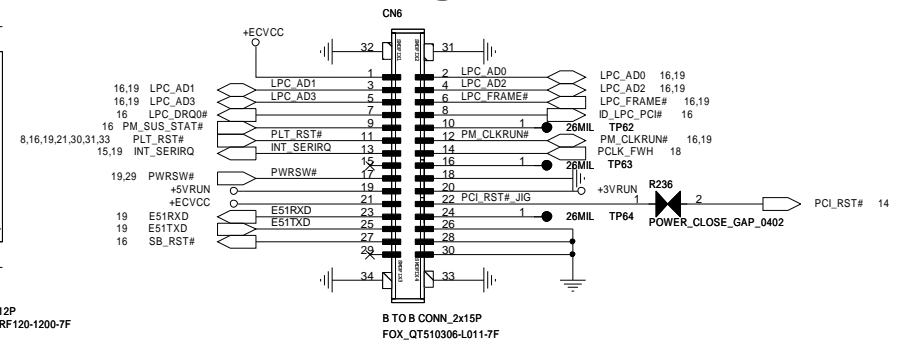
BIOS ROM



EXTERNAL SPI ROM INTERFACE



Debug Port

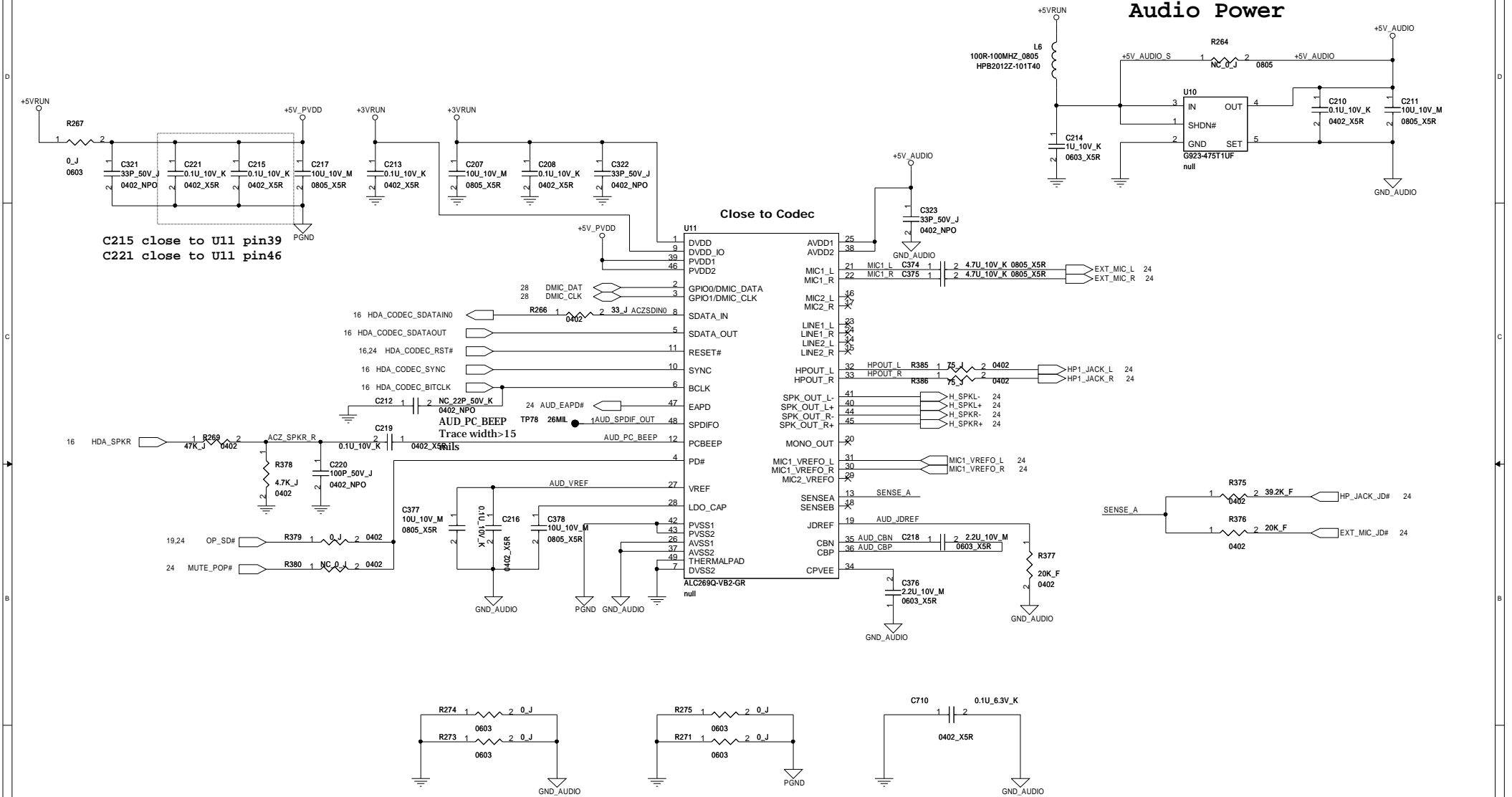


CCPBG

KB/TP/Debug Port

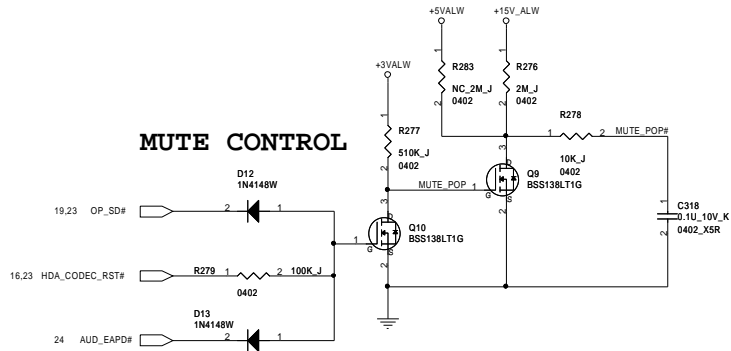
Size	Document Number	Rev
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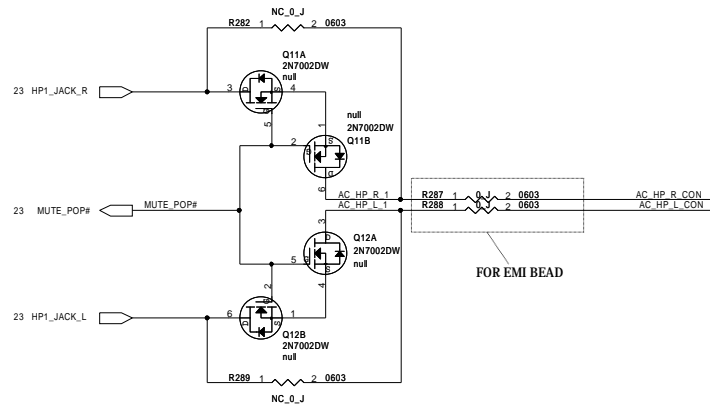


CCPBG			
Title Audio Codec ALC269Q			
Size A3	Document Number	M9F1	Rev 0.1
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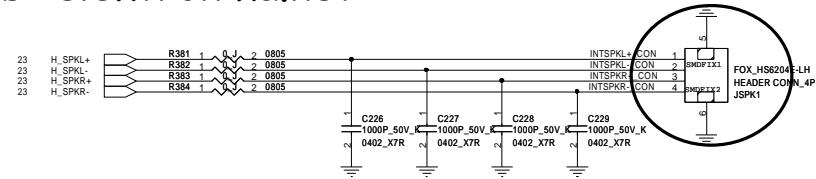
MUTE CONTROL



HP CONN



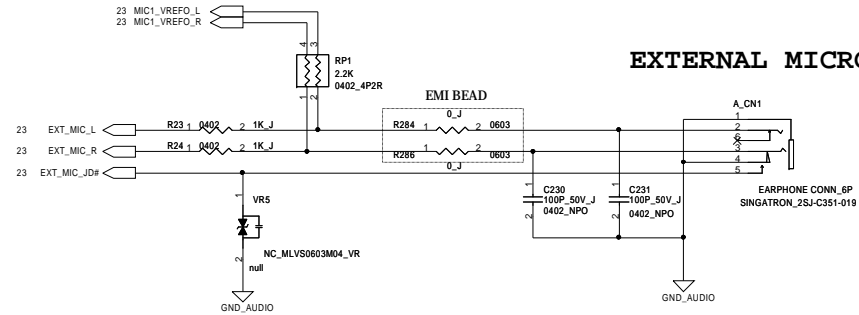
FOR EMI BEAD



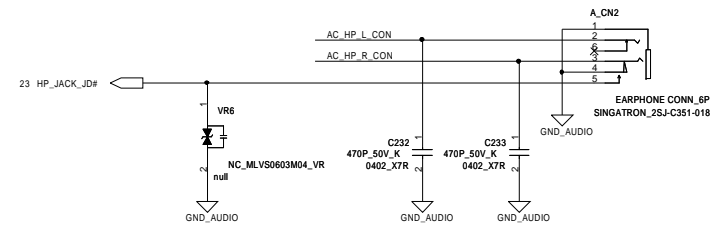
BFT Test Point for Speaker (BOTTOM side)

tpc60b_100	TP87	1	INTSPKL+ CON
tpc60b_100	TP88	1	INTSPKL- CON
tpc60b_100	TP89	1	INTSPKR+ CON
tpc60b_100	TP90	1	INTSPKR- CON

EXTERNAL MICROPHONE



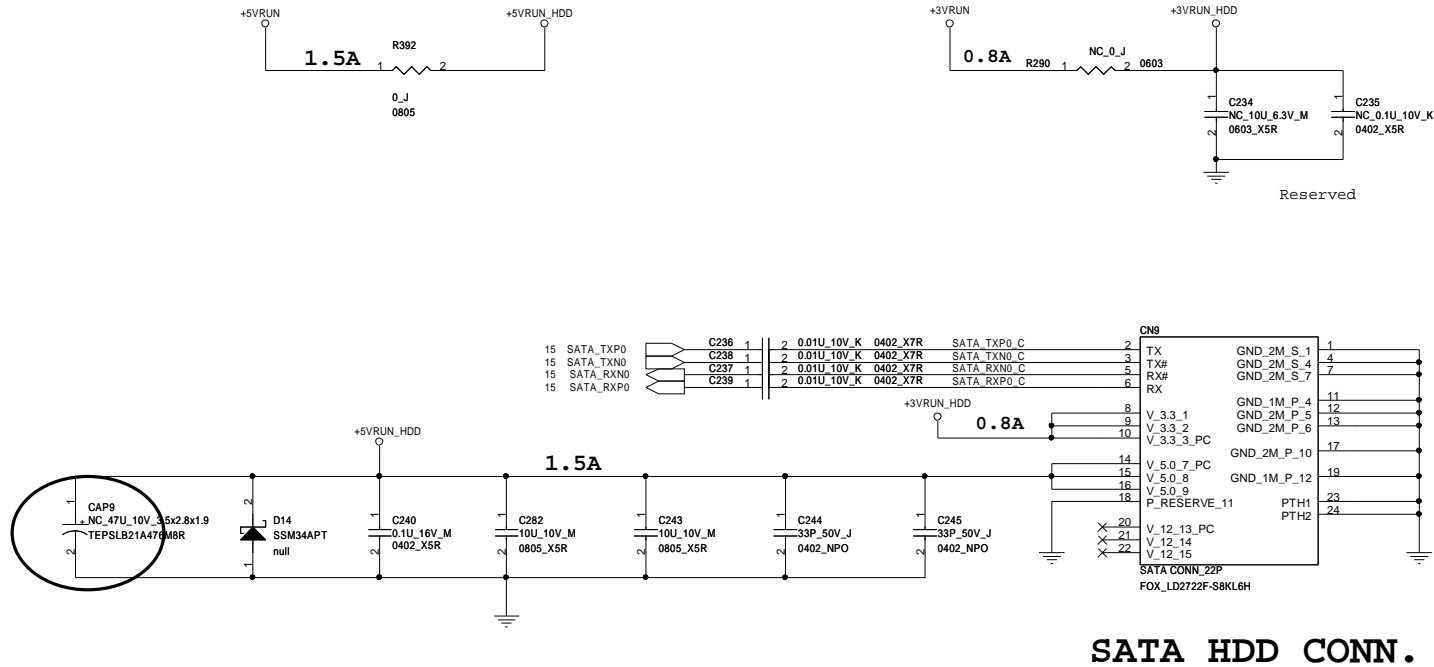
HEADPHONE



CCPBG

MIC & Audio Jack

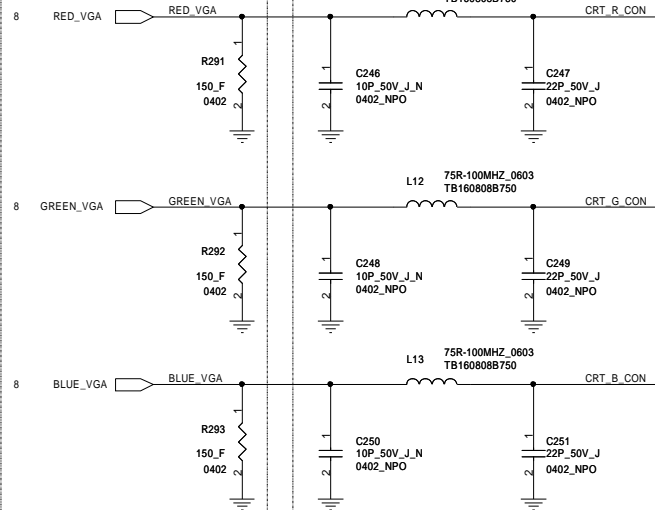
Size	Custom	Document Number	M9F1	Rev	0.1
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SATA HDD CONN.

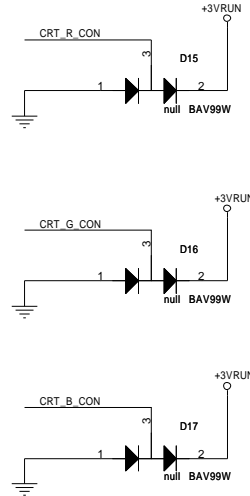
CCPBG		
SATA HDD		
Size A3	Document Number M9F1	Rev 0.1
Date:	Wednesday, March 17, 2010	Sheet 25 of 44

Terminal Resistor



Filter Circuit (1 pole)

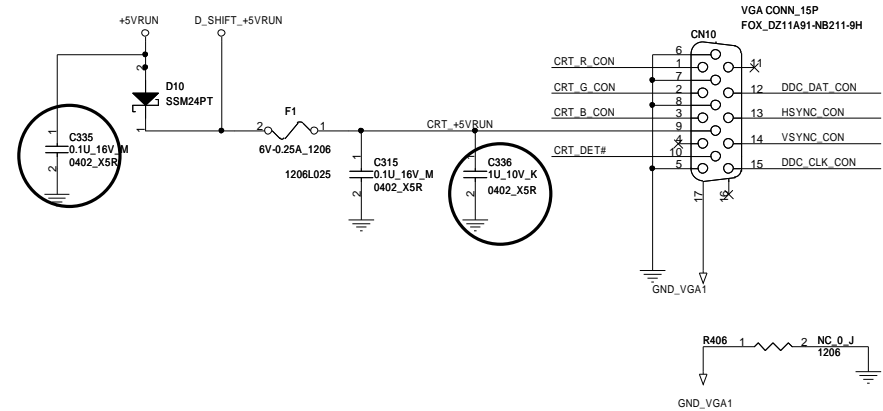
ESD Protection Circuit



Place ESD Diodes Near D-Sub Conn.

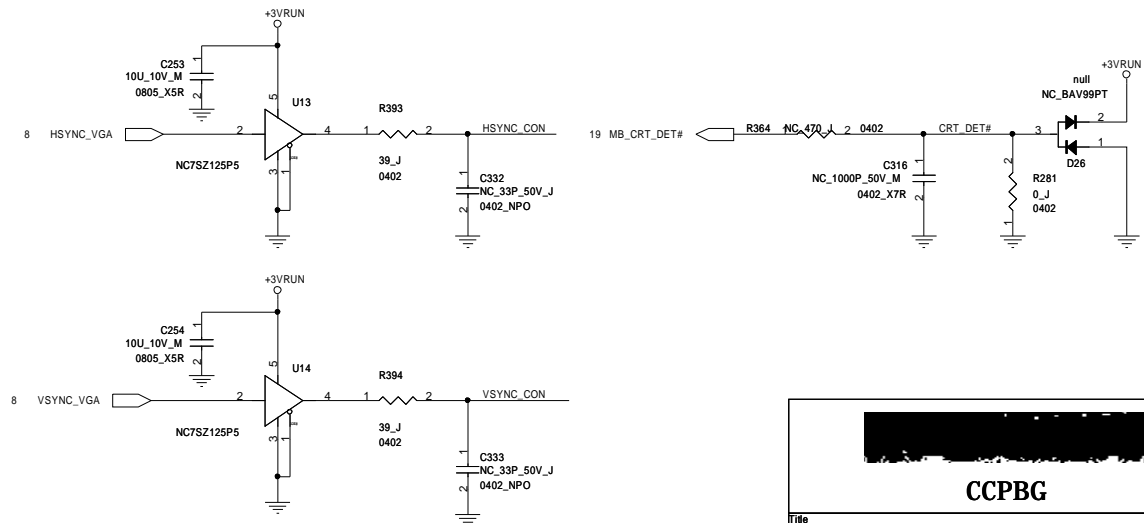
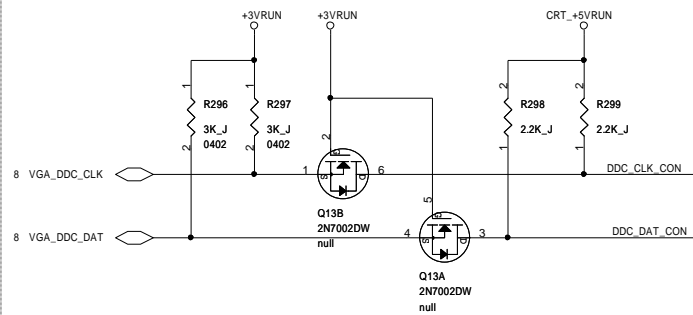
RGB routing

1. from SCH to the first 150 ohm resistor: 12 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 7 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 200 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



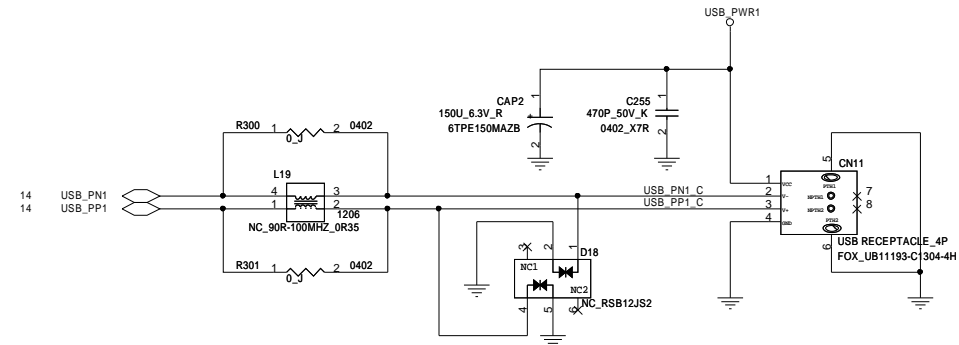
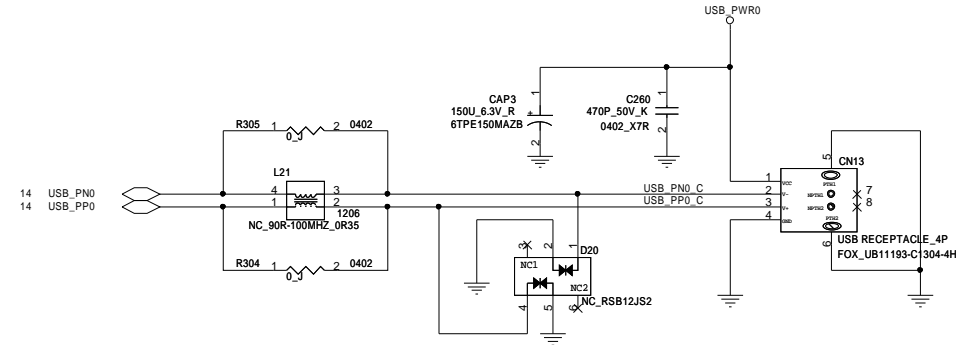
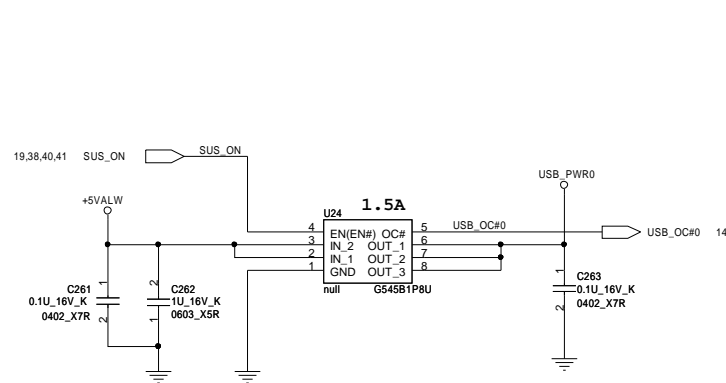
The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

Level Shifter for DDC BUS

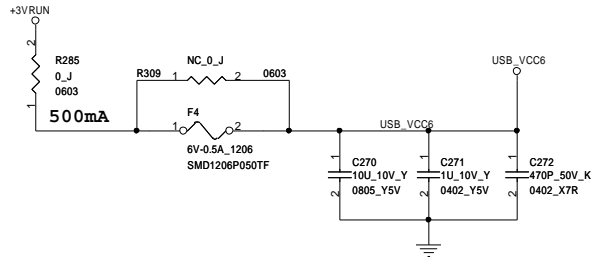


CCPBG

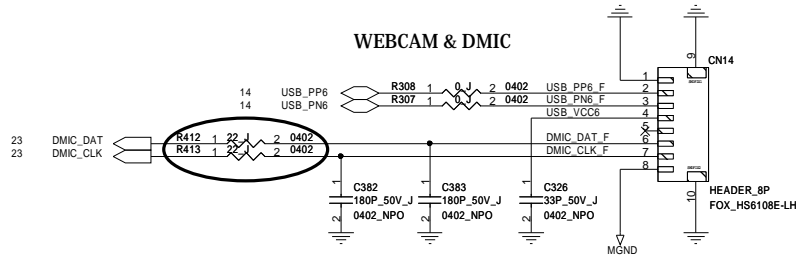
Title			
VGA Connector (D-Sub)			
Size	Document Number	Rev	
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CCPBG		
Title		
USB Connector x 3		
Size	Document Number	Rev
Custom	M9F1	0.1
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WEBCAM & DMIC

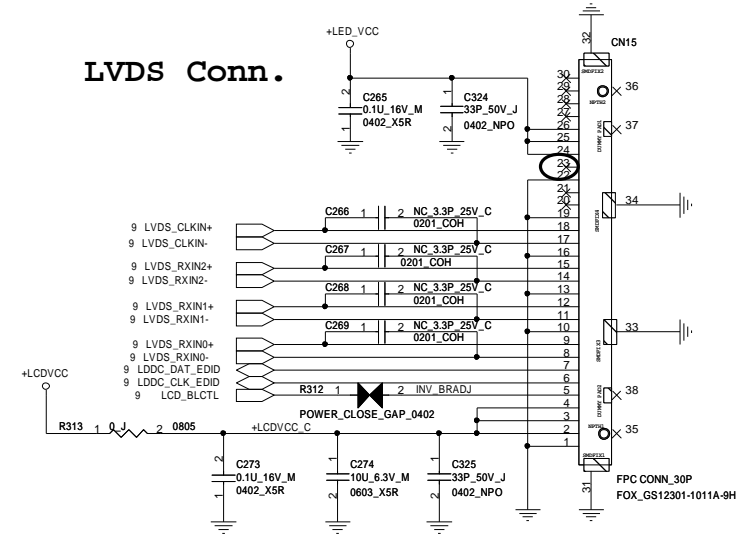


Close to CN14

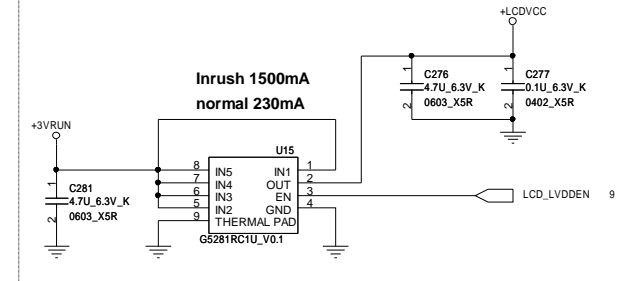
BFT Test Point for Camera (BOTTOM side)

tpc40t_75	TP147	1	USB_PP6_F
tpc40t_75	TP148	1	USB_PN6_F
tpc40t_75	TP149	1	USB_VCC6
tpc40t_75	TP150	1	DMIC_DAT_F
tpc40t_75	TP151	1	DMIC_CLK_F
tpc40t_75	TP152	1	MGND

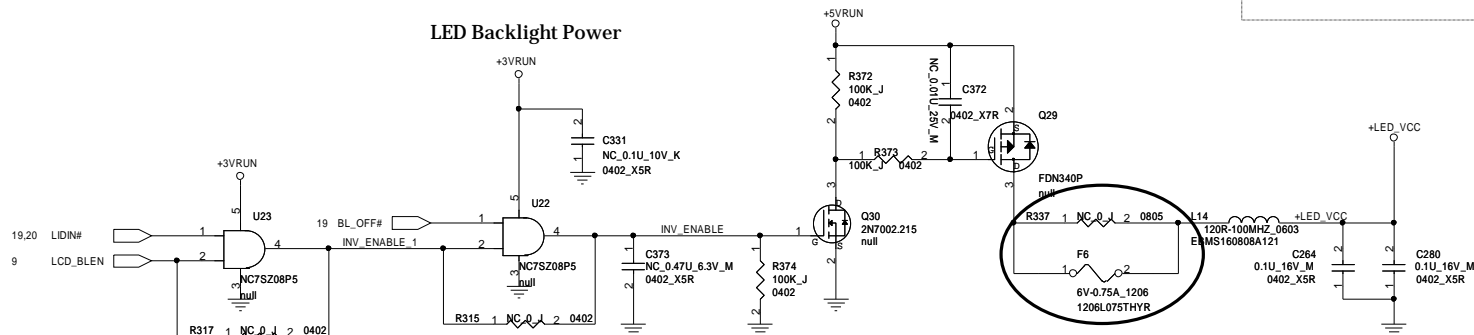
LVDS Conn.



LCD Core Power



LED Backlight Power

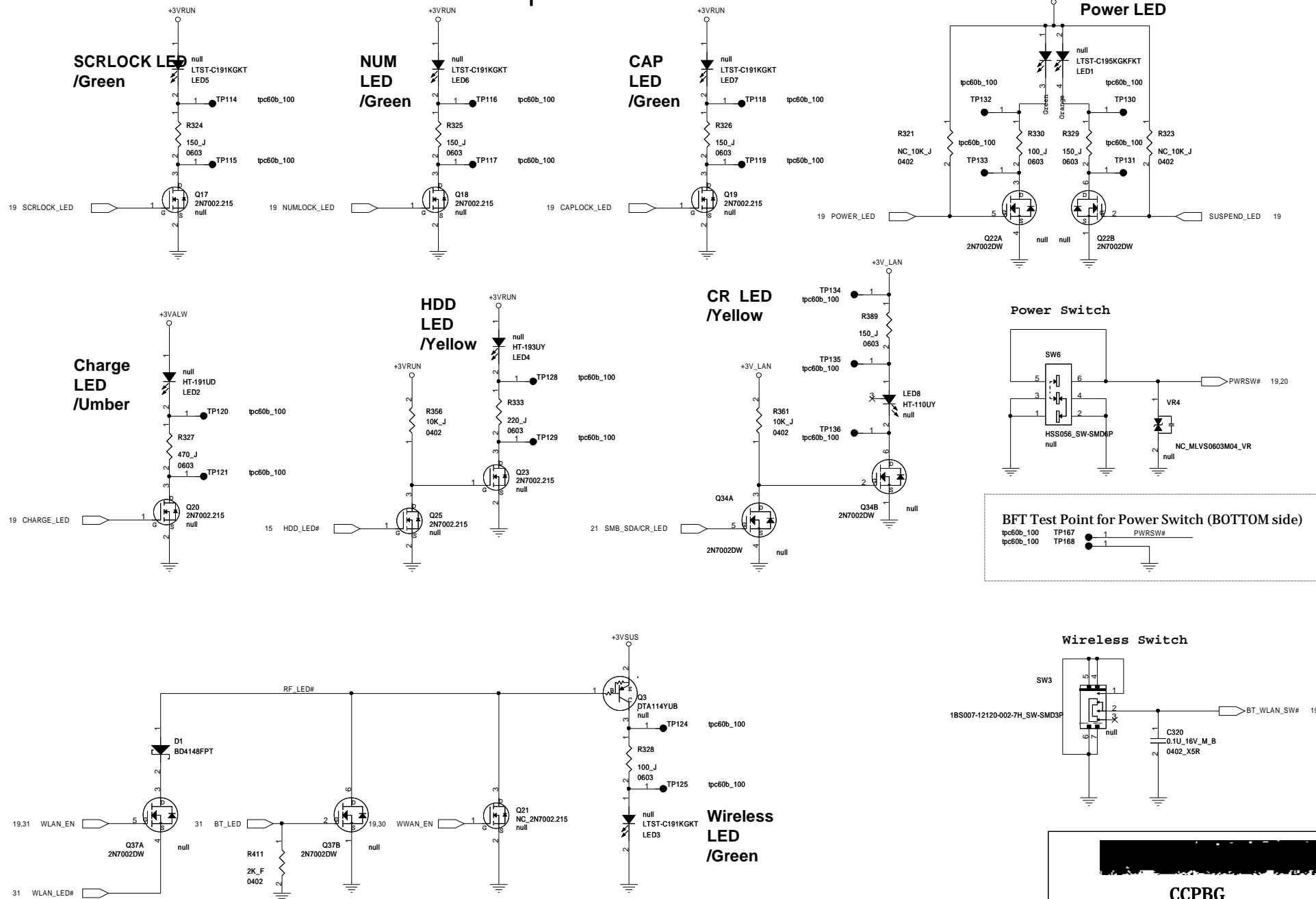


CCPBG

LVDS & WEBCAM

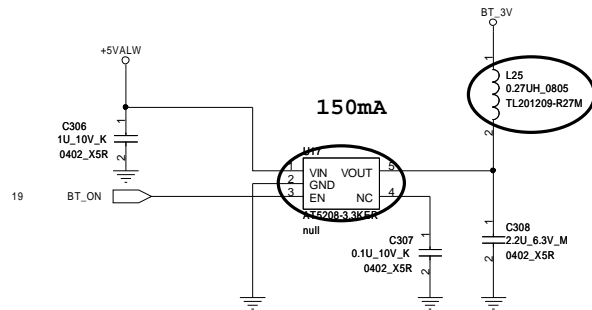
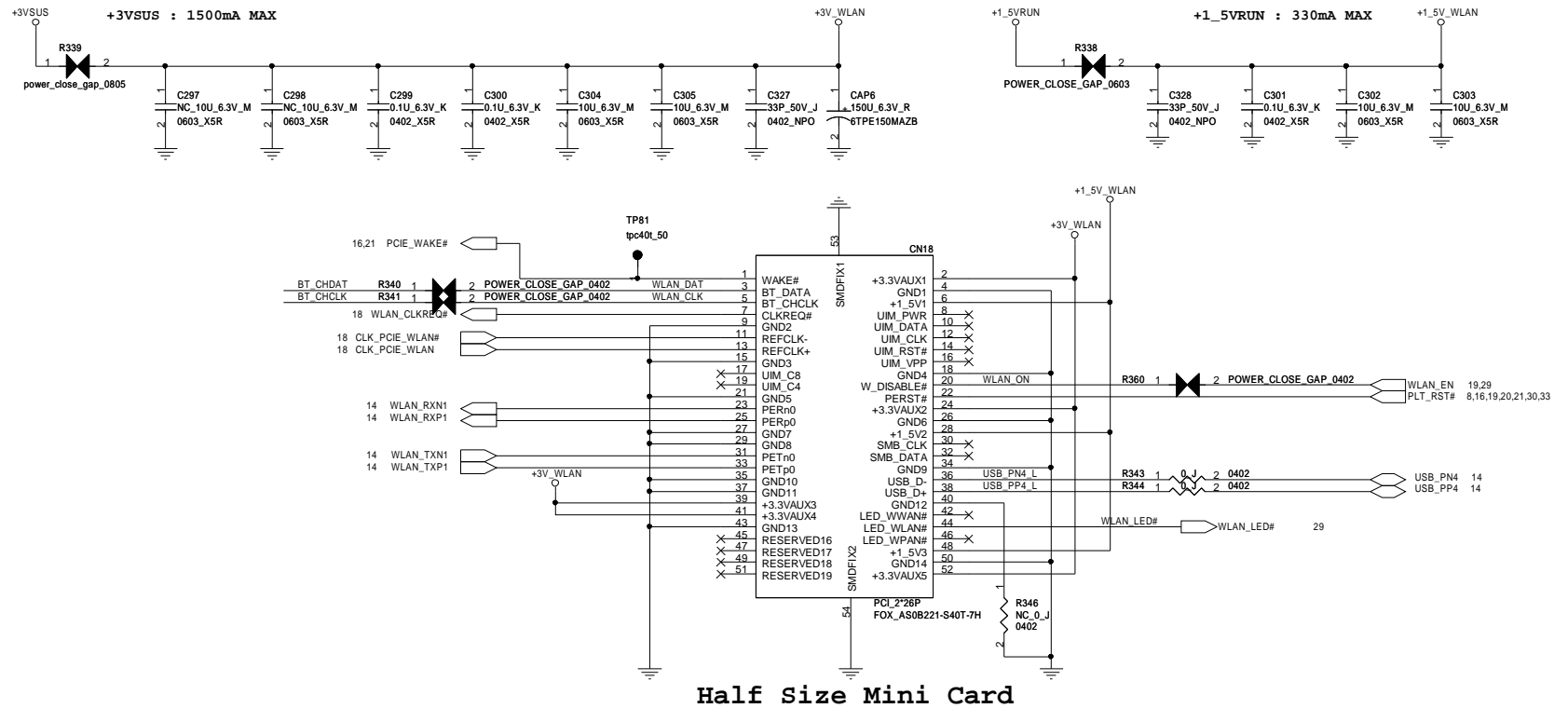
M9F1

Title	Document Number	Rev
Size	Custom	0.1
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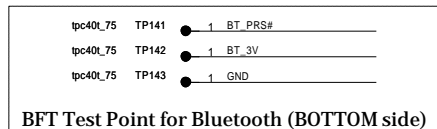
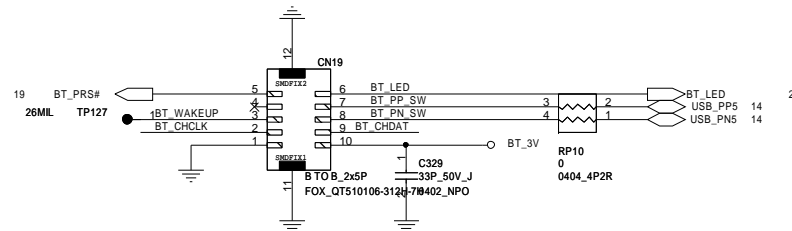


CCPBG

Title		
Power Switch & LED		
Size	Document Number	Rev
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Date:	Wednesday, March 17, 2010	Sheet 29 of 44



Bluetooth CONN.



CCPBG			
Mini PCIE - WIFI & BT			
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5

4

3

2

1

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D

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C

B

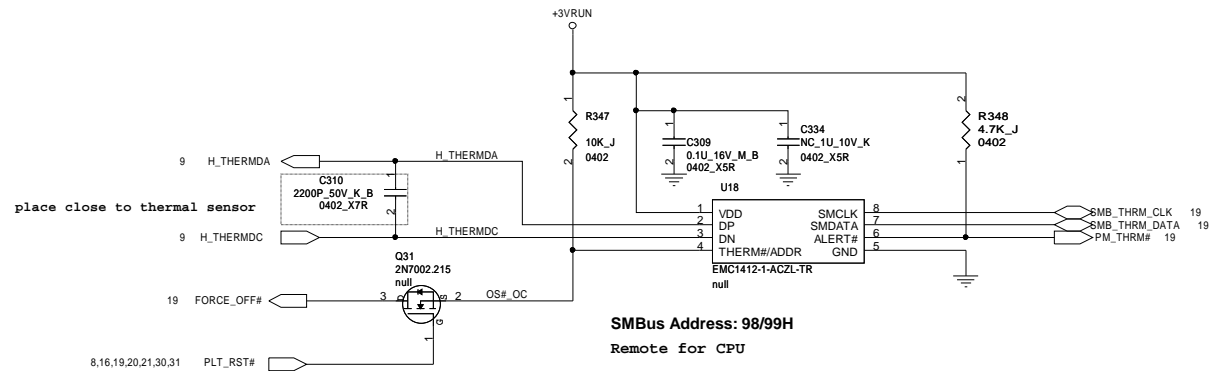
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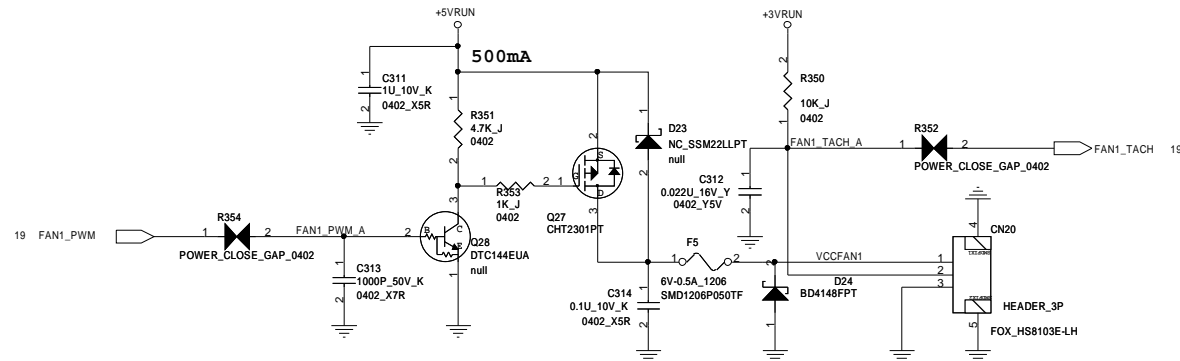
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CPU Thermal Sensor



FAN

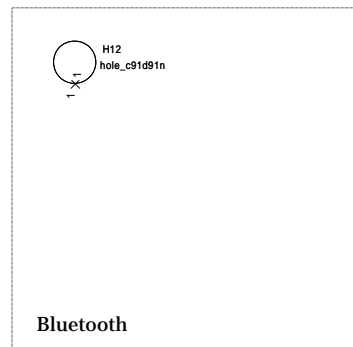
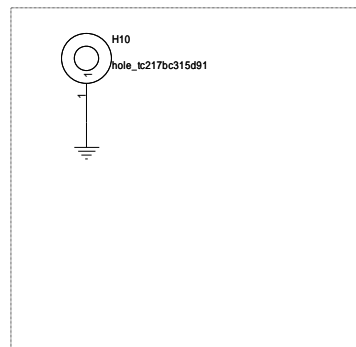
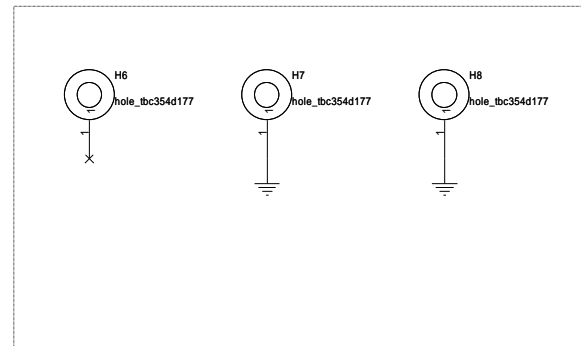
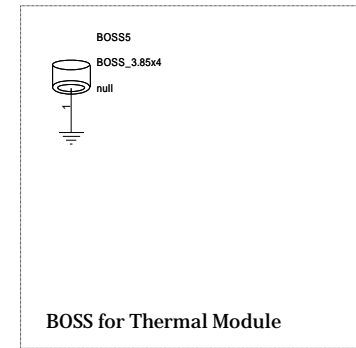
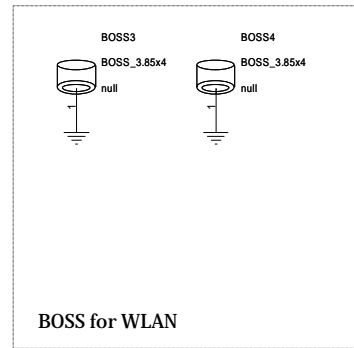
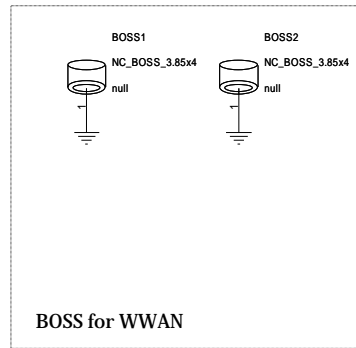


BFT Test Point for FAN (BOT side)

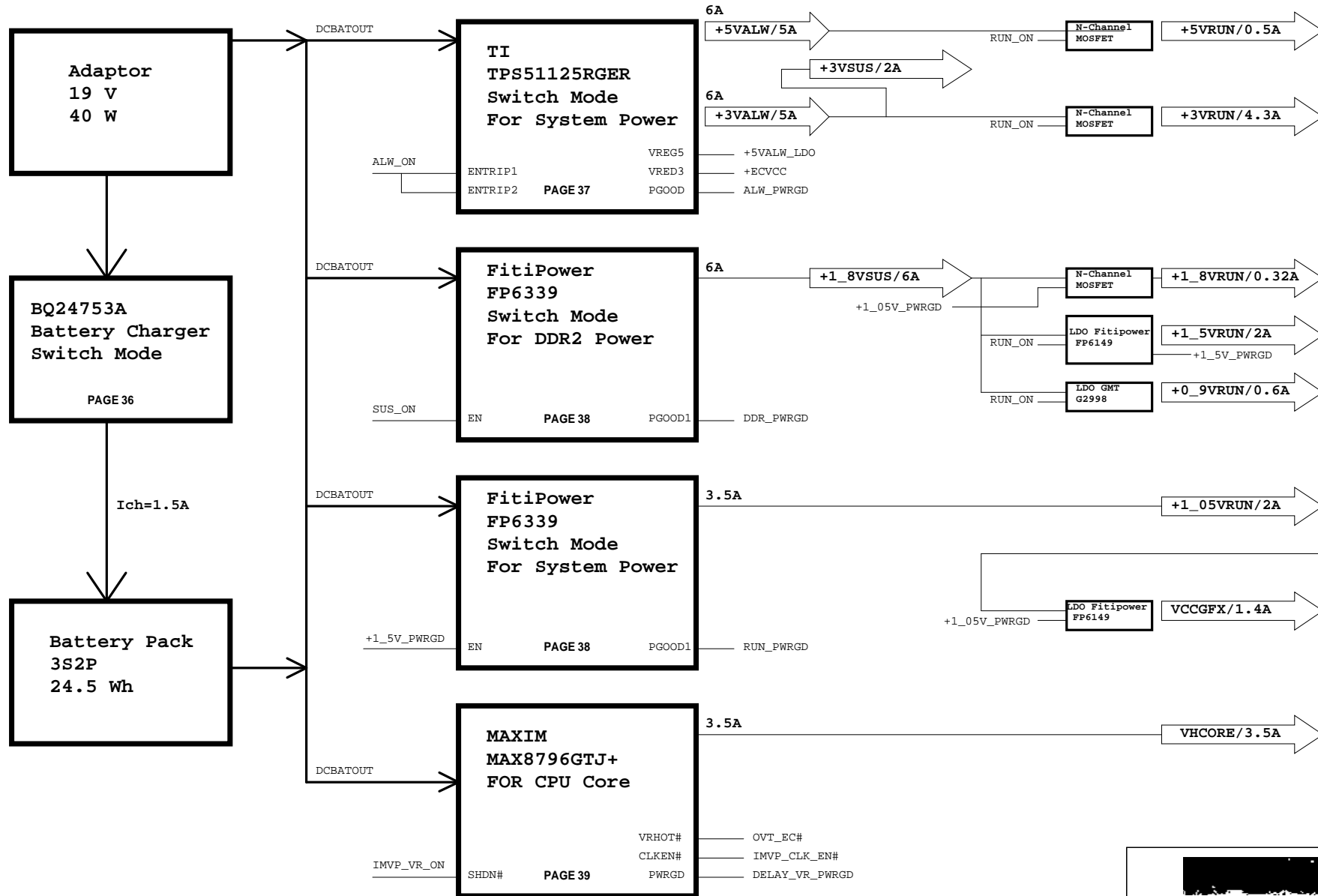
tpc60b_100	TP83	1	VCCFAN1
tpc60b_100	TP84	1	FAN1_TACH_A
tpc60b_100	TP85	1	
tpc60b_100	TP86	1	FAN1_PWM_A

CCPBG

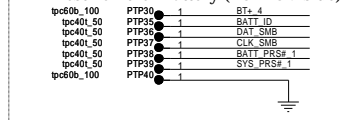
Title			
Thermal & Fan			
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M9F1 Power Block Diagram



BFT Test Point for Battery (BOTTOM side)



Battery CONN.

1.5A

	CP	PWRLIMIT
40W	1.92A/36.48W	2A/38W

CCPBG

DCIN&Charger

M9F1

Title

Size
Custom

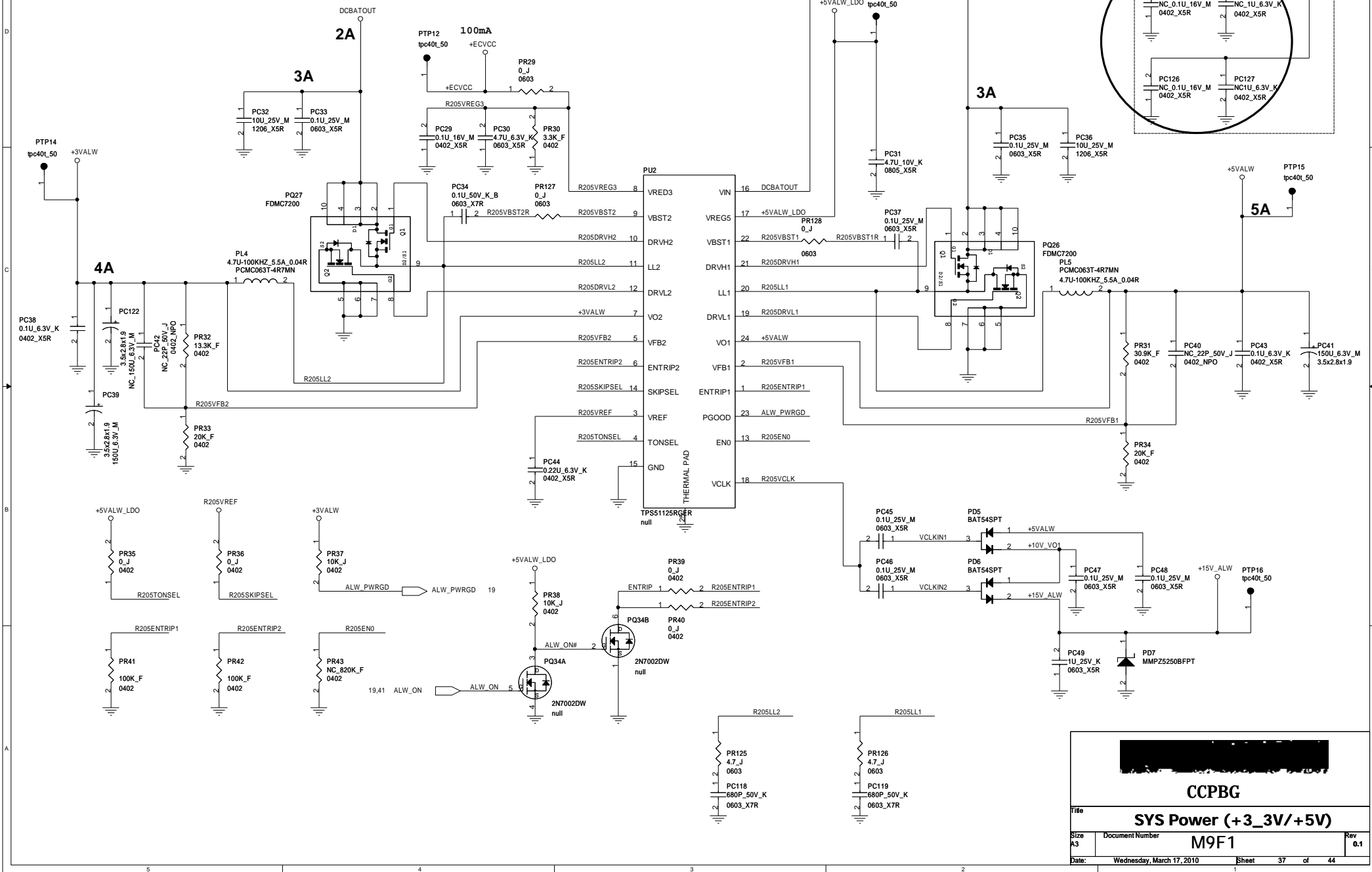
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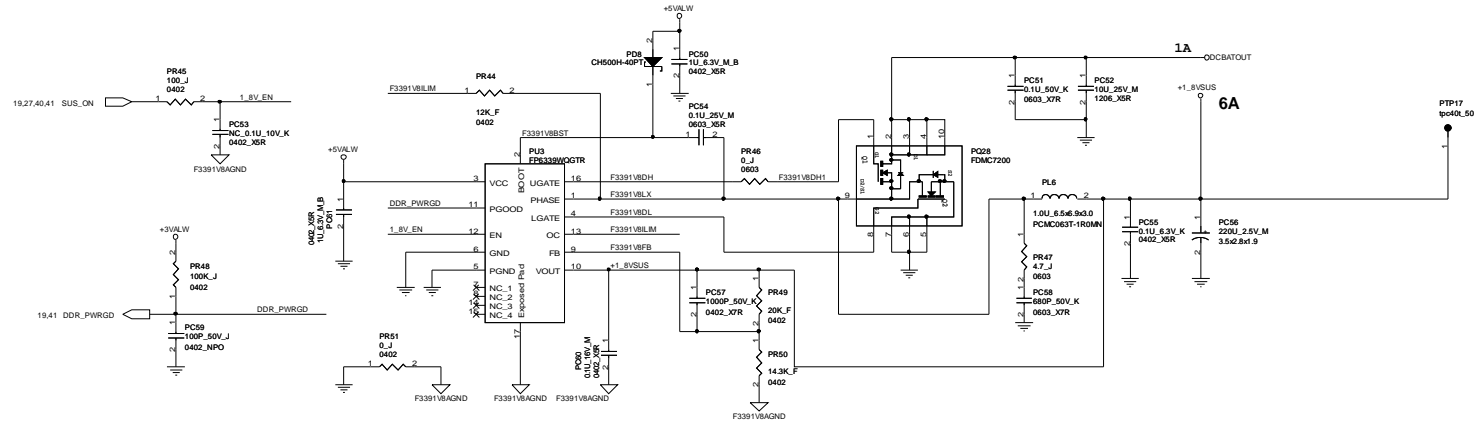
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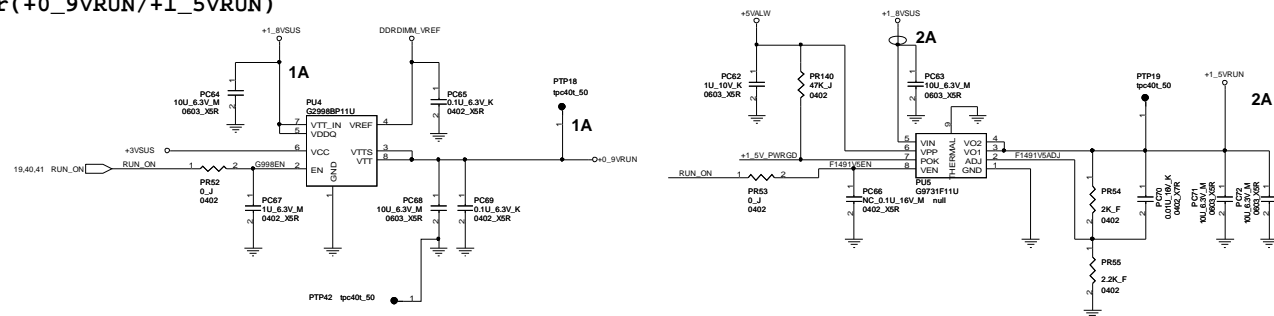
CCPBG

Title		
SYS Power (+3_3V/+5V)		
Size	Document Number	Rev
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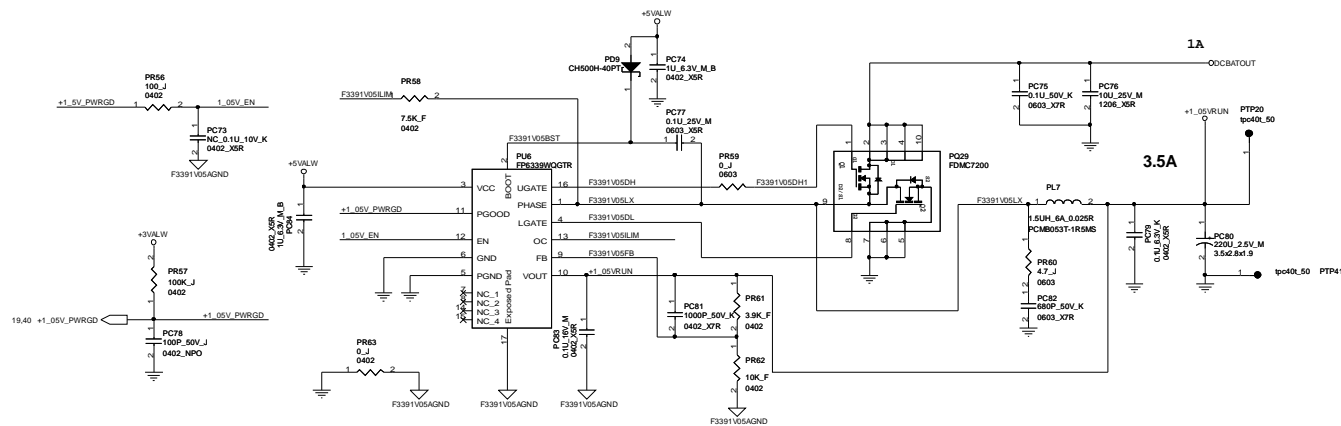
M9F1 SYS Power(+1_8VSUS)



M9F1 SYS Power(+0_9VRUN/+1_5VRUN)



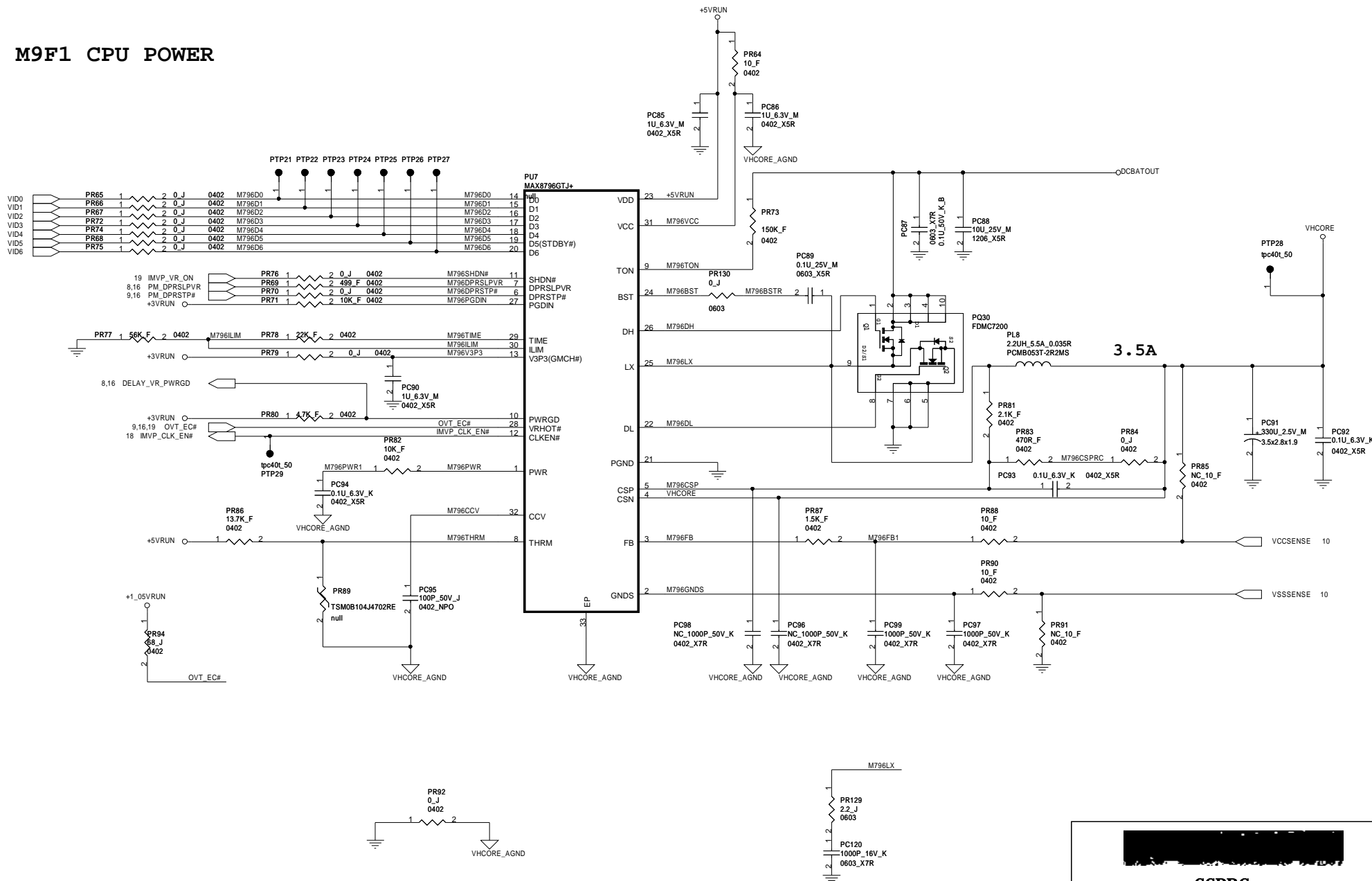
M9F1 SYS Power(+1_05V)



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SYS Power(+1_8V/+1_05V)			
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M9F1 CPU POWER



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CPU POWER

M9F1

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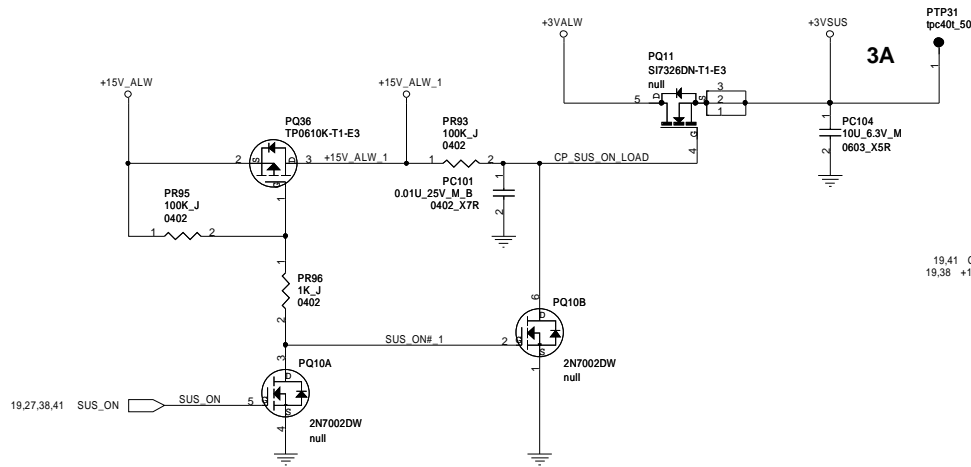
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Date: Wednesday, March 17, 2010

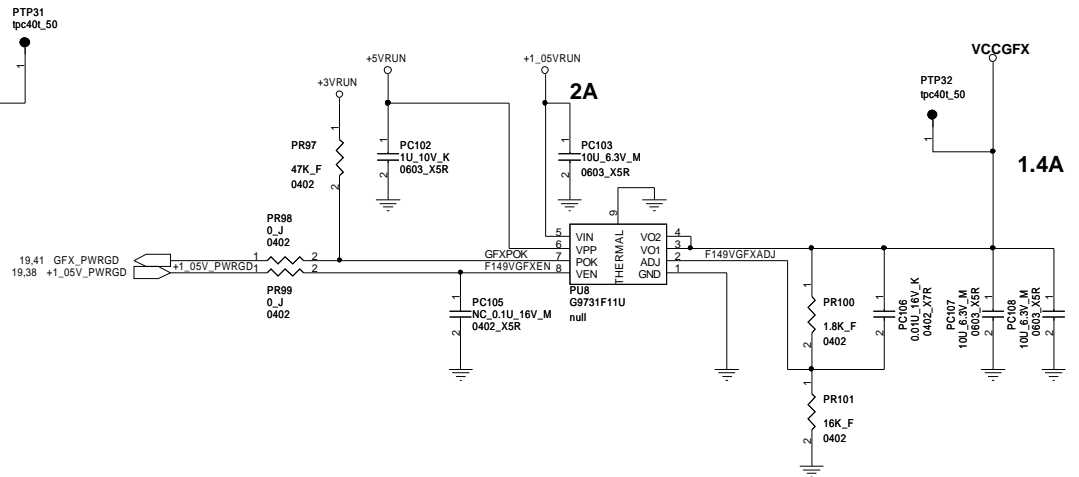
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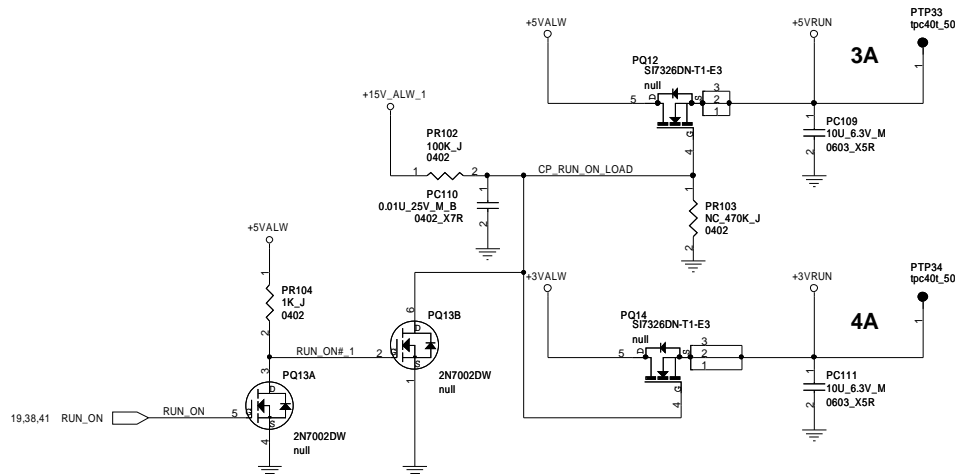
M9F1 Others power plan (+3VSUS)



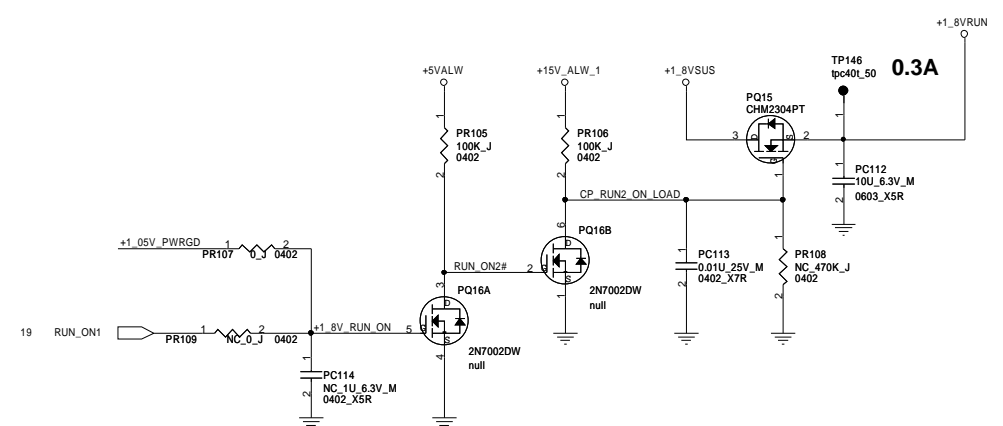
M9F1 GFX Power (VCCGFX/+0.89V)



M9F1 Others power plan (+5V_RUN/+3V_RUN)



M9F1 Others power plan (+1_8V_RUN)



CCPBG

Others power plan

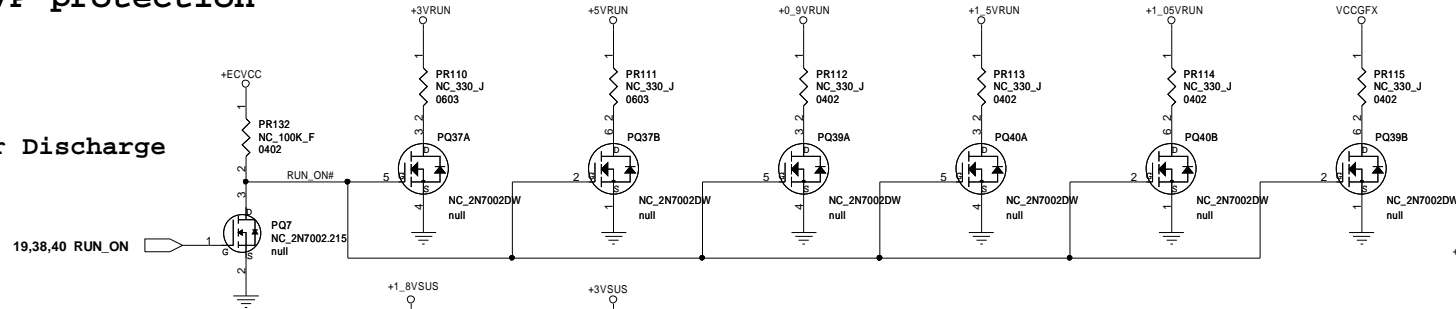
M9F1

Rev 0.1

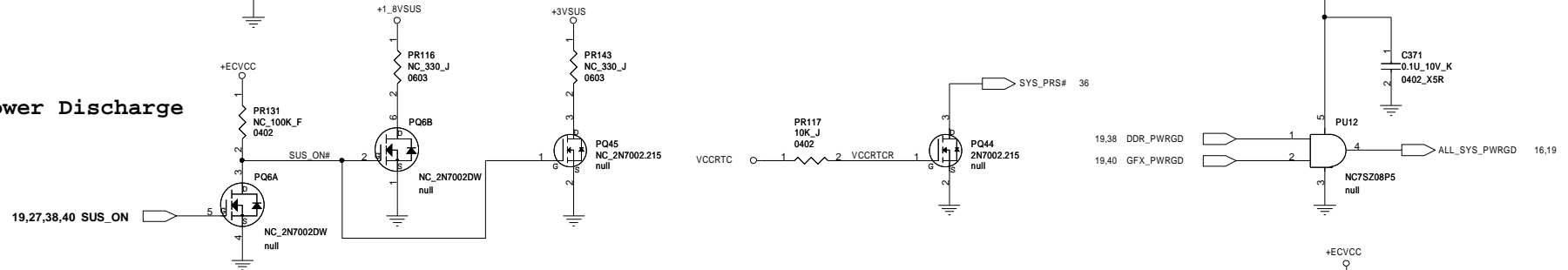
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M9F1 OVP protection

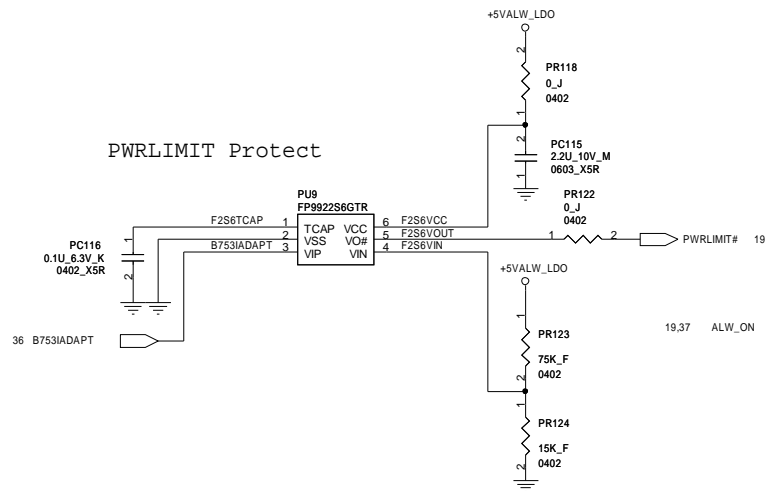
S0 Power Discharge



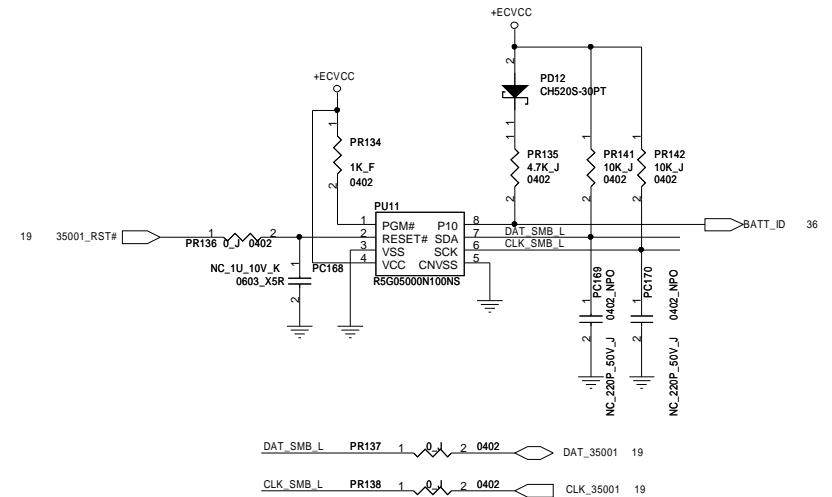
S3 Power Discharge



PWRLIMIT Protect



Battery UVP point 8.5V



CCPBG

OVP protection

M9F1

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M9F1 EVT

2010/01/27

1. P22, Remove net "GND_VGA" and make CN8.9 & CN8.11 no connect
2. P26, Remove net "GND_VGA" and make CN10.16 no connect
3. P26, Delete R407

2010/02/01

1. P21, Change R409 and R410 footprints from 0805 to 1206.
2. P26, Change R406 footprint from 0805 to 1206.

2010/02/02


1. P28, Add U23, Reserve R317 for Lid Switch control LVDS backlight.
2. P19, Delete RF_LED#.
3. P29, Add Q37, D1, Q3, Reserve D2, R411 for wireless LED.
4. P30, Add WWAN_LED#.
5. P31, Delete TP91, TP126.
6. P34, Unconnect H6 to GND.
7. P36, Add PR139, PR144 for powerlimit EC control.
8. P41, NC PC116, PU9, PR118, PC115, PR122, PR123, PR124 for powerlimit EC control.
9. P19, Add C720.
10. P40, Change PQ11, PQ12, PQ14 to SI7326DN-T1-E3.
11. U39 Co-layout with U12.

2010/02/03

1. P19, Add C721.
2. P36, Add PR145, PR146.
3. P36, Change PR18 to 160K.
4. P19, Change EC_VADAPT to U5.100, BT_WLAN_SW# to U5.124.
5. P21, Reserve C381, C386, C387, C388, C389, C390, C391, C392, C393.
6. P29, Delete D2.
7. P30, Delete WWAN_LED#.
8. P37, Stuff PC39, NC PC122.
9. P28, NC CN15.32, CN15.34.

2010/02/04

1. P29, Change R411 to 100K.

			
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M9F1 DVT

2010/02/05

1. P26, Change U13, U14 to 14-NC7S212-5P00.

2010/02/10

1. P19, Add R233 to reserve one GPIO for BT_WLAN_SW# (default NC, use U5.100 to be wireless switch)
2. P19, Add R357 and R359 to reserve U5.100 for wireless switch and power limit (default R357 is 0ohm and R359 is NC)
3. P19, set C720 and C721 to be NC.
4. P16, stuff PU9, PC116, PR118, PC115, PR123 and PR124 for hardware power limit
5. P41, Set R136 and R138 to be NC, and set R270 and R272 to be 10K. MB ID = 00 for M9F1

2010/02/22

1. P20, Delete U39
2. P28, CN15.32 and CN15.34 connects to GND.
3. P16, Change CN2 to 1N-0002009-M1T0.
5. P34, Delete SPR1.
6. P36, Change PCN2 to 2N-000700Y-MKG0.
7. P29, Change R411 to 2K.

2010/02/23

1. P41, NC PR132, PR110, PR111, PR112, PR113, PR114, PR115, PR131, PR116, PR143, PQ7, PQ37, PQ39, PQ40, PQ6, PQ45.



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DVT Change Note

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M9F1 PVT

2010/03/11

1. P24, Change JSPK1 to 1N-000400C-M1T0.
2. P31, Change U17 to 15-AT52083-0000, change R358 to L25 .
3. P20, Change CN3 to 1N-0006004-FXT0.
4. P28, Change CN15.23 from GND to NC.
5. P28, Change L23, L24 to R412, R413.
6. P36, Delete PR139.
7. P19, Change R357 to close jump.
8. P26, Add C335, C722.
9. P21, Change R398, R399, R400, R401, R402, R403, R404, R405 to 56ohm.

2010/03/12


1. P19, Stuff R342, R345 for system ID.
2. P25, Reserve CAP9.
3. P10, Reserve D34, D35, D36.

2010/03/15

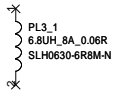
1. P26, C722 change to C336
2. P24, JSPK1 changes net name for speaker pin compatible
3. P37, Add PC124, PC125, PC126 and PC127 for EMC
4. P18, Add R390, R391.
5. P25, Change CAP9 to 1C-44R0476-M200.
6. P21, Change R409, R410 to stuff.

2010/03/15

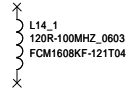
1. P28, Change F6 to 1M-F6V0A75-0002, NC R337.
2. P18, Change R390, R391 to 33ohm.

		
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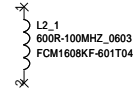
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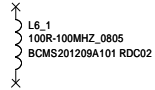
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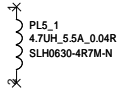
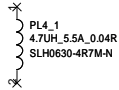
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L1

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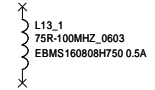
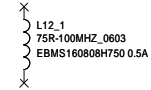
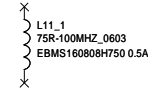
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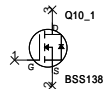
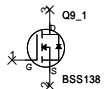
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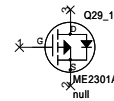
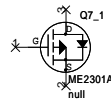
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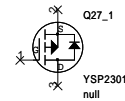
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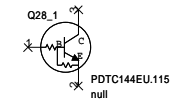
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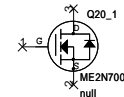
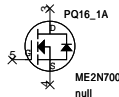
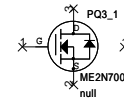
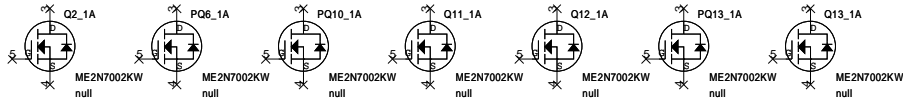


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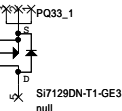
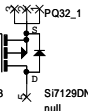
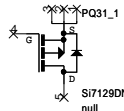


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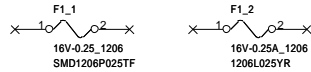


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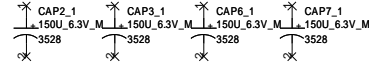
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F9

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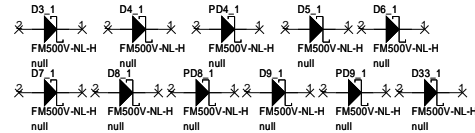
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PD5, PD6

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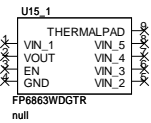
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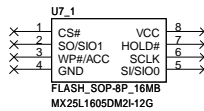
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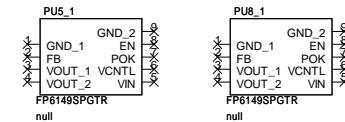
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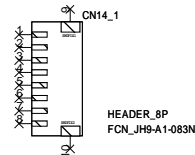
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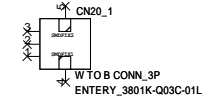
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