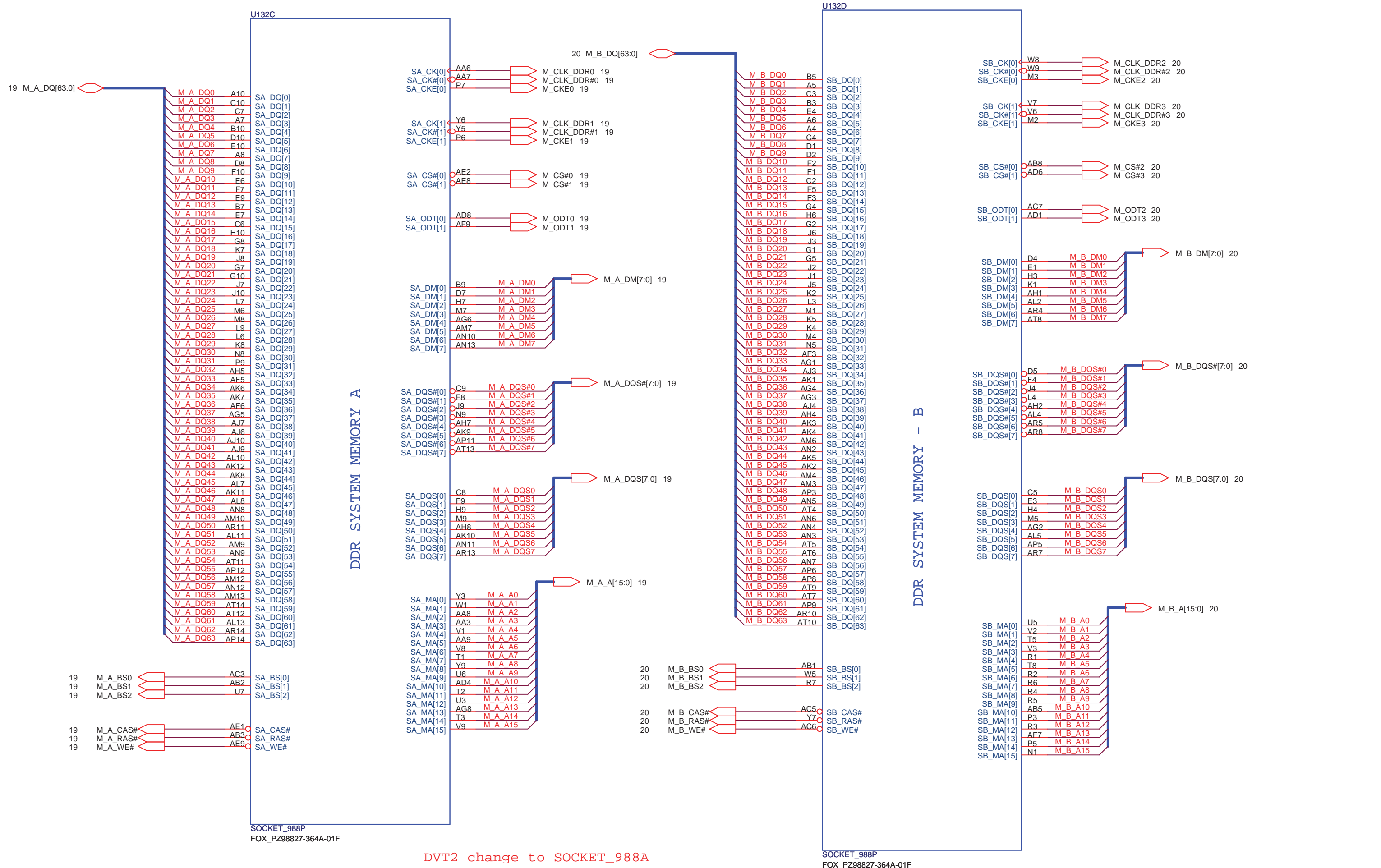


For Disable Arrandale Graphic  
In addition, FDI\_RXN[7:0] and FDI\_RXP[7:0] can be left floating on the PCH.  
FDI\_TX[7:0] and FDI\_TX#[7:0] can be left floating on the Arrandale. The FDI\_FSXNC[0], FDI\_FSXNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

DVT2 change to SOCKET\_988A

```
2009.10.19
Change RP81 TO NC
Change RP82 TO mount
```



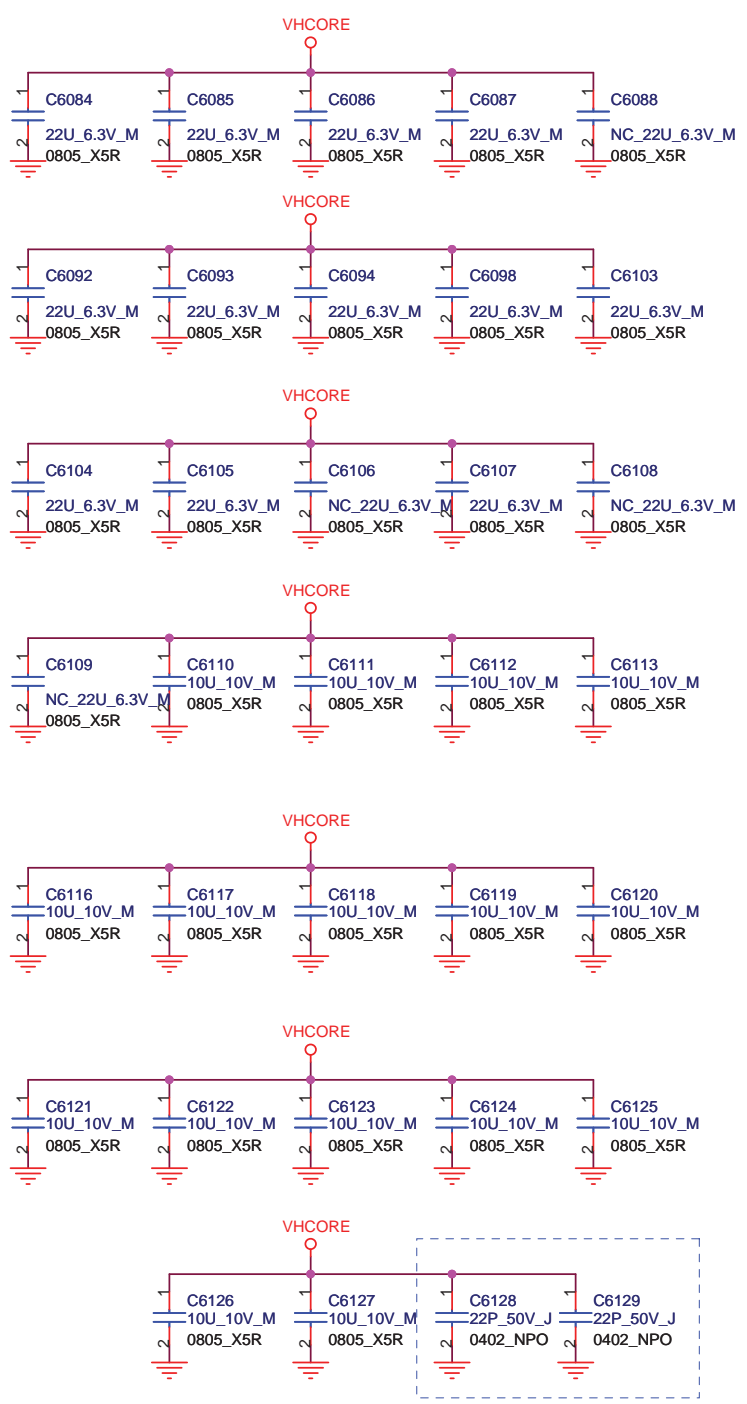


DVT2 change to SOCKET\_988A



2008-09-12  
Delete R5785 0ohm resistor for voltage drop problem

### 48A (ARD SV)



For RF Noise

### VHCORE

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

SOCKET\_988P  
FOX\_PZ98827-364A-01F

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

- VTT0\_1 AH14
- VTT0\_2 AH12
- VTT0\_3 AH11
- VTT0\_4 AH10
- VTT0\_5 J14
- VTT0\_6 J13
- VTT0\_7 H14
- VTT0\_8 H12
- VTT0\_9 G14
- VTT0\_10 G13
- VTT0\_11 G12
- VTT0\_12 G11
- VTT0\_13 F14
- VTT0\_14 F13
- VTT0\_15 F12
- VTT0\_16 F11
- VTT0\_17 F14
- VTT0\_18 F12
- VTT0\_19 D14
- VTT0\_20 D13
- VTT0\_21 D12
- VTT0\_22 C14
- VTT0\_23 C13
- VTT0\_24 C12
- VTT0\_25 C11
- VTT0\_26 B14
- VTT0\_27 B12
- VTT0\_28 A14
- VTT0\_29 A13
- VTT0\_30 A12
- VTT0\_31 A11

- PSI# AN33
- VID[0] AK35
- VID[1] AK33
- VID[2] AK34
- VID[3] AL35
- VID[4] AL33
- VID[5] AM33
- VID[6] AM35
- PROC\_DPRS LPVR AM34
- VTT\_SELECT G15

- ISENSE AN35
- VCC\_SENSE AJ34
- VSS\_SENSE AJ35
- VTT\_SENSE B15
- VSS\_SENSE\_VTT A15

PSI#	PSI#	53,54
VID[0]	AK35	VID0 53,54
VID[1]	AK33	VID1 53,54
VID[2]	AK34	VID2 53,54
VID[3]	AL35	VID3 53,54
VID[4]	AL33	VID4 53,54
VID[5]	AM33	VID5 53,54
VID[6]	AM35	VID6 53,54
PROC_DPRS LPVR	AM34	PM_DPRS LPVR 53,54

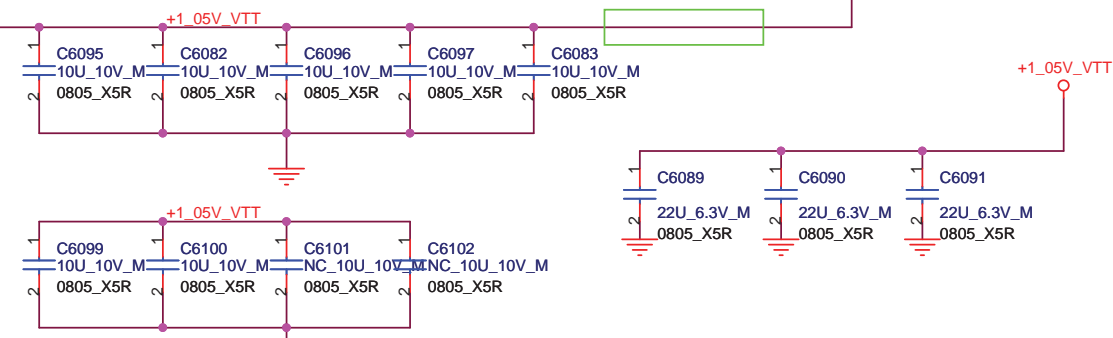
VTT\_SELECT G15 TP689 20MIL

ISENSE AN35 IMVP\_IMON 53

VCC\_SENSE AJ34 VCCSENSE 53  
VSS\_SENSE AJ35 VSSSENSE 53

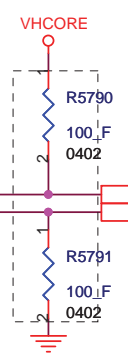
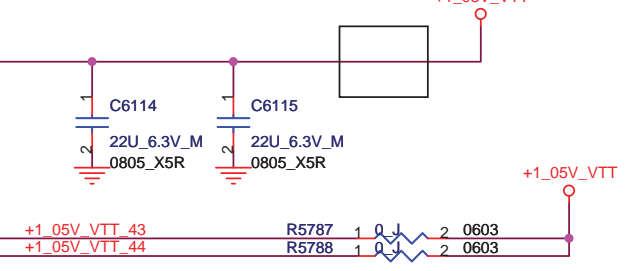
VTT\_SENSE B15 VTT\_SENSE 58  
VSS\_SENSE\_VTT A15 TP581 20MIL

### 18A(ARD SV) (VTT)



2009.10.23  
Delete R5786 for PVT

### 18A(ARD SV) (VTT)

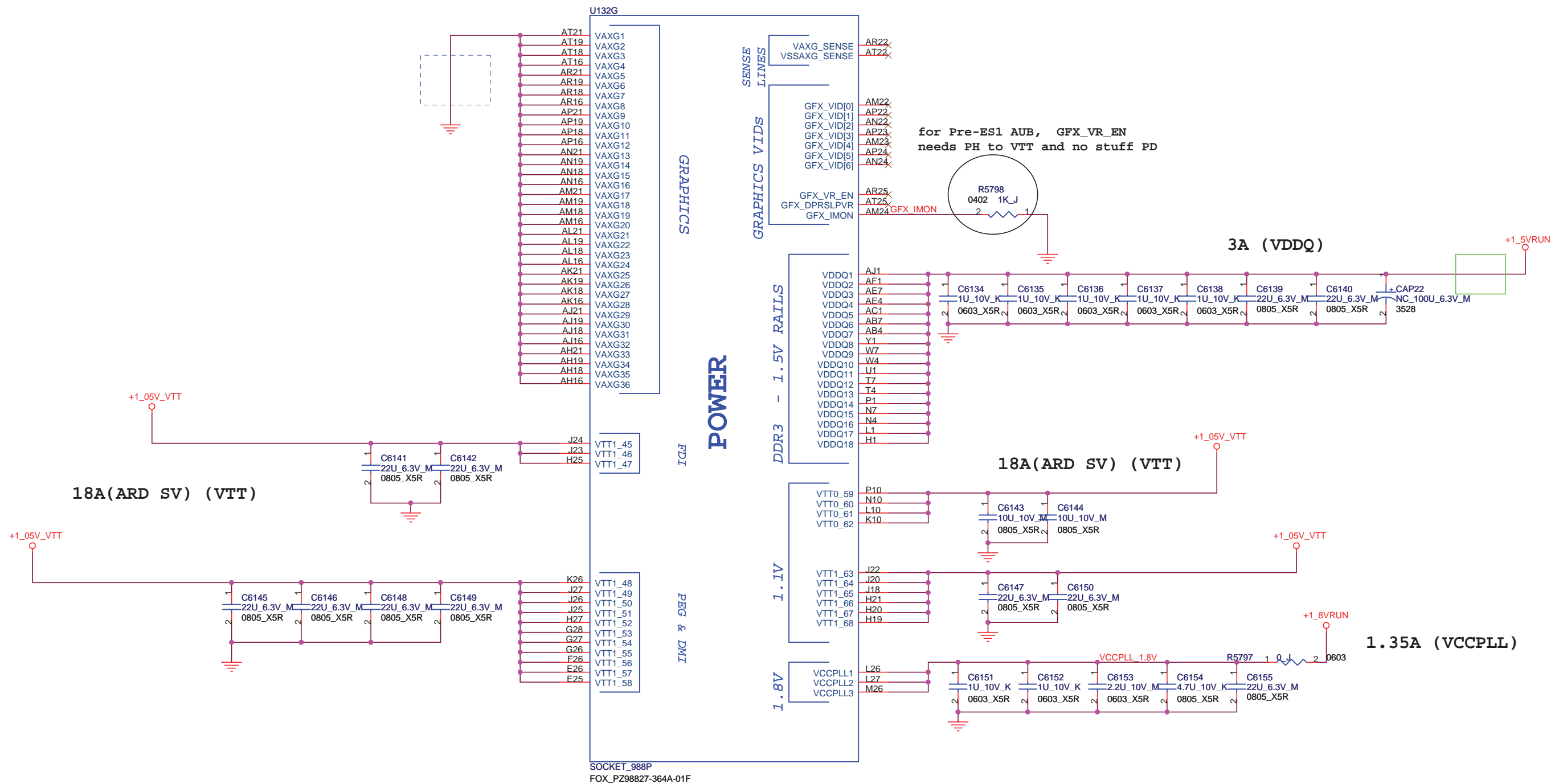


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		ARD(POWER)	
Size	Document Number	Rev	1.1
Custom	M9A0 MP	Date:	Wednesday, October 28, 2009
Sheet		5	of 73

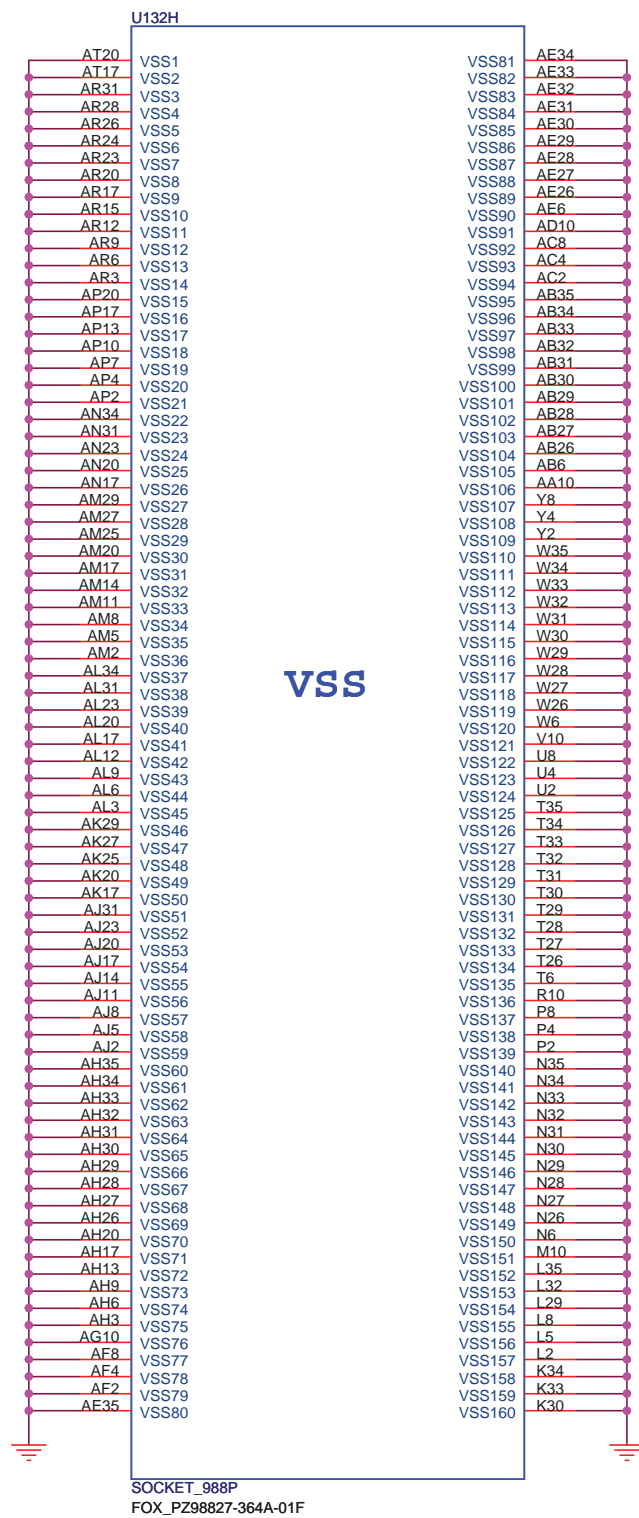
DVT2 change to SOCKET\_988A

For Disable Arrandale Graphic  
VAXG should be connected to GND when disable iGPU.

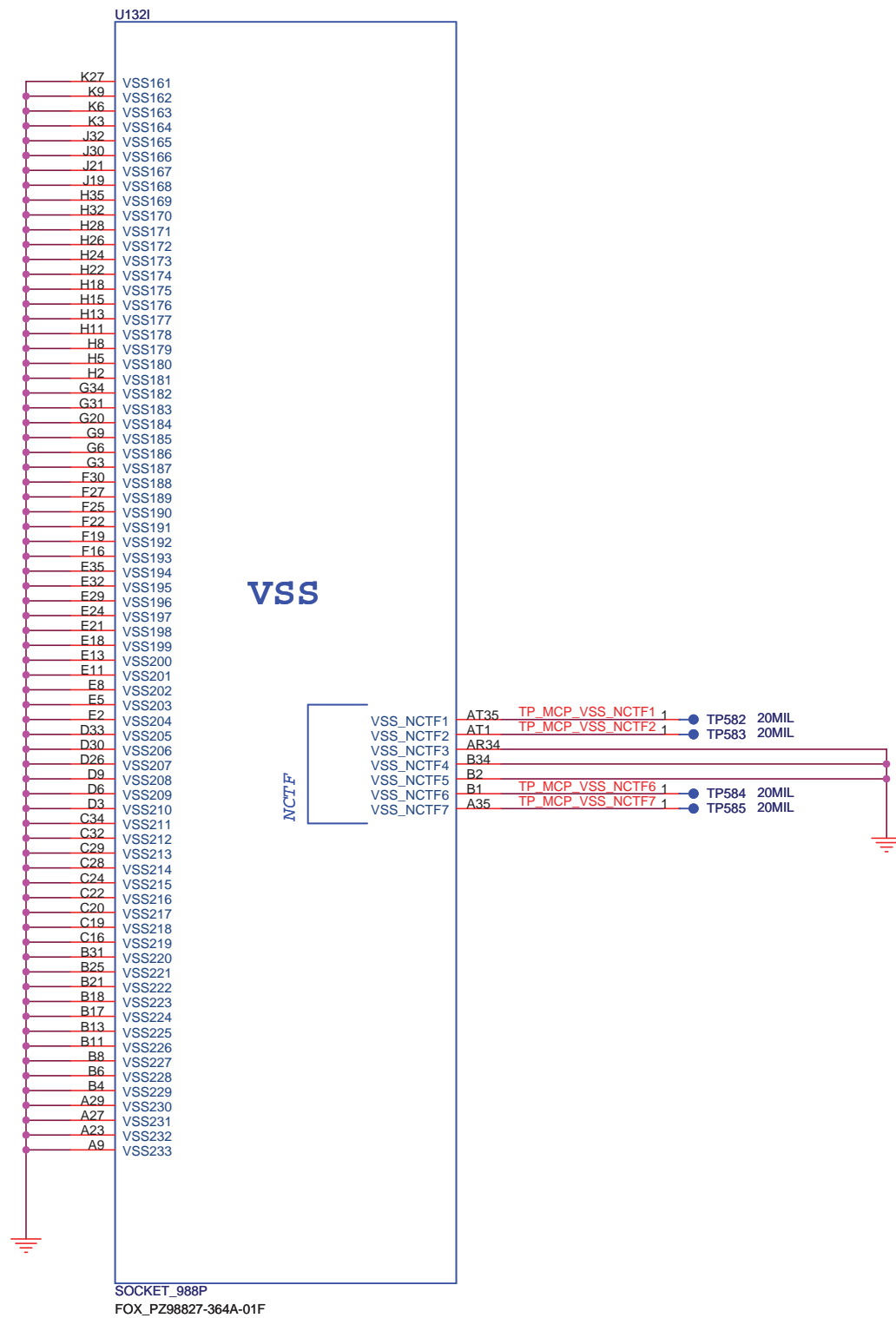
For Disable Arrandale Graphic  
VAXG\_SENSE and VSSAXG\_SENSE on Arrandale can be left as no connect.



DVT2 change to SOCKET\_988A



DVT2 change to SOCKET\_988A

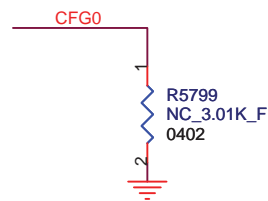


```
PCI Express Configuration Select
CFG0      1 : Single PEG      * default
          0 : Bifurcation enable
```

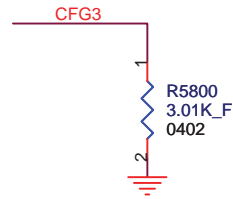
3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount

The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

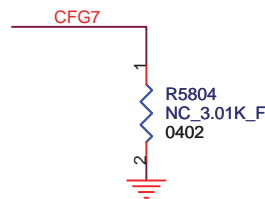
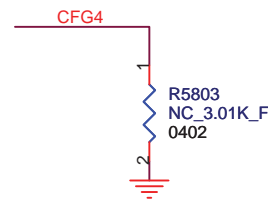
CFG pin is latch on the rising edge of CPU powergood.



```
CFG3      PCI Express Static Lane
Reversal
CFG3      1 : Normal
0 : Lane Numbers Reversed  *
      15 -> 0 , 14-> 1 , ...
```

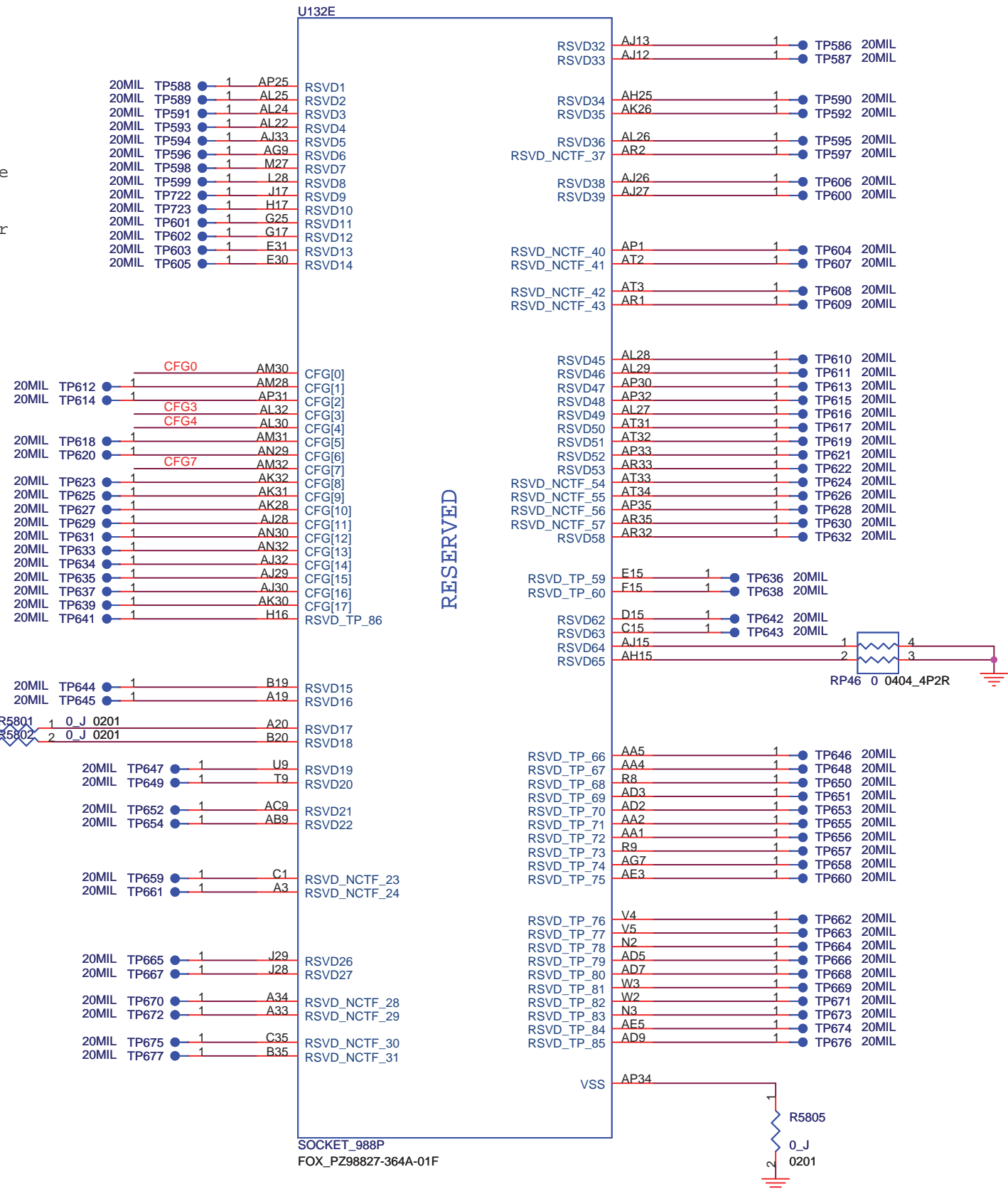


```
CFG4      Display Port Presence
CFG4      1 : Disabled ; No Physical Display Port
           attached to Embedded Display Port
           0 : Enable ; An external Display Port device
           is connected to the Embedded Display Port
```



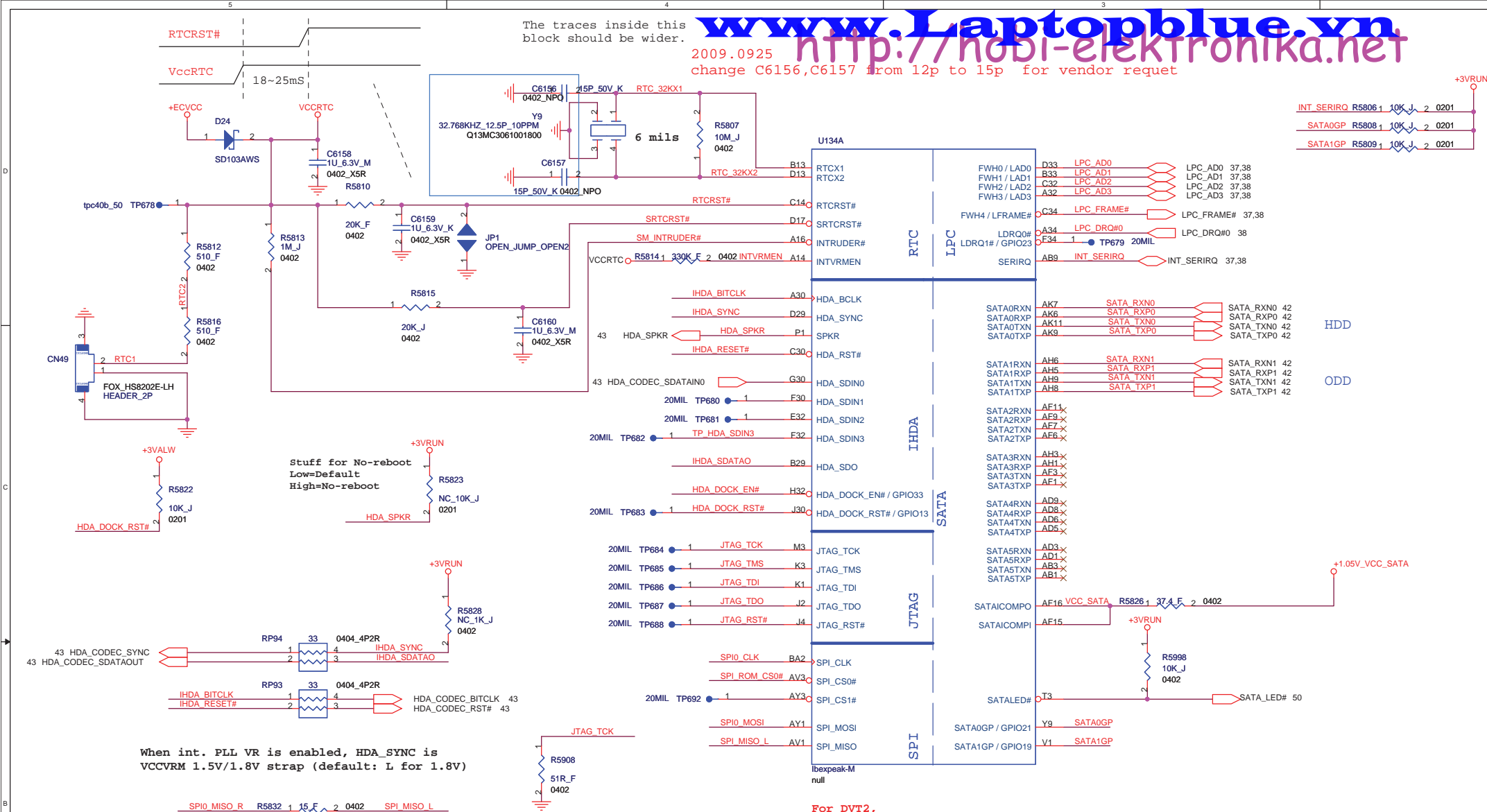
## 2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



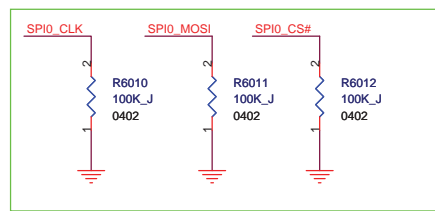
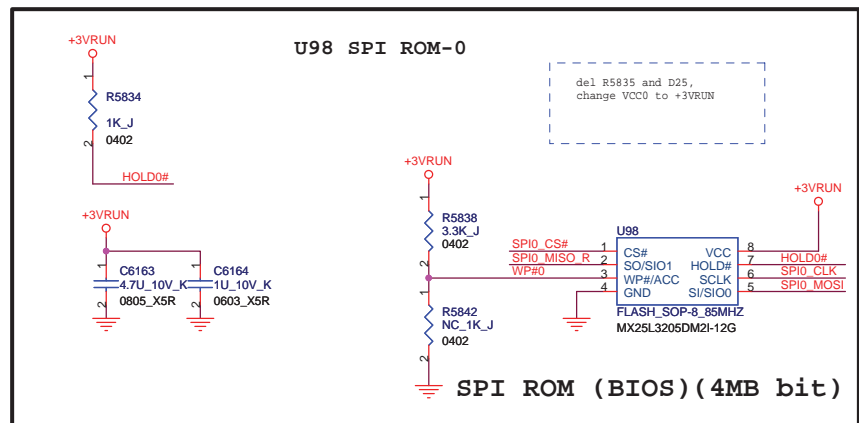
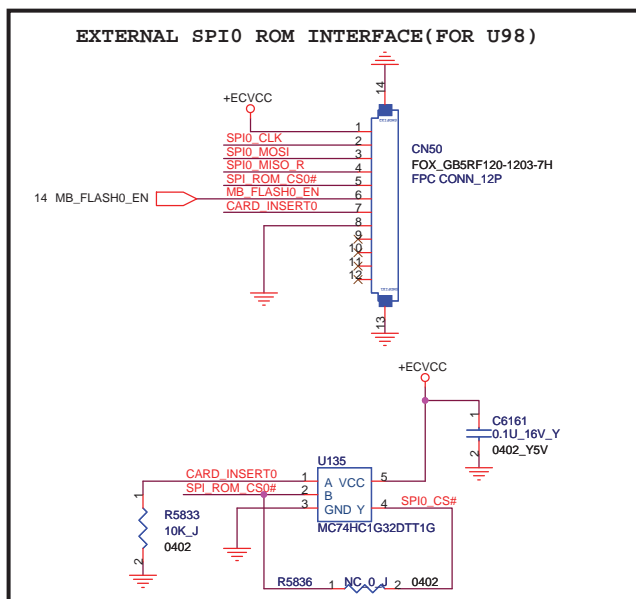
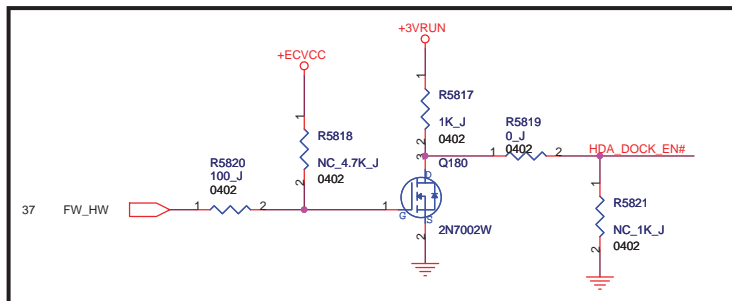
DVT2 change to SOCKET\_988A





[HDA\_DOCK\_EN#/GPIO33]

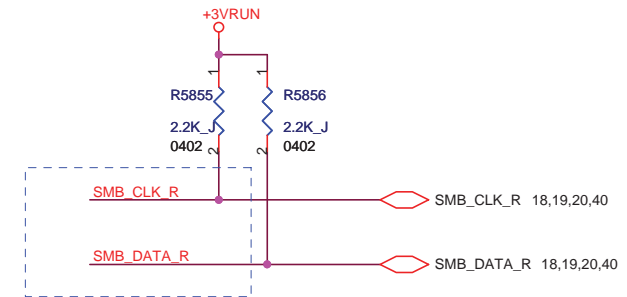
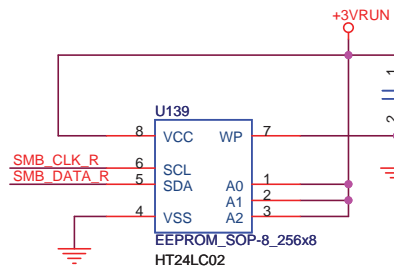
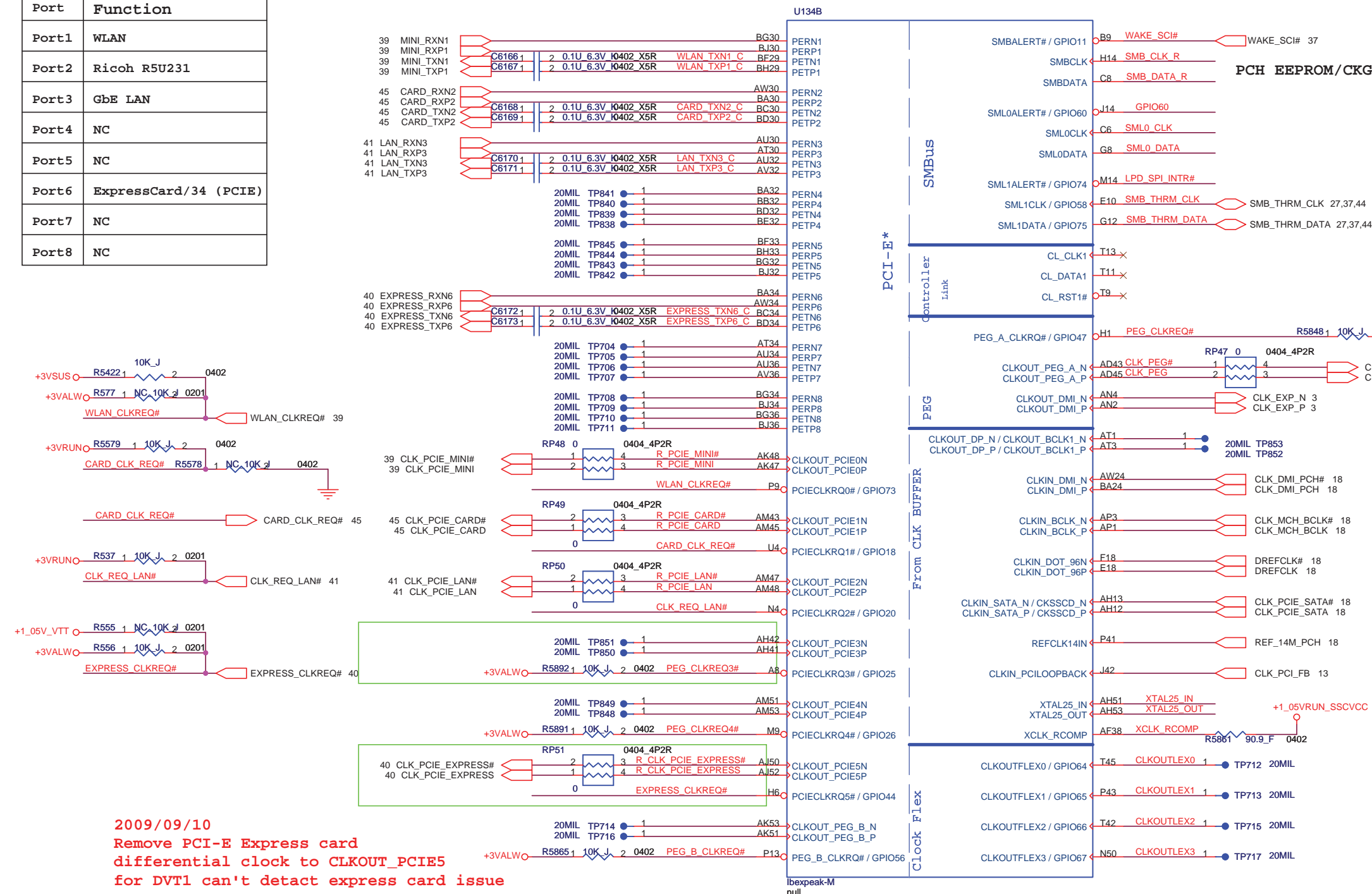
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.  
High (1) - Security measure defined in the Flash Descriptor will be enabled



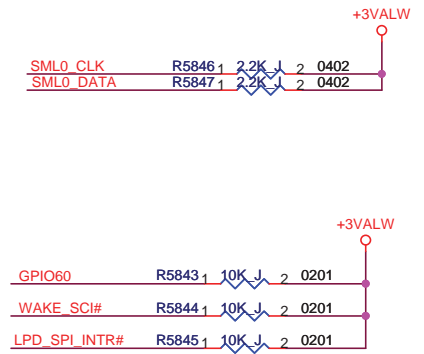
add follow EDS

PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCI-E)
Port7	NC
Port8	NC

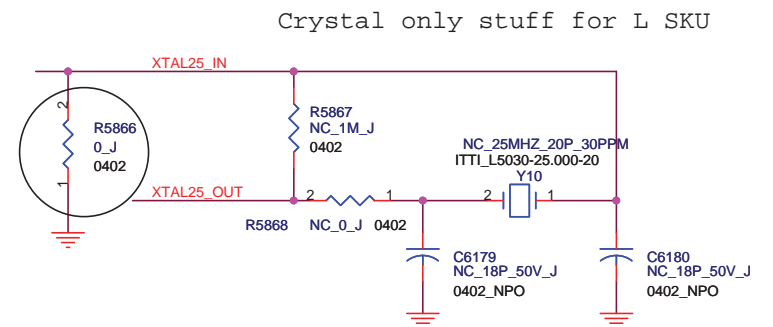


EC/THM/dGPU  
(SMBus Address: 94h, 96h)



From CLK BUFFER

Clock Flex



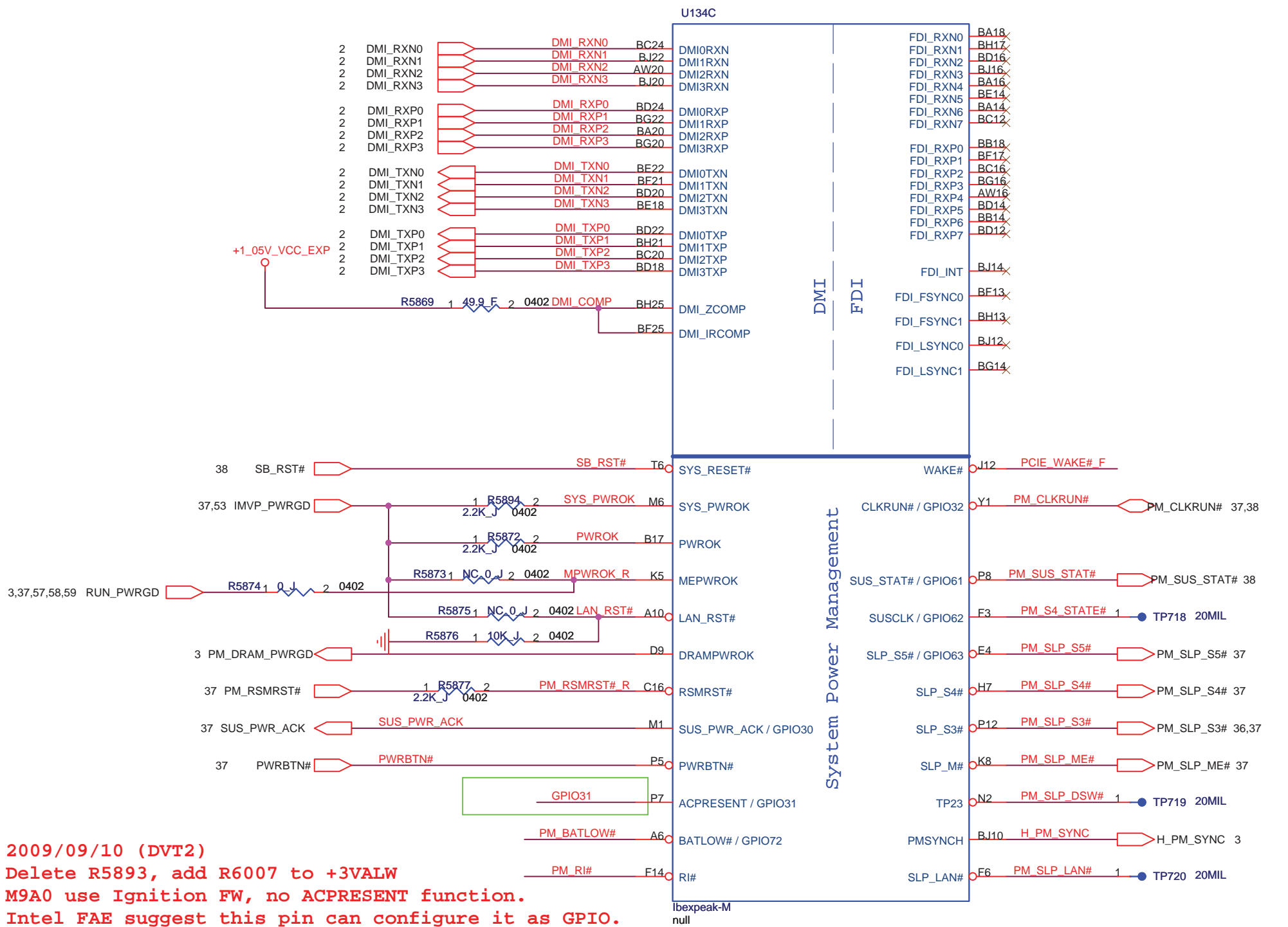
Calpella Platform - Design Guide - Addendum /  
Update - Rev. 1.52 (Doc #414044).).  
XTAL\_IN should be pulled to GND via a 0ohm by  
default.  
This pull-down resistor on XTAL\_IN should only  
be un-stuffed when 25Mhz crystal is used.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		PCH (PCI-E, SMBUS, CLK)	
Size	Document Number	Rev	
Custom	M9A0 MP	1.1	
Date:	Friday, October 23, 2009	Sheet	10 of 73

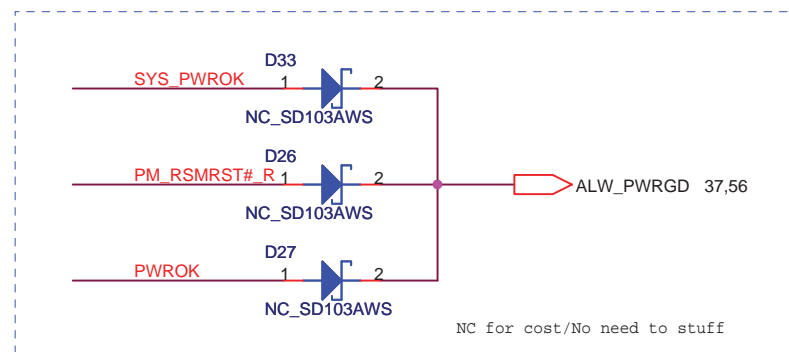
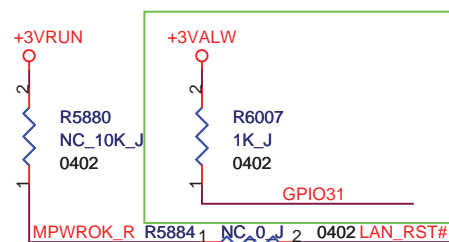
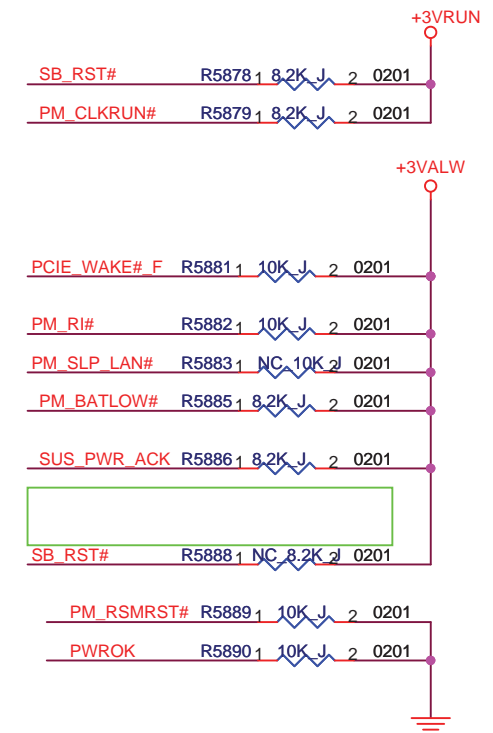
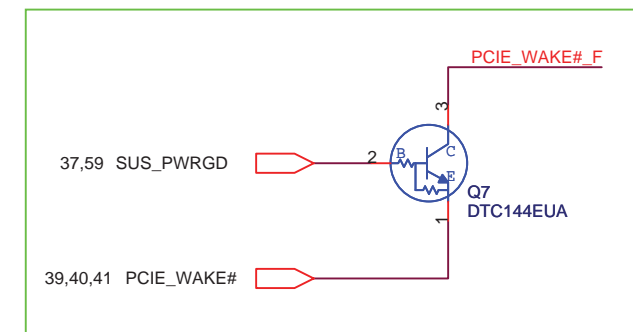
For Disable Auburndale Graphic

In addition, FDI\_RXN[7:0] and FDI\_RXP[7:0] can be left floating on the PCH.

FDI\_TX[7:0] and FDI\_TX#[7:0] can be left floating on the Arrandale. The  
GFX\_IMON, FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT  
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



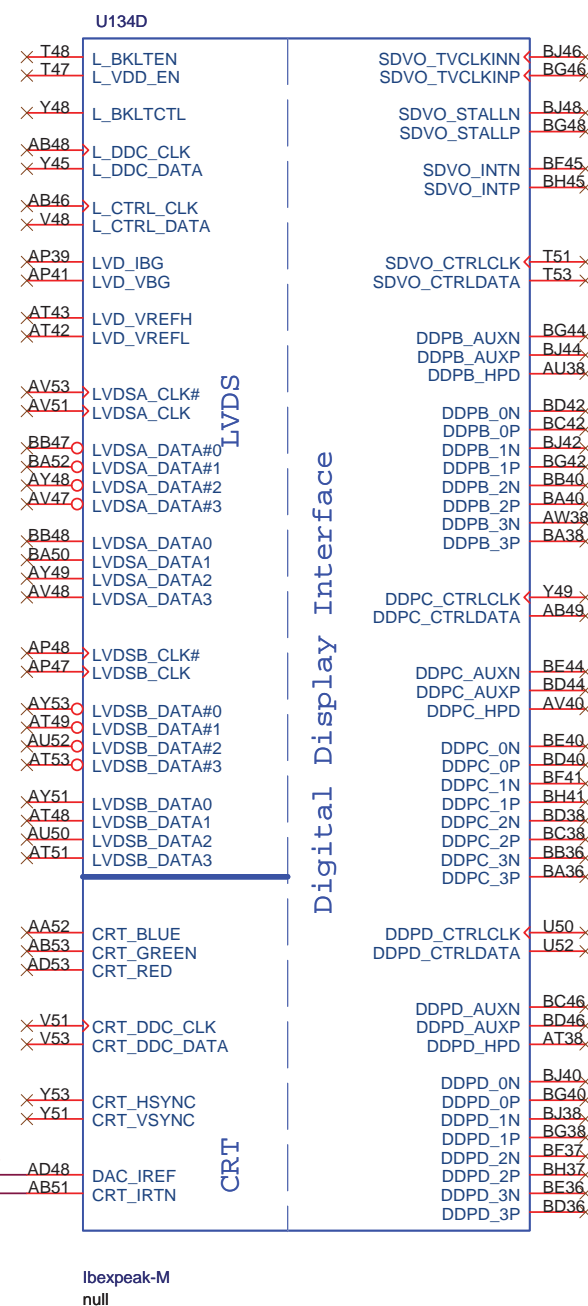
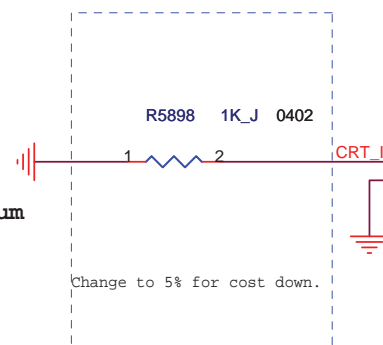
2009.0928  
Add the Q7 as MOR request.



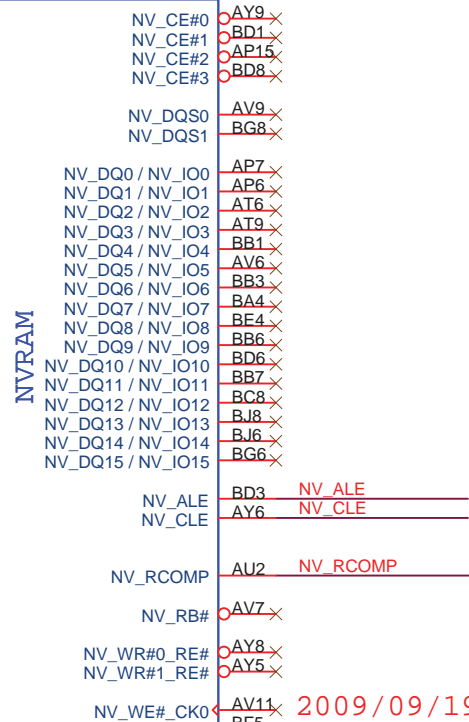
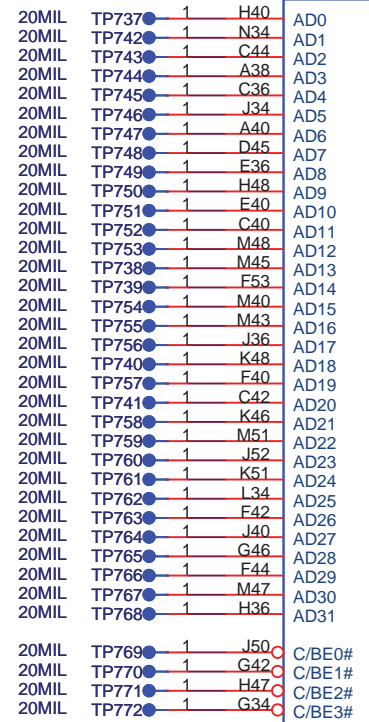
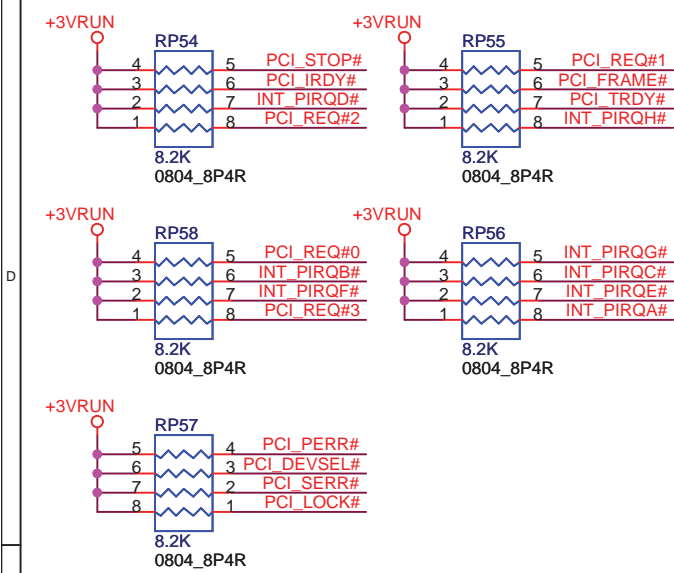
PM\_SLP\_ME# 1 TP721 20MIL

2009/09/10 (DVT2)  
Delete R5887 and Net name AC\_Present  
M9A0 use Ignition FW, no ACPRESENT function.  
Intel FAE suggest this pin can configure it as GPIO.

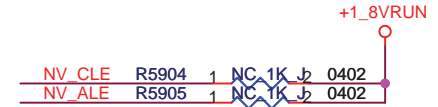
Calpella Platform - Design Guide - Addendum  
/ Update - Rev. 1.52 (Doc #414044).).



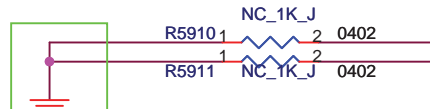
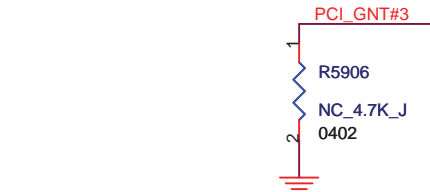




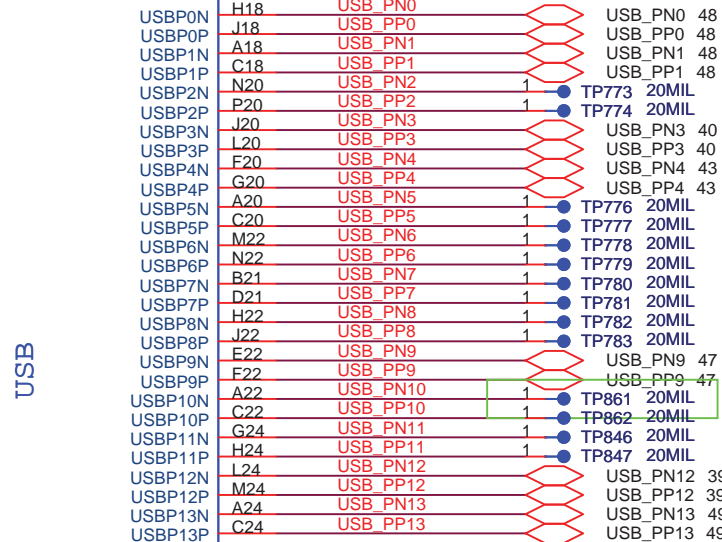
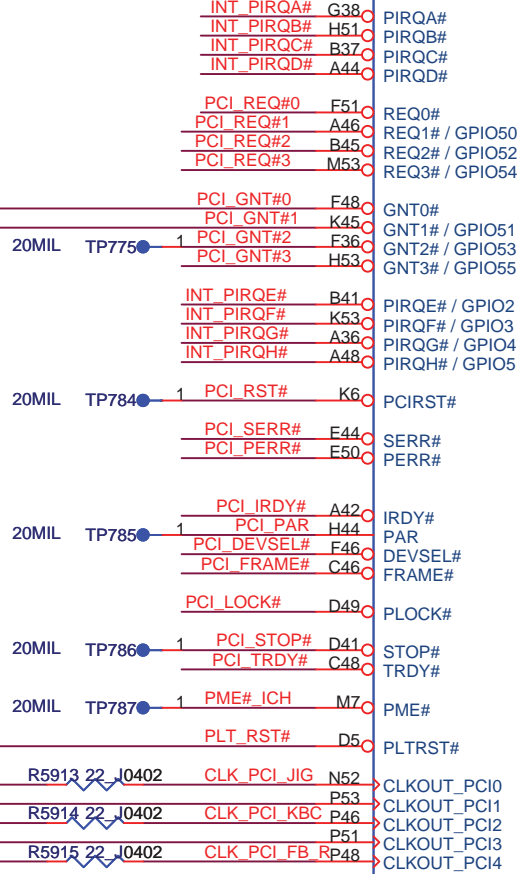
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



Intel Anti-Theft Technology  
Disabled when Low , NC R1616  
Enabled when High , Stuff R1616

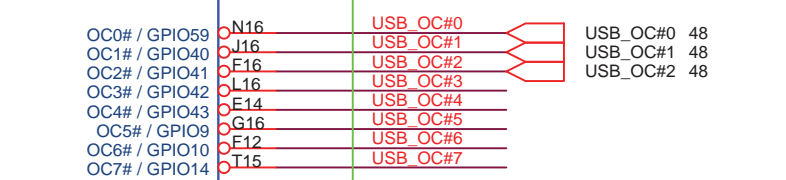
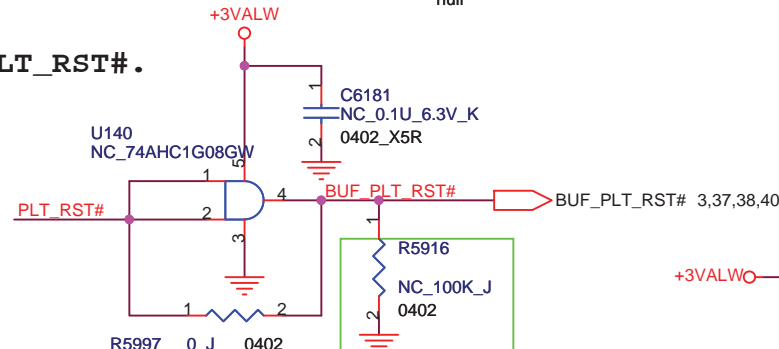


Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required.  
Boot from PCI: Connect GNT1# to ground with 1-k? pull-down resistor. Leave GNT0# Floating.  
Boot from LPC: Connect both GNT0# and GNT1# to ground with 1K? pull-down resistor.

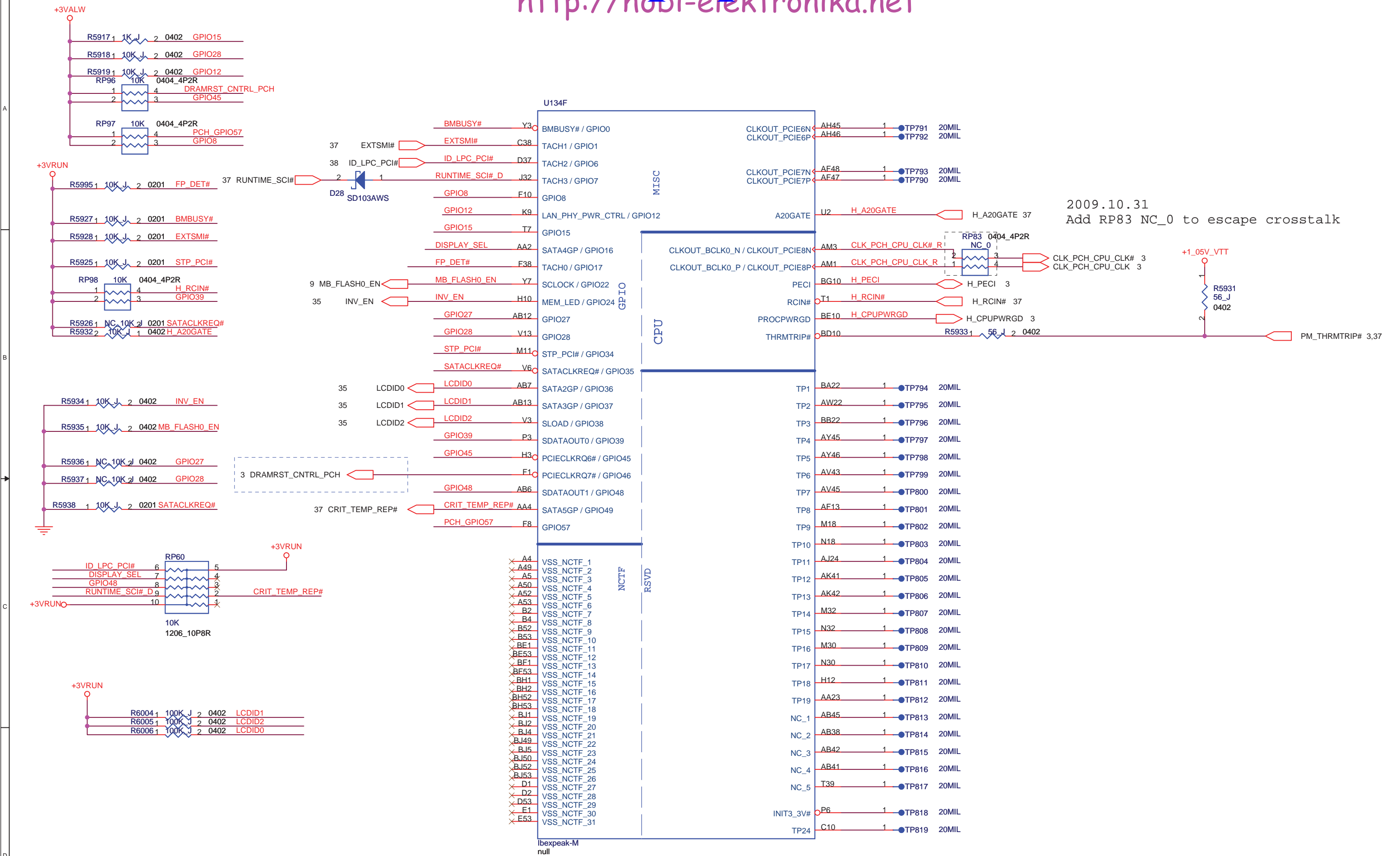


USB PORT	Function
PORT-0	External Port-0
PORT-1	External Port-1
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-2
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	No finger print
PORT-11	
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

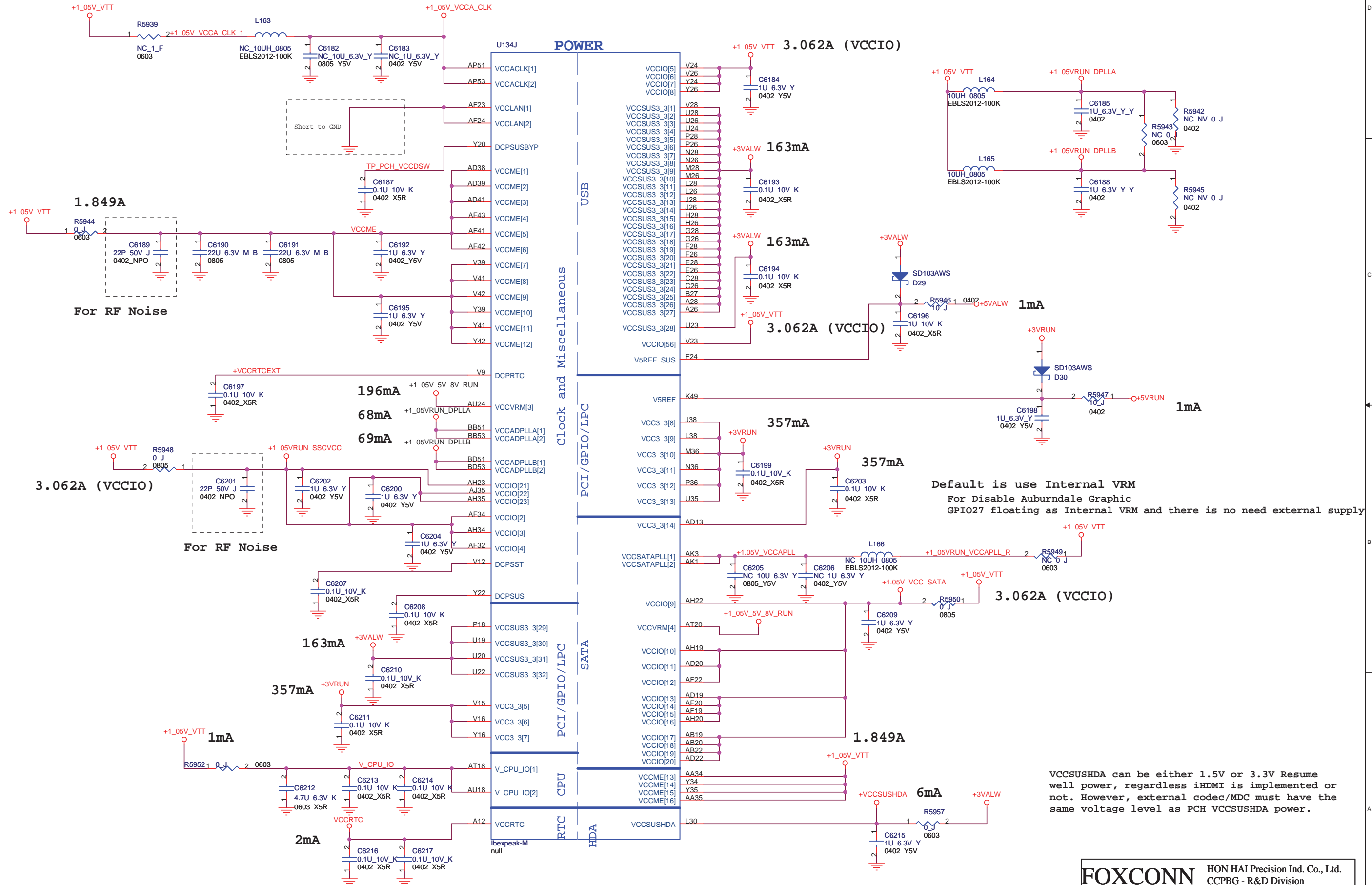
Buffer to reduce loading on PLT\_RST#.



2009/09/19  
Add USB\_OC#1



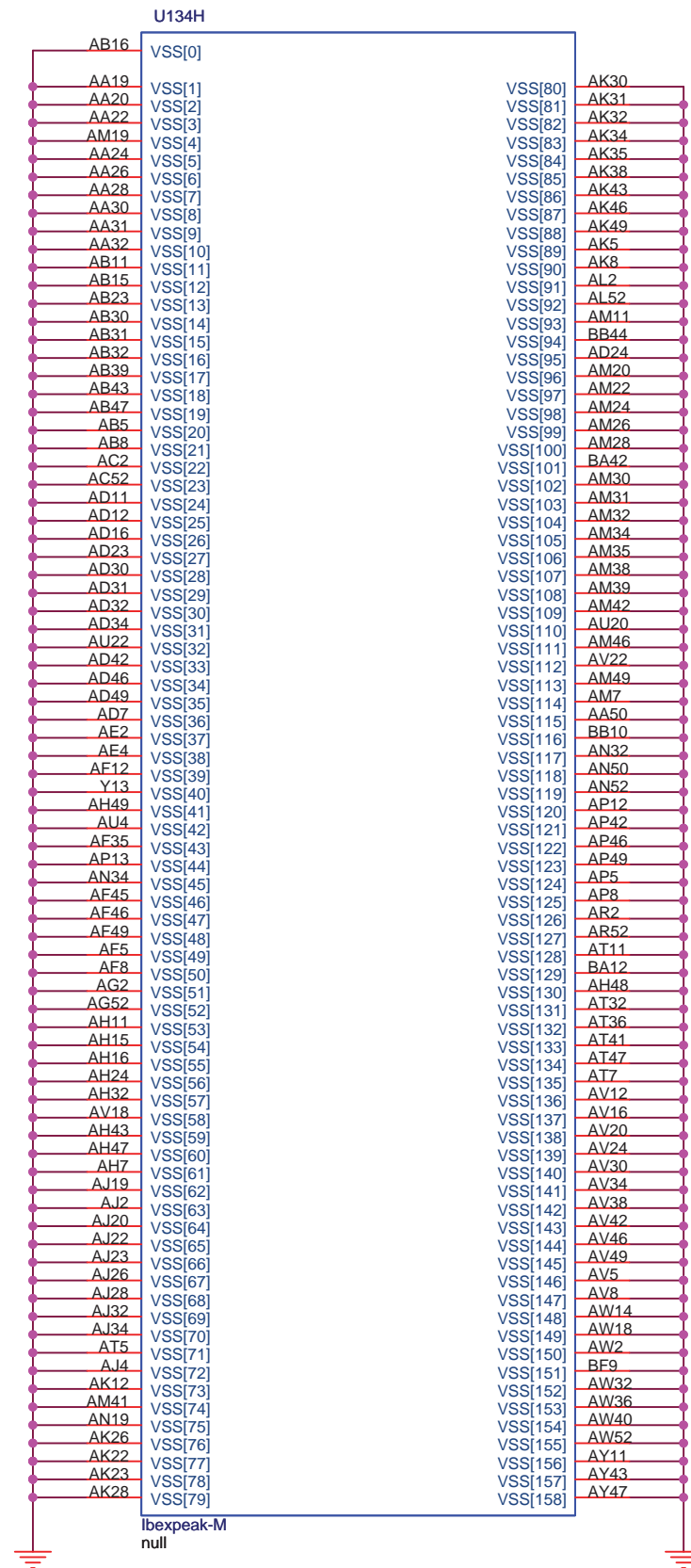
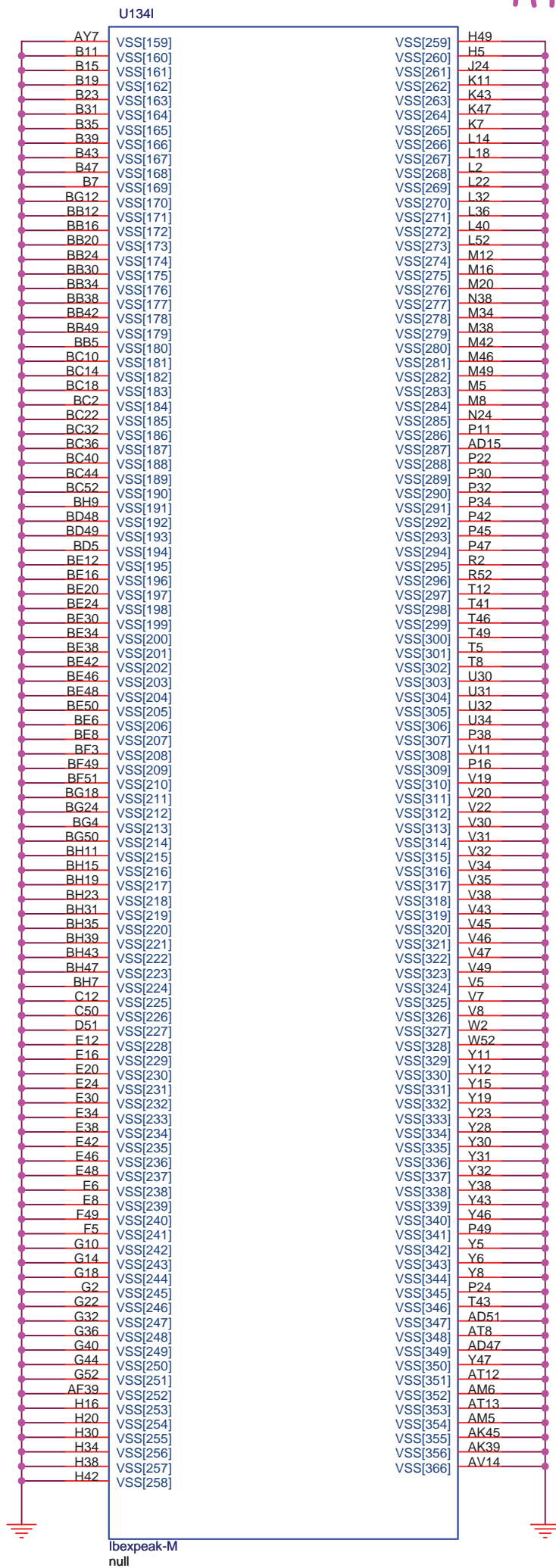
Default is use Internal VRM  
For Disable Auburndale Graphic  
GPIO27 floating as Internal VRM and there is no need external supply



VCCSUS3\_3 can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUS3\_3 power.

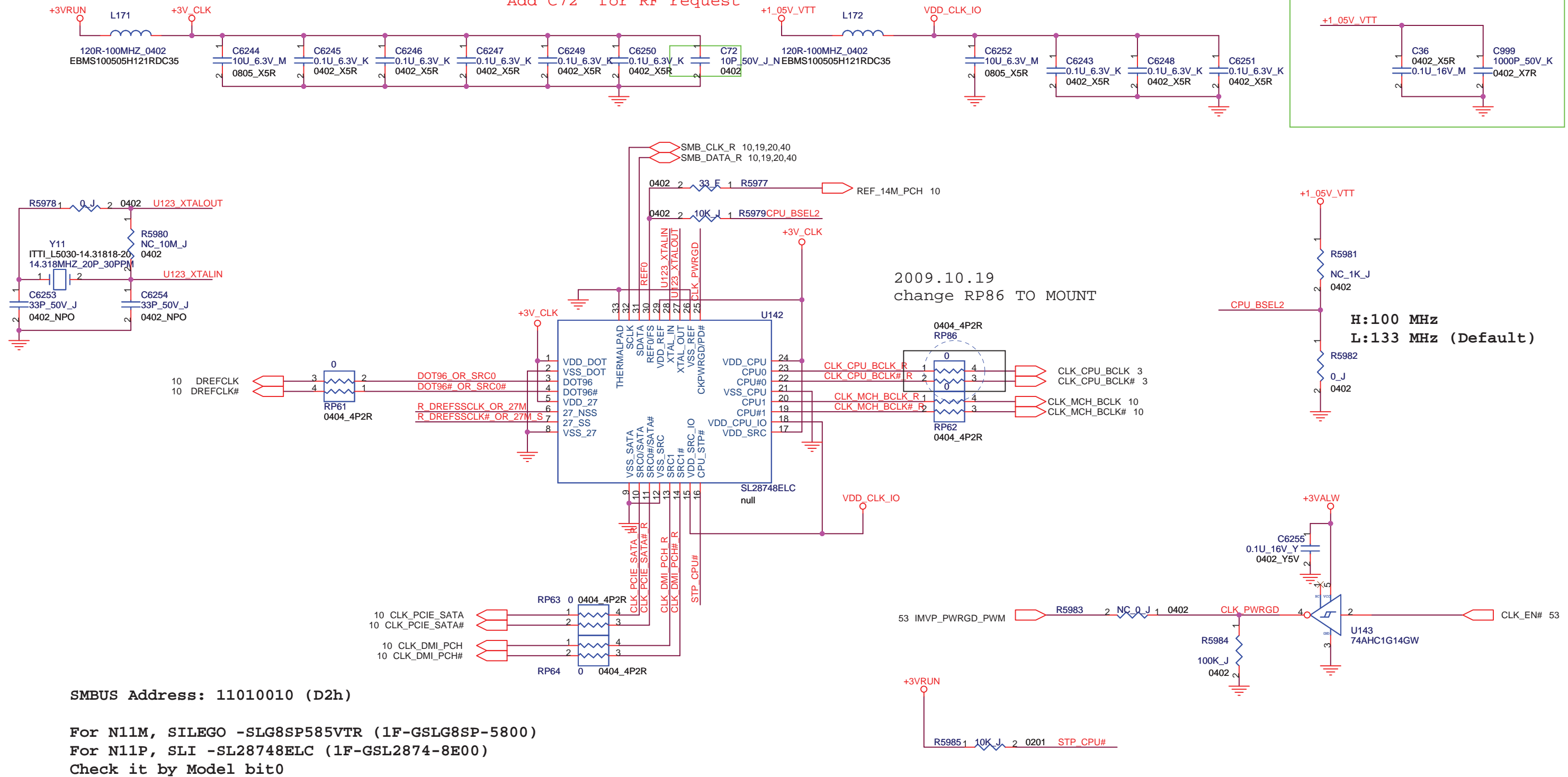


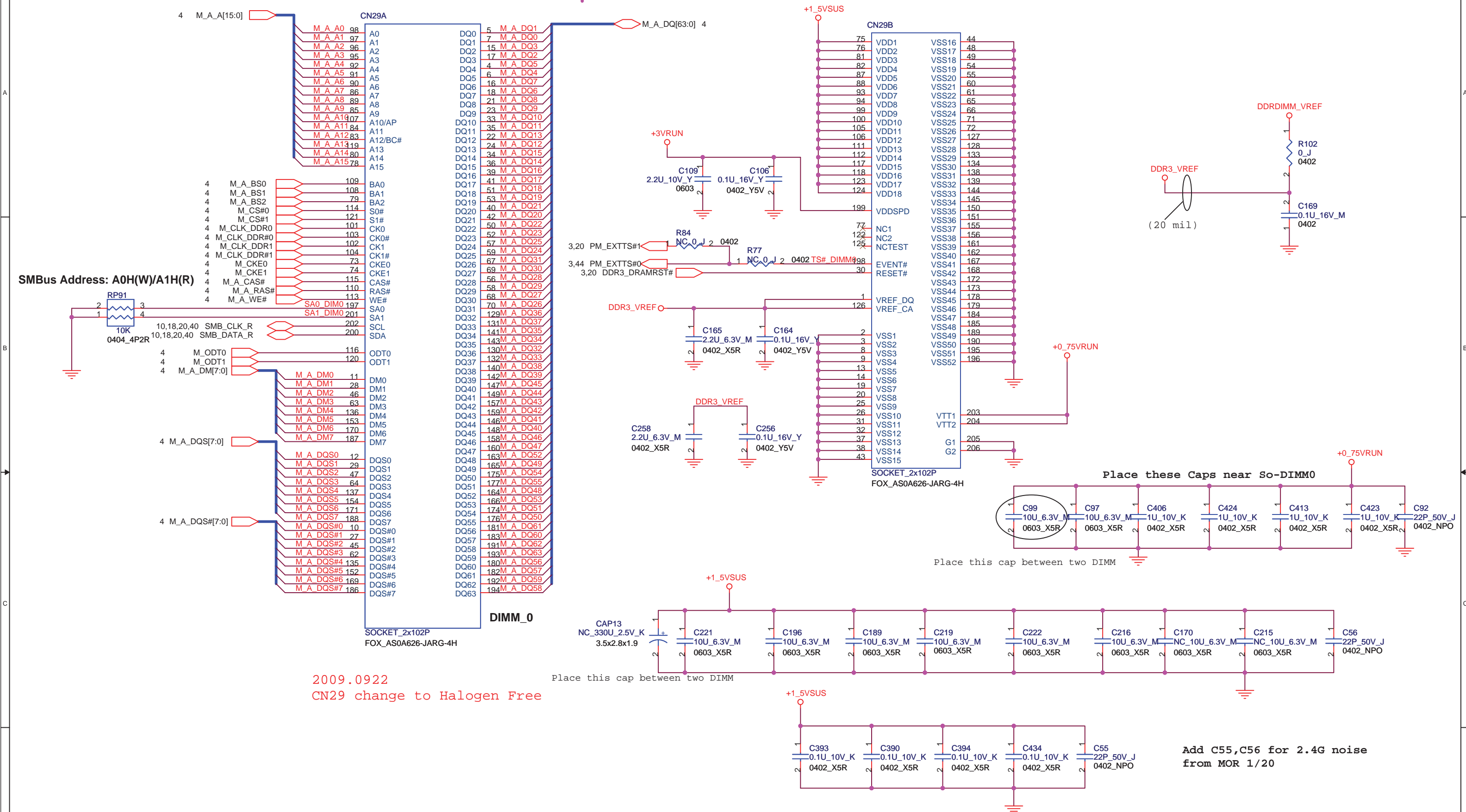


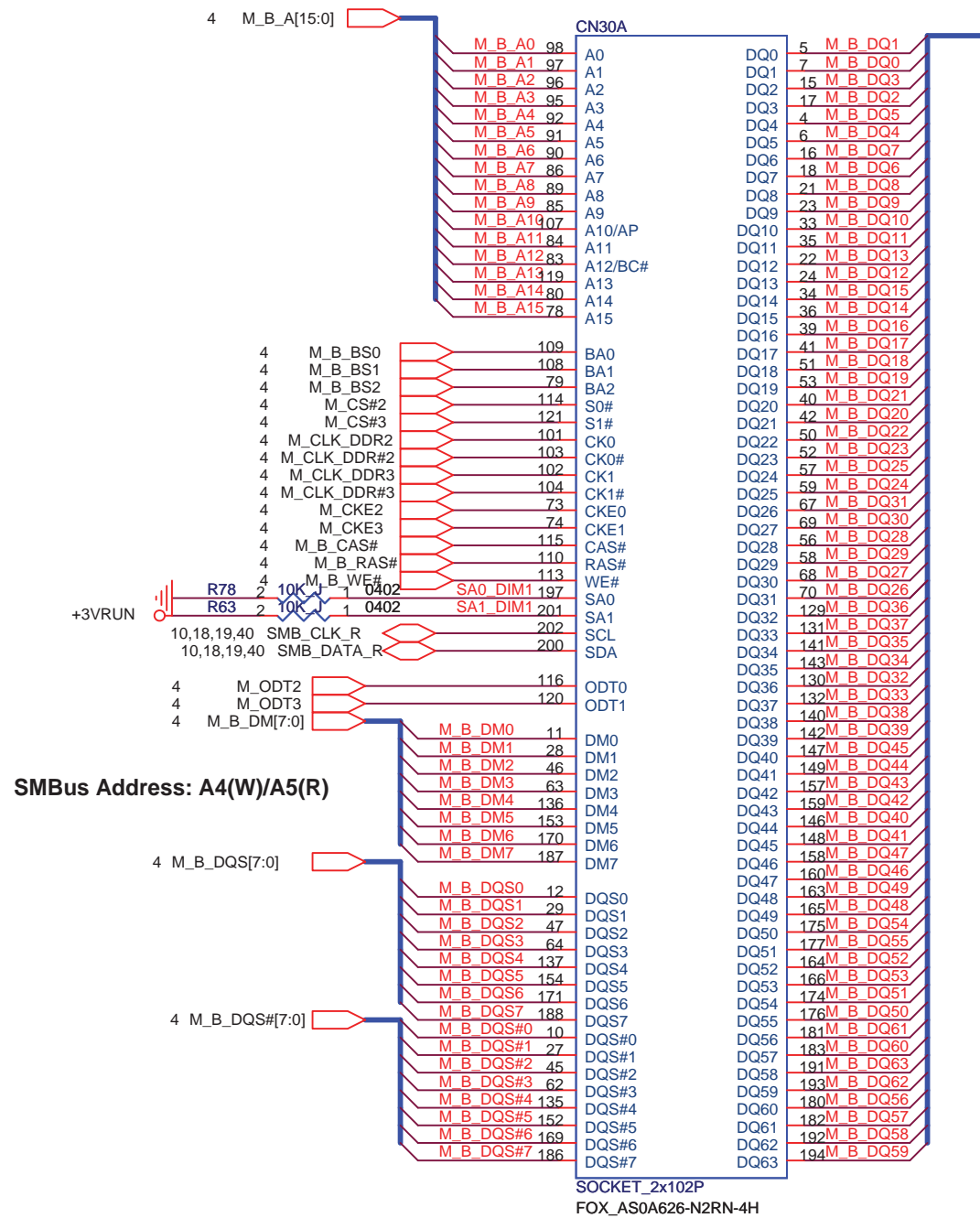


2009.0925  
ADD for EMI request

2009.0925  
Add C72 for RF request

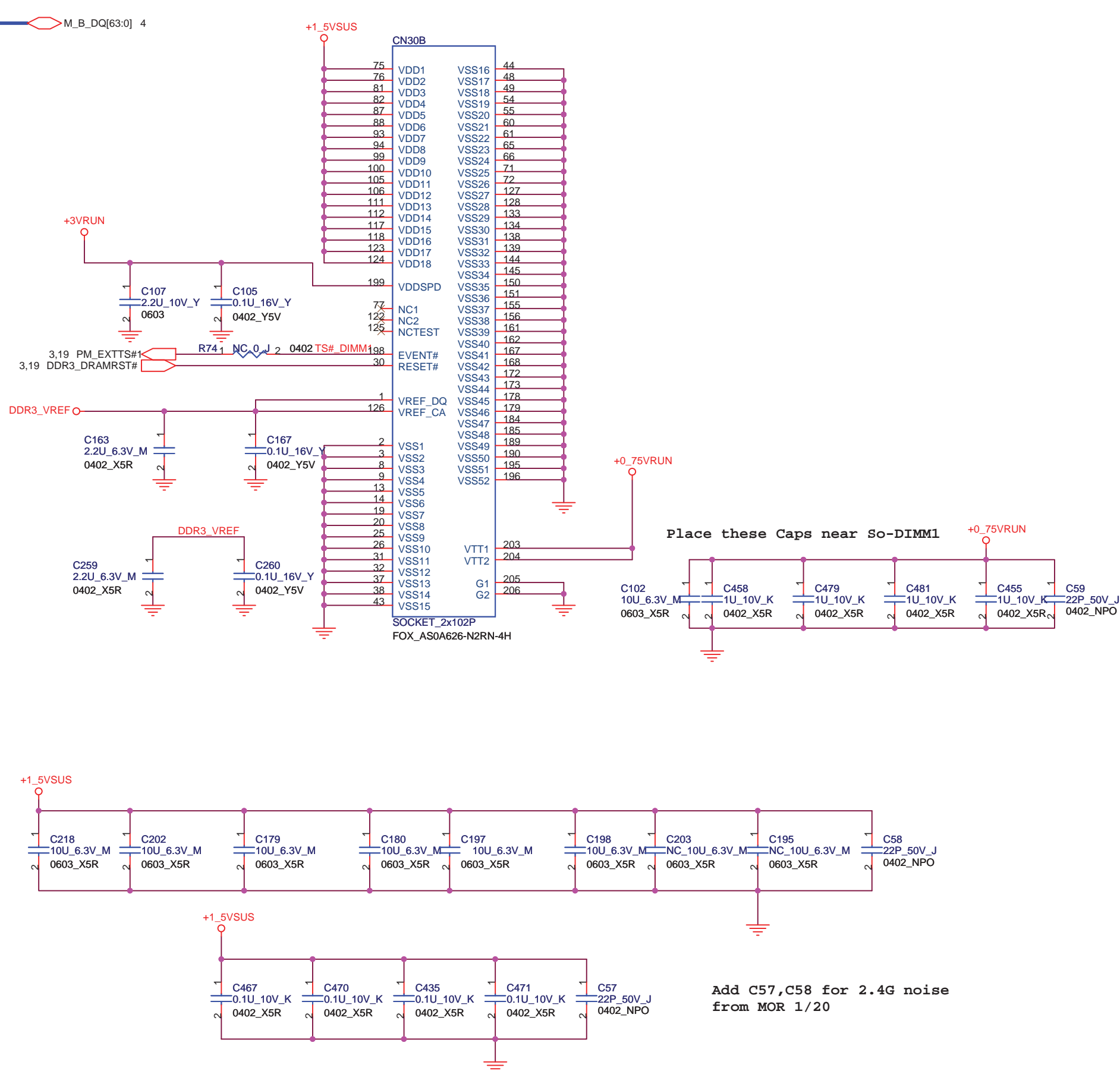




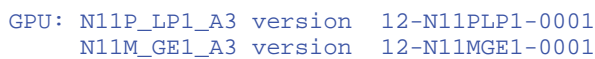


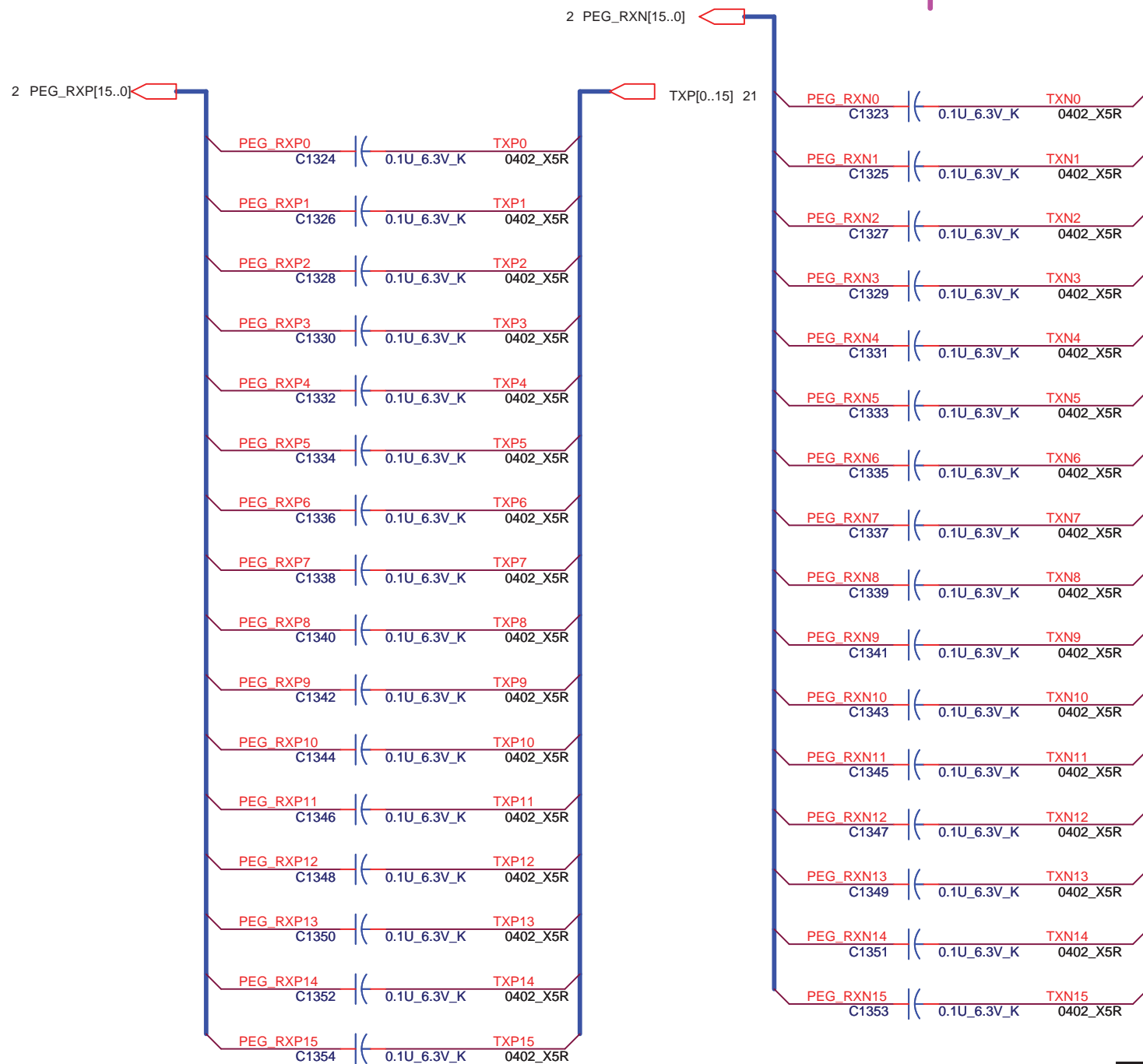
SMBus Address: A4(W)/A5(R)

2009.0922  
CN30 change to Halogen Free







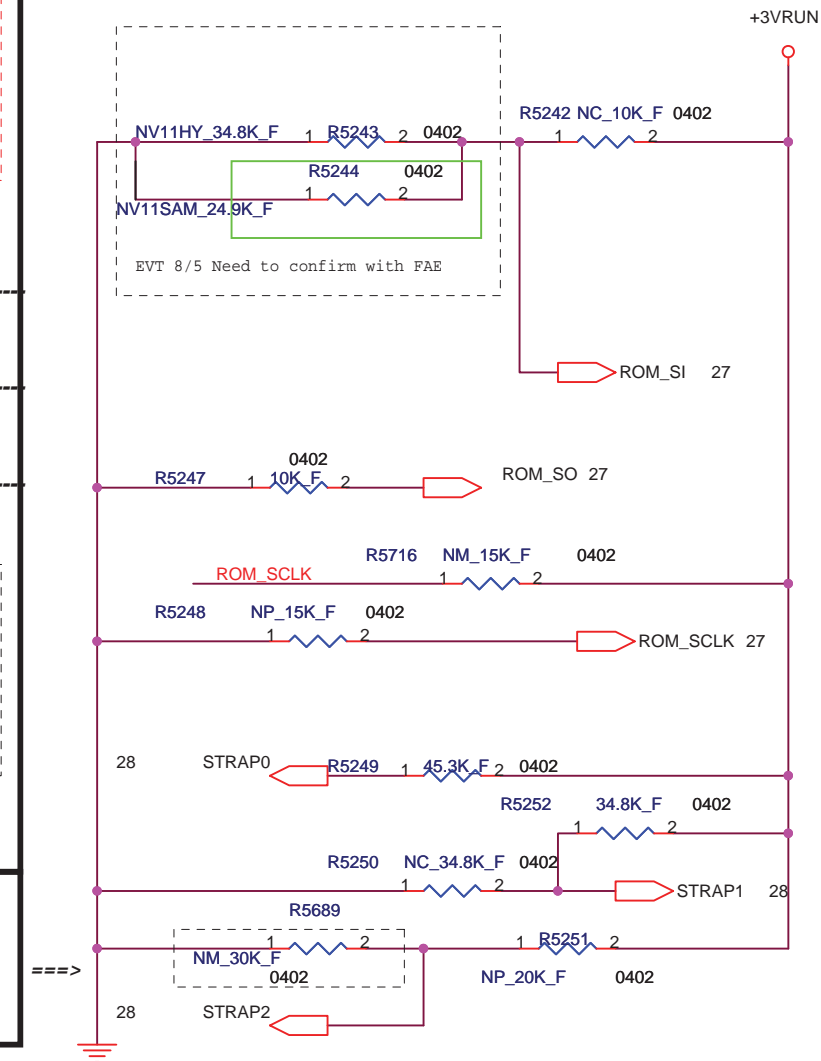


<b>XCLK_417</b> 0 (27M Hz) 1 (Reserved) <b>FB_0_BAR_SIZE</b> 0 256MB 1 (Reserved) <b>SMB_ALT_ADDR</b> 0 0x9E 1 0x9C(multi-GPU usage) <b>VGA_DEVICE</b> 0 3D device(class code 302h) 1 VGA device(class code 300h)	<b>ROM_SO</b>  0001
<b>SUB_VENDOR</b> 0 (No vedio BIOS ROM) 1 (BIOS ROM is present)  <b>SLOT_CLK_CFG</b> 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk)  <b>PEX_PLL_EN_TERM</b> 0 (Disable) 1 (Enable)	<b>ROM_SCLK</b> N11P-LP1 0010 N11M-GE1 1010
<b>USER[3:0]</b> 1111	<b>STRAP0</b> (1111)
<b>N10x/N11x 3GIO_PADCFG[3:0]</b> 1110	<b>STRAP1</b> (1110)
<b>N11X PCI_DEVID[3:0]</b> N11P-LP1 1011b N11M-GE1 0101b <b>PCI_DEVICE IDs</b> N11P-LP1 (0x0A2B) N11M-GE1 (0x0A75)	<b>Strap2</b> N11P-LP1 1011 N11M-GE1 0101
0000 64-bit Reserved 1110 32Mx32 GDDR3 - 136 ball 64-bit Hynix - 35K pul Low. 0100 32Mx32 GDDR3 - 136 ball 64-bit Samsung- 25K pull Low <b>ROM_SI</b>	

8/3 [DVT] Revise the Strap Pin value as FAE provided for DVT Sample.

- N11M-GE1 x0A75
- N11P-LP1 0x0A2B

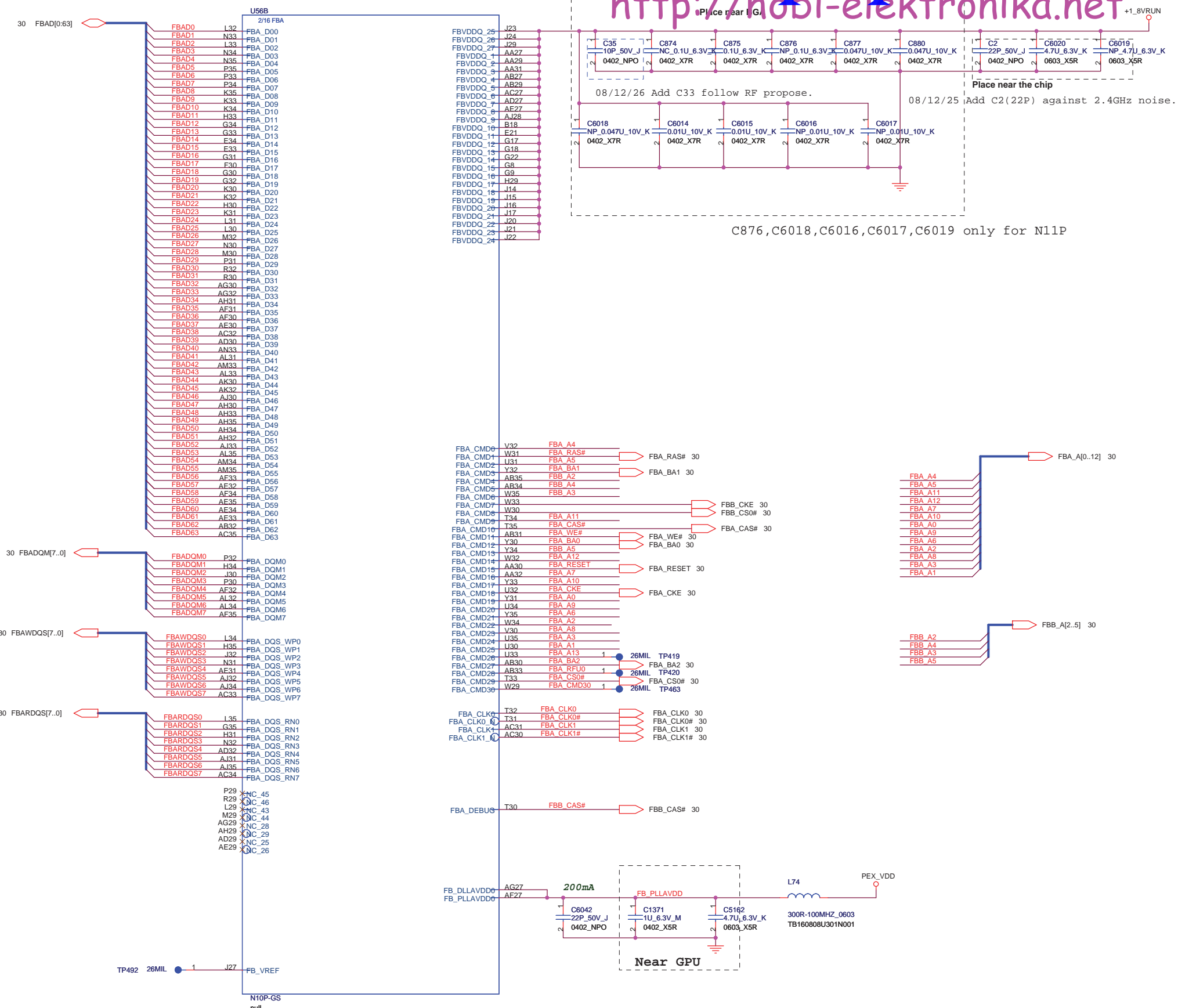
2009/9/10  
N11P-LP1+SANSUNG(H2) SKU and N11M-GE1 +SANSUANG(M2 SKU )need change BOM  
R5244 change from 1R-0004532-F200(45.3K) to 1R-0002492-F200(24.9K) for nVIDIA FAE suggest

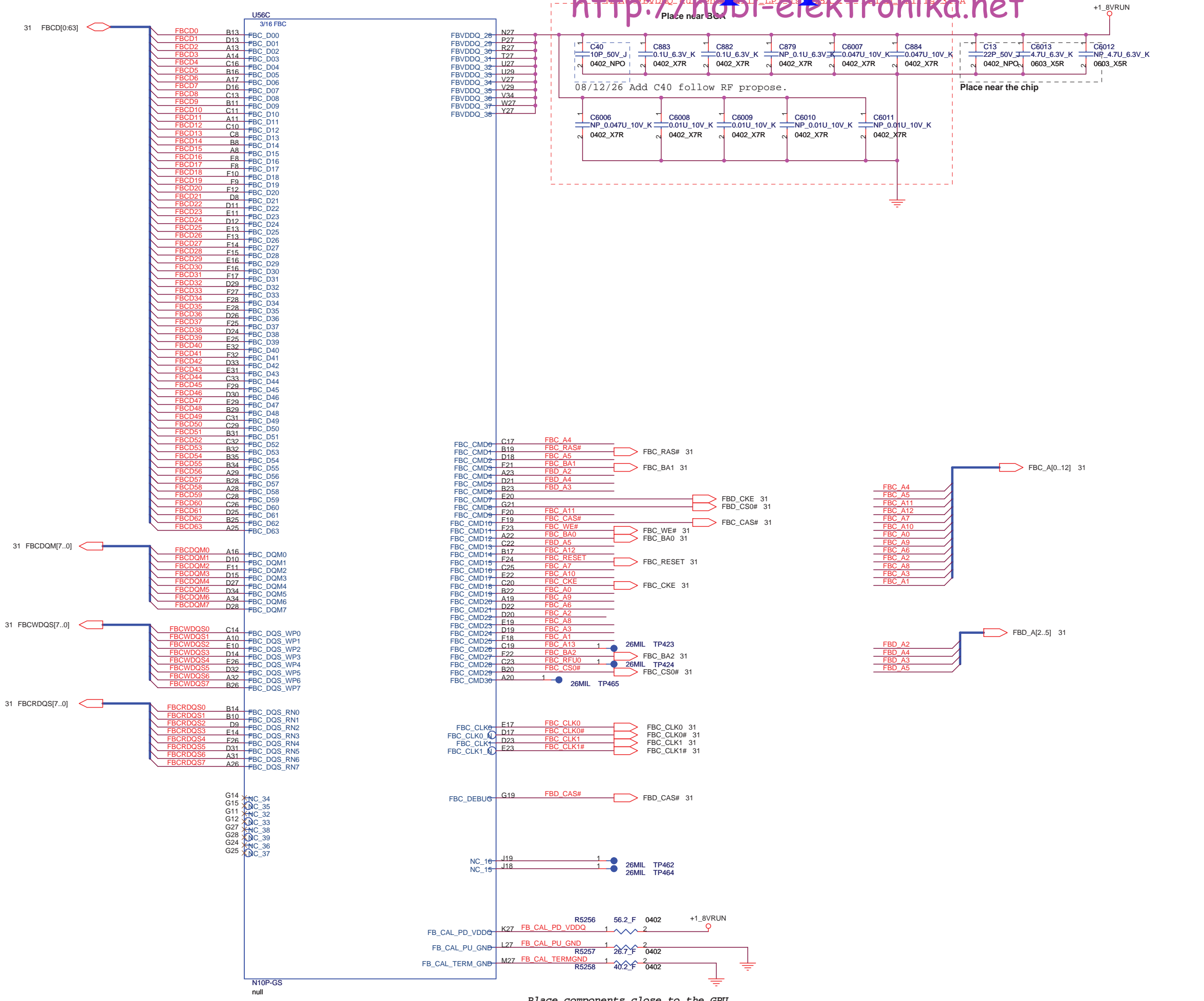


Logical Strap bit Mapping		
Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

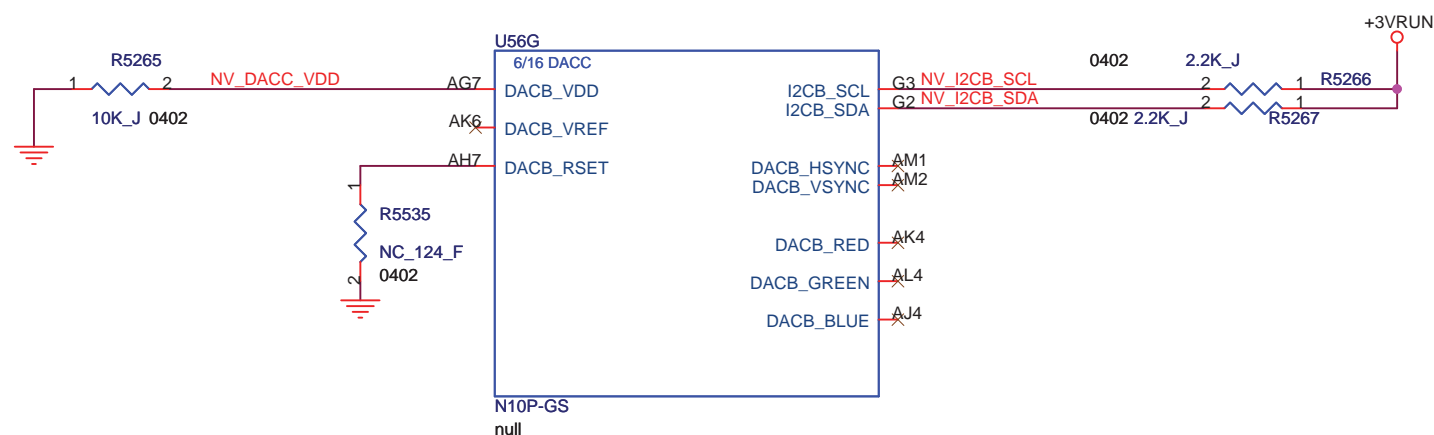
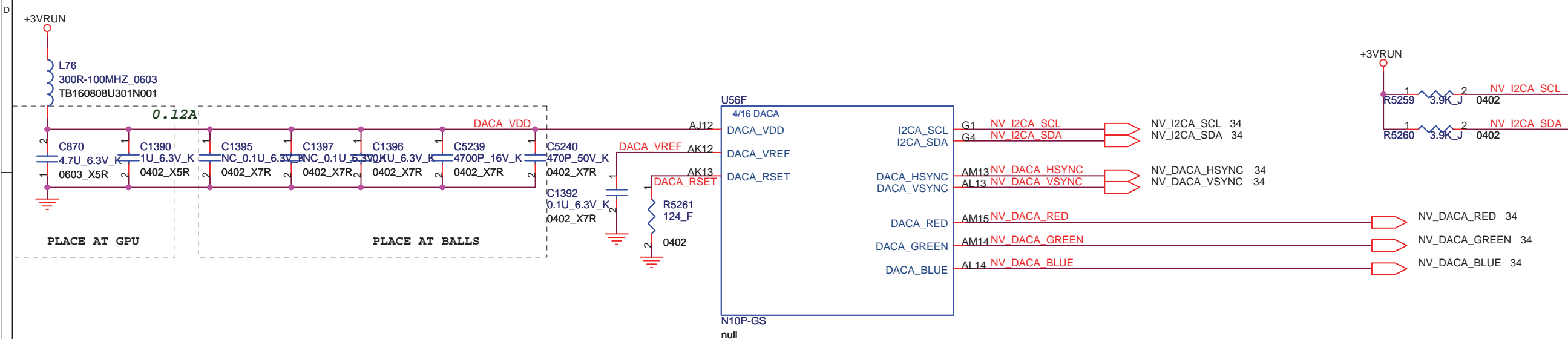
Strap Options					
Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04642-001\_v01\_secured>

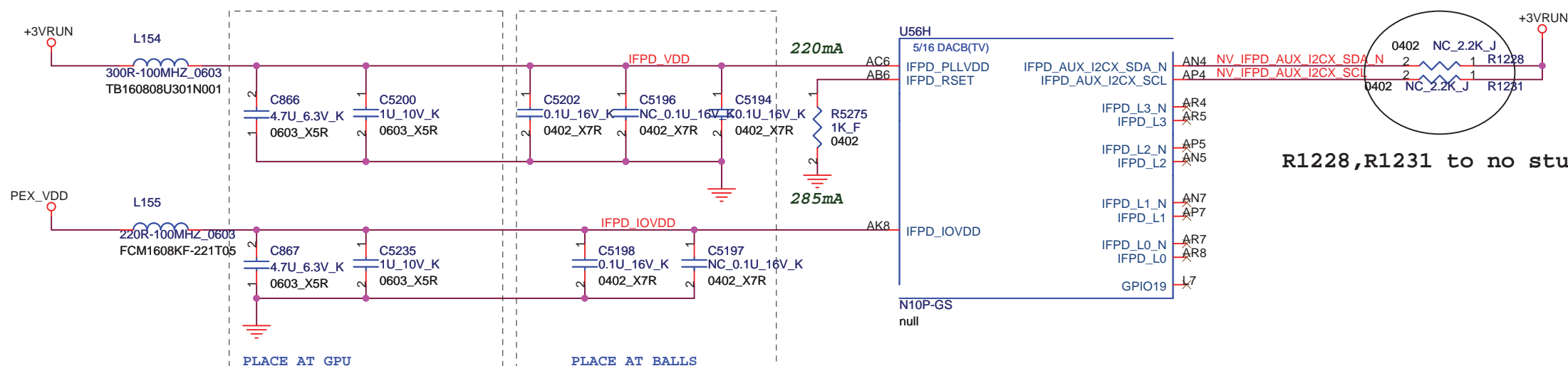








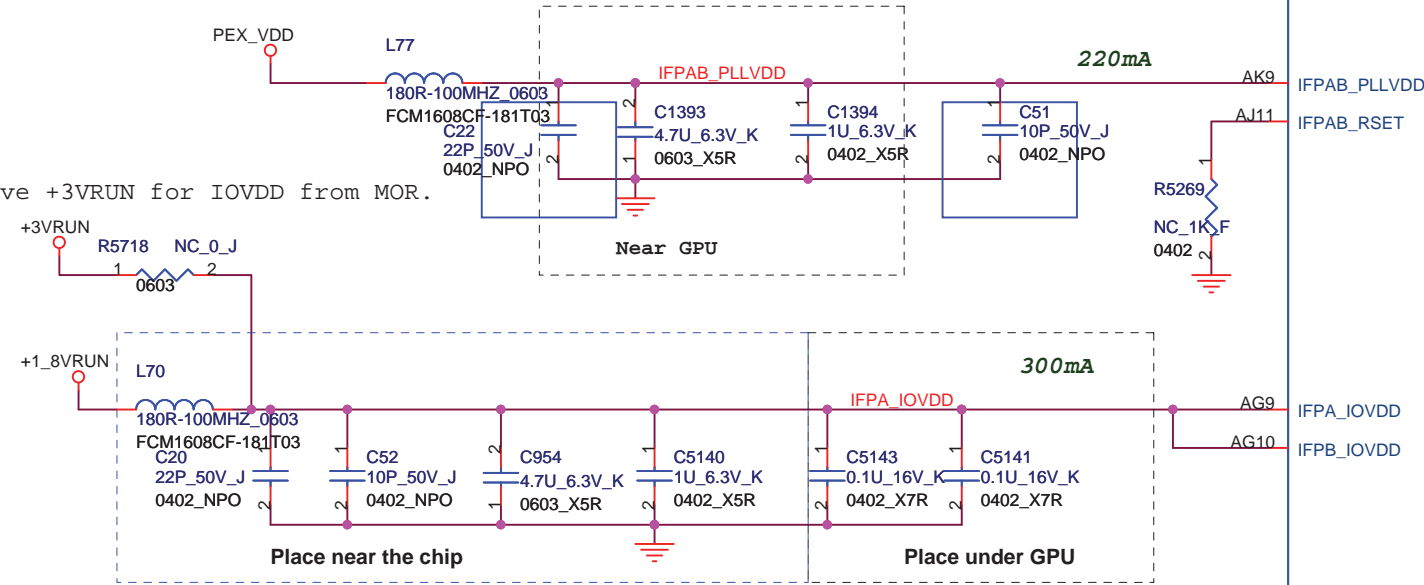
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCLK	SCL
	VGA-DDCDA	SDA



R1228,R1231 to no stuff ---MOR 5/25

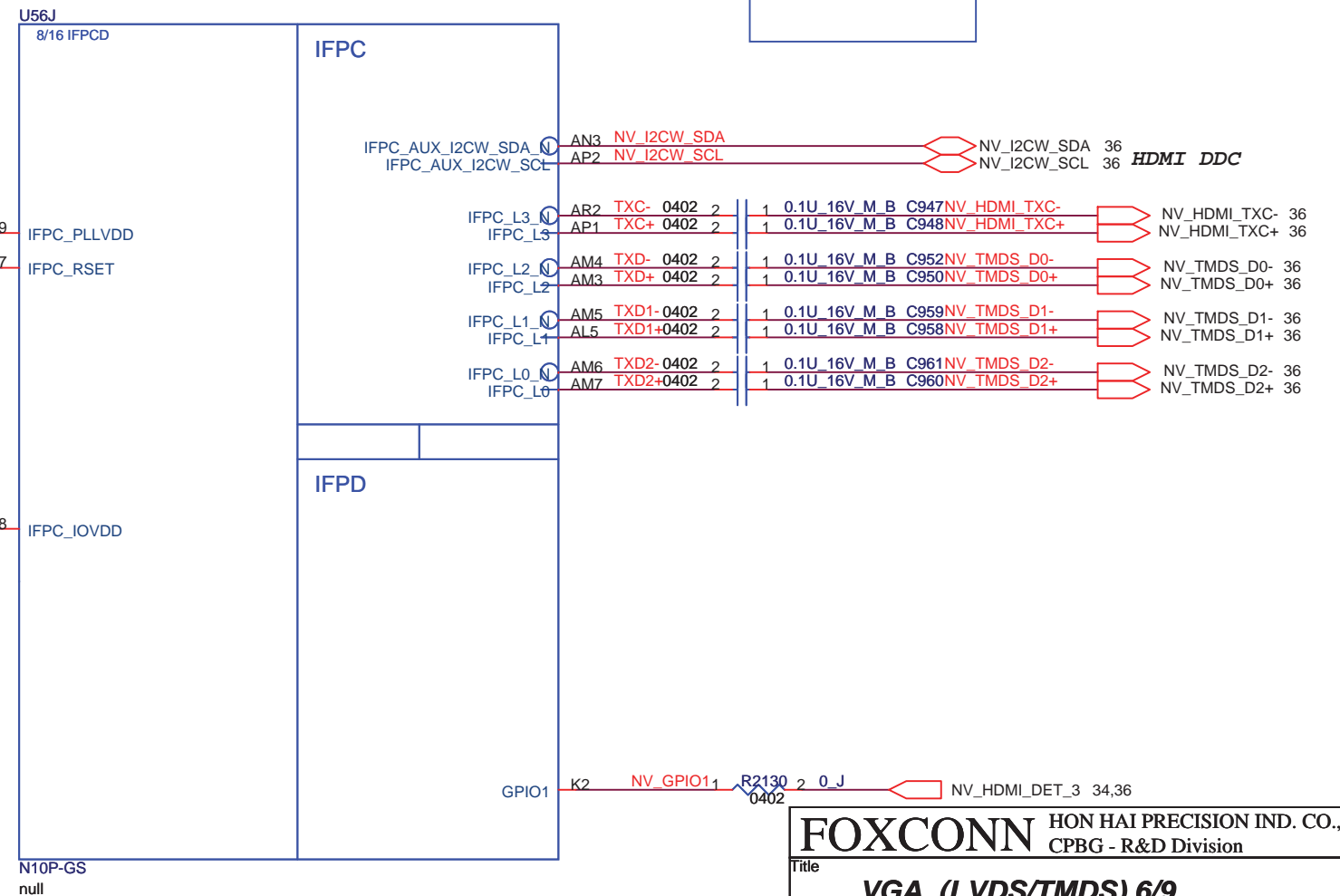
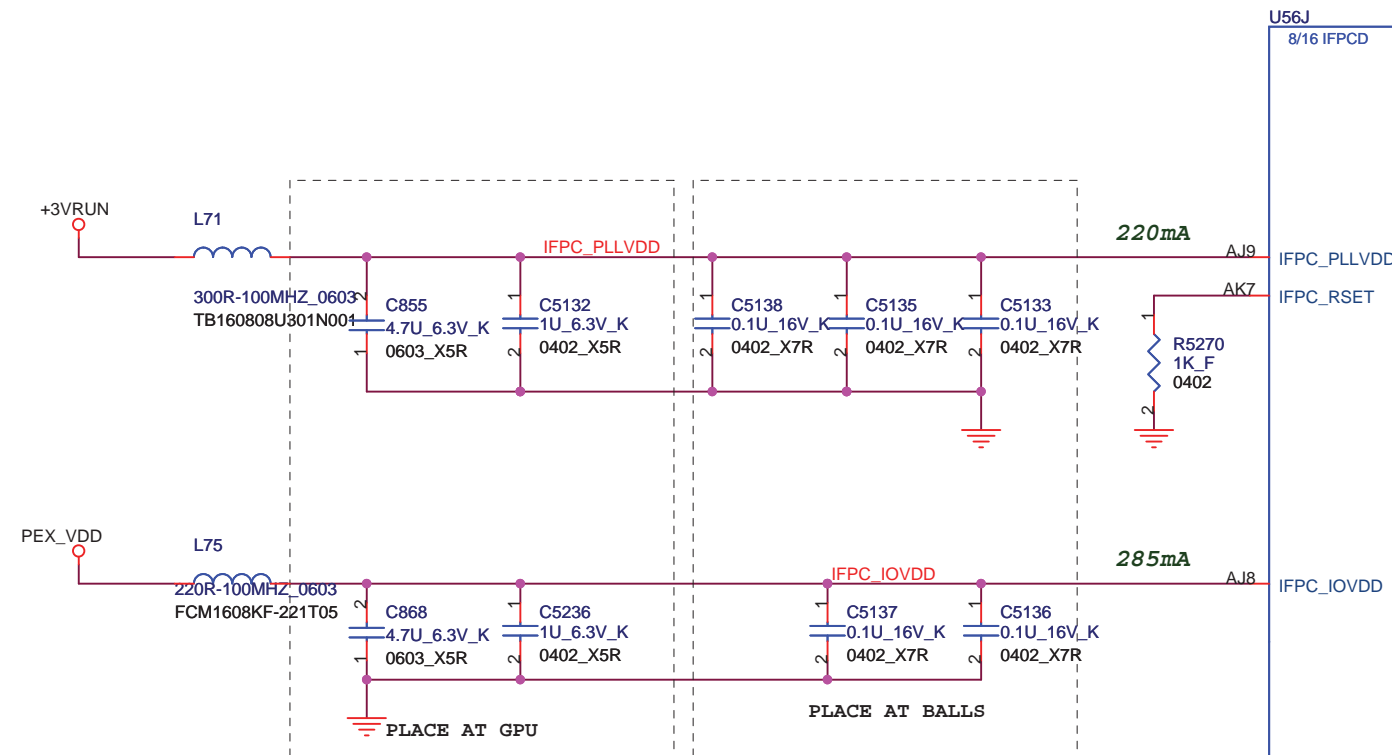
08/12/26 Add C51,C52 10p follow RF propose.

09/02/05 Reserve +3VRUN for IOVDD from MOR.

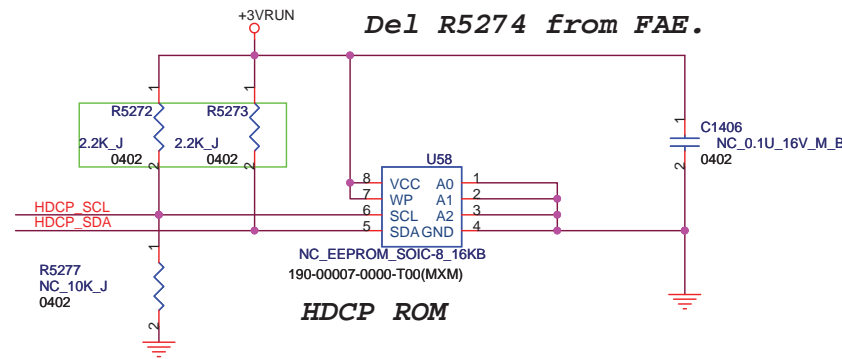


08/12/25 Add C20,C22 against 2.4GHz noise.

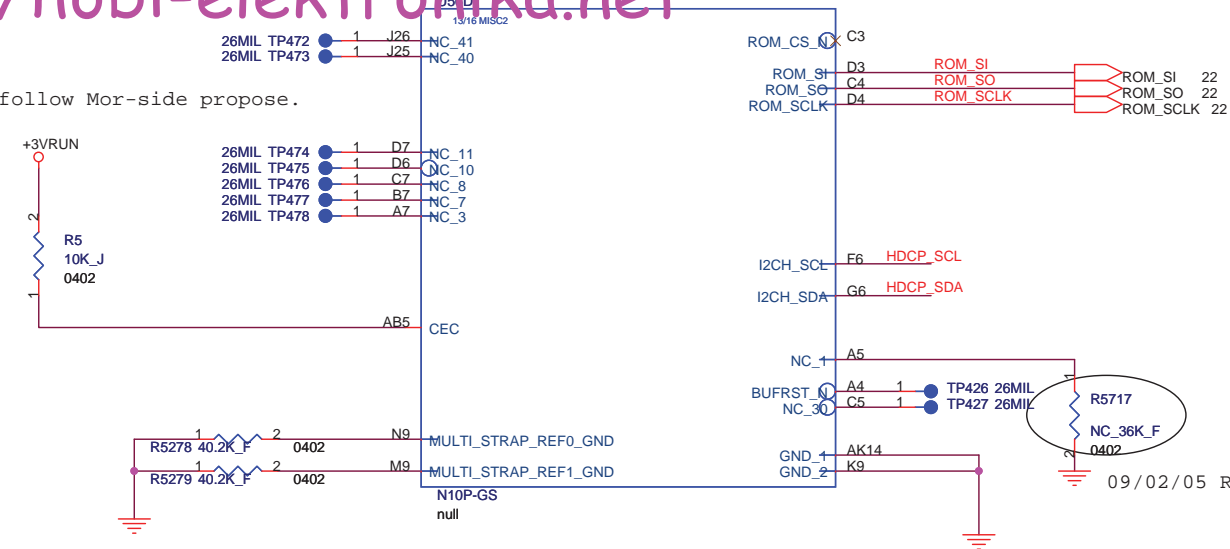
08/12/22 Change R1056,R1057 from 2.2K to 3.9K follow Mor-side propose.



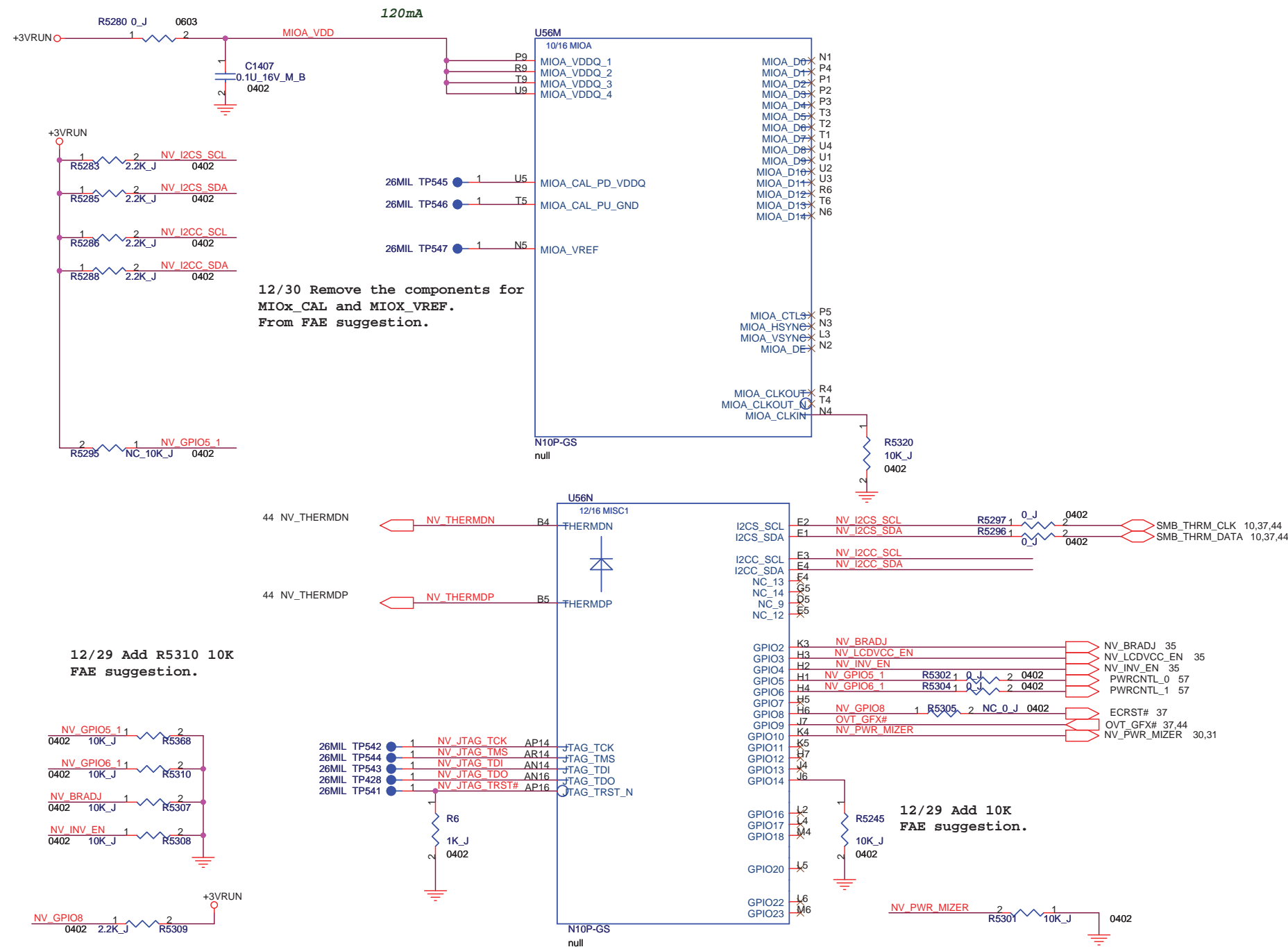
08/12/26 Add R5 follow Mor-side propose.



```
2009.0921
change R5272,R5273from NC to mount
```

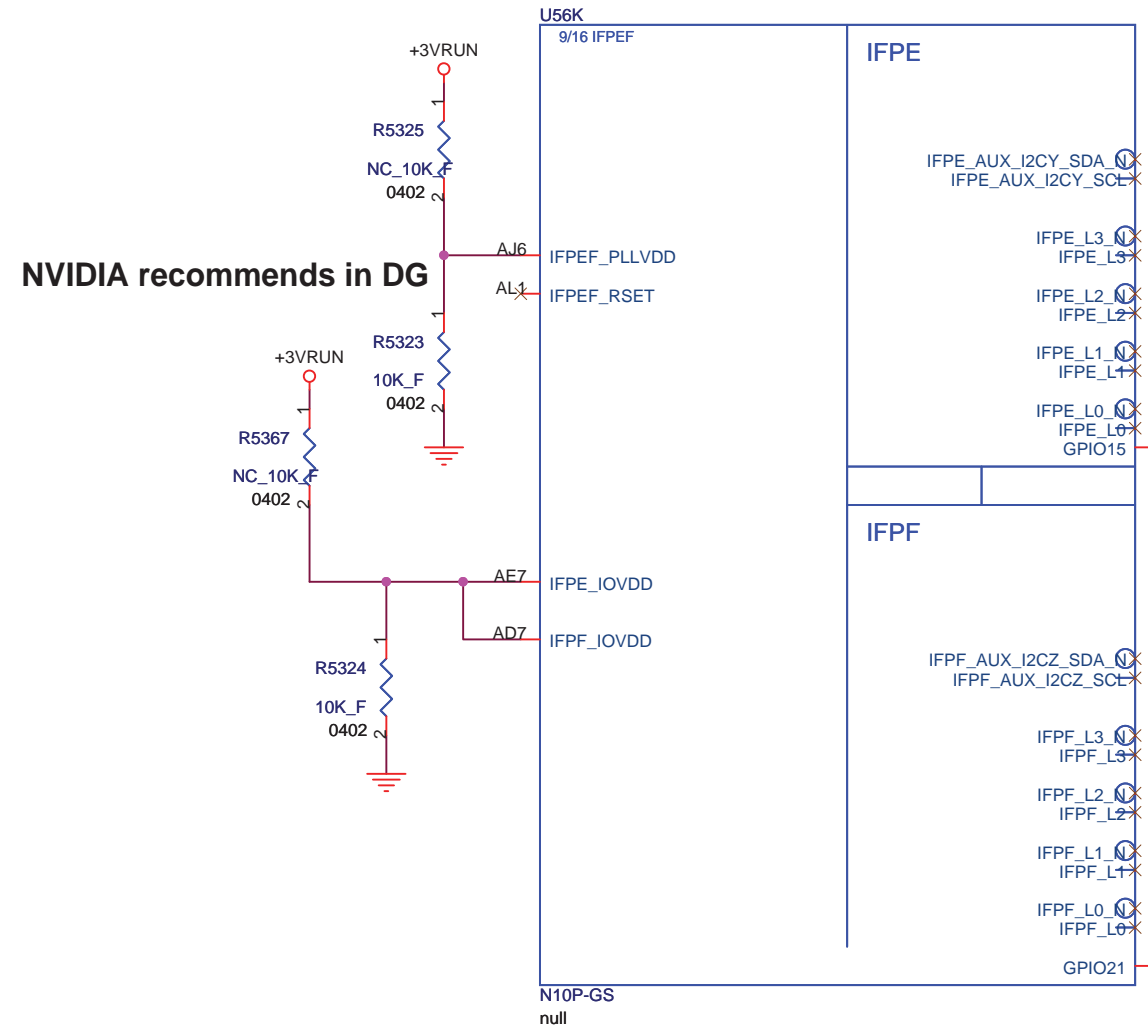
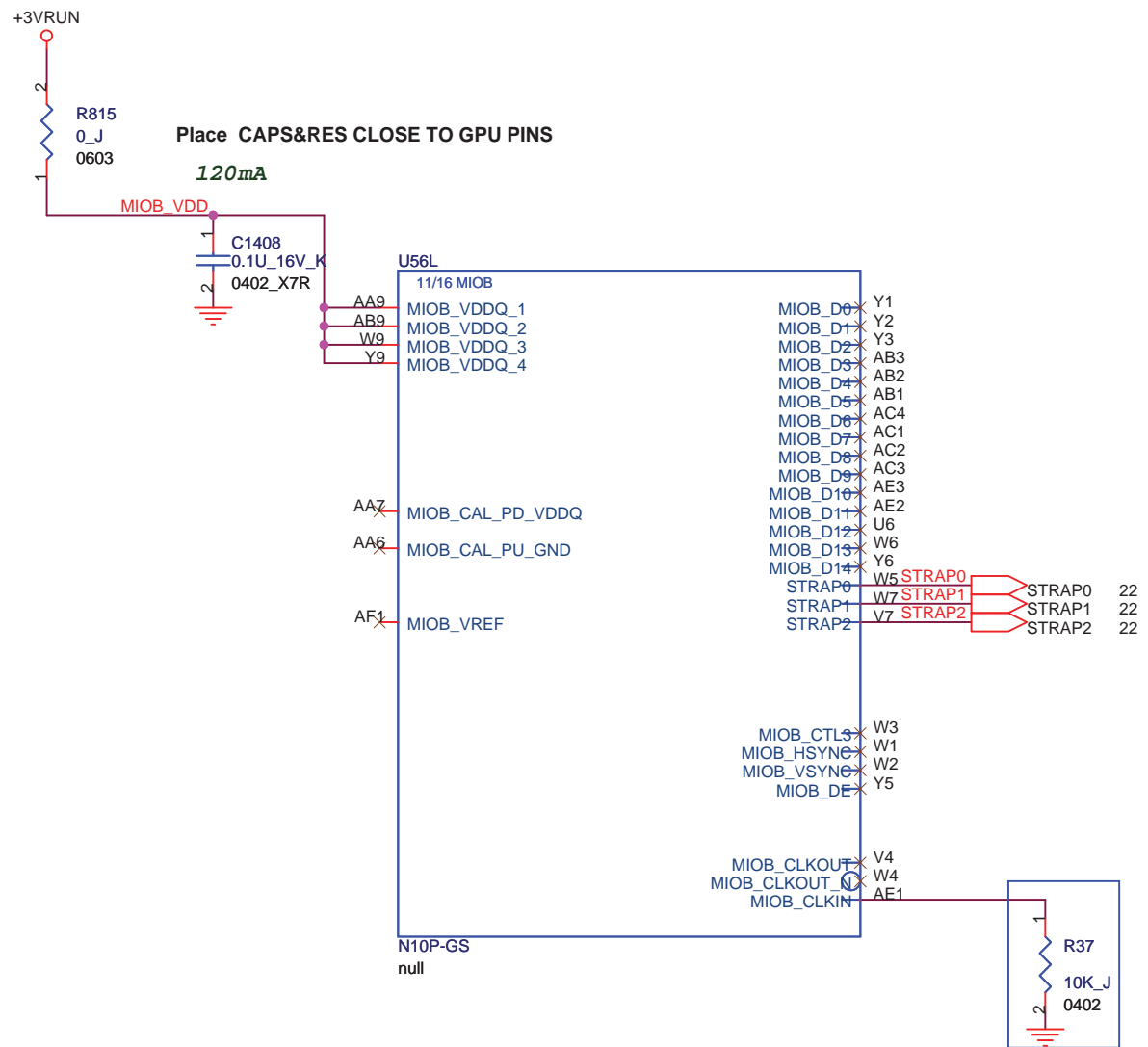
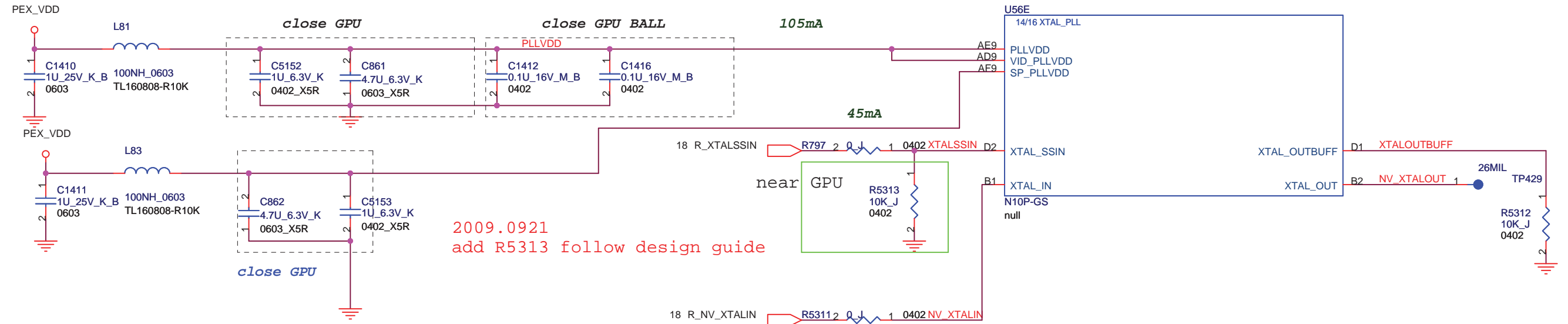


09/02/05 Reserve R5717 follow Mor-side propose.



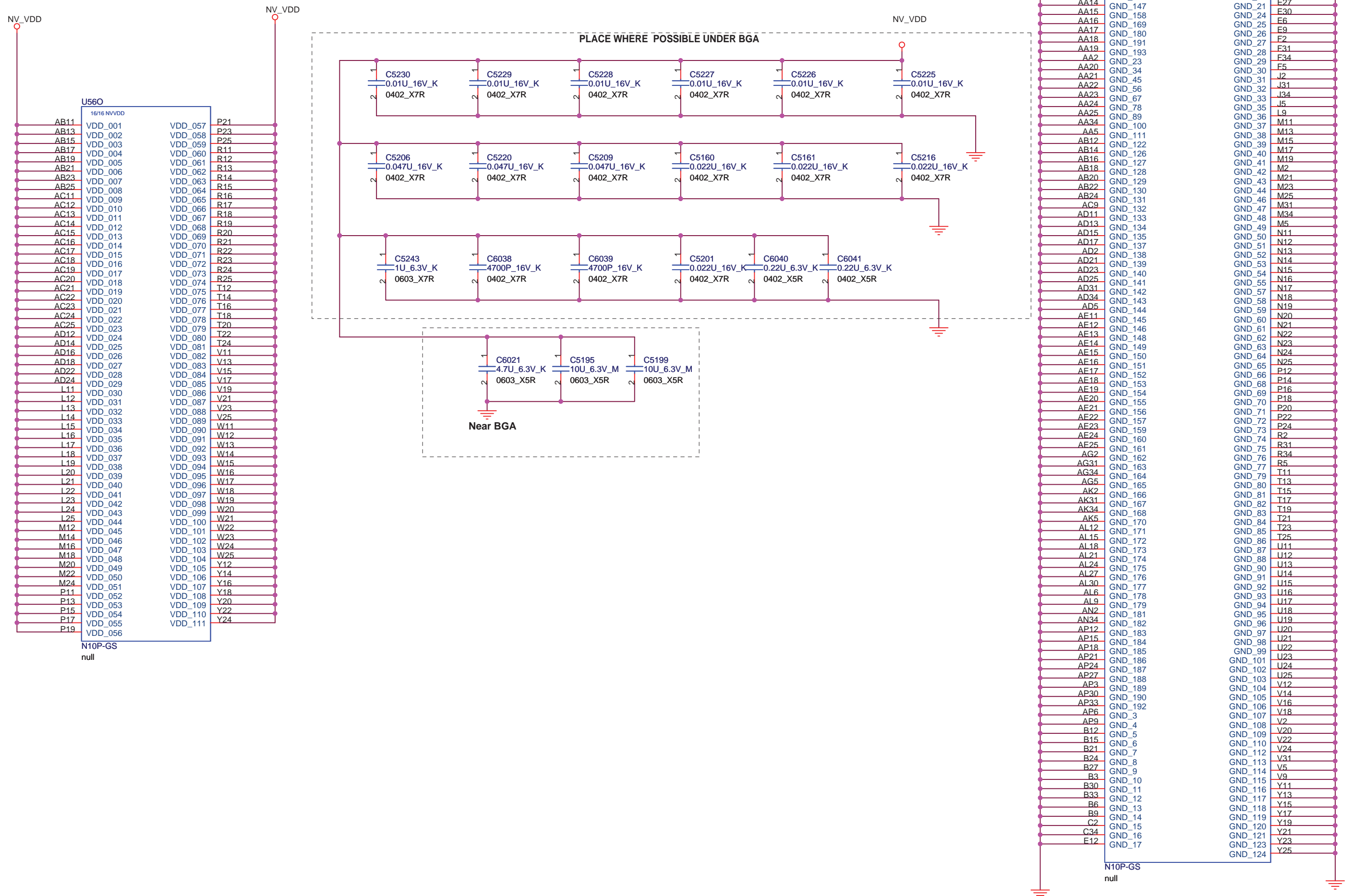
GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	YES		
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0)	Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	FOR Power Control NVDD	
GPIO6	O	No	FOR Power Control NVDD	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low

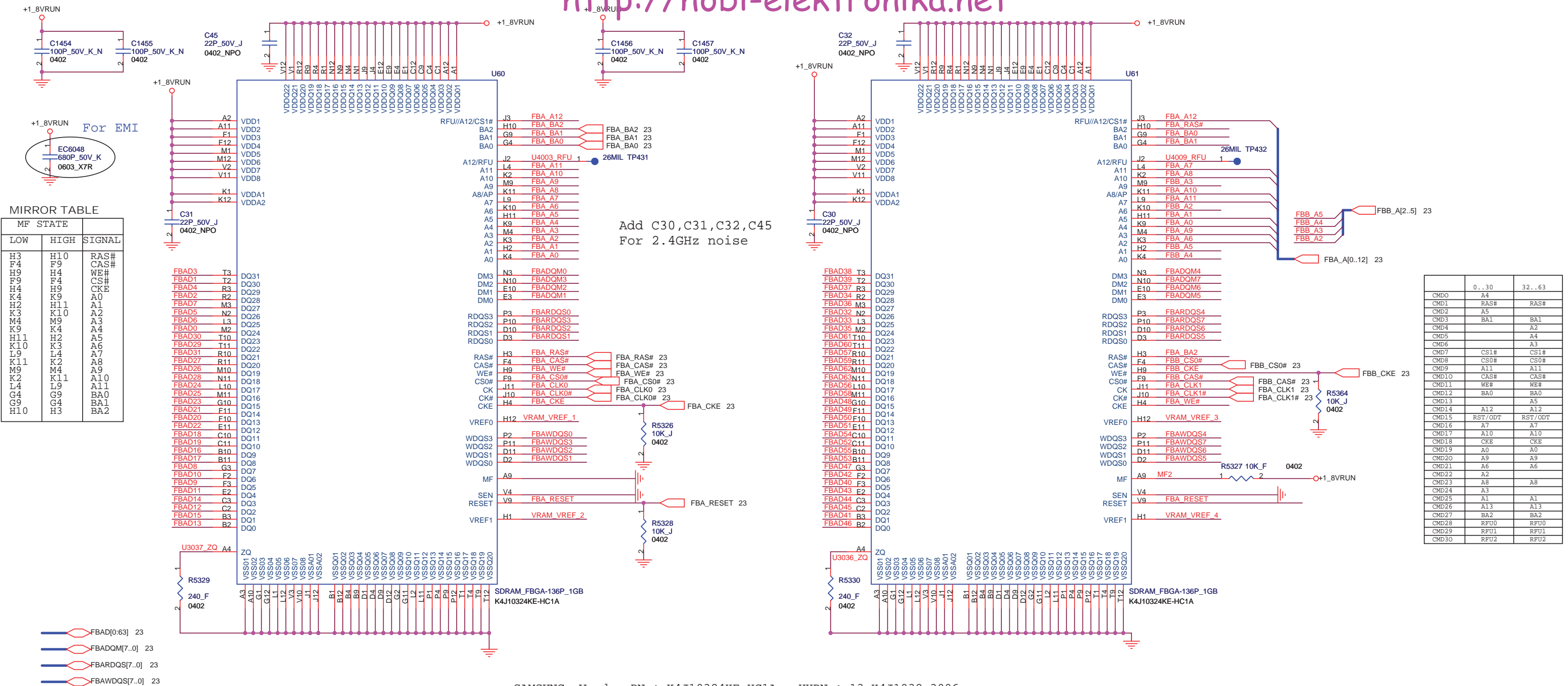
SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor



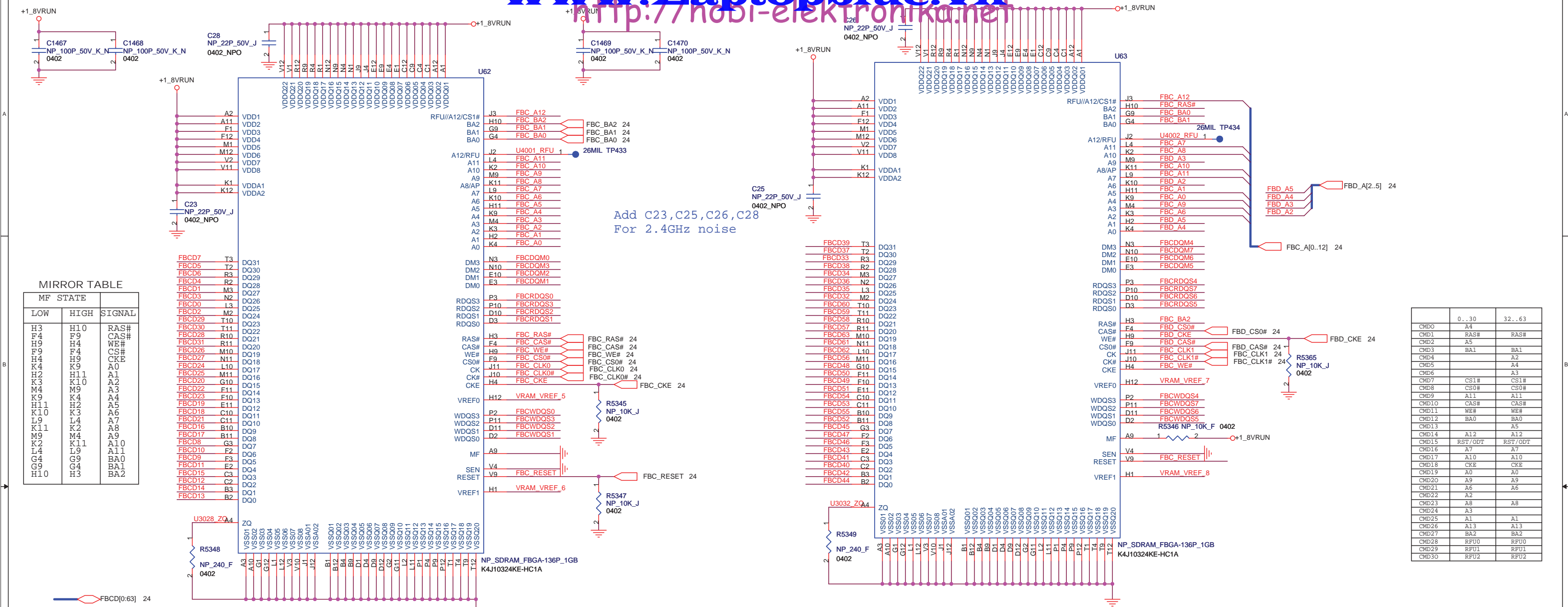


N11M\_GE1 is 16.29A





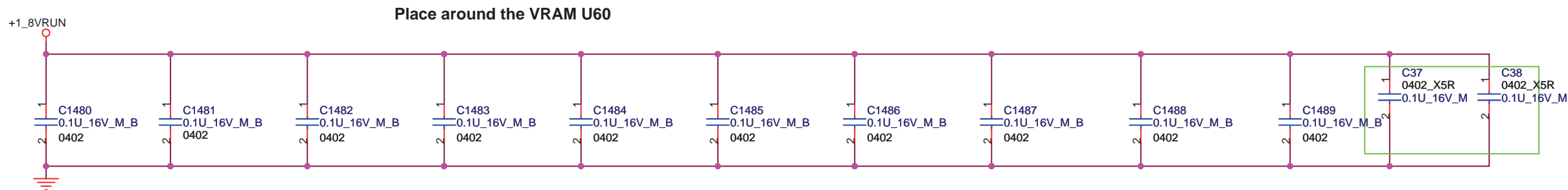
	0..30	32..63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A1
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2



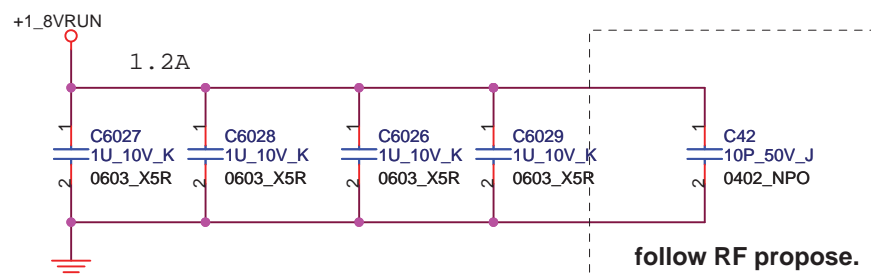
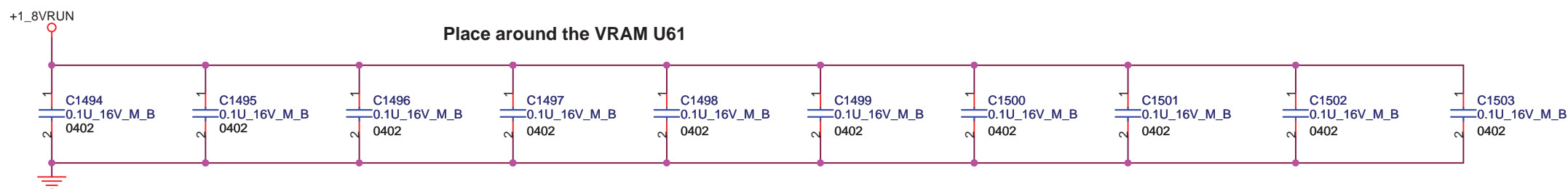
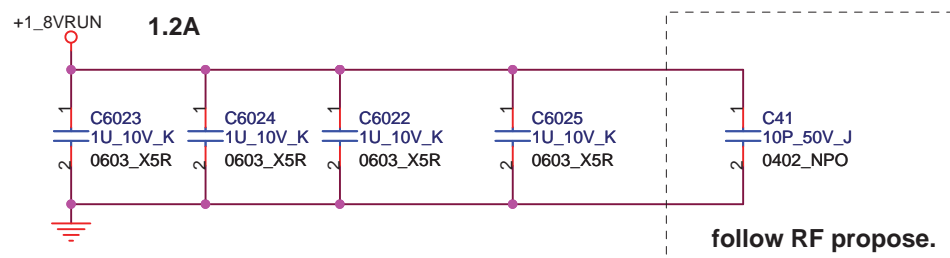
	0...30	32...63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

FOXCONN HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D DivisionTitle  
**VRAM(GDDR)# 2/2**Size  
Custom  
Document Number  
**M9A0\_MP**

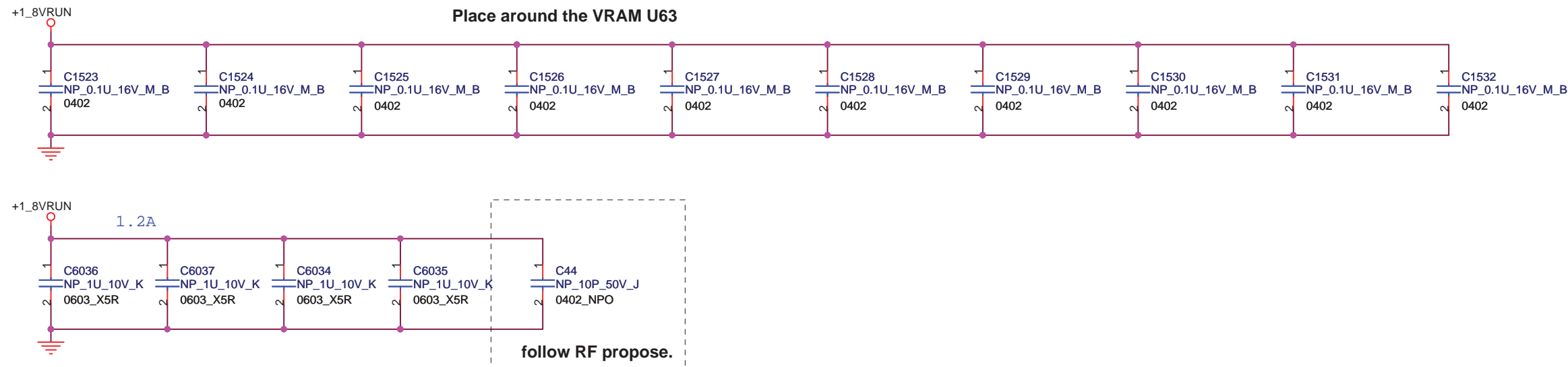
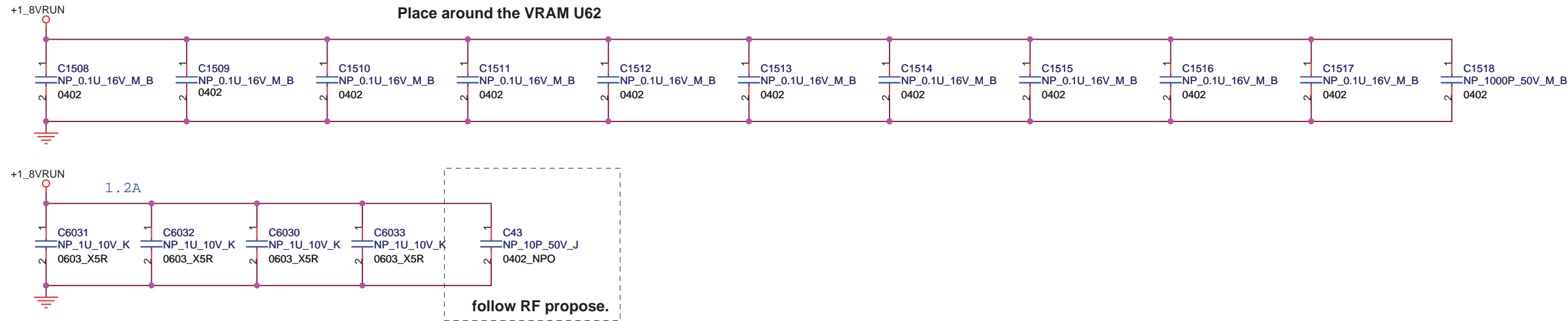
Date: Thursday, November 19, 2009 Sheet 31 of 73 Rev 1.1

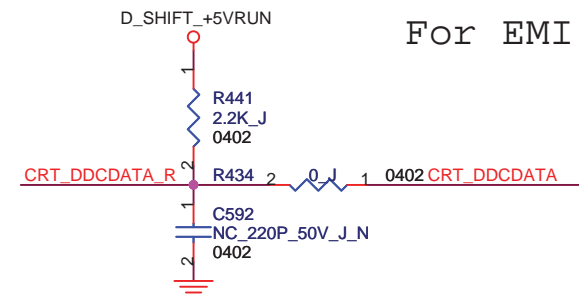
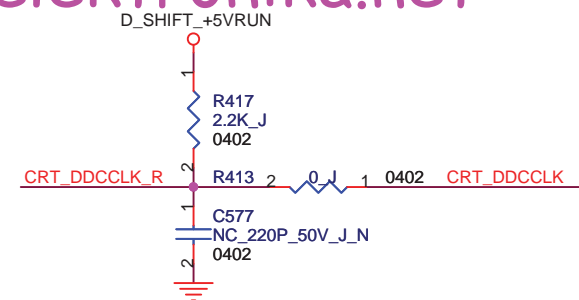


2009.0925  
ADD C37,C38 for EMI request

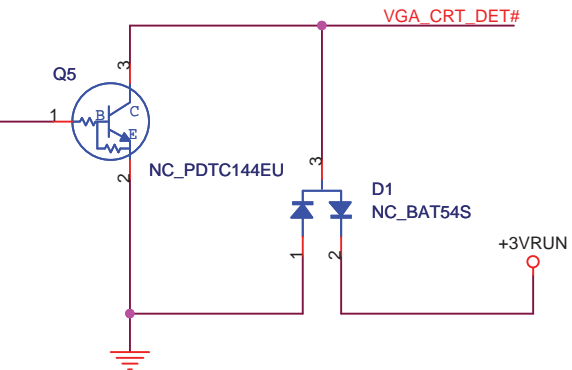






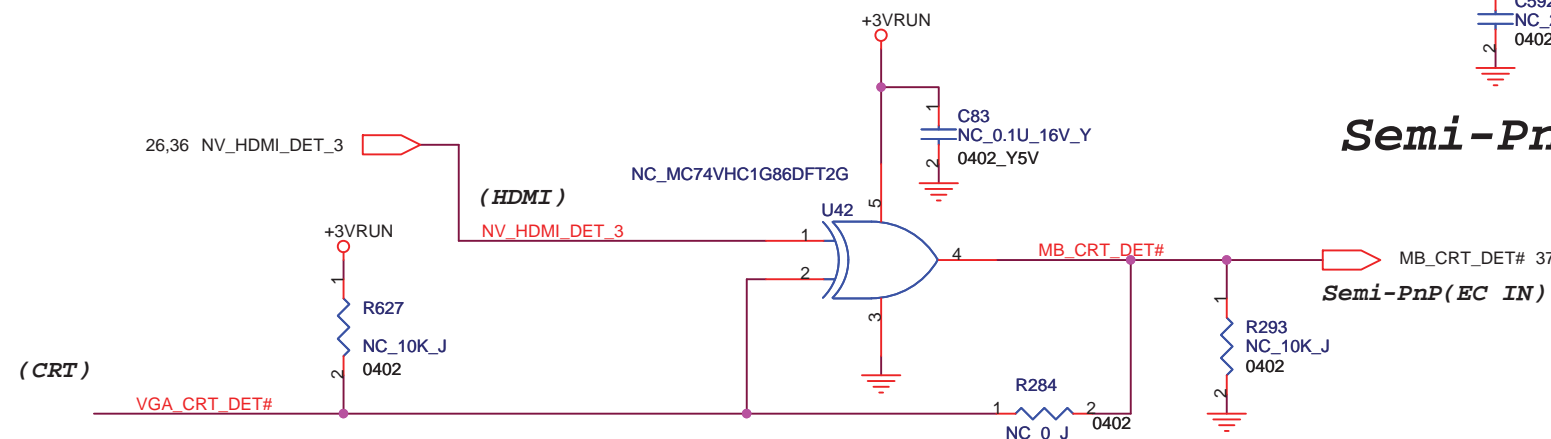


Semi-PnP

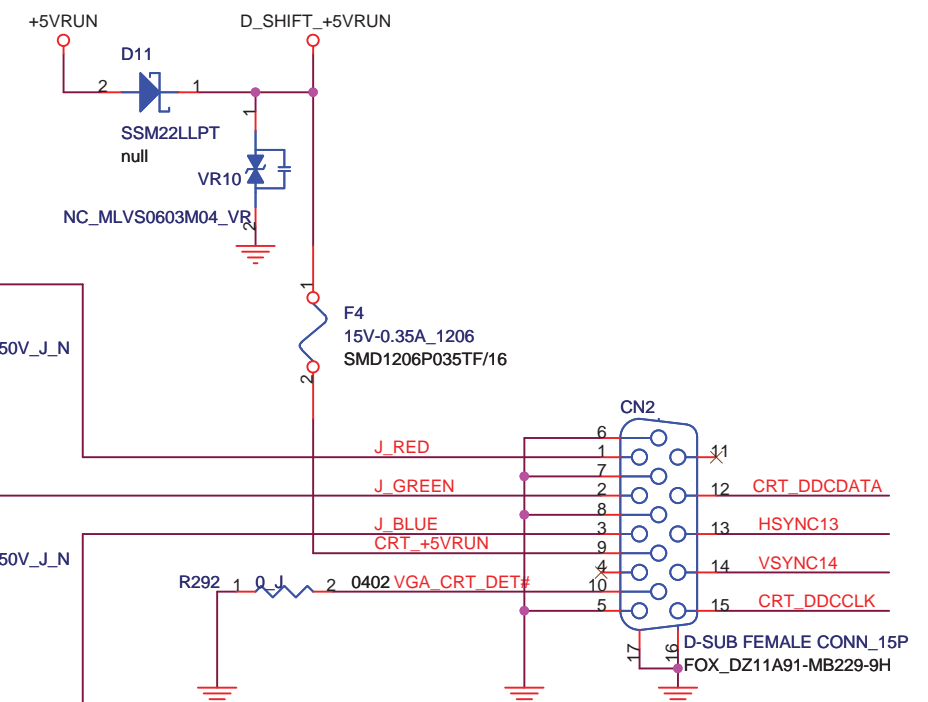
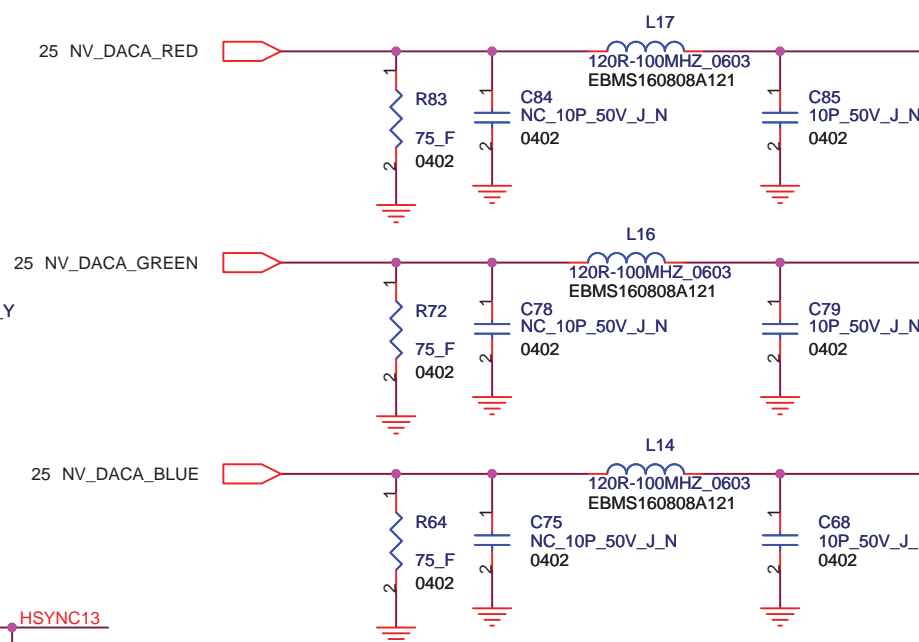


For EMI

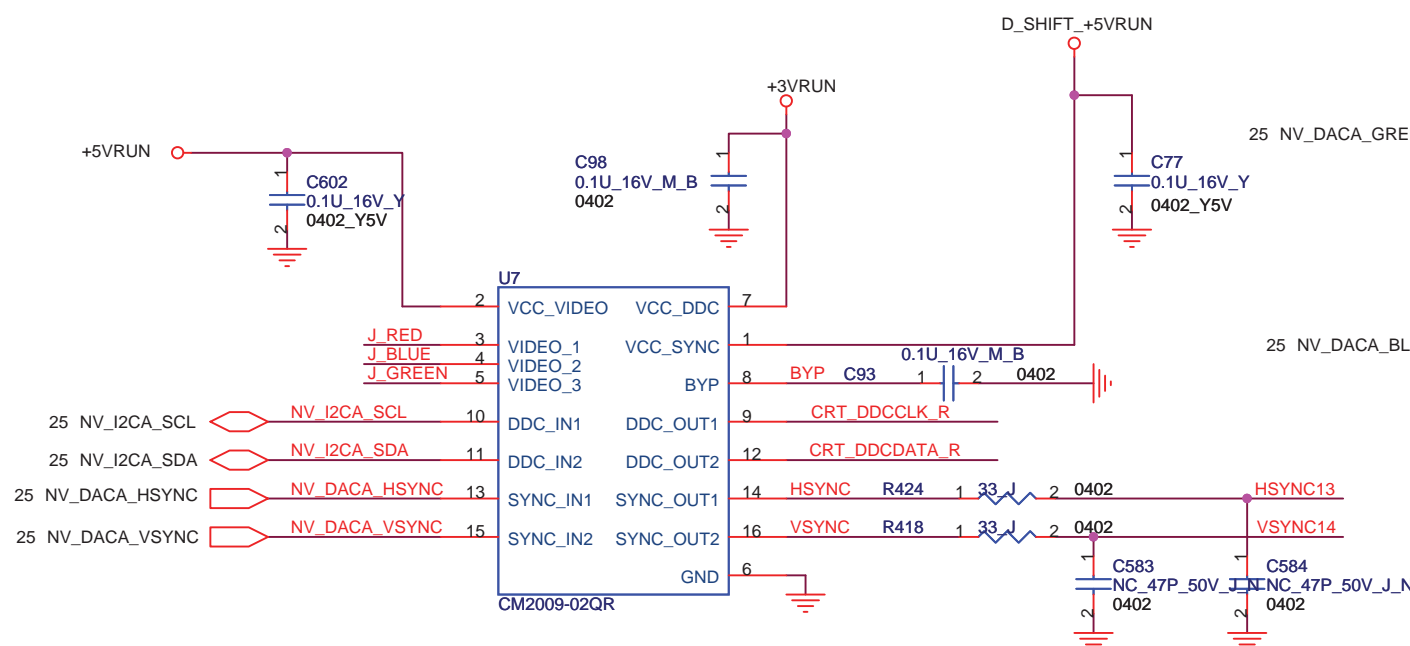
## Semi-PnP Circuit

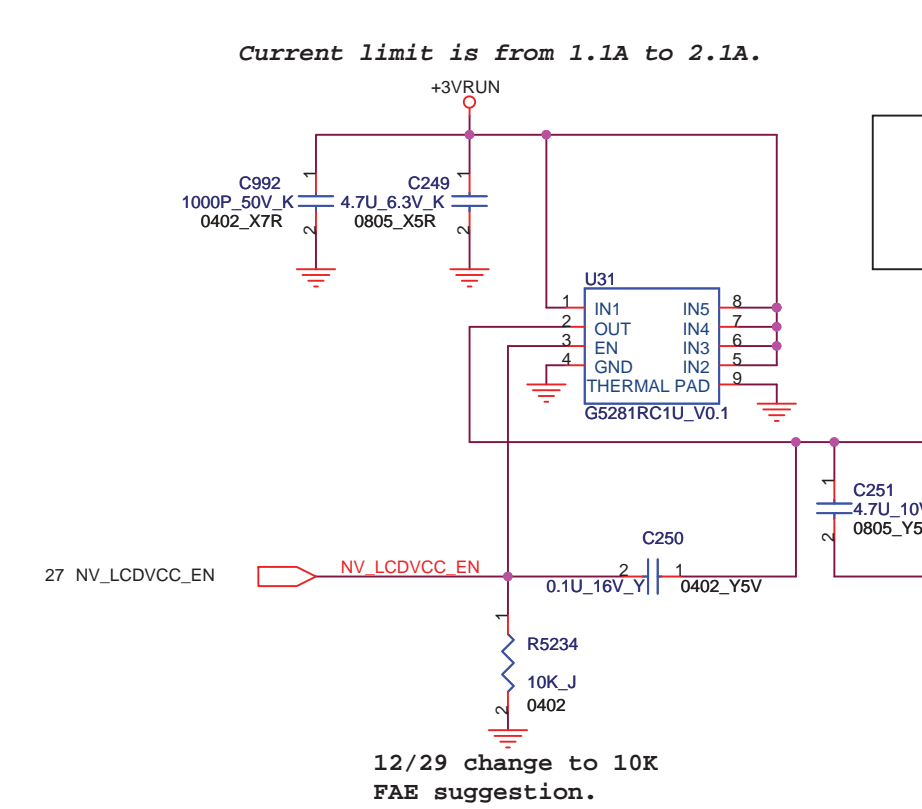
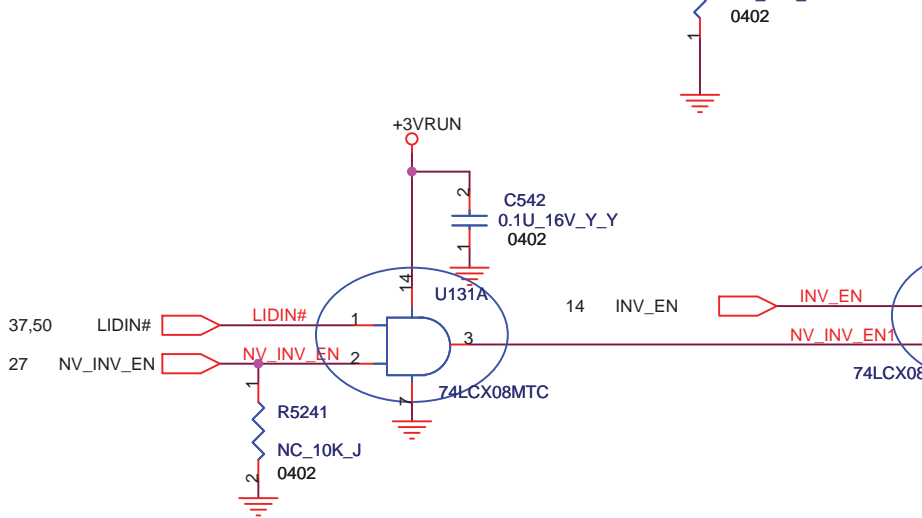
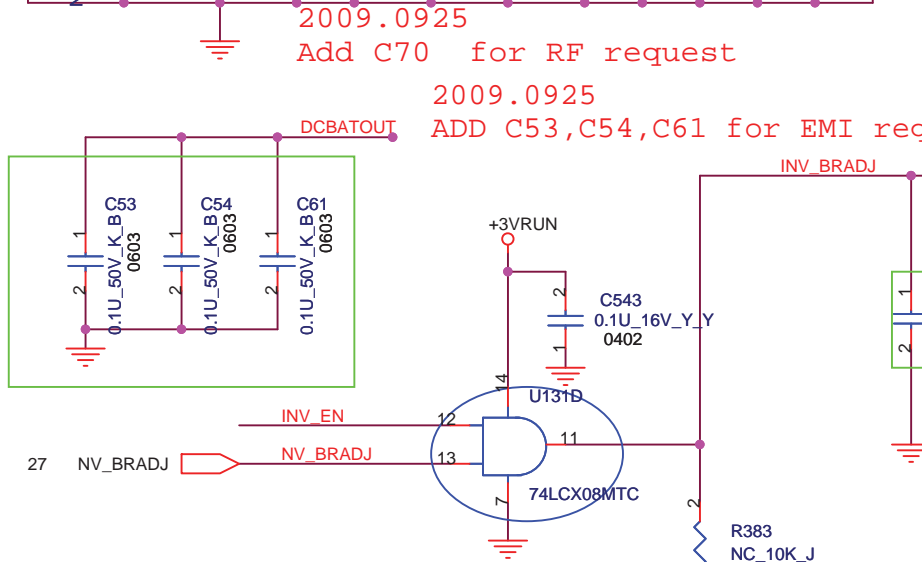
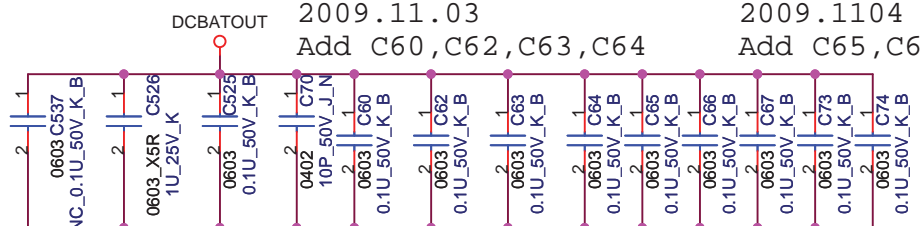


Change R83,R72,R64 to 75ohm --MOR 2/27

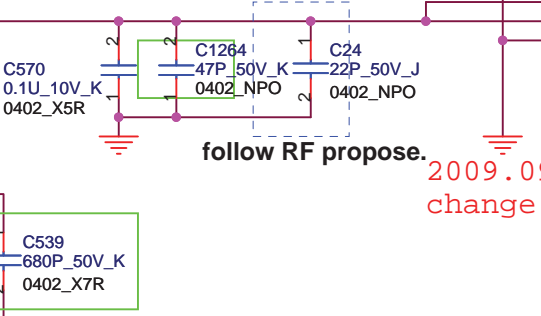
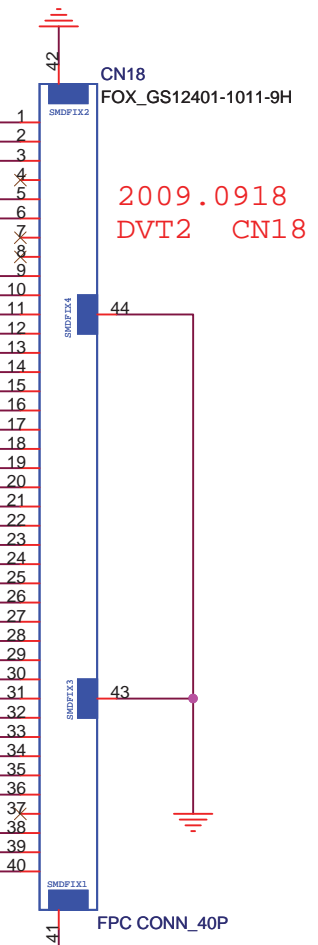
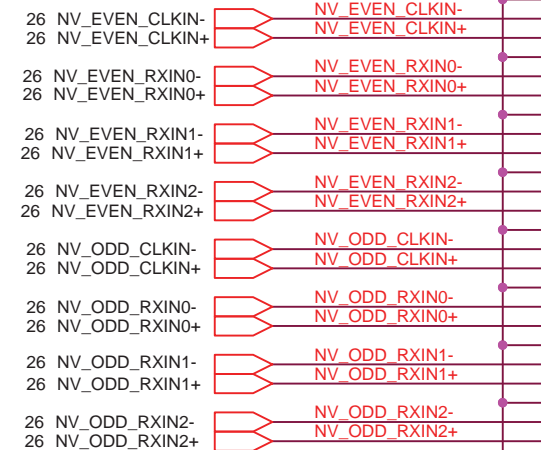
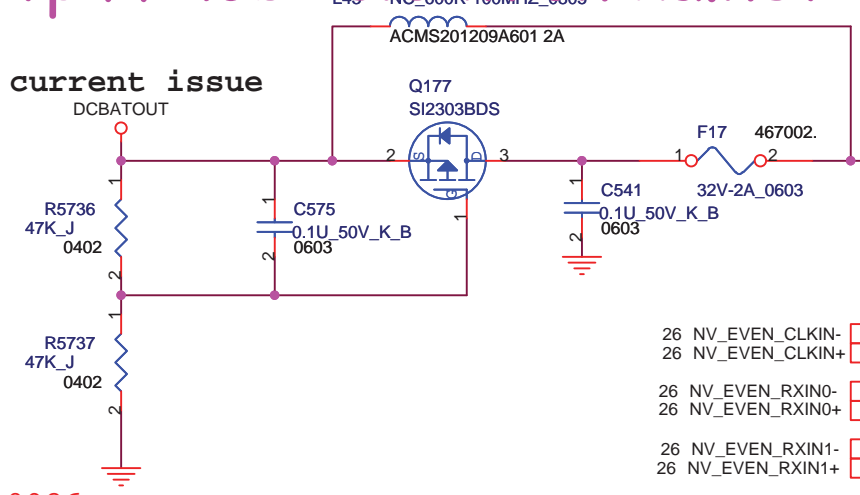


CRT CONNECTOR

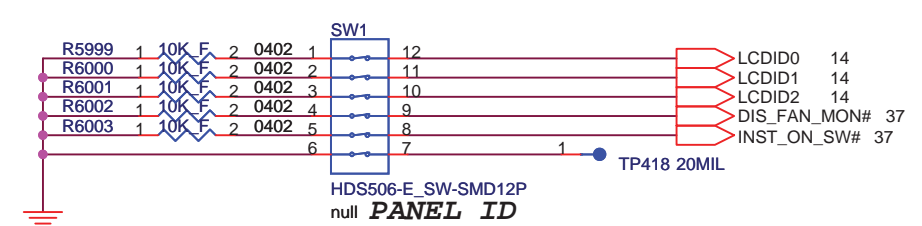
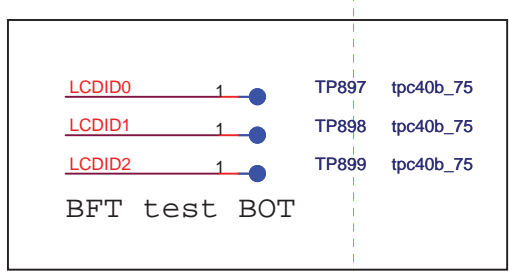
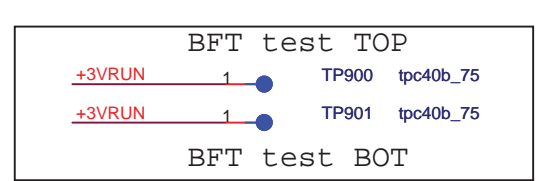




For rush current issue

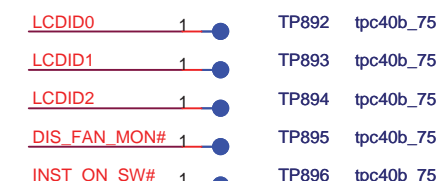


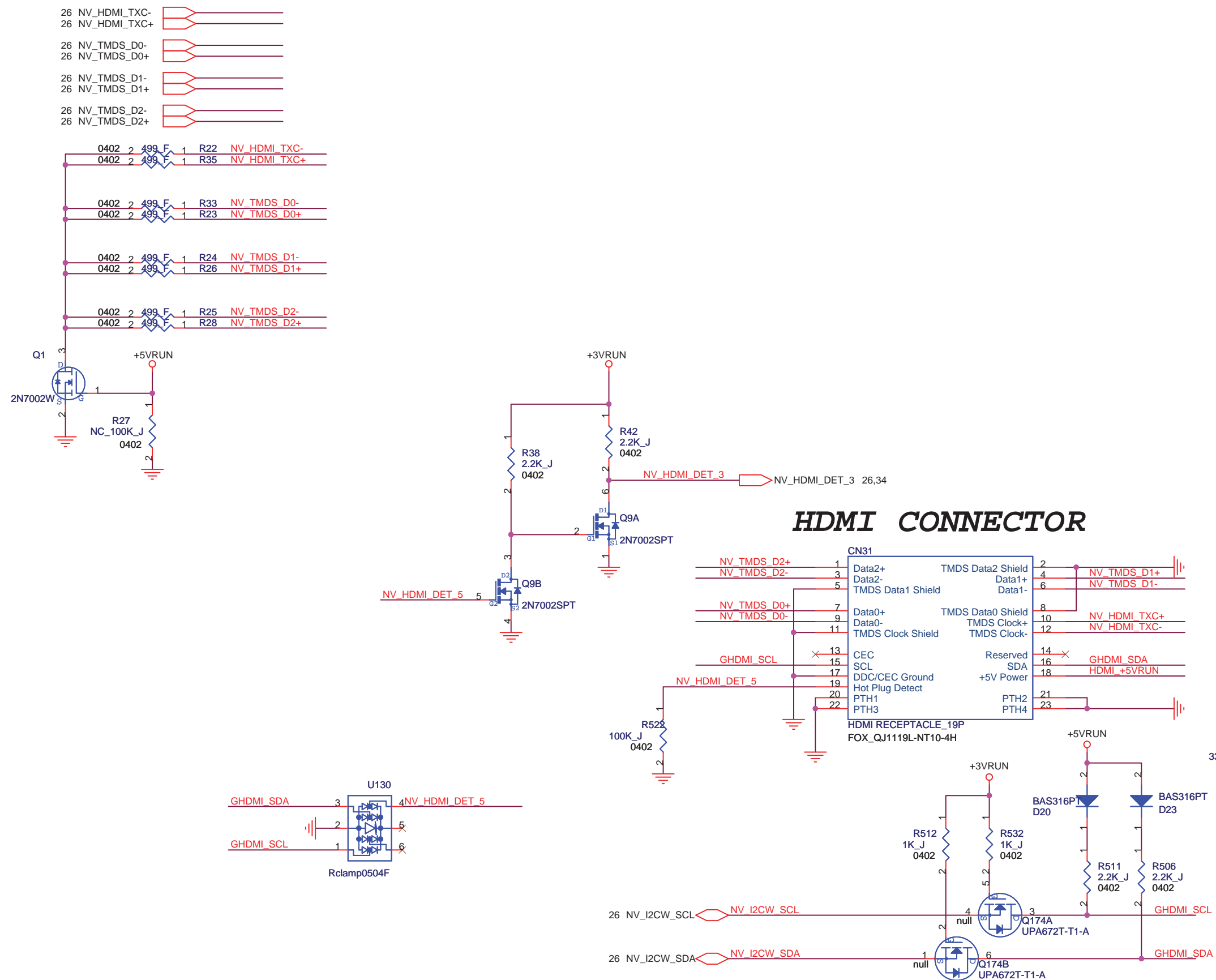
2009.10.23  
Delete J2,J3



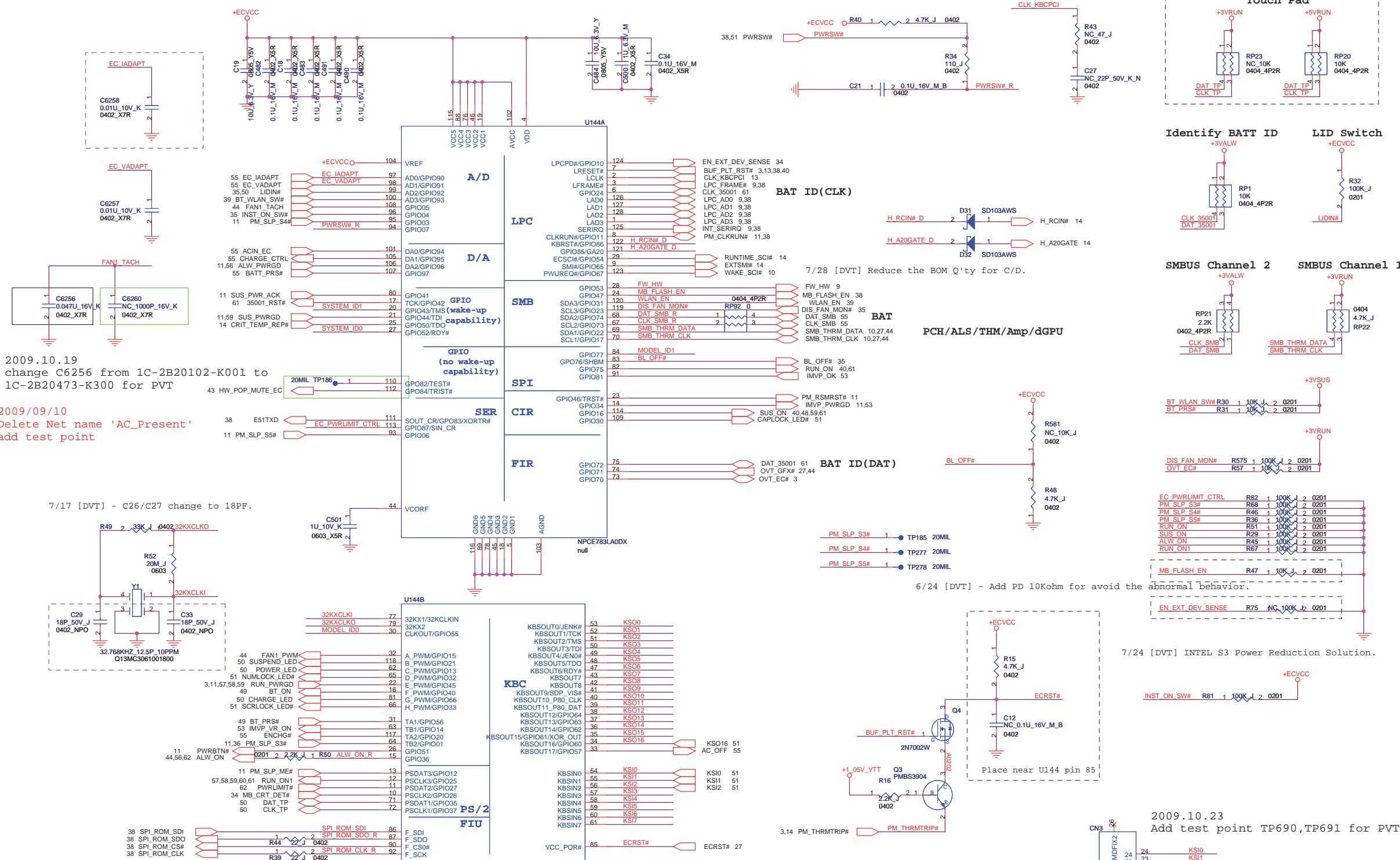
2009.10.23  
Add test point TP897,TP898,TP899 ,  
TP900,TP901 for PVT

	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
AUO B140XW02 V1	0	0	0	0
LGD LP140WH2-TLN1	0	0	1	0
SAMSUNG LTN140AT08	0	0	1	1
AUO B140RW02 V0	0	1	0	0
DISABLE FAN LOCK FUNCTION	0	X	X	X









2009.10.19  
change C6256 from 1C-2B20102-K001 to  
1C-2B20473-K300 for PVT

2009/09/10  
Delete Net name 'AC\_Present'  
add test point

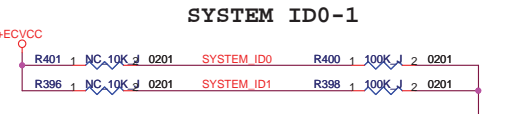
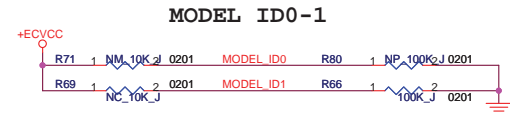
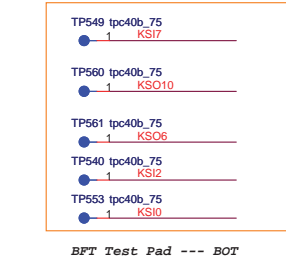
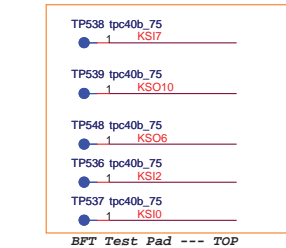
7/17 [DVT] - C26/C27 change to 18PF.

6/24 [DVT] - Add PD 10Kohm for avoid the abnormal behavior.

7/24 [DVT] INTEL S3 Power Reduction Solution.

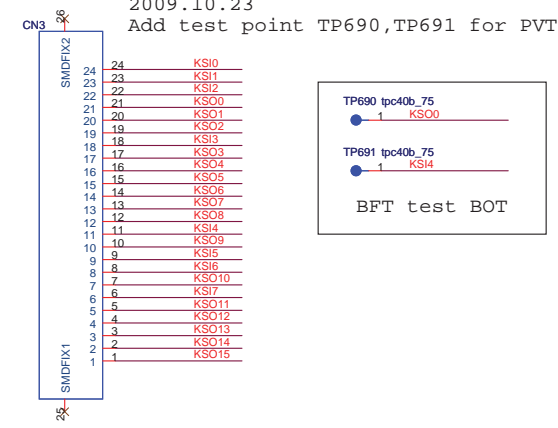
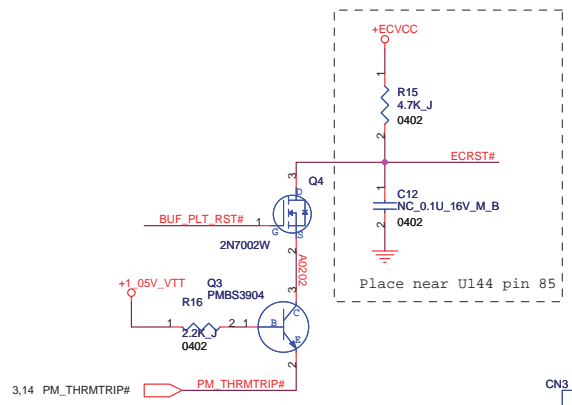
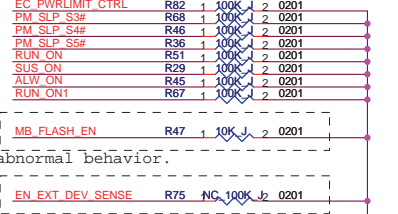
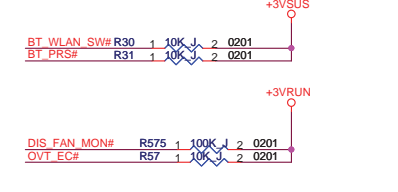
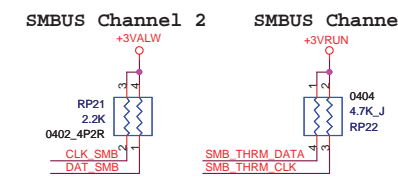
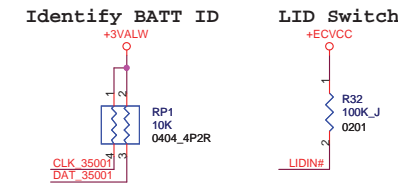
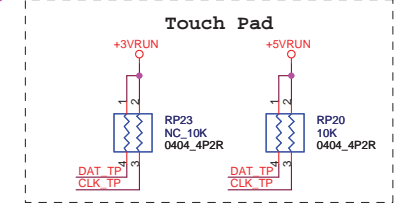
2009.10.23  
Add test point TP690,TP691 for PVT

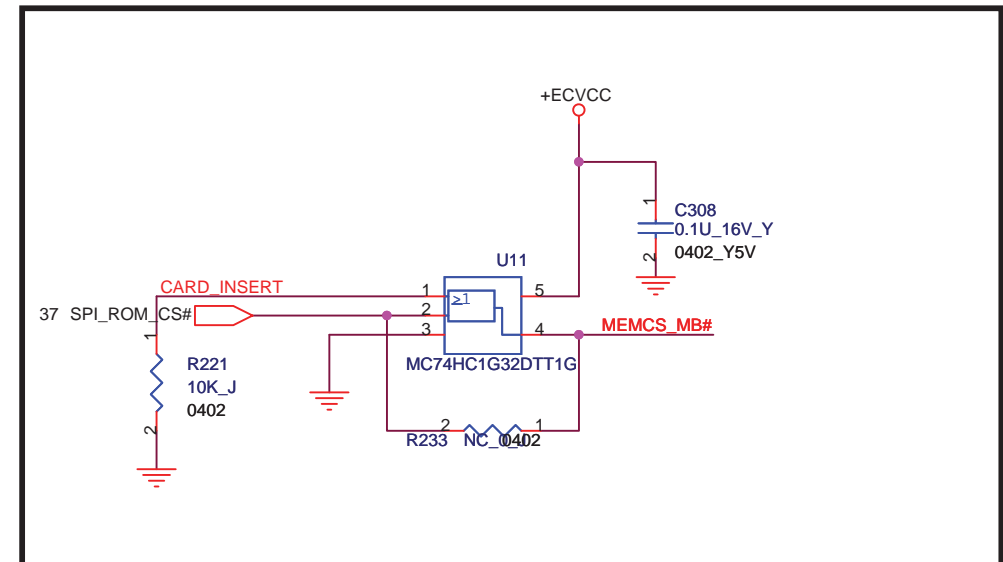
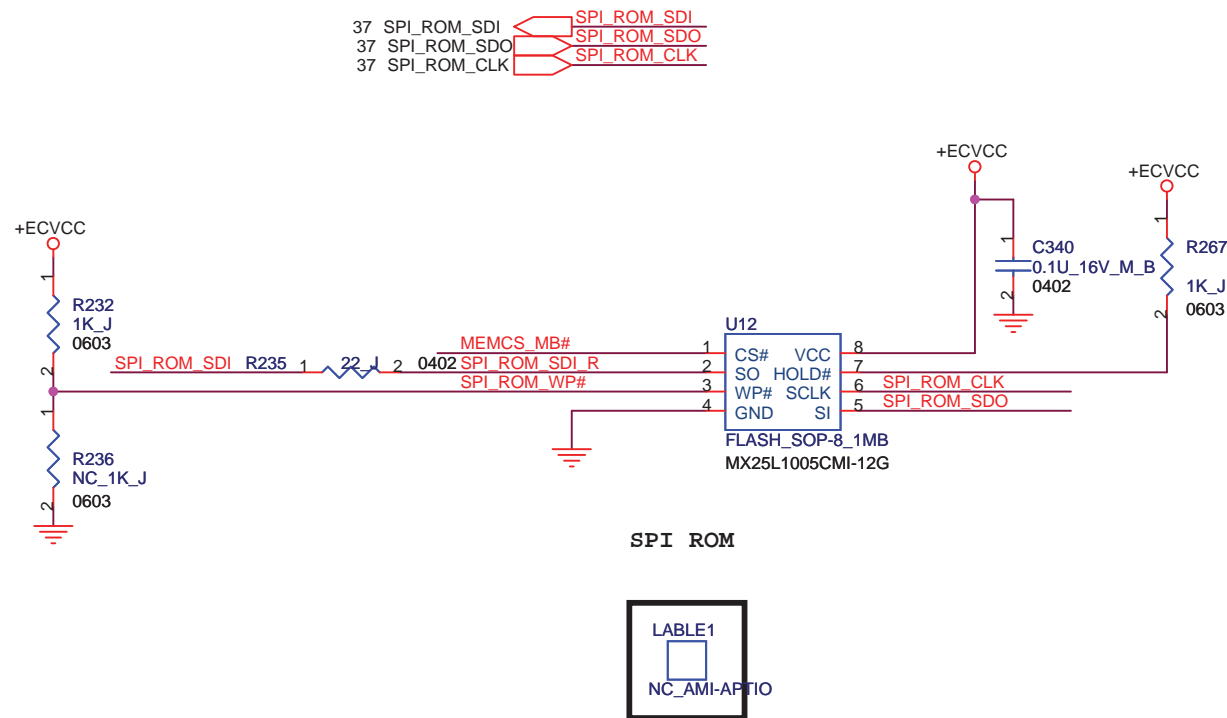
2009.10.22  
delete C468, C513, U25, R76, R55, R41, R73, C60,(NC) for PVT



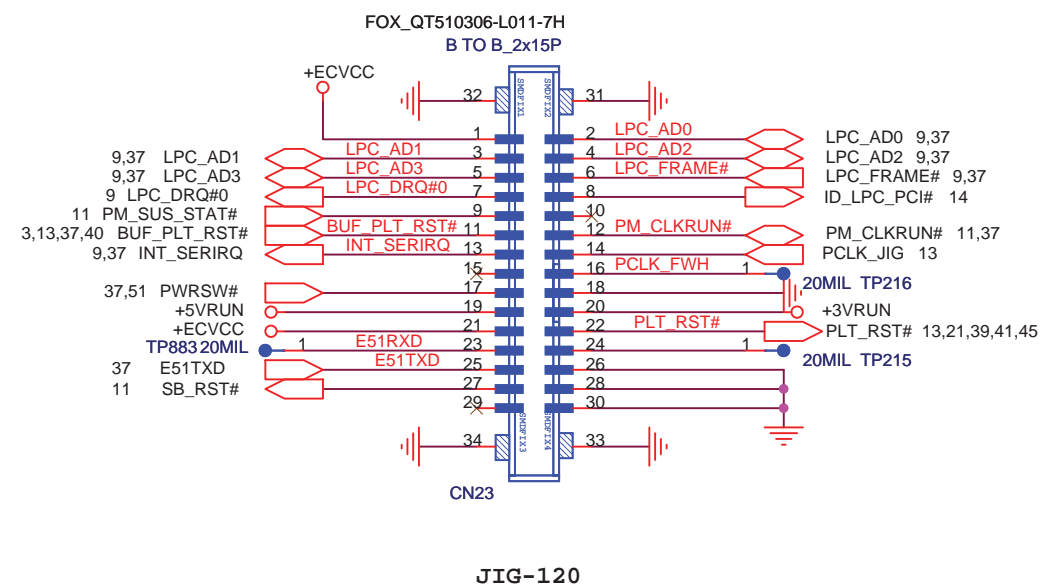
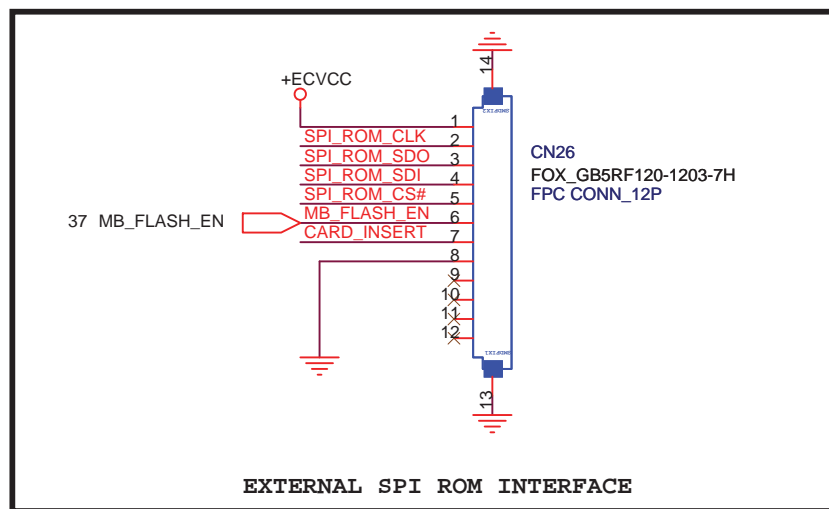
ID1 (Reserve)	ID0	SKU
0	0	SLI+N11P
0	1	SILEGO+N11M
1	0	
1	1	

ID1	ID0	SKU
0	0	M9A0
0	1	Reserve
1	0	Reserve
1	1	Reserve

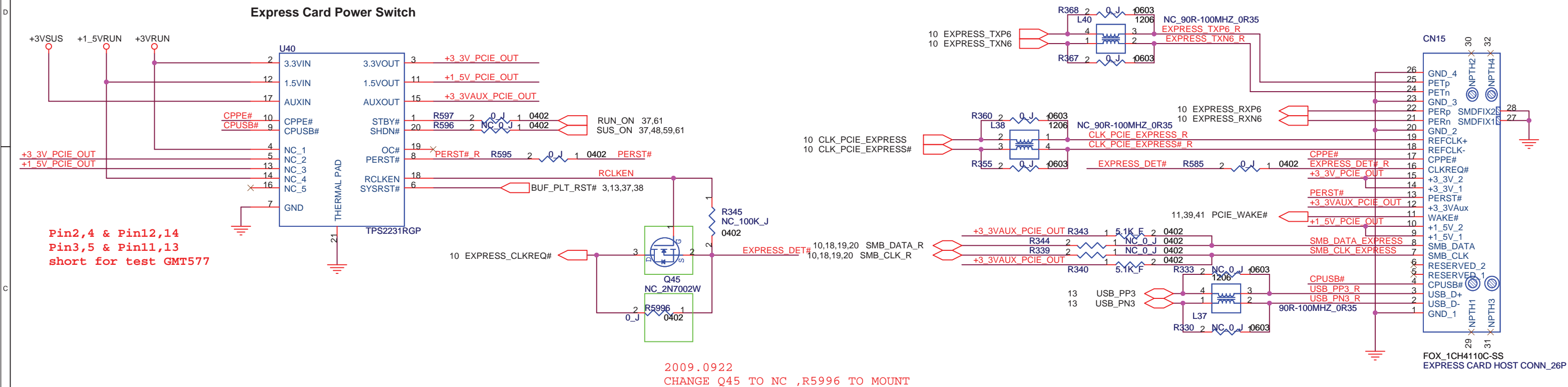




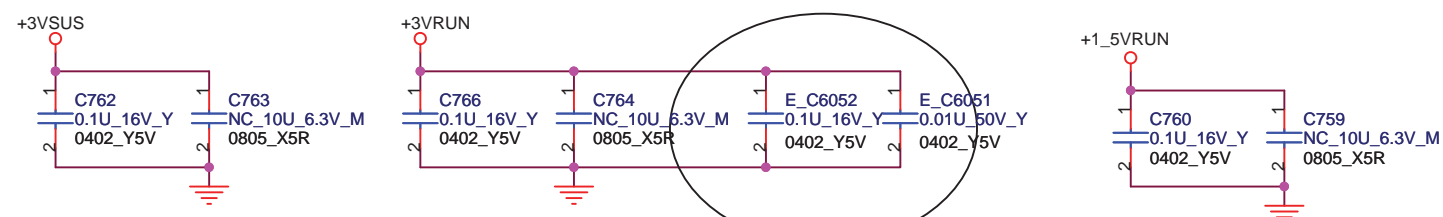
2009.10.23  
Delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518



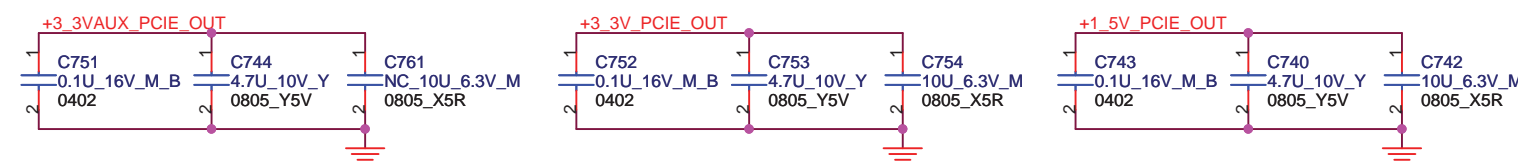
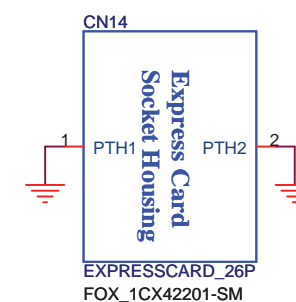




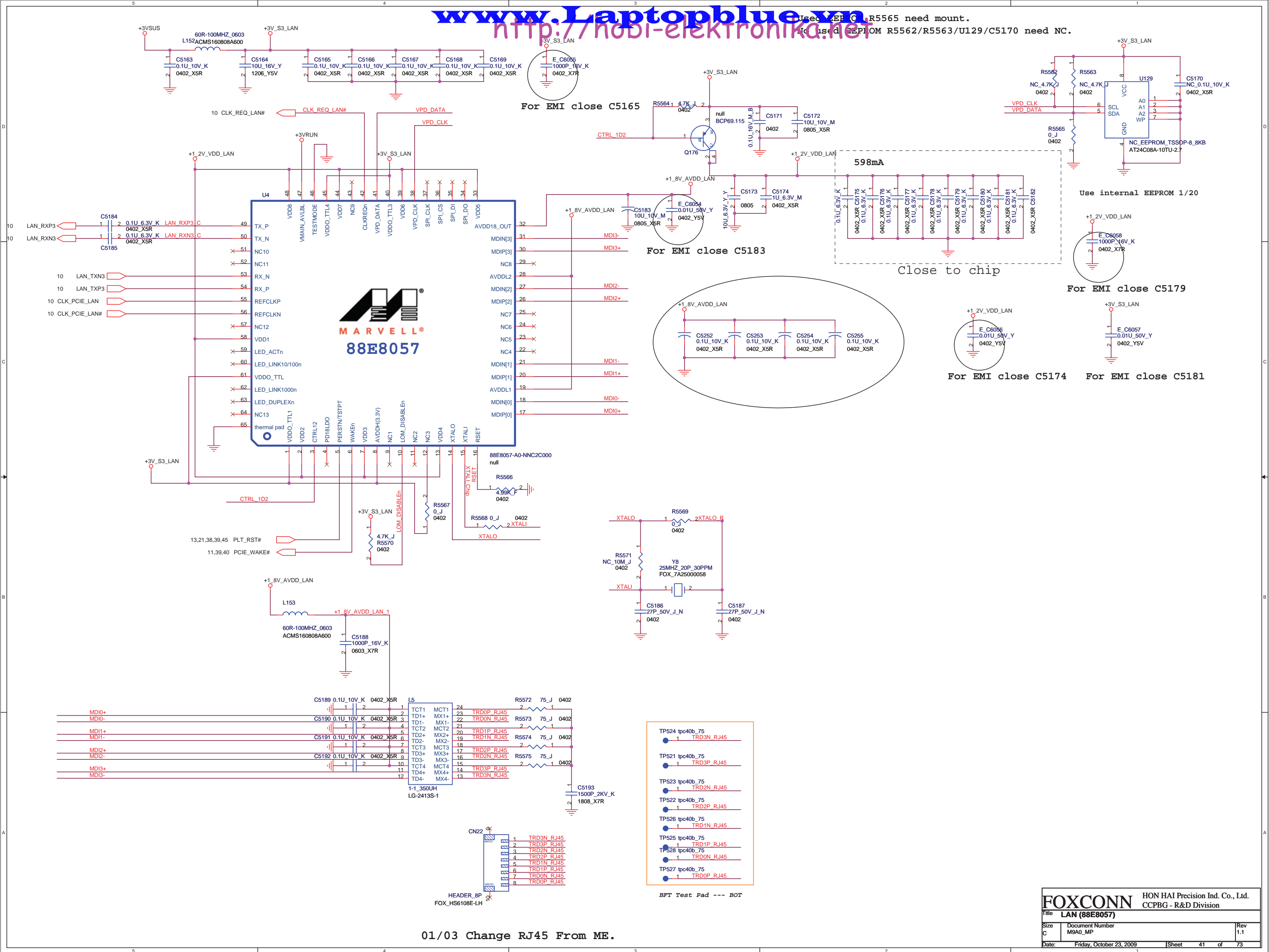
**Express Card Slot.**



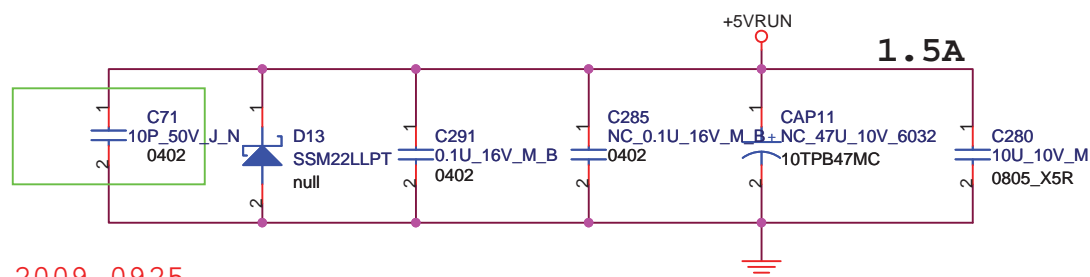
For EMI close C764



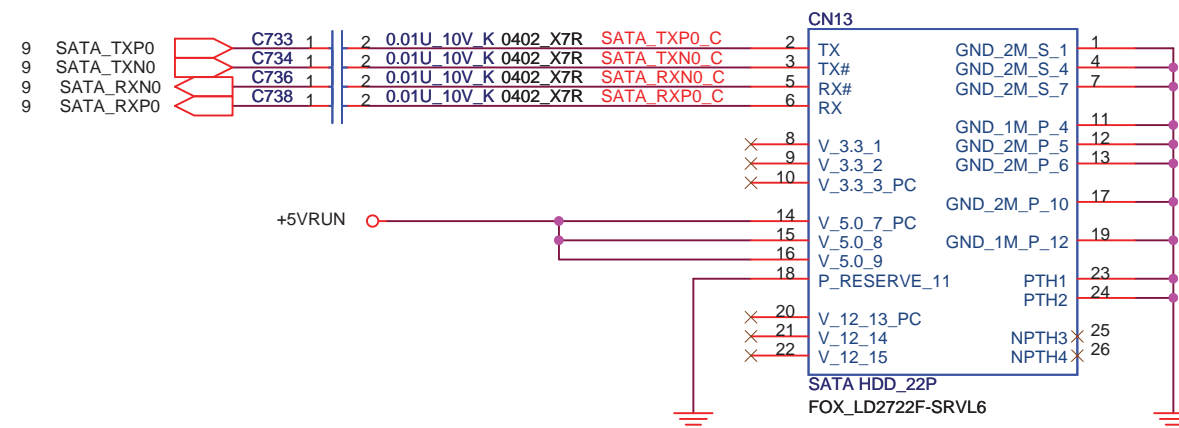




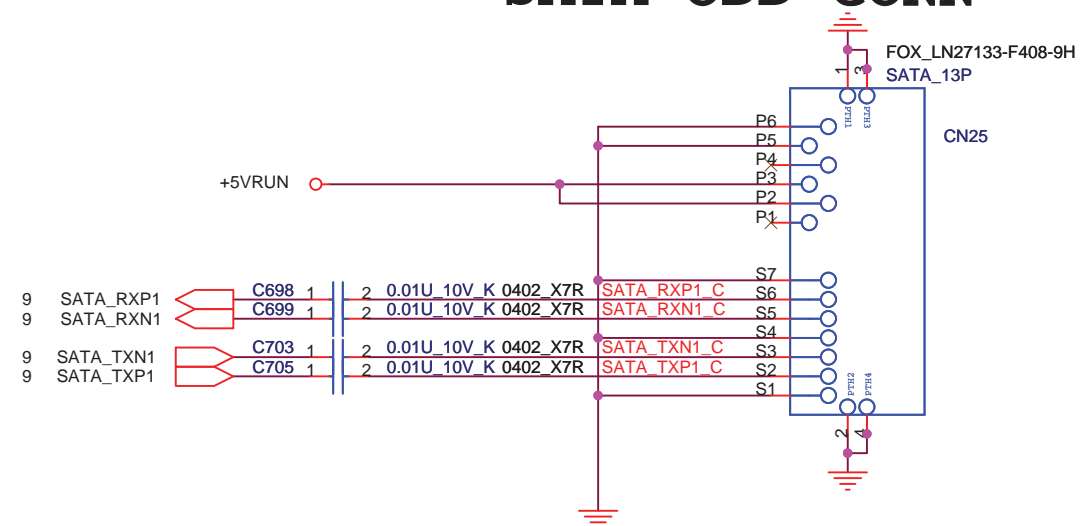
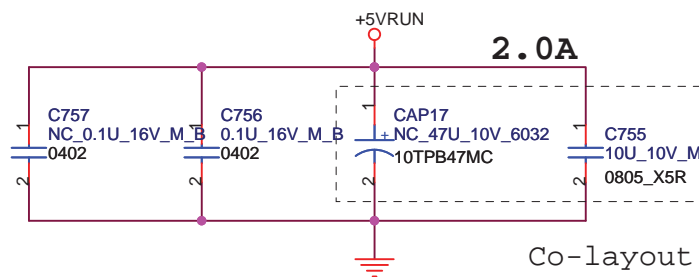
## SATA HDD CONN



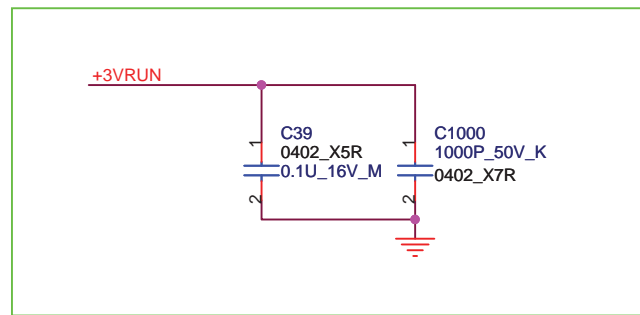
2009.0925  
Add C71 for RF request



## SATA ODD CONN

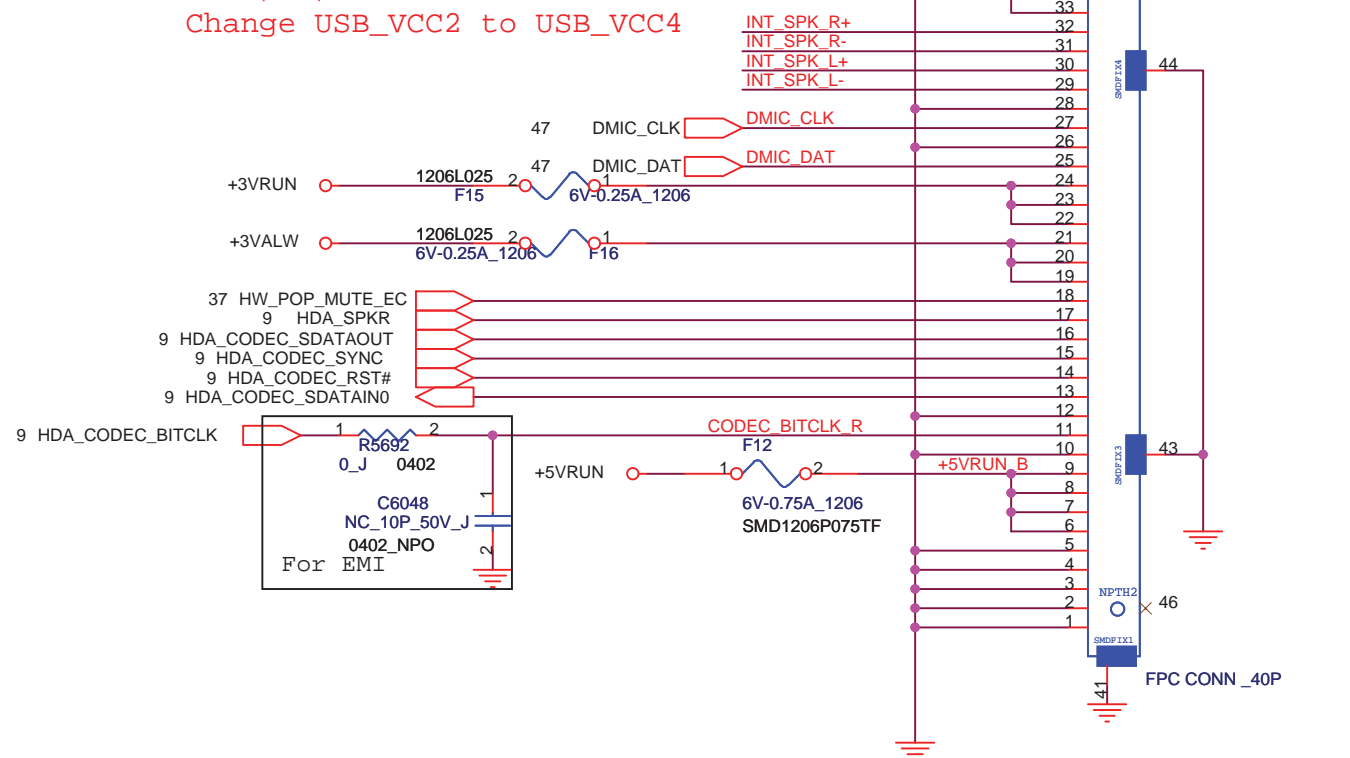


2009.0922  
CN25 change to Halogen Free

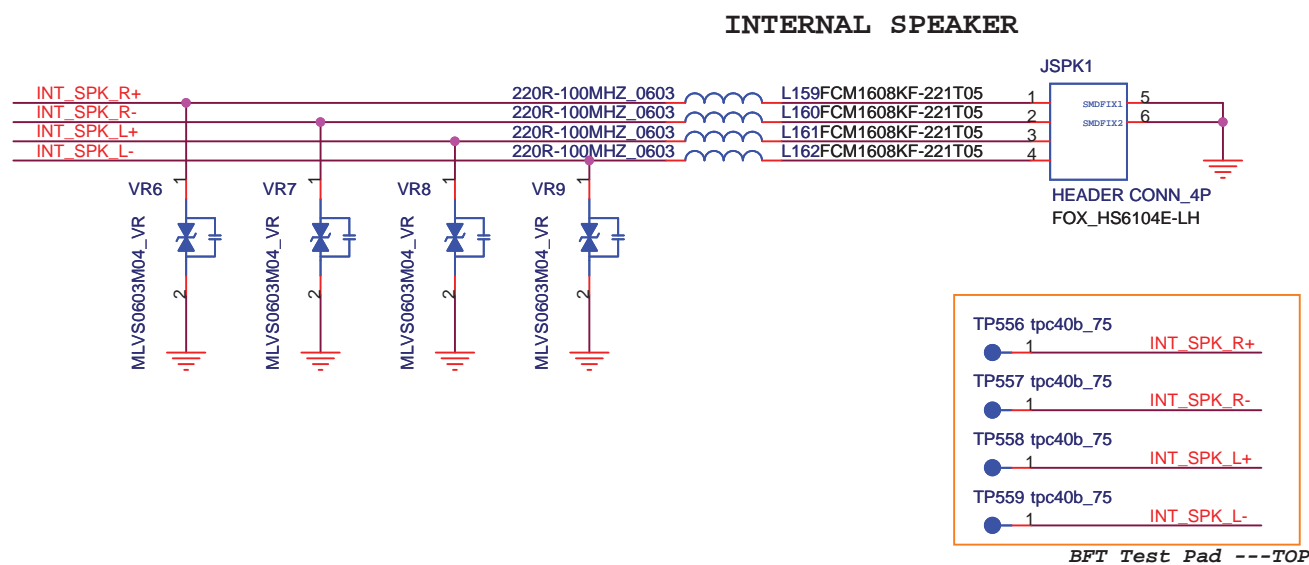


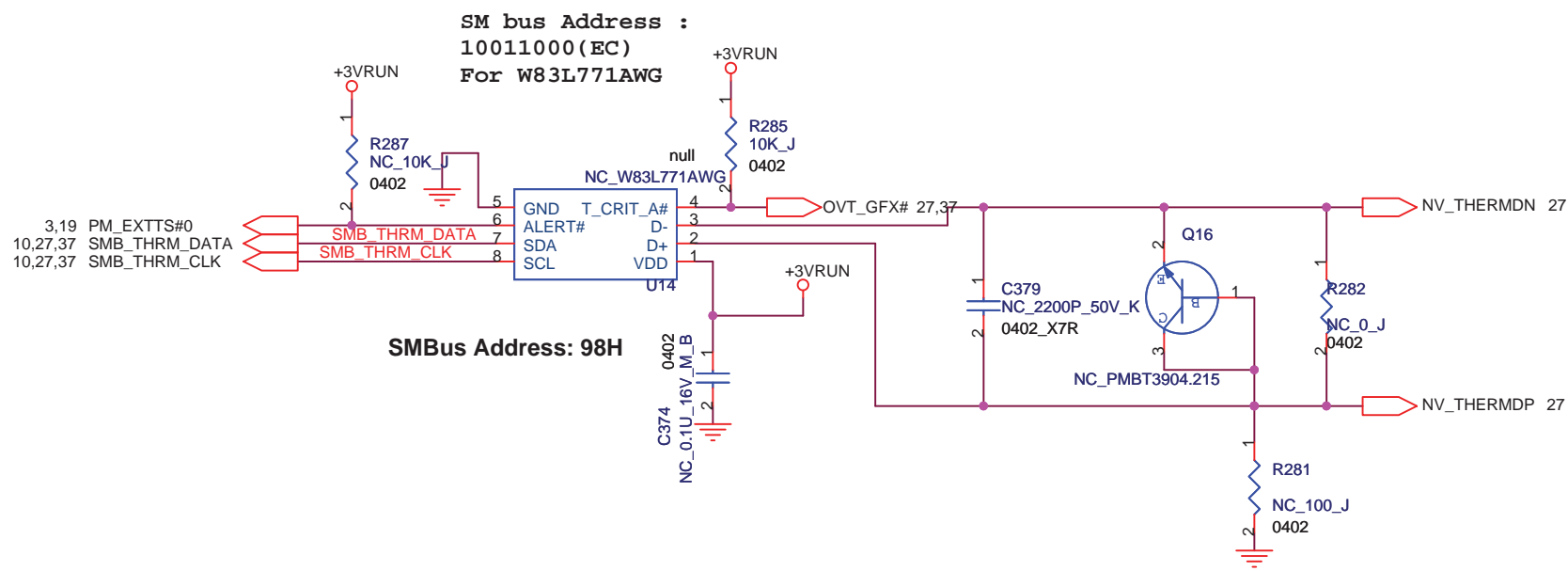
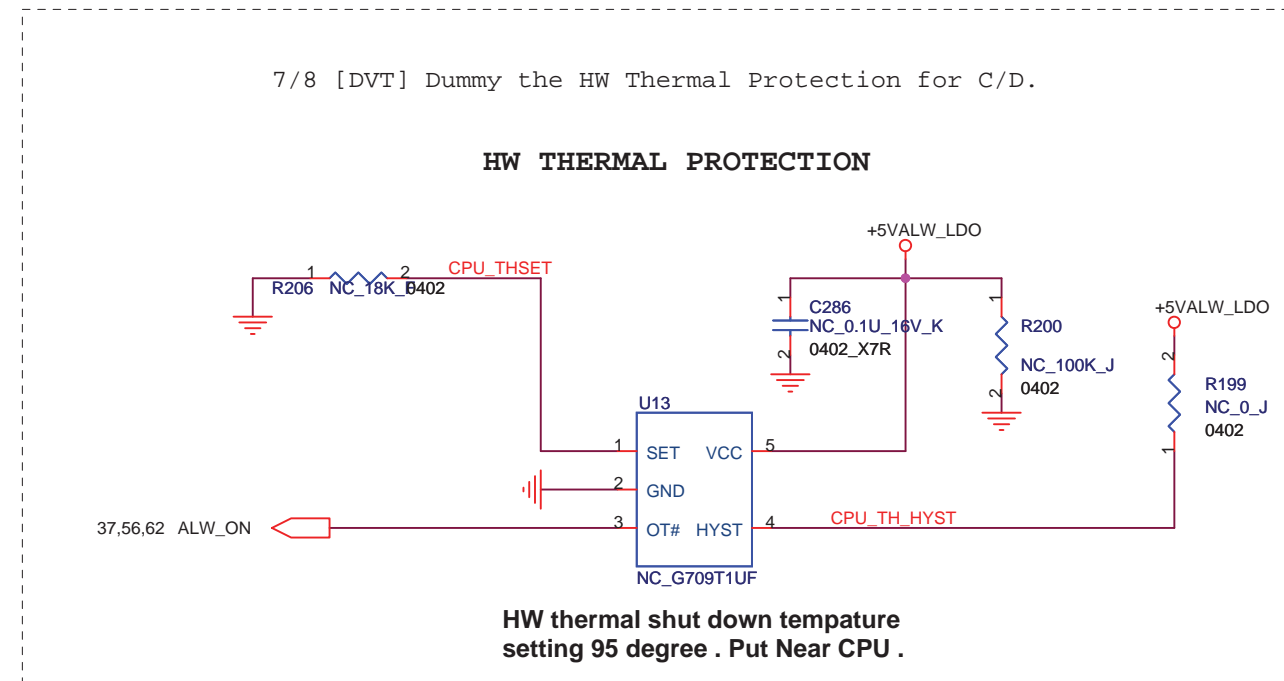
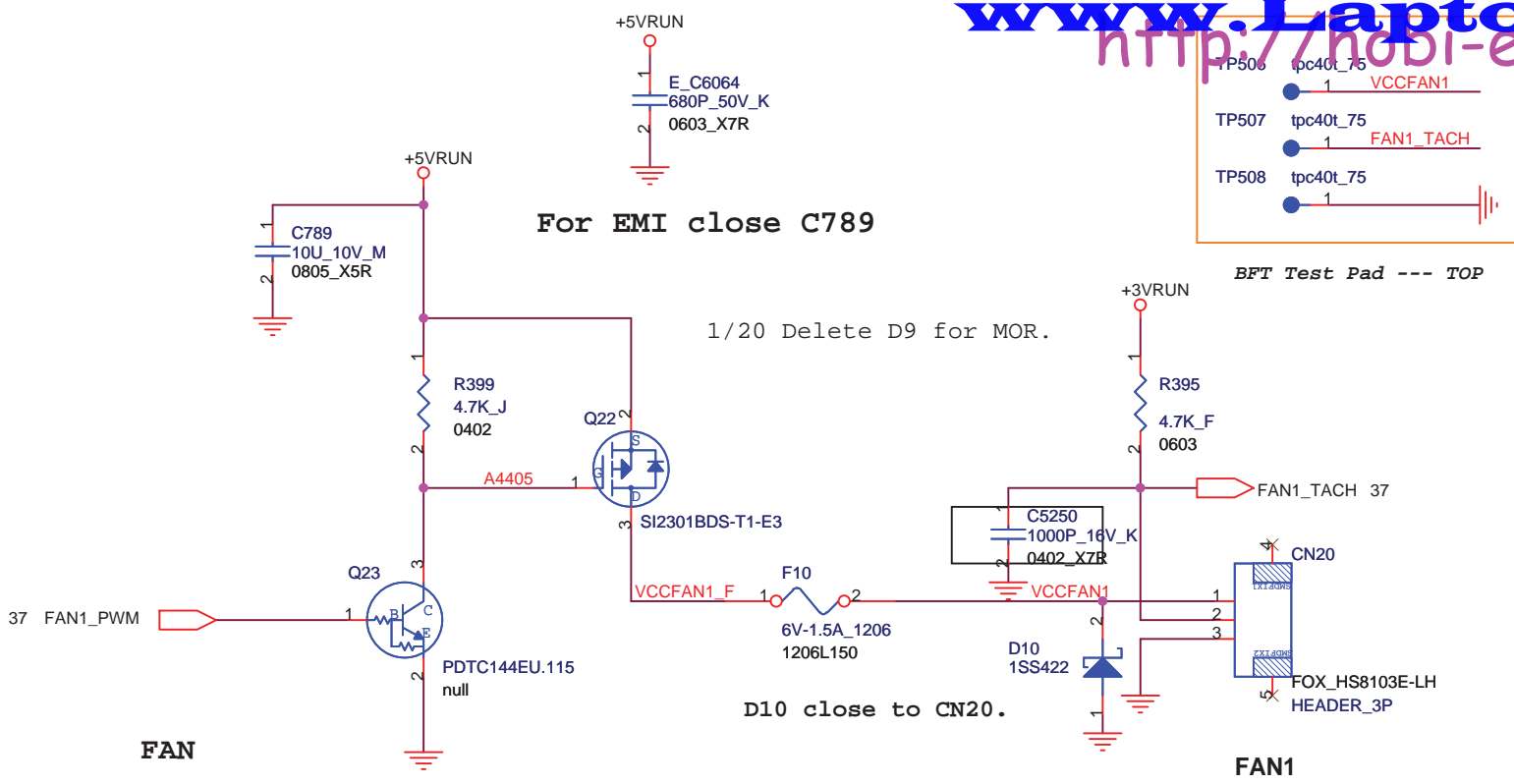
2009.0925  
ADD for EMI request

2009/09/19  
Change USB\_VCC2 to USB\_VCC4



## Audio & USB WTB CONN.







Delete parts for R5U231 protocol measurement.

Change CN35 From ME request.

Close to U21

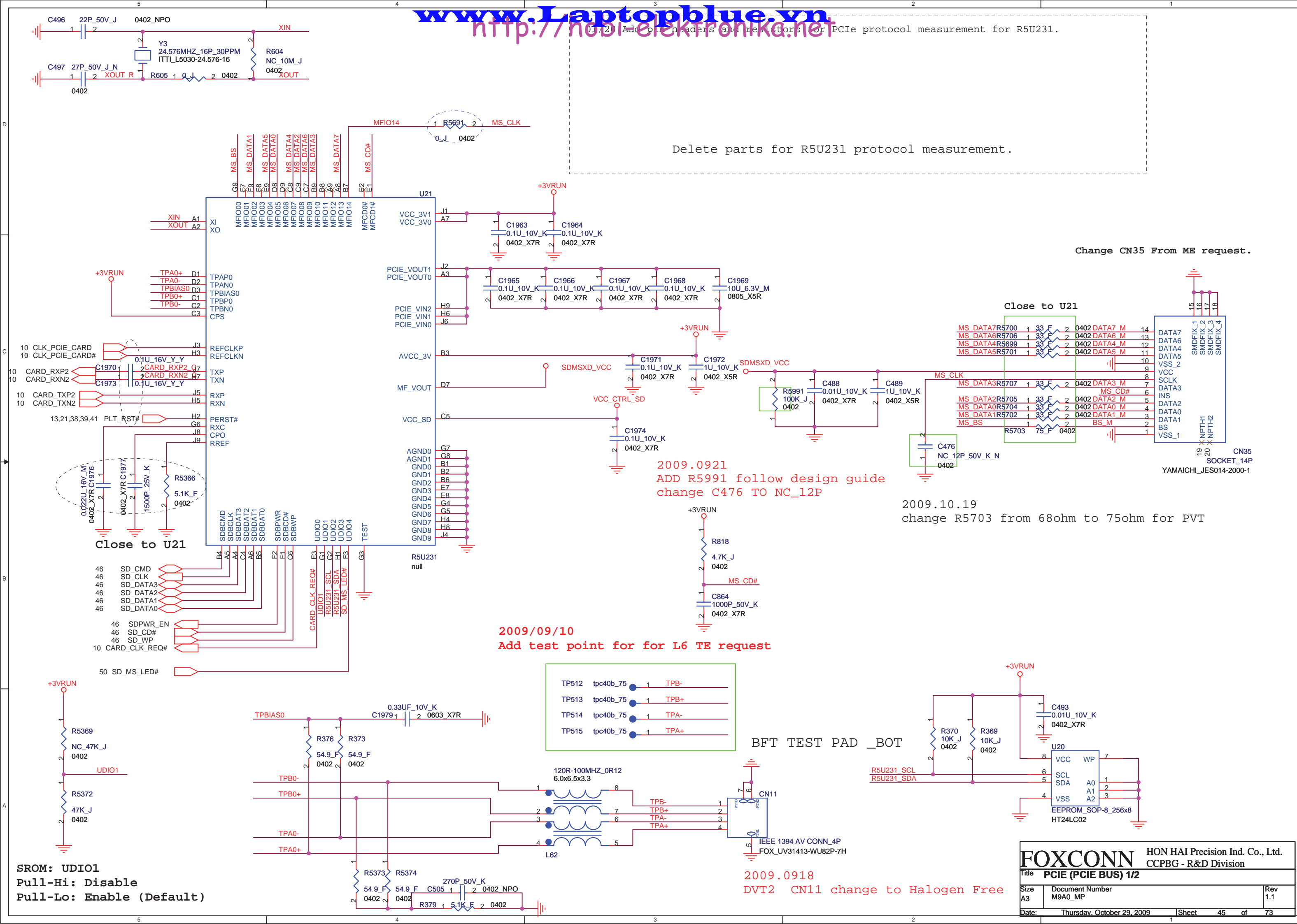
2009.10.19  
change R5703 from 68ohm to 75ohm for PVT

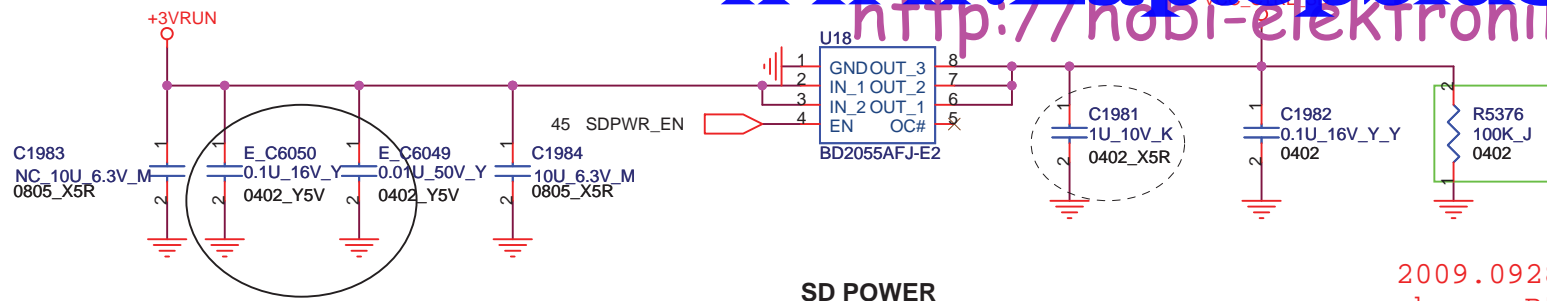
2009.0921  
ADD R5991 follow design guide  
change C476 TO NC\_12P

2009/09/10  
Add test point for for L6 TE request

BFT TEST PAD \_BOT

2009.0918  
DVT2 CN11 change to Halogen Free

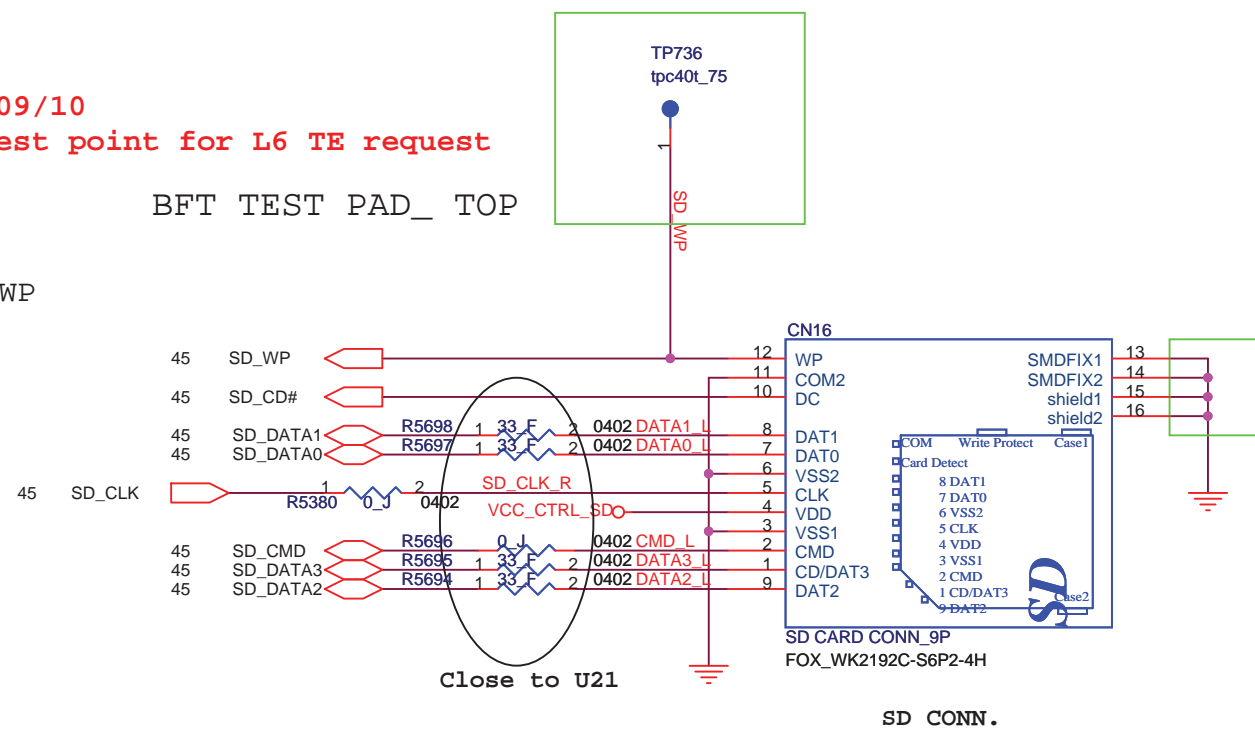
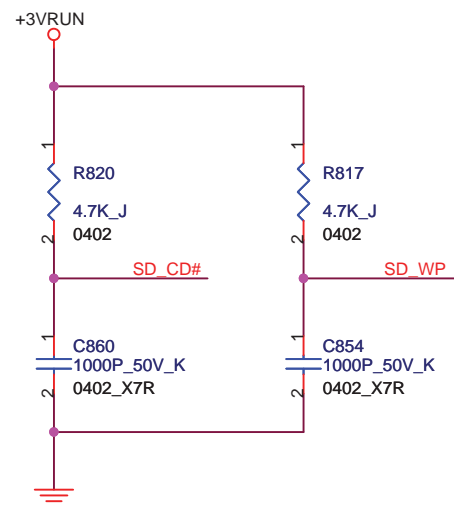




2009/09/10  
Add test point for L6 TE request

BFT TEST PAD\_ TOP

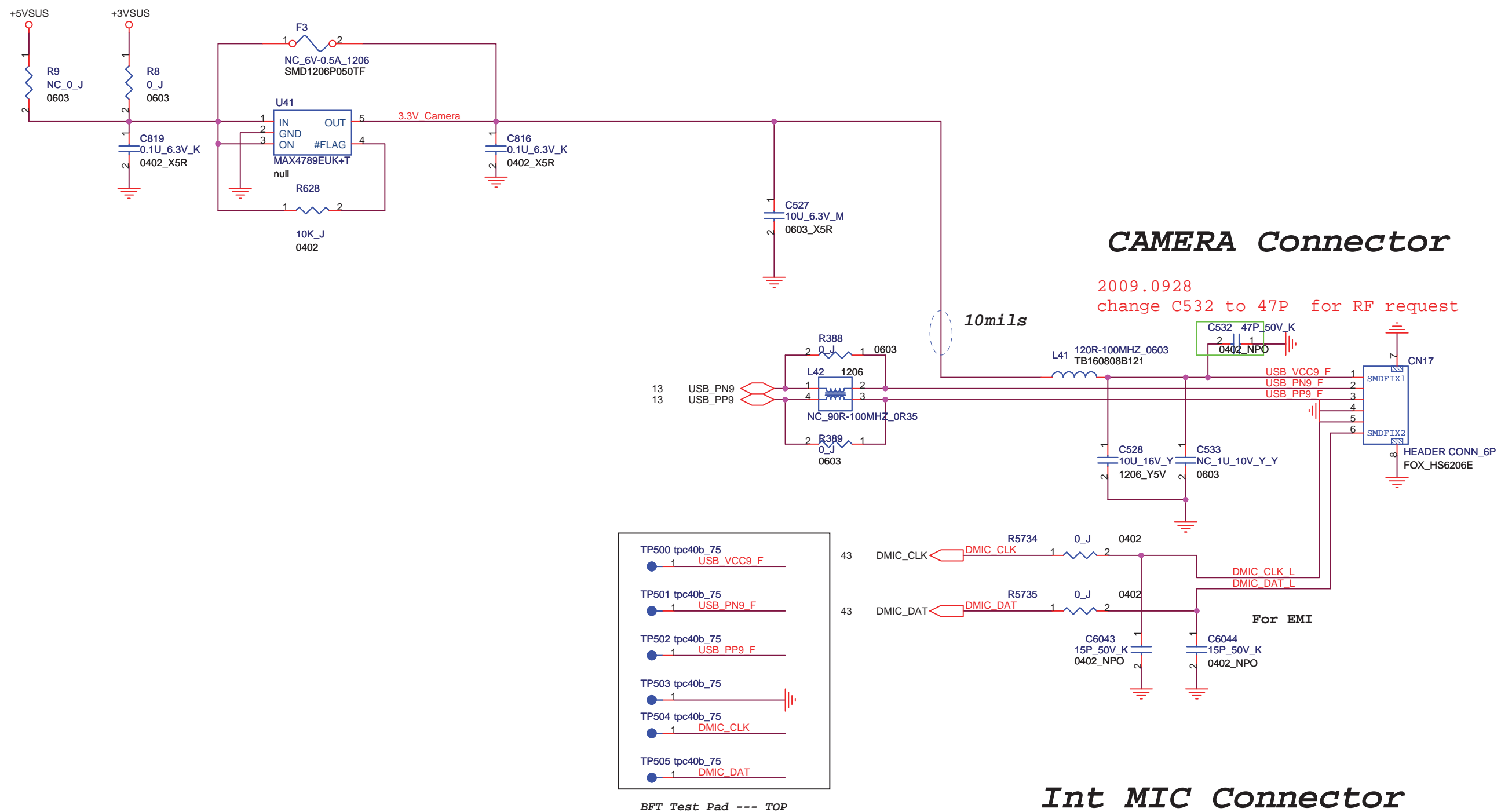
2009.10.23  
change net SD\_WP# to SD\_WP



For EMI

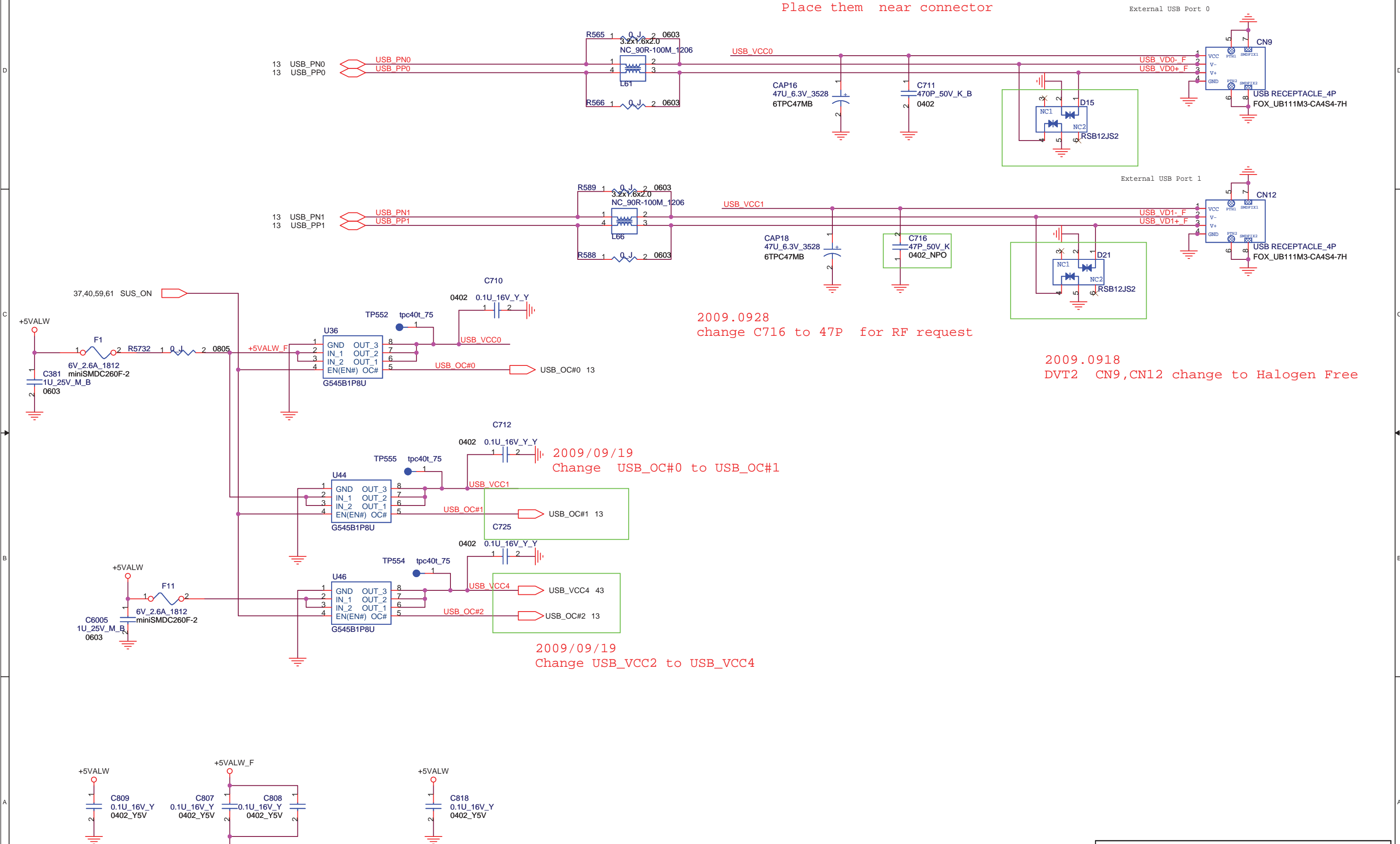


2009.0921  
change C1986 to 12p



2009.0921

change D15,D21from NC to mount  
Place them near connector



2009.0928

change C716 to 47P for RF request

2009.0918

DVT2 CN9,CN12 change to Halogen Free

2009/09/19

Change USB\_OC#0 to USB\_OC#1

2009/09/19

Change USB\_VCC2 to USB\_VCC4

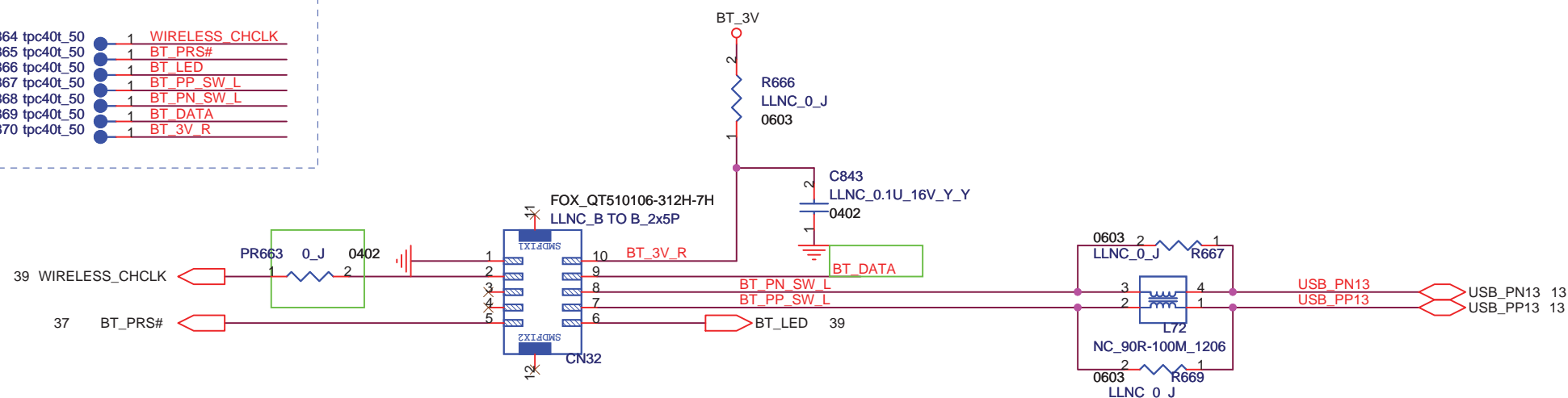


## Bluetooth connector

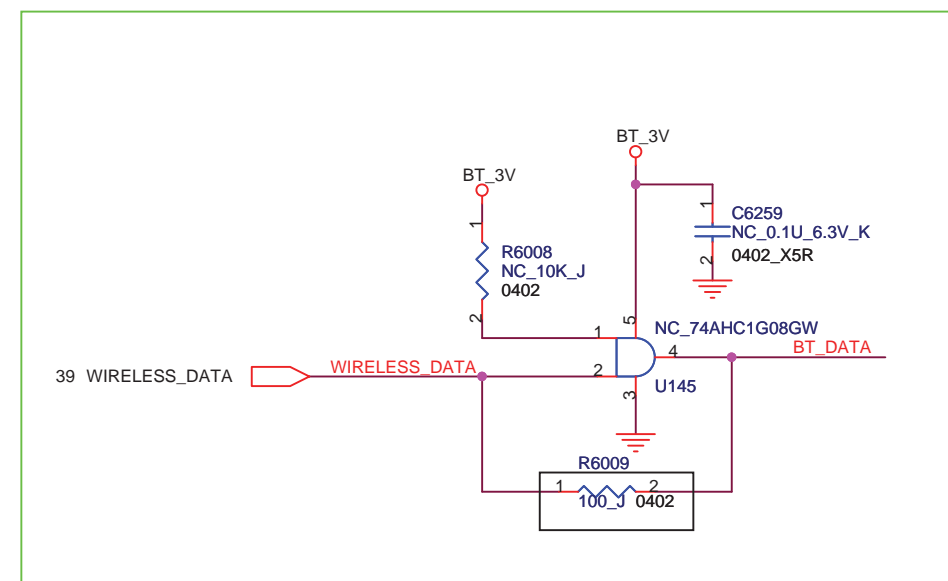
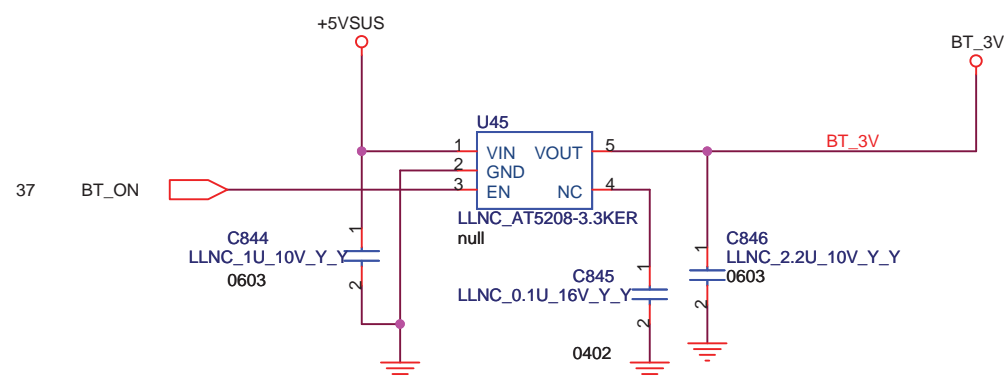
BOT Side

PVT

TP864 tpc40t_50	1	WIRELESS_CHCLK
TP865 tpc40t_50	1	BT_PR#
TP866 tpc40t_50	1	BT_LED
TP867 tpc40t_50	1	BT_PP_SW_L
TP868 tpc40t_50	1	BT_PN_SW_L
TP869 tpc40t_50	1	BT_DATA
TP870 tpc40t_50	1	BT_3V_R

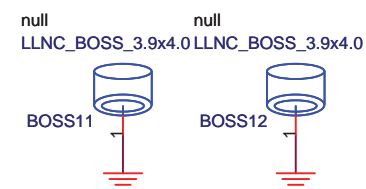


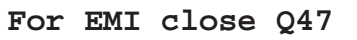
2009.0921  
WIRELESS\_DATA/WIRELESS\_CHCLK follow M930



2009.11.19  
Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

## Bluetooth





2009/09/10

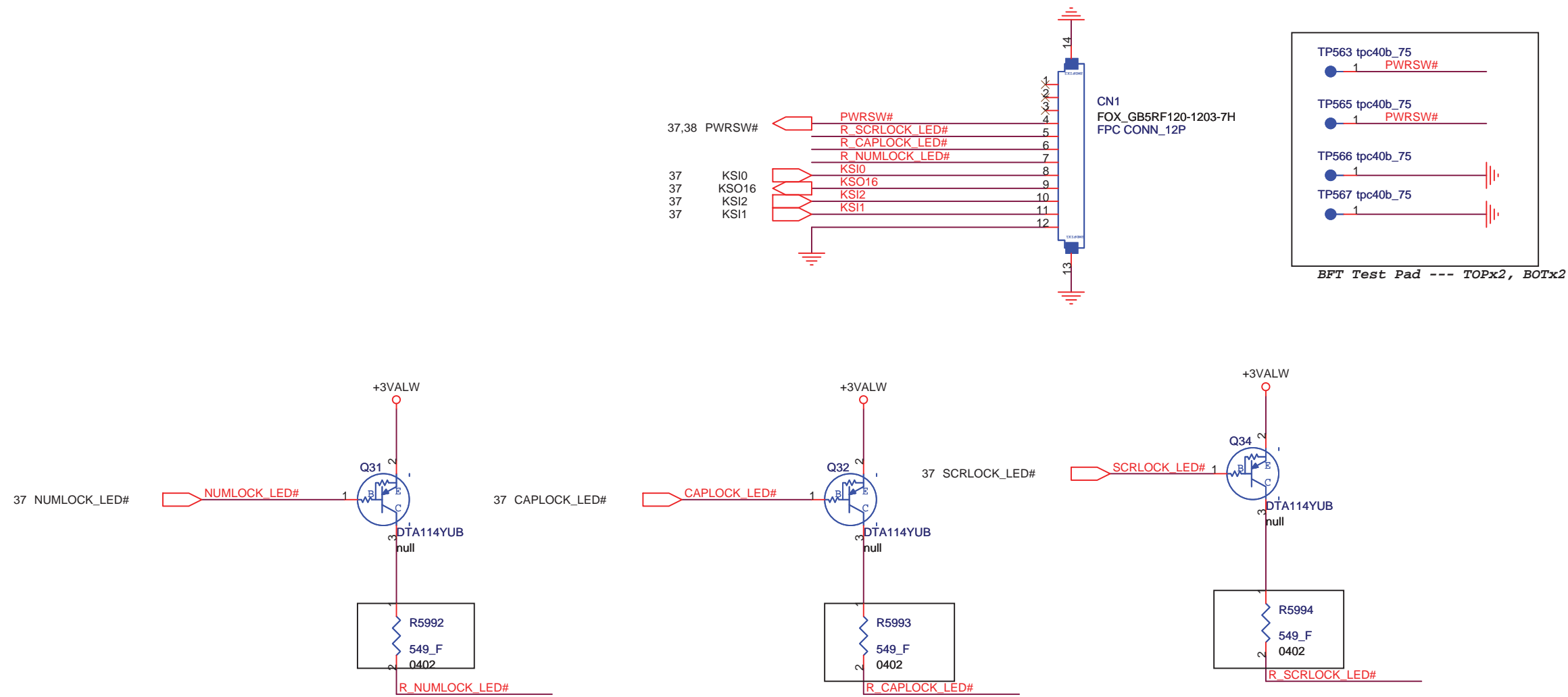
### Add test point for L6 TE request



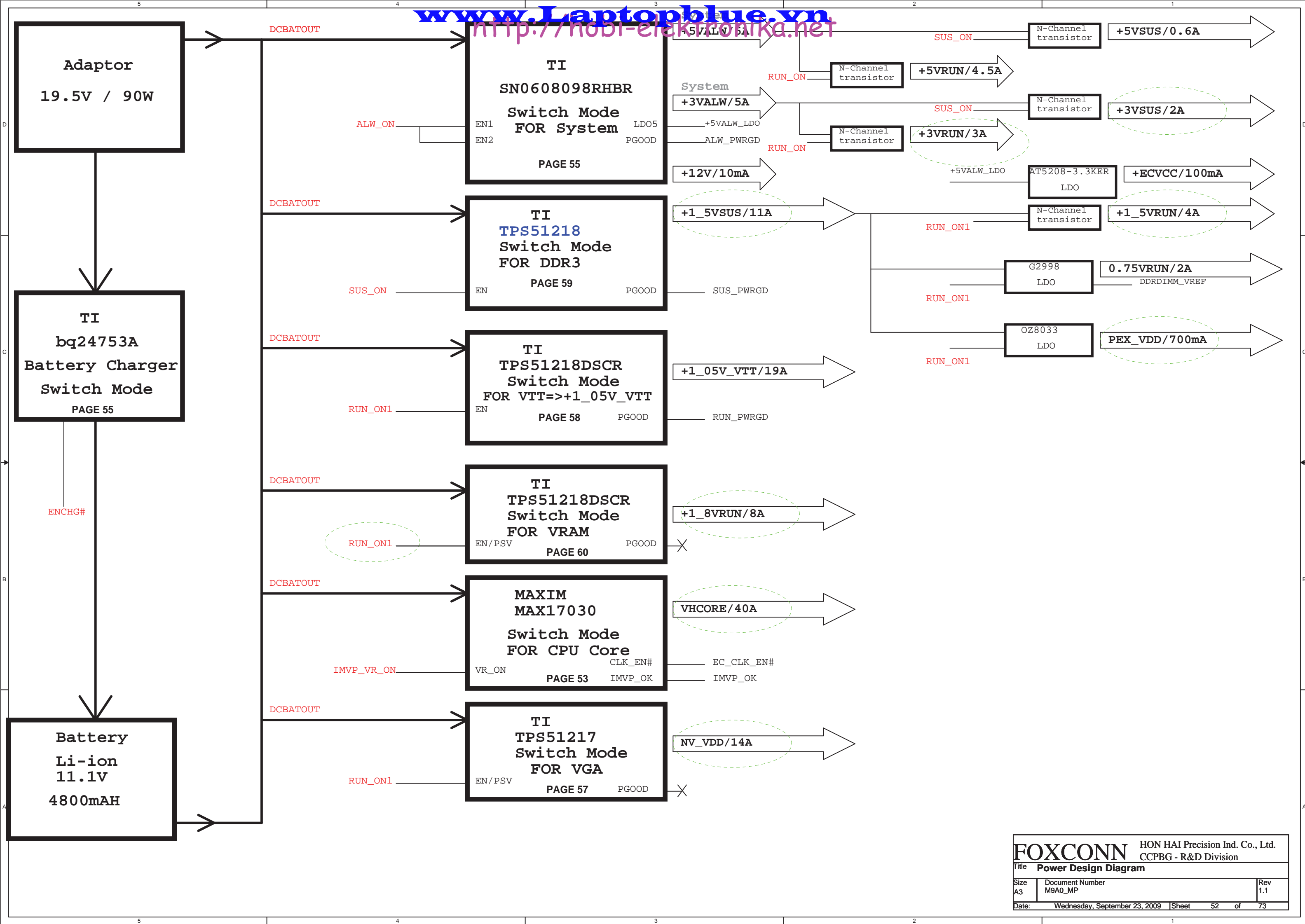
HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Size	Document Number	Rev
A3	M9A0_MP	1.1

Date:	Friday, October 23, 2009	Sheet	50	of	73
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2009.10.30  
change R5992,R5993,R5994 from 120ohm to 549ohm follow M870





2009.10.22  
change PC112 from 68U to 47U for power request

Place these CAPS  
close to FETs

4A

ODCBATOUT

2009.0929  
Add PC206 NC\_0.1U reserve  
for Return patch

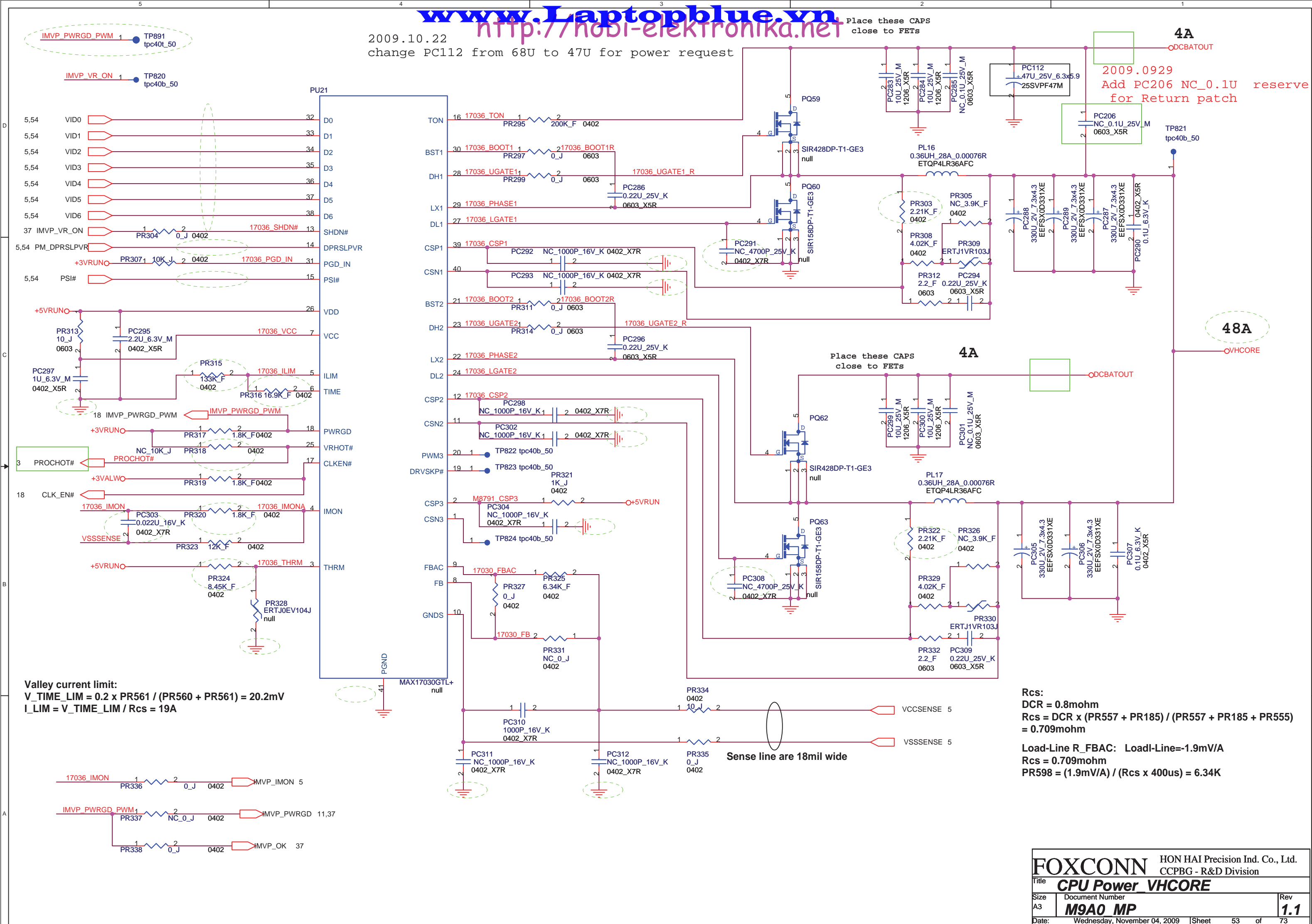
48A

OVHCORE

4A

ODCBATOUT

Rcs:  
DCR = 0.8mohm  
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm$   
Load-Line R\_FBAC: Load-Line=-1.9mV/A  
 $Rcs = 0.709mohm$   
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$



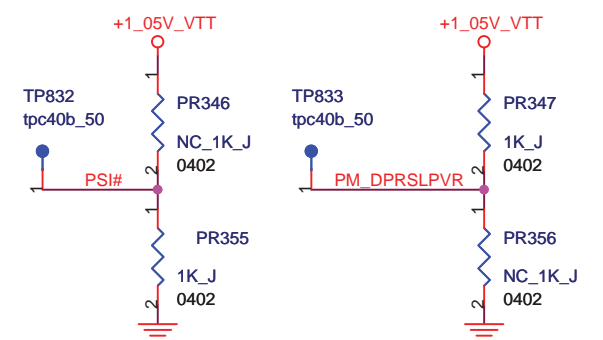
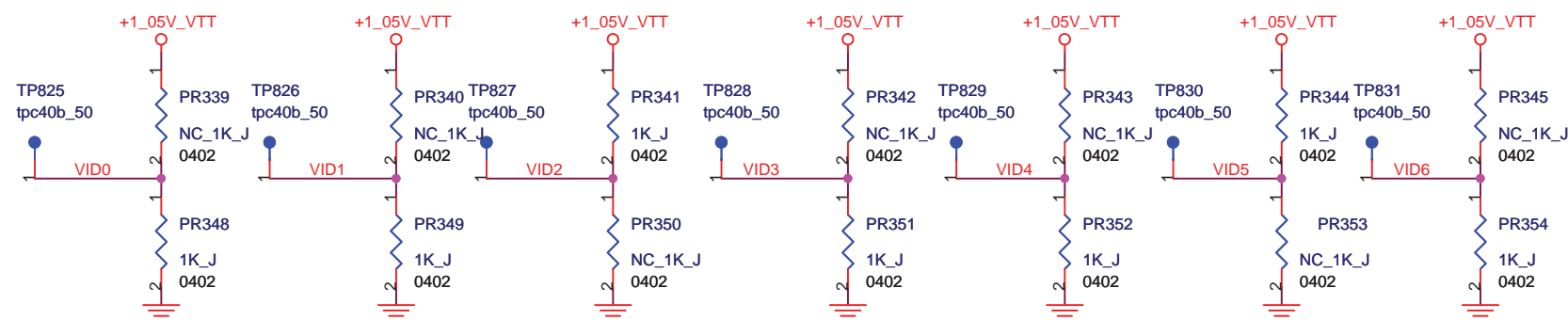
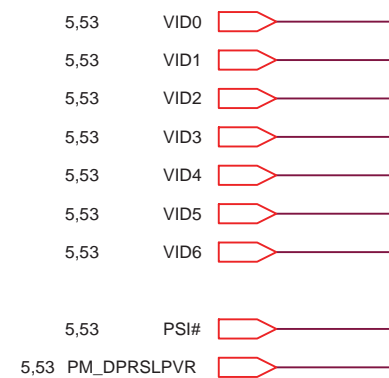
Valley current limit:  
 $V\_TIME\_LIM = 0.2 \times PR561 / (PR560 + PR561) = 20.2mV$   
 $I\_LIM = V\_TIME\_LIM / Rcs = 19A$

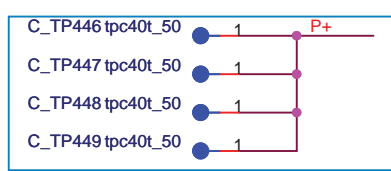
Sense line are 18mil wide

Default value of VID [6:0] = [ 0100100] ,   PSI = 0   ,   PROC\_DPRSLPVR = 1

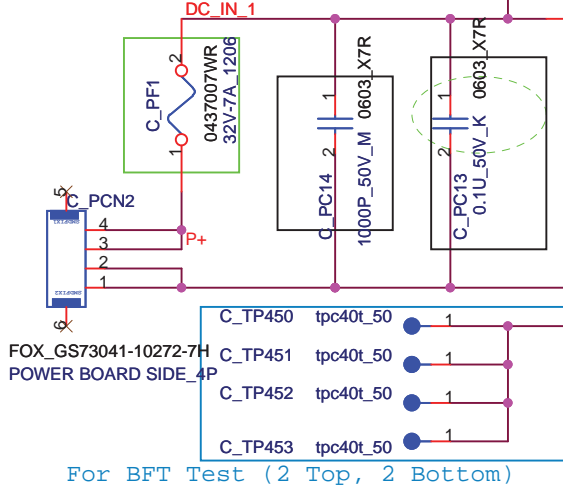
Market Segment Selection MSID[2:0] = [100] (SV)

- 416056\_416056\_Ard\_EDS\_Rev.1.1 - 403779\_Clarksfield\_MPG\_Rev1.5

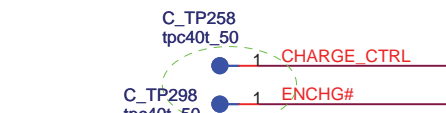




For BFT Test (2 Top, 2 Bottom)

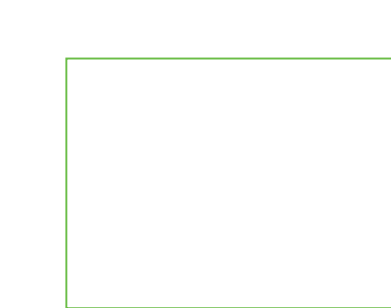


For BFT Test (2 Top, 2 Bottom)



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

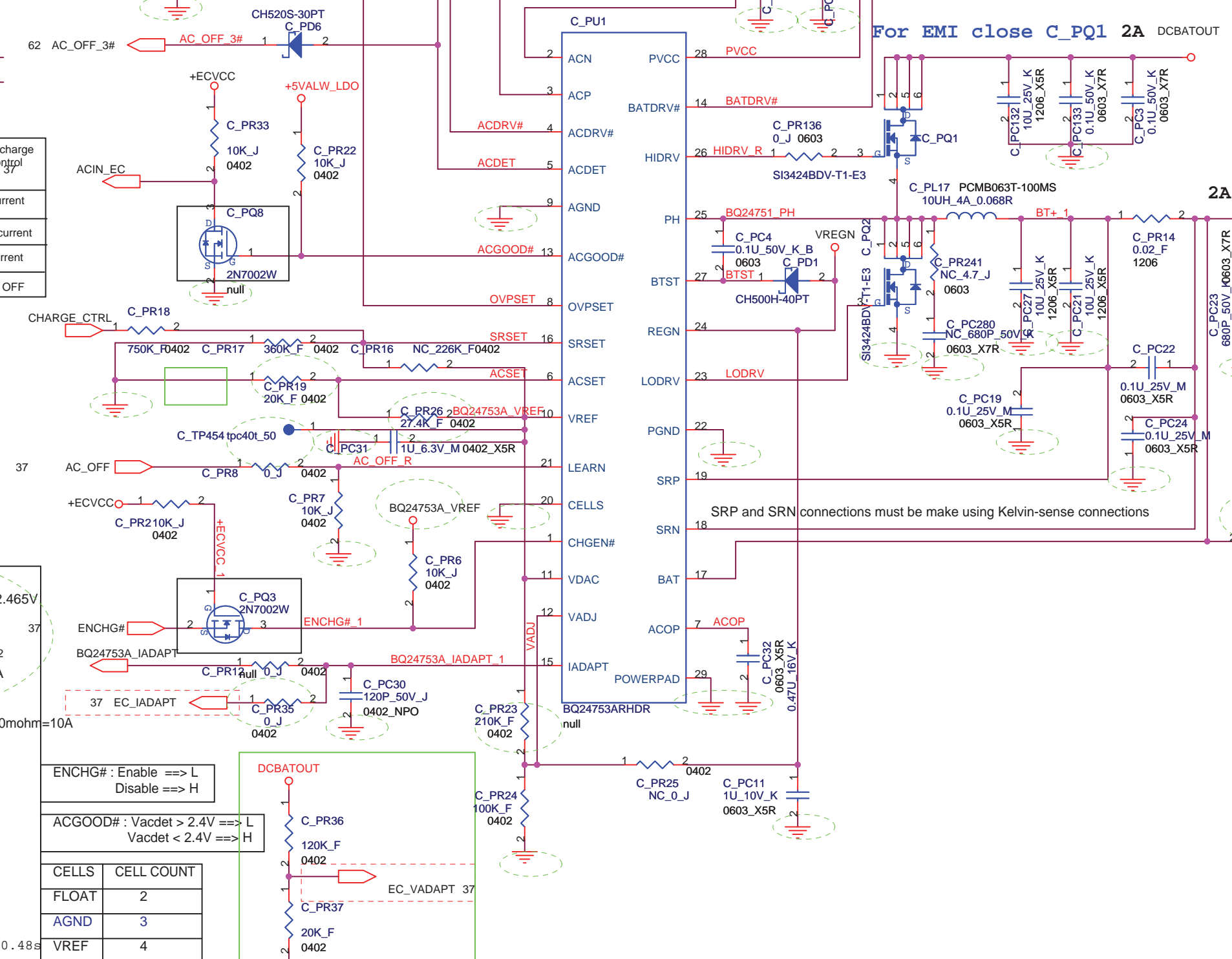


$VREF=3.3V \rightarrow VDAC$   
 $Vbat=cell\ count * [4V + 0.512 * (Vadj/Vvadc)] = 12.465V$   
 (Vbat=4.2V when Vadj connected to REGN)  
 $Icharge=(Vsrset/Vvdac) * (0.1/PR15) = 1.5A$   
 $Iadapater=(Vacset/Vvdac) * (0.1/PR657) = 4.22A$   
 $IADAPT=(Vacp - Vacn) * 20$   
 Input OCP:  $(VACP-VACN)max/PR4=100mV/10mohm=10A$   
 Input OVP : 22.2V  
 Input UVP : 17V  
 Battery OCP :  $Icharge * 145\%$   
 Battery OVP :  $Vbat * 104\%$   
 Pre-charge :  $<2.9V/cell \implies Icharge/8$   
 Battery OTP :  $Tshut=155\ degree$   
 $Fsw : 300KHz$   
 Time that input current limit :  
 $t=(Cacop * 2) / (18uA/V * V(PVCC-ACP)) = 0.48s$

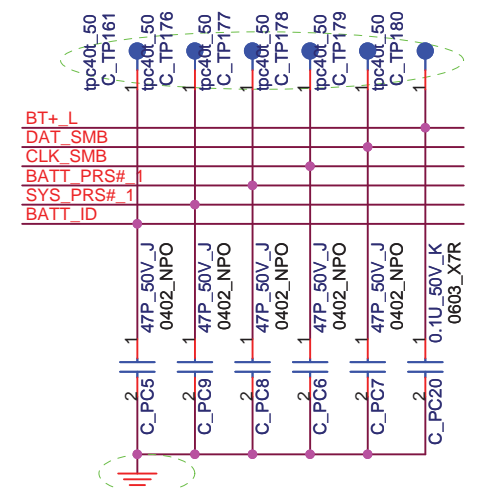
ENCHG# : Enable ==> L  
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L  
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

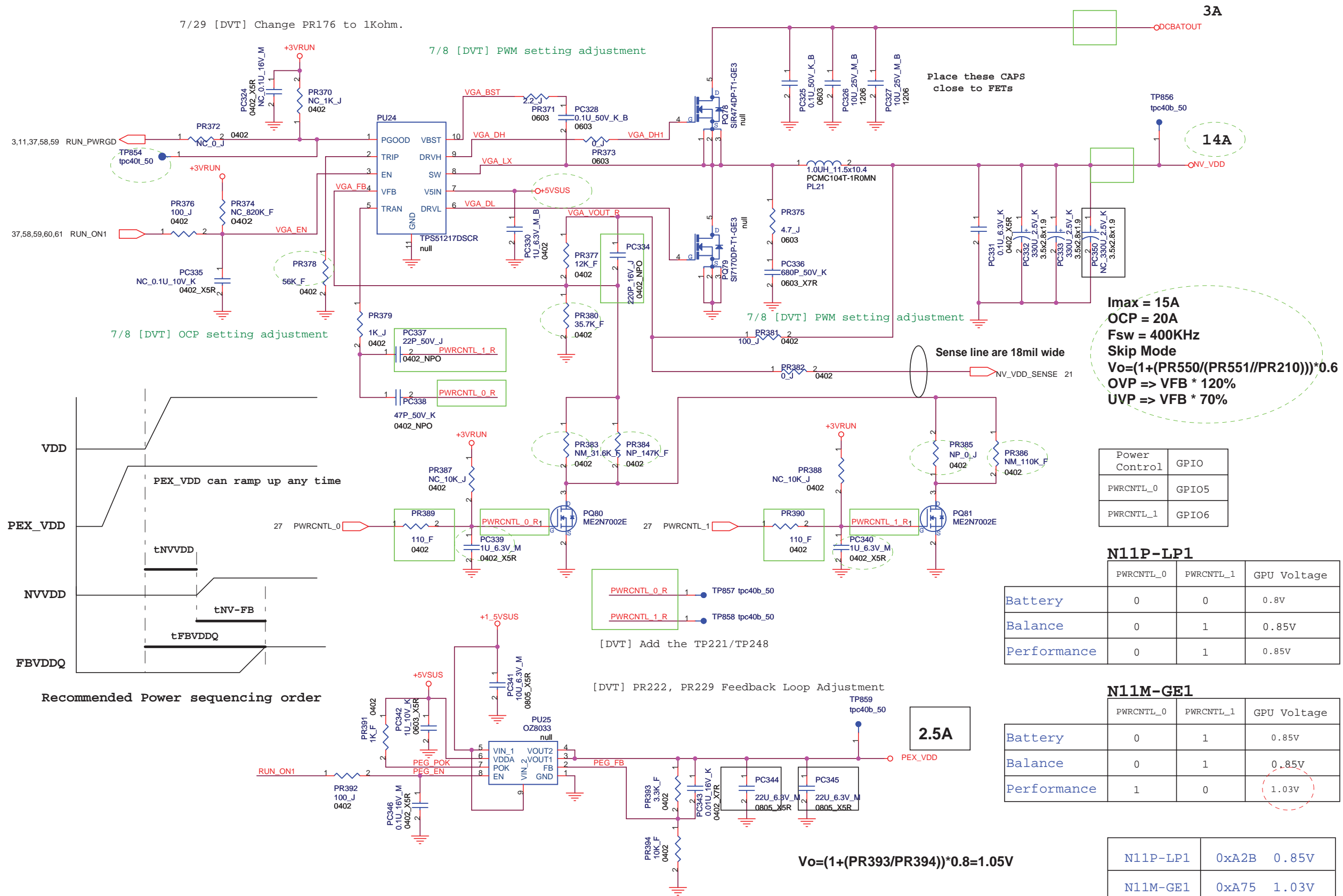


Battery CONN.









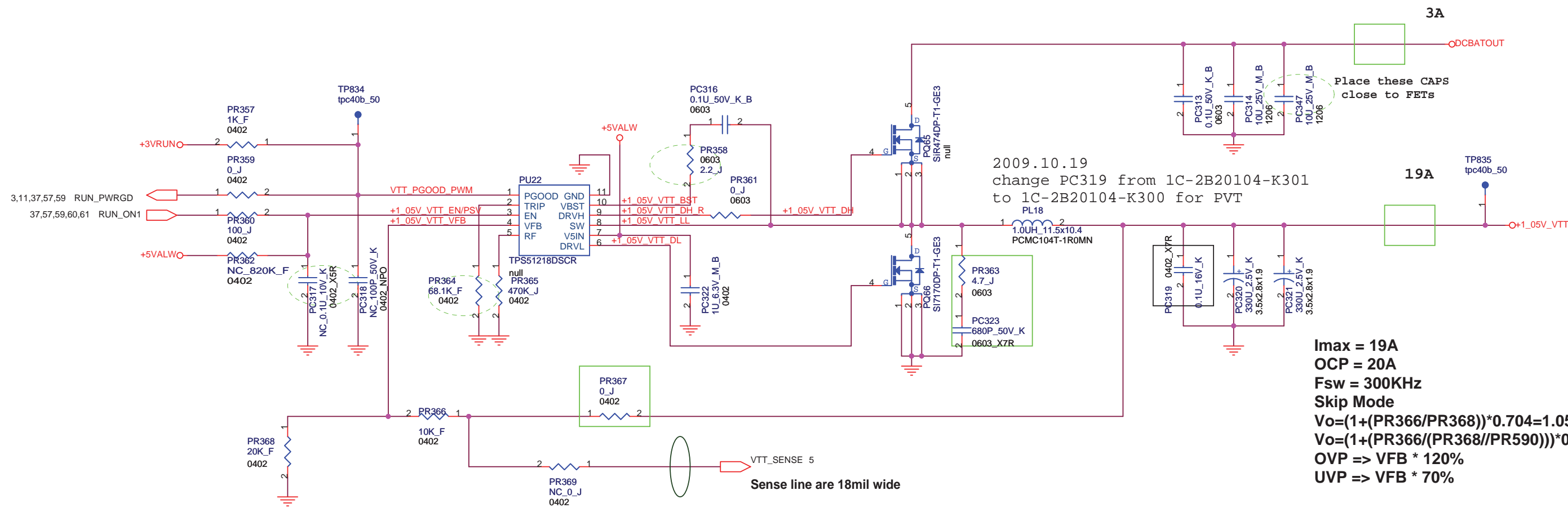
Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

N11P-LP1			
	PWRCNTL_0	PWRCNTL_1	GPU Voltage
	0	0	0.8V
	0	1	0.85V
e	0	1	0.85V

### N11M-GE1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
	0	1	0.85V
	0	1	0.85V
e	1	0	1.03V

N11P-LP1	0xA2B	0.85V
N11M-GE1	0xA75	1.03V
P8 P12	0.85 V 0.8 V	

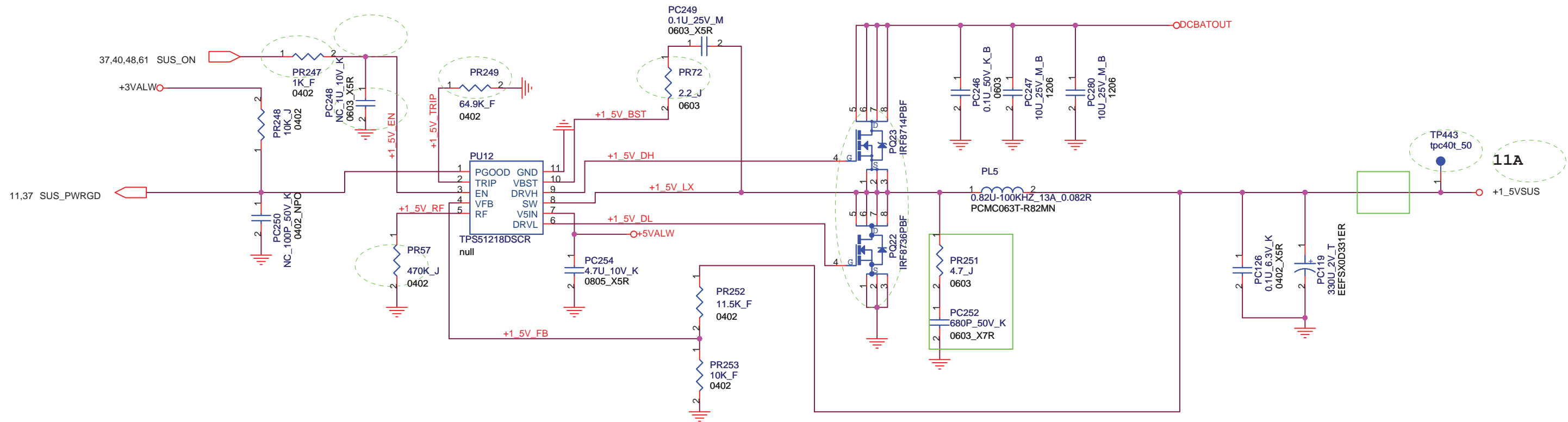


2009.10.19  
change PC319 from 1C-2B20104-K301  
to 1C-2B20104-K300 for PVT

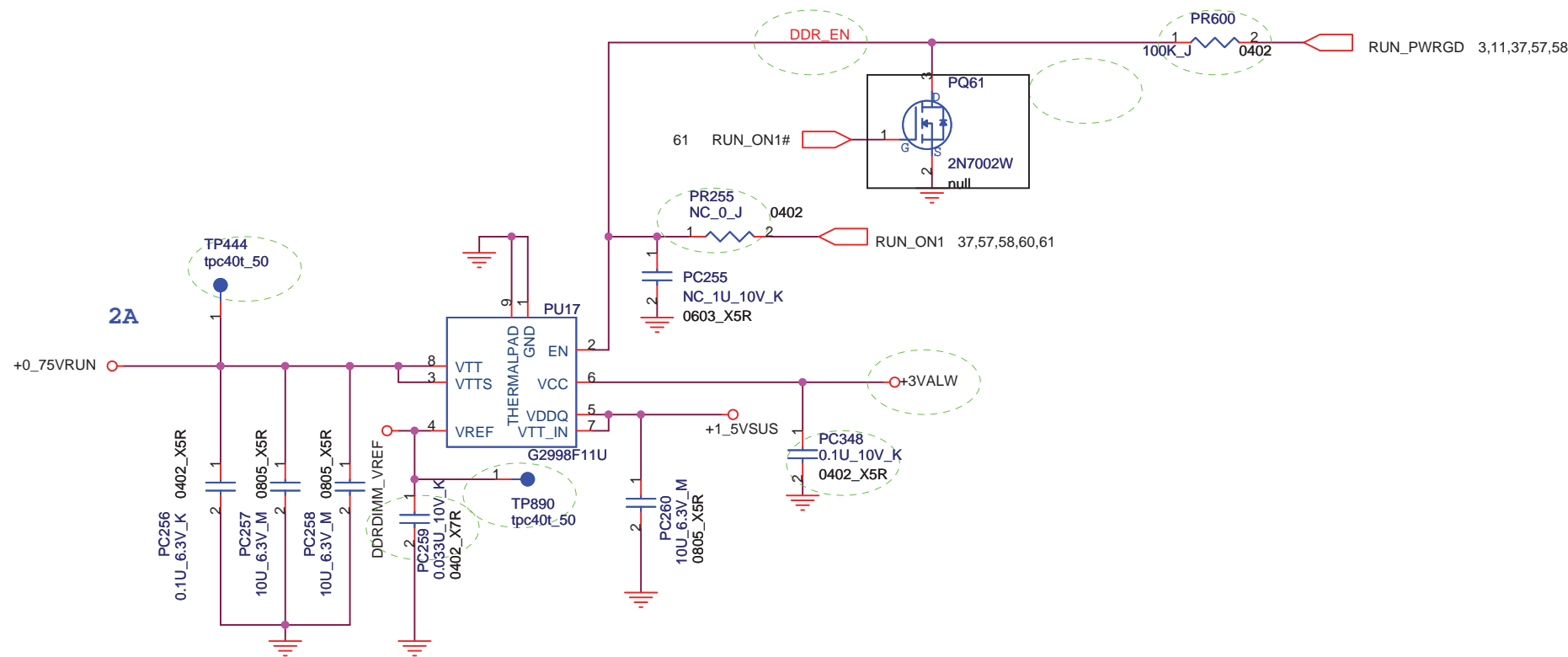
Imax = 19A  
OCP = 20A  
Fsw = 300KHz  
Skip Mode  
 $V_o = (1 + (PR366/PR368)) * 0.704 = 1.05V$   
 $V_o = (1 + (PR366/(PR368//PR590))) * 0.704 = 1.1V$   
OVP => VFB \* 120%  
UVP => VFB \* 70%

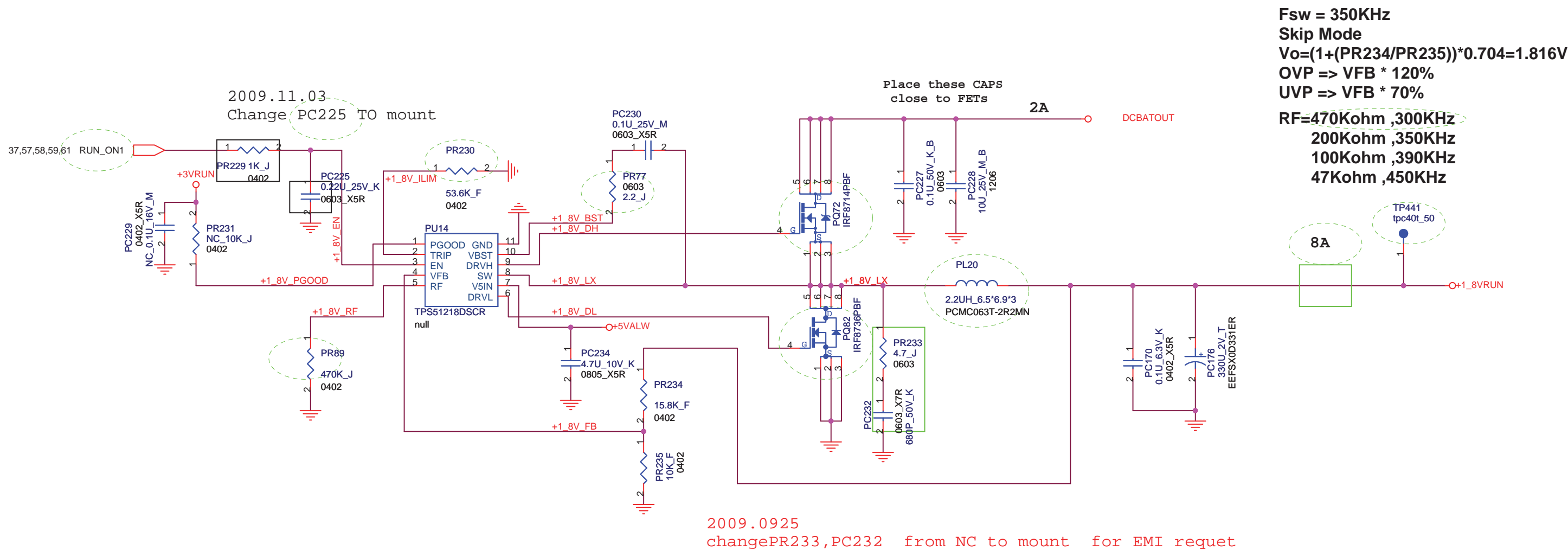
2009.0925  
change PR363, PC323 from NC to mount for EMI request

$R_F = 470K\Omega, 300KHz$   
200Kohm, 350KHz  
100Kohm, 390KHz  
47Kohm, 450KHz



2009.0925  
change PR251,PC252 from NC to mount for EMI request

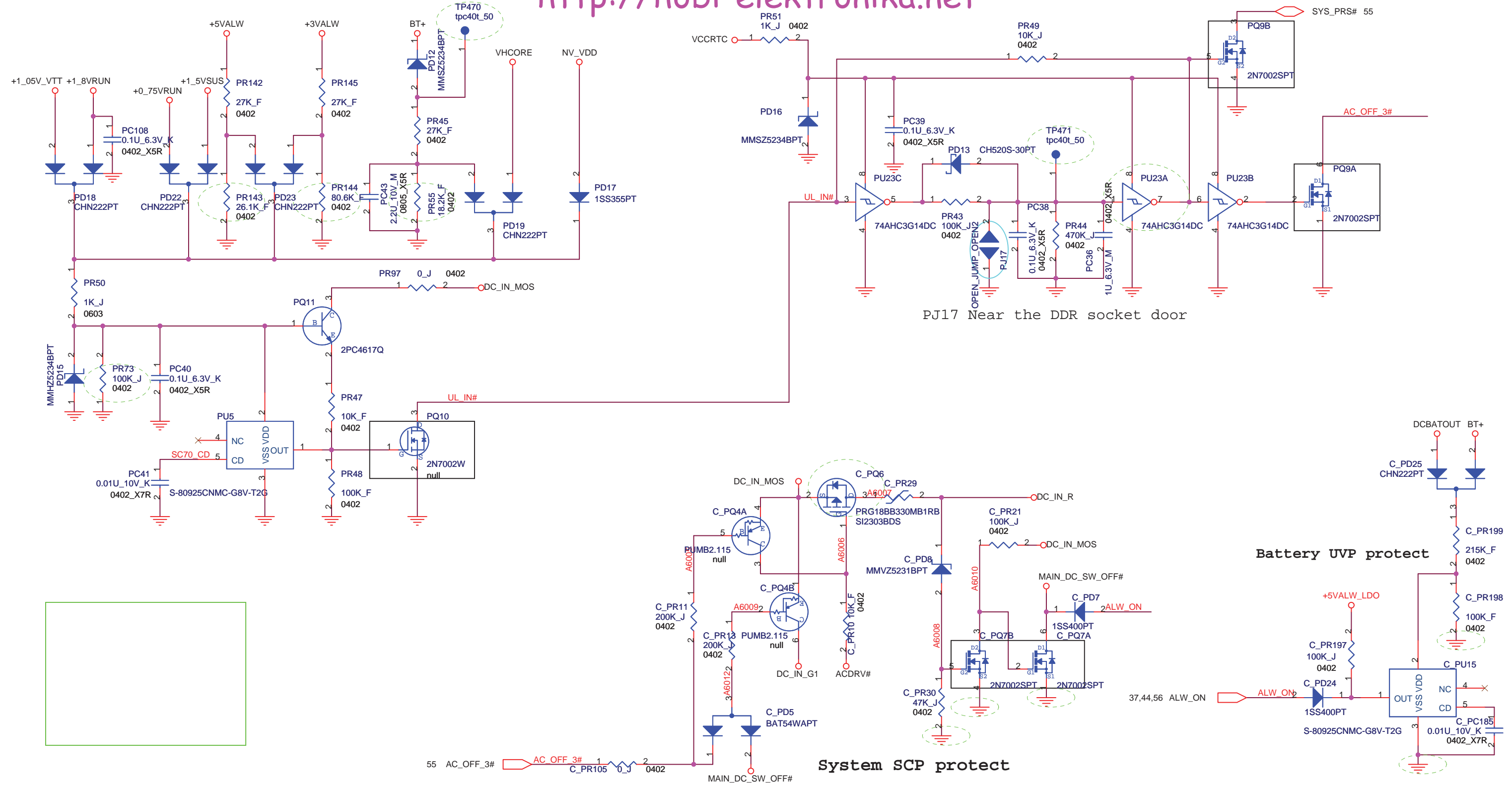




Fsw = 350KHz  
Skip Mode  
 $V_o = (1 + (PR234/PR235)) * 0.704 = 1.816V$   
OVP => VFB \* 120%  
UVP => VFB \* 70%  
RF=470Kohm ,300KHz  
200Kohm ,350KHz  
100Kohm ,390KHz  
47Kohm ,450KHz







System SCP protect

Battery UVP protect

PWRLIMIT Protect

VIINP	90W adaptor
PWRLIMIT	1.3V/85W

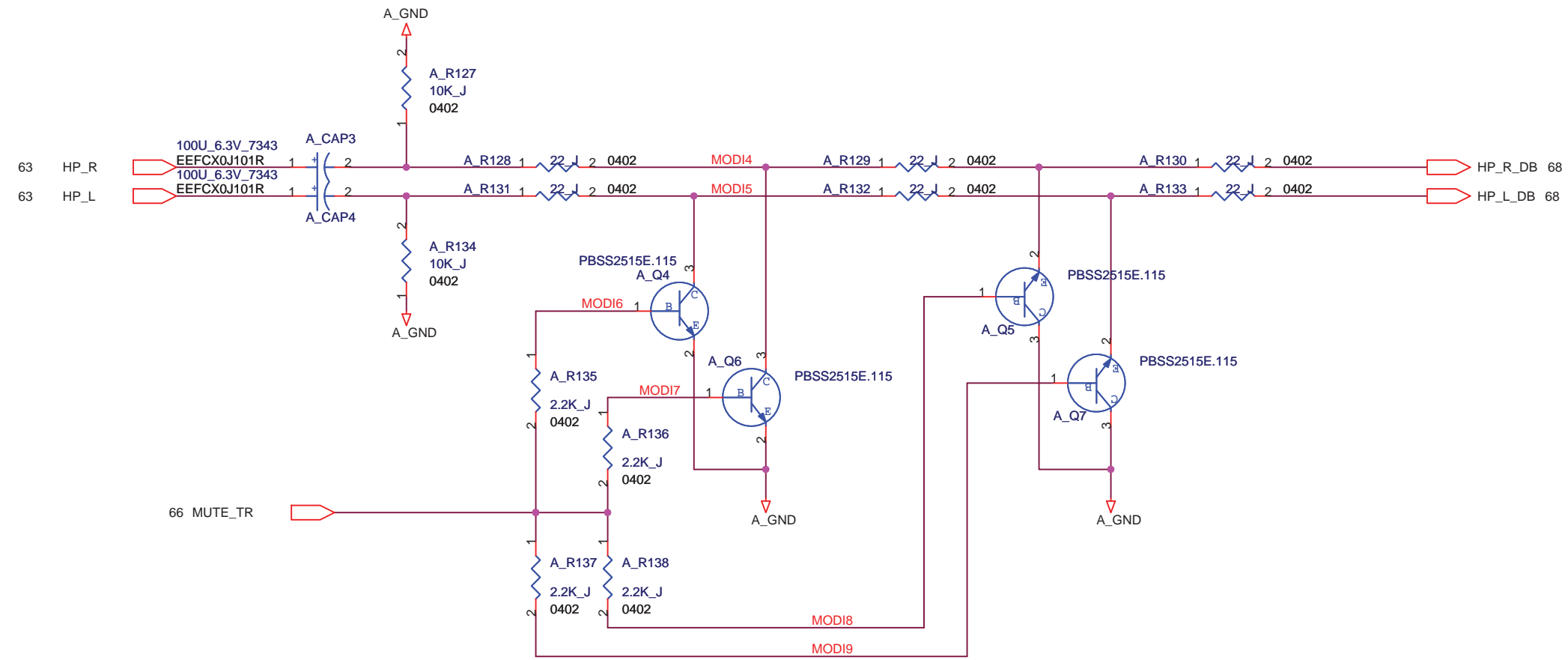
adapter max load : 5.7A/3000ms  
adapter OCP : 7.5Amax

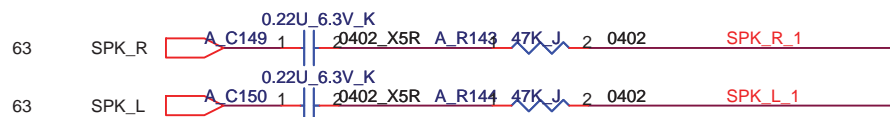
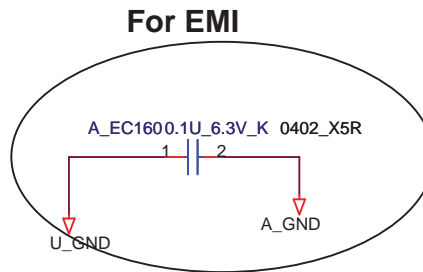
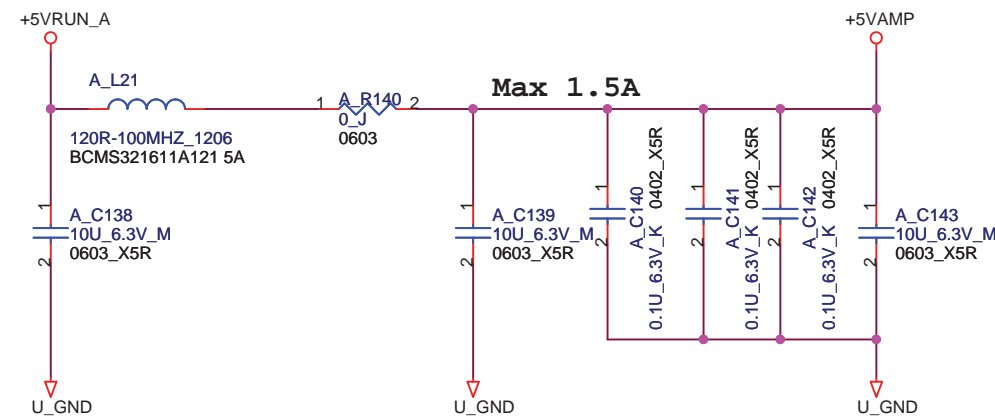


2009.11.03  
change A\_C23,A\_C22 from 15PF to 22PF for EMI request

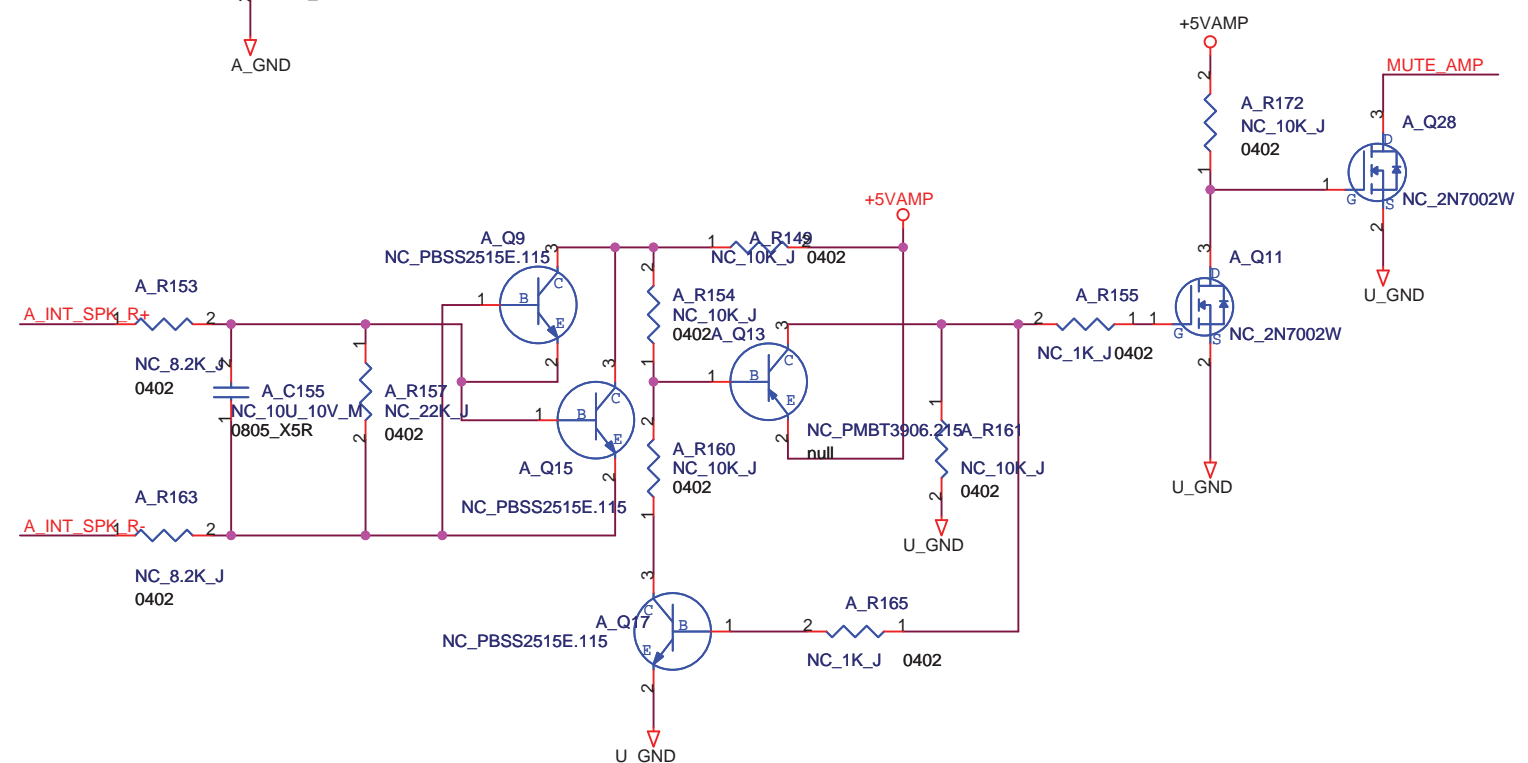
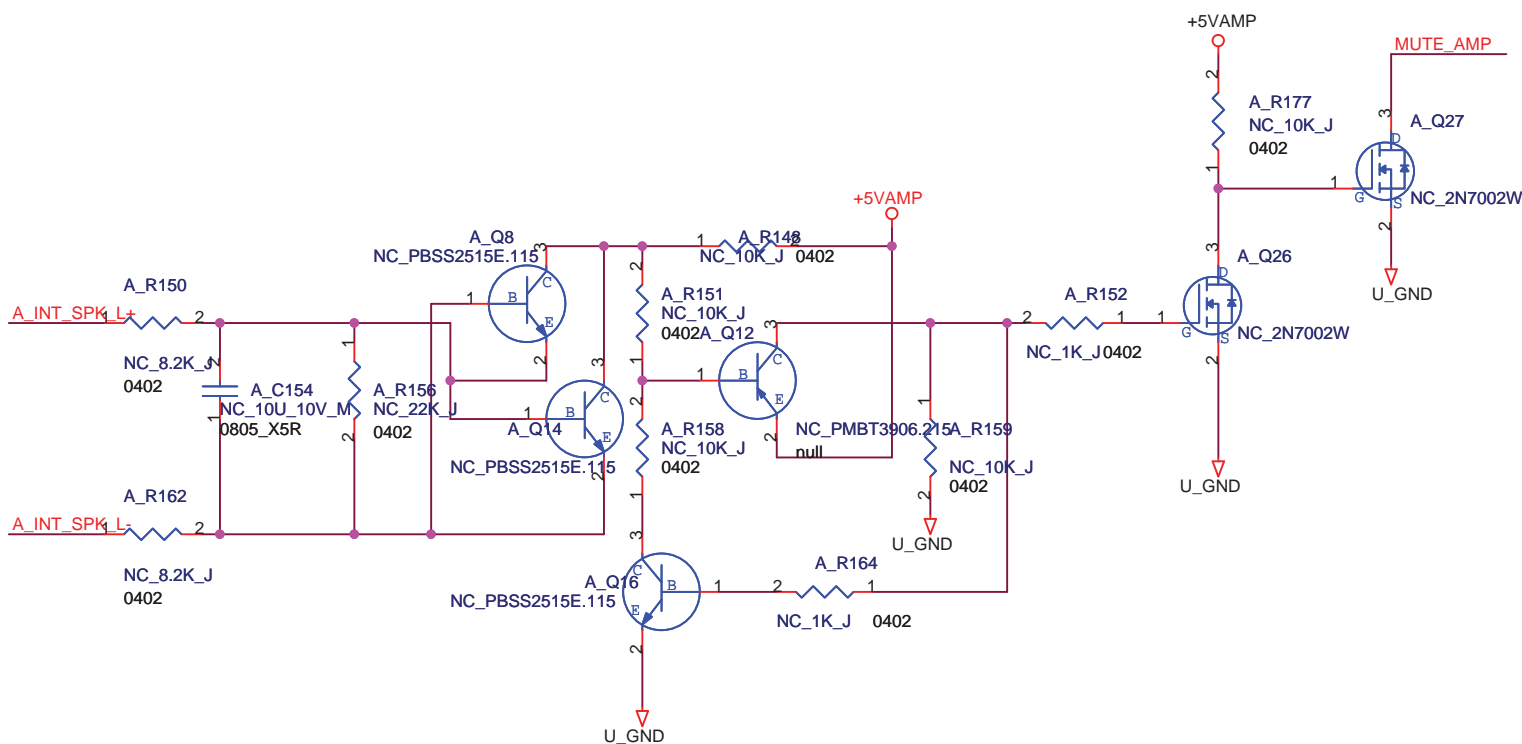
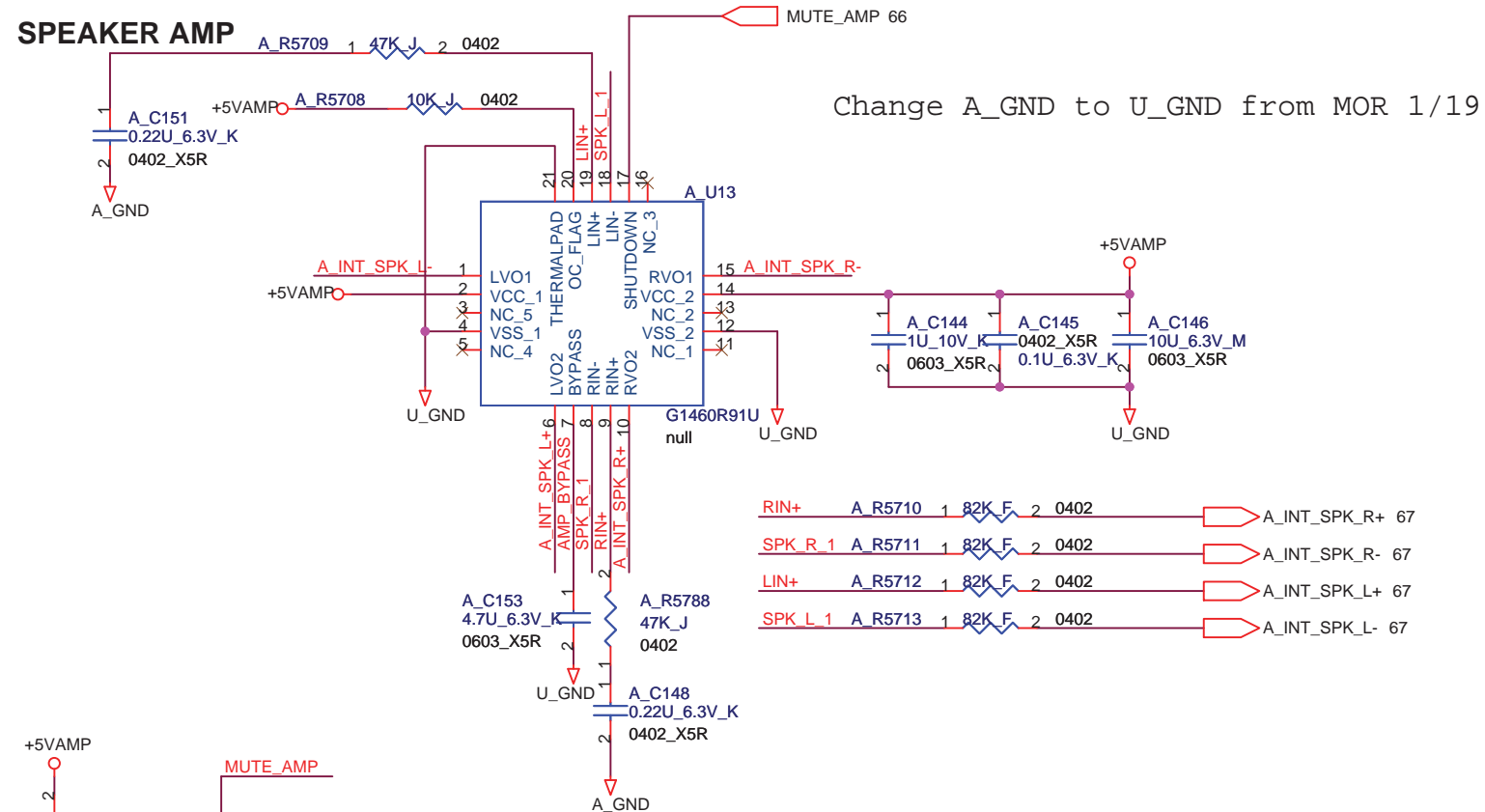


PC BEEP

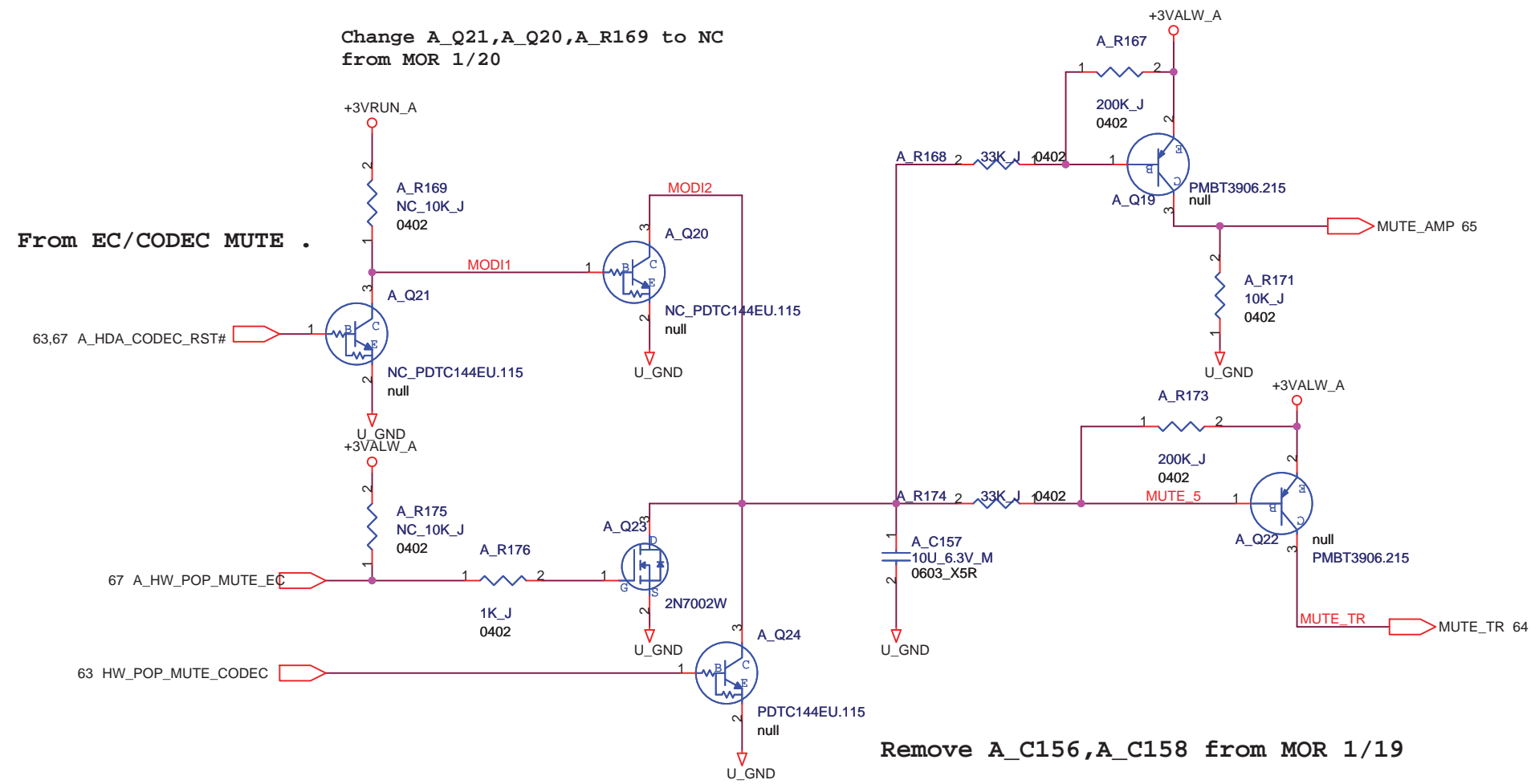




### SPEAKER AMP



For Mor request, add the speaker cable short protection circuit

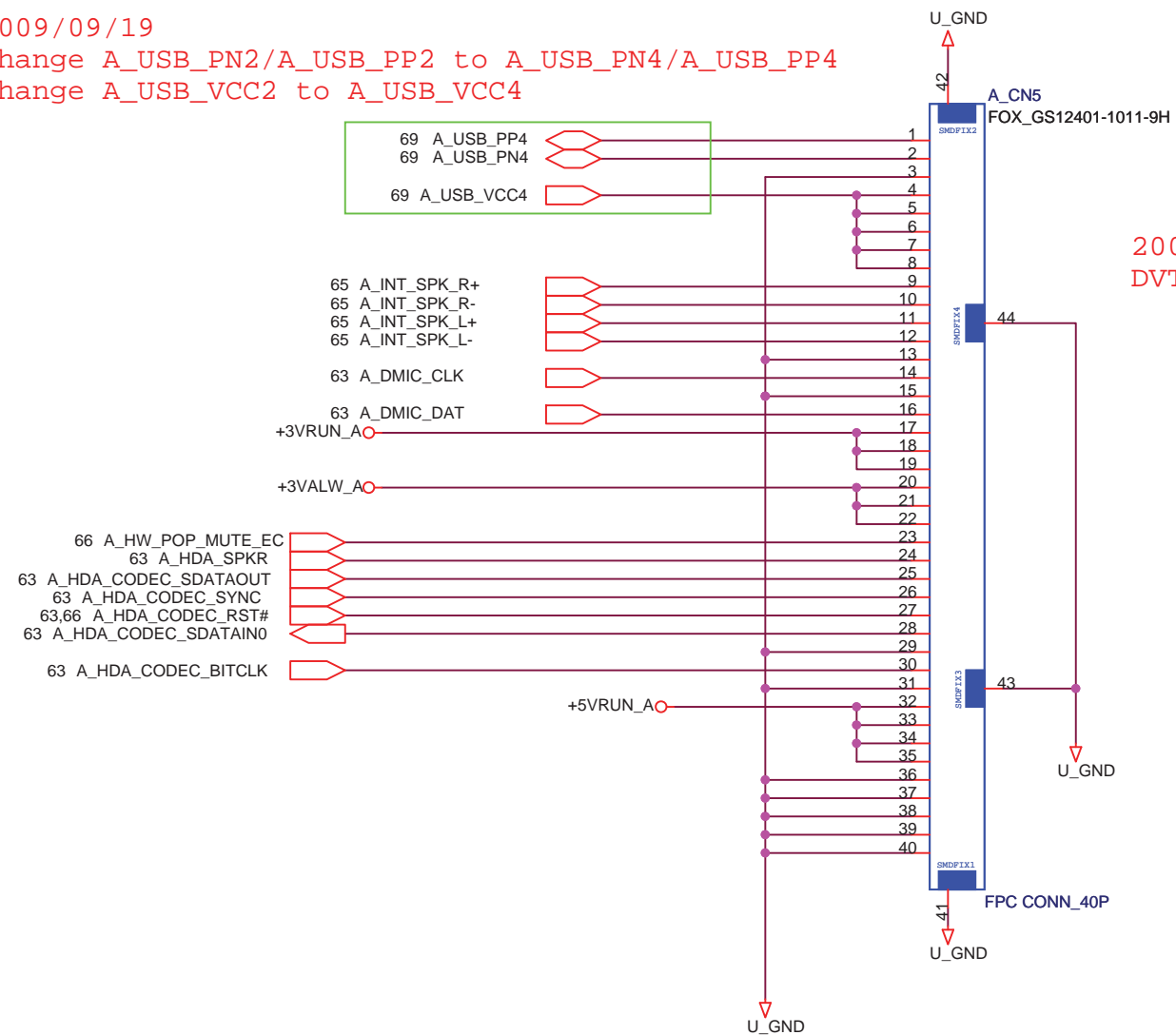




2009/09/19

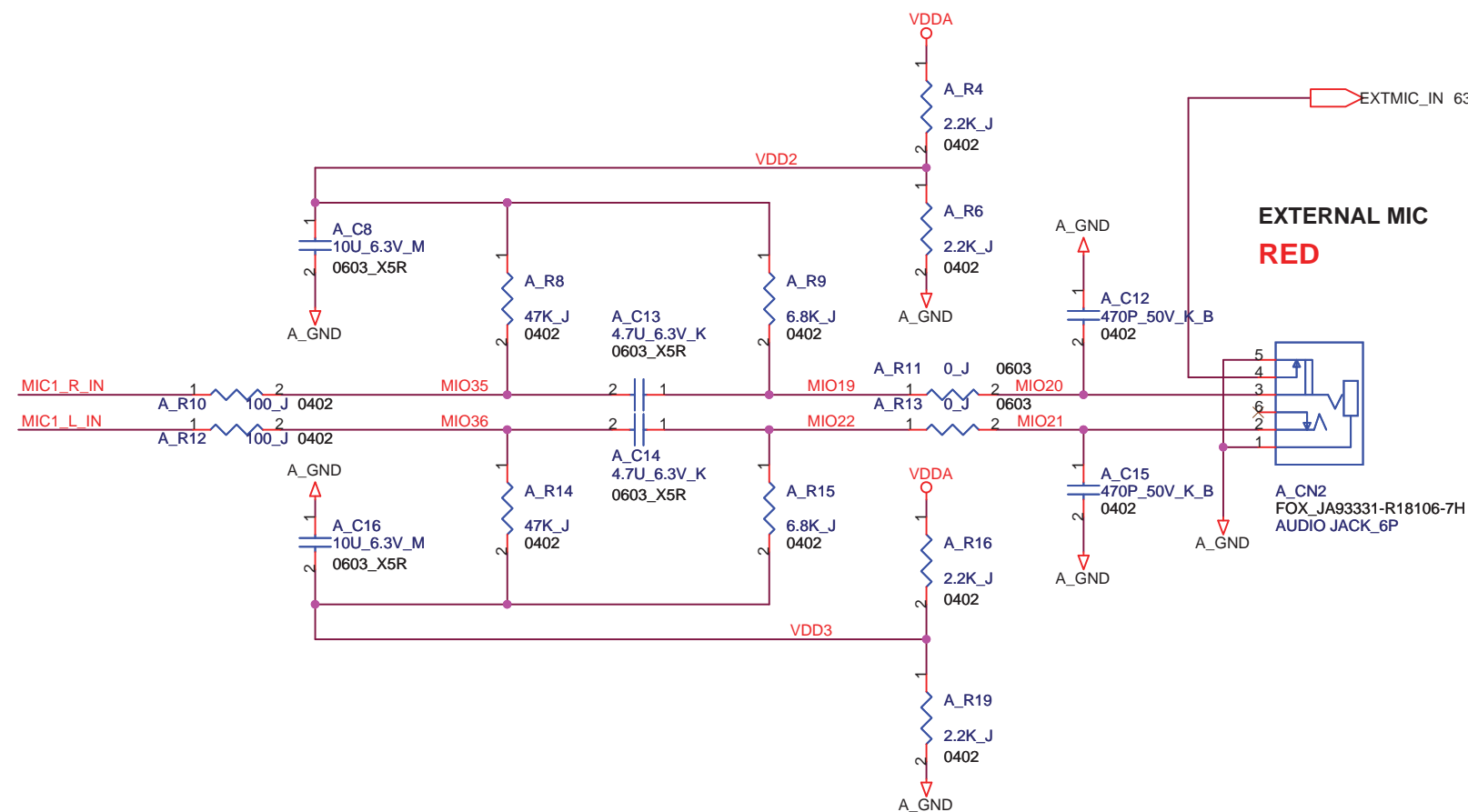
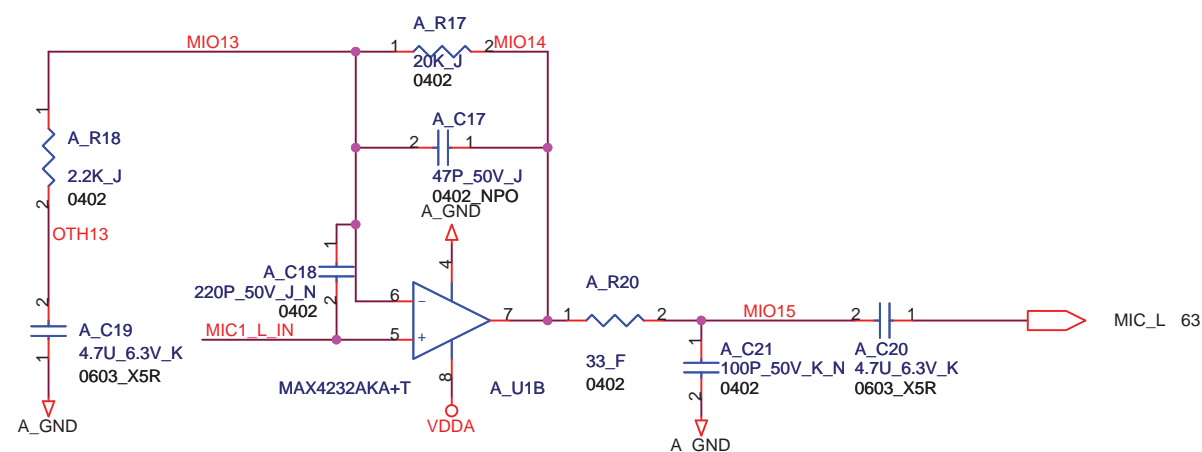
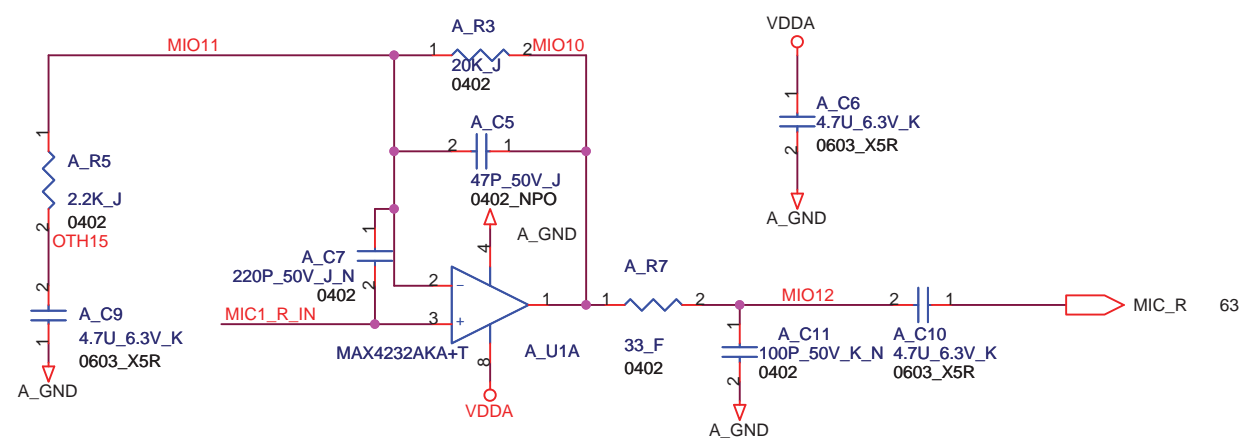
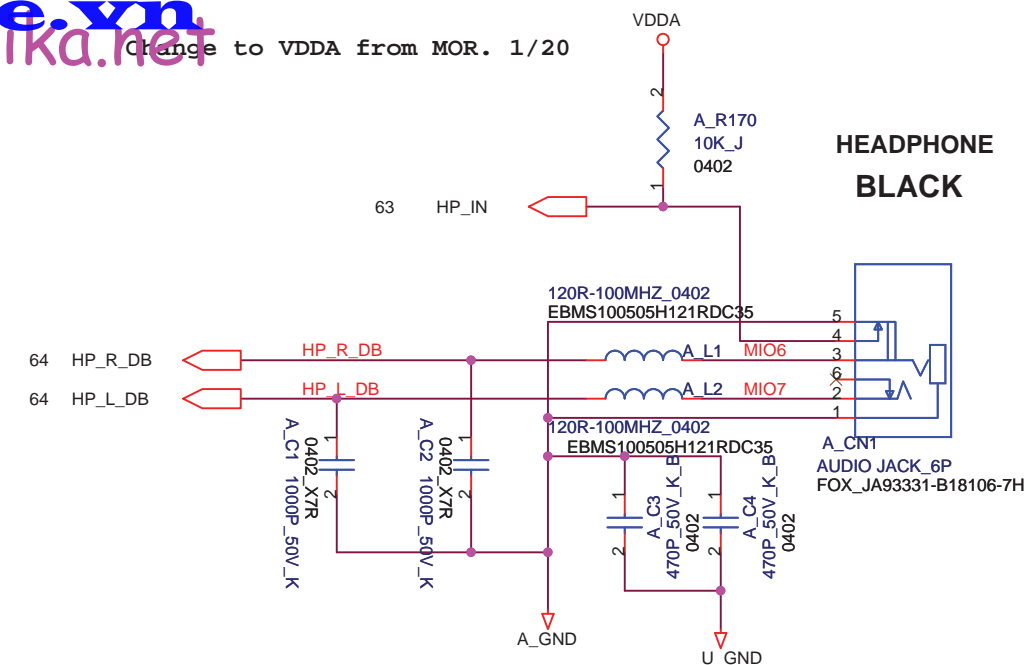
Change A\_USB\_PN2/A\_USB\_PP2 to A\_USB\_PN4/A\_USB\_PP4

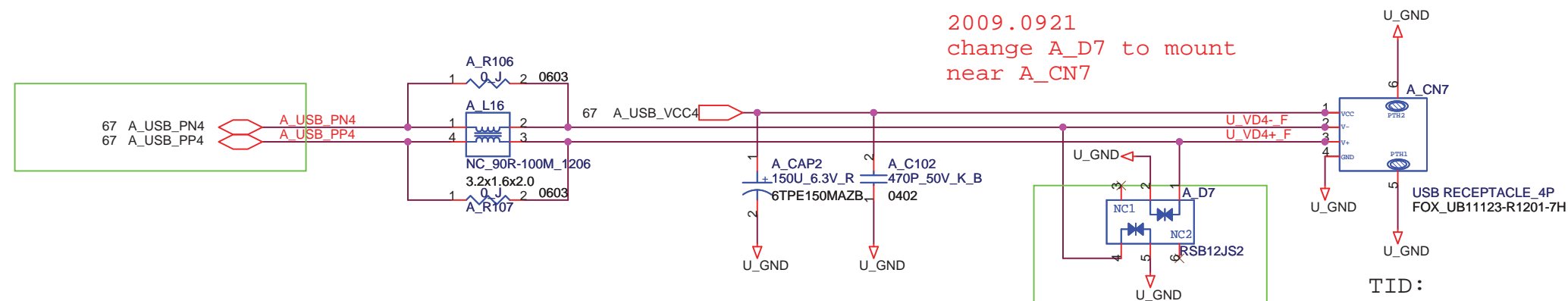
Change A\_USB\_VCC2 to A\_USB\_VCC4



2009.0918

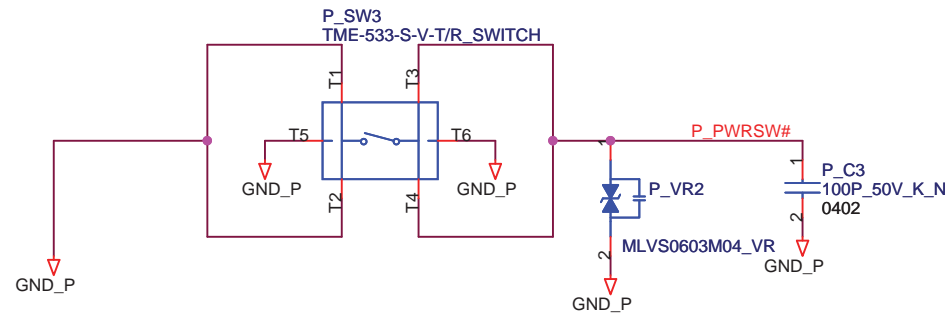
DVT2 A\_CN5 change to Halogen Free



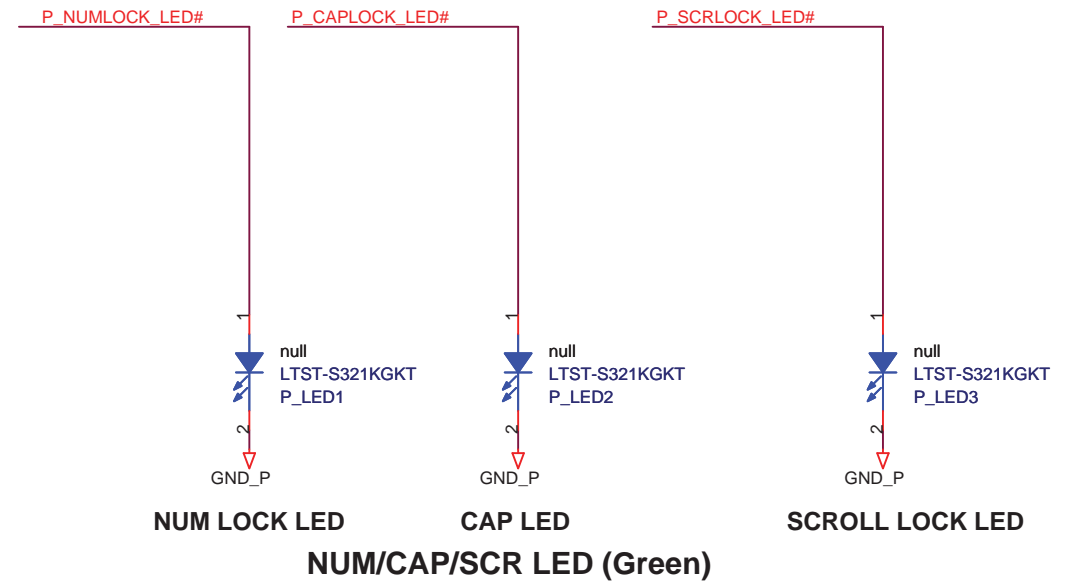
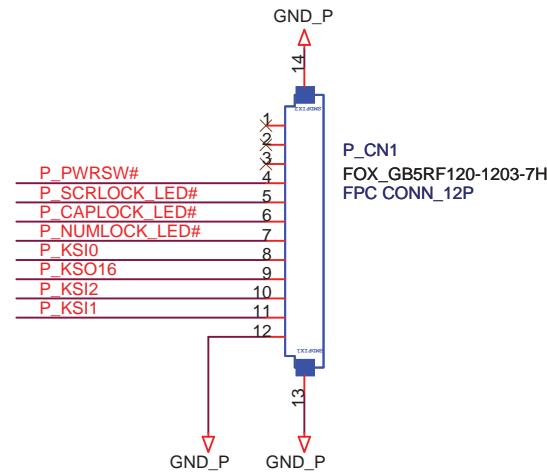


VespaCP no fingerprint function, so this page reserve

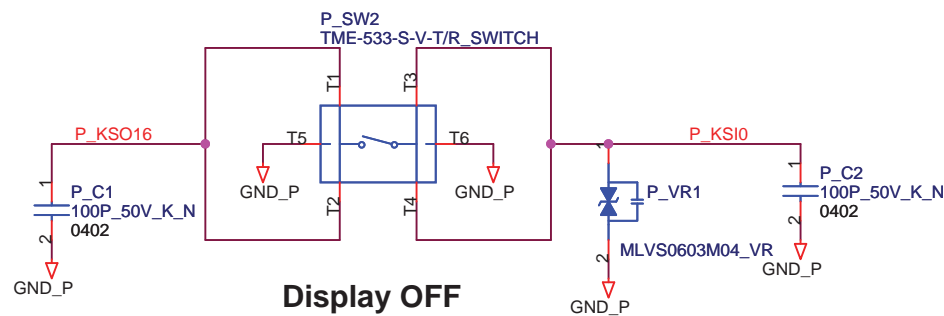
## POWER BUTTON



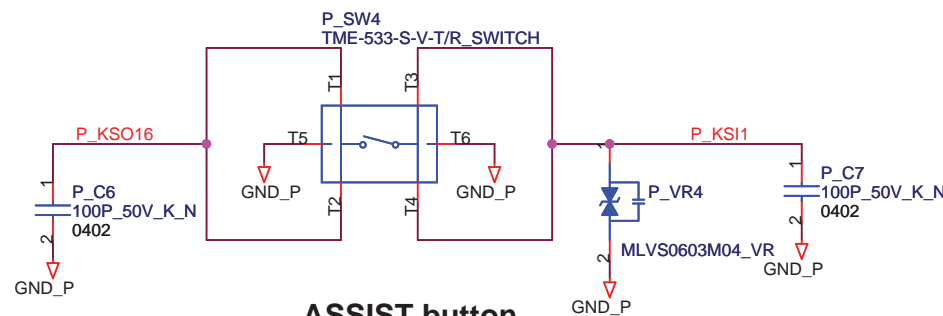
## Power Button Board



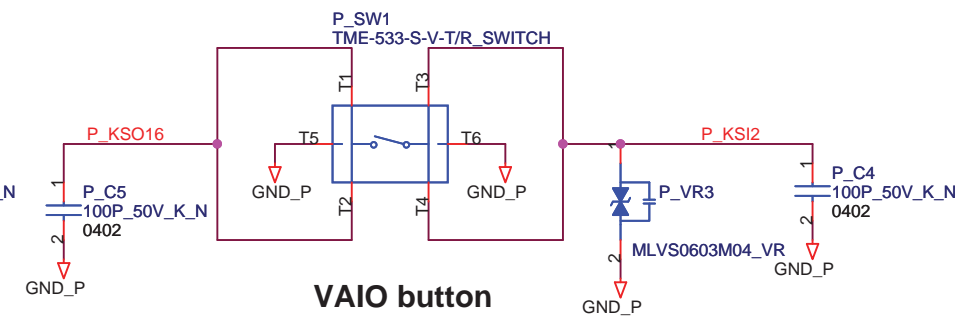
## Display OFF



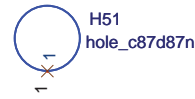
## ASSIST button



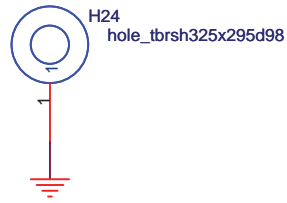
## VAIO button



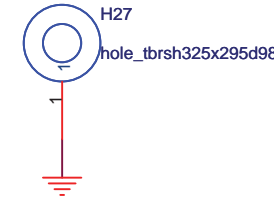




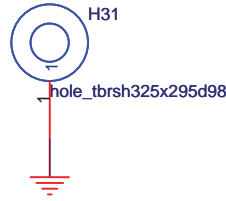
Near BAT



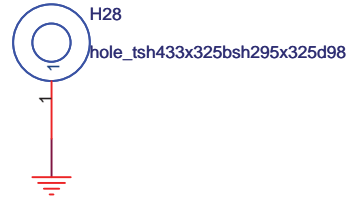
Near VRAM



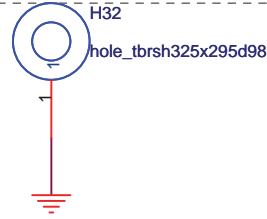
Near CRT



Near FAN



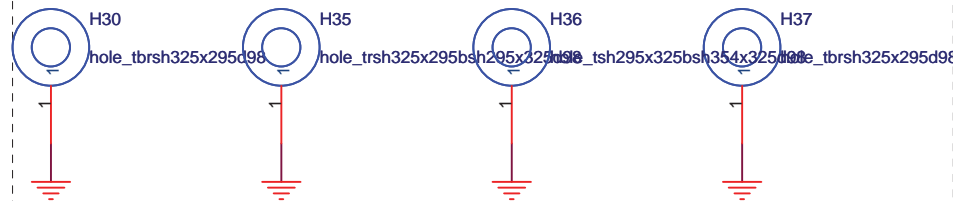
Near MS/SD Card



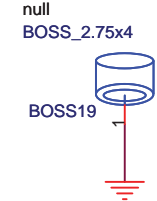
Near LVDS



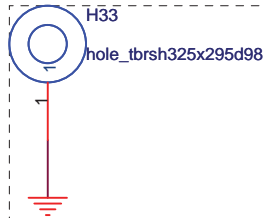
CPU



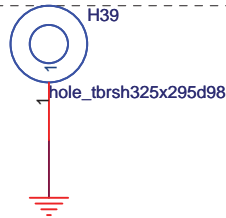
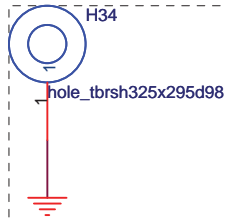
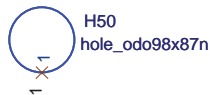
Near Express Card



For Thermal



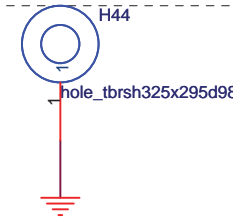
Near USB



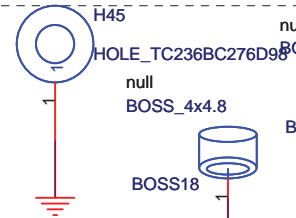
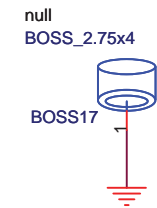
Near ODD



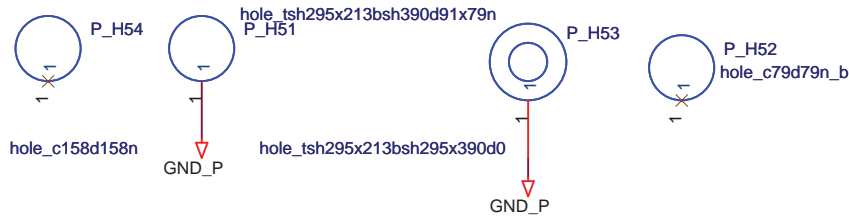
Del H42/H43, combine with CN25



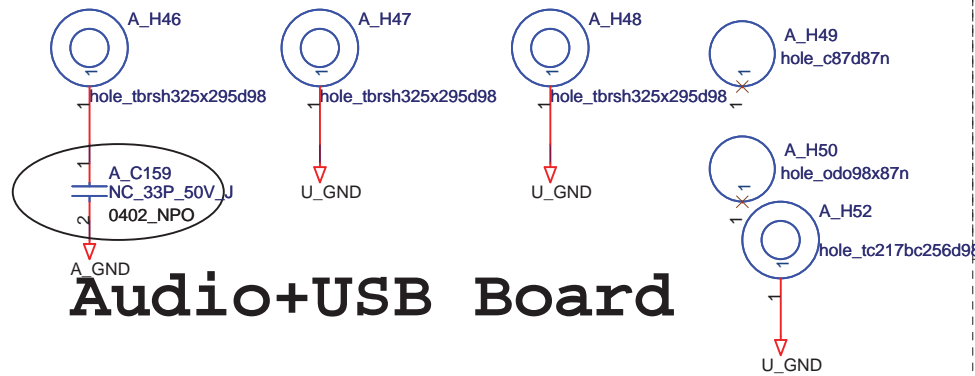
Near HDD



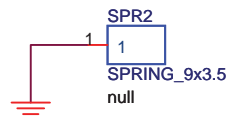
Near Charger Board  
for EMI



Function Board



Audio+USB Board



2009.10.20  
change SPR2 to 9 X3.5

2009/0910

1. Add S/D CARD test point for L6 TE request  
TP736

2. Add MS CARD test point for L6 TE request  
TP690, TP691, TP693, TP694, TP695, TP696, TP697  
TP702, TP724, TP698, TP699, TP700, TP701, TP703

delete

3. Add I\_LINK test point for L6 TE request  
TP512, TP513, TP514,TP515

4. Add TOUCHPAD test point for L6 TE request  
TP551, TP550, TP535, TP534 ,TP562, TP564

5.Delete R5893, R5887 and trace AC PRESENT,  
add R6007 to +3VALW in page 11, delete trace AC PRESENT,  
add test point TP186 in page 37. VespaCP use Ignition FW,  
no ACPRESENT function.  
Intel FAE suggest this pin can configure as GPIO.

6.change C6131 from NC\_470P\_16V\_K to 0.047U\_16V\_K follow Intel suggest

7. Change trace (CLK-PCIE-EXPRESS#,CLK-PCIE-EXPRESS,EXPRESS-CLKREQ#) from  
U134(AH42,AH41,A8) to (AJ50,AJ52,H6) for DVT1 express card can't detect issue.

8. Change page 70 from finger print to reserve, VespaCP no this function.

2009/0912

9. Delete R5785 0ohm resistor for voltage drop problem

10. Change RP82 from NC to mount for SI test  
Change RP81 from mount to NC for SI test  
Change RP86 from NC to mount for SI test

2009/0914

11.delete finger print

12.delete TP417,link to gnd

13.CN16 PIN 15 LINK TO GND  
14.CN35: change 0ohm to 33ohm

15.PCH: GNT0# and GNT1# change from pull high to +3vsus to pull low to gnd

16.DC\_IN: DELETE C\_PQ9 ,C\_PR34  
change C\_PR36,C\_PR37 from NC to mount  
C\_PFI change to 0437007.WR

17.+1.05V: change PC319 from Y5V to X5R

18. VHCORE: change OVT\_EC# to PROCHOT#

20.other: add PD31  
change PR275 from 10K to 4.7K

21.OVP: DELETE PR78 ,PQ17  
change PC35, PU2, PC37, PR240, PR108,PR39,  
PR36 from mount to NC

22.N11P-LP1+SANSUNG(H2) SKU and  
N11M-GE1 +SANSUANG(M2 SKU )need change BOM  
R5244 change from 1R-0004532-F200(45.3K) to  
1R-0002492-F200(24.9K) for nVIDIA FAE suggest

2009.0918

23. CN11, CN18, CN34, CN9, CN12, A\_CN7, A\_CN5 change to Halogen Free

2009/09/19

1.Change A\_USB\_PN2/A\_USB\_PP2 to A\_USB\_PN4/A\_USB\_PP4  
Change A\_USB\_VCC2 to A\_USB\_VCC4 in page 67

2. Change A\_USB\_PN2/A\_USB\_PP2 to A\_USB\_PN4/A\_USB\_PP4  
Change A\_USB\_VCC2 to A\_USB\_VCC4  
Change U\_VD2+\_F/U\_VD2-\_F to U\_VD4+\_F/U\_VD4-\_F in page 69

3.Change USB\_VCC2 to USB\_VCC4  
Change USB\_OC#0 to USB\_OC#1 in page 48

4.Add USB\_OC#1  
Change USB\_PN10/USB\_PP10 to test point in page 13

5.Change USB\_VCC2 to USB\_VCC4 in page 43

2009.0921

Page 50  
1.R531 Delete,then pull CN34 pin4 to GND.  
2.Remove the Test point TP562 to +5VRUN.

2009.0925

1.change R5245,R5273 to NC to mount  
2.add R5313 for IOK\_J  
3.change R5916 TO NC  
4.change D15,D21,A\_D7 TO mount and place them near connector  
5.WIRELESS\_DATA/WIRELESS\_CHCLK change ,please refere to page 49  
6.ADD R5991 for 100K\_J  
7.change C476 TO NC\_12P  
8.change C1986 TO 12P  
9.ADD R6010,R6011,R6012 to pull-down SPI0\_CLK,SPI0\_MOSI,SPI0\_CS# in page 09  
10.change CN25,CN29,CN30 TO Halogen Free  
11.change D13,D11 TO 16-SSM22LL\_PT00  
12.change R5910,R5911 to NC\_1K  
13.DELETE TP498,TP491,TP490,TP495,TP494,TP509  
14.CHANGE Q45 TO NC ,R5996 TO MOUNT  
15.change CN21 TO 1N-1052000-0000 for ME request  
16.change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request  
17.page 57:change net PWRCNTL\_0\_R to PWRCNTL\_1\_R  
change net PWRCNTL\_1\_R to PWRCNTL\_0\_R  
change PR389,PR380 TO 110 ohm  
change PC334 to 220P\_16V\_J 0402  
change PC337 to 220P\_50V\_J 0402  
delete PJ23,PJ24,PJ25,PJ26

18.page 53:delete PJ18,PJ19

19.page 56:delete PJ1,PJ2

20.page 58:delete PJ20,PJ21,PJ22  
ADD PR367/0 ohm

21.page 59:delete PJ5

22.page 60:delete PJ3

23.page 06:delete PJ43

2009.0923

ADD test point TP490,TP491,TP494,TP495,TP498,TP509

2009.0925

ADD C6260 NC\_1000P\_16V\_K

2009.0925

For EMI request  
1.Add Cap.C36 0.1U,C999 1000PF on net +1\_05V\_VTT  
2.Add Cap.C37,C38 0.1U on net +1\_8VRUN  
3.Add Cap. C39 0.1U,C1000 1000PF on net +3VRUN  
4.Add Cap.C53,C54,C61 0.1U on net DCBATOUT  
5.Add SPR2

2009.0925

ADD C70,C71,C72 10P for RF request

2009.0925

change C6156,C6157 from 12p to 15p for vendor request

2009.0925

change PR245,PC269,PR236,PC266,PR363,PC323,PR251,  
PC252,PR233,PC232 from NC to mount for EMI request

2009.0926

For EMI request  
1.Add PC62 0.1U on net +1\_8V\_LX ,place it near PQ72  
2.change C539 from NC to 680P  
3.Add C549 680P on net INV\_BRADJ,place it near LVDS connector

2009.0928

For RF request  
change C1264,C716,C532 to 47P

2009.0928

change R5376 to 100K follow design guide

2009.0928

change PC337 to 22P

2009.0928

Add Q7 for MOR request

2009.0929

Add PC206 NC\_0.1U reserve for Return patch

2009.0929

change RP86 ,RP82 TO NC  
change RP81 TO mount

2009.10.19

1.Change PC319 from 1C-2B20104-K301 To 1C-2B20104-K300.  
2.change R5703 from 68ohm to 75 ohm  
3 NC RP81 for 1R-1010000-JP00  
4. MOUNT RP82, RP86 for 1R-1010000-JP00  
5. change C5250 from 1C-2B20473-K300 to 1C-2B20102-K001  
6. change C6256 from 1C-2B20102-K001 to 1C-2B20473-K300

2009.10.20

change SPR2 from 4x3 to 7x2.5

2009.10.22

PAGE37:delete C468, C513, U25, R76, R55, R41, R73, C60 (NC), TP871,  
TP872,TP873,TP876,TP878,TP880,TP874.TP875,TP877,TP879,TP881,  
TP882 for PVT  
PAGE53:change PC112 from 68U to 47U for power request

2009.10.23

Page 35 : deleteJ2,J3  
Page 38 : delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518  
Page 05 : delete R5786  
Page 37 : add TP690, TP690  
PAGE 45,46:change net SD\_WP# to SD\_WP  
Page 35 : Add test point TP897,TP898,TP899 for PVT

page 35 : add TP900,TP901 for +3VRUN

2009.10.28

page 57: Change PC344 to 1C-2B70226-M100.  
Add PC345 1C-2B70226-M100.  
Change PEX\_VDD to 2.5A.

2009.10.30

page 55: Change C\_PQ3,C\_PQ8 to 17-2N7002W-0000.

page 59: Change PQ61 to 17-2N7002W-0000.

page 61: Change PQ58 to 17-2N7002S-PT00.

page 62: Change C\_PQ7 to 17-2N7002S-PT00.  
Change PQ10 to 17-2N7002W-0000.  
Change PQ9 to 17-2N7002S-PT00.

Page 51:change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

Page 36:change Q9 to 17-2N7002S-PT00.  
Page 03:change Q179 to 17-2N7002S-PT00

Page 72 :change SPR2 to 9 X3.5

2009.10.31

page 57: Add PC350 1C-33U0337-KX00 NC\_330U\_2.5V\_K.

Page 14 : add RP83 NC\_0 to escape crosstalk

2009.11.3

Page60 : Change PC225 TO mount  
page 60: Delete PC62.

page 60: Change PR229 to 1K\_J.  
Change PC225 to 0.22U\_25V\_K.

2009.11.03

Page 35:add C60,C62,C63,C64

For EMI request  
1:Page 55 change C\_PC14 to 4700pf  
change C\_PC13 to 0.1U  
2: Page 55 change C\_PC156 to 2200pf  
3.Page 63 change A\_C23,A\_C22 from 15PF to 22PF

2009.11.4

Page 35:add C65,C66,C67,C73,C74 for FAN issue

page 55: Change C\_EC6066 to 1C-2B30104-K000.

page 56: Add TP442.

page 56: Change E\_C6060 to 1C-2B30104-K000.  
Change E\_C6059 to 1C-2B30104-K000.  
Change E\_C6067 to 1C-2B30104-K000.  
Change E\_C6068 to 1C-2B30104-K000.  
Change E\_C6062 to 1C-2B30104-K000.  
Change E\_C6061 to 1C-2B30104-K000.

2009.11.16

change C\_PC14, C\_PC156 to 1000P for EMI request

2009.11.19

Page49: Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

2009.11.19

Page 55: Add C\_PQ26,C\_PQ27,C\_PQ9 NC\_TPCC8102 for 2nd source.