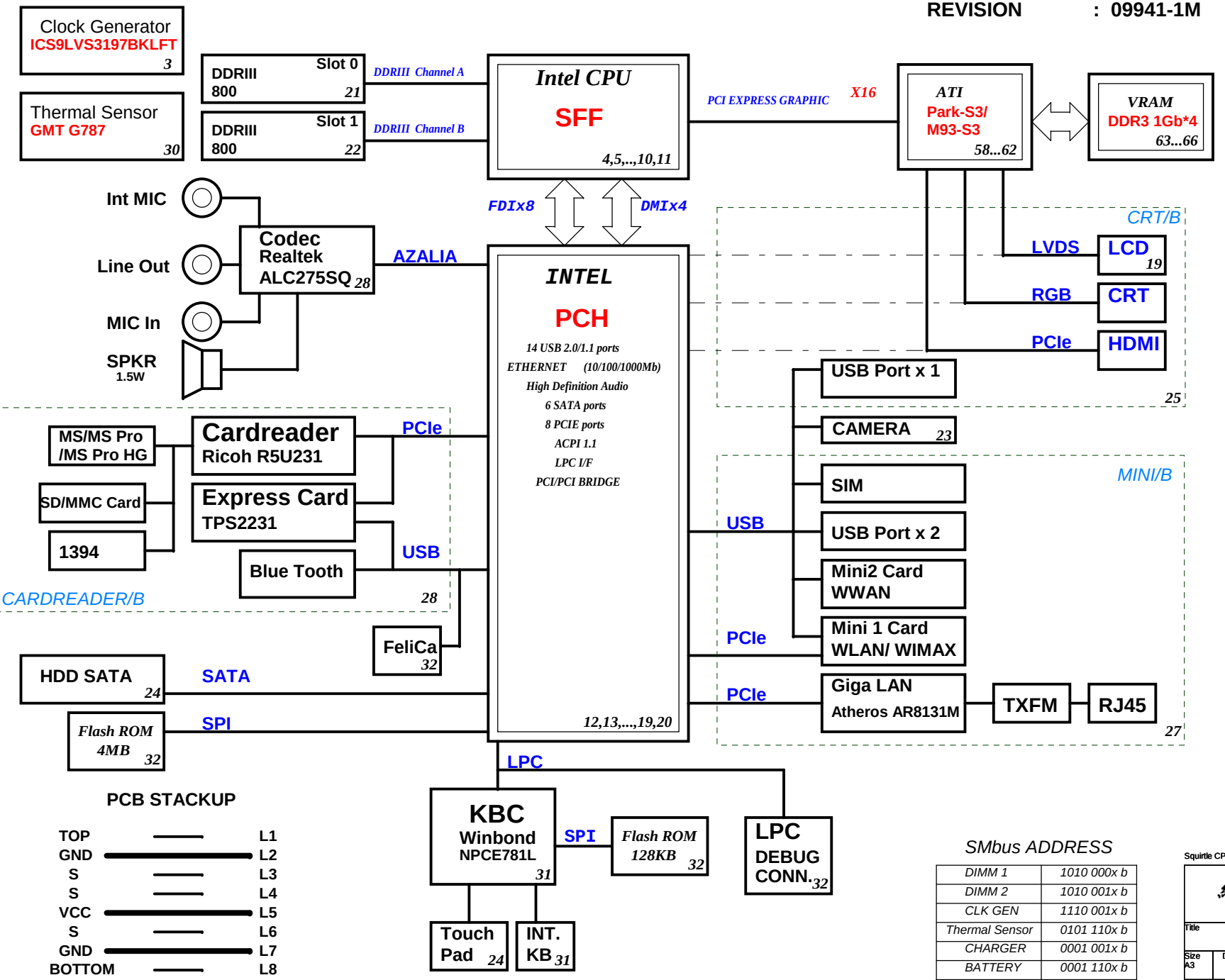
CADIZ-CP Block Diagram

PROJECT CODE : 91.4JH01.001
PCB P/N : 48.4JH01.01M
REVISION : 09941-1M



PCB STACKUP

TOP	—	L1
GND	═══	L2
S	—	L3
S	—	L4
VCC	═══	L5
S	—	L6
GND	═══	L7
BOTTOM	—	L8

SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

SYSTEM DC/DC
RT8223 — 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5(9A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8209 — 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)

RT8209 — 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(13.5A)

RT9026 — 36

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A

CHARGER
BQ24751 — 32

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC
ADP3211 — 36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A

VGA/ GFX Core
ADP3211 — 40

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE/ VCC_GFXCORE 11A

Squirtle CP DIS SAMSUNG

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: CADIZ-CP | Rev: -1M
Date: Saturday, April 24, 2010 | Sheet 1 of 57

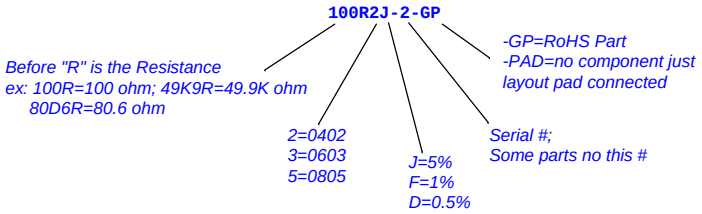
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

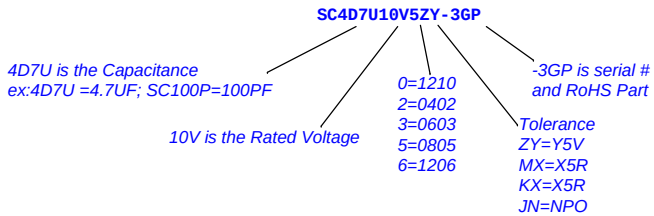
Processor Strapping

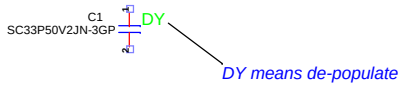
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Resistor



Capacitor





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Title: **Reference**

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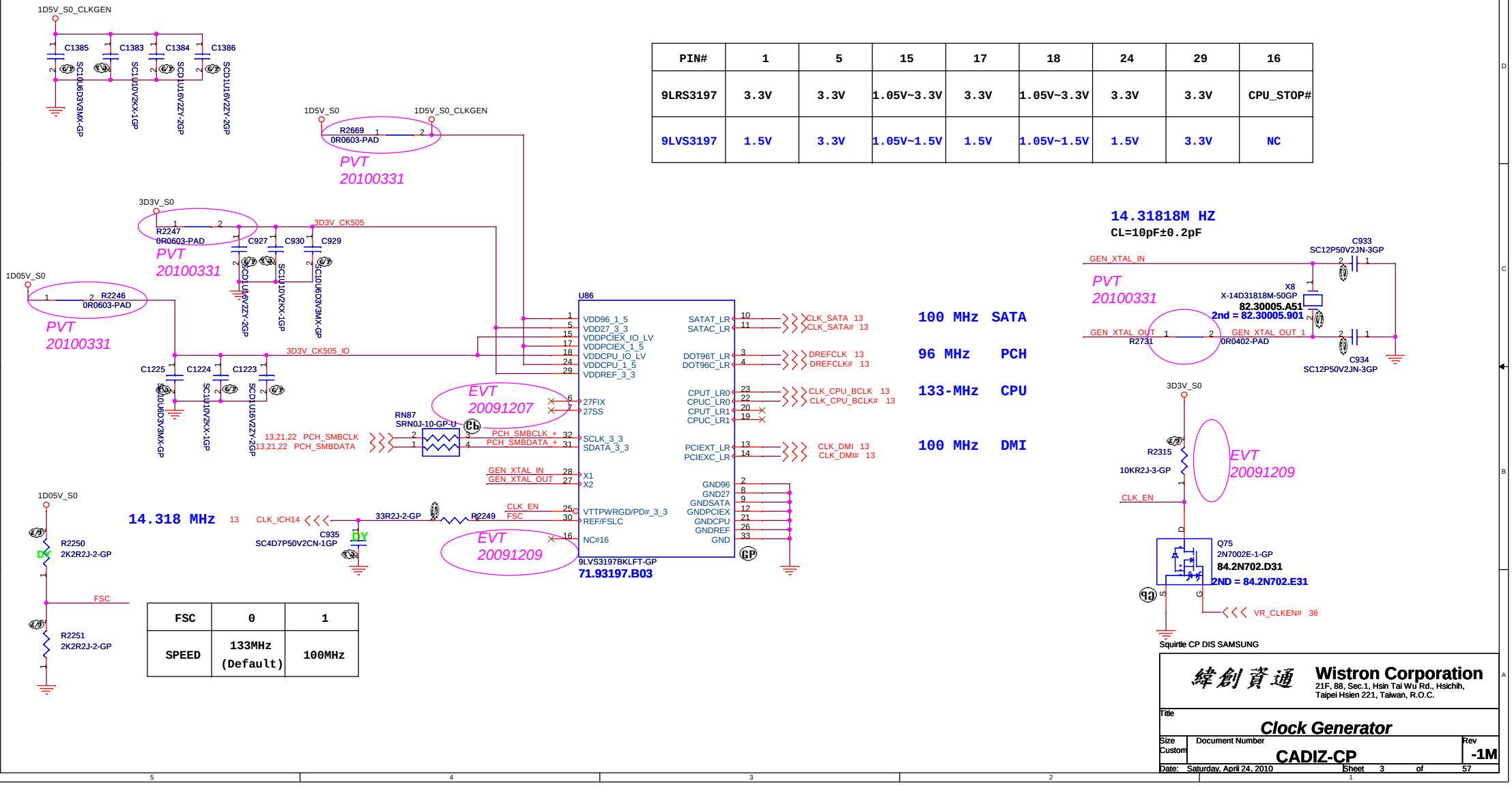

PIN#	1	5	15	17	18	24	29	16
9LRS3197	3.3V	3.3V	1.05V~3.3V	3.3V	1.05V~3.3V	3.3V	3.3V	CPU_STOP#
9LVS3197	1.5V	3.3V	1.05V~1.5V	1.5V	1.05V~1.5V	1.5V	3.3V	NC

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator

Size: Custom | Document Number: CADIZ-CP | Rev: -1M

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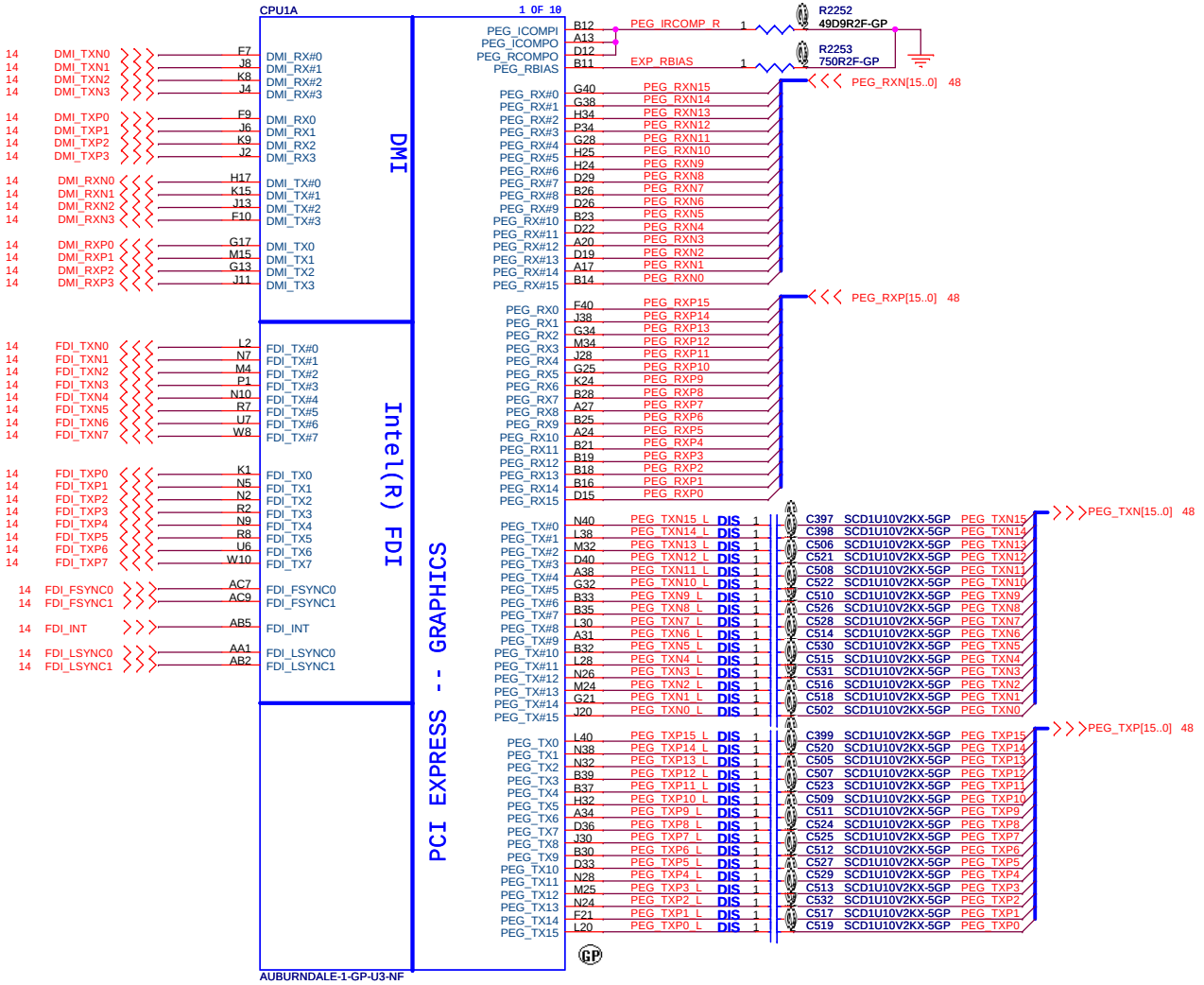

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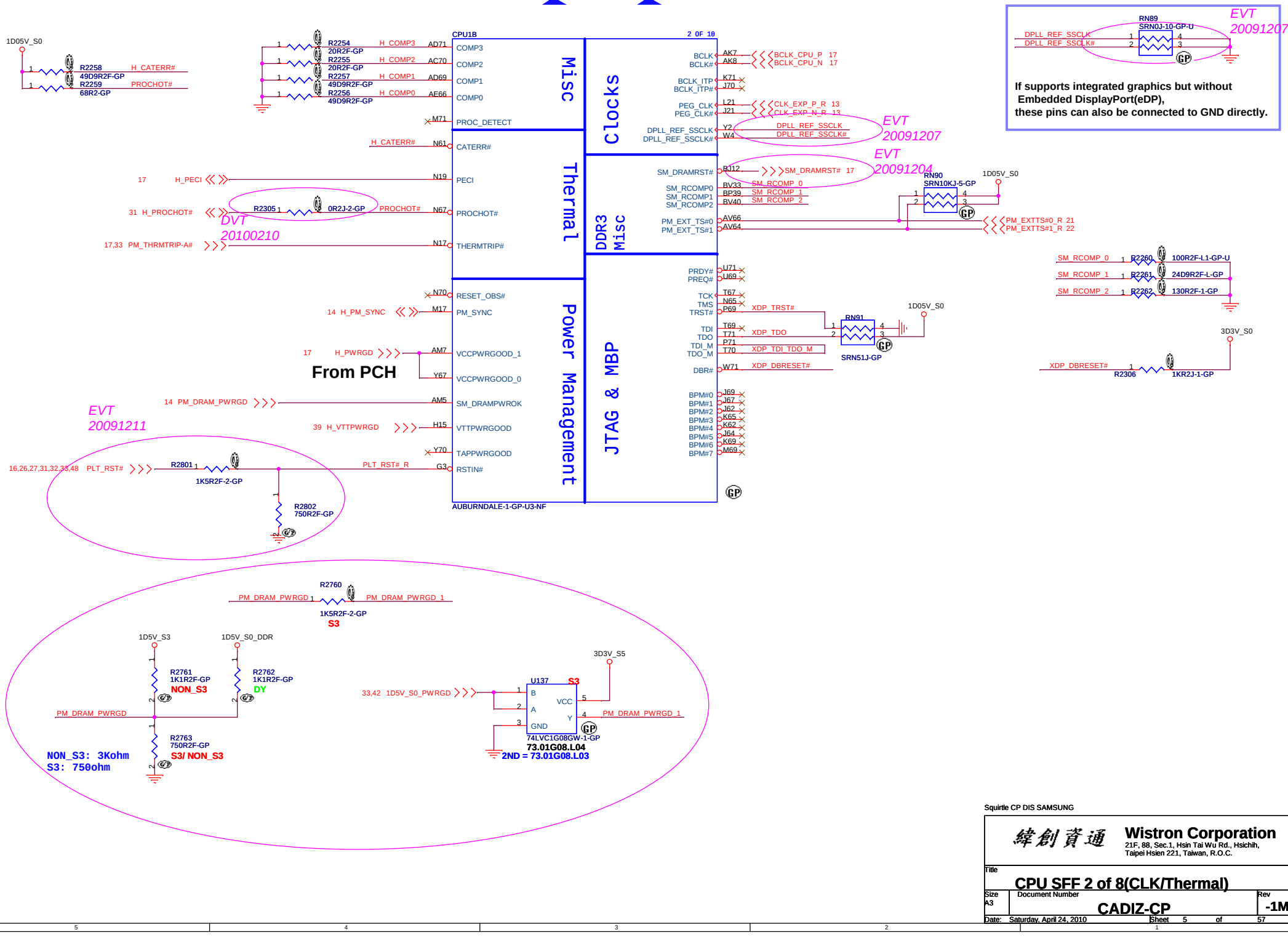
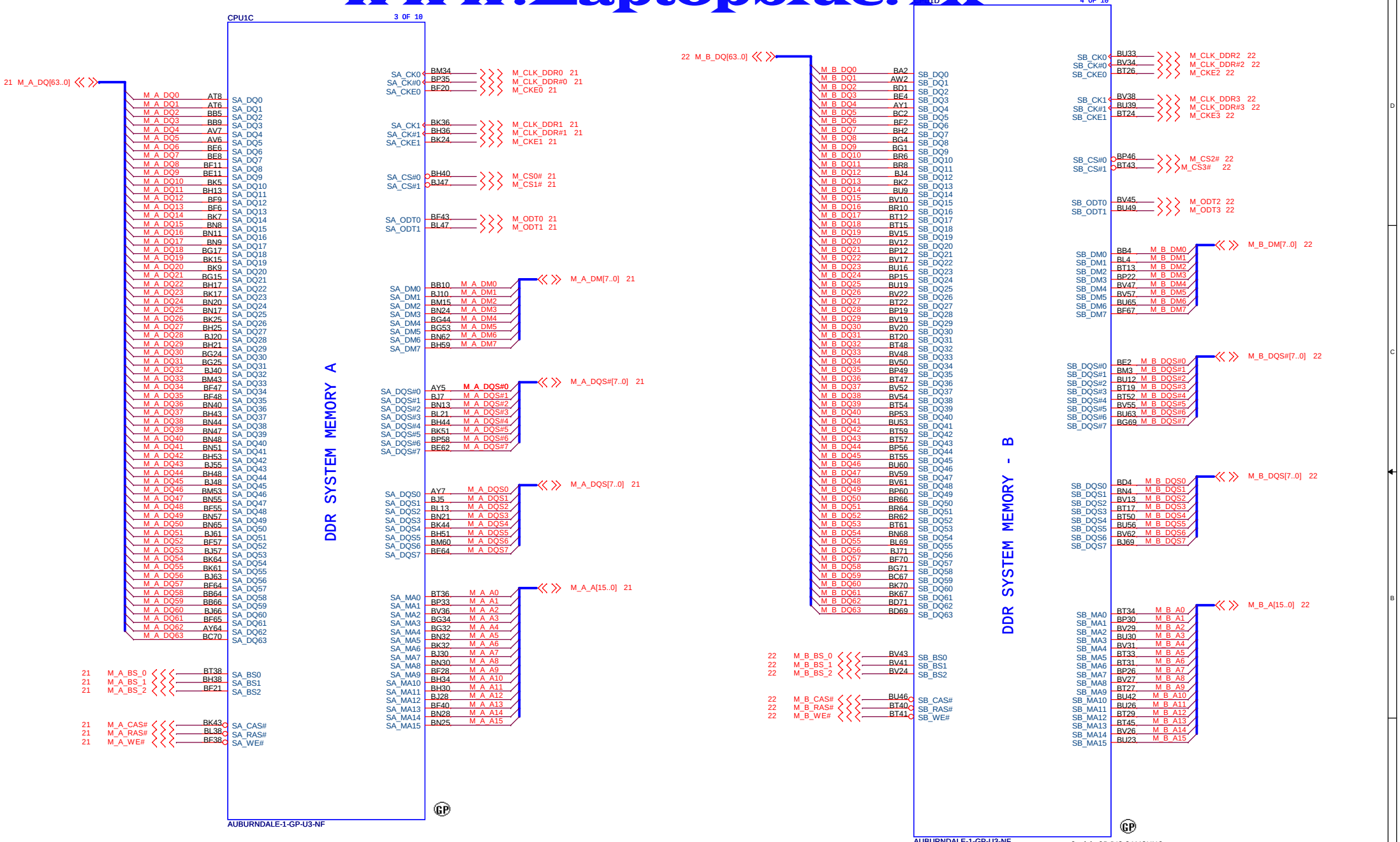
Title	CPU SFF 1 of 8(DMI/FDI/PEG)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 4 of 57	





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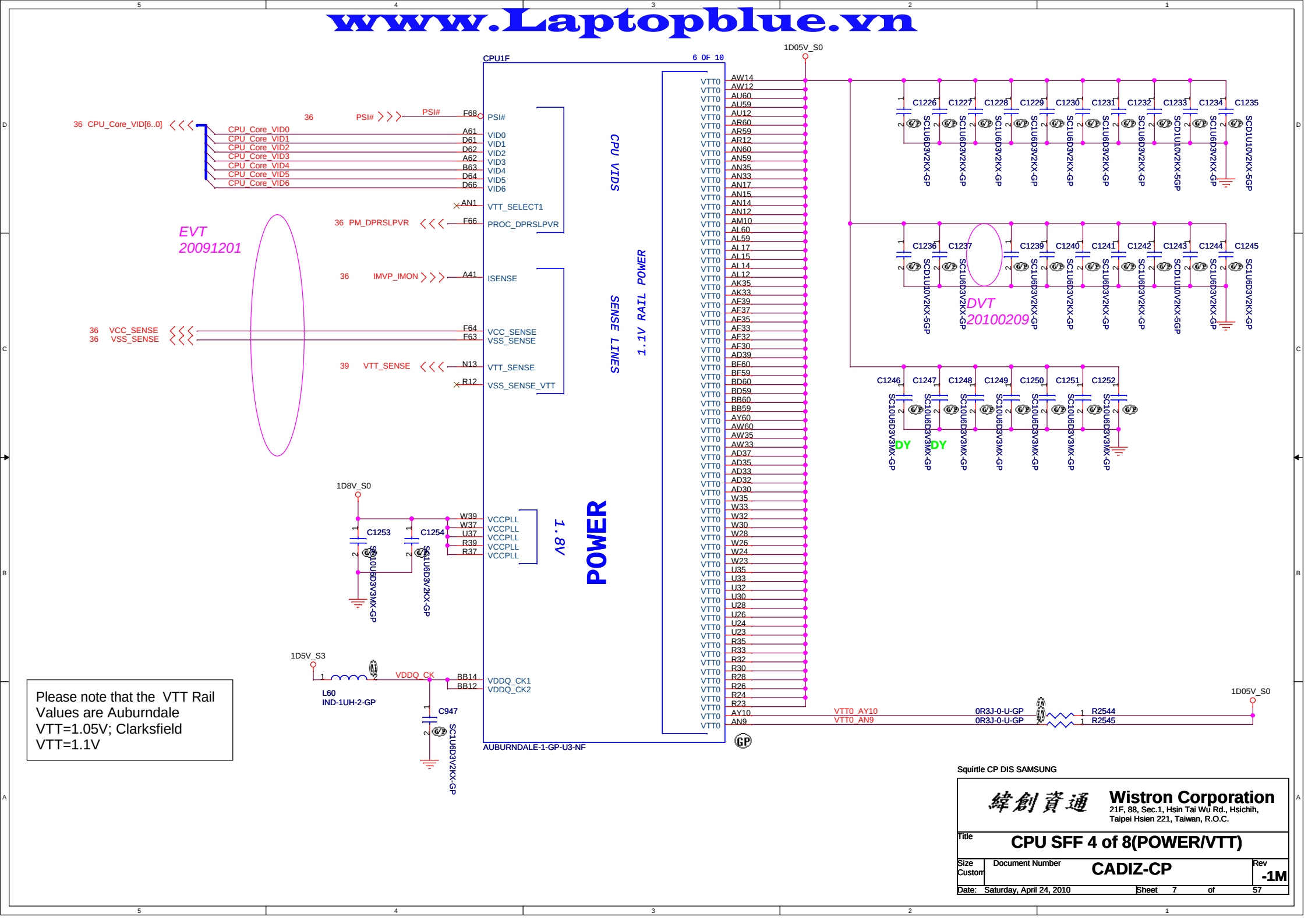
Title: CPU SFF 3 of 8(DDR)

Size	Document Number	Rev
A3	CADIZ-CP	-1M

Date: Saturday, April 24, 2010 Sheet 6 of 57



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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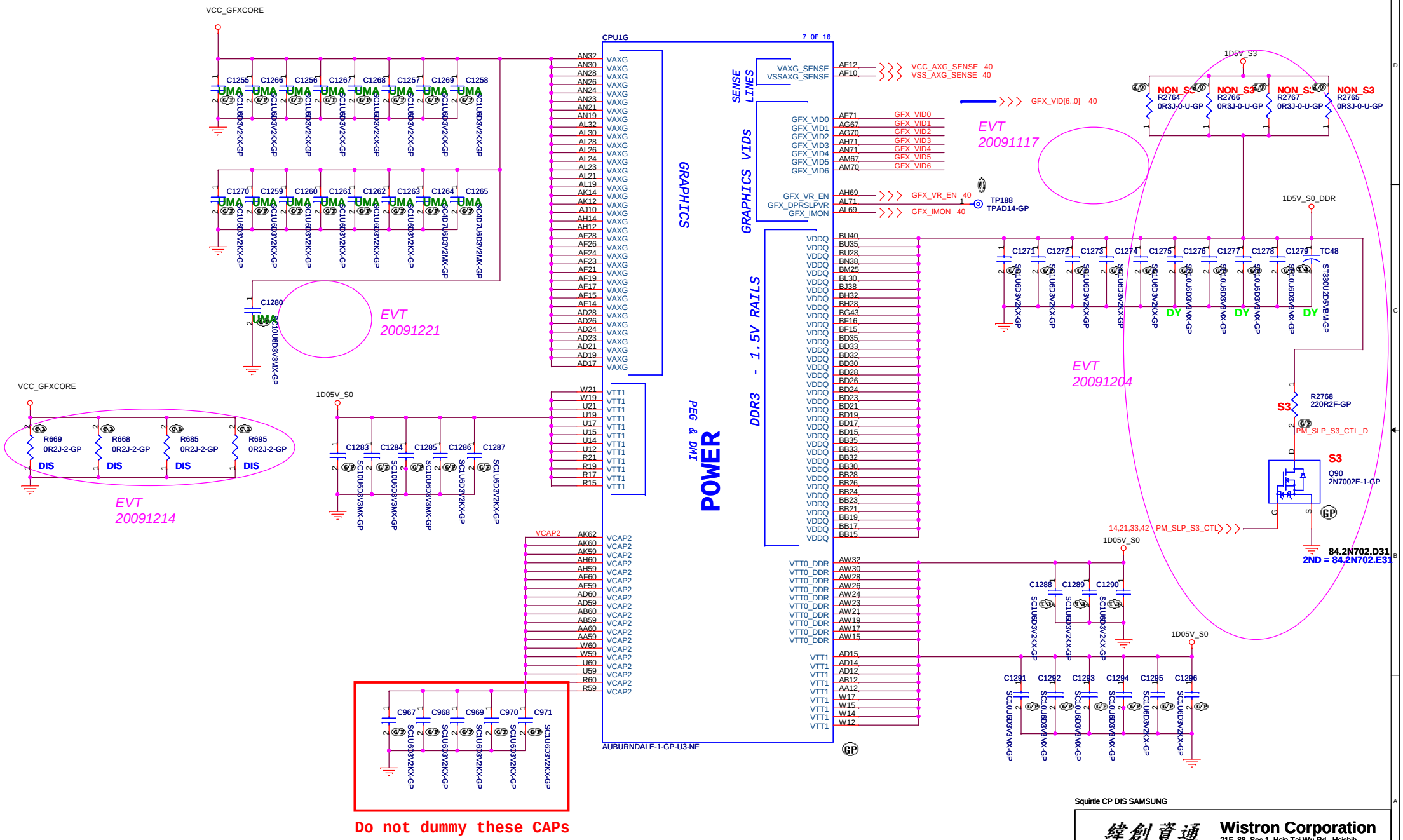
Title	CPU SFF 4 of 8(POWER/VTT)		
Size: Custom	Document Number: CADIZ-CP		Rev: -1M
Date: Saturday, April 24, 2010	Sheet 7 of 57		



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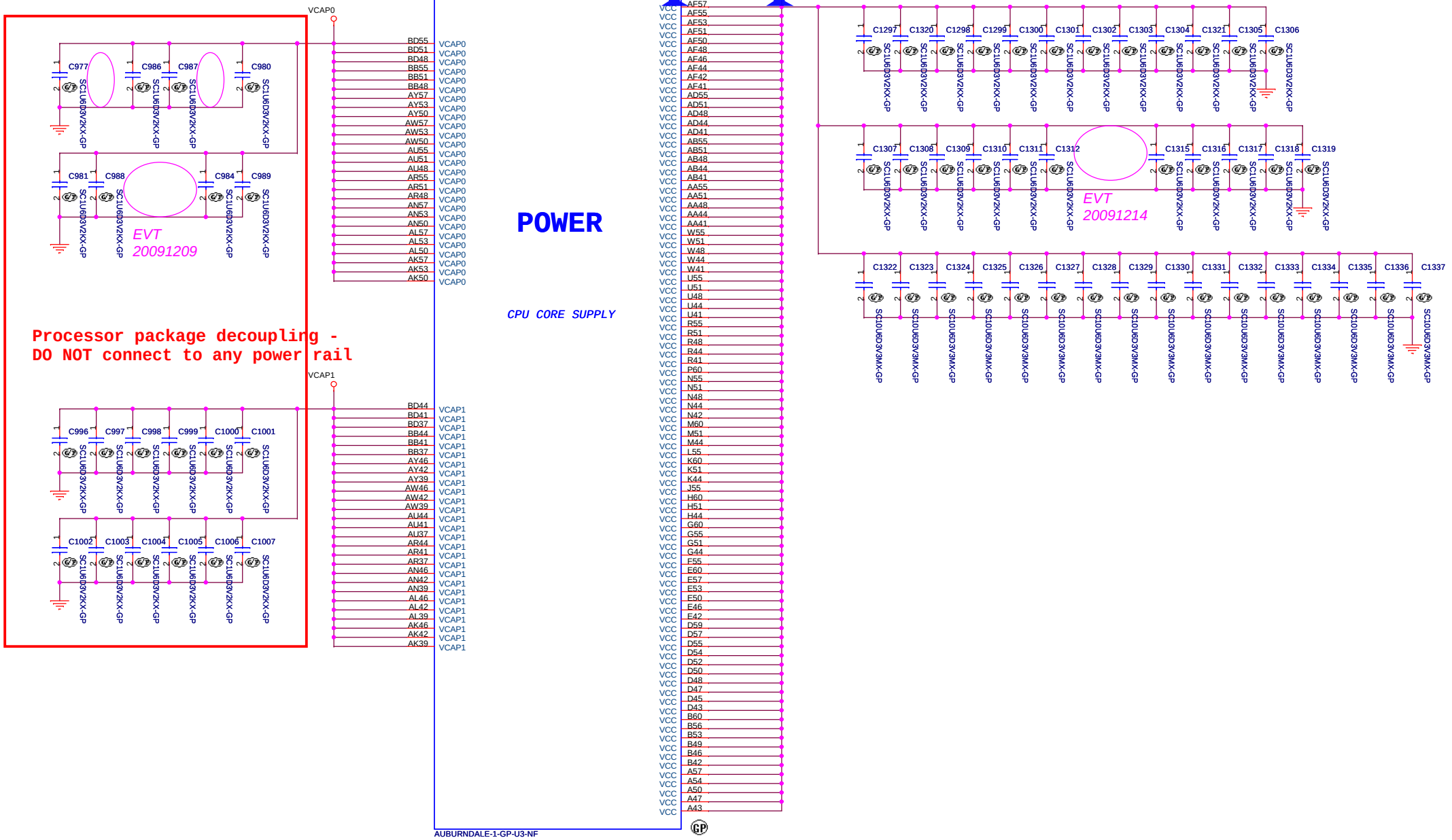
Title	CPU SFF 5 of 8(PWR/DDR/GFX/)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 8 of 57	



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Title	CPU SFF 6 of 8(CPUCORE)	
Size A3	Document Number CADIZ-CP	Rev -1M
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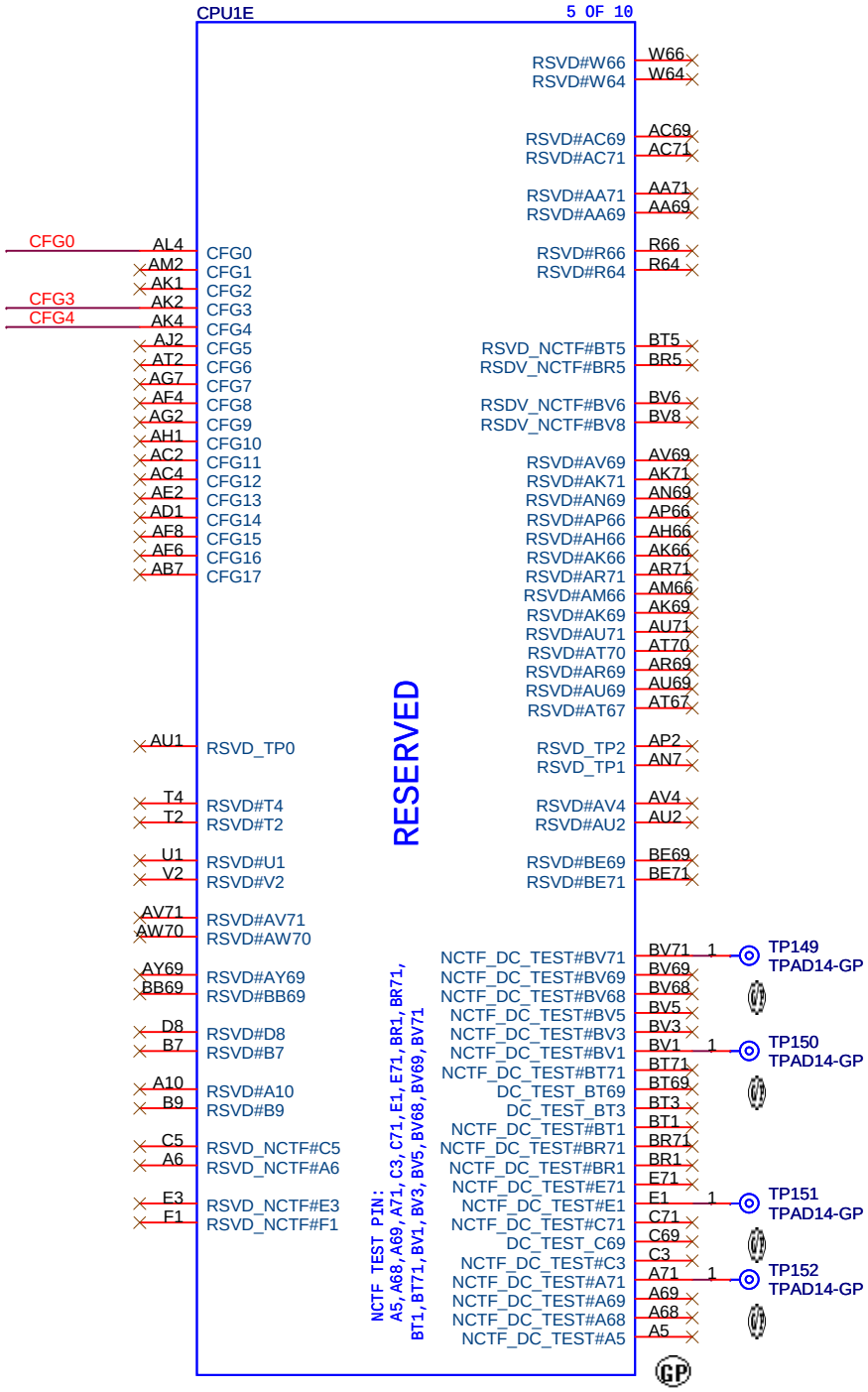

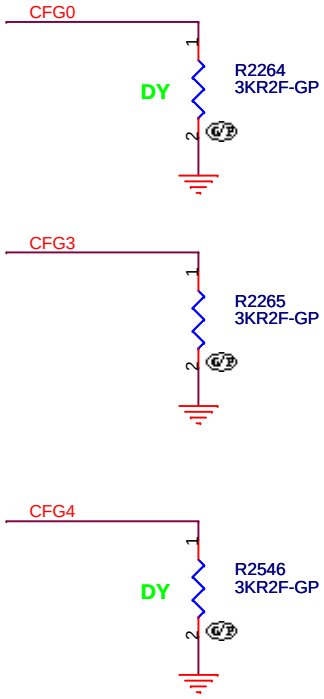

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: **CPU SFF 7 of 8(RESERVED)**

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CPU1I

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VSS

AUBURNDALE-1-GP-U3-NF

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VSS

AUBURNDALE-1-GP-U3-NF

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Title: CPU SFF 8 of 8(VSS)

Size	Document Number	Rev
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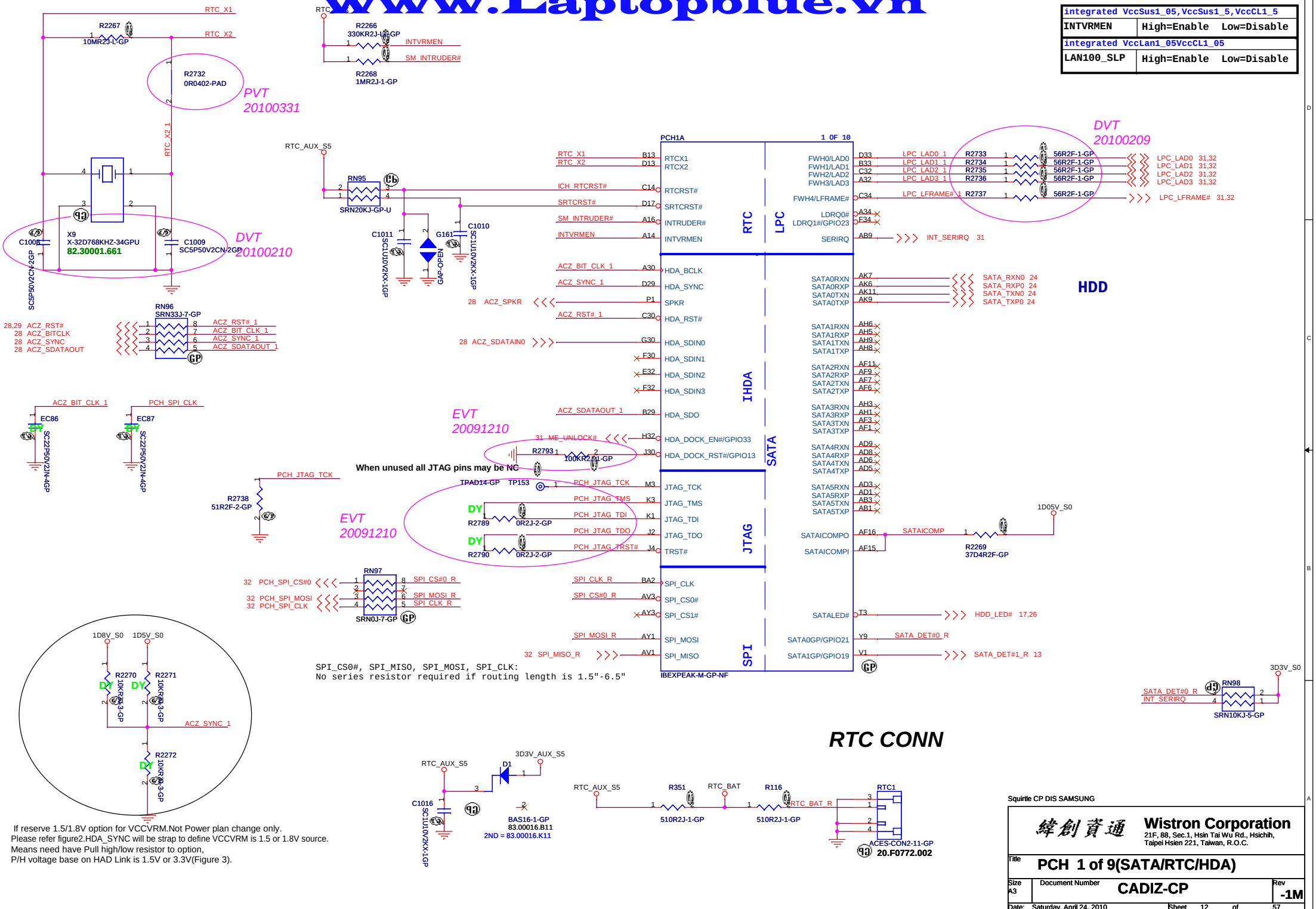
integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



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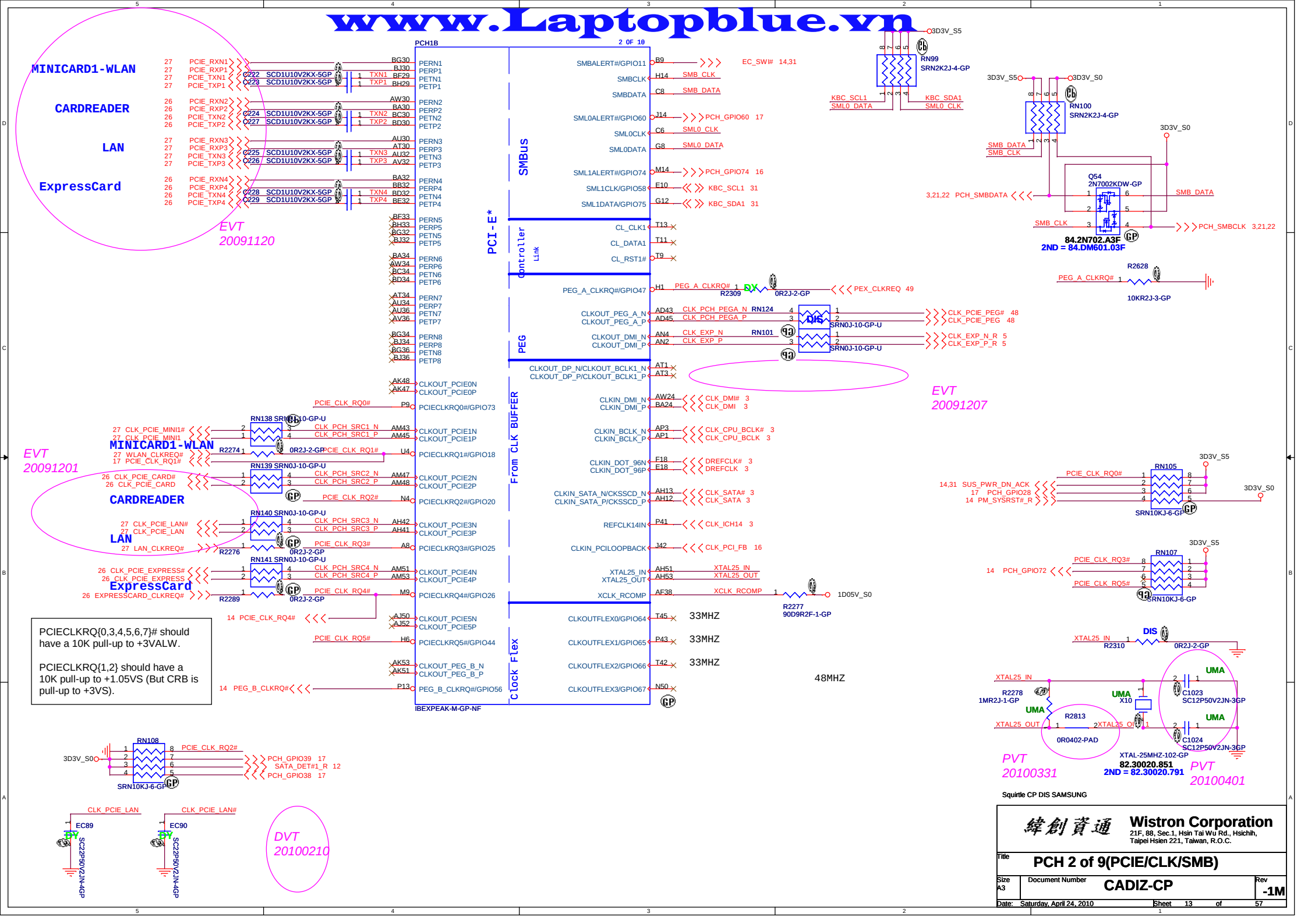
Title	PCH 1 of 9(SATA/RTC/HDA)		
Size A3	Document Number CADIZ-CP		Rev -1M
Date: Saturday, April 24, 2010	Sheet 12 of 57		



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Title	PCH 2 of 9(PCIE/CLK/SMB)	
Size A3	Document Number CADIZ-CP	Rev -1M
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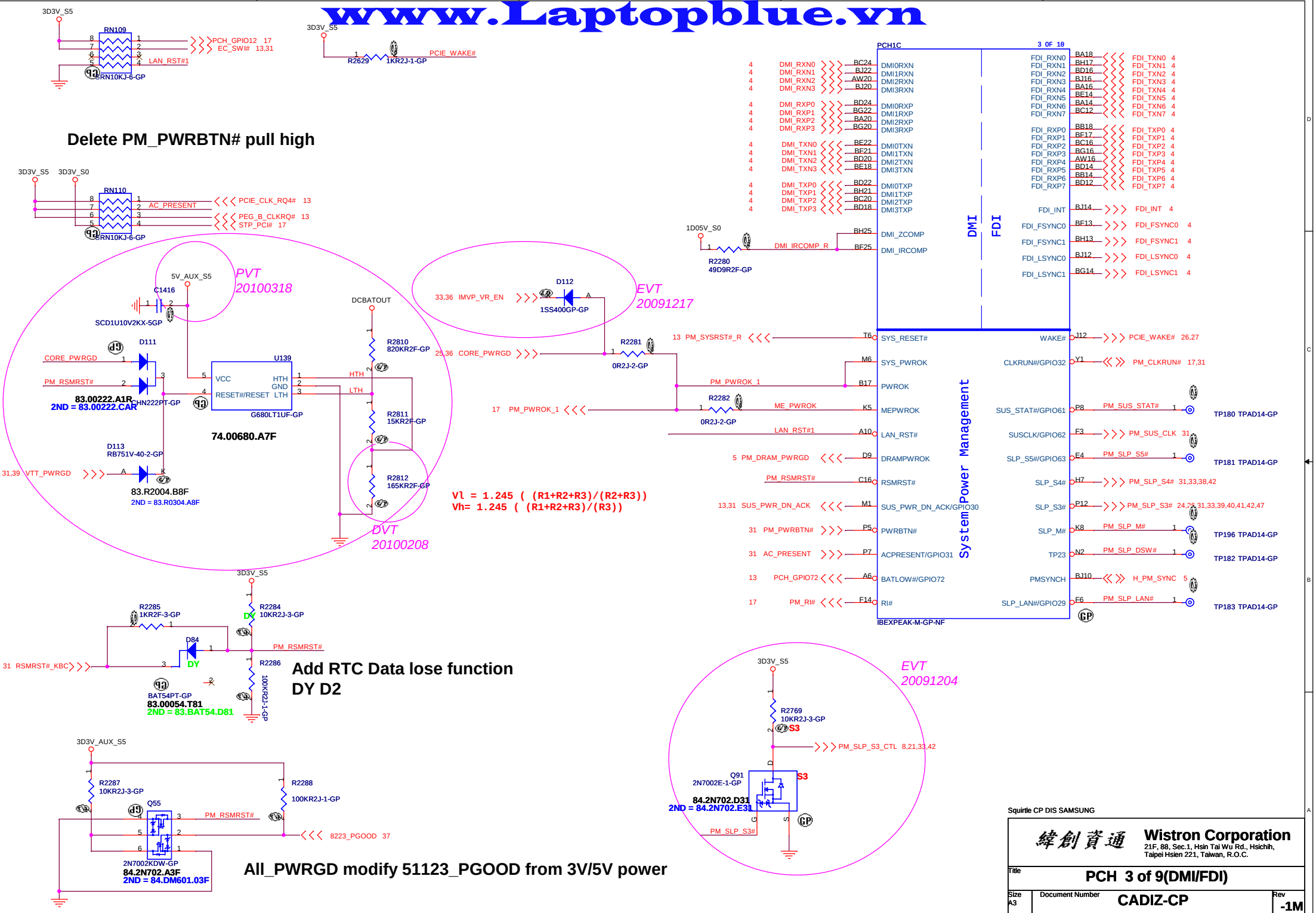
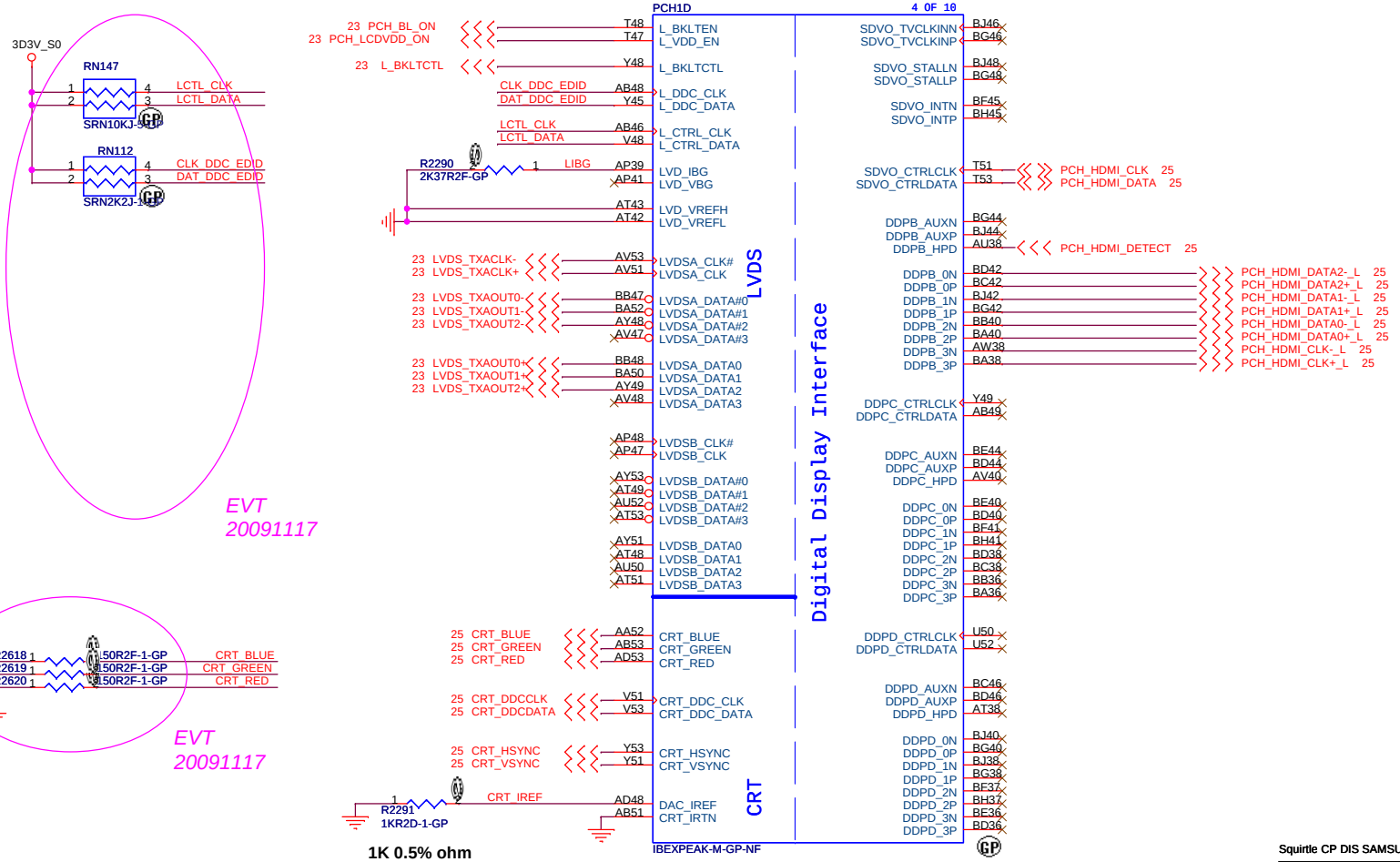


Panel backlight enable control for LVDS
used to gate power into the backlight circuit



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Title: PCH 4 of 9(LVDS/CRT/DP)

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3D3V_S0

RN114 SRN8K2J-4-GP
- 1 — 8 — INT_PIRQH#
- 2 — 7 — PCI_REQ1#
- 3 — 6 — PCI_FRAME#
- 4 — 5 — dGPU_SELECT#

RN144 SRN8K2J-4-GP
- 1 — 8 — PCI_IRDY#
- 2 — 7 — PCI_STOP#
- 3 — 6 — INT_PIRQD#
- 4 — 5 — PCI_SERR#

RN115 SRN8K2J-4-GP
- 1 — 8 — PCI_REQ3#
- 2 — 7 — INT_PIRQF#
- 3 — 6 — INT_PIRQB#
- 4 — 5 — PCI_REQ0#

RN145 SRN8K2J-4-GP
- 1 — 8 — PCI_DEVSEL#
- 2 — 7 — PCI_TRDY#
- 3 — 6 — PCI_PERR#
- 4 — 5 — PCI_PLOCK#

RN116 SRN8K2J-4-GP
- 1 — 8 — INT_PIRQE#
- 2 — 7 — INT_PIRQA#
- 3 — 6 — INT_PIRQC#
- 4 — 5 — INT_PIRQG#

PCI_GNT0# — 1 — DY — R2292 1KR2J-1-GP
PCI_GNT1# — 1 — DY — R2293 1KR2J-1-GP
USE SPI

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

These pins are left as NC, because the function is disable.

PCH1E — 5 OF 10

PCI
- AD0 H40, AD1 N34, AD2 C44, AD3 A38, AD4 C36, AD5 J34, AD6 A40, AD7 D45, AD8 E36, AD9 H48, AD10 F40, AD11 C40, AD12 M48, AD13 M45, AD14 F53, AD15 M40, AD16 M43, AD17 J36, AD18 K48, AD19 F40, AD20 C42, AD21 K46, AD22 M51, AD23 J52, AD24 K51, AD25 L34, AD26 F42, AD27 J40, AD28 G46, AD29 F44, AD30 M47, AD31 H36
- C/BE0# J50, C/BE1# G42, C/BE2# H47, C/BE3# G34
- INT_PIRQA# G38 — PIRQA#
- INT_PIRQB# H51 — PIRQB#
- INT_PIRQC# B37 — PIRQC#
- INT_PIRQD# A44 — PIRQD#
- PCI_REQ0# F51 — REQ0#
- PCI_REQ1# A46 — REQ1#/GPIO50
- dGPU_SELECT# B45 — REQ2#/GPIO52
- PCI_REQ3# M53 — REQ3#/GPIO54
- PCI_GNT0# F48 — GNT0#
- PCI_GNT1# K45 — GNT1#/GPIO51
- F36 — GNT2#/GPIO53
- H53 — GNT3#/GPIO55
- INT_PIRQE# B41 — PIRQE#/GPIO2
- INT_PIRQF# K53 — PIRQF#/GPIO3
- INT_PIRQG# A36 — PIRQG#/GPIO4
- INT_PIRQH# A48 — PIRQH#/GPIO5
- K6 — PCIRST#
- PCI_SERR# F44 — SERR#
- PCI_PERR# E50 — PERR#
- PCI_IRDY# A42 — IRDY#
- H44 — PAR
- PCI_DEVSEL# F46 — DEVSEL#
- PCI_FRAME# C46 — FRAME#
- PCI_PLOCK# D49 — PLOCK#
- PCI_STOP# D41 — STOP#
- PCI_TRDY# C48 — TRDY#
- M7 — PME#
- D5 — PLTRST#

NVRAM
- NV_CE#0 AY9, NV_CE#1 BD1, NV_CE#2 AP15, NV_CE#3 BD8
- NV_DQS0 AV9, NV_DQS1 BG8
- NV_DQ0/NV_IO0 AP7, NV_DQ1/NV_IO1 AP6, NV_DQ2/NV_IO2 AT6, NV_DQ3/NV_IO3 AT9, NV_DQ4/NV_IO4 BB1, NV_DQ5/NV_IO5 AV6, NV_DQ6/NV_IO6 BB3, NV_DQ7/NV_IO7 BA4, NV_DQ8/NV_IO8 BE4, NV_DQ9/NV_IO9 BB6, NV_DQ10/NV_IO10 BD6, NV_DQ11/NV_IO11 BB7, NV_DQ12/NV_IO12 BC8, NV_DQ13/NV_IO13 BJ8, NV_DQ14/NV_IO14 BJ6, NV_DQ15/NV_IO15 BG6
- NV_ALE BD3, NV_CLE AY6
- NV_RCOMP AU2
- NV_RB# AV7
- NV_WR#0_RE# AY8, NV_WR#1_RE# AY5
- NV_WE#_CK0 AV11, NV_WE#_CK1 BF5

USB
- USBP0N H18, USBP0P J18 — USBPN0 27, USBPP0 27
- USBP1N A18, USBP1P C18 — USBPN1 27, USBPP1 27
- USBP2N N20, USBP2P P20
- USBP3N J20, USBP3P L20 — USBPN3 26, USBPP3 26
- USBP4N F20, USBP4P G20 — USBPN4 25, USBPP4 25
- USBP5N A20, USBP5P C20
- USBP6N M22, USBP6P N22
- USBP7N B21, USBP7P D21
- USBP8N H22, USBP8P J22 — USBPN8 27, USBPP8 27
- USBP9N E22, USBP9P F22 — USBPN9 23, USBPP9 23
- USBP10N A22, USBP10P C22 — USBPN10 27, USBPP10 27
- USBP11N G24, USBP11P H24 — USBPN11 32, USBPP11 32
- USBP12N L24, USBP12P M24 — USBPN12 26, USBPP12 26
- USBP13N A24, USBP13P C24 — USBPN13 27, USBPP13 27
- USBRBIAS# B25 — USB_RBIAS_PN — 1 — R2294 22D6R2F-L1-GP
- USBRBIAS D25
- OC0#/GPIO59 N16 — USB_OC#0 — USB_OC#0 27
- OC1#/GPIO40 J16 — USB_OC#1 — USB_OC#1 27
- OC2#/GPIO41 F16 — USB_OC#2 — USB_OC#2 25
- OC3#/GPIO42 L16 — USB_OC#3
- OC4#/GPIO43 E14 — USB_OC#4
- OC5#/GPIO9 G16 — USB_OC#5
- OC6#/GPIO10 F12 — USB_OC#6 — USB_OC#6 17
- OC7#/GPIO14 T15 — USB_OC#7

IBEXPEAK-M-GP-NF

These pins are left as NC, because the function is disable.

USB Table

Pair	Device
0	External #0
1	External #1
2	NC
3	EXPRESS CARD
4	External #2
5	NC
6	NC
7	NC
8	WIMAX(HS)
9	CAMERA(HS)
10	WWAN(HS)
11	FELICA(FS)
12	BLUETOOTH(FS)
13	MULTIMEDIA SIM(FS)

EVT 20091120

5,26,27,31,32,33,48 PLT_RST# — 1 — R2295 100KR2J-1-GP — DY

RN117 SRN22-3-GP
- 32 PCLK_FWH — 2
- 13 CLK_PCI_FB — 1
- CLK_PCI_SIO_R — 4 — N52 CLKOUT_PCI0
- CLK_PCI_FB_R — 3 — P53 CLKOUT_PCI1
- P46 CLKOUT_PCI2
- P51 CLKOUT_PCI3
- P48 CLKOUT_PCI4

31 CLK_PCI_KBC — R2297 — 1 — 47R2J-2-GP — CLK_PCI_KBC_R

PCLK_FWH — EC92 — DY — SC2259V2IN-4GP

DVT 20100210

13 PCH_GPIO74 — RN152 SRN10KJ-6-GP
- USB_OC#3 — 8
- 7
- USB_OC#0 — 6
- USB_OC#7 — 5
- 1
- 2
- 3
- 4

3D3V_S5

EVT 20091214

3D3V_S5

RN35 SRN10KJ-6-GP
- USB_OC#4 — 8
- USB_OC#1 — 7
- USB_OC#2 — 6
- USB_OC#5 — 5
- 1
- 2
- 3
- 4

Squirtle CP DIS SAMSUNG

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Title	PCH 5 of 9(PCI/USB)	
Size A3	Document Number CADIZ-CP	Rev -1M
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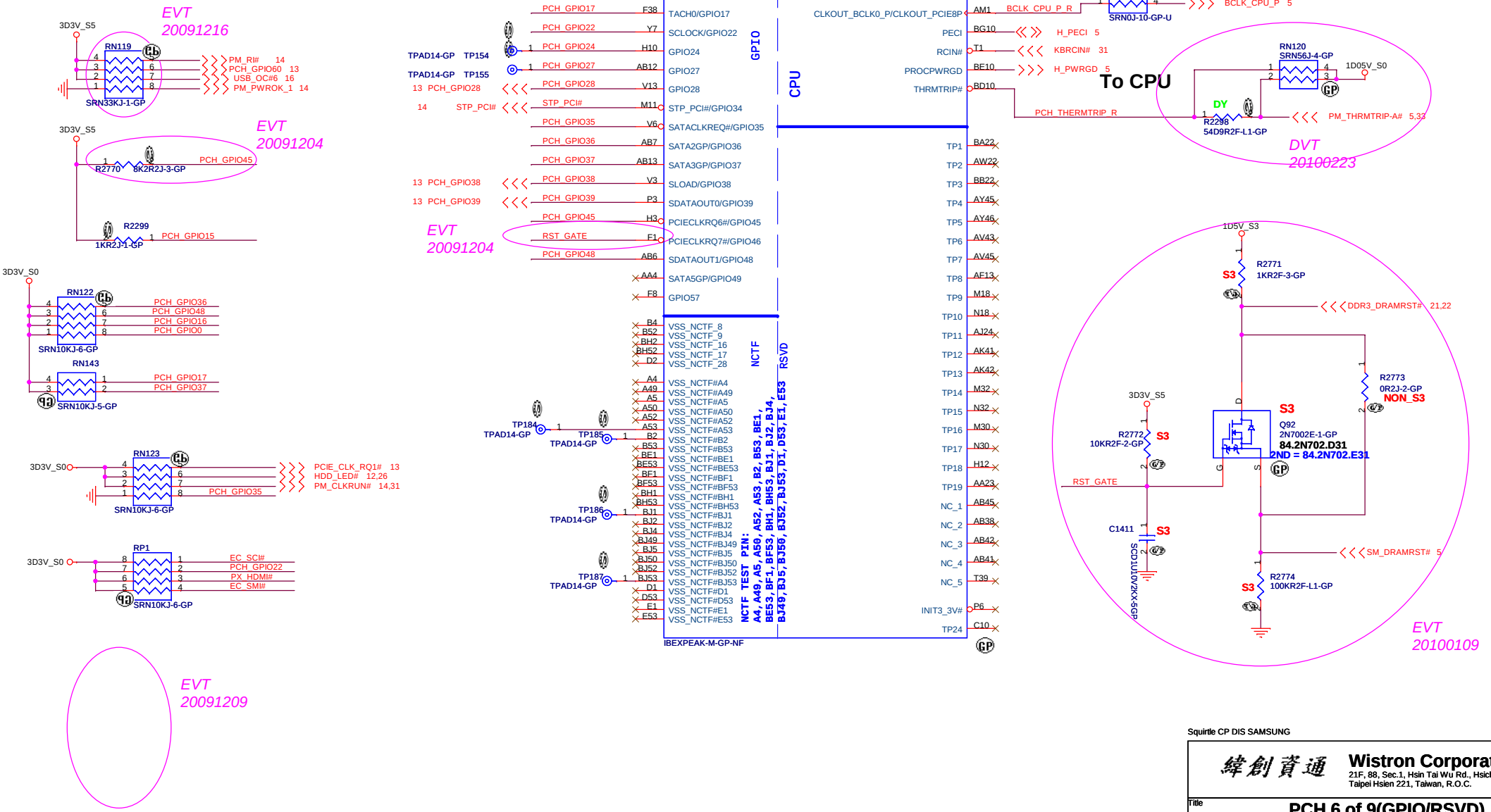
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

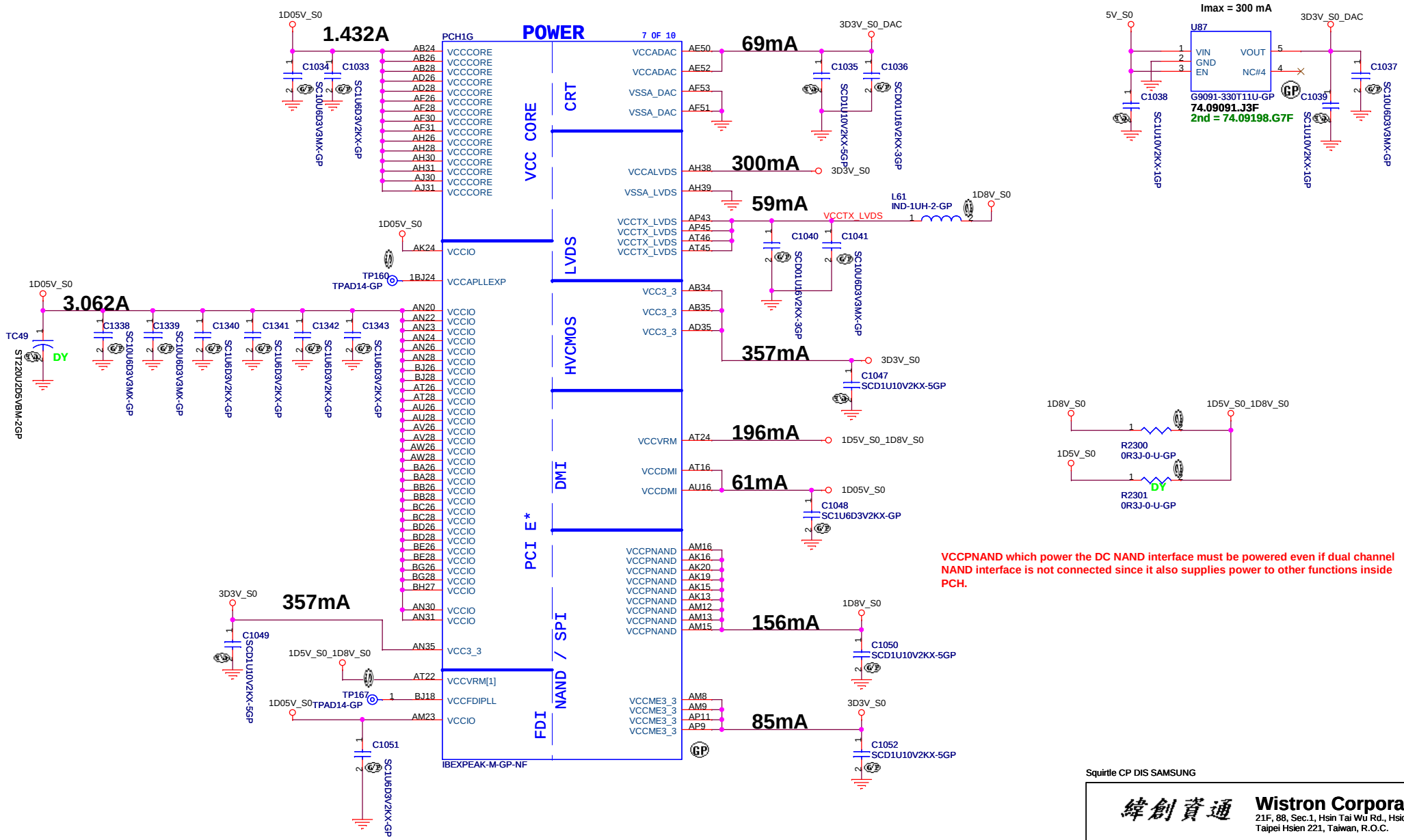
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 6 of 9(GPIO/RSVD)	
Size A3	Document Number CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 17 of 57	

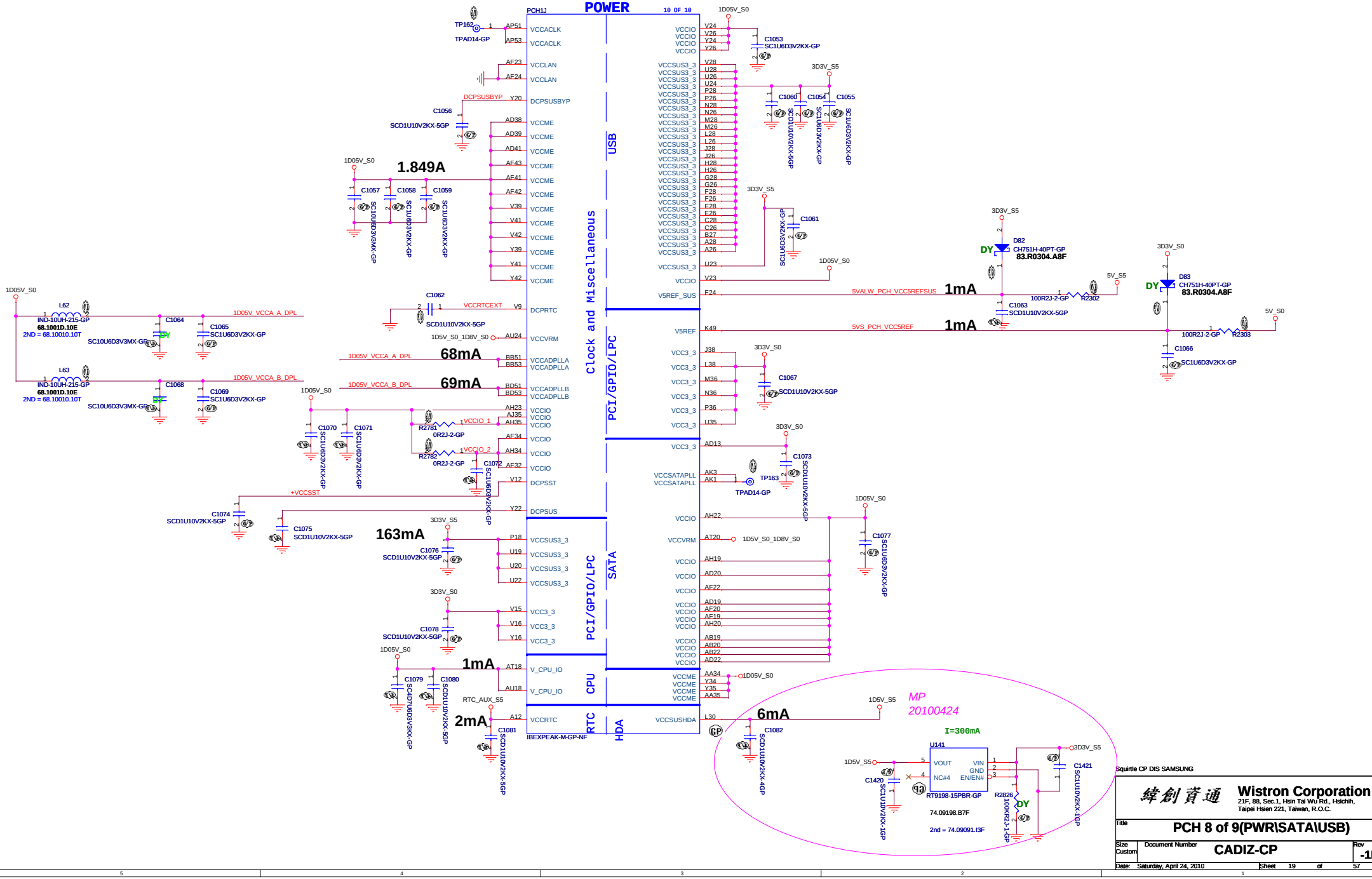


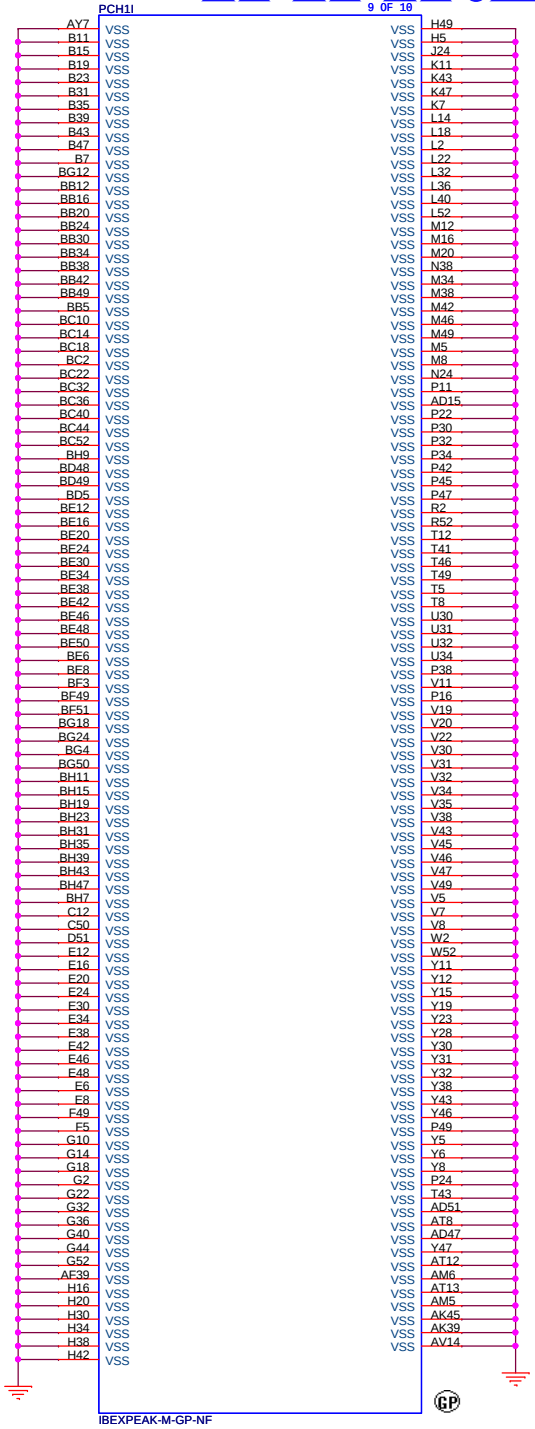
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

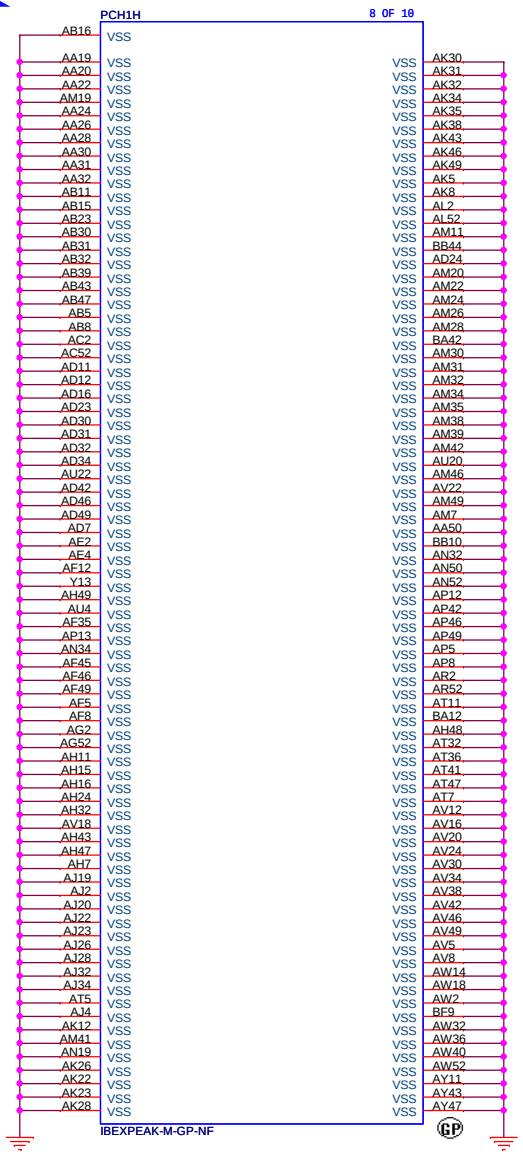
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 7 of 9(PWR/VCORE/LVDS)	
Size: Custom	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 18 of 57	







Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

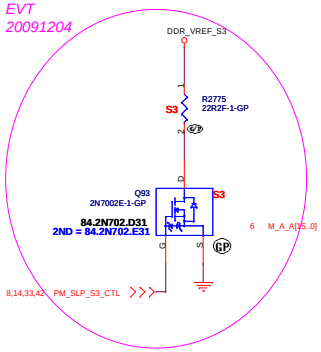
Title: **PCH 9 of 9(VSS)**

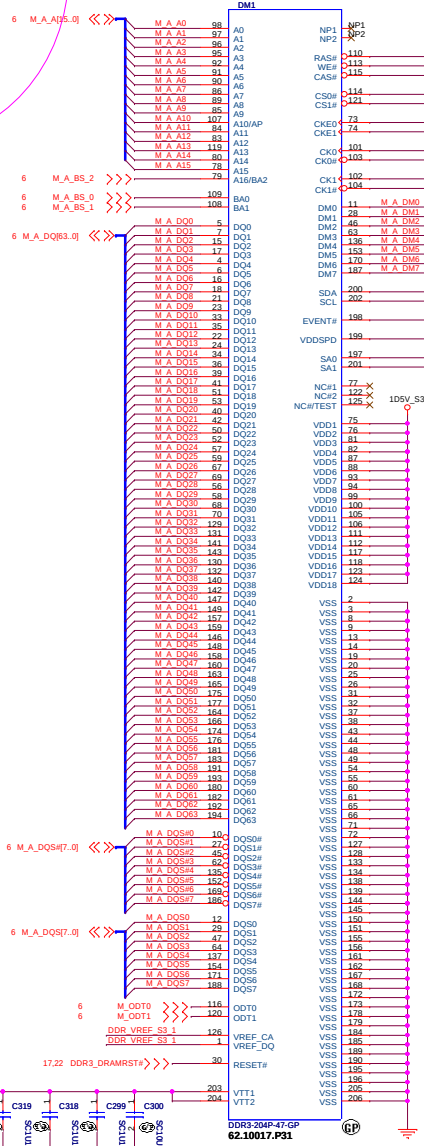
Size	Document Number	Rev
A3	CADIZ-CP	-1M

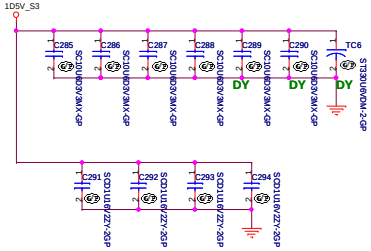
Date: Saturday, April 24, 2010 Sheet 20 of 57

EVT
20091204

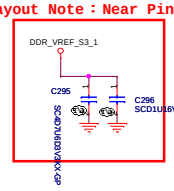
DDR3 SOCKET_1



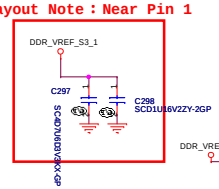




Layout Note : Near Pin 126

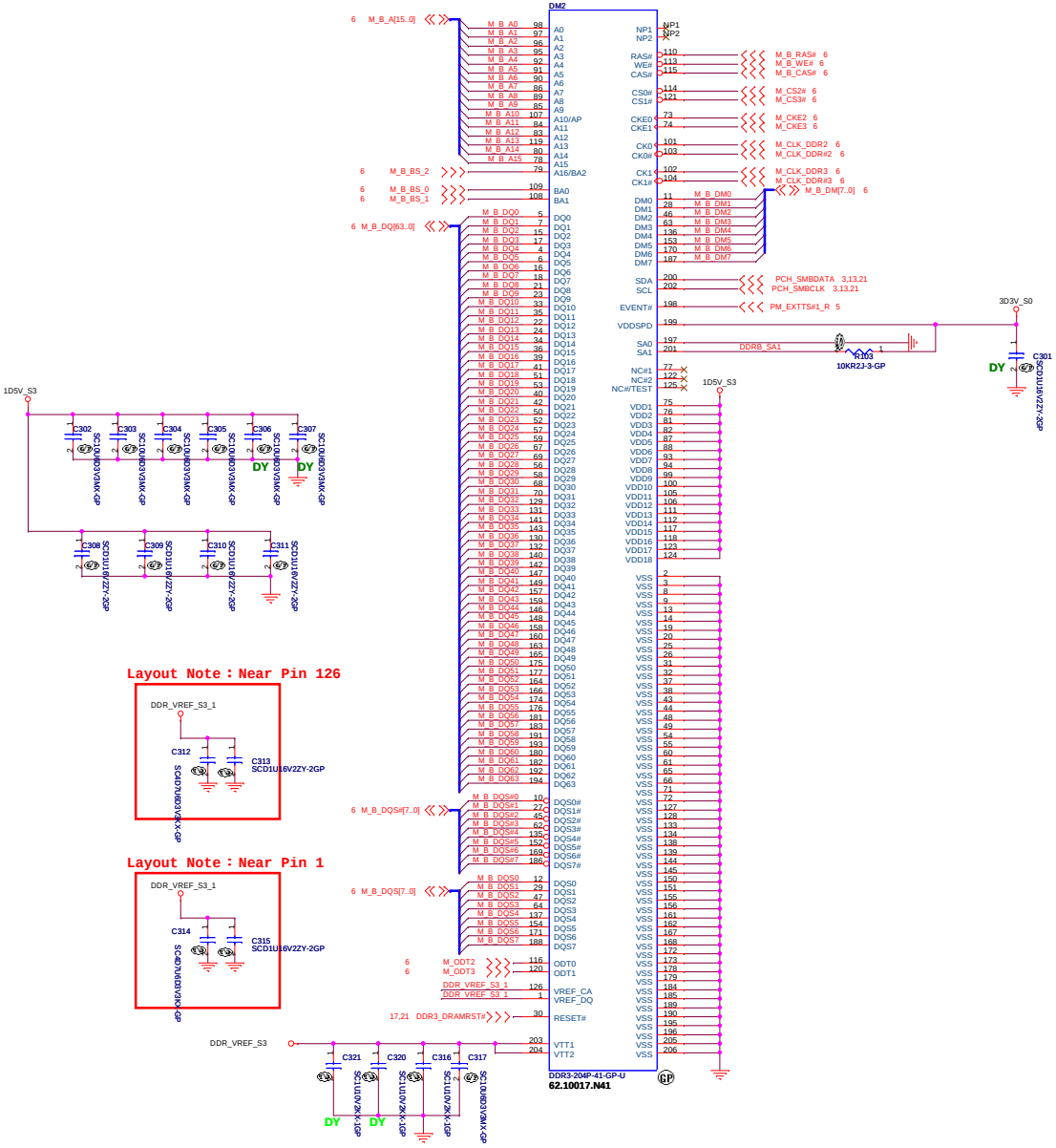


Layout Note : Near Pin 1



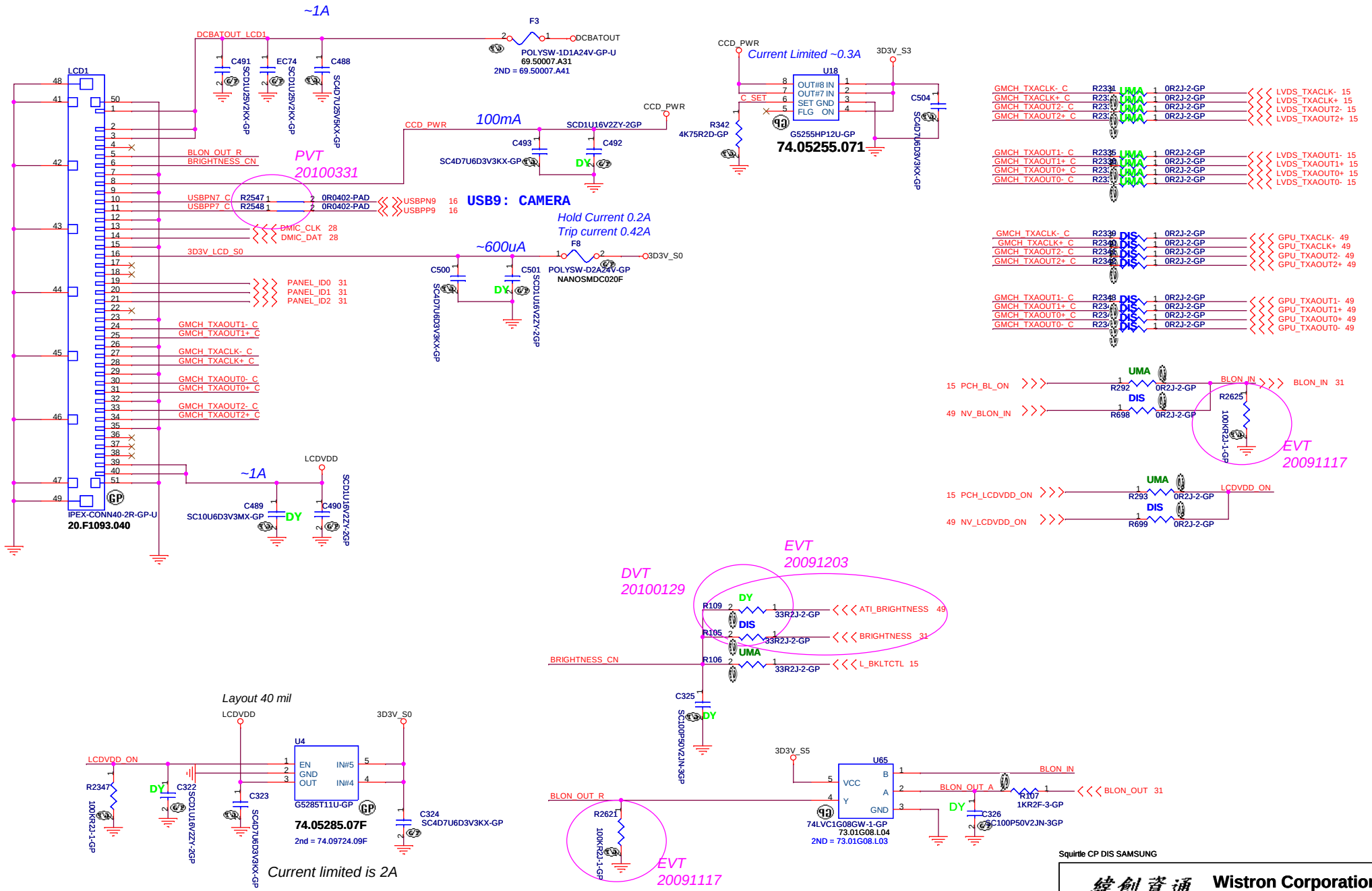
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR3 Socket1	
Size	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 21 of 57	

DDR3 SOCKET_2



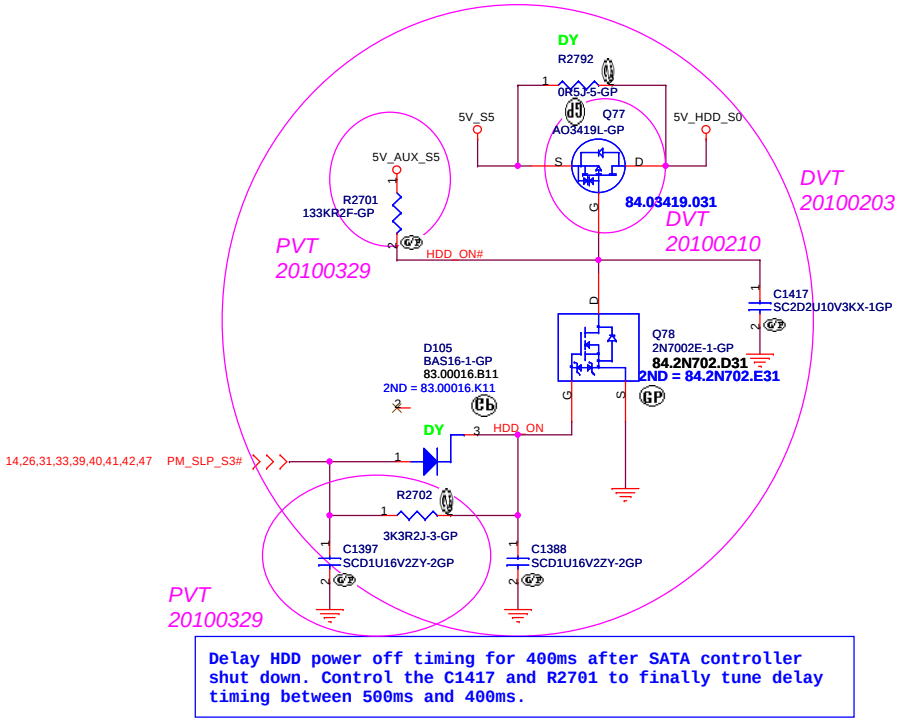
緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	DDR3 Socket2		
Size	Document Number	CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010	Sheet 22 of 57		

LCD/CCD CONN



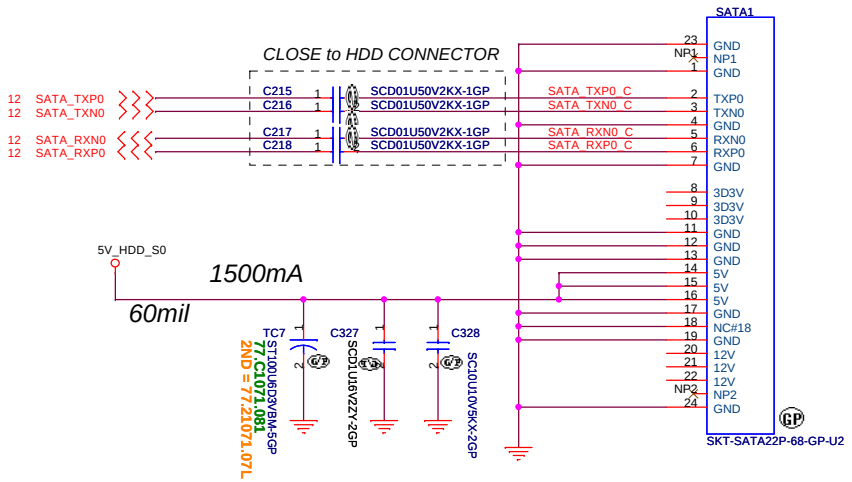
Squirtle CP DIS SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**LCD CONN**
Size	Document Number: **CADIZ-CP** — Rev: -1M
Date: Saturday, April 24, 2010	Sheet 23 of 57

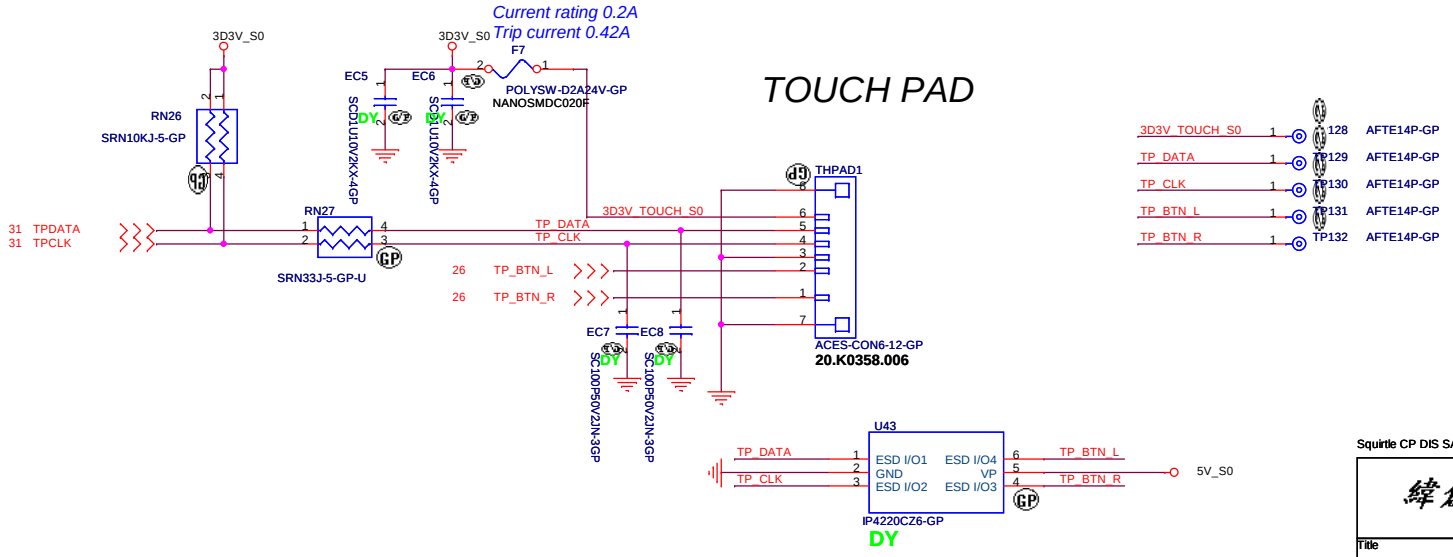


Delay HDD power off timing for 400ms after SATA controller shut down. Control the C1417 and R2701 to finally tune delay timing between 500ms and 400ms.

HDD Connector



TOUCH PAD



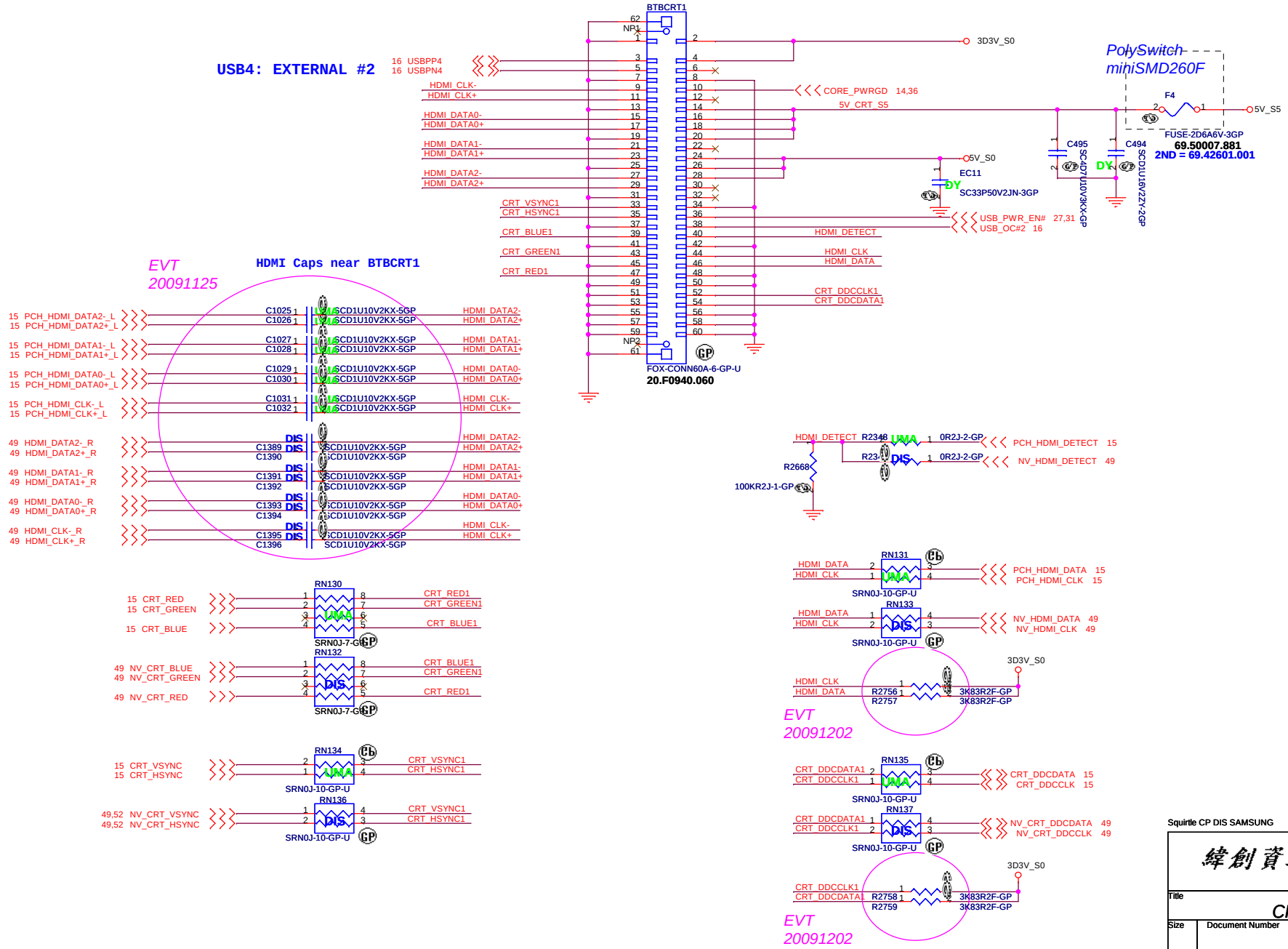
Squirtle CP DIS SAMSUNG

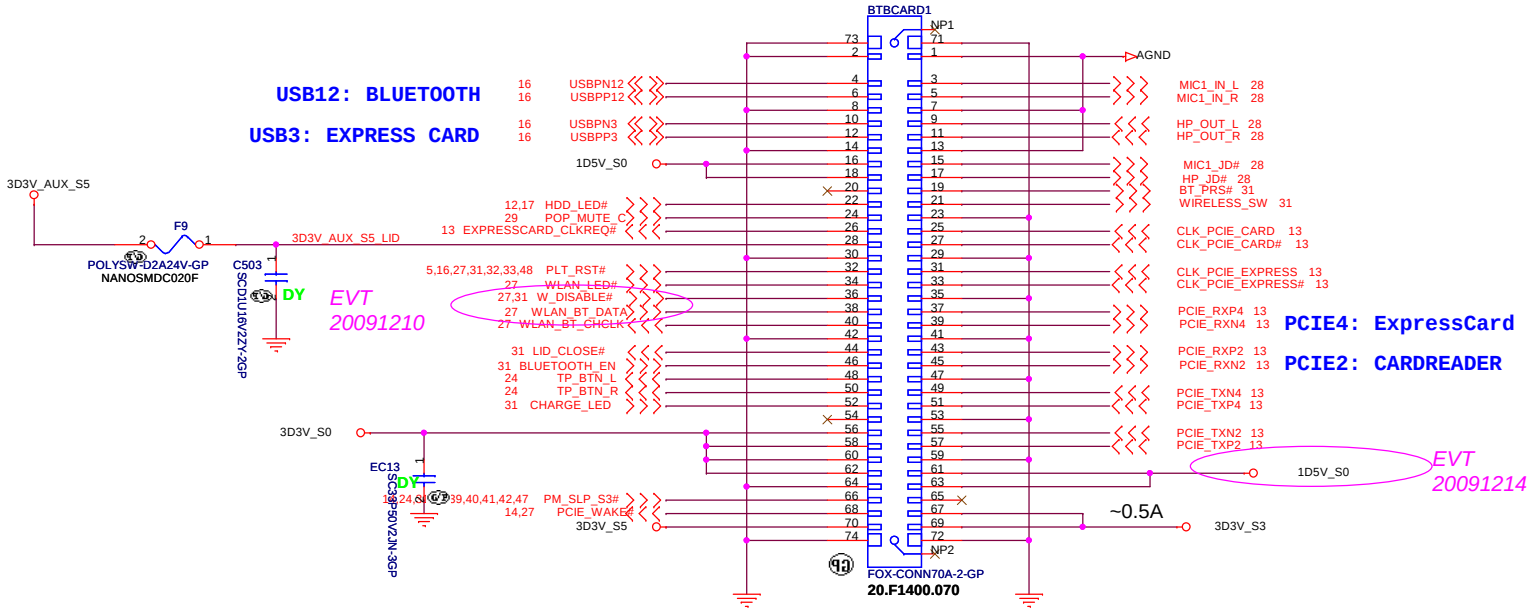
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD CONN & TOUCHPAD**

Size	Document Number	Rev
	CADIZ-CP	-1M

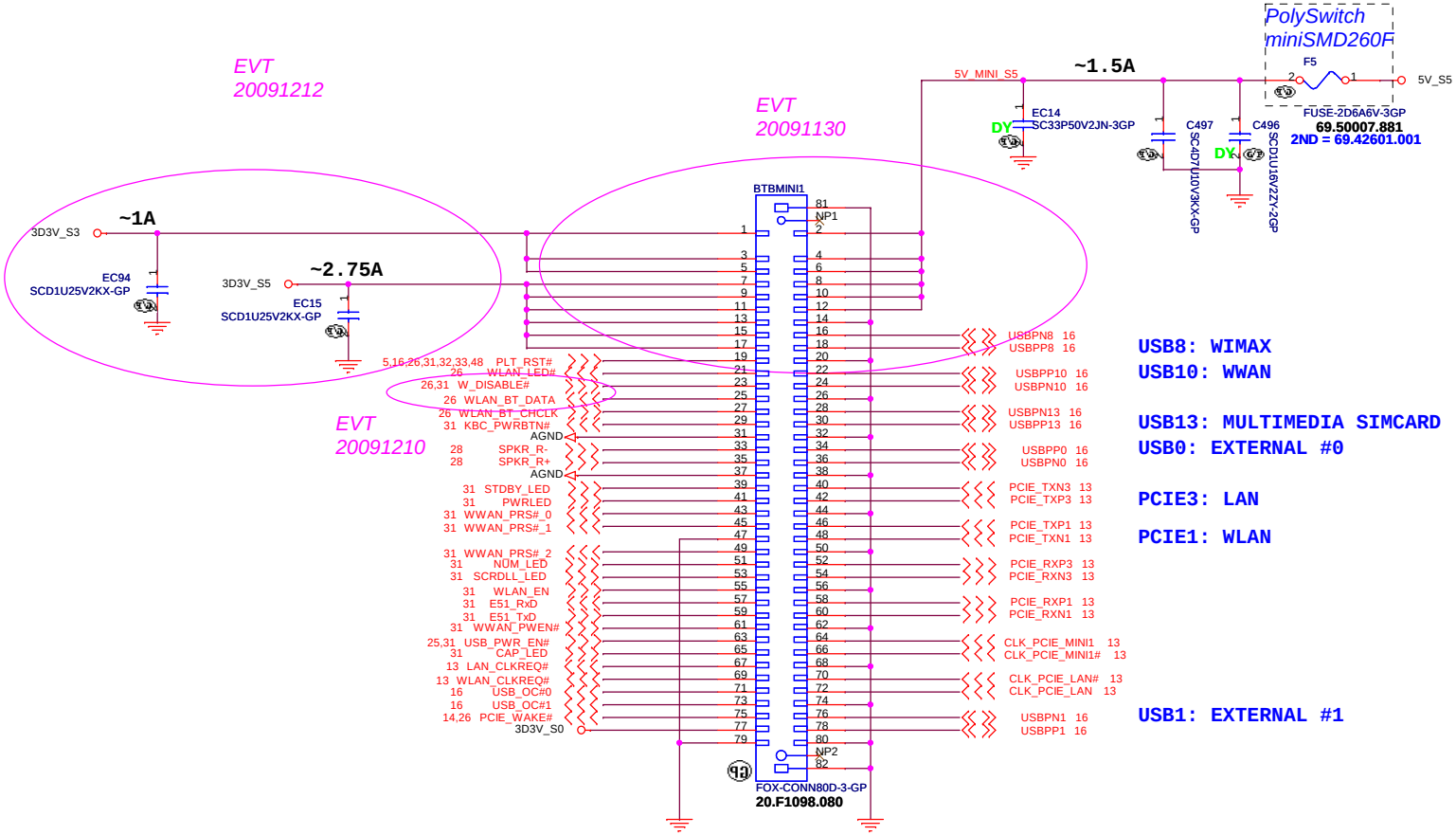
Date: Saturday, April 24, 2010 Sheet 24 of 57





Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CARDREADER BD CONN		
Size	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 26 of 57	



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI BD CONN***

Size	Document Number	Rev
A3	CADIZ-CP	-1M

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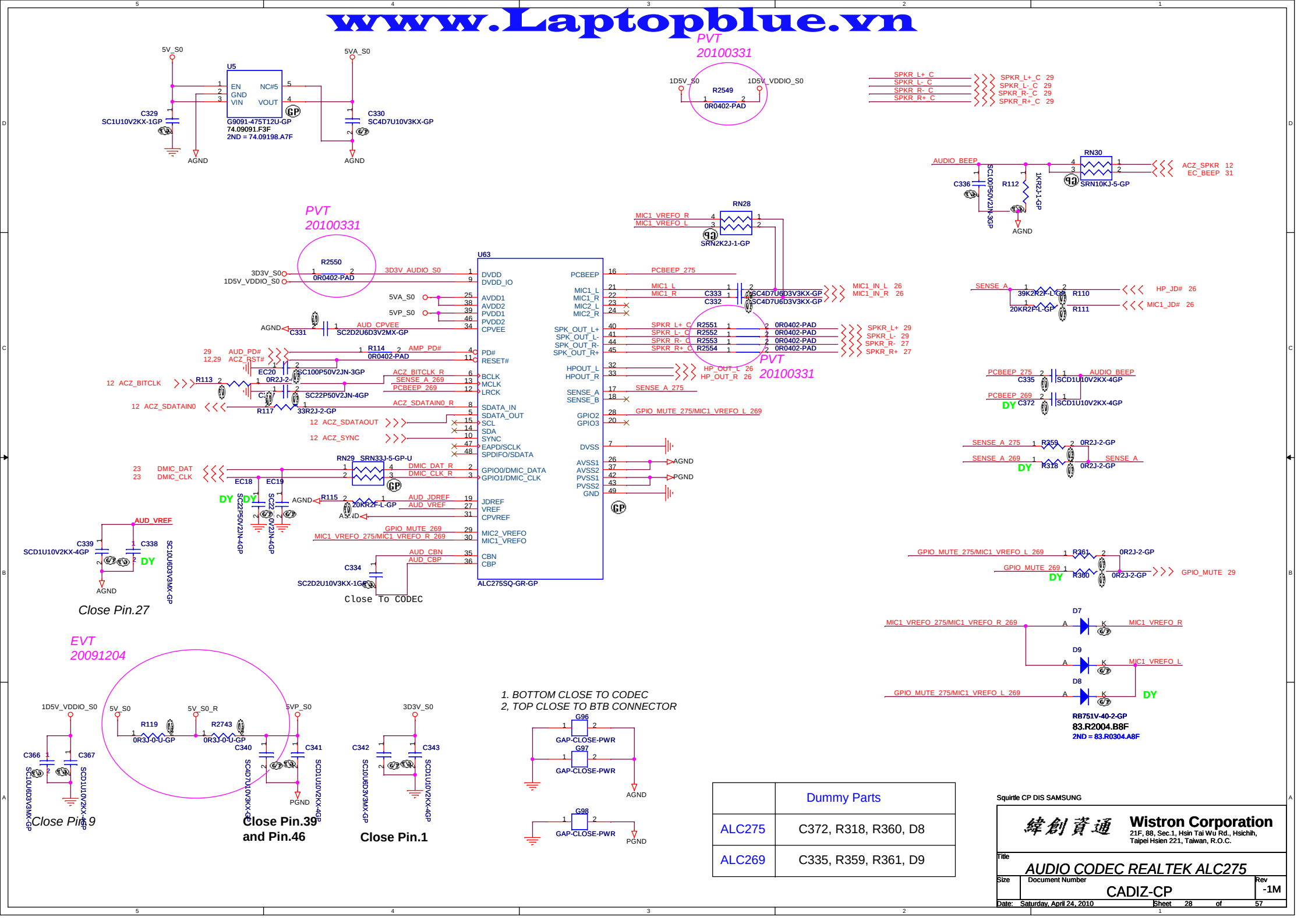

	Dummy Parts
ALC275	C372, R318, R360, D8
ALC269	C335, R359, R361, D9

Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC275*

Size	Document Number	Rev
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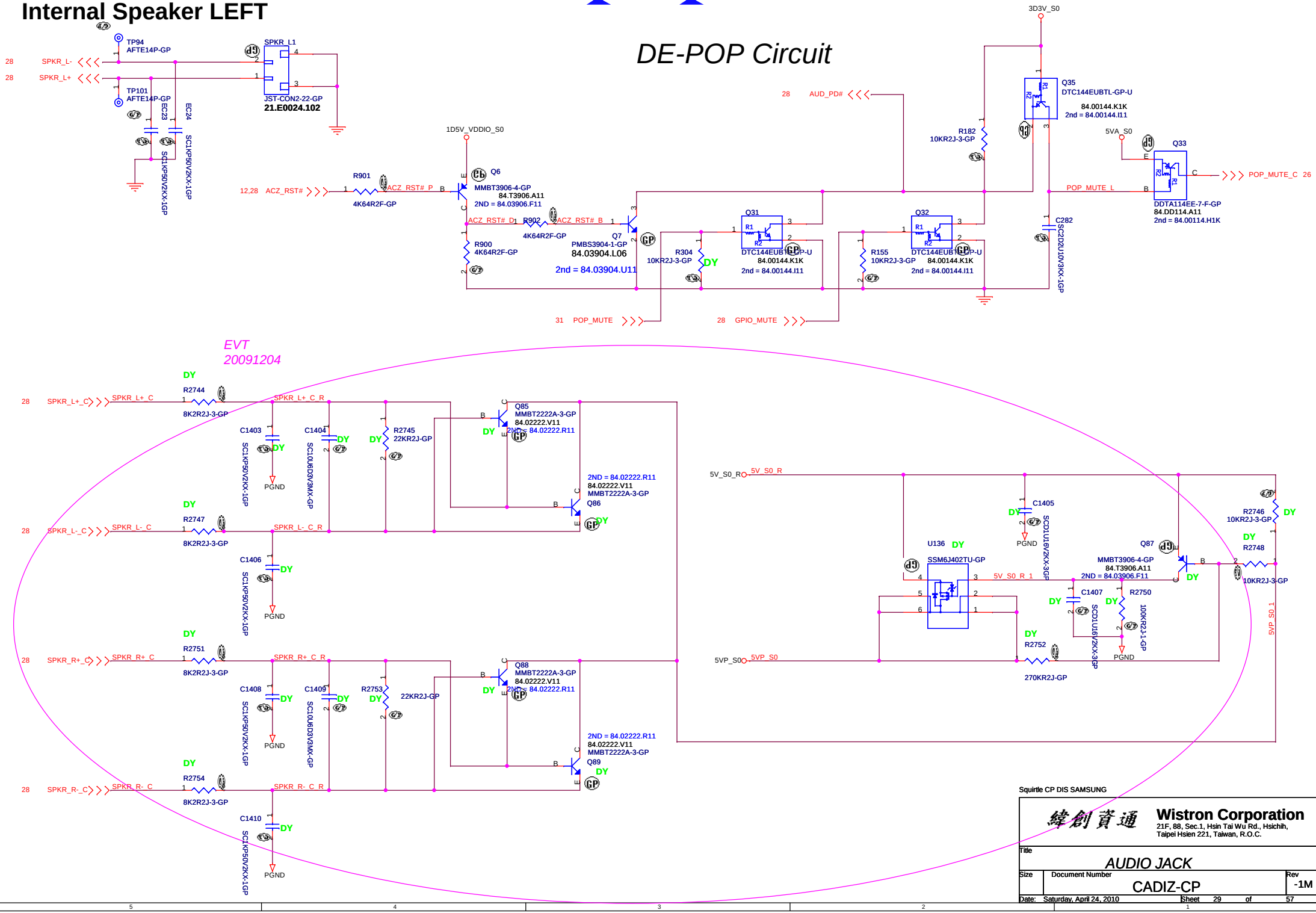
Internal Speaker LEFT

DE-POP Circuit



EVT
20091204

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size	Document Number: CADIZ-CP	Rev: -1M
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for T8 thermal diode

84.03904.L06
2nd = 84.03904.U11
Q3 PMBS3904-1-GP
C118 SC2200P50V2KX-2GP
G787_DP2
G787_DN2

C1252 & C1254 CLOSE TO G787

for system thermal diode

84.03904.L06
2nd = 84.03904.U11
Q15 PMBS3904-1-GP
C346 SC2200P50V2KX-2GP
G787_DP1
G787_DN1

EVT
20091201

49 GPU_TEMP+ R2712 0R2J-2-GP G787_DN2
DIS

49 GPU_TEMP- R2713 0R2J-2-GP G787_DP2
DIS

5V_FAN_S0
C344 SC4D7U10V3KX-GP
C345 SCD1U16V2ZY-2GP

5V_FAN_S0 1 TP136 AFTE14P-GP
FAN_PWM 1 TP137 AFTE14P-GP
FAN_TACH 1 TP138 AFTE14P-GP
FAN_PRS# 1 TP139 AFTE14P-GP

ps. FAN1 POWER TRACE WIDTH ~15 MIL
Max current is 235mA;
Stopped is ~10mA

31 FAN_PWM1 R358 0R2J-2-GP
SCD1U16V2ZY-2GP DY EC9 FAN_PWM

FAN1
FAN_PWM
FAN_TACH
31 FAN_PRS#
EC81 SC220P50V2JN-3GP
EC35 SC220P50V2JN-3GP
MLX-CON5-12-GP
20.F0693.005

5V_S0
R350 DY 0R2J-2-GP
R355 10KR2J-3-GP
D23 RB551V30-GP
31 FAN_TACH1
FAN_TACH
83.R5003.H8H
2ND = 83.5R003.08F

5V_S0
R426 100R2J-2-GP
C533 SCD1U16V2KX-3GP
C147 DY SC10U6D3V3MX-GP

5V_S0_THERMAL

U15
VCC
THERM# PURE_HW_SHUTDOWN#
THERM_SET THERM_SET
DXP1 G787_DP1
DP2DN3 G787_DP2
DN2DP3 G787_DN2
ALERT# ALERT# R291 10KR2J-3-GP 3D3V_S0
SDA SMBD_THERM 31
SCL SMBC_THERM 31
TEST TPAD14-GP TP49 TP28
SGND1 G787_DN1
NC#8 NC#9 NC#12 NC#15
GND GND
G787R41U-GP
74.00787.0B3

R429 21KR2F-GP
R430 49K9R2F-L-GP

T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC

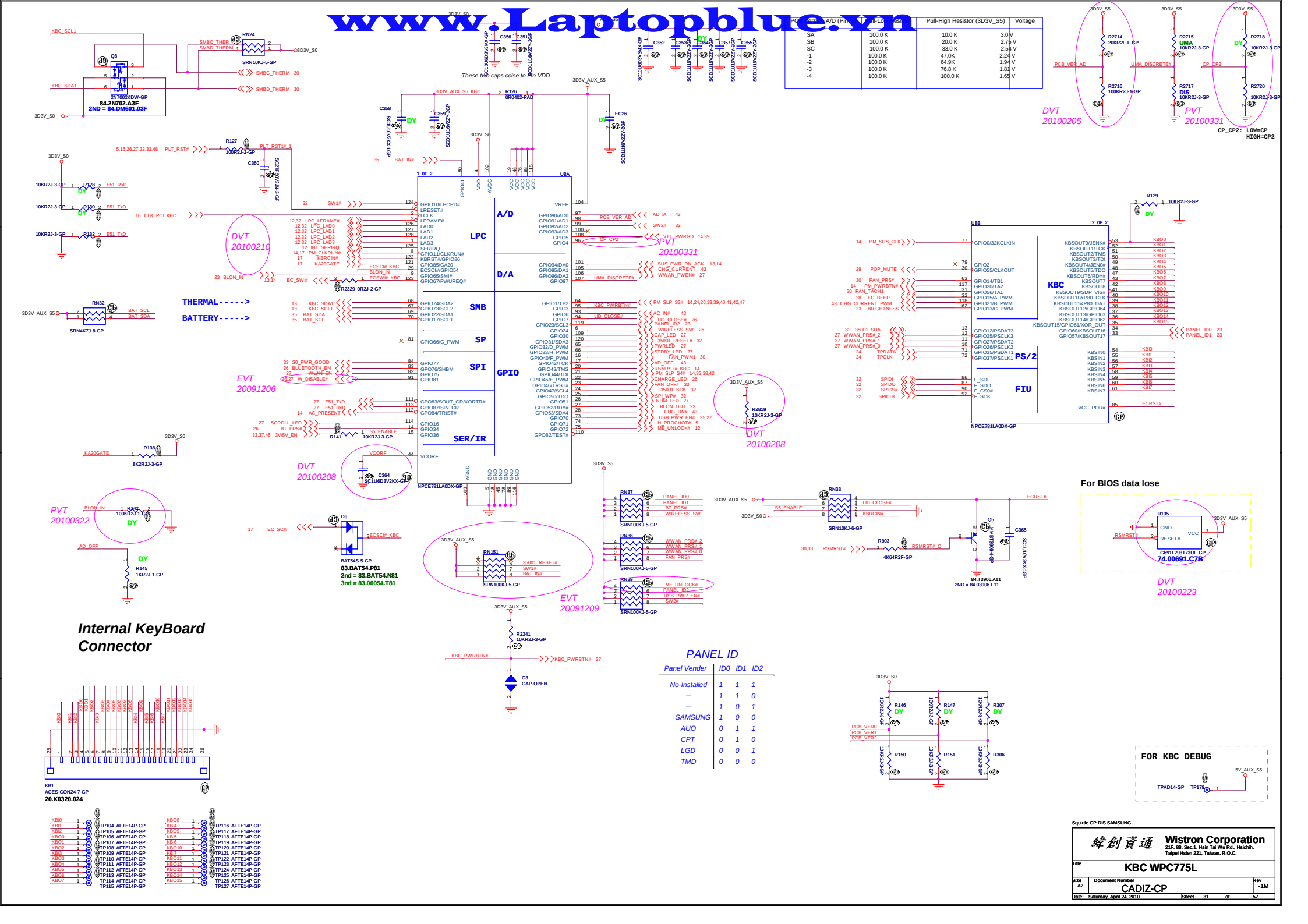
5V_S0
Q47 AO3413-GP
5V_FAN_S0
84.03413.A31
2nd = 84.02130.031
R73 100KR2J-1-GP
FAN_OFF
Q13 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
31 FAN_OFF#

3D3V_S0
R125 10KR2J-3-GP
PURE_HW_SHUTDOWN#
3D3V_S0
Q4 2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
RSMRST# 31,33

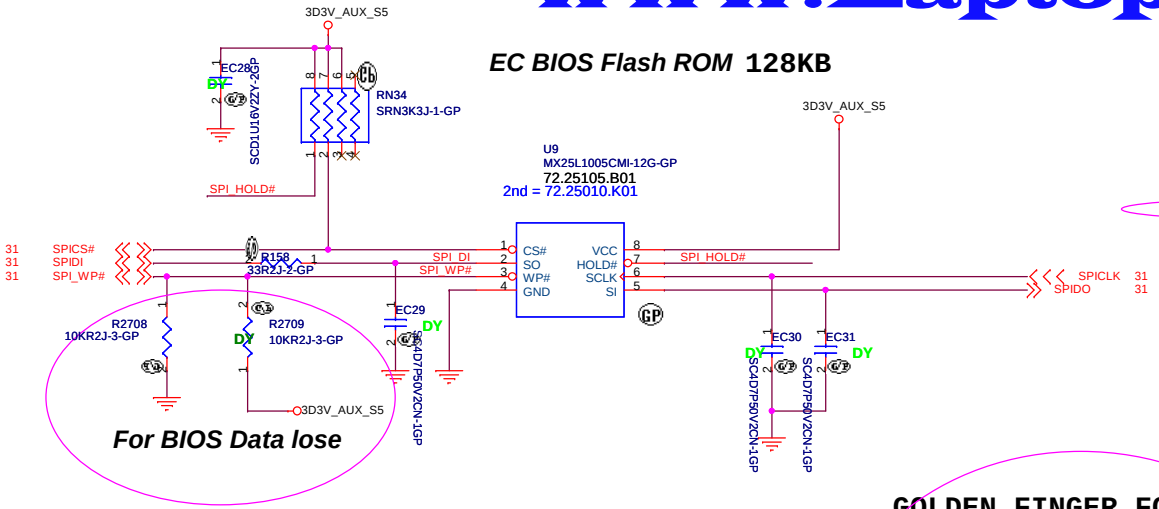
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

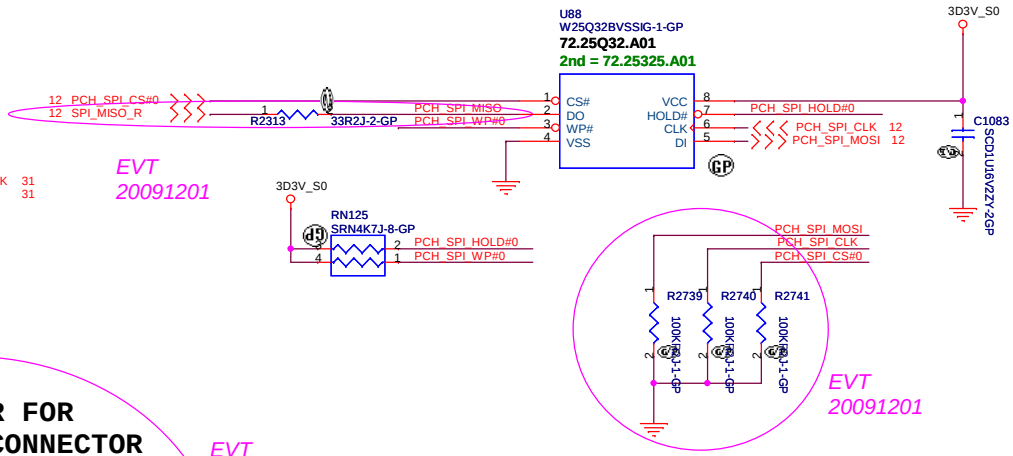
Title: Thermal/Fan Controllor
Size | Document Number: CADIZ-CP | Rev: -1M
Date: Saturday, April 24, 2010 Sheet 30 of 57



EC BIOS Flash ROM 128KB

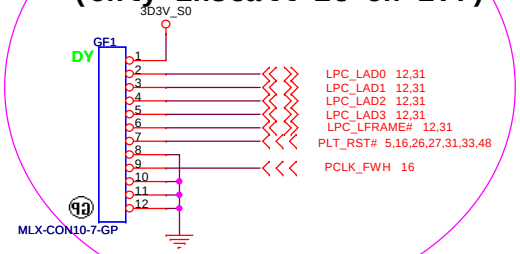


System BIOS Flash ROM (4MB)

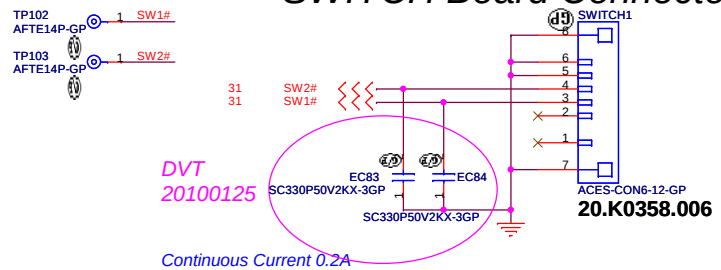


GOLDEN FINGER FOR DEBUG BOARD CONNECTOR (only install it on EVT)

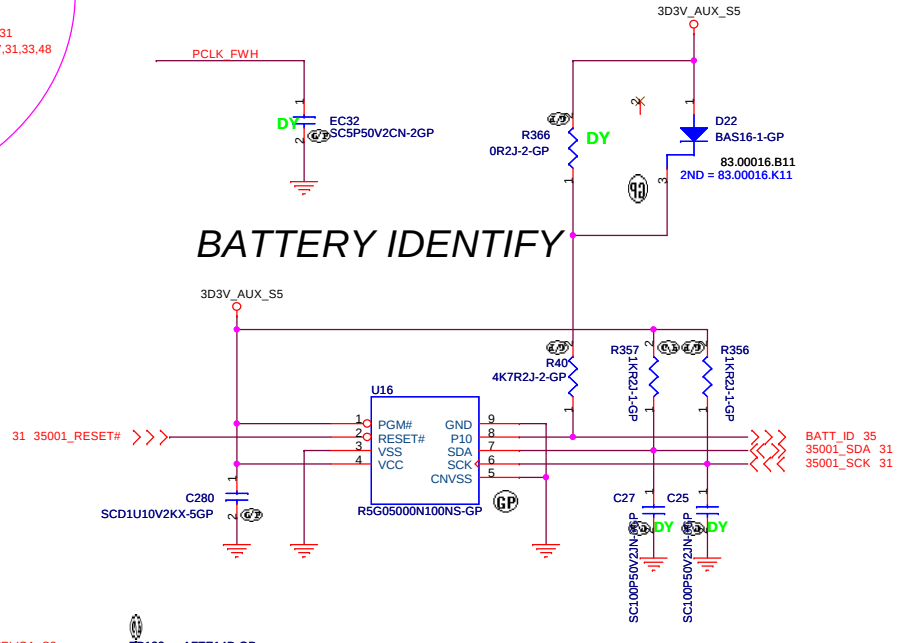
EVT 20091202



SWITCH Board Connector

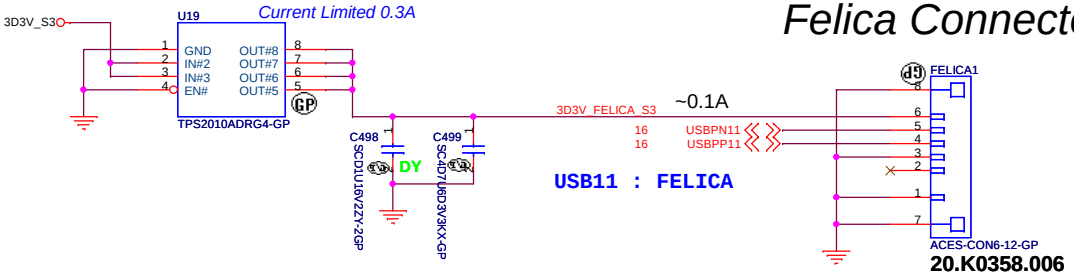


BATTERY IDENTIFY



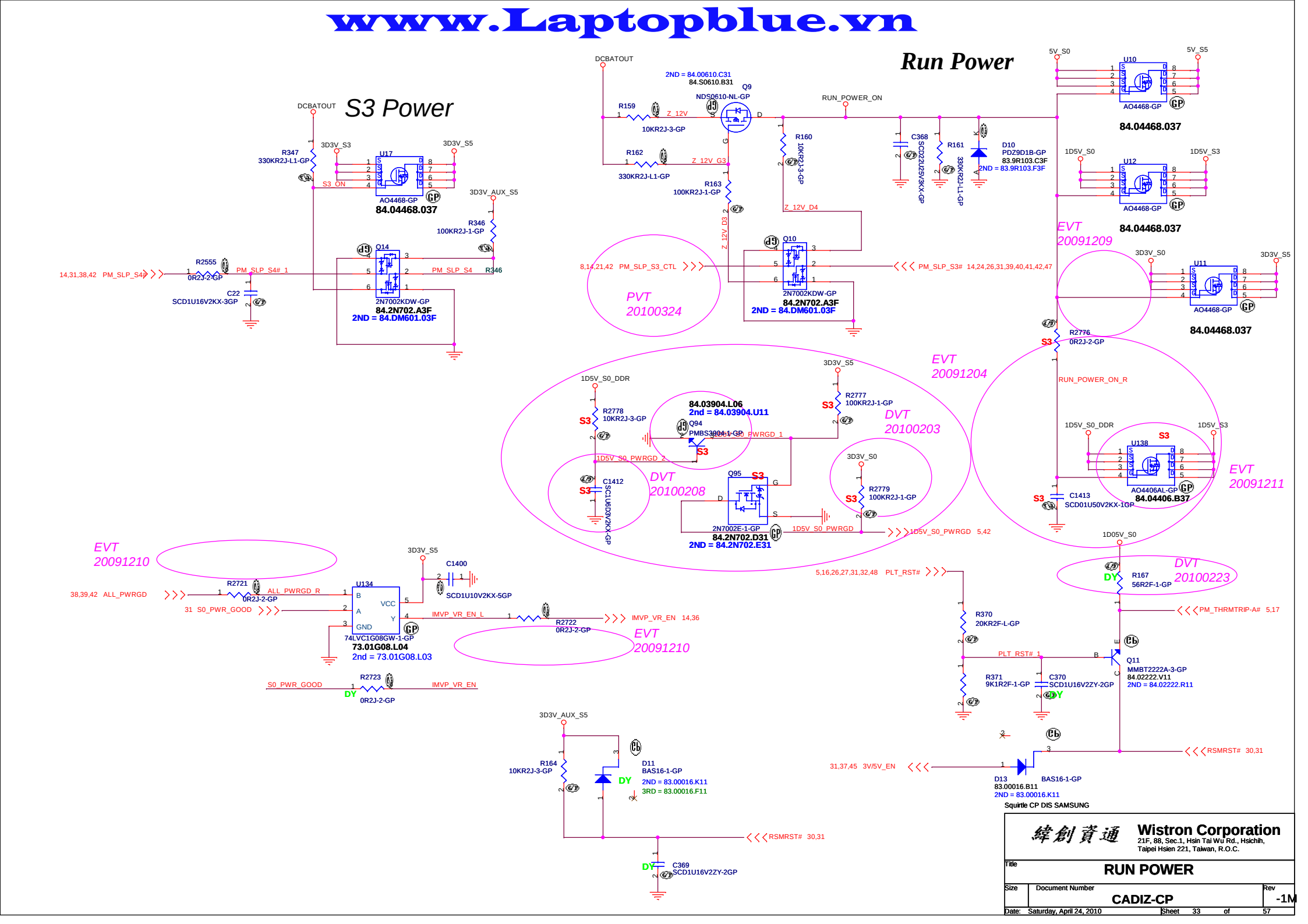
Continuous Current 0.2A
Current Limited 0.3A

Felica Connector



Squirtle CP DIS SAMSUNG

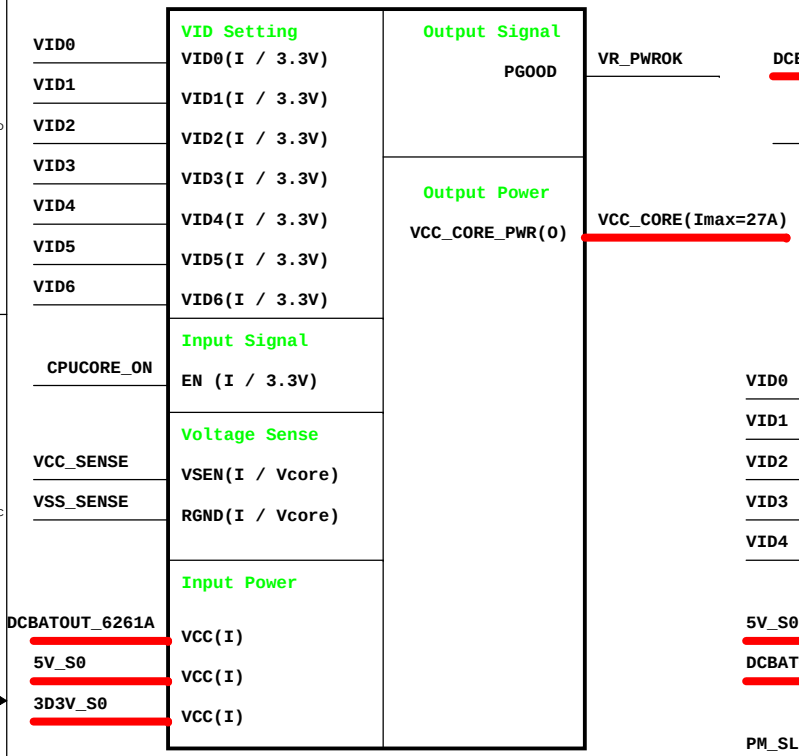
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BIOS & SW/C & BAT ID & Felica	
Size	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 32 of 57	



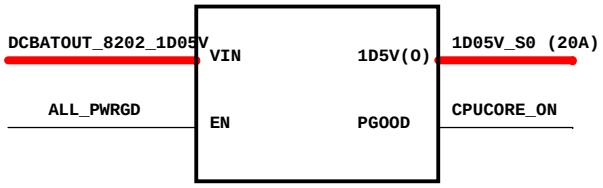
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER
Size	Document Number: CADIZ-CP
Rev	-1M
Date:	Saturday, April 24, 2010
Sheet	33 of 57

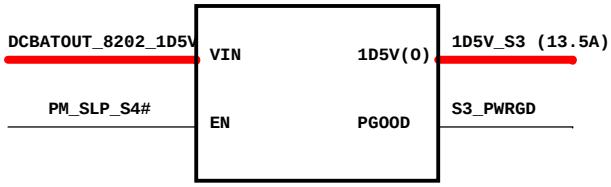
CPU_CORE
ADP3211



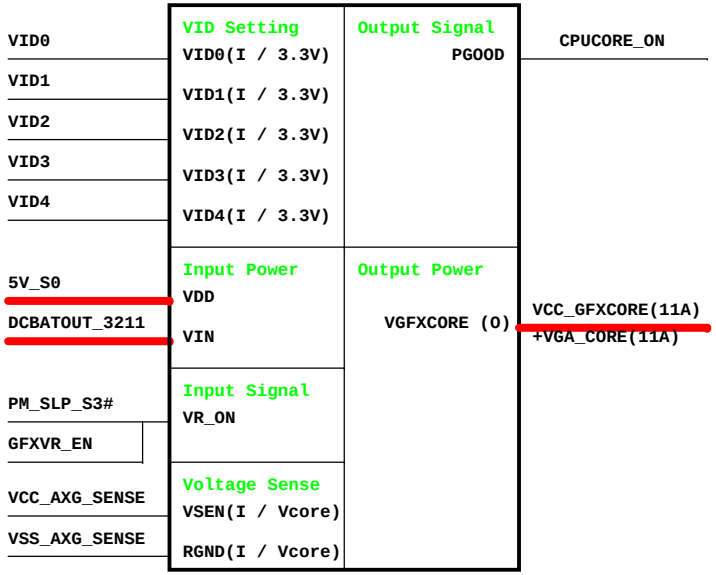
RT8209 1D05V_S0



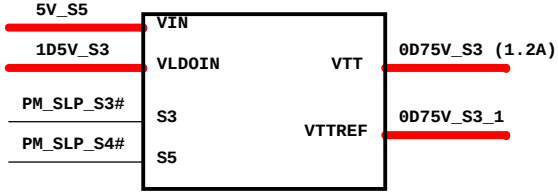
RT8209 1D5V_S3



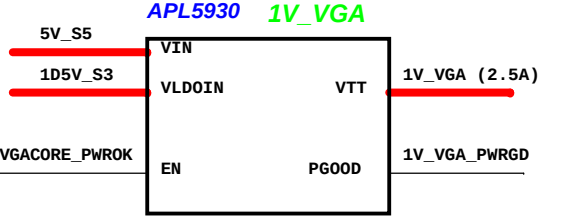
GFX_CORE/ VGA_CORE
ADP3211



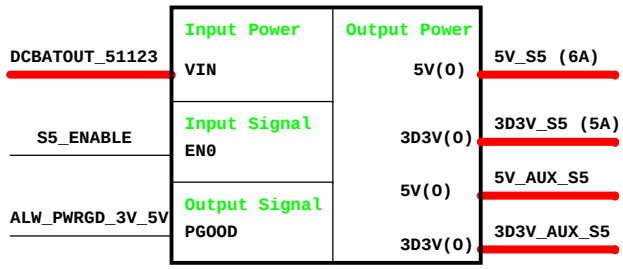
RT9026 0D75V_S0



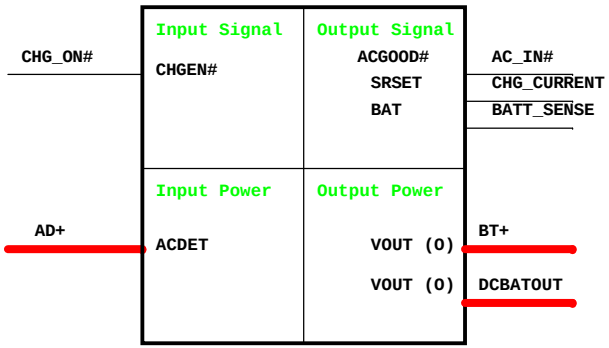
APL5930 1V_VGA



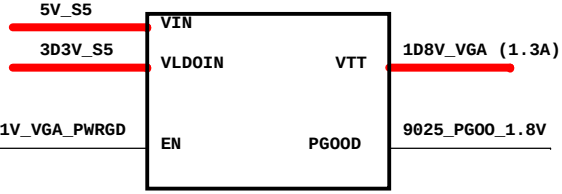
5V/3D3V
RT8223



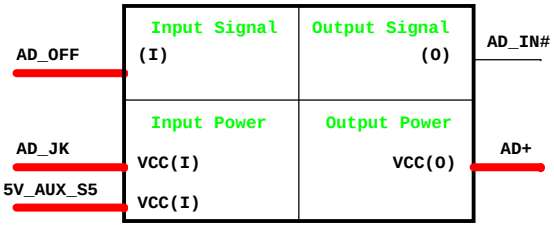
Charger BQ24751



G9661 1D8V_VGA



Adapter



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

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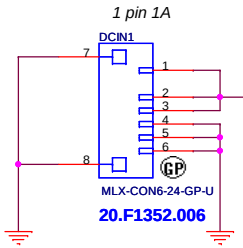
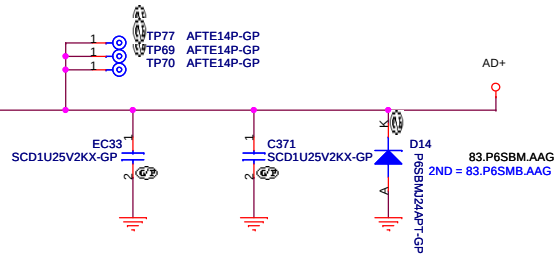
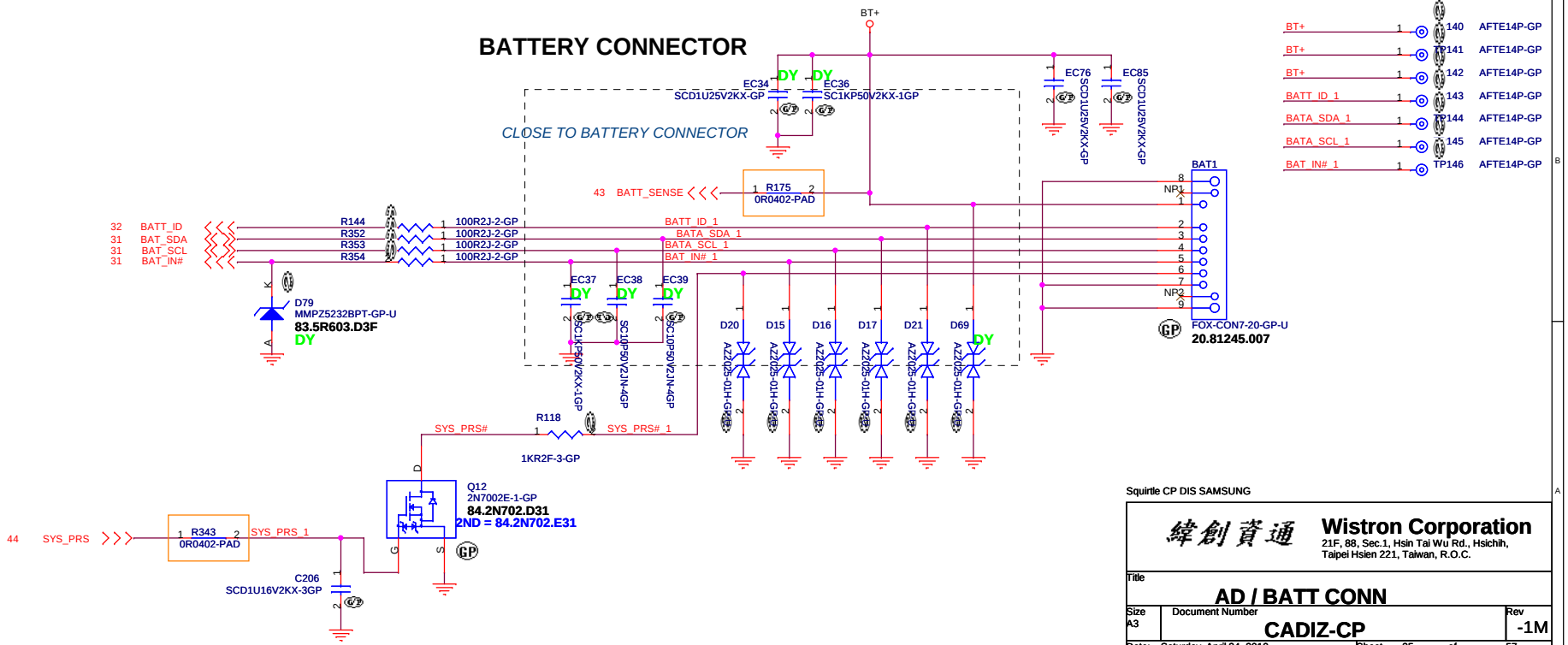
DC IN Connector



Adaptor in to generate DCBATOUT

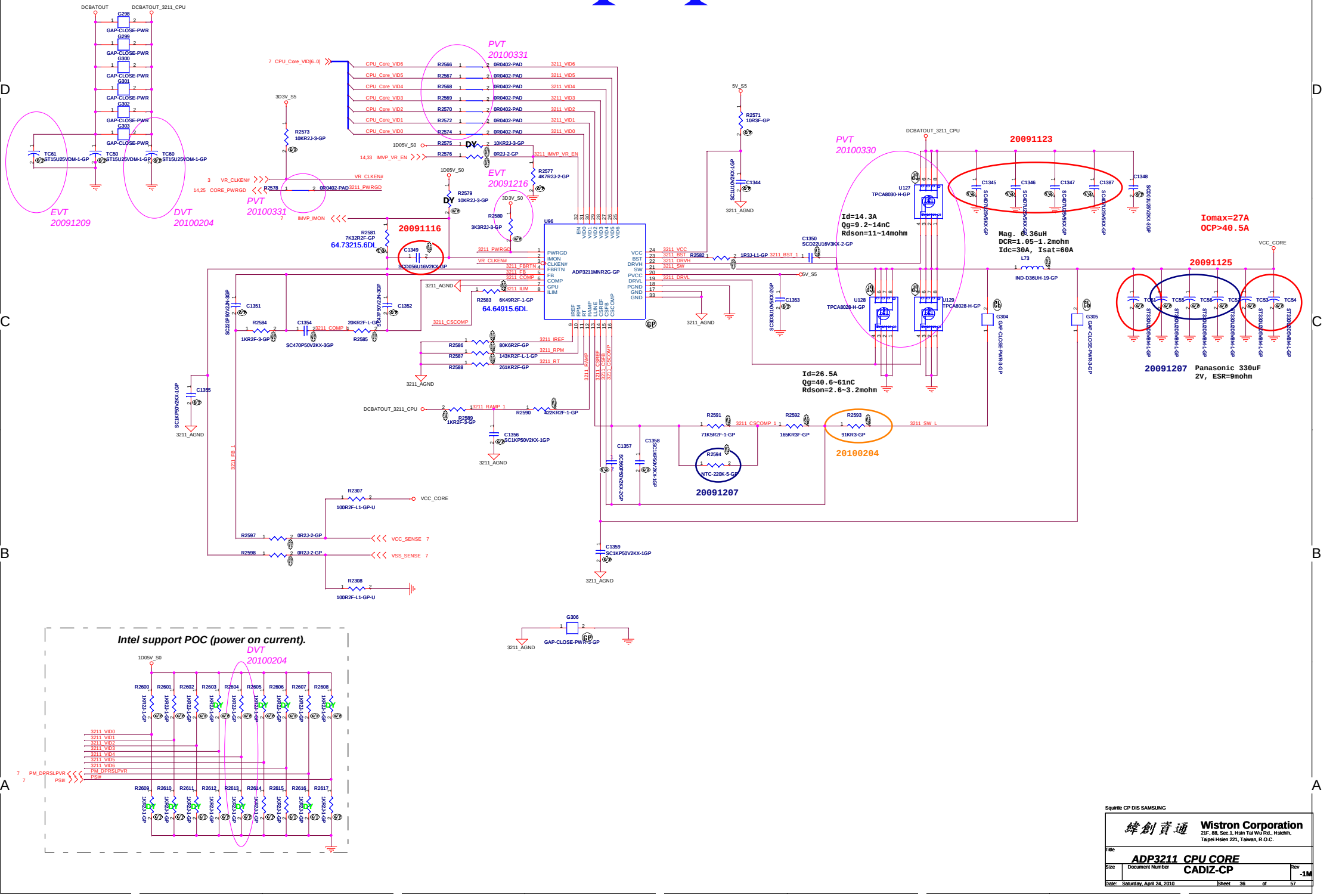


BATTERY CONNECTOR



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD / BATT CONN		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 35 of 57	



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU CORE

Size: CADIZ-CP | Document Number | Rev: -1M

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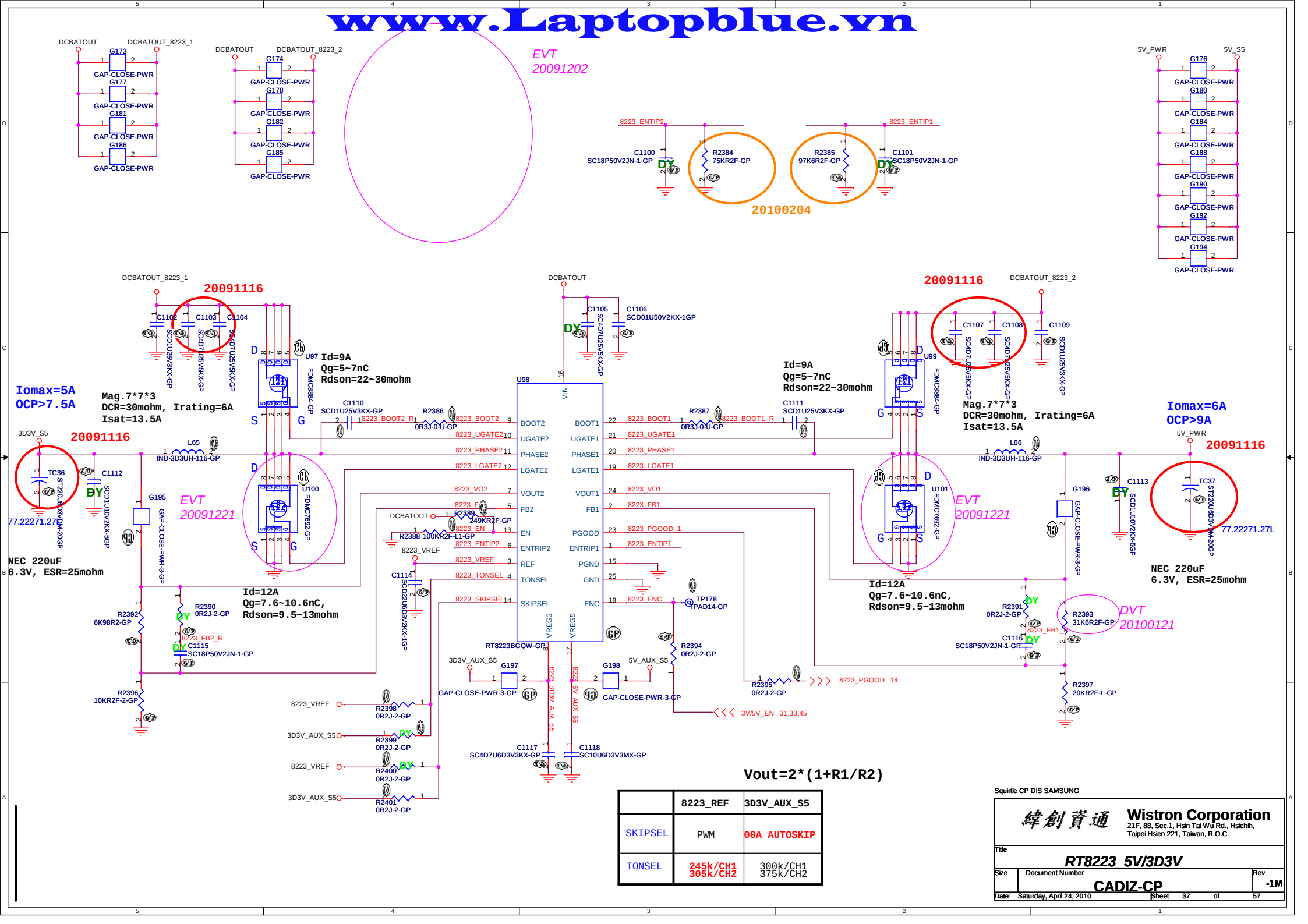

	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size	Document Number	Rev
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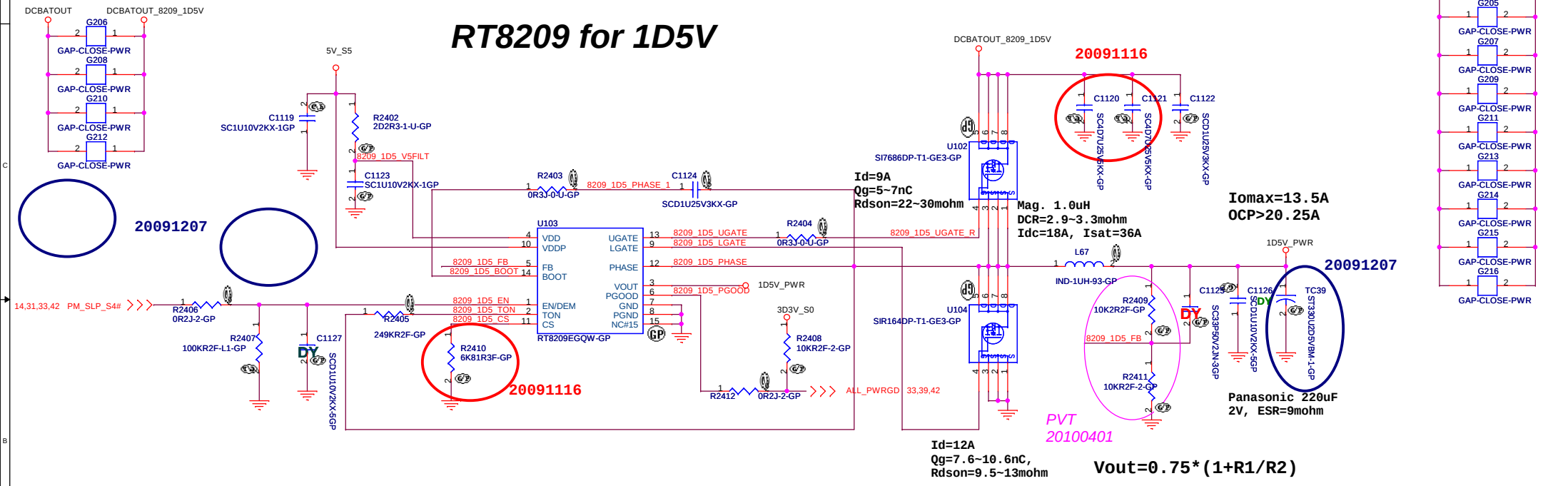
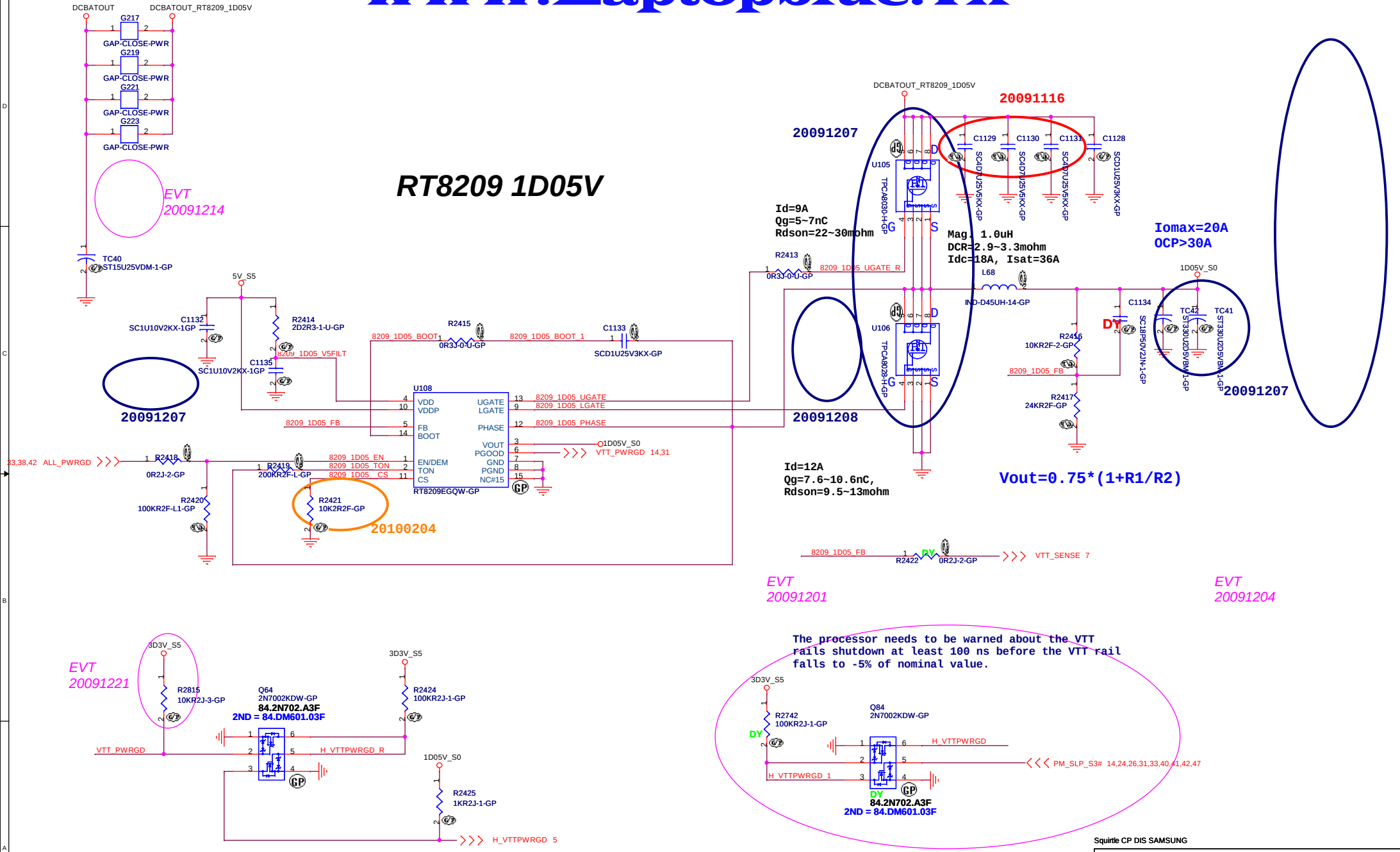
RT8209 for 1D5V



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209_1D5V		
Size	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 38 of 57	

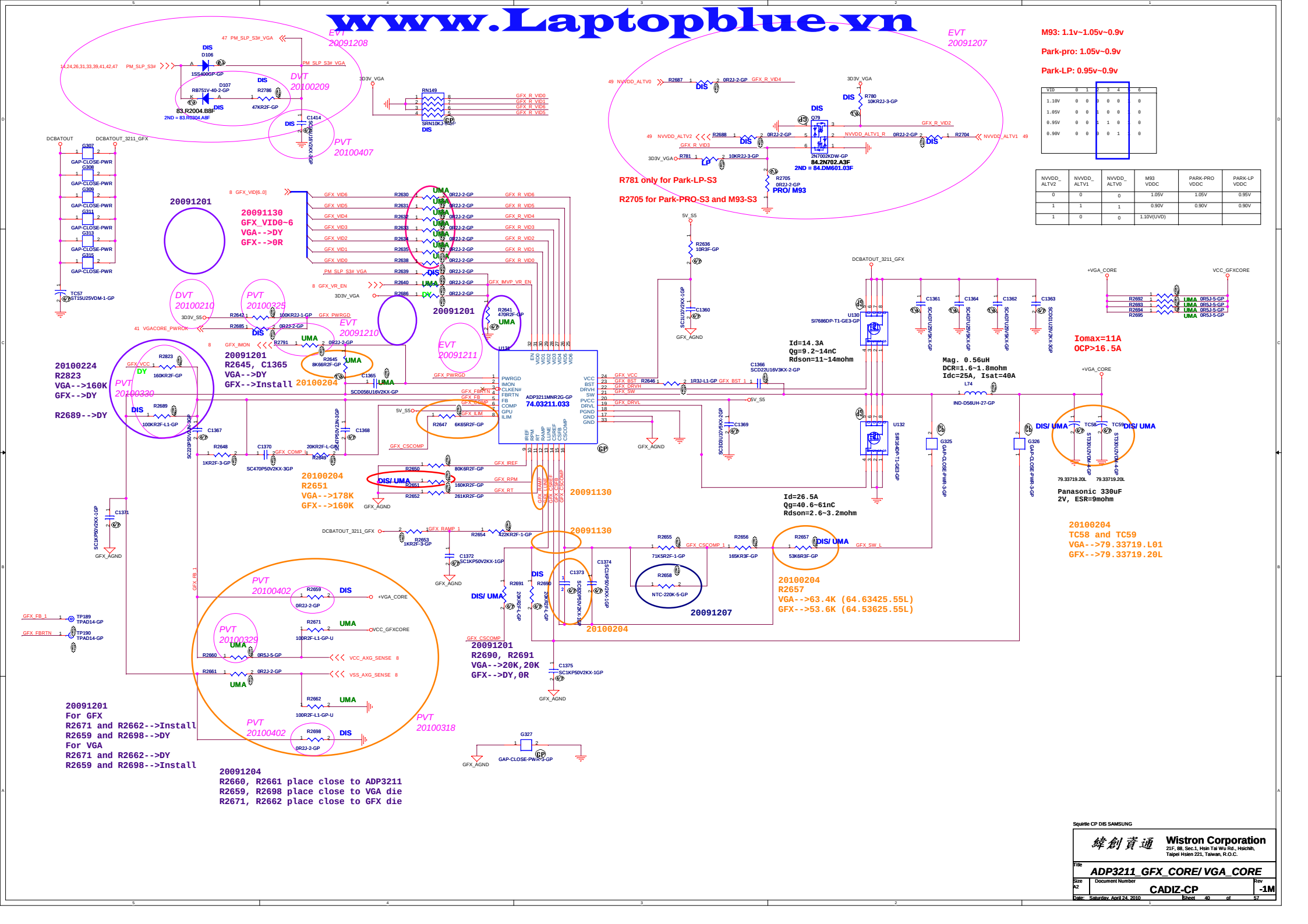
RT8209 1D05V



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209_1D05V		
Size	Document Number: CADIZ-CP		Rev: -1M
Date: Saturday, April 24, 2010	Sheet 39 of 57		



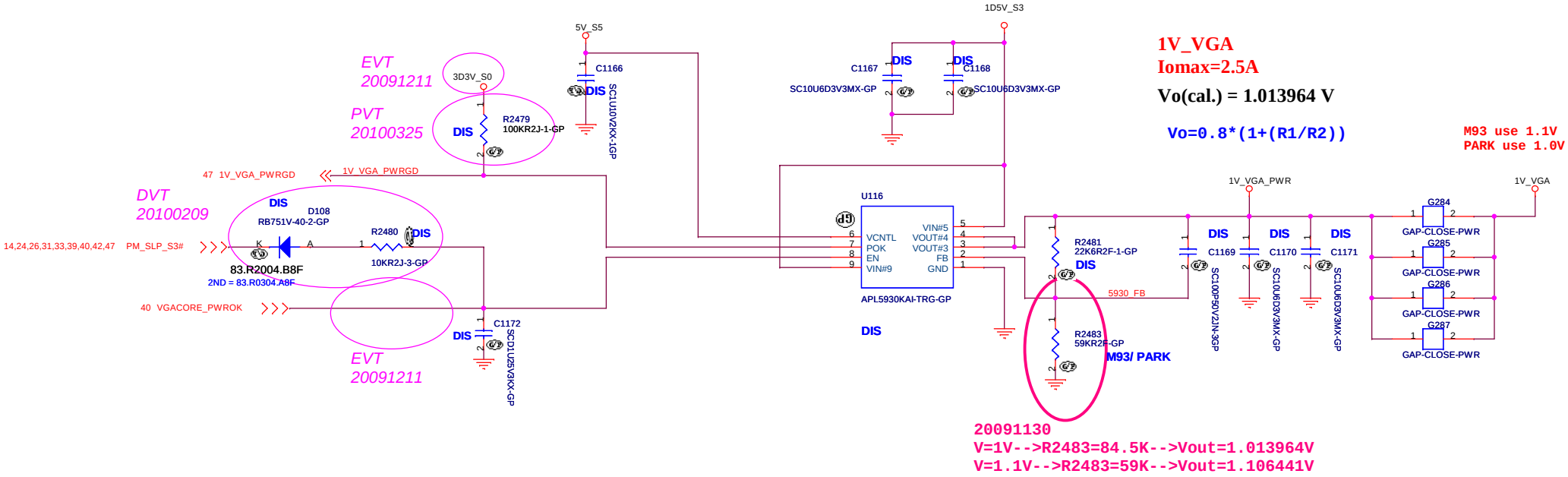
VID	0	1	2	3	4	5	6
1.10V	0	0	0	0	0	0	0
1.05V	0	0	0	1	0	0	0
0.95V	0	0	0	1	1	0	0
0.90V	0	0	0	0	0	1	0

NVVDD_ ALTV2	NVVDD_ ALTV1	NVVDD_ ALTV0	M93 VDDC	PARK-PRO VDDC	PARK-LP VDDC
0	0	0	1.05V	1.05V	0.95V
1	1	1	0.90V	0.90V	0.90V
1	0	0	1.10V(UVD)		

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADP3211_GFX_CORE/ VGA_CORE		
Size: A2	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 40 of 57	

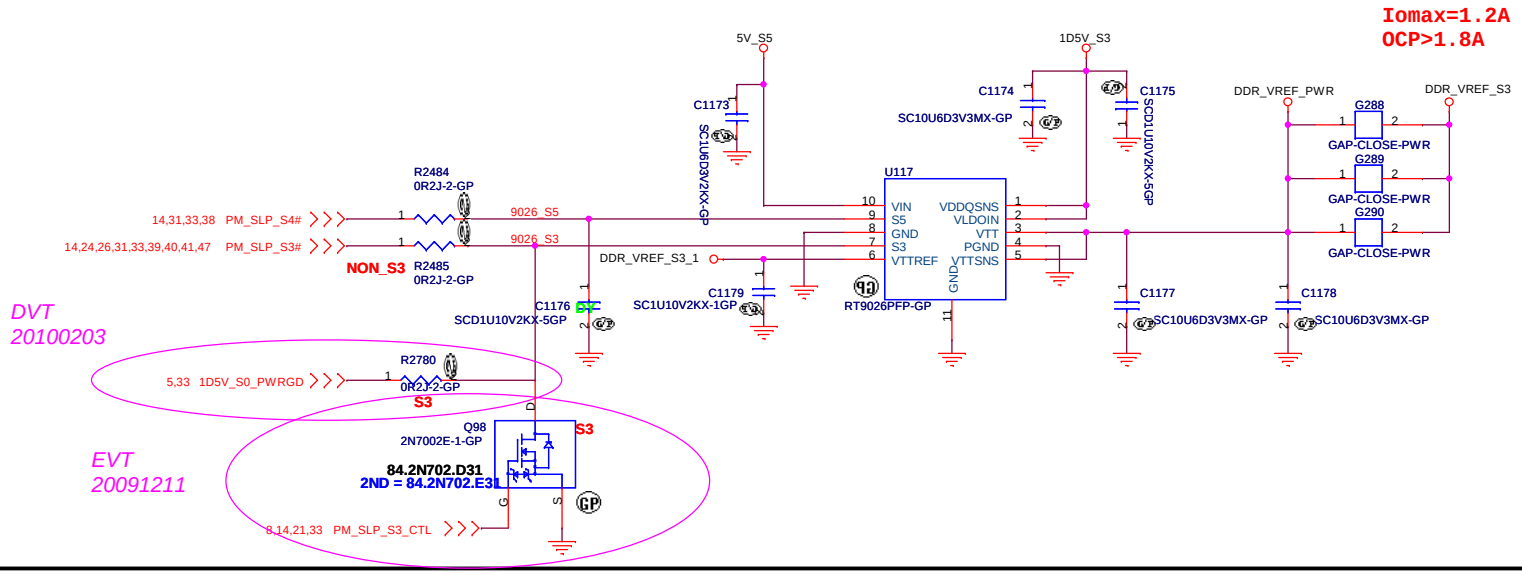
APL5930 for 1V_VGA



Squirtle CP DIS SAMSUNG

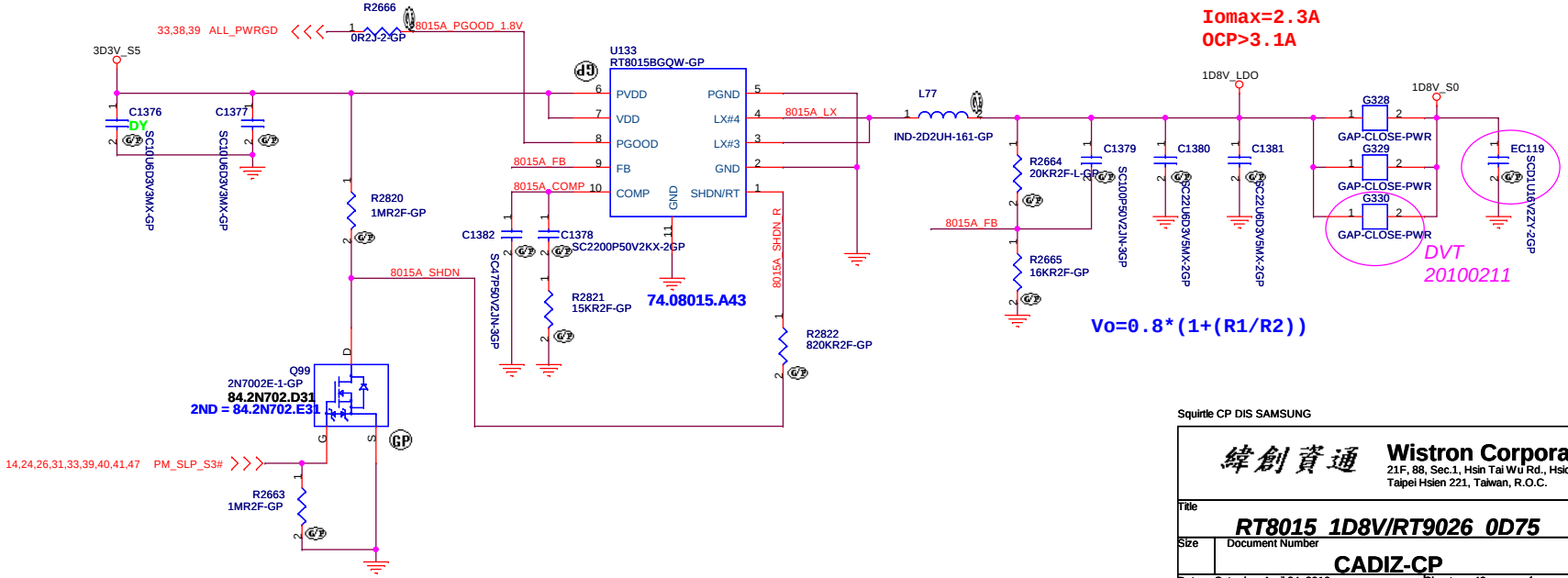
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ISL62881_+VCC_GFXCORE*		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 41 of 57	

RT9026 for 0D75V_S3



20100209

RT8015 for 1D8V_S0



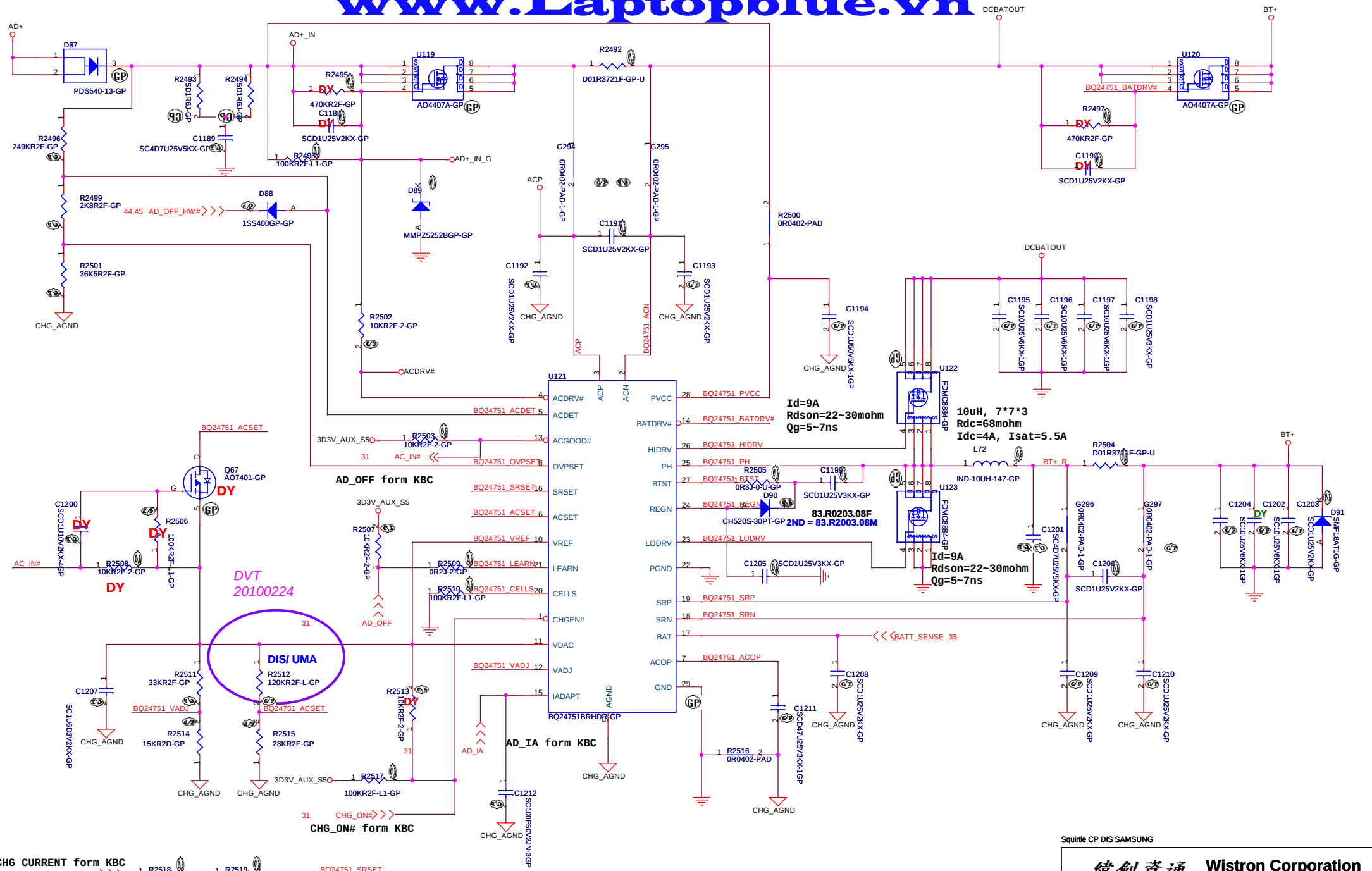
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8015_1D8V/RT9026_0D75

Size | Document Number: CADIZ-CP | Rev: -1M

Date: Saturday, April 24, 2010 | Sheet 42 of 57



Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BQ24751 Charger

Size	Document Number	Rev
A3	CADIZ-CP	-1M

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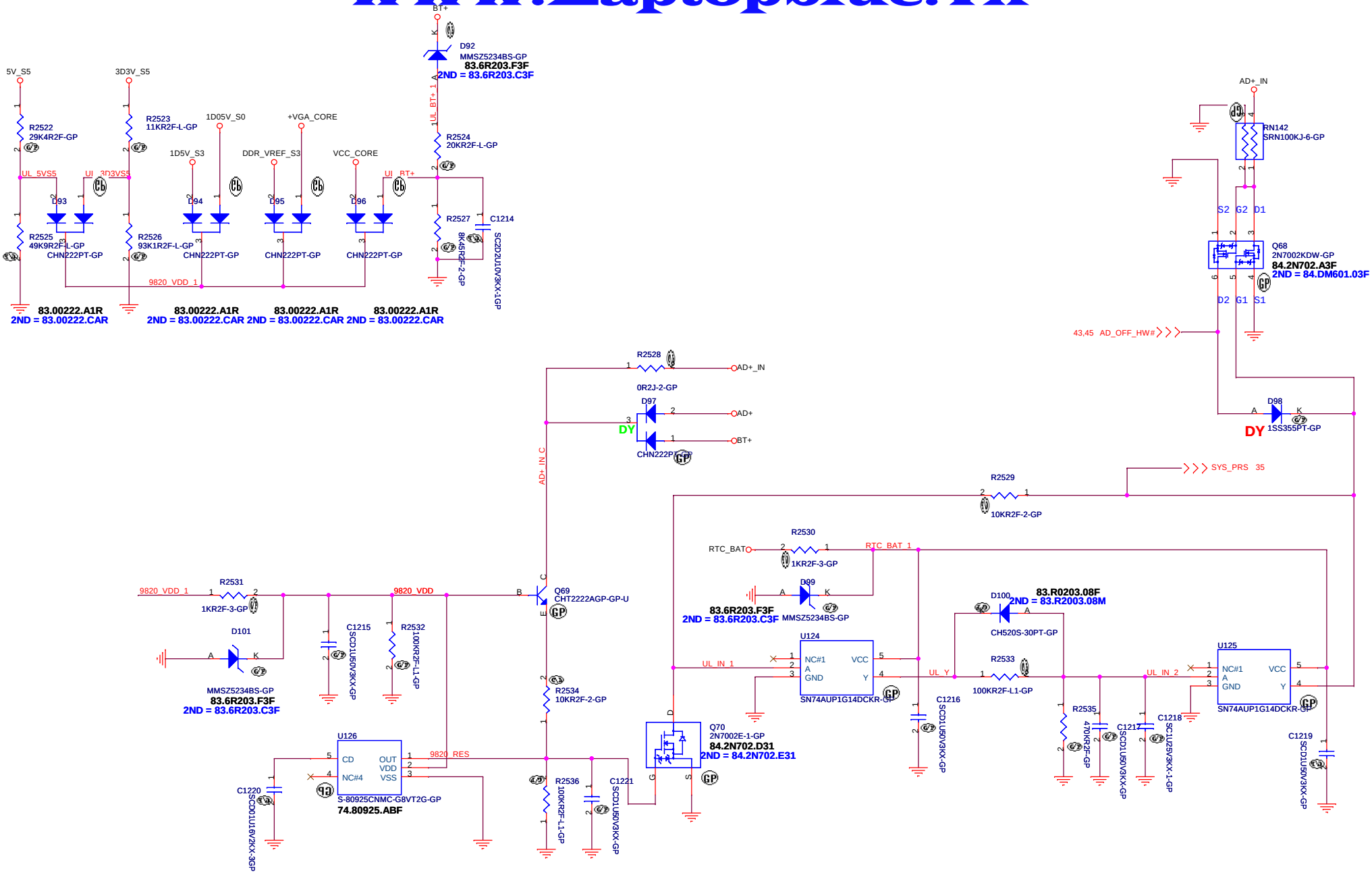
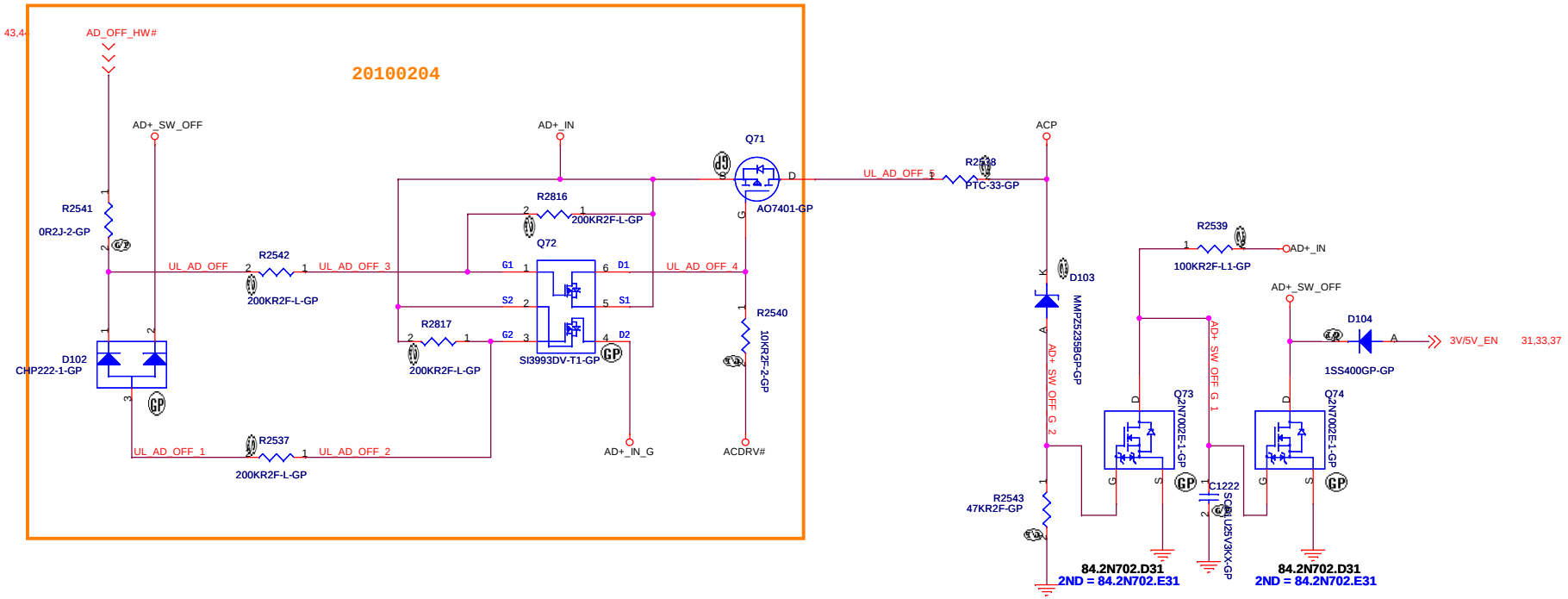


Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: UL circuit		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
Date: Saturday, April 24, 2010	Sheet 44 of 57	



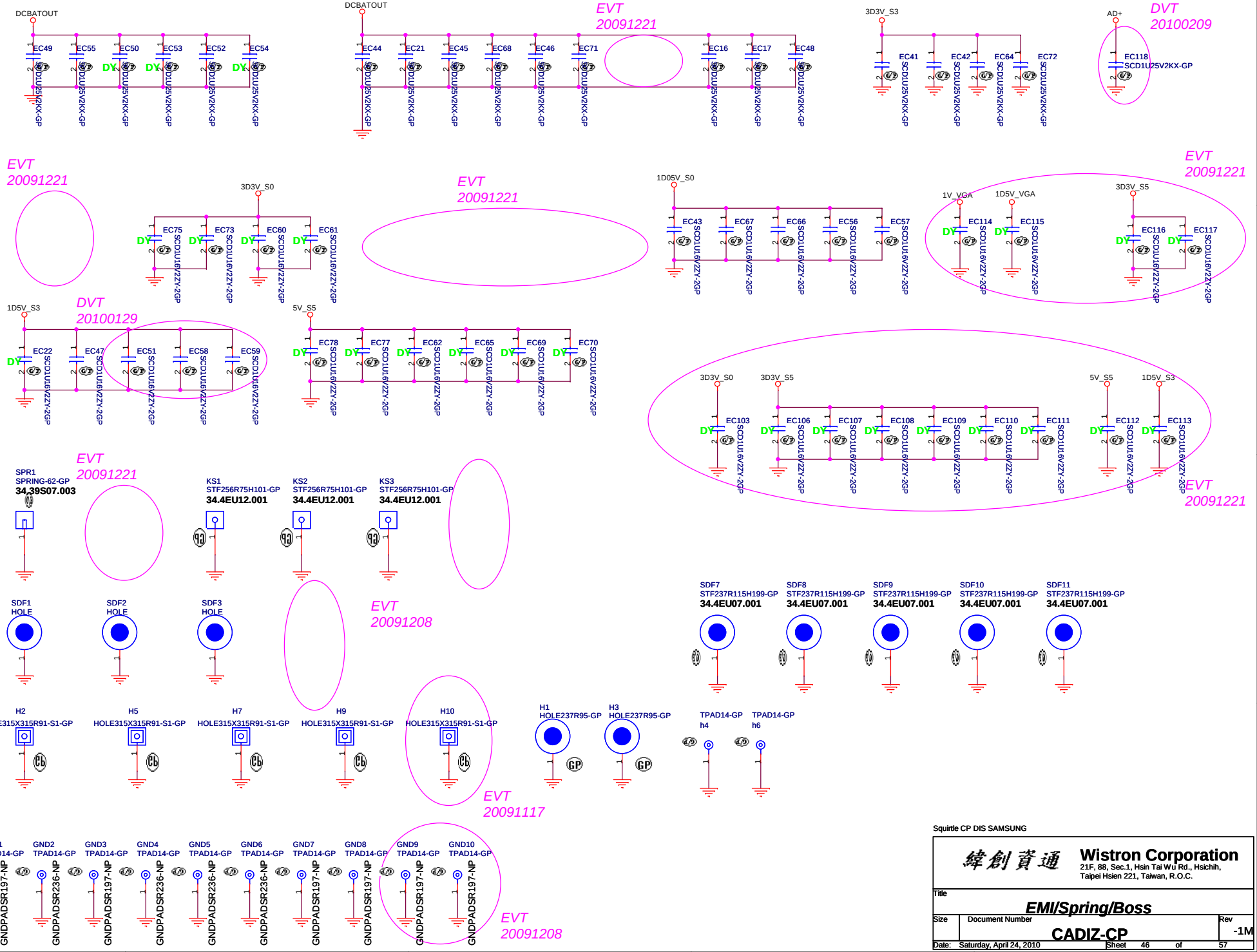
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UVP Protect

Size: A3 | Document Number: CADIZ-CP | Rev: -1M

Date: Saturday, April 24, 2010 | Sheet 45 of 57



Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
	CADIZ-CP	-1M

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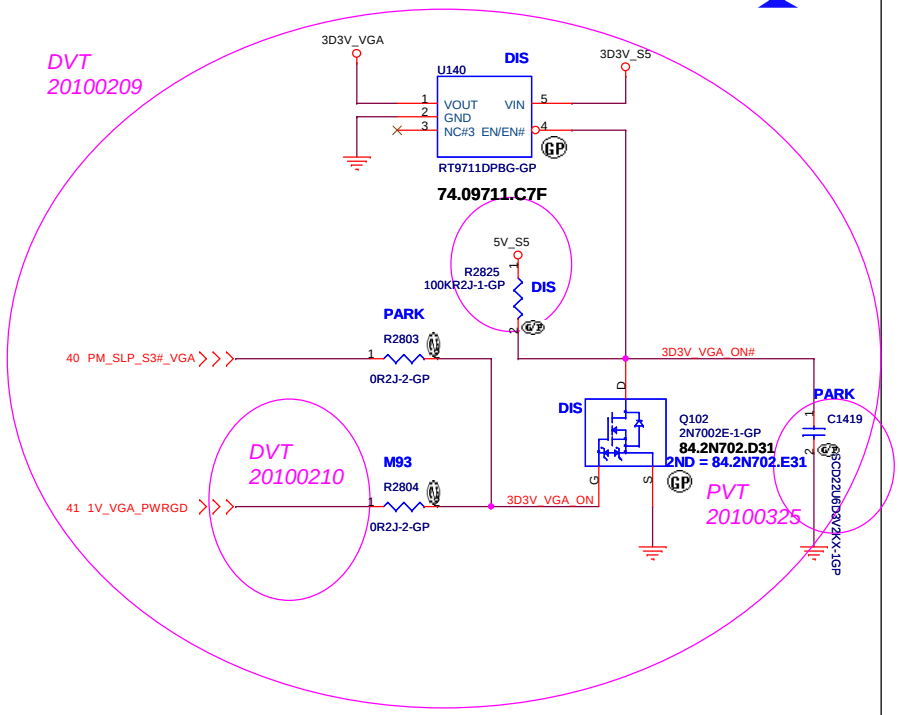

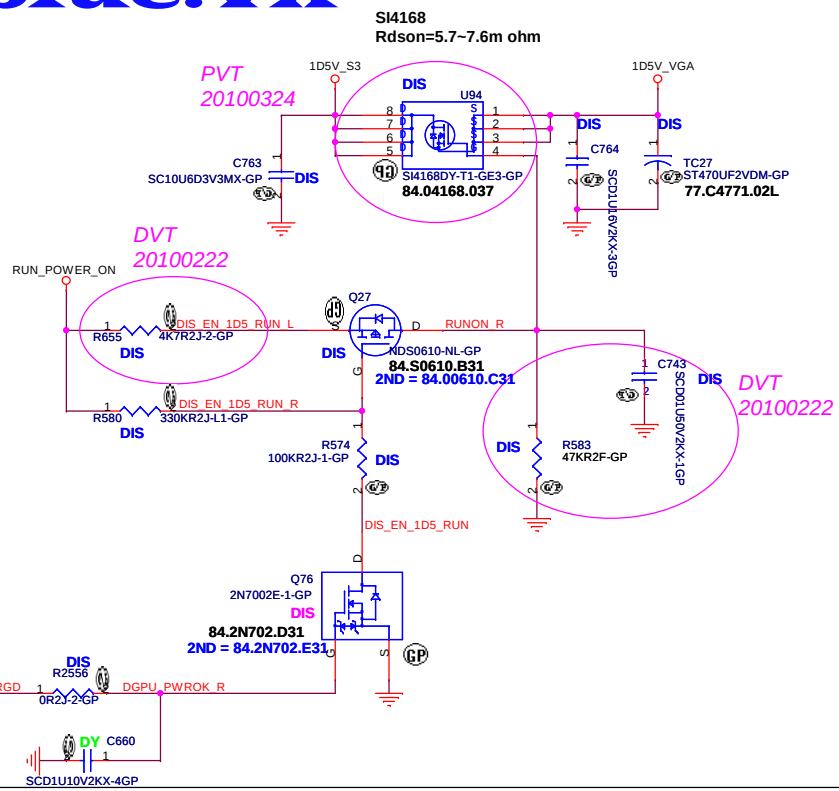

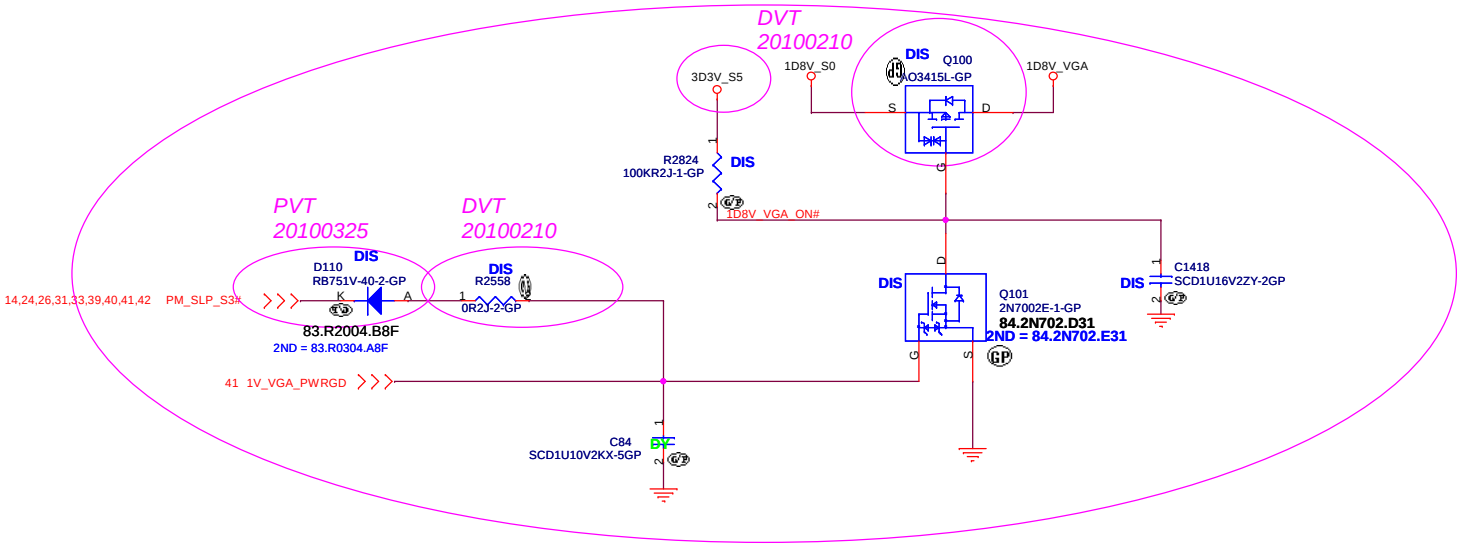

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

Size	Document Number	Rev
A3	CADIZ-CP	-1M

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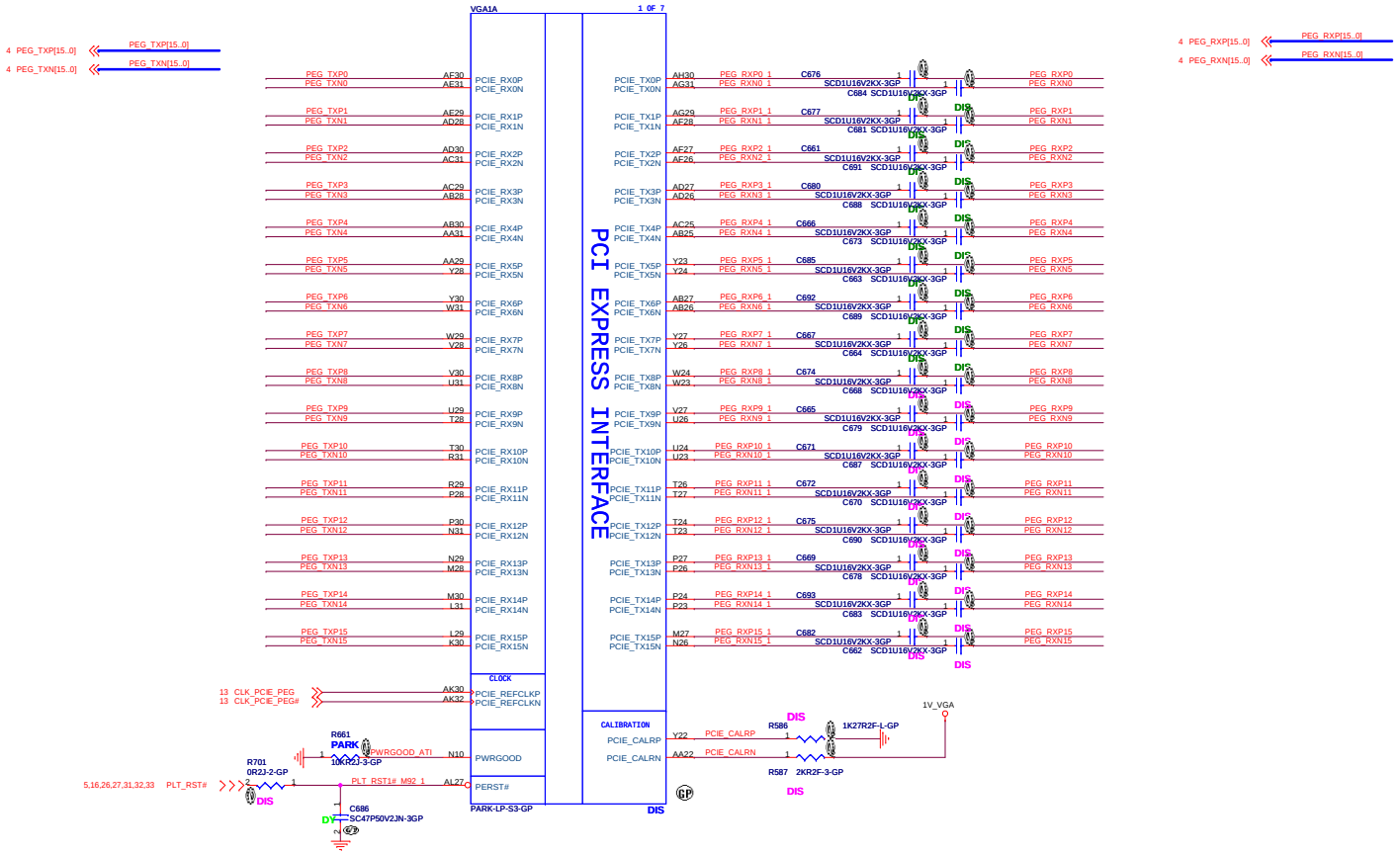

EVT
20091210

BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

Squintle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison PCIE**

Size	Document Number	Rev
A2	CADIZ-CP	-1M

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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5TQ1G63BFR-12C (800MHz)
1000 512MB Samsung-K4W1G1646E-HC12 (800MHz)

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

EVT 20091207
EVT 20091117
EVT 20091208
PVT 20100401

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison IO
Size: Custom | Document Number: CADIZ-CP | Rev: -1M
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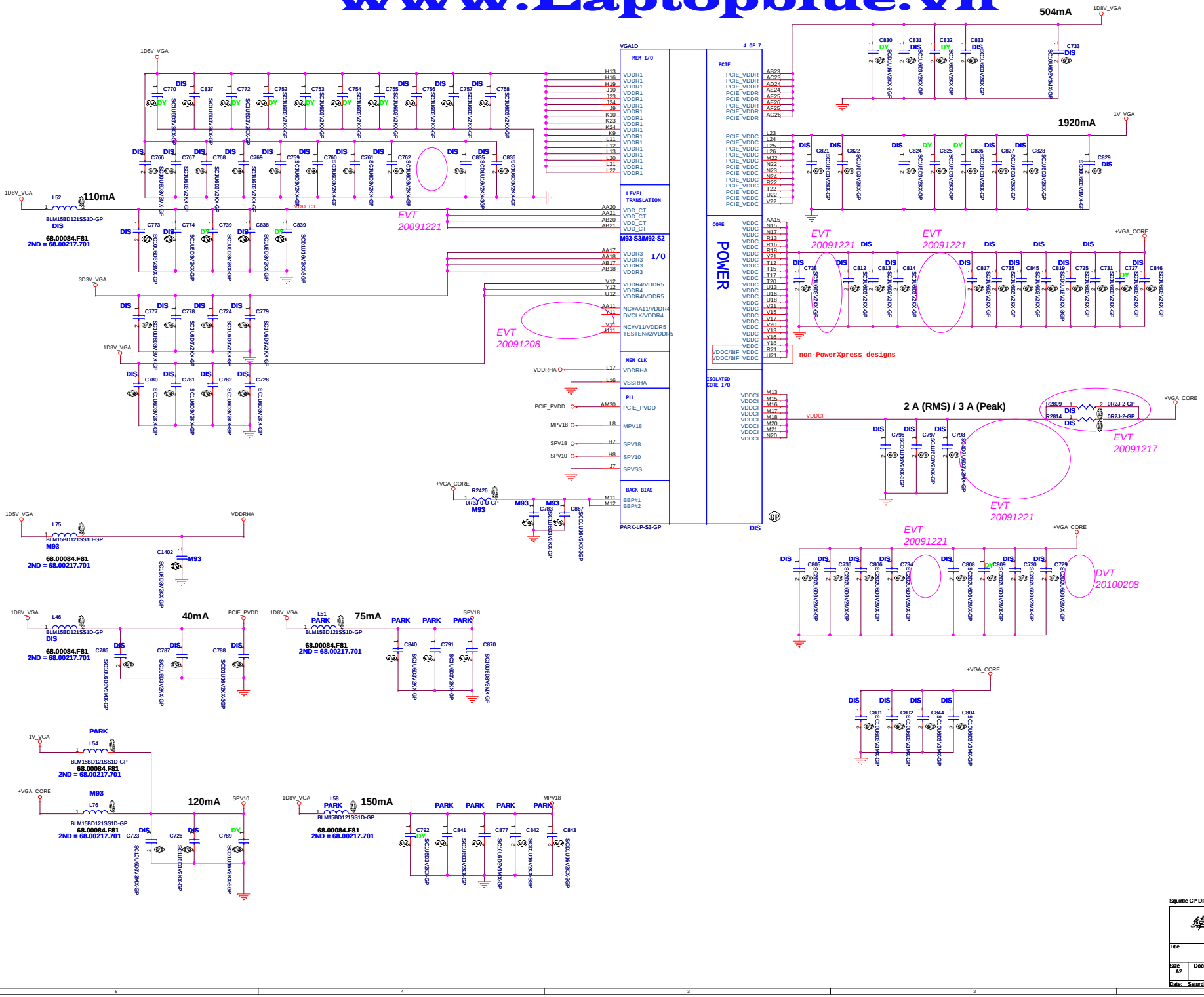


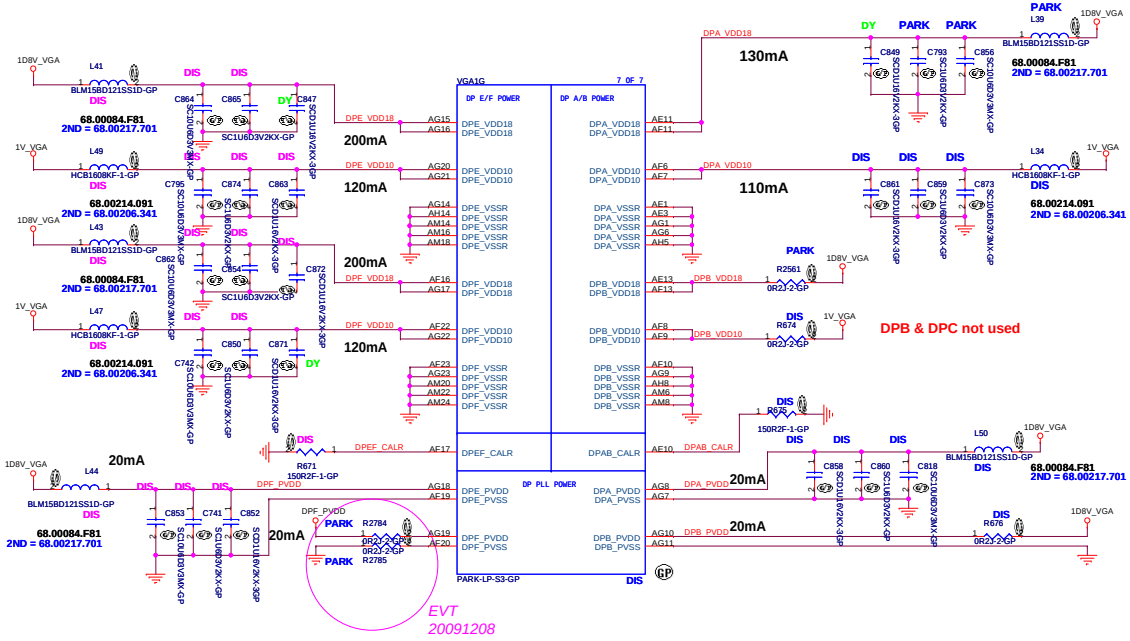
Squirtle CP DIS SAMSUNG

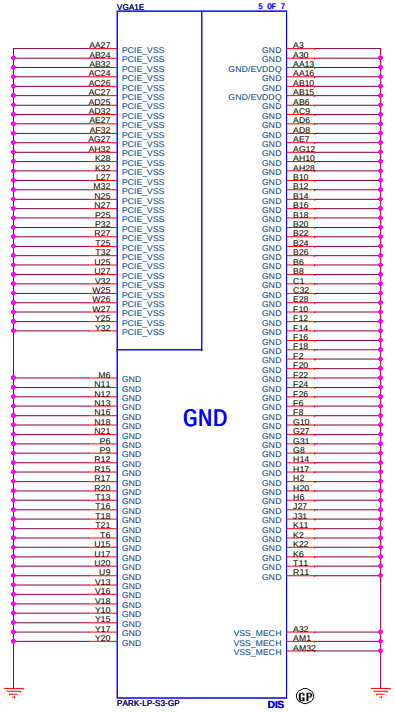
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison POWER

Size: A2 | Document Number: CADIZ-CP | Rev: -1M

Date: Saturday, April 24, 2010 | Sheet 50 of 57





Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DP POWER_GND		
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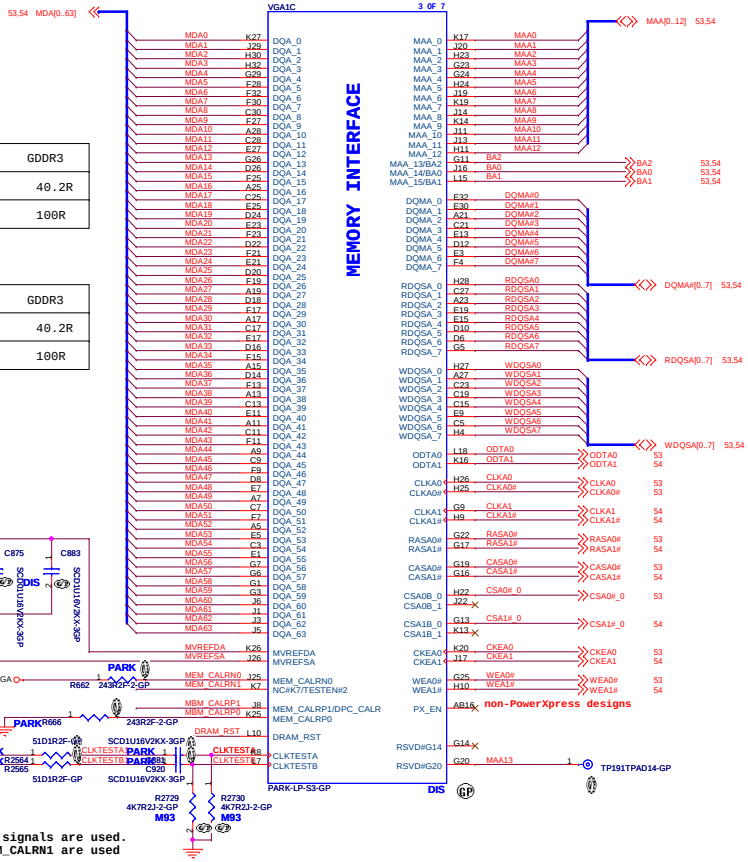
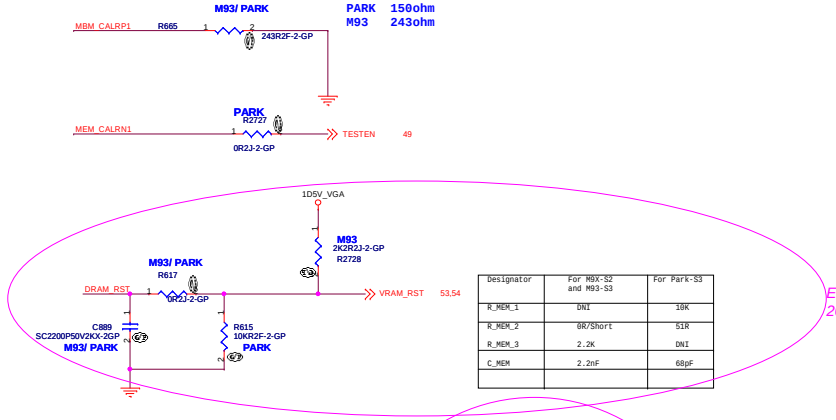
For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R





Designator	For M9X-S2 and M93-S3	For Park-S3
R_MEM_1	DNI	10K
R_MEM_2	0R/Short	51R
R_MEM_3	2.2K	DNI
C_MEM	2.2nF	68pF

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

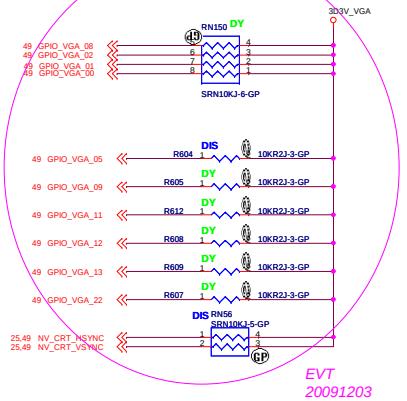
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	0
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Squirtle CP DIS SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

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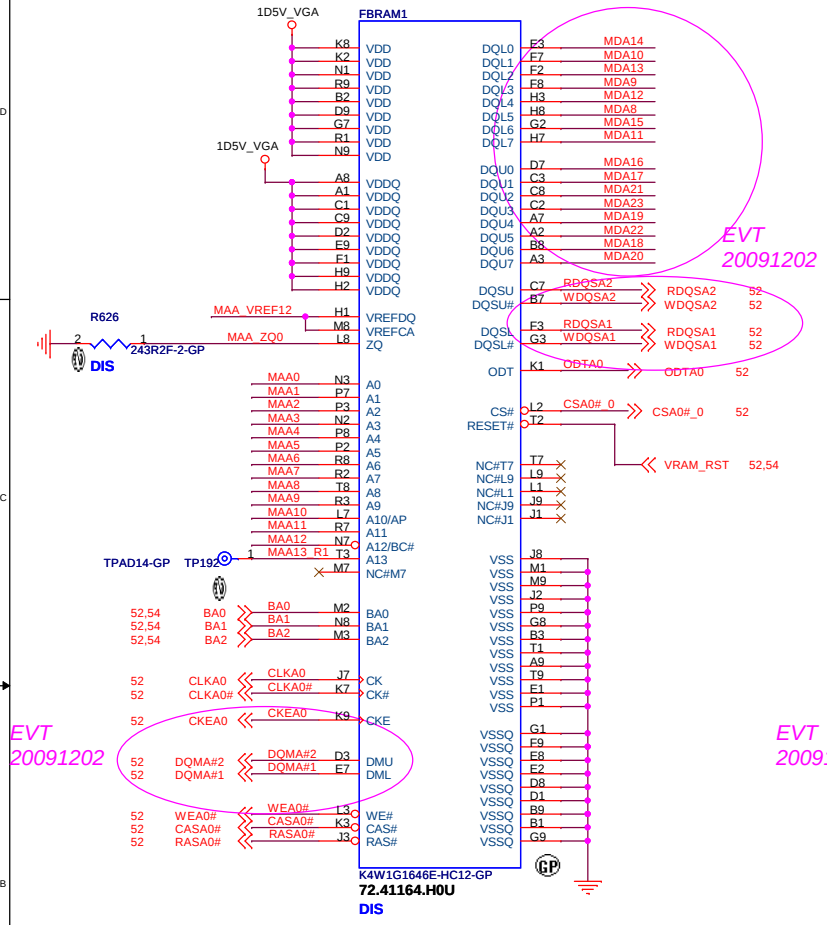
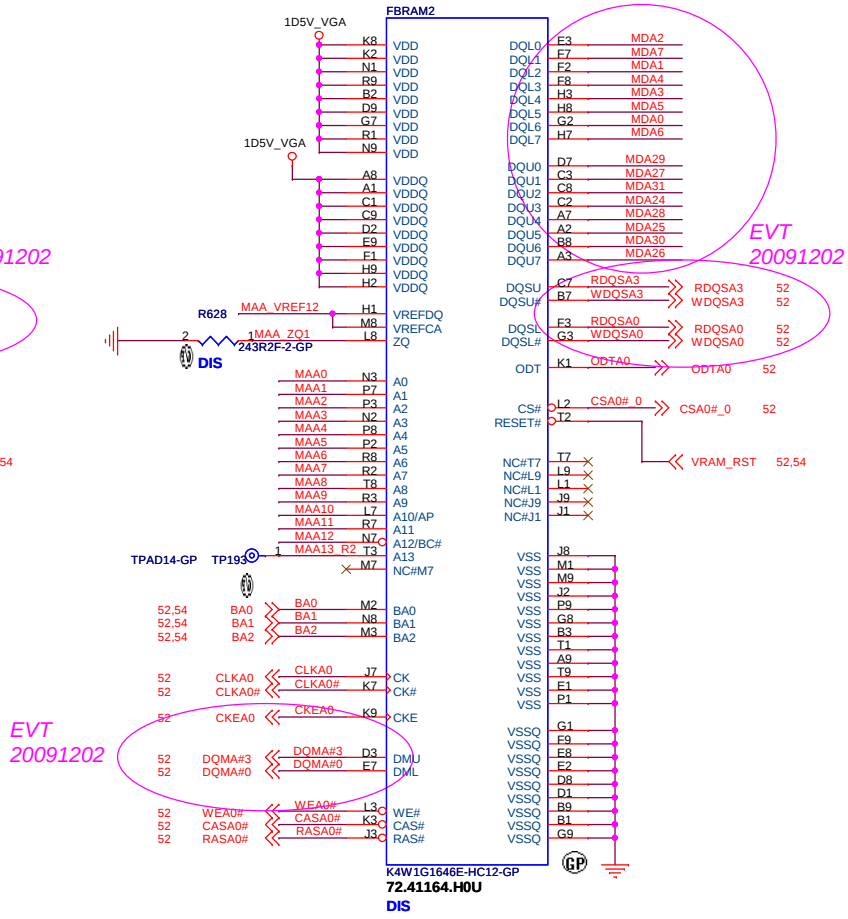
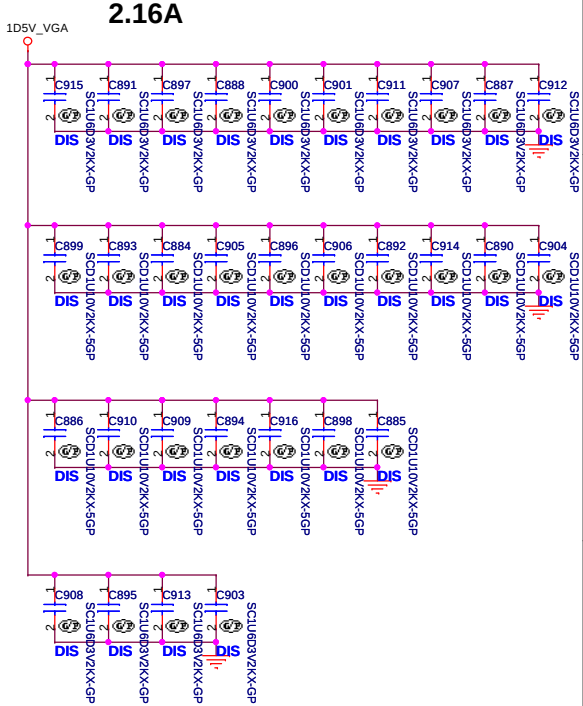
DDR3

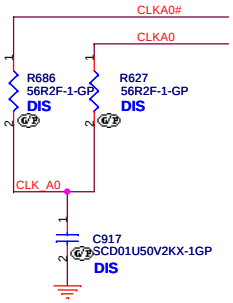


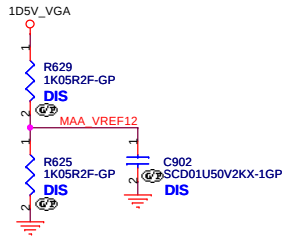




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

52,54 DQMA#[0..7]
52,54 RDQSA[0..7]
52,54 WDQSA[0..7]
52,54 MAA[0..12] MAA[0..12]
52,54 MDA[0..63] MDA[0..63]





Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(1/2)		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
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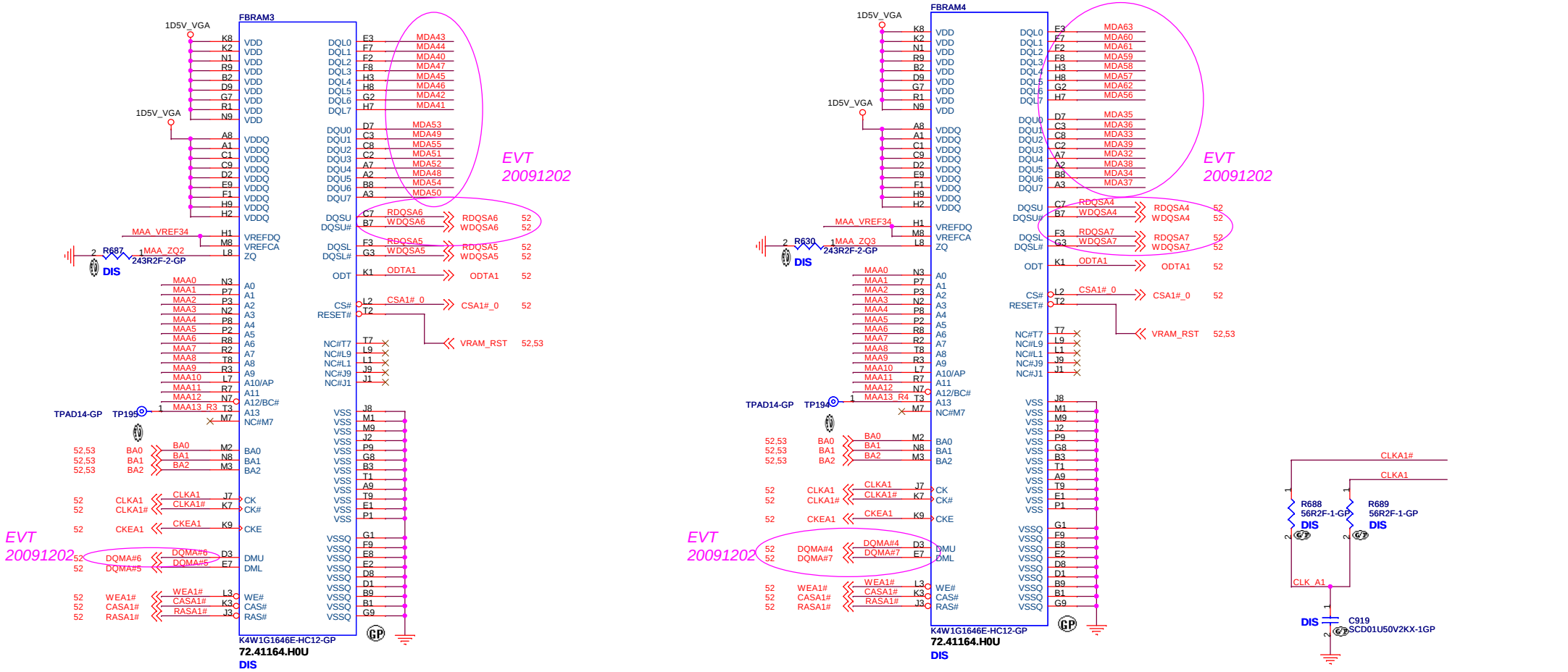
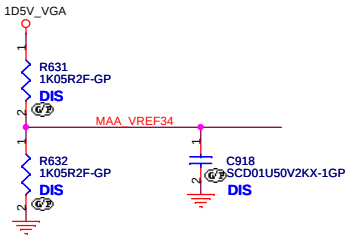
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

52,53 DQMA#[0..7]
52,53 RDQSA[0..7]
52,53 WDQSA[0..7]
52,53 MAA[0..12] MAA[0..12]
52,53 MDA[0..63] MDA[0..63]

Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/2)*		
Size: A3	Document Number: CADIZ-CP	Rev: -1M
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EVT

(2009/11/17)
P.8 [CPU SFF(5 of 8)-PWR/DDR/GFX] Delete R2263 (GFX_VR_EN double pull-low)
P.15 [PCH 4 of 9(LVDS/CRT/DP] Delete RN22 (CLK_DDC_EDID, DAT_DDC_EDID double pull-high)
P.15 [PCH 4 of 9(LVDS/CRT/DP] Modify RN112 and add RN147
P.15 [PCH 4 of 9(LVDS/CRT/DP] Change RN113 to three single resisters for PCH RGB signal.
P.23 [LCD CONN] Add R2621, R2625 100Kohm pull-low for BLON_IN and BLON_OUT_R
P.25 [CRT BD CONN] Add RN146 pull-high to 3D3V_S0 for CRT_DDCCLK1 and CRT_DDCDATA1
P.47 [EMI/Spring/Boss] ME add stand off KS1~KS4 and H10
P.50 [PARK-S3 IO] Change RN86 to three single resisters for VGA RGB signal.

(2009/11/20)
P.13 PCH (2 of 9)-PCIE/CLK/SMB Modify PCI express ports connection assigned table
P.16 PCH (5 of 9)-PCI/USB Modify USB ports connection assigned table
P.27 MINI BD CONN Add USB port for MINI1 WIMAX function

(2009/11/23)
P.25 [CRT BD CONN] Delete RN126~RN129

(2009/11/25)
P.24 [HDD CONN & TOUCHPAD] Add HDD protection circuit
P.27 MINI BD CONN Modify WIMAX USB pair connection
P.25 [CRT BD CONN] Change HDMI 0.1UF caps to BTBCRT1 side..

(2009/11/27)
P.32 [BIOS & SW/C & BAT ID & Felic] Add 10Kohm pull low for SPI_WP#

(2009/11/30)
P.27 MINI BD CONN Modify 5V_MINI_S5, 3d3v_s3 and USB8 net arrangement
P.3 Clock Generator Add damping resistor for the 14MHz crystal
P.12 PCH (1 of 9)-SATA/RTC/HDA Add damping resistor for the 32KHz crystal

(2009/12/01)
P.13 PCH (2 of 9)-PCIE/CLK/SMB Modify PCI express clock connection assigned table
P.40 ADP3211_GFX_CORE/ VGA_CORE Modify VGA/ GFX co-lay power circuit
P.30 Thermal/Fan Controllor Modify thermal contral circuit.
P.32 [BIOS & SW/C & BAT ID & Felic] Modify net name SPI_MOSO_R to SPI_MISO_R
P.32 [BIOS & SW/C & BAT ID & Felic] Add 100K ohms pull-down resistors on each SPI0_CLK, SPI0_MOSI and SPI0_CS# net.
P.12 PCH (1 of 9)-SATA/RTC/HDA Add damping resistor for LPC_LAD0~LPC_LAD3 and LPC_LFRAME#
P.7 CPU SFF(4 of 8)-POWER/VTT Delete VCORE SENSE pin double pull high/low resistors.
P.39 RT8209_1D05V Add sequence circuit for VTTPWRGOOD and VTT.

(2009/12/02)
P.29 AUDIO JACK Add speaker protection circuit.
P.32 [BIOS & SW/C & BAT ID & Felic] Add golden finger debug connector GF1 and only install it on EVT
P.37 [RT8223_5V/3D3V] Delete 3D3V_PWR 7pcs gaps for more place.
P.12 PCH (1 of 9)-SATA/RTC/HDA Add test point for JTAG.
P.25 [CRT BD CONN] Change HDMI_CLK, HDMI_DATA, CRT_DDCCLK1, CRT_DDCDATA1 pull high resistors to 3.83Kohm.
P.53 [VRAM(1/2)] Swap VRAM DQ, DQS, DM net.
P.54 [VRAM(3/4)] Swap VRAM DQ, DQS, DM net.

(2009/12/03)
P.13 PCH (2 of 9)-PCIE/CLK/SMB Change PCIE_CLK_RQ2# to pull low for cardreader.
P.23 [LCD CONN] Change descrete brightness source from EC to VGA.
P.52 [M93/ PARK-S3 Memory / Straps] Modify GPIO setting

(2009/12/04)
P.40 ADP3211_GFX_CORE/ VGA_CORE Modify sense pin circuit.
P.28 Audio Codec ALC275 Modify speaker protection circuit.
P.29 AUDIO JACK Modify speaker protection circuit.
P.39 RT8209_1D05V Delete 1D05V output gaps.
P.42 G9661_1D8V/ RT9026_0D75 Add S3 Power Reduction schematics.
P.5 CPU SFF(2 of 8)-CLK/Thermal Add S3 Power Reduction schematics.
P.17 PCH (6 of 9)-GPIO/RSVD Add S3 Power Reduction schematics.
P.33 RUN POWER Add S3 Power Reduction schematics.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX Add S3 Power Reduction schematics.
P.21 DDR3-SOCKET_1 Add S3 Power Reduction schematics.
P.14 PCH (3 of 9)-DMI/FDI Add S3 Power Reduction schematics.

(2009/12/07)
P.31 KBC_NPCE781L / KB Modify W_Disable# direction to output from EC
P.27 MINI BD CONN Modify W_Disable# direction to output from EC
P.13 PCH (2 of 9)-PCIE/CLK/SMB Delete RN102 and omit the routing prom PCH to CPU
P.5 CPU SFF(2 of 8)-CLK/Thermal alway install RN89 for UMA and DIS.
P.27 MINI BD CONN Modify power source 6 pins of 3D3V_S3 to 3D3V_S5 for WWAN power off sequence by software request.
P.36 ADP3211_CPU CORE Power team update circuit and add EL CAP at DCBATOUT for acoustic noise.
P.38 RT8209_1D5V Power team modify circuit.
P.39 RT8209_1D05V Power team modify circuit
P.40 ADP3211_GFX_CORE/ VGA_CORE Power team modify circuit and VID GPIO setting.
P.49 M93/ PARK-S3 IO Delete VGA_XIN1 net from VGA to CLKGEN and add TP for VGA_JTAG pins and modify PEX_CLKREQ pull high to 3D3V_S5
P.3 Clock Generator Delete the net "VGA_XIN1" net from VGA to CLKGEN routing.

(2009/12/08)
P.46 EMI/Spring/Boss Delete SDF4, KS4 and add GND9, GND10 for ME request.
P.50 M93/ PARK-S3 POWER Pins A11, Y11, V11, U11 can left unconnected at M93-S3 and PARK-S3.
P.51 M93/ PARK-S3 DP POWER_GND DPF_PVDD, DPF_PVSS add damping resistor for PARK-S3.
P.49 M93/ PARK-S3 IO Change A2VSSQ connection to clean ground.
P.52 M93/ PARK-S3 Memory / Straps Modify "DRAM_RST" output circuit.
P.39 RT8209_1D05V Power team modify circuit (delete U107)
P.40 ADP3211_GFX_CORE/ VGA_CORE Modify VGA power sequence
P.41 APL5930_1V Modify VGA power sequence
P.48 M93/ PARK-S3 PCIE Modify VGA power sequence

(2009/12/09)
P.33 RUN POWER Delete R344 and C28.
P.3 Clock Generator Modify symbol to 9LVS3197BKLFT that only one CLKGEN source we will use. Delete pin16 CPU_STOP# to NC for 9LVS3197BKLFT.
P.31 KBC_NPCE781L / KB Add 100Kohm pull up resistor for ME_UNLOCK# and combine 3pcs 100Kohm pull up to one 8P4R resistor.
P.36 ADP3211_CPU CORE Change TC60 power plane from DCBATOUT to DCBATOUT_3211_CPU and add TC61 for DCBATOUT
P.9 CPU SFF(6 of 8)-CPUCORE Delete C978, C979, C982, C983 for placement.
P.17 PCH (6 of 9)-GPIO/RSVD Change PCH_GPIO57 DIS/UMA selection to KBC.

(2009/12/10)
P.36 ADP3211_CPU CORE Change net 3211_PWRGD pull high 1Kohm to 3D3V_S0
P.12 PCH (1 of 9)-SATA/RTC/HDA Change 4pcs TP to two dummy 0402 resistor for layout space.
P.33 RUN POWER Delete R2720 and R513.
P.14 PCH (3 of 9)-DMI/FDI Delete R464 and PM_PWROK connection to PCH.B17(PWROK).
P.48 M93/ PARK-S3 PCIE Delete M93 +BBP circuit.
P.27 MINI BD CONN Add one more power pin on BTBMINI1 for 3D3V_S3.
P.36 ADP3211_CPU CORE Modify VID[5:3] setting for 27A CPU core power rating.
P.26 CARDREADER BD CONN Modify WLAN_BT_DATA direction
P.27 MINI BD CONN Modify WLAN_BT_DATA direction
P.40 ADP3211_GFX_CORE/ VGA_CORE Add R2791 0ohm resistor installed on UMA SKU to separate the connection between VGA power circuit and CPU
P.12 PCH (1 of 9)-SATA/RTC/HDA Add R2793 pull low resistor on la
P.39 RT8209_1D05V Add sequence circuit for VTTPWRGOOD and VTT when system suddenly moves to G3 by removing both AC and battery at the same time.
P.14 PCH (3 of 9)-DMI/FDI Add sequence circuit for SYS_PWROK , PWROK, MEPWROK when system suddenly moves to G3 by removing both AC and battery at the same time.

(2009/12/11)
P.5 CPU SFF(2 of 8)-CLK/Thermal Modify RN93 resistor to two single resistors.
P.40 ADP3211_GFX_CORE/ VGA_CORE Delete R2644 and change R2642 to 10Kohm.
P.41 APL5930_1V Delete R2482.
P.47 ATI POWER Modify R2330 pull-up from 3D3V_S3 to 3D3V_S0.
P.41 APL5930_1V Modify R2479 pull-up from 3D3V_S3 to 3D3V_S0.
P.47 ATI POWER Modify 3D3V_VGA sequence circuit.
P.27 MINI BD CONN Modify to 8pin 3D3V_S3.
P.33 RUN POWER Change U138 to AO4406AL.

(2009/12/12)
P.27 MINI BD CONN Modify BTBMINI1 to 3pins of 3D3V_S3 and 6pins of 3D3V_S5.

(2009/12/14)
P.36 ADP3211_CPU CORE Change R2573 from 1.91Kohm to 10Kohm.
P.26 CARDREADER BD CONN Modify 5V_S0 power to 1D5V_S0 because 5V_S0 has not used on cardreader board.
P.16 PCH (5 of 9)-PCI/USB Modify USB_OC#3~USB_OC#7 to single pull-up.
P.39 RT8209_1D05V Delete G227, G225.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX Change R669,R668,R685,R695 to 0402 resistors.
P.9 CPU SFF(6 of 8)-CPUCORE Delete C1313, C1314.
P.14 PCH (3 of 9)-DMI/FDI Add D112 to match the sequence IMVP_VR_EN and SYS_PWROK/PCH_PWROK.

(2009/12/14)
P.50 M93/ PARK-S3 POWER Add 0ohm 0805 resistor for VDDCI.

(2009/12/15)
P.14 PCH (3 of 9)-DMI/FDI Modify reset circuit for POWEROK and VTTPWRGOOD sequence when system suddenly moves to G3.
P.13 PCH (2 of 9)-PCIE/CLK/SMB Add 0ohm resistor for XTAL25_OUT.

(2009/12/16)
P.14 PCH (3 of 9)-DMI/FDI Modify reset circuit for POWEROK,PM_RSMRST# and VTTPWRGOOD sequence when system suddenly moves to G3.
P.40 ADP3211_GFX_CORE/ VGA_CORE Modify VCC_AXG_SENSE,VSS_AXG_SENSE connection.
P.17 PCH (6 of 9)-GPIO/RSVD [Bom change] change RN119 from 10Kohm to 33Kohm.
P.36 ADP3211_CPU CORE [Bom change] change R2580 from 1Kohm to 3.3Kohm.
P.39 RT8209_1D05V [Bom change] delete Q84, R2742.

(2009/12/17)
P.14 PCH (3 of 9)-DMI/FDI Change D112 direction.
P.50 M93/ PARK-S3 POWER Change one 0805 resistor to two 0402 resistors for layout placement space.
P.40 ADP3211_GFX_CORE/ VGA_CORE Change R2660 size from 0402 to 0805 for VCC_AXG_SENSE/ VSS_AXG_SENSE routing.

(2009/12/21)
P.46 EMI/Spring/Boss EMC add EC103, EC106~EC117 for 3D3V_S0, 3D3V_S5, 5V_S5, 1D5V_S3, 1V_VGA, 1D5V_VGA.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX Delete C1282, C1281 and change C1264, C1265 to 4.7uF for layout placement space.
P.50 M93/ PARK-S3 POWER Delete C834, C807, C800, C811, C816, C815, C737, C799 and change C789 to 4.7uF for layout placement space.
P.46 EMI/Spring/Boss Delete EC80, EC79, EC82, EC59, EC58, EC51, EC12, SPR2 for layout placement space.
P.31 KBC_NPCE781L / KB Change PCB version setting for power saving in S5.
P.39 RT8209_1D05V Add VTT_PWRGD pull-up resistor.
P.37 [RT8223_5V/3D3V] Because the shortage of FDMC8296, change U100, U101 to FDMC7692.

(2010/01/09)
P.17 PCH (6 of 9)-GPIO/RSVD [BOM Change] change Q92 from transistor to MOS 2N7002 and change C1411 from 0.047uF to 0.1uF.
P.33 RUN POWER [BOM Change] change Q94, Q95 from transistor to MOS 2N7002.

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(2010/01/21)
P.38 [RT8209_1D5V] [BOM change] R2409 change from 30Kohm to 31.6Kohm.
P.37 [RT8223_5V/3D3V] [BOM change] R2393 change from 30Kohm to 31.6Kohm.
(2010/01/25)
P.13 [PCH (2 of 9)-PCIE/CLK/SMB] [BOM change] C1023, C1024 change from 18pF to 15pF.
P.49 [M93/ PARK-S3 IO] [BOM change] C719, C721 change from 10pF to 12pF.
P.32 [BIOS & SW/C & BAT ID & Felic] [BOM change] Add EC83, EC84 to 330pF for EMC request.
(2010/01/29)
P.23 [LCD CONN] [BOM change] Change DIS brightness source to EC control.
P.46 [EMI/Spring/Boss] Add EC51, 58,59 to 0.1uF for EMC request.
(2010/02/03)
P.24 [HDD CONN & TOUCHPAD] Change R2701 to 91Kohm and add C1417 to 2,2uF for HDD protection.
P.33 [RUN POWER] [BOM change] change R2779 to 100Kohm for 1D5V_S0_PWRGD.
P.42 [G9661_1D8V/ RT9026_0D75] [BOM change] change R2780 to 0ohm for 1D5V_S0_PWRGD.
(2010/02/04)
P.36 [ADP3211_CPU CORE] Change TC60 from EL CAP to POSCAP and change R2593 to 91Kohm.
P.37 [RT8223_5V/3D3V] Change R2384 to 75Kohm and change R2385 to 97.6Kohm.
P.39 [RT8209_1D05V] Change R2421 to 10.2Kohm.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Modify +VGA_CORE feedback trace connection and change C1373 to 820pF
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Change R2645 to 8.66Kohm for GFX.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Change R2657 to 63.4Kohm and cahnge R2647 to 6.65Kohm for VGA.
P.45 [UVP Protect] Change Q72 to P-MOSFET and add R2816, R2817 to 200Kohm.
P.36 [ADP3211_CPU CORE] Dummy R2613.
Close all open power gaps.
(2010/02/05)
P.31 [KBC_NPCE781L / KB] Change R2714 to 20Kohm for PCB version.
P.33 [RUN POWER] Add a dummy resistor R2818 to 100Kohm.
Close all open power gaps.
(2010/02/08)
P.14 [PCH (3 of 9)-DMI/FDI] Change R2812 to 165Kohm.
P.49 [M93/ PARK-S3 IO] Change R2562, R2563 options to PARK.
P.50 [M93/ PARK-S3 POWER] Change L75, R2426, C783, C867 options to M93.
P.50 [M93/ PARK-S3 POWER] Change L58, C841, C877, C842, C843 options to PARK.
P.52 [M93/ PARK-S3 Memory / Straps] Change R665 to 243ohm, R617 to 0ohm, C889 to 2.2nF for M93.
P.41 [APL5930_1V] Change R2483 to 59Kohm for M93.
P.50 [M93/ PARK-S3 POWER] Delete C810 for placement space.
P.33 [RUN POWER] Cahnge Q94 to transister, C1412 to 1uF, R2818 to 330Kohm and stuff it.
P.31 [KBC_NPCE781L / KB] Add R2819 pull-up to 3D3V_AUX_S5 and change C364 to 1uF for vender request.
P.24 [HDD CONN & TOUCHPAD] Modify R2701pull-up to 5V_AUX_S5 and dummy D105.
P.47 [ATI POWER] Change 3D3V_VGA solution from MOS to switch.
(2010/02/09)
P.42 [RT8015_1D8V/ RT9026_0D75] Change 1D8V_S0 power solution to RT8015.
P.46 [EMI/Spring/Boss] Add EC118 to 0.1uF at AD+ for EMC request.
P.47 [ATI POWER] Change 1D8V_VGA power solution and R2558 to 1Kohm.
P.7 [CPU SFF(4 of 8)-POWER/VTT] Delete C1238 for placement space.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Add R2823 to 267Kohm and dummy R2689.
P.14 [PCH (3 of 9)-DMI/FDI] Change U139 VCC to 3D3V_AUX_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Change D107 to 83.R2004.B8F and R2786 to 47Kohm.
P.41 [APL5930_1V] Change D108 to 83.R2004.B8F and R2480 to 10Kohm.
P.12 [PCH (1 of 9)-SATA/RTC/HDA] Change R2733~R2737 to 56ohm.
P.47 [ATI POWER] Modify 3D3V_VGA solution.
(2010/02/10)
P.47 [ATI POWER] Change R2824 pull up to 3D3V_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] Change R2642 pull up to 3D3V_S5.
P.47 [ATI POWER] Change R2558 to 0ohm, delete D109, R2788, C1415.
P.12 [PCH (1 of 9)-SATA/RTC/HDA] Change C1008, C1009 to 5pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB] Delete EC91 for placement space.
P.16 [PCH (5 of 9)-PCI/USB] Delete EC93 for placement space.
P.31 [KBC_NPCE781L / KB] Delete C363 for placement space.
P.50 [M93/ PARK-S3 POWER] Stuff C821 to 1uF.
P.47 [ATI POWER] Change Q100 to AO3415.
P.24 [HDD CONN & TOUCHPAD] Change Q77 to AO3419.
P.17 [PCH (6 of 9)-GPIO/RSVD] Stuff R2298 to 54.9ohm and dummy RN120 for THERMTRIP#.
P.33 [RUN POWER] Stuff R167 to 56ohm for THERMTRIP#.
P.5 [CPU SFF(2 of 8)-CLK/Thermal] Stuff R2305 to 0ohm for PROCHOT#.
(2010/02/11)
P.42 [RT8015_1D8V/ RT9026_0D75] Add more one gap G330 for 1D8V_S0.
P.42 [RT8015_1D8V/ RT9026_0D75] Add EC119 to 0.1uF for EMC request.
(2010/02/22)
P.41 [APL5930_1V] Change R2479 to 10Kohm for vga sequence.
P.47 [ATI POWER] Change C743 to 0.01uF, R583 to 47Kohm and R655 to 4.7Kohm for vga sequence.
P.33 [RUN POWER] Dummy R2818.
(2010/02/23)
P.17 [PCH (6 of 9)-GPIO/RSVD] Dummy R2298 and stuff RN120 for THERMTRIP#.
P.33 [RUN POWER] Dummy R167 for THERMTRIP#.
P.47 [ATI POWER] Change U94 to AO4430 Rds=5.5~7.5mohm
P.31 [KBC_NPCE781L / KB] Change U135 to G691L293T73UF.

(2010/02/24)
P.38 [RT8209_1D5V] [BOM change] R2409 change from 31.6Kohm to 30Kohm.
P.43 [BQ24751_Charger] [BOM change] R2512 change from 120Kohm to 63.4Kohm for DIS.
P.40 [ADP3211_GFX_CORE/ VGA_CORE] [BOM change] R2823 change from 267Kohm to 160Kohm for DIS.

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PVT

(2010/03/18)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Modify +VGA_CORE feedback trace connection.
P.14 [PCH (3 of 9)-DMI/FDI]	Change U139 VCC from 3D3V_AUX_S5 to 5V_AUX_S5.

(2010/03/22)

P.31 [KBC_NPCE781L / KB]	[BOM change] Dummy R142 double pull low.

(2010/03/24)

P.47 [ATI POWER]	[BOM change] Change U94 toSI4168 Rds=5.7~7.6mohm.
P.33 [RUN POWER]	Delete R2818 and change Q10 pin5 connection to PM_SLP_S3_CTL.

(2010/03/25)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2642 to 100Kohm for VGA sequence.
P.41 [APL5930_1V]	[BOM change] Change R2479 to 100Kohm for VGA sequence.
P.47 [ATI POWER]	[BOM change] Change D110 to RB751V for VGA sequence.
P.47 [ATI POWER]	[BOM change] C1419 to 0.22uF for VGA sequence PARK only.

(2010/03/29)

P.24 [HDD CONN & TOUCHPAD]	[BOM change] Change R2701 to 133Kohm and change R2702 to 3.3Kohm for HDD protection sequence.
P.24 [HDD CONN & TOUCHPAD]	Add C1379 to 0.1uF for HDD protection sequence.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2660 0ohm resistor to 0805 size.

(2010/03/30)

P.36 [ADP3211_CPU CORE]	Change U127 to TPCA8030 and change U128, U129 to TPCA8028 for VCC_CORE quality.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Dummy R2823 and add R2689 to 100Kohm for VGACORE level.

(2010/03/31)

P.31 [KBC_NPCE781L / KB]	Add CP and CP2 option circuit.
Change 0ohm resistors to 0ohm pads	0402-pad: R2547, R2732, R2566, R2553, R2568, R2567, R2574, R2552, R2554, R2572, R2550, R2570, R2549, R2731, R2569, R2551, R2578, R2548 0603-pad: R2669, R2246, R2247

(2010/04/01)

P.38 [RT8209_1D5V]	[BOM change] Change R2411 to 10Kohm and change R2409 to 10.2Kohm to rise 1% of 1D5V_S3 level.
P.49 [M93/ PARK-S3 IO]	[BOM change] C719, C721 change to 6.8pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	[BOM change] C1023, C1024 change to 12pF.

(2010/04/02)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2659, R2698 to 0ohm resistor for VGA_CORE transition overshoot.

(2010/04/07)

P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change C1414 0.1UF capacitor from Y5V to X7R.

(2010/04/12)

P.49 [M93/ PARK-S3 IO]	[BOM change] Add 2nd source for X7.

MP

(2010/04/21)

P.19 [PCH (8 of 9)-PWR\SATA\USB]	Change VCCSUSHDA power plane to 1.5V_S5.

(2010/04/24)

P.19 [PCH (8 of 9)-PWR\SATA\USB]	Add R2826 dummy pull low resistor for enable pin.

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