

## Schematics Page Index (Title / Revision / Change Date)

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28	VRAM(BYPASS) 2/2	1.00	2006/04/10	68	SYS Power(+1.5V/+1.05V)	1.00	2006/04/10
29	TVIN and OUT/Semi-PnP	1.00	2006/04/10	69	DDR2 Power(+1.8V/+0.9V)	1.00	2006/04/10
30	CRT	1.00	2006/04/10	70	CPU Vcore ---MAX8771	1.00	2006/04/10
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33	Hot plug behavior & IDC ARRANGEMENT block diagram	1.00	2006/04/10	73	VGA POWER(+1.1V/ +1.2V)	1.00	2006/04/10
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37	ICH7-M PCI/USB 1 1/5	1.00	2006/04/10	77	HISTORY(PVT)	1.00	2006/04/10
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40	ICH7-M POWER 4/5	1.00	2006/04/10	80	Power On Sequence Timing	1.00	2006/04/10

Project Code &amp; Schematics Subject: MS20 MP Main Board

PCB P/N: 1P-0064100-8011 (FUBAI)  
1P-1064506-8011 (HANSTAR)

P. Leader	Check by	Design by
紀博文/楊朝川	楊朝川	楊朝川
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CUPBG - R&D Division		
Index Page		
Rev. 1.00	Document Name	Rev. 1.00
MS20-1-01 Main Board (MS20-101)		
Date: 2006/04/10		

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40	ICH7-M( POWER) 4/5	1.00	2006/04/10	80	Power On Sequerce Timing	1.00	2006/04/10

P. Leader	Check by	Design by

Project Code & Schematics Subject: MS20 MP Main Board

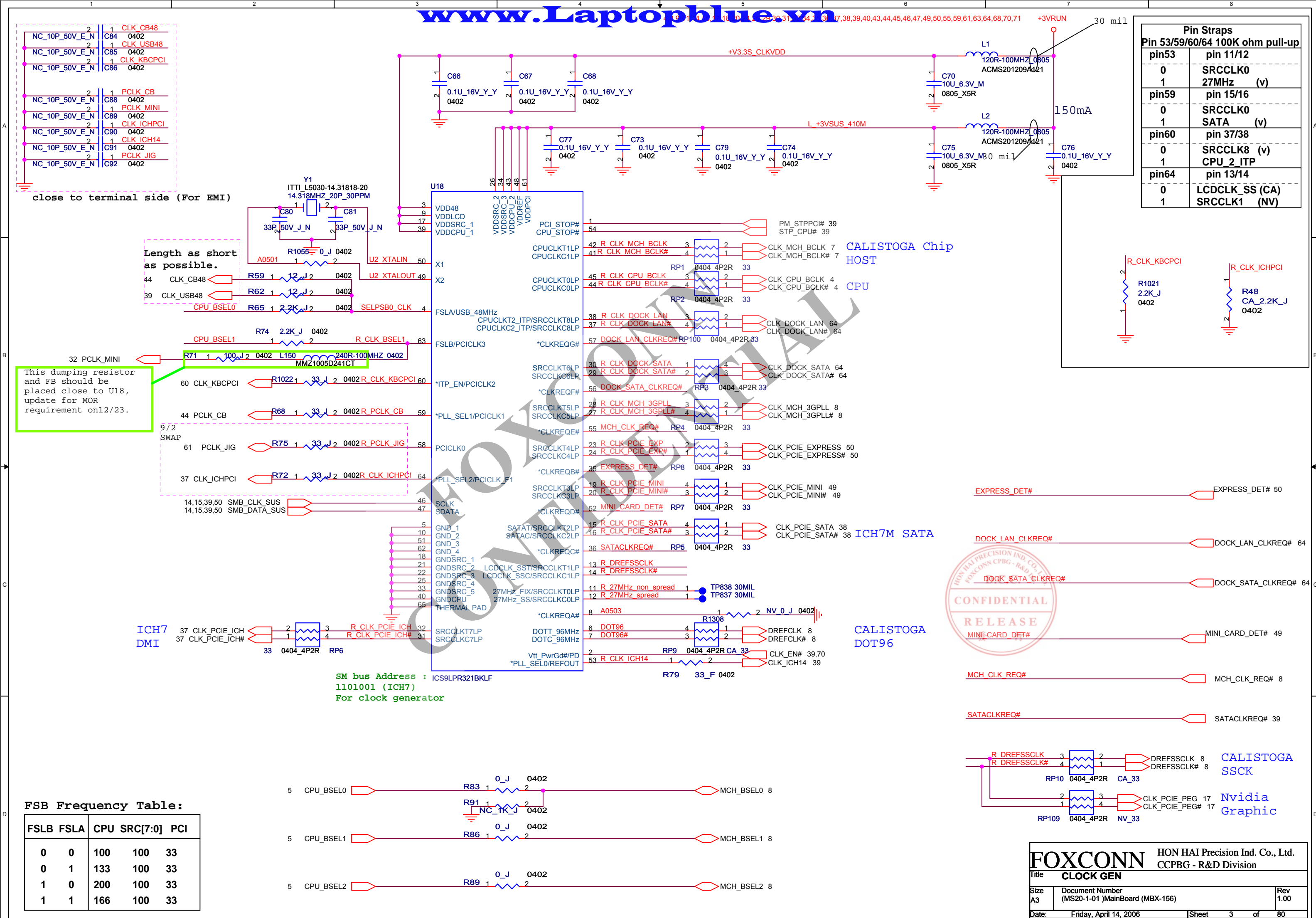
PCB P/N: 1P-0064100-8011 (FUBAI)  
1P-1064506-8011 (HANSTAR)

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
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Size A3	Document Number (MS20-1-01 )MainBoard (MBX-156)	Rev 1.00
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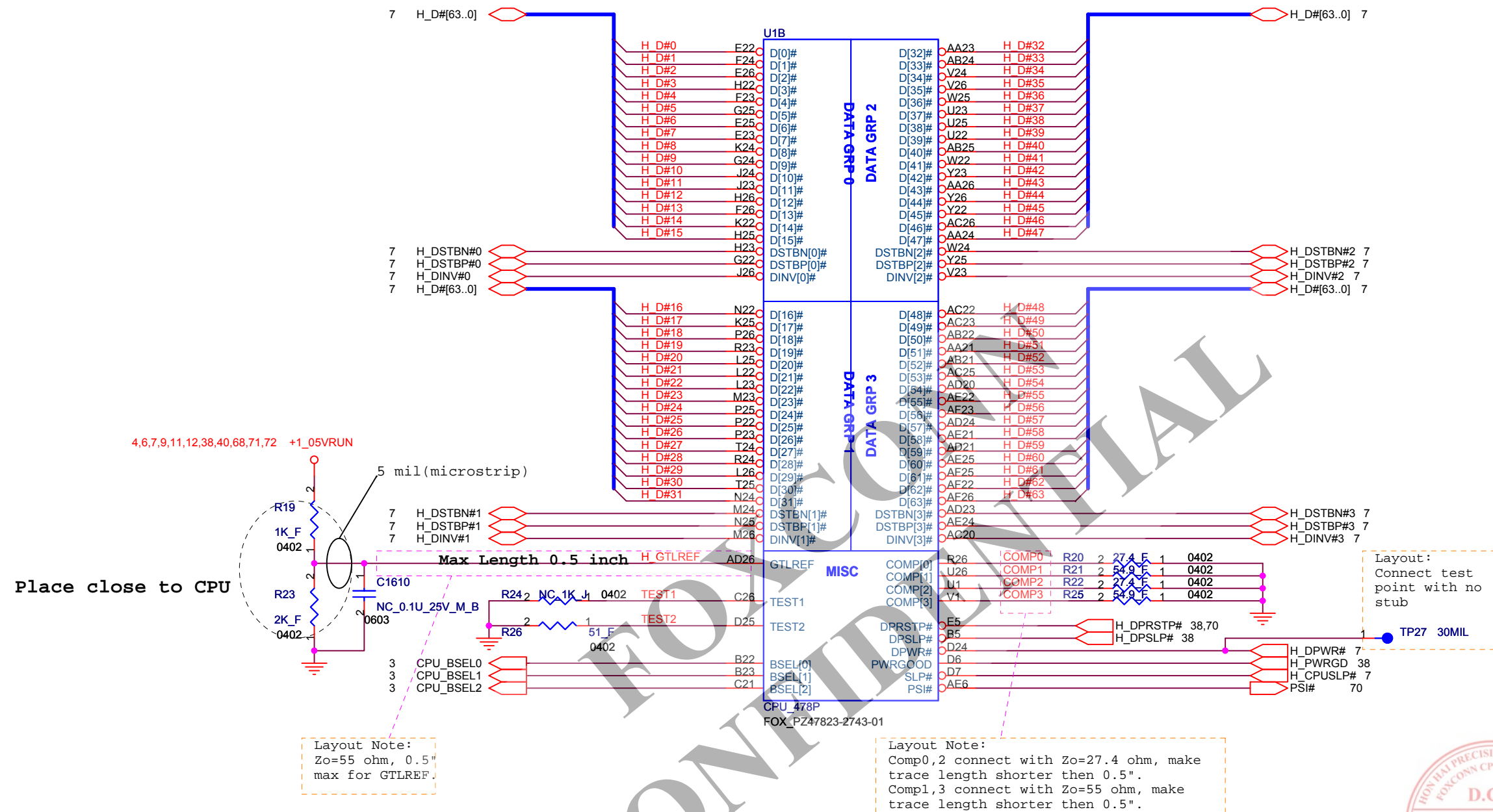
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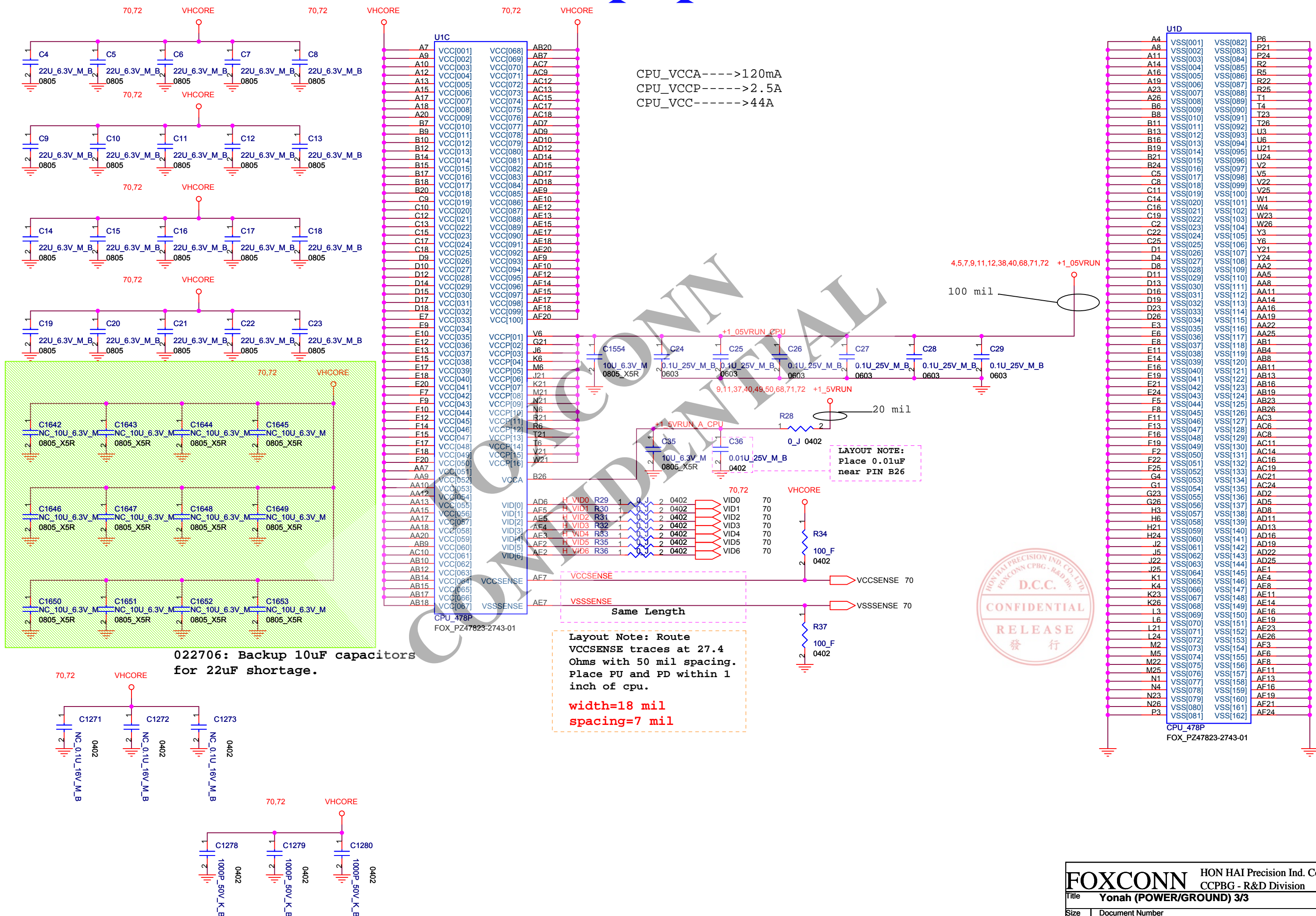
	Symbol ahead of value for NC components	945PM + G7XM + Infineon or Samsung VRAM	NVH_
BOTH	NC_	945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM	CA_	945PM + G7XM + Hynix VRAM	NVIS_
945GM	NV_	945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M	NV73_	945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M	NV72_	945PM + G73M-U	NV8M_, NV7273_
945PM + G72M or G73M-U	NV73Only_	*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_

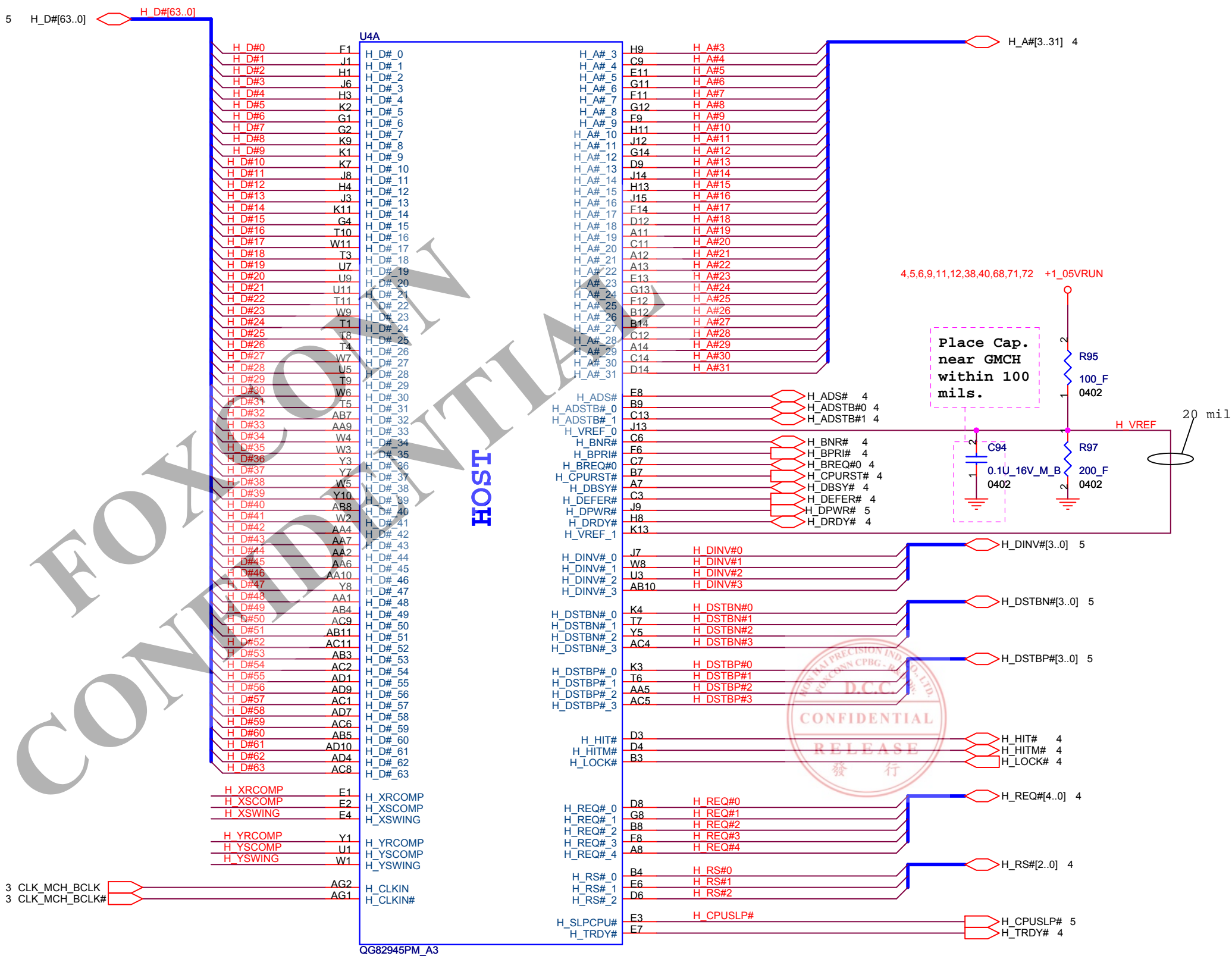












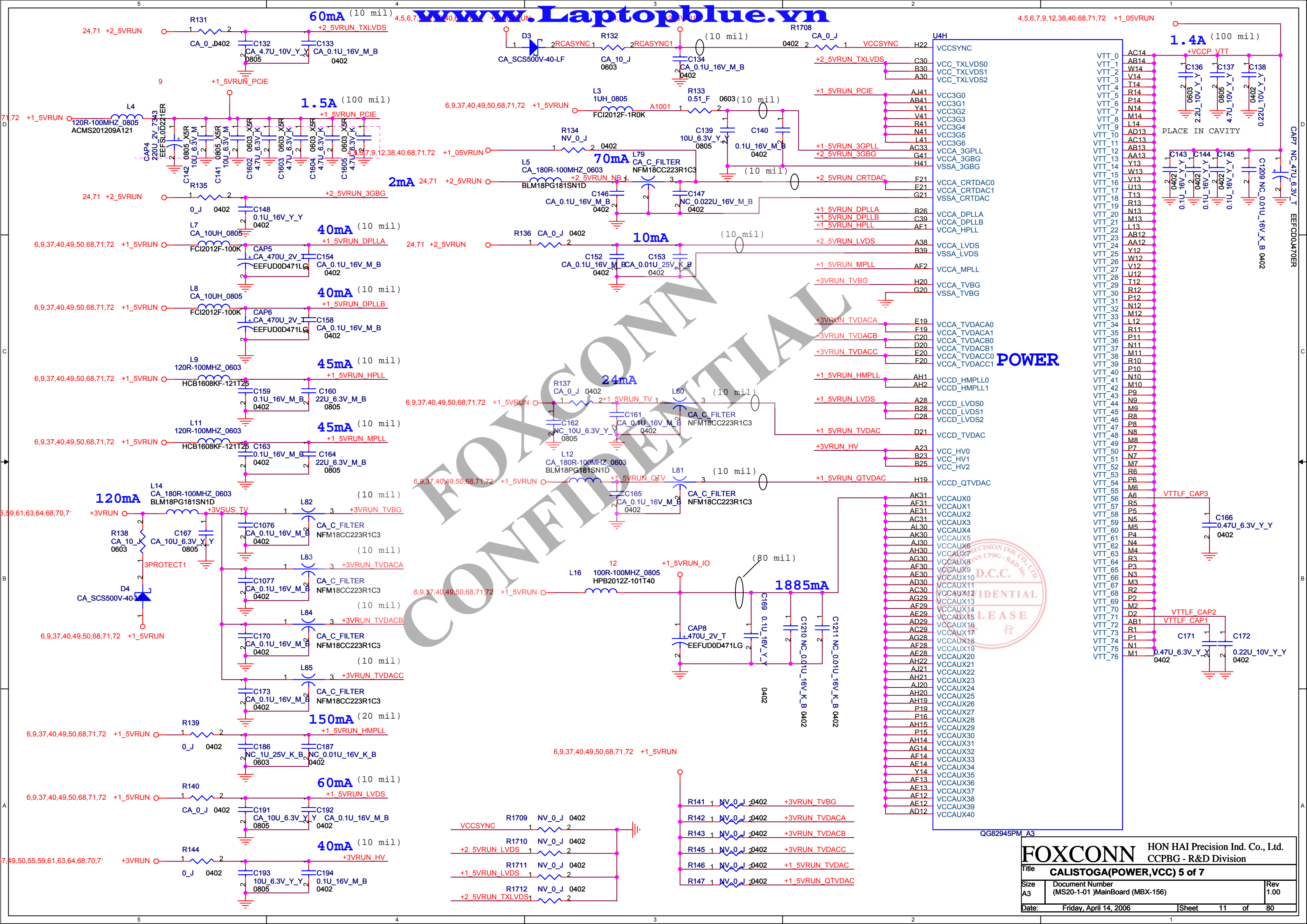
















8 MCH\_CFG\_5 ◀ 1 30MIL TP554

MCH_CFG_5	Low = DMIx2 High = DMIx4
-----------	-----------------------------

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------

8 MCH\_CFG\_18 ◀ 1 30MIL TP555

8 MCH\_CFG\_6 ◀ 1 30MIL TP556

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	---

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
--------------------------------------	--

8 TP\_MCH\_CFG\_7 ◀ TP\_MCH\_CFG\_7

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
--------------------------	--

8 MCH\_CFG\_19 ◀ 1 30MIL TP558

8 MCH\_CFG\_9 ◀ 1 30MIL TP559

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation
---	--

For layout convenience

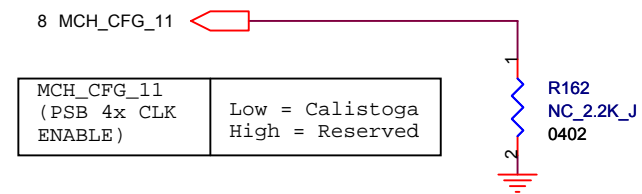
MCH_CFG_20 (PCIE Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
---	---

8 MCH\_CFG\_20 ◀ 1 30MIL TP561

8 MCH\_CFG\_10 ◀ 1 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
--	-----------------------------------

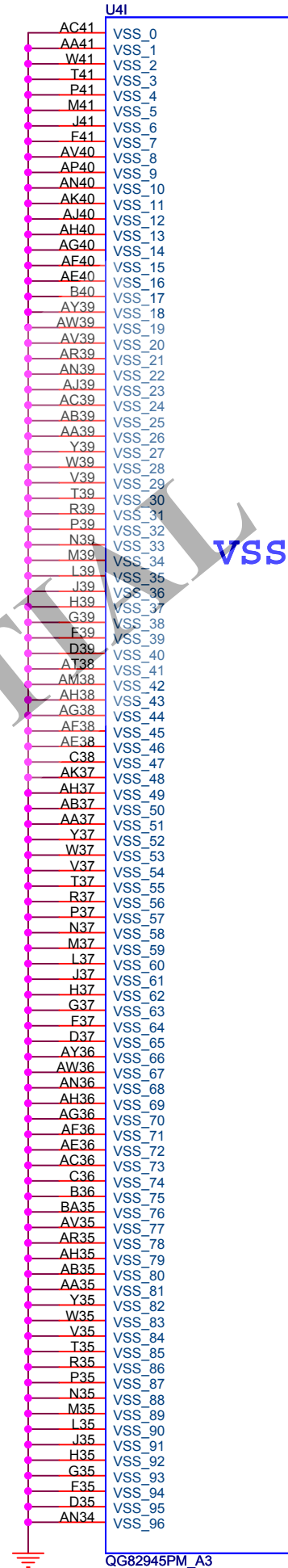
Layout Noe:  
Location of all MCH\_CFG strap resistors  
needs to be close to trace to minimize  
stub

8 MCH\_CFG\_12 ◀ 1 30MIL TP562  
8 MCH\_CFG\_13 ◀ 1 30MIL TP563

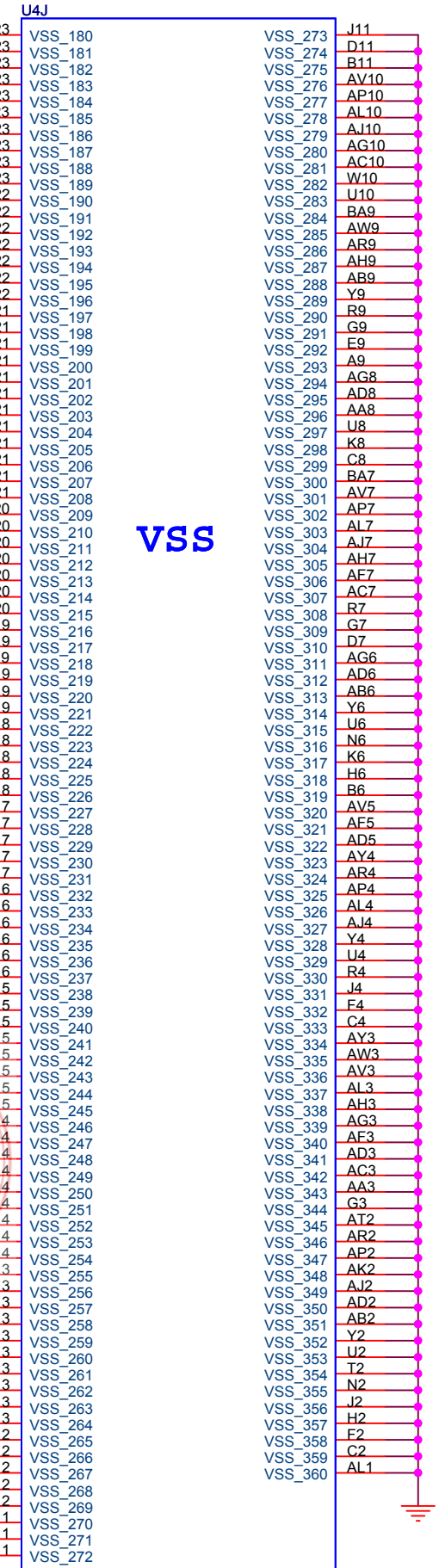
MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---

8 MCH\_CFG\_16 ◀ 1 30MIL TP564

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
------------------------------------	---

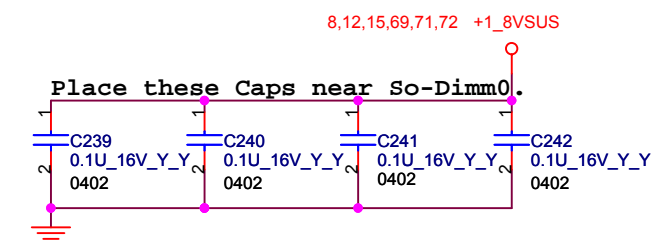
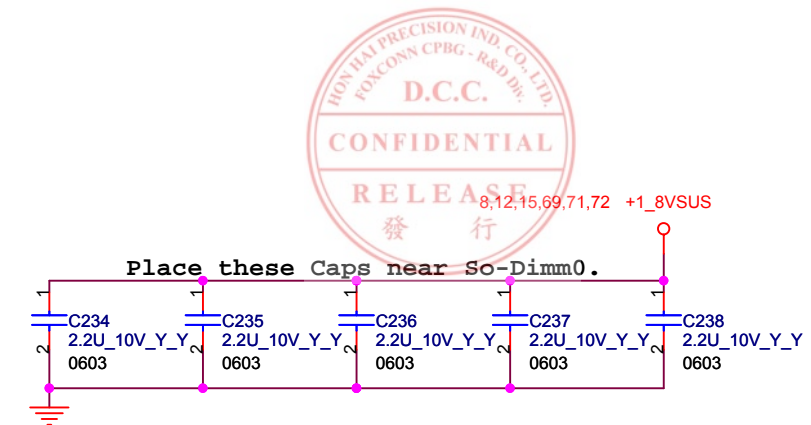
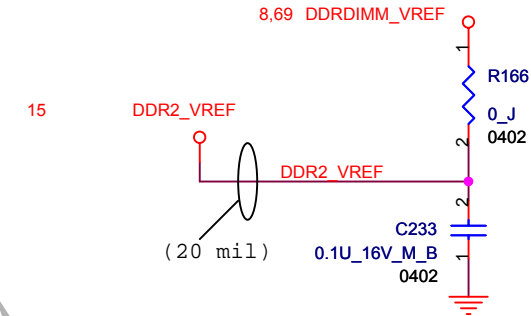
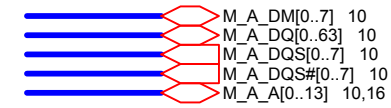


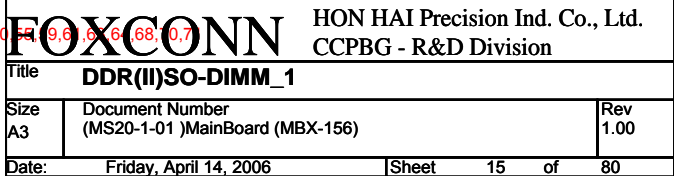
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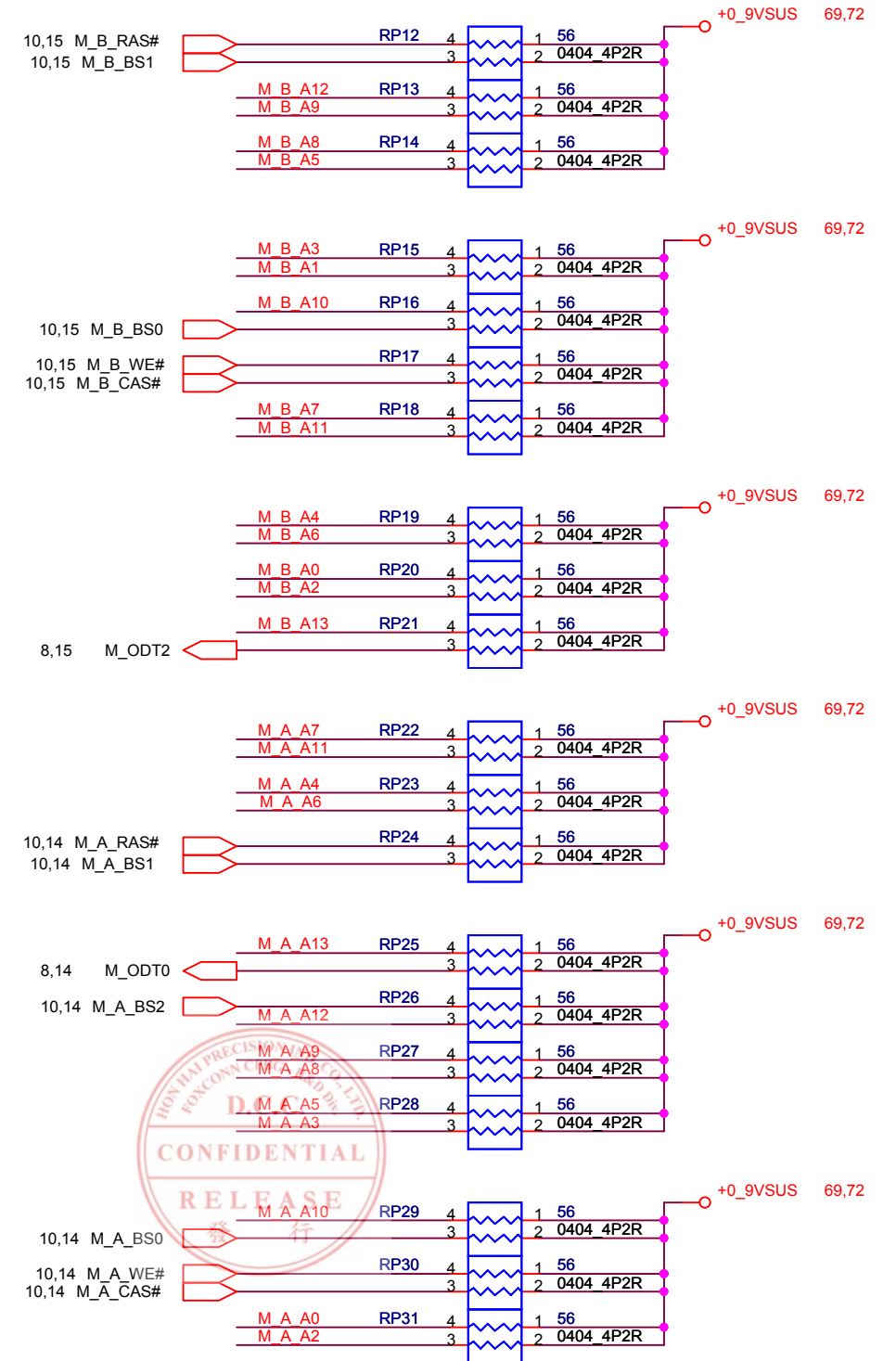
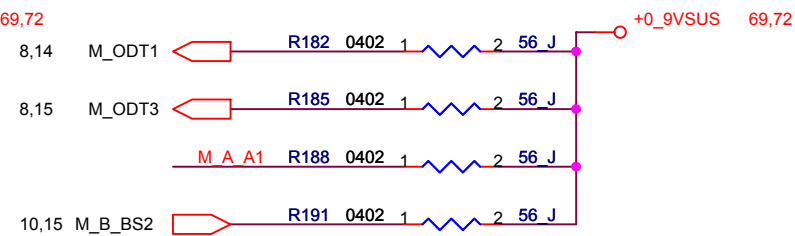
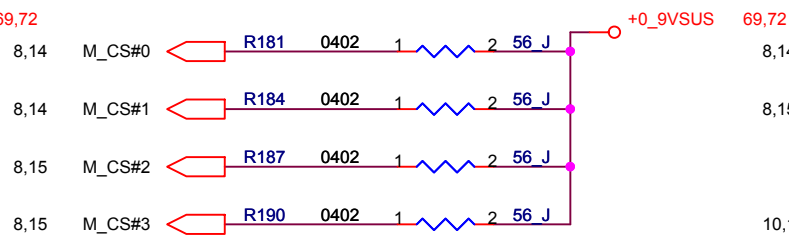
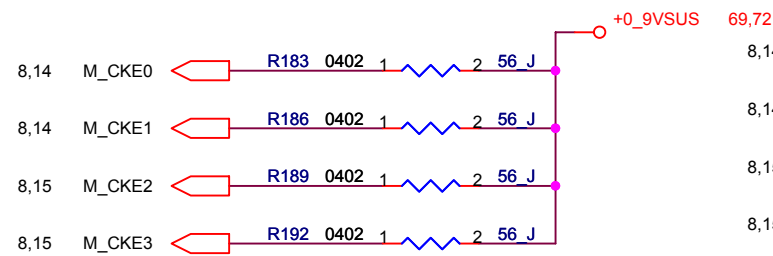
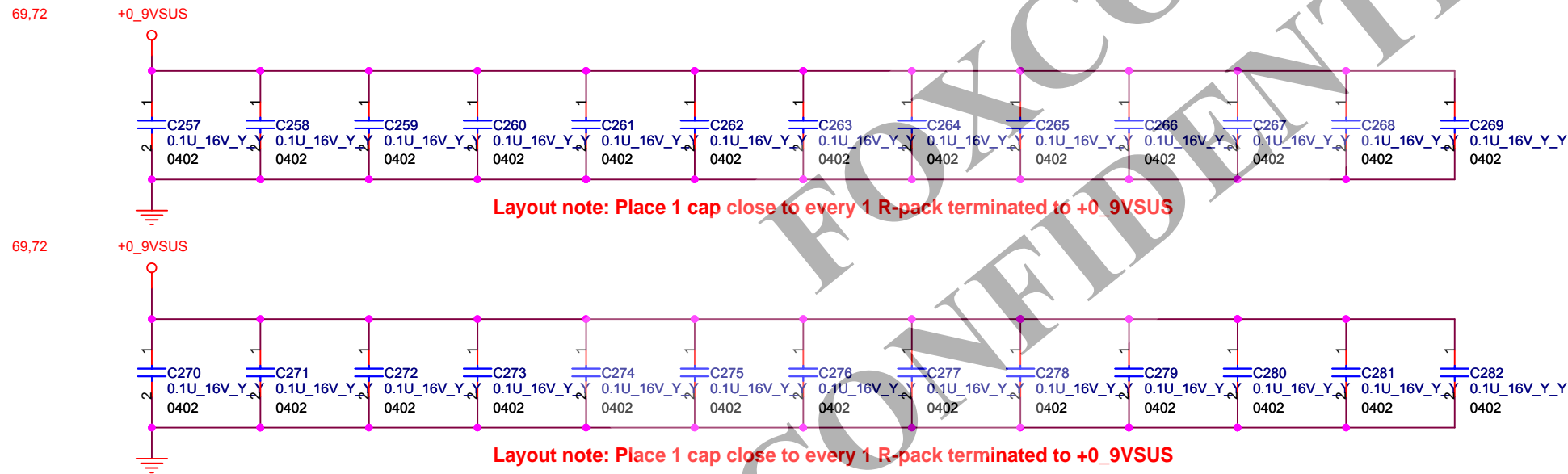


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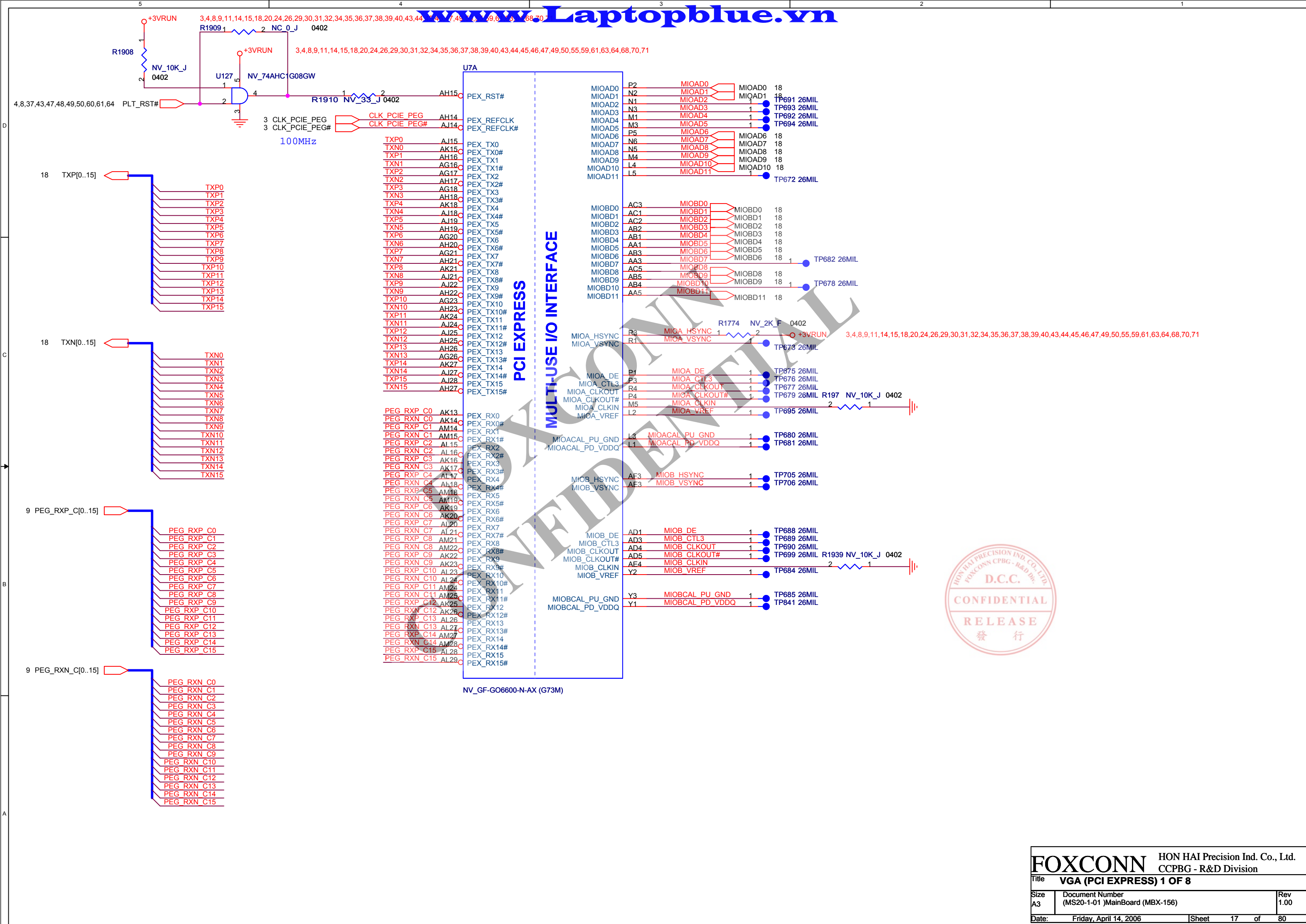


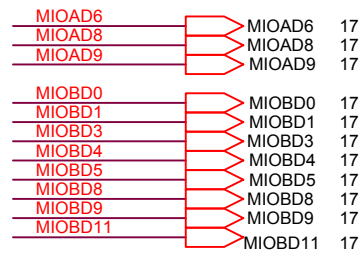
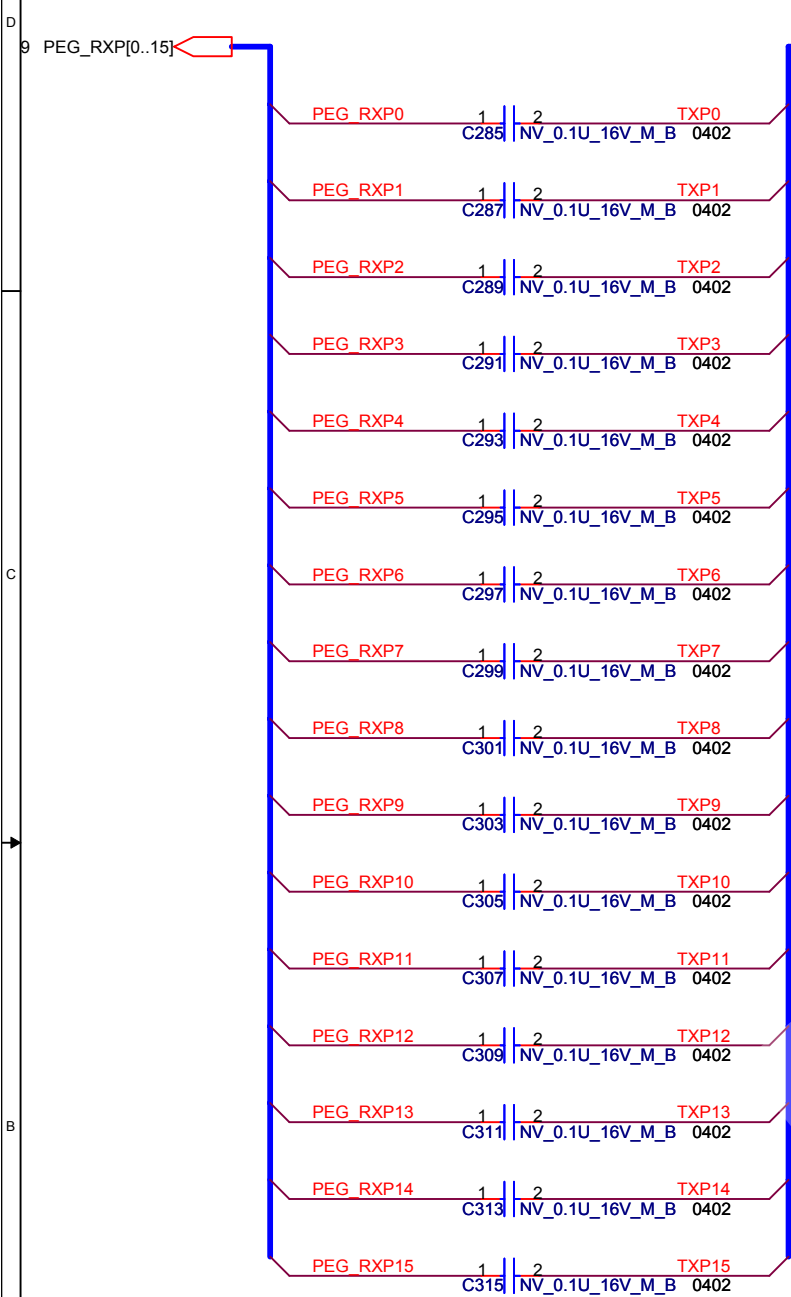












TVMODE (NV43M/G7X)  
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

TXN[0..15] 17

Strap for GDDR3-136ball

0001 16Mx32Infineon

0010 16Mx32Hynix

0011 16Mx32Samsung

0101 8Mx32Infineon

0110 8Mx32Hynix

0111 8Mx32Samsung

SUBVENDOR

0 (USE SYSTEM BIOS)

1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.  
DEFAULT "0"

3GIO\_PADCFG[2:0]

001 for NV43/NV44

010 for G7X/NV42

G72M/G73M/NV43M

PCI\_DEVID[3:0]="1000"->8

G73M-U

PCI\_DEVID[3:0]="1001"->9

CRYSTAL (NV43M/G7X)  
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

ROM\_TYPE (NV43M/G7X) NC

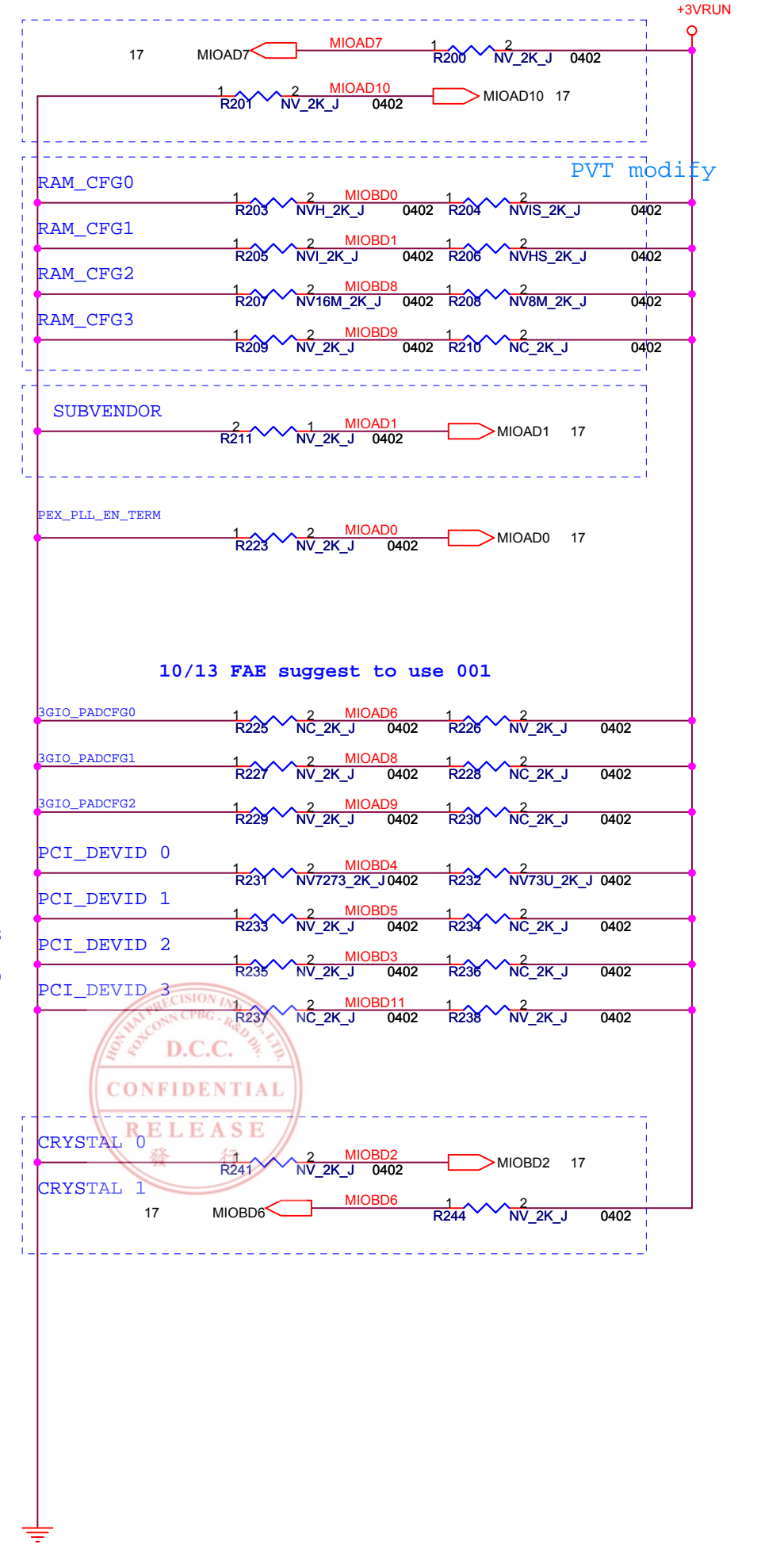
MIOBD10, MIOBD\_HSYNC

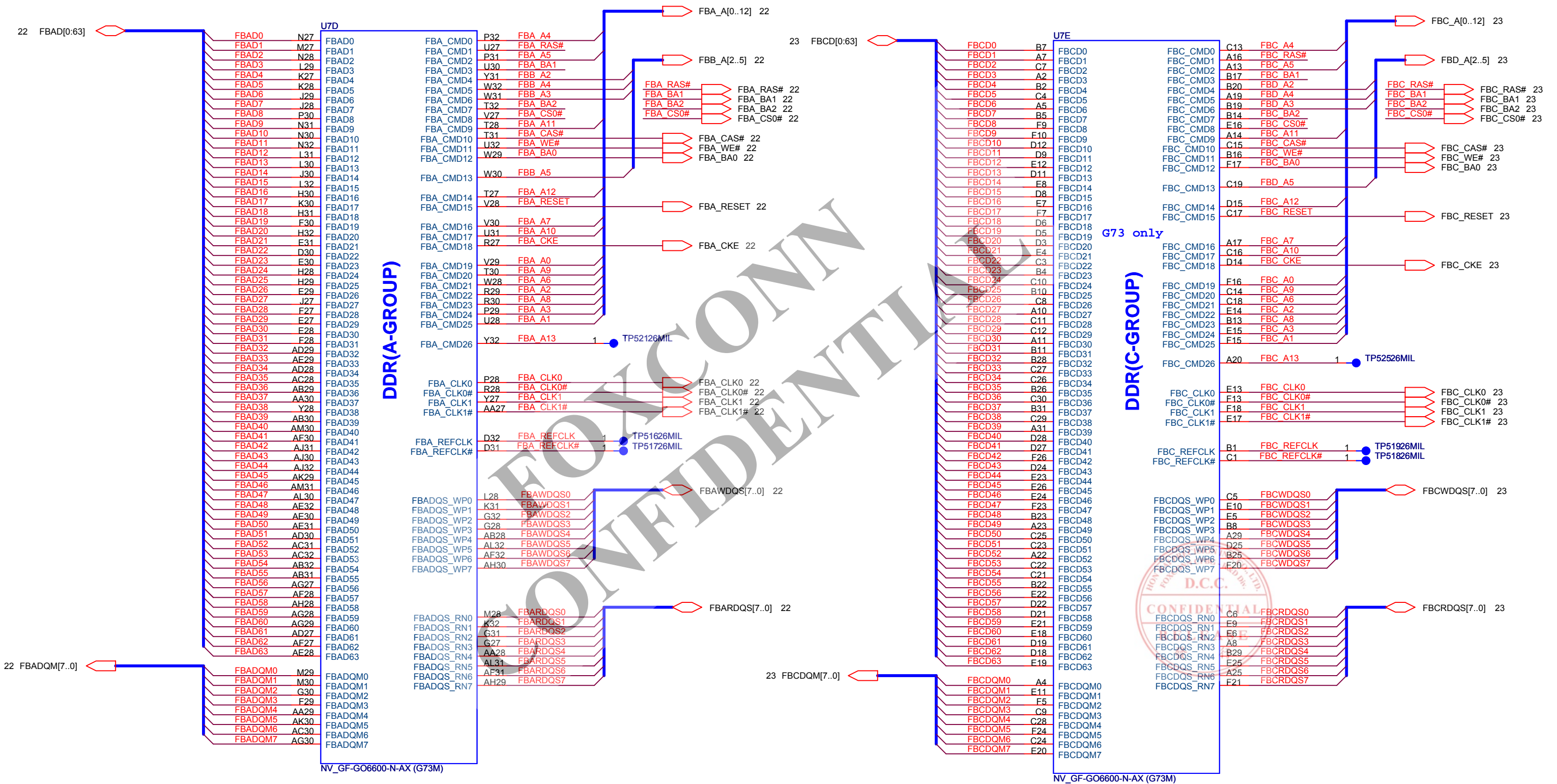
00 PARALLEL

01 SERIAL\_AT25F

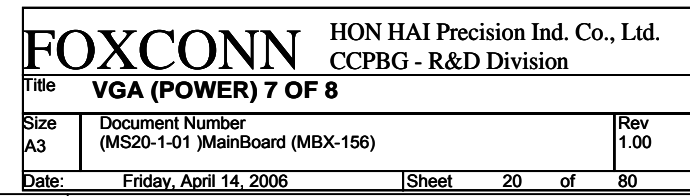
10 SERIAL\_SST45VF

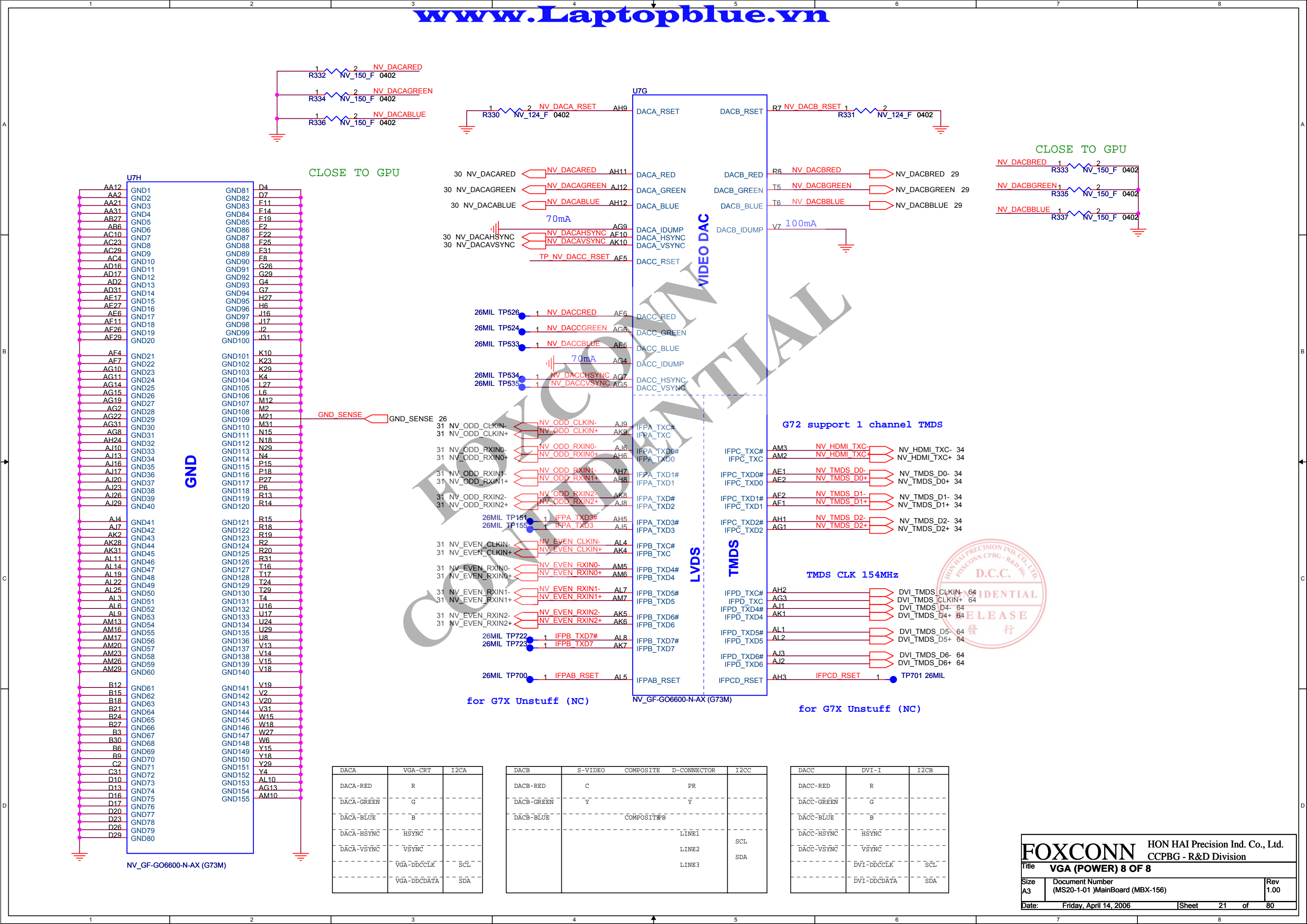
11 LPC











DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE	FB	
			LINE1	
			LINE2	SCL
			LINE3	SDA

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Diagram illustrating the connection of the NV\_GF-GO6600-N-AX (G73M) GPU to the motherboard, showing various signal lines and components.

**GPU Pinout (U7H):**

- AA12: GND1
- AA2: GND2
- AA21: GND3
- AA31: GND4
- AB27: GND5
- AB6: GND6
- AC10: GND7
- AC23: GND8
- AC29: GND9
- AC4: GND10
- AD16: GND11
- AD17: GND12
- AD2: GND13
- AD31: GND14
- AE17: GND15
- AE27: GND16
- AE6: GND17
- AE11: GND18
- AE26: GND19
- AE29: GND20
- AF4: GND21
- AF7: GND22
- AG10: GND23
- AG11: GND24
- AG14: GND25
- AG15: GND26
- AG19: GND27
- AG2: GND28
- AG22: GND29
- AG31: GND30
- AG8: GND31
- AH24: GND32
- AJ10: GND33
- AJ13: GND34
- AJ16: GND35
- AJ17: GND36
- AJ20: GND37
- AJ23: GND38
- AJ26: GND39
- AJ29: GND40
- AJ4: GND41
- AJ7: GND42
- AK2: GND43
- AK28: GND44
- AK31: GND45
- AL11: GND46
- AL14: GND47
- AL19: GND48
- AL22: GND49
- AL25: GND50
- AL3: GND51
- AL6: GND52
- AL9: GND53
- AM13: GND54
- AM16: GND55
- AM17: GND56
- AM20: GND57
- AM23: GND58
- AM26: GND59
- AM29: GND60
- B12: GND61
- B15: GND62
- B18: GND63
- B21: GND64
- B24: GND65
- B27: GND66
- B3: GND67
- B30: GND68
- B6: GND69
- B9: GND70
- C2: GND71
- C31: GND72
- D10: GND73
- D13: GND74
- D16: GND75
- D17: GND76
- D20: GND77
- D23: GND78
- D26: GND79
- D29: GND80

**GPU Pinout (U7G):**

- D4: GND81
- D7: GND82
- F11: GND83
- F14: GND84
- F19: GND85
- F2: GND86
- F22: GND87
- F25: GND88
- F31: GND89
- F8: GND90
- G26: GND91
- G29: GND92
- G4: GND93
- G7: GND94
- H27: GND95
- H6: GND96
- J16: GND97
- J17: GND98
- J2: GND99
- J31: GND100
- K10: GND101
- K23: GND102
- K29: GND103
- K4: GND104
- L27: GND105
- L6: GND106
- M12: GND107
- M2: GND108
- M21: GND109
- M31: GND110
- N15: GND111
- N18: GND112
- N29: GND113
- N4: GND114
- P15: GND115
- P18: GND116
- P27: GND117
- P6: GND118
- R13: GND119
- R14: GND120
- R15: GND121
- R18: GND122
- R19: GND123
- R2: GND124
- R20: GND125
- R31: GND126
- T16: GND127
- T17: GND128
- T24: GND129
- T29: GND130
- T4: GND131
- U16: GND132
- U17: GND133
- U24: GND134
- U29: GND135
- U8: GND136
- V13: GND137
- V14: GND138
- V15: GND139
- V18: GND140
- V19: GND141
- V2: GND142
- V20: GND143
- V31: GND144
- W15: GND145
- W18: GND146
- W27: GND147
- W6: GND148
- Y15: GND149
- Y18: GND150
- Y29: GND151
- Y4: GND152
- AL10: GND153
- AG13: GND154
- AM10: GND155

**Connections:**

- DACA:** NV\_DACARED, NV\_DACAGREEN, NV\_DACABLUE, NV\_DACAHSYNC, NV\_DACA\_VSYNC, NV\_DACC\_RSET.
- DACB:** NV\_DACBRED, NV\_DACBGREEN, NV\_DACBBLUE, NV\_DACBHSYNC, NV\_DACB\_VSYNC, NV\_DACB\_RSET.
- DACC:** NV\_DACCRED, NV\_DACCGREEN, NV\_DACCBLUE, NV\_DACC\_IDUMP, NV\_DACC\_HSYNC, NV\_DACC\_VSYNC, NV\_DACC\_RSET.
- IFPA:** NV\_ODD\_CLKIN-, NV\_ODD\_CLKIN+, NV\_ODD\_RXIN0-, NV\_ODD\_RXIN0+, NV\_ODD\_RXIN1-, NV\_ODD\_RXIN1+, NV\_ODD\_RXIN2-, NV\_ODD\_RXIN2+, NV\_EVEN\_CLKIN-, NV\_EVEN\_CLKIN+, NV\_EVEN\_RXIN0-, NV\_EVEN\_RXIN0+, NV\_EVEN\_RXIN1-, NV\_EVEN\_RXIN1+, NV\_EVEN\_RXIN2-, NV\_EVEN\_RXIN2+, IFPA\_TXC#, IFPA\_TXD0#, IFPA\_TXD1#, IFPA\_TXD2#, IFPA\_TXD3#, IFPA\_TXD4#, IFPA\_TXD5#, IFPA\_TXD6#, IFPA\_TXD7#, IFPA\_RSET.
- IFPB:** NV\_ODD\_CLKIN-, NV\_ODD\_CLKIN+, NV\_ODD\_RXIN0-, NV\_ODD\_RXIN0+, NV\_ODD\_RXIN1-, NV\_ODD\_RXIN1+, NV\_ODD\_RXIN2-, NV\_ODD\_RXIN2+, NV\_EVEN\_CLKIN-, NV\_EVEN\_CLKIN+, NV\_EVEN\_RXIN0-, NV\_EVEN\_RXIN0+, NV\_EVEN\_RXIN1-, NV\_EVEN\_RXIN1+, NV\_EVEN\_RXIN2-, NV\_EVEN\_RXIN2+, IFPB\_TXC#, IFPB\_TXD0#, IFPB\_TXD1#, IFPB\_TXD2#, IFPB\_TXD3#, IFPB\_TXD4#, IFPB\_TXD5#, IFPB\_TXD6#, IFPB\_TXD7#, IFPB\_RSET.
- IFPC:** NV\_HDMI\_TXC-, NV\_HDMI\_TXC+, NV\_TMDS\_D0-, NV\_TMDS\_D0+, NV\_TMDS\_D1-, NV\_TMDS\_D1+, NV\_TMDS\_D2-, NV\_TMDS\_D2+, NV\_TMDS\_CLKIN-, NV\_TMDS\_CLKIN+, NV\_TMDS\_D4-, NV\_TMDS\_D4+, NV\_TMDS\_D5-, NV\_TMDS\_D5+, NV\_TMDS\_D6-, NV\_TMDS\_D6+, IFPCD\_RSET.
- IFPD:** NV\_HDMI\_TXC-, NV\_HDMI\_TXC+, NV\_TMDS\_D0-, NV\_TMDS\_D0+, NV\_TMDS\_D1-, NV\_TMDS\_D1+, NV\_TMDS\_D2-, NV\_TMDS\_D2+, NV\_TMDS\_CLKIN-, NV\_TMDS\_CLKIN+, NV\_TMDS\_D4-, NV\_TMDS\_D4+, NV\_TMDS\_D5-, NV\_TMDS\_D5+, NV\_TMDS\_D6-, NV\_TMDS\_D6+, IFPD\_RSET.

**Tables:**

DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDA	SDA

DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DDCCLK	SCL
	DVI-DDCDA	SDA

**Notes:**

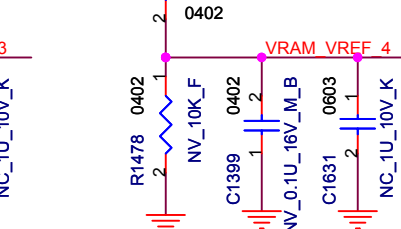
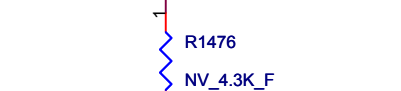
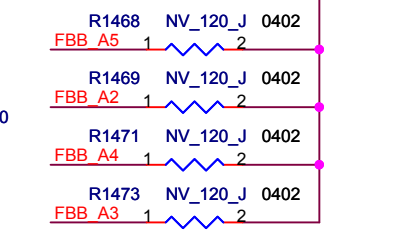
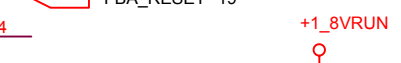
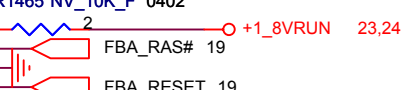
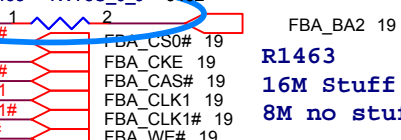
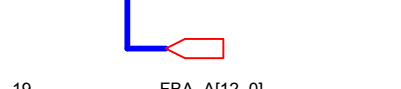
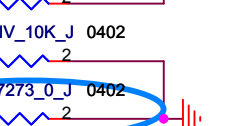
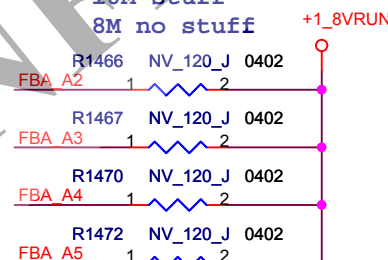
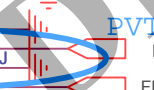
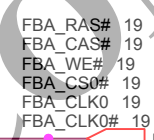
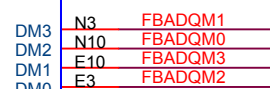
- for G7X Unstuff (NC)
- for G7X Unstuff (NC)

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**VGA (POWER) 8 OF 8**

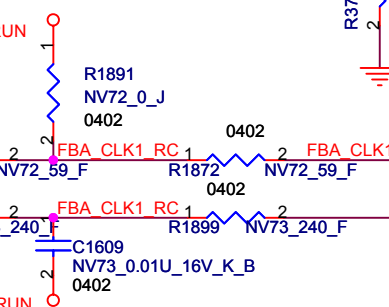
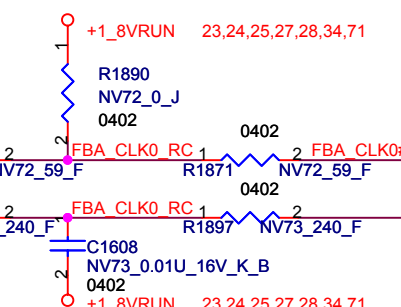
Size A3 Document Number (MS20-1-01) MainBoard (MBX-156) Rev 1.00

Date: Friday, April 14, 2006 Sheet 21 of 80

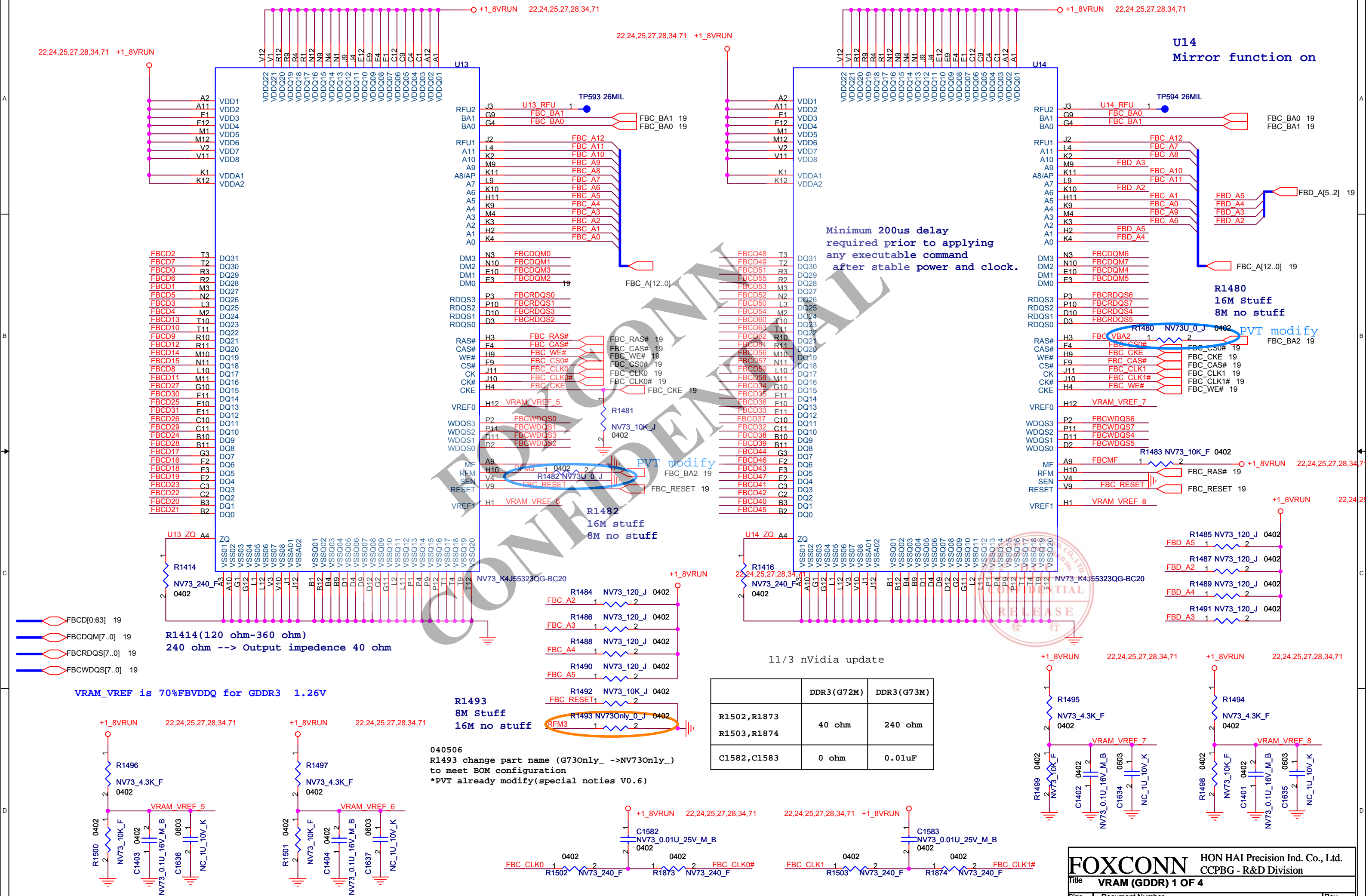


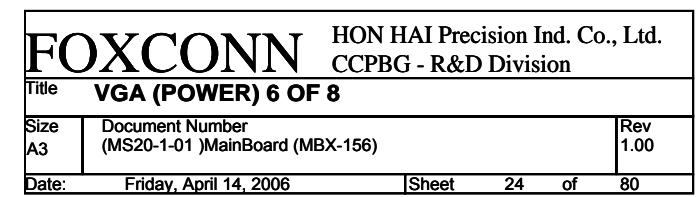
12/20 NVidia update

FAB suggestion on 10/26  
Close to VRAM









**www.Laptopblue.vn**

For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

U7I

**POWER**

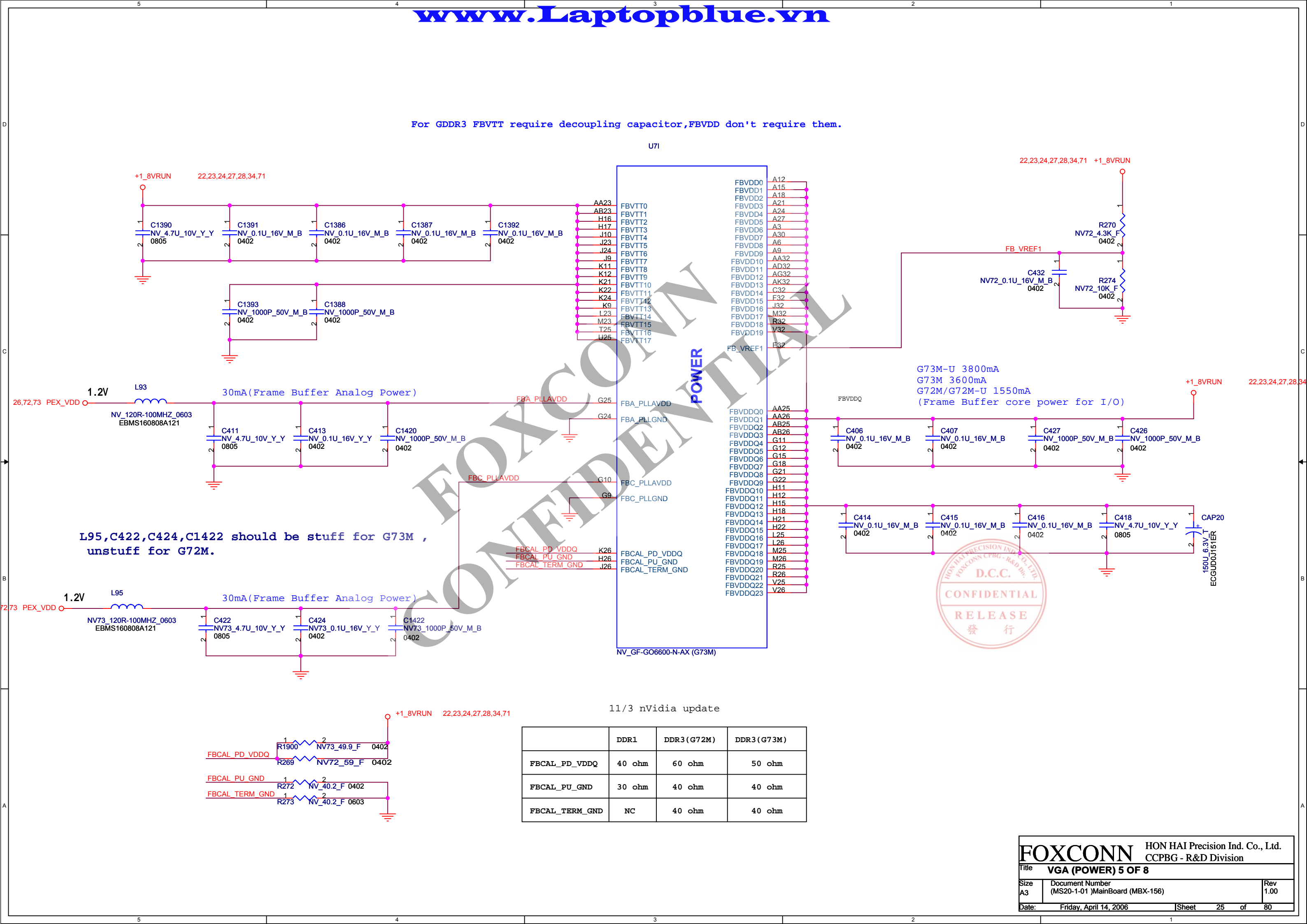
NV\_GF-GO6600-N-AX (G73M)

L95,C422,C424,C1422 should be stuff for G73M ,  
unstuff for G72M.

11/3 nVidia update

	DDR1	DDR3 (G72M)	DDR3 (G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division  
Title **VGA (POWER) 5 OF 8**  
Size A3 Document Number (MS20-1-01 )MainBoard (MBX-156) Rev 1.00  
Date: Friday, April 14, 2006 Sheet 25 of 80



www.Laptopblue.vn

For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

U71

1.2V L93 NV 120R-100MHZ\_0603 EBMS160808A121

30mA(Frame Buffer Analog Power)

1.2V L95 NV73 120R-100MHZ\_0603 EBMS160808A121

30mA(Frame Buffer Analog Power)

L95,C422,C424,C1422 should be stuff for G73M , unstuff for G72M.

11/3 nVidia update

	DDR1	DDR3 (G72M)	DDR3 (G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

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VGA (POWER) 5 OF 8

Document Number (MS20-1-01 )MainBoard (MBX-156)

Rev 1.00

Friday, April 14, 2006

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For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

U71

1.2V L93 NV 120R-100MHZ\_0603 EBMS160808A121

30mA(Frame Buffer Analog Power)

1.2V L95 NV73 120R-100MHZ\_0603 EBMS160808A121

30mA(Frame Buffer Analog Power)

L95,C422,C424,C1422 should be stuff for G73M , unstuff for G72M.

11/3 nVidia update

	DDR1	DDR3 (G72M)	DDR3 (G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

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VGA (POWER) 5 OF 8

Document Number (MS20-1-01 )MainBoard (MBX-156)

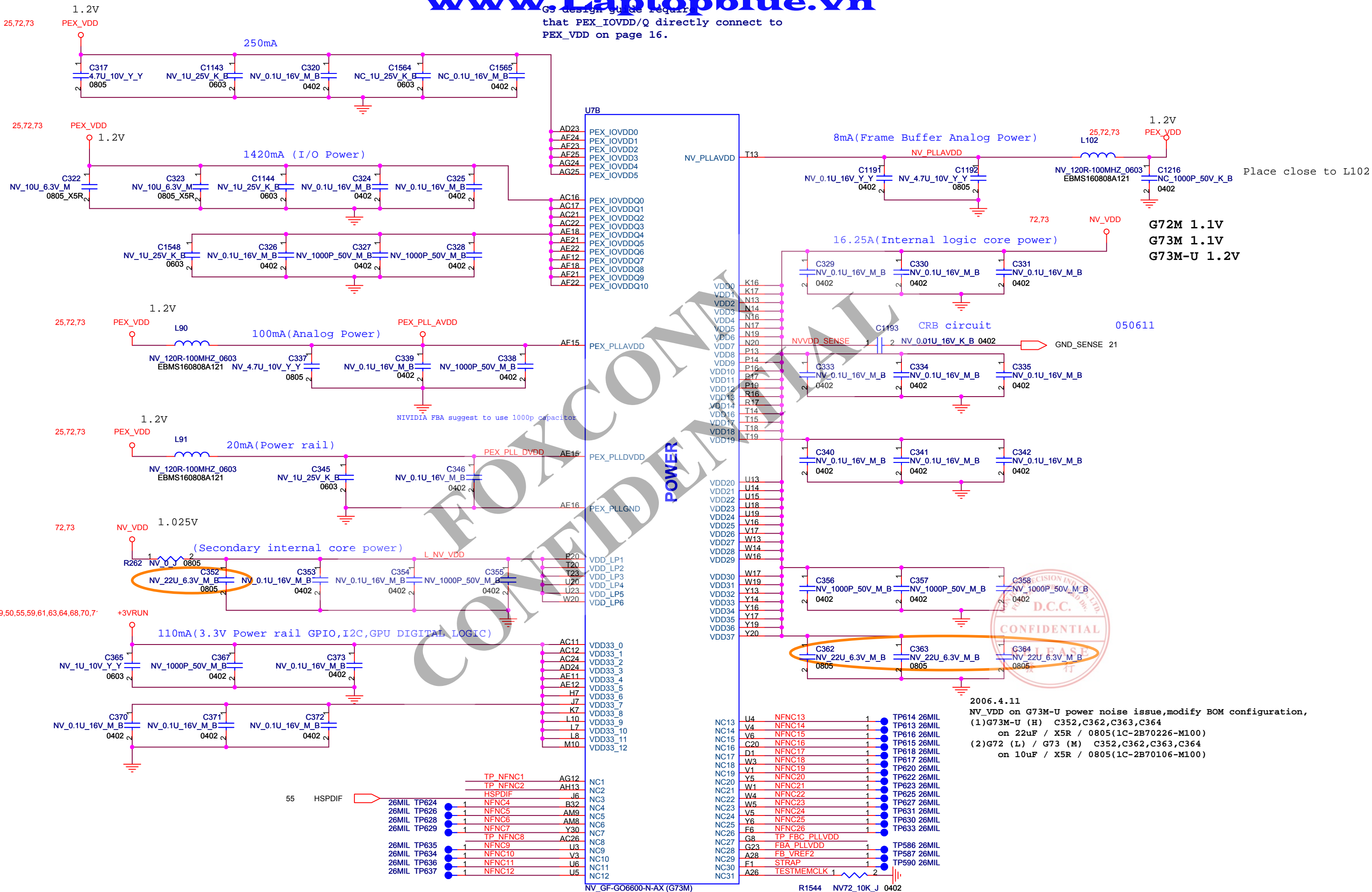
Rev 1.00

Friday, April 14, 2006

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that PEX\_IOVDD/Q directly connect to  
PEX\_VDD on page 16.

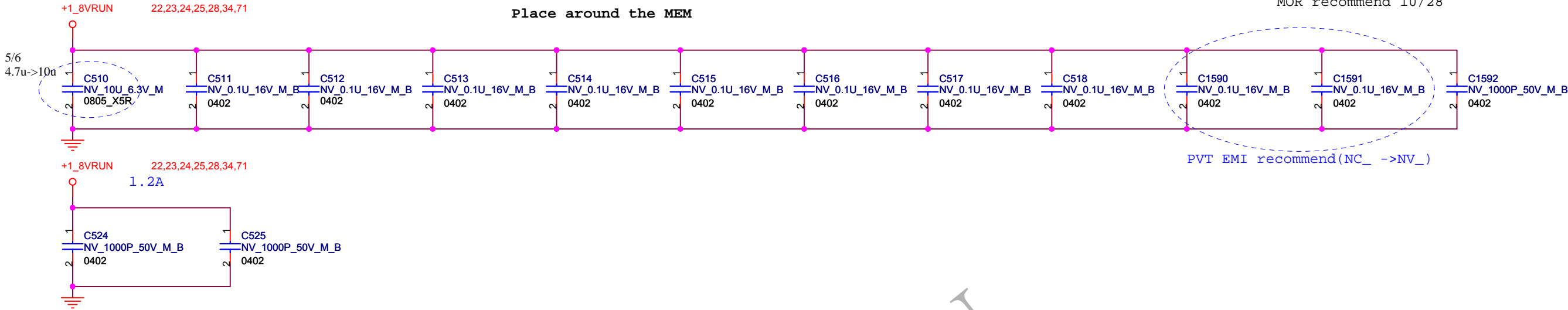


G73M Pin A26-NC  
G72M Pin A26 need stuff R305 10K

Decoupling for Tright MEMORY

Place around the MEM

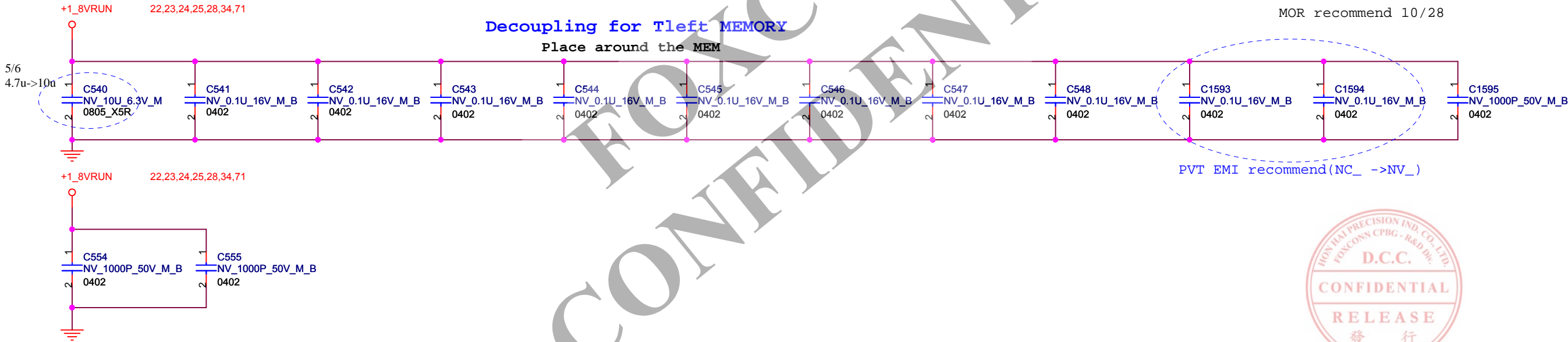
MOR recommend 10/28



Decoupling for Tleft MEMORY

Place around the MEM

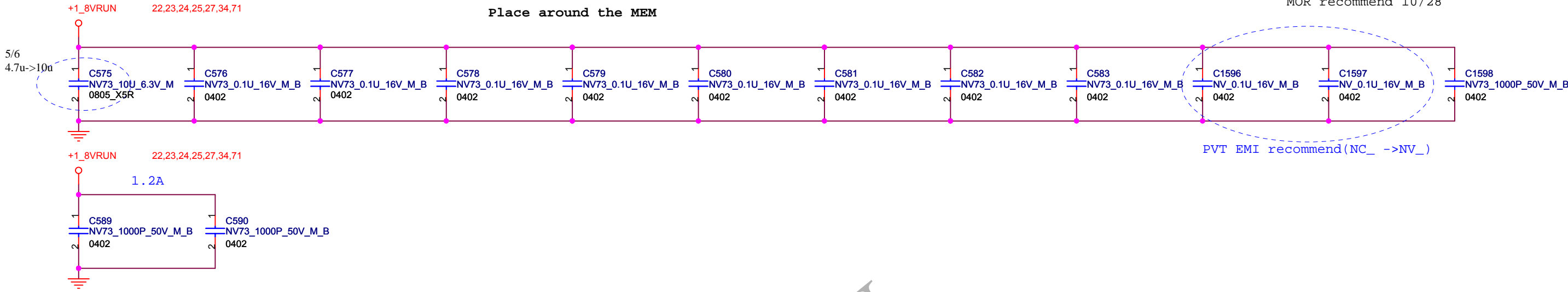
MOR recommend 10/28



Decoupling for Bright MEMORY

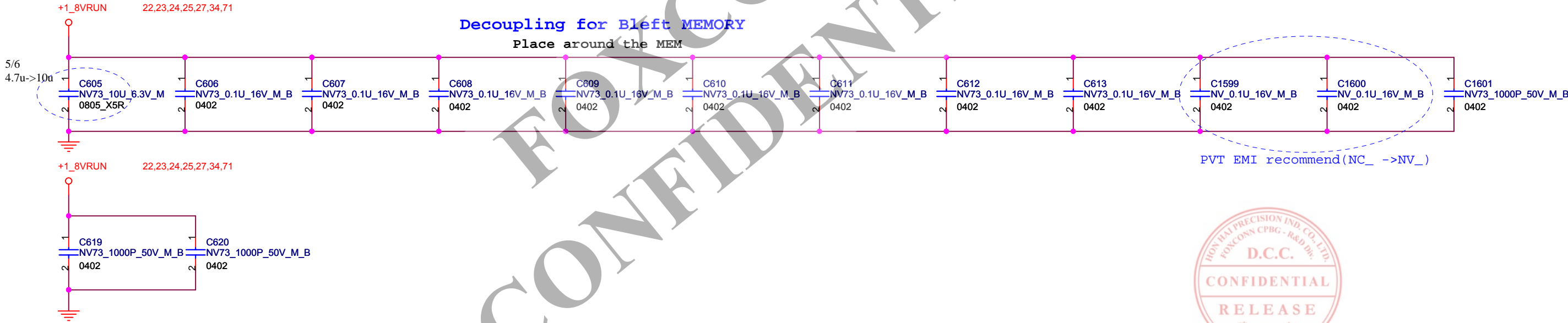
Place around the MEM

MOR recommend 10/28



Decoupling for Bleft MEMORY

Place around the MEM



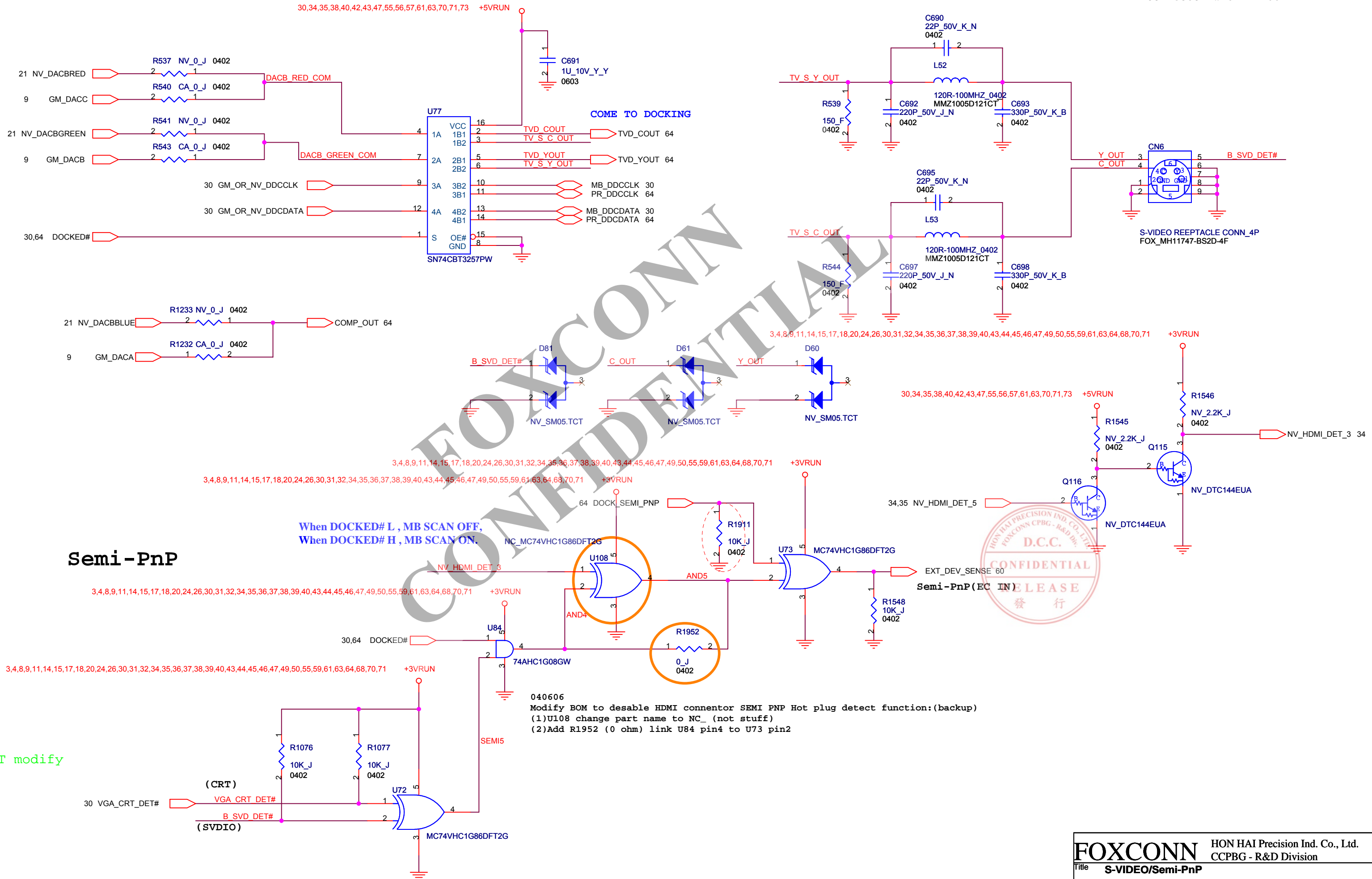


## S-VIDEO ANALOG SWITCH

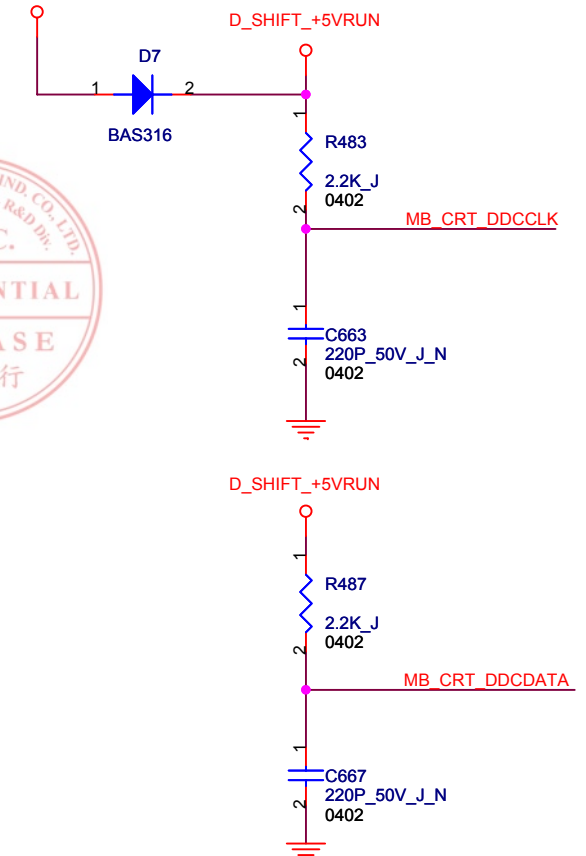
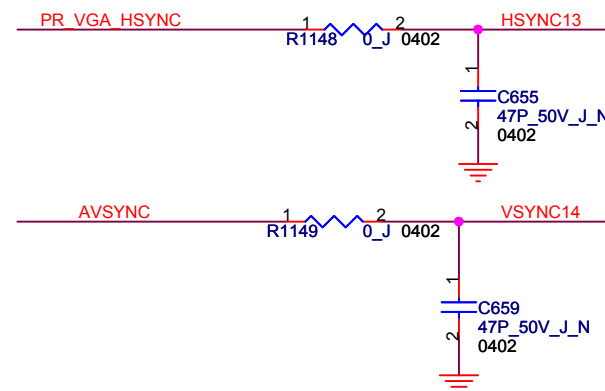
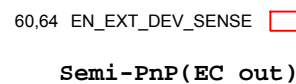
H : S-VIDEO&CVBS  
L : PORT REPLICATOR

## S-VIDEO

These compoent close to S-Video  
connector within 700 mil



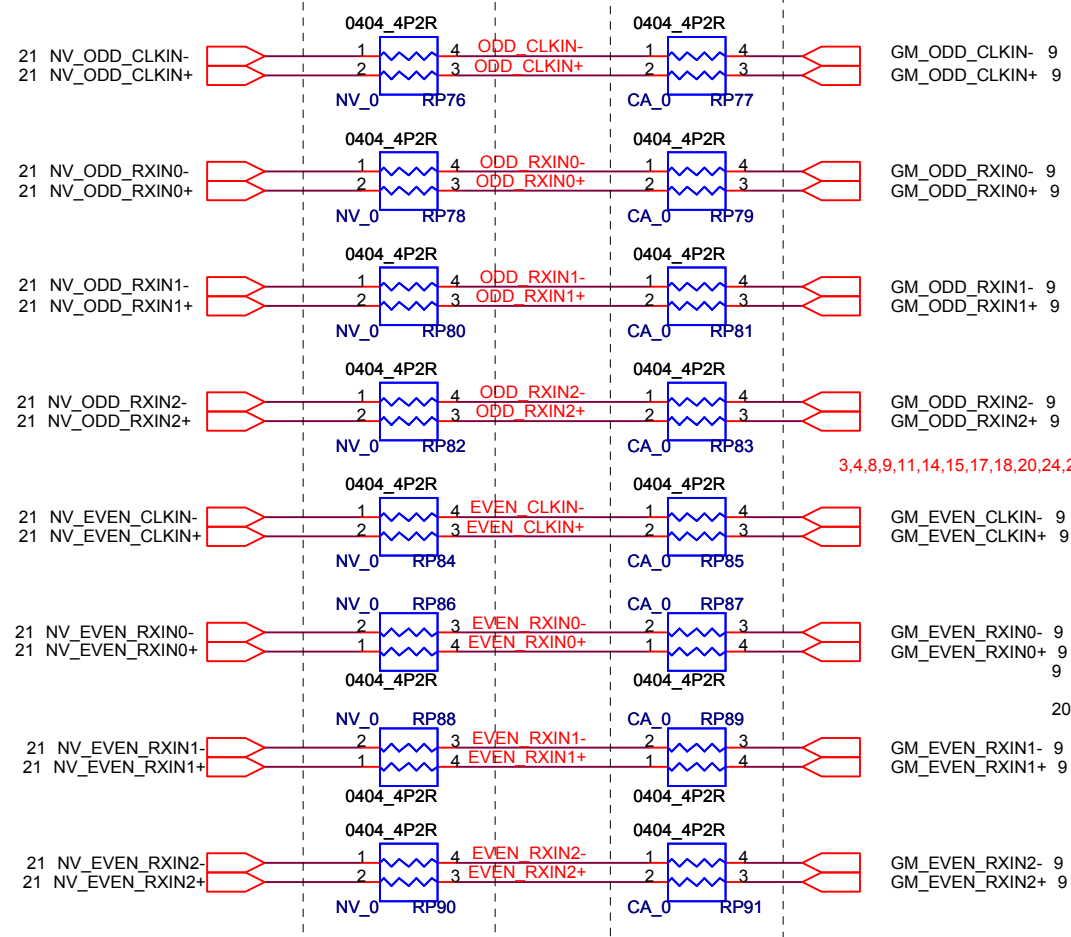
29,34,35,38,40,42,43,47,55,56,57,61,63,70,71,73 +5VRUN



## LVDS

## Group1

## Group2

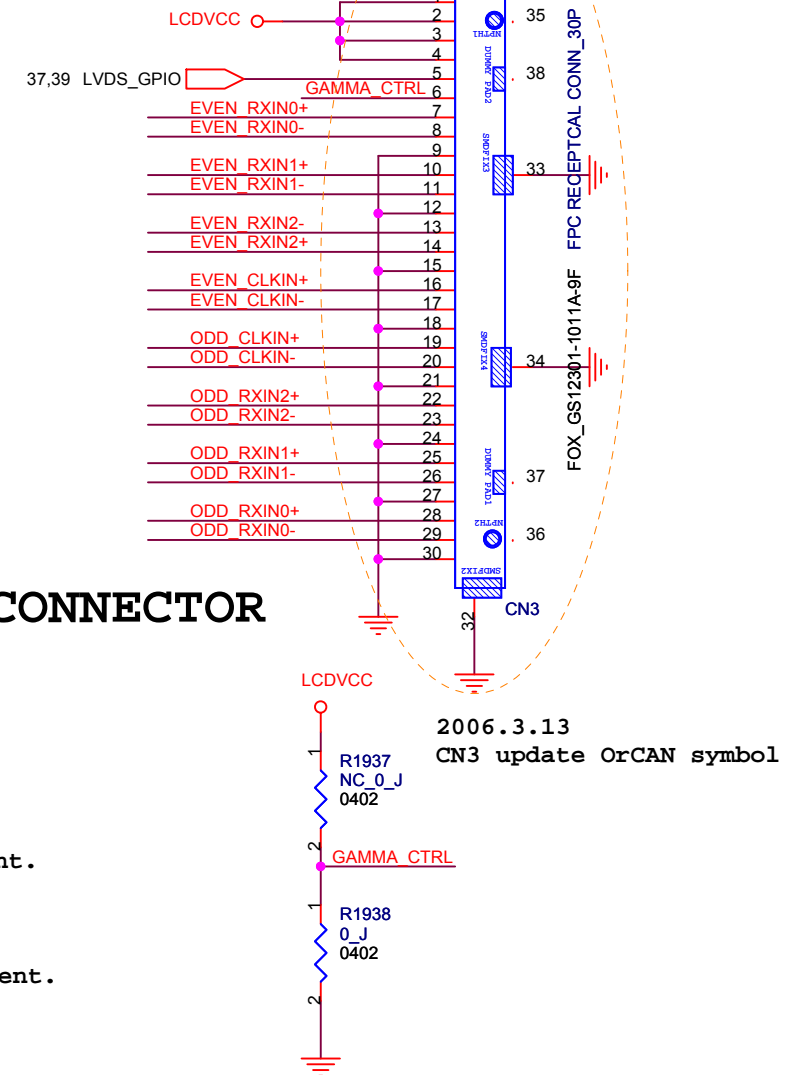


Place C640 and C1558 close to CN49.

U106,U15,U16 can use ON (MC74VHC1G08DFT2G)  
H.H. PN:14-MC74VHC-1G04

## INVERTER CONNECTOR

## LVDS CONNECTOR



2006.3.13  
CN3 update OrCAN symbol

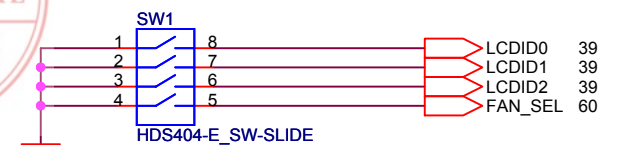
9/7 change for customer requirement.

9/7 change for customer requirement.

Place C650 close to CN3



PANEL ID



FAN\_SEL:  
H: Foxconn FAN  
L: MOR cooling unit

Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP
Device Name	LP171WP7-TLA1	LP171WX2-A4K3	LQ170M1LA04
Panel ID Check[3...0]	0001	0010	0100

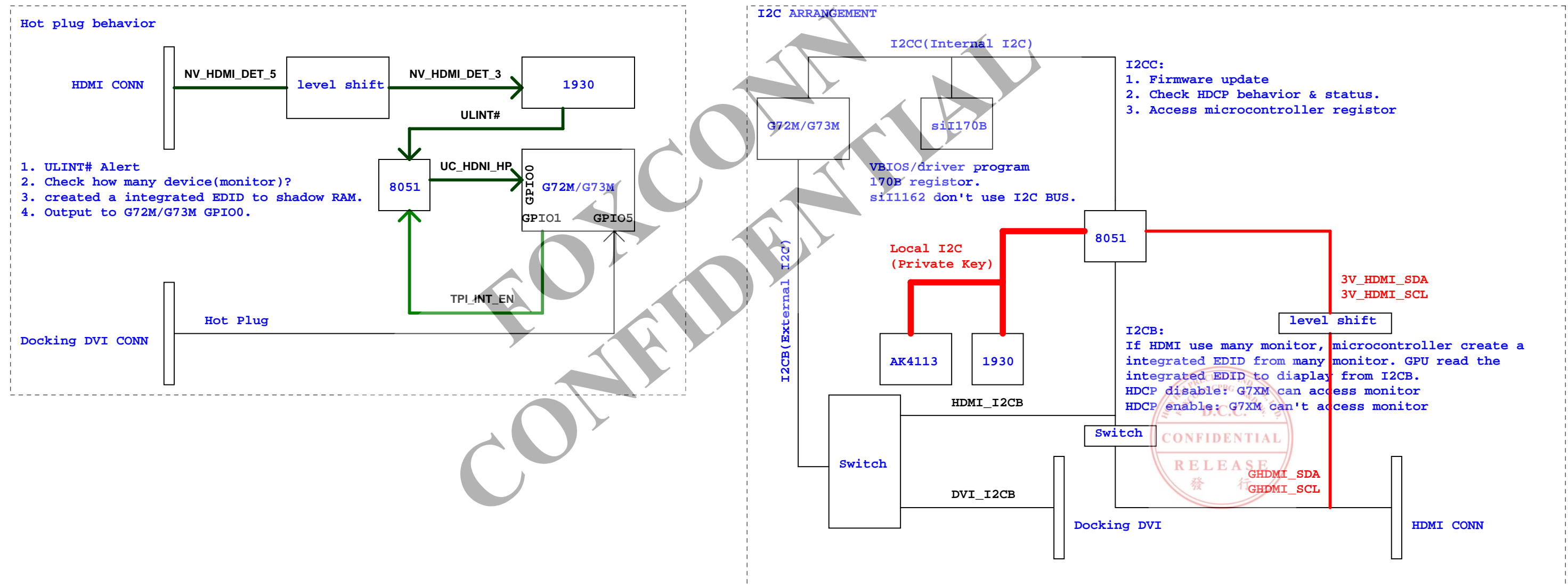
FOXCONN HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

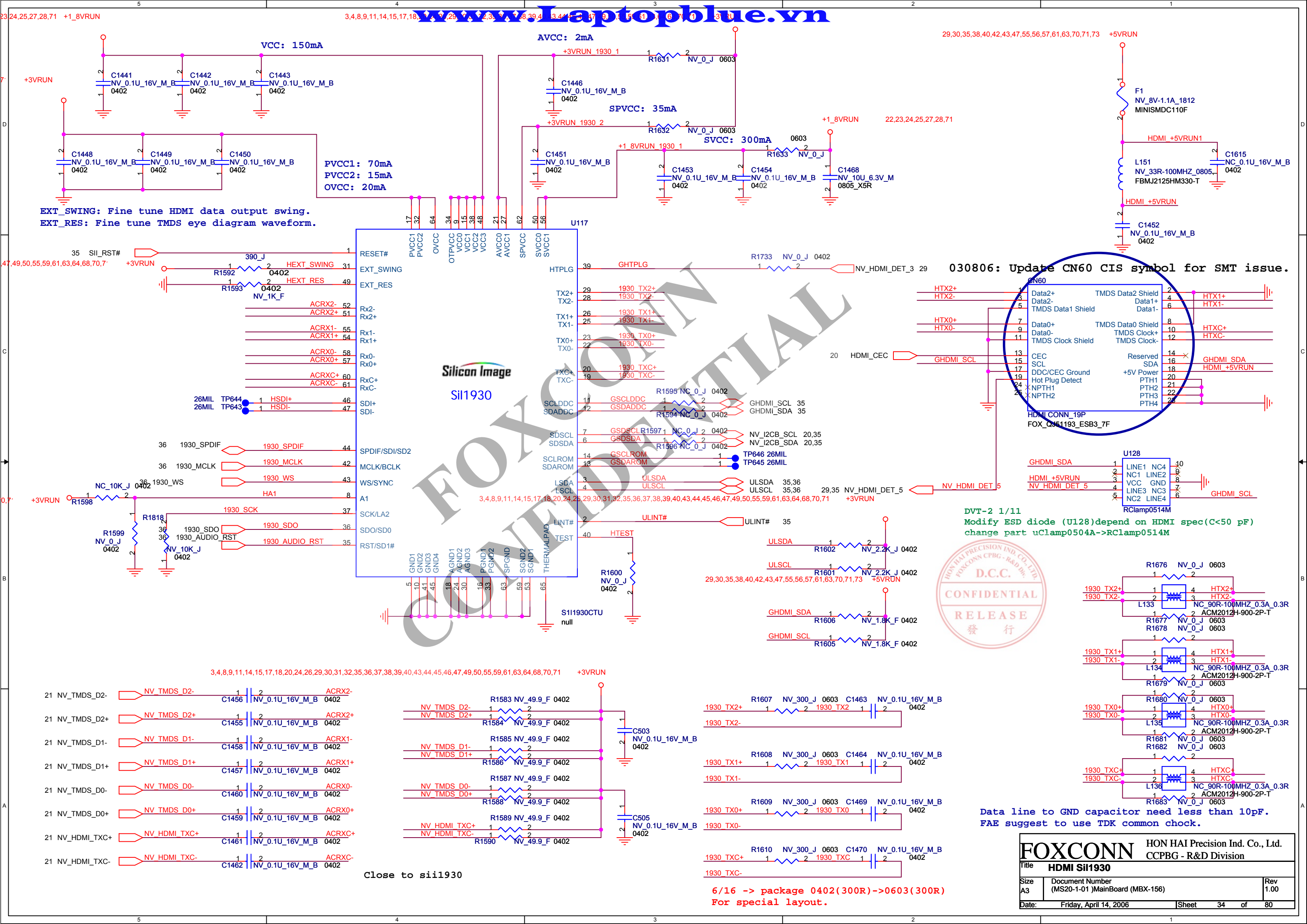
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Size	Document Number		
A3	(MS20-1-01) MainBoard (MBX-156)		
Date:	Friday, April 14, 2006	Sheet	31 of 80



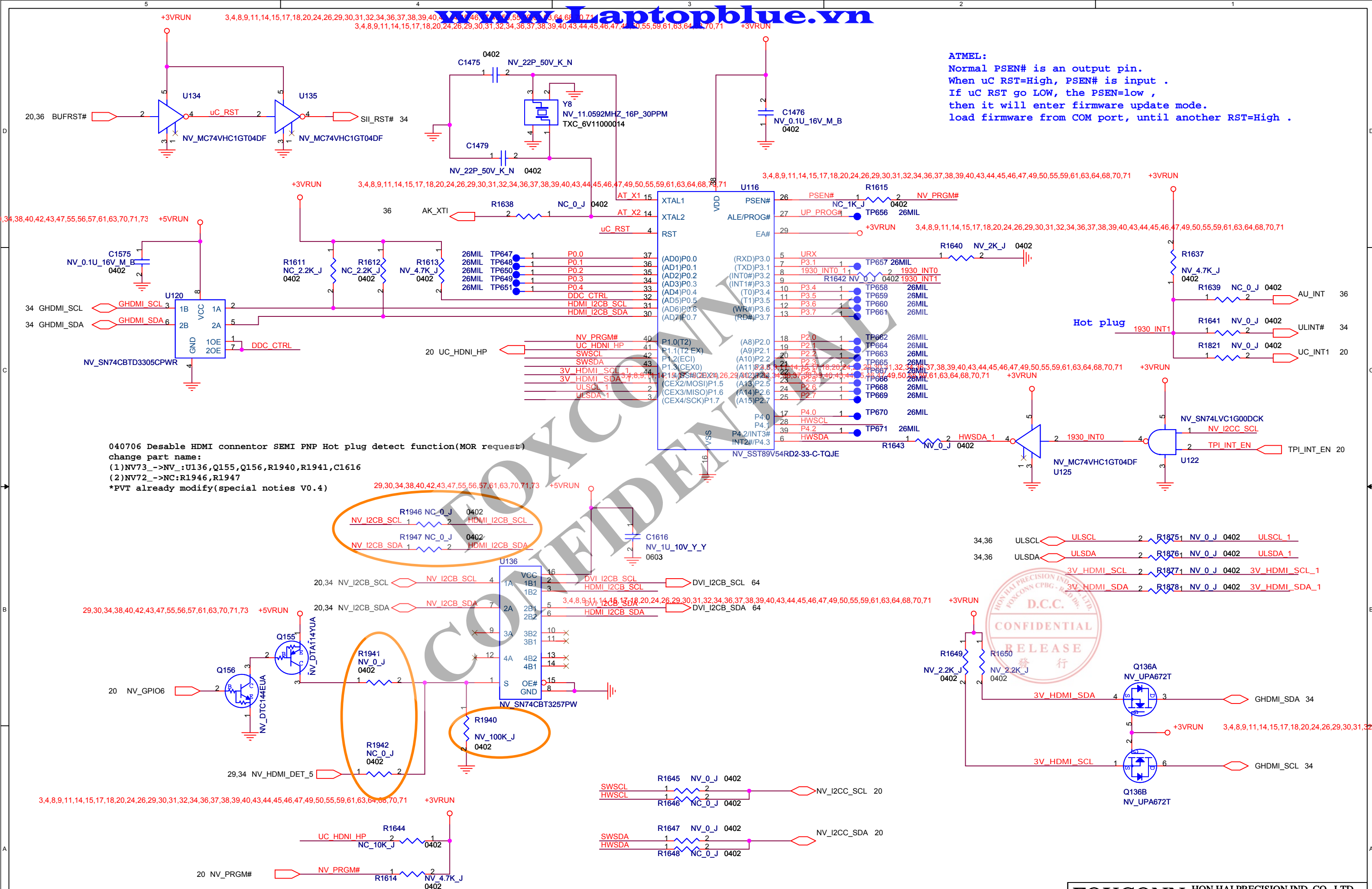


# Hot plug behavior & I2C ARRANGEMENT block diagram



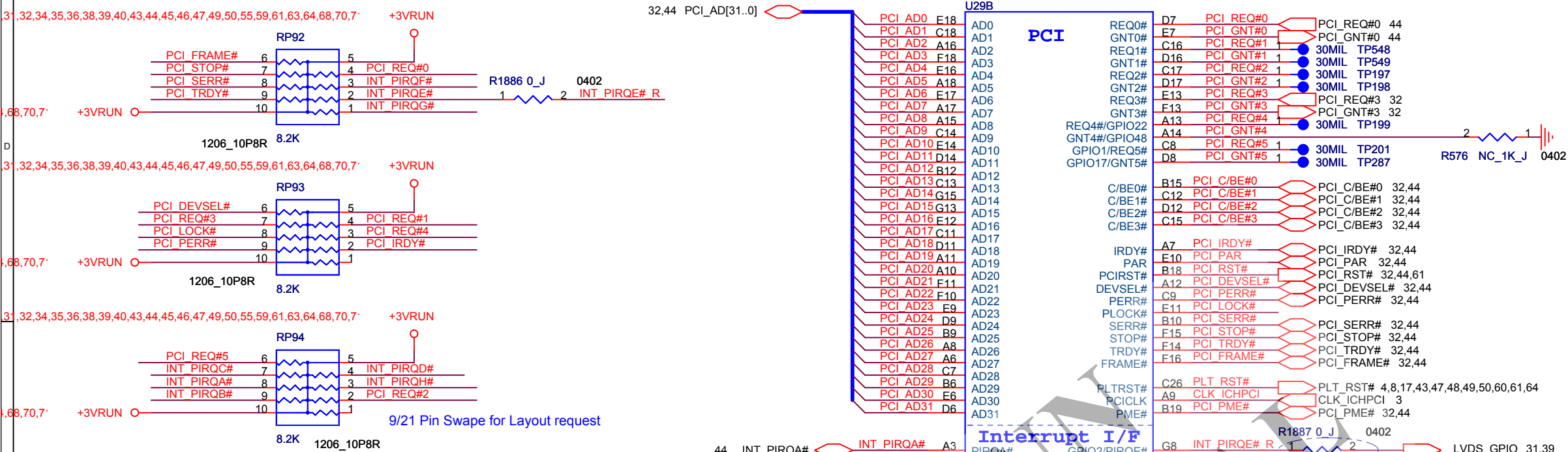








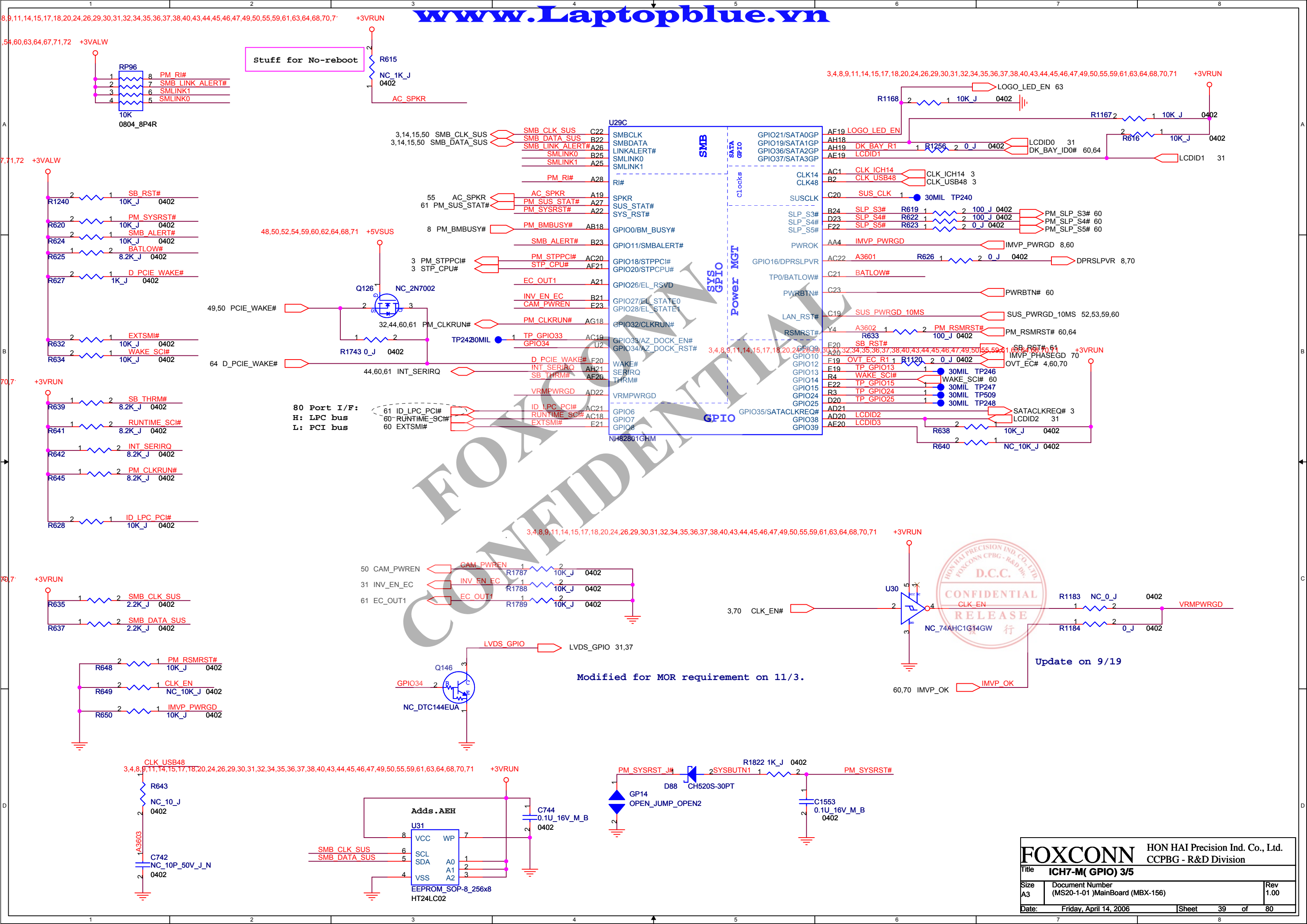
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Title <b><i>MINI-PCI CONN.</i></b>			
Size A3	Document Number (MS20-1-01 )MainBoard (MBX-156)		Rev 1.00
Date:	Friday, April 14, 2006	Sheet	36 of 80



Place within 500 mils of ICH and don't routing next to high speed signals



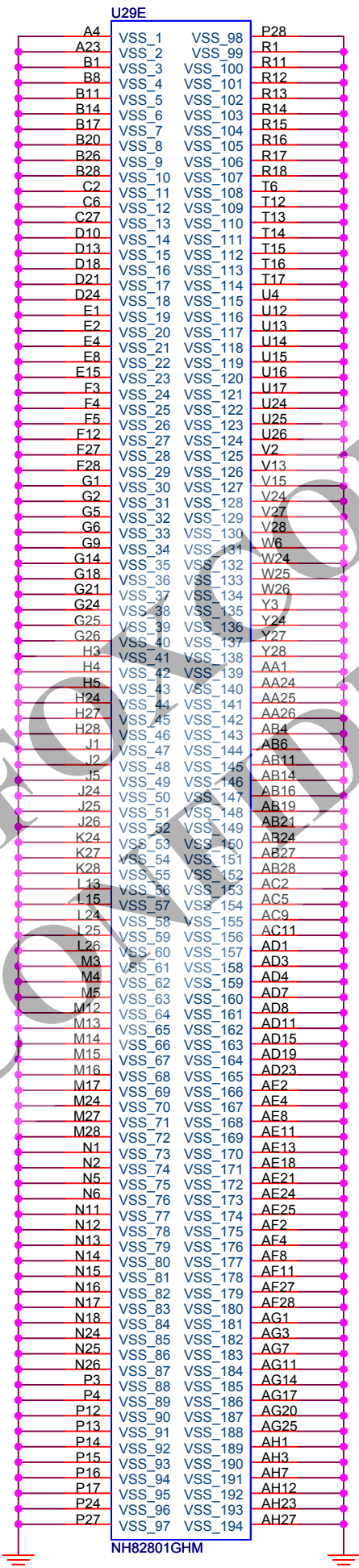


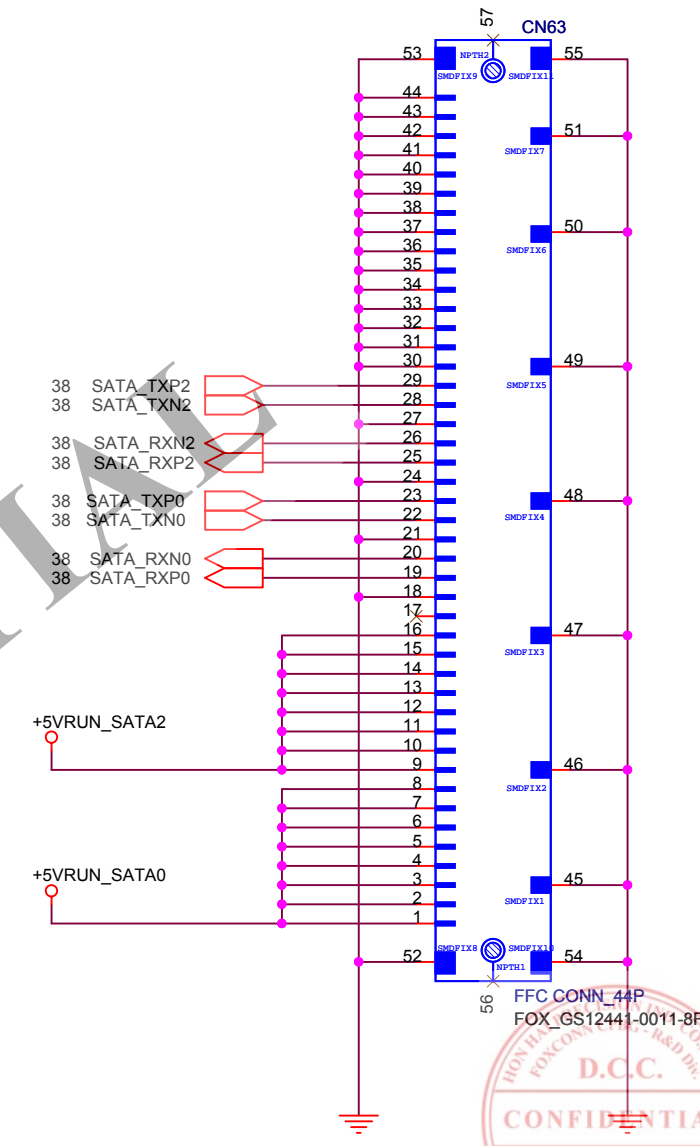
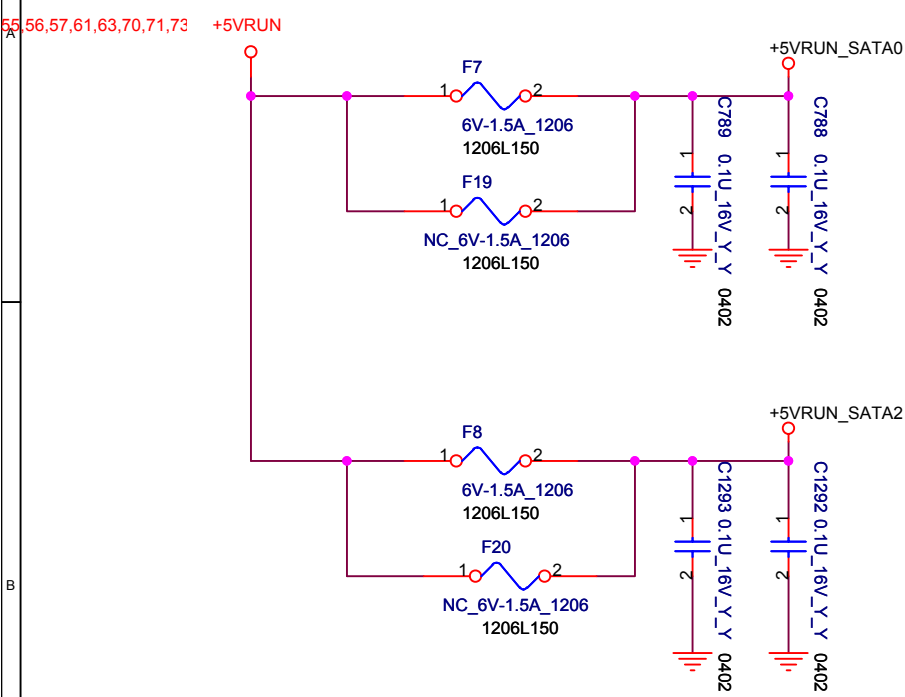


Place within 100  
mils of ICH on the  
bottom side or 140  
mils on the top  
near pin AG9.

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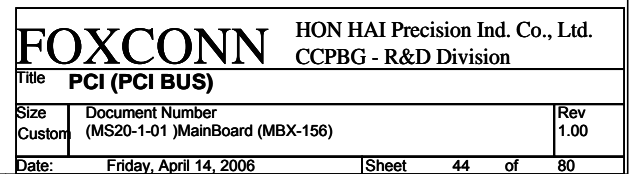


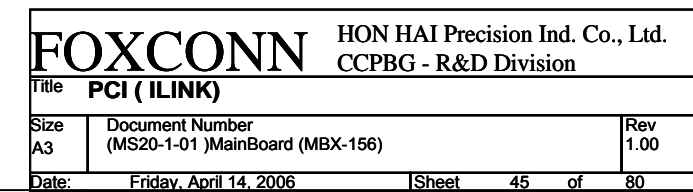


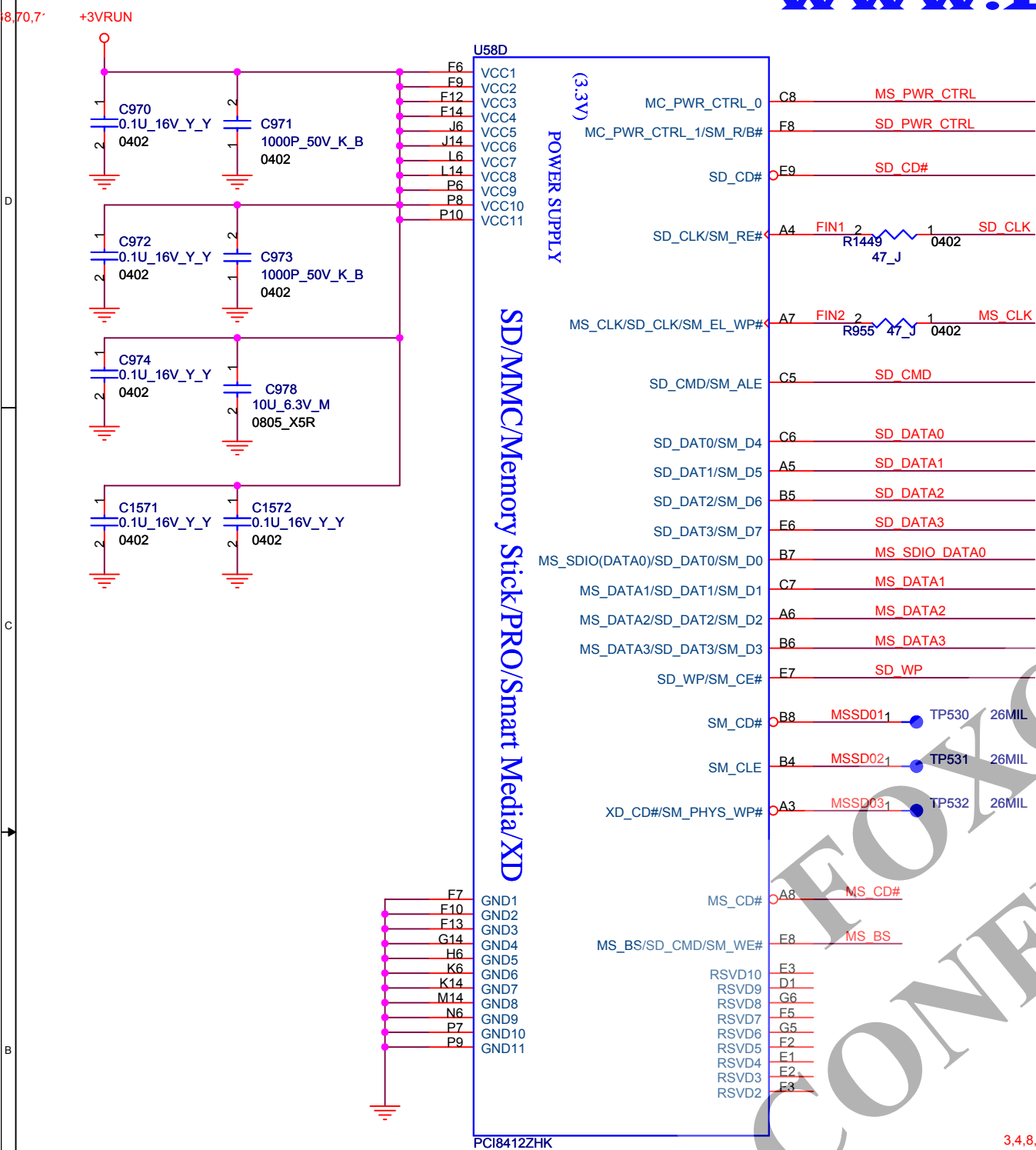






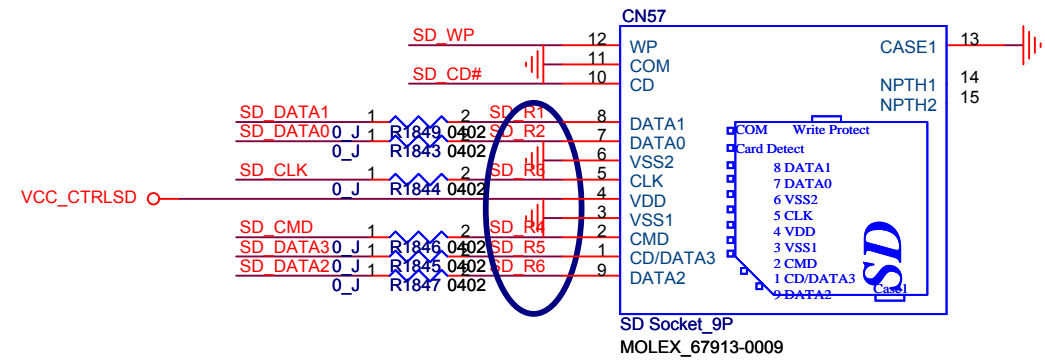






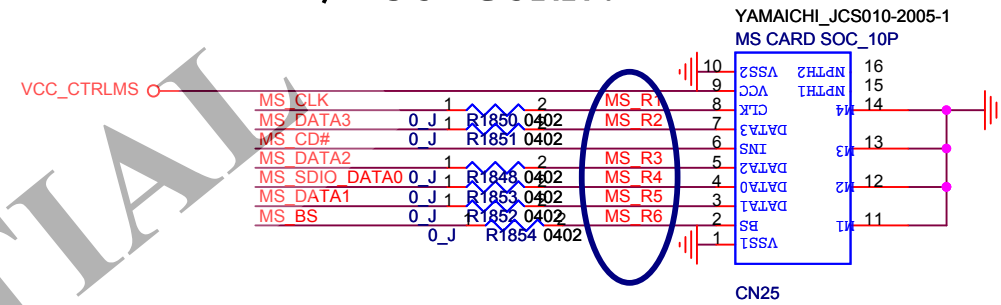
## SD CONN.

WAIT FOR CHANGE FOXCONN CONNECTOR

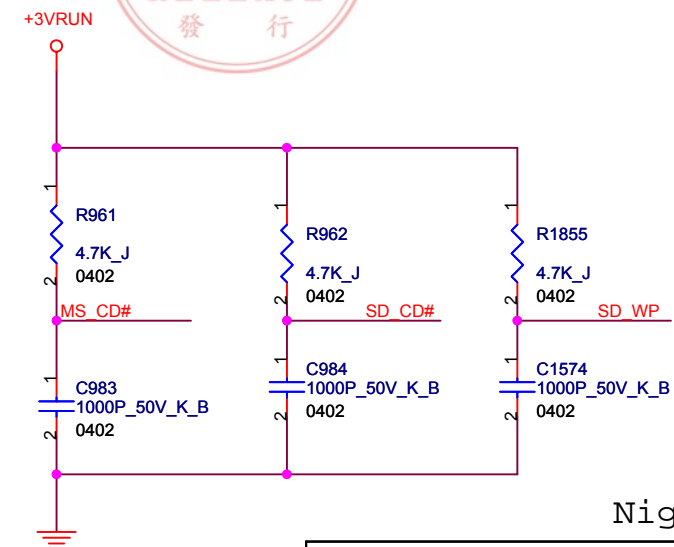
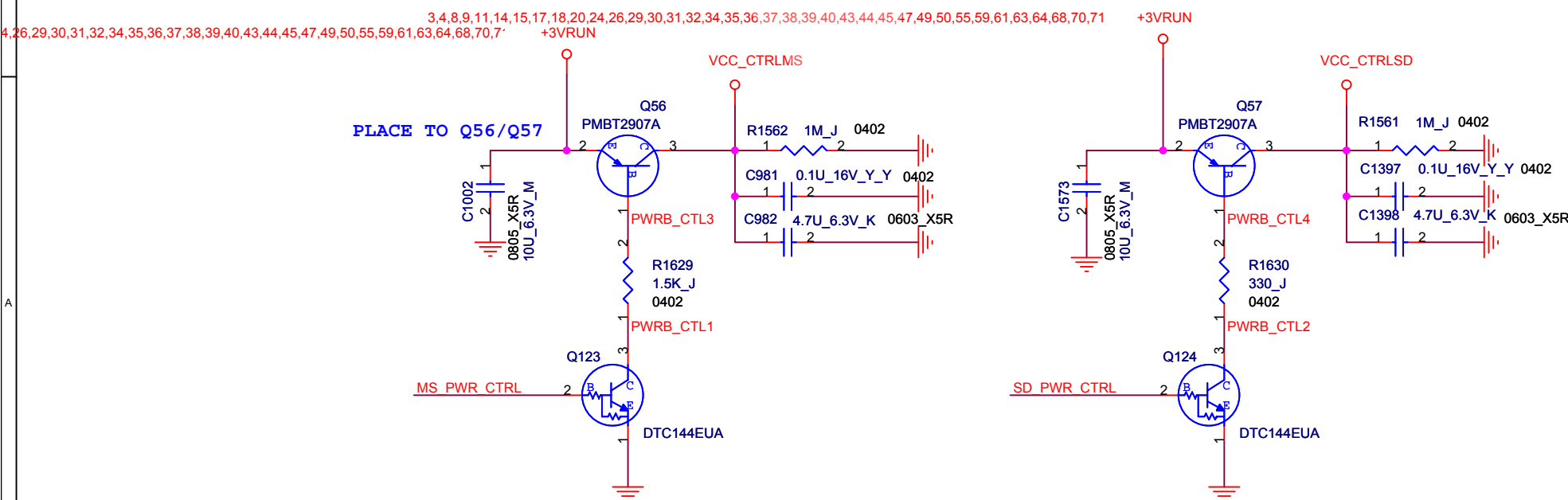
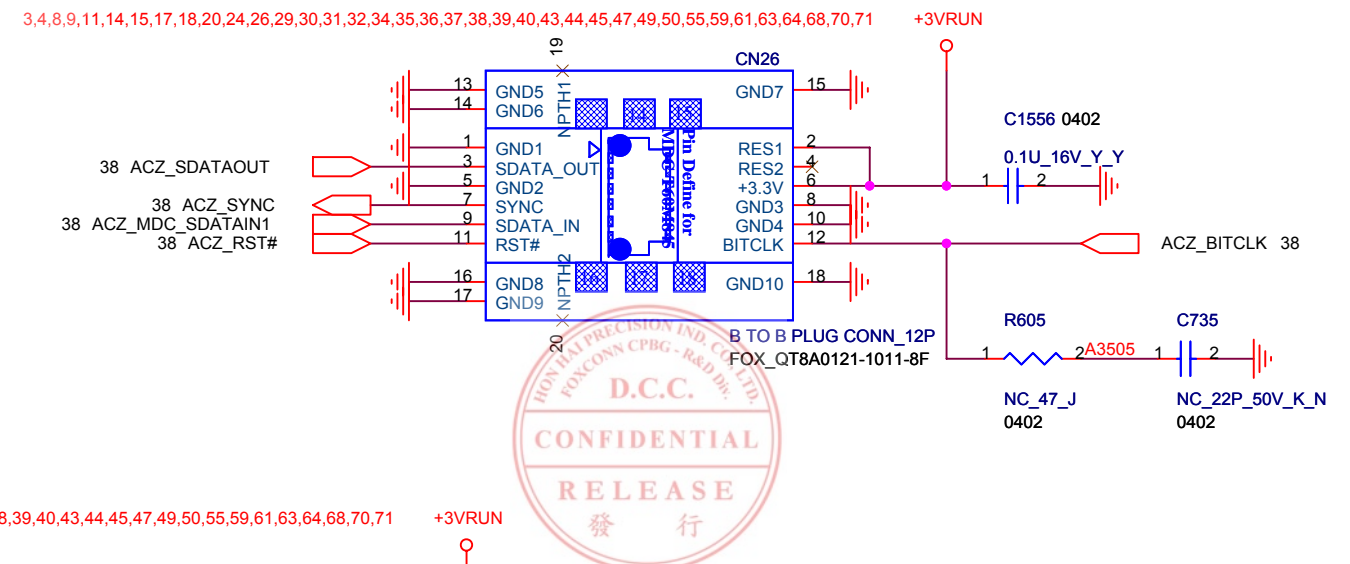


030306: MS\_R and SD\_R net name changed each other

## MS STD/DUO CONN.

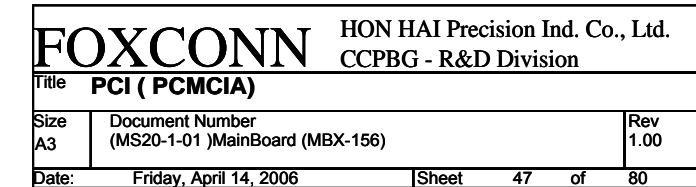


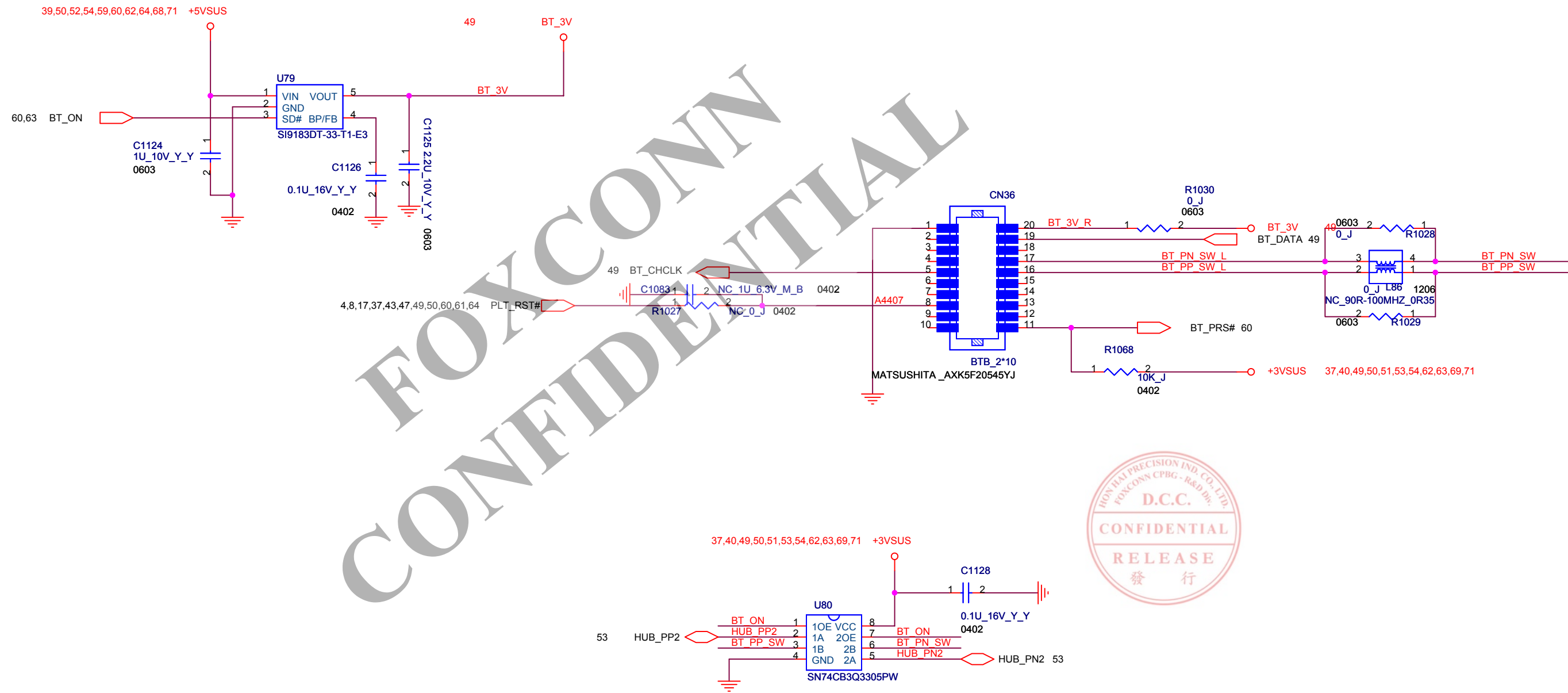
## MDC CONN.

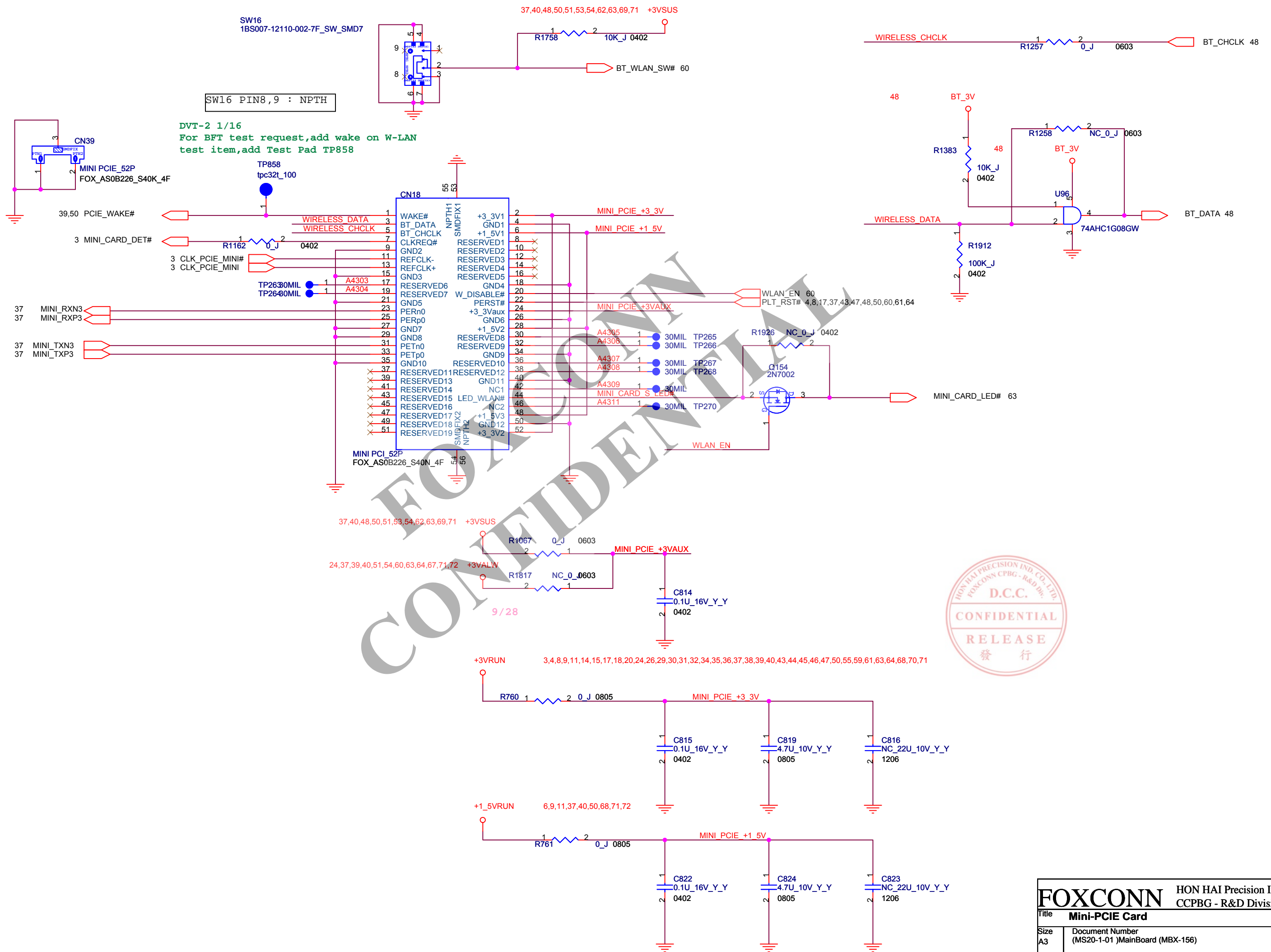


Nigel Hu



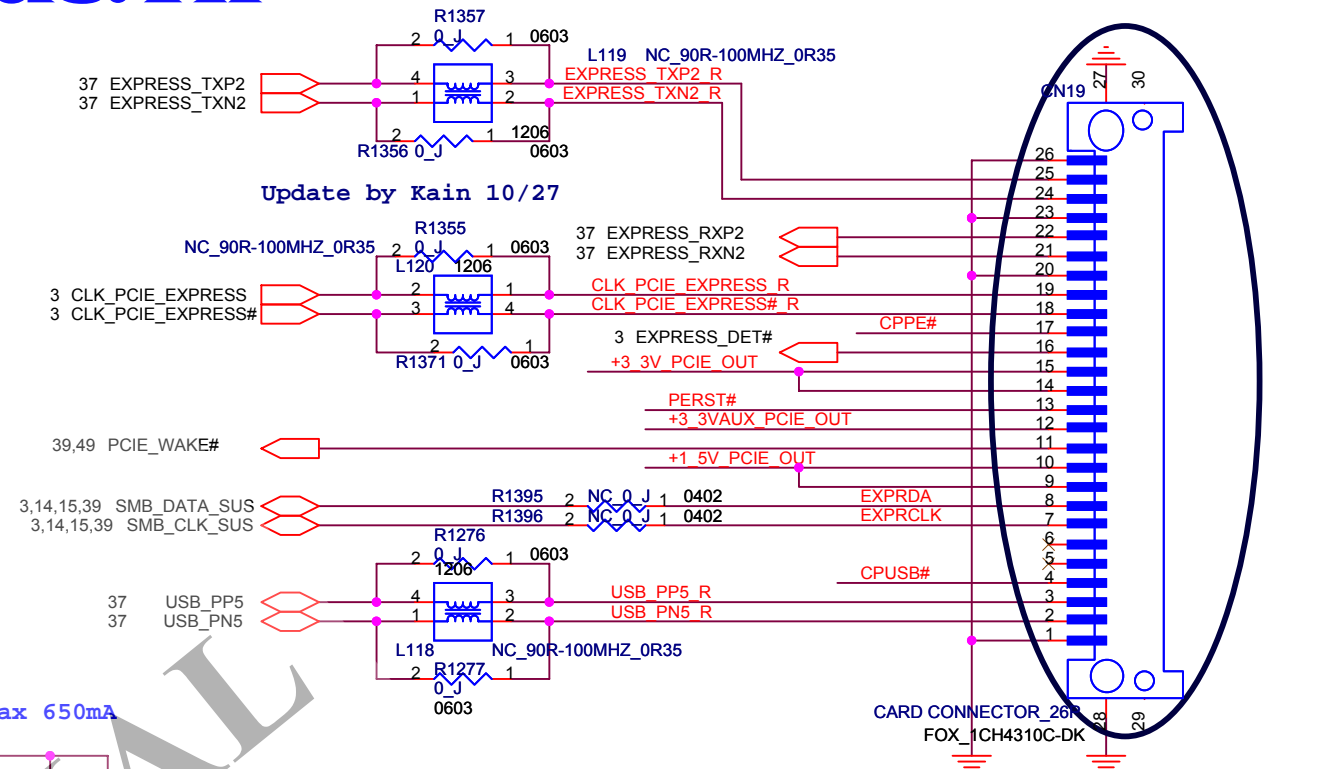
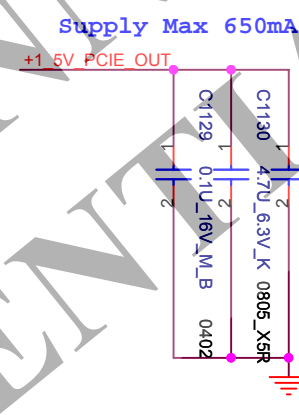
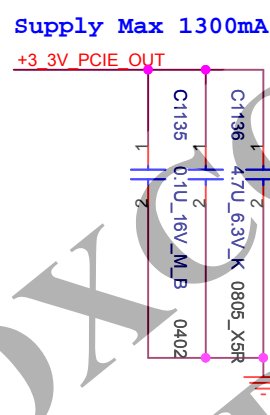
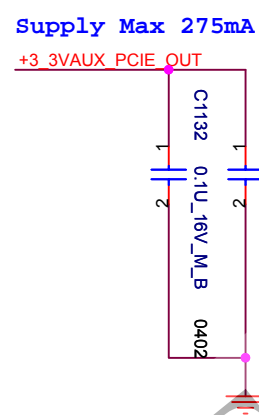
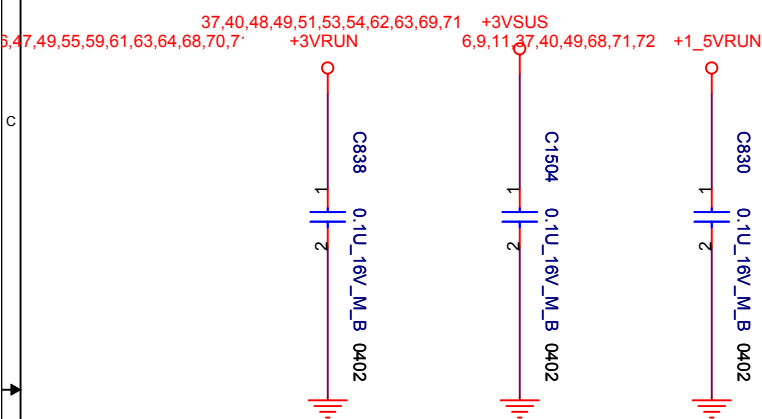
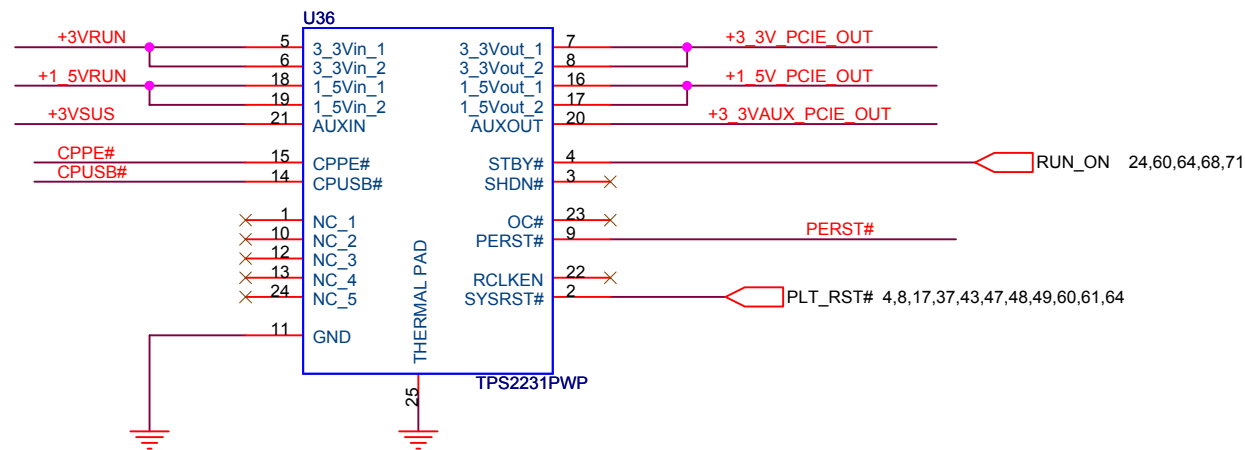




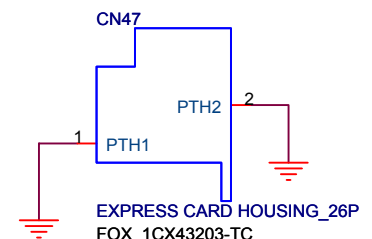
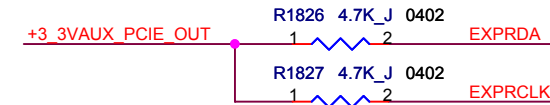




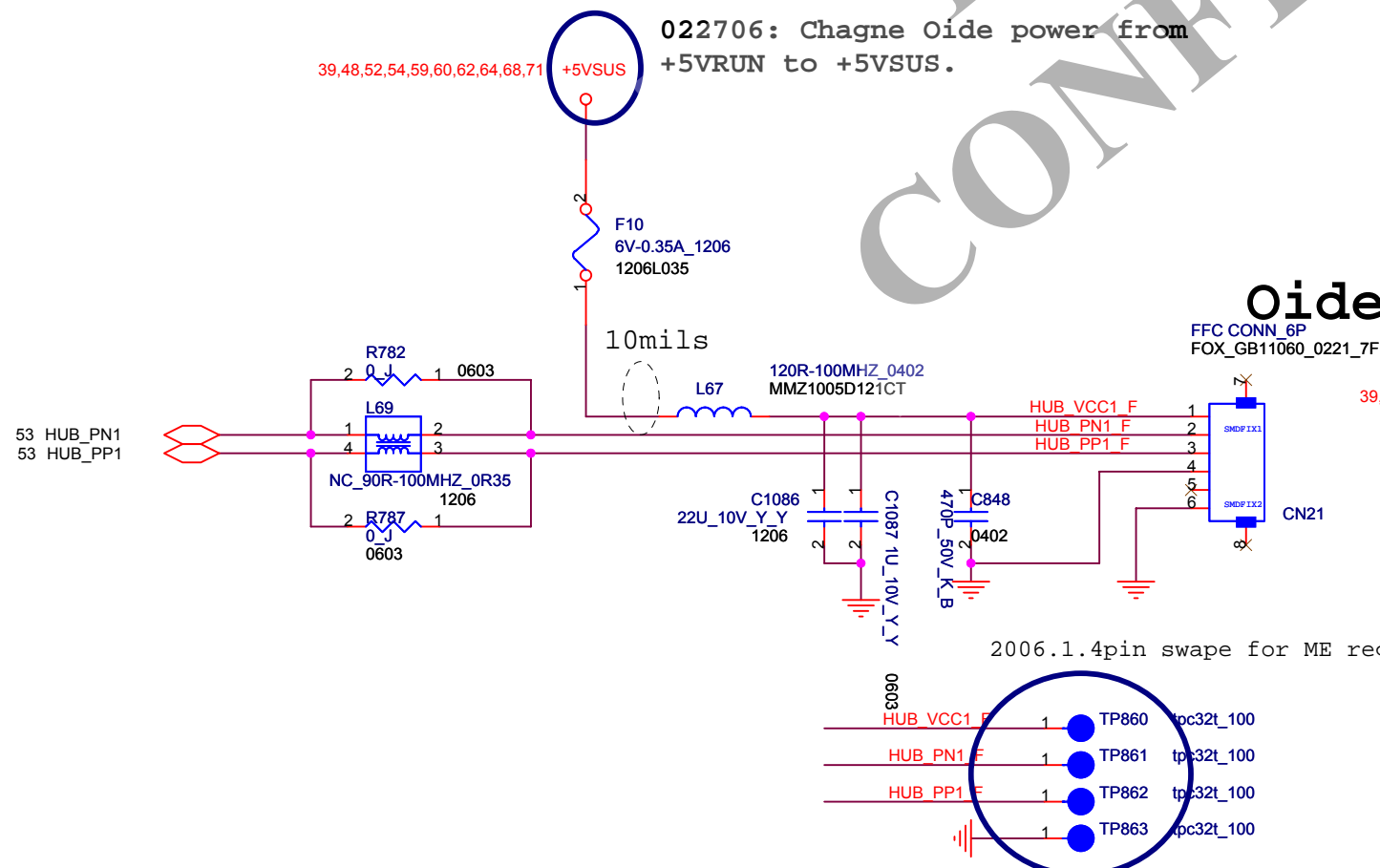
VOLTAGE INPUTS(I)			LOGIC INPUTS			VOLTAGE OUTPUTS(II)			MODE(III)
AUXIN	3.3VIN	1.5VIN	SRDN	STBT	CP#	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted



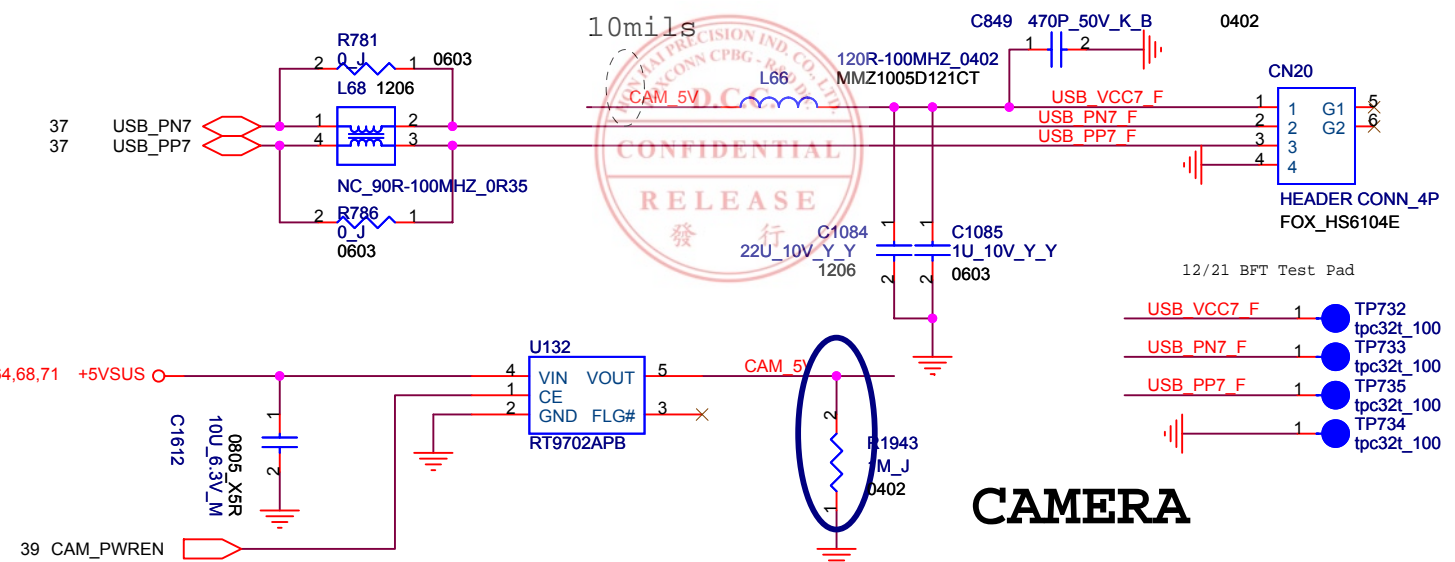
030706: Change CN19 parts for SMT issue.



022706: Chagne Oide power from +5VSRUN to +5VSUS.



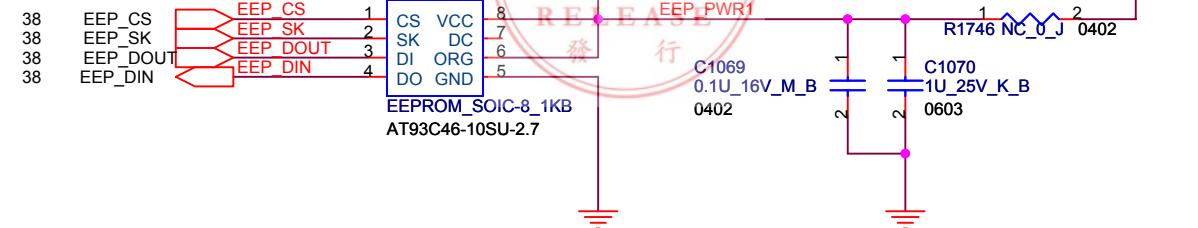
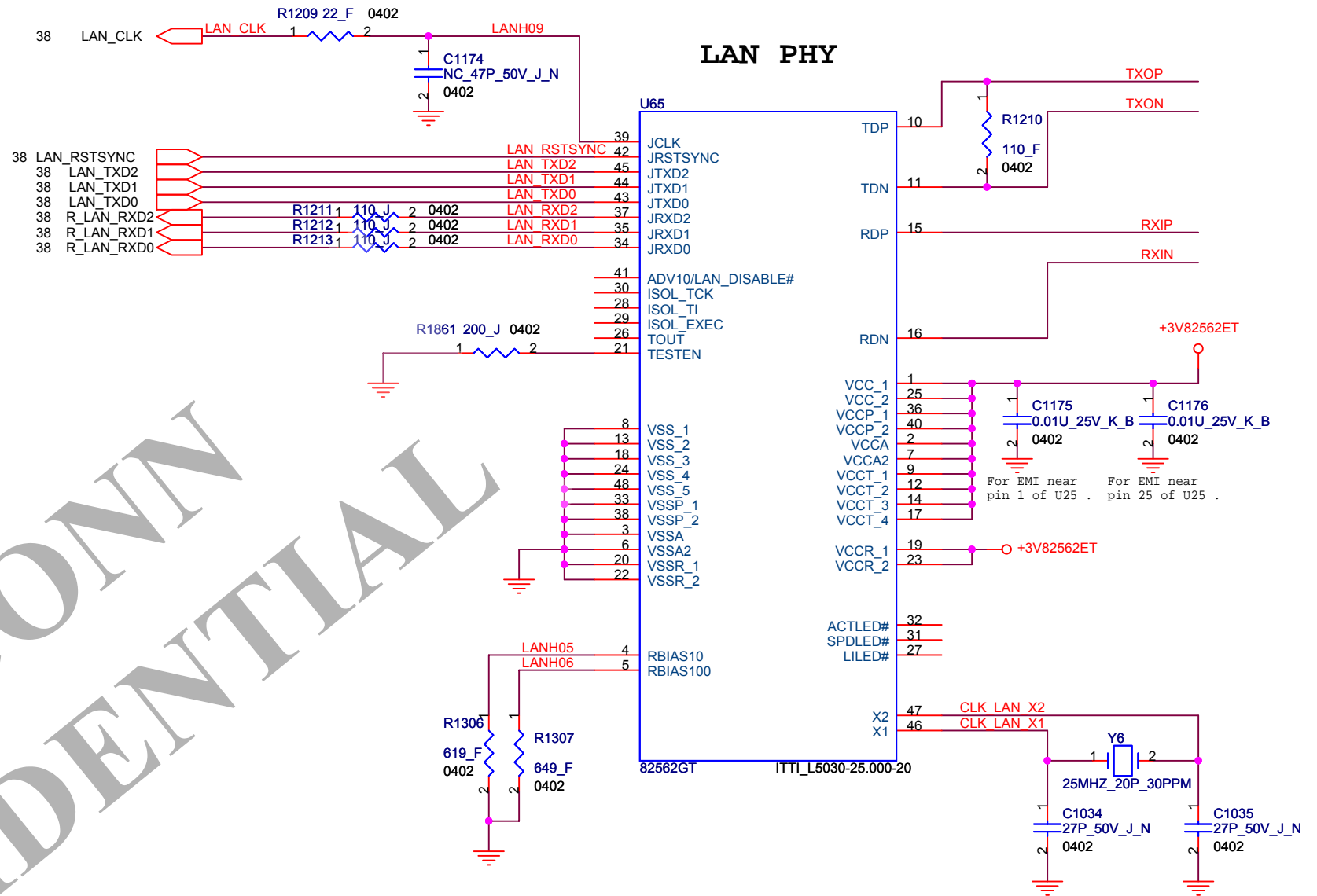
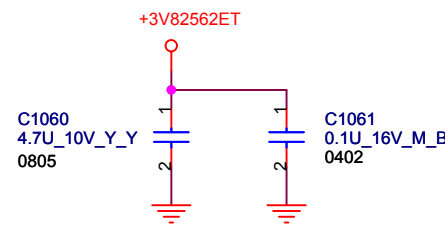
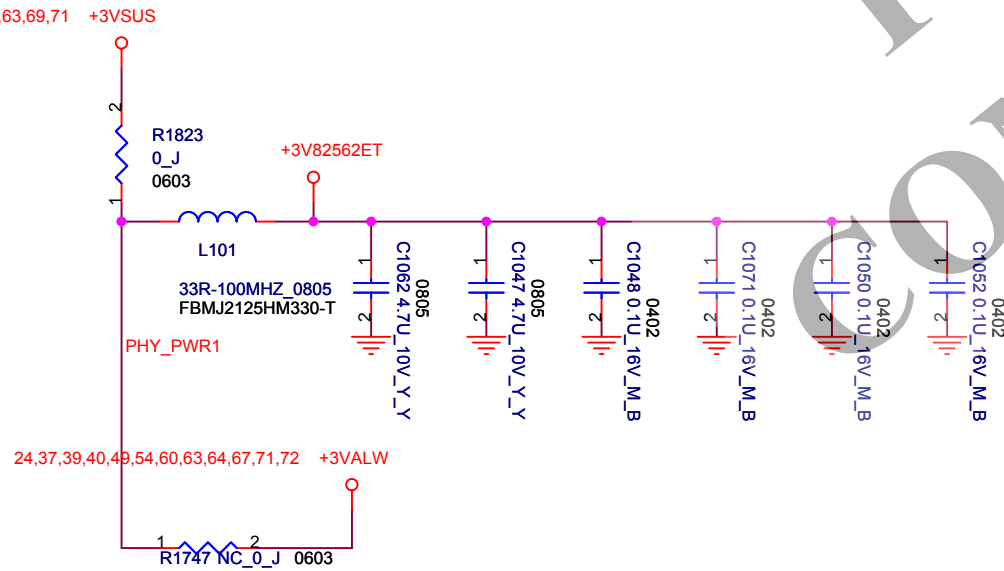
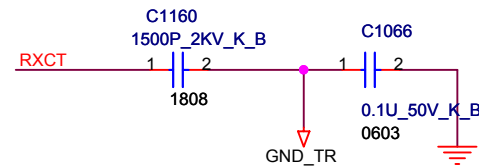
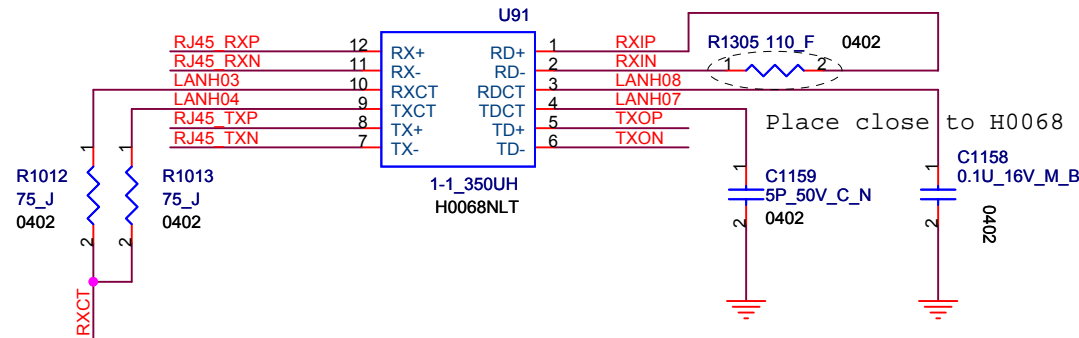
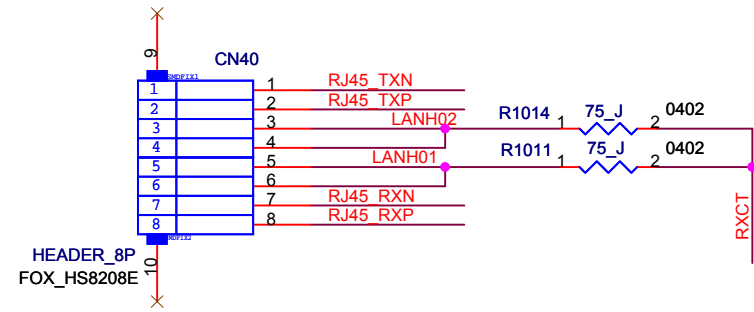
2006.1.4pin swape for ME request



022706: Add discharge resistor for camera.

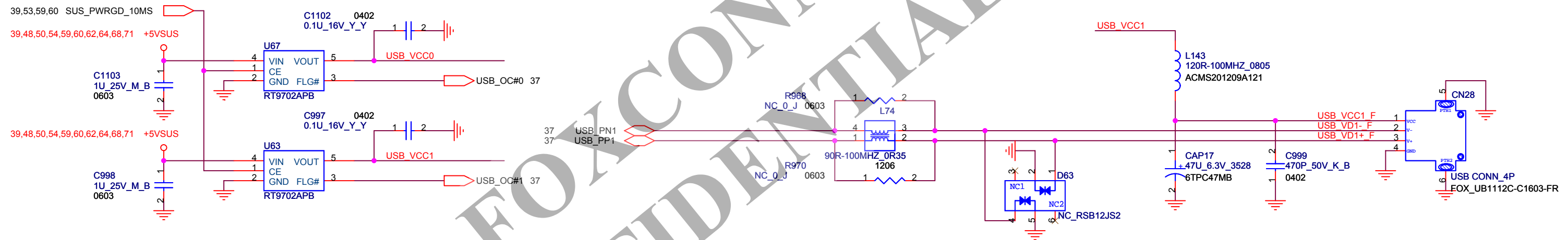
12/21 BFT Test Pad

RJ45_TXN	1	TP736
RJ45_TXP	1	TP738
LANH02	1	tpc32t_100
LANH01	1	TP739
RJ45_RXN	1	tpc32t_100
RJ45_RXP	1	TP740
		TP737
		tpc32t_100
		TP741
		tpc32t_100



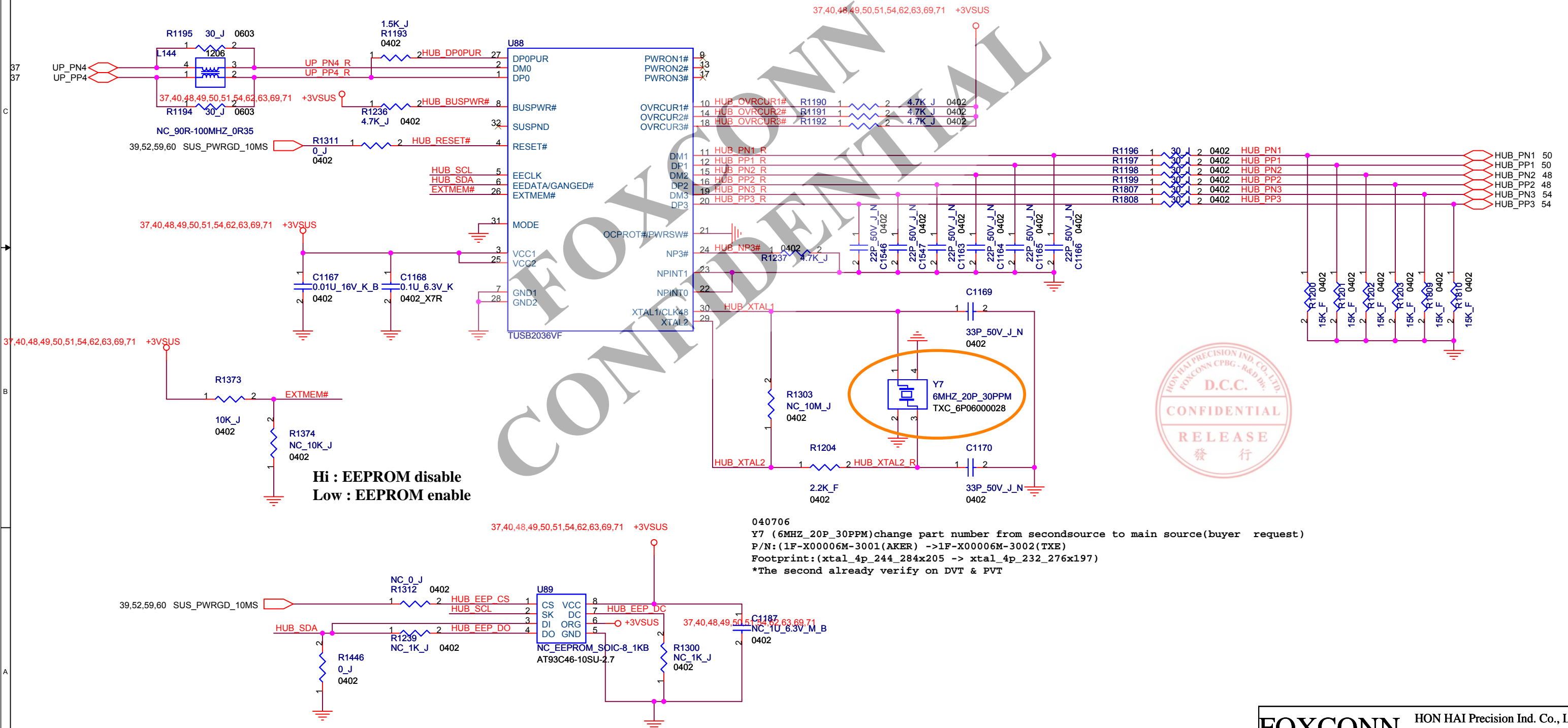
Default for S3 waking up event ,  
backup for S4 waking up event

## USB CONN X 2

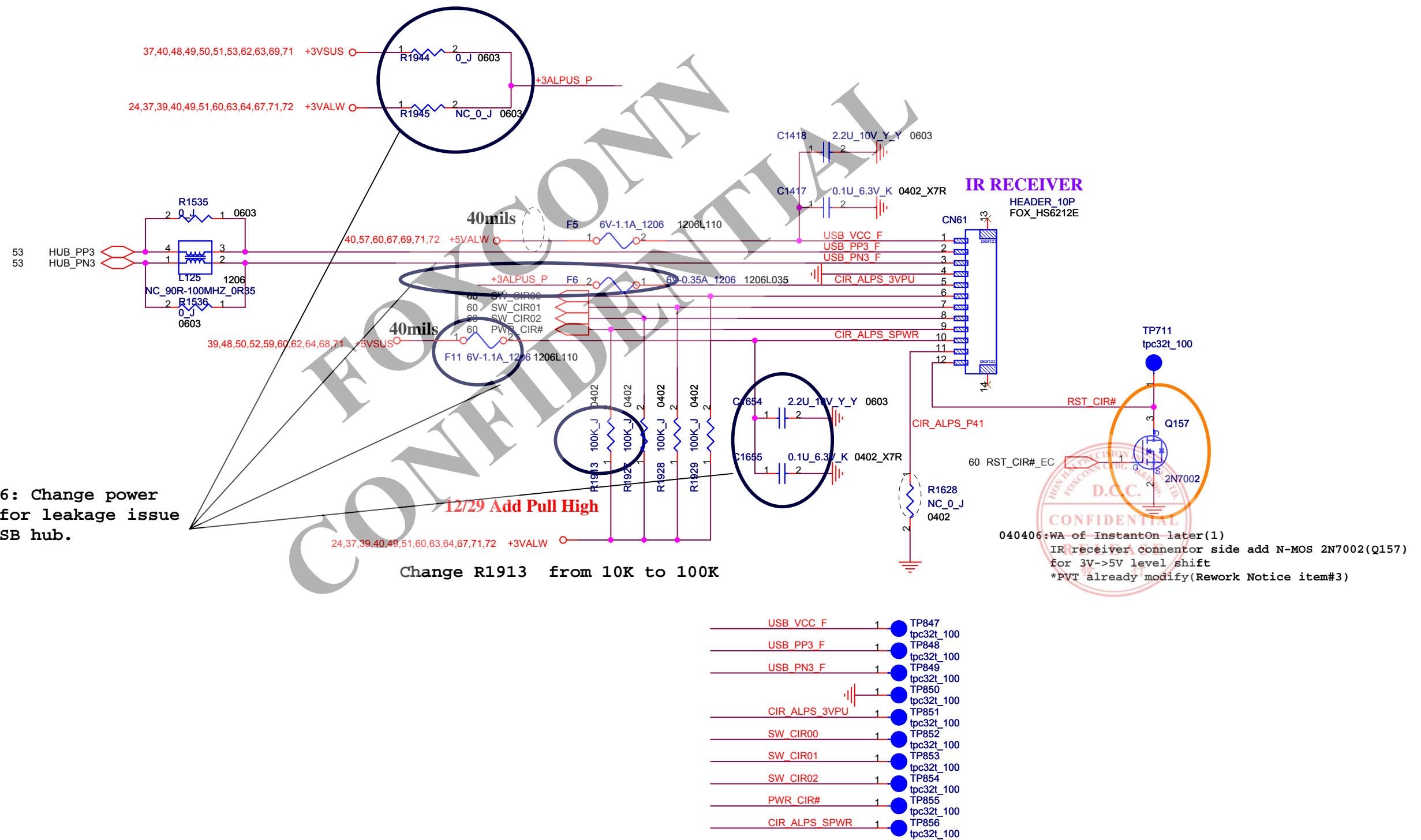


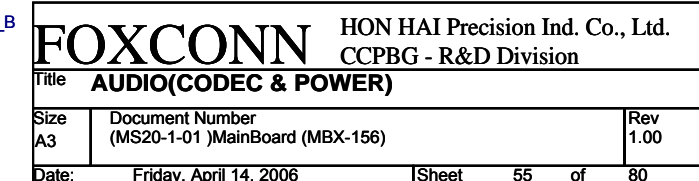


Application design in datasheet 27 ohm;  
but 30ohm is also in range of USB Spec.

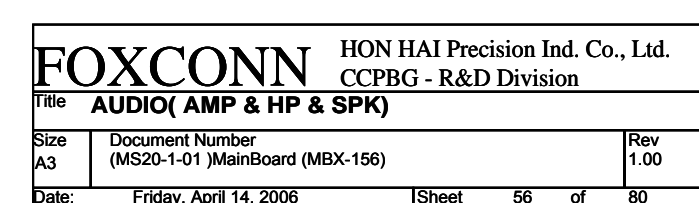


030106: Change power  
plan for leakage issue  
of USB hub.





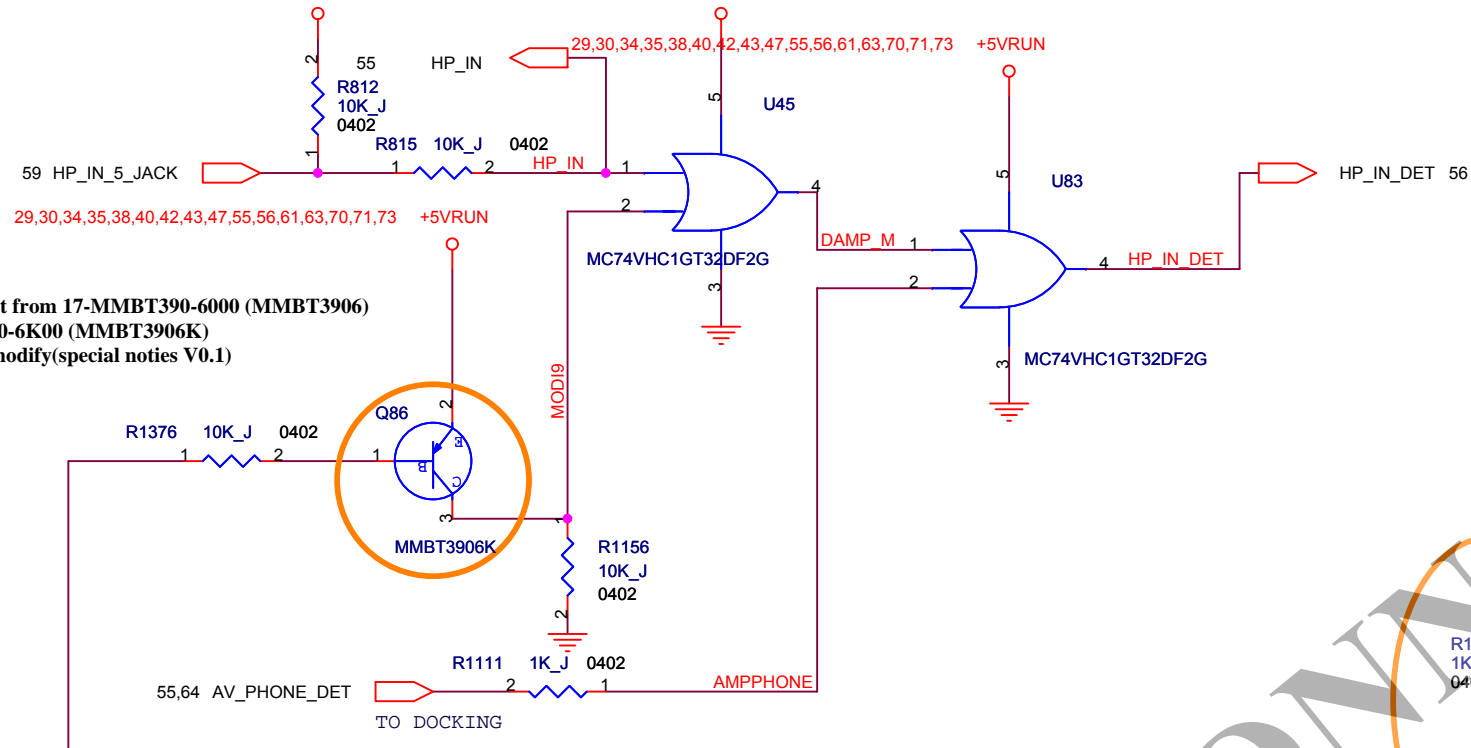




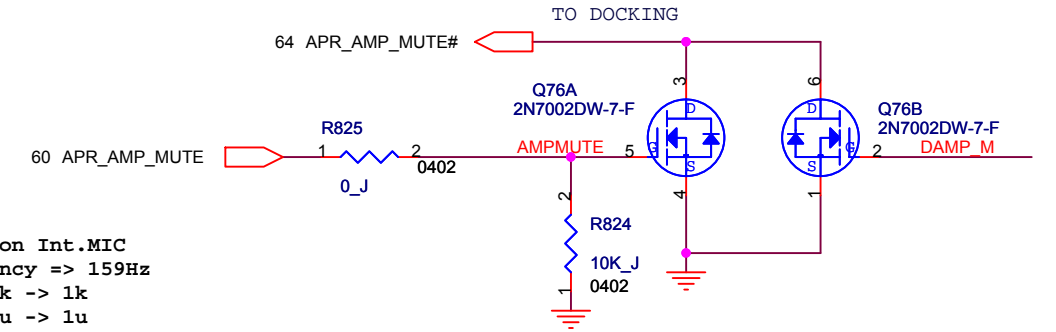
29,30,34,35,38,40,42,43,47,55,56,61,63,70,71,73 29,30,34,35,38,40,42,43,47,55,56,61,63,70,71,73 +5VRUN

040506

Q86 change part from 17-MMBT390-6000 (MMBT3906)  
to 17-MMBT390-6K00 (MMBT3906K)  
\*PVT already modify(special noties V0.1)

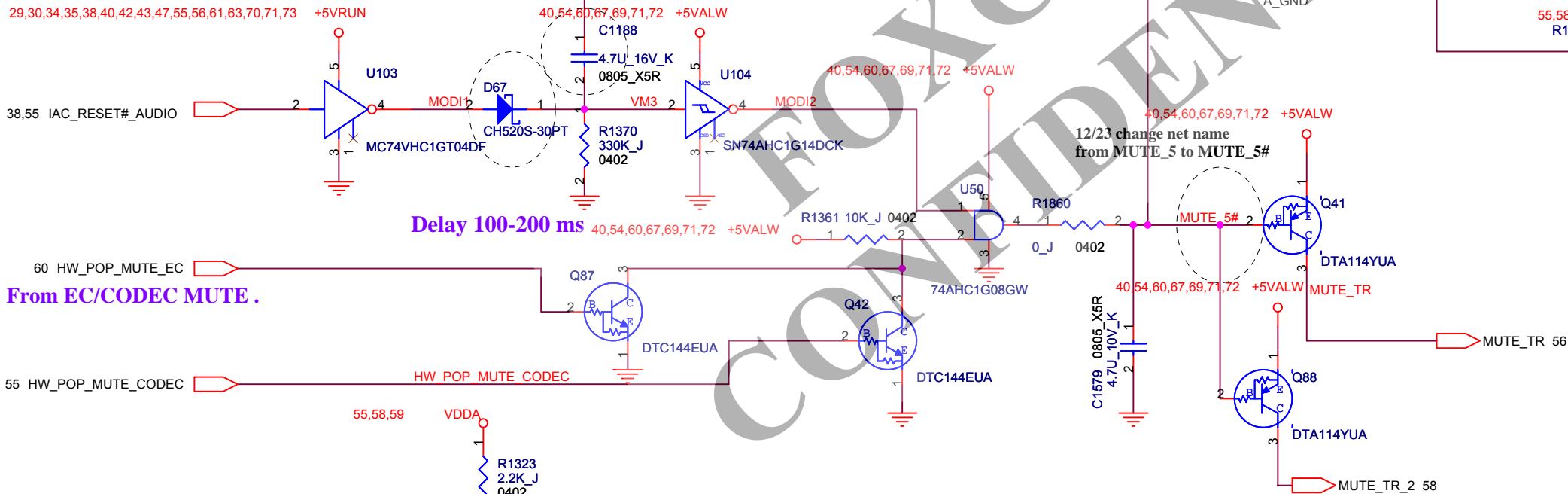


040606 FAN Noise on Int.MIC  
(1)Cut-off frequency => 159Hz  
R1319 : 2.2k -> 1k  
C1232 : 2.2u -> 1u  
(2)Cut-off frequency =>7.2kHz  
R1318: 22k -> 10k  
C1230: 220p -> 2200p  
\*MOR Nishio-san suggest 3/31



12/24 change part  
from 16-ASKS020-3S00 to 16-CH520S3-0P00

12/5 modify capacitor value

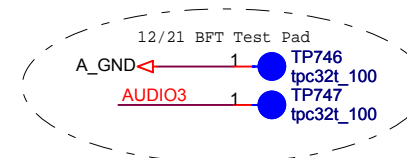


Delay 100-200 ms

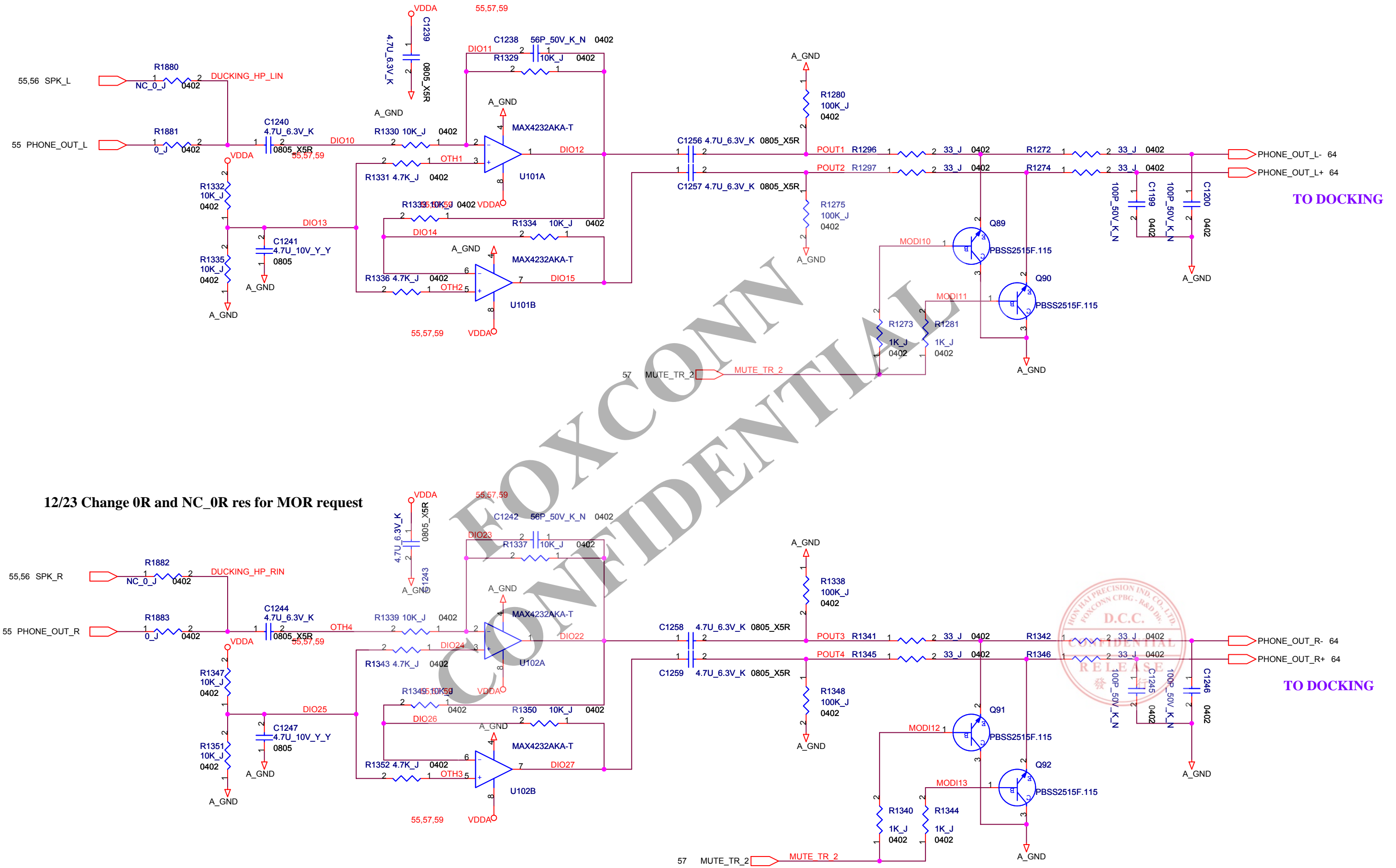
12/23 change net name  
from MUTE\_5 to MUTE\_5#



INTERNAL  
MIC(Non)

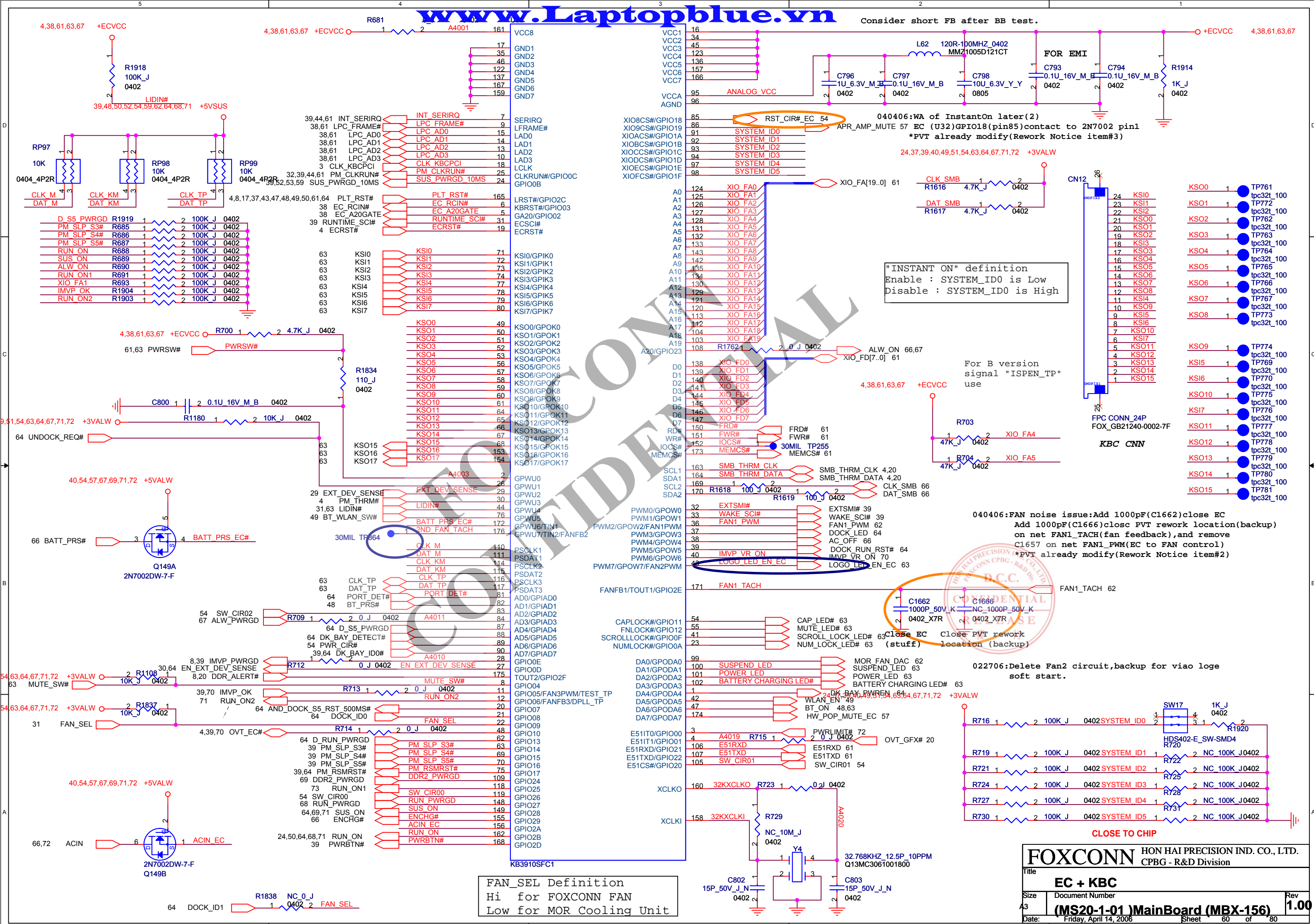


## PHONE OUT





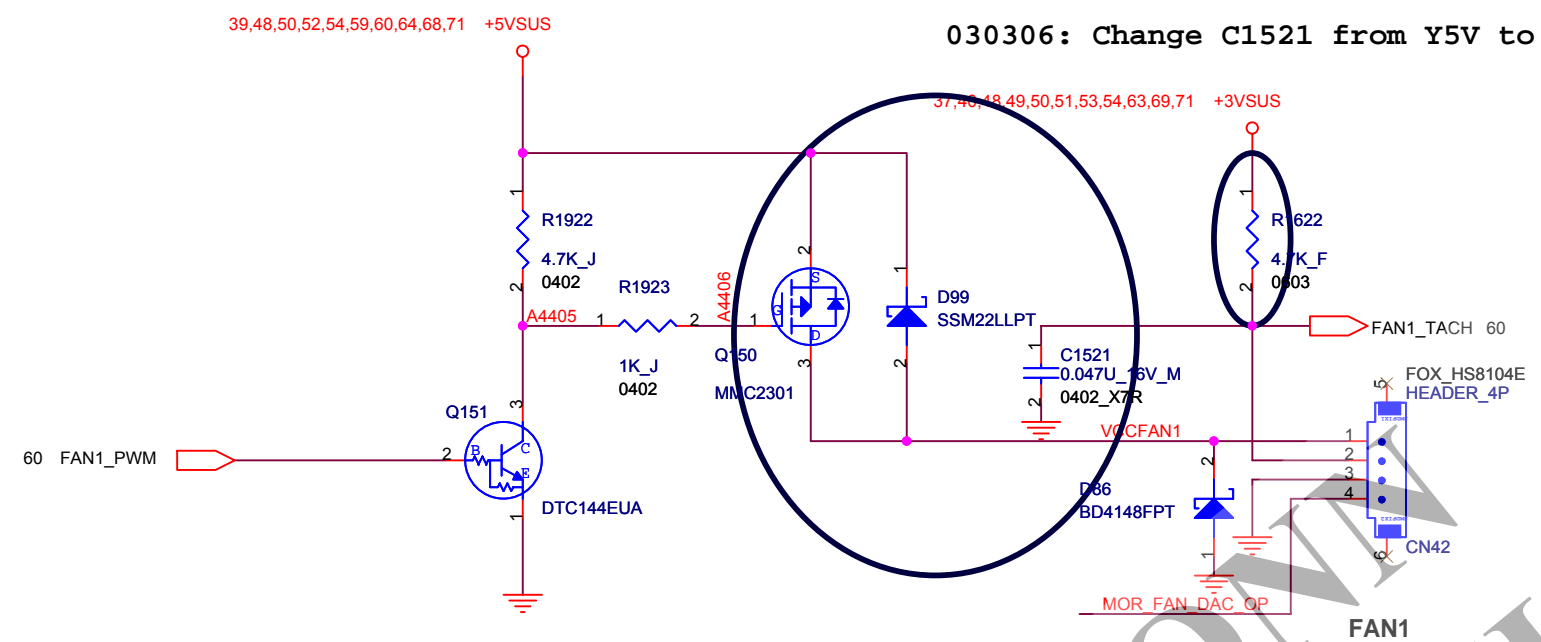




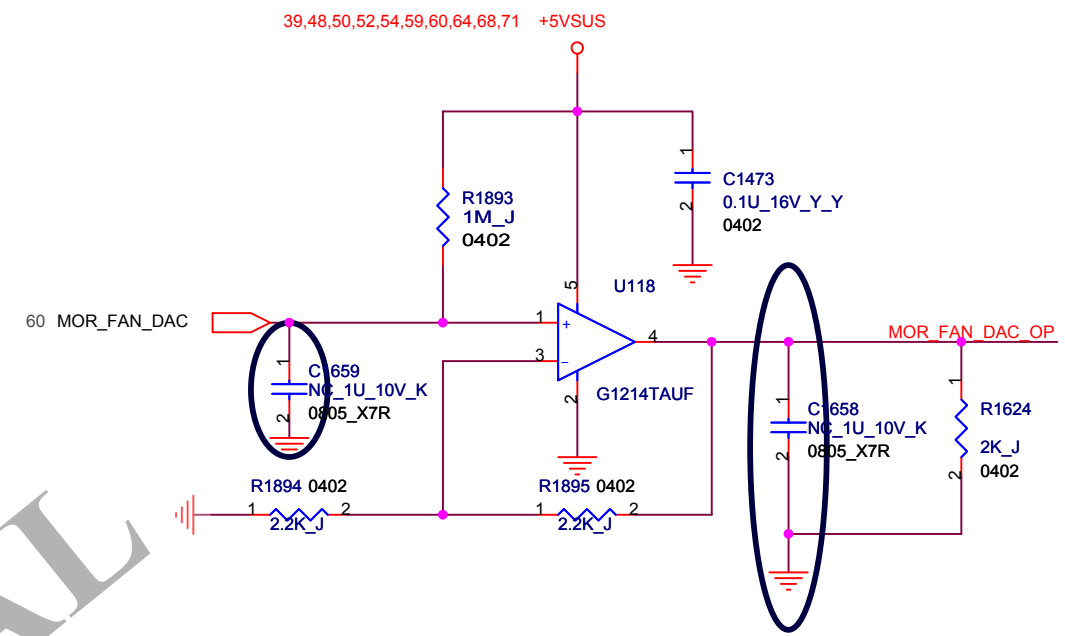




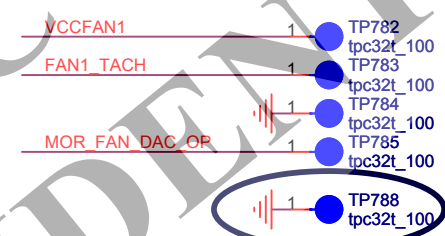
022706: Add doide for inverse current and change pull-high resistor from 10K to 4.7K.



030306: Change C1521 from Y5V to X7R.



022706: Add capacitor for cooling unit.  
031106: C1658 change to NC



030506: Backup Test Pad.

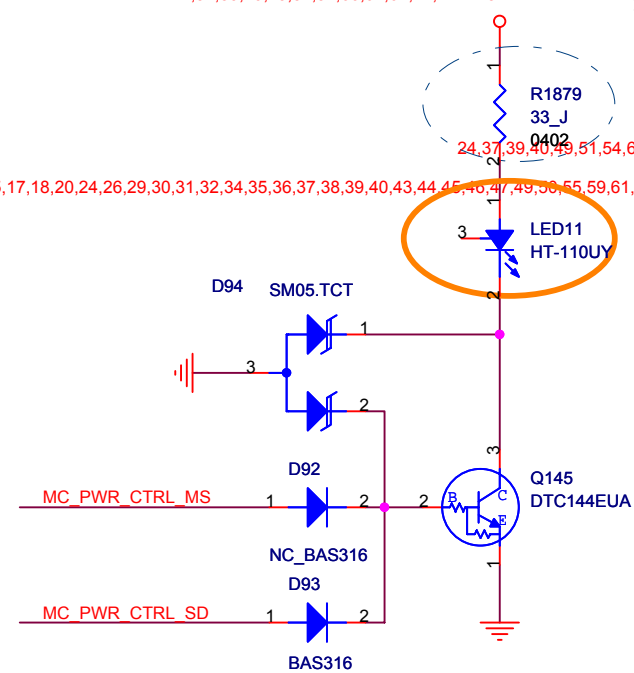
# FAN(FAN1+MOR FAN)



030306: Delet FAN2 circuit.

24,37,39,40,49,51,54,60,64,67,71,72 +3VALW

040506 Modify SD LED brightness  
LED11 change part from 16-HT110Y0-0000  
(Vendor P/N : HT-110Y) to 16-HT110UY-0000.  
(Vendor P/N : HT-110UY)

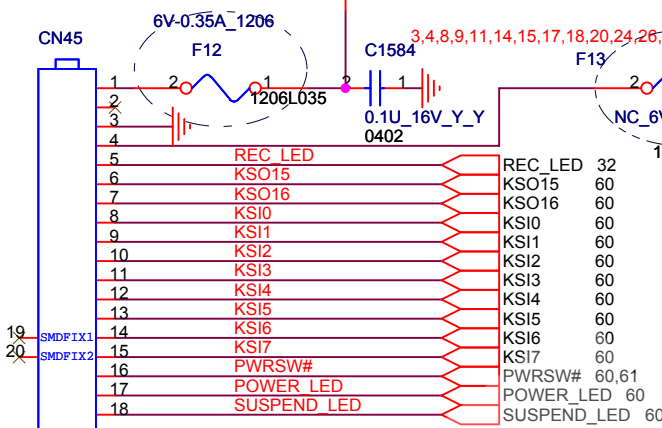


SD LED

TP789 tpc32t\_100  
TP790 tpc32t\_100  
TP796 tpc32t\_100  
TP791 tpc32t\_100  
KSO16 tpc32t\_100  
TP792 tpc32t\_100

PWRSW# tpc32t\_100  
POWER\_LED tpc32t\_100  
SUSPEND\_LED tpc32t\_100  
TP804 tpc32t\_100  
TP803 tpc32t\_100  
TP805 tpc32t\_100

24,37,39,40,49,51,54,60,64,67,71,72 +3VALW



FPC BOTTOM CONN\_18P 060301: Add 6 fulse for short issue.  
FOX\_GB11180-0221-7F

60 POWER\_LED  
60 SUSPEND\_LED  
60 BATTERY CHARGING LED#  
38,64 SATA\_LED#  
44 MC\_PWR\_CTRL\_MS  
44 MC\_PWR\_CTRL\_SD

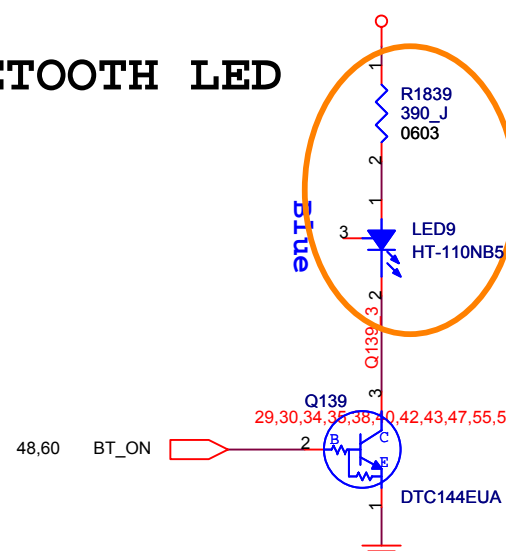
POWER\_LED  
SUSPEND\_LED  
BATTERY CHARGING LED#  
SATA\_LED#  
MC\_PWR\_CTRL\_MS  
MC\_PWR\_CTRL\_SD

TP806 tpc32t\_100  
TP807 tpc32t\_100  
TP809 tpc32t\_100  
TP810 tpc32t\_100  
TP812 tpc32t\_100  
TP811 tpc32t\_100  
TP814 tpc32t\_100  
TP813 tpc32t\_100  
TP815 tpc32t\_100

To LED Board Connector

## BLUETOOTH LED

29,30,34,35,38,40,42,43,47,55,56,57,61,70,71,73 +5VRUN



040506 Modify Bluetooth LED brightness  
(1) LED9 change part from 16-HT110NB-0000  
(Vendor P/N : HT-110NB) to 16-HT110NB-5000.  
(Vendor P/N : HT-110NB5) (The same with MS10)  
(2) R1839 change part from 1R-0000201-J200  
(200ohm,5%,0402) to 1R-0000391-J300.  
(390 ohm,5%,0603) (The same with MS10)

TP816 tpc32t\_100  
TP818 tpc32t\_100  
TP817 tpc32t\_100  
TP819 tpc32t\_100  
TP821 tpc32t\_100  
TP820 tpc32t\_100

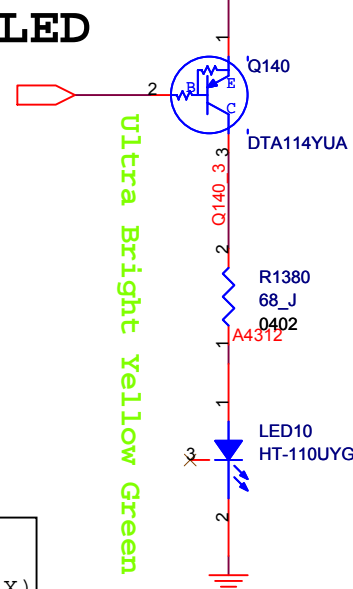
CLK\_TP tpc32t\_100  
DAT\_TP tpc32t\_100  
LIDIN# tpc32t\_100

030306: Change S/N from 1N-0010000-M0X0  
to 1N-0010000-MWG0.

To Touch Pad Board Connector

## WLAN LED

49 MINI\_CARD\_LED#



LED IF SPEC:  
20mA (TYP) , 30mA (MAX)

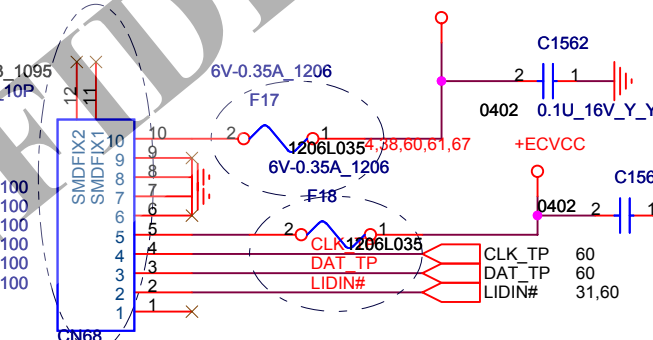
D95  
Q139 3 2  
Q140 3 1  
SM05.TCT

60 LOGO\_LED\_EN\_EC  
39 LOGO\_LED\_EN  
R1948 NC\_0402  
R1949 0\_J 0402  
31 INV\_ENABLE

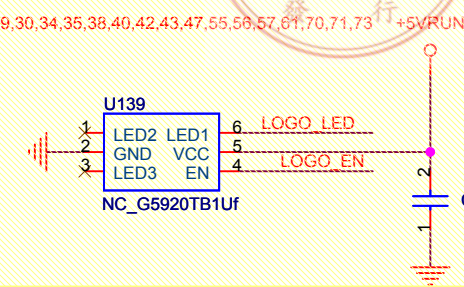
030906: Add two 0ohm resistors for Viao loge  
soft start issue.

29,30,34,35,38,40,42,43,47,55,56,57,61,70,71,73 +5VRUN

29,30,34,35,38,40,42,43,47,55,56,57,61,70,71,73 +5VRUN



030306: Backup for  
MAX1916 chip



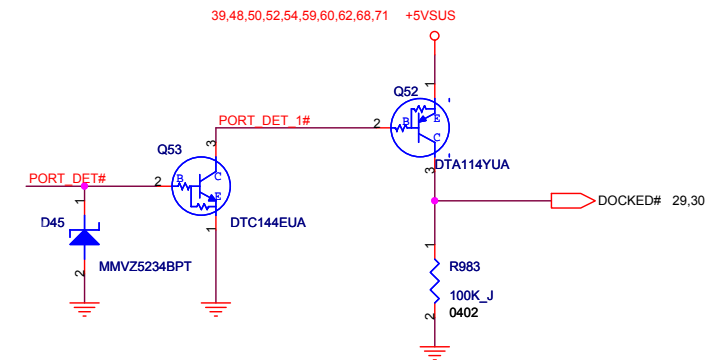
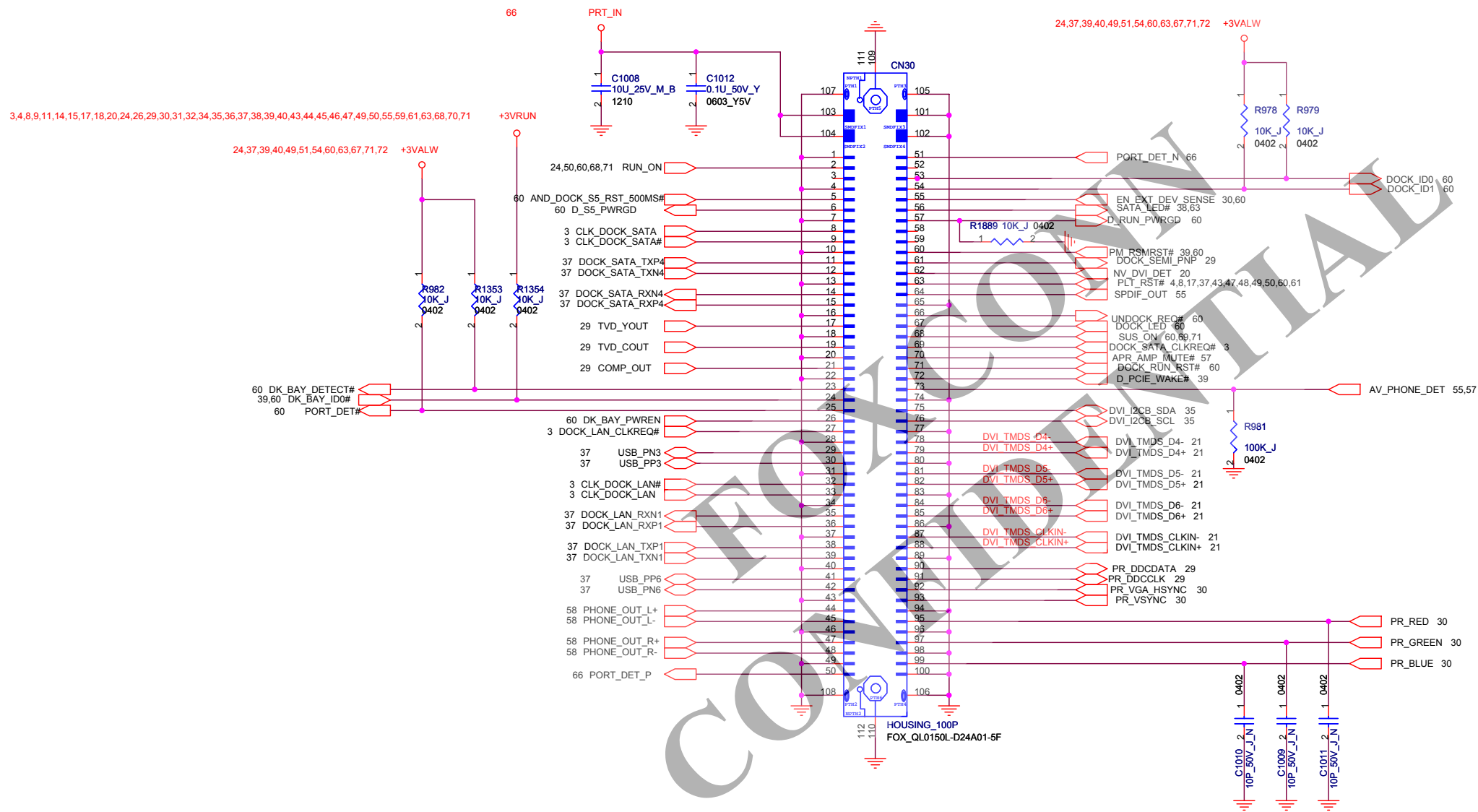
To AV Function Board Connector

FOXCONN HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

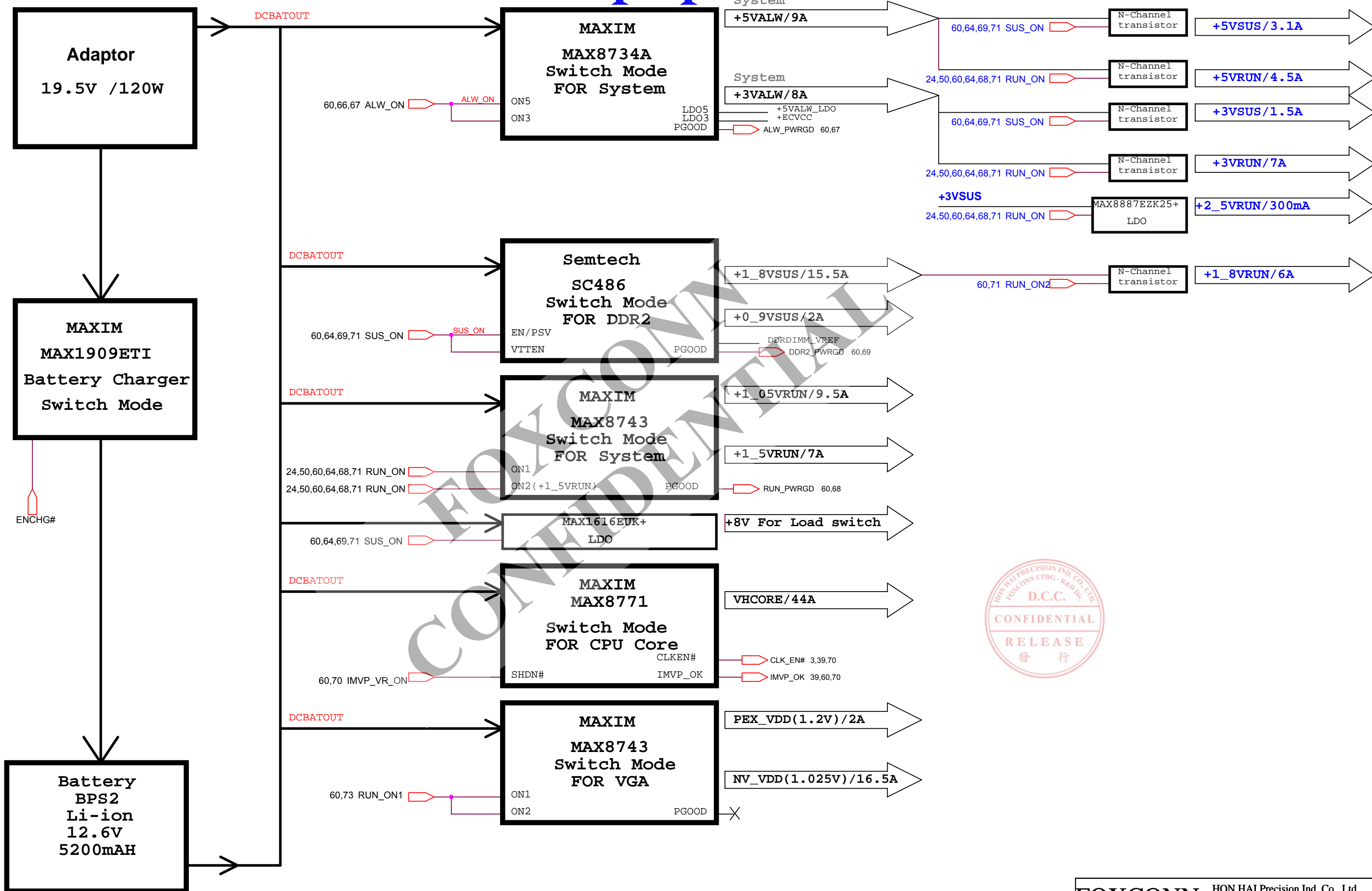
POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED

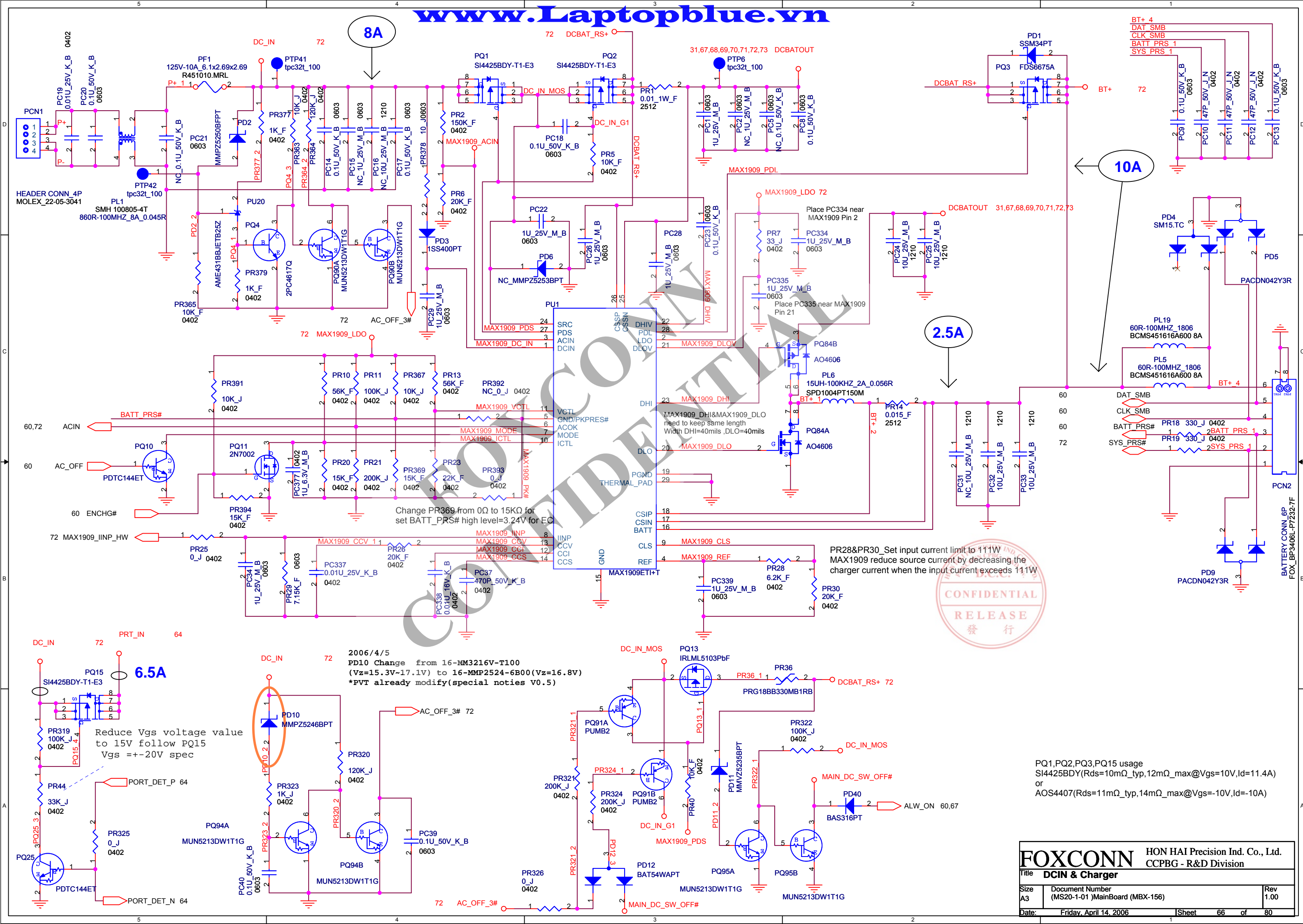
Size Document Number (MS20-1-01) MainBoard (MBX-156) Rev 1.00

Date: Friday, April 14, 2006 Sheet 63 of 80









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9.5A

5V LDO/100mA

5.5A

4A

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length Width DH5=40mils,DL5=40mils

Set output to 5.137V for TV-Tuner&HDD spec request by Nishio-San 12/27

Adjust Current Limit setting

5V LIMIT@11A(10.1~13.2A)  
3V LIMIT@10.5A(10.2~12.7A)

TON connect to GND = 5V/400KHZ, 3.3V/500KHZ

CONFIDENTIAL

FOXCONN

HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

System Power 3.3V&5V

Document Number (MS20-1-01) MainBoard (MBX-156)

Rev 1.00

Date: Friday, April 14, 2006

Sheet 67 of 80

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9.5A

5V LDO/100mA

5.5A

4A

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length Width DH5=40mils,DL5=40mils

Set output to 5.137V for TV-Tuner&HDD spec request by Nishio-San 12/27

Adjust Current Limit setting

5V LIMIT@11A(10.1~13.2A)  
3V LIMIT@10.5A(10.2~12.7A)

TON connect to GND = 5V/400KHZ, 3.3V/500KHZ

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

System Power 3.3V&5V

Document Number (MS20-1-01) MainBoard (MBX-156)

Rev 1.00

Date: Friday, April 14, 2006

Sheet 67 of 80

www.Laptopblue.vn

9.5A

5V LDO/100mA

5.5A

4A

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length Width DH5=40mils,DL5=40mils

Set output to 5.137V for TV-Tuner&HDD spec request by Nishio-San 12/27

Adjust Current Limit setting

5V LIMIT@11A(10.1~13.2A)  
3V LIMIT@10.5A(10.2~12.7A)

TON connect to GND = 5V/400KHZ, 3.3V/500KHZ

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

System Power 3.3V&5V

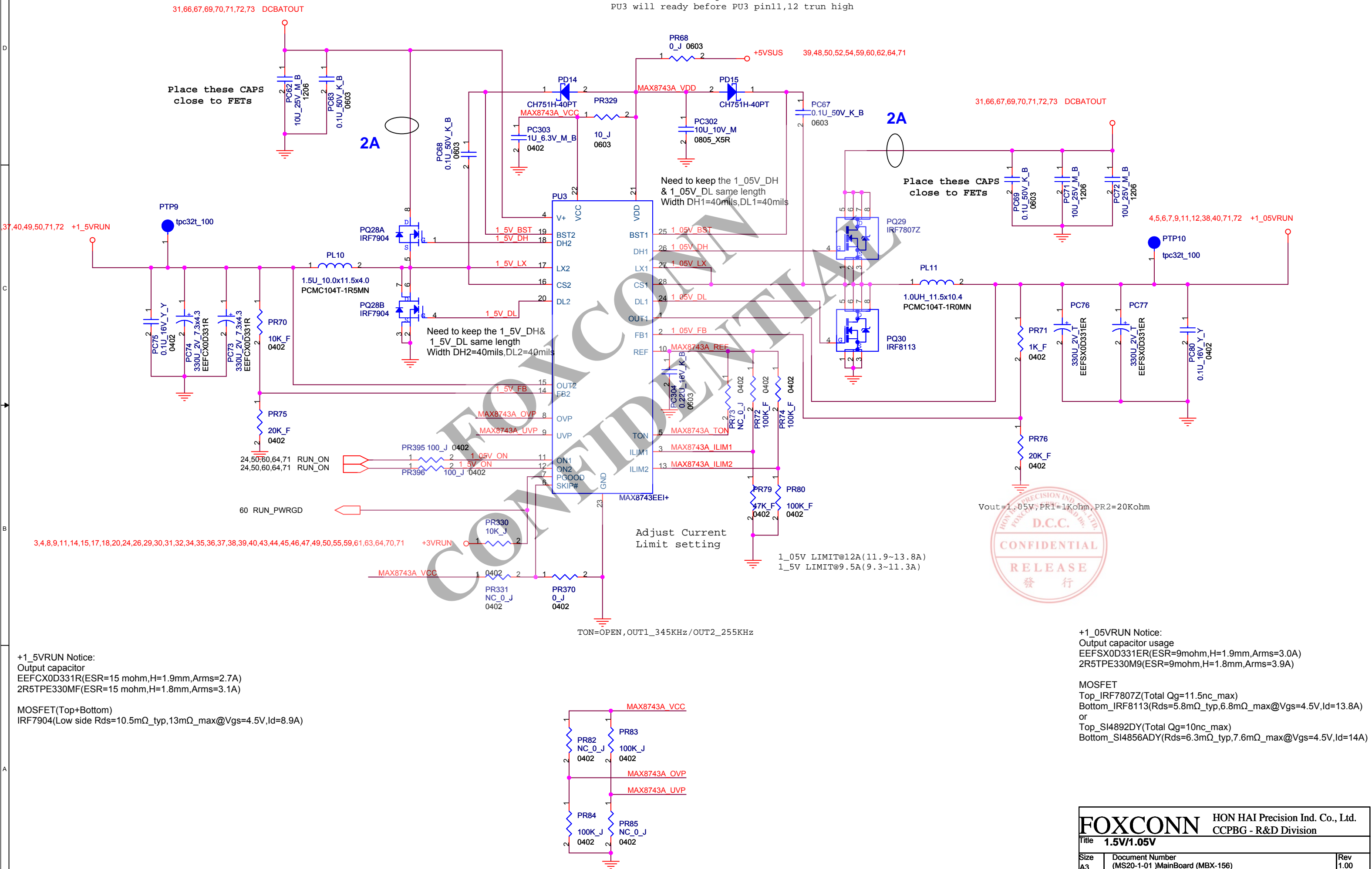
Document Number (MS20-1-01) MainBoard (MBX-156)

Rev 1.00

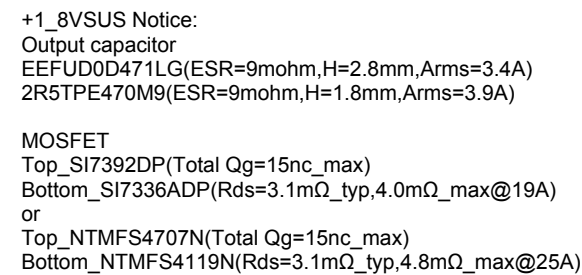
Date: Friday, April 14, 2006

Sheet 67 of 80

Use +5VSUS for PU3 pin21 to ensure  
PU3 will ready before PU3 pin11,12 turn high

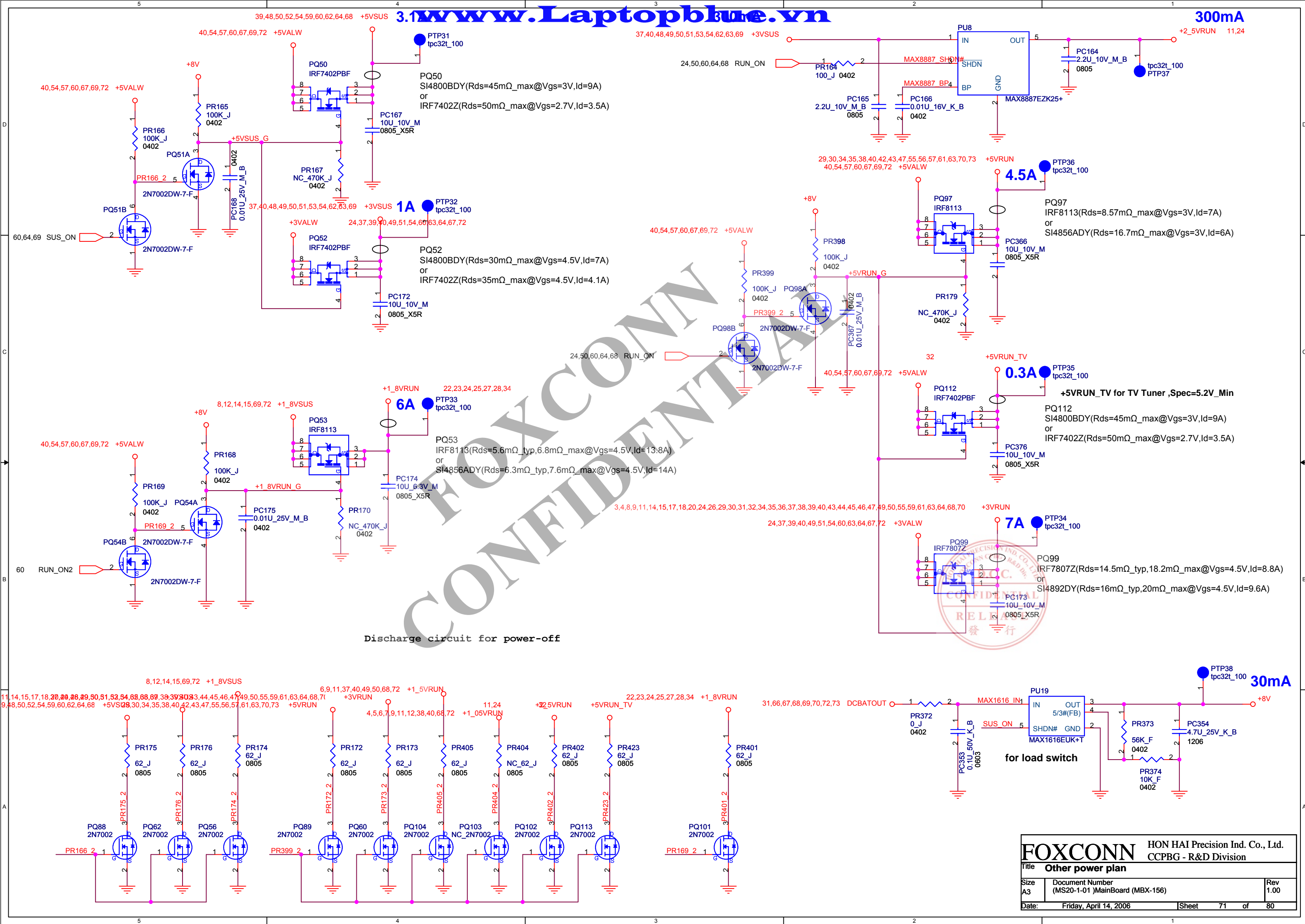


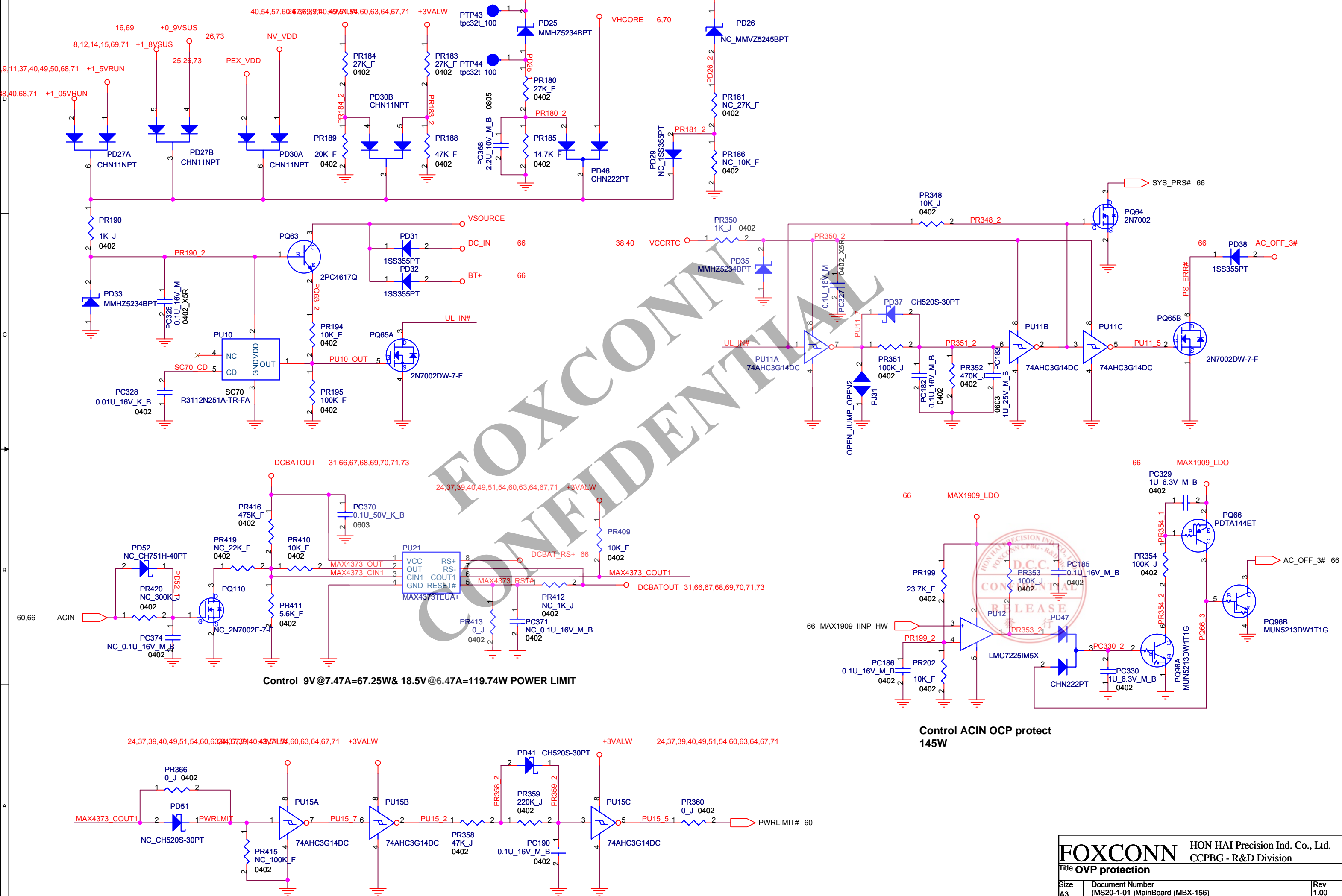




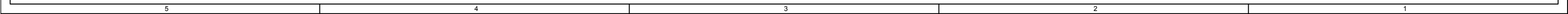
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>DDRII 1.8V/0.9V</b>			
Size A3	Document Number (MS20-1-01 )MainBoard (MBX-156)		Rev 1.00
Date:	Friday, April 14, 2006	Sheet	69 of 80





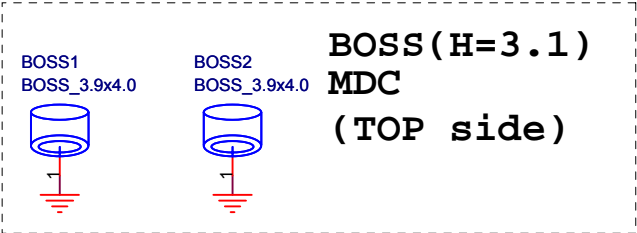
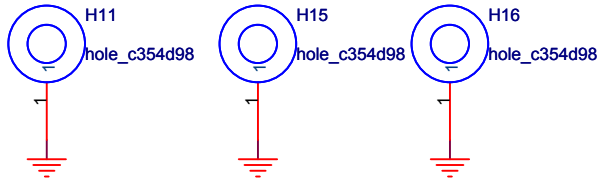






HOLE

Type 1



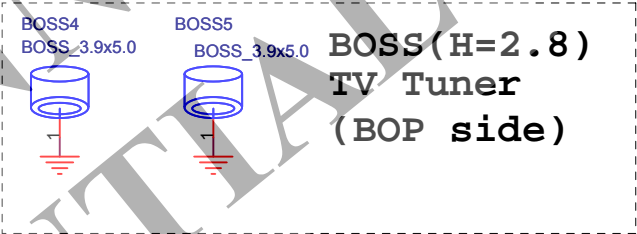
Type 2

10/24  
Remove Screw Hole H2  
P/N 1X-HOLE000-0108  
beacuse the Hole overlay  
with CN32 and layout will  
modify component screw shipe

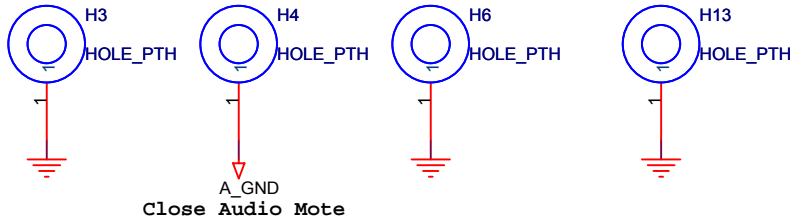


Type 3

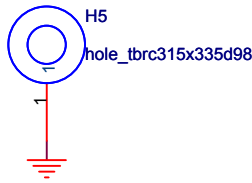
10/24  
Remove Screw Hole H1  
P/N 1X-HOLE000-0110  
beacuse the Hole overlay  
with CN32 and layout will  
modify component screw shipe



Type 4



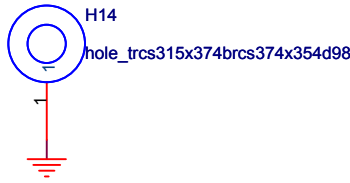
Type 5



Type NPTH Guide (spherical)HOLD



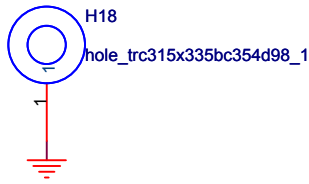
Type 6



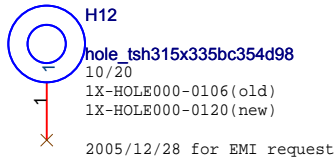
Type NPTH Guide (oval-shaped)HOLD



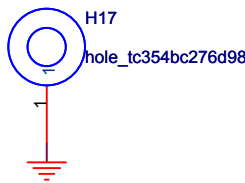
Type 7



Type 8



Type 9



Type CPU



(2005/09/19)

- 1.Update the NB and CPU circuit base on intel new design guide revision 1.5
- 2.Changed the wake event from S3 to S4 for lan .
- 3.Modified the MS current resistor from 1K to 1.5K to meet customer specification.
- 4.Express card power plane changed.
- 5.SB some power changed .
- 6.Modify HDMI circuit
- 7.Back Part value "NV"
- 8.Replease LVDS of 945GM interface

(2005/09/21)

- 1.Oide power plane change from 5VSUS to 5VRUN on page 48.
- 2.C1131 was connected to net "+1\_5V\_PCIE\_OUT" on page 48.
- 3.Change R1672~R1675 from stuff to no sutff on page 34.
- 4.Add one series 0ohm resistor to net "1930\_ACZ\_SDIN2" on page 34.
- 5.Add pull-up resistor to LDDC\_CLK/DATA and L\_CLKCTLA/CLKCTLB according to intel design guide on page 9.
- 6.ODD/SATA HDD change power plan from SUS to RUN
- 7.CN19/CN47/CN26 updata CIS Library
- 8.CN26 MDC modem Pin 2-Pin 6 short
- 9.CN12 KB connentor change type updata CIS library

(2005/09/22)

- 1.CN48 change from P/N:1N-1080000-0000 to P/N:1N-1068000-0000
- 2.page 72 add battery in current limit protection
- 3.page 66 modified battery input circuit.
- 4.page 46 Modify 2nd FAN circuit
- 5.page 55 Modify CIR interface
- 6.page 54 Modify Audio Board interface

- 7.Delete R772/R774/R1096 and Q35 on page 48.

- 8.Backup express card and Wlan wake event signal leakage circuit and change net name "D\_PCIE\_WAKE#" on page 35 and 44.
- 9.Default for wake S3,backup for wake S4 circuit on page 36 and 61.
- 10.USB power change from +5valw to +5vsus on page 45.
- 11.Modify the resistors for CRT and TV disable on page 9.
- 12.Update CN29 for new symbol on page 45.
- 13.Modify EC pin out
- 14.Modify Mini PCIE power plan from SUS to RUN
- 15.Modify HDMI circuit
- 16.Change Y8 package to 5mm\*7mm(H=1.2)
- 17.GPIO require from EC to SB Waiting S/W assign SB GPIO

(2005/09/23)

- 1.Change R162 from stuff to no stuff on page 13 .

- 2.Change R1354 pull-up power from +3VSUS to +3VRUN on page 44.

3. Pull " +1\_5VRUN\_DPLLA" and "+1\_5VRUN\_DPLLA" up to +1\_5VRUN for high type and change CAP5/6 to CA on page 11.
- 4.Pull LVDS clock up to +1\_5RUN and down to GND for high tye base on design version 1.5 on page 8.
- 5.Add one inductance and one capacitor for SATSPLL power filter on page 36.
- 6.Add Function RUN\_ON & AND\_DOCK\_S5\_RST\_100MS# & D\_S5\_PWRGD on page 44.
- 7.Detele HDCP\_SCL & HDCP\_SDA on page 44
- 8.Change MC\_PWR\_CTRL\_MS# to MC\_PWR\_CTRL\_MS; Change MC\_PWR\_CTRL\_SD# to MC\_PWR\_CTRL\_SD on page 56
- 9.Delete R925,R926 on page 56

(2005/09/27)

- 1.Delete R1739~1741 on page 9
- 2.Move three GPIO signals from EC to SB on page 35.
- 3.Change L4 and C142 value on page 11.
- 4.Add two 0ohm resistor for backup S4 wake event on page 61.
- 5.Modify Docking DVI chip from siil70B to siil162
- 6.Modify FAN circuit
- 7.Change CAP to FB on Audio internal speaker connector
- 8.Page 53 USB HUB 2.0->1.1

(2005/09/27)

- 1.PR407 change 0.012 ohm into 0.01 ohm
- 2.PQ3 change FDS6675A into SI4425BDY
- 3.PF1 change 8A into 10A
- 4.PD11 change MMVZ5231BPT into MMVZ5235BPT
- 5.PCN2 change package
- 6.De1 PQ75,Change PQ72,PQ74 to POWERPAK package
- 7.Add PC374,PC375
- 8.Modify GFX/HDMI circuit,review bypass and reciver RES.
- 9.Modify Docking pin out(Alex chen)

(2005/10/03)

- 1.Modify VRAM DDR3 Address pin swape(Alex chen)

(2005/10/04)

- 1.Schematic page swape
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify SATA/PATA circuit
- 5.Modify SB SATA interface add SATA AC Coupling cap

(2005/10/06)

- 1.Modify Power circuit
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify Mini PCIE Circuit
- 5.Delect R27,R130,R1772,R1773 and add the circuit for reboot.
- 6.Delect SM\_VREF buffer circuit ,because the DDRDIMM\_VREF can meet specification on page8.

(2005/10/07)

- 1.Modify CIR circuit ,change polyswitch
- 2.Modify GFX VRAM pin swape
- 3.Modify docking circuit
- 4.Add c? beside MDC Power on page 46
- 5.Detele R963 on page 47
- 6.Detele R1093,R1095,R1097; Detele C840,C834,C832,C1134 By on page 50
- 7.Change R1307 form 649 to 620 on page 51
- 8.Update DVI\_TMDS\* Net Name on page64

(2005/10/11)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.HDMI RP122,RP123,RP124,RP125 pin1-pin4 & pin2-pin3 pin swape.
- 5.Modify Power circuit

(2005/10/13)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.Modify Power circuit
- 5.Modify I/O Board connentor
- 6.Updata OrCAD symbol CN1,CN2,CN14,CN18,CN25,CPU,NB,Codec
- 7.Add Screw ,Boss,Power sequency page

(2005/10/19)

- 1.Change panel ID for Allen requirement on page39 .
- 2.Add 0.1u capacitance beside Vcppl1Vcpp2 on page 44
- 3.Change C954,C955 form 1u to 0.1u ; chang R931 form 10k to 43k on page 44
- 4.Add 2 capacitance of 0.1u beside +3VRUN on page 46
- 5.Change R1630 form 1.5k to 1k on 10/17 on page 46
- 6.change D62,D63 place on page 52
- 7.Add ten resistances on SD and MS signals according to MOR requirement.
- 8.Changed cap19/17 value from 150uF to 47uF according to MOR requirement on page52.
- 9.Add one 10uF capacitor and pull up SD\_WP on page46.
- 10.Aadded R? 1R-000010X-F300 (1ohm 1%, 0603, 1/10W) according to latest checklist on page 40.
- 11.MIDIFY POWER CIRCUIT
- 12.MODIFY VGA circuit
- 13.MODIFY EC circuit
- 14.MODIFY SATA/ODD circuit

(2005/10/20)

- 1.Page43 PATA CD-ROM: CN32 Pin3(Audio\_GND) connect to GND.
- 2.Page49 Mini-PCIE Card:only support S3 Wake On WLAN, so change Mini\_PCIE\_+3VAUX Default to +3VSUS (R1067 NC=>ON)(R1817 ON=>NC)

(2005/10/20)

- 1.Change the value of R91 to 1K and let PR126 no stuff.
- 2.Update connector pin connection according to Steve's comment.
- 3.Modify EC/Daughter Board connentor Circuit

(2005/10/24)

- 1.U126 pin27 Add 33pF and 12pF capacitor for RF frequency countermeasure.The small capacitance capacitor is put on close to 27 pin.
- 2.Delete L112.
- 3.A\_GND GNDD connection through L(NC) at one point. Make this circuit on M/B. (This circuit is moved from Audio daughter board.)
- 4.U41 pin1 Change to following circuit.
- 5.U68 pin 1/pin 27 Add 1 kohm buffer resistance on IN\_L. Add 1 kohm buffer resistance on IN\_R.
- 6.Q112 It is necessary to check there is no chance not to be ON because of an internal resistance of Digital Tr(Q112) in the case of emitter follower.
- 7.U68 CP\_GND do not have any connection to GND in schematics. There is no problem to connect A\_GND.
- 8.Change the connection GNDD to A\_GND.(C1291)
- 9.U50 Add the following RC filter(R:0 ohm,C:4.7uF) circuit between U50 4pin and MUTE\_5
- 10.Modify VGA circuit

(2005/10/26)

- 1.Modify Power circuit
- 2.Delete TP682,TP684,TP619,TP621
- 3.Audio add E-CAP

(2005/10/27)

- 1.change PCI7412 to PCI8412
- 2.Connentor Pin swap CN21,for FFC pin1 to pin1,
- 3.Common chock pin swap L68, L120 for layout request
- 4.Modify Power circuit
- 5.Modify GFX circuit

(2005/11/01)

- 1.Modify GFX circuit (includse ESD diode)
- 2.Modify Power circuit
- 3.Delete TP41,TP557
- 4.SATA CN63 Pin15.16.17.18.19.20 +3VRUN\_SATA\*->NC
- 5.SATA Delete Componment F9 & F10 & C791 & C792 & C1295 & C1296
- 6.Add SD LED
- 7.SPDIIF Add R1835 (MOR request) for matching the impedance

(2005/11/01)

- 1.Change C141 value from 0.1uF to 10uF on page 11.
- 2.Change R1307 value from 620\_F to 649\_F on page 51.
- 3.Add two resistors for clock amplitude tune on page 3.
- 4.Add one pull-low resistor in D\_RUN\_PWRGD on page64.
- 5.Modified for MOR requirement on page37 and page 39.
- 6.Delete LVDS\_GPIO in EC pin85 and then make EC pin85 as Test Point.
- 7.Ducking Hot\_Dock issue add pull down 10K(R1889) on D\_RUN\_PWRGD



- 1.MUTE\_SW#(R1108) change from pull +ECVCC to pull +3VALW  
2.CN42(FAN1)Pin swape  
3.MOR COOLING UNIT,Add for 0V,1V,1.9V,5V control,solving 5V ringback  
4.SD/MS LED(LED11) revise for too dark issue  
5.BLUETOOTH LED(LED9) revise for too dark issue  
6.SONY LOGO LED(U126)change from +3VRUN to +5VRUN,& change from AHC(CMOS) to AHCT(TTL)

(2005/12/08)

- 1.(U18)Change the connection for clock amplitude issue.(Add C1606,C1607,swape R1884,R1885 with L1,L2)  
2.(U11)Update VDDR3 CLK terminal for G73(Add C1608,R1896,R1897) =>Omit by 12/21 item#9  
3.(U12)Update VDDR3 CLK terminal for G73(Add C1609,R1898,R1899)  
4.(VDDR3) RFM1(R1464),FBA\_VBA2(R1463) change to NC  
5.(EC)BATT\_PRS# add circuit controlled by +3VALW(Add Q147,R1905)  
6.(EC)PWRSW# (R700)pull up from +ECVCC to +3VALW  
7.(EC)(Pull Down for EC strap issue)(Add RUN\_ON2 R1903,IMVP\_OK R1904)  
8.(EC)Swap MUTE\_SW# with IMVP\_OK (pin8<->pin11)for EC strap(TEST\_TP) issue  
9.(EC)MUTE\_SW# pull up(R1108) change from +ECVCC to +3VALW  
10.(EC)Swap OVT\_EC# with RUN\_ON2(R713<->R714)for EC strap(DPLL\_TP) issue  
11.(EC)Change BIOS(U32->U34->CN14) net name SIO\_FA[0..19] & SIO\_FD[0..7]to XIO\_FA[0..19] & XIO\_FD[0..7]  
12.(EC)XIO\_FA4(R703) & XIO\_FA5(R704)pull res change from 470K to 47K based on MS10 PVT revise  
13.(EC) pin39 change from DOCK\_RUN\_RST to DOCK\_RUN\_RST#  
14.(EC)PU CIR\_ALPS\_SW1 for EC strap(ISP\_TP)(Add R1906)  
15.(EC)pin156 ACIN Control by +3VALW(AddQ148,R1907)  
16.(GFX)FBCAL\_PD\_VDDQ add pull res (add R1900)  
17.(GFX)reverse INV\_EN\_EC to conctect NONETNA2(add NC R1901)  
18.(Audio)MUTE\_5 add 10K RES to Q112(add R1902)  
19.(GFX)PLT\_RST# to GFX add a AND circuit(Add R1908,R1909,R1910,U127)  
20.(HDMI)Del BUFIRST# to microcontroller reverse gate(Del U124)  
21.(Audio)modify capacitor value C1118 to 4.7u  
22.(Thermal sanner)change part U8 (15-F75383M-0000->15-F75383M-1000)  
23.(S-VIDEO ANALOG SWITCH)U77 change part U77 SN74CBT3257PW(NEW) <-> TS5A23157DGS(OLD)  
24.(S-VIDEO ANALOG SWITCH)change throuth U77:PR\_DDCCLK,PR\_DDCDATA,MB\_DDCCLK,MB\_DDCDATA,GM\_OR\_NV\_DDCCLK,GM\_OR\_NV\_DDCDATA.  
25.(SEMI-PNP)Modify SEMI-PNP circuit  
26.(CRT)Modify CRT circuit:  
27.(HDMI)U123 pin44 pull up res R1690 NC\_10K\_J <- NV72\_10K\_J  
28.(HDMI)Modify Y8 circuit.  
29.(PCMCIA)U62 pin12 connent to PLT\_RST#  
28.(Audio)Change part Q77,Q78,Q89,Q90,Q91,Q92,Q143,Q144(17-2SC5376-0000->17-PBSS251-5F00)  
29.(SD)power control circuit R1630 (1K->330R)  
30.(HDMI)U116 change part (SST89V54RD2-33-C-TQ <- NV\_SST89V52RD2-33-C)  
31.(Audio)Q112 change part (MMBT3906 <- 2SC5376)

(2005/12/15)

- 1.(POWER)Page 66----Change PR44 from 13K\_J to 33K\_J, Change PQ3 from SI4425BDY-T1-E3 to FDS6675A, Change PD1 from SSM34APT to SSM34PT.  
2.(POWER)Page 67----Change PC350 from NC to 10U\_25V\_M\_B, Change PR67 from NC to 0\_J, Change PR63 from NC to 100K\_J, change PR64 from 120K\_F to 160K\_F, change PR65 from 147K\_F to 120K\_F,Change from PJ29 to PR57 0\_J, Delete PJ2&PJ4 and short, Delete PJ1&PJ3 and short, Delete PR414, Add PR422 1K\_J.  
3.(POWER)Page 68----Change PR79 from 56K\_F to 47K\_F, Delete PJ5&PJ6 and short, Delete PJ7&PJ8 and short.  
4.(POWER)Page 69----Change PR305 from 8.2K\_F to 6.2K\_F, Delete PJ11 and short, Delete PJ9,PJ11&PJ37 and short.  
5.(POWER)Page 70----Delete "Reserve for improve CLK\_EN# wrong timing" circuit, Change PC276 & PC283 from NC to 10U\_25V\_M\_B, Change PD18 & PD45 from SKS30-04AT-G to SSM34PT.Del PQ111,PR422  
6.(POWER)Page 71----Change PQ104 from NC to 2N7002,Change PR404 from 62\_J to NC, Change PQ50&PQ97 from IRF7807Z to IRF7402PBF, Delete PJ41 and short, Delete PJ28 and short,Delete PJ40 and short.  
7.(POWER)Page 72----Change Power Limit circuit.(Add PR366,Del PQ109,PC188,PC189,PR207,PR208,PR212,PR213,PU14, change part:PQ110 NPN->N-MOS  
8.(POWER)Page 73----Change PR227 from 56K\_F to 47K\_F, Change PR417 from 560\_F to 2K\_F, Change PR418 from 22K\_F to 10K\_F, Delete PJ32,PJ33&PJ35 and short, Delete PJ34 and short.  
9.(CKG) Del C1606,C1607,R1884 and R1885 on page 3.  
10.(CPU) Add 0.1uF capacitor(C1610) for GTLREF on page 5.  
11.(Docking)Change Net From DK\_BAY\_PWEN to DK\_BAY\_PWREN  
12.(Docking)Change Net From DK\_BAY\_ID# to DK\_BAY\_ID0#  
13.(Docking)Change Net From AND\_DOCK\_S5\_RST\_100MS# to AND\_DOCK\_S5\_RST\_500MS#  
14.(Docking)Change Net From DK\_BAY\_ID# to DK\_BAY\_ID0#  
15.(GFX)Modify BOM configuration for G73M-U(BLOCK DIAGRAM).  
16.(GFX)Modify PCI\_DEVID[3:0]="1001"->9 for G73M-U.  
17.(GFX)Add pull down 10K ohm resistor to DOCK\_SEMI\_PNP. (R1911)  
18.(GFX)Update the pannel ID Spec.  
19.(GFX)Change the reset signal to PCI\_RST for U116 and U117(Nvidia suggestion).  
20.(EC)Add DIP SW17(HDS401-E) for Instant ON selection.Delete R717,R716 change from CA\_100K\_J to 100K\_J  
21.(EC)Change CIR\_ALPS\_SW0 to SW\_CIR00 for the same as IR module net name  
22.(EC)Change CIR\_ALPS\_SW1 to SW\_CIR01 for the same as IR module net name  
23.(EC)Change CIR\_ALPS\_SW2 to SW\_CIR02 for the same as IR module net name  
24.(EC) Change CIR\_ALPS\_WAKE# to PWR\_CIR# for the same as IR module net name  
25.(EC)Change LIDIN# power source from +3VALW to +ECVCC due to SW/Kenny request  
26.(EC)PWRSW# Pull High change from +3VALW to +ECVCC  
27.(EC)Add KS015 and redefine CN45 Pin4 ~ Pin6 for SW/Kenny Request  
28.(CIR)Change EC to CIR connentor CN61 net name  
29.(CIR)Add PWR\_CIR# pull up RES R1913  
30.(GFX)U8 modify  
31.(EC)System ID pull up power source change from +ECVCC->+3VALW  
32.(Audio)CVREF bypass CAP change from C863(10U)->(1U)  
33.(Mini PCIE)WIRELESS Add R1912 pull up RES.  
34.(EC) Add +ECVCC discharge RES (R1914)  
35.(Touch Pad)LIDIN# pull up from +3VALW ->+ECVCC  
36.(EC)Q147,Q148 change part from P-MOS->NPN  
37.(SB) LVDSGPIO R1887 change to NC

(2005/12/21)

- 1.(EC)12/20,40 Revise SW17 from HDS401-E to HDS402-E\_SW-SMD4 cause the vendor has stopped producing HDS401-E.  
2.(EC)12/21,43 Revise C802/C803 from 10pf to 15pf due to Steve's SI test report.  
3.(POWER)Page 67----Del PR422  
4.(POWER)Page 69----Change PD19 to PD48  
5.(POWER)Page 72----Change PU22A to PU15A, Change PU22B to PU15B  
6.(POWER)Other-----Add 32mil test point for BFT test  
7.(MDC)MDC connentor change to P/N: 1N-0012000-F0X0 ,BOSS1/BOSS2 P/N:1M-1A40M20-3100) the same with MS10  
8.(CARD BUS)CARD BUS control change PCI7412 to 8412  
9.(SB)RP95 pin swape for Layout request

(2006/1/3)

- 1.(GFX)Modify Si1162 power net S11\_62\_PVCC.  
2.(GFX)Add FBA\_CLK0\_RC and FBA\_CLK1\_RC net name.  
3.(GFX)Modify R378,R380,R1871,R1872 from 40ohm to 60ohm for Nvidia suggestion.  
4.(GFX)Remove Si1162 and other parts to cancel G72M DVI Function.  
5.(GFX)Add two Inverter gate to prevent the glitch from Silicon 1930.  
6.(GFX)Update the reset signal of HDMI UCODEC,HDMI Microcontroller and HDMI Silicon 1930.  
7.(GFX)Remove C432,R270,R274 on G73M SKU.  
8.(GFX)Add TP682, TP678 test point because MIOBD7 and MIOBD10 unused.  
9.(GFX)Modify HW strap for Infineon VRAM and update the BOM configuration in block diagram page.  
10.(GFX)Change ESD diode D78,D79,D80 to meet the HDMI Spec.  
11.(GFX)Delete the page 33(DVO-TMDS Si1162) for layout space.  
12.(GFX)Add 1 switch to divide DVI DDC from HDMI DDC.  
13.(GFX)12/27 Remove R195,R196,R1729,R1730 and C284 for G72M DVI funtion missing.  
14.(GFX)Change R1592 from 360 ohm to 390 ohm for Silicon Image suggestion.  
15.(GFX)Modify the INV\_EN\_EC to control INV\_BRADJ for the Nvidia glitch issue on MS10.  
16.(POWER)Page 71----Change PQ52,PQ112 from IRF7807Z to IRF7402PBF,Change PQ97 from IRF7402PBF to IRF7807Z.  
17.(POWER)Page 72----Change PD52,PR420,PC374,PQ110 to NC.  
18.(POWER)Page 67----Change PR49 from 160K to 187K, Change PR52 from 100K to 120K.  
19.(ICH7)12/23 Change U30 and R1183 to NC and change R1184 to stuff on page 39.  
20.(ICH7)12/23 Add two 2N7002 for leakage on page 38  
21.(camera)Add 10uF capacitor for camera power,and add modify OCP circuit (add u133,del Q79,Q80)on page 50.  
22.(CKG)12/23 change dumping resistor from 33 ohm to 100ohm and add FB between dumping resistor and clock generator for MOR requirement on page 3.  
23.(CKG)12/28 Del 27MHZ circuit for Nvidia on page 3.  
24.(USB)12/28 Change USB connectors to white type on page 52.  
25.(EC)12/22,45 : Revise net name from FAN1\_PWM to 2ND\_FAN\_PWM for error correction.  
26.(EC)12/22,46 : Remove R1915 for moving pull high R from connector(CN68) side to EC side  
27.(EC)12/22,47 : Add pull +ECVCC high R for moving from connector(CN68) side to EC side  
28.(EC)12/23,48 : Revise H\_RCIN# to EC\_RCIN# and H\_A20GATE to EC\_A20GATE for matching leakage-proof circuit in P32  
29.(EC)12/23,49 : Revise 2ND\_FAN component to NC due to Ted request 12/22. (R1920-R1923,R1767,C1615,C1616,C1618,Q150,D87,CN65)  
30.(EC)12/23,50 : Revise net name from FAN2\_DAC to MOR\_FAN\_DAC due to Ted request 12/22.  
31.(EC)12/23,51 : Revise net name from FAN2\_DAC\_OP to MOR\_FAN\_DAC\_OP due to Ted request 12/22.  
32.(EC)12/23,52 : Add 0 ohm(NC) for improving clock skew of PCLK\_JIG.  
32.(EC)12/23,53 : Revise R693,R1904,1903 from 10K to 100K for improving driving ability  
33.(EC)12/23,54 : Add 1k ohm for avoiding EC directly short to GND.  
34.(EC)12/26,55 : Change CN62 from HS8202B to HS8102E due to Mechanical 12/23 outline file  
35.(EC)12/26,56 : Due to leakage of original circuit we revise 12/23 BATT\_PRS# controlled by ALW power well circuit.  
36.(EC)12/26,57 : Due to leakage of original circuit we revise 12/23 ACIN controlled by ALW power well circuit.  
37.(EC)12/27,58 : D\_S5\_PWRGD add pull down 100k ohm due to Hibino San request(12/26 mail).  
38.(EC)12/28,59 : Delete R1540 due to too dark issue  
39.(EC)12/28,60 : Add PWRSW# test point due to BFT request.  
40.(EC)12/28,61 : Change LED11 from HT-110UYG to HT-110UY due to error color correction.  
41.(EC)12/28,64 : Change BT LED power source from +3VRUN to +5VRUN and R1839 from 68 ohm to 82 ohm due to too dark issue.  
42.(EC)12/28,65 : Add ESD protector of SD LED due to Jacky Su/EMI request on 12/28.  
43.(EC)12/28,66 : Add ESD protector of Bluetooth LED and WLAN LED due to Jacky Su/EMI request on 12/28.  
45.(Ducking) Page64 CN30 pin 75,pin76 change net name NV\_I2CB\_SDA->DVI\_I2CB\_SDA NV\_I2CB\_SCL->DVI\_I2CB\_SCL  
46.(GFX)Modify the INV\_EN\_EC to control INV\_BRADJ for the Nvidia glitch issue on MS10.  
47.(GFX)EMI suggestion:mount Cap.C1592,C1595,C1598,C1601.  
48.(GFX)EMI suggestion:add cap.0.1uF on LCDVCC near CN3.Mount C1558 near CN49.  
49.(GFX)EMI suggestion:add EMI bead on HDMI +5VSUS before C1452,and near CN60.reserve cap.0.1uF on +5VRUN near F1.  
50.(GFX)EMI suggestion:add ESD Diode for AV\_IN\_GND.  
51.(W-LAN)Page 49,Change R1912 from 1M to 100k ohm(Nishio San Request)  
52.(W-LAN)Add FET on MINI\_CARD\_LED# between CN18 pin 44(P.49) and Q140 2pin(P.63) and control FET by using WLAN\_EN that Wireless Off Control signal from EC .(Nishio San Request worry about only SW Driver control.)  
53.(W-LAN)Prepare big Capacitor pad 22uF(1206) pad for MINI\_PCIE +3.3V and MINI\_PCIE +1.5V for each. Because .1in is bigger than .11abg from point of view of power consumption.  
54.(SD)change SD socket to 67913-0009(easy repaiy issue)  
55.(LAN).XTAL Y6 Load CapC1034,C1035 change 22pF->27pF

(2005/12/31)

- 1.(POWER)Page 67----Change PR49 from 187K to 160K, Change PR52 from 120K to 102K.  
2.(POWER)Page 72----Change PC368 from NC to 2.2U\_10V\_M\_B  
3.(EC)12/30,67 : Change R1920 from NC\_1K to 1K due to error correction.  
4.(EC)12/30,68 : Change TP785 net name from FAN2\_DAC\_OP to MOR\_FAN\_DAC\_OP due to error correction.  
5.(EC)12/30,69 : Swap CN68 for change T/P FFC from bending to no bending.  
6.(EC)12/31,70 : Add constant current circuit MAX1916 due to MOR request.  
7.(GFX)EMI suggestion:Add 33pF Cap to SVIN\_Y\_1 and SVIN\_C\_1.  
8.(GFX)EMI suggestion:Change C1516,C1517,C1518,C1566,C1567,C1568 from 0.1uF to 220pF.  
9.(GFX)EMI suggestion:add ESD Diode for SVIN\_Y\_GND and SVIN\_C\_GND.  
10.(GFX).Add 1uF capacitor(NC) to VRAM\_VREF for VRAM Max Load Drop.  
11.(GFX).Add two resistor to LVDS CONN pin6 for Gamma control.  
12.(Audio) Modify CN64 pin definf  
13.(Audio)Change audio amp from MAXIN to TI  
14.(USB)Delete EXT USB connentor (MB CN29),and move USB signal to CN64.

(2006/01/03)

- 1.(GFX)page 17.Add MIOB\_CLKIN (R1939)10K ohm to GND  
2.(GFX)page 35.Add NV\_HDMI\_DET\_5 (R1940)100K ohm to GND  
3.(EC)page 63.Add PWRSW# (TP846) Test Pad on BOT side  
4.(ESD)page 63.Change Part D94,D95 from PACDN042Y3R to SM05.TCT  
5.(ICH7) page 37 INT\_PIRQ#\_R conctect to GND(R1887) NC->0R  
6.(GFX) page 25 (+1\_8VRUN) CAP20 change 47uF to 150 uF

(2006/01/04)

- 1.(Oide)page 50.CN21.pin swape for ME request

(2006/01/20)

- 1.(Power)page 70.PR138 change from 13K to 16K due to 青建德 revise on 1/20.

(2006/01/21)

- 1.(ICH)page 37.Change R1886 from NC to 0 ohm due to control Gamma function.  
2.(OIDE)page 50.Change F10 from 1206L150 to 1206L035 due to short current protect.

(2006/1/12)DVT-2

- 1.(GFX) For some HDMI device no support detect pin function issue, (1)Page 20 NV\_GPIO6 del TP610,add off page port. (2)Page 35 Add backup circuit,NV\_GPIO6(level shift) to switch(U136 pin1)Add part:Q156,Q155,R1942,(NC)R1941  
2.(GFX)Page 35 HDMI 12C double pull up issue change R1611,R1612 NV->NC, because page 20,R1385,R1386 still pull up.  
3.(Audio Conn)Page 59.For Audio Board USB2.0 HUB request, (1)CN64 pin 16 change GND to +3VSUS. (2)add FUSE(F9),and bypass CAP(C1641)  
4.(CIR) Page 54 For BFM request,add CIR test pad (TP847-TP856)  
5.(GFX) Page 34 Modify ESD diode (U128)depend on HDMI spec(C<50 pF) change part uClamp0504A->RClamp0514M (Modify Layout & BOM)  
6.(SATA) Page 42 Modify SATA connentor pin define,pin swape and add power pin to meet 7200RPM HDD current(MAX 5.2A/2 HDD)  
7.(SATA) Page 38 SATA signal Eye test Fail issue,change C724-C727,C1549-C1512 from P/N:1C-2B20392-K000(0402)->P/N:1C-2B30392-K001(0603) the same with MS10

(2006/1/16)DVT-2

- 1.(FAN-2) Page 62 Modify second FAN2 short with FAN1 issue  
2.(FAN-2) Page 62 FAN2 component cost down Q152,Q153,R1924,R1925 change to NC  
3.(SD LED) Page 63 LED11 change part HARVATEK\_HT\_110UY ->HARVATEK\_HT\_110Y

(2006/1/18)DVT-2

- 1.(ICH7) Page37 For support LVDS\_GPIO function,ICH7 INT\_PIRQ#\_R pull up RES.R1886 change 0R->NC  
2.(FAN-1) Page62 Modify fan speed feedback function,stuff C1521  
3.(W-LAN) Page49 For BFT test request,add wake on W-LAN test item,add Test Pad TP858  
4.(Audio) Page55 for Audio jack ESD issue,change Q117,Q118,Q119 form 17-2N70020-0000 ->17-2N7002K-0000  
5.(Oide) Page50 For I/O current protect request.Add F10, (This part only for placement,Wait to change part of I hold=0.35A,I trip=0.7A)





(2006/2/27)

- 1. Add doide for fan inverse current on page 62
- 2. Add capacitor 1uF for cooling unit on page 62.
- 3. Add capacitor 1000pF for fan noise on page 62 and should place colse to EC pin.
- 4. Chagne Oide power from +5VRUN to +5VSUS on page 50.
- 5. Audio coupling capacitor co-layout on page 56.
- 6. Backup 10uF capacitors for 22uF shortage on page 6.
- 7. Add discharge resistor for camera on page 50.
- 8. Change power plan for leakage issue of USB hub and change the fulse specification on page 54 , CN61 pin10 trace shold place same as pin1.
- 9. Add 6 fulse for FFC short issue on page 63.
- 10.Chagne CAP5 to "CA"
- 11.Add 2.2uf and 0.1uF capacitor for SMK power and add optional select for Alps pull-high power.

(2006/3/3)

- 1.(VIDEO)Modify the HW strap of VRAM for PVT
- 2.(VIDEO)Modify R1463,R1464,R1475,R1480,R1482,R1493 for 16Mx32 and 8Mx32 VRAM configuration
- 3.(VIDEO)U136 change switch control from NV\_HDMI\_DET\_5 to NV\_GPIO6
- 4.(VIDEO)Add two 0 ohm resistors to avoid the switch for NV\_I2CB because G72M only support HDMI
- 5.Change codec CIS symbol to four plus.
- 6. Add open jump on RTCRST# net on page 38.
- 7. Delet fan2 circuit and change the pull-high resistor of fan\_tach from 10K to 4.7K.
- 8. Back up logo led circuit for GMT solution on page 63.
- 9. MS\_R and SD\_R net name changed each other on page46.
- 10.Change connector S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0 for S/N wrong on page32.
- 11.Change CN68 S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0 for S/N wrong on page63.
- 12.Change the resistor (R1839) of bluetooth to 200ohm for too light issue on page 63.
- 13.Change the resistor (R1879) of SD card to 33 ohm for too dark issue on page 63.

(2006/3/9)

- 1. Change C1521 from Y5V to X7R on page 62
- 2. R585 change from 20K\_J to 22K\_F
- 3. Boss4 and Boss5 change to "NV73\_" on page 74.
- 4. Add one test point on signal "2ND\_FAN\_TACH" on page 60.
- 5. Add 4 test points on CN21 connector for TE test on page50.
- 6. Change net name from "EN\_EXT\_DEV\_SENSE#" to "EN\_EXT\_DEV\_SENSE" on page 30,60 and 64.
- 7. Delet R1906 on page 60 for CIR double pull-high issue.
- 8. Change R1913 from 10K to 100K on page 54.
- 9. Change CN19 parts for SMT issue on page50.
- 10.Change CN64 PIN16 from +3VSUS to GND and change PIN6 from USB\_PP2 to USB\_VCC2, Shift Pin 6&8 to Pin 8&10, Delet F9 and C1641 on page59.
- 11.Backup fusle for HDD voltage drop issue on page42.
- 12.Update U117 CIS symbol on page 34.
- 13.Update CN60 CIS symbol for SMT issue on page34
- 14.Add two 0ohm resistors for Viao loge soft start issue on page 63 and page60.
- 15.(Power)Page 69-----Change PR91 from 15.8K\_F to 16.5K\_F.
- 16.(Power)Page 70-----Change PR299/PR114/PR115 to 10 ohm, Change PR300 to 0 ohm, Change PC127 from NC to 1000P\_50V\_K\_B, Change PC126 to PR397 10K ohm. Change PR387 to 2.7K ohm.
- 17.(Power)Page72----Change PC326&PC327 from 0.1U\_16V\_Y\_Y to 0.1U\_16V\_M (X5R)
- 18.(Power)Page71----Change PQ97 from IRF7807Z to IRF8113.
- 19.(Video)Page 20,R1820change to NC,because The MS20 CEC line capacitance = 777pF is much bigger than 100PF spec. After remove this resistor, CEC cap reduced to 39PF. Pass.(This GPIO11 is no function on our system, Silicon Image suggest remove it.)
- 20.(Video)Page 74-BOSS4,BOSS5 change part name from NV73\_->TV\_
- 21.(Video)Page 32 change part name from NV73\_->TV\_
- 22.(Video)Page 32 CN67,change PCB Footprint to co-layput "molex" & "Foxconn"part
- 23.page 63 CN68 change PCB Footprint to co-layout "molex" & "Foxconn"part
- 24.page 15 add C1661 (0.1uF) close CN2 pin1 (DDR2\_VREF) for voltage level noise debug.

(2006/3/11)

- 1.Page 62 C1658 change to NC
- 2.Page 56 CAP24,CAP25 change to NC
- 3.Page 70 PR397 change part 10K(5%) to 10K(1%)
- 4.(VIDEO)Page 35 R1940 change part name NV\_100K\_J to NV73\_100K\_J
- 5.(VIDEO) page 27,Page 28 PVT EMI recommend(NC\_ ->NV\_):C1590,C1591,C1593,C1594,C1596,C1597,C1599,C1600

(2006/3/13)

"Not neet to modiy BOM and Layout "

- 1.change title block ver "1.0" to "0.40"
- 2.page 34.HDMI circuit, change net name(1)HDMI\_+5VSUS->HDMI\_+5VRUN (2)HDMI\_+5VSUS1->HDMI\_+5VRUN1

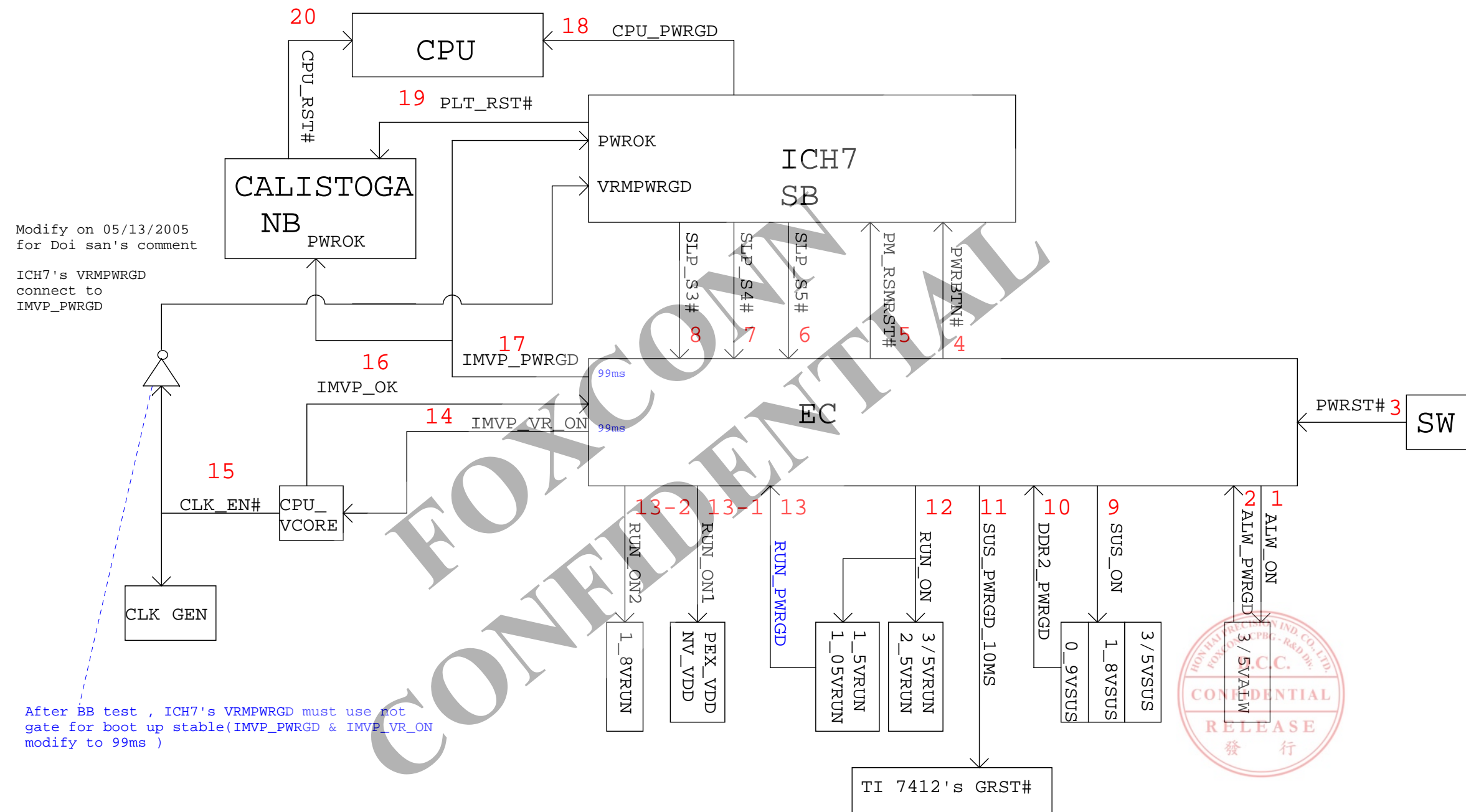


- 1.(page60)FAN noise issue:Add 1000pF(C1662)closc EC Add 1000pF(C1666)closc PVT  
rework location(backup only) on net FAN1\_TACH(fan feedback),and remove  
C1657 on net FAN1\_PWM(EC to FAN control)  
\*PVT already modify(Rework Notice item#2)
- 2.(page 70)TV turner noise issue:  
(1)Add PR424(2.2 ohm), PC378(47pF) on net MAX8771\_LX1,  
(2)Add PR425(2.2 ohm), PC379(47pF) on net MAX8771\_LX2  
(3)PR299 change value from 10 ohm to 0 ohm  
\*PVT already modify(special noties V0.8)
- 3.(page54)WA of InstantOn later(1)  
IR receiver connentor side add N-MOS 2N7002(Q157) for 3V->5V level shift  
\*PVT already modify(Rework Notice item#3)
- 4.(page60)WA of InstantOn later(2)  
EC (U32)GPIO18(pin85)contact to 2N7002 pin1  
\*PVT already modify(Rework Notice item#3)
- 5.(page29)Modify BOM to desable HDMI connentor SEMI PNP Hot plug detect function:(backup)  
(1)U108 change part name to NC\_ (not stuff)  
(2)Add R1952 (0 ohm) link U84 pin4 to U73 pin2
- 6.(page32)TV module modify BOM roul  
(1)Mini PCI socket circuit group change part neam from TV\_ to normal.  
(2)Special mini stereo jack and S-VIDEO in group change part name from TV\_ to JDTVNC\_  
(JP digital tuner sku NOT stuff)
- 7.(page32)TV Tuner EMC request  
(1) add R1950(0 ohm) link net AV\_IN\_GND to GND  
(2) add C1663(470pF) link net AUDIO\_IN\_L\_1 to AV\_IN\_GND  
(3) add C1664(470pF) link net AUDIO\_IN\_R\_1 to AV\_IN\_GND  
(4) add C1665(100pF) link net VIDEO\_COMP\_1 to AV\_IN\_GND
- 8.(page66)PD10 Change from 16-MM3216V-T100(Vz=15.3V~17.1V) to 16-MMP2524-6B00(Vz=16.8V)  
\*PVT already modify(special noties V0.5)
- 9.(page35)Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request)  
change part name:  
(1)NV73\_->NV\_:U136,Q155,Q156,R1940,R1941,C1616  
(2)NV72\_->NC:R1946,R1947  
\*PVT already modify(special noties V0.4)
- 10.R1493 change part name (G73Only\_->NV73Only\_) to meet BOM configuration  
\*PVT already modify(special noties V0.6)
- 11.(page57)Q86 change part from 17-MMBT390-6000 (MMBT3906) to 17-MMBT390-6K00 (MMBT3906K)  
\*PVT already modify(special noties V0.1)
- 12.Modify Bluetooth LED brightness  
(1)LED9 change part from 16-HT110NB-0000(Vendor P/N : HT\_110NB) to 16-HT110NB-5000.(Vendor P/N : HT-110NB5)  
(The same with MS10)  
(2)R1839 change part from 1R-0000201-J200 (200ohm,5%,0402) to 1R-0000391-J300.(390 ohm,5%,0603)  
(The same with MS10)
- 13.Modify SD LED brightness  
LED11 change part from 16-HT110Y0-0000(Vendor P/N : HT\_110Y)to 16-HT110UY-0000.(Vendor P/N : HT-110UY)
- 14.(page7~page13) updata U4(NB) part to meet KCL  
change from 12-0K58000-A300(945 PM ,QK5800,Version A3) to 12-0G82945-A301(945 PM ,QG82945PM (SL8Z4),Version A3)
- 15.(page37~page41) updata U29(SB) part to meet KCL  
change from 12-0K17000-B000(82801GHM1,QK1700,Version B0) to 12-NH82801-0000(NH82801GHM,(SL8YR),Version B0)
- 16.FAN Noise on Int.MIC  
(1)Cut-off frequency => 159Hz  
R1319 : 2.2k -> 1k  
C1232 : 2.2u -> 1u  
(2)Cut-off frequency =>7.2kHz  
R1318: 22k -> 10k  
C1230: 220p -> 2200p  
\*MOR Nishio-san suggest 3/31
- 17.(page63)Power Button Board Connector back up power plan bypass cap C1507 change to NC  
(modify BOM change part name NC\_)
- 18.Y7 (6MHZ\_20P\_30PPM)change part number from secondsource to main source(buyer request)  
P/N:(1F-X00006M-3001(AKER) ->1F-X00006M-3002(TXE)  
Footprint:(xtal\_4p\_244\_284x205 -> xtal\_4p\_232\_276x197)  
\*The second already verify on DVT & PVT
- 19.(page43)ESD 10KV on ODD reboot issue  
(1)add C1668(100pF) on net ODD\_RESET#  
(2)add C1667(0.1uF) on net +5VRUN
- 20.(page73)NV\_VDD on G73M-U power noise issue, change PR417 (PU16-FB2) from 2K to 2.1K  
(to setting NV\_VDD voltage on G73M-U from 1.2V to 1.21V)
- 21.(page26)NV\_VDD on G73M-U power noise issue,modify BOM configuration,  
(1)G73M-U (H) C352,C362,C363,C364 on 22uF / X5R / 0805(1C-2B70226-M100)  
(2)G72 (L) / G73 (M) C352,C362,C363,C364 on 10uF / X5R / 0805(1C-2B70106-M100)
- 22.(page31) CN3 (LVDS CONNECTOR) update OrCAN symbol



FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title <b>History(PVT)</b>		
Size A3	Document Number (MS20-1-01 )MainBoard (MBX-156)	Rev 1.00
Date:	Friday, April 14, 2006	Sheet 78 of 80

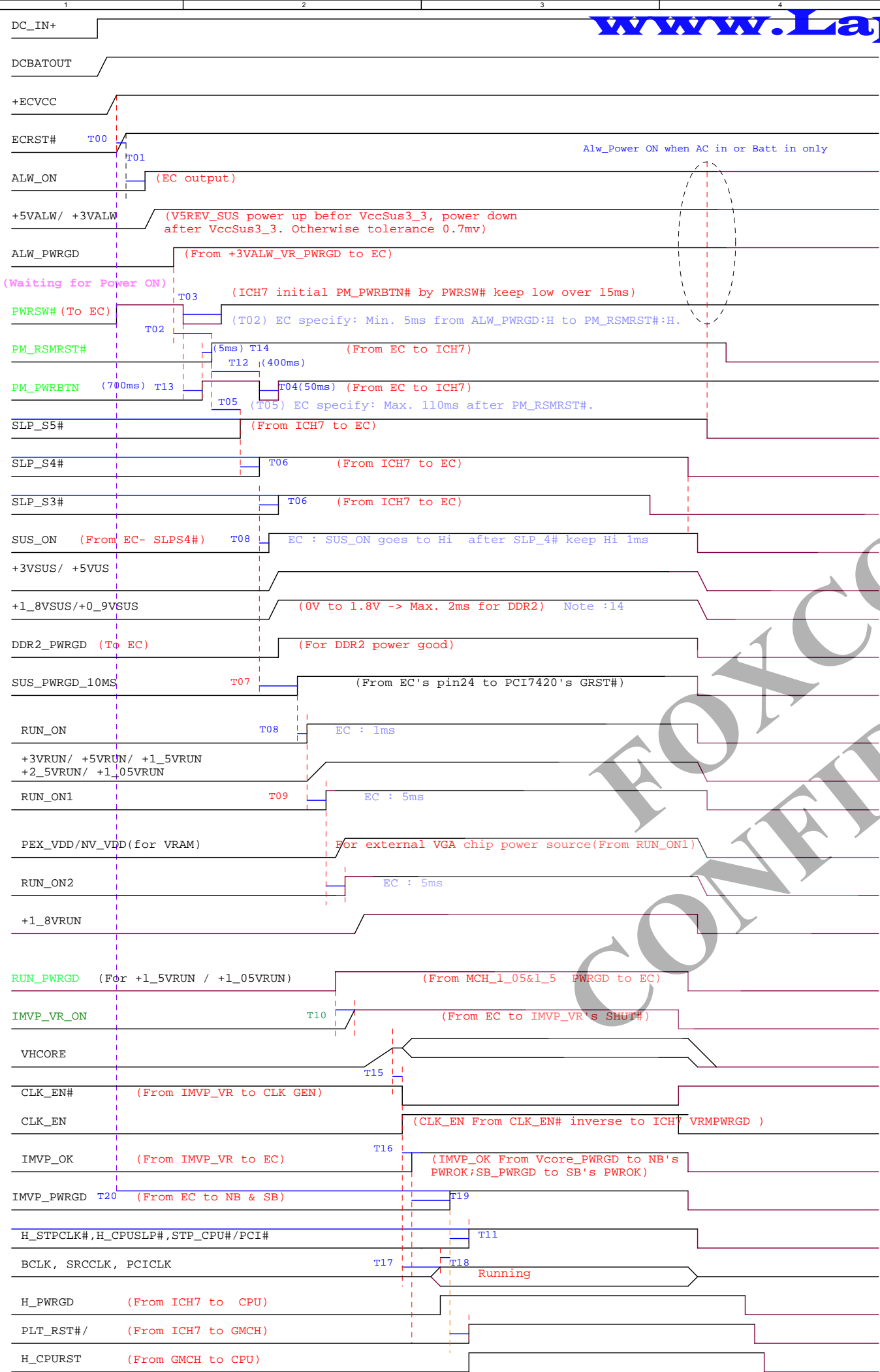
# MS20 Power On Sequerce Block Diagram





# MS20 Power On Sequerence Timing

Version : 0.1  
Modified date : 2006/4/6



NOTE : ( EC KB3910 Min. response time is 1ms)

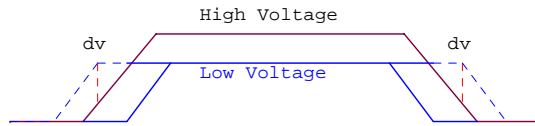
1. T00 : R=47K , C = 0.1uF is ENE recommand value please refer to KB3910B0-AN4A-200
2. T01 : When RTC battery already is present, this timing is always meet specification, so we don't control it.
3. T02 : ALW\_PWRGD:H to PM\_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing) Doi-San request 10ms 05/17
4. T04 : For MS01 SPEC Min. is 50 ms (Normal SPEC is 20ms)
5. T05 : RSMRST# active High to SLP\_S5# active High Max. is 110ms (Please reference Intel 16971 Page 301 of t232 timing)
6. T06 (Please reference Intel 16971 Page 301 of t234 timing)
7. T07 : For MS01 current SPEC Min. is 25 ms (Please refer Intel 16971 Page 301 t208 SPEC is Min 10ms )
8. T08 : For MS01 current SPEC Min. is 1 ms (1ms is EC KB3910 at least response time)
9. T09 : For MS01 current SPEC
10. T10 : Please refer to Intel 16971 Page 300 of t214 timing
11. T11 : Please refer to Intel 16971 Page 303 of t216 timing
12. T12 : PM\_RSMRST# ACTIVE HIGH TO PM\_PWRBTN# ACTIVE LOW is 400ms (Normal SPEC is 110ms; Please reference Intel 16971 Page 301 of t232 timing)
13. T13 : For MS01 current SPEC Min. is 700 ms (Normal SPEC is 1ms that EC can response)
14. T14 : For MS01 current SPEC Min. is 5 ms
15. DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
16. IMVP\_OK is same with SB\_PWRGD (reserved And Gate with SYS\_PWRGD)
17. In NV4X power sequence : NV\_VDD , VRAM\_VDD, PEX\_VDD and VRAM\_TERM can ramping up anytime after +3VRUN starts ramping up. (Please refer to DG-00969\_v05c Page 50 for NV4x GPU power sequencing description)
19. T15 : Please refer to MAX8736 datasheet page 7 & page 25 Figure 8
20. T16 : Please refer to MAX8736 datasheet page 25 Figure 8
21. T17 : Please refer to Intel CK410(14690) page 53
22. T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
23. CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
24. T20 : From ECRST# L->H to IMVP\_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed. (Requested by Doi's san 05/13)



Remark: (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV)  
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF\_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH\_VCC(1.05V), dt:0.7mV
4. +1\_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2\_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3\_3VRUN -> +1\_5VRUN(TV), dt:0.7mV

R/C delay  
(47K/  
0.1uF)



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Don't control	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min. 700ms	Min. 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	