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51	USB2.0		
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53	FAN/ HW Protect		
54	Daughter Board Conn.		
55	CAM/OIDE		
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57	AUDIO(AMP & SPK)		
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75	HOLE & BOSS		
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77	HISTORY1		
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80			

P. Leader	Check by	Design by

DVT to PVT

Project Code & Schematics Subject: M780 EVT Main Board

PCB P/N: FUBAI 1P-0086102-8010

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

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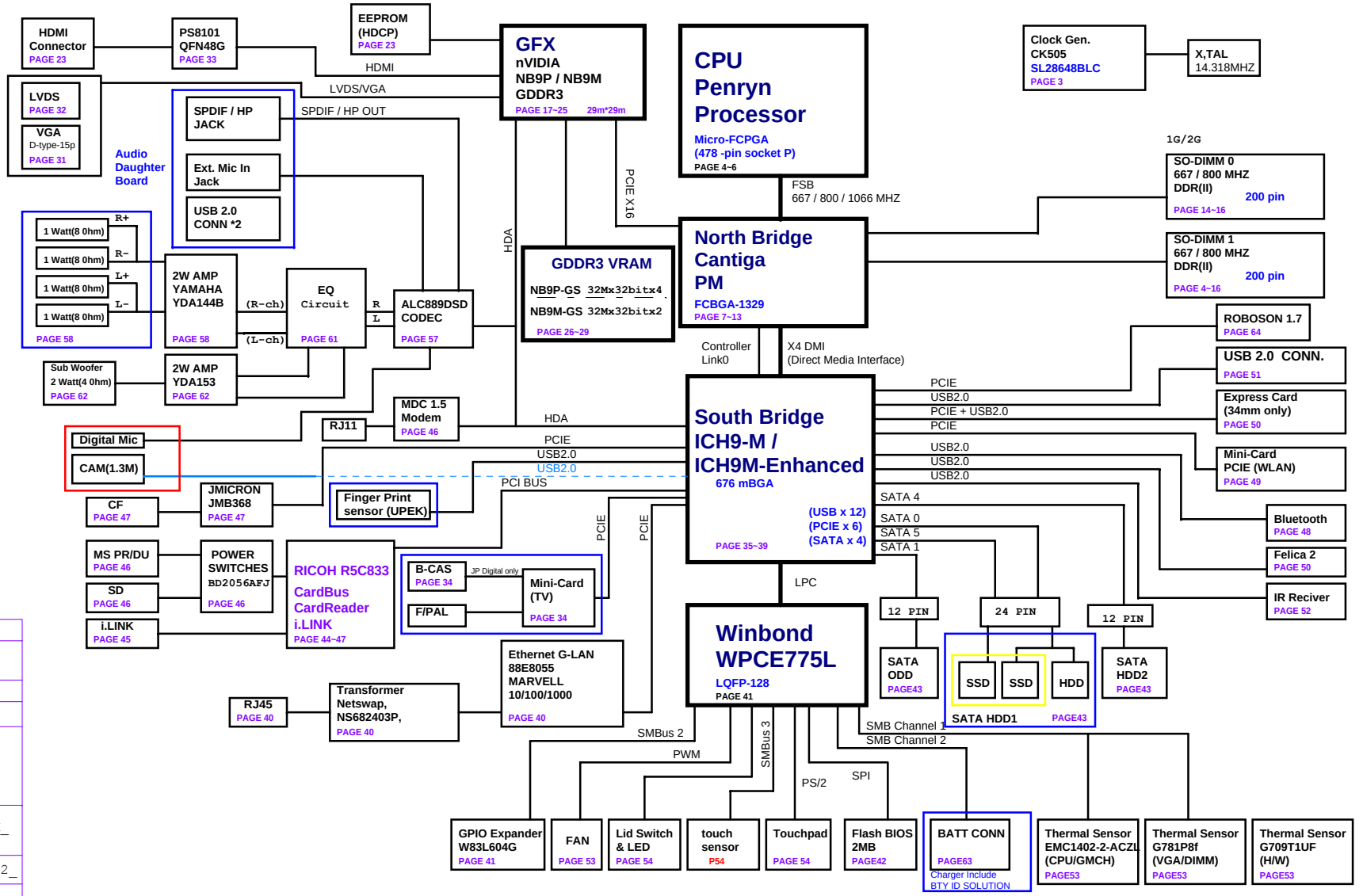
M780 Montevina Block Diagram



TI CHARGER BQ24751 P.63

INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC ISL6236IRZA-T P.64

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW

SYSTEM DC/DC SC411 P.65

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM

SYSTEM DC/DC ISL6269A P.66

INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS

SYSTEM DC/DC G2998 P.66

INPUTS	OUTPUTS
DCBATOUT	+0_9VRUN

CPU DC/DC ISL6266A P.67

INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC APL5913 P.70

INPUTS	OUTPUTS
+1_5VRUN	APL5913

SYSTEM DC/DC SC411 P.70

INPUTS	OUTPUTS
DCBATOUT	NV_VDD

M780 BOM configuration

unstuff	NC_
NB9P-GS + NB9M-GS	NV_
for L model	NV9L_
for M model	NV9M_
B-CAS Card, FeliCa module for J SKU stuff Roboson,TV Tuner ,IR,Reciever,CF Card Slot unstuff for L Model	LNC_
for H M model	NV9HM_
for L model 32Mx32 GDDR3	NV9L32_
for H model	NV9H_
for Qimonda VRAM	NV9QI_
for Samsung VRAM	NV9SAM_

H-model used ICH9M enhanced
L-model used NB9M-GS

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Title: Block Diagram

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2007/11/12 delete damp resistor

Clock Request	Clock Request Function
CR#3	Pull 475 ohm to ground(FOR ICH9)
CR#4	EXPRESS_CLK_DET#
CR#6	MINI_CARD_DET#
CR#7	CF_REQ_IN#
CR#9	MCH_CLK_REQ#
CR#10	ROBSON_CLK_DET#
CR#11	MINI_CARD_TV_DET#
CR#A	SATACLKREQ#

FSB Frequency Table:

close to clk gen (For EMI)

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

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Title: CLOCK GEN (SL28648LFXC)

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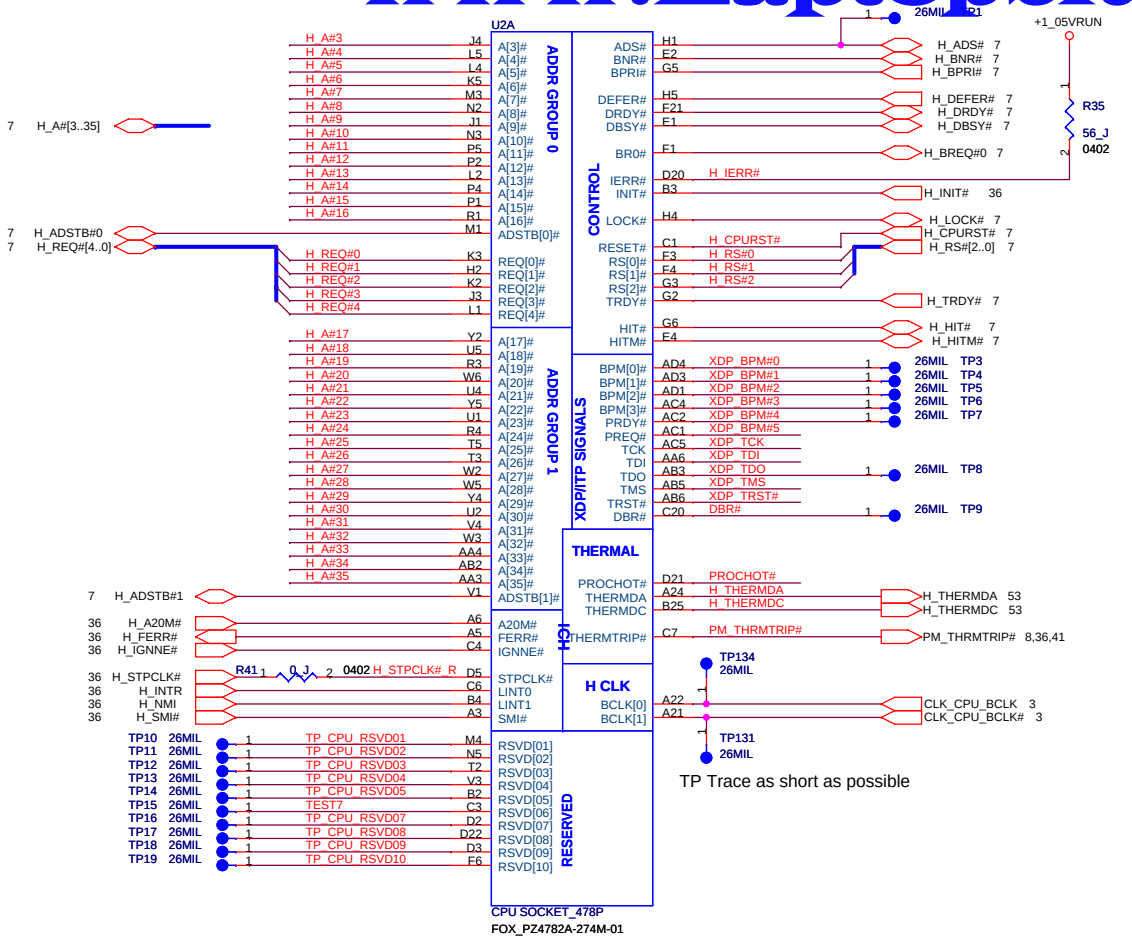
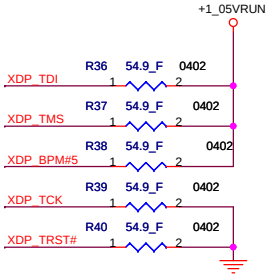
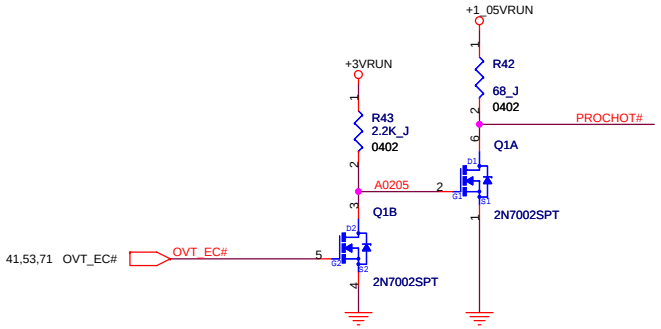


TP Trace as short as possible

as Close as possible to Pin out trace





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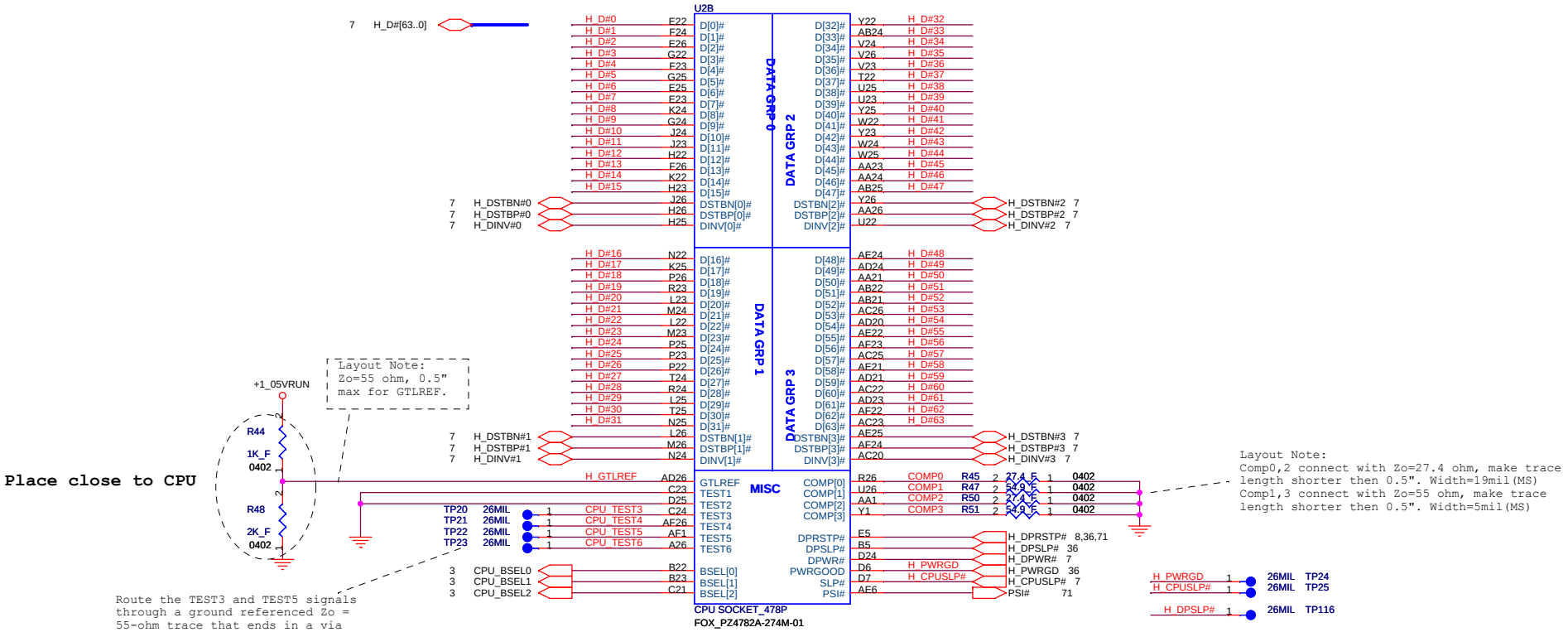

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Title	Penryn (HOST BUS) 2/3		
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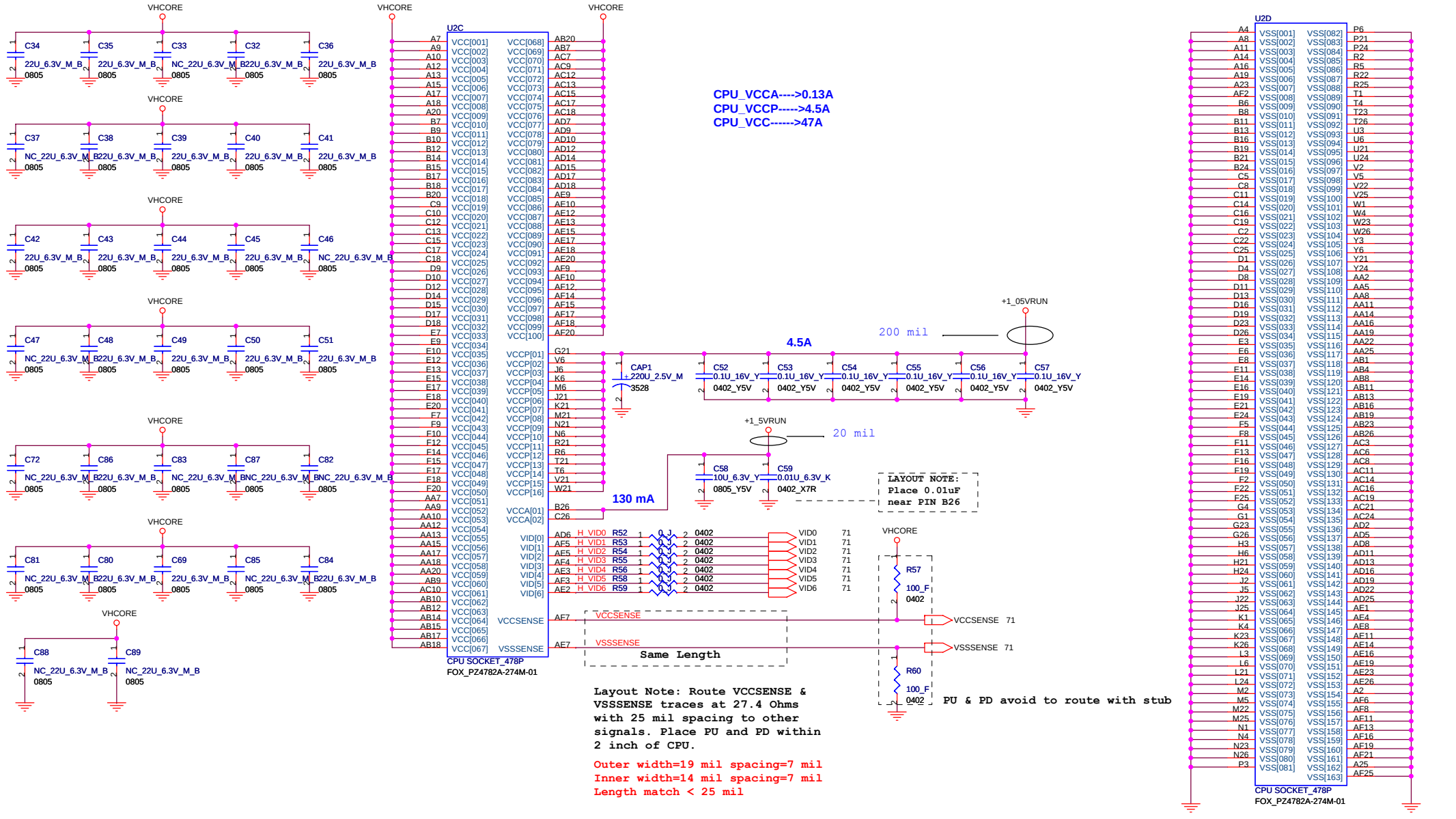

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Title	Penryn (HOST BUS) 3/3	
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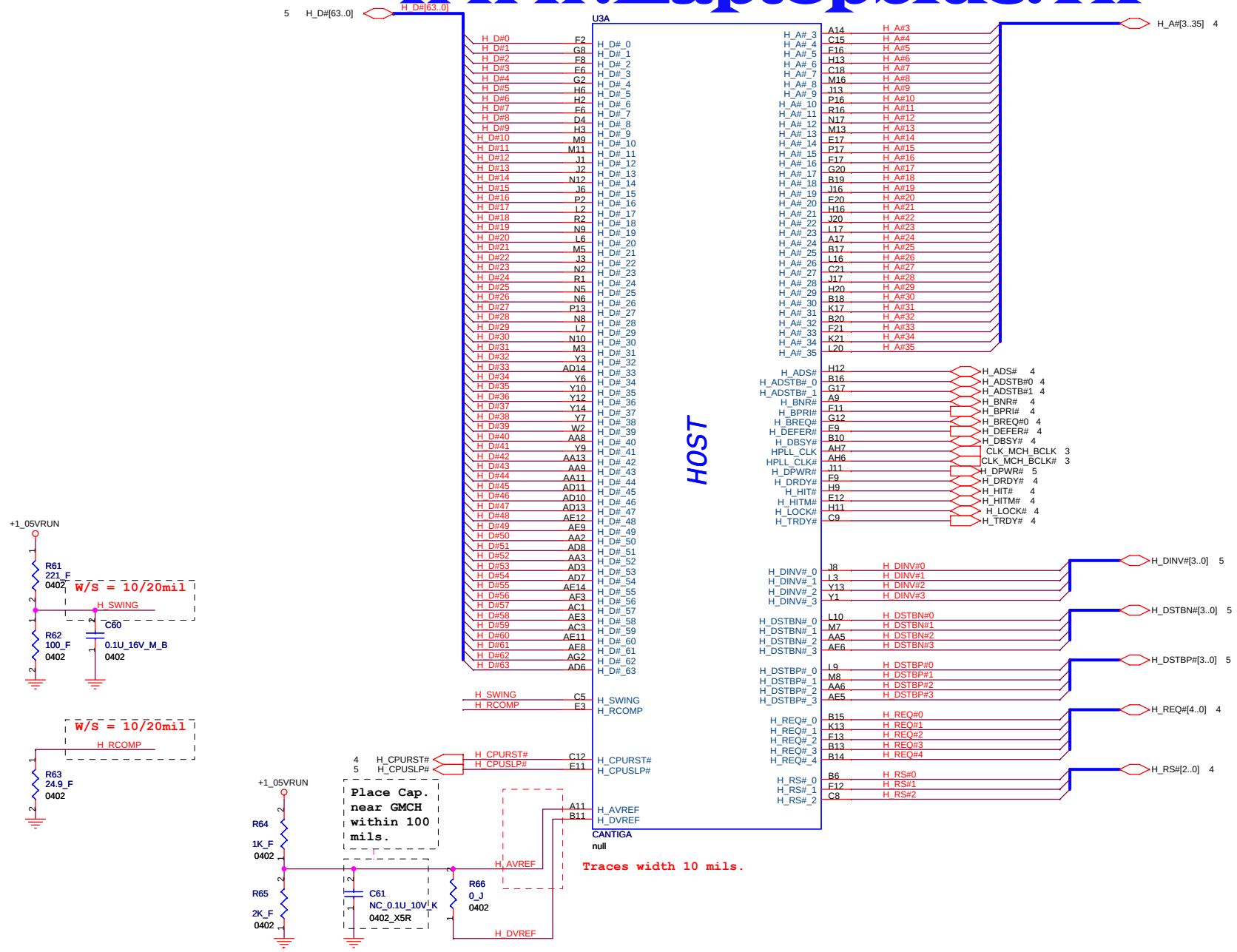

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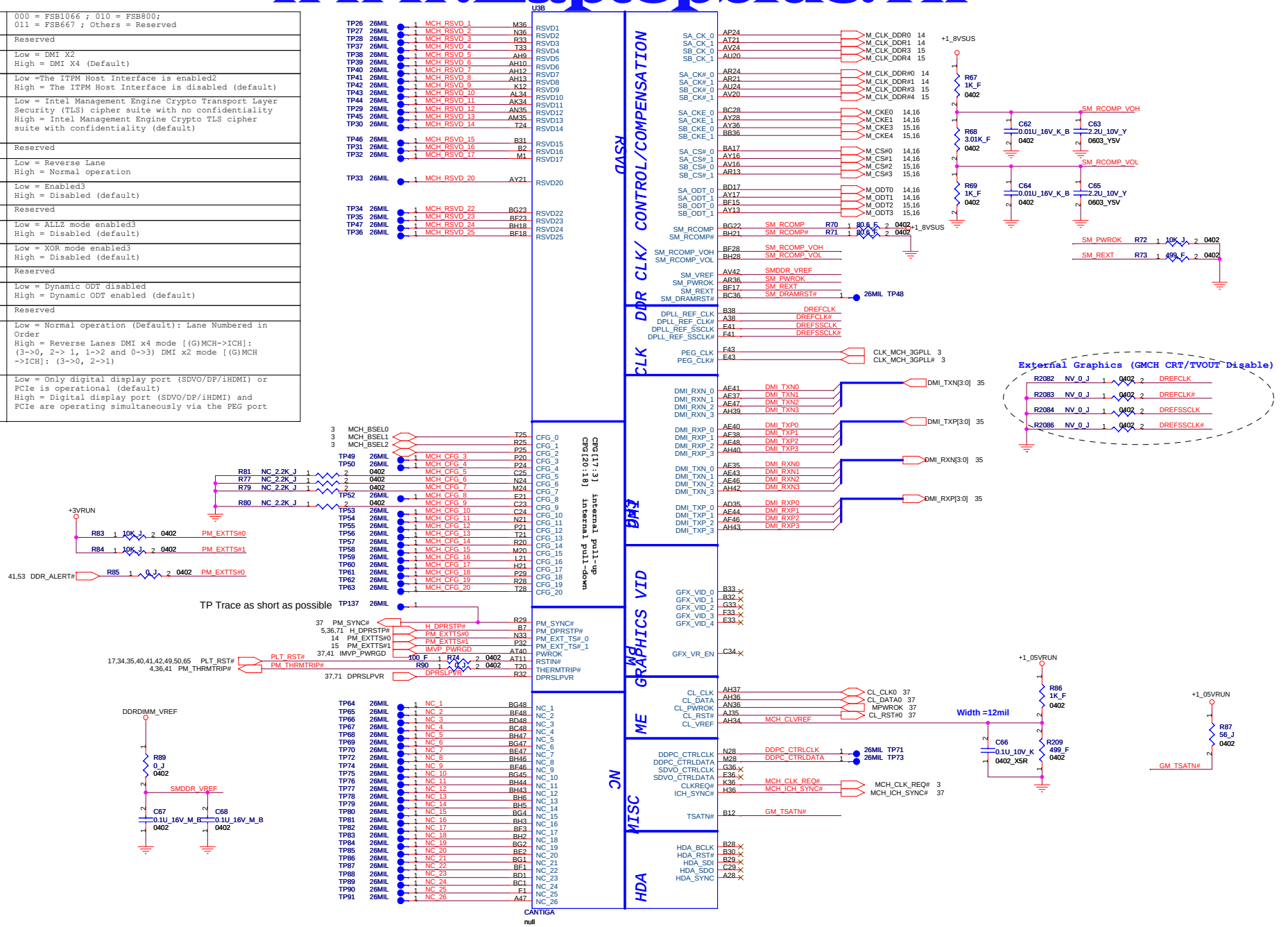
MCH_CFG_2~0 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Reverse Lane High = Normal operation
MCH_CFG_10 PCIE Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (DMI) 2/7	
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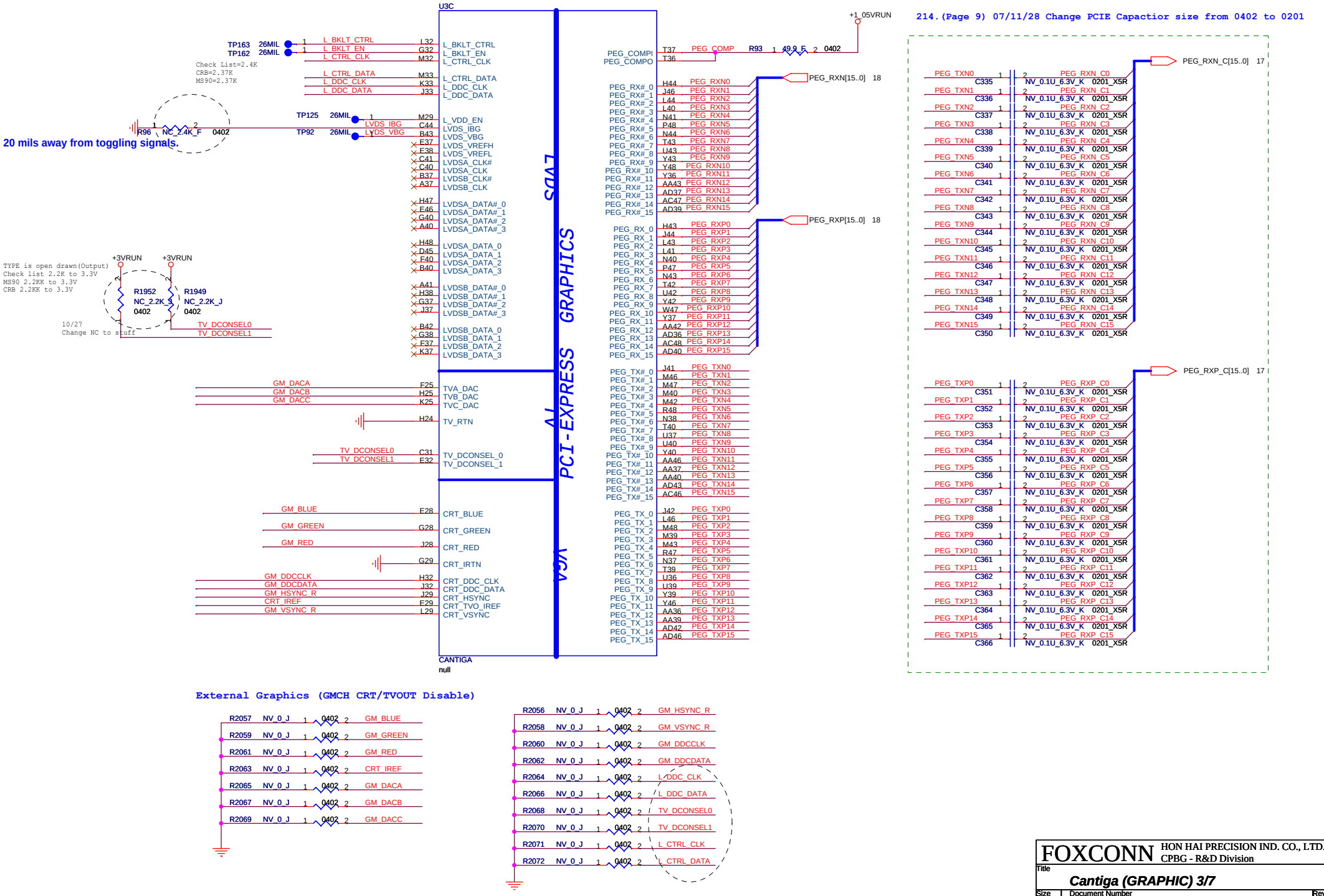
214.(Page 9) 07/11/28 Change PCIE Capactior size from 0402 to 0201

20 mils away from toggling signals.

External Graphics (GMCH CRT/TVOUT Disable)



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
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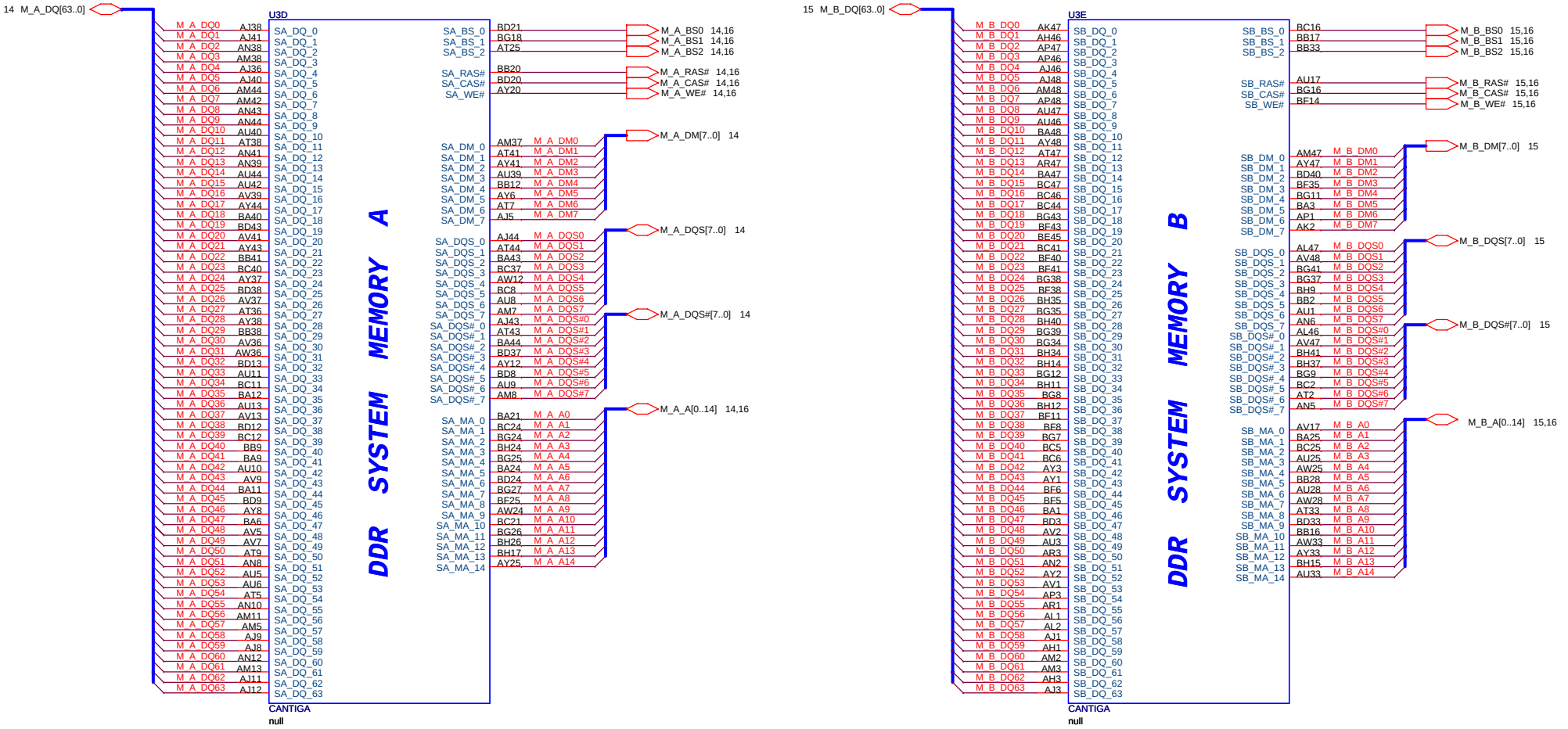

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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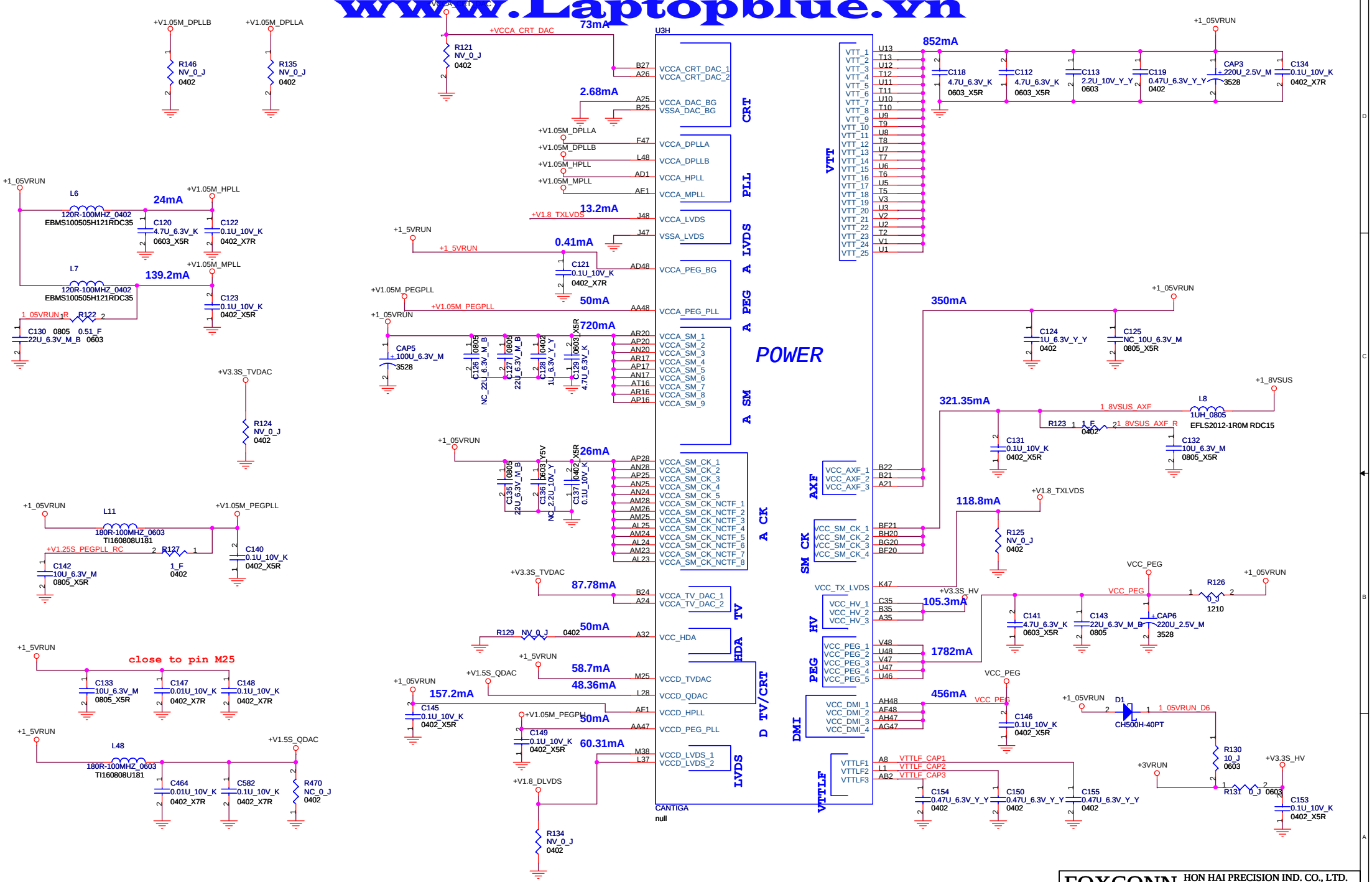

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Cantiga (POWER,VCC) 5/7	
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1.21A

U3F

+1_05VRUN

VCC CORE

POWER

CANTIGA

null

R136 0_J 0402

VCC_MCH_35

VCC NCTF

+1_05VRUN

3A

+1_8VSUS

U3G

VCC SM POWER

+VGFX_CORE

R149 0_J 0402

+1_05VRUN

CAP7 220U_2.5V_M 3528

C157 22U_6.3V_M_B 0805

C158 0.22U_10V_Y_Y 0402

C159 0.22U_10V_Y_Y 0402

C160 0.1U_10V_K 0402_X7R

308 mils from the Edge.

Cavity Capacitors

VCC_SM_36 VCC_SM_37 VCC_SM_38 VCC_SM_40 VCC_SM_42

C259 NC_0.1U_6.3V_K 0201_X5R

C248 NC_0.1U_6.3V_K 0201_X5R

C246 NC_0.1U_6.3V_K 0201_X5R

C247 NC_0.1U_6.3V_K 0201_X5R

C245 NC_0.1U_6.3V_K 0201_X5R

+1_8VSUS

C167 0.1U_10V_K 0402_X7R

CAP10 330U_2V_T EEFSX0D331ER

C168 22U_6.3V_M_B 0805

C169 22U_6.3V_M_B 0805

Place C837 where LVDS and DDR2 taps.

Place on the Edge.

6.326A

+VGFX_CORE

VCC GFX

VCC GFX NCTF

VCC SM LF

26MIL TP94 VCC_AXG_SENSE

26MIL TP95 VSS_AXG_SENSE

C170 0.1U_10V_K 0402_X7R

C171 0.1U_10V_K 0402_X7R

C173 0402

C174 0402

C172 0402

C175 1U_6.3V_M 0402_X5R

C176 1U_6.3V_M 0402_X5R

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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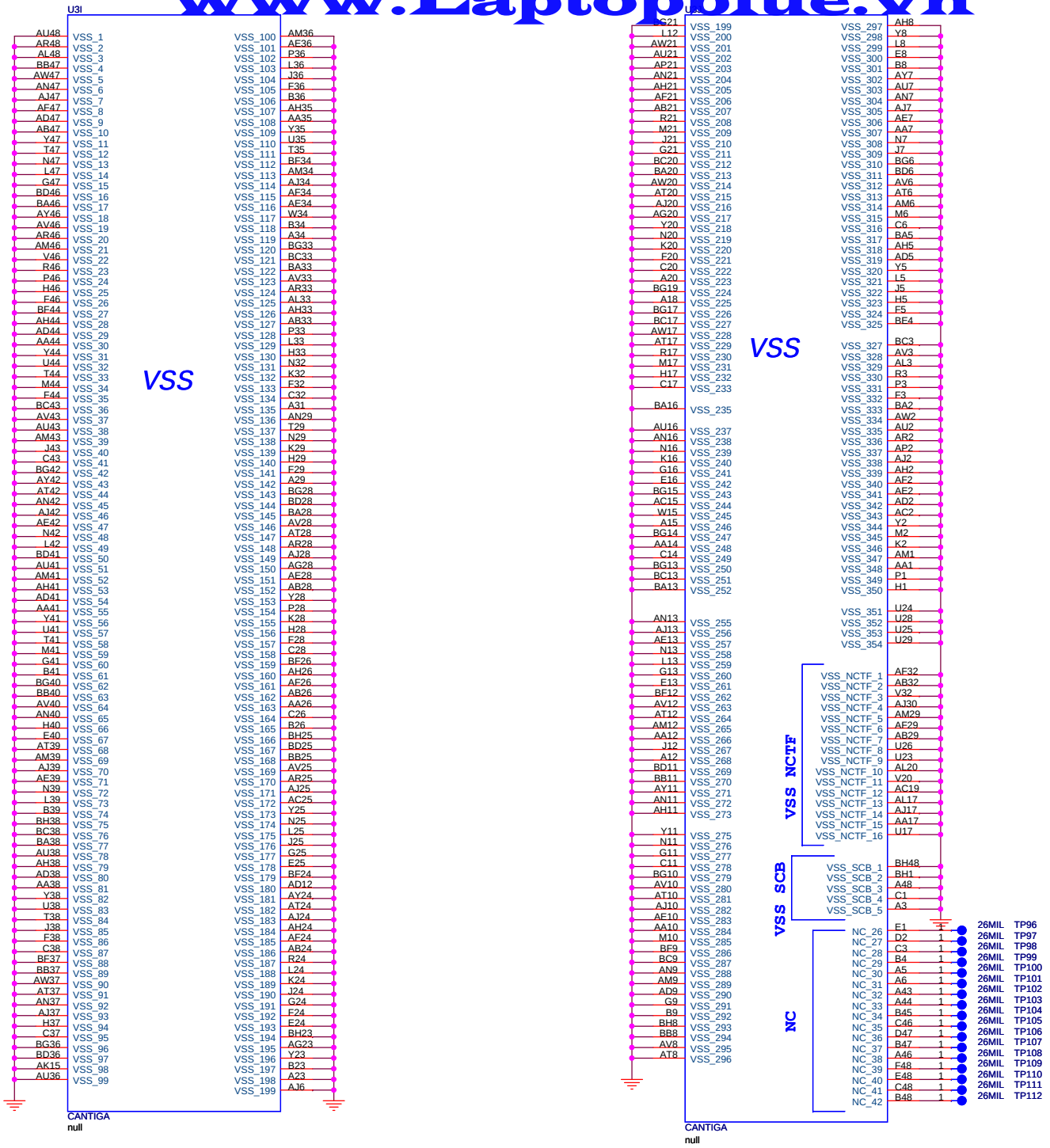

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
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1.8V per DIMM=3.08A Height = 5 mm

+1_8VSUS

C177 0.1U_16V_M_B 0402
C178 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

DDR2_VREF

CN2

1	VREF	VSS46	2				
3	VSS47	DQ4	4	M_A_DQ4			
5	DQ0	DQ5	6	M_A_DQ5			
7	DQ1	VSS15	8				
9	VSS37	DM0	10	M_A_DM0			
11	DQS#0	VSS5	12				
13	DQS0	DQ6	14	M_A_DQ6			
15	VSS48	DQ7	16	M_A_DQ7			
17	DQ2	VSS16	18				
19	DQ3	DQ12	20	M_A_DQ12			
21	VSS38	DQ13	22	M_A_DQ13			
23	DQ8	VSS17	24				
25	DQ9	DM1	26	M_A_DM1			
27	VSS49	VSS53	28				
29	DQS#1	CK0	30	M_CLK_DDR0 8			
31	DQS1	CK0#	32	M_CLK_DDR#0 8			
33	VSS39	VSS41	34				
35	DQ10	DQ14	36	M_A_DQ14			
37	DQ11	DQ15	38	M_A_DQ15			
39	VSS50	VSS54	40				
41	VSS18	VSS20	42				
43	DQ16	DQ20	44	M_A_DQ20			
45	DQ17	DQ21	46	M_A_DQ21			
47	VSS1	VSS6	48				
49	DQS#2	NC3	50	DDR2_EXTTS#0 R138 1 NC_0_J 2 0402 PM_EXTTS#0 8			
51	DQS2	DM2	52	M_A_DM2			
53	VSS19	VSS21	54				
55	DQ18	DQ22	56	M_A_DQ22			
57	DQ19	DQ23	58	M_A_DQ23			
59	VSS22	VSS24	60				
61	DQ24	DQ28	62	M_A_DQ28			
63	DQ25	DQ29	64	M_A_DQ29			
65	VSS23	VSS25	66				
67	DM3	DQS#3	68	M_A_DQS#3			
69	NC4	DQS3	70	M_A_DQS3			
71	VSS9	VSS10	72				
73	DQ26	DQ30	74	M_A_DQ30			
75	DQ27	DQ31	76	M_A_DQ31			
77	VSS4	VSS8	78				
79	CKE0	CKE1	80	M_CKE1 8,16			
81	VDD7	VDD8	82				
83	NC1	A15	84				
85	A16_BA2	A14	86	M_A_A14			
87	VDD9	VDD11	88				
89	A12	A11	90	M_A_A11			
91	A9	A7	92	M_A_A7			
93	A8	A6	94	M_A_A6			
95	VDD5	VDD4	96				
97	A5	A4	98	M_A_A4			
99	A3	A2	100	M_A_A2			
101	A1	A0	102	M_A_A0			
103	VDD10	VDD12	104				
105	A10/AP	BA1	106	M_A_BS1 10,16			
107	BA0	RAS#	108	M_A_RAS# 10,16			
109	WE#	S0#	110	M_CS#0 8,16			
111	VDD2	VDD1	112				
113	CAS#	ODT0	114	M_ODT0 8,16			
115	S1#	A13	116	M_A_A13			
117	VDD3	VDD6	118				
119	ODT1	NC2	120				
121	VSS11	VSS12	122				
123	DQ32	DQ36	124	M_A_DQ36			
125	DQ33	DQ37	126	M_A_DQ37			
127	VSS26	VSS28	128				
129	DQS#4	DM4	130	M_A_DM4			
131	DQS4	VSS42	132				
133	VSS2	DQ38	134	M_A_DQ38			
135	DQ34	DQ39	136	M_A_DQ39			
137	DQ35	VSS55	138				
139	VSS27	DQ44	140	M_A_DQ44			
141	DQ40	DQ45	142	M_A_DQ45			
143	DQ41	VSS43	144				
145	VSS29	DQS#5	146	M_A_DQS#5			
147	DM5	DQS5	148	M_A_DQS5			
149	VSS51	VSS56	150				
151	DQ42	DQ46	152	M_A_DQ46			
153	DQ43	DQ47	154	M_A_DQ47			
155	VSS40	VSS44	156				
157	DQ48	DQ52	158	M_A_DQ52			
159	DQ49	DQ53	160	M_A_DQ53			
161	VSS52	VSS57	162				
163	NCTEST	CK1	164	M_CLK_DDR1 8			
165	VSS30	CK1#	166	M_CLK_DDR#1 8			
167	DQS#6	VSS45	168				
169	DQS6	DM6	170	M_A_DM6			
171	VSS31	VSS32	172				
173	DQ50	DQ54	174	M_A_DQ54			
175	DQ51	DQ55	176	M_A_DQ55			
177	VSS33	VSS35	178				
179	DQ56	DQ60	180	M_A_DQ60			
181	DQ57	DQ61	182	M_A_DQ61			
183	VSS3	VSS7	184				
185	DM7	DQS#7	186	M_A_DQS#7			
187	VSS34	DQS7	188	M_A_DQS7			
189	DQ58	VSS36	190				
191	DQ59	DQ62	192	M_A_DQ62			
193	VSS14	DQ63	194	M_A_DQ63			
195	SDA	VSS13	196				
197	SCL	SA0	200	SA0_DIM0 R139 2 10K_J 1 0402			
199	VDD(SPD)	SA1	200	SA1_DIM0 R140 2 10K_J 1 0402			

SMDFIX1 SMDFIX2 NPTH1 NPTH2 201 202 203 204

DDR2_200P
FOX_AS0A426-N2RN-4F

DIMM_0

8,16 M_CKE0
10,16 M_A_BS2
10,16 M_A_BS0
10,16 M_A_WE#
10,16 M_A_CAS#
8,16 M_CS#1
8,16 M_ODT1

3,15,37,50 SMB_DATA_SUS
3,15,37,50 SMB_CLK_SUS
+3VRUN

C189 2.2U_10V_Y_Y 0603
C190 0.1U_16V_Y 0402_Y5V

M_A_DM[0..7] 10
M_A_DQ[0..63] 10
M_A_DQS[7..0] 10
M_A_DQS#[7..0] 10
M_A_A[0..14] 10,16

DDRDIMM_VREF
R137 0_J 0402
DDR2_VREF
DDR2_VREF
(20 mil)
C179 0.1U_16V_M_B 0402

Place these Caps near So-DIMM0
+1_8VSUS
C180 2.2U_10V_Y_Y 0603
C181 2.2U_10V_Y_Y 0603
C182 2.2U_10V_Y_Y 0603
C183 2.2U_10V_Y_Y 0603
C184 2.2U_10V_Y_Y 0603

Place these Caps near So-DIMM0
+1_8VSUS
CAP17 330U_6.3V_M 7.3x4.3x2.8
C185 0.1U_16V_Y_Y 0402
C186 0.1U_16V_Y_Y 0402
C187 0.1U_16V_Y_Y 0402
C188 0.1U_16V_Y_Y 0402

SMBus Address: A0H(W)/A1H(R)

Place DIMM_0 near GMCH

206.(Page 14) 07/11/27 change DDR2 CONN(CN1) from FOX_AS0A426-N5SN-7F to FOX_AS0A426_MN2RN_7F

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR(II)SO-DIMM_0	
Size A3	Document Number M780(MBX-194)	Rev 0.1
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1.8V per DIMM=3.08A Height = 4 mm

DDR2_VREF

C191 0.1U_16V_M_B 0402

C192 2.2U_10V_Y_Y 0603

0.1 µF and 2.2 µF placed close to VREF pins

+1_8VSUS

CN1

DDR2 SDRAM SO-DIMM (200P)

1	VREF	VSS46	2
3	VSS47	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS15	8
9	VSS37	DM0	10
11	DQS#0	VSS5	12
13	DQS0	DQ6	14
15	VSS48	DQ7	16
17	DQ2	VSS16	18
19	DQ3	DQ12	20
21	VSS38	DQ13	22
23	DQ8	VSS17	24
25	DQ9	DM1	26
27	VSS49	VSS53	28
29	DQS#1	CK0	30
31	DQS1	CK0#	32
33	VSS39	VSS41	34
35	DQ10	DQ14	36
37	DQ11	DQ15	38
39	VSS50	VSS54	40
41	VSS18	VSS20	42
43	DQ16	DQ20	44
45	DQ17	DQ21	46
47	VSS1	VSS6	48
49	DQS#2	NC3	50
51	DQS2	DM2	52
53	VSS19	VSS21	54
55	DQ18	DQ22	56
57	DQ19	DQ23	58
59	VSS22	VSS24	60
61	DQ24	DQ28	62
63	DQ25	DQ29	64
65	VSS23	VSS25	66
67	DM3	DQS#3	68
69	NC4	DQS3	70
71	VSS9	VSS10	72
73	DQ26	DQ30	74
75	DQ27	DQ31	76
77	VSS4	VSS8	78
79	CKE0	CKE1	80
81	VDD7	VDD8	82
83	NC1	A15	84
85	A16_BA2	A14	86
87	VDD9	VDD11	88
89	A12	A11	90
91	A9	A7	92
93	A8	A6	94
95	VDD5	VDD4	96
97	A5	A4	98
99	A3	A2	100
101	A1	A0	102
103	VDD10	VDD12	104
105	A10/AP	BA1	106
107	BA0	RAS#	108
109	WE#	S0#	110
111	VDD2	VDD1	112
113	CAS#	ODT0	114
115	S1#	A13	116
117	VDD3	VDD6	118
119	ODT1	NC2	120
121	VSS11	VSS12	122
123	DQ32	DQ36	124
125	DQ33	DQ37	126
127	VSS26	VSS28	128
129	DQS#4	DM4	130
131	DQS4	VSS42	132
133	VSS2	DQ38	134
135	DQ34	DQ39	136
137	DQ35	VSS55	138
139	VSS27	DQ44	140
141	DQ40	DQ45	142
143	DQ41	VSS43	144
145	VSS29	DQS#5	146
147	DM5	DQS5	148
149	VSS51	VSS56	150
151	DQ42	DQ46	152
153	DQ43	DQ47	154
155	VSS40	VSS44	156
157	DQ48	DQ52	158
159	DQ49	DQ53	160
161	VSS52	VSS57	162
163	NCTEST	CK1	164
165	VSS30	CK1#	166
167	DQS#6	VSS45	168
169	DQS6	DM6	170
171	VSS31	VSS32	172
173	DQ50	DQ54	174
175	DQ51	DQ55	176
177	VSS33	VSS35	178
179	DQ56	DQ60	180
181	DQ57	DQ61	182
183	VSS3	VSS7	184
185	DM7	DQS#7	186
187	VSS34	DQS7	188
189	DQ58	VSS36	190
191	DQ59	DQ62	192
193	VSS14	DQ63	194
195	SDA	VSS13	196
197	SCL	SA0	198
199	VDD(SPD)	SA1	200
201	GND1	GND2	202
203	NPTH1	NPTH2	204

DDR2_200P

FOX_AS0A426-NARN-4F

DIMM_1

M_B_DQ0 M_B_DQ1 M_B_DQS#0 M_B_DQS0 M_B_DQ2 M_B_DQ3 M_B_DQ8 M_B_DQ9 M_B_DQS#1 M_B_DQS1 M_B_DQ10 M_B_DQ11 M_B_DQ16 M_B_DQ17 M_B_DQS#2 M_B_DQS2 M_B_DQ18 M_B_DQ19 M_B_DQ24 M_B_DQ25 M_B_DM3 M_B_DQ26 M_B_DQ27 M_B_DQ32 M_B_DQ33 M_B_DQS#4 M_B_DQS4 M_B_DQ34 M_B_DQ35 M_B_DQ40 M_B_DQ41 M_B_DM5 M_B_DQ42 M_B_DQ43 M_B_DQ48 M_B_DQ49 M_B_DQS#6 M_B_DQS6 M_B_DQ50 M_B_DQ51 M_B_DQ56 M_B_DQ57 M_B_DM7 M_B_DQ58 M_B_DQ59

M_B_DQ4 M_B_DQ5 M_B_DM0 M_B_DQ6 M_B_DQ7 M_B_DQ12 M_B_DQ13 M_B_DM1 M_B_DQ14 M_B_DQ15 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ28 M_B_DQ29 M_B_DQS#3 M_B_DQS3 M_B_DQ30 M_B_DQ31 M_B_A14 M_B_A11 M_B_A7 M_B_A6 M_B_A4 M_B_A2 M_B_A0 M_B_DQ36 M_B_DQ37 M_B_DM4 M_B_DQ38 M_B_DQ39 M_B_DQ44 M_B_DQ45 M_B_DQS#5 M_B_DQS5 M_B_DQ46 M_B_DQ47 M_B_DQ52 M_B_DQ53 M_B_DM6 M_B_DQ54 M_B_DQ55 M_B_DQ60 M_B_DQ61 M_B_DQS#7 M_B_DQS7 M_B_DQ62 M_B_DQ63

M_CLK_DDR3 8
M_CLK_DDR#3 8
M_CLK_DDR4 8
M_CLK_DDR#4 8

DDR2_EXTTS#1 R141 1 NC_0_J 2 0402 PM_EXTTS#1 8

M_B_BS1 10,16
M_B_RAS# 10,16
M_CS#2 8,16
M_ODT2 8,16

8,16 M_CKE3
M_CKE4 8,16
10,16 M_B_BS2
10,16 M_B_BS0
10,16 M_B_WE#
10,16 M_B_CAS#
8,16 M_CS#3
8,16 M_ODT3

SA0_DIM1 R142 2 10K_J 1 0402
SA1_DIM1 R143 2 10K_J 1 0402
+3VRUN

3,14,37,50 SMB_DATA_SUS
3,14,37,50 SMB_CLK_SUS

C202 2.2U_10V_Y_Y 0603
C203 0.1U_16V_Y 0402_Y5V

M_B_DM[0..7] 10
M_B_DQ[0..63] 10
M_B_DQS[7..0] 10
M_B_DQS#[7..0] 10
M_B_A[0..14] 10,16

+1_8VSUS

Place these Caps near So-DIMM1.

C193 2.2U_10V_Y_Y 0603
C194 2.2U_10V_Y_Y 0603
C195 2.2U_10V_Y_Y 0603
C196 2.2U_10V_Y_Y 0603
C197 2.2U_10V_Y_Y 0603

+1_8VSUS

Place these Caps near So-DIMM1.

CAP18 330U_6.3V_M 7.3x4.3x2.8
C198 0.1U_16V_Y_Y 0402
C199 0.1U_16V_Y_Y 0402
C200 0.1U_16V_Y_Y 0402
C201 0.1U_16V_Y_Y 0402

SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0

207.(Page 14) 07/11/27 change DDR2 CONN(CN2) from FOX_AS0A426_N4RC_4F to FOX_AS0A426_MARN_7F

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	DDR(II)SO-DIMM_1
Size A3	Document Number M780(MBX-194) Rev 0.1
Date: Friday, June 13, 2008	Sheet 15 of 79

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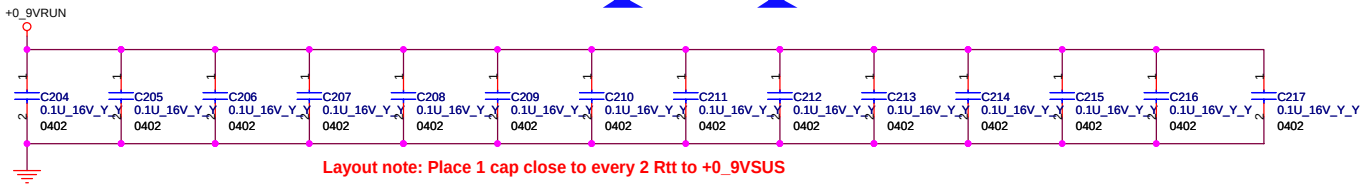
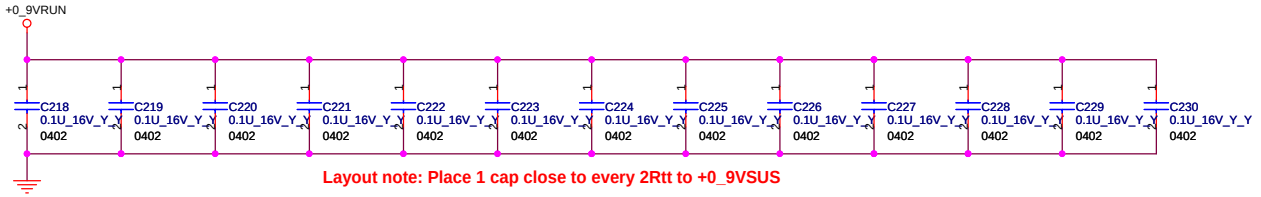


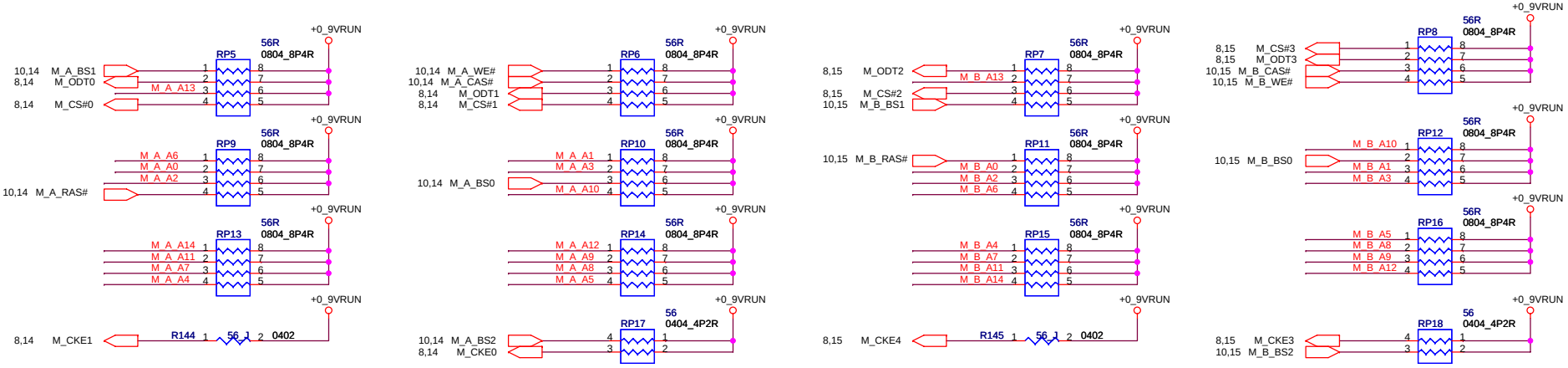
Layout note: Place 1 cap close to every 2 Rtt to +0_9VSUS



Layout note: Place 1 cap close to every 2Rtt to +0_9VSUS

10,14 M_A_A[0..14]

10,15 M_B_A[0..14]



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: DDR(II)Termination		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 16 of 79	

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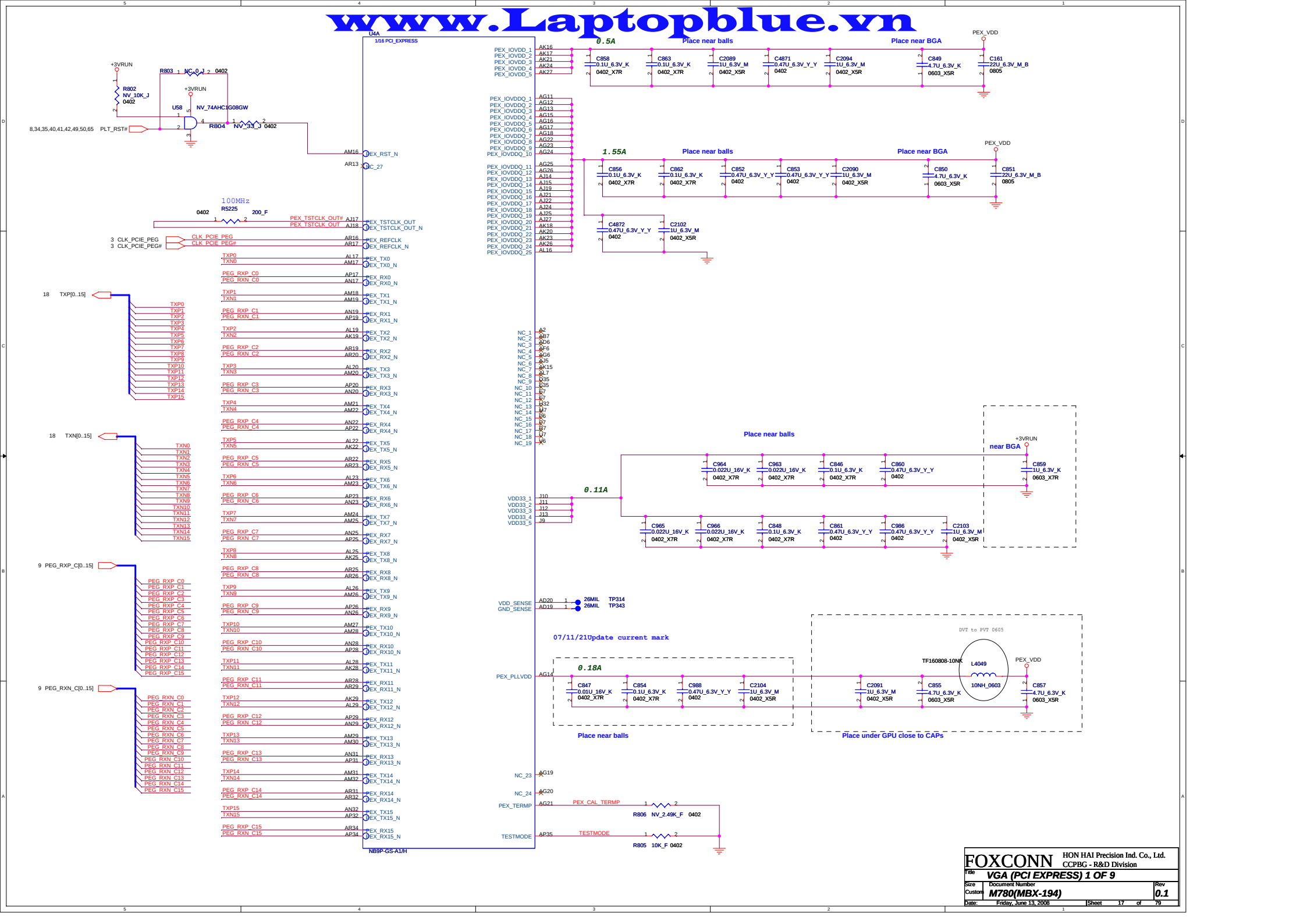

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	VGA (PCI EXPRESS) 1 OF 9
Size: Custom	Document Number: M780(MBX-194)
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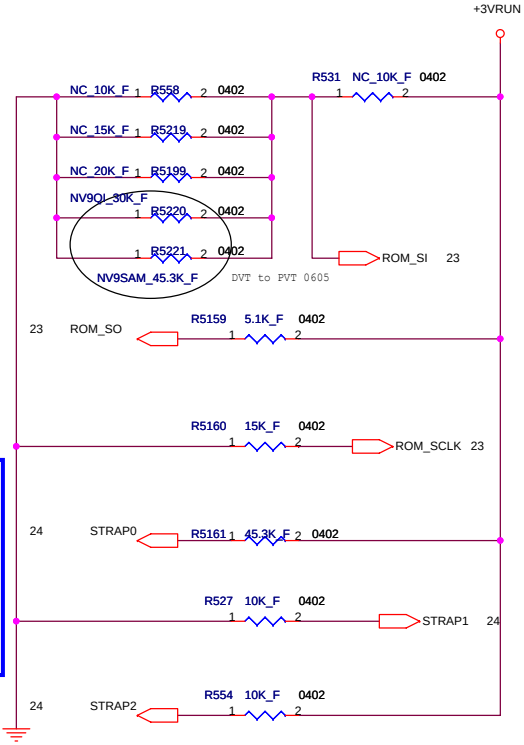
XCLK_277 0 (Reserved) 1 (27M Hz)	
NB9X TVMODE[2:0] 000	
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present)	ROM_SI (XXXX)
SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk)	ROM_SO (1000)
PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK (0010)
USER[3:0] 1000	STRAP0 (1111)
NB9X 3GIO_PADCFG[3:0] 0001	STRAP1 (0001)
NB9X PCI_DEVID[4:0] NB9P-GS X1001 NB9M-GS X1001	STRAP2 (1001)

<< ROM_SI Setting condition >>

H Model
=> 32Mx32bx4 - 0101 Qimonda - 30K pull Low

M Model
=> 32Mx32bx4 - 0101(Qimonda) - 30K pul Low

L Model
=> 32Mx32bx2 - 0101 Qimonda - 30K pull Low



0100 64-bit Reserved
0101 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung

0000 64-bit Reserved
0001 16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010 16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011 16Mx32 GDDR3 - 136 ball 64-bit Samsung

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-03276-001_v01_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: VGA (PCI-EXPRESS/STRAP) 2 OF 9

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

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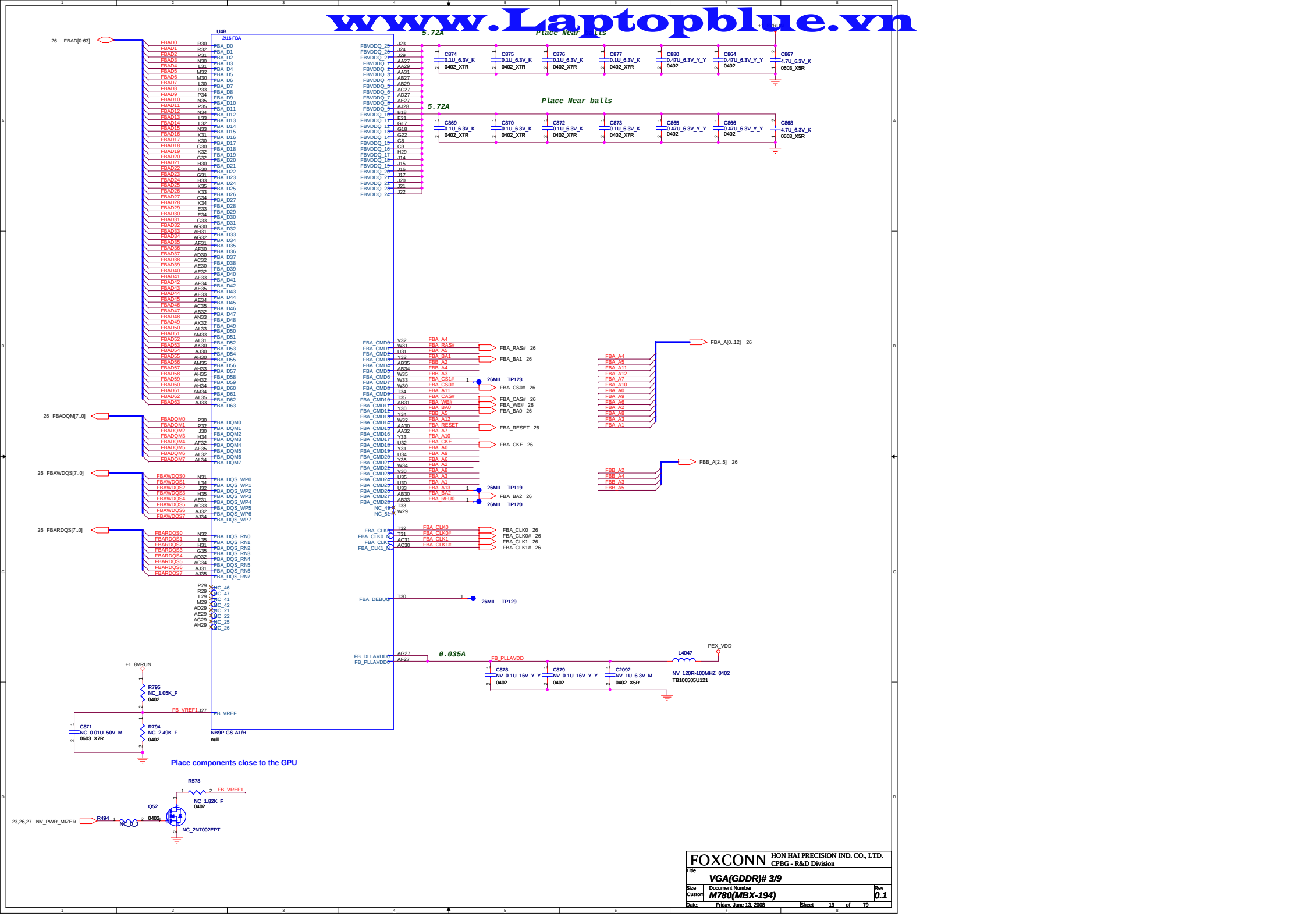

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(GDDR)# 3/9	
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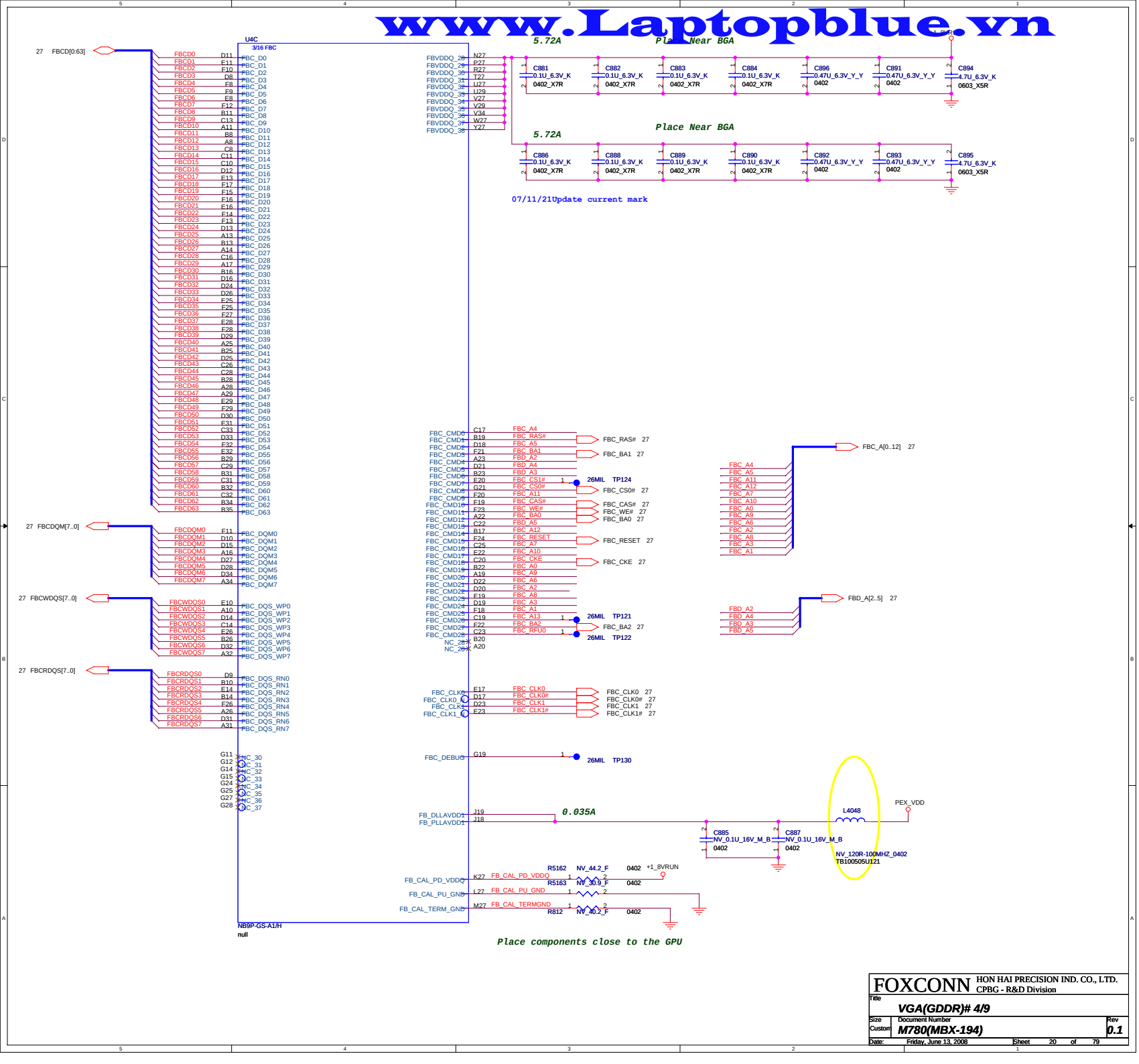

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA(GDDR)# 4/9	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
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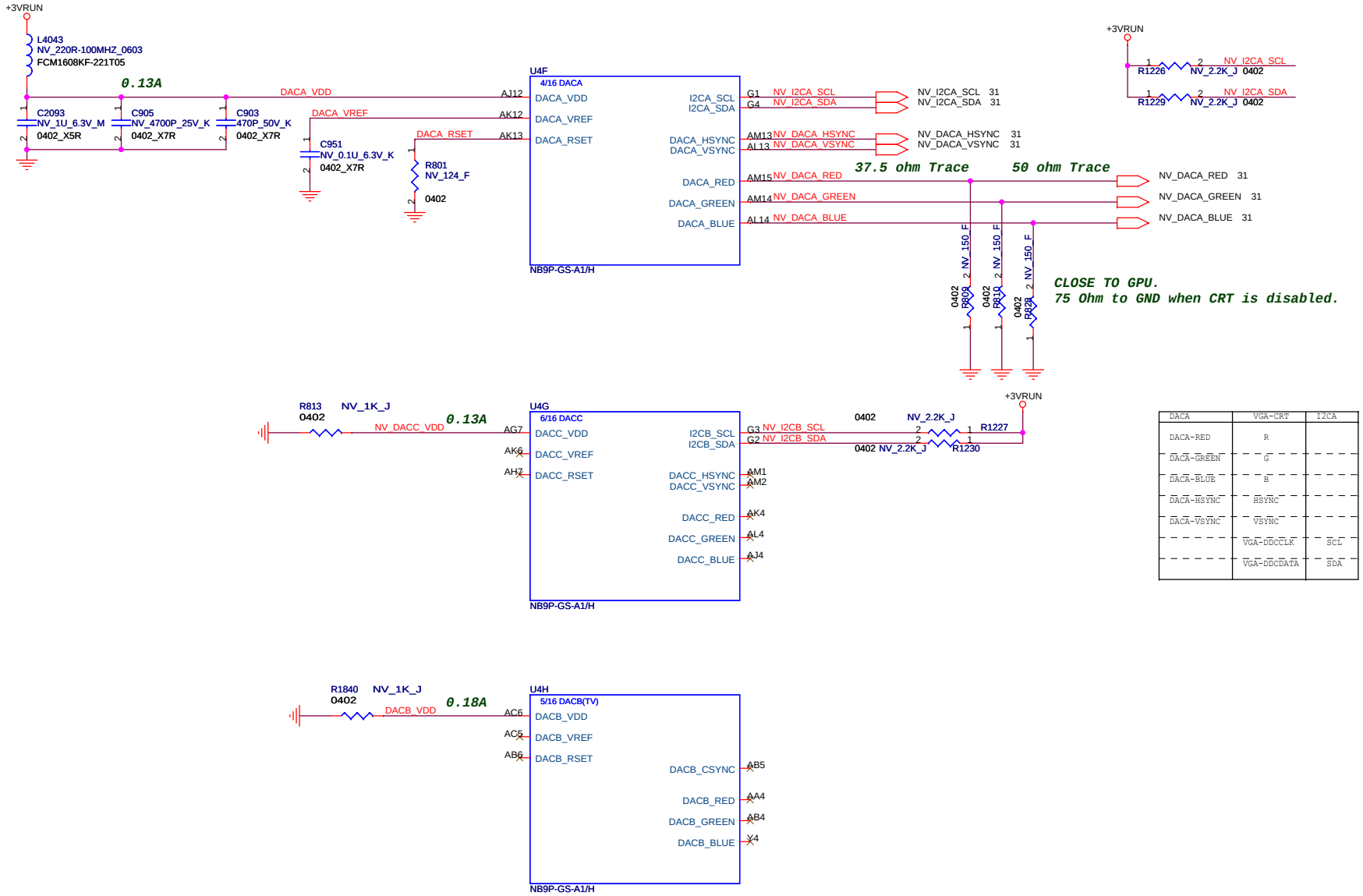

DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (CRT)5/9

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

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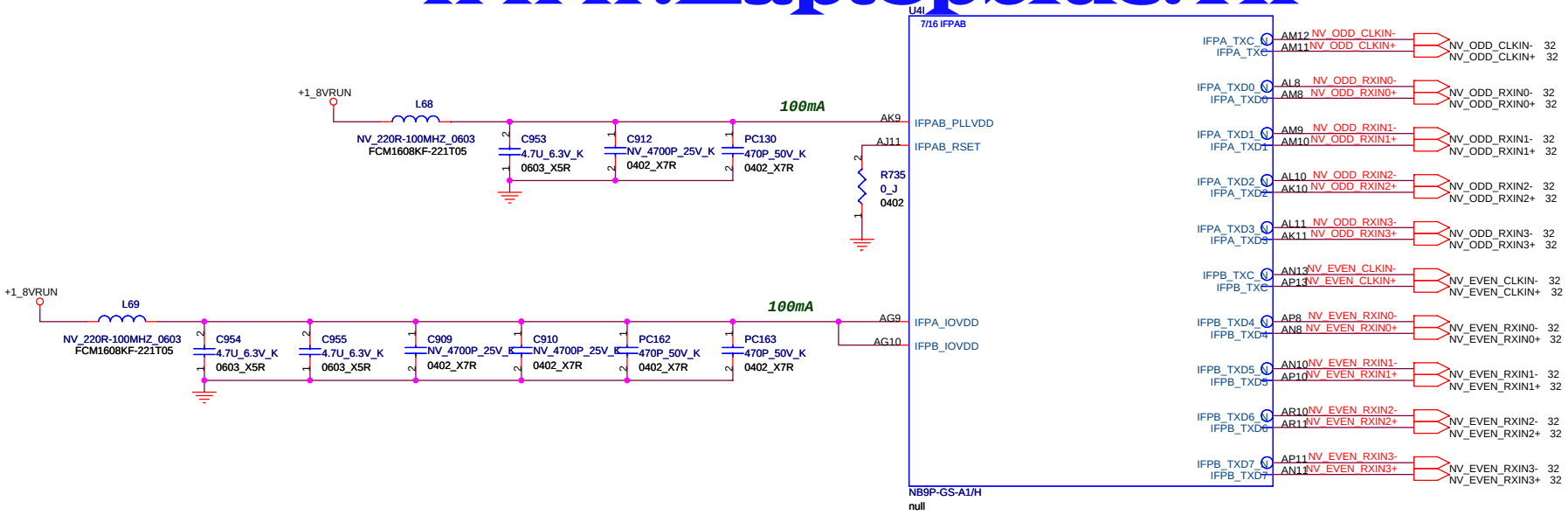

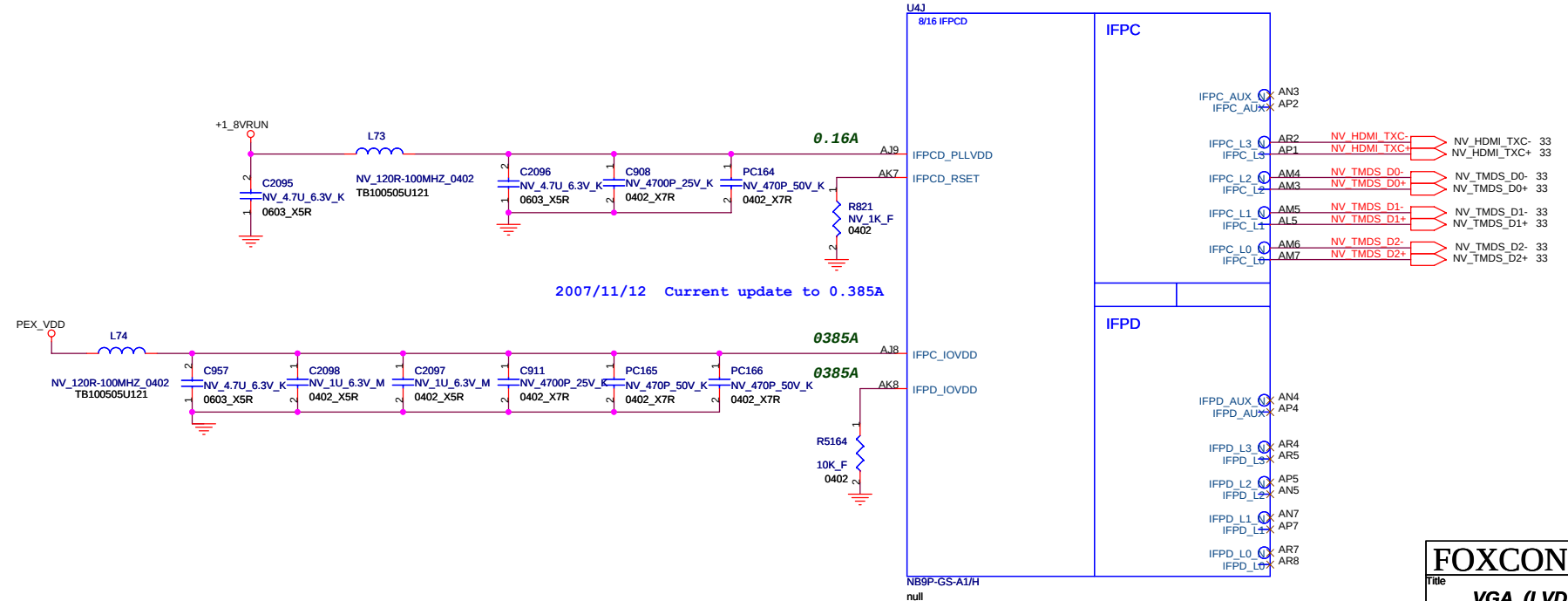

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (LVDS/TMDS) 6/9

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

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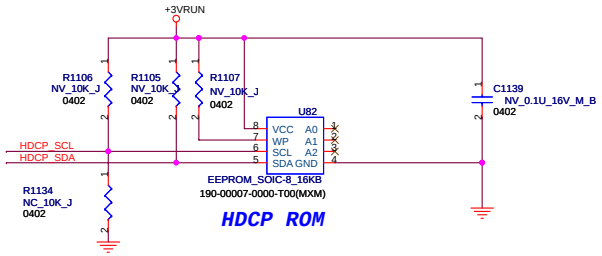
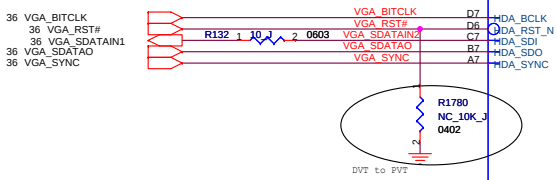
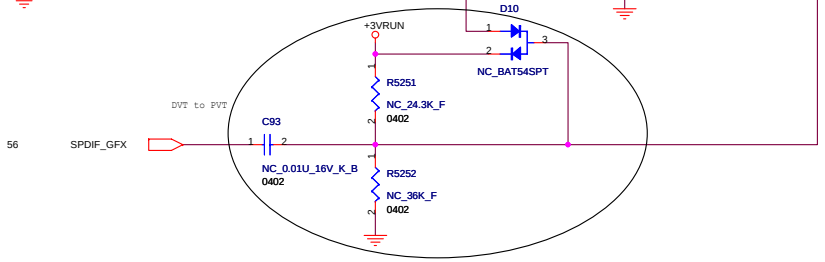
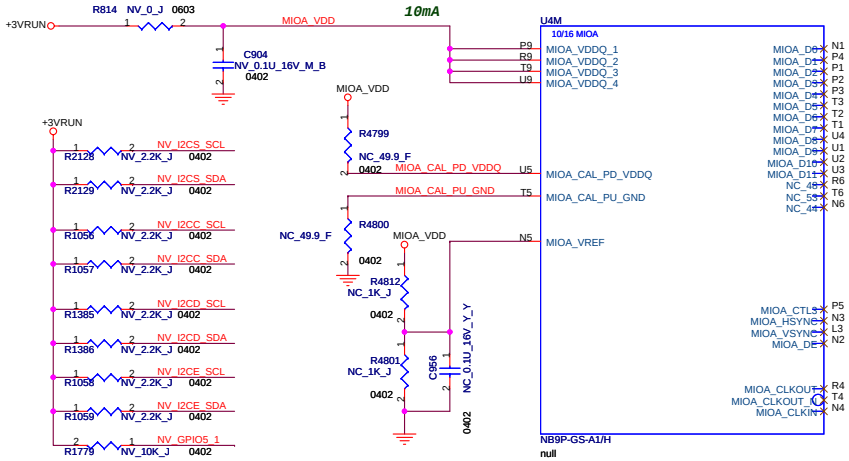
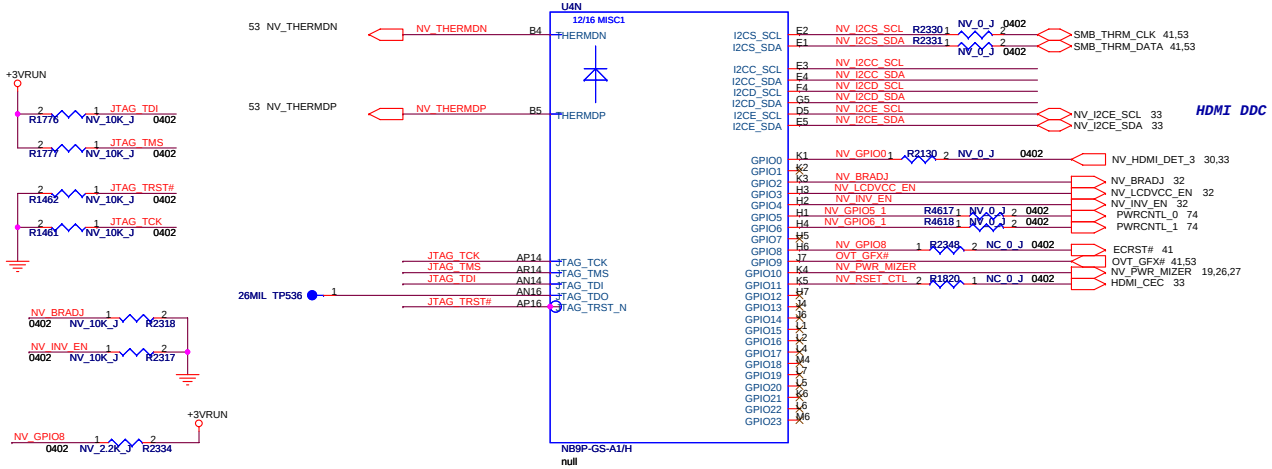








GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)	**Active High**
GPIO1	I	Yes		
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	**Active High**
GPIO3	O	No	Panel Power(LCD0_VDD)	**Active High**
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	**Active High**
GPIO5	O	Yes	FOR NVDD 0.9V~1.17V	**Active High**
GPIO6	O	No	reserve for NVDD adjust.	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	**Active Low**
GPIO10	O	No	Memory Vref switch(MEM VREF)	**Active High**
GPIO11	I/O	No	HDMI CEC Function Backup	



SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(All Other I2C_Compatibal Bus Signals)
I2CD_SCL I2CD_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CE_SCL I2CE_SDA	I/O	Notebook DVI I2C_Compatibal Bus Signals
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (XTAL/GPIO) 7/9

Size: Custom | Document Number: M780(MBX-194) | Rev: 0.1

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PEX_VDD

close GPU BALL

L66

C898 1U_25V_K_B 0603

NV_120R-100MHZ_0402 TB100505U121

C907 NV_1U_25V_K_B 0603

C906 NV_0.1U_16V_M_B 0402

C902 NV_1U_25V_K_B 0603

C899 NV_1U_25V_K_B 0603

C900 NV_4700P_25V_K 0402_X7R

C901 NV_0.1U_16V_M_B 0402

0.14A

U4E

AF9 PLLVDD

AD9 VID_PLLVDD

AF9 SP_PLLVDD

3 R_XTALSSIN R797 NV_0_J 0402 XTALSSIN D2 XTAL_SSIN

3 R_NV_XTALIN R796 NV_0_J 0402 NV_XTALIN B1 XTAL_IN

XTAL_OUTBUFF D1 XTALOUTBUFF

XTAL_OUT B2 NV_XTALOUT 1 26MIL TP345

NB9P-GS-A1/H

null

NB9M: XTALIN use 3.3V level

R1135 NV_10K_J 0402

R586 NC_10M_J 0402

NV_XTALIN 1 2 NV_XTALOUT

R590 NC_0_J 0402

Y8 NC_27MHZ_20P_20PPM ITTI_L5020-27.000-20

NC_27P_50V_J_N C945 0402

NC_27P_50V_J_N C944 0402

DVT to PVT

+3VRUN

R1542 NC_10K_J 0402

SS_S0

R1543 NC_10K_J 0402

C996 NC_1U_10V_Y_Y 0603

C828 1000P_50V_M_B 0402

R332 NC_10K_J 0402

XTALOUTBUFF R336 NC_22_J 0402 XTALOUTBUFF_R

SS_S0 VGA27MSSOUT

XTALSSIN R334 NC_22_J 0402

R333 NC_10K_J 0402

R335 NC_10K_J 0402

U26

X1/ICLK X2

GND VDD

S0 PD#

SSCLK REFCLK

NC_MK1726-08

REFCLK1 1 TP161 26MIL

Tis chip can use MK1726 or P1819B

R823 NV_0_J 0603

10mA

+3VRUN

MIOB_VDD

C943 NV_0.1U_16V_M_B 0402

U4L

11/16 MIOB

AA9 MIOB_VDDQ_1

AB9 MIOB_VDDQ_2

W9 MIOB_VDDQ_3

Y9 MIOB_VDDQ_4

AA7 MIOB_CAL_PD_VDDQ

AA6 MIOB_CAL_PU_GND

AF1 MIOB_VREF

MIOB_D0 Y1

MIOB_D1 Y2

MIOB_D2 Y3

MIOB_D3 AB3

MIOB_D4 AB2

MIOB_D5 AB1

MIOB_D6 AC4

MIOB_D7 AC1

MIOB_D8 AC2

MIOB_D9 AC3

MIOB_D10 AE3

MIOB_D11 AE2

NC_50 U6

NC_51 W6

NC_52 Y6

STRAP0 W5 STRAP0

STRAP1 W7 STRAP1

STRAP2 V7 STRAP2

STRAP0 18

STRAP1 18

STRAP2 18

MIOB_CTL3 W3

MIOB_HSYNC W1

MIOB_VSYNC W2

MIOB_DE Y5

MIOB_CLKOUT V4

MIOB_CLKOUT_N W4

MIOB_CLKIN AE1 MIOB_CLKIN 2 0402 1

R1941 NV_10K_J

NB9P-GS-A1/H

null

U4K

9/16 IFPEF

IFPE

AJ6 IFPEF_PLLVDD

AL1 IFPEF_RSET

R5170 10K_F 0402

IFPE_AUX_N AD4

IFPE_AUX AE4

IFPE_L3_N AE5

IFPE_L3 AE6

IFPE_L2_N AF5

IFPE_L2 AF4

IFPE_L1_N AG4

IFPE_L1 AH4

IFPE_L0_N AH5

IFPE_L0 AH6

AE7 IFPE_IOVDD

AD7 IFPF_IOVDD

IFPF

IFPF_AUX_N AF2

IFPF_AUX AF3

IFPF_L3_N AH3

IFPF_L3 AH2

IFPF_L2_N AH1

IFPF_L2 AJ1

IFPF_L1_N AJ2

IFPF_L1 AJ3

IFPF_L0_N AL3

IFPF_L0 AL2

NB9P-GS-A1/H

null

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (INTER DISPLAY) 8/9

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

Date: Tuesday, June 17, 2008 | Sheet 24 of 79

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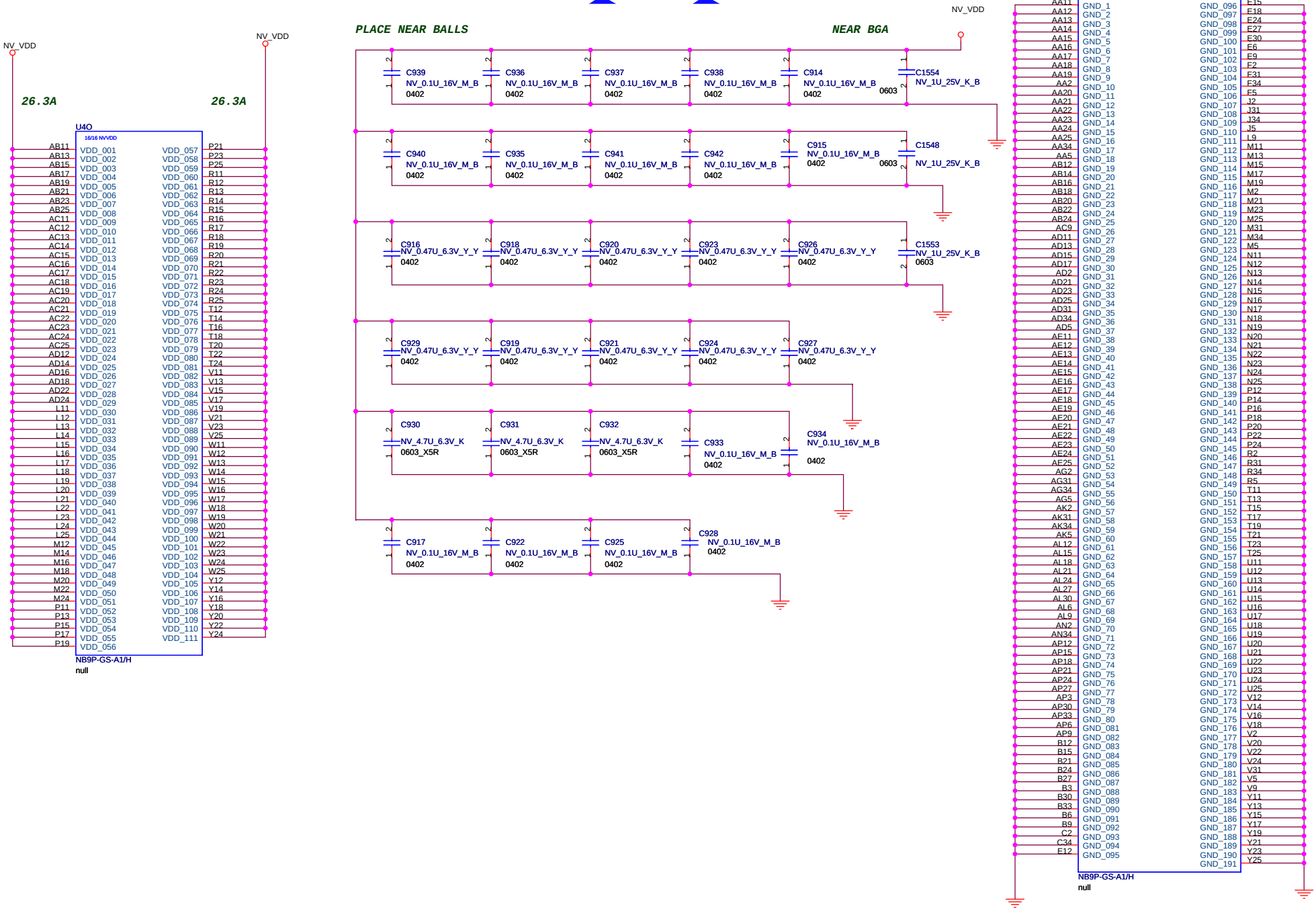

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA(POWER/GROUND) 9/9

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

Date: Friday, June 13, 2008 | Sheet 25 of 79

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MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

NV_PWR_MIZER	VREF	
	H	50%
	L	70%

R66,R85 (120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(GDDR)# 1/2	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 26 of 79	

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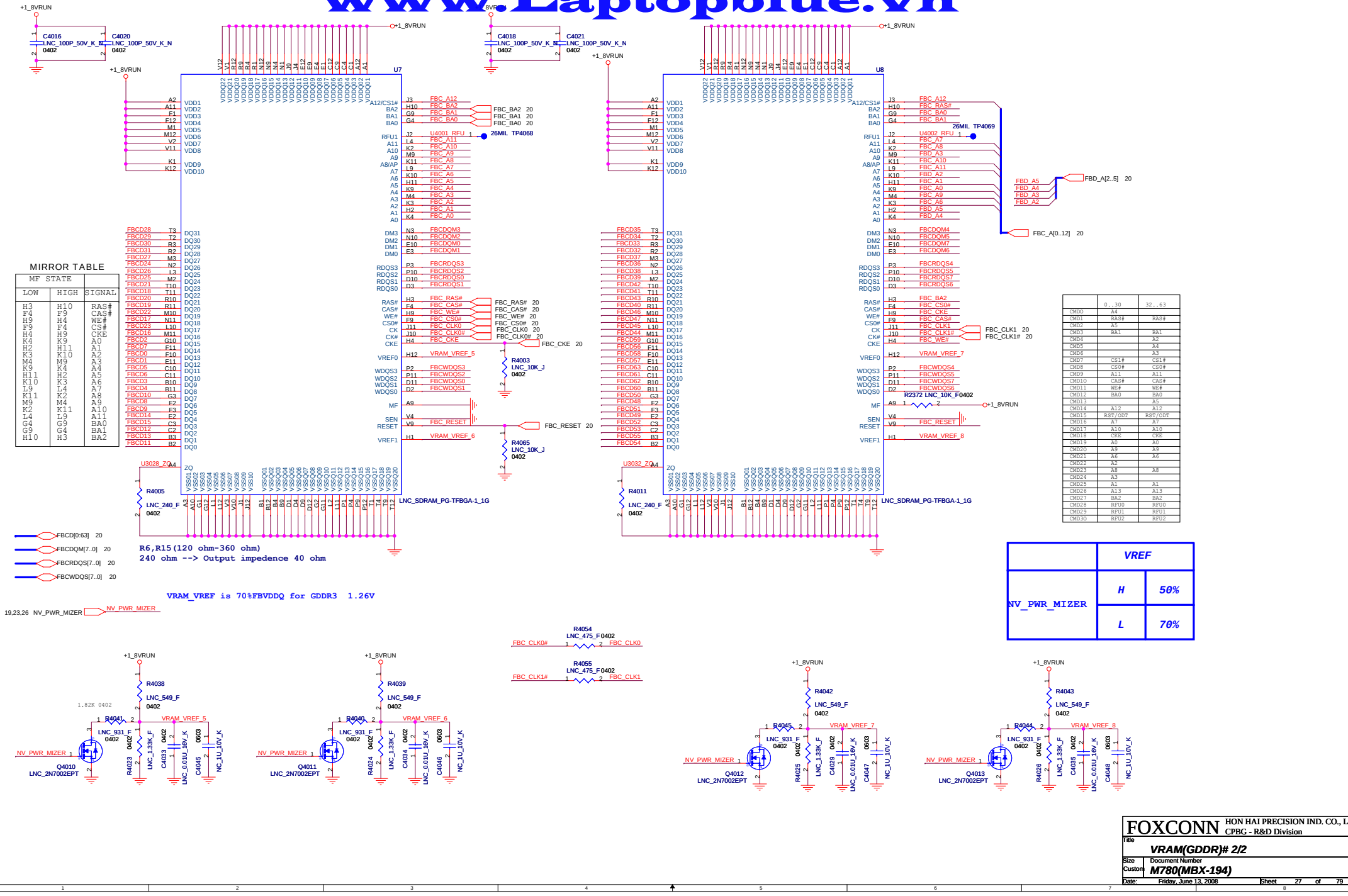

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

	VREF	
NV_PWR_MIZER	H	50%
	L	70%

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM(GDDR)# 2/2	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
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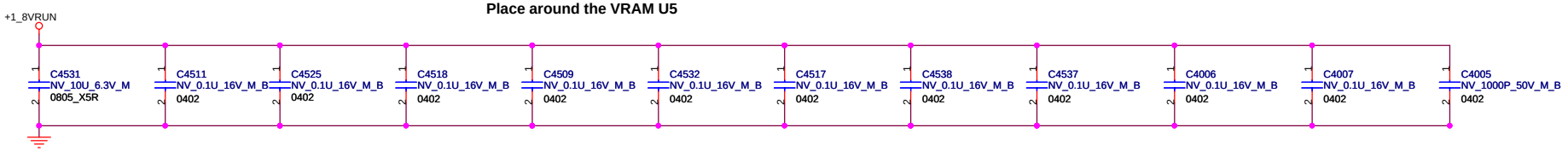
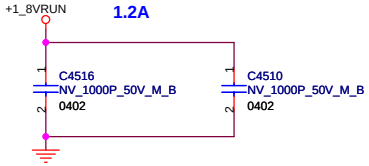
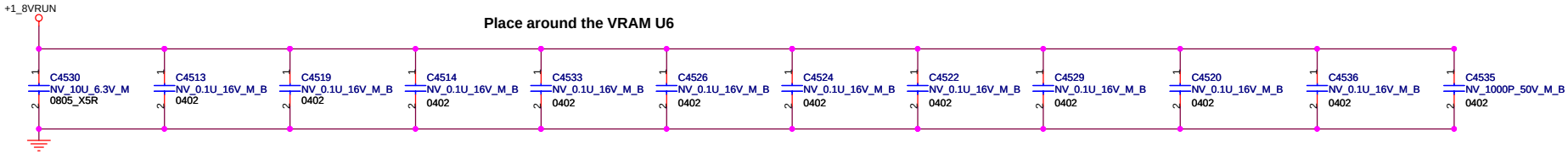
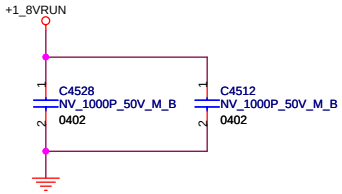
Place around the VRAM U5





Place around the VRAM U6





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM (POWERBYPASS) 1 OF 2	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 28 of 79	

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+1_8VRUN

Place around the VRAM U7

C4540 LNC_10U_6.3V_M 0805_X5R
C4543 LNC_0.1U_16V_M_B 0402
C4554 LNC_0.1U_16V_M_B 0402
C4544 LNC_0.1U_16V_M_B 0402
C4563 LNC_0.1U_16V_M_B 0402
C4565 LNC_0.1U_16V_M_B 0402
C4541 LNC_0.1U_16V_M_B 0402
C4552 LNC_0.1U_16V_M_B 0402
C4548 LNC_0.1U_16V_M_B 0402
C4545 LNC_0.1U_16V_M_B 0402
C4549 LNC_0.1U_16V_M_B 0402
C4550 LNC_1000P_50V_M_B 0402
C993 1000P_50V_K 0402_X7R

+1_8VRUN

1.2A

C4551 LNC_1000P_50V_M_B 0402
C4546 LNC_1000P_50V_M_B 0402

+1_8VRUN

Place around the VRAM U8

C4634 LNC_10U_6.3V_M 0805_X5R
C4637 LNC_0.1U_16V_M_B 0402
C4595 LNC_0.1U_16V_M_B 0402
C4053 LNC_0.1U_16V_M_B 0402
C4636 LNC_0.1U_16V_M_B 0402
C4638 LNC_0.1U_16V_M_B 0402
C4073 LNC_0.1U_16V_M_B 0402
C4597 LNC_0.1U_16V_M_B 0402
C4058 LNC_0.1U_16V_M_B 0402
C4588 LNC_0.1U_16V_M_B 0402
C4628 LNC_0.1U_16V_M_B 0402
C4604 LNC_1000P_50V_M_B 0402

+1_8VRUN

C4630 LNC_1000P_50V_M_B 0402
C4625 LNC_1000P_50V_M_B 0402

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***VRAM (POWERBYPASS) 2 OF 2***	
Size A3	Document Number ***M780(MBX-194)***	Rev ***0.1***
Date: Friday, June 13, 2008	Sheet 29 of 79	

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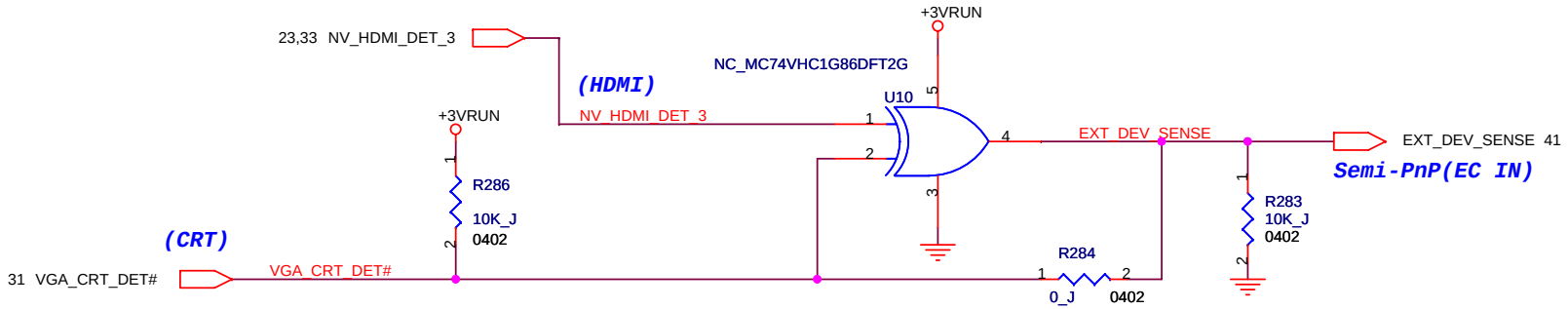
Semi-PnP Circuit



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Semi-PnP		
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 30 of 79	

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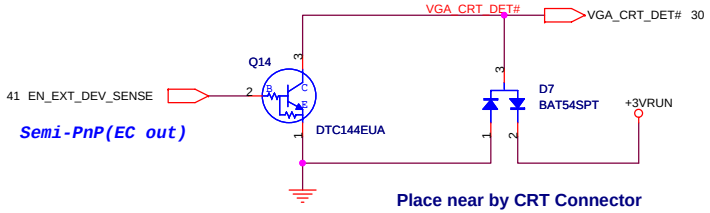
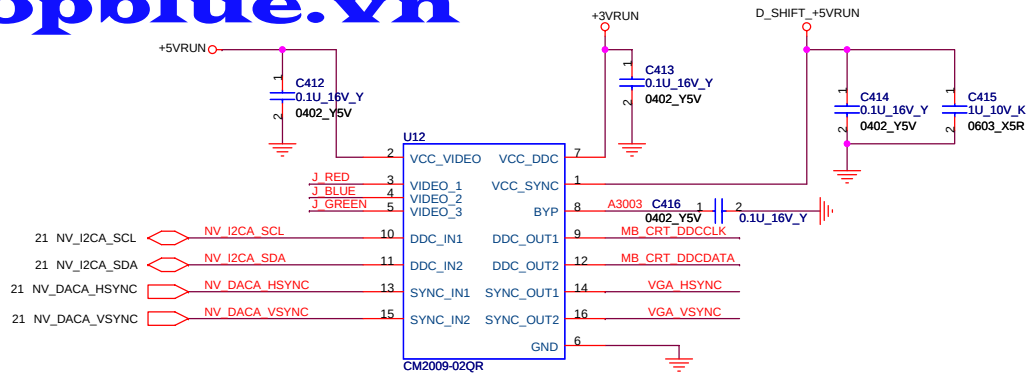
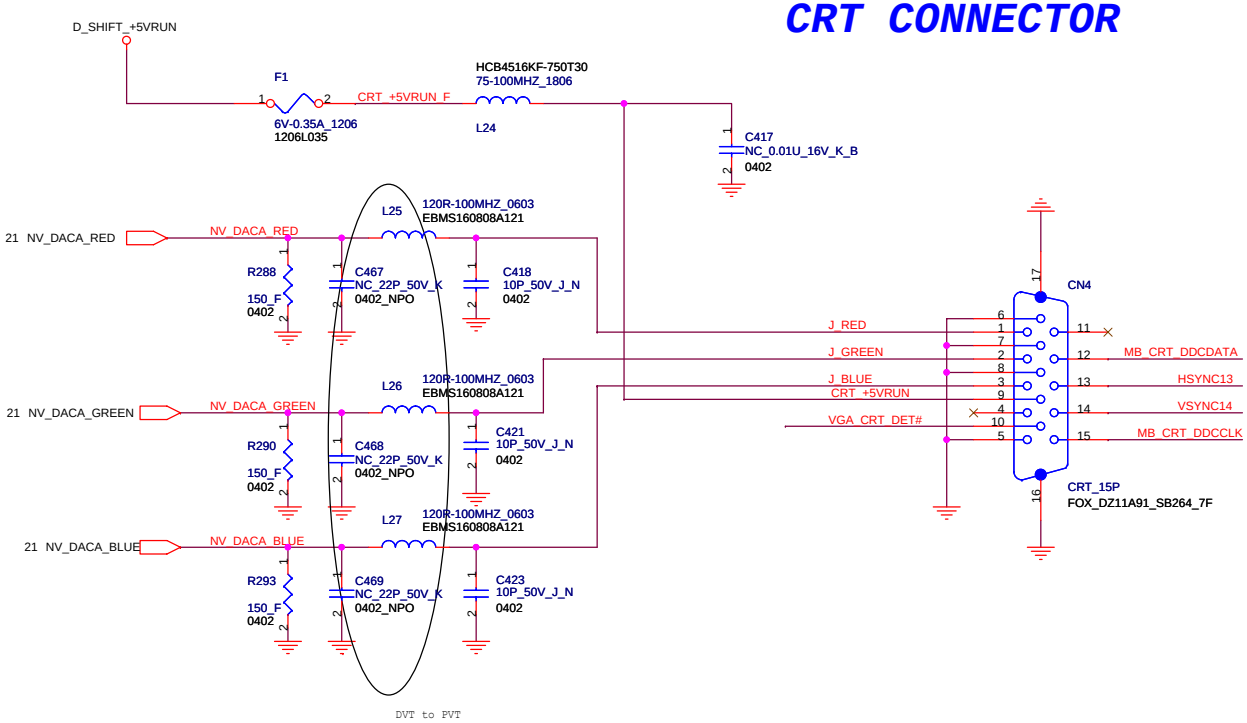
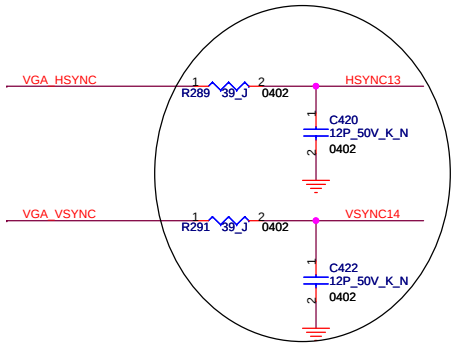
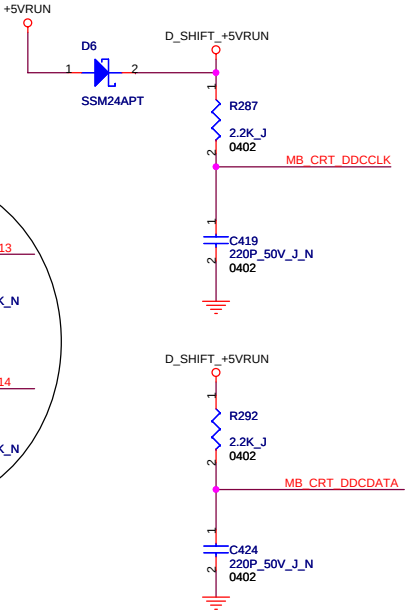
CRT CONNECTOR











FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
Date: Thursday, June 26, 2008	Sheet 31 of 79	

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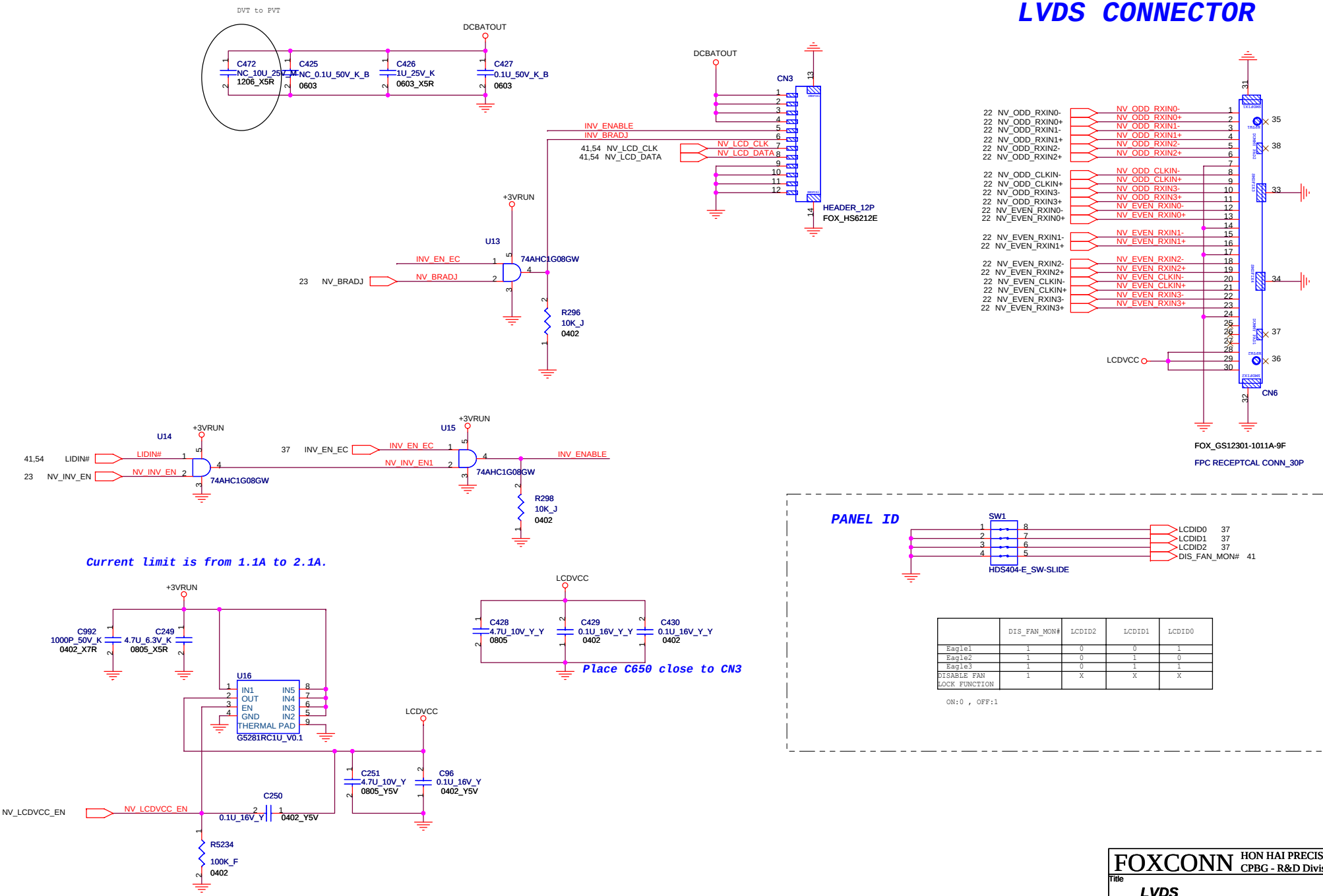
BLU CONNECTOR

LVDS CONNECTOR



	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
Eagle1	1	0	0	1
Eagle2	1	0	1	0
Eagle3	1	0	1	1
DISABLE FAN LOCK FUNCTION	1	X	X	X

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CPBG - R&D Division

Title: LVDS

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

Date: Tuesday, July 01, 2008 | Sheet 32 of 79

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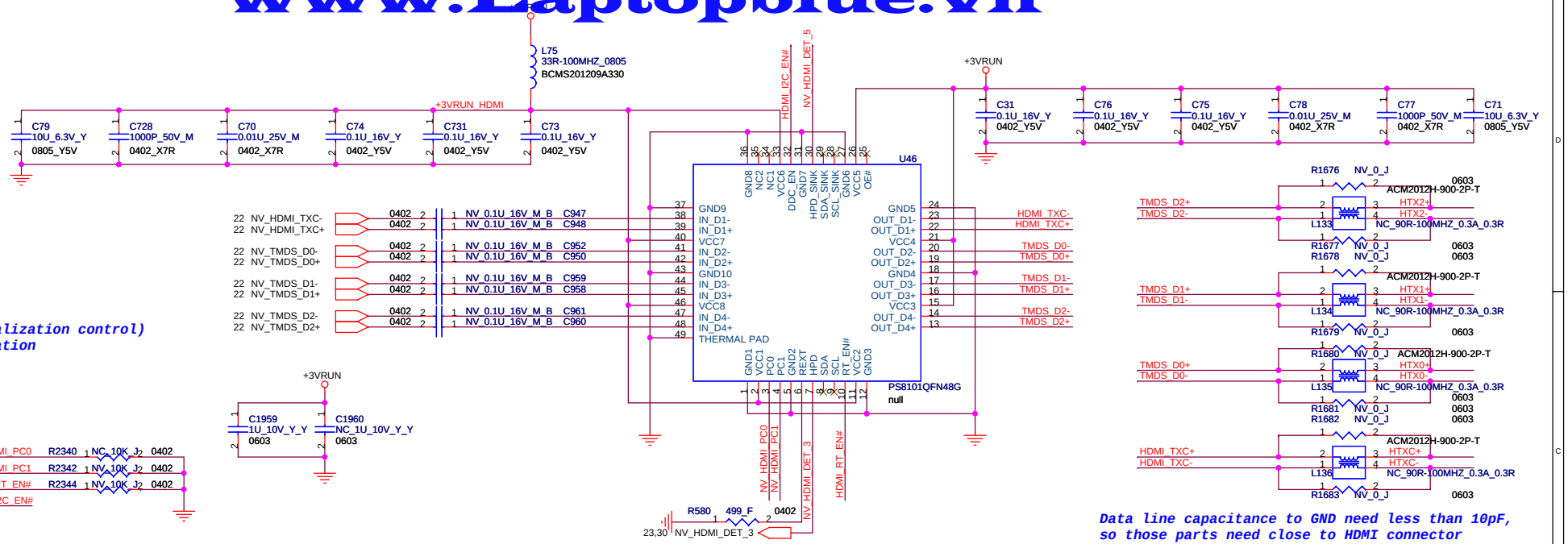
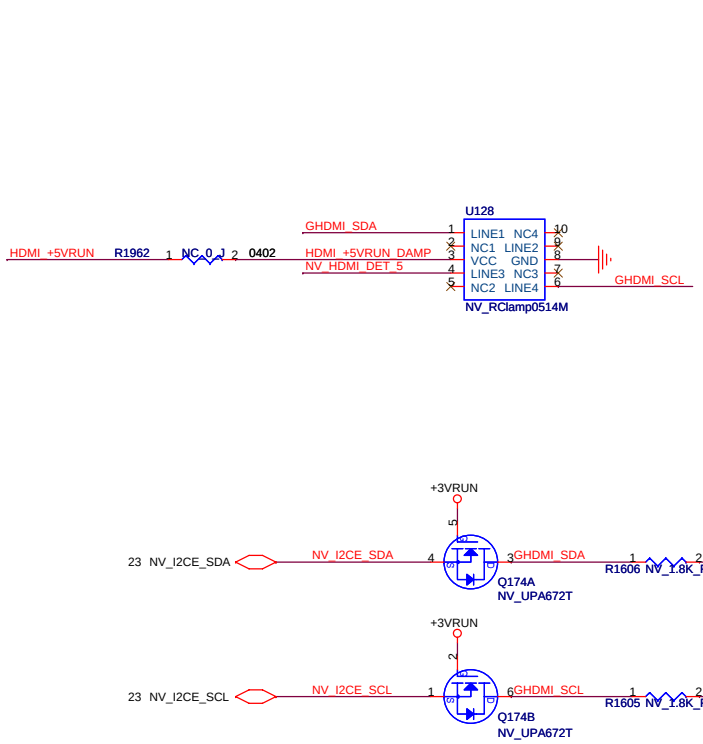
HDMI CONNECTOR



(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB

Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 33 of 79	

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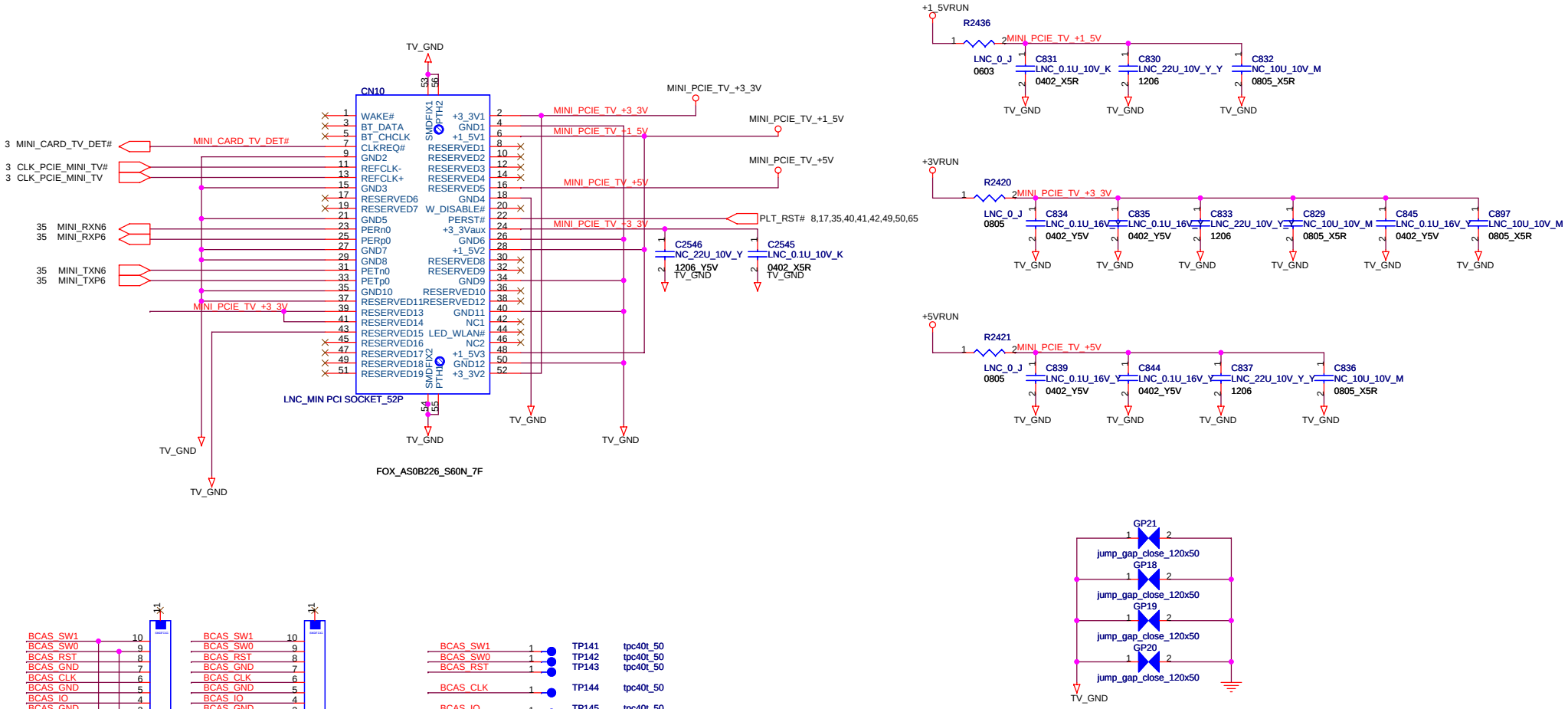

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	MINI-PCIE CONN(TV)	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 34 of 79	

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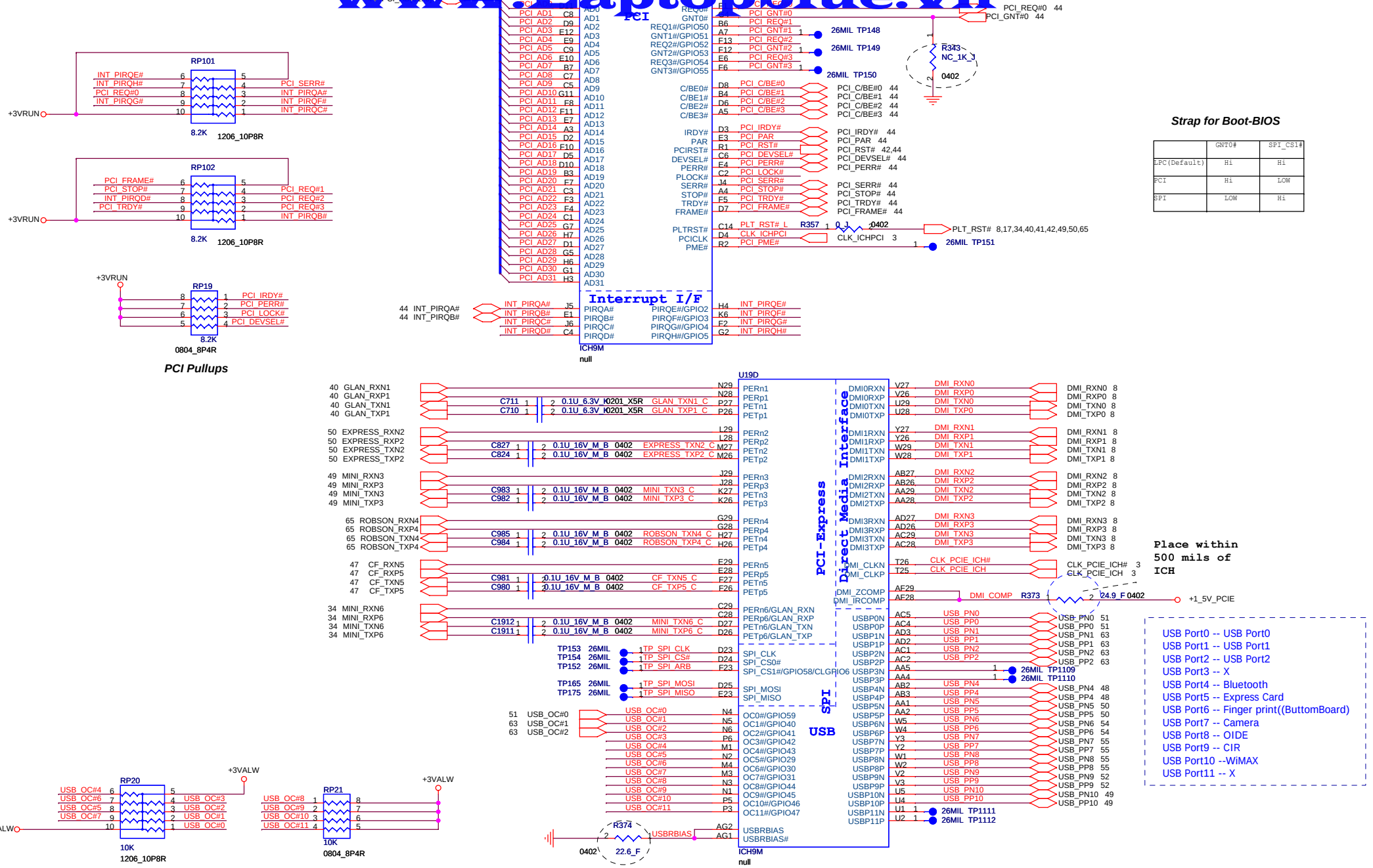

	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ICH9-M(PCI/DMI/USB/PCIE) 1/5

Size: A3 | Document Number: M780(MBX-194) | Rev: 0.1

Date: Friday, June 13, 2008 | Sheet 35 of 79

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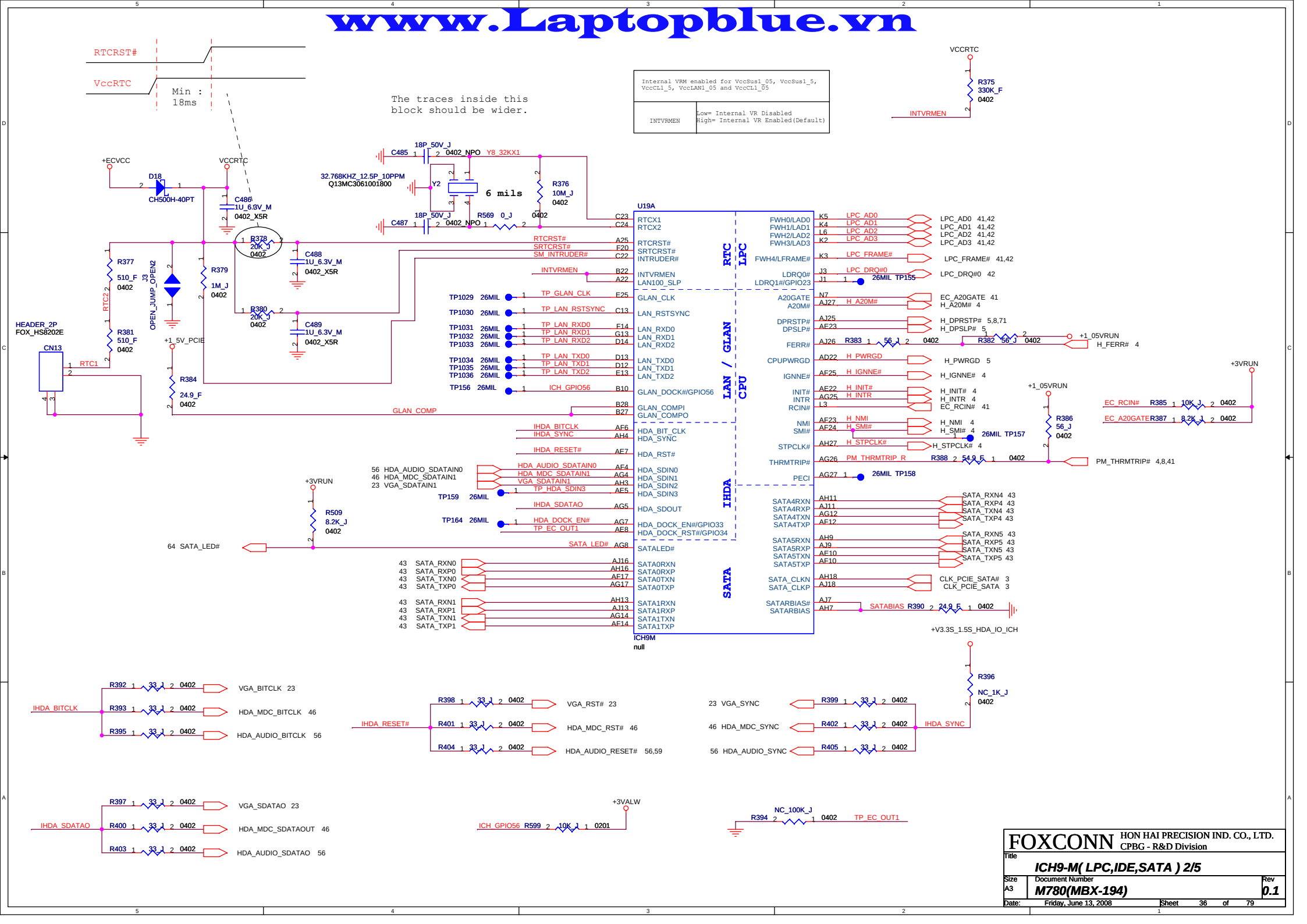

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*ICH9-M(LPC,IDE,SATA) 2/5*
Size: A3	Document Number: *M780(MBX-194)*
Rev	*0.1*
Date: Friday, June 13, 2008	Sheet 36 of 79

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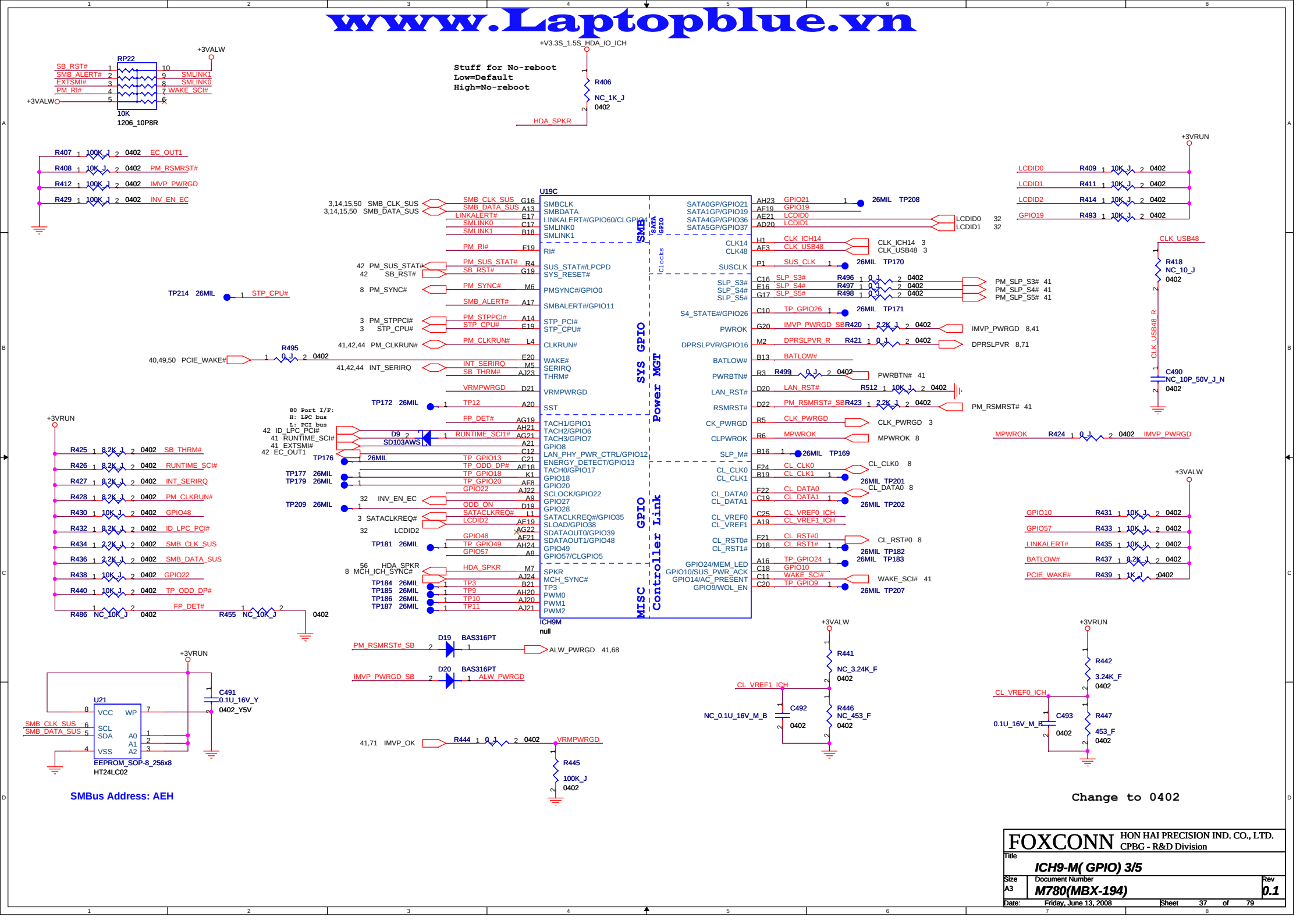

FOXCONN	HON HAI PRECISION IND. CO., LTD.	
	CPBG - R&D Division	
Title	ICH9-M(GPIO) 3/5	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 37 of 79	

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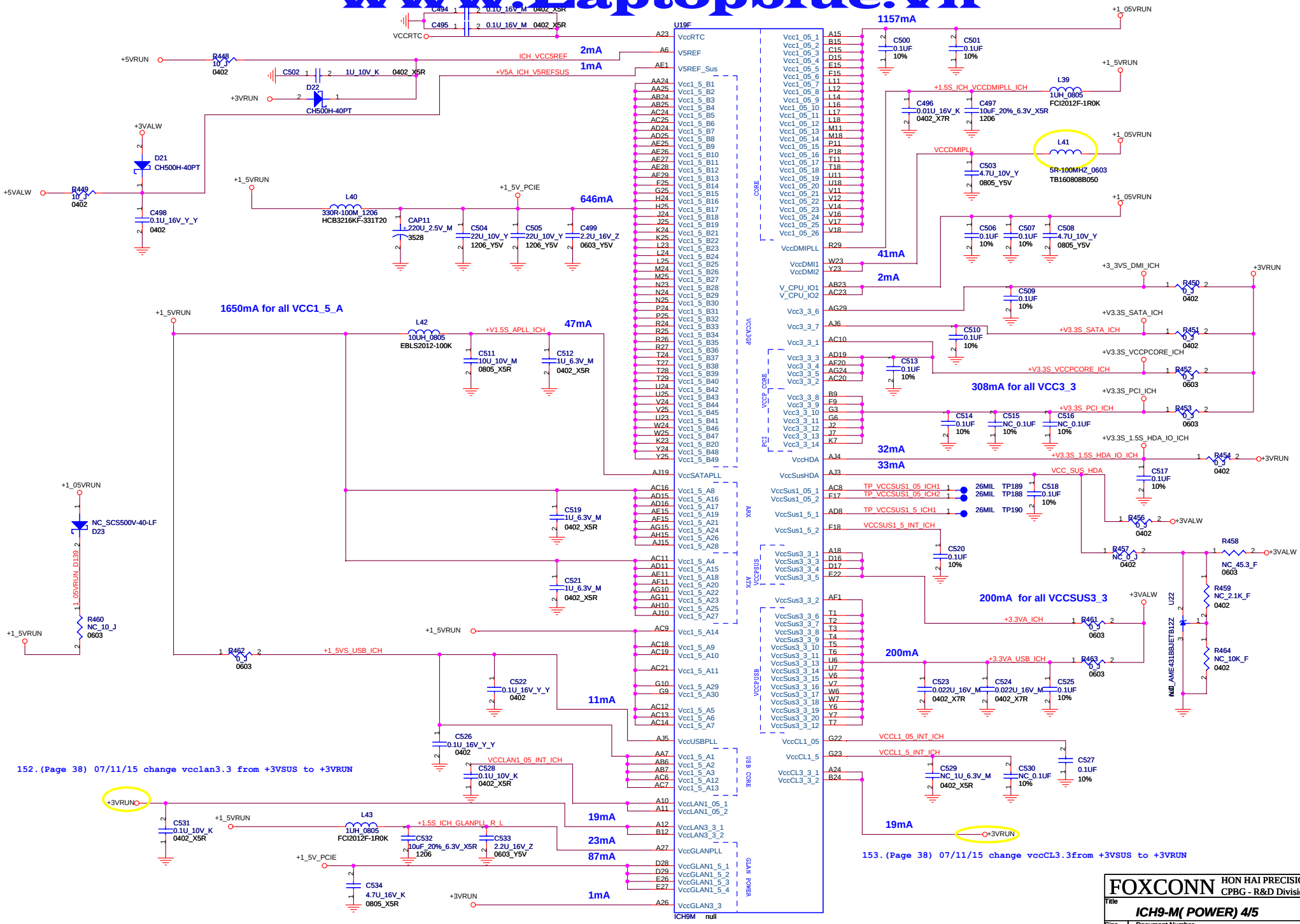

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	ICH9-M(POWER) 4/5
Size: Custom	Document Number: M780(MBX-194)
Rev	0.1
Date:	Friday, June 13, 2008
Sheet	38 of 79

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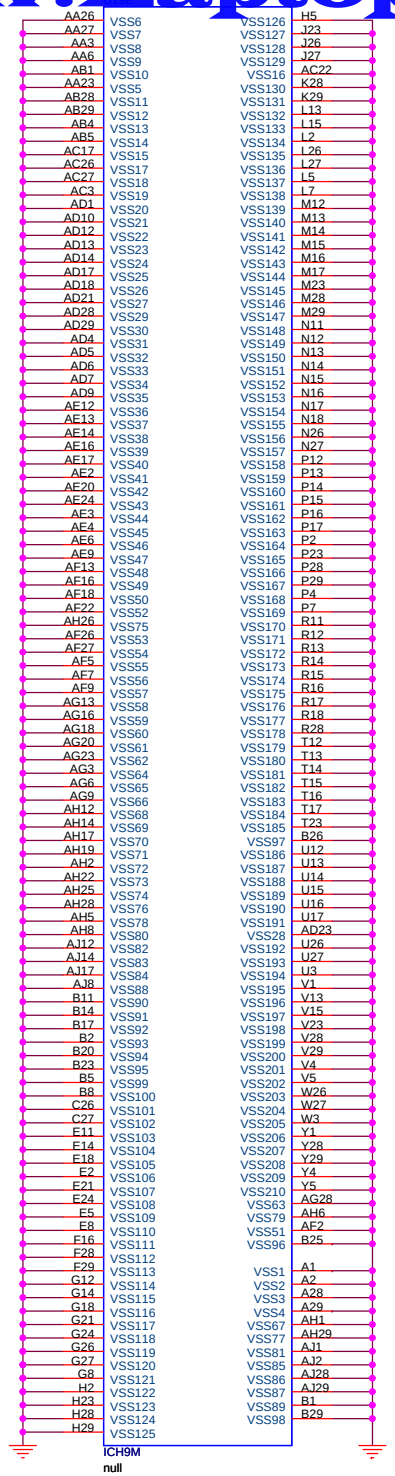

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	ICH9-M(GND) 5/5	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 39 of 79	

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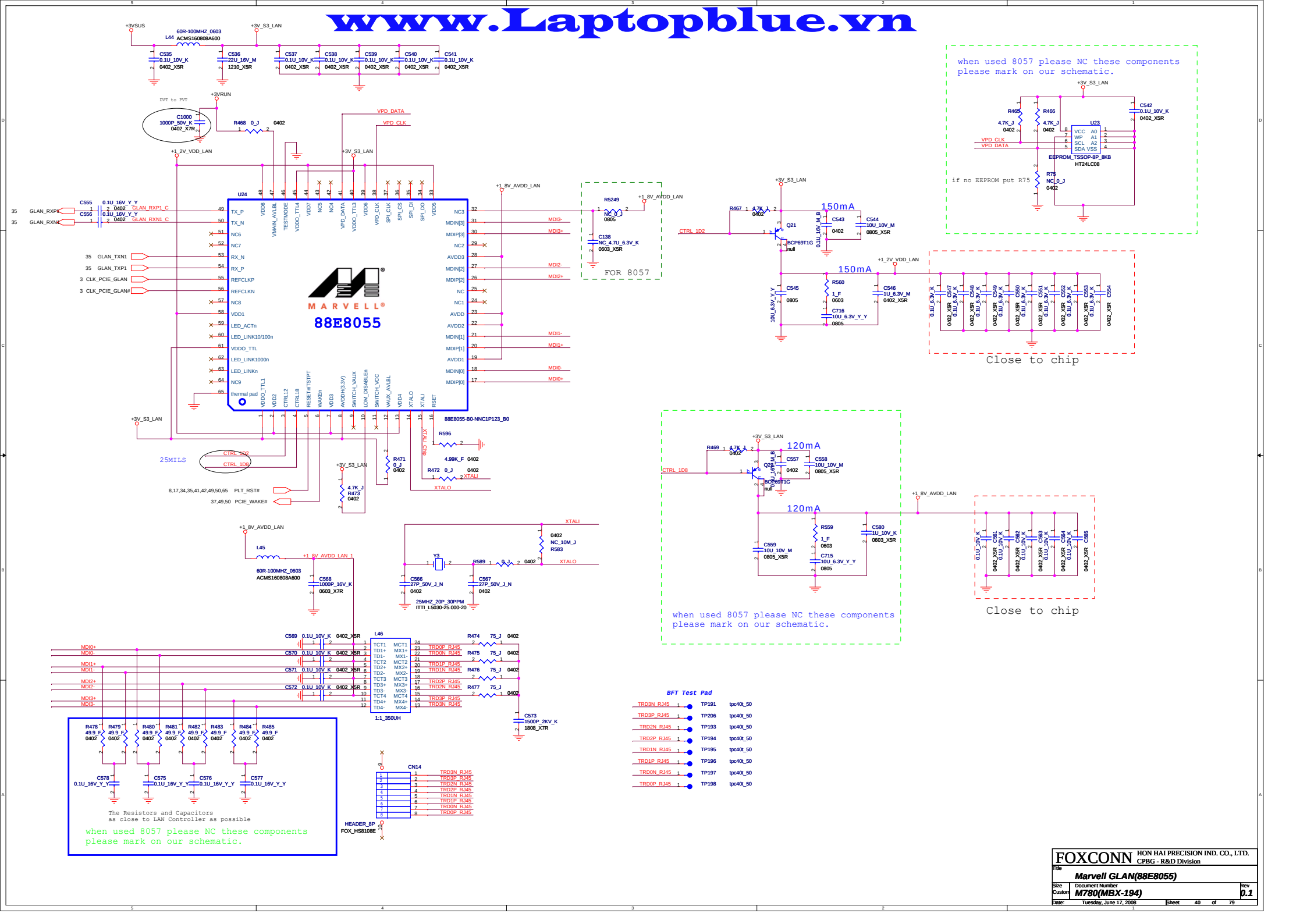

Title	Marvell GLAN(88E8055)
Size / Custom	Document Number: M780(MBX-194)
Rev	0.1
Date	Tuesday, June 17, 2008
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FOXCONN — HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division

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SMBUS Channel 2 +3VALW RP25 2.2K 0402_4P2R CLK_SMB DAT_SMB
SMBUS Channel 1 +3VRUN RP26 4.7K_J 0404 SMB_THRM_CLK SMB_THRM_DATA

U170A WPCE775L_0DG null

A/D: AD0/GPI90 AD1/GPI91 AD2/GPI92 AD3/GPI93 AD4/GPIO05 AD5/GPIO04 AD6/GPIO03 AD7/GPIO07
D/A: DA0/GPI94 DA1/GPI95 DA2/GPI96 DA3/GPI97
GPIO (wake-up capability): GPIO41 TCK/GPIO42 GPIO43/TMS GPIO44/TDI GPIO59/TDO GPIO52/RDY#
GPIO (no wake-up capability): GPO82/TRIS# GPO84/BADDR0
SER: SOUT_CR/GPO83/BADDR1 GPIO67/SIN_CR GPIO06
LPC: LPCPD#/GPIO10 LRESET# LCLK LFRAME# GPIO24 LAD0 LAD1 LAD2 LAD3 SERIRQ CLKRUN#/GPIO11 KBRST# GA20 ECSCI#/GPIO54 SMI#/GPIO65 PWUREQ#/GPIO67
SMB: SDA4/GPIO53 SCL4/GPIO47 SDA3/GPIO31 SCL3/GPIO23 SDA2/GPIO74 SCL2/GPIO73 SDA1/GPIO22 SCL1/GPIO17
SPI: SPI_DI/GPIO77 SPI_DO/GPO76/6SHBM SPI_SCK/GPIO75 GPIO61
CIR: GPIO46/TRST# GPIO34 GPIO16 GPIO30
FIR: GPIO72 GPIO71 GPIO70
KBC: KBSOUT0/JENK# KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4/JEN0# KBSOUT5/TDO KBSOUT6/RDY# KBSOUT7 KBSOUT8 KBSOUT9 KBSOUT10 KBSOUT11 KBSOUT12/GPIO64 KBSOUT13/GPIO63 KBSOUT14/GPIO62 KBSOUT15/GPIO61/XOR_OUT KBSOUT16/GPIO60 KBSOUT17/GPIO57 KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7 VCC_POR#
PS/2 FIU: PSDAT3/GPIO12 PSCLK3/GPIO25 PSDAT2/GPIO27 PSCLK2/GPIO26 PSDAT1/GPIO35 PSCLK1/GPIO37 F_SDI F_SDO F_CS0# F_SCK

CN15 HEADER_32P FOX_GB1SH320-1280-7F
TP309 TP310 TP311 tpc40l_50
C723 1U_10V_K 0603_X5R
C699 10U_6.3V_Y_T C697 0.1U_16V_M_ST C700 0.1U_16V_M_ST C719 0.1U_16V_M_ST C721 0.1U_16V_M_ST C718 0.1U_16V_M_ST C698 0.1U_16V_M_ST
C722 10U_6.3V_Y_T C720 0.1U_16V_M_B C717 0.1U_16V_M_B C716 1U_6.3V_M_B

R514 33K_J 0402 R515 20M_J 0603 Y4 32.768KHZ_12.5P_10PPM Q13MC3061001800 C590 18P_50V_J 0402_NPO C591 18P_50V_J 0402_NPO 32KXCLKO 32KXCLKI

LID Switch: R489 100K_J 0402 LIDIN#

(for touch sensor): MM_IRQ# CF_IN# PWRLIMIT# SCRLOCK_LED# DAT_TP CLK_TP

R520 4.7K_J 0402 ECRST# C594 NC_0.1U_16V_M_B 0402 Q23 ME2N7002E PLT_RST# Q25 PMBS3904 R532 2.2K 0402 +1.05VRUN PM_THRMTRIP#

M780 Model System ID definition

	H	N	L(32M)
SysID0	1	0	1
SysID1	1	1	0
SysID2	0	0	0
SysID3	0	0	0

SMBus Address: 3EH
U159 W83L604G null
C465 47P_50V_J_N 0402 C466 47P_50V_J_N 0402
CF_PWR_ON# 47 DDR_ALERT# 8,53 CF_REST_CARD# 47 CF_REST_IC# 47 CF_REQ_IN2# 3

POWER ON / POWER OFF
CF_PWR_ON# CF_REQ_IN2# CF_REST_IC# CF_REST_CARD#

R516 NC_47_J 0402 C592 NC_22P_50V_K_N 0402 R488 110_J 0402 C588 0.1U_16V_M_B 0402 PWRSW# PWRSW#_R

TP: RP23 10K 0404_4P2R C91 0.01U_16V_K_B 0402 DAT_TP CLK_TP
LCD: RP24 10K 0404_4P2R CLK_35001 DAT_35001 RP27 10K 0404_4P2R NV_LCD_CLK NV_LCD_DATA

R1778 10K_J 0402 C998 1000P_50V_K 0402_X7R R3025 10K_J 0402 C2580 1U_10V_Y 0603_Y5V C913 1000P_50V_K 0402_X7R C371 220P_50V_J_N 0402 C1002 1000P_50V_K 0402_X7R

R785 NV9L32_100K_J R2277 NV9L_100K_J R786 NC_100K_J R790 NV9M_100K_J R792 NV9HM_100K_J R791 NC_100K_J R789 NV9L_100K_J R793 100K_J R787 R788 100K_J

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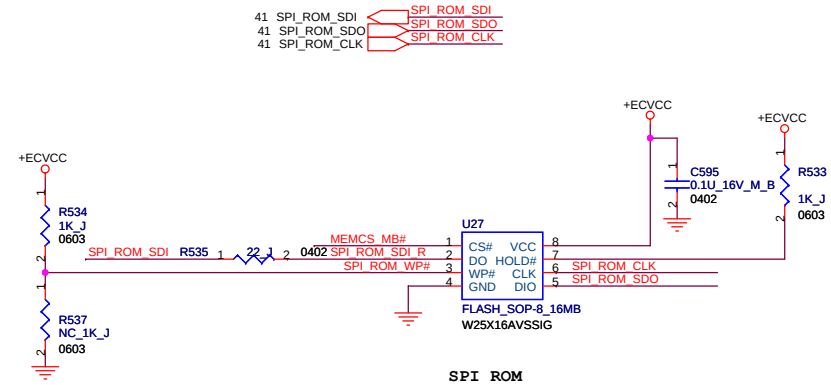
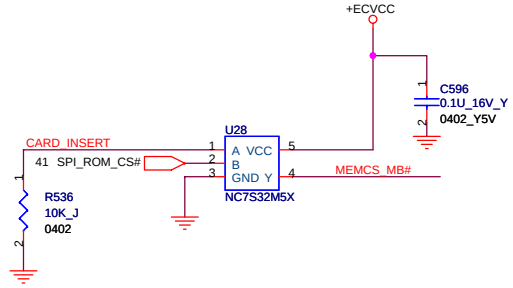
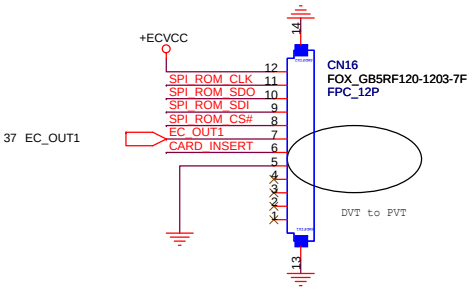
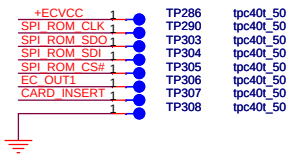


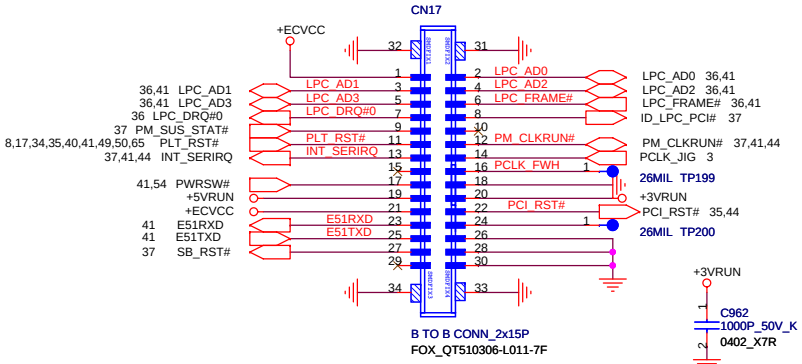
SPI ROM





EXTERNAL SPI ROM INTERFACE





JIG-120

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	Flash ROM/SPI		
Size A3	Document Number M780(MBX-194)		Rev 0.1
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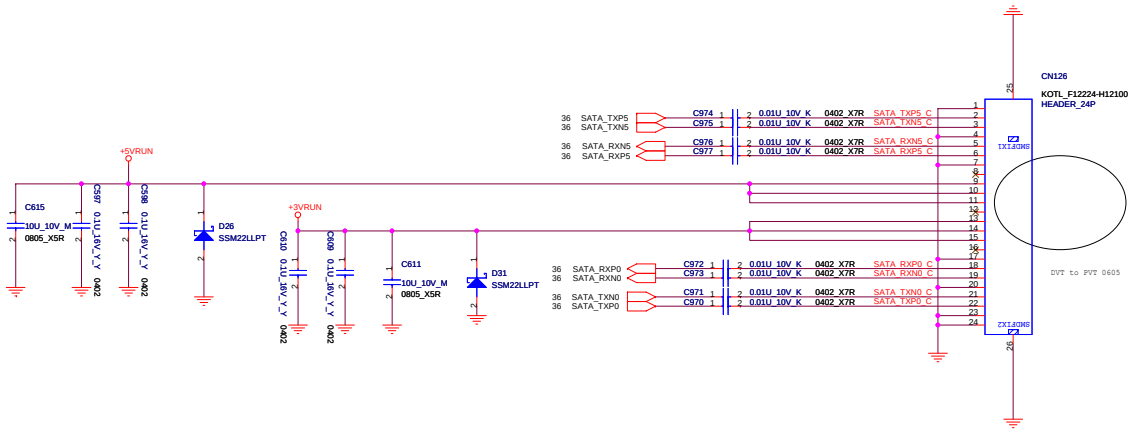
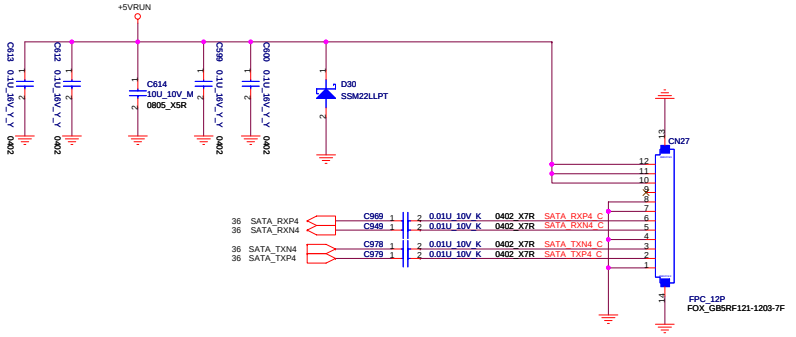
SATA HDD CONN(FPC)

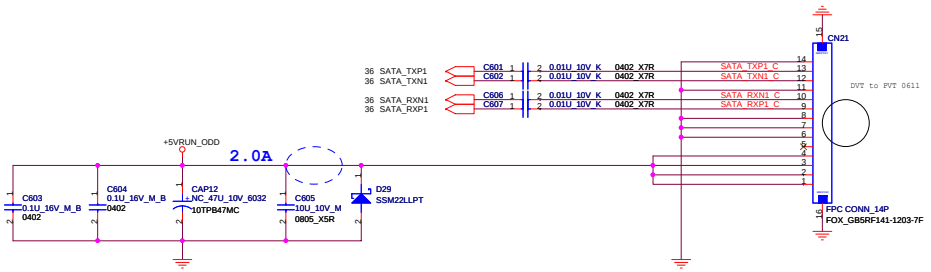


SATA HDD CONN1(FPC)



SATA0 : HDD or SSD (just connect to 24 Pin connector)
SATA1 : ODD (fixed)
SATA4 : HDD.(fixed for Single HDD connector)
SATA5 : SSD.(just connect to 24 Pin connector)

SATA ODD CONN(FPC)



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title	SATA HDD/CD-ROM	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
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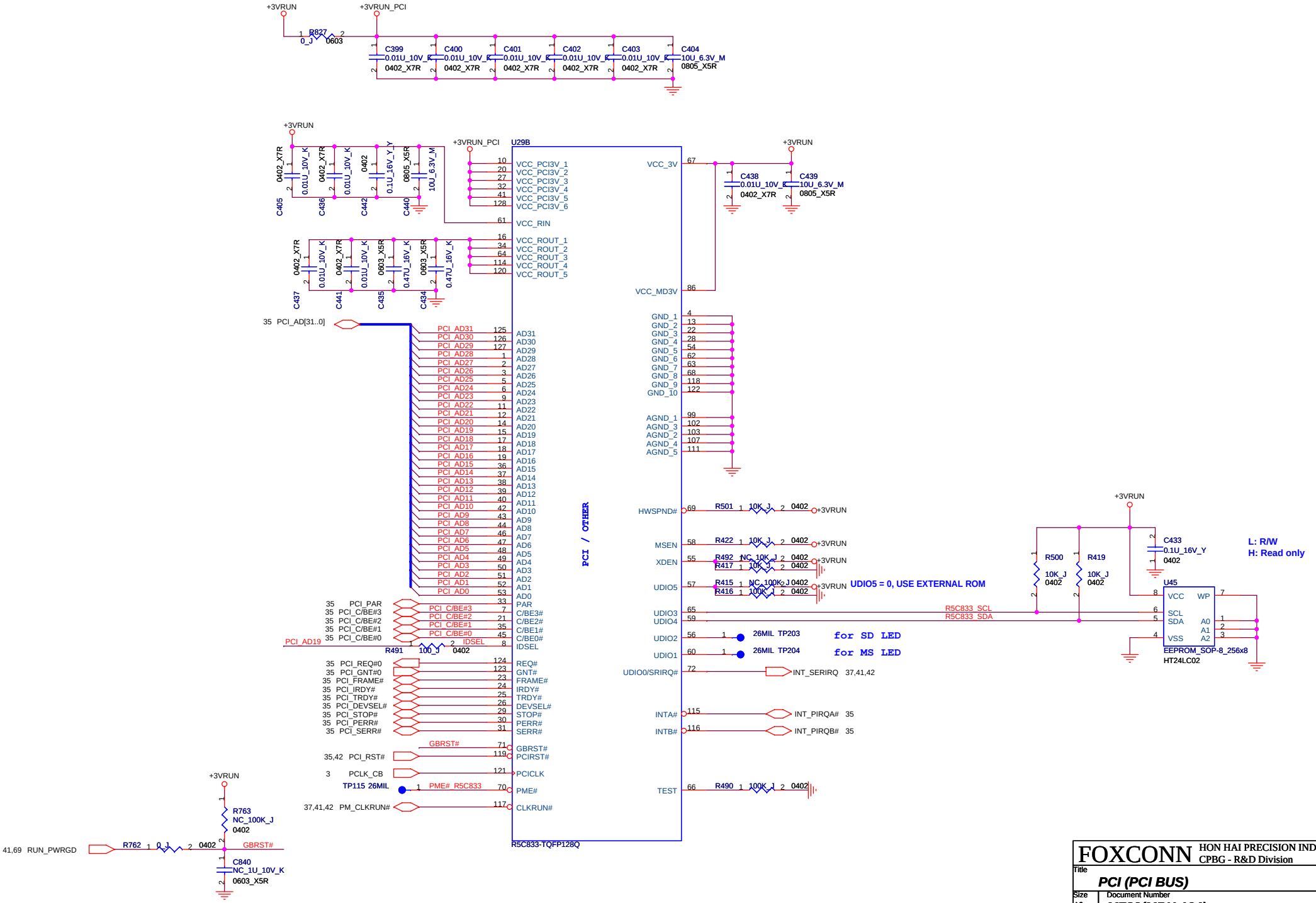

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (PCI BUS)	
Size A3	Document Number M780(MBX-194)	Rev 0.1
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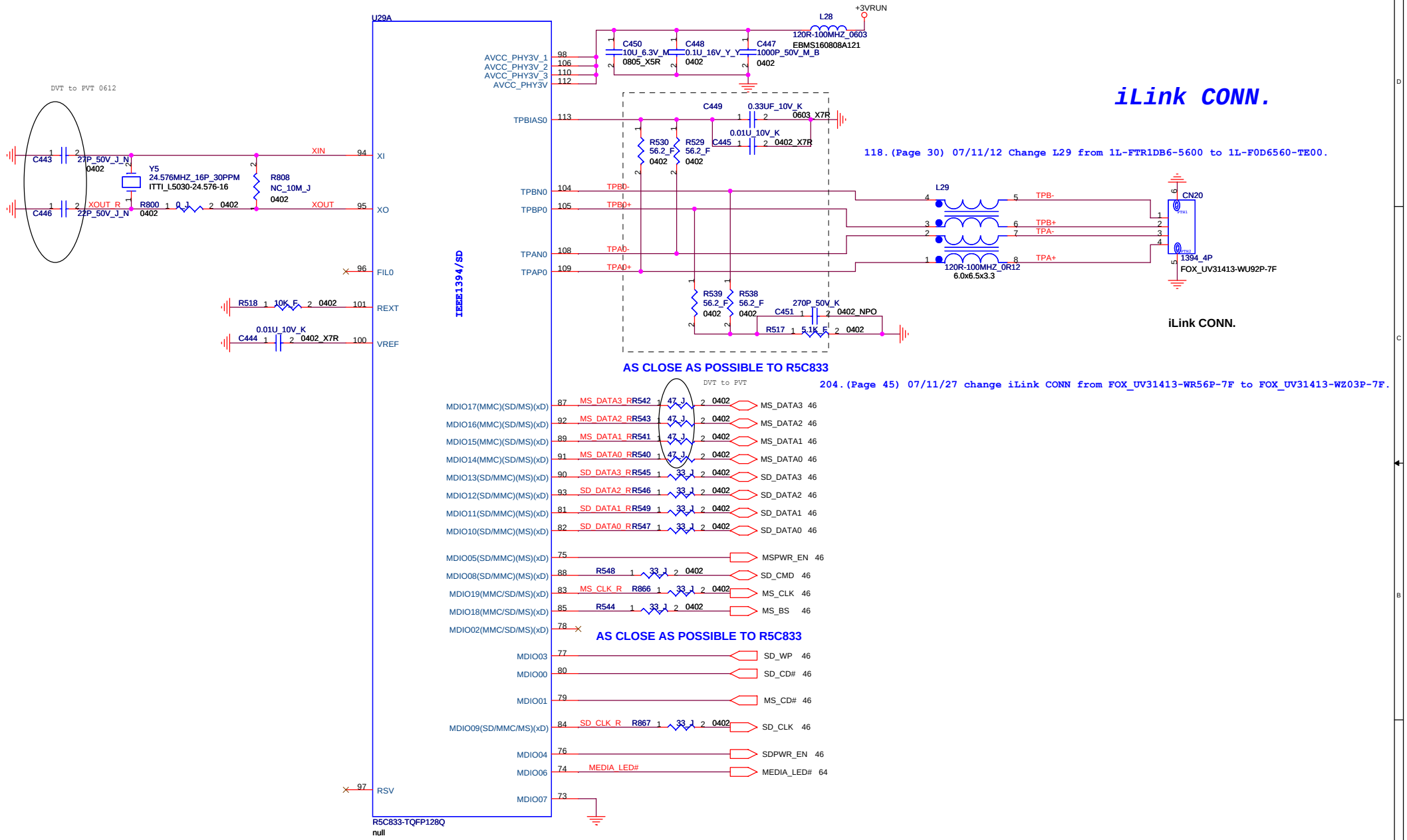

iLink CONN.

118.(Page 30) 07/11/12 Change L29 from 1L-FTR1DB6-5600 to 1L-F0D6560-TE00.

iLink CONN.

204.(Page 45) 07/11/27 change iLink CONN from FOX_UV31413-WR56P-7F to FOX_UV31413-WZ03P-7F.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (ILINK)		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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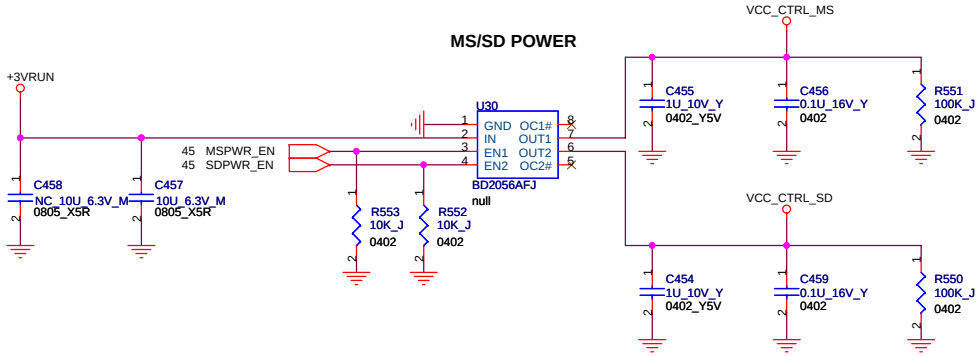
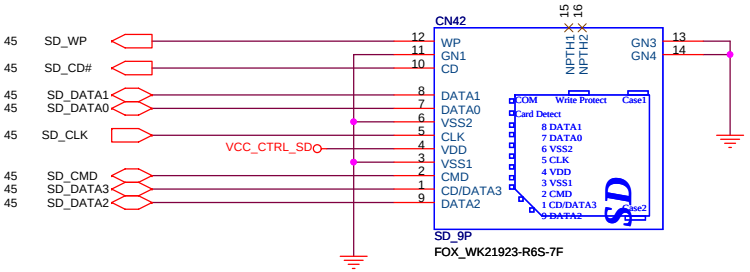
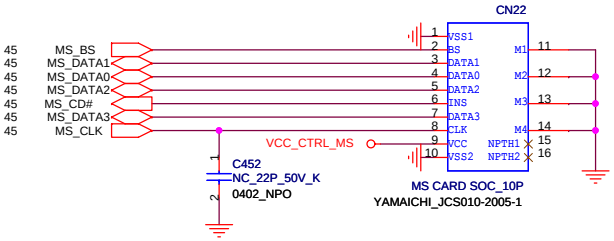
MS/SD POWER

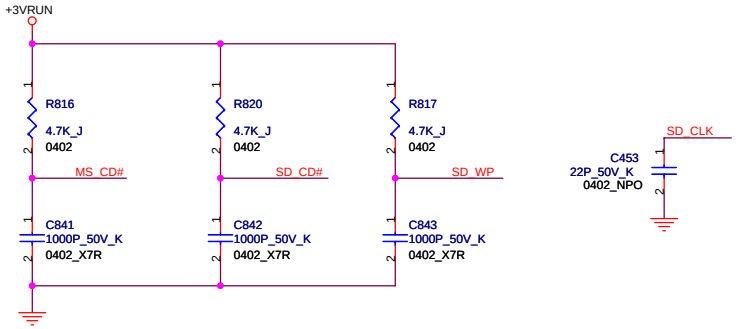


SD CONN.

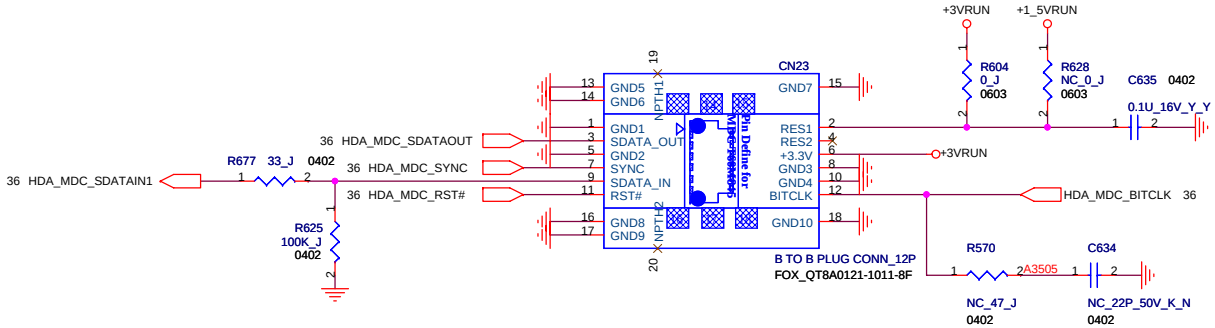


MS STD/DUO CONN.





MDC CONN.



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (MS-DUO/MDC)	
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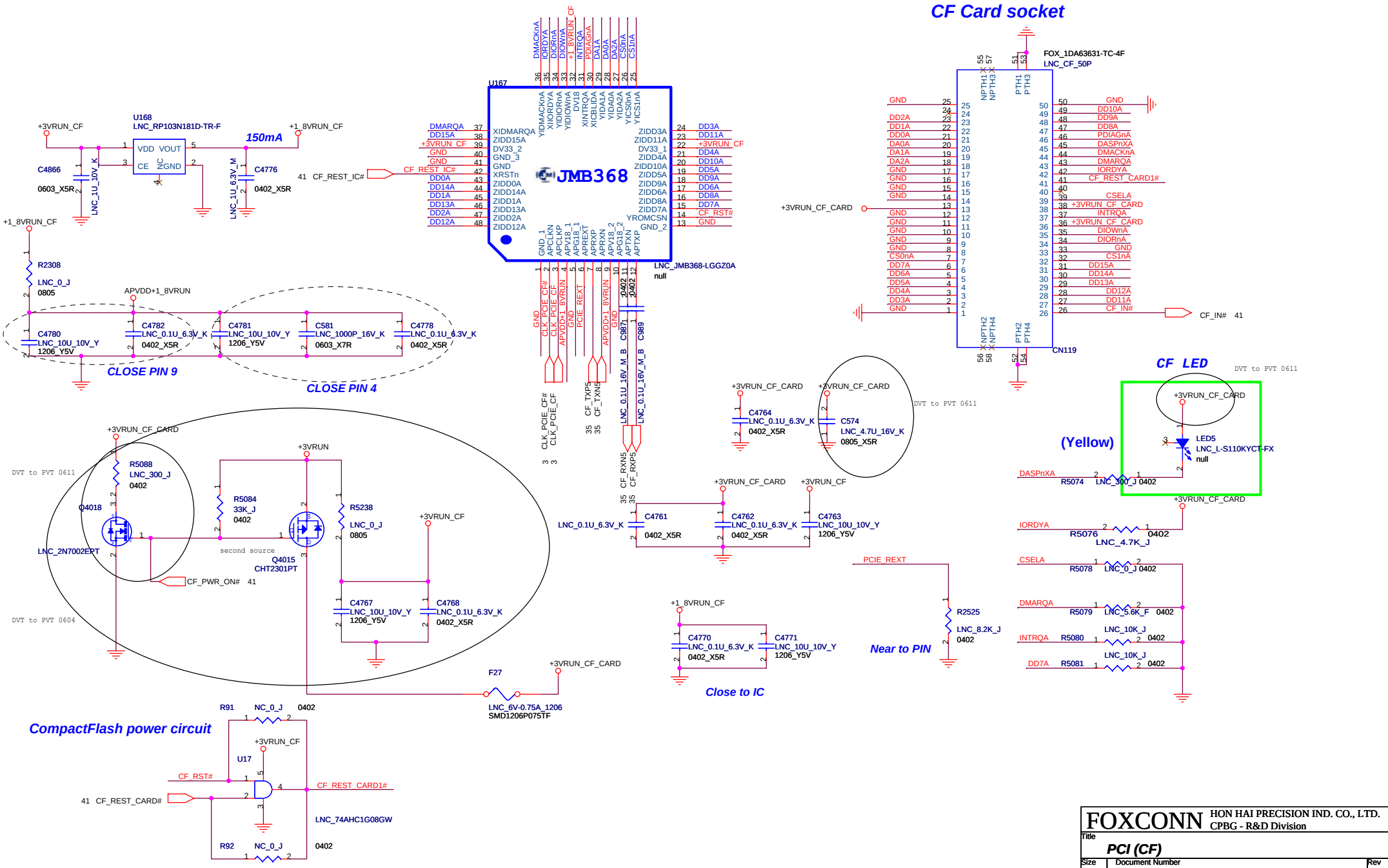

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (CF)		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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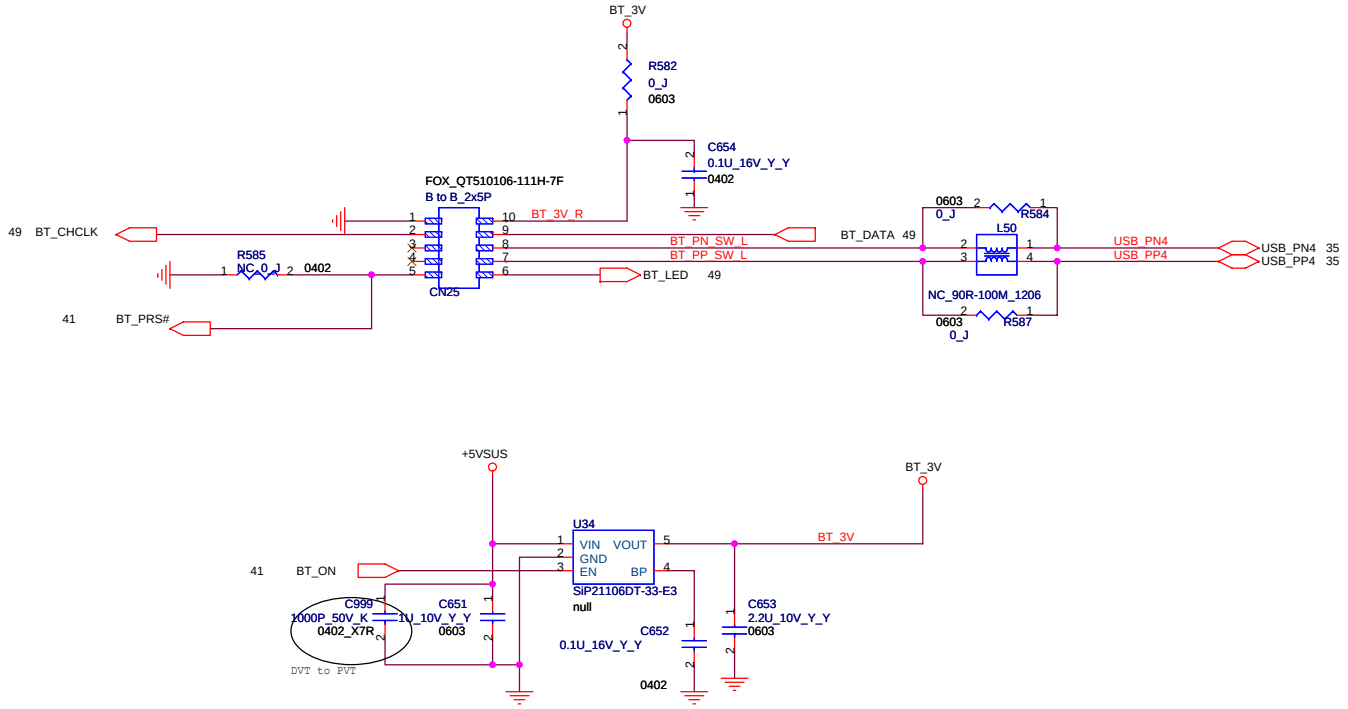
Bluetooth connector



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Bluetooth		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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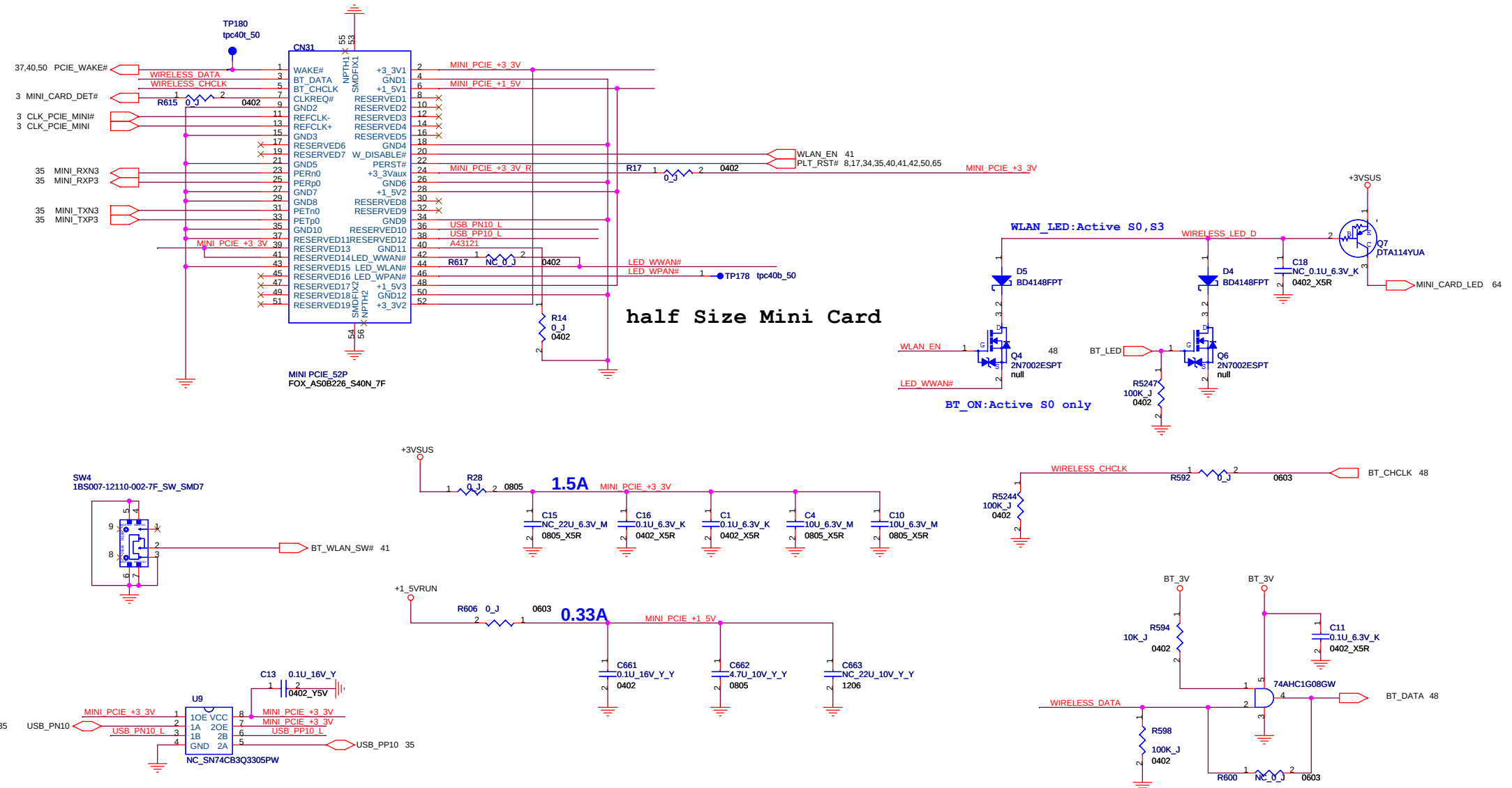
Mini-PCIE Card connector(WLA)



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Mini-PCIE Card(WLA)		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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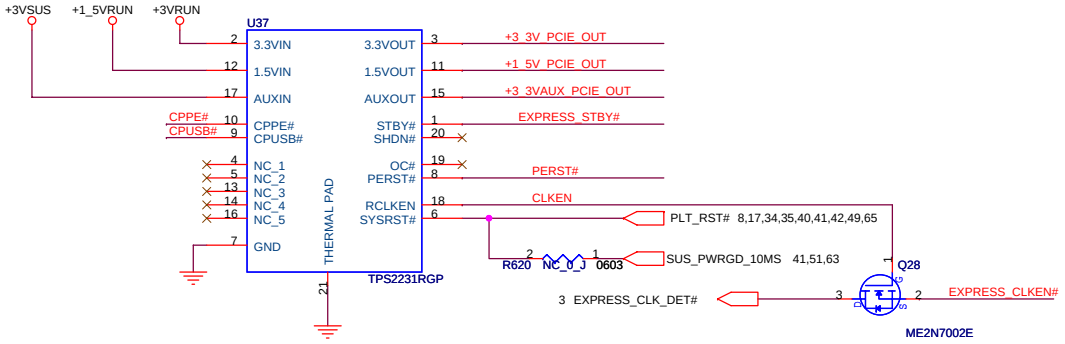
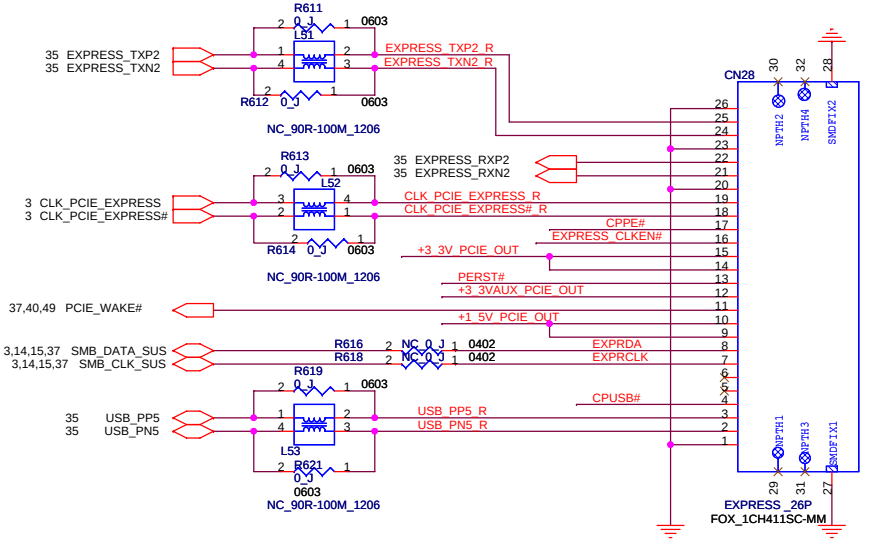
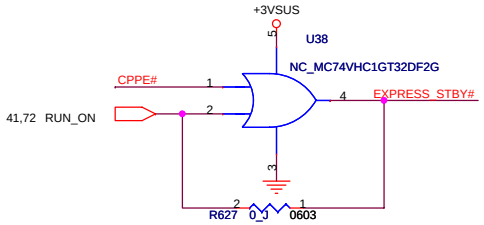
EXPRESS Card Slot

VOLTAGE INPUTS (1)			LOGIC INPUTS			VOLTAGE OUTPUTS			MODE
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP (4)	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

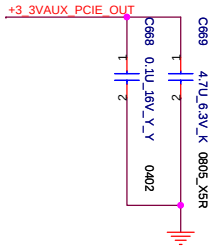
+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A



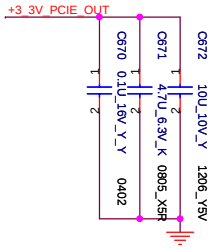




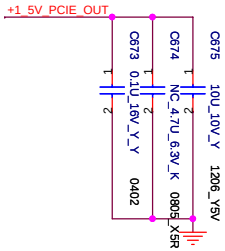
Supply Max 275mA

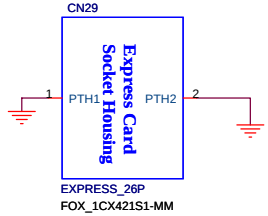


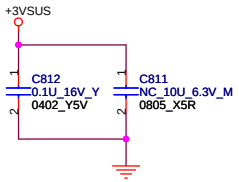
Supply Max 1300mA

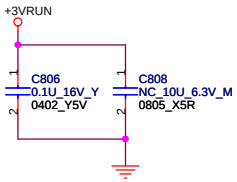


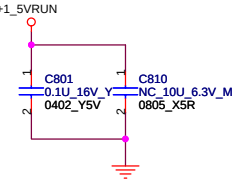
Supply Max 650mA











FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	EXPRESS CARD		
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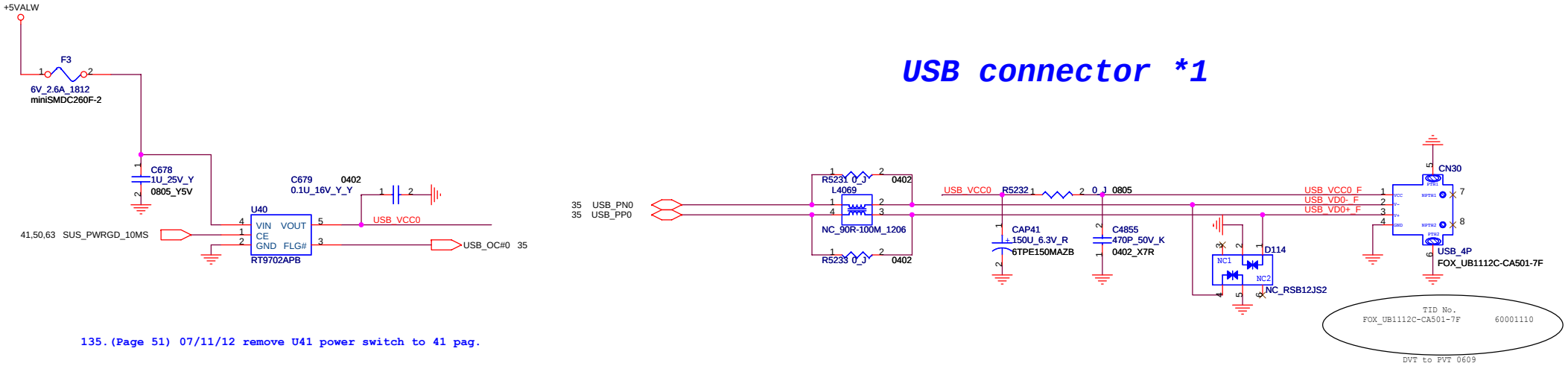
USB connector *1



135.(Page 51) 07/11/12 remove U41 power switch to 41 pag.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: USB2.0		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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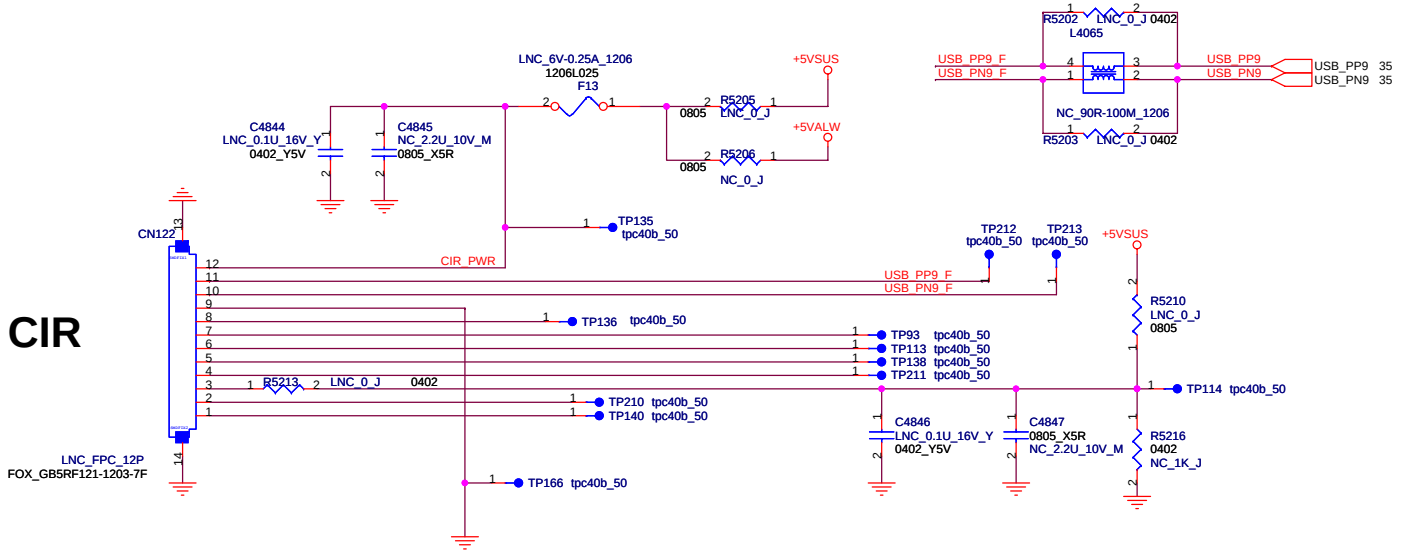
IR Rreceiver connector



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CIR Reciver		
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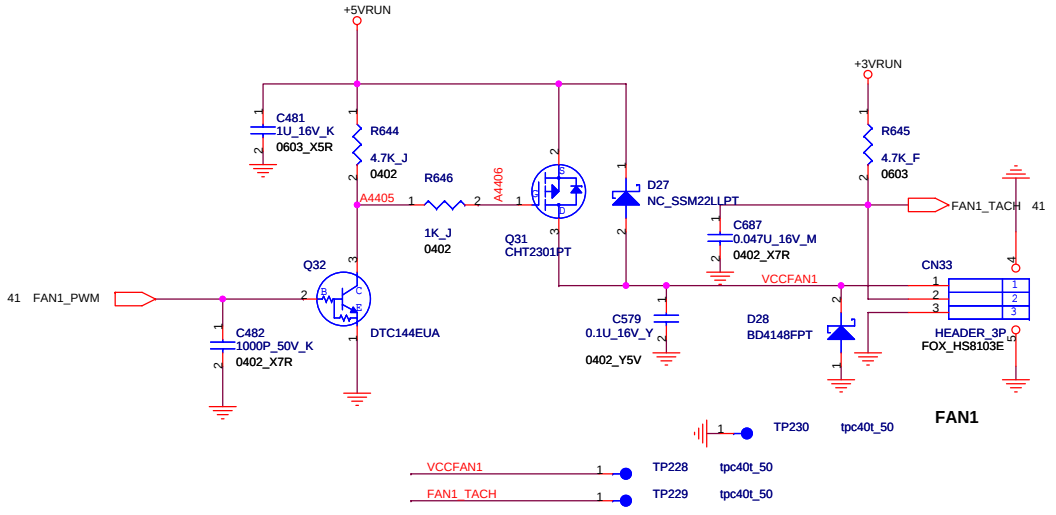
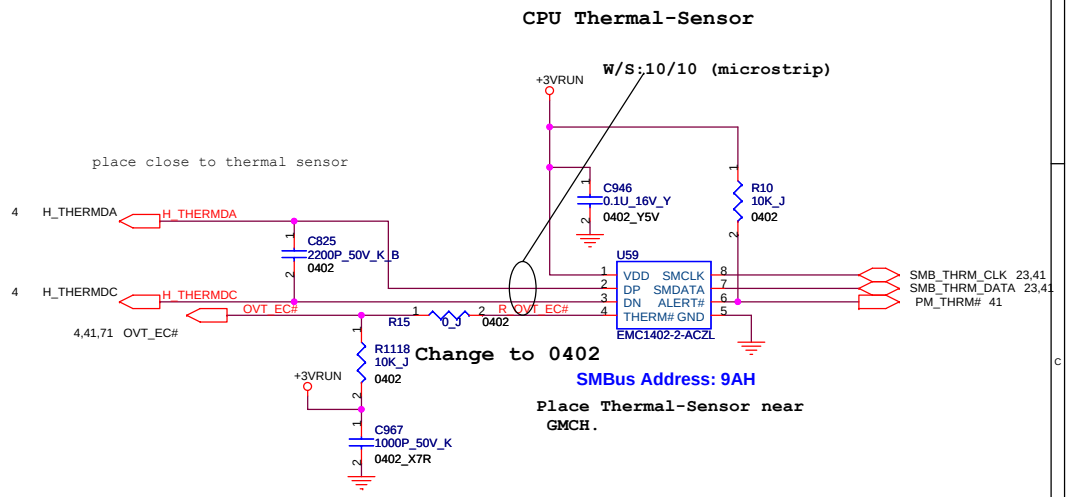
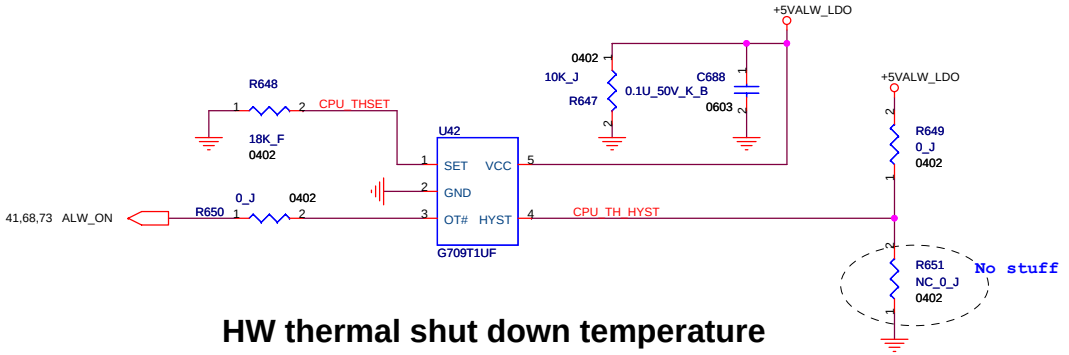
FAN circuit



CPU Thermal-Sensor

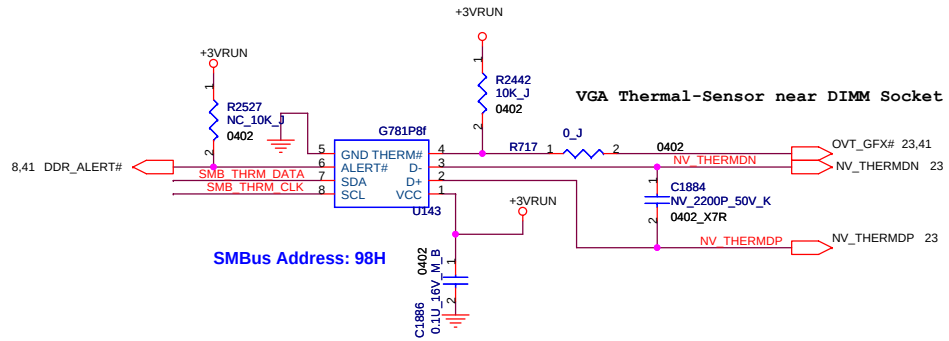


HW THERMAL PROTECTION



HW thermal shut down temperature setting 95 degree . Put Near CPU .

VGA Thermal-Sensor



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: FAN / HW THERMAL PROTECTION		
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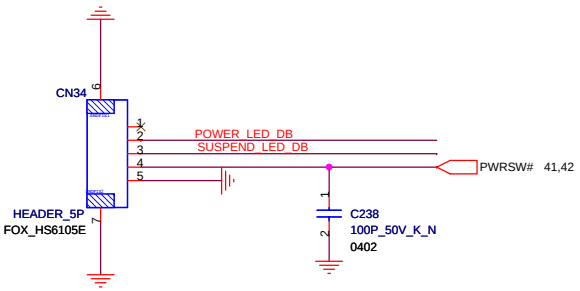
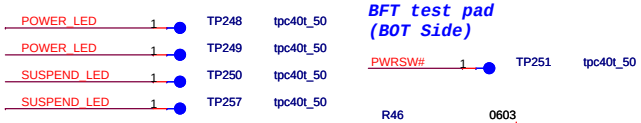
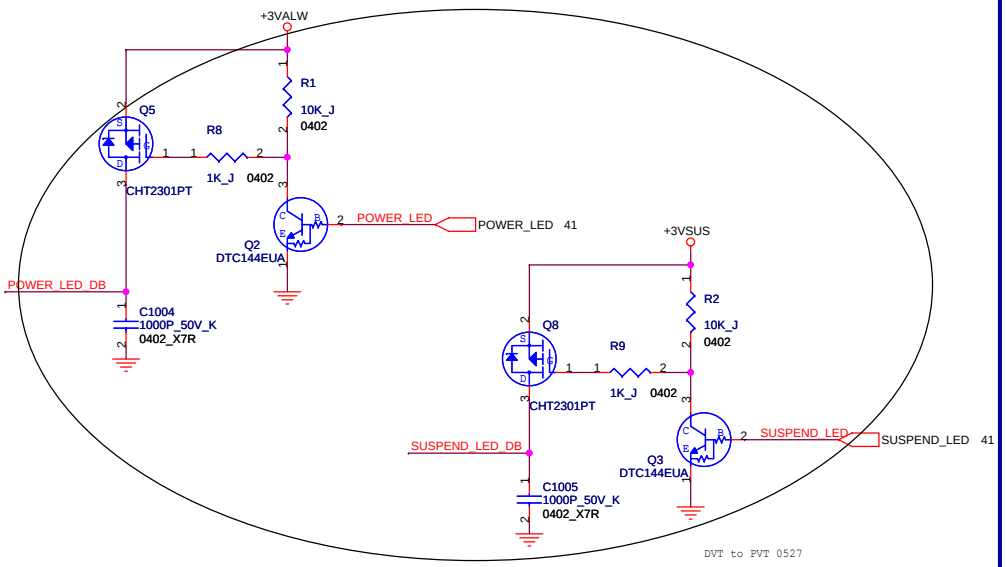
To Power Button Board Connector



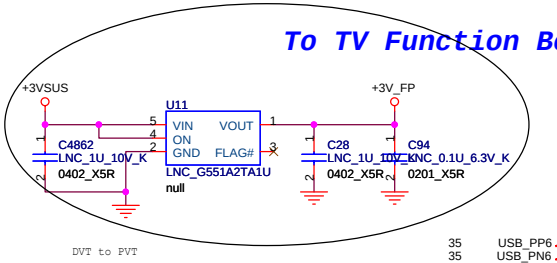
BFT test pad (TOP Side)

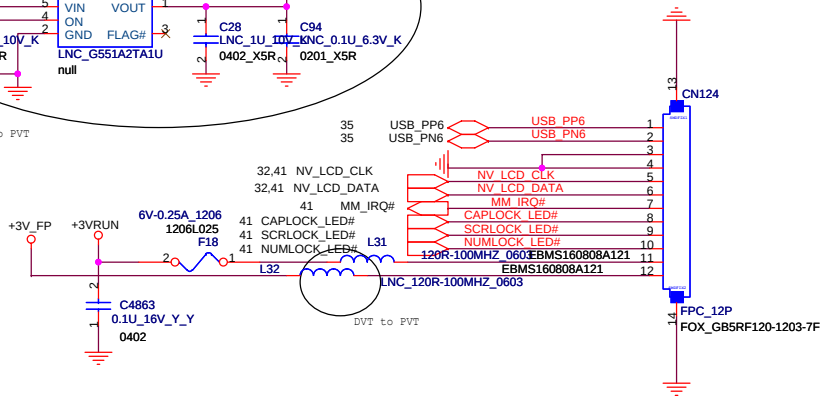
BFT test pad (BOT Side)



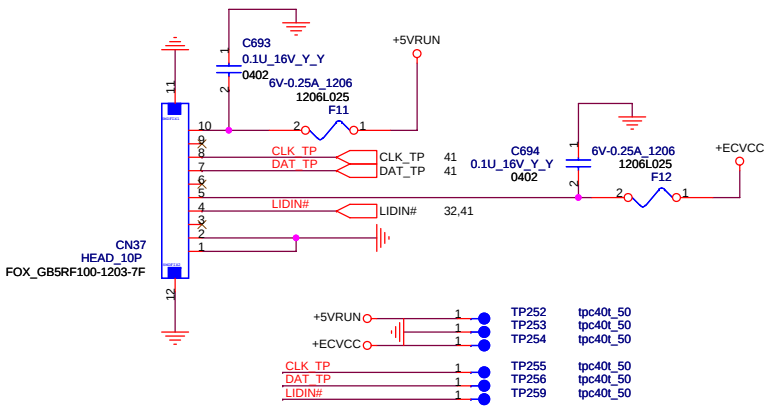


To TV Function Board Connector (FFC)





To Touch Pad Board Connector (FFC)



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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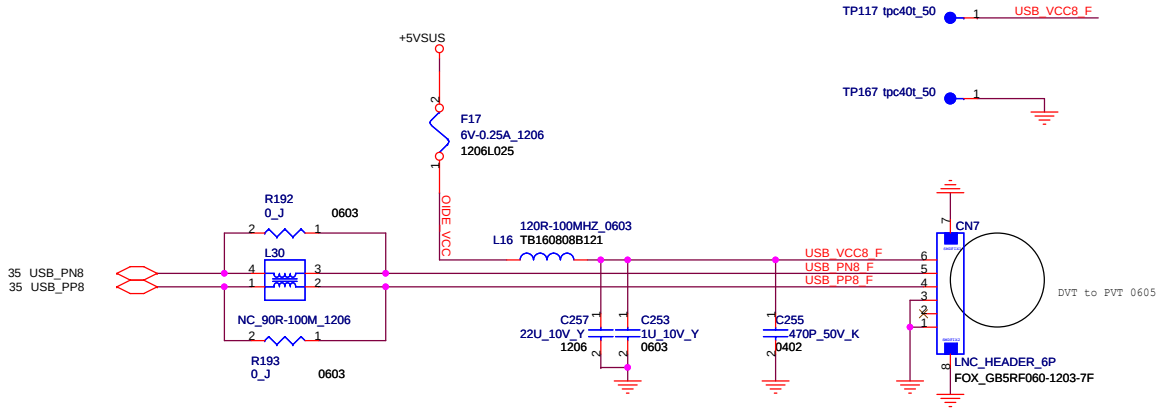
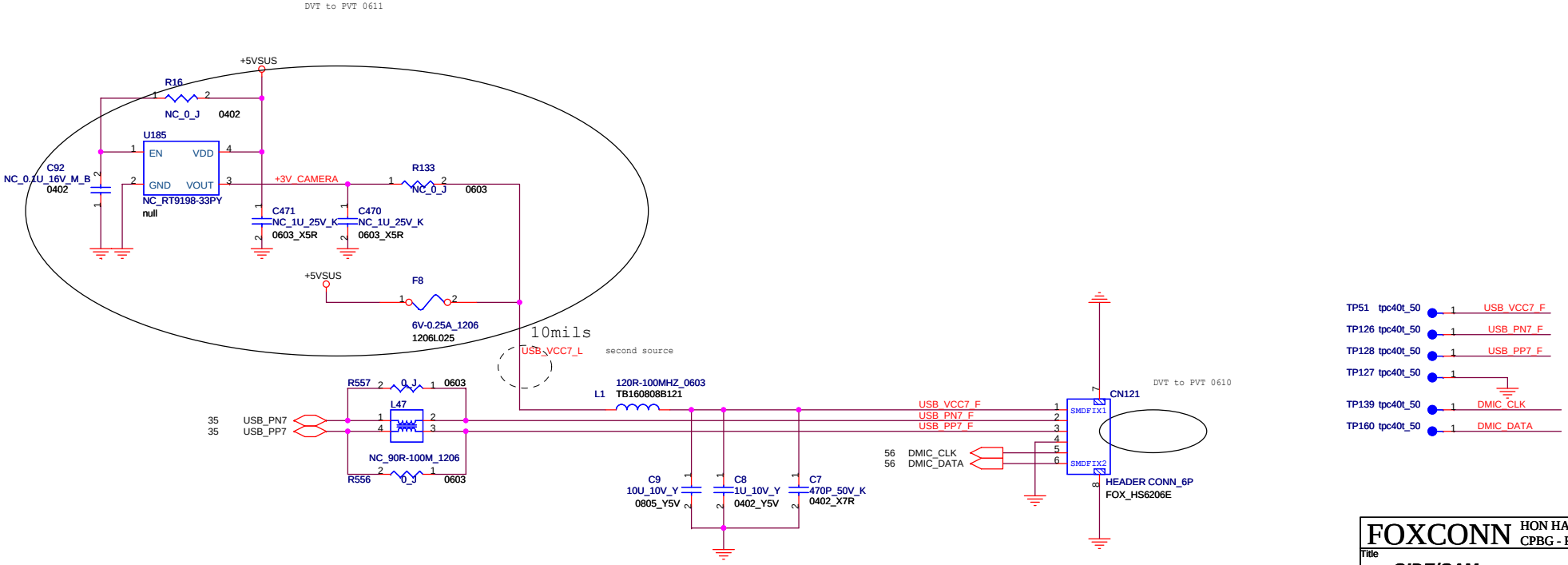
OIDE Connector



CAMERA +MIC CONN.



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	OIDE/CAM	
Size A3	Document Number M780(MBX-194)	Rev 0.1
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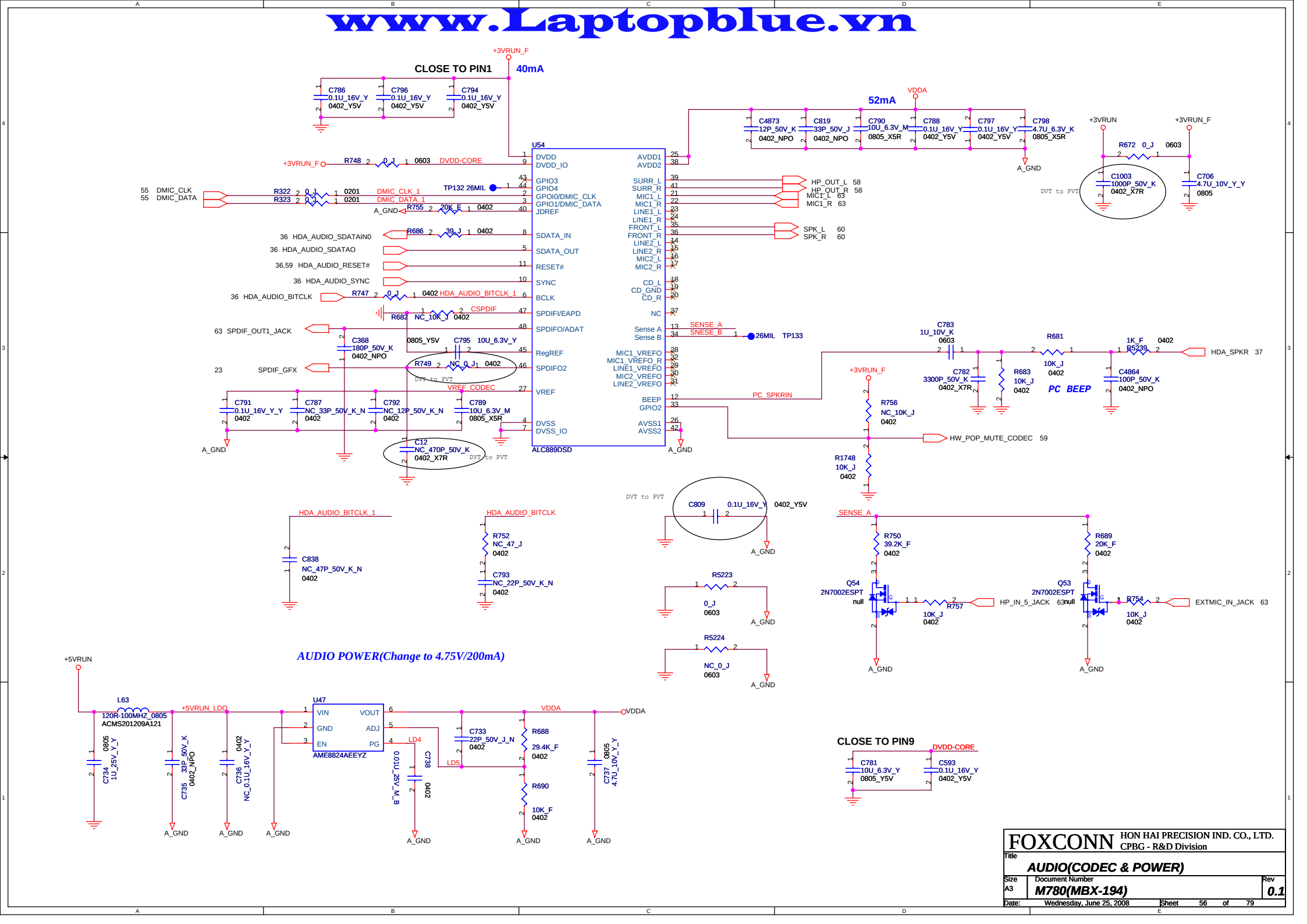

AUDIO POWER(Change to 4.75V/200mA)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **AUDIO(CODEC & POWER)**

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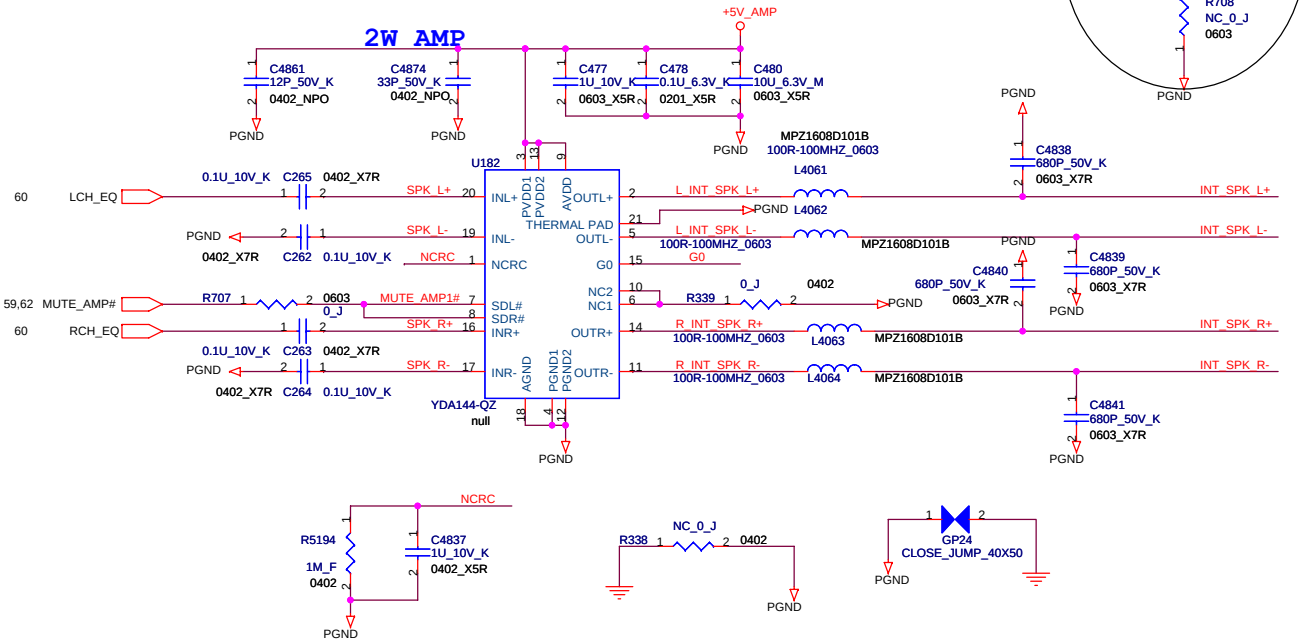
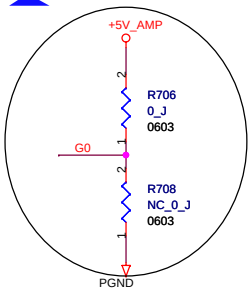
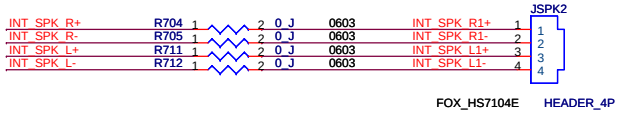
SPEAKER AMP





INTERNAL SPEAKER Connector

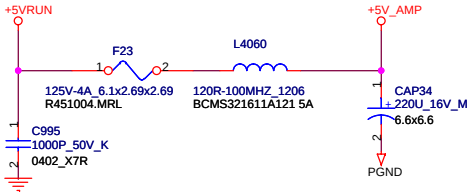


BFT Test Pad

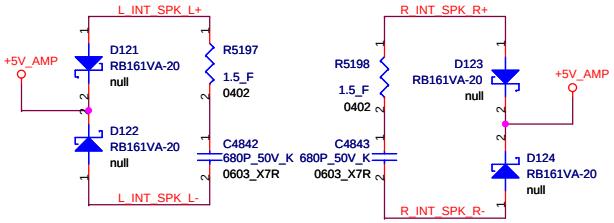
(20mil)

INT_SPK_L1+	1	TP282	tpc40t_50	INT_SPK_R1+	1	TP299	tpc40t_50
INT_SPK_L1-	1	TP283	tpc40t_50	INT_SPK_R1-	1	TP287	tpc40t_50

SPEAKER POWER



Close to Amp



GAIN

External adjustable	Adjustable range from 12db to 18db
Fixed	Pull high=18db Pull low=12db

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(AMP & SPK)		
Size A3	Document Number M780(MBX-194)		Rev 0.1
Date: Friday, June 13, 2008	Sheet 57 of 79		

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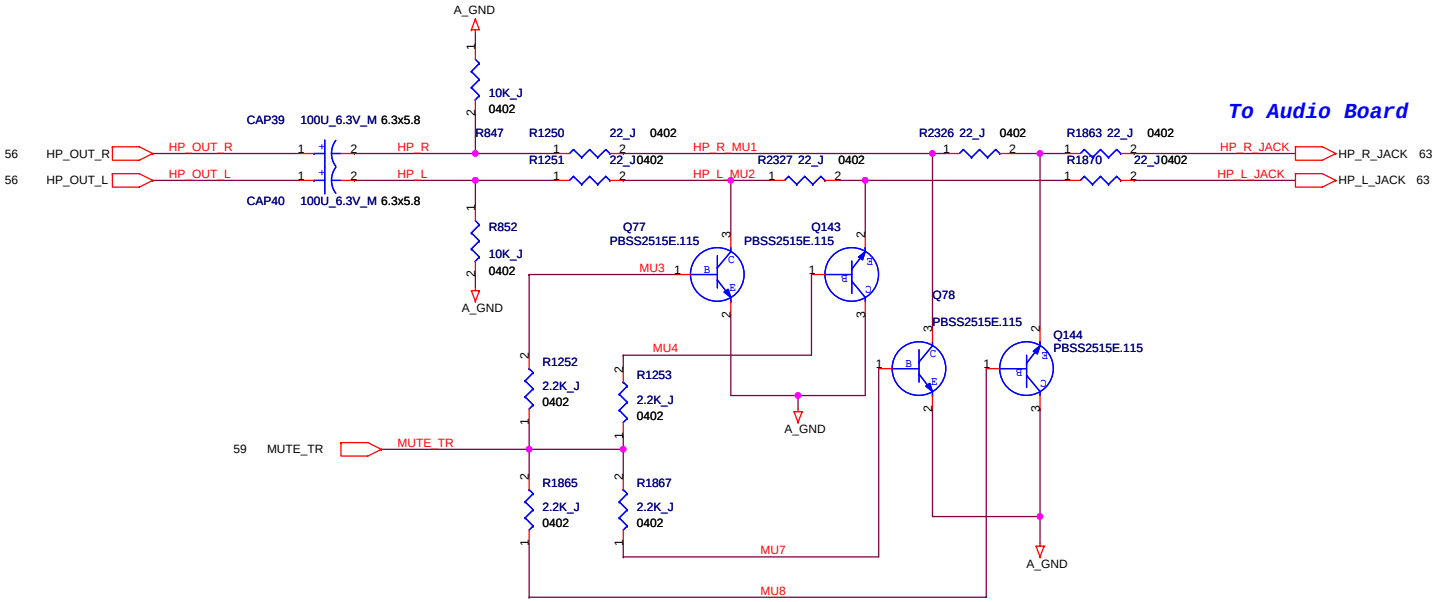

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: AUDIO (HP)		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 58 of 79	

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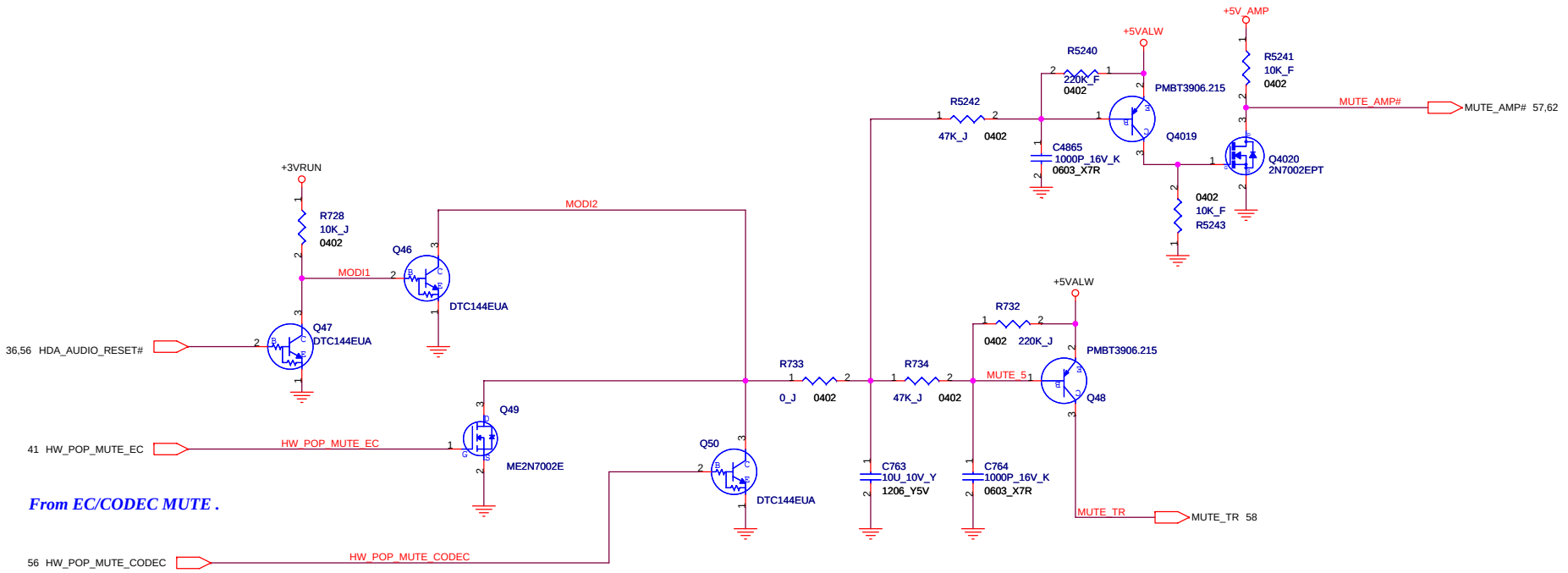

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO (MUTE)	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 59 of 79	

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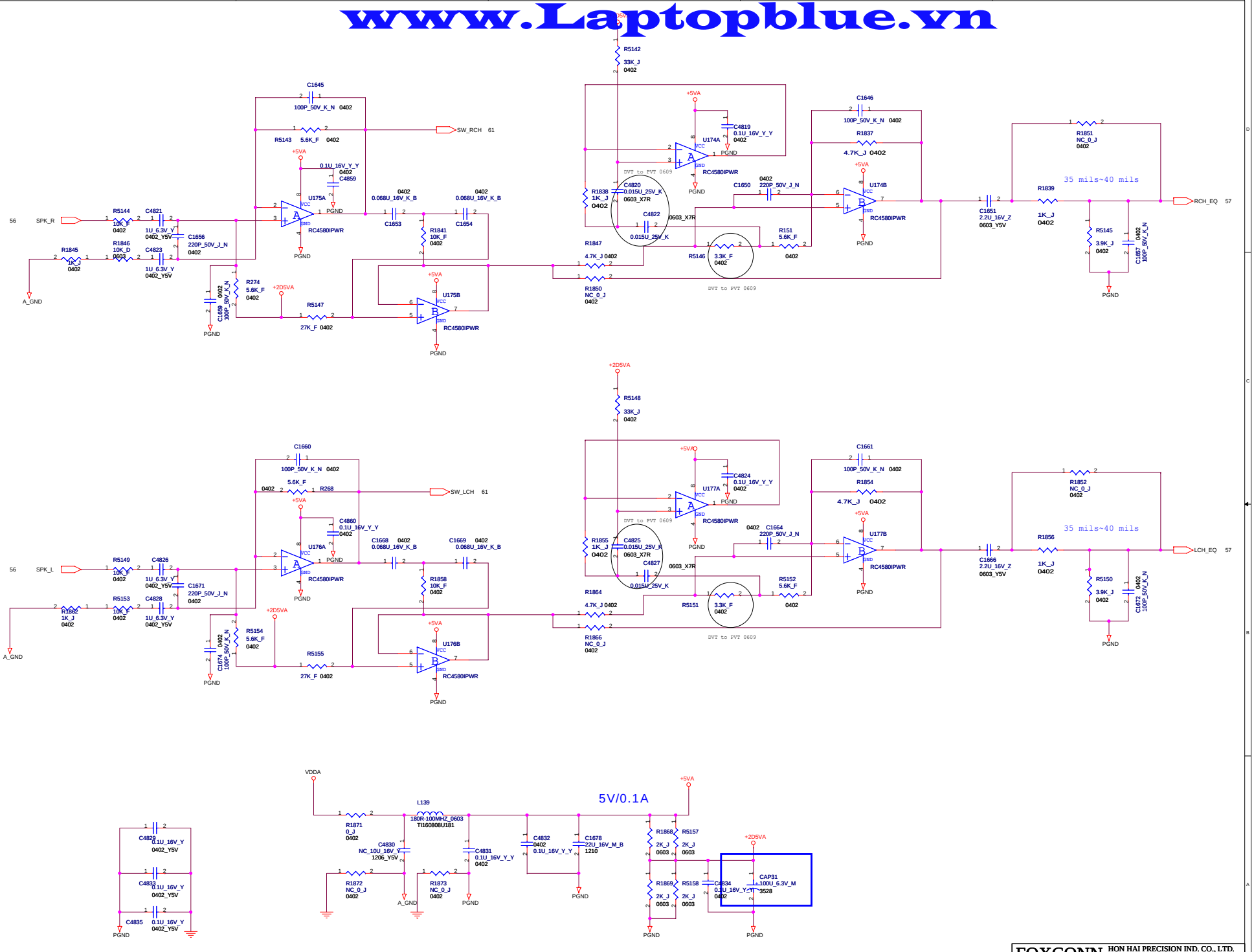

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO(EQ)	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 60 of 79	

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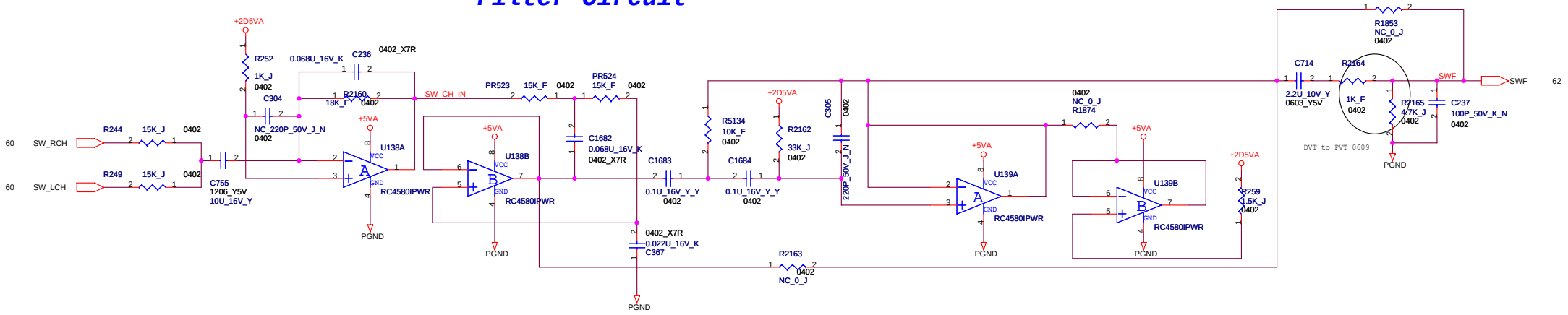
Vendor recommendation not use for
1) Input impedance
As described in the datasheet (P5),match input impedance at IN+ and IN-.
We are afraid of pop noise on this board.
Current SWF impedance is too big, so we recommend to reduce SWF output impedance.
Does R2164,R2165 and C237 Circuit need?

Filter Circuit



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Filter Circuit		
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 61 of 79	

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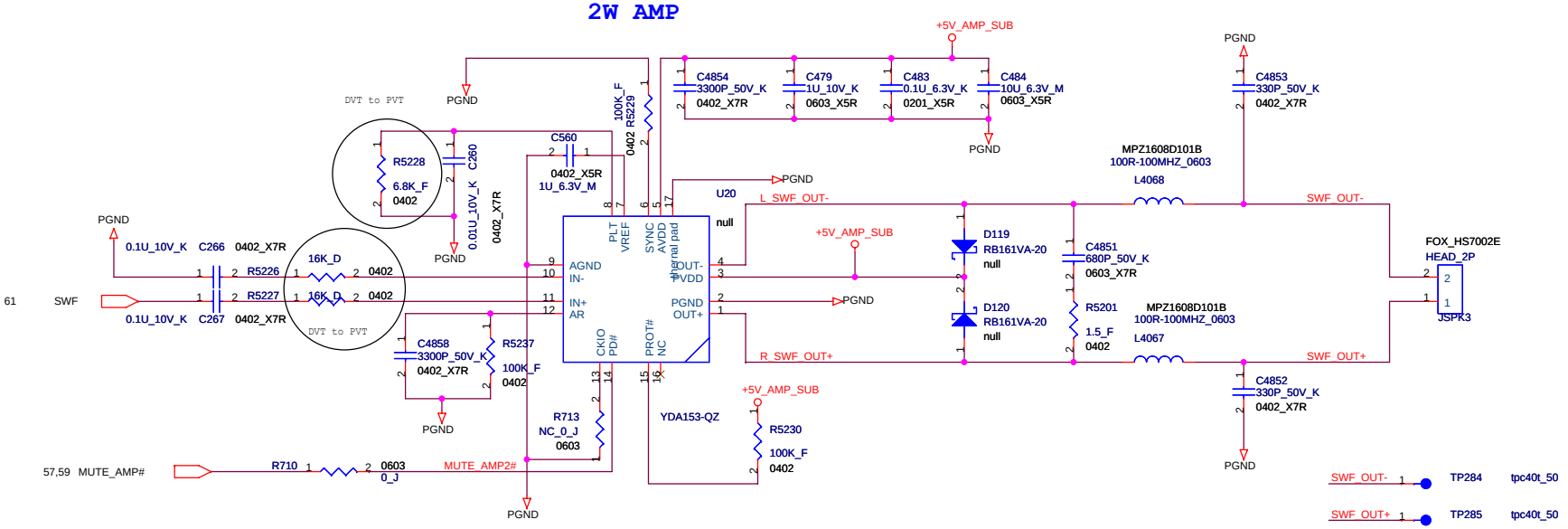
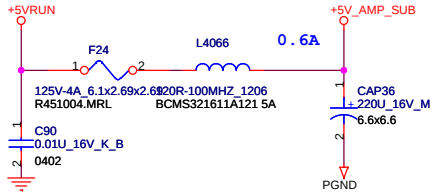
SUB_WOOFER AMP

C479,C484
Locate them close to PVDD pin

2W AMP



SUB_WOOFER POWER



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(Subwoofer AMP)		
Size A3	Document Number M780(MBX-194)		Rev 0.1
Date: Friday, June 27, 2008	Sheet 62 of 79		

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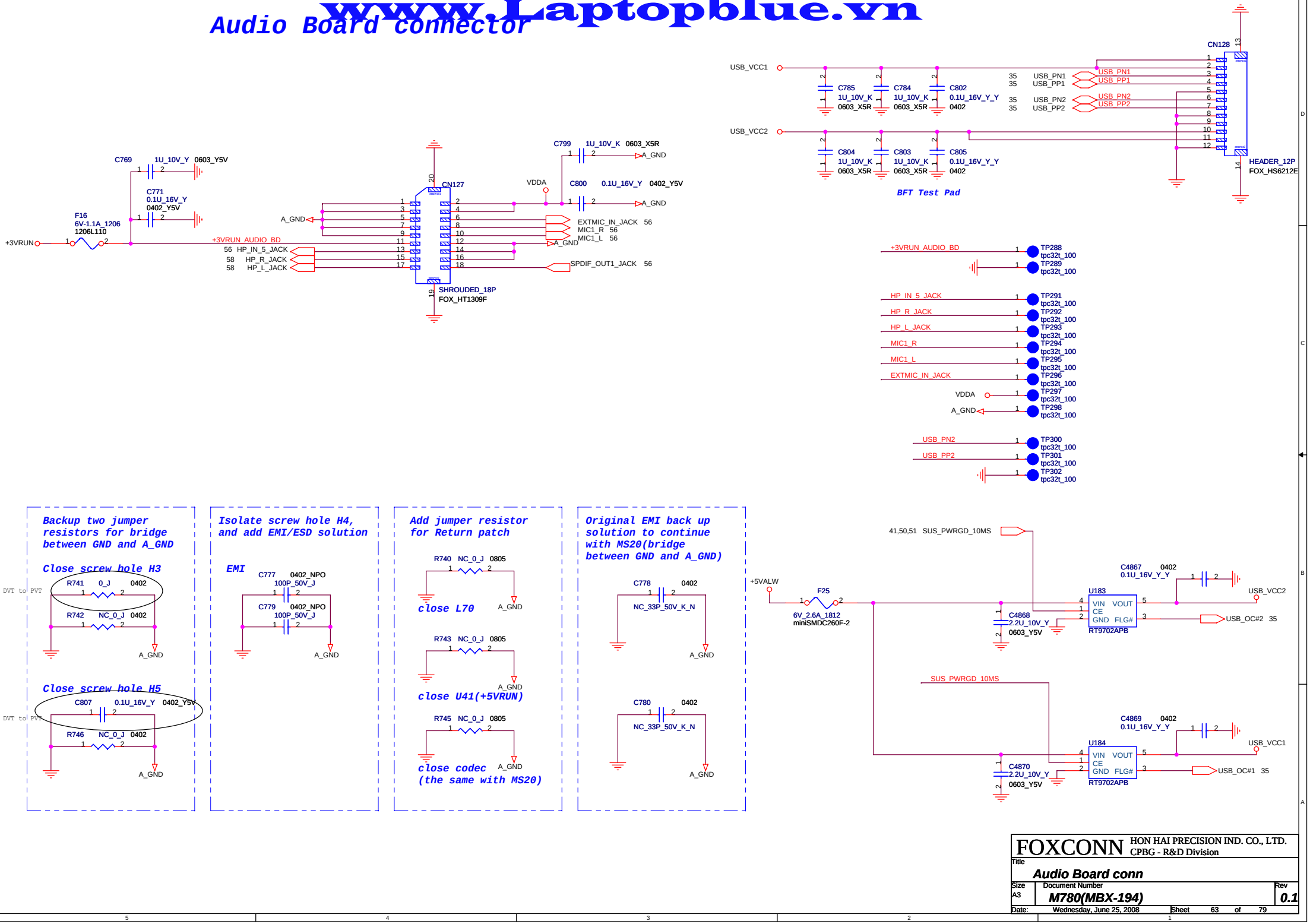
Audio Board connector



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Audio Board conn	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Wednesday, June 25, 2008	Sheet 63 of 79	

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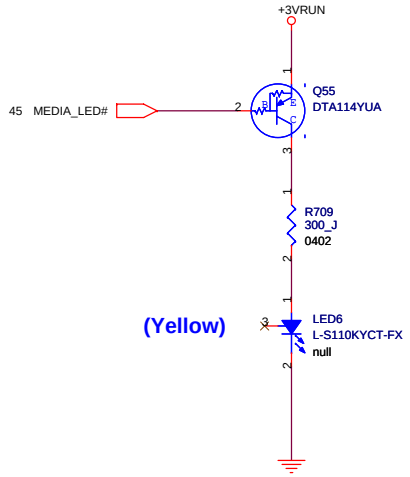
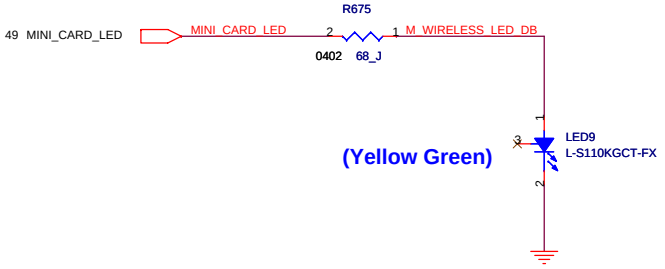
MS/SD LED



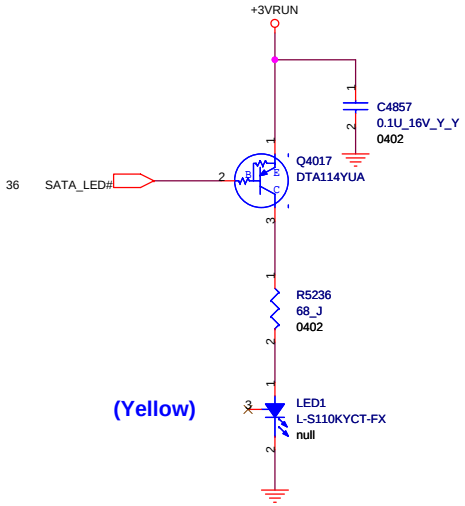
230.(Page 64) 07/12/05 Change MS/SD LED control signal share one LED

WLAN/BLUETOOTH LED

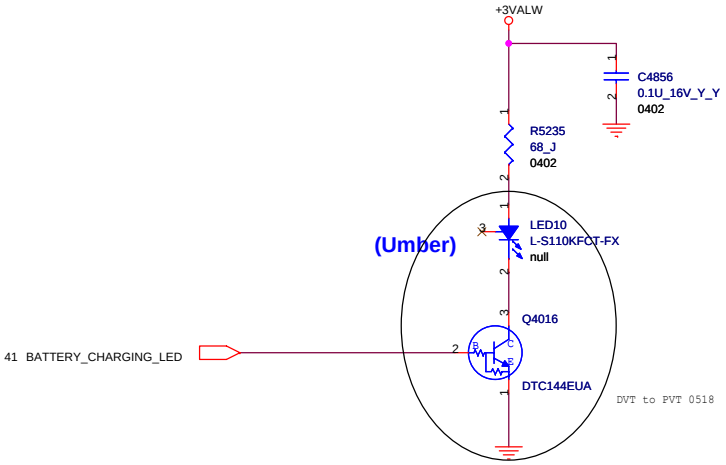


232.(Page 64) 07/12/05 Change Wirless/BluetoothLED control signal share one LED

HDD/ODD LED



Charge LED



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED status	
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Friday, June 13, 2008	Sheet 64 of 79	

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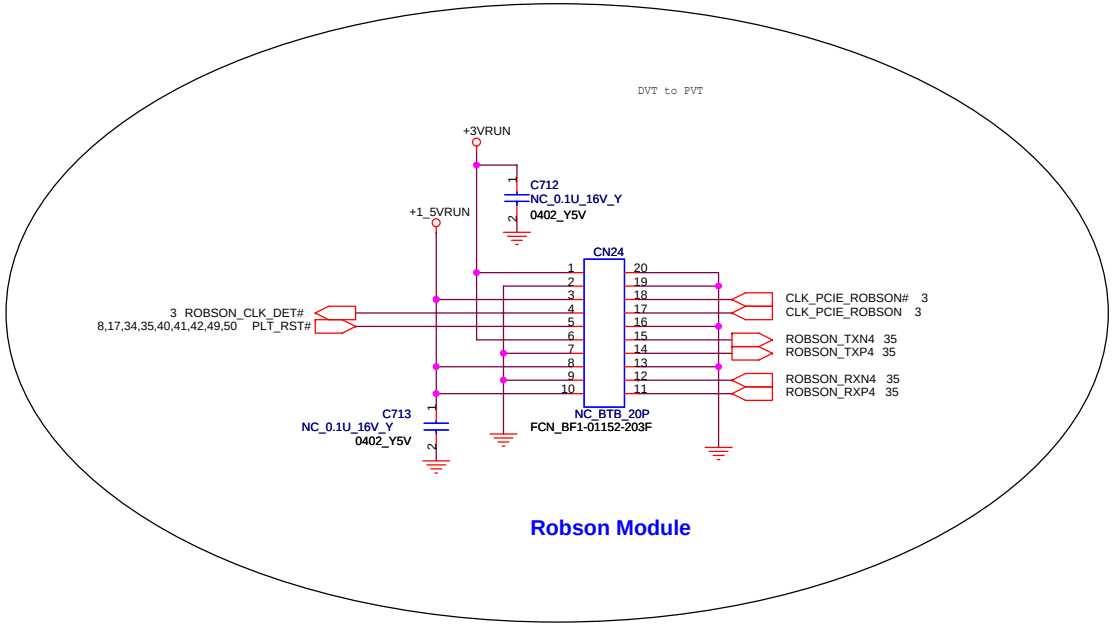

Robson Module

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Robson1.6 Connector***	
Size A3	Document Number ***M780(MBX-194)***	Rev ***0.1***
Date: Wednesday, June 25, 2008	Sheet 65 of 79	

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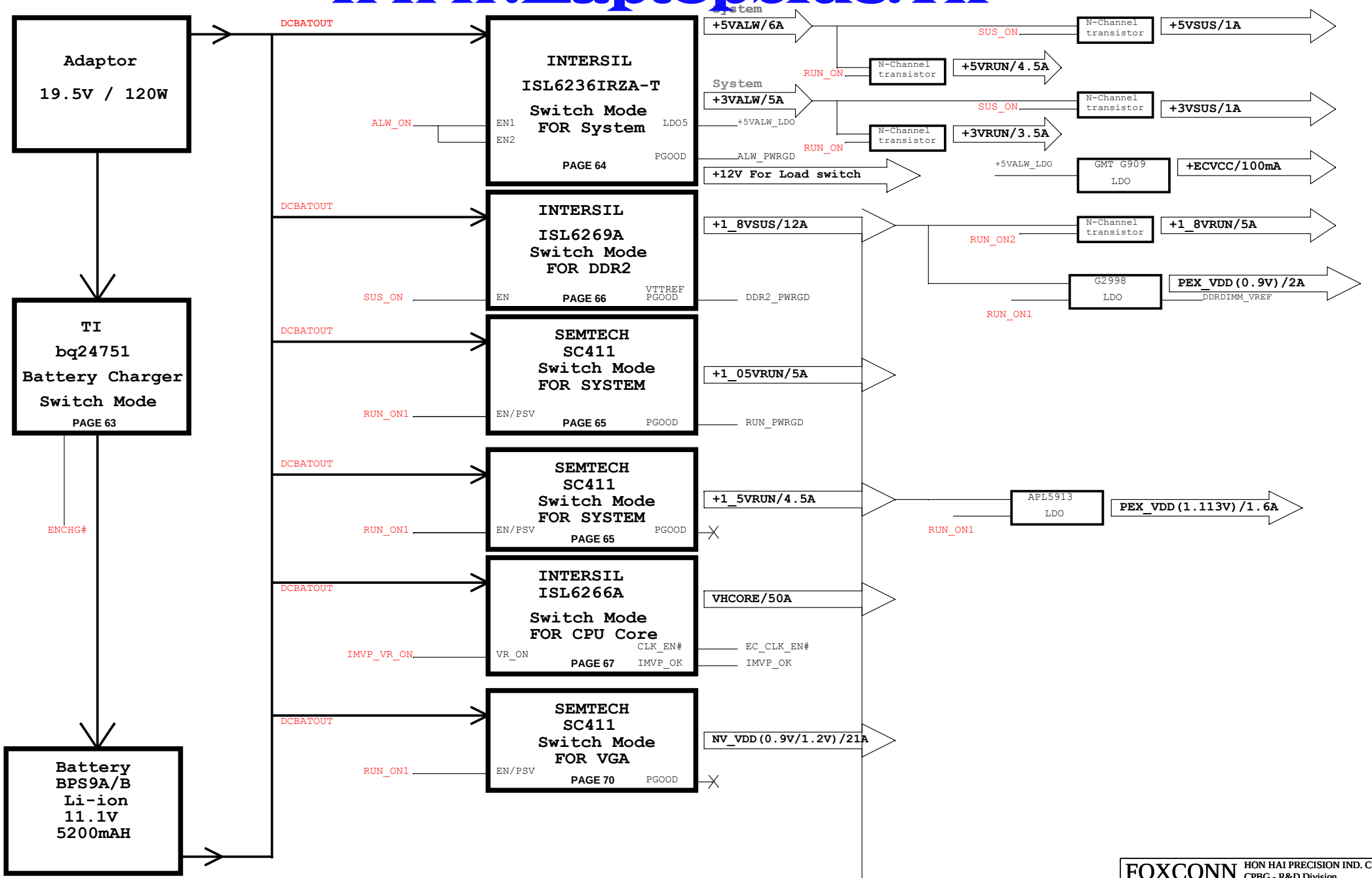
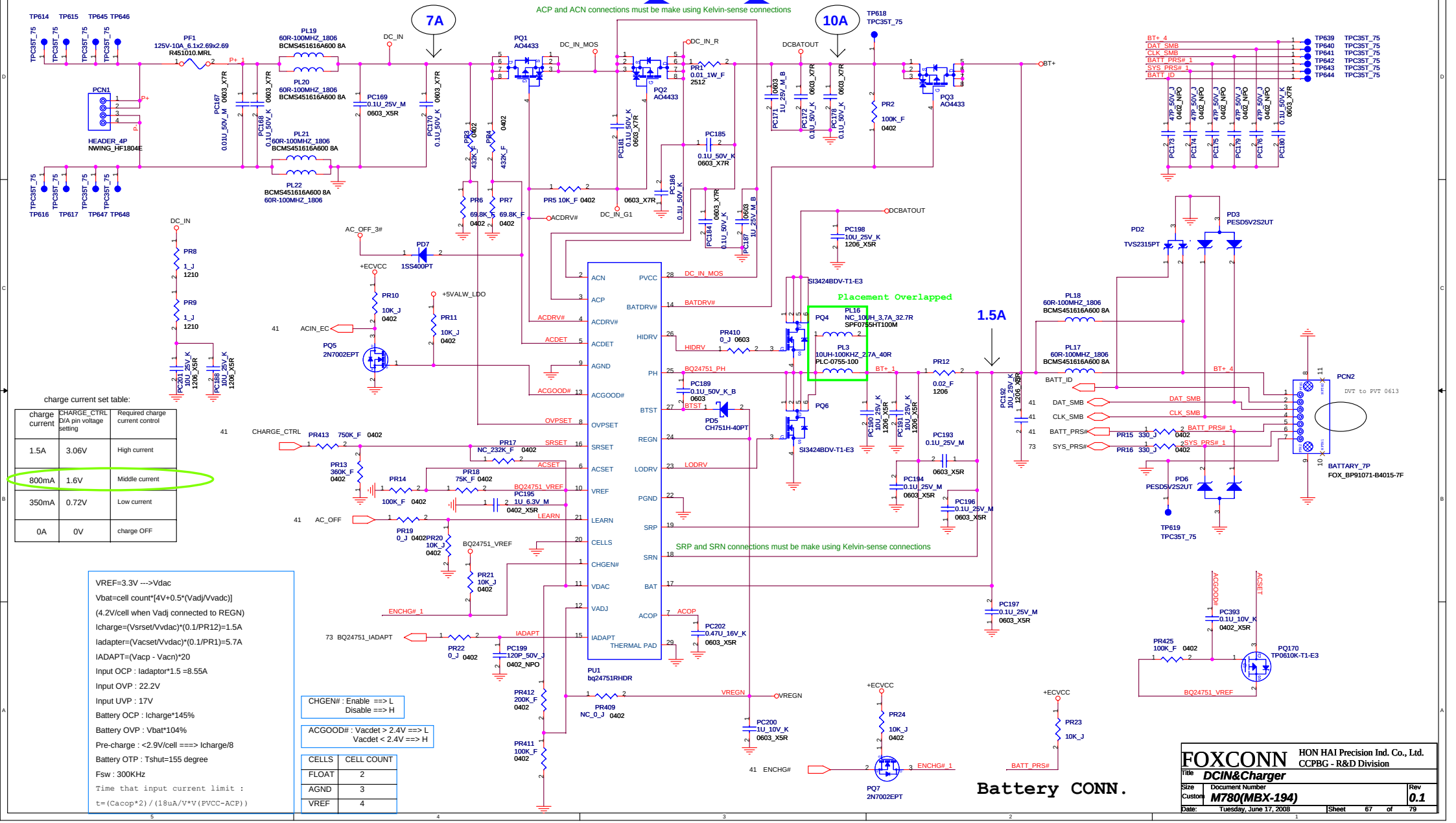


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*Power Design Diagram*	
Size: Custom	Document Number: *M780(MBX-194)*	Rev: *0.1*
Date: Friday, June 13, 2008	Sheet 66 of 79	

www.Laptopblue.vn



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
800mA	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V --->Vdac
Vbat=cell count*[4V+0.5*(Vadj/Vvadc)]
(4.2V/cell when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR12)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR1)=5.7A
IADAPT=(Vacp - Vacn)*20
Input OCP : Iadaptor*1.5 =8.55A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))

CHGEN# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DCIN&Charger		
Size: Custom	Document Number: M780(MBX-194)		Rev: 0.1
Date: Tuesday, June 17, 2008		Sheet 67 of 79	

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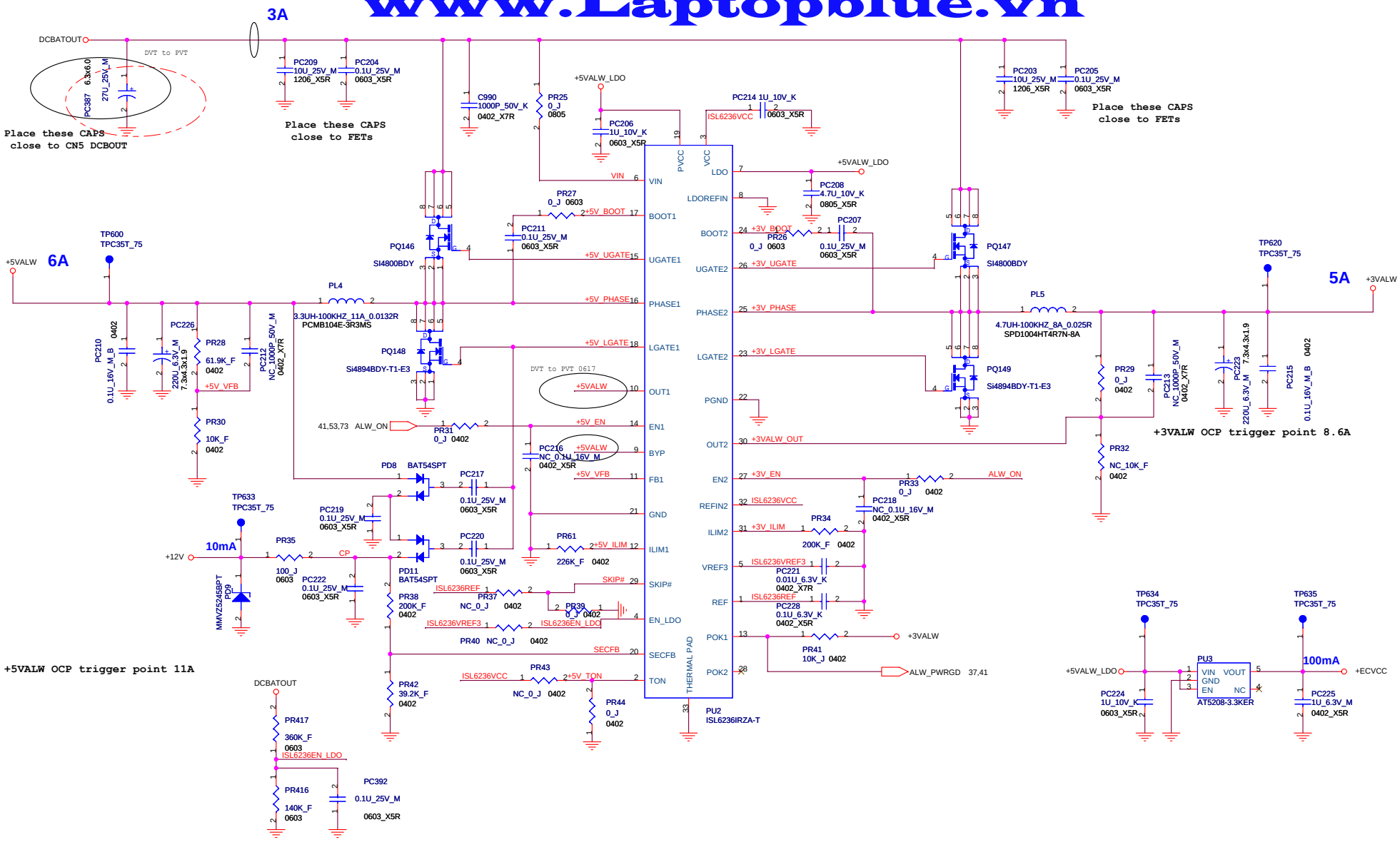

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))

Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u

+5VALW=((PR28/PR30)+1)*VFB1

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	SYS Power (+3_3V/+5V)		
Size: Custom	Document Number: M780(MBX-194)		Rev: 0.1
Date: Tuesday, July 01, 2008	Sheet 68 of 79		

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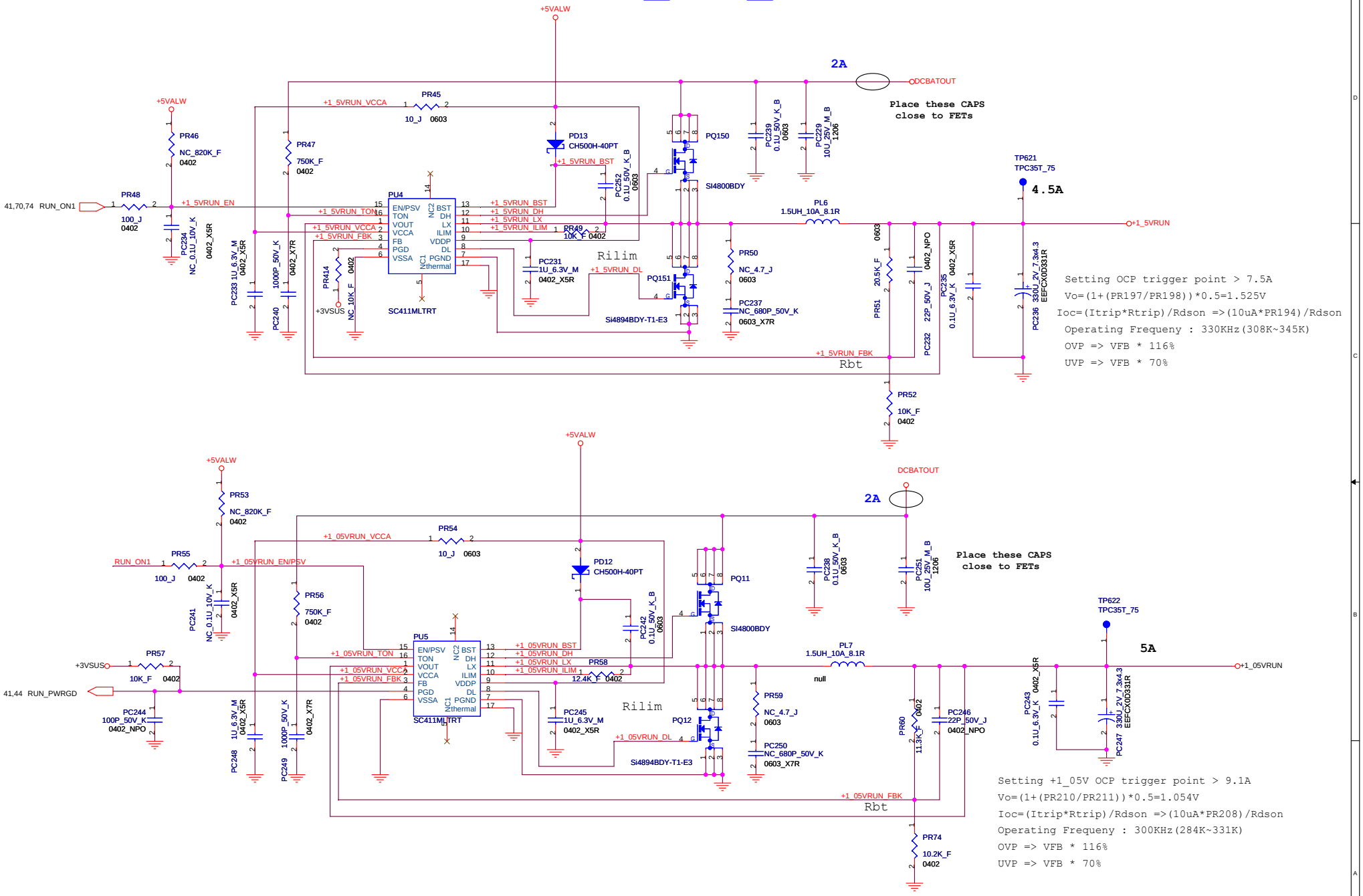

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_5V/+1_05V)	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Tuesday, June 17, 2008	Sheet 69 of 79	

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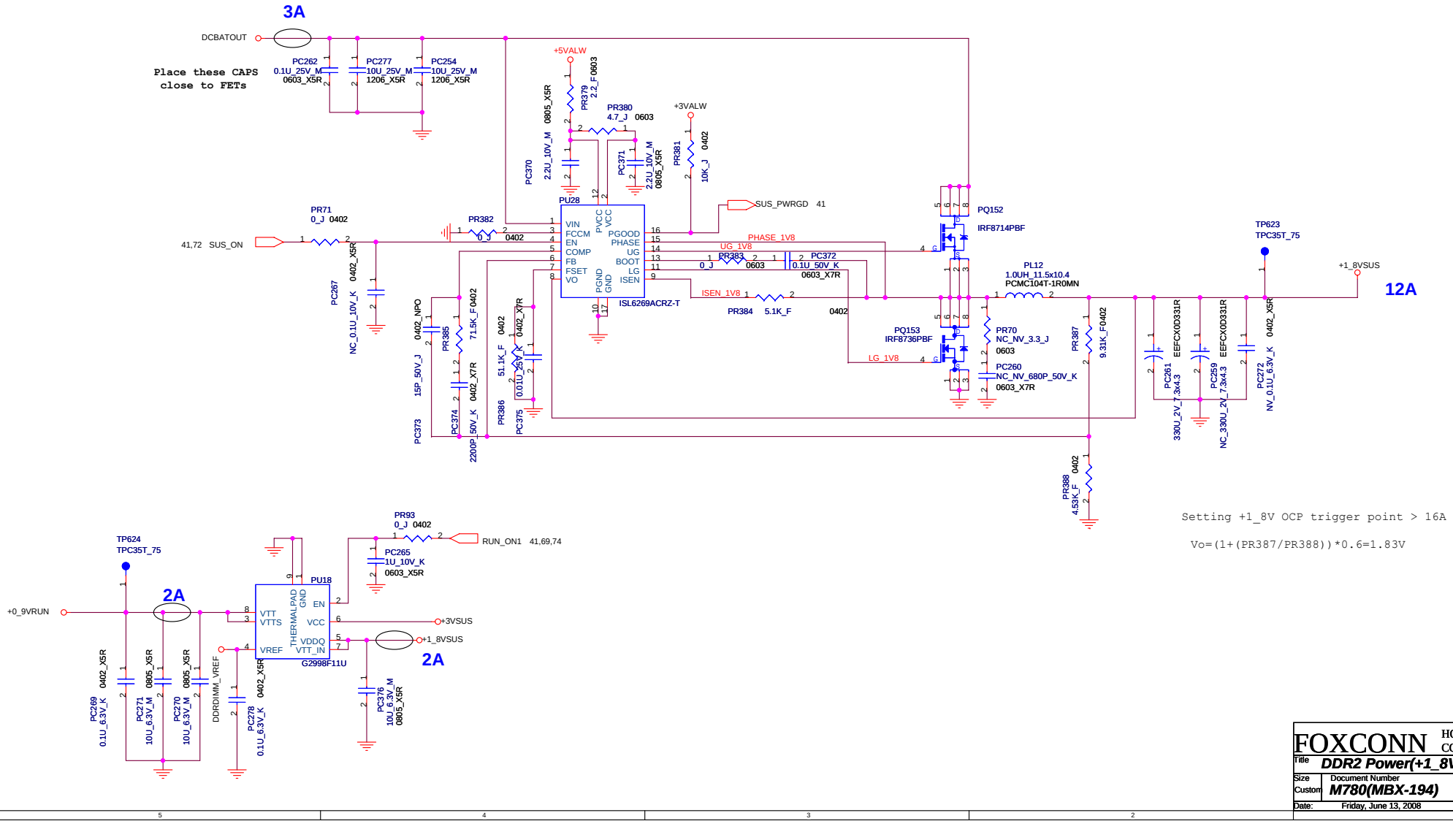

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR2 Power(+1_8V/+0_9V)	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Friday, June 13, 2008	Sheet 70 of 79	

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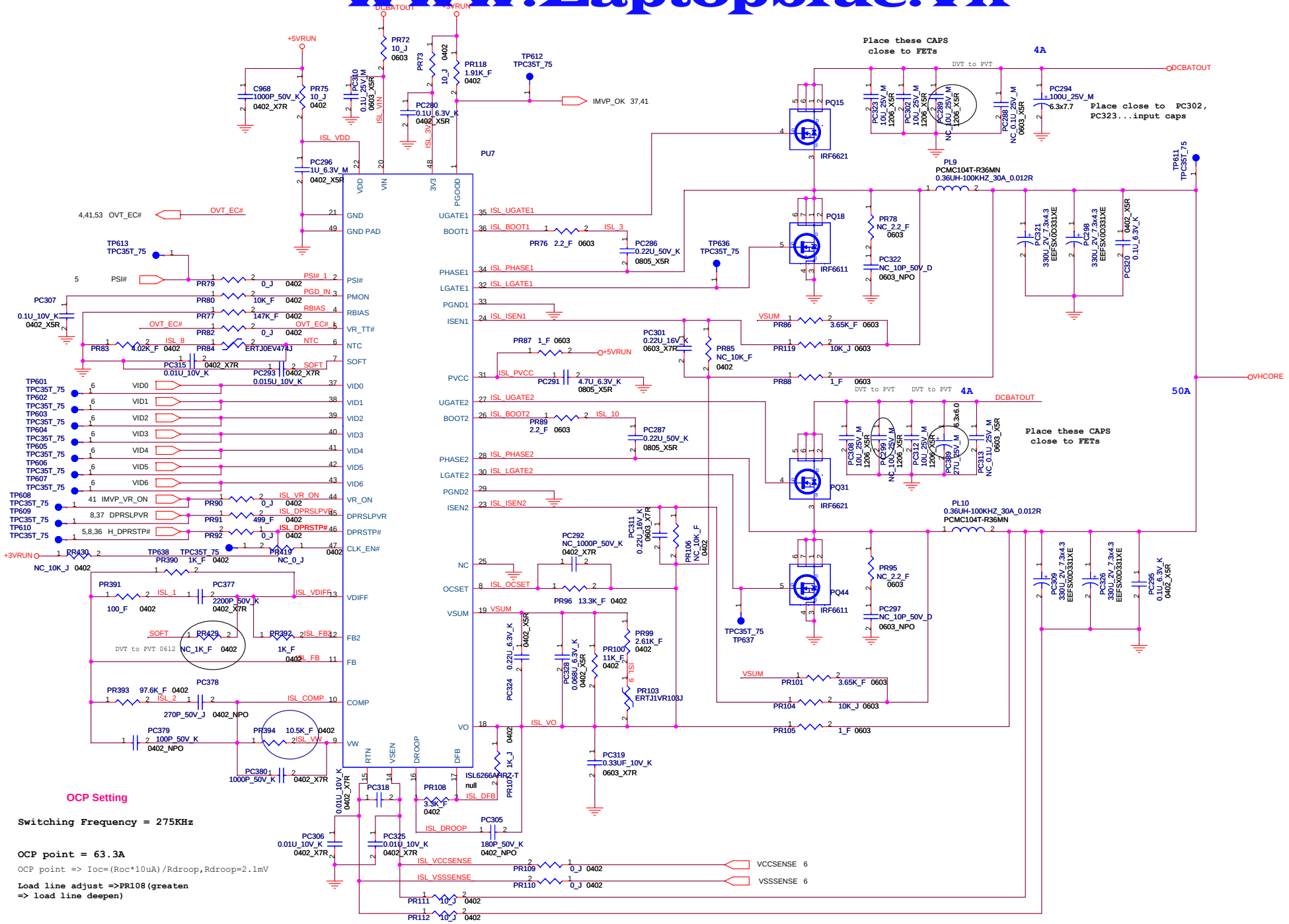

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CPU_Vcore---ISL6266A		
Size: Custom	Document Number: M780(MBX-194)		Rev: 0.1
Date: Tuesday, July 01, 2008	Sheet 71 of 79		

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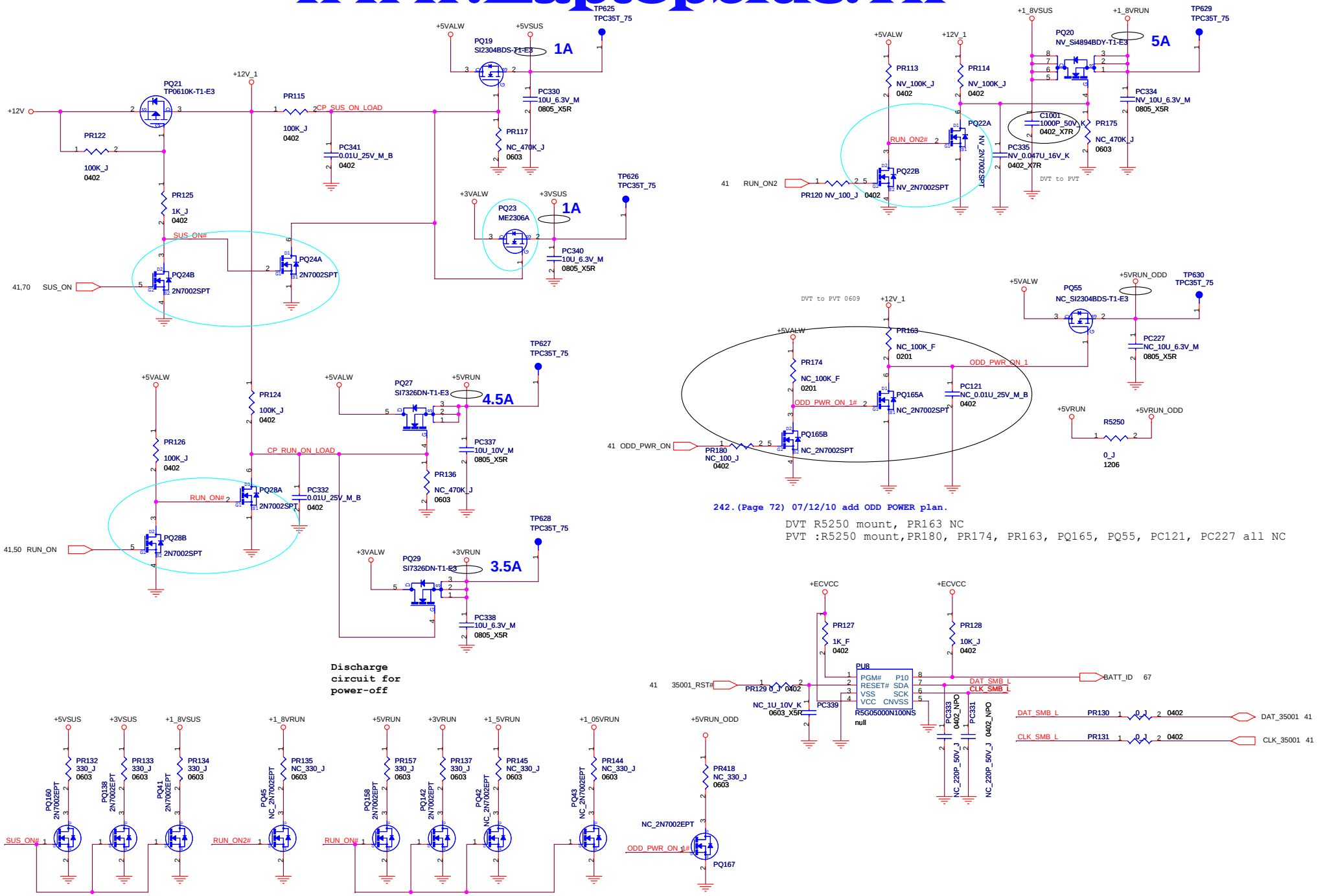

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
Date: Tuesday, June 17, 2008	Sheet 72 of 79	

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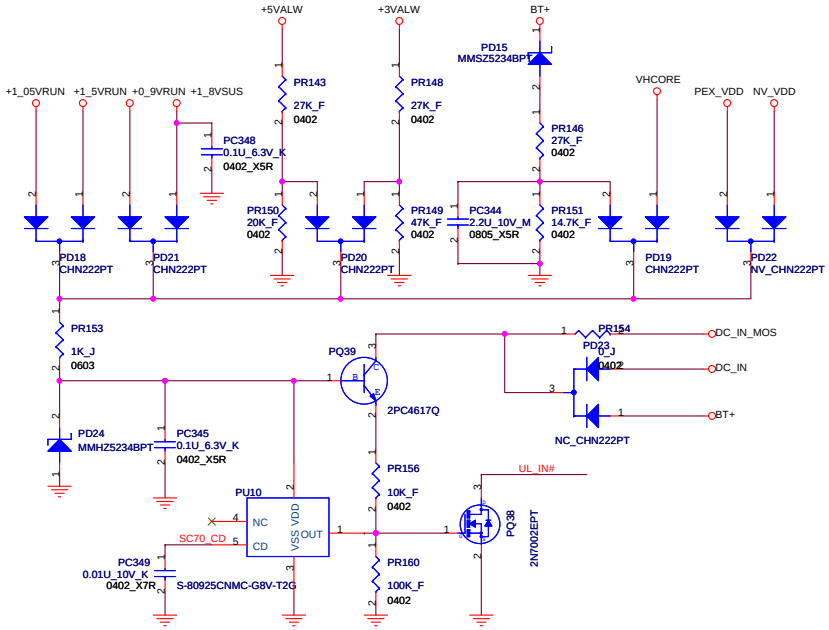
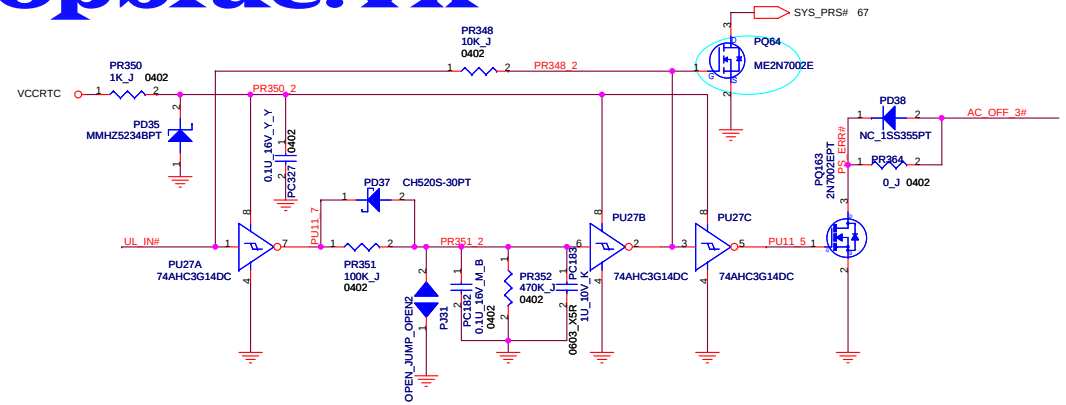
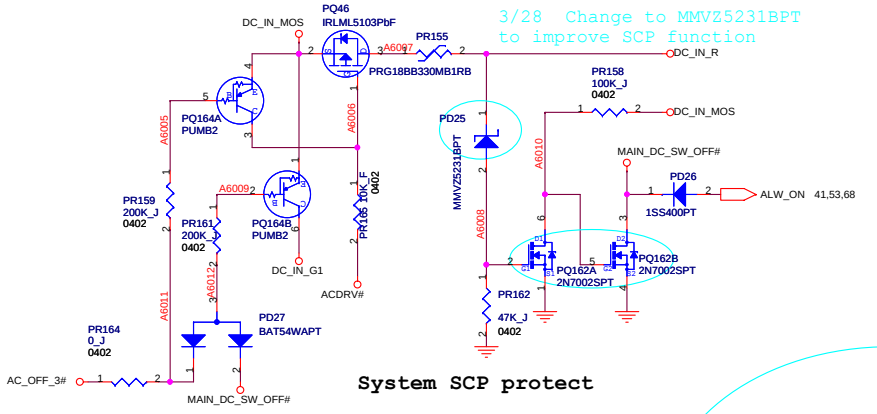
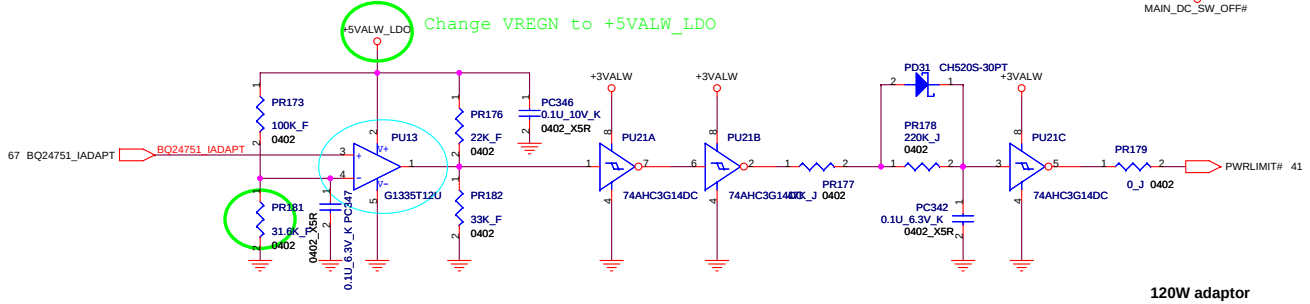


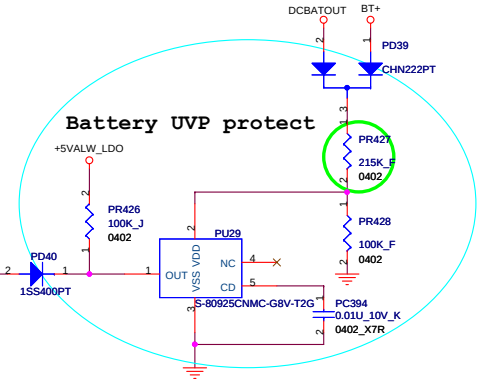




3/28 Change to MMVZ5231BPT to improve SCP function

System SCP protect





3/28 Add battery UVP protect circuit to separate SCP and OCP function.

120W adaptor

PWRLIMIT	1.2V/114W

Adaptor max load: 7.7A under 3 sec
Adaptor OCP: 9.7A typ
11A max

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: OVP protection		
Size: Custom	Document Number: M780(MBX-194)	Rev: 0.1
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TABLE(01/08)

NB9P	I/O	Inter pull low			PR402: 23.2K_1%_0402,1R-0002322-F200 PR272: 61.9K_1%_0402,1R-0006192-F200
GPU Voltage			1.05V	0.9V	
PWRCNTL_0	O	Yes	H	L	

NB9M	I/O	Inter pull low			PR423: 29.4K_1%_0402,1R-0002942-F200 PR424: 39.2K_1%_0402,1R-0003922-F200
GPU Voltage			1.17V	0.9V	
PWRCNTL_0	O	Yes	H	L	

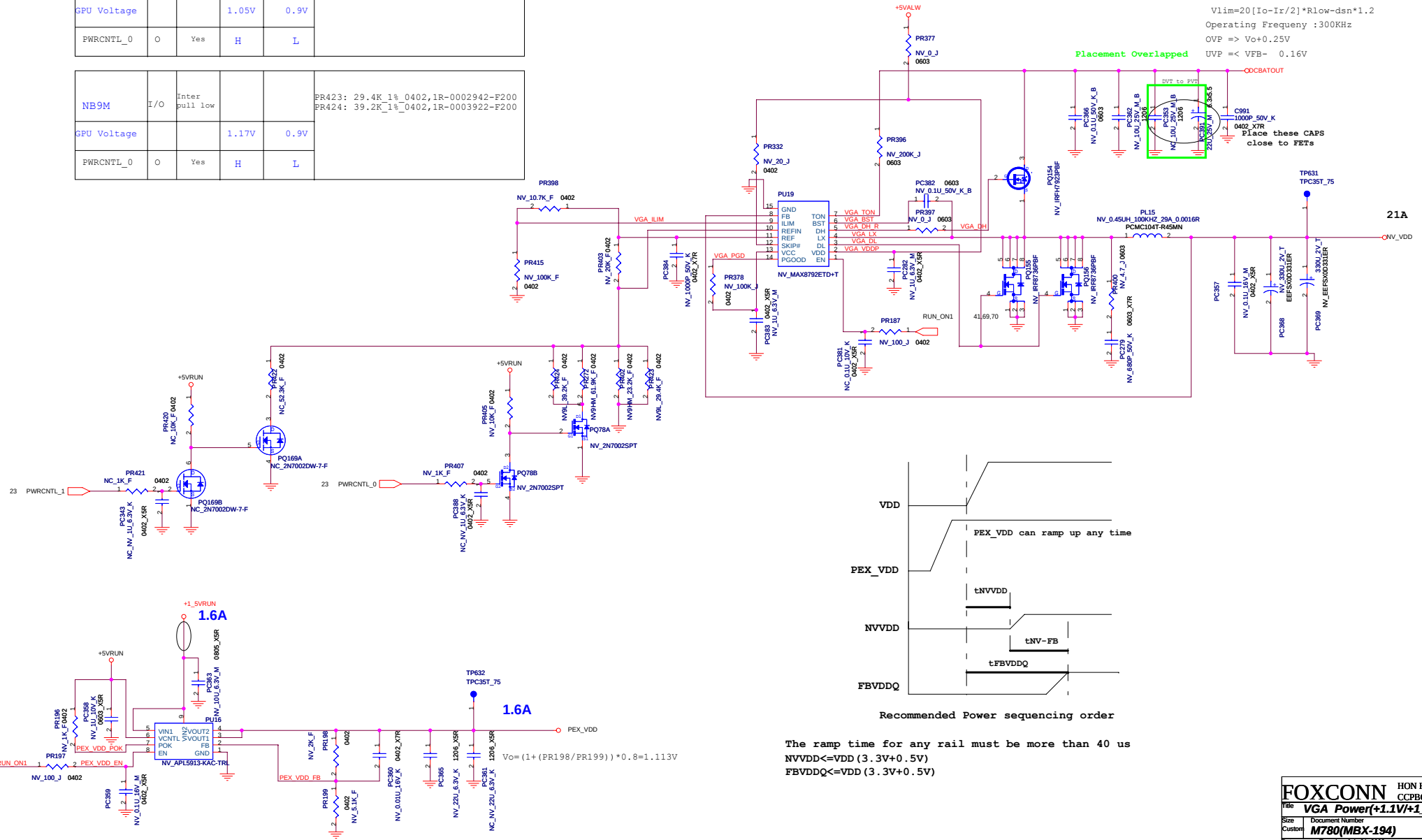
Setting current limit trigger point >25A
Vo=Vf; Vf=((PR272+PR402)/(PR403+PR272+PR402))*2
Vlim=20[Io-Ir/2]*Rlow-dsn*1.2
Operating Frequeny :300KHz
OVP => Vo+0.25V
UVP =< VFB- 0.16V

Placement Overlapped

DVT to PVT

Place these CAPS close to FETs

21A



Recommended Power sequencing order

The ramp time for any rail must be more than 40 us
NVVDD<=VDD(3.3V+0.5V)
FBVDDQ<=VDD(3.3V+0.5V)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	VGA_Power(+1.1V/+1_2V)		
Size: Custom	Document Number: M780(MBX-194)		Rev: 0.1
Date: Tuesday, July 01, 2008	Sheet 74 of 79		

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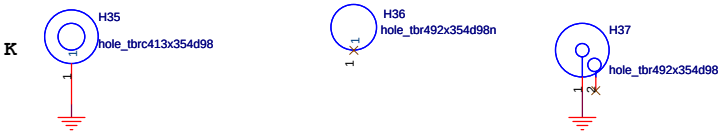
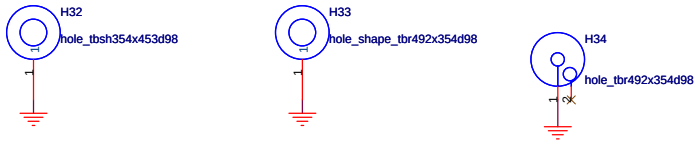
HOLE(TOP SIDE)

Type 1





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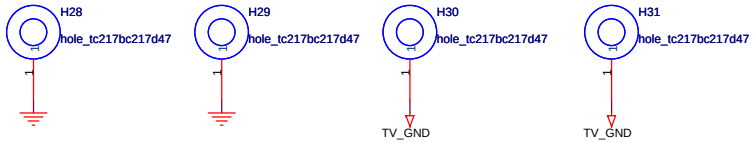
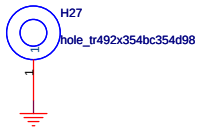
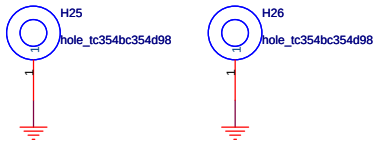


Type 3



Type 4



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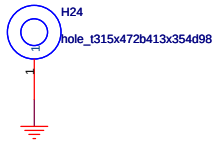
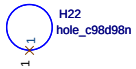
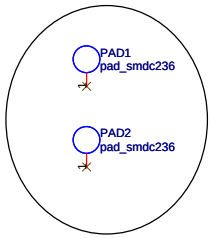


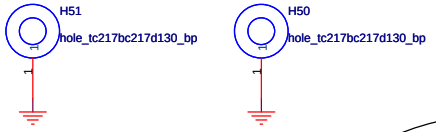
Type 6



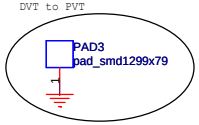
DVT to PVT 0617



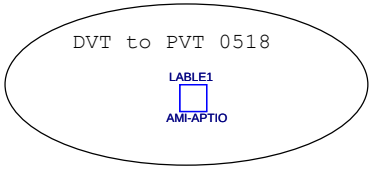
Robason Hole



DVT to PVT

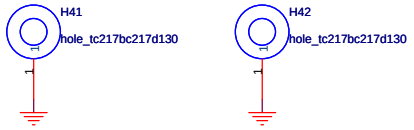


DVT to PVT 0518

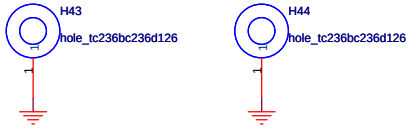


HOLE(BUTTOM SIDE)

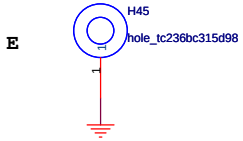
Type 2



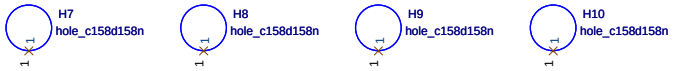
Type 3

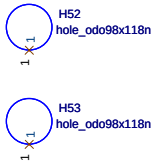


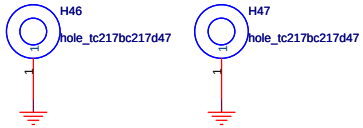
Type 4

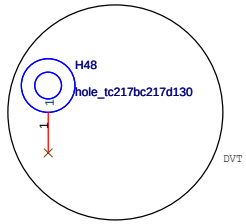


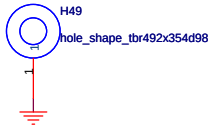
Type CPU











FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: HOLE & BOSS		
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1
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M780 EVT Change History

1.(Page 37) 07/08/21 As ICH9 LAN_RST# need to pull low to GND,Add 10K to GND.
2.(Page 41) 07/08/21 Change EC Ping38(RUN ON2) pull low value from 100K to 4.7k.
3.(Page 38) 07/08/29 Dut to HDA bus is changed to 1.5V level, HDA_CODEC_RST# signal is not able to turn on MOSFET "Q47", so changed to 3V for HDA Power Plane.
4.(Page 61) 07/09/07 finger print solution update (UPEK cost down)
5.(Page 57) 07/09/07 Change Codec from CXD9872AKDNBEC3XR to ALC889S for Audio solution.
6.(Page 57) 07/09/07 Change resistor of codec BEEP (R683) to 10k depend on W(V^2/R).
7.(Page 57) 07/09/15 Change thermal sensor(U59) to 15-EMC1402-0000.
8.(Page2) 07/09/19 Lid interface mark "PS2" change to placed at T/P block.
9.(Page 33) 07/09/19 delete all "CA" marking of components.
10.(Page 55) 07/09/19 remove D-MIC to CAM path and clear D-MIC circuit.
11.(Page 23) 07/09/19 delete PLVDD plane for all.
12.(Page 41) 07/09/26 Change EC from WPC8763L to WPCE775L for EMI issue.
13.(Page 48) 07/09/26 Change BT Power switch from SI9183DT-33-T1-E3 to SiP21106DT-33-E3 for EOL.
14.(Page 44-47) 07/09/26 Change PCI Card reader from PCI8412 to R5C833 for CF card soultion.

POWER Change History

15.(Page 64) 07/09/28 Change PQ6 IR7904 to PQ146/PQ148:SI4800B/SI4894 ==>component cost down
16.(Page 64) 07/09/28 Change PL4 from 3.3U(CY) to 4.7U(AOL)==>component cost down
17.(Page 64) 07/09/28 Change PQ9 IR7904 to PQ147/PQ149:SI4800B/SI4894==>component cost down
18.(Page 64) 07/09/28 Change PL5 from 3.3U(CY) to 4.7U(AOL)==>component cost down
19.(Page 64) 07/09/28 Change PU2 AGND to PGND
20.(Page 65) 07/09/28 Change PQ10 IR7904 to PQ150/PQ151:SI4800B/SI4894==>component cost down
21.(Page 65) 07/09/28 Change PL7 from 1.0U(CY) to 1.5U(CY) for improve efficiency
22.(Page 65) 07/09/28 Change Pc247 from 330U(EEFSX) to 330U(EEFCX) ==>component cost down
23.(Page 65) 07/09/28 delete PC230==> cost down
24.(Page 65) 07/09/28 Change PU4,PU5 from AGND to PGND
25.(Page 66) 07/09/28 Change DDR solution FROM TPS5116 to ISL6269A+G2998F11U ==>cost down
26.(Page 67) 07/09/28 Change CPU PWM IC PU7 from ISL6262A to ISL6266A,and PR390 from 1.82k to 1k,PR391 from 453 to 400,PC316 from470P TO 2200P,PR398 from NC to 1k,PR393 from 182k to 97.6k,PC379from 120P to 100P,PR394 from6.81k to 8.25k.
27.(Page 67) 07/09/28 Change PU7 AGND to PGND
28.(Page 68) 07/09/28 Change PQ27 SI4800B to SI7362DN
29.(Page 70) 07/09/28 Change PU15 TPS5117 to PU19 SC411 solution for TPS5117 light loading bug
30.(Page 70) 07/09/28 Change PU16 from APL5912 to APL5913==> cost down
31.(Page 65) 07/09/29 Change PL6 from 1.5U(CY) to 1.5U(AOL)==>component cost down
32.(Page 64/65/66/70) 07/09/29 Change PC210/PC215/PC235/PC243/PC256/PC357 from 0.1U_0402_Y5V to 0.1U_0402_X5R_6.3V due to power regulator output filter cap temperature chateractor tolerance.
33.(Page 70) 07/09/29 Add PR407,PR408 0_0402 for remote sense detect
34.(Page 63) 07/09/29 Add PR410: 0_0603,reserve for EMI.
36.(Page 63) 07/09/29 channge to program charger voltage ; add PR412: 191K, PR411: 100k ,reserve PR409
35.(Page 63) 07/09/29 channge charger current setting to DAC input ; add PR413:750K,change PR13 from 100k to 499k,delete PR17: 232K
37.(Page 65) 07/09/29 reserve PR414 for 1.5V power good pull high resistor.
38.(Page 65) 07/09/29 change 1.05V power good pull high power from +3Vrun to +3Vsus ==>design issue
39.(Page 65) 07/10/03 delete PC253==> cost down
40.(Page 65) 07/10/03 Change PQ11/PQ12 FDS8880/FDS8896 to SI4800B/SI4894==>component cost down
41.(Page 65) 07/10/03 Change PL7 from 1.5U(CY) to 1.5U(DELTA)==>component cost down
42.(Page 65) 07/10/03 Change PL6 from 1.5U(AOL) to 1.5U(DELTA)==>component cost down
43.(Page 68) 07/10/03 Change PQ29 FDS8880 to SI7362DN
44.(Page 68) 07/10/03 Change PQ20 FDS8896 to SI4894
45.(Page 63) 07/10/03 Change PD2 from PESD15VS2UT to SMD15C because PESD15VS2UT have shortage issue
46.(Page 51) 07/10/05 Change USB Power Plane from +5VSUS to +5VALW.
47.(Page 3) 07/10/05 Update R2087 Pull High to +3VRUN.
48.(Page 3) 07/10/05 Change resistor(1947) to unstuff.
49.(Page 64) 07/09/29 reserve PC387:ECCAP:100U(NC);PC388POSCAP:15U(NC) near CN5 DCBOUTfor NOISE debug
50.(Page 3) 07/10/08 Change CLK gen from ICS9LPRS365 to ICS9LPRS392.
51.(Page 3) 07/10/24 Change CLK gen from ICS9LPRS392 to SLZ8648LFXC for cost down.
52.(Page 60) 07/10/24 Add Subwoodер circuit for MOR side request.
53.(Page 60) 07/10/24 Add Robson2 circuit for MOR side request.
54.(Page 41) 07/10/24 Change GPIO Expander from W83L603G to IW83L604G.
55.(Page 41) 07/10/24 Update EC(Pin define)for M760 Project.
56.(Page 47) 07/10/24 Add C987,C989 for design rule.
57.(Page 60) 07/10/24 Add TV tuner power sequence request need two GPIO pin controller time (RUN_ON_TV1,RUN_ON_TV2) for TV team.
58.(Page 47) 07/10/24 Add two GPIO pin(CF_REQ_IN1#,CF_REST) controll reset (JMB368 and CF Card) for CF time request.
59.(Page 18) 07/10/26 updated the circuit Strapping portion for NVDIA.
60.(Page 23) 07/10/26 updated the circuit Strapping portion for NVDIA.
61.(Page 24) 07/10/26 updated the circuit Strapping portion for NVDIA.
62.(Page 3) 07/10/26 updated BLOCK DIAGRAM for AUDIO function.
63.(Page 32) 07/10/29 updated LVDS Pin define.
64.(Page 33) 07/10/29 delete GAMMA function for MOR side request.
65.(Page 3) 07/10/30 delete R3017 for CF solution.
66.(Page 35) 07/10/30 updated USB function define for ICH9 USB Port.
67.(Page 34) 07/10/30 delete USB_PN11,USB_PN11 pin for TV tuner function.
68.(Page 3) 07/10/30 updated BLOCK DIAGRAM for AUDIO function.
69.(Page 32) 07/10/30 add NV_ODD_RXIN3-,NV_ODD_RXIN3+,NV_EVEN_RXIN3-,NV_EVEN_RXIN3+,for LVDS Pin define.
70.(Page 42) 07/10/31 Change U27 Flash ROM from 13-W25X80V-7000(8M) to 13-W25X16V-7000(16M).
71.(Page 30) 07/11/1 Remove S-OUT Circuit according to MOR side information.
72.(Page 18) 07/11/06 Update VGA Portion.
ROM_SI should follow below memory strap setting
RAM_CFG[3:0] Config FB Bus Width Definitions
0000 64-bit Reserved
0001 16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010 16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011 16Mx32 GDDR3 - 136 ball 64-bit Samsung
0100 64-bit Reserved
0101 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung
73.(Page 18) 07/11/06 Change ROM_SO to 5Kohm pull up to 3.3V
74.(Page 18) 07/11/06 Change ROM_SCLK to 15Kohm pull down to GND.
75.(Page 18) 07/11/06 Change Strap0 to 5K pull ulp to 3.3V
76.(Page 19) 07/11/06 Change Components for FBVref switch can be NC(R794,R795,C871,R578,R494 and Q52)
77.(Page 19) 07/11/06 FBA_Debug just reserve a TP.
78.(Page 20) 07/11/06 FBC_Debug just reserve a TP.
79.(Page 20) 07/11/06 According to PDN update for FBCAL_PD_VDDQ is 44.2Ω, FBCAL_PU_GND is 30.9Ω, FB_CAL_TERM_GND is 40Ω
80.(Page 22) 07/11/06 delete bead L70 for IFPAB_PLLVDD.
81.(Page 22) 07/11/06 delete bead L71 for IFPAB_IOVDD.
82.(Page 22) 07/11/06 delete bL72 for IFPCD_PLLVDD.
83.(Page 22) 07/11/06 add 10Kohm pull to GND for IFPD_IOVDD.
84.(Page 23) 07/11/06 Change R4799,R4800,R4812,R4801 and C956 to NC.
85.(Page 23) 07/11/06 delete R1775,R815 for VGA portion.
86.(Page 24) 07/11/06 Add IFPEF_PLLVDD to 10Kohm pull to GND.
87.(Page 24) 07/11/06 delete R4808,R4809,R4810,R4811 and C958 are not required.
88.(Page 24) 07/11/06 Change R4799,R4800,R4812,R4801 to NC.
89.(Page 26) 07/11/06 Change R4052 and R4103 to 475 ohm.
90.(Page 27) 07/11/06 Change R4594 and R4580 to 475 ohm.
91.(Page 41) 07/11/06 add GPIO PIN LVDS_CLK,LVDS_DATA,for LCD information.
92.(Page 55) 07/11/06 combined Camera & D-MIC for MOR requestion.
93.(Page 47) 07/11/06 add GPIO PIN CF_REST_IC#,CF_REST_CARD# for CF timeing.
94.(Page 34) 07/11/06 delete Mini Streo Jack,S-Video IN for MOR requestion.
95.(Page 41) 07/11/06 updated EC GPIO pin table for EC team requestion.
96.(Page 12) 07/11/06 updated VCC Power portion for yellow mark.
97.(Page 32) 07/11/07 Change U16 from GS48B2P1U to GS281RC1U by the comment from MOR side.
98.(Page 1) 07/11/12 updated Index page.
99.(Page 2) 07/11/12 updated Block diagram for HDMI and HDD mark.
100.(Page 3) 07/11/12 change CLK gen Power Plan.
101.(Page 3) 07/11/12 delete Clk gen damp resistor PR27~PR35.
102.(Page 8) 07/11/12 Change R206 from 511 ohm to 499 ohm for CRB.
103.(Page 8) 07/11/12 Change R5217 from 200 ohm 1%
104.(Page 18) 07/11/12 Add R5219 and R5221 for Hinex Strap.
105.(Page 22) 07/11/12 Change IFPAB_RSET to NC for NVIDA .
106.(Page 22) 07/11/12 2007/11/12 Update IFPC_IOVDD 0.385A
107.(Page 23) 07/11/12 2007/11/12 Update GPIO Table for NVDD 1.15V~1.2V.
107.(Page 23) 07/11/12 2007/11/12 Update I2C_ present status.
108.(Page 23) 07/11/12 Change GPIO1,GPIO7 and GPIO12~23 to NC for NVIDA .
109.(Page 30) 07/11/12 Change U10 from NC to populate.
110.(Page 30) 07/11/12 Change R284 from populateto NC
111.(Page 33) 07/11/12 Delete R2193,R2194 R1940,C1616,U136 for Cost down evaluation
112.(Page 34) 07/11/12 Change Ground from TV_GND1 to TV_GND.
113.(Page 40) 07/11/12 Add R559,R560,C715,C716 and Marvell.
114.(Page 40) 07/11/12 Change R596 from 4.86k to 4.99k
115.(Page 43) 07/11/12 Add C611 and D26 for STAT Power setting.
116.(Page 44) 07/11/12 Change R492 from populate to NC.
117.(Page 44) 07/11/12 Change R417 from NC to populate.
118.(Page 45) 07/11/12 Change L29 from 1L-FTR1DB6-5600 to 1L-F0D6560-TE00.
119.(Page 46) 07/11/12 Change R816,R820,R817 from populate to NC.
120.(Page 46) 07/11/12 Add R625 to Ground for design spec.
121.(Page 46) 07/11/12 Reverse +1_5VRUN Power plane for HDA Spec.
122.(Page 47) 07/11/12 Change R2525 from 8.2k to 6.8k
123.(Page 48) 07/11/12 Delete R601,Q26,R588,R597
124.(Page 49) 07/11/12 Add CN1 connector for full size Mini Card.
125.(Page 49) 07/11/12 Update pin define for wirless card spec.
126.(Page 49) 07/11/12 Change R593 from populate to NC.
127.(Page 49) 07/11/12 Add U9 for wriless and usb power switch.
128.(Page 49) 07/11/12 delete +3V_RUN power.
129.(Page 49) 07/11/12 delete R597.
130.(Page 49) 07/11/12 Add C10.
131.(Page 50) 07/11/12 Change U37 from TPS2231PW to TPS2231RGP for Cost down.
132.(Page 50) 07/11/12 delete R622,R630,R623,R629,C664,C665.
133.(Page 50) 07/11/12 Update power plan.
134.(Page 50) 07/11/12 delete Constant-voltage +1_5VSUS Circuit.
135.(Page 51) 07/11/12 remove U41 power switch to Function board.
136.(Page 53) 07/11/12 Add C481,C482,C579 for stable voltage.
137.(Page 53) 07/11/12 Change Q31 from MMC2301 to CHT2301PT.
138.(Page 53) 07/11/12 Change D27 from populate to NC.
139.(Page 57) 07/11/12 delete C732 for doulb part.
140.(Page 57) 07/11/12 Change C785,C784,C705 to R5222,R5223,R5224.
141.(Page 47) 07/11/12 Delete U169 (flash)for CF solution.
142.(Page 62) 07/11/13 Change sub_woofer amp to YAMAHA(YDA153A)
143.(Page 47) 07/11/13 Update HP circuit
144.(Page 47) 07/11/14 Add Audio Power(+12VRUN)PU6 for EQ power.
145.(Page 41) 07/11/14 Add GPIO pin (RUN_ON_A) for AUDIO power(EQ circuit) require.
146.(Page 41) 07/11/14 Change GPIO pin Net(EN_EXT_DEV_SENSE,BT_PRS#) for EC team require.
147.(Page 11) 07/11/14 Change R133 from populate to NC for system hang up soon when system boot up.
148.(Page 11) 07/11/14 Connect VCCD_QDAC to 1.5V RUN for Intel require.
149.(Page 32) 07/11/15 Change Net(NV_LCDVCC_EN#) to NV_LCDVCC_EN
150.(Page 36) 07/11/15 Add Net(ICH_GPIO56) pull high(10K ohm) to +3VALW.
151.(Page 36) 07/11/15 Change R375 from 332k to 330k.
152.(Page 38) 07/11/15 change vcclan3.3 from +3VSUS to +3VRUN
153.(Page 38) 07/11/15 change vccCL3.3from +3VSUS to +3VRUN
154.(Page 54) 07/11/15 Add EXPRESS CARD Connector(CN26),(CN29) for design require.
155.(Page 54) 07/11/16 Add CN123,CN124 for Design require
156.(Page 47) 07/11/16 Change U168 from GMT to RICOH
157.(Page 34) 07/11/19 Change Ground TV power sequence.
158.(Page 58) 07/11/19 Change CAP34 from 100u to 220u for Mor request.
159.(Page 62) 07/11/19 Change CAP35 from 100u to 220u for MOR request.
160.(Page 57) 07/11/20 Change Net(HP_IN) to HP_IN#.
161.(Page 26) 07/11/20 Change R4030,R4031,R4032,R4036,change from"1.05K"to"549 ohm"for NVIDA CRB.
162.(Page 27) 07/11/20 Change R4038,R4039,R4042,R4043 change from"1.05K" to "549 ohm" for NVIDA CRB.
163.(Page 26) 07/11/20 Change R4033,R4034,R4035,R4037,change from"1.82K"to"931 ohm" for NVIDA CRB.
164.(Page 27) 07/11/20 Change R4041,R4040,R4045,R4044 change from"1.82K" to "931 ohm" for NVIDA CRB.
165.(Page 26) 07/11/20 Change R4019,R4020,R4021,R4022, change from"2.49K"to"1.33K" for NVIDA CRB.
166.(Page 26) 07/11/20 Change R4019,R4020,R4021,R4022, change from"2.49K" to "1.33K" for NVIDA CRB.
167.(Page 61) 07/11/20 Change EQ Circuit Power plane .
168.(Page 61) 07/11/20 Delete U178 for MOR side require.
169.(Page 61) 07/11/20 Add filter circuit on SW_RCH and SW_LCH for MOR side require.
170.(Page 63) 07/11/20 DDelete SW_LCH signal to PGND for Mor side require.
171.(Page 57) 07/11/20 Delete SNESE_B (Cap to AGND) for Vendor suggestion
172.(Page 57) 07/11/20 Delete Cap and keep in NC for Keep floating .
173.(Page 57) 07/11/20 Add 10uF to Digital GND for Vendor suggestion.
174.(Page 57) 07/11/21 Change Net(HP_IN) to HP_5_JACK for Audio portion.
175.(Page 60) 07/11/21 Add U181 for logic accuracy.
176.(Page 32) 07/11/21 Change CN5 from FOX_HS8106E to HS8212 for MOR request.
177.(Page 48) 07/11/21 Delete Bus switch(U35) for MOR side request.
178.(Page 49) 07/11/21 Delete Controll Link bus to ICH9 side for MOR side request.
179.(Page 49) 07/11/21 Add C4784(10u) for MOR side request.
180.(Page 49) 07/11/21 delete R597,R595 for MOR side request.
181.(Page 49) 07/11/21 delete CN27 for MOR side request.
182.(Page 60) 07/11/23 Update Mute circuit for time not synchronize from vendor suggestion.
183.(Page 46) 07/11/23 Chang R816,R820,R817 from NC to populate for MOR request.

POWER Change History

184.(Page 68) 7/11/22 change PR13 from 499K to 360K for charge current set table change.
185.(Page 68) 07/11/22 change PR412 from 191K to 200K for charge voltage set .
186.(Page 68) 07/11/22 delete PD4 200K for leakage current issue .
187.(Page 68) 07/11/22 add 2nd source SPF0755H.
188.(Page 69) 07/11/22 delete PR44 because the 3V/5V pwm F change from 400k/500k to 400k/300k
189.(Page 72) 07/11/22 change PC319 from 0.22u to 0.33u
190.(Page 75) 07/11/22 change PR187 from 100 to 51K,add PR415: 200K, for setting PU19 only working in PWM mode.
191.(Page 75) 07/11/22 delete reserve schematic:PR403,PR405,PC385,PQ156,PR402
192.(Page 75) 07/11/22 change PR404 from NC to 10K,PR406 from 0 to 1k ,PC386 from NC to 1u for NV_VDD softstart
193.(Page 75) 07/11/22 change PC290 from22P to 100P for NV_VDD change smoothly
194.(Page 69) 07/11/22 change PL4 from4.7U to 3.3U ,PR61 from 162k to 300K for increasing +5v power burger and OCP setting to 11A.
195.(Page 69) 07/11/22 change PR34 from 162k to 255K for OCP setting to 8.9A.
196.(Page 70) 07/11/22 change PR58 from 8.2k to 16.2K for OCP setting to 9.1A.
197.(Page 70) 07/11/22 change PR49 from 8.2k to 12.7K for OCP setting to 7.5A.
198.(Page 71) 07/11/22 change PQ152 from fds8880 to IRF8714,PQ153 from FDS8896 to IRF8736 for increasing power efficiency.
199.(Page 75) 07/11/22 change PQ154 from SI7686DP to IR7923,PQ155 from SI7336 to IRF8736,add PQ156:IRF8736 ,change PL15 from 1.0UH to 0.56UH for NB9P power budget upgrad to 21A

EE Change History

200.(Page 41) 07/11/27 change Power plane from +5VSUS to +5VRUN
201.(Page 51) 07/11/27 change Power plane from +5VSUS to +5VALW
202.(Page 64) 07/11/27 change Power plane from +5VSUS to +5VALW
203.(Page 53) 07/11/27 change Power plane from +5VSUS to +5VRUN
204.(Page 45) 07/11/27 change iLink CONN from FOX_UV31413-WR56P-7F to FOX_UV31413-WZ03P-7F.
205.(Page 31) 07/11/27 change CRT CONN from DS11A91-WR205-4F to FOX_DS11A91-SR281-4F.
206.(Page 14) 07/11/27 change DDR2 CONN(CN1) from FOX_AS0A426-N5SN-7F to FOX_AS0A426_N2RN_7F
207.(Page 15) 07/11/27 change DDR2 CONN(CN2) from FOX_AS0A426_N4RC_4F to FOX_AS0A426_NARN_7F
208.(Page 43) 07/11/27 change ODD CONN(CN21) from FOX_LN27137-D001-9F to FOX_GB5RF120-1200-7F
209.(Page 34) 07/11/27 change TV CONN(CN10) from FOXCONN_AS0B226-S52N-7F to FOX_AS0B226_S60N_7F
210.(Page 53) 07/11/27 change FAN CONN(CN33) from FOX_HS8104E to FOX_HS8103E
211.(Page 32) 07/11/27 change FAN CONN(CN33) from FOX_HS8212Eto FOX_HS8112E
212.(Page 56) 07/11/27 delete logo LED circuit.
213.(Page 32) 07/11/27 add pull low resistor 100k to ground.
214.(Page 9) 07/11/28 Change PCIE Capactior size from 0402 to 0201
215.(Page 18) 07/11/28 Change PCIE Capactior size from 0402 to 0201
216.(Page 64) 07/11/28 delete CAPLOCK_LED#,SCRLOCK_LED#,NUMLOCK_LED# and remove to LED BOARD.
217.(Page 43) 07/11/28 Add STAT HDD Connector for ME request.
218.(Page 43) 07/11/28 Change STAT HDD Connector for ME request.
219.(Page 41) 07/11/28 Add Expander SMBus Pull H to +ECVCC.
220.(Page 41) 07/11/28 Add Net (NV_LCD_CLK/DAT) Pull H to +3VRUN
221.(Page 41) 07/11/28 Change R2523,R2522,R2518 to NC.
222.(Page 41) 07/11/28 Change SYSTEM ID Pull H to +ECVCC.
223.(Page 41) 07/11/28 Remove SYSTEMID0 for Logo LED removing.
224.(Page 59) 07/11/28 All plane chage to ALW.
225.(Page 59) 07/11/29 Change Q47,Q49 due to the BJT internal resistor and EC outpout level concern.
for the purpose to avoid system hang up when Boot and abnoraml RST.plz change Q47 & Q49 to the same components as M760.
226.(Page 75) 07/11/30 Add PC391 25V_27U reserve PC362/PC353 for decreasing Audio noise.
227.(Page 69) 07/11/30 Change PC387 to 25V_27U.
228.(Page 63) 07/12/05 Change CN123 from FOX_QT510206-2001-9F to FOX_HT1215F.
229.(Page 52) 07/12/05 Change CN122 from FOX_QT510206-2001-9F to FOX_GB5RF120-1200-7F.
230.(Page 64) 07/12/05 Change MS/SD LED control signal share one LED
231.(Page 64) 07/12/05 Change HDD/ODD LED control signal share one LED
232.(Page 64) 07/12/05 Change Wirless/BluetoothLED control signal share one LED
233.(Page 64) 07/12/05 Delete bluetooth Net BT_PIO#.
234.(Page 43) 07/12/05 Delete ODD Net ODD_DP#.
235.(Page 53) 07/12/06 Change thermal sensior U59 to G7801P81U.
236.(Page 49) 07/12/06 Change WLA Conn CN31 to FOX_AS0B226_S40N_7F.
237.(Page 50) 07/12/07 Change EXPRESSConn CN29 to FOX_1CX421S1-MM.
238.(Page 57) 07/12/07 Change Audio Conn JSPK1 to FOX_HS7108E.
239.(Page 62) 07/12/07 Change Audio Conn JSPK3 to FOX_HS7102E.
240.(Page 50) 07/12/10 Change EXPRESSConn CN28 to FOX_1CH411SC-MM.
241.(Page 33) 07/12/10 Change HDMIConn CN60 to FOX_QJ5119L-NT03-4F.
242.(Page 72) 07/12/10 add ODD POWER plan.
243.(Page 47) 07/12/12 add R5238 for MOR side request.
244.(Page 47) 07/12/12 Change Net CF_PWR to CF_IN# for timing issue.
245.(Page 52) 07/12/14 Reverse Power Plan for MOR side request.
246.(Page 67) 07/12/21 ADD PL17,PL18 8A bead for BATT
247.(Page 59) 07/12/21 Change Q46 to PDTC144EU for MOR side require.
248.(Page 59) 07/12/21 change from +3VALW to +3VRUN.
249.(Page 60) 07/12/21 delete R1848 for MOR side require.
250.(Page 60) 07/12/21 delete R1849 for MOR side require.
251.(Page 43) 07/12/21 Add R5208 ,R5207 for SSD power .
252.(Page 60) 07/12/21 delete R5156 for MOR side require.
253.(Page 60) 07/12/21 Change R5143 to 5.6k for MOR side require.
254.(Page 60) 07/12/21 Change R274 to 5.6k for MOR side require.
255.(Page 60) 07/12/21 Change R268 to 5.6k for MOR side require.
256.(Page 60) 07/12/21 Change R5154 to 5.6k for MOR side require.
257.(Page 60) 07/12/21 change C4820,C4822,C4825,C4827 from 0.047u to 0.068u/50V.
258.(Page 60) 07/12/21 delete +5VRUN ,and change R1871 from NC to 0 ohm.
259.(Page 61) 07/12/21 change R252 from 10k ohm to 1k ohm.
260.(Page 61) 07/12/21 change C236 from 0.1u/16V to 0.068u/16V.
261.(Page 61) 07/12/21 change C1682 from 0.22u/10V to 0.068u/16V.
262.(Page 61) 07/12/21 change C1683 from 0.22u/10V to 0.1u/16V.
263.(Page 61) 07/12/21 change change C367 from 0.068u/16V to 0.047u/16V.
264.(Page 61) 07/12/21 change R2162 from 39k ohm to 33k ohm.
265.(Page 61) 07/12/21 change C1684 from 0.22u/10V to 0.1u/16V.
266.(Page 61) 07/12/21 change R2164 from 3.3k ohm to 1k ohm.
267.(Page 61) 07/12/21 change L4068,L4067 from PBY201209T to MPZ1608D101B(TDK).
268.(Page 61) 07/12/21 change U138,U139 from NJM4565V to RC4580IPWR.
269.(Page 63) 07/12/23 Add fuse F16
270.(Page 74) 07/12/24 Change PC391 from 27u_25V to 22u_25V ,add PC362 MLCC10U_25V for decreasing input ESR
271.(Page 69) 07/12/24 Change PR49 from 12.7K to 12.4K ,add PR58 from 16.2k to 15.4k for cutting in 2nd source in DVT
272.(Page 61) 07/12/25 add R5239,C4864 for mor side require.
273.(Page 59) 07/12/25 add Mute_AMP# circuit modification for mor side require.
274.(Page 23) 07/12/25 Change L66,L73,L74 to TB100505U121
275.(Page 67) 07/12/25 Delete common choke to 4*BEAD PL19,PL20,PL21,PL22 because height limit
276.(Page 40) 07/12/25 Change Connection from GND_TR to normal Ground.
277.(Page 40) 07/12/25 Delet C574 and R486
278.(Page 59) 07/12/25 Change R5240 to 220k
279.(Page 74) 08/01/04 FOR NB9P: PR403 to 20k,PR402:23.2K,PR272=61.9K
280.(Page 74) 08/01/04 FOR NB8M: PR403 to 20k,PR402:29.4K,PR272=160K
281.(Page 74) 08/01/04 FOR NB8M/9P: ADD PQ78,PQ169,PR422:52.3K_0402_1%,PR420:10K_0402,PR421:1K_0402
282.(Page 70) 08/01/04 CHANGE PR384 to 5.1k for OCP margin
283.(Page 70) 08/01/05 CHANGE PU3 from G909-330T1U to AT5208 for decreasing inrushing current
284.(Page 68) 08/01/05 ADD PC392 :0.1U_25V
285.(Page 67) 08/01/05 ADD delete (reserve PD4)
286.(Page 74) 08/01/05 For NB9M MV voltage modified,change PR402 to 29.4k_1%_0402,PR272_1%_0402 to 39.2k_1%_0402 ,PR420/PR422/PQ165/PR
287.(Page 63) 08/01/08 Please remove these 2 fuses.F25 & U183/184 are enough for USB VBus current limiting.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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EVT TO DVT

Page 20 .Add power source for FB_DLLAVDD1 & FB_PLLAVDD1

Page 61. change R2164 from 1K to 2.7K for MOR request

Page 57. change SPK AMP Gain setting to 18dB for MOR request

Page 48,49. change BT LED control signal source from BT module directly

Page 32,41. Use SW1 one pin to disable Fan monitor function

Page 54. F11,F12,F18,F19 change from 350mA to 250mA

Page 59. Change Q4019 pin 2 from +3VALW to +5VALW

Page 37. Change EC_OUT1 pin to GPIO12

Page 41. Add R572,R573,R574 pull low

Page 61. R259 NC

Page 41. Add C465,C466 47pF pull low

Page 24. Add R586,R590 for MOR request.

Page 3. Add R5248 in series for MCH_CLK_REQ#.

Page 47. Add F27 Poly switch for CF card protection.

Page 37. Add D9 diode for RUNTIME_SCI# leakage.

Page 41. Add D17,D24 for EC_RCIN#,EC_A20GATE leakage.

Page 23. Add R1779 for PWRCNTL_0 pull high.

Page 37. Add R455 for Finger print Detect.

Page 60,63. Remove C4830,R740,R743,R745 for MOR request.

Page 33. Add R340,Q122,R2373,Q123 for HDMI drop issue.

Page 3. Add C820 ,C821 for Robson CLK to match rising and falling time spec.

Page 52. Add F13 for CIR FFC protection.

Page 40. Add R75 ,R5249,C138 for 8057 used

Page 49. Remove C18,add R617 for MOR request.

Page 41. Add C913 for EMI.

Page 42. Add C962 for EMI.

Page 53. Add C967 for EMI.

Page 71. Add C968 for EMI.

Page 68. Add C990 for EMI.

Page 74. Add C991 for EMI.

Page 32. Add C992 for EMI.

Page 56. Add C368 for TV .

Page 60. change C4820,C4822,C4825,C4827 to 0.047U
R5146,R5151 to 1.8k R151,R5152 t o5.6k

Page 61. change R244,R249 to15k R2160 to 18k, PR523,PR524 to 15k, C367 to 0.022U, R2164 to 1.8k.

Page 31. Add C467,C468,C469 for EMI.

Page 46. Mount C453 for EMI.

Page 41. Add R575 for CF always power on.

Page 37. Remove R455,R486 for FP_DET#,change by BIOS detect.

Page 6. add C88,C89 for MOR request.

Page 72. add R5250 for MOR request.

Page 34. add C370,C369 for EMI

Page 41. add C371 for EMI

Page 29. add C993 for EMI

Page 26. add C994 for EMI

Page 41. change charge LED to high active.

Page 57. add C995 for EMI.

Page 33. add C997 for EMI.

Page 62. add C90 for EMI.

Page 41. add C91 for EMI.

Page 54. add C238 for EMI.

Page 47. add U17 ,R91,R92 for CF solution.

Page 73. change PR181 from 34k to 31.6k for changing power limit from 118W to 114W

DVT TO PVT

Page 64(LED Status) .charging LED logic change
Page 75(HOLE & BOSS) .Add AMI label on M/BD
Page 31(CRT) .change VSYNC and HSYNC resistor and capacitor for SI test fail.
Page 54(Daughter Board Conn) .change PWR and Suspend LED logic same as M760 for more brightness.
Page 47(PCI CF) .separate CF controller power and card power for hot-plug issue.

Page .change NV9P,9M ,HDCP KEY HH P/N

Page 17(VGA (PCI-E) 1/9) .L4049 change vendor

Page 41(EC+KBC (WPCE775L) .change RP24,RP25 to +3VALW
Page 67(DCIN&Charger) .Delete PJ1 and PJ2
Page 68(SYS Power (+3_3V/+5V) .Delete PJ3 and PJ4
Page 69(SYS Power(+1_5V/+1_05V) .Delete PJ7 and PJ8
Page 70(DDR2 Power(+1_8V/+0_9V) .Delete PJ10 and PJ13
Page 71(CPU_Vcore---ISL6266A) .Delete PJ12
Page 74(VGA Power(0.9V/+1_05V) .Delete PJ15,PJ16,PJ17

Page 43(SATA HDD/CD-ROM) .change CN126 to KOTL
Page 3(CLOCK GEN (SL28648BLC) .U123 change HH P/N
Page 18(VGA (PCI-E BUS)Strap 2/9) .add samsung VRAM strap pin
Page 55(OIDE/CAM) .change OIDE connector to LNC PVT 0605.pdf

Page 60(AUDIO(EQ) .C4820,C4822,C4825,C4827; Change from 0.047µ/50V to 0.015µ/25V,R5146,R5151; Change from 1.8k to 3.3k
Page 61(AVD20 (Filter Circuit) .R2164 change to 1k,R2165 change to 4.7k
Page 72(Others power plan) .R5250 mount,PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC
Page 51(USB 2.0) .add USB connector TID No.

Page 55(OIDE/CAM) .change camera connector for easy to unplug.

Page 43(SATA HDD/CD-ROM) .change ODD connector to 14 pin
Page 75(HOLE & BOSS) .change H48 to PTH type
Page 55(OIDE/CAM) .reserve 3.3V for camera module.
Page 47(PCI CF) .change discharge circuit for CF card power,add 4.7U for CF card power ,change CF card LED power source.
Page 45(PCI (ILINK) .change Y5 capacitor for accuracy.
Page 71(CPU_Vcore---ISL6266A) .PR429 NC
Page 67(DCIN&Charger) .PCN2 add two pillars to fix position for our prodution line smoothly. PVT 0613.pdf

Page 1(index) .change HH P/N

Page 75(HOLE & BOSS) .add two PAD for ME request
Page 68(SYS Power (+3_3V/+5V) .PU2 Pin9 ,pin10 connect from +5VALW_PWM to +5VALW PVT 0617.pdf

Page 41(EC+KBC (WPCE775L) .mount R516,C592 for EMI
Page 24(VGA (INTER DISPLAY) 8/9) .mount C828 for EMI
Page 41(EC+KBC (WPCE775L) .add C998 for EMI
Page 48(bluetooth) .add C999 for EMI
Page 40(Marvell GLAN(88E8055) .add C1000 for EMI
Page 72(Others power plan) .add C1001 for EMI
Page 41(EC+KBC (WPCE775L) .add C1002 for EMI
Page 56(AUDIO(CODEC & POWER) .add C1003 for EMI
Page 54(Daughter Board Conn) .add C1004,C1005 for EMI
Page 54(Daughter Board Conn) .add L31,L32 for EMI

Page 23(VGA (XTAL/GPIO) 7/9) . reserve D10,R5251,R5252,C93,R1780 for HDMI Audio issue.
Page 56(AUDIO(CODEC & POWER) . reserve R749,C12 for HDMI Audio issue.

Page 63(Audio BOARD conn) . mount R741,change R744 to C807 0.1u for EMI

Page 56(AUDIO(CODEC & POWER) .change R5222 to C809 0.1uf for EMI.

Page 42(AUDIO(Flash ROM/SPI) .CN16 change from 1200 to 1203 for EOL issue.

Page 65(Robson 1.7 Connector) .remove CN24,C712,C713 for Robson no used.
Page 65(AUDIO (SUBWOOFER AMP).change R5228 from 68k to 6.8k for MOR request.
Page 75(HOLE & BOSS) .Add PAD 3 for ME request.
Page 75(LVDS) .reserve C472 for invertor power PVT 0625.pdf

Page 31(CRT) .change L25,L26,L27 to 120R bead,C467,C468,C469 to NC.

Page 62(AUDIO (SUBWOOFER AMP) .change R5226,R5227 to 0.5% resistors

Page 54(Daughter Board Conn) .add U11 for finger print protection. PVT 0627.pdf

Page 71(CPU_Vcore---ISL6266A) .PC389 NC,PC299,PC289 mount for solid cap issue.
Page 68(SYS Power (+3_3V/+5V) .PC387 NC for solid cap issue
Page 74(VGA Power(0.9V/+1_05V) .PC391 NC,PC353 mount for solid cap issue.
Page 32(LVDS) .Add C472 for solid cap issue.
Page 45(PCI (ILINK) .change R540~R543 to 47 ohm for MS overshoot and undershoot issue.
Page 41(EC+KBC (WPCE775L) .R516,C592 NC for signal quality.
Page 3(CLOCK GEN (SL28648BLC) .change R767 to 47 ohm for EMI issue. PVT 0629.pdf

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