


Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	06/10/2	36	EXPRESS/OIDE/TP	1.0	06/10/2
02	Block Diagram	1.0	06/10/2	37	PCI (PCI BUS)	1.0	06/10/2
03	Yonah(HOST BUS) 1/2	1.0	06/10/2	38	PCI (ILINK)	1.0	06/10/2
04	Yonah(HOST BUS) 2/3	1.0	06/10/2	39	PCI (MS)	1.0	06/10/2
05	Yonah(Power/Grnd) 3/3	1.0	06/10/2	40	PCI (PCMCIA)	1.0	06/10/2
06	CALISTOGA (HOST) 1/7	1.0	06/10/2	41	USB2.0	1.0	06/10/2
07	CALISTOG (DMI) 2/7	1.0	06/10/2	42	CRT	1.0	06/10/2
08	CALIST (GRAPHIC) 3/7	1.0	06/10/2	43	DB CONNS & LED	1.0	06/10/2
09	CALISTOGA (DDR2) 4/7	1.0	06/10/2	44	Power Design Diagram	1.0	06/10/2
10	CALIST (POWER, VCC) 5/7	1.0	06/10/2	45	DC IN/Charger (MAX1909)	1.0	06/10/2
11	CALIST (VCC CORE) 6/7	1.0	06/10/2	46	SYSPWR(+3VALW/+5VALW)	1.0	06/10/2
12	CALIST (VSS) 7/7	1.0	06/10/2	47	SYSPWR(+1 5VRUN/+1 05VRUN)	1.0	06/10/2
13	DDR1(SO-DIMM 0) 1/3	1.0	06/10/2	48	VHICORE(ISL6262)	1.0	06/10/2
14	DDR1(SO-DIMM 1) 2/3	1.0	06/10/2	49	Others power plan	1.0	06/10/2
15	DDR1(Termination) 3/3	1.0	06/10/2	50	OVP protection	1.0	06/10/2
16	PCI-E(S/STRAP) 1/7	1.0	06/10/2	51	VGAPWR(VGACORE(10)	1.0	06/10/2
17	PCI-E(S/STRAP) 2/7	1.0	06/10/2	52	DDR2PWR(+3V BUS/+0.9V)	1.0	06/10/2
18	PCI-E(S/STRAP) 3/7	1.0	06/10/2	53	CDCKA	1.0	06/10/2
19	PCI-E(S/STRAP) 4/7	1.0	06/10/2	54	ROSE	1.0	06/10/2
20	PCI-E(S/STRAP) 5/7	1.0	06/10/2	55	POWER SQUELCH	1.0	06/10/2
21	PCI-E(S/STRAP) 6/7	1.0	06/10/2	56	HP	1.0	06/10/2
22	PCI-E(S/STRAP) 7/7	1.0	06/10/2				
23	VRAN(DDR3)	1.0	06/10/2				
24	VRAM(POWERBYPASS)	1.0	06/10/2				
25	LVDS / S VIDEO	1.0	06/10/2				
26	ICH7-M(PCI/USB) 1/5	1.0	06/10/2				
27	ICH7-M(LPC, IDE, SATA) 2/5	1.0	06/10/2				
28	ICH7-M(GPIO) 3/5	1.0	06/10/2				
29	ICH7-M(POWER) 4/5	1.0	06/10/2				
30	ICH7-M(GND) 5/5	1.0	06/10/2				
31	SATA HDD/CD-ROM	1.0	06/10/2				
32	EC+KBC	1.0	06/10/2				
33	Flash ROM/XBUS	1.0	06/10/2				
34	Mini Card/BT	1.0	06/10/2				
35	FAN/HW THERMAL PROTECT	1.0	06/10/2				

PCB P/N: 1P-0069700-8011 - Unimicro
1P-0069201-8011 - NANYA

Project Code & Schematics Subject: MS60 Main Board

P. Leader		Check by	Design by
10/3		10/3	10/3
<div style="text-align: center;">  <p>CONFIDENTIAL</p> </div>			
FOXCONN HION HAI PRECISION IND. CO., LTD. CPBG - R&D Division			
Index Page			
Size	Document Number		Rev
Custn	MS60-1-01 (MBX-159)		1.0
Date	Monday, October 02, 2006		Sheet 1 of 58

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	06/10/2	36	EXPRESS/OIDE/TP	1.0	06/10/2
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09	CALISTOGA (DDRII) 4/7	1.0	06/10/2	44	Power Design Diagram	1.0	06/10/2
10	CALIST (POWER,VCC) 5/7	1.0	06/10/2	45	DC_IN/Charger (MAX1909)	1.0	06/10/2
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12	CALIST (VSS) 7/7	1.0	06/10/2	47	SYSPWR(+1_5VRUN/+1_05VRUN)	1.0	06/10/2
13	DDRII(SO-DIMM_0) 1/3	1.0	06/10/2	48	VHCORE(ISL6262)	1.0	06/10/2
14	DDRII(SO-DIMM_1) 2/3	1.0	06/10/2	49	Others power plan	1.0	06/10/2
15	DDRII(Termination) 3/3	1.0	06/10/2	50	OVP protection	1.0	06/10/2
16	VGA(PCI-E/STRAP) 1/7	1.0	06/10/2	51	VGAPWR(VGACORE&IO)	1.0	06/10/2
17	VGA(PCI-E/STRAP) 2/7	1.0	06/10/2	52	DDR2PWR(+1_8V_SUS/+0_9VRUN)	1.0	06/10/2
18	VGA(GDDR3) 3/7	1.0	06/10/2	53	CLOCK GEN	1.0	06/10/2
19	VGA(TMDS/LVDS) 4/7	1.0	06/10/2	54	HOLE	1.0	06/10/2
20	VGA(SS) 5/7	1.0	06/10/2	55	POWER SEQUENCE	1.0	06/10/2
21	VGA(MULTIUSE) 6/7	1.0	06/10/2	56	History	1.0	06/10/2
22	VGA(TV/CRT) 7/7	1.0	06/10/2				
23	VRAM(GDDR3)	1.0	06/10/2				
24	VRAM(POWERBYPASS)	1.0	06/10/2				
25	LVDS / S_VIDEO	1.0	06/10/2				
26	ICH7-M(PCI/USB) 1/5	1.0	06/10/2				
27	ICH7-M(LPC,IDE,SATA)2/5	1.0	06/10/2				
28	ICH7-M(GPIO) 3/5	1.0	06/10/2				
29	ICH7-M(POWER) 4/5	1.0	06/10/2				
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31	SATA HDD/CD-ROM	1.0	06/10/2				
32	EC+KBC	1.0	06/10/2				
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34	Mini_Card/BT	1.0	06/10/2				
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PCB P/N:

1P-0069700-8011 - Unimicro

1P-0069201-8011 - NANYA

Project Code & Schematics Subject: MS60 Main Board



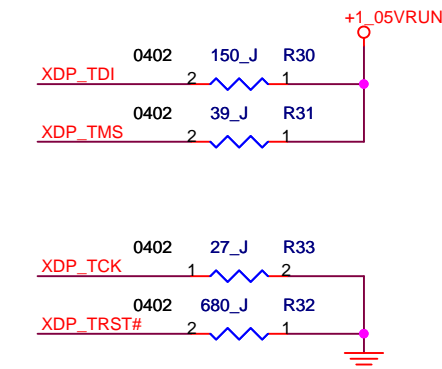
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Title **Index Page**

Size	Document Number	Rev
Custom	MS60-1-01 (MBX-159)	1.0

Date: Monday, October 02, 2006 Sheet 1 of 56



Layout note:
no stub on
H_STPCLK#

```

ICH7M's GPIO12:  VIL---> -0.5V ~ 0.8V
                  VIH--->  2.0V ~ 3.3+0.5V
YONAH'S PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
                  VIH--->  0.7*VCCP ~ VCCP+0.1

```

28,32,35,48 OVT_EC# OVT_EC# 1

Q6
PDTCT144EU

Q7
2N7002EPT

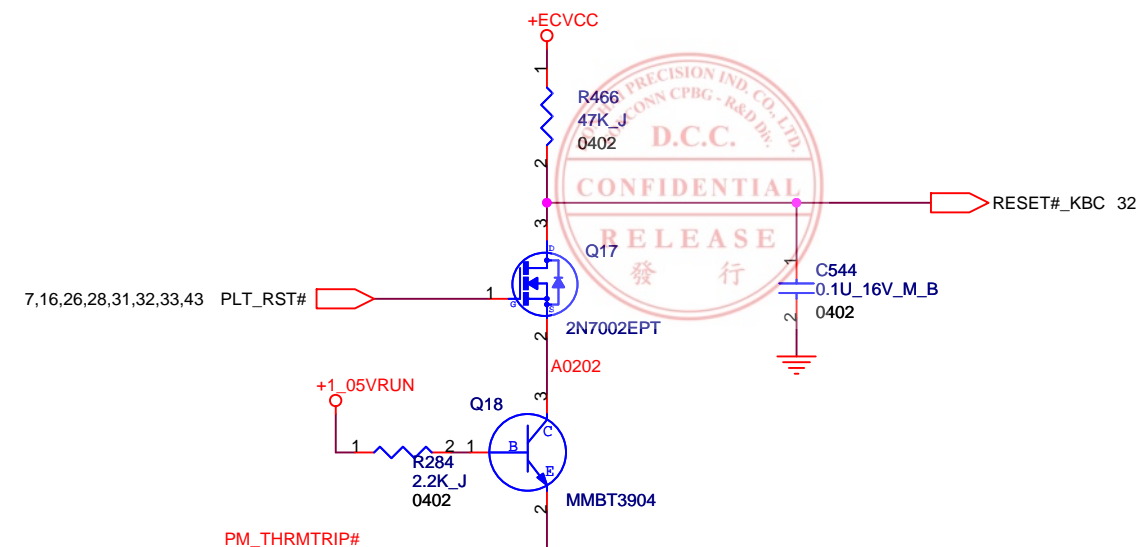
R14
56_F
0402

R16
2.2K_J
0402

PROCHOT#
If PROCHOT# CPU, IMVP resistor

+3VVRUN

+1_05VRUN



Place close to CPU

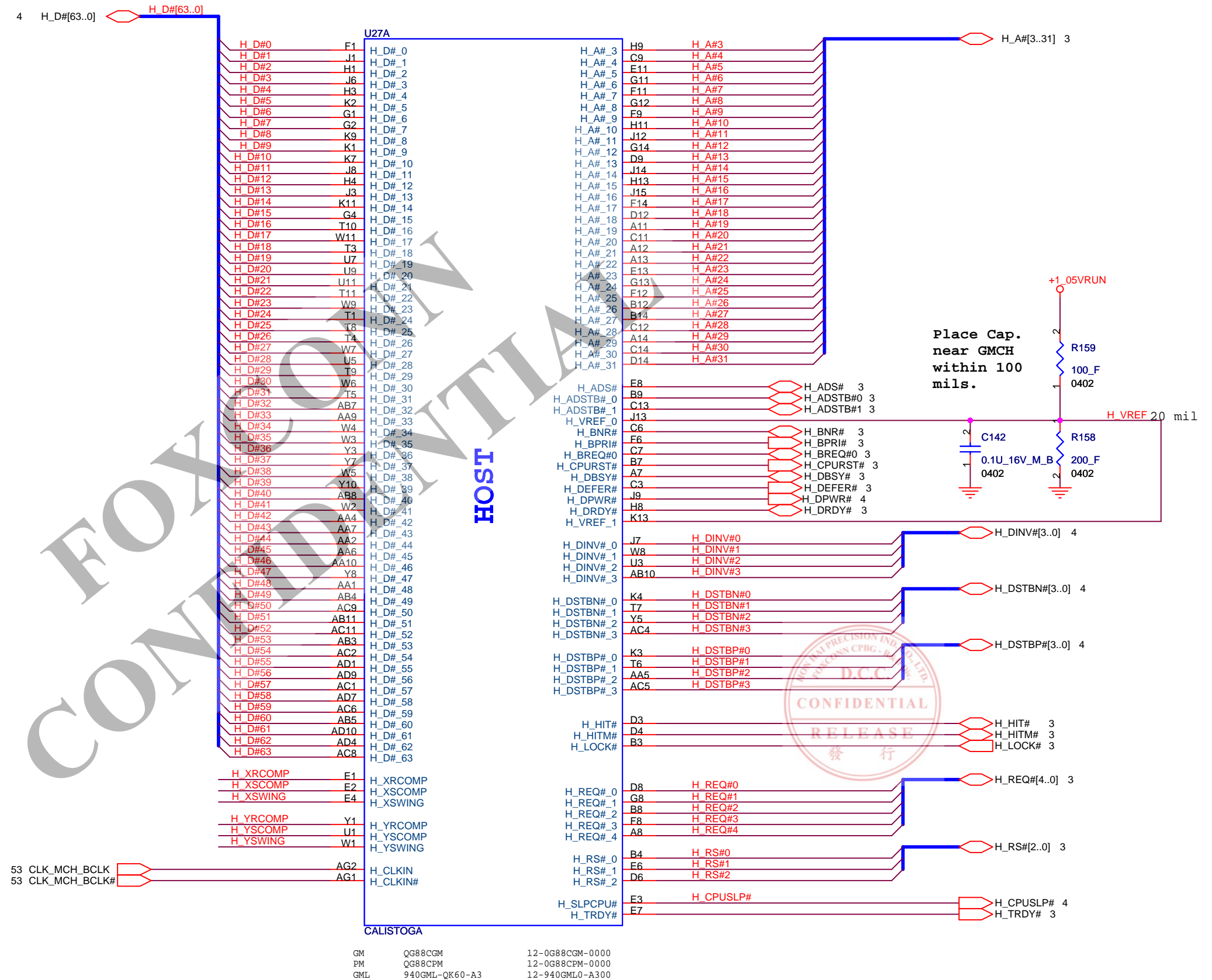
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

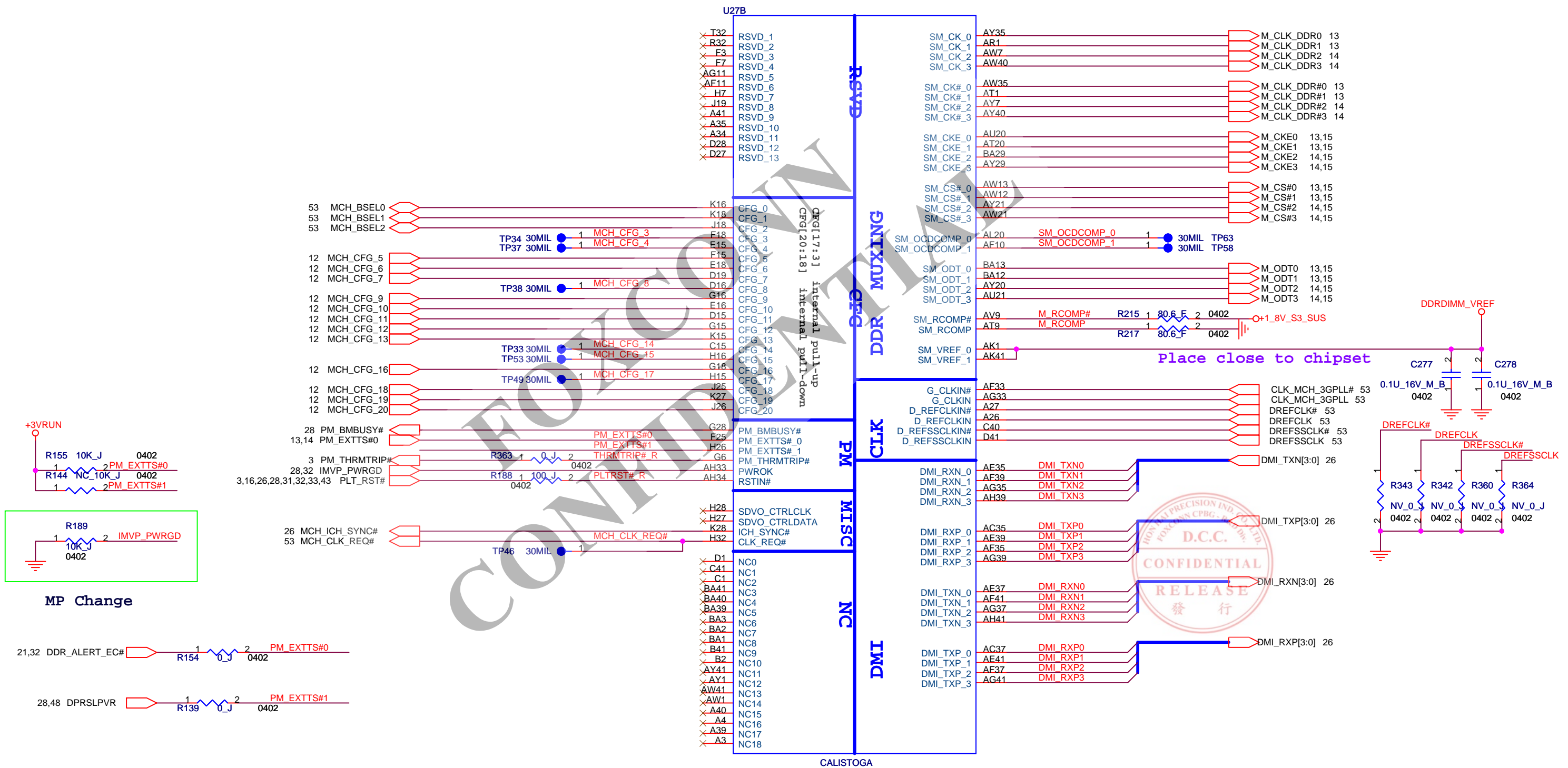
FSB Frequency Table:

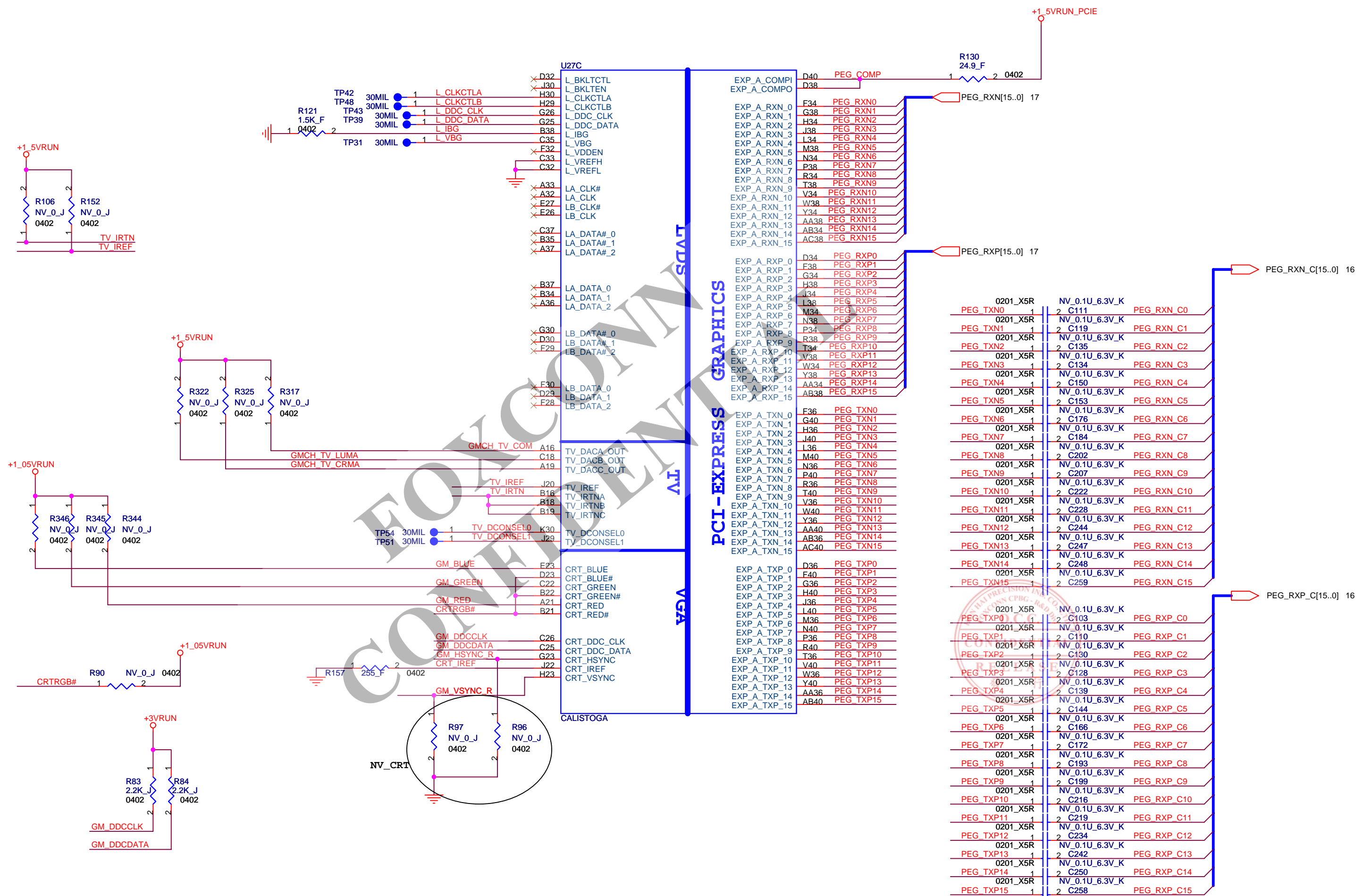
BSEL[2:0]	Freq.(MHz)
LLL	Reserve
L L H	133
L H L	Reserve
L H H	166

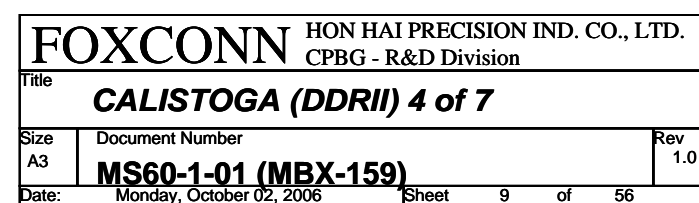
Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

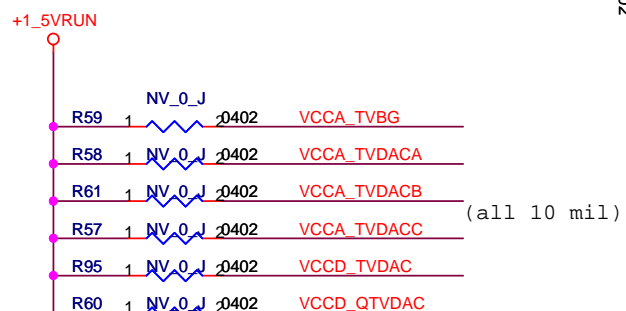
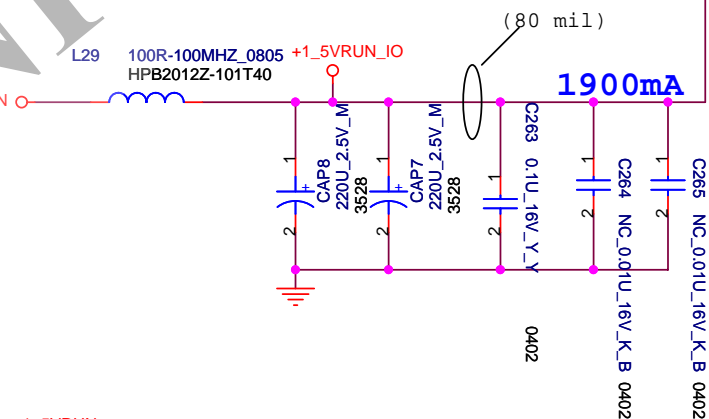
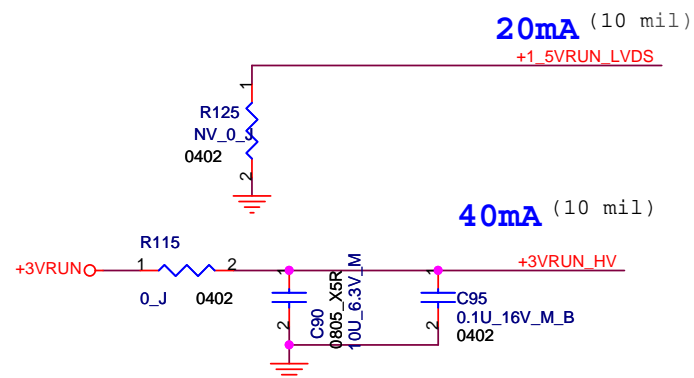
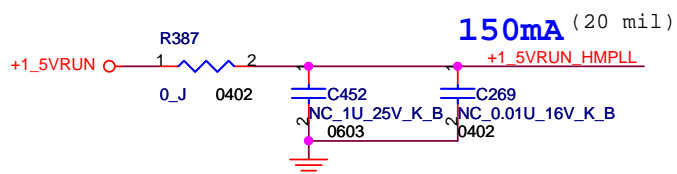
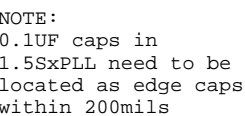




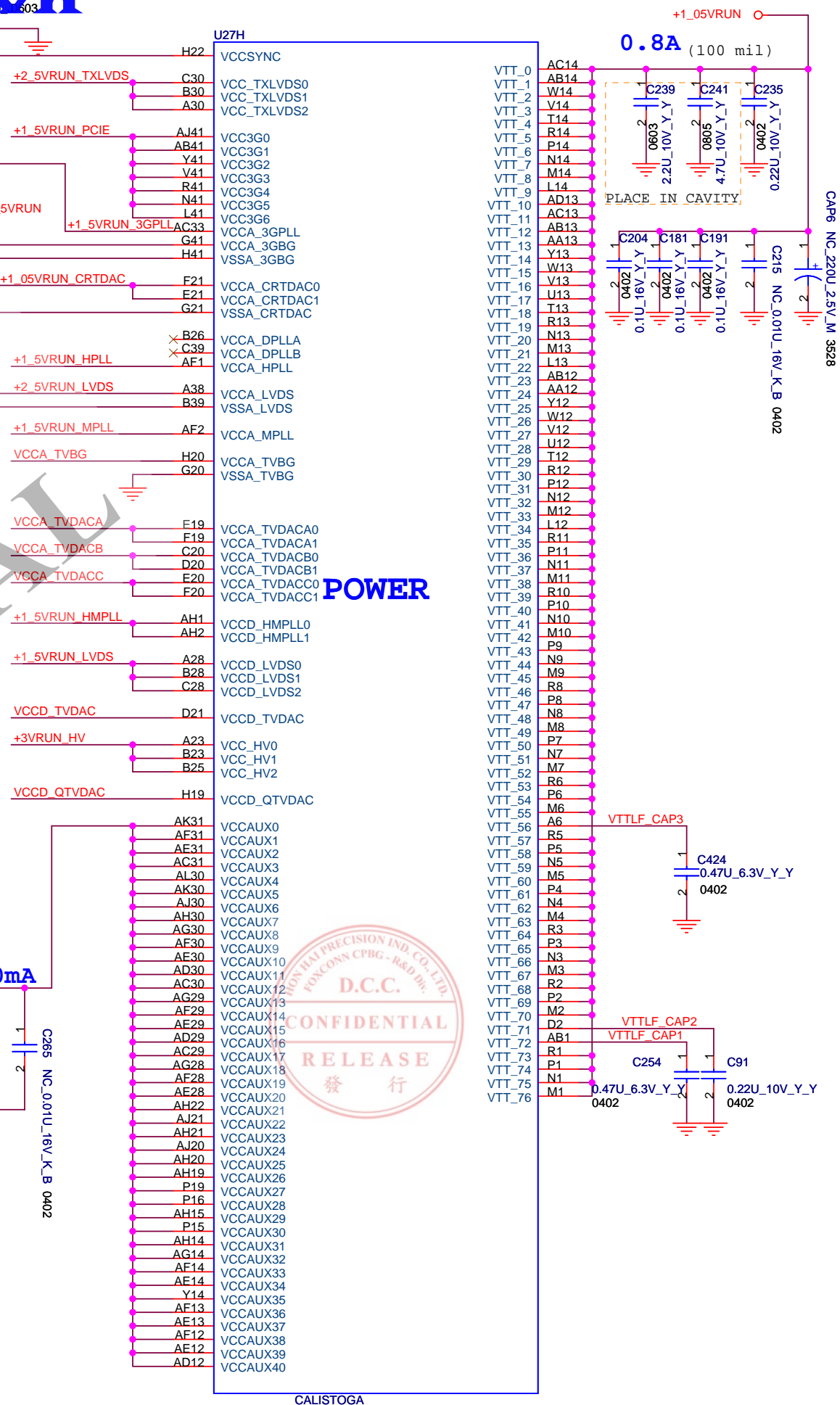








POWER



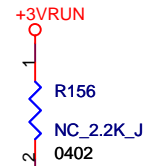
CALISTOGA



7 MCH_CFG_5 ◀ 1 30MIL TP45

MCH_CFG_5	Low = DMIx2 High = DMIx4
-----------	-----------------------------

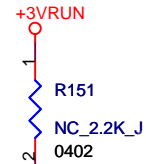
MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------



7 MCH_CFG_6 ◀ 1 30MIL TP40

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	---

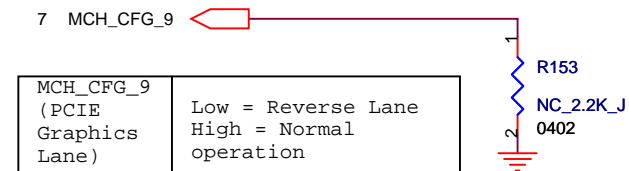
MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
-----------------------------------	--



7 MCH_CFG_7 ◀ 1 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
--------------------------	---

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
---	---



For layout convenience

7 MCH_CFG_10 ◀ 1 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
-------------------------------------	-----------------------------------

7 MCH_CFG_20 ◀ 1 30MIL TP52

7 MCH_CFG_11 ◀

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga
-----------------------------------	-----------------------------------

7 MCH_CFG_12 ◀ 1 30MIL TP47
7 MCH_CFG_13 ◀ 1 30MIL TP55

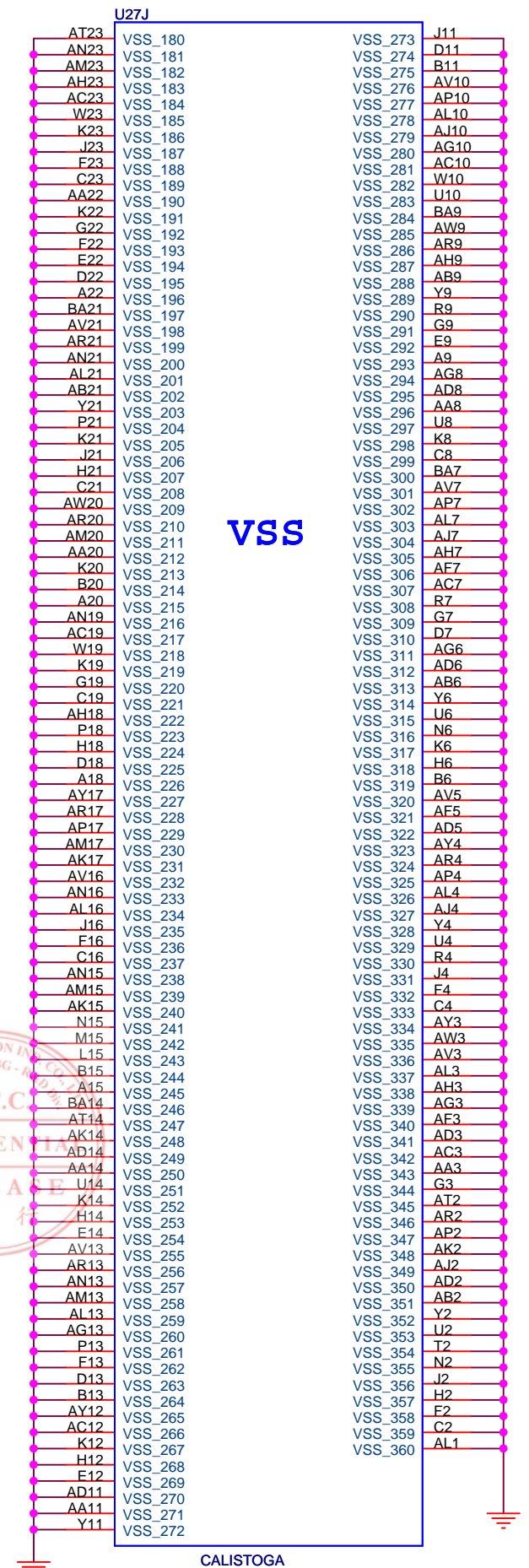
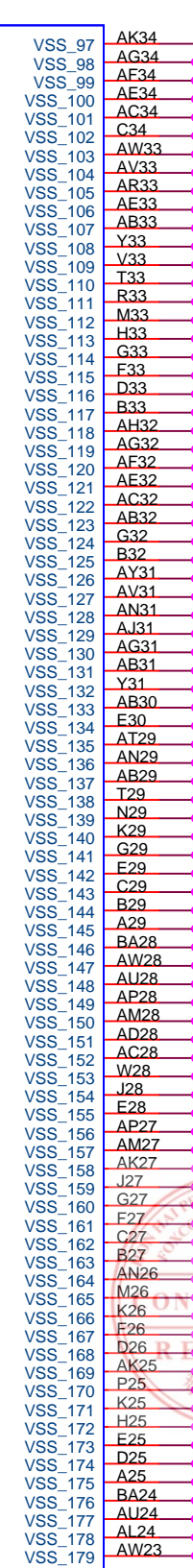
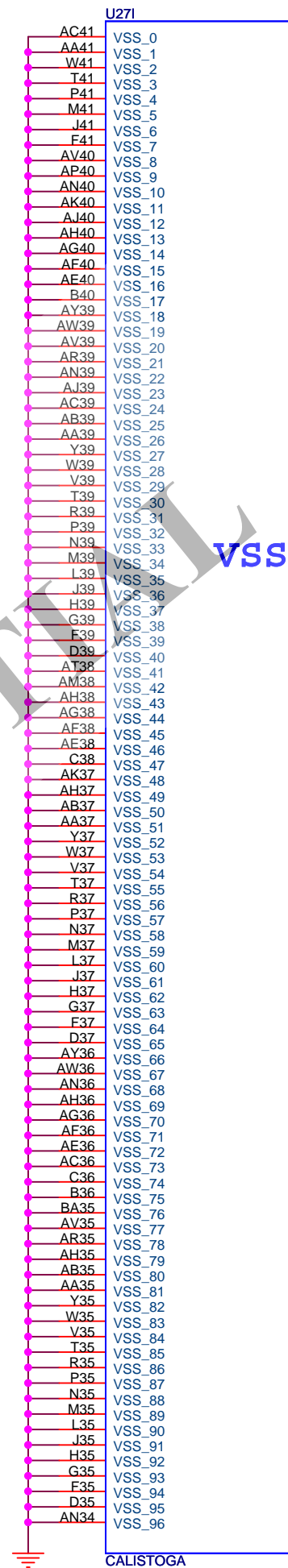
MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---

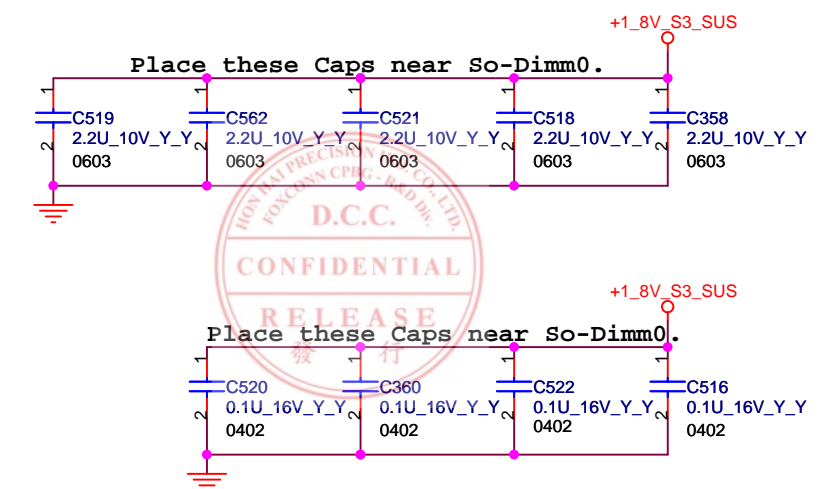
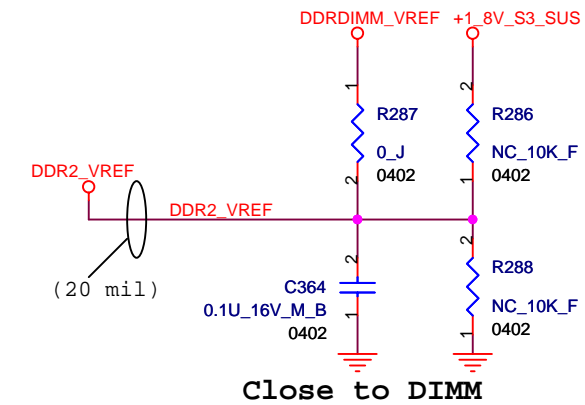
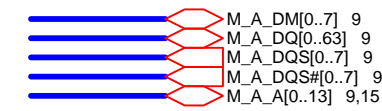
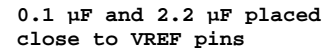
7 MCH_CFG_16 ◀ 1 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
---------------------------------	---

Layout Noe:
Location of all MCH_CFG strap resistors
needs to be close to trace to minimize stub

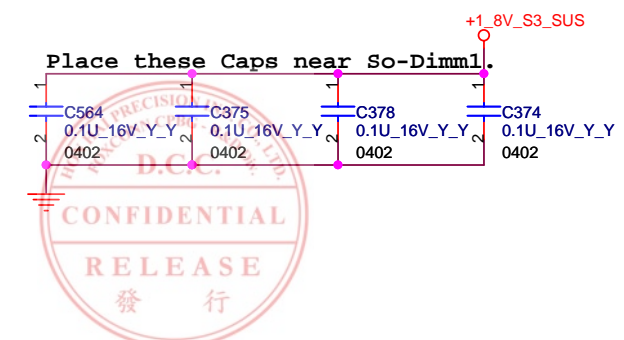
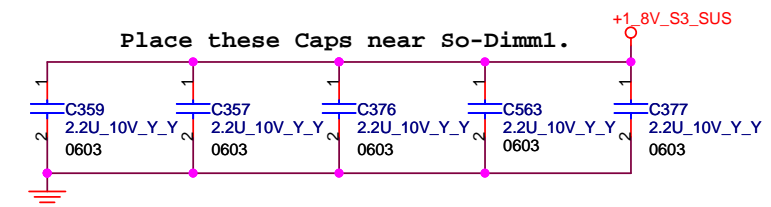
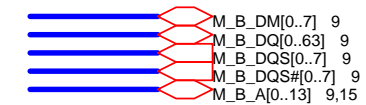
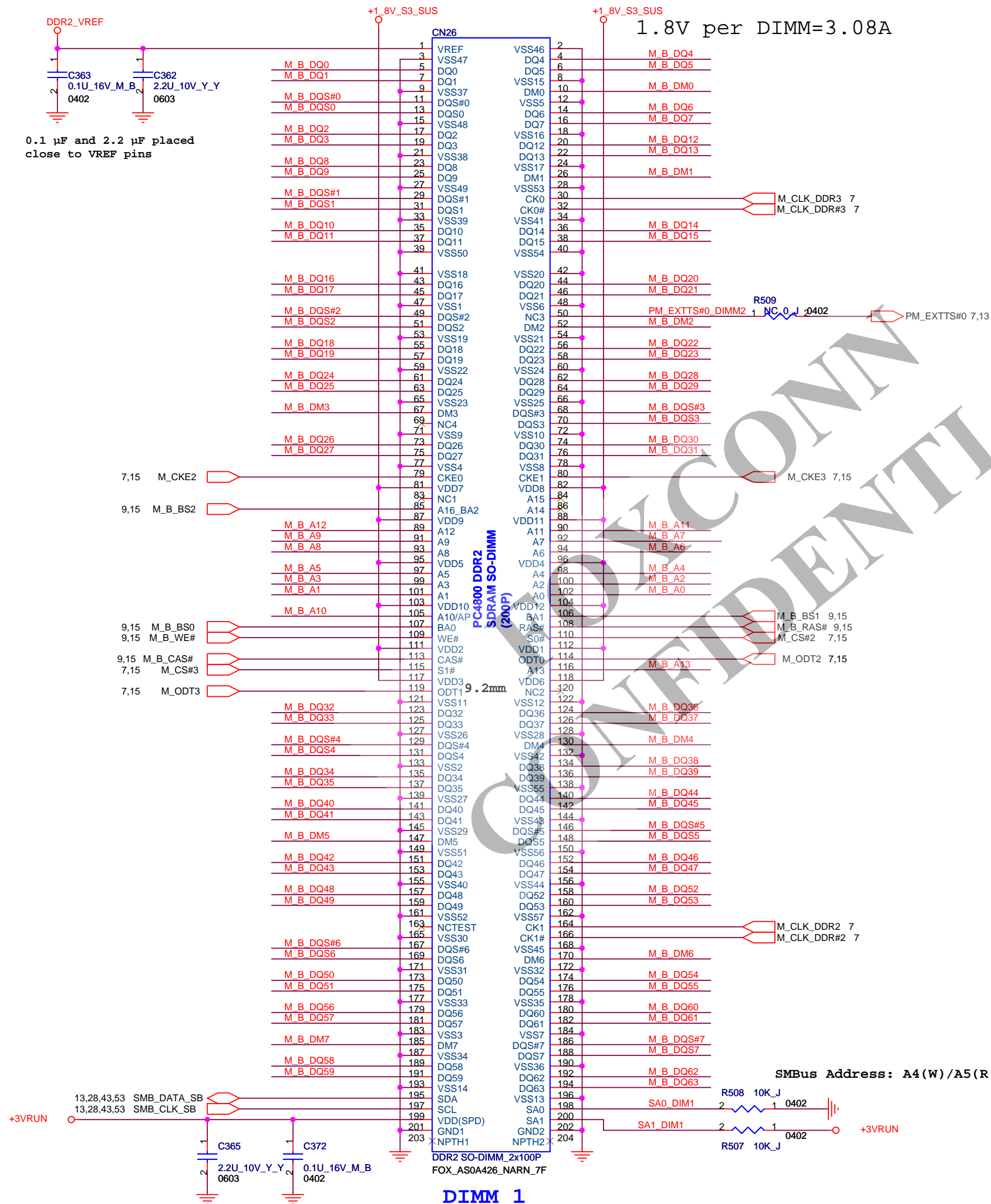
Check CALISTOGA version , after A2 version , if
sysfec can't boot up then NC the pull low R

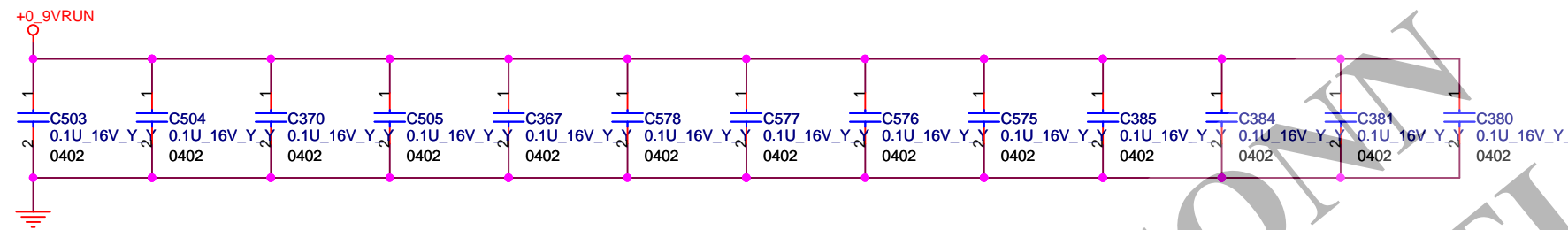




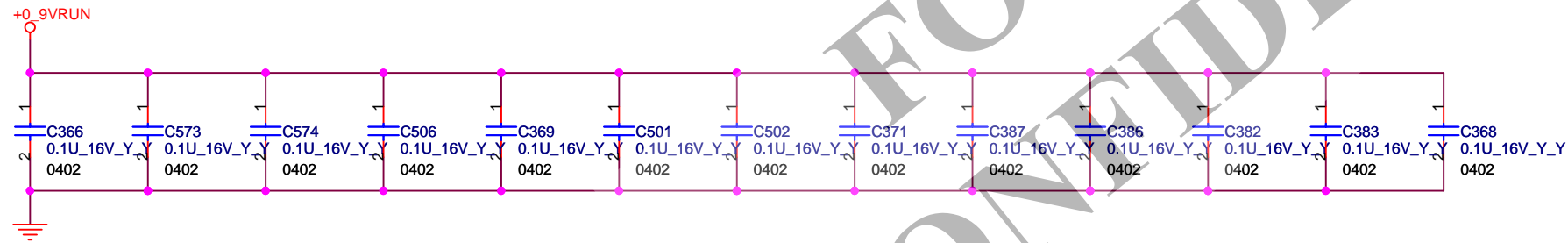
SMBus Address: A0(W)/A1(R)

DIMM_0





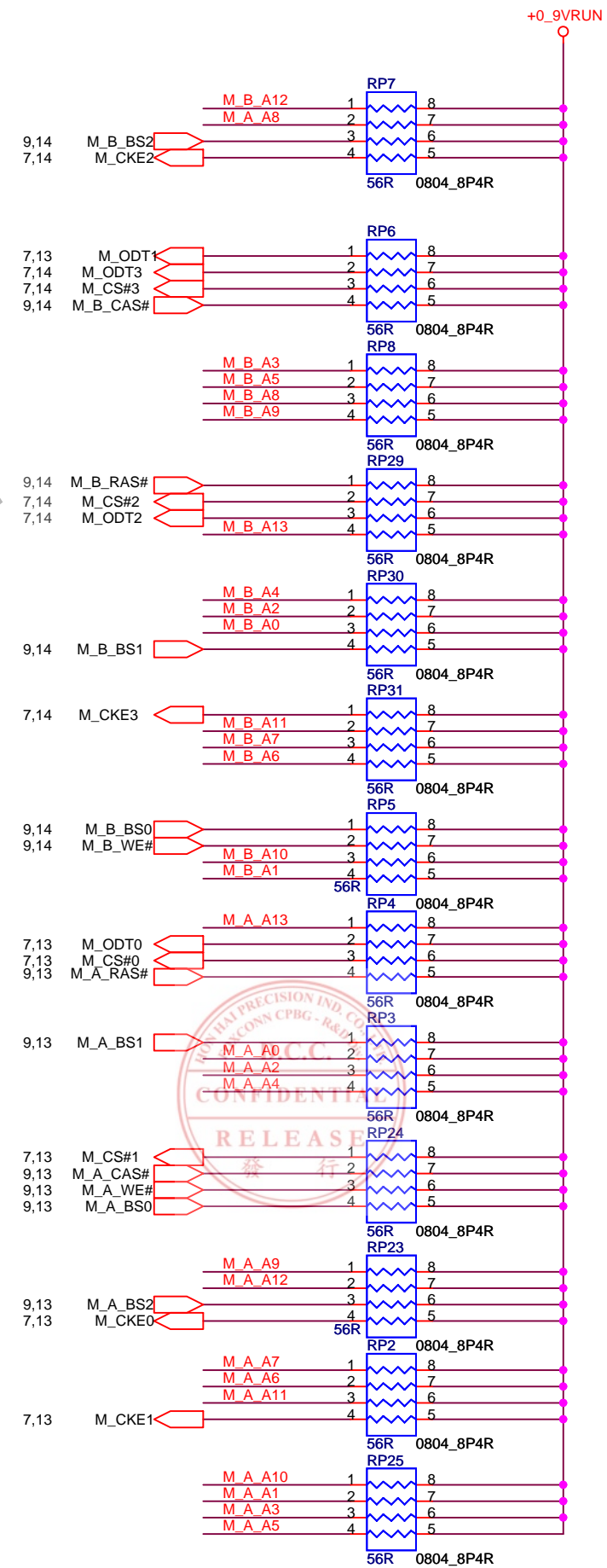
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN

9,13 M_A_A[0..13]

9,14 M_B_A[0..13]





TVMODE		
NTSC (01)		
MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

Strap for GDDR3-136ball		
0001	16Mx32	Infineon
0010	16Mx32	Hynix
0011	16Mx32	Samsung
0101	8Mx32	Infineon
0110	8Mx32	Hynix
0111	8Mx32	Samsung

SUBVENDOR	
0	(USE SYSTEM BIOS)
1	(USE EXTERNAL ROM)

PANEL ID CONFIG
NC

MIOAD0 is used to set
the PCI Express PLL
termination enable.
DEFAULT "0"

3GIO_PADCFG[2:0]
001 for G7X

G72M/G73M
PCI_DEVID[3:0]="1000"->8

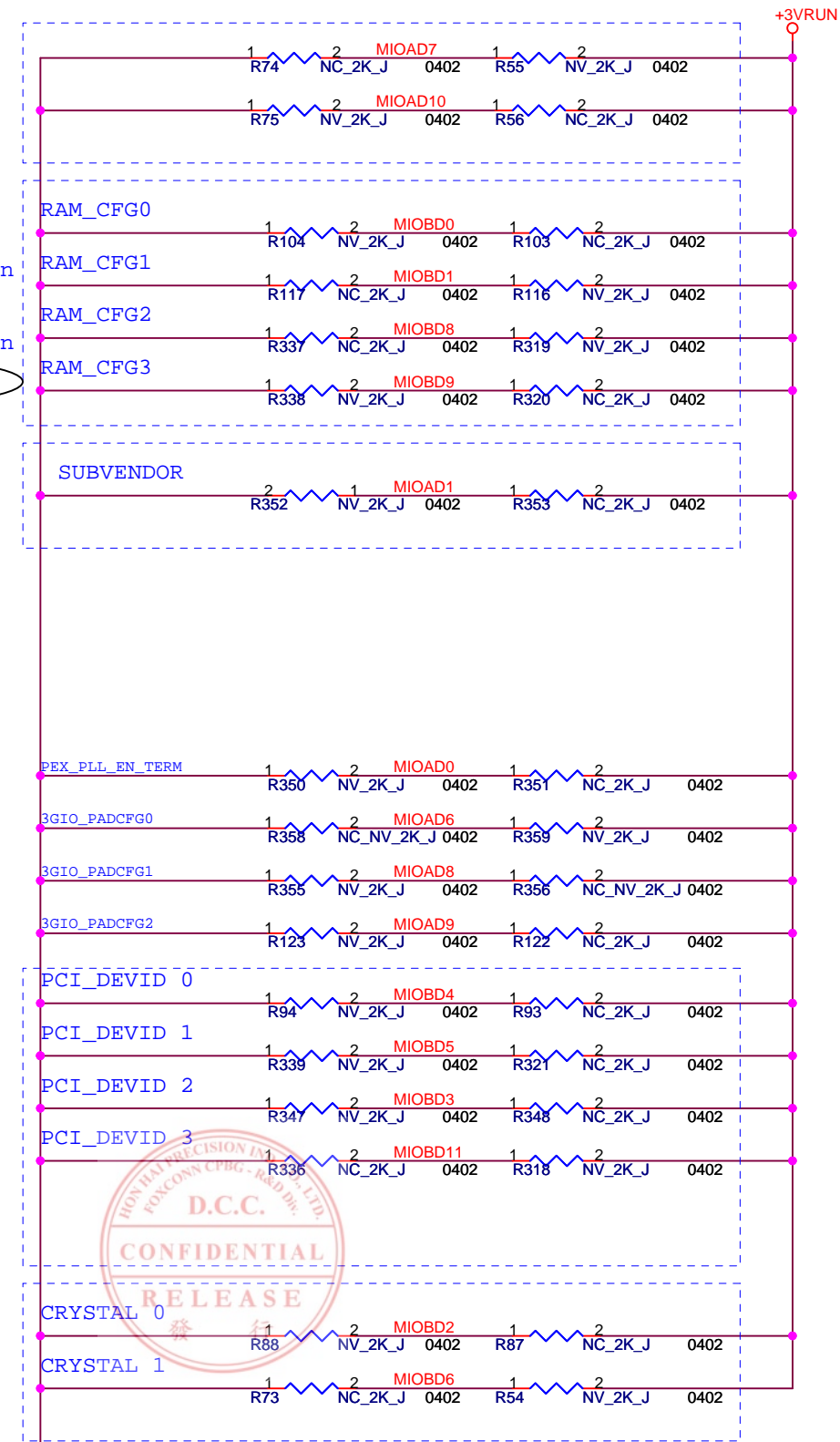
CRYSTAL		
10 (27M Hz)		
MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

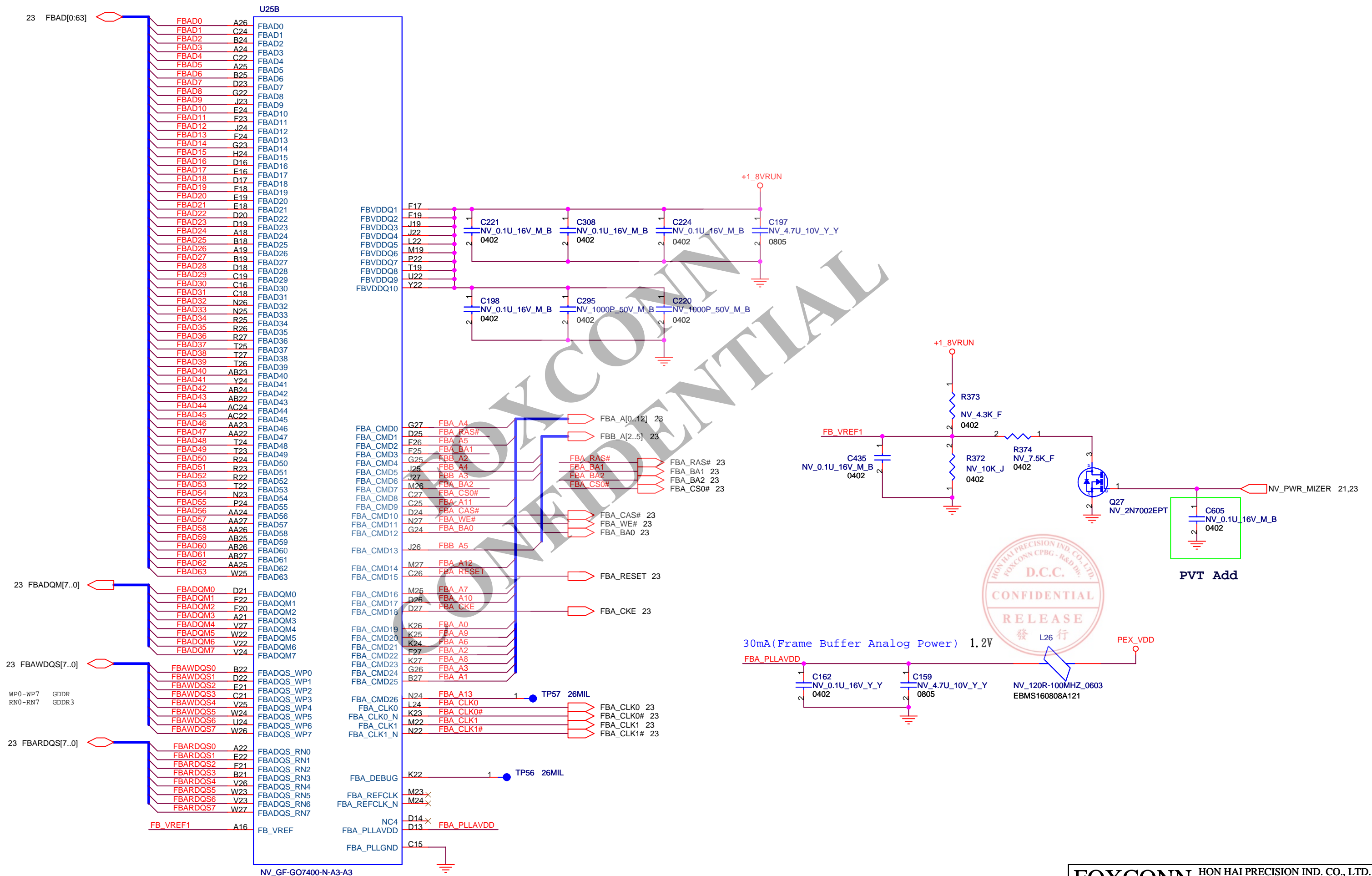
ROM_TYPE NC

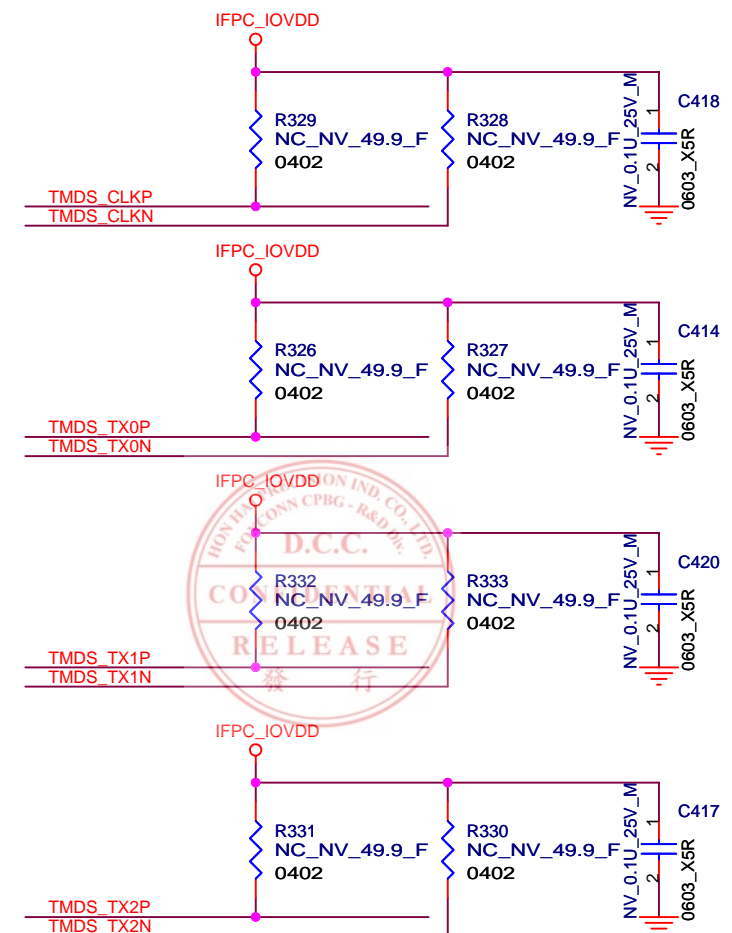
00	PARALLEL
01	SERIAL_AT25F
10	SERIAL_SST45VF
11	LPC

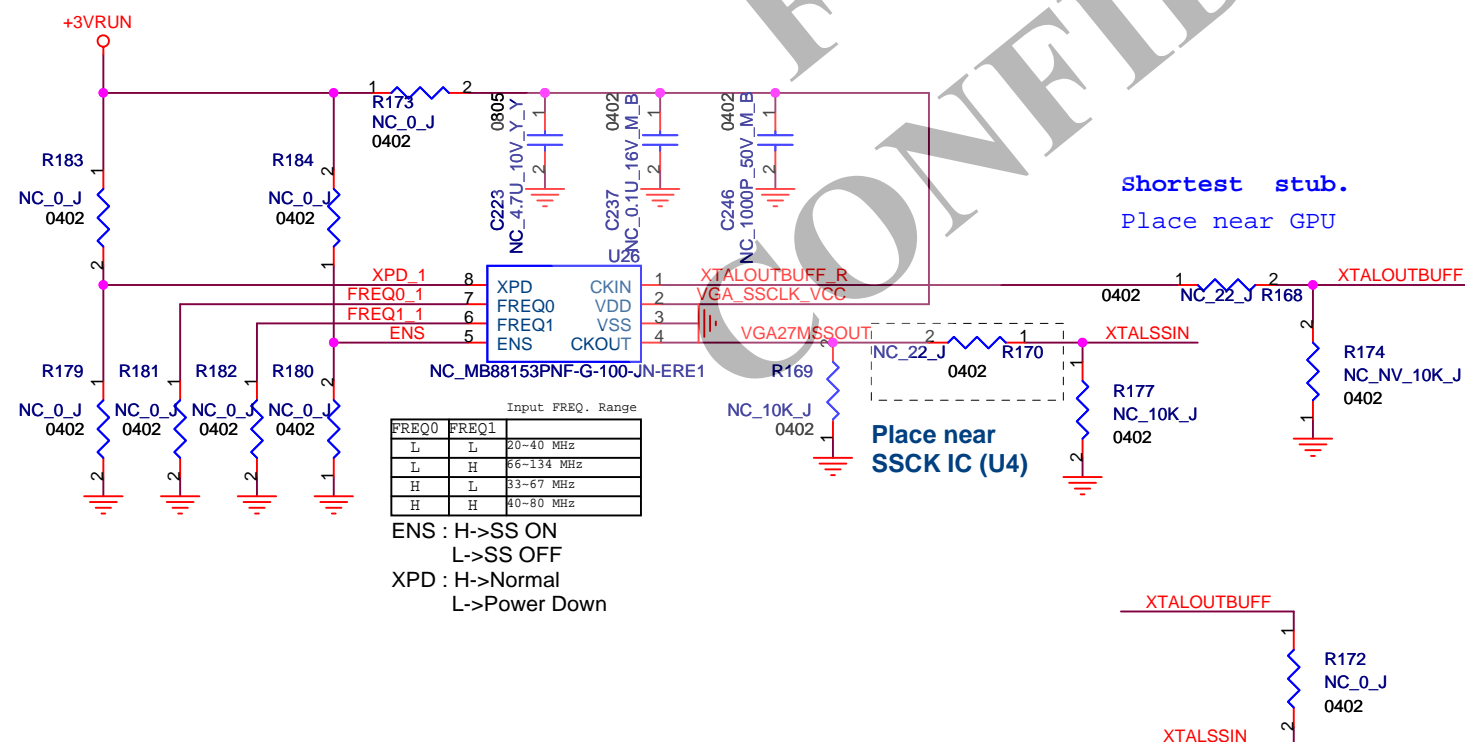
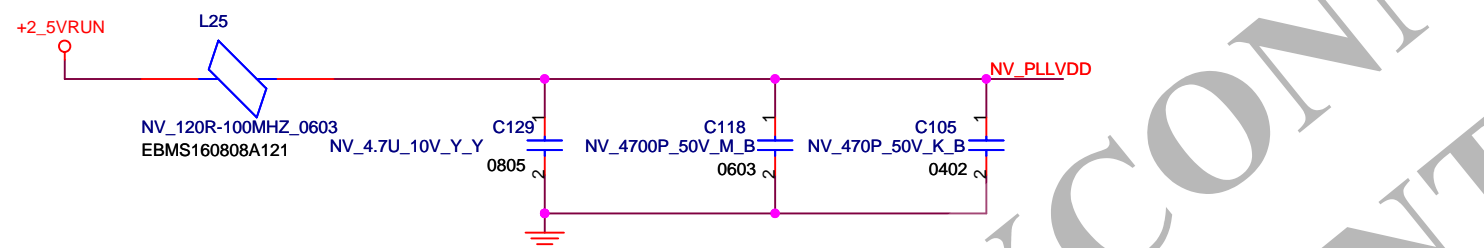
MIOAD0	MIOAD0	16
MIOAD1	MIOAD1	16
MIOAD6	MIOAD6	16
MIOAD7	MIOAD7	16
MIOAD8	MIOAD8	16
MIOAD9	MIOAD9	16
MIOAD10	MIOAD10	16

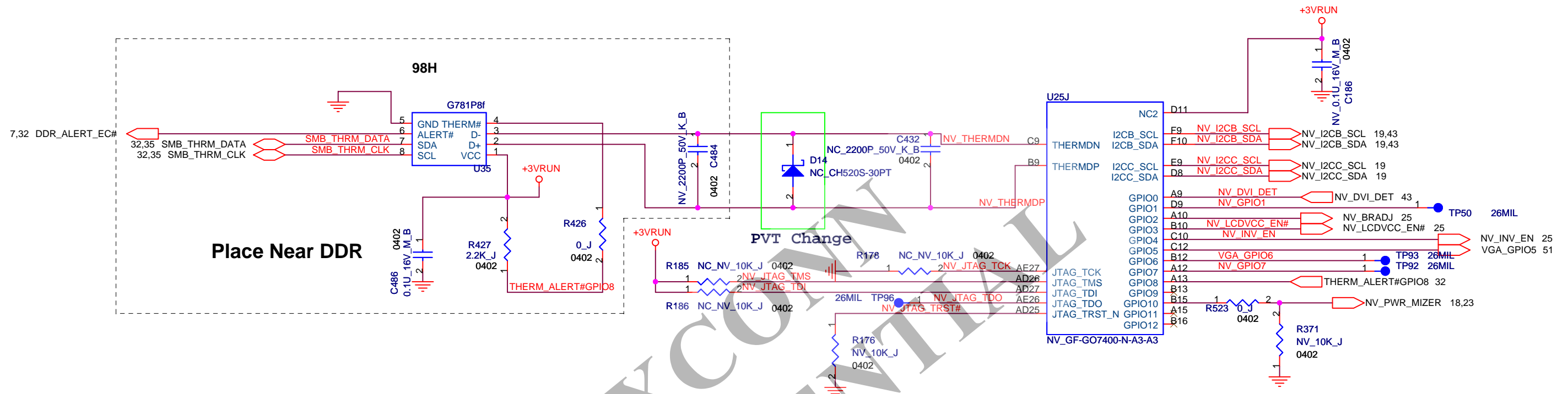
MIOBD0	MIOBD0	16
MIOBD1	MIOBD1	16
MIOBD2	MIOBD2	16
MIOBD3	MIOBD3	16
MIOBD4	MIOBD4	16
MIOBD5	MIOBD5	16
MIOBD6	MIOBD6	16
MIOBD8	MIOBD8	16
MIOBD9	MIOBD9	16
MIOBD11	MIOBD11	16











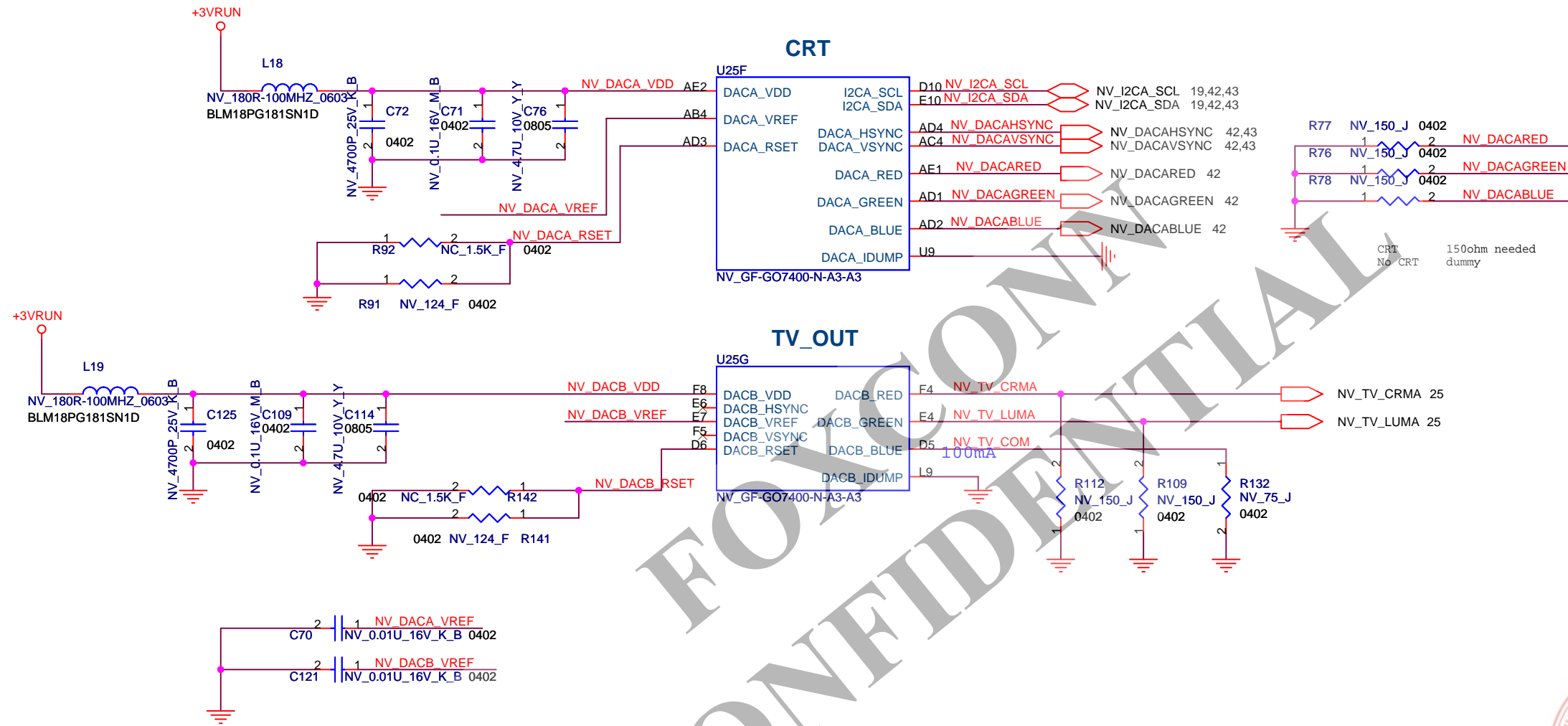
Check Spec.

	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPIO6	O	Yes	
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Power Mizer control signal
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

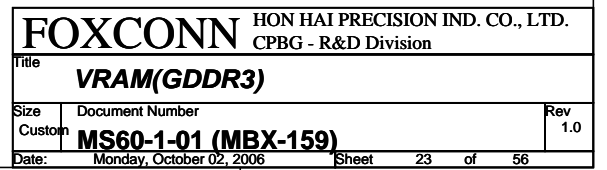
PWR_MIZER LEVEL	H	L
Vref	50% FBVDDQ	70% FBVDDQ

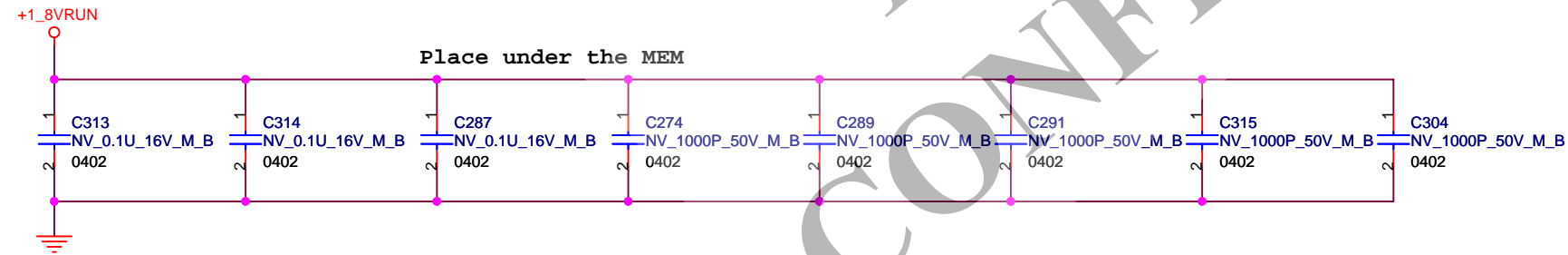
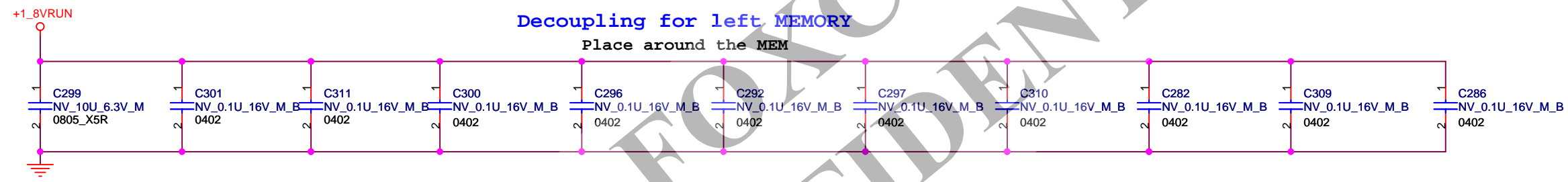
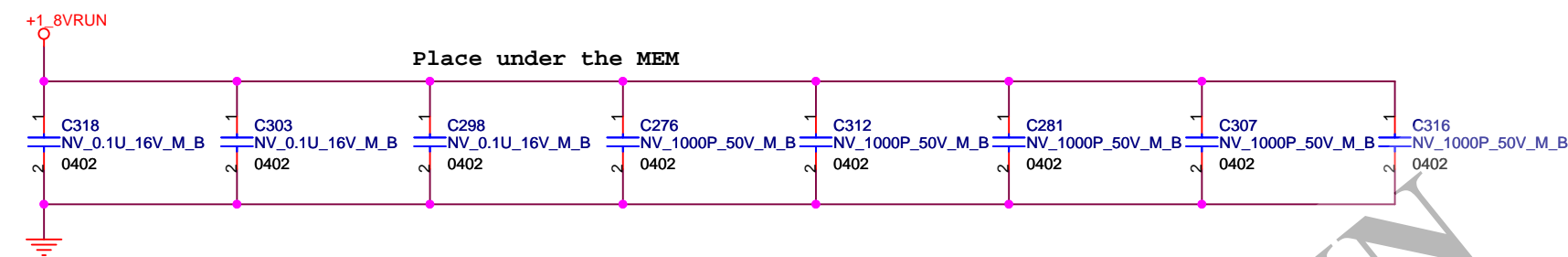
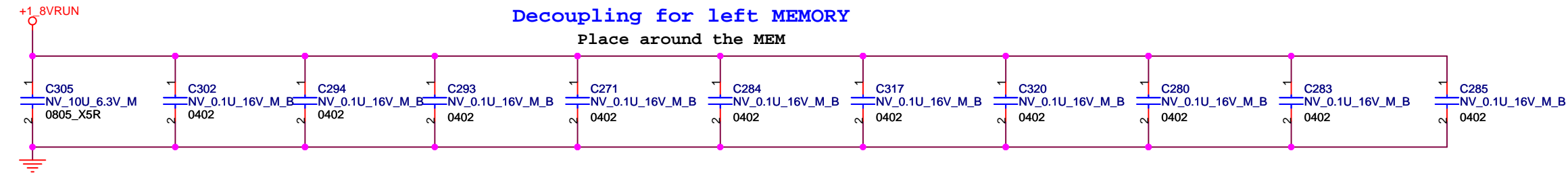


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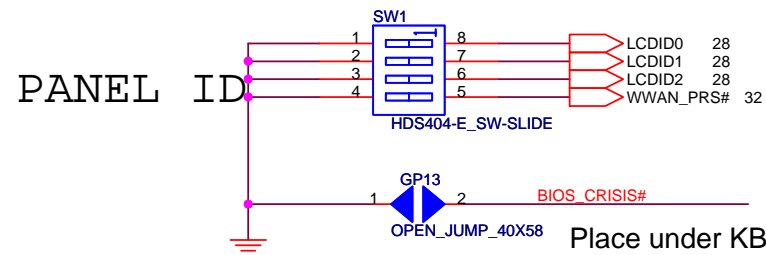
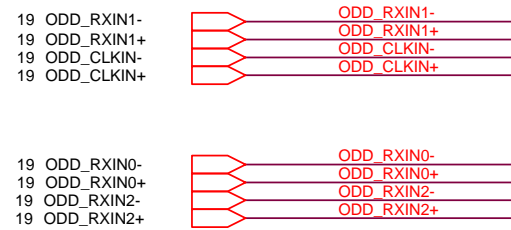


DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCCLK			SCL
	VGA-DDCDATA			SDA
DACC	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACC-RED	C		PR	
DACC-GREEN	Y		Y	
DACC-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCCLK			SCL
	DVI-DDCDATA			SDA



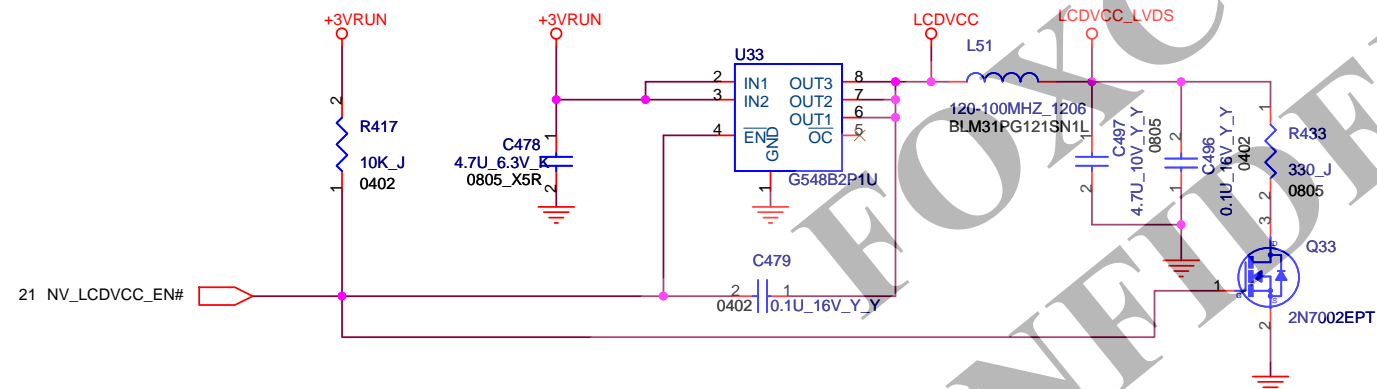


LVDS

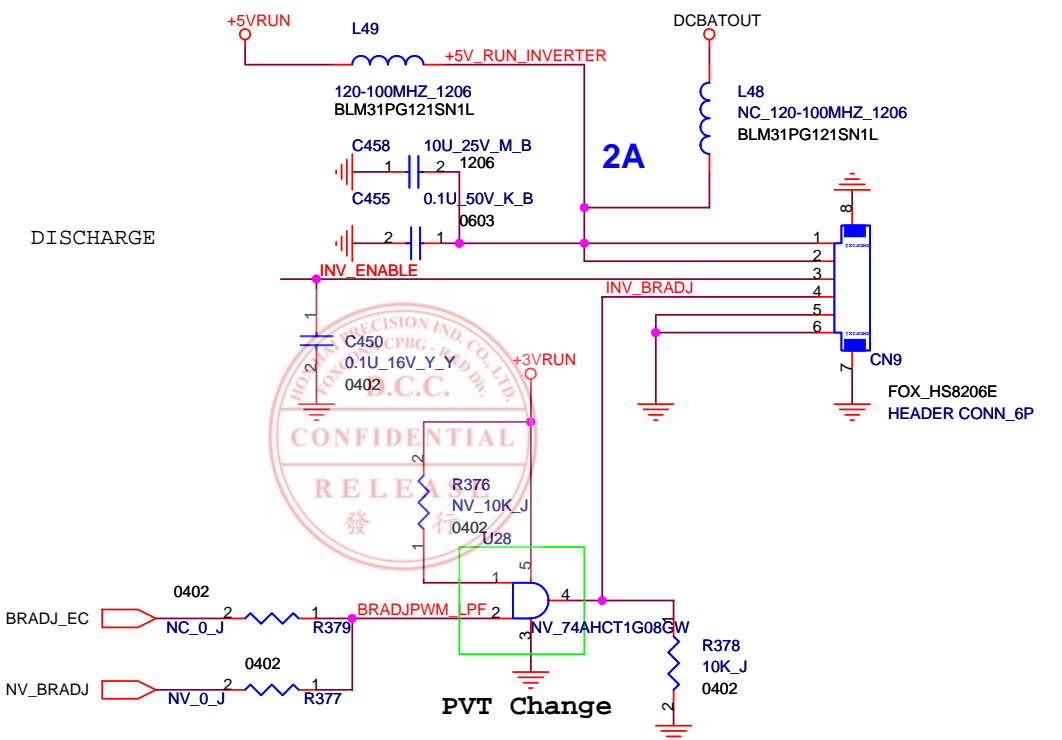
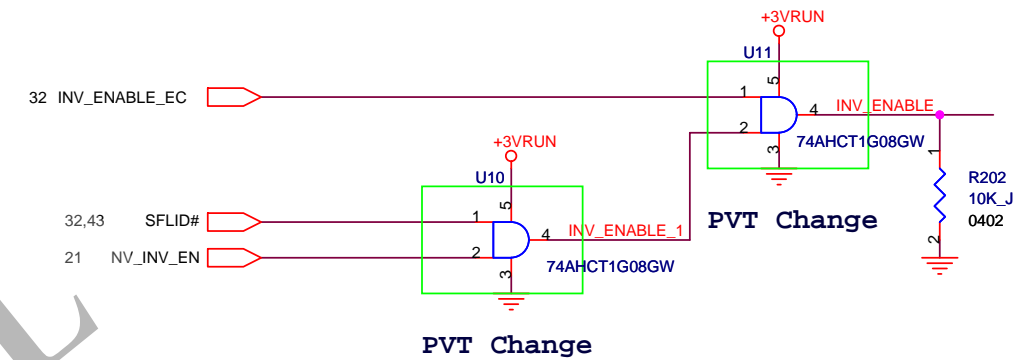
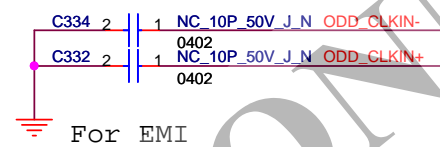


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

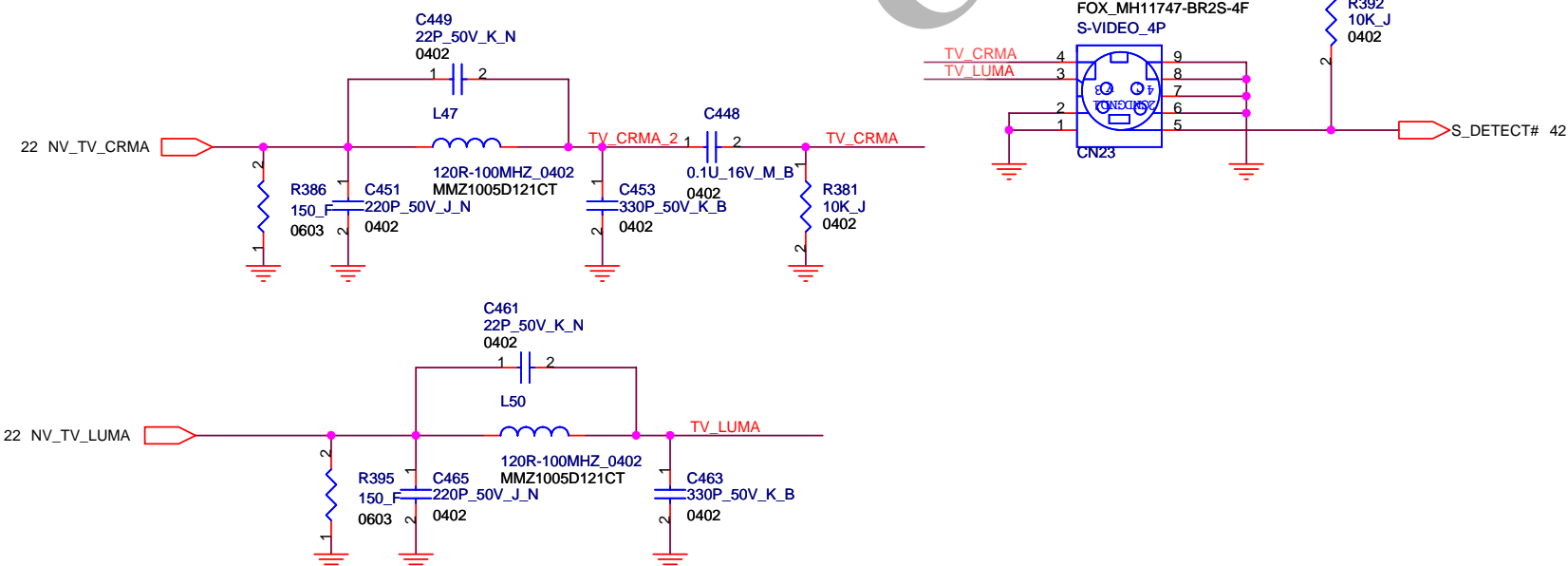
LCD POWER



LVDS CONNECTOR



INVERTER CONNECTOR

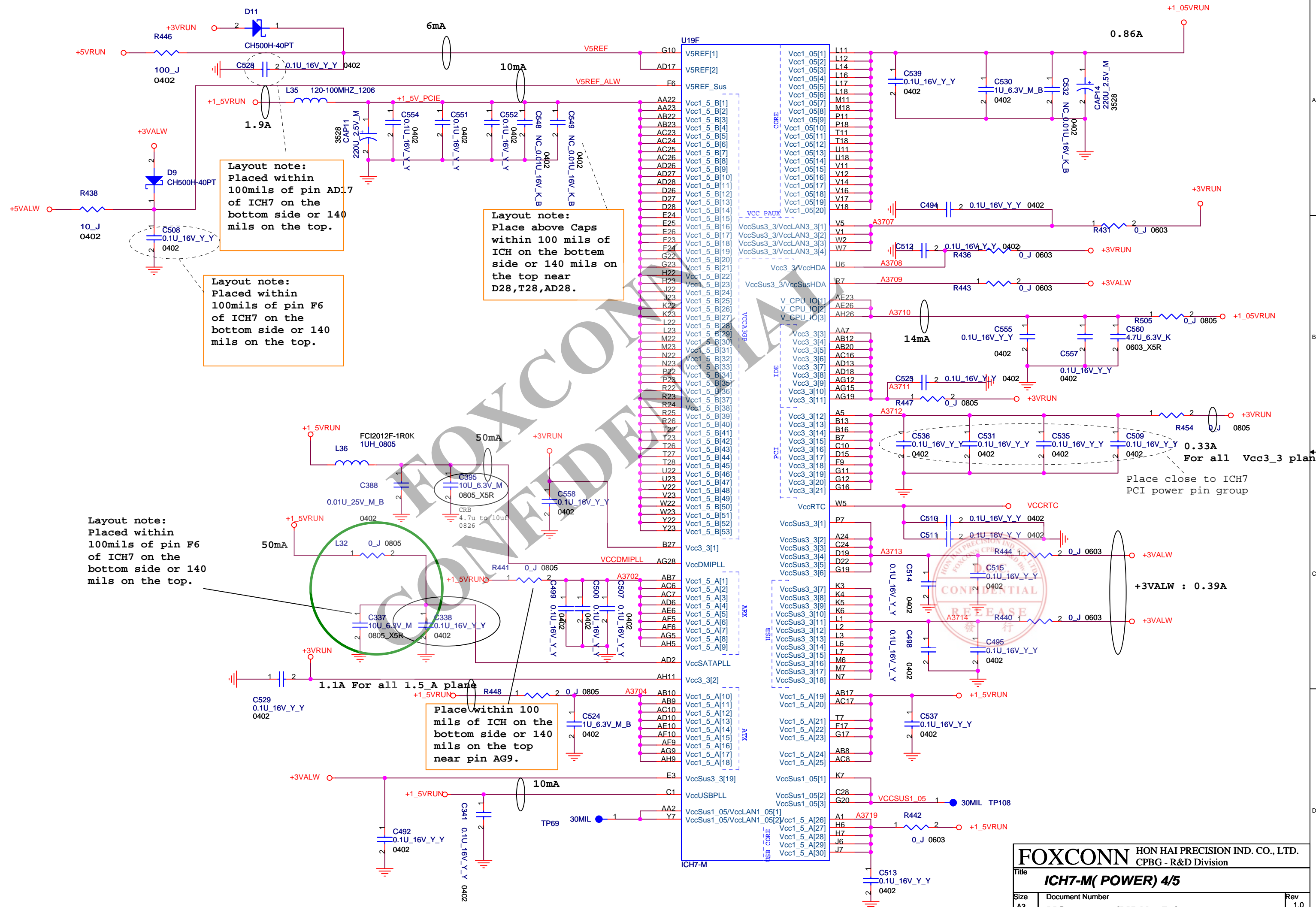


S-VIDEO

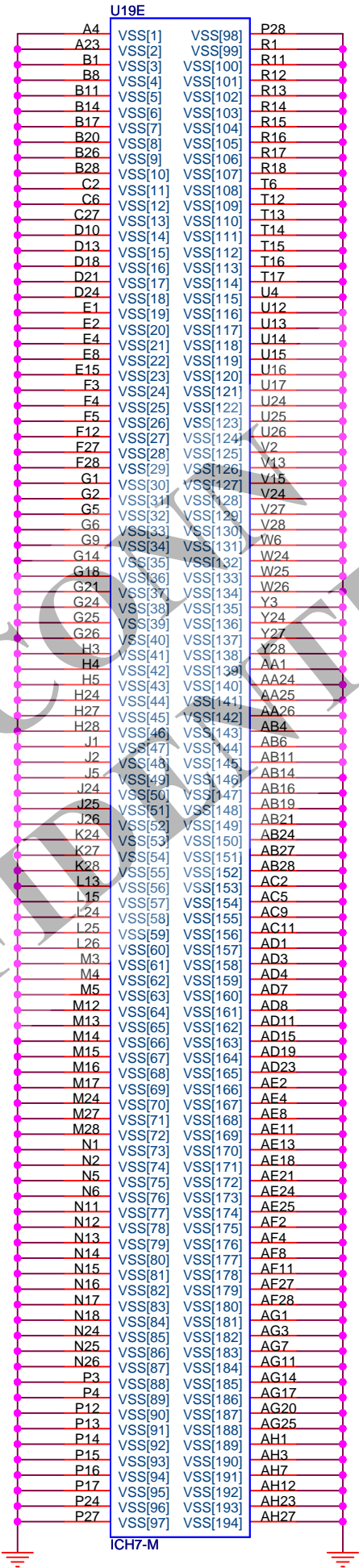
FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title	LVDS / S_VIDEO	
Size	Document Number	Rev
Custom	MS60-1-01 (MBX-159)	1.0
Date:	Monday, October 02, 2006	Sheet 25 of 56

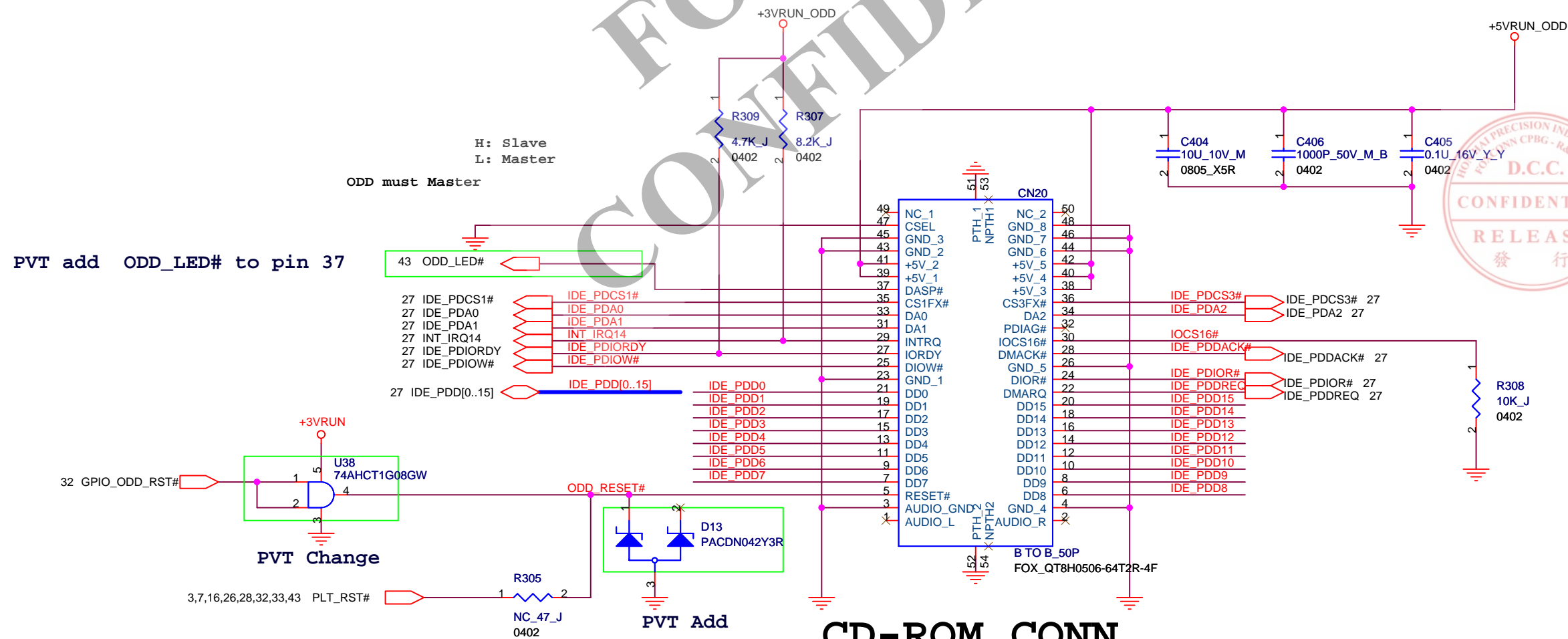
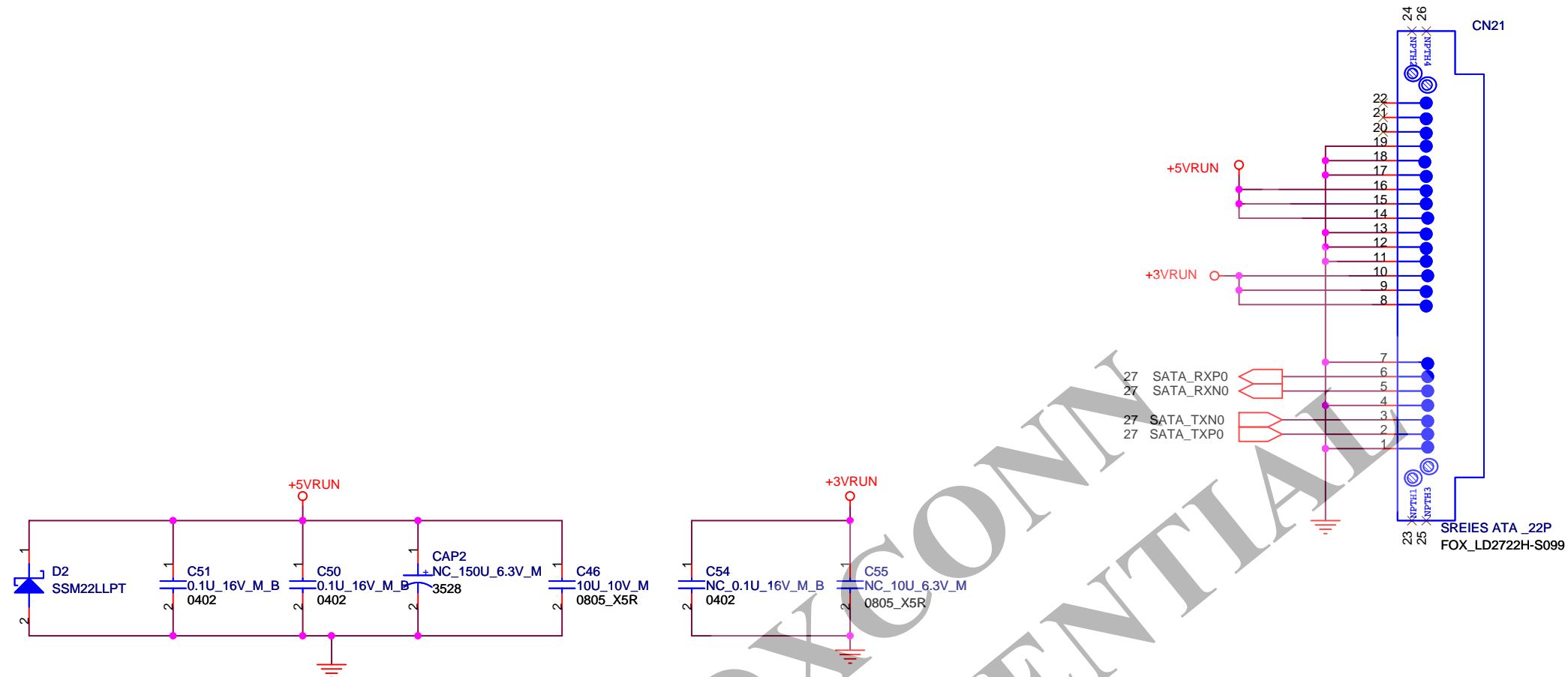




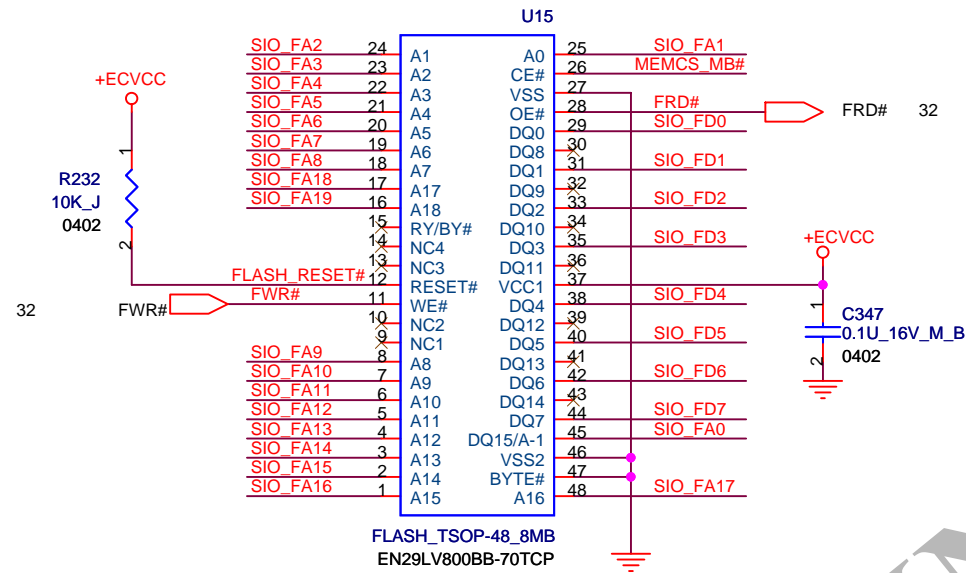
CONFIDENTIAL



SATA HDD CONN



32 SIO_FA[19..0]
32 SIO_FD[7..0]



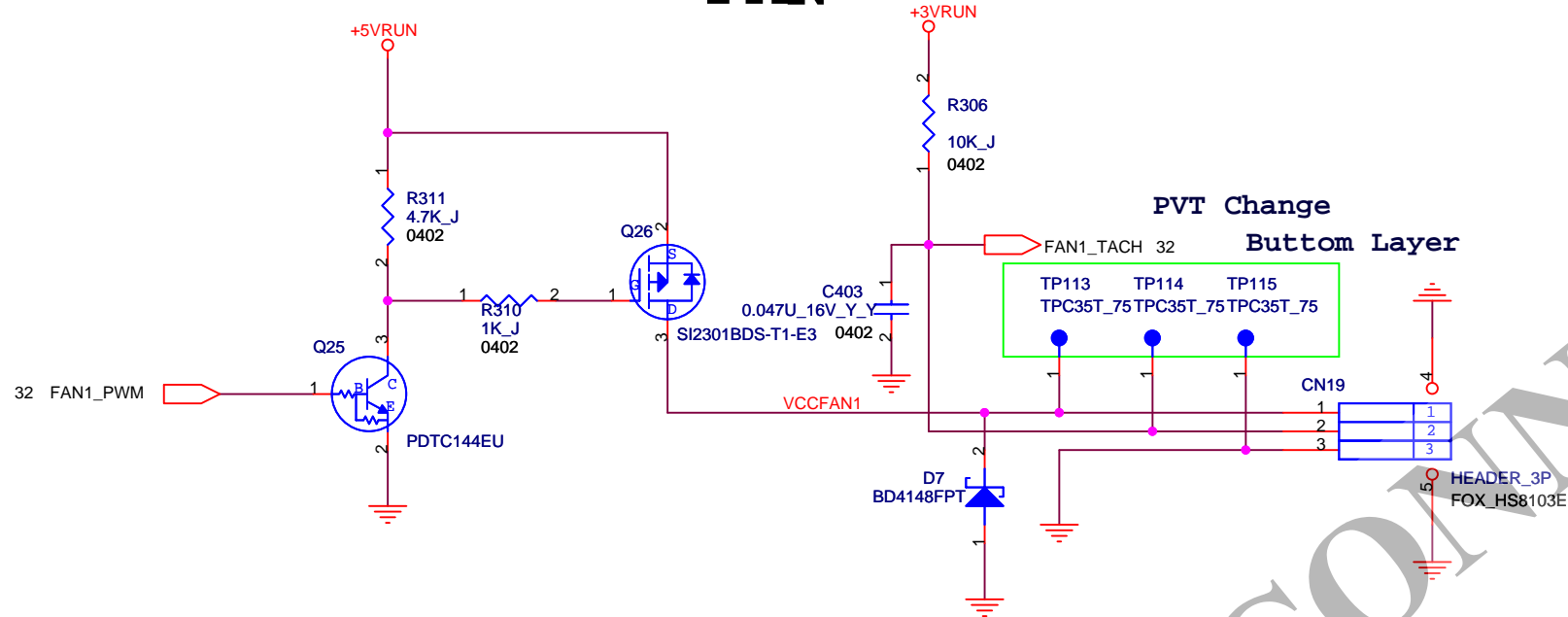
WWAN FOR MS60-L ONLY!!

FOXCONN
CONFIDENTIAL

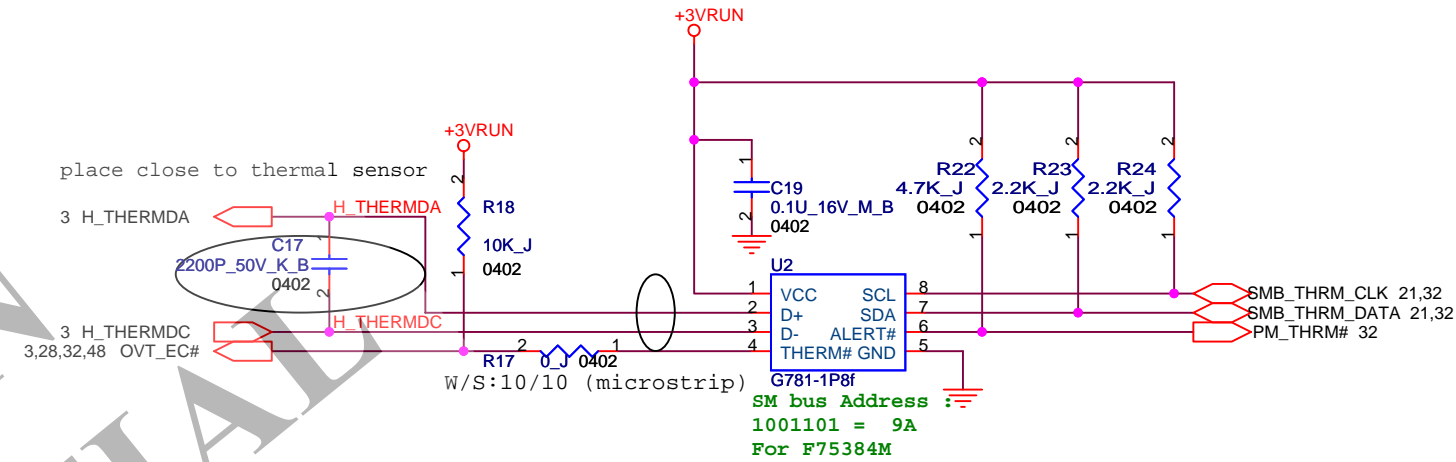


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
WWAN			
Size	Document Number		Rev
Custom	MS60-1-01 (MBX-159)		1.0
Date:	Monday, October 02, 2006	Sheet	34 of 56

FAN

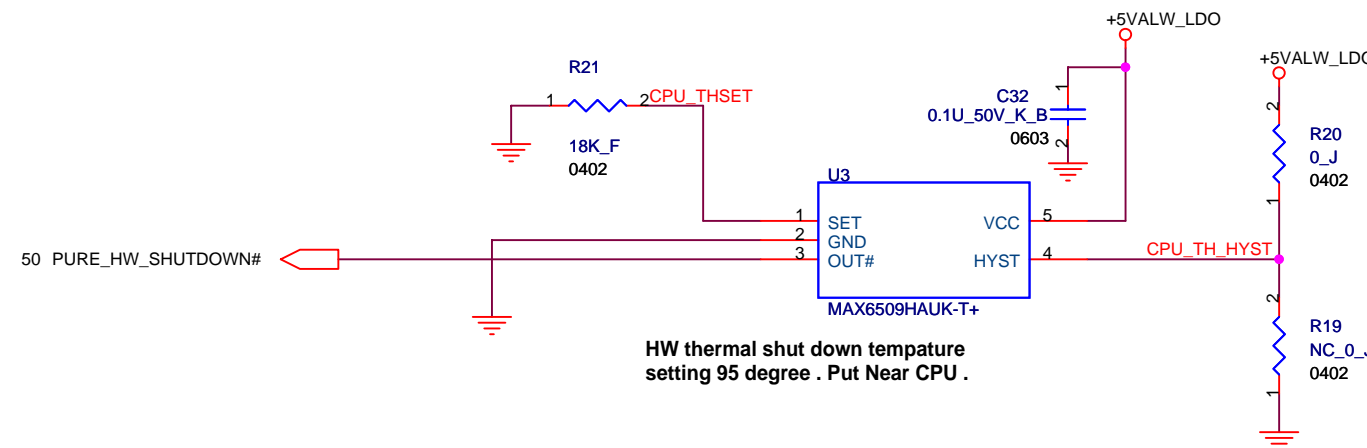


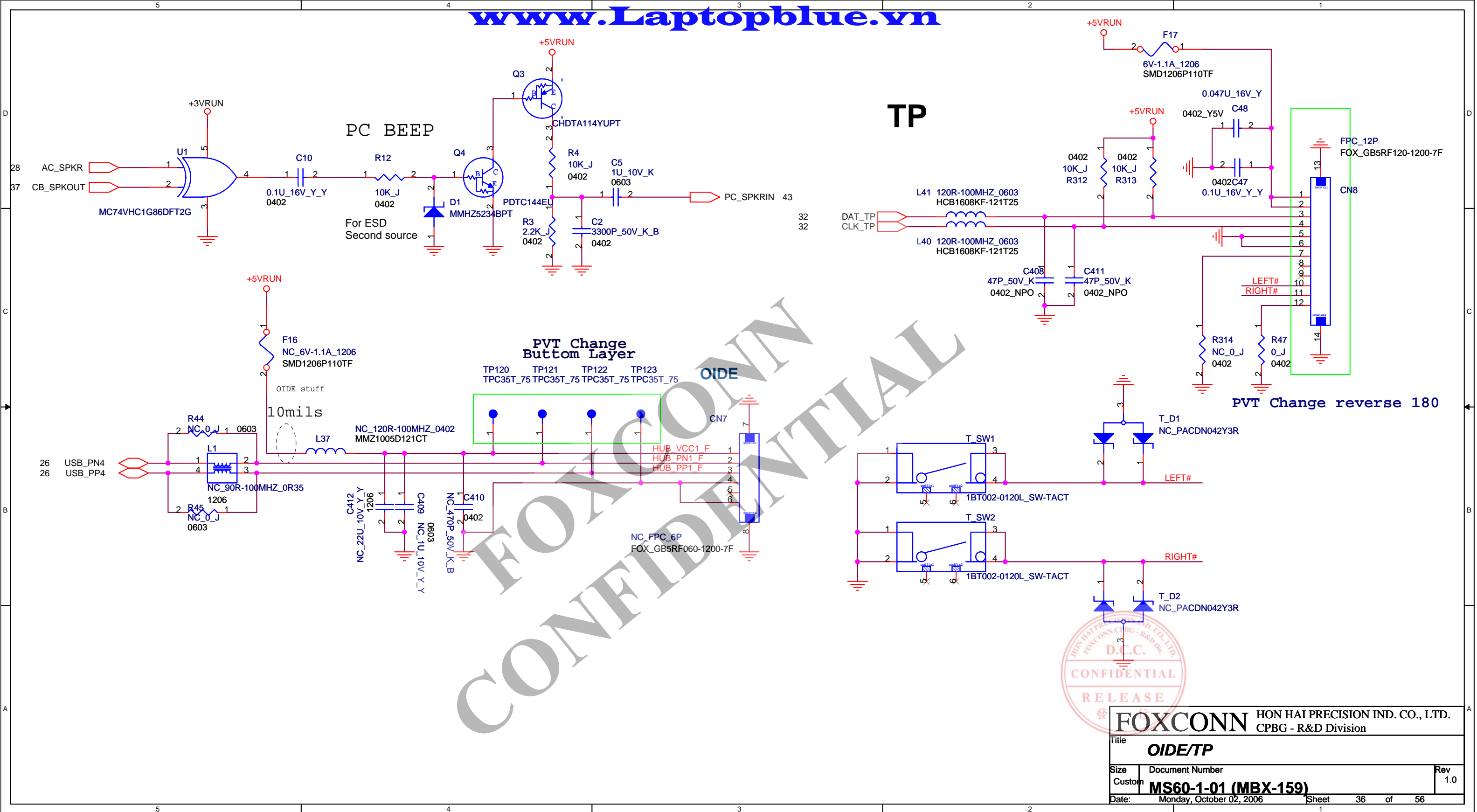
CPU SENSOR

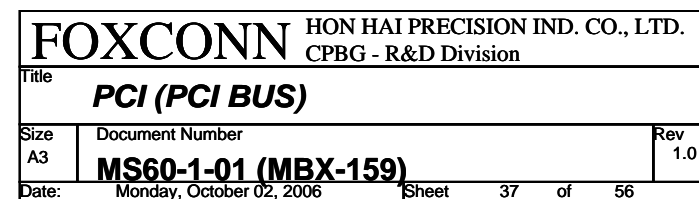


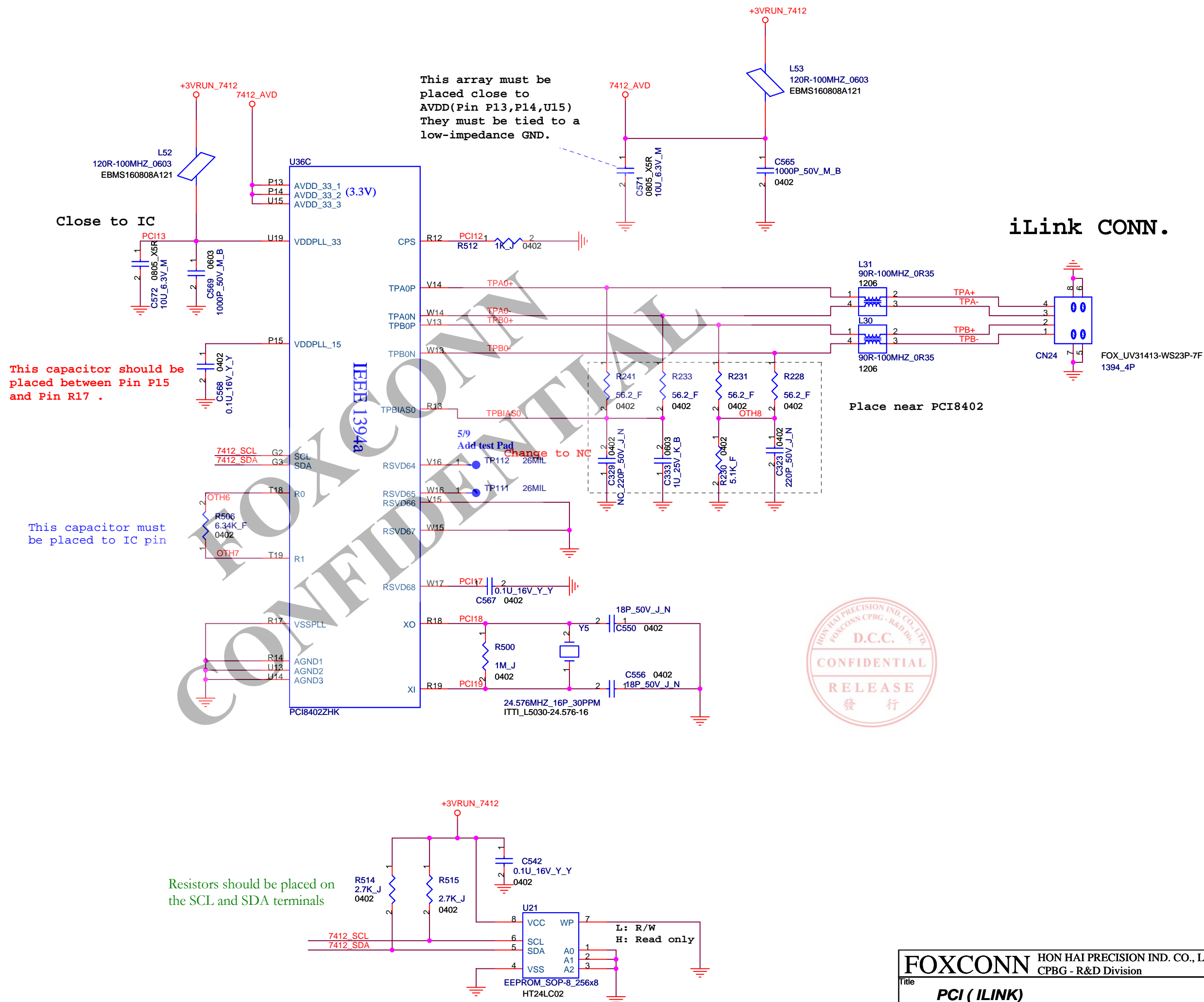
Place Thermal-Sensor near
CPU & GMCH.

HW THERMAL PROTECTION

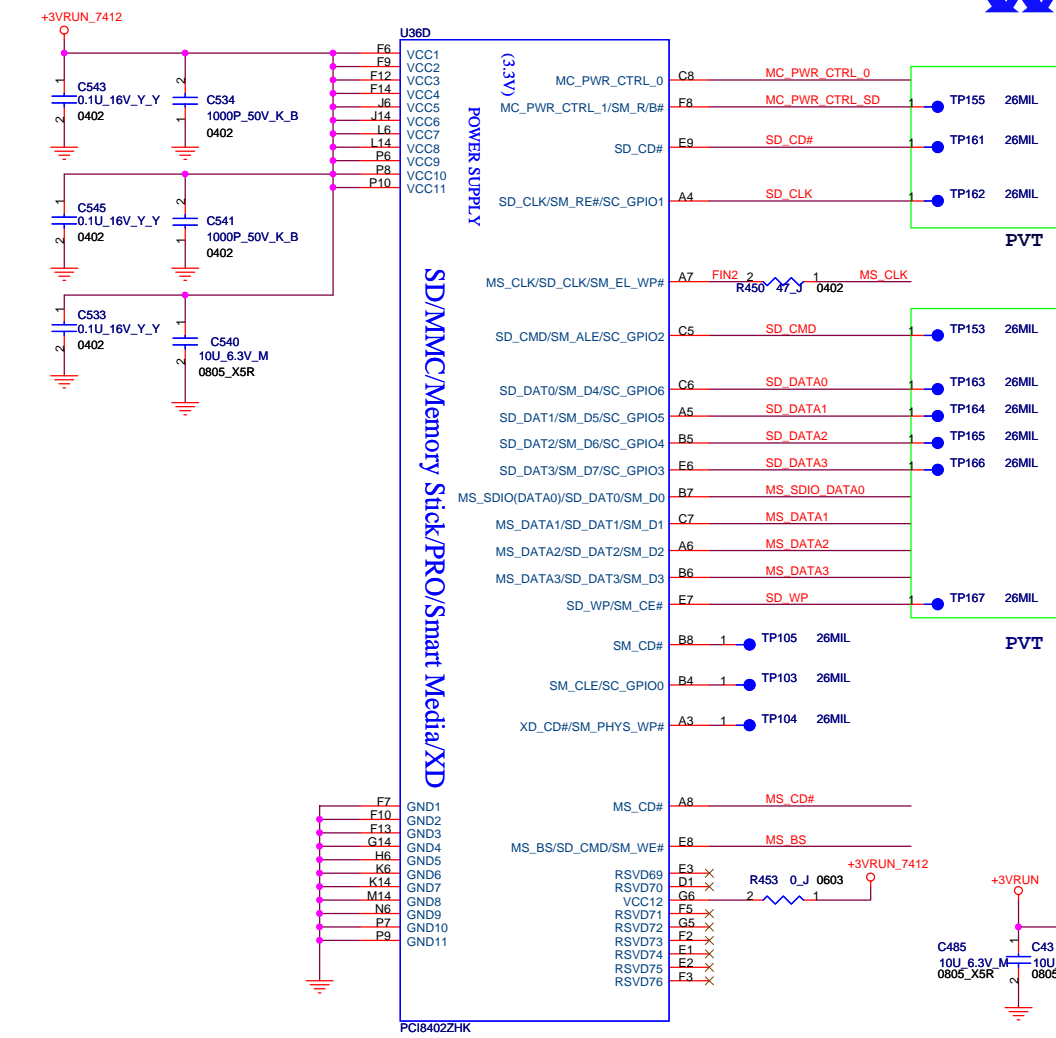








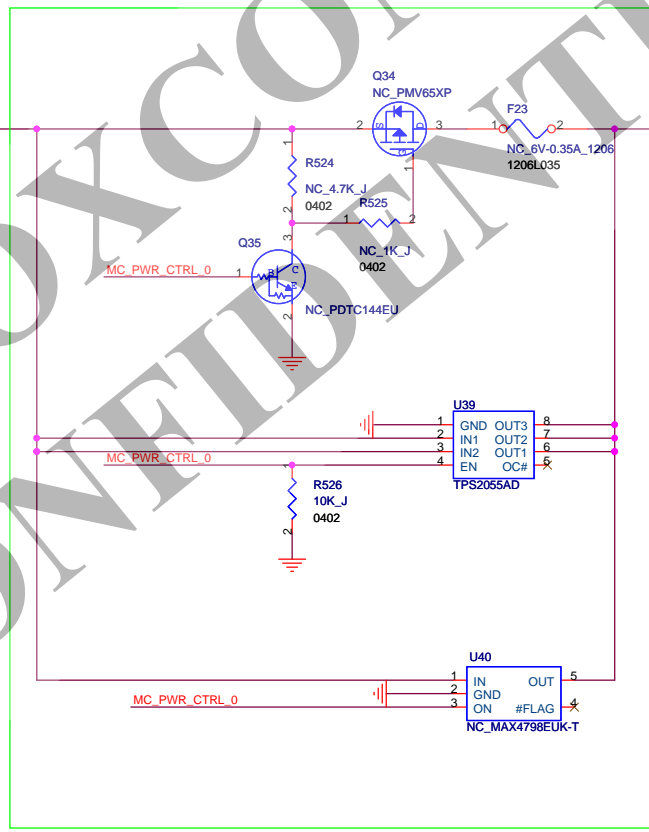
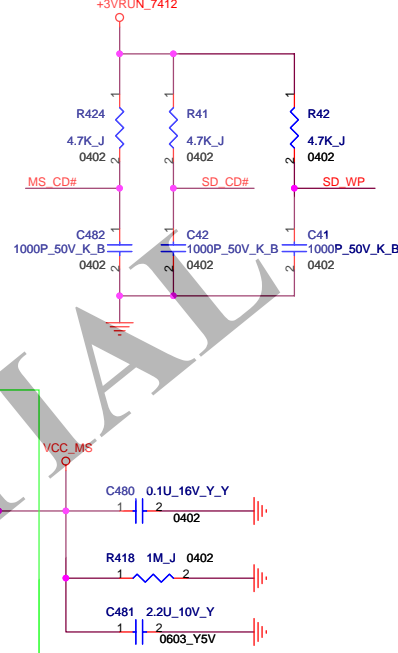
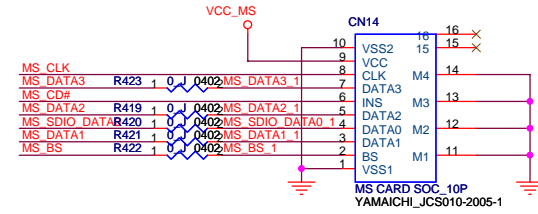
MS Duo / Pro

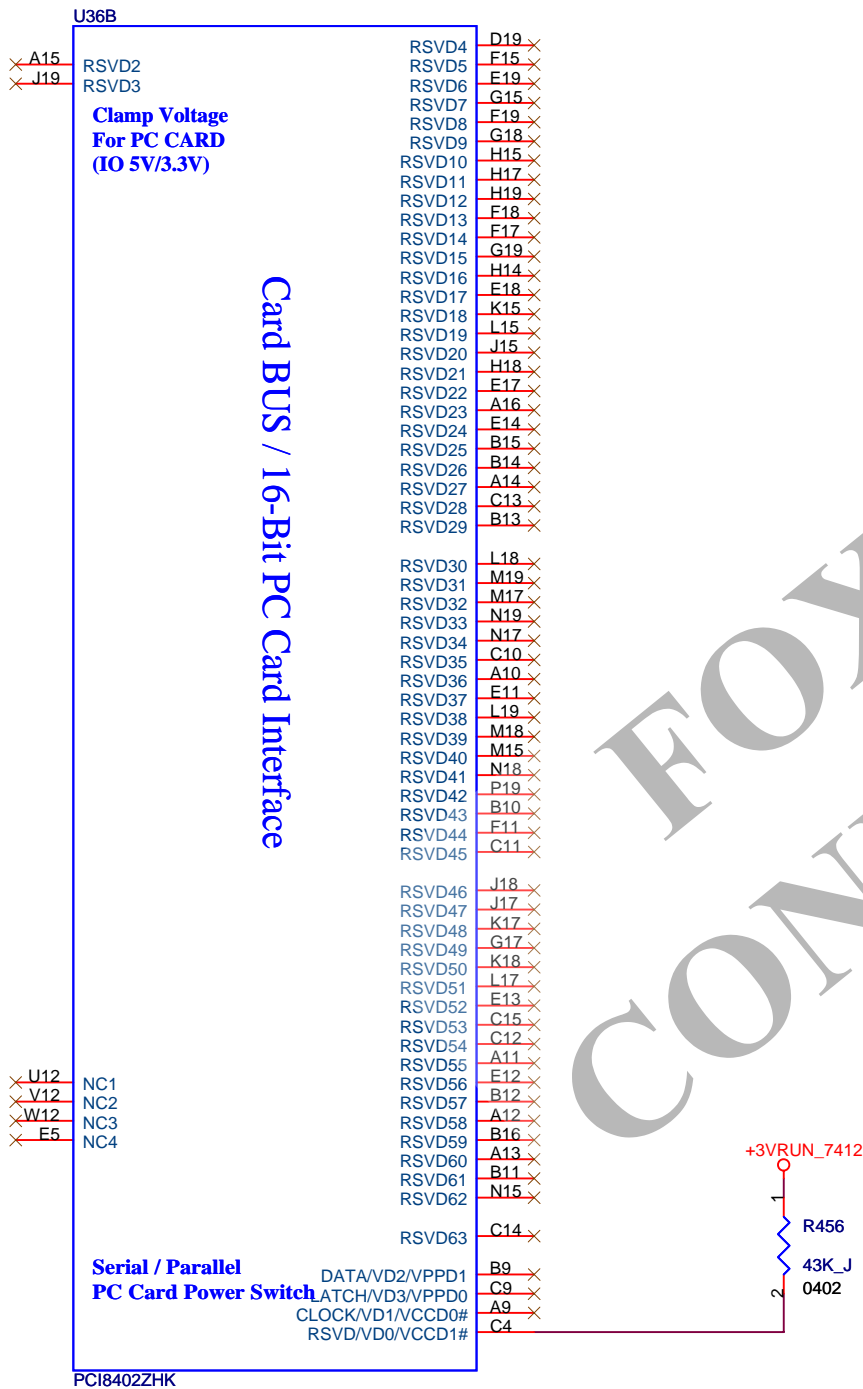


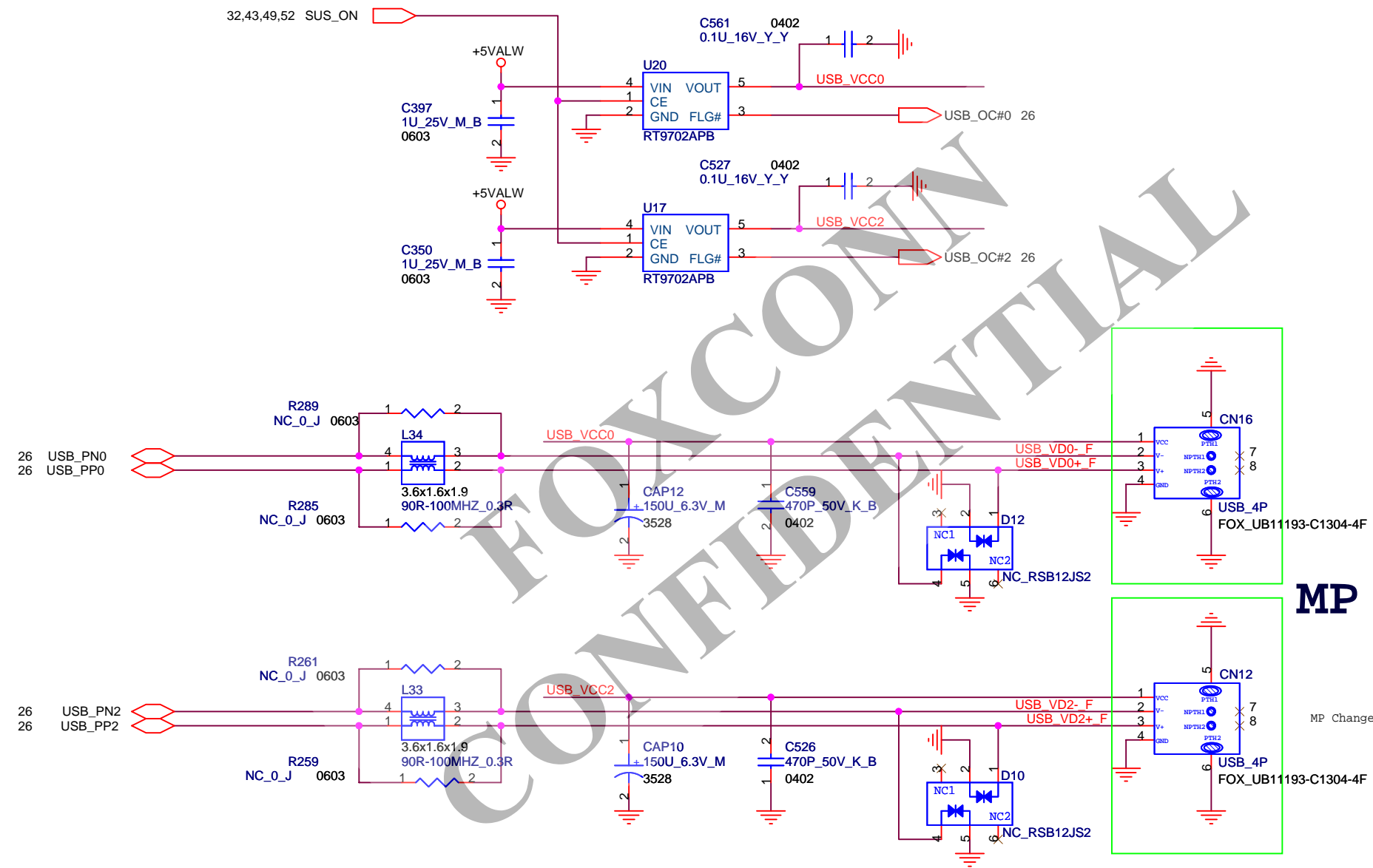
PVT Change to test point

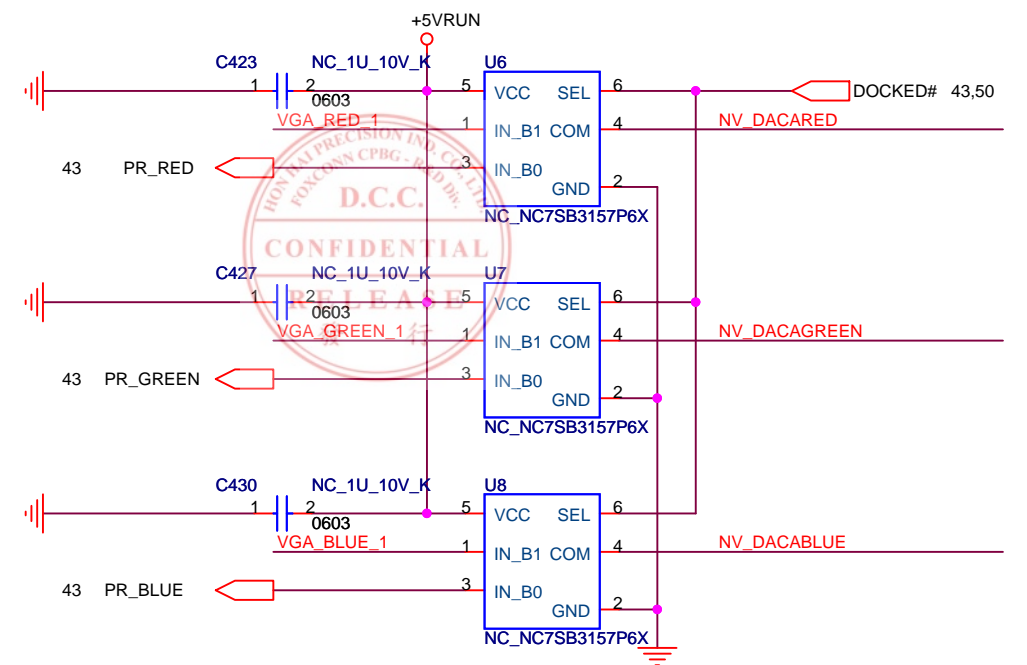
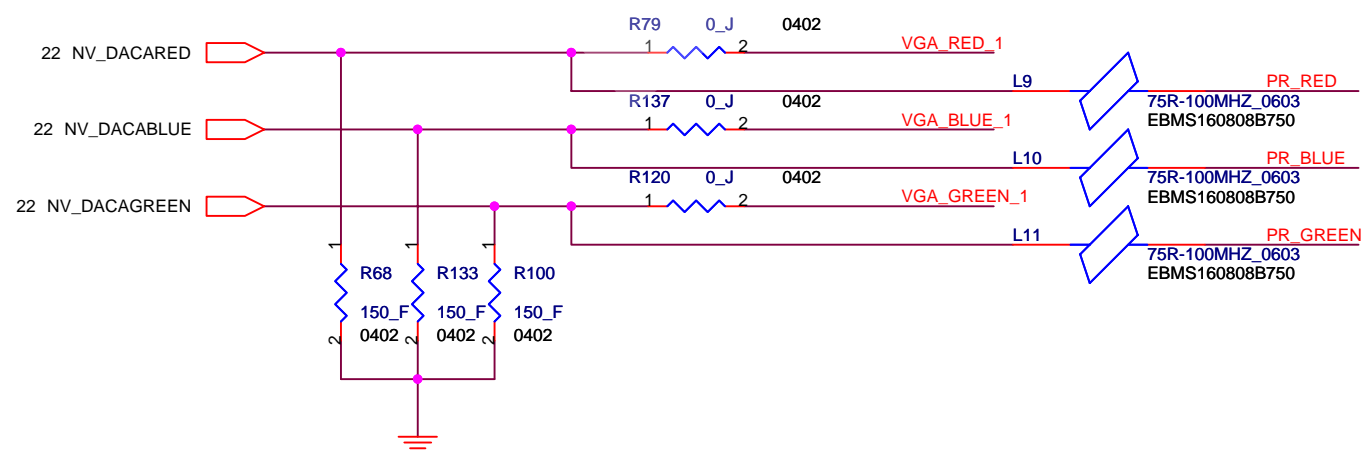
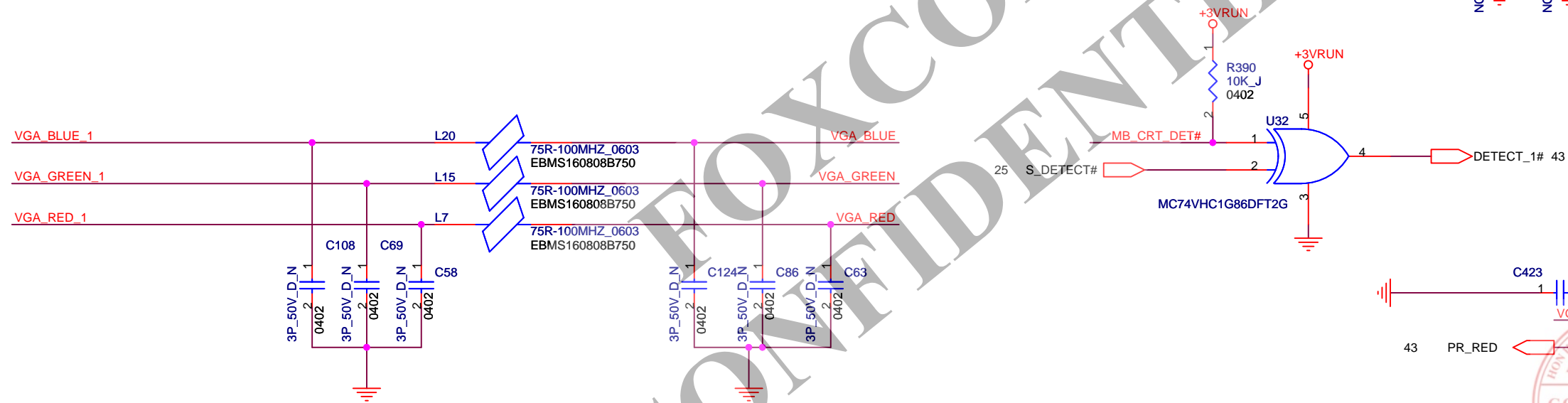
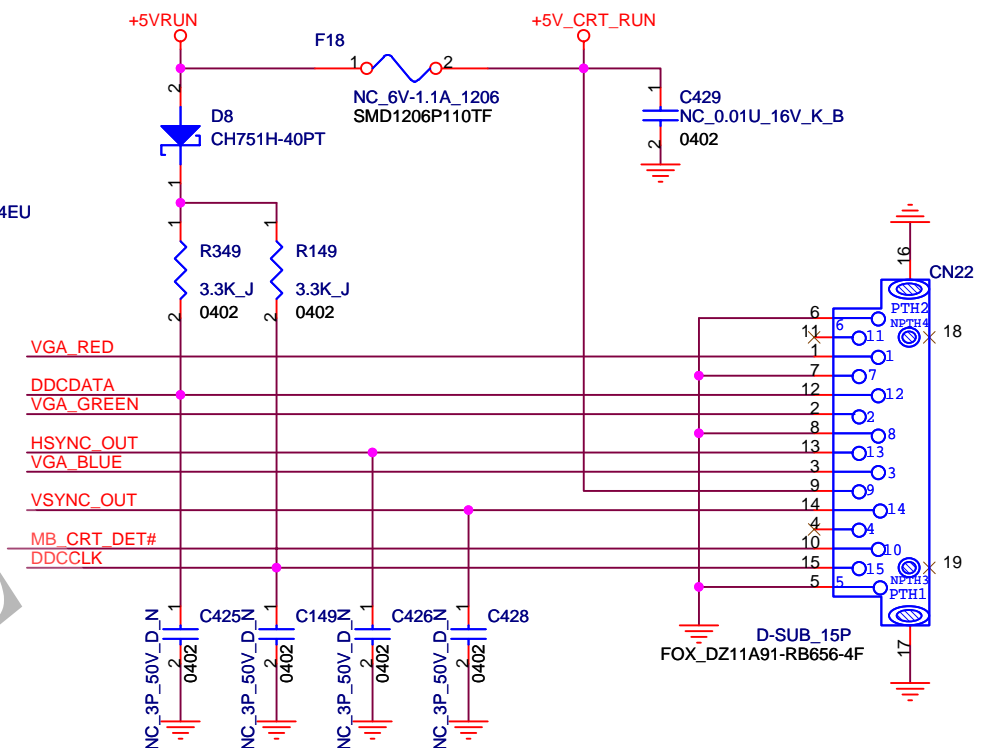
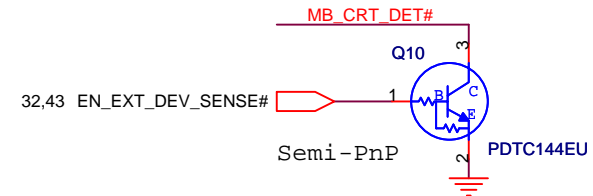
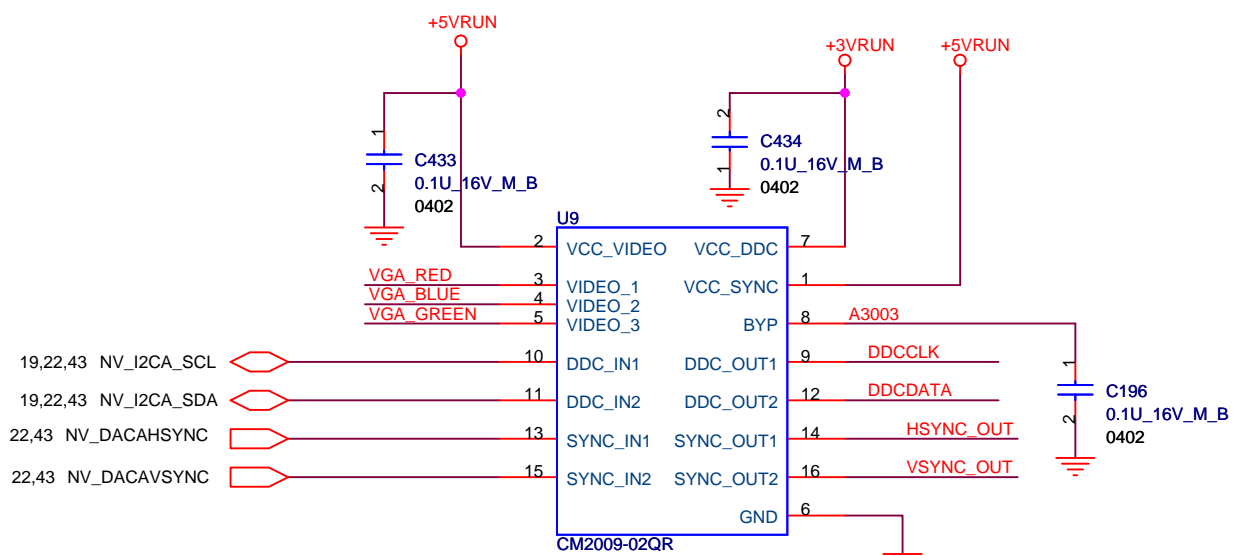
PVT Change to test point

MP Change

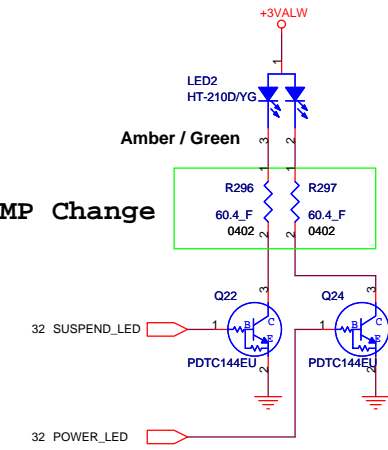




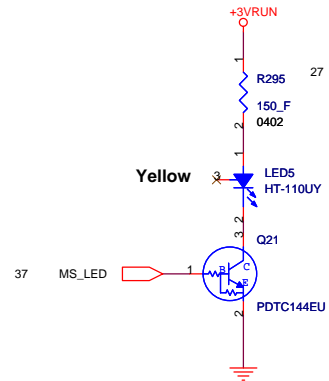




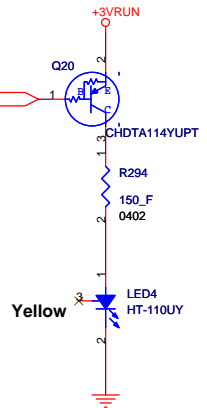
MP Change



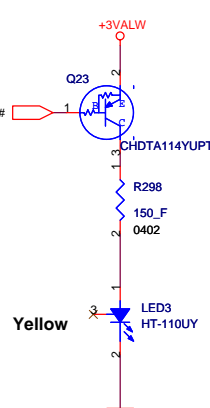
Yellow



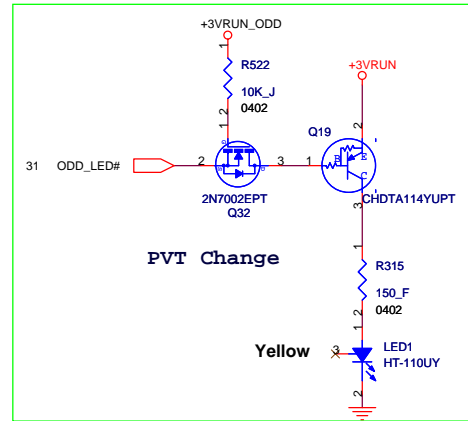
Yellow



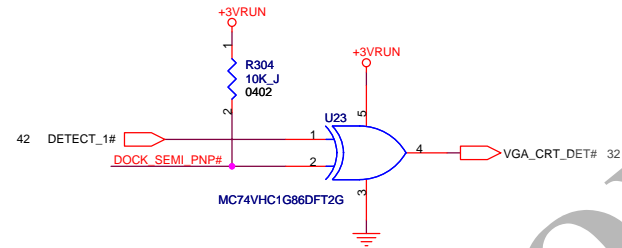
Yellow



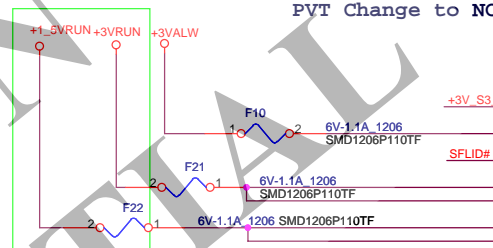
PVT Change



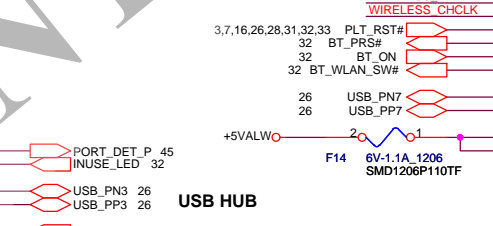
DOCK SEMI PNP#



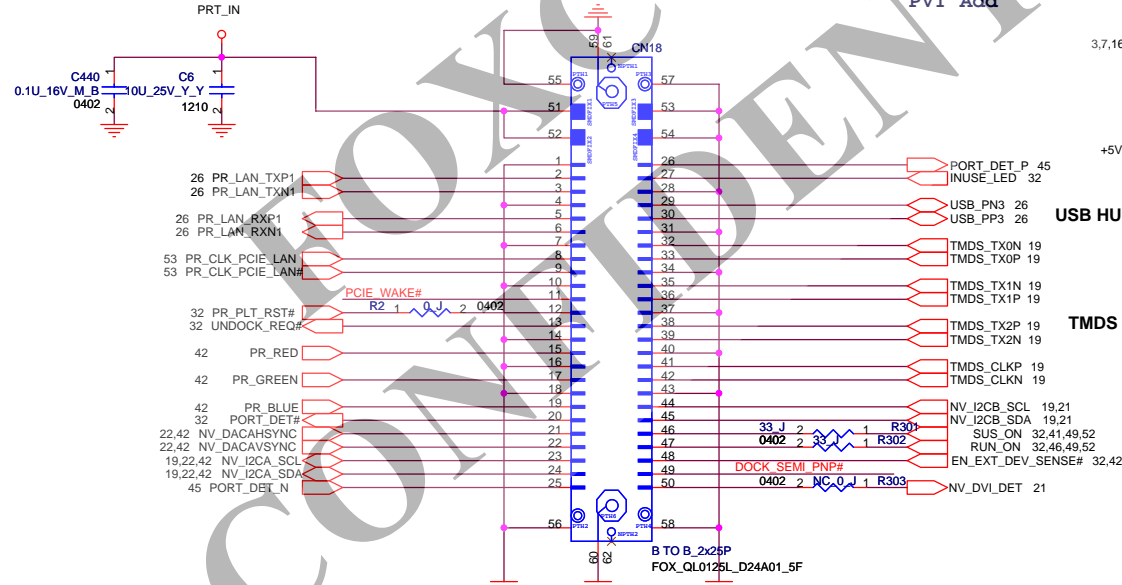
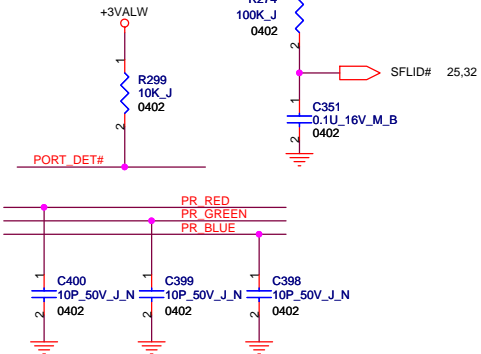
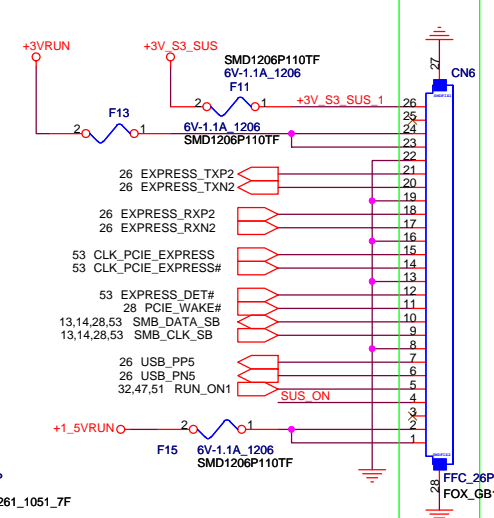
PVT Change to GB11261_1051_7F



PVT Add



PVT Change to GB11261_1051_7F

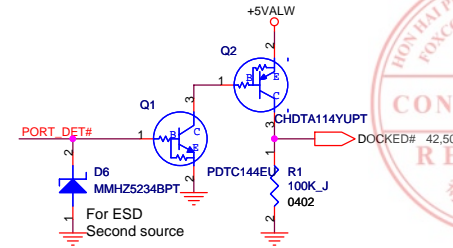


Replicator Port

USB HUB

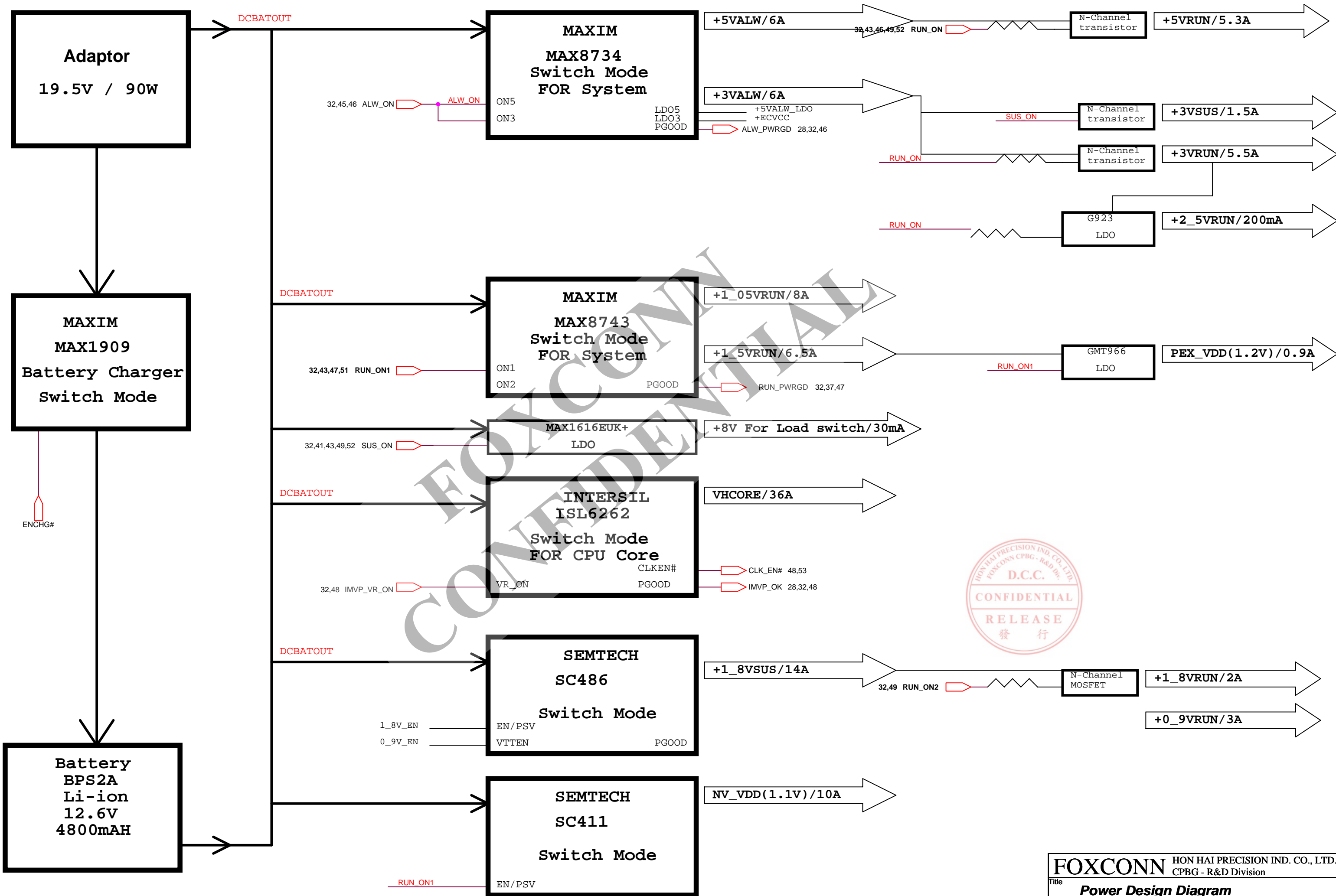
TMDS

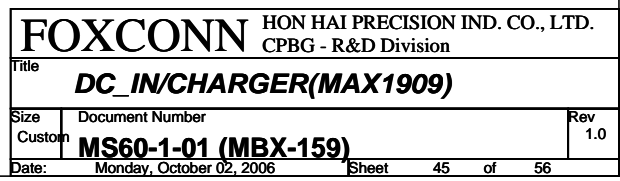
PVT Change to GB11261_1051_7F

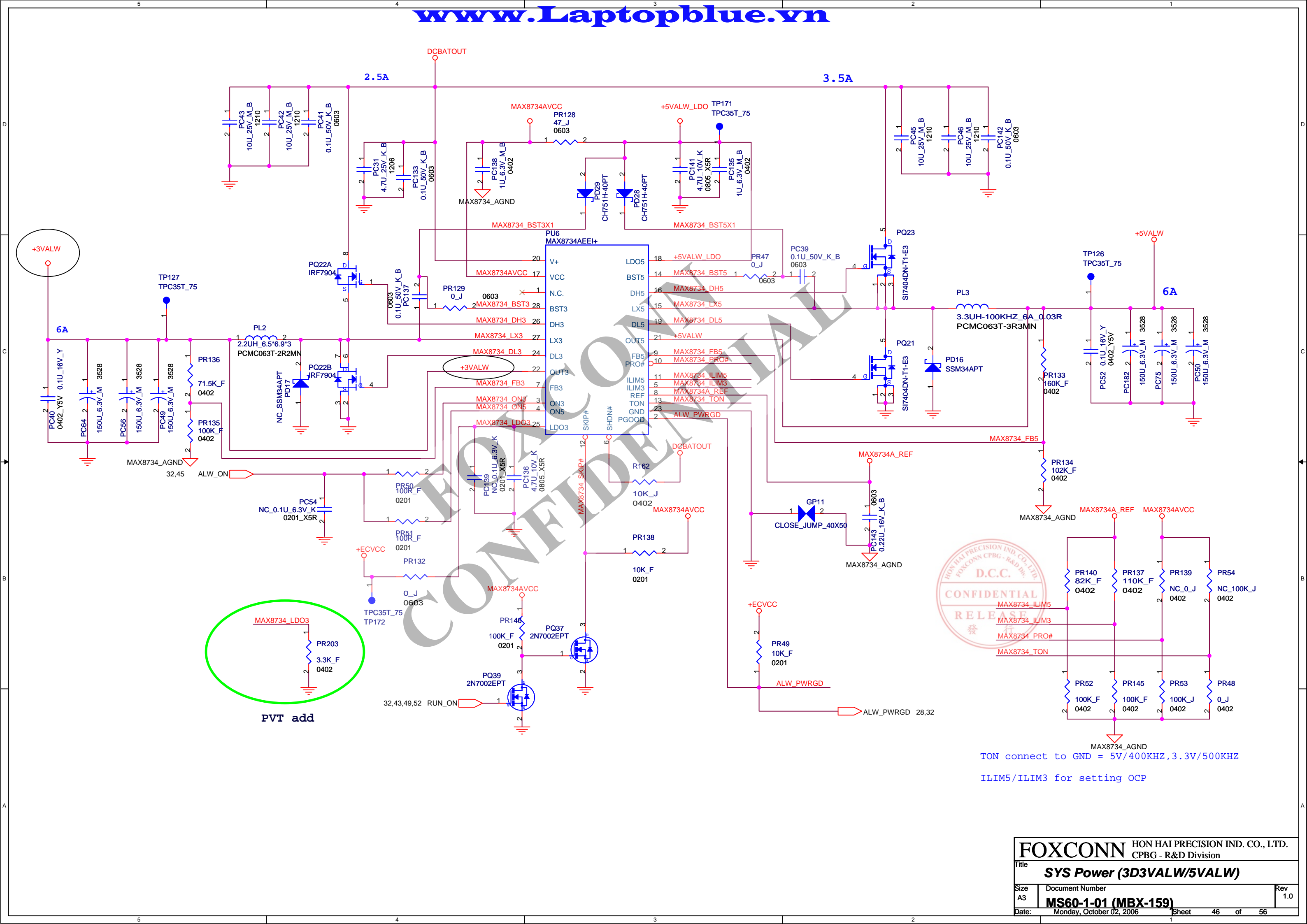


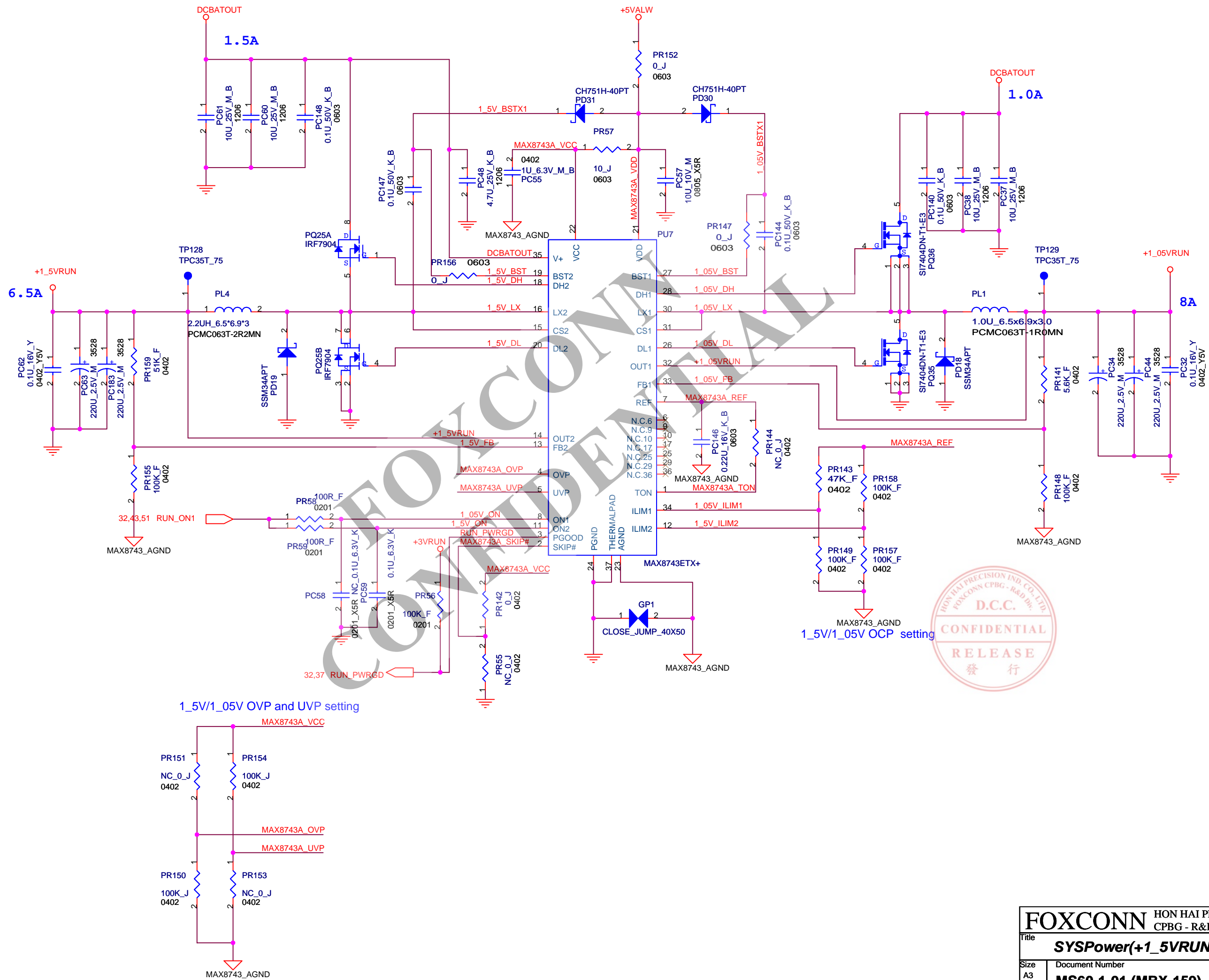
PVT Change to GB11261_1051_7F

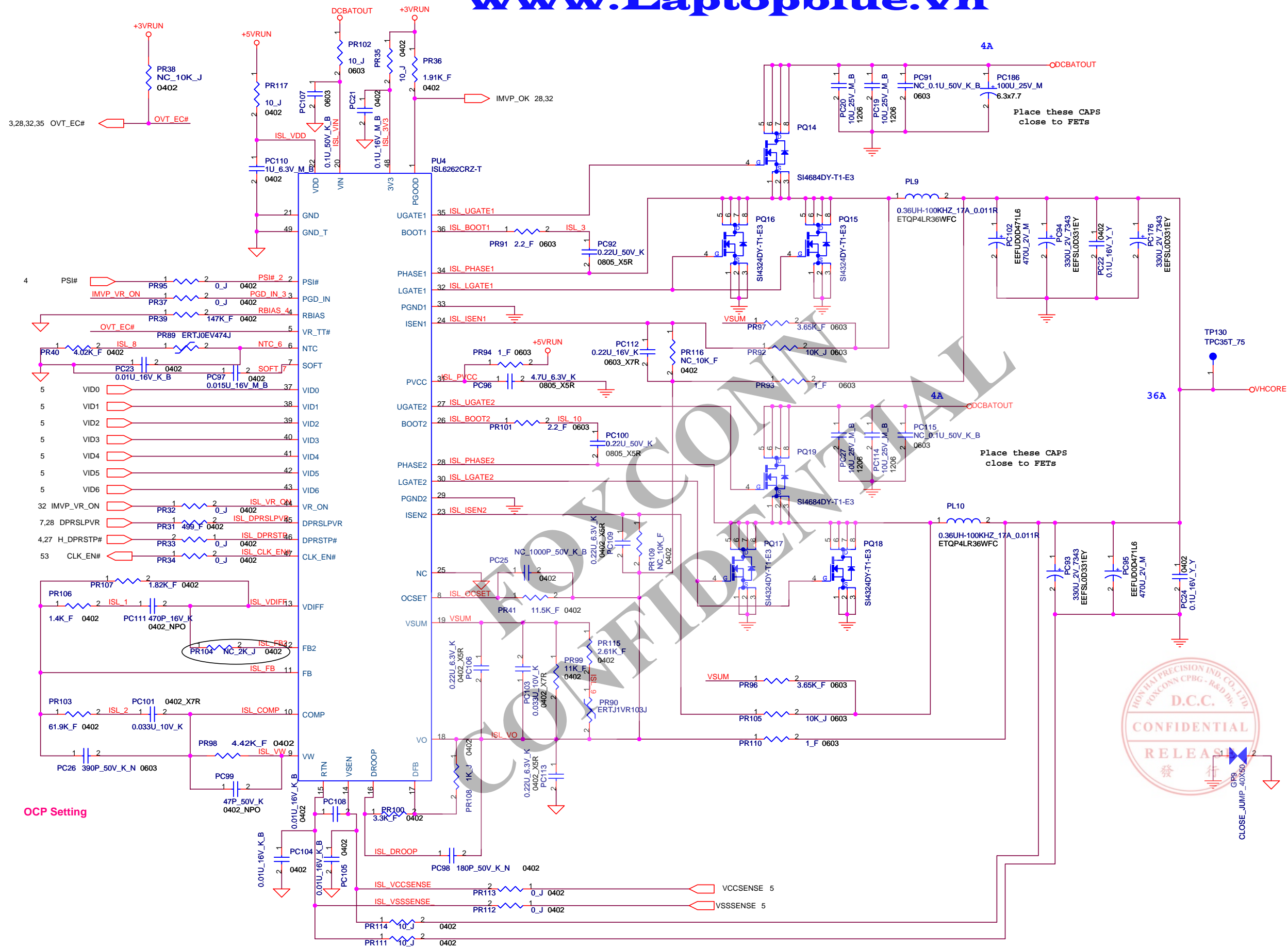






[illegible]



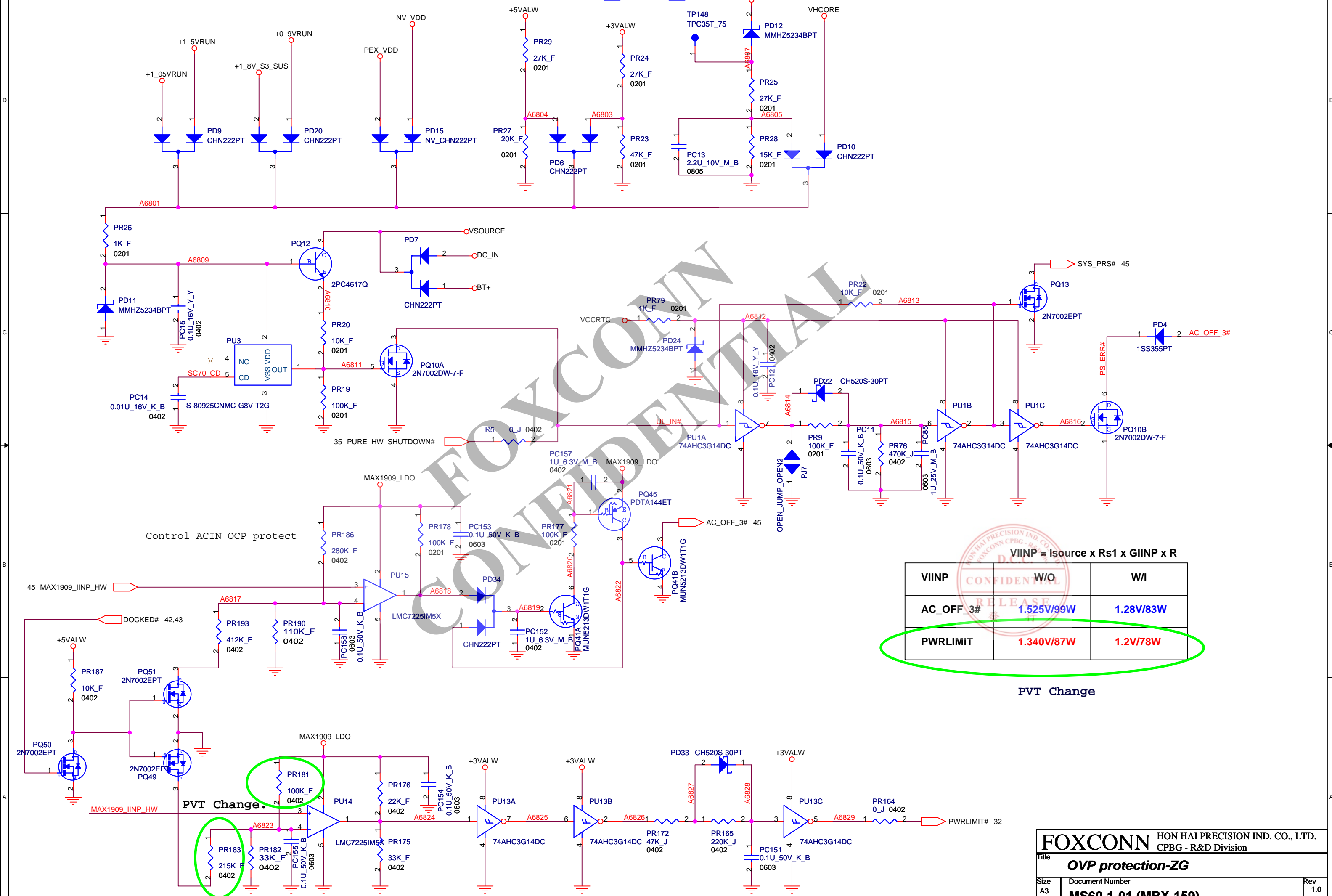


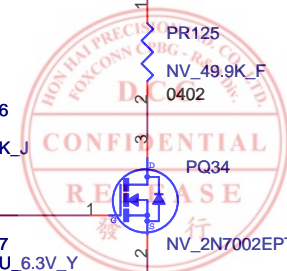
OCP Setting

VID0 TP131 TPC35T_75
VID1 TP133 TPC35T_75
VID2 TP135 TPC35T_75
VID3 TP137 TPC35T_75
VID4 TP139 TPC35T_75
VID5 TP140 TPC35T_75
VID6 TP141 TPC35T_75

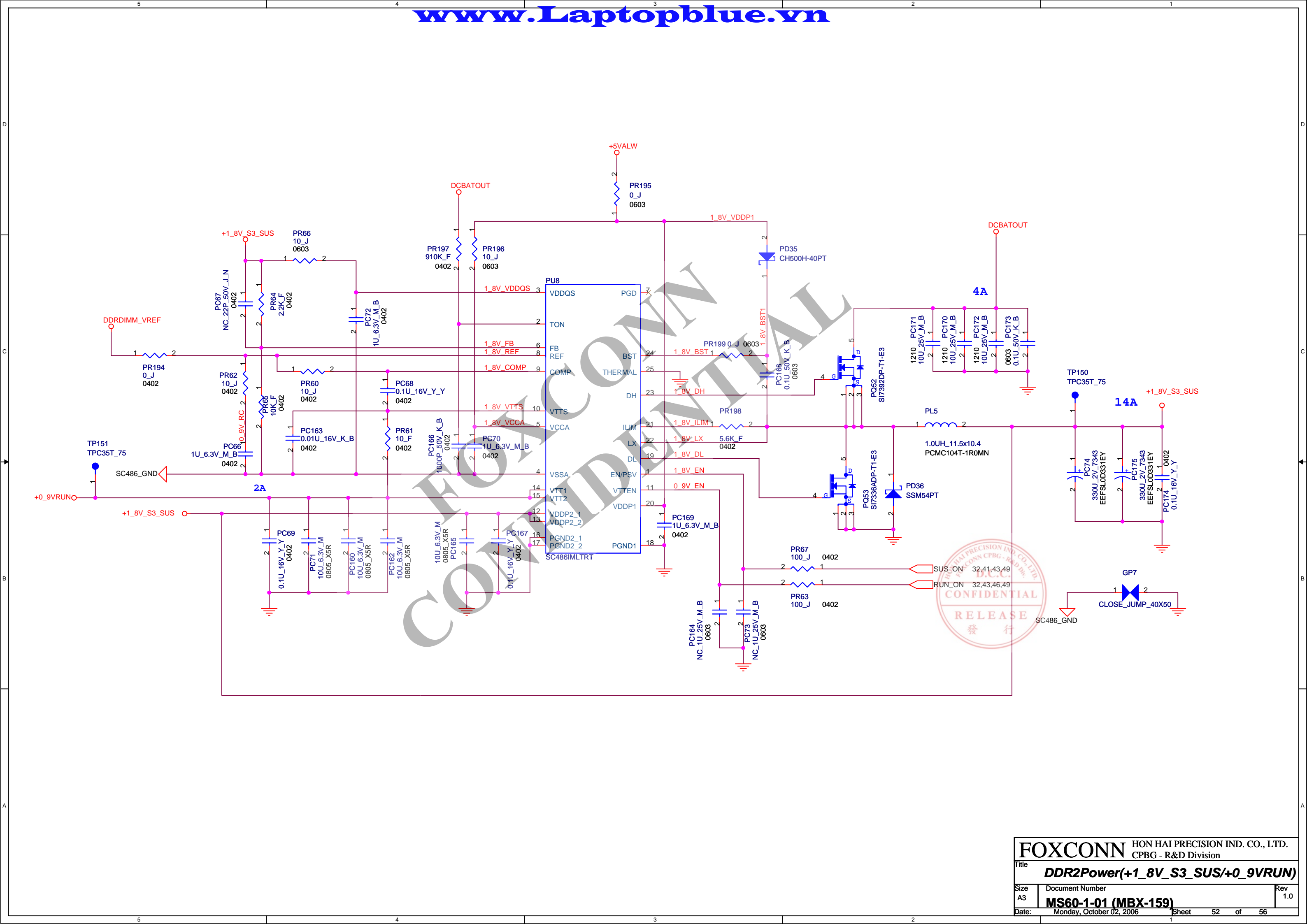
DPRSLPVR TP132 TPC35T_75
IMVP_VR_ON TP134 TPC35T_75
PSI# TP136 TPC35T_75
H_DPRSTP# TP138 TPC35T_75

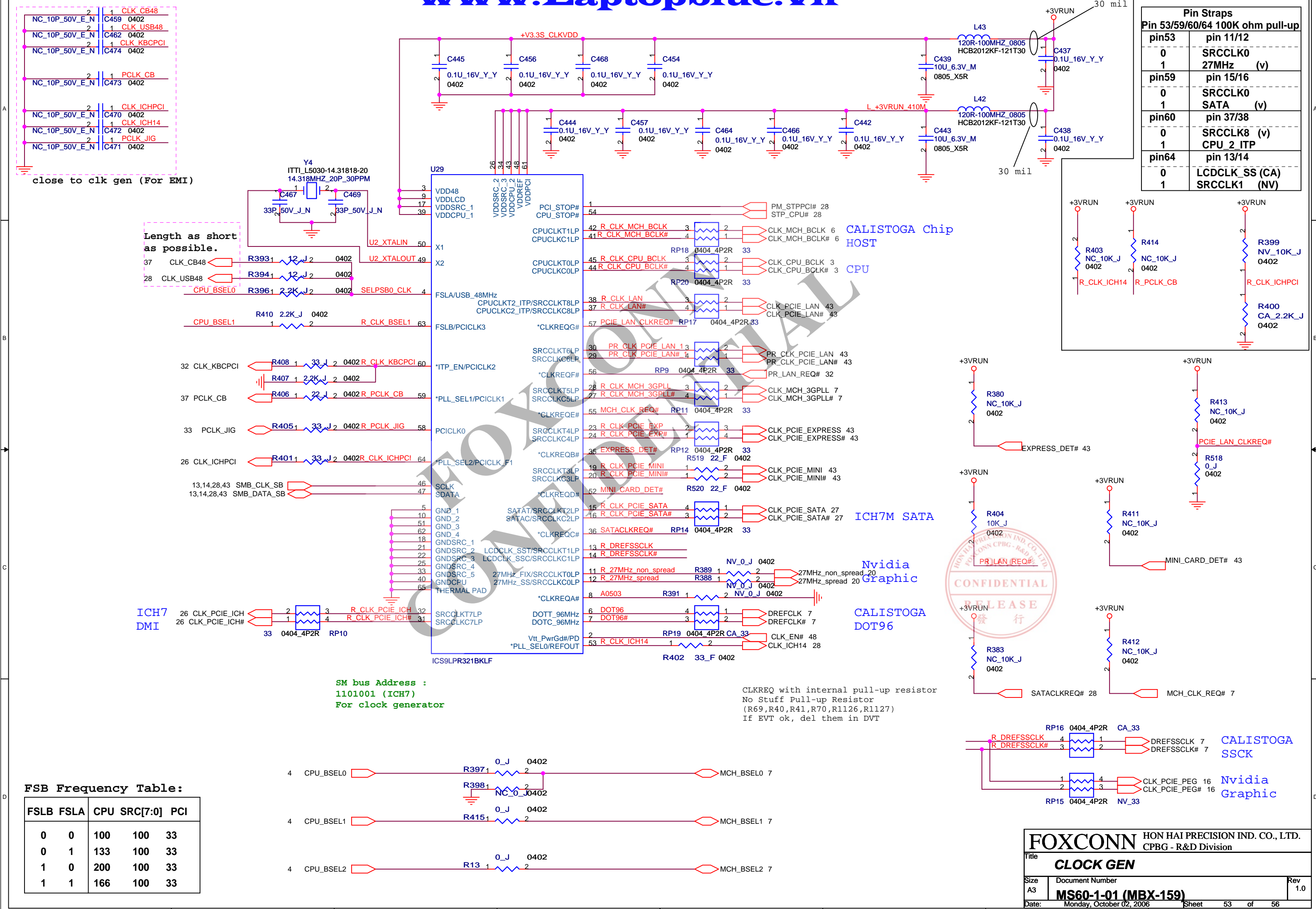


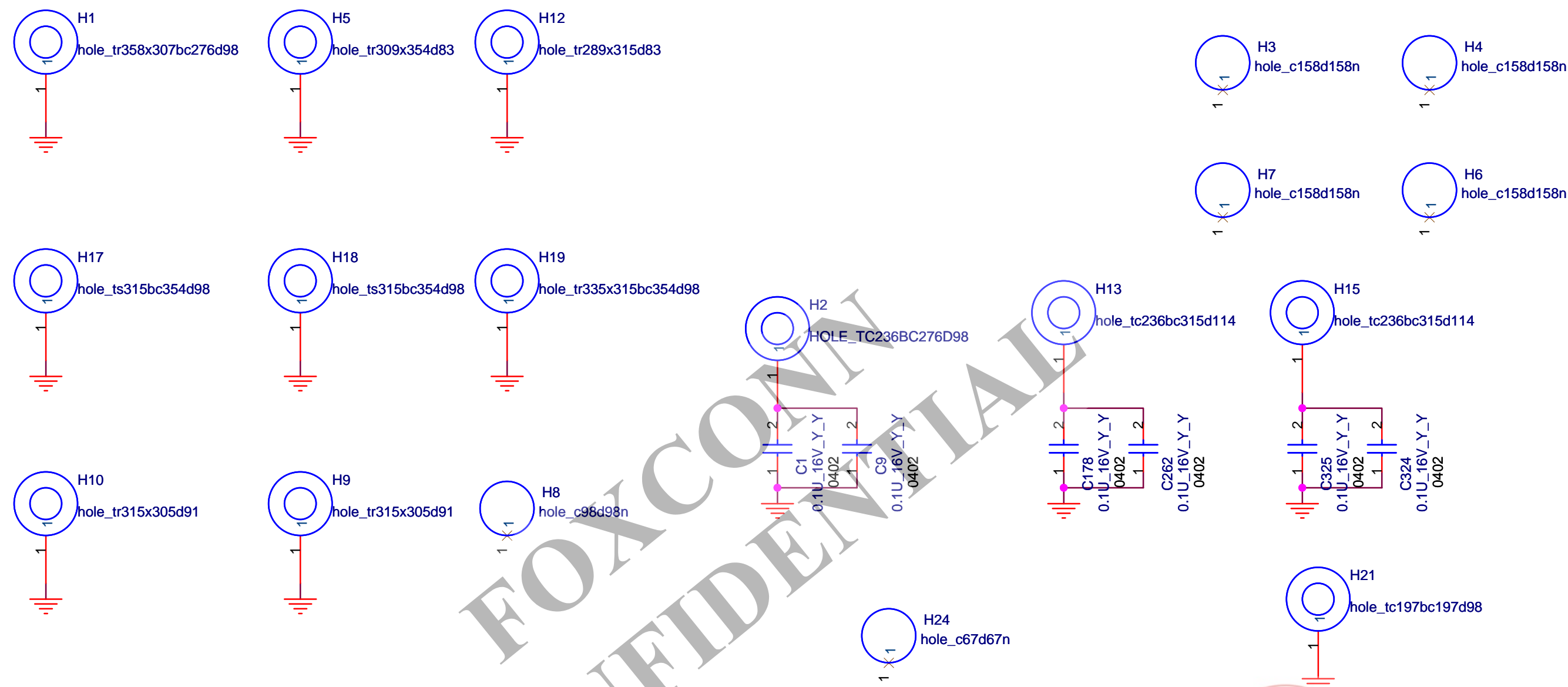




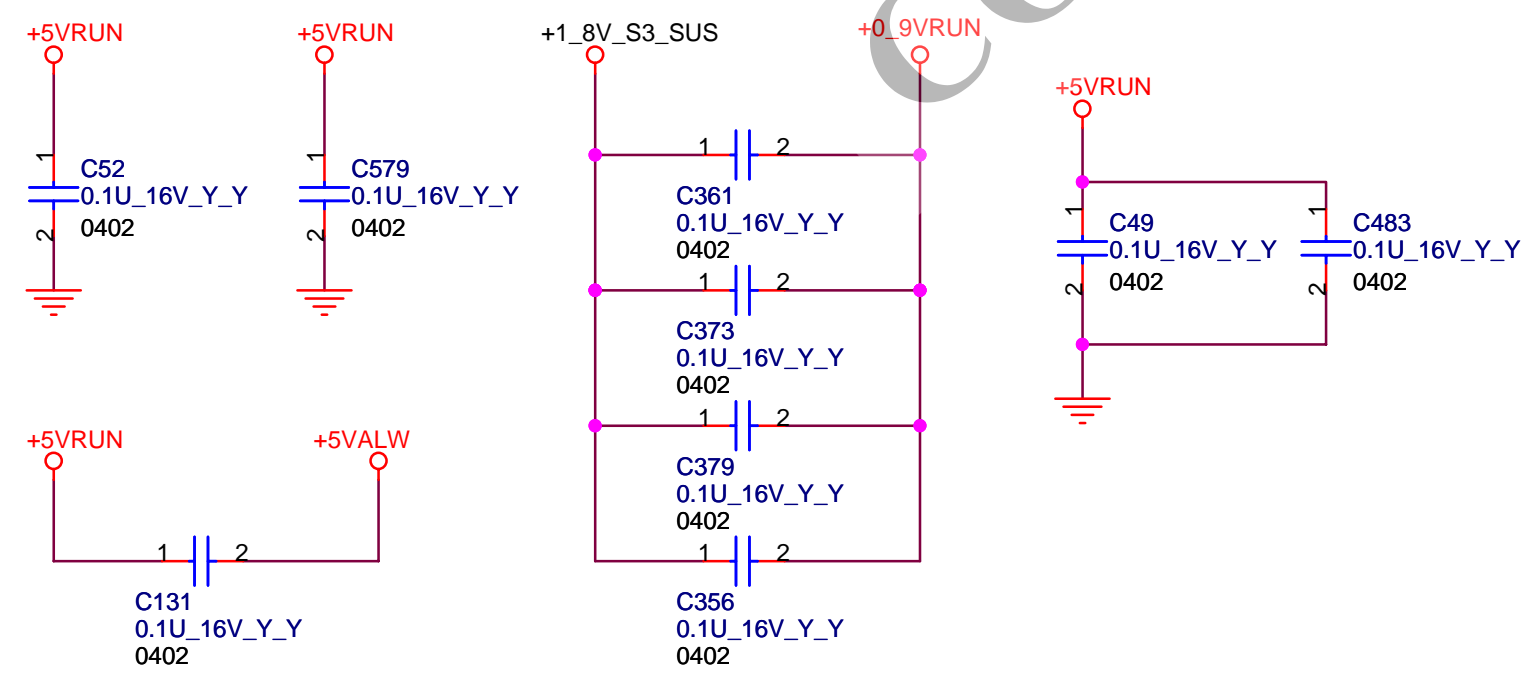
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
VGA POWER(VGACORE&IO)			
Size	Document Number	Rev	
A3	MS60-1-01 (MBX-159)	1.0	
Date:	Monday, October 02, 2006	Sheet	51 of 56







FOR EMI



FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title HOLE		
Size A4	Document Number MS60-1-01 (MBX-159)	Rev 1.0
Date: Monday, October 02, 2006	Sheet 54	of 56

according to ME requirement.

factor according to ME requirement.

2NDING CN3 Pin1 for WWAN removing.

or WWAN removing.

for Debug BD LED.

and replace with PLT_RST#.

related circuit in Page#10/25/42.

It's from EC Pin#1 to Pin176 for Noise decreasing.

update to improve VGA power feedback.

for ODD connector also new power plane control for this.

or VGA improvement.

or customer's comment.

replace with R51R520 for WLAN issue improving.

1 for VRAM.

VGA Power modification.

ector footprint to FOX_UB11193_C1301_4F.

BOM Connector that is FOX_UB11193_C1304_4F

<115>2006/8/08 Change R433 to 330.

<116>2006/8/08 add C95 PIN26 to +3V_33_SUS .

<117>2006/8/08 add C95 PIN19,20 to 3V1RUN .

<118>2006/8/08 add C95 PIN16,17 to 1.5VRUN .

<119>2006/8/08 Change RR8 to 19.1K.

<120>2006/8/08 Change PR181 to 100K.

<121>2006/8/08 Change PR183 to 127K.

<122>2006/8/08 add F20,F21,F22 to 1M-F06/V1A1-F000.

<123>2006/8/08 del F20

<124>2006/8/08 add R523 .

<125>2006/8/08 Would R303 N.C. DVI-I Hot Plug Detect" is implemented by not Glx but EC as usual.

<126>2006/8/08 Change RR8 to 22.1K.

<127>2006/8/11 Change RR15 to 1R-0000203-F100.

<128>2006/8/11 Change RR183 to 1R-002163-F200.

<129>2006/8/04 add D15,D16 to 16-3C-S500V-4000.

<130>2006/8/04 add Q34 to 17-PM-69-XP-0000

<131>2006/8/04 add Q35 to 12-FDTC144-EU00

<132>2006/8/04 add R524 to 1R-0000472-J200

<133>2006/8/04 add R525 to 1R-0000102-J200.

<134>2006/8/04 add F23 to 1M-F006A35-F000

<135>2006/8/04 add U39 to 15-TPS2055-0000.

<136>2006/8/04 add U40 to 15-MAX4798-0000.

<137>2006/8/04 add R526,R527 to 1R-0000109-J200.

<138>2006/8/04 del R521,U34.

<139>2006/8/04 Change CN12,CN16 to 1N-0004000-FEG0.

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		CPBG - R&D Division	
History			
Doc No	Document Name		Rev
MS60-1-01 (MBX-159)			1.0
Date	Monday, October 02, 2006		Sheet 56 of 56