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BOM configuration

SKU	Stuff	No stuff
NB8M-256MB-Samsung	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVH_
NB8M-256MB-Qimonda	NV_,NVNB8M_,NV128bit_,NV16M_,NVQ_,NVQ/S_	NC_*,NVNB8P_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8M-256MB-Hynix	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVQ/S_
NB8M-128MB-Samsung	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVH_
NB8M-128MB-Qimonda	NV_,NVNB8M_,NV64bit_,NV16M_,NVQ_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVH/S_,NVH_
NB8M-128MB-Hynix	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVQ/S_
NB8M-64MB-Hynix	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV128bit_,NV16M_,NVQ/S_,NVQ_
NB8M-64MB-Samsung	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVH_
NB8P-256MB-Samsung	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVH_
NB8P-256MB-Qimonda	NV_,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVQ/S_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8P-256MB-Hynix	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVQ/S_
GM965/GL960	CA_	No CA_

Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request

"no CA_" means all of other prefix including the "NC_" prefix.

Project Code & Schematics Subject: MS91 Main Board

PCB P/N:

1P-0076100-8010(FUBAI)
1P-0076500-8010(HANNSTAR)
1P-0076200-8010(NAN YA)

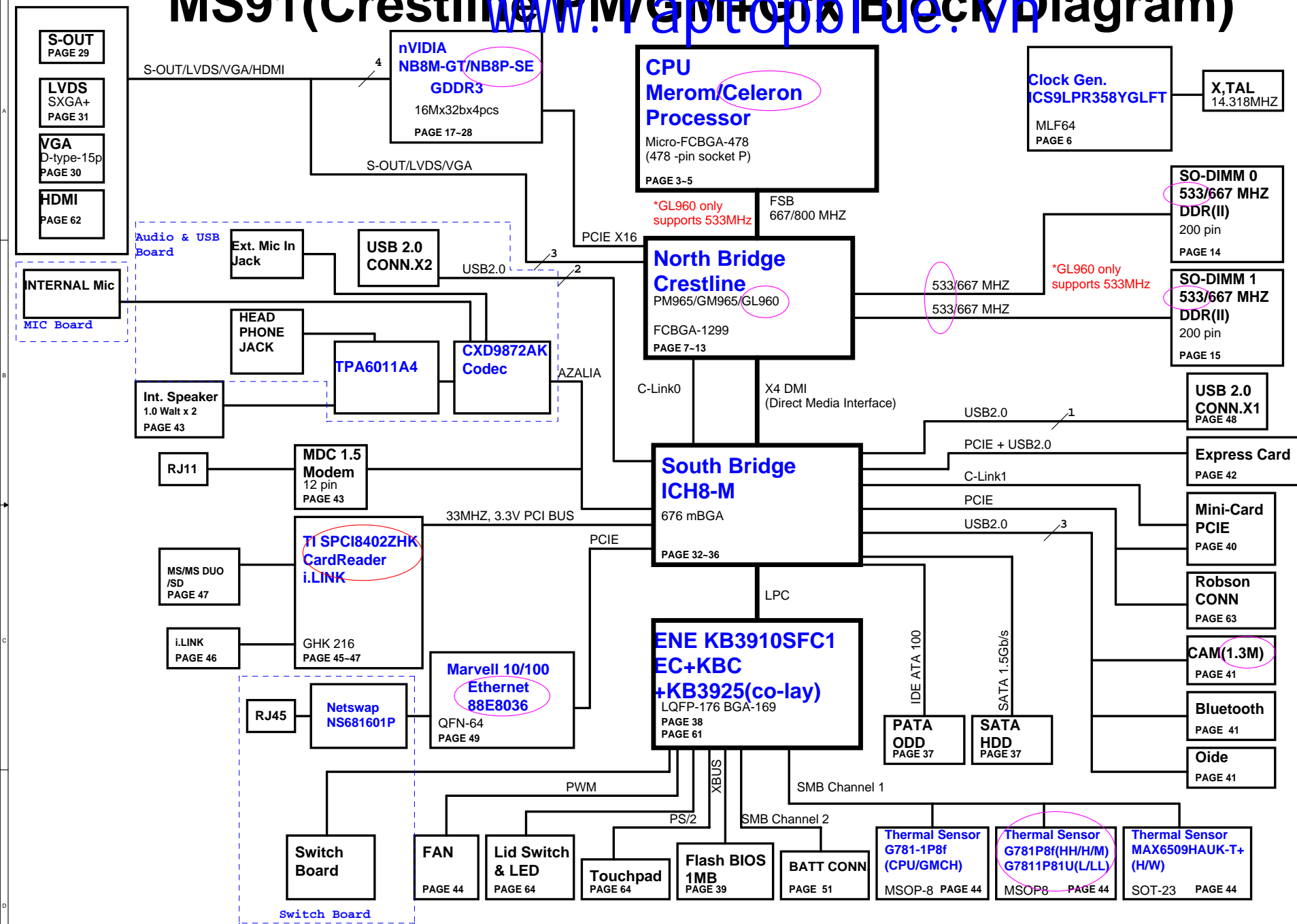
The "NC_*" include "NC_CA_"and "NC_NV*", the are prefix which comes from MS90 schematic,it means NC also, but if the component is needed again, "NC_CA_" is only for Low module only and "NC_NV*" only for HH/H/M module only.the rule is help to remind this.

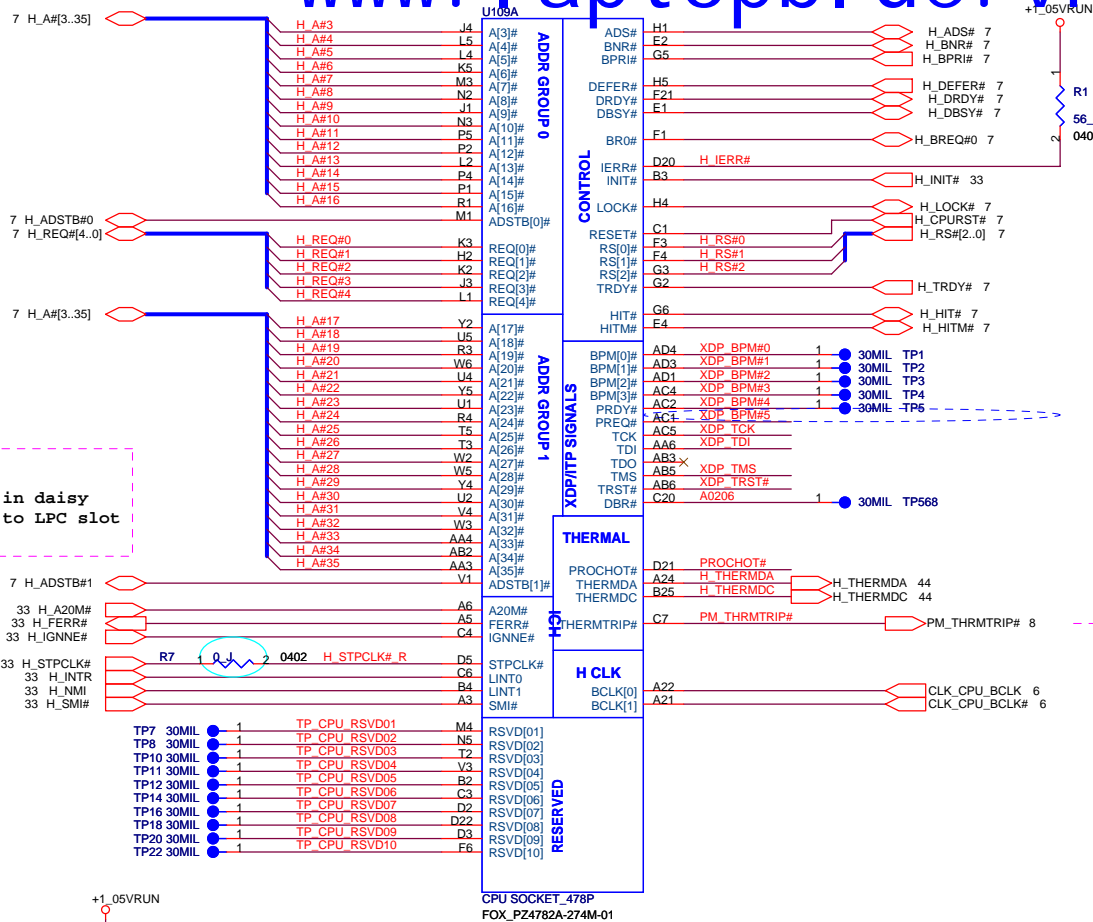
P. Leader	Check by	Design by

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

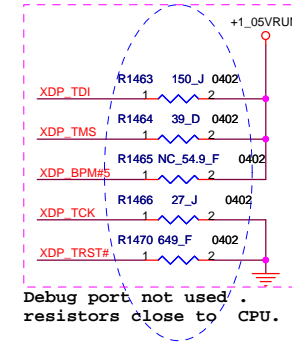
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Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 1	of 66

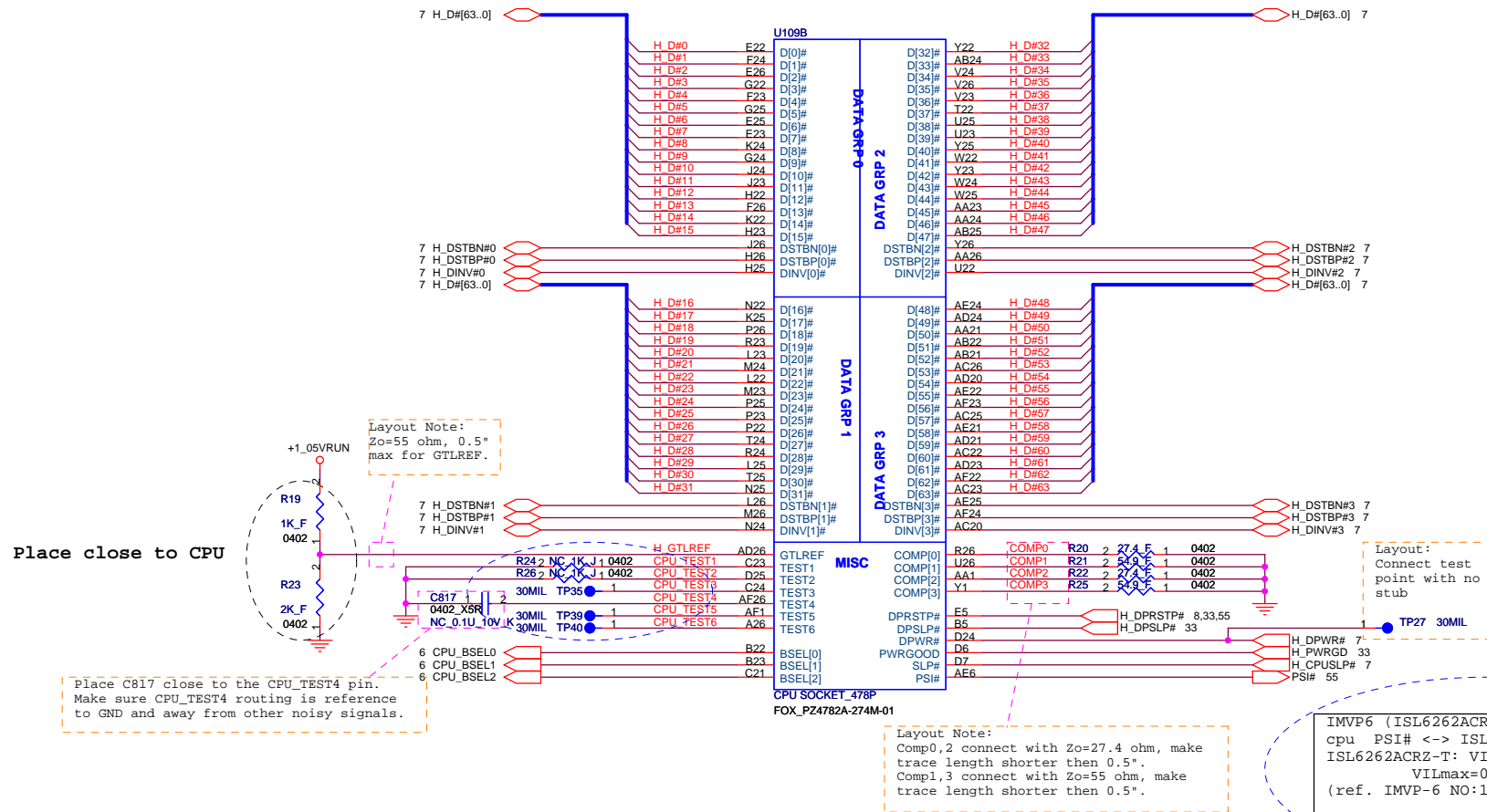
MS91 (Crestline PM/GM+Gfx Block Diagram)

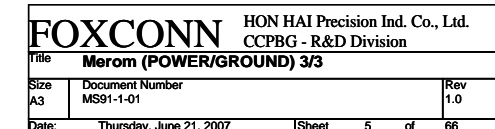


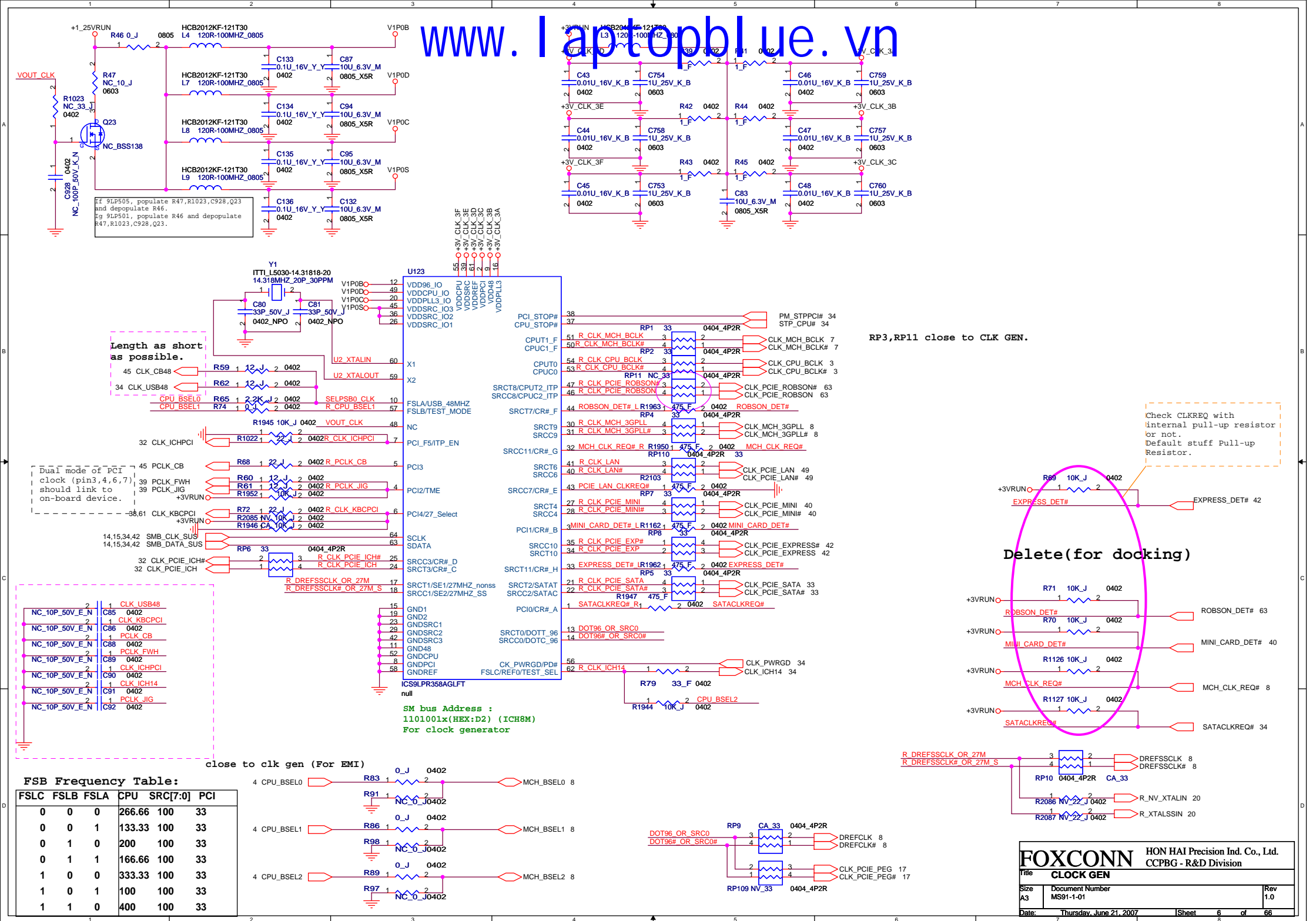


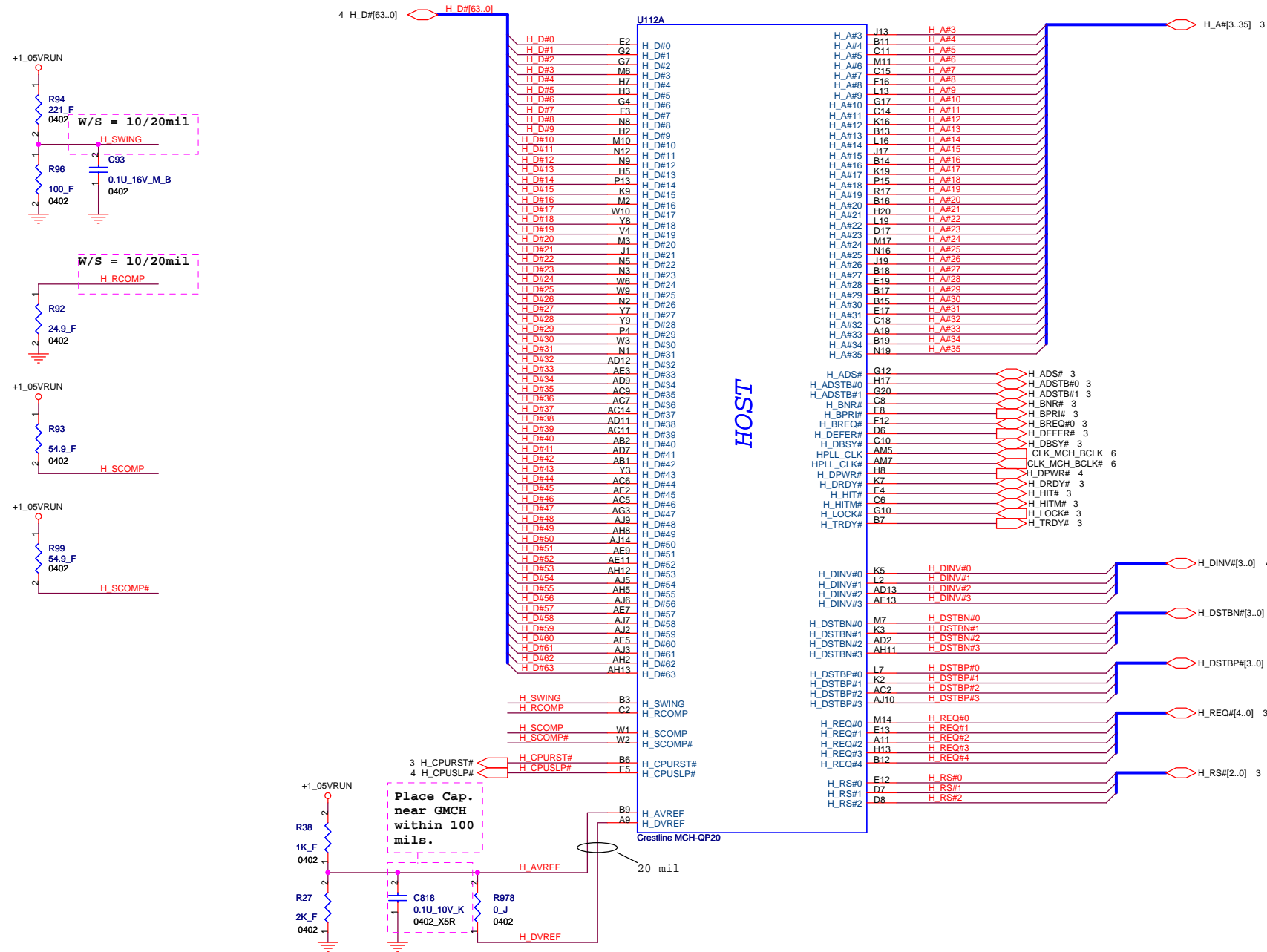
Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

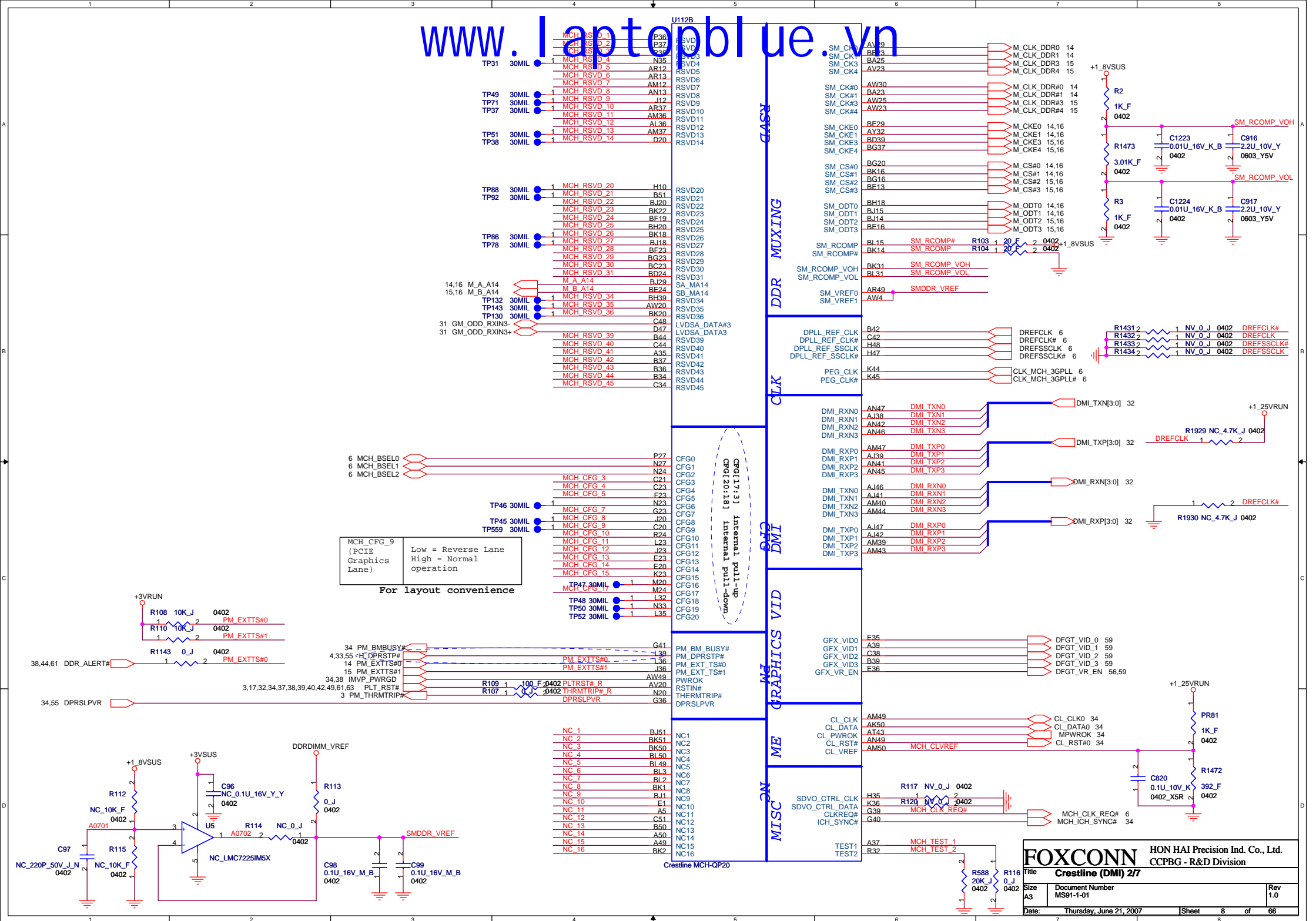


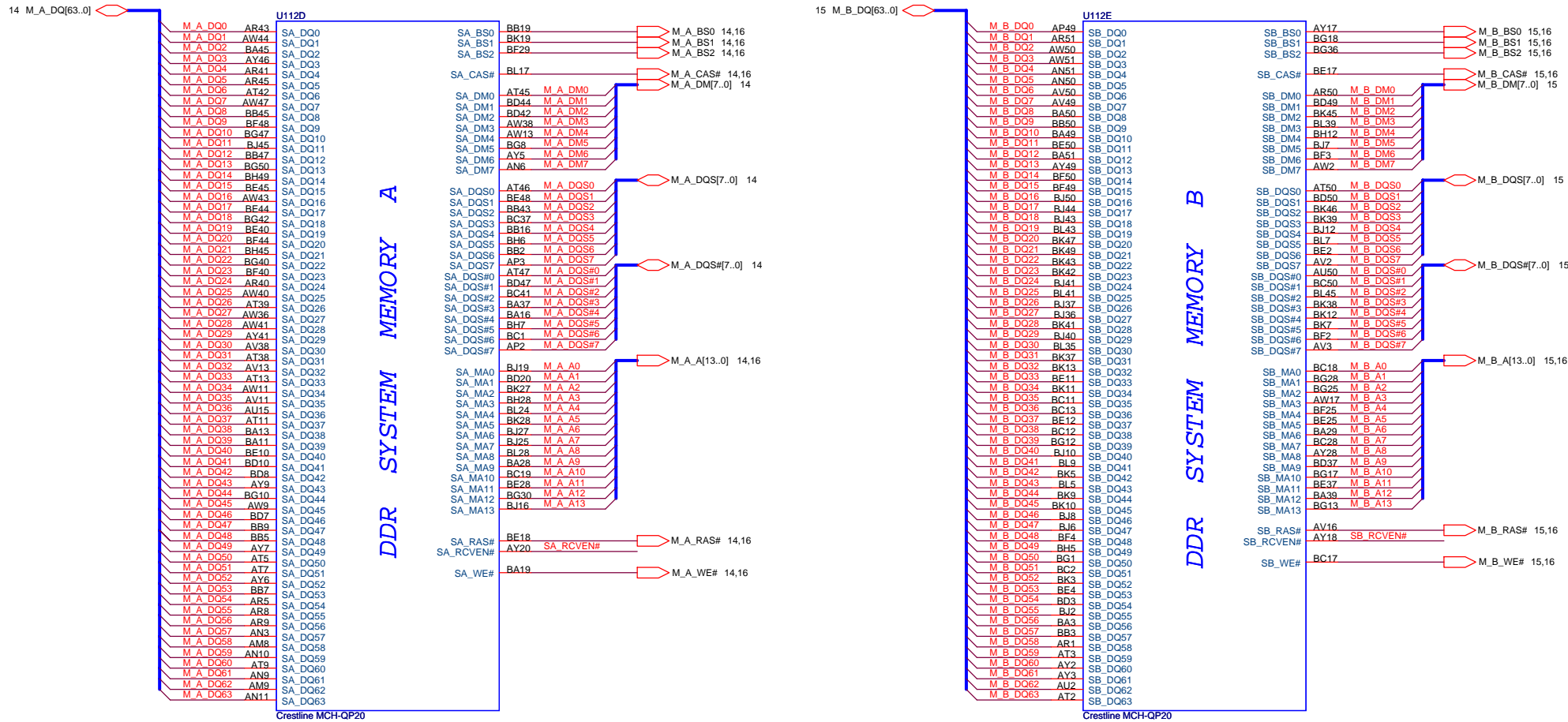


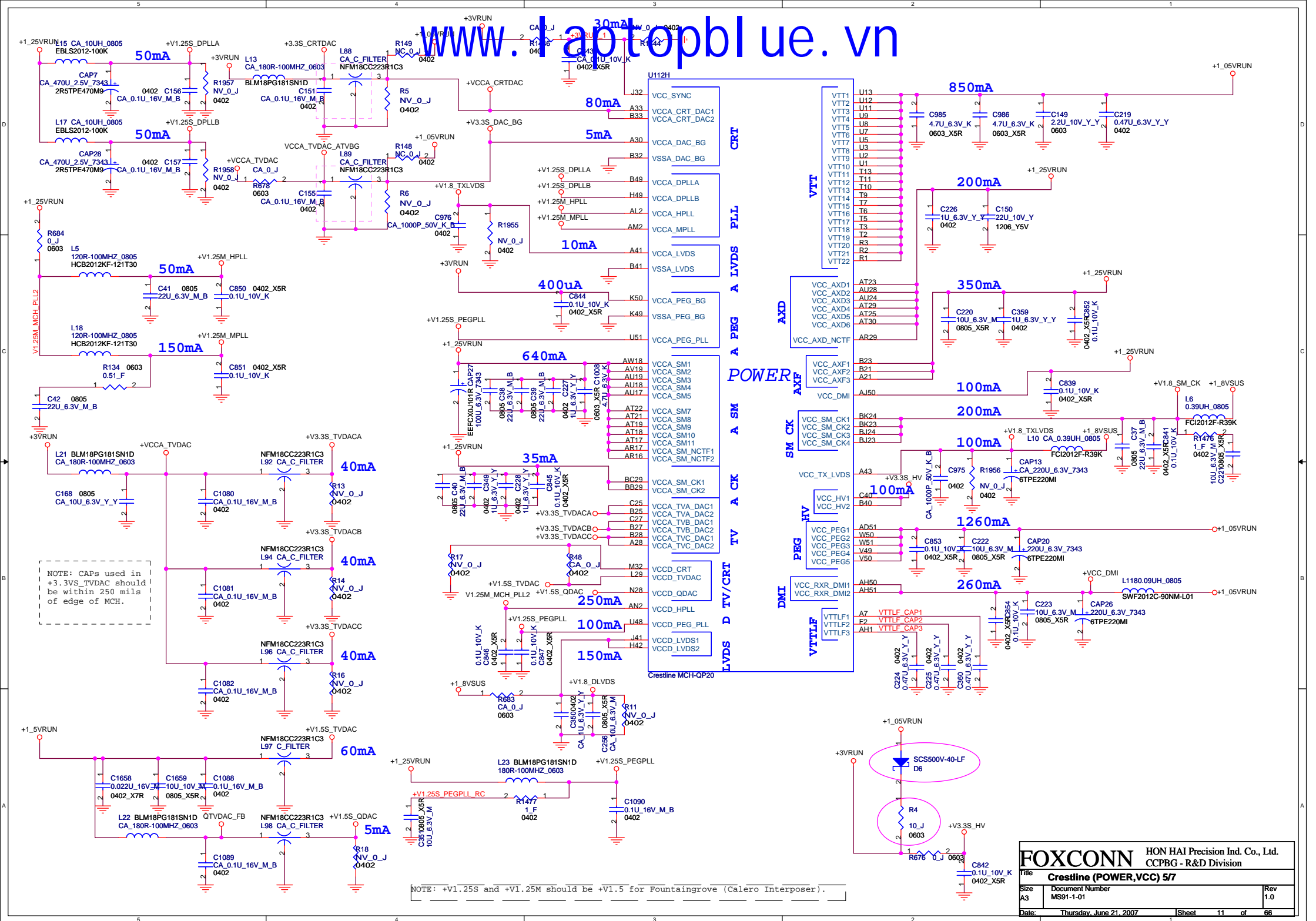




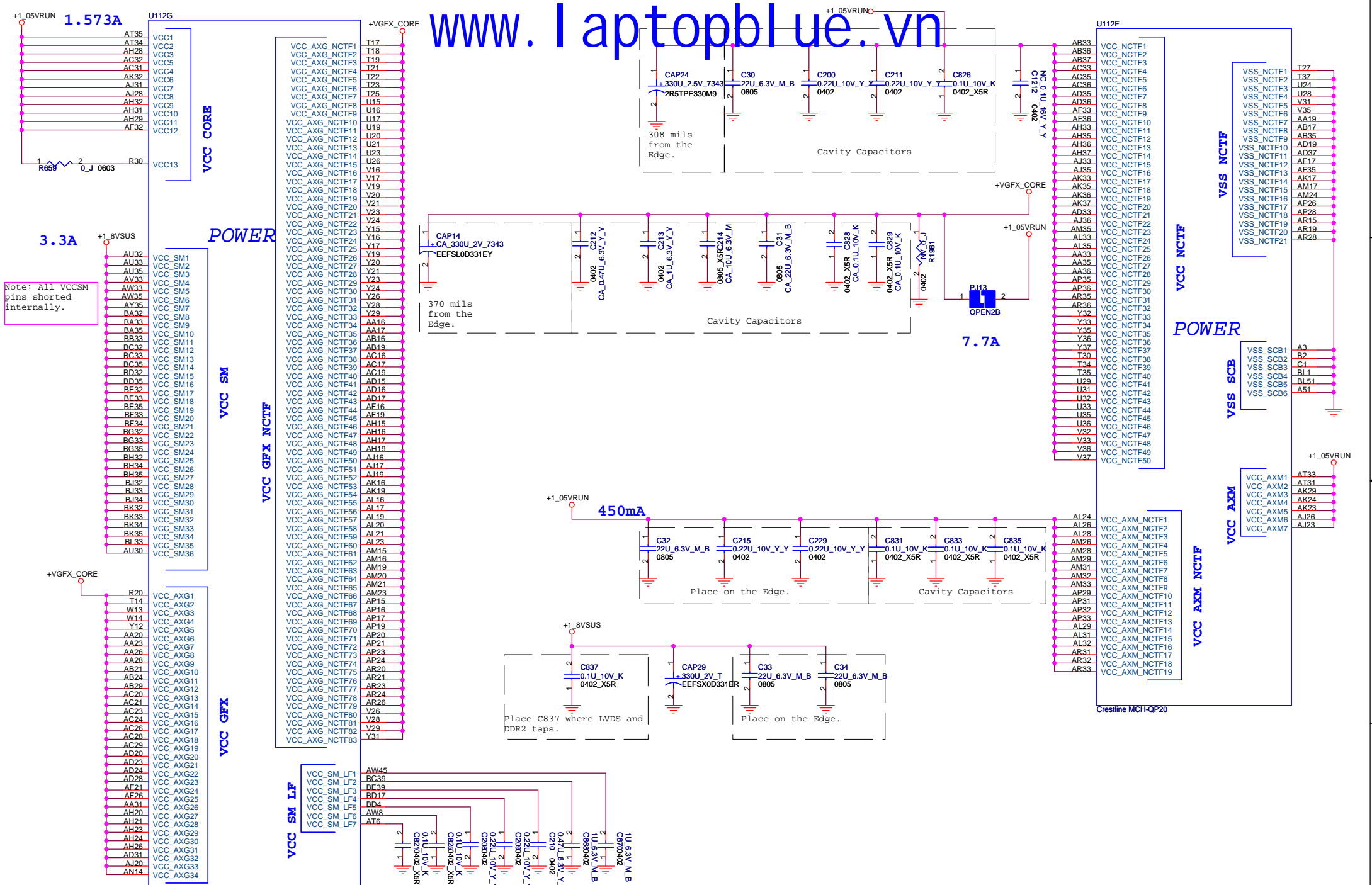


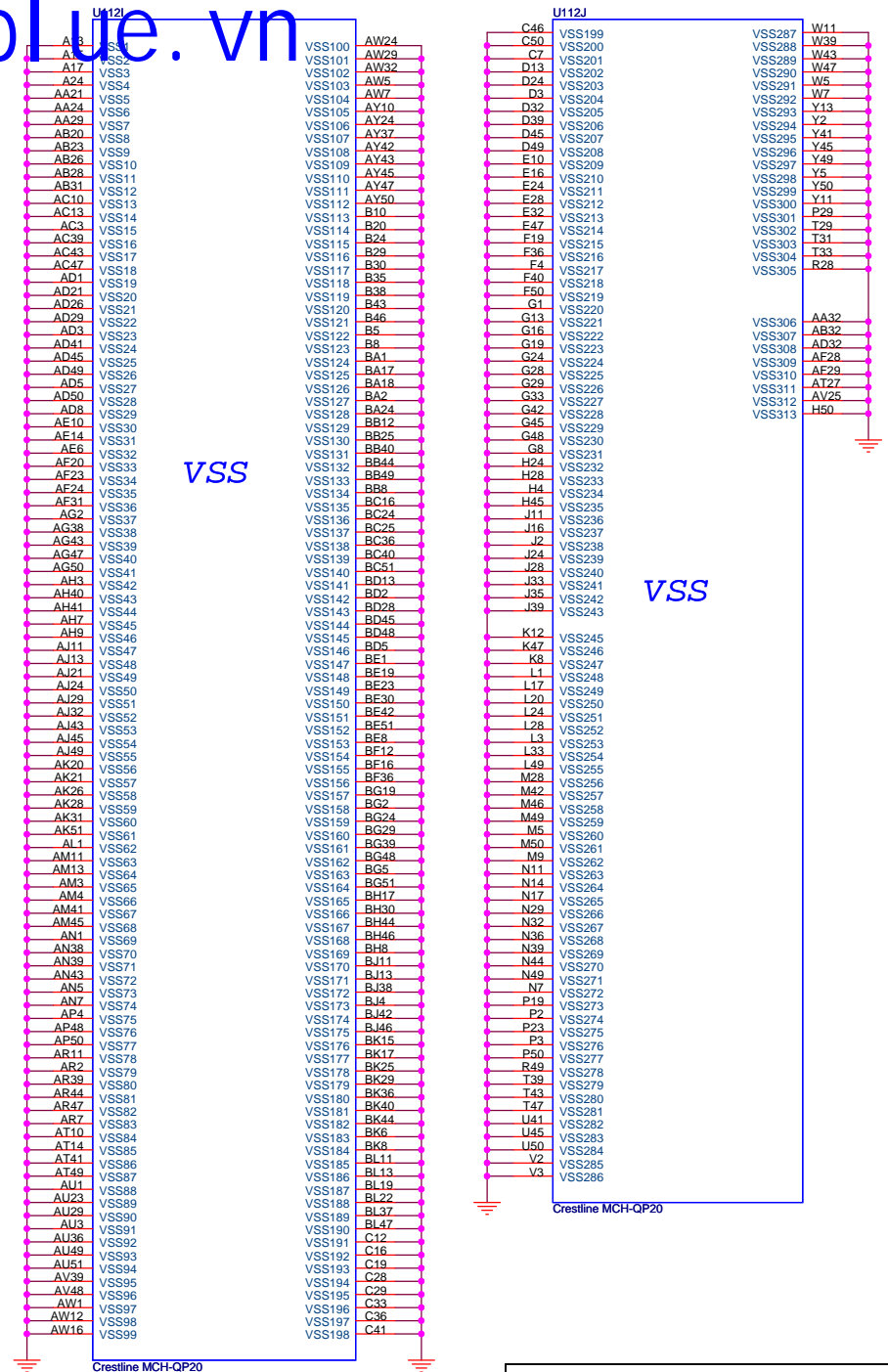




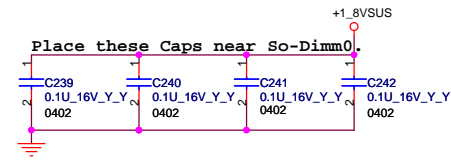
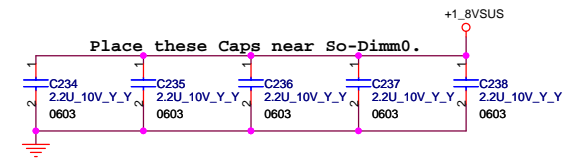
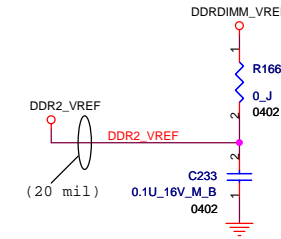
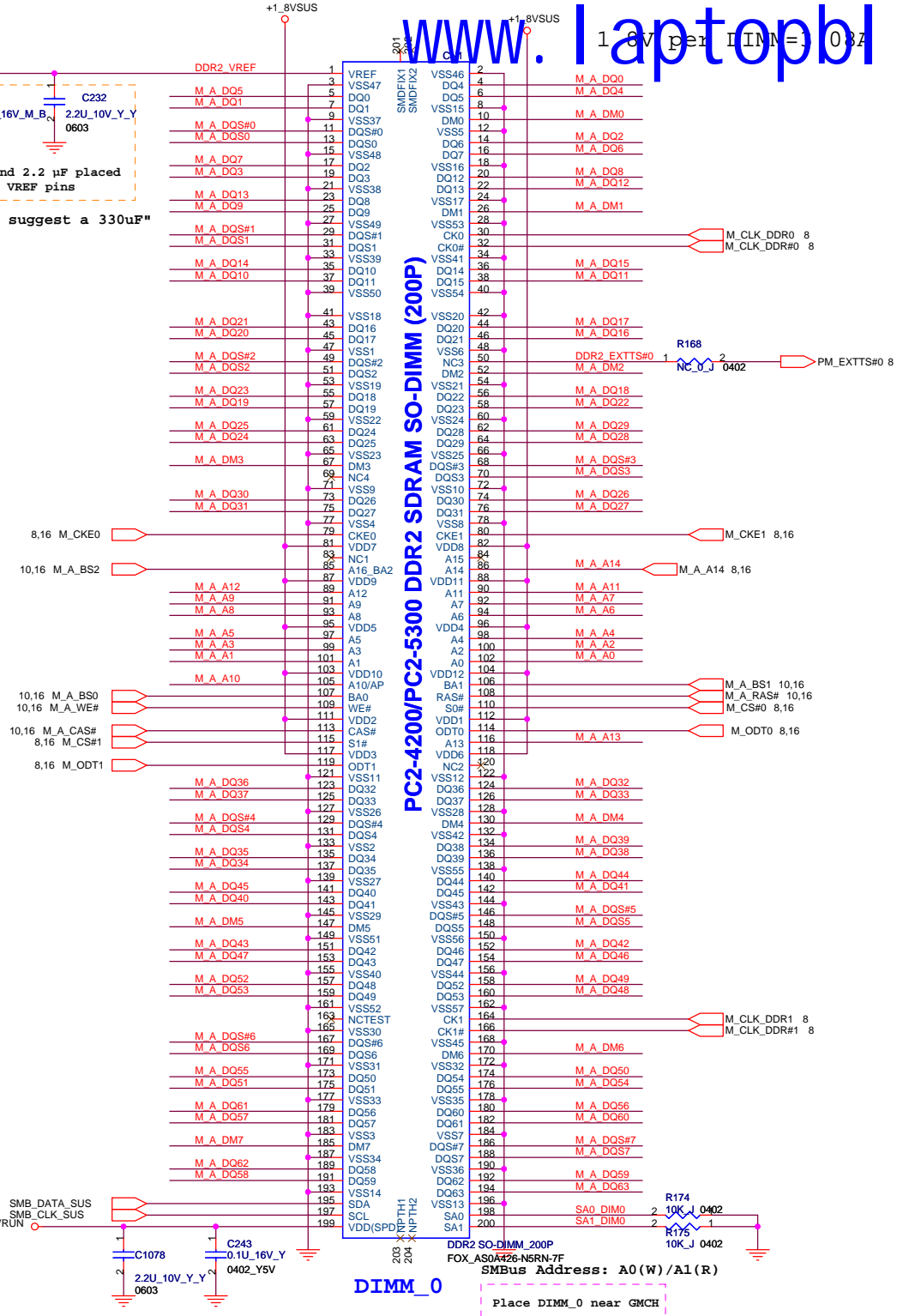
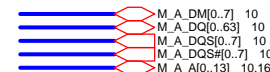
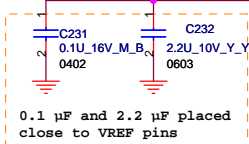


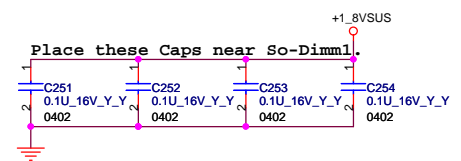
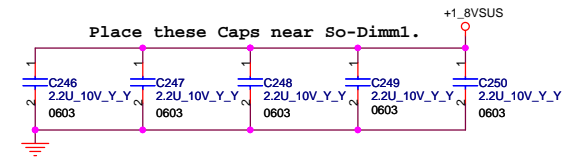
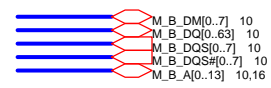
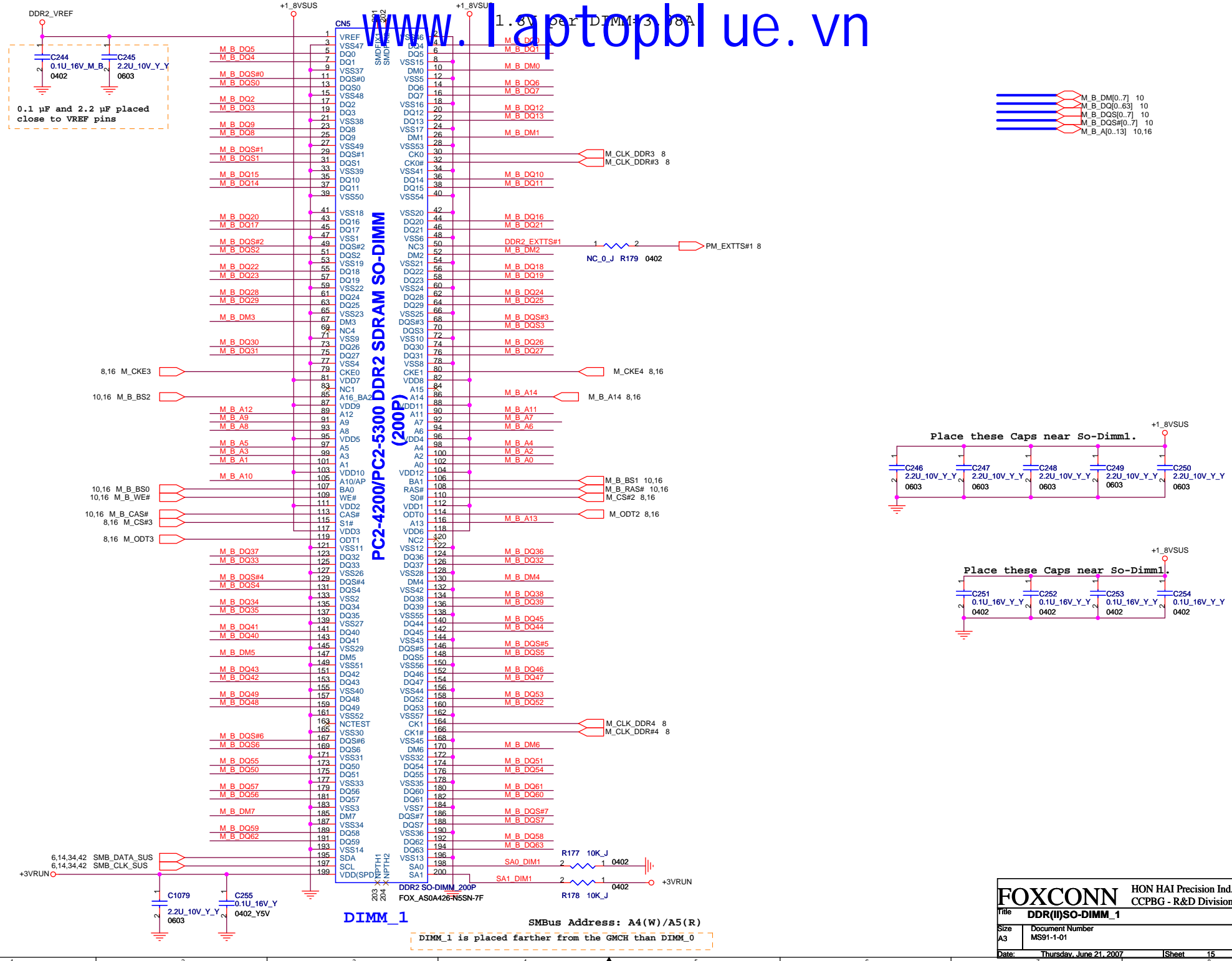
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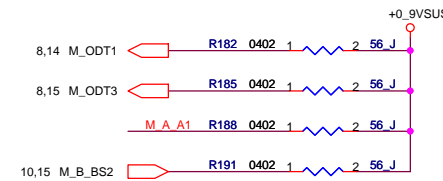
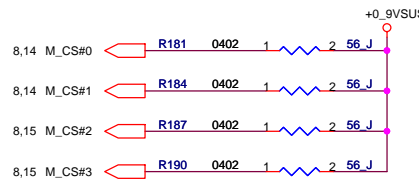
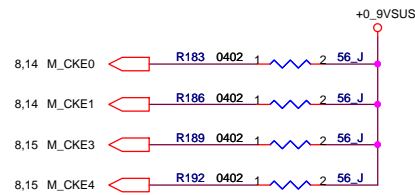
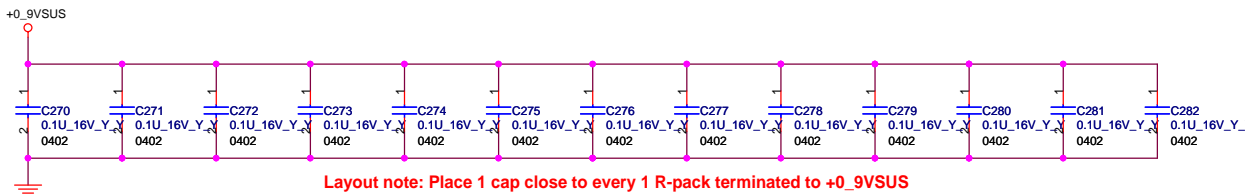
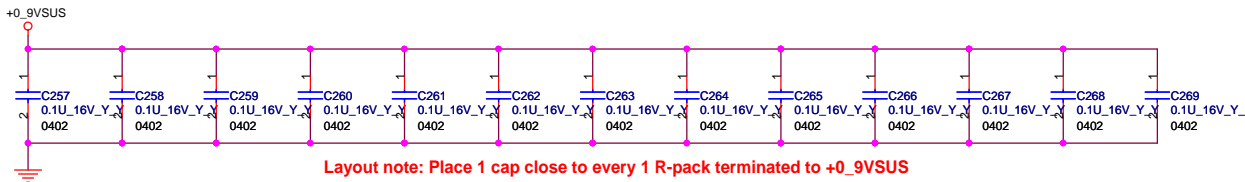
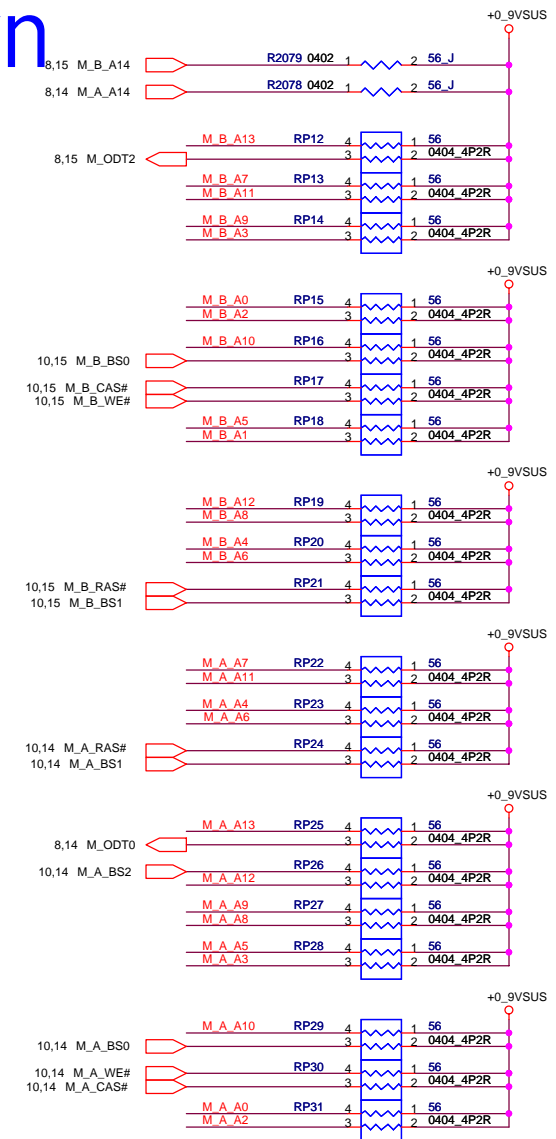


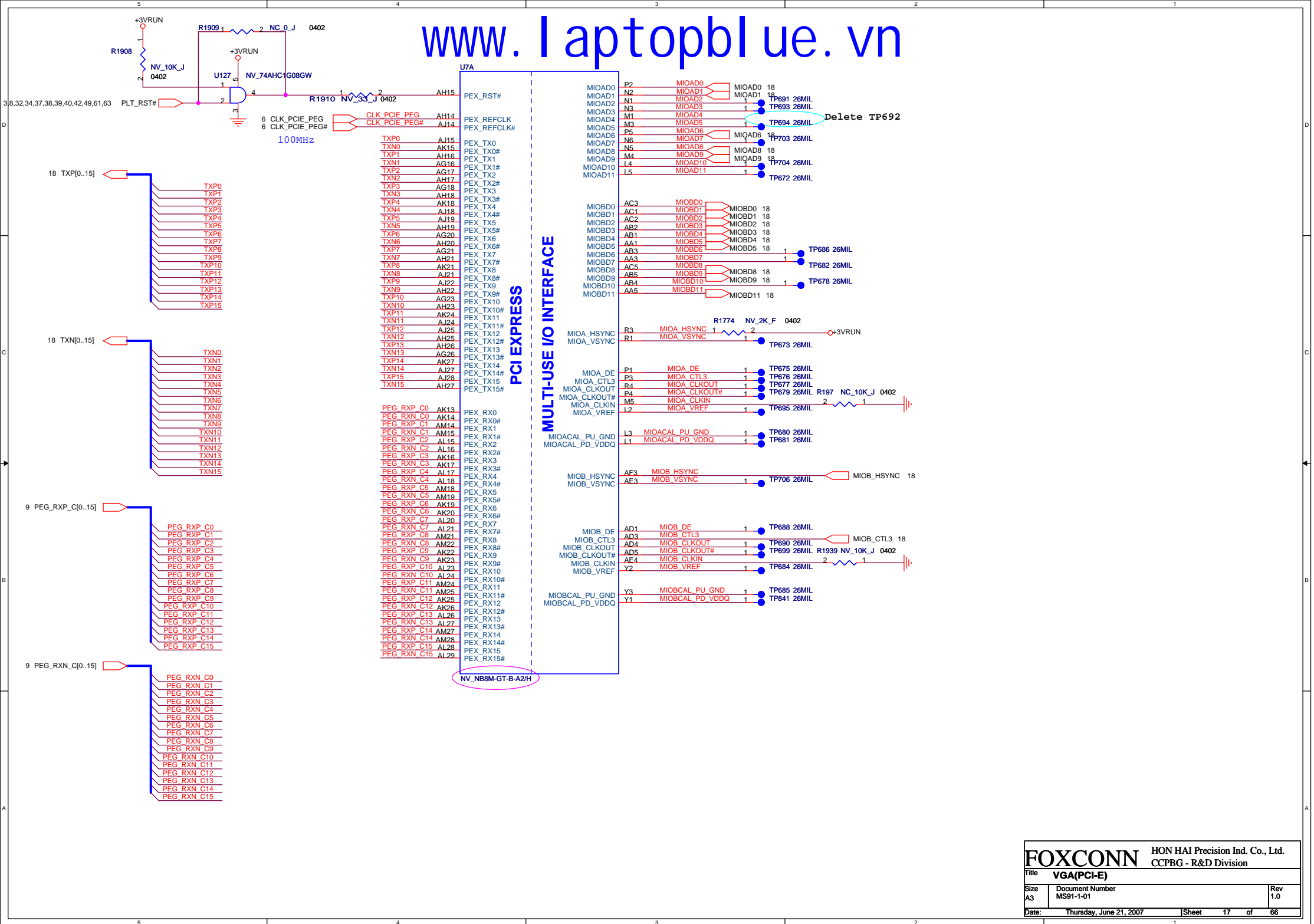


"Intel check list suggest a 330uF"



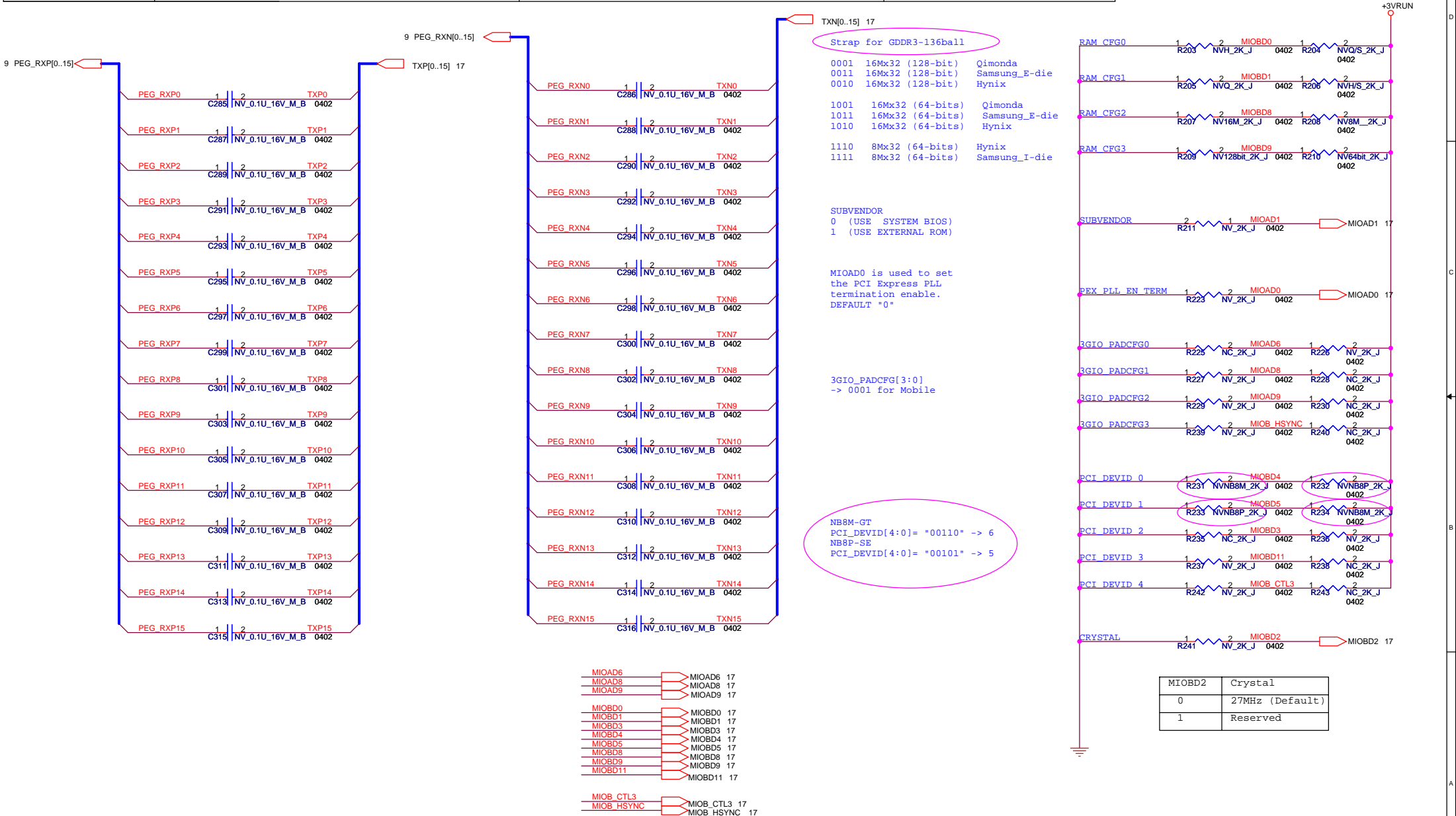




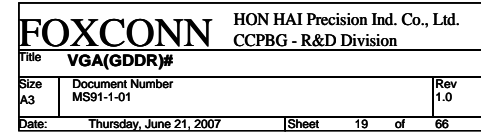


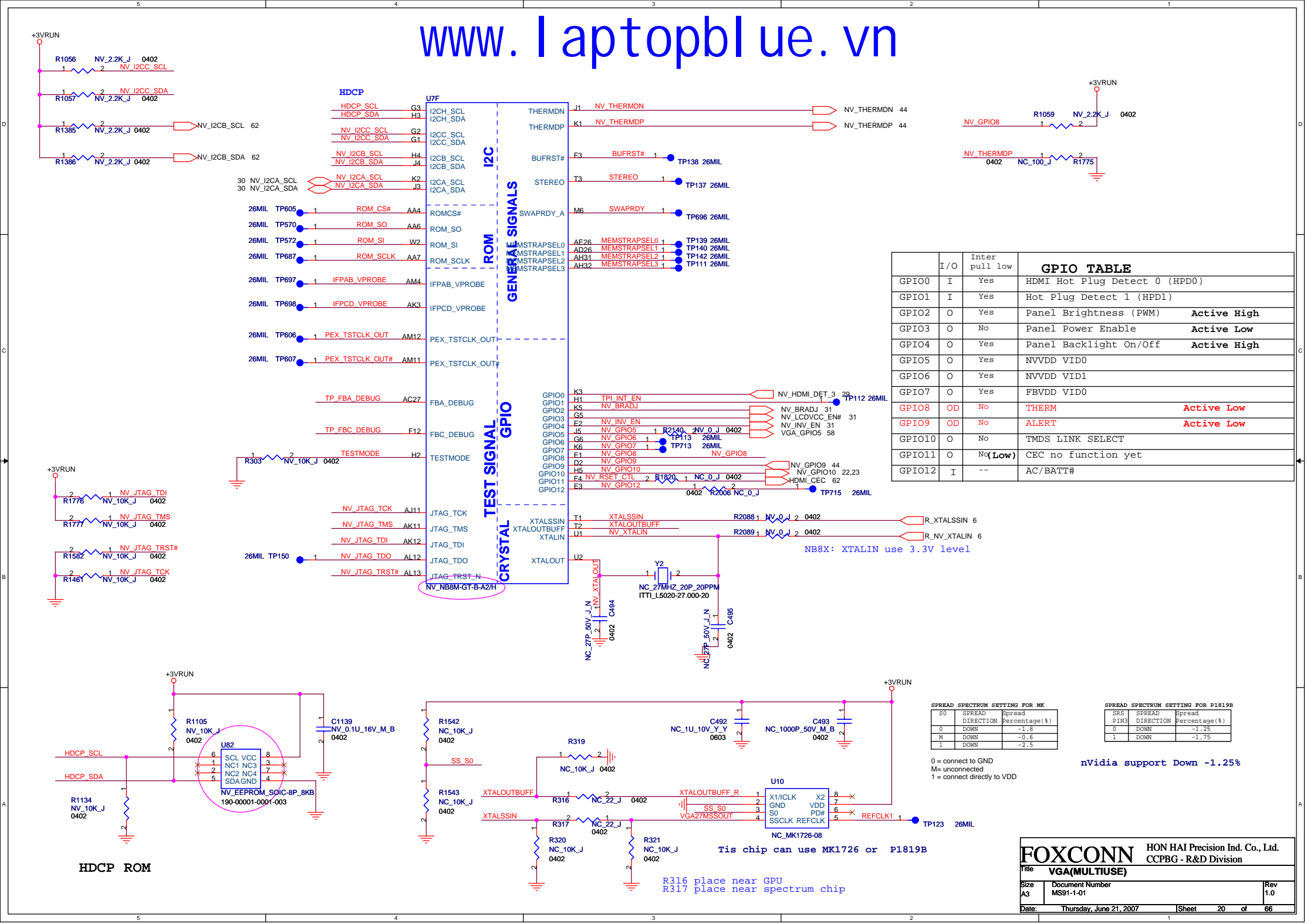
SKU	HH		H		M	
Vender	Hynix	Qimonda	Samsung	Qimonda	Samsung	Hynix
Vendor PN	HY5RS123235BFP-14	HYB18H512321BF-14	K4J523240-CE-14	HYB18H512321BF-14	K4J523240-CE-14	HY5RS573225BFP-14
H.H PN	13-HY5RS12-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HY5RS12-3001
Configuration	NB8X with 4pcs (16Mx32) GDDR3		NB8M-GT with 2pcs (16Mx32) GDDR3		NB8M-GT with 2pcs (8Mx32) GDDR3	
LOCATION	Stuff U11,U12,U13,U14		Stuff U11,U12; No stuff U13,U14		Stuff U11,U12; No stuff U13,U14	

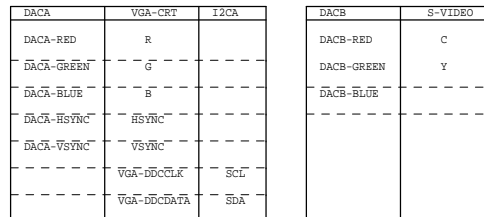
FAB: TV Mode Strap no use, remove.
(MIOAD7, MIOAD10, MIOBD6)

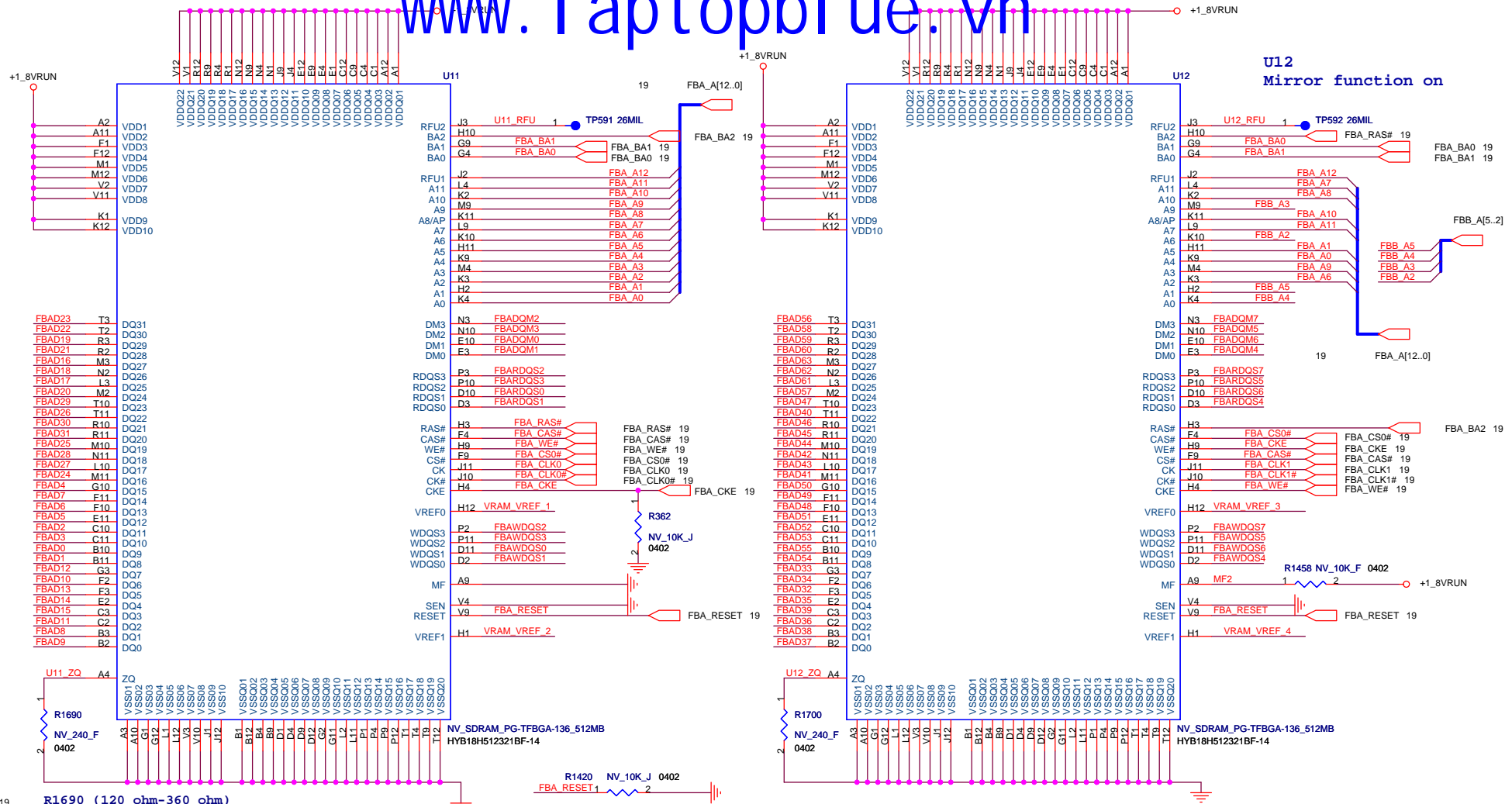


MIOBD2	Crystal
0	27MHz (Default)
1	Reserved





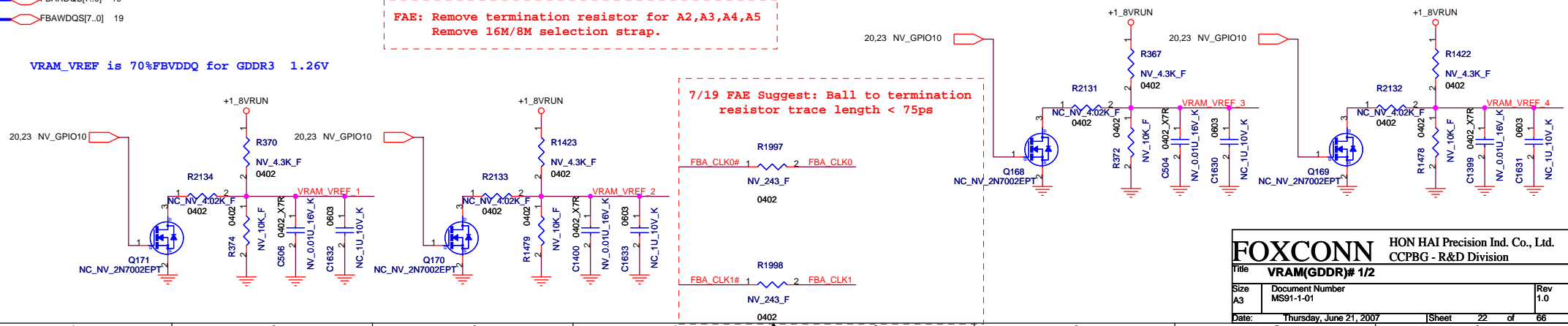


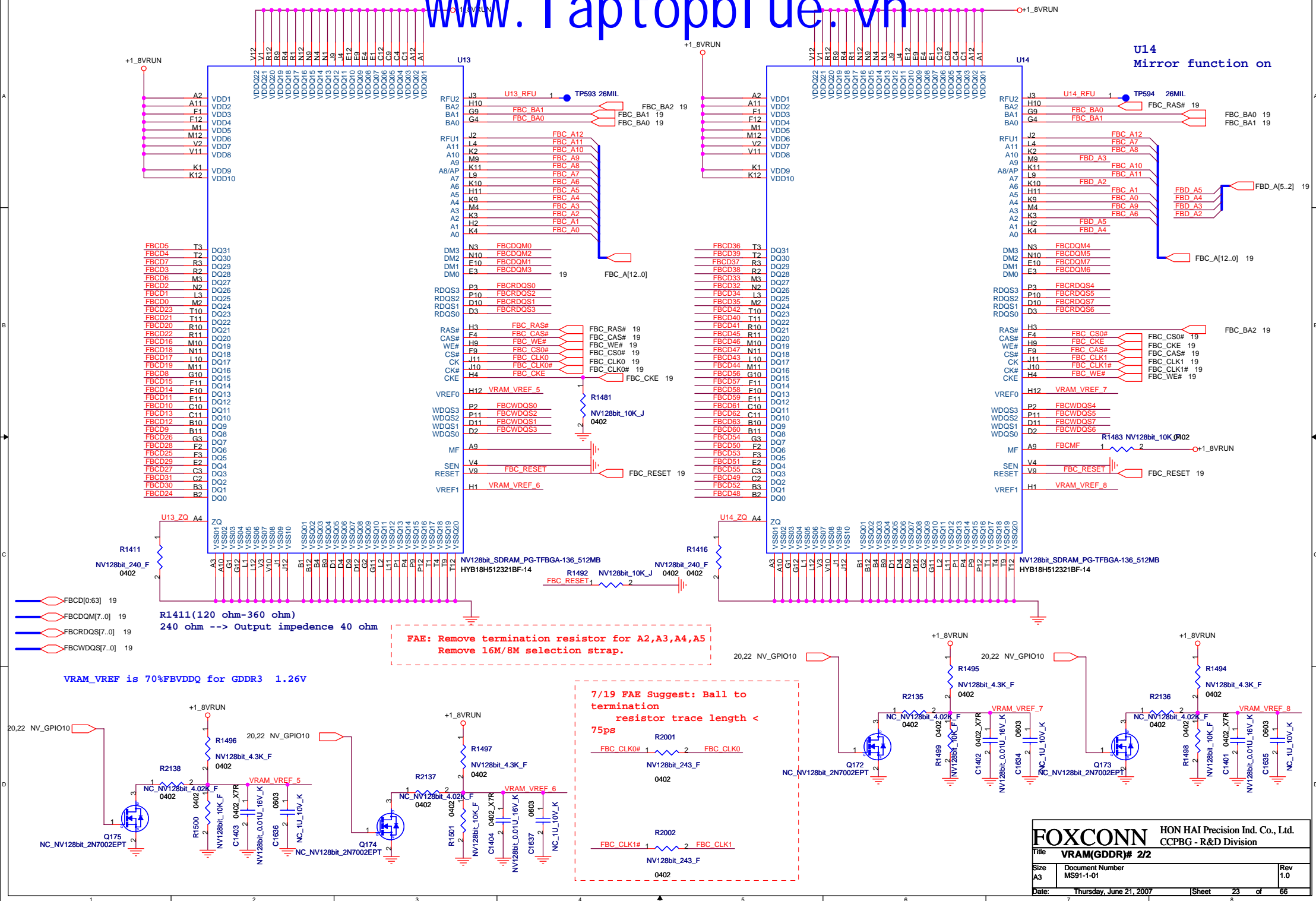


FAE: Remove termination resistor for A2,A3,A4,A5
Remove 16M/8M selection strap.

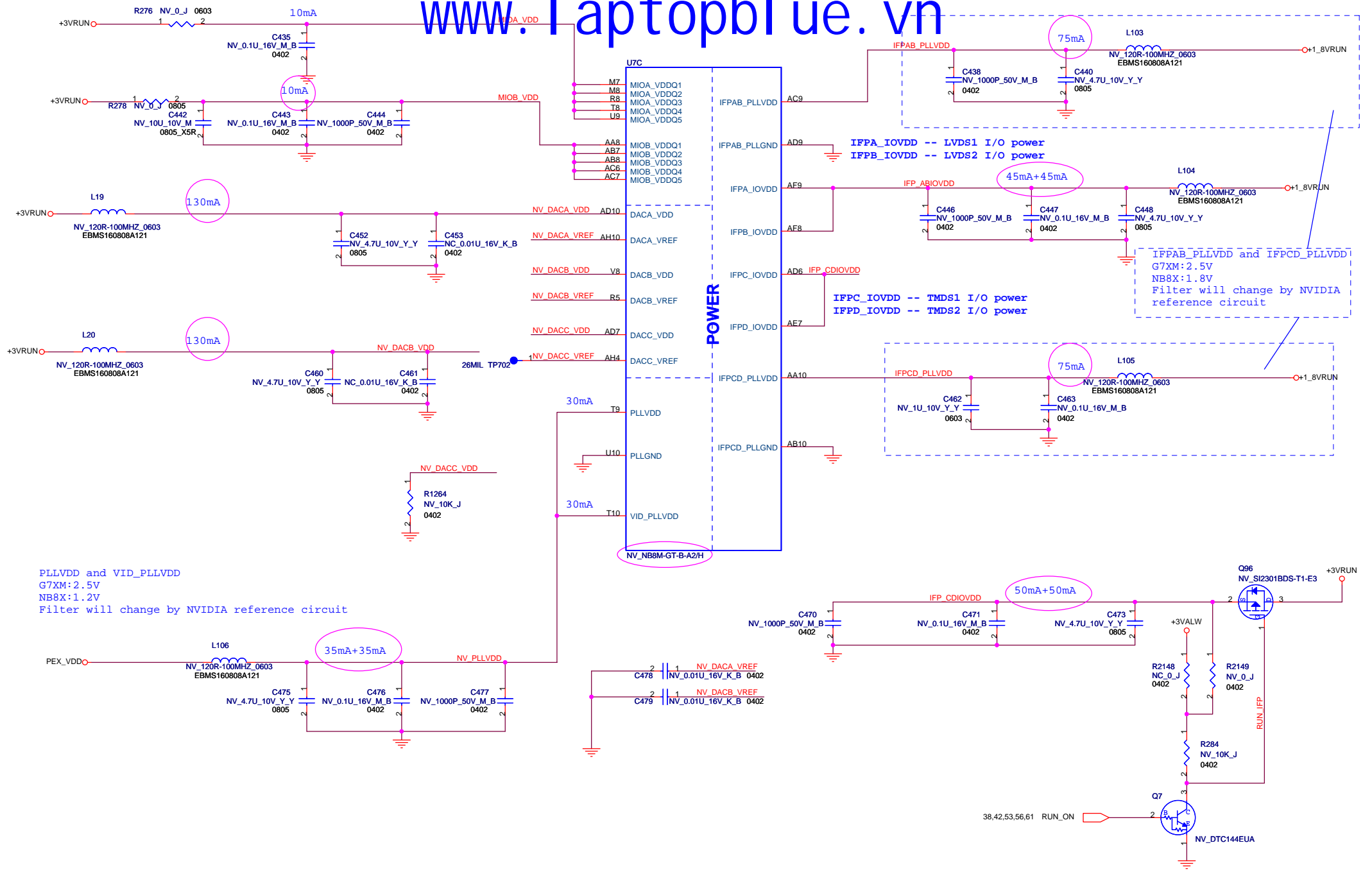
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

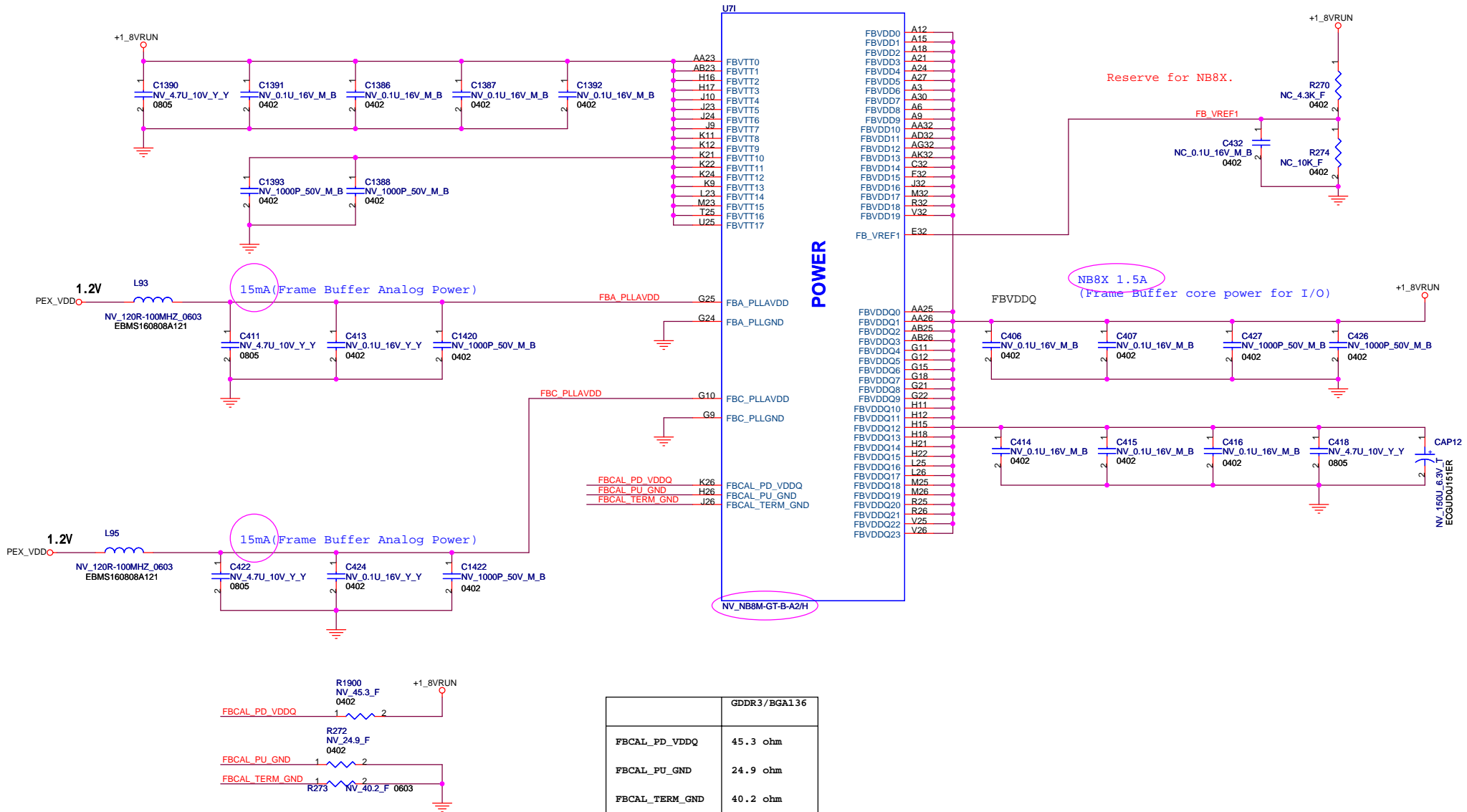
19 FAE Suggest: Ball to termination
resistor trace length < 75ps

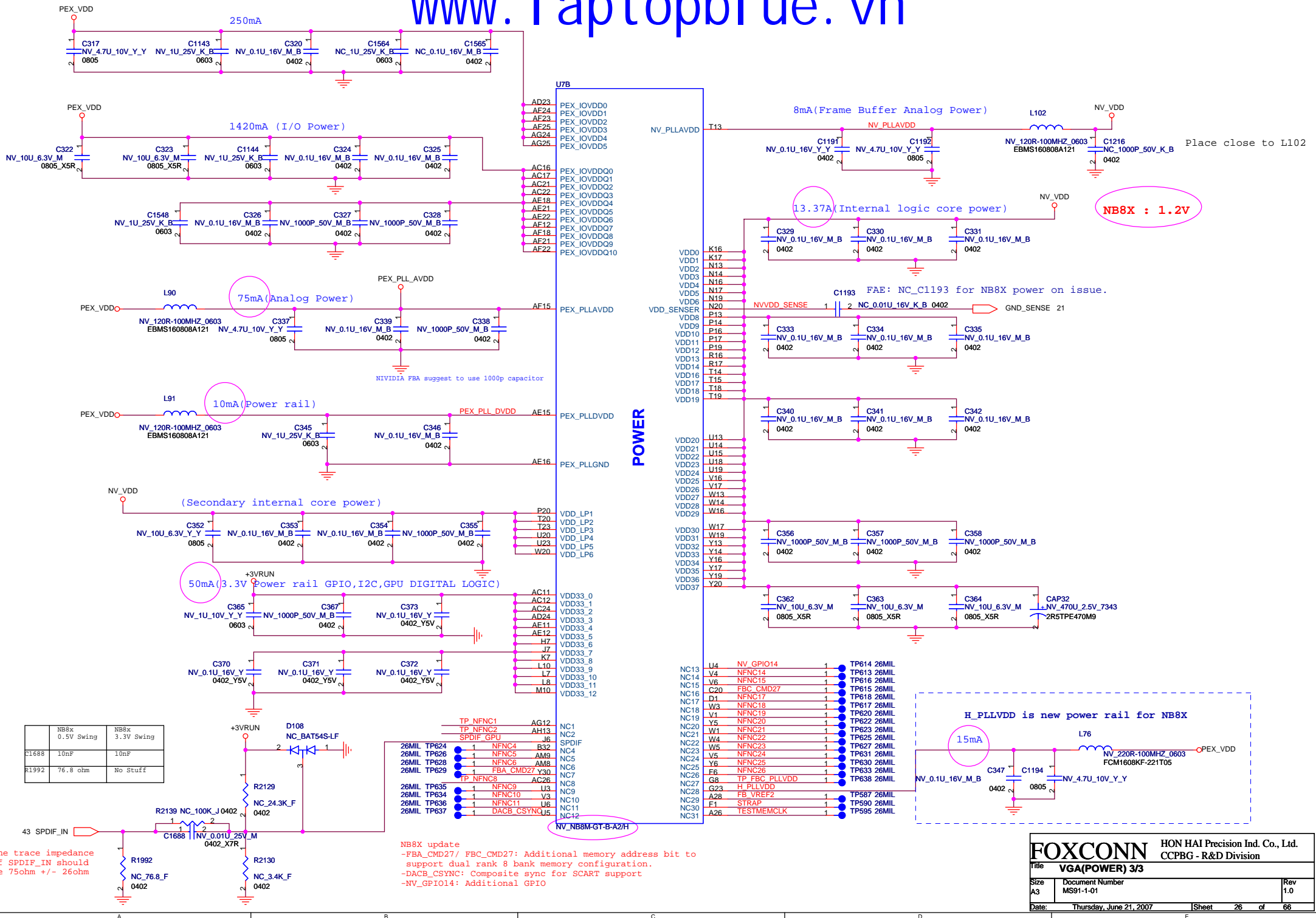




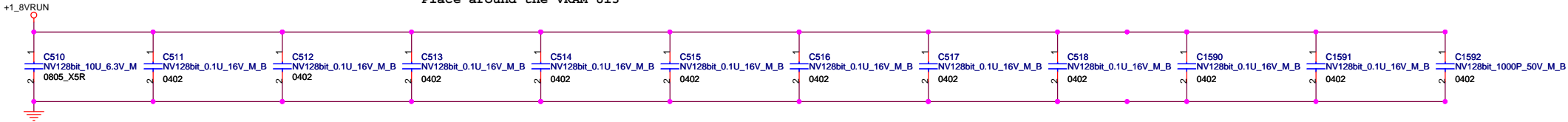
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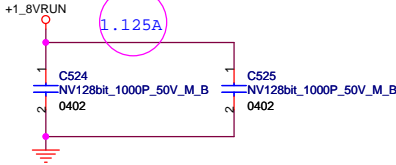




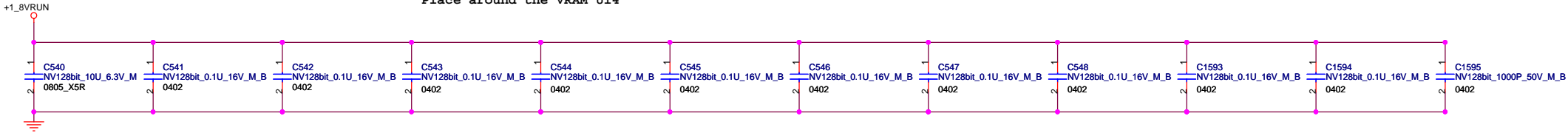
Place around the VRAM U13



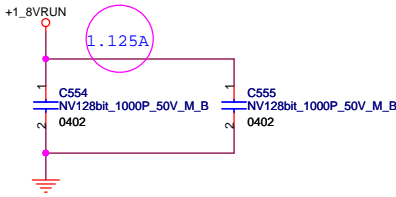
1.125A



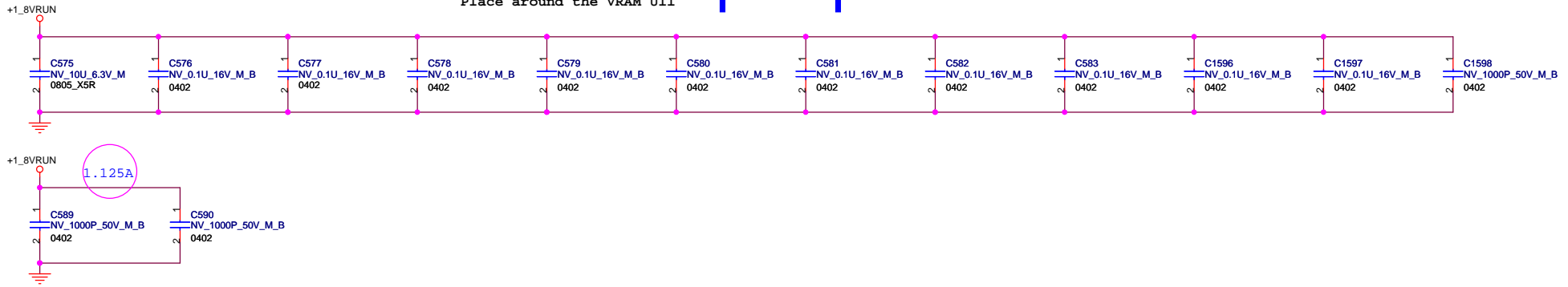
Place around the VRAM U14



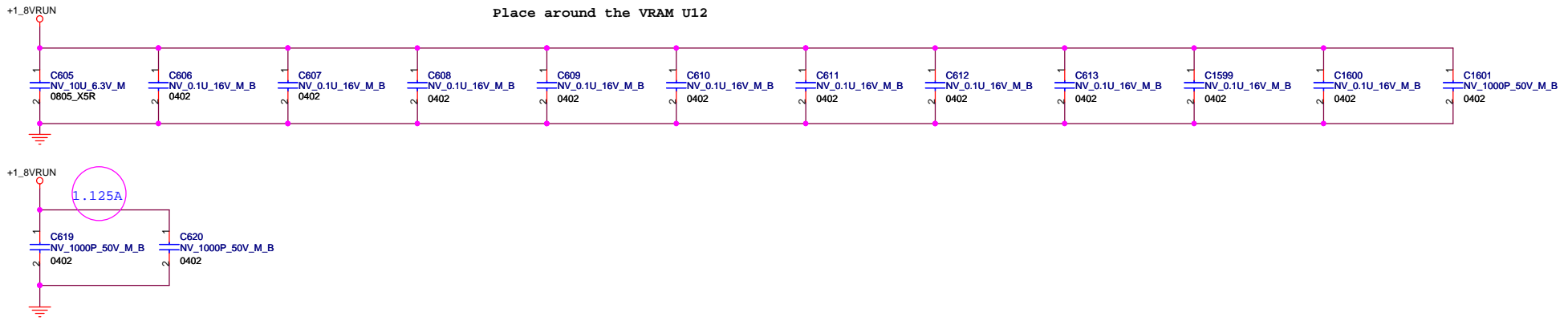
1.125A



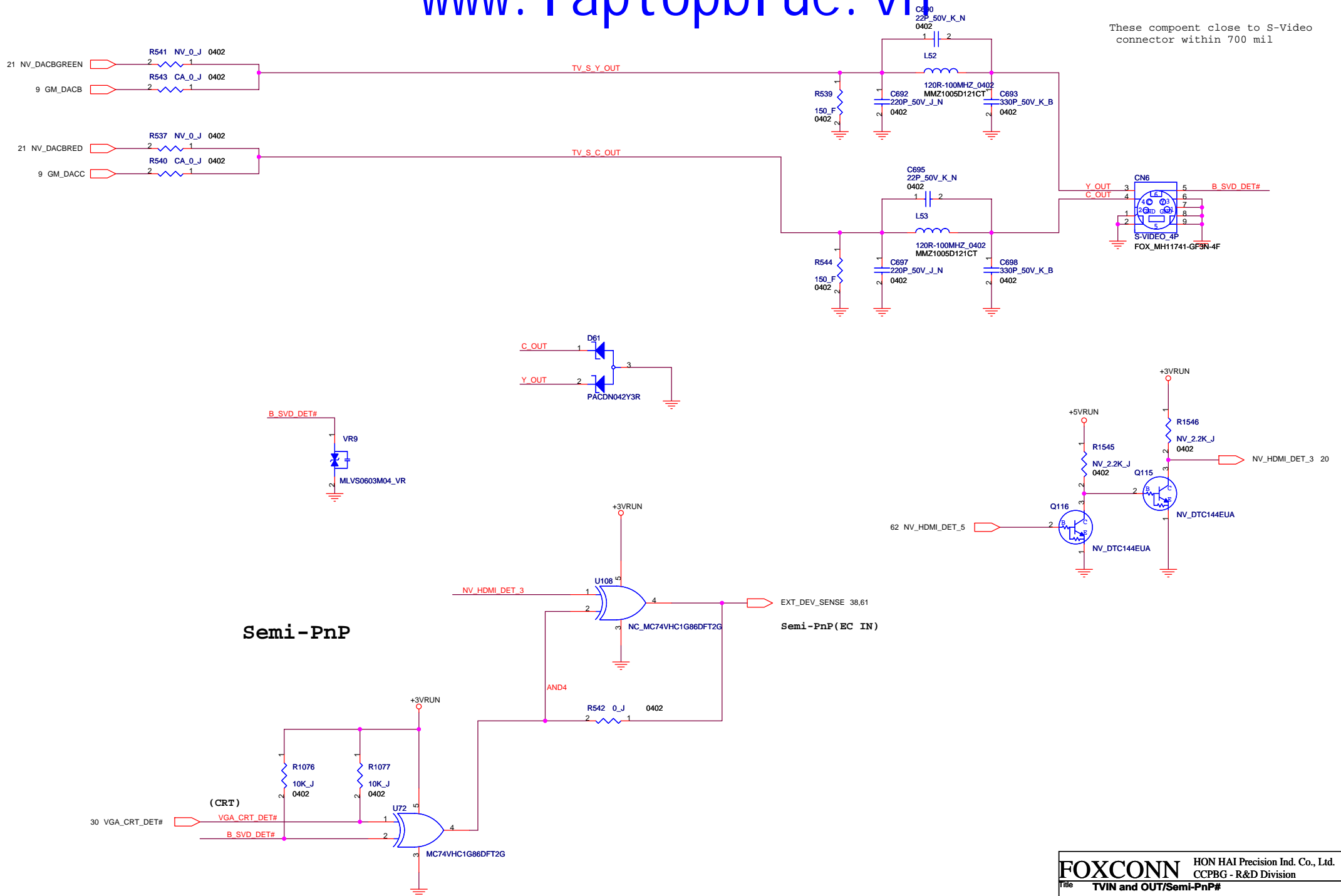
Place around the VRAM U11

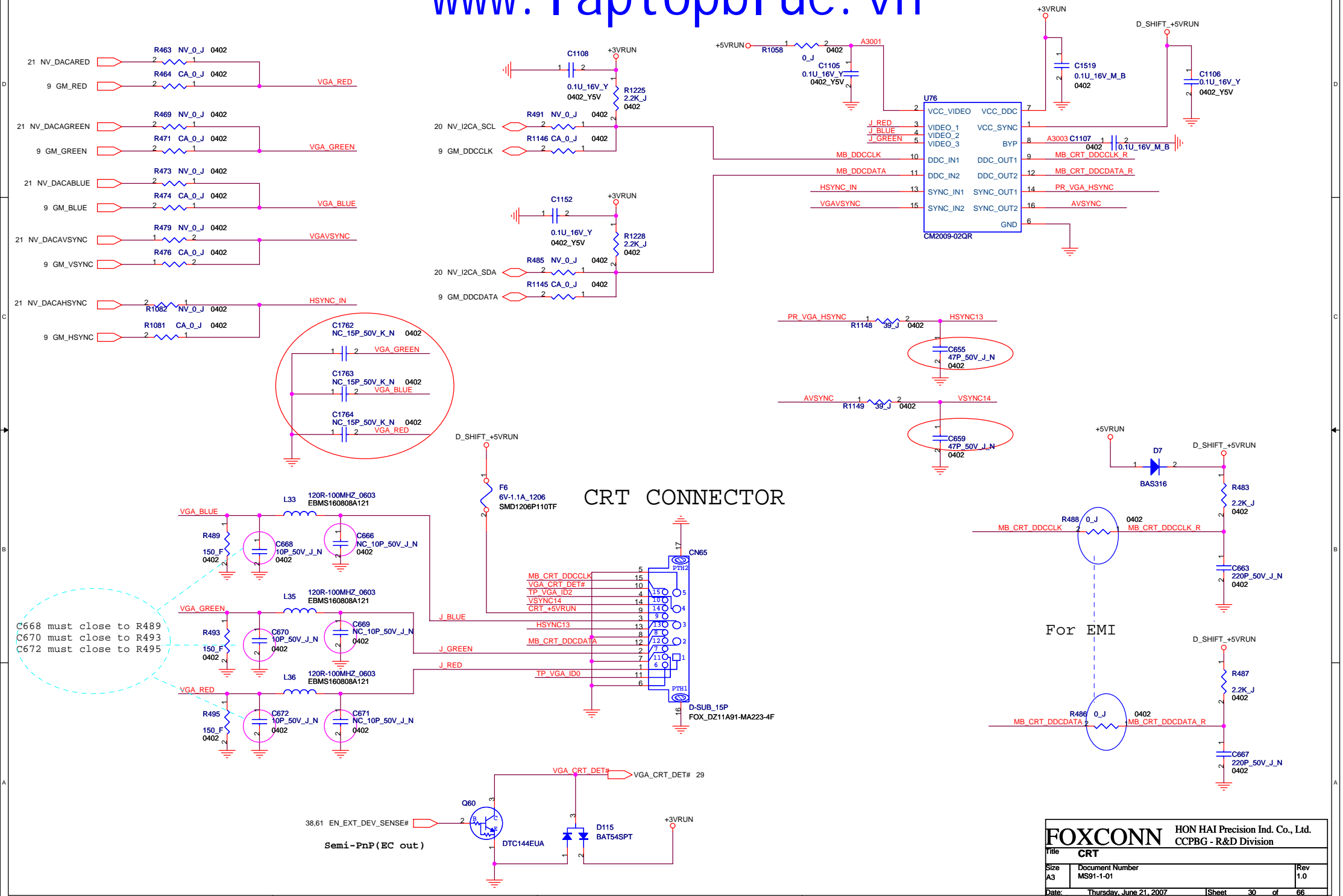


Place around the VRAM U12

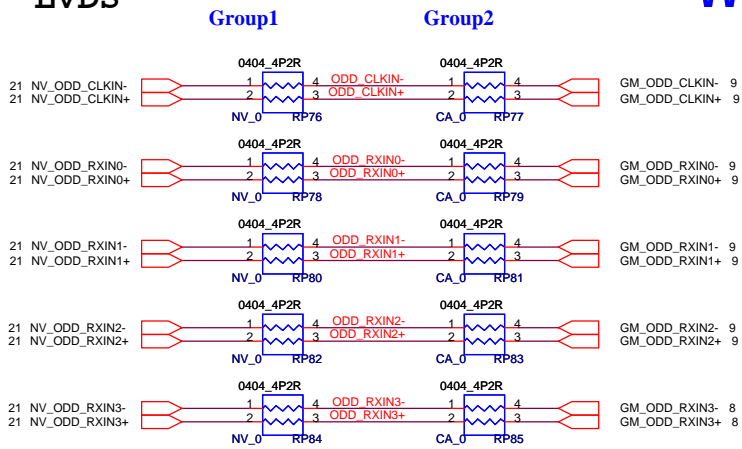


These compoent close to S-Video
connector within 700 mil

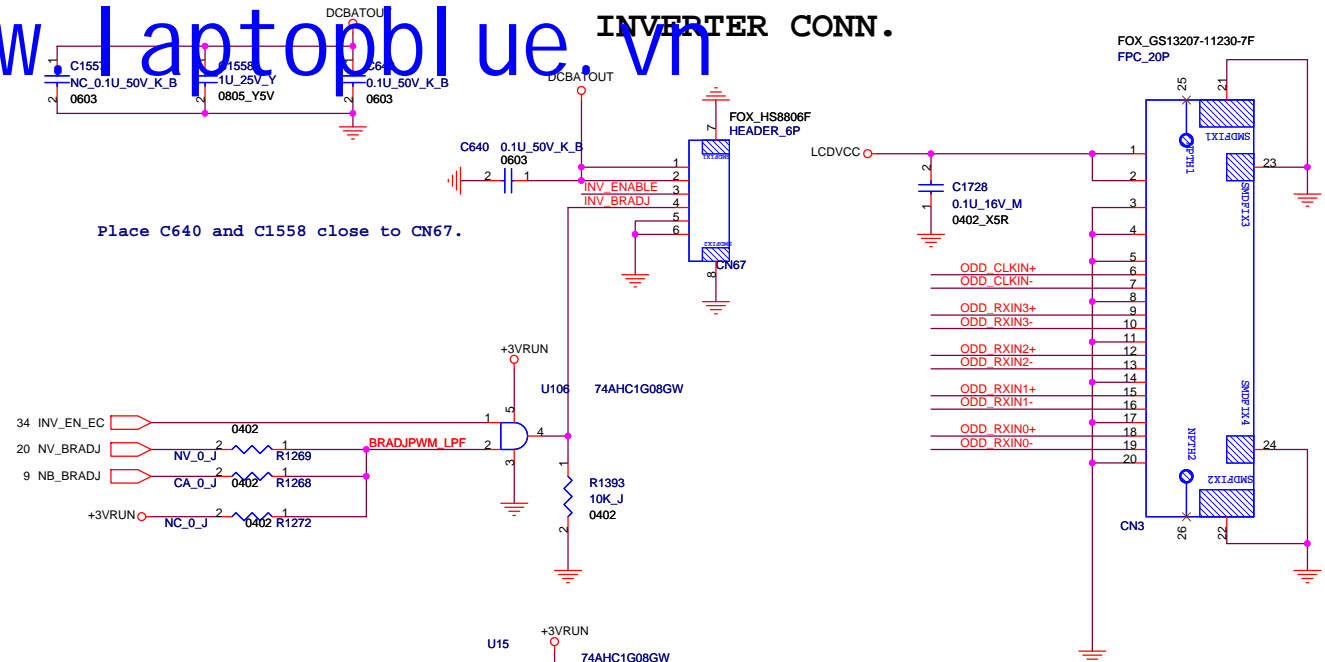




Group1,Group2 should be close

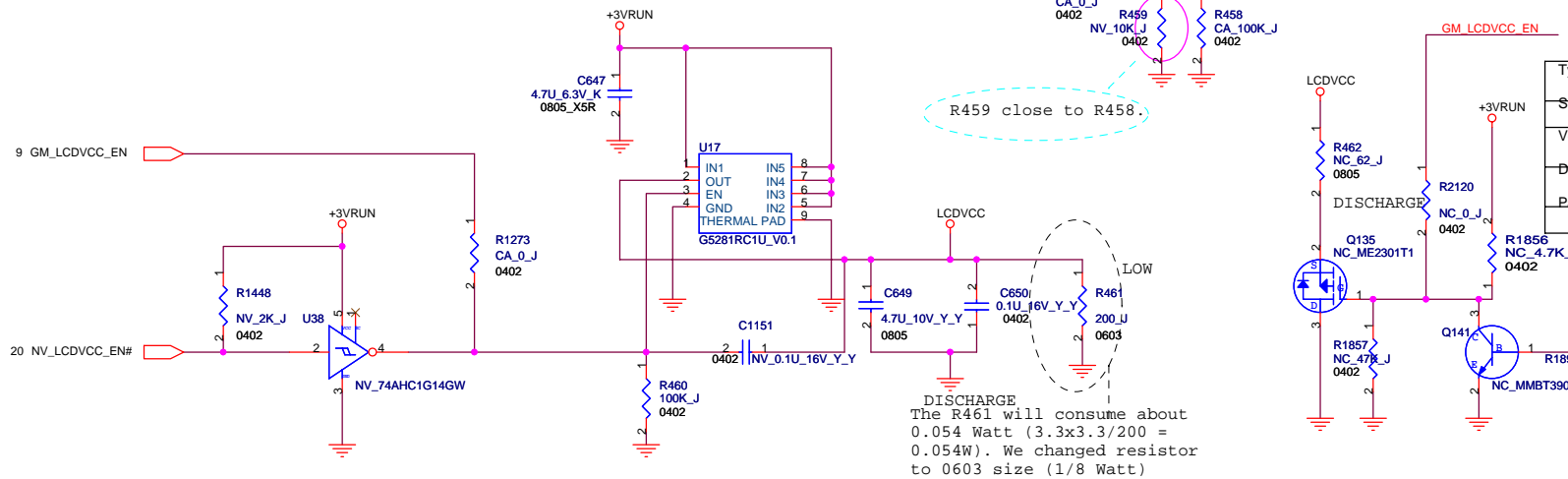
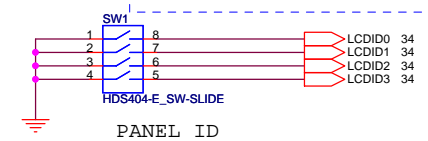


INVERTER CONN.



LVDS CONNECTOR

EVT use 30pin
DVT modify to 20pin

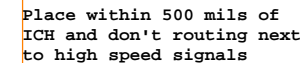
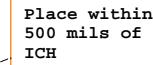


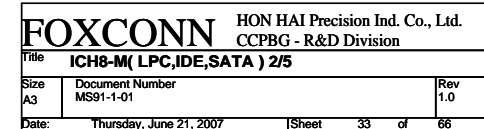
LCDID3 is for InstantOn switch
Enable: 0
Disable: 1

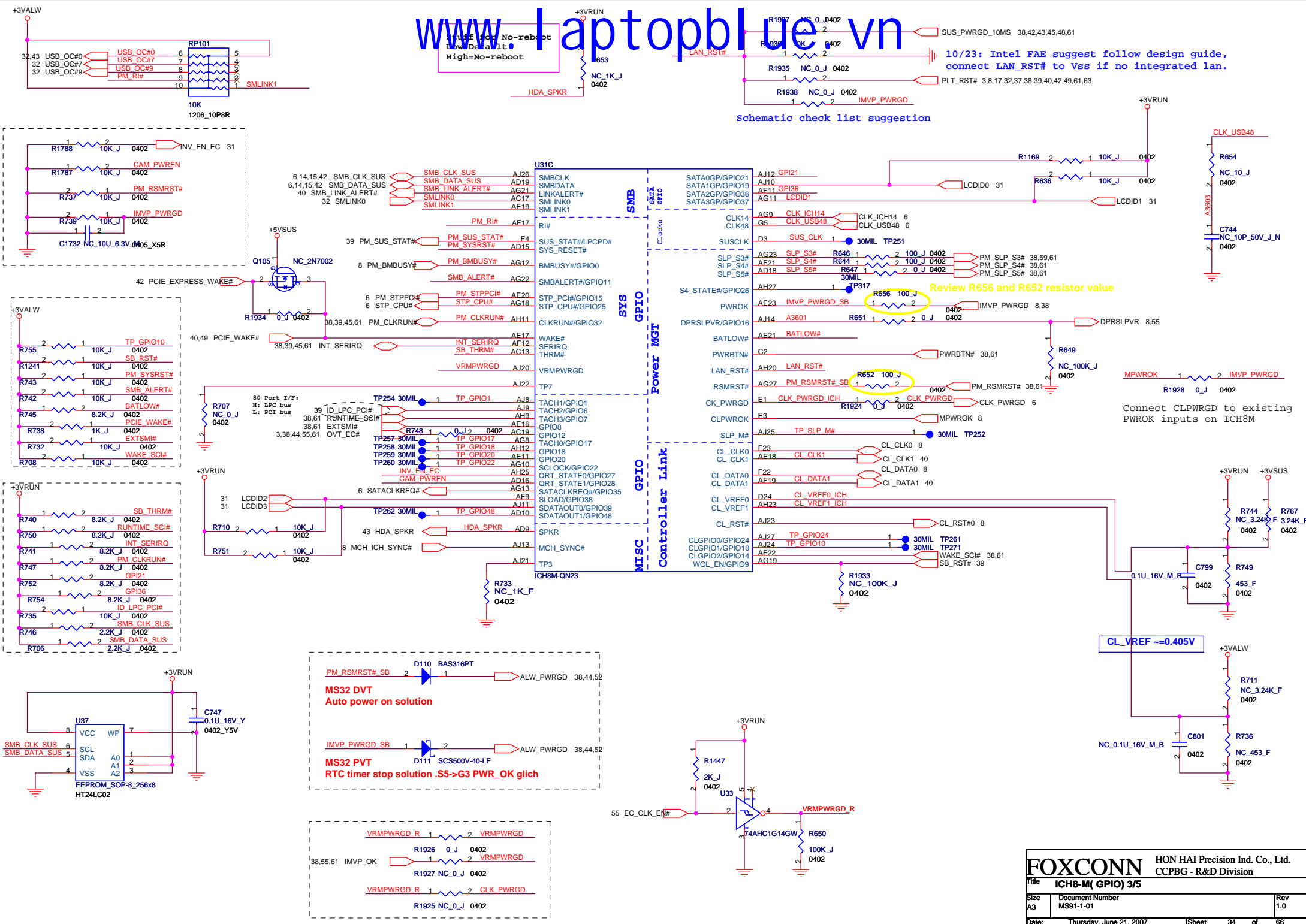
Type	WXGA	WXGA	WXGA	WXGA
Size	15.4" W	15.4" W	15.4" W	15.4" W
Vender	Samsung (2 lamp)	CPT (1 lamp)	AUO (2 lamp)	AUO (1 lamp)
Device Name	LTN154XB-L01	CLAA154WA05AN	B154EW07	GD15TL07
Panel ID [2, 0]	001	101	010	100

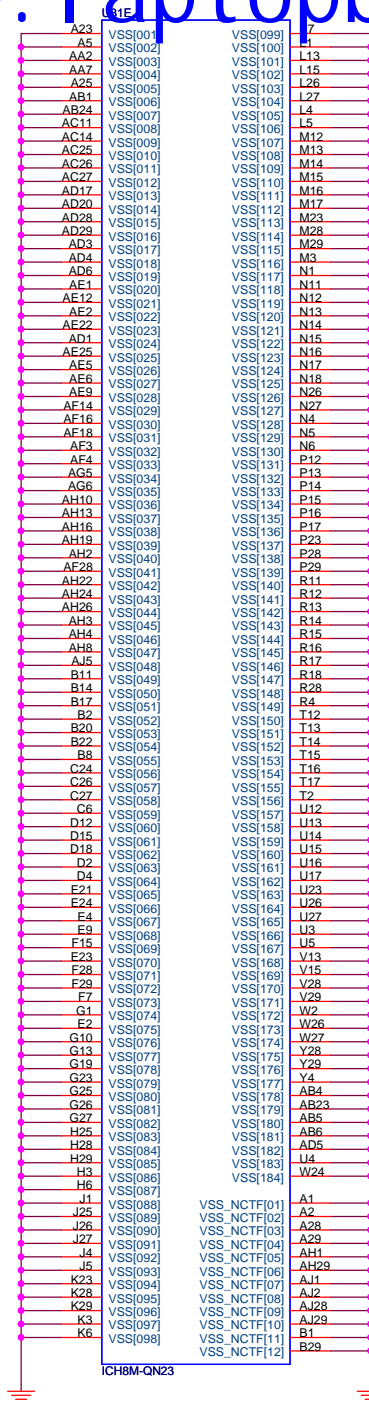


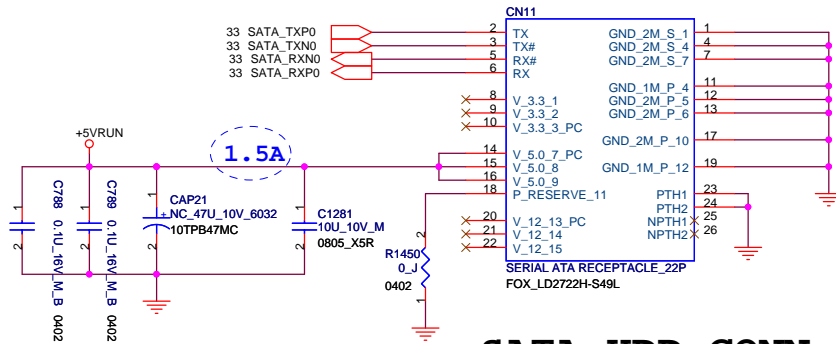
ICH8M-QN23



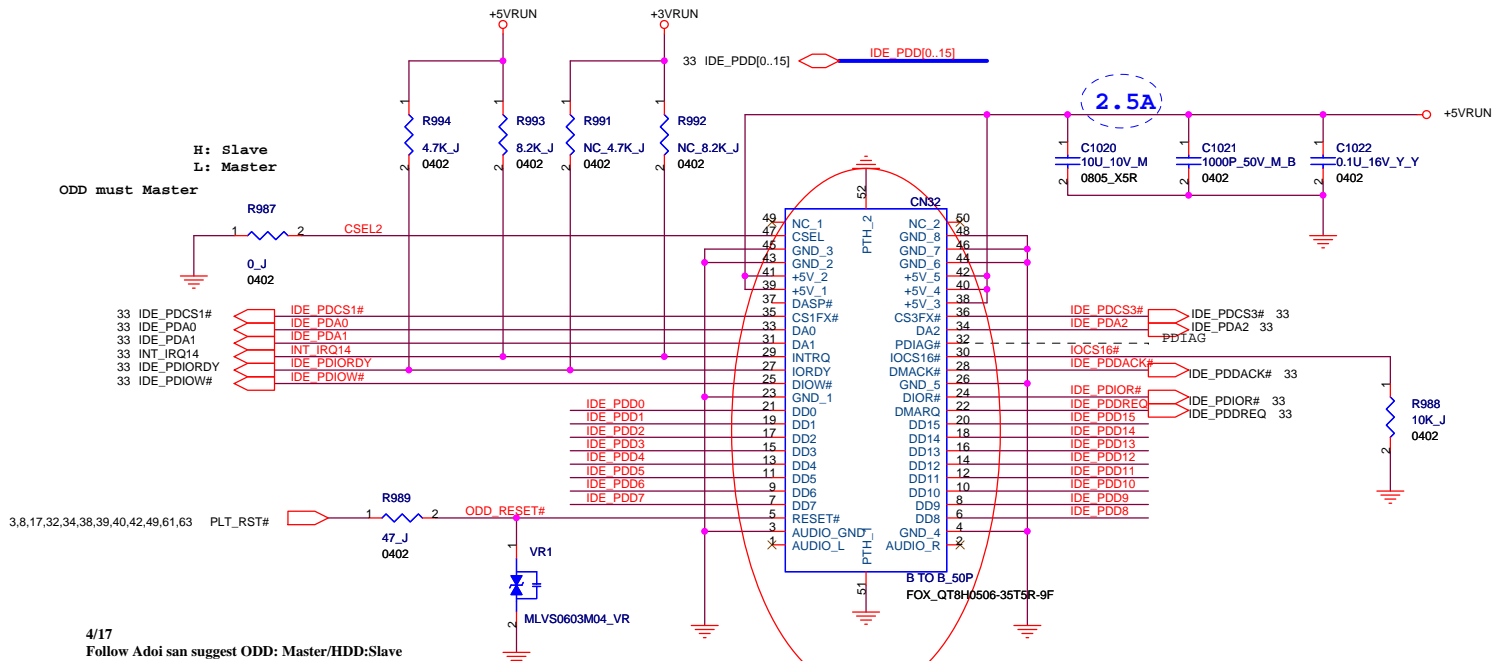






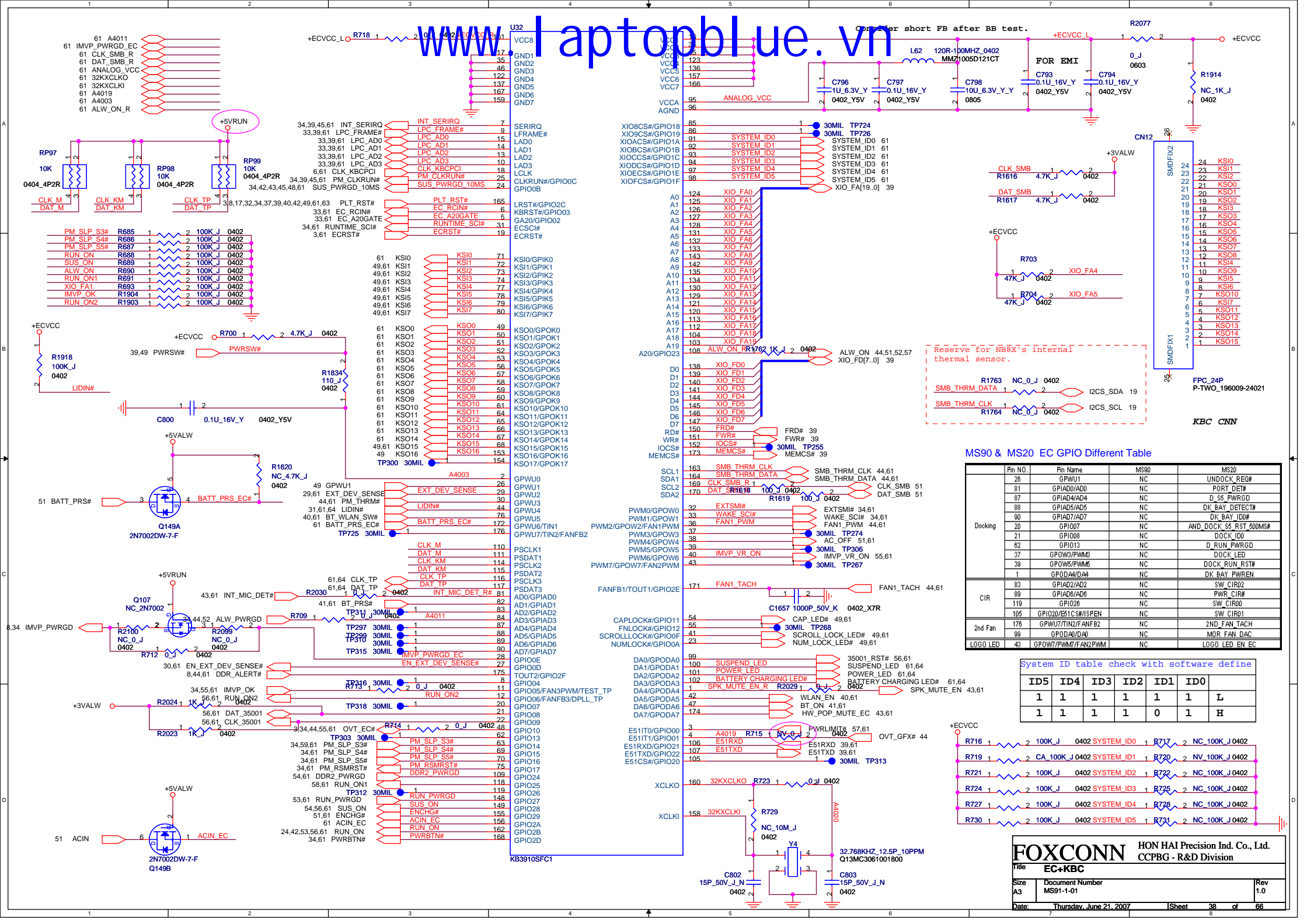


SATA HDD CONN



For ESD.

CD-ROM CONN



Reserve for NB8x's internal thermal sensor.

SMB_THRM_CLK 1 2 0402

SMB_THRM_DATA 1 2 0402

R763 NC_0_J 0402

R764 NC_0_J 0402

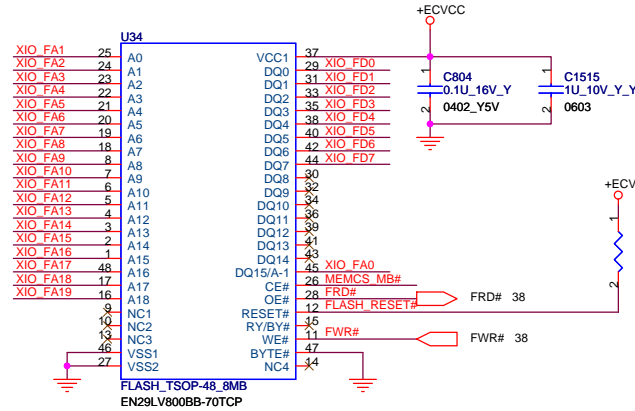
MS90 & MS20 EC GPIO Different Table

Pin NO.	Pin Name	MS90	MS20
26	GPWU1	NC	UNDOCK_REO#
81	GPIAD0/AD0	NC	PORT_DET#
87	GPIAD4/AD4	NC	D_S5_PWRGD
88	GPIAD6/AD6	NC	DK_BAY_DETECT#
90	GPIAD7/AD7	NC	DK_BAY_IDO#
20	GPIOD7	NC	AND_DOCK_S5_RST_600MS#
21	GPIOD8	NC	DOCK_IDO
62	GPIOD13	NC	D_RUN_PWRGD
37	GPWD3/PWM3	NC	DOCK_LED
39	GPWD5/PWM5	NC	DOCK_RUN_RST#
1	GPDA4/DA4	NC	DK_BAY_PWREN
83	GPIAD2/AD2	NC	SW_CIR02
89	GPIAD6/AD6	NC	PWR_CIR0
119	GPIOD26	NC	SW_CIR00
105	GPIOD20/ES1CS#/ISPEN	NC	SW_CIR01
176	GPWU7/TIN2/FANFB2	NC	2ND_FAN_TACH
99	GPDA0/DA0	NC	MOR_FAN_DAC
43	GPWU7/PWM7/FAN2PVM	NC	LOGO_LED_EN_EC

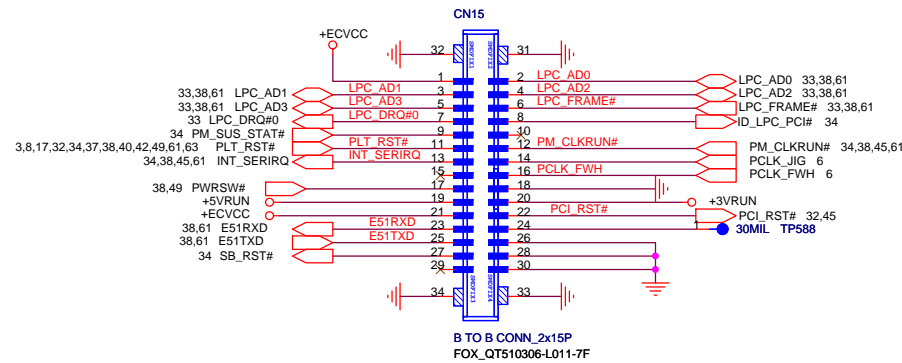
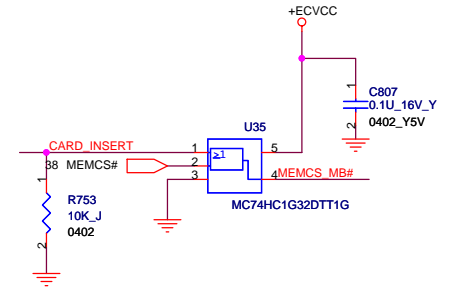
System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
1	1	1	1	1	1	L
1	1	1	1	0	1	H

38 XIO_FA[19..0]
38 XIO_FD[7..0]

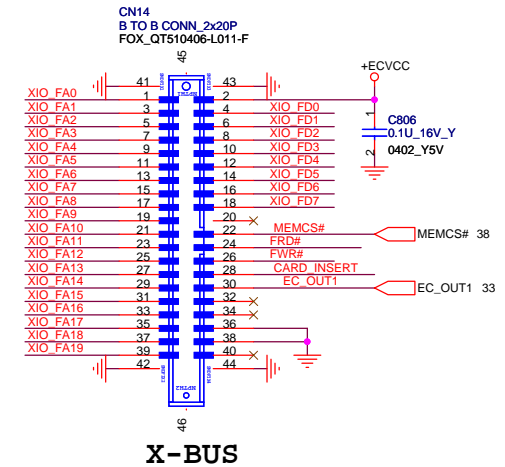


FLASH BIOS

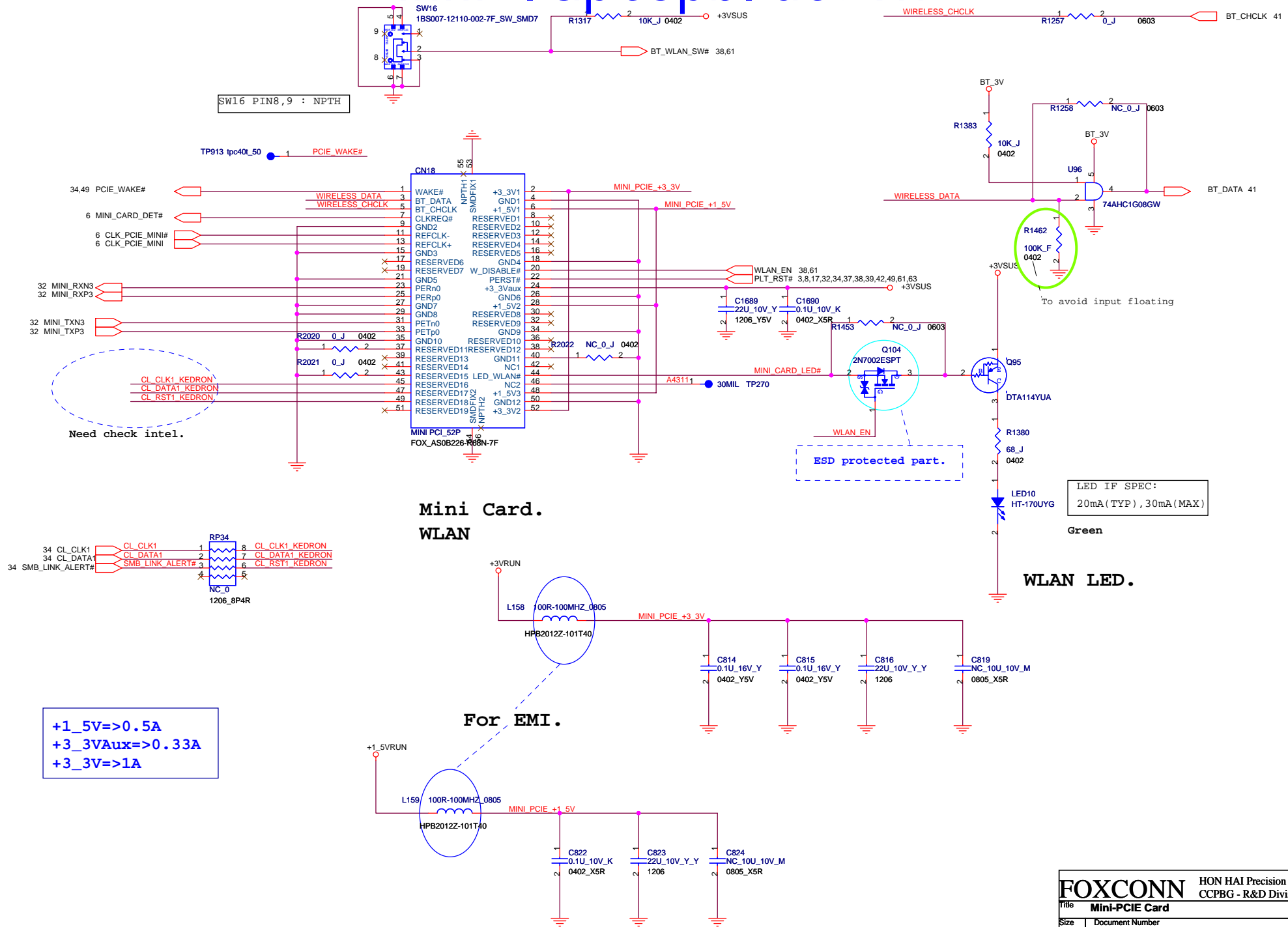


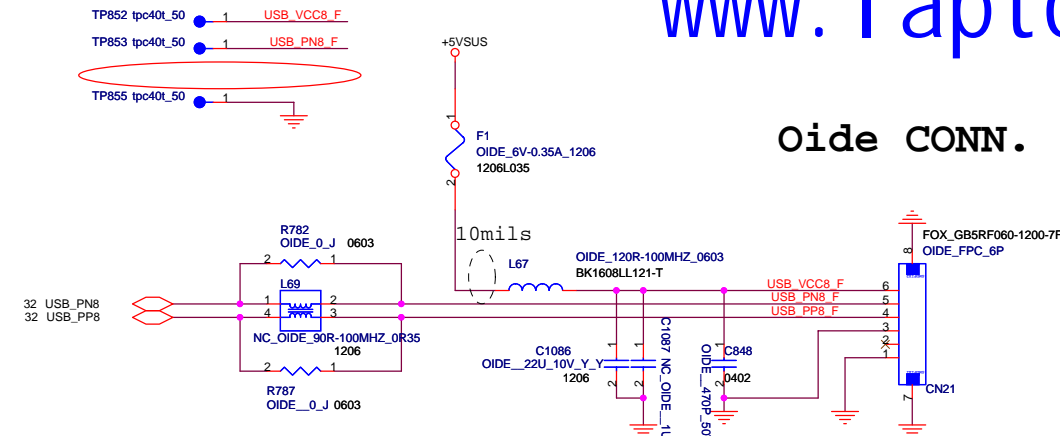
JIG-120

Pin 18 of JIG-120 is useless in debug board,
so we let pin 18 NC.



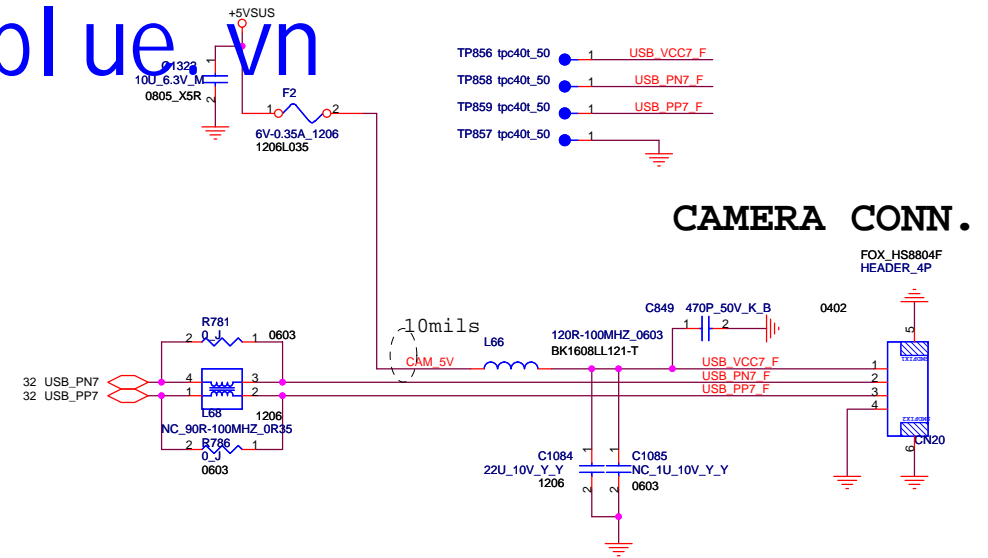
X-BUS



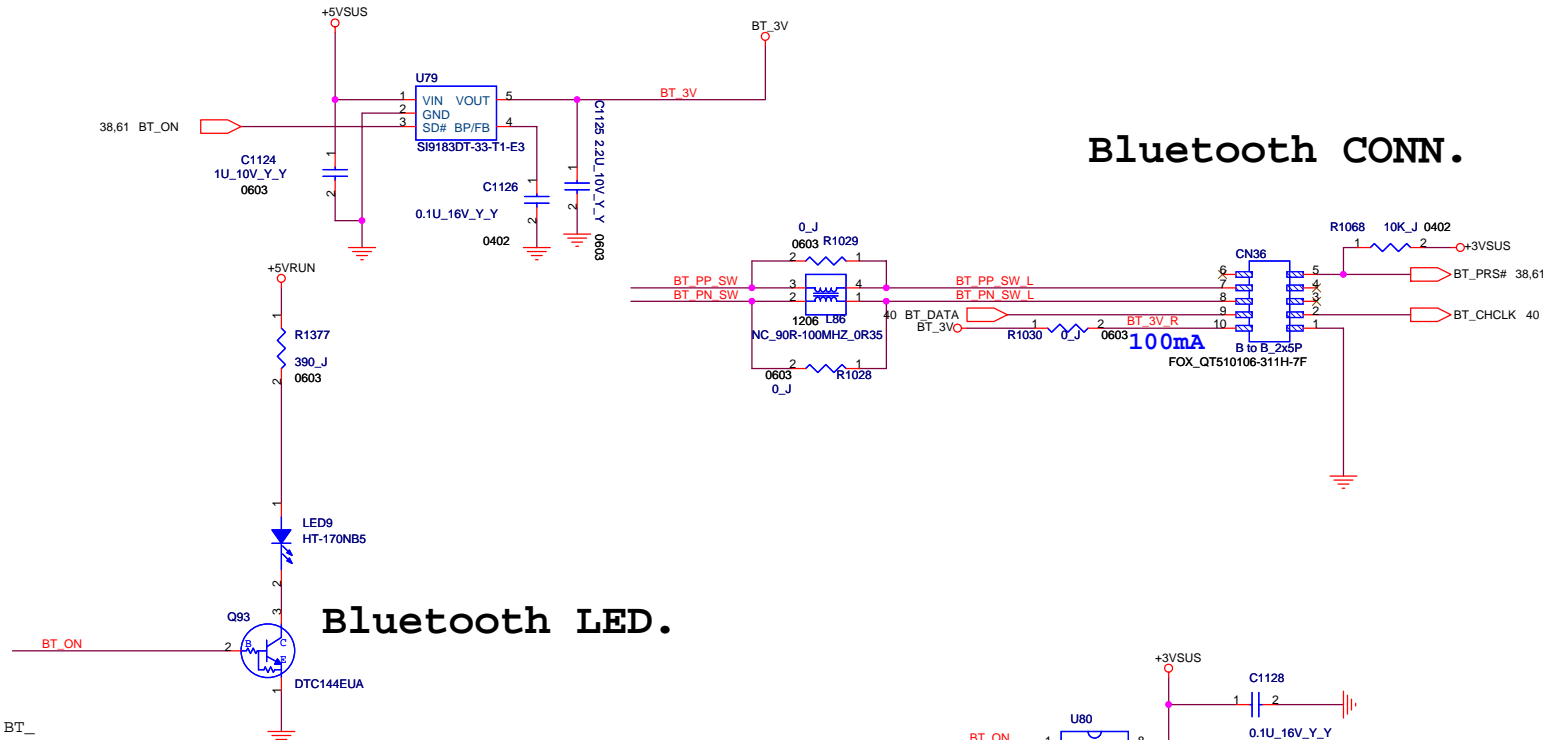


BOM Notice: OIDE_

W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff



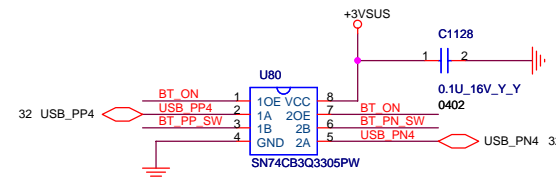
Bluetooth CONN.

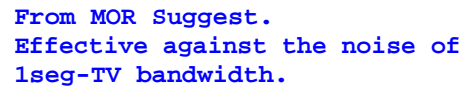


Bluetooth LED.

BOM Notice: BT_

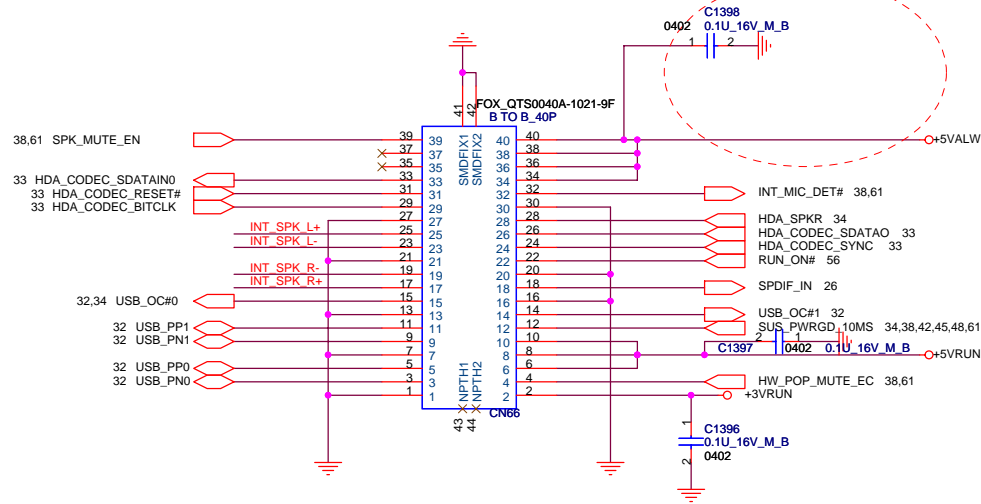
W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff



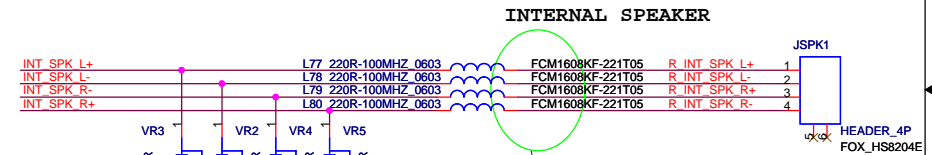
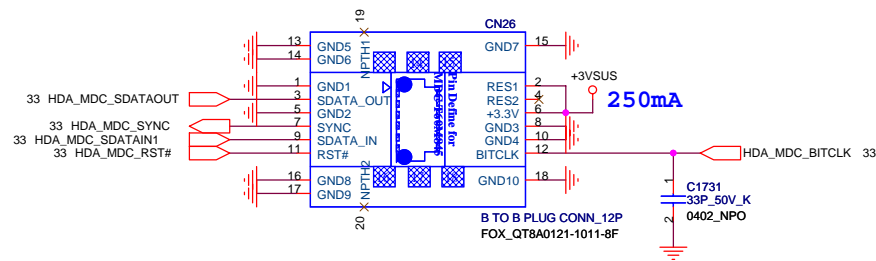


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Audio & USB Board CONN.



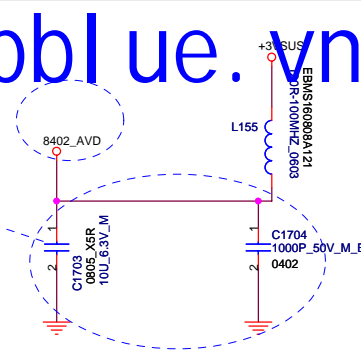
MDC CONN.



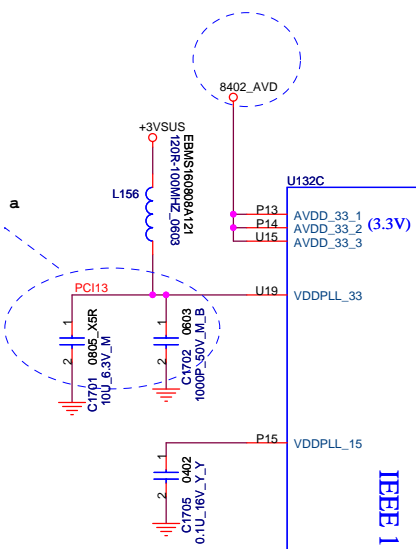
Close CONN for EMI.

- TP863 tpc40t_50 1 R_INT_SPK L+
- TP864 tpc40t_50 1 R_INT_SPK L-
- TP866 tpc40t_50 1 R_INT_SPK R+
- TP865 tpc40t_50 1 R_INT_SPK R-

This array must be placed close to AVDD(Pin P13,P14,U15) They must be tied to a low-impedance GND.



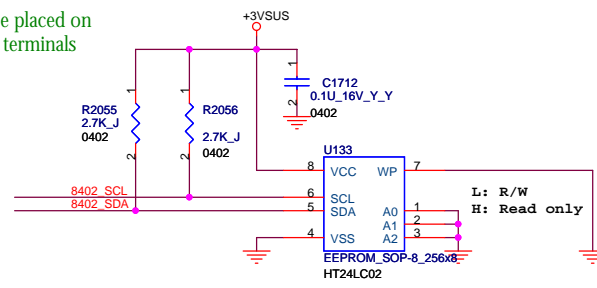
This array must be placed close to VDDPLL(Pin U19) They must be tied to a low-impedance GND.



This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

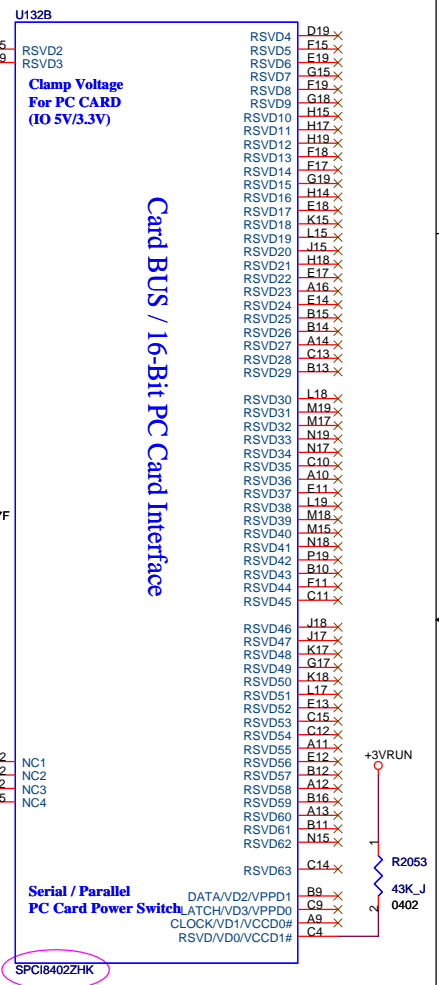
VSSPLL must be tied to a low-impedance GND.

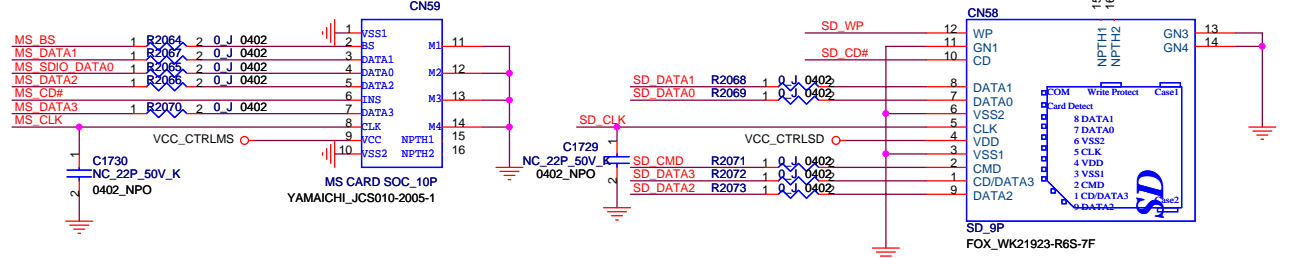
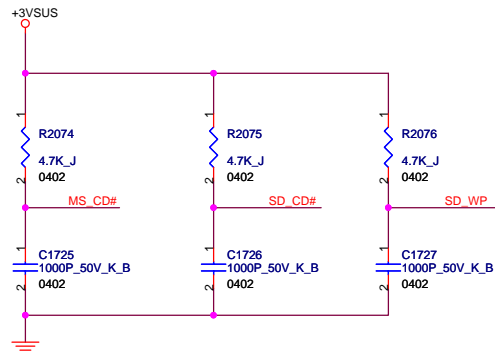
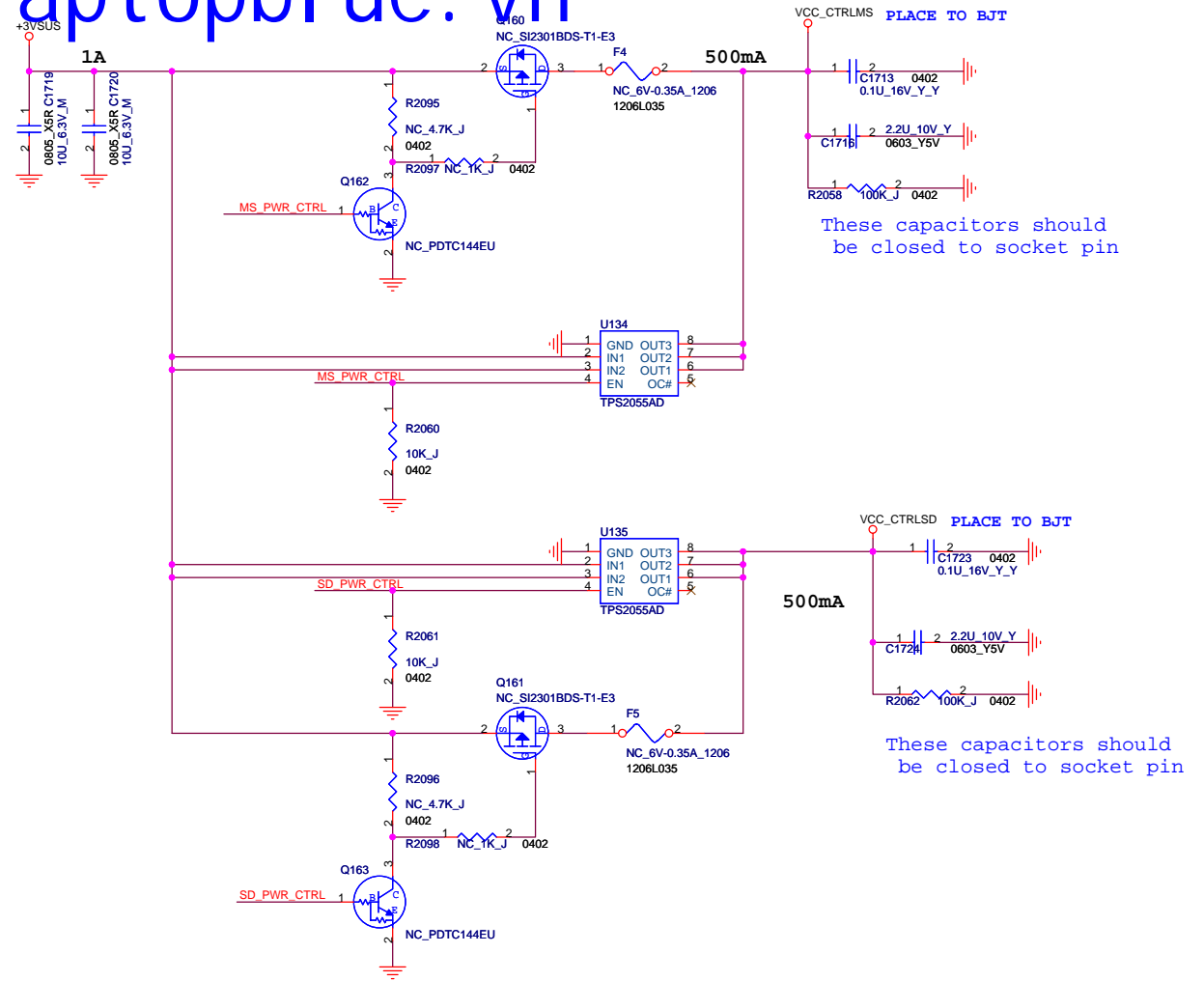
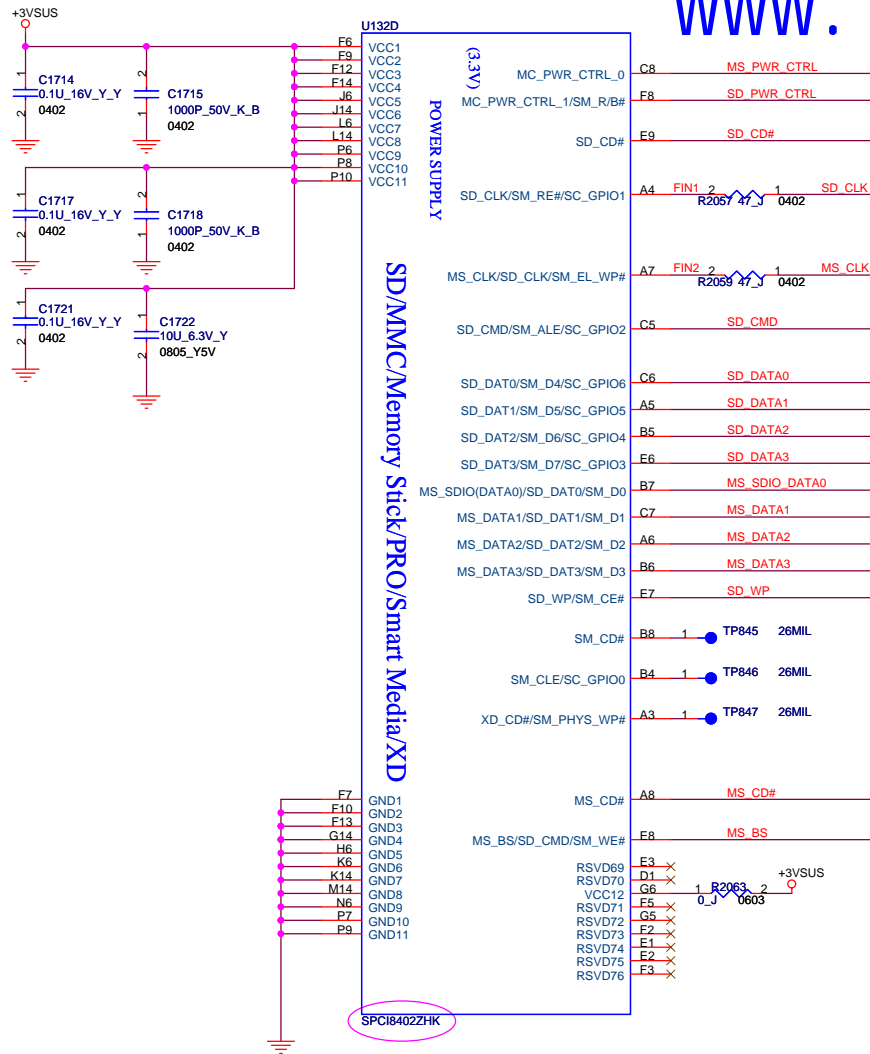


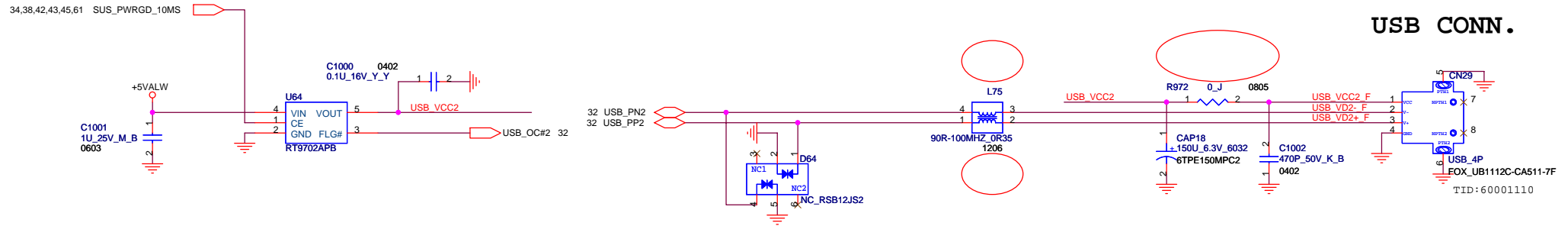
Resistors should be placed on the SCL and SDA terminals

iLink CONN.

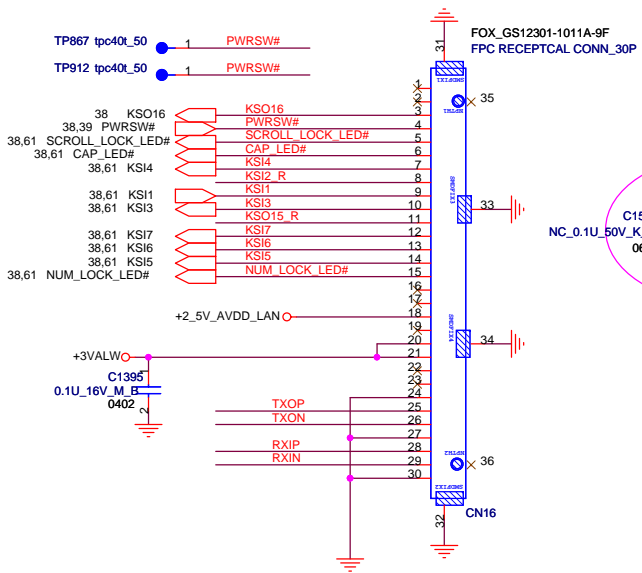
Place near PCI8402.



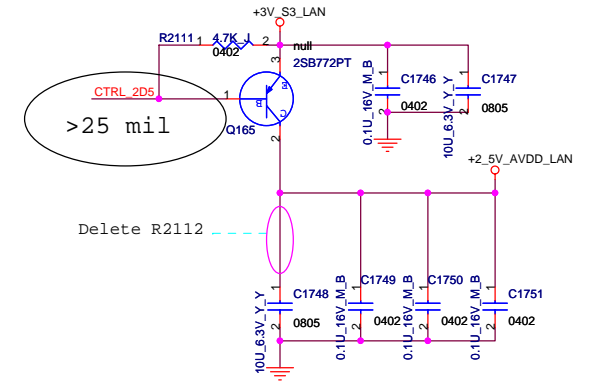
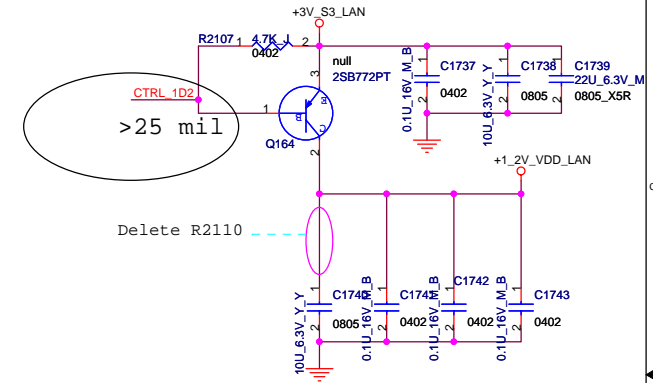
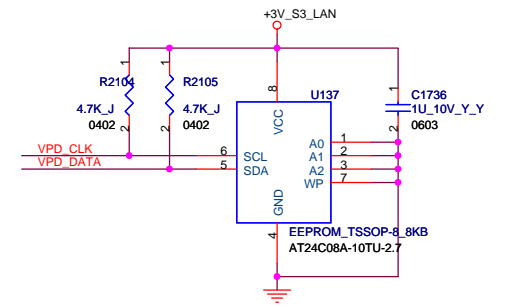
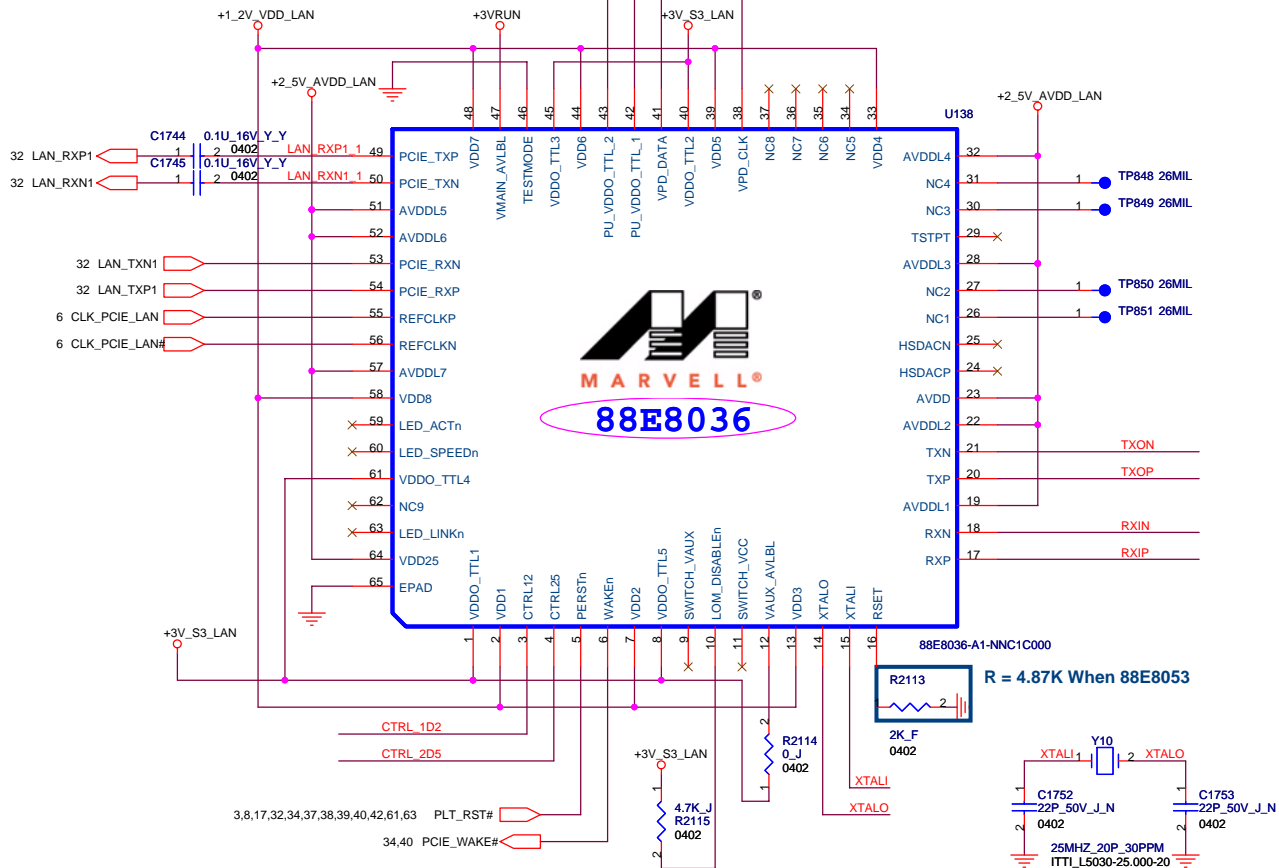




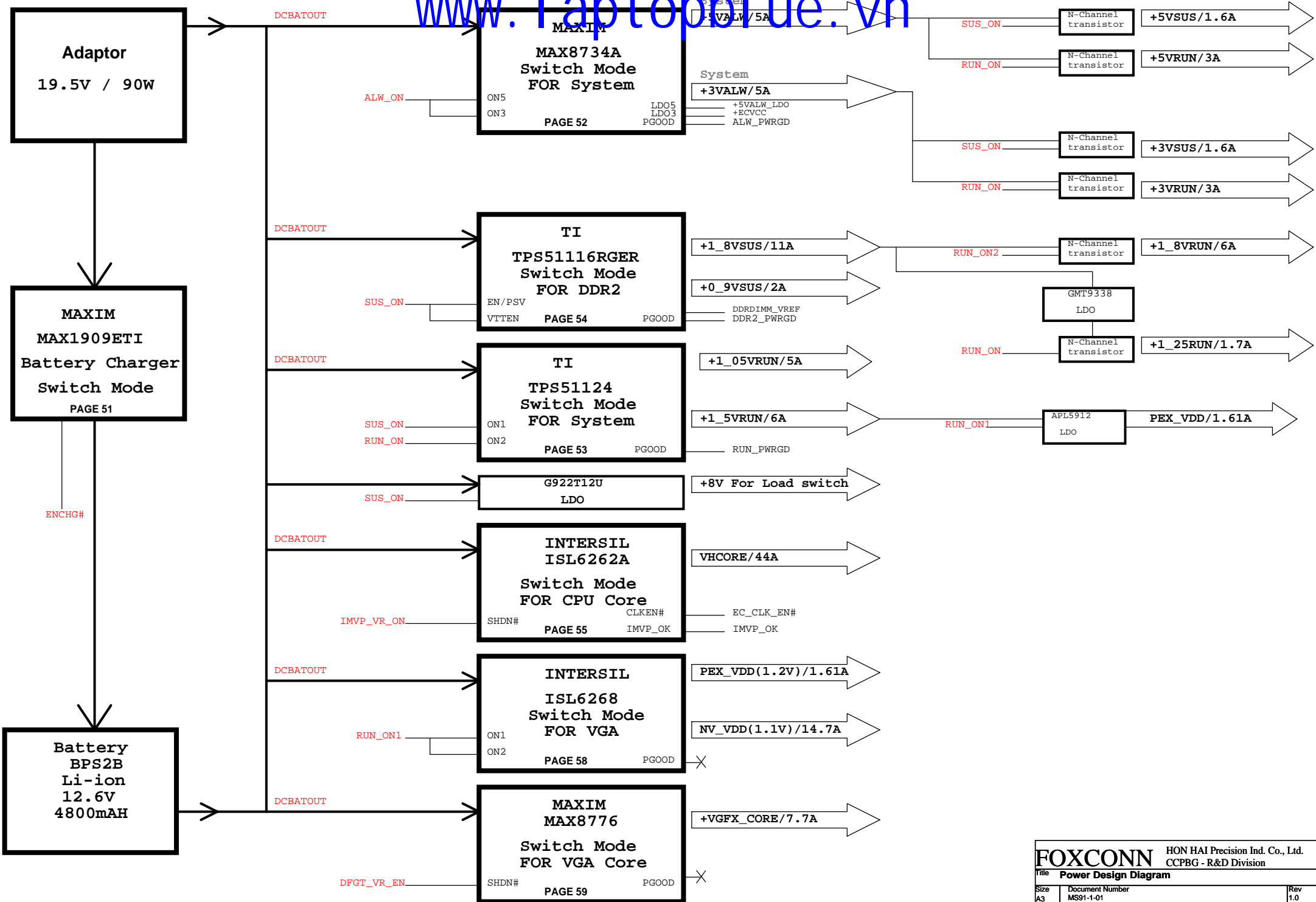
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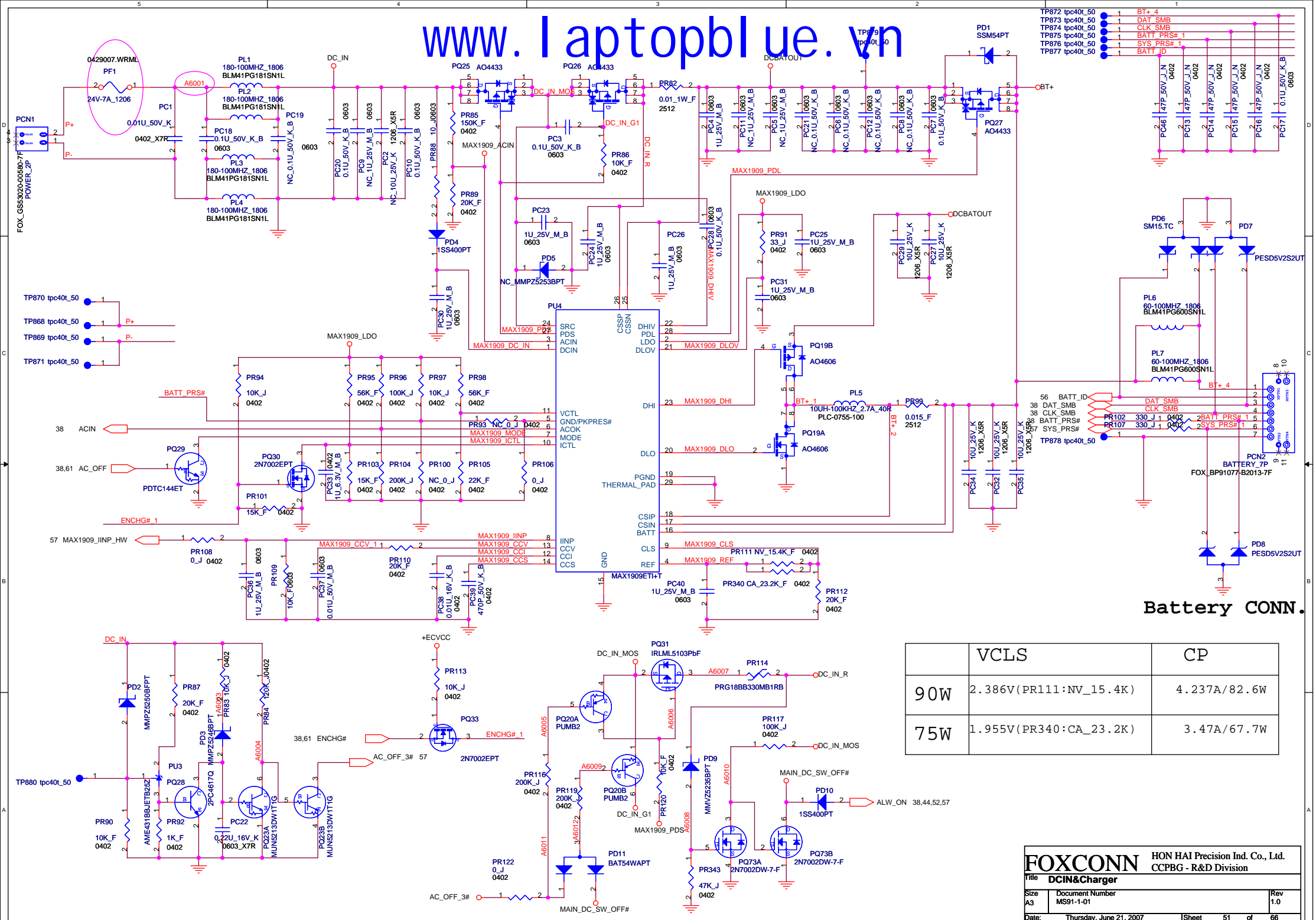


Switch Board CONN.

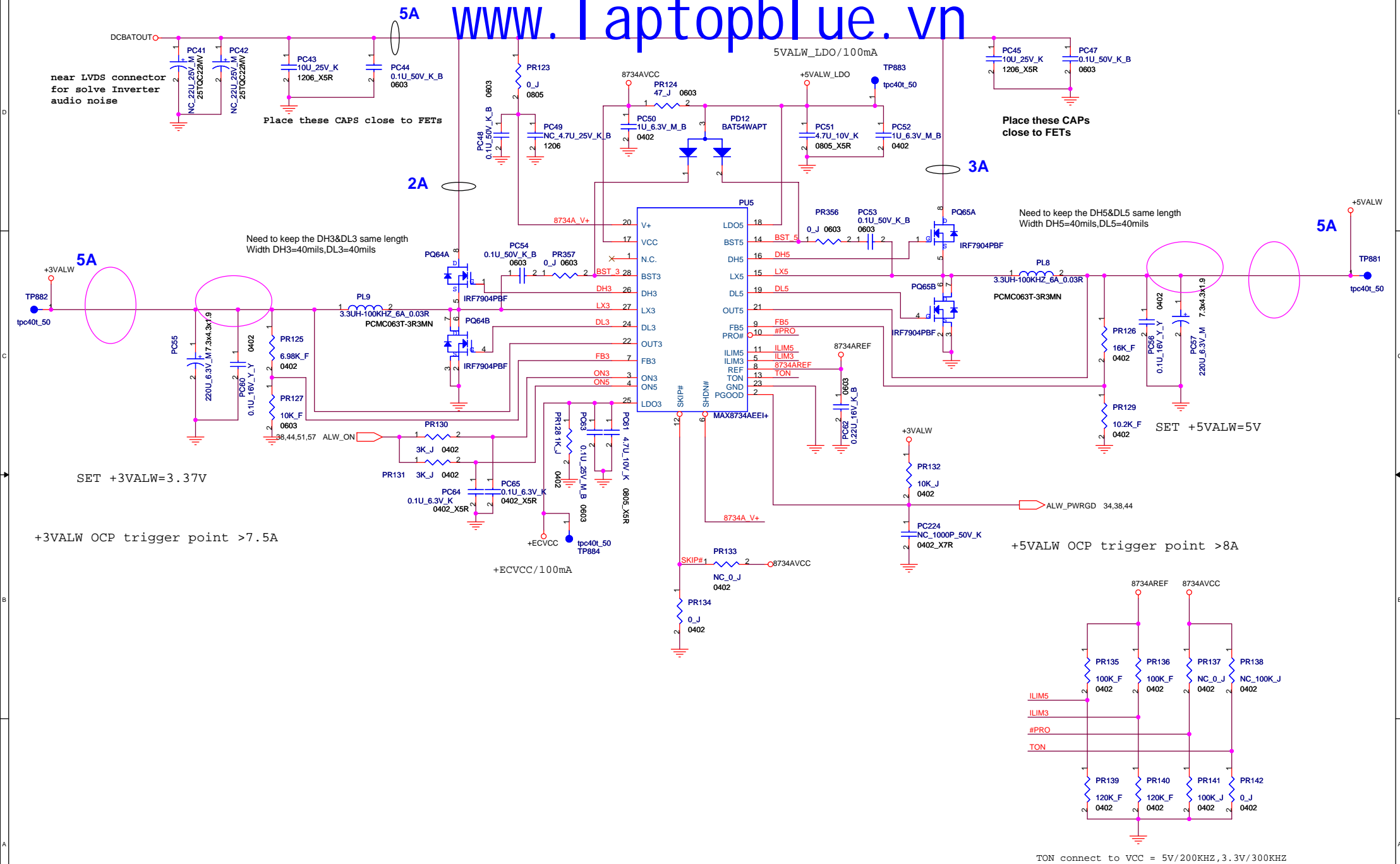


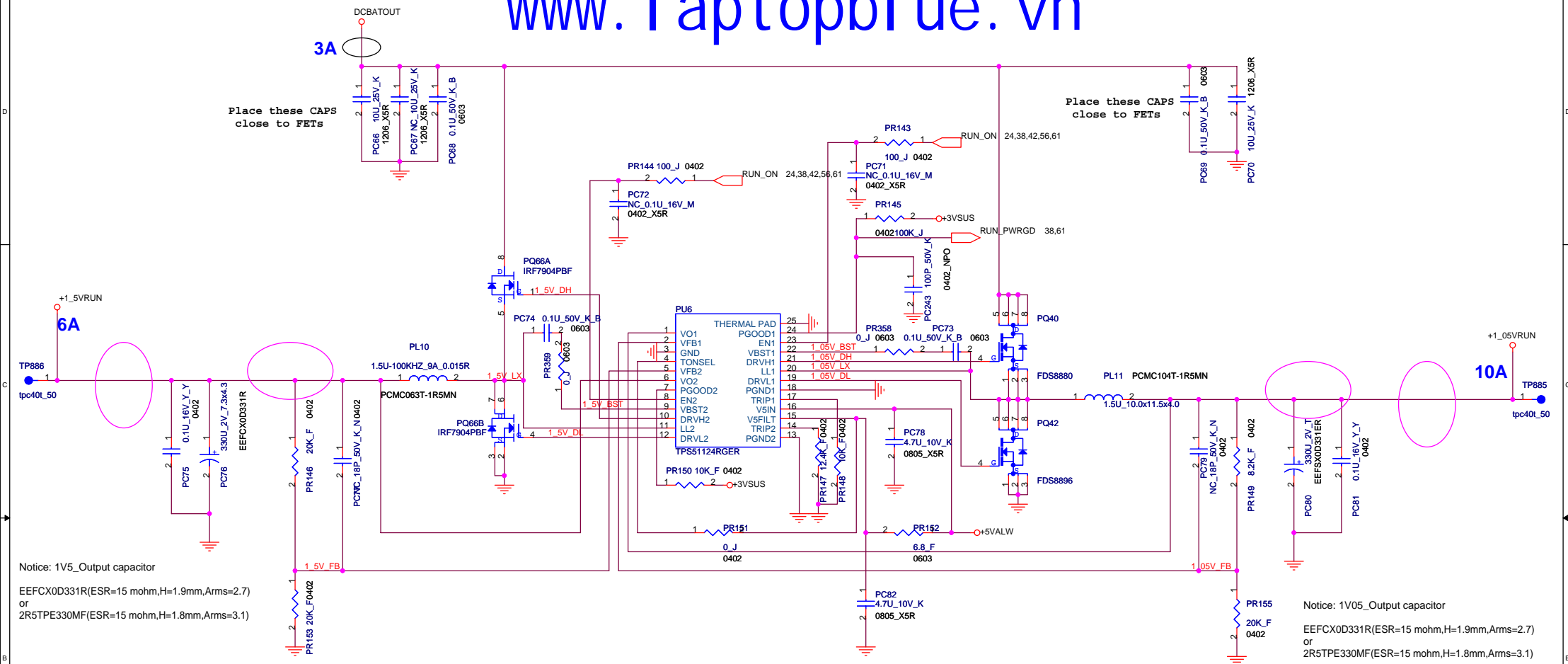
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
LAN (88E039)			
Size A3	Document Number MS91-1-01	Rev 1.0	
Date:	Thursday, June 21, 2007	Sheet	49 of 66

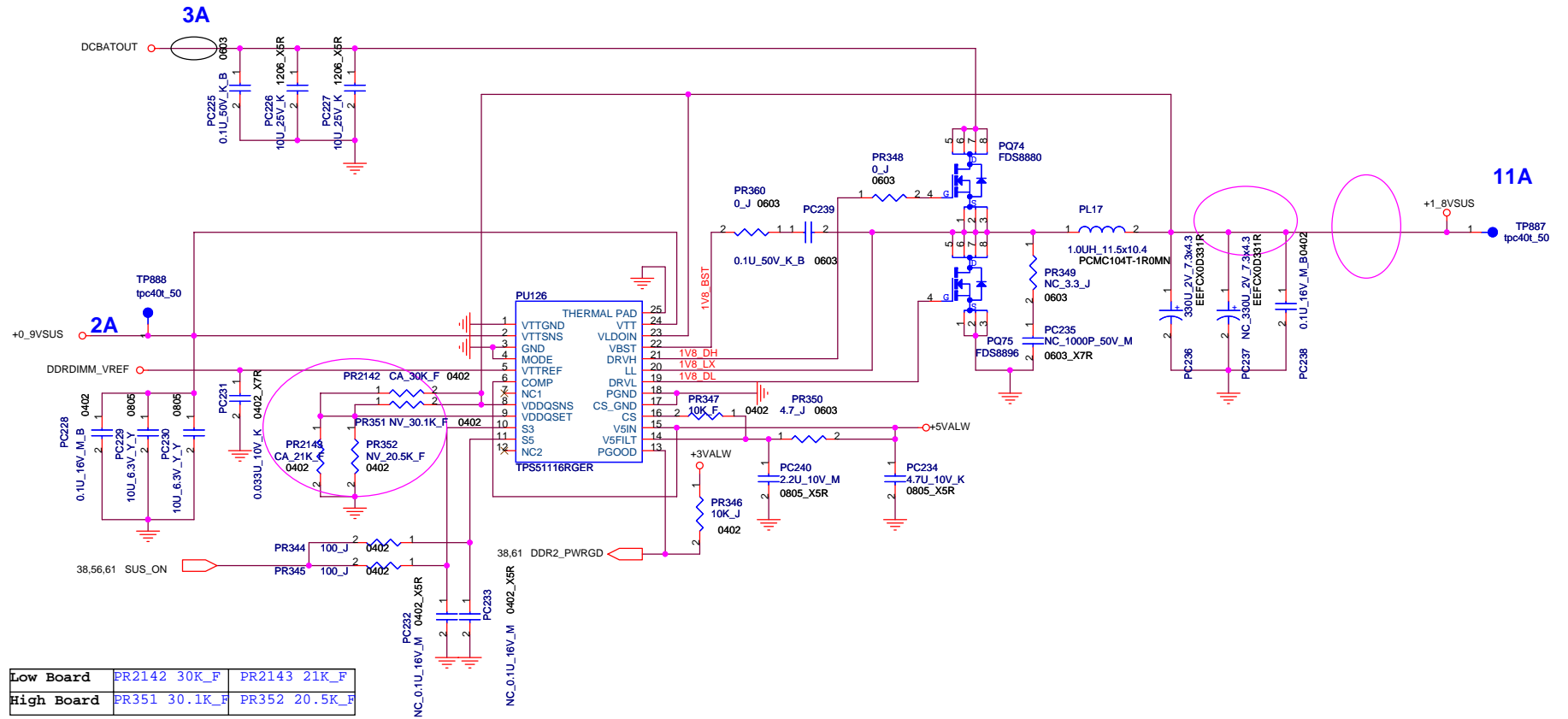




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Setting +1_8VSUS OCP trigger point to 16A

3,34,38,44,61 OVT_EC# OVT_EC#

Place these
close to F

Delete PJ7

Delete PC120

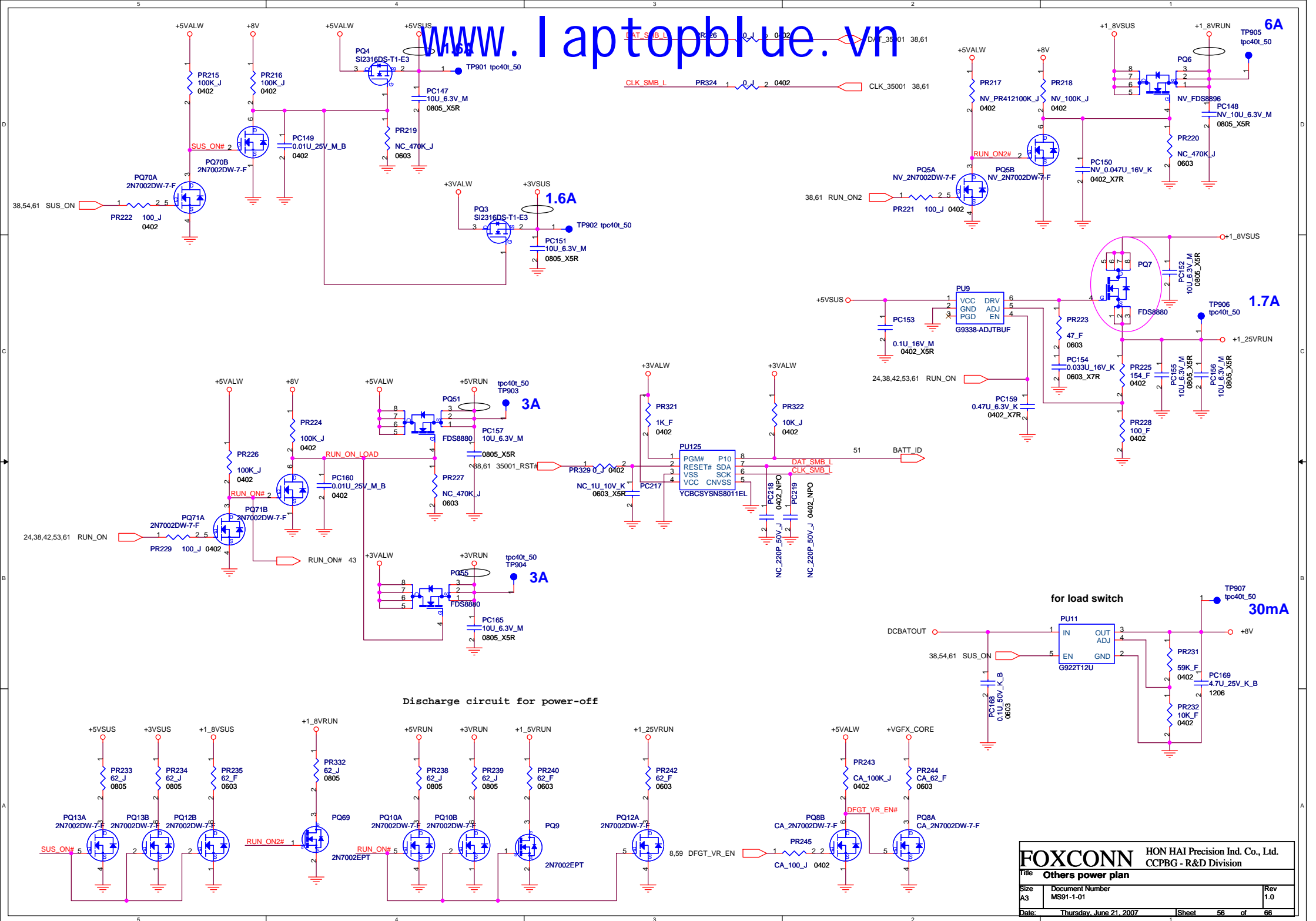
CORE

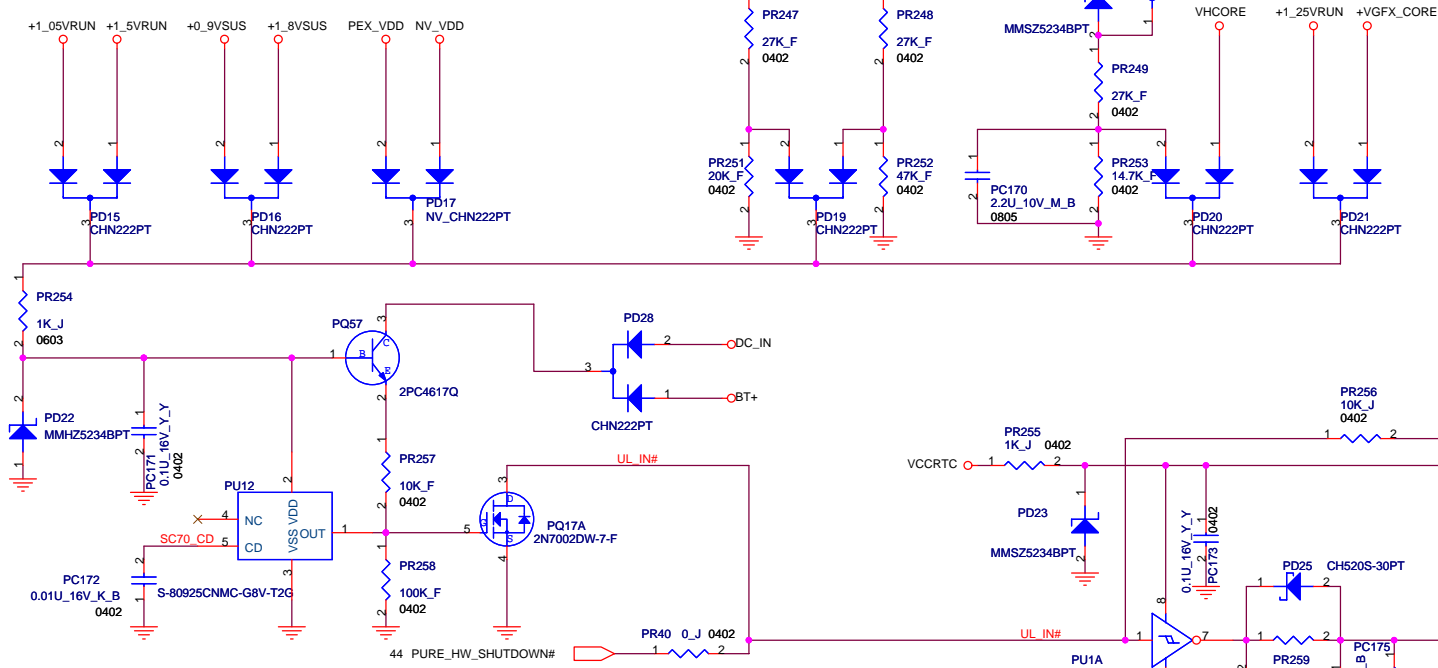
EVT2 0509

Delete PC223

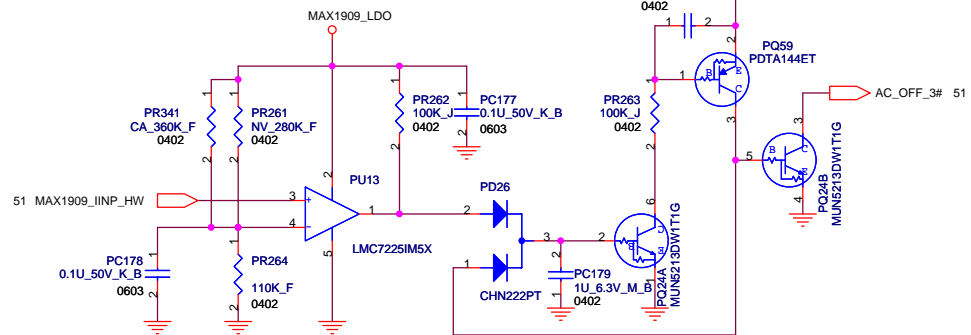
OCP Setting

OCP trigger point 65A <10uS

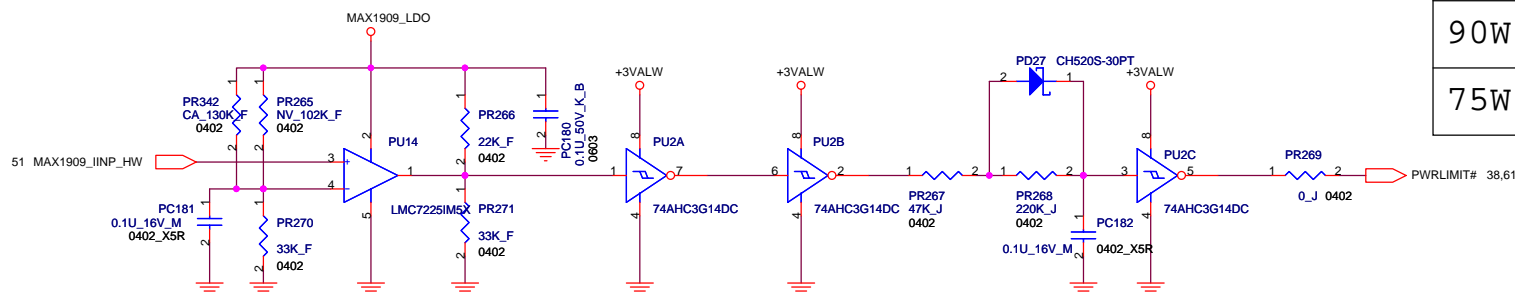




Control ACIN OCP protect



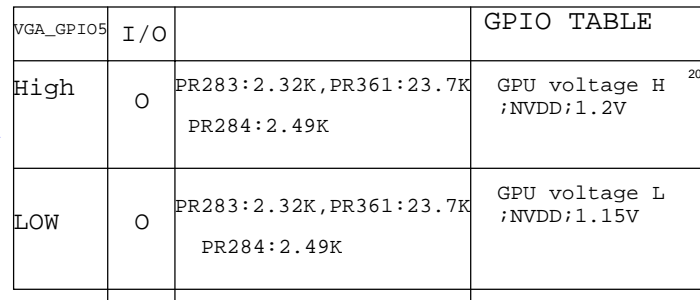
Setting ACIN OCP trigger point to 5.077A

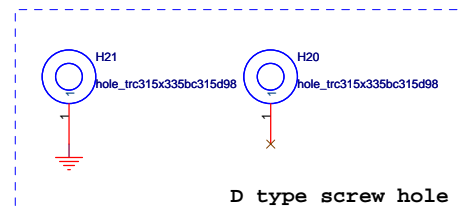
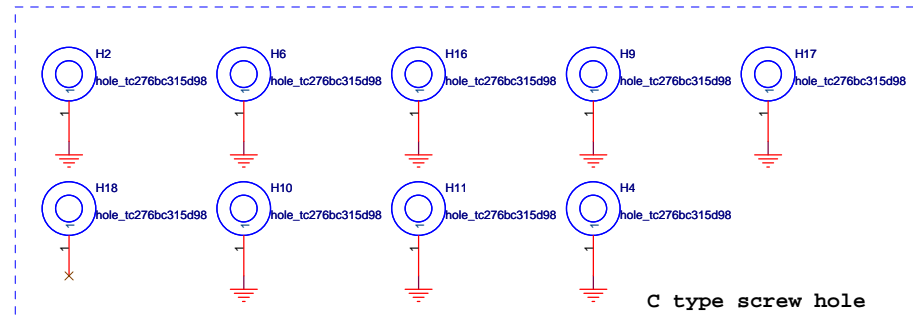
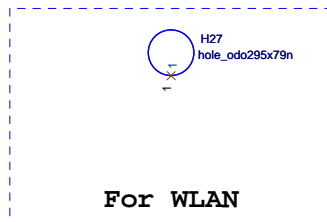
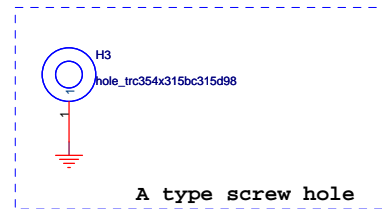
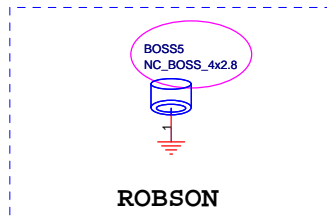
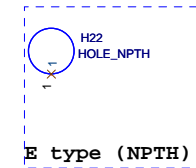
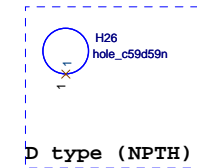
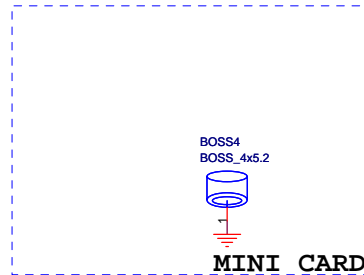
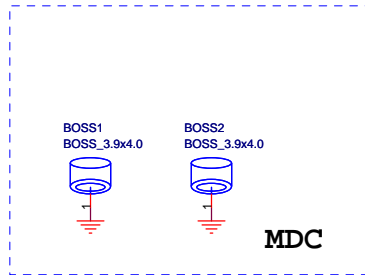
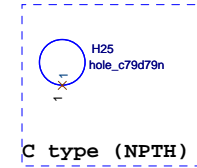
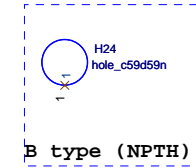
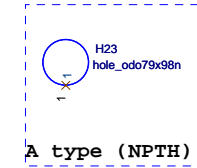
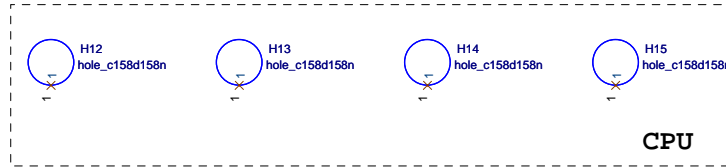


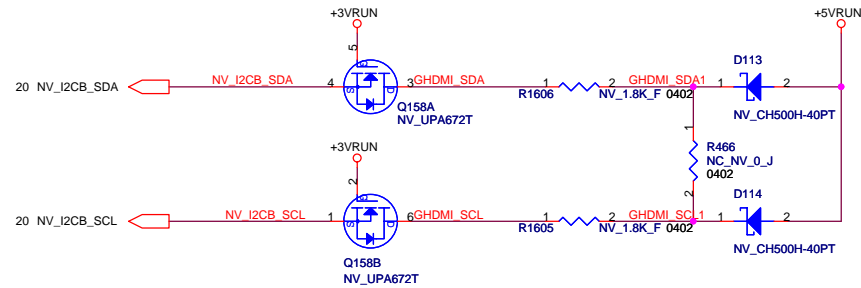
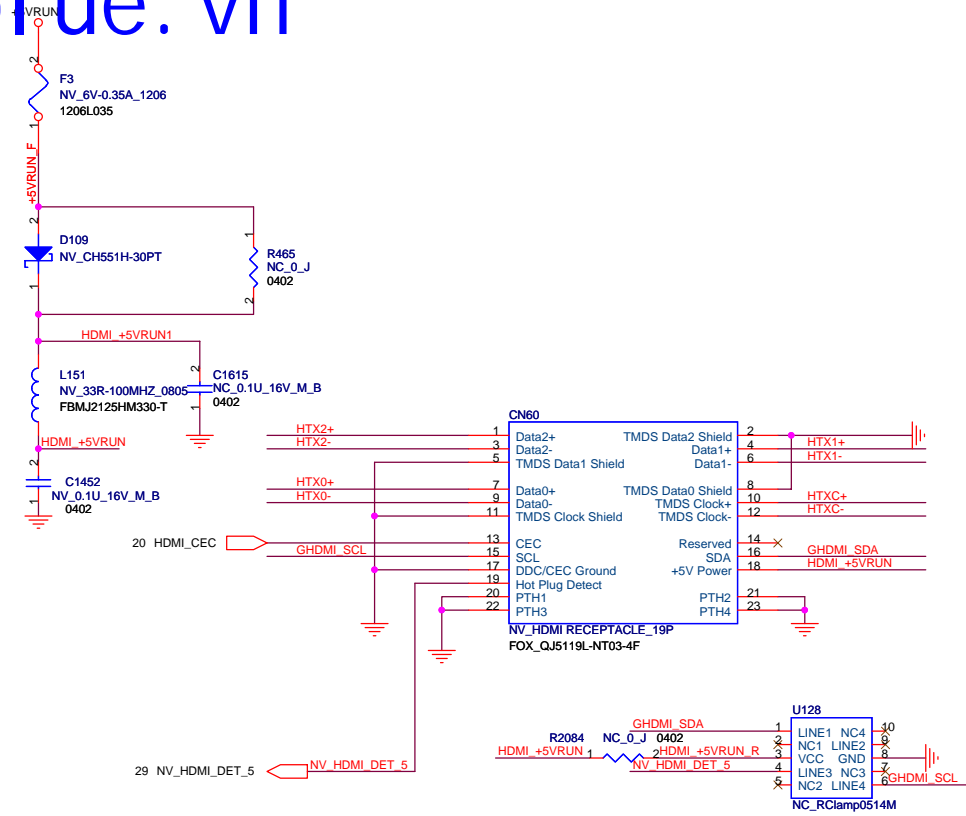
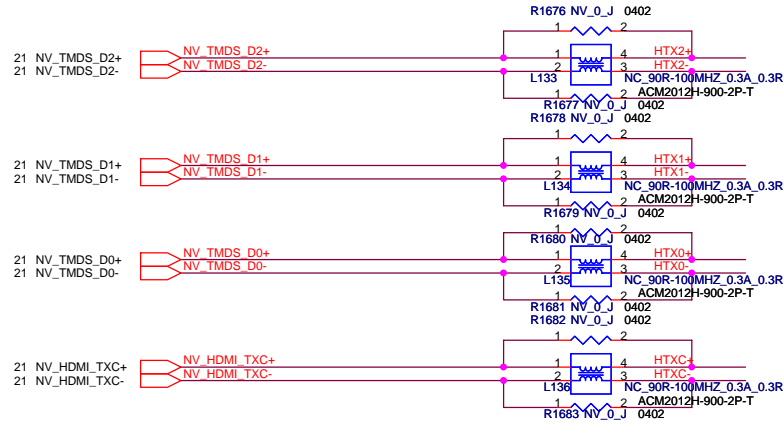
Setting PWRLIMIT# trigger point to 4.15A

		ACIN OCP
90W	PR261:NV_280K	5.07A/98.9W
75W	PR341:CA_360K	4.21A/82.1W

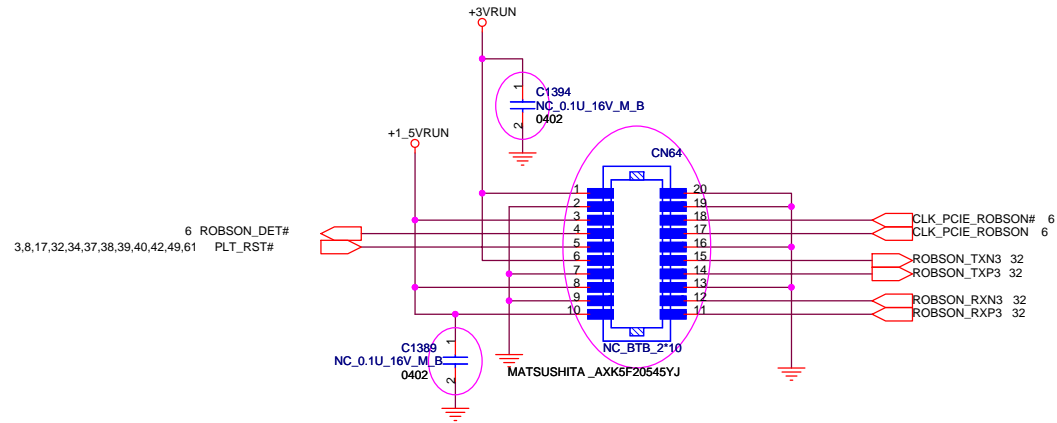
		PWRLIMIT
90W	PR265:NV_102K	4.4A/85.8W
75W	PR342:CA_130K	3.64A/71W



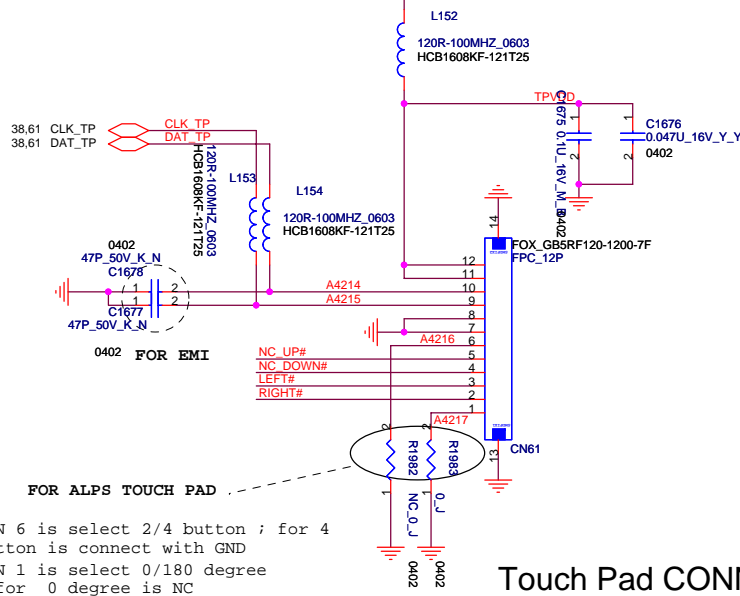
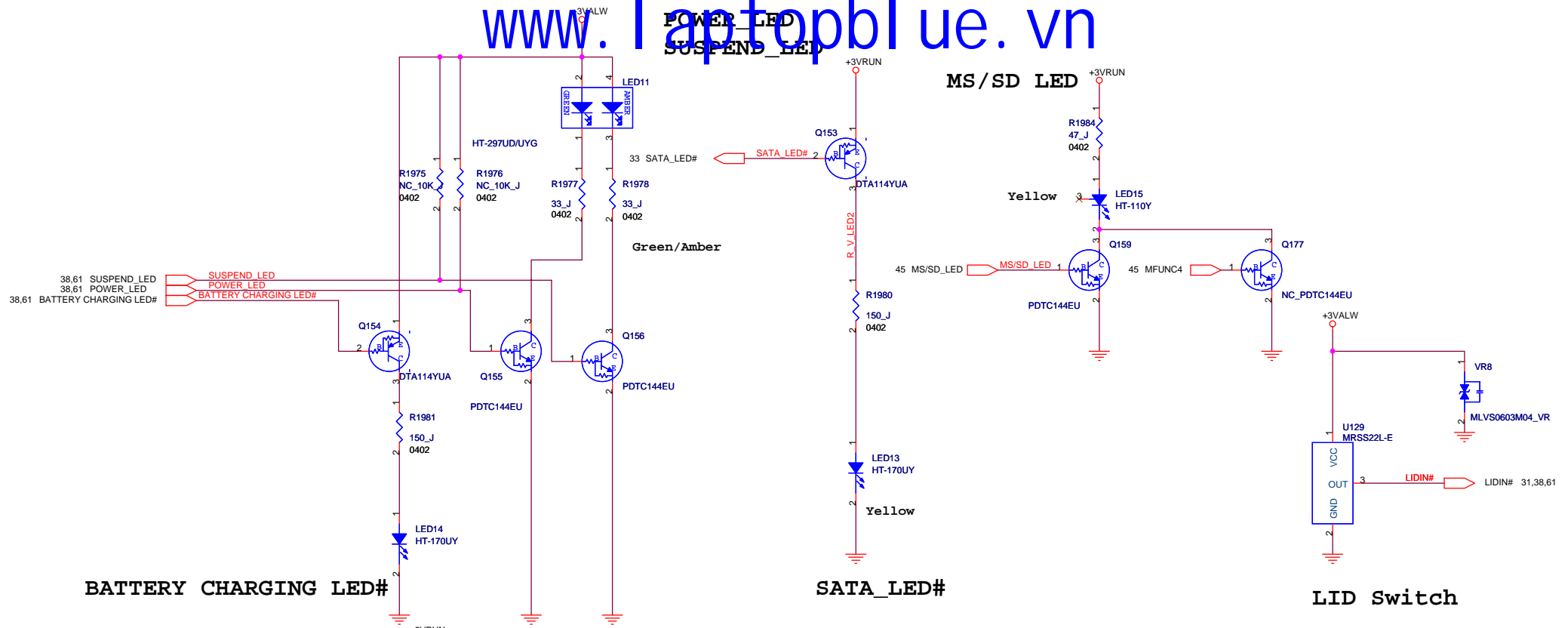




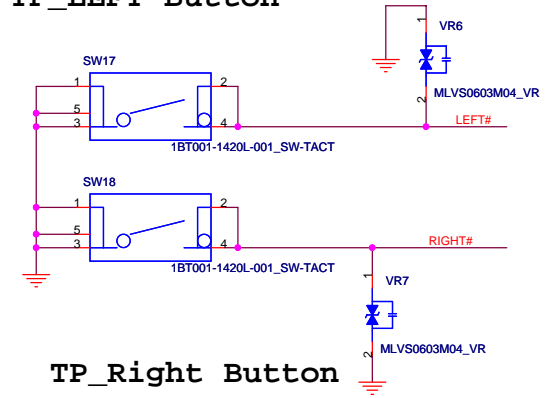
ROBSON Board CONN



C1389,C1394 close to CN64.



TP_LEFT Button



MS91 DVT

(2007/04/04)

P.51 Move PF1 close to the PCN1 for MS1X burn out issue.

P.52,53,54,55,58 Add PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for DVT debug.

P.54 Add PR2142, PR2143, change PR352 value 20.5K_F to NV_20.5K_F, PR351 value 30.1K_F to NV_30.1K_F.Because H version and L version need different voltage level.

P.6,32,63 Change RP11 value NC_33 to 33,
C1394 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C1389 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C735 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C730 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
CN64 value NC_BT_B_2*10 to BTB_2*10,
for robson function need.

(2007/04/06)

p.2 Block diagram update for MS91 feature spec.

P.49 Change U138 from MARVELL 88E8036 to MARVELL 88E8039 for MS91 feature spec.

P.18 Add two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for backup solution.

P.18 Change PCI device ID: Change
R231 value NV_2K_J to NVNB8M_2K_J,
R232 value NC_2K_J to NVNB8P_2K_J,
R233 value NC_2K_J to NVNB8P_2K_J,
R234 value NV_2K_J to NVNB8M_2K_J.

(2007/04/09)

p.51 Move the net A6001 close to PF1 for moved PF1.

p.30 Change C666 10P_50V_J_N to NC_10P_50V_J_N,
C669 10P_50V_J_N to NC_10P_50V_J_N,
C671 10P_50V_J_N to NC_10P_50V_J_N for EMI request.

p.30 Add C668,C670,C672 for EMI request.

p.31 Add R459 for nVidia suggest.

(2007/04/11)

p.49 Delete R2110,R2112 for Marvell suggest.

p.38 Change touch pad power from +5VSUS to +5VRUN for design mistake.

p.55 Delete PC120 PC223 for save layout space.

(2007/04/12)

P.1 Add MS91 BOM configuration.

P.60 Change BOSS5 value NC_BOSS_4x2.8 to BOSS_4x2.8 for lock robson.

(2007/04/13)

P.52 Add net name +3VALW_PWM and +5VALW_PWM becuase add PJ2 and PJ1.

P.53 Add net name +1_5VRUN_PWM and +1_05VRUN_PWM becuase add PJ4 and PJ3.

P.54 Add net name +1_8VSUS_PWM becuase add PJ5.

P.55 Delete PJ7 and change DCBATOUT+ to DCBATOUT for save layout space.

P.58 Add net name NV_VDD_PWM and PEX_VDD+ becuase add PJ9 and PJ11.

P.59 Add net name +VGFX_CORE_PWM becuase add PJ12.

(2007/04/16)

P.1 Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request.

P.18 Delete two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for needless to backup solution.

(2007/04/17)

P.44 Add U8 solution for H/L has differente thermal sensor.

Change Q176 value from CA_MMBT3904.215 to NC_MMBT3904.215 for new solution.

P.44 Delete C62,U139,R2031,R2032,R73 for delete VGA thermal sensor.

P.24 Change MIOB_VDD current from 900mA to 10mA.
NV_DACA_VDD from 135mA to 130mA.
NV_DACB_VDD from 200mA to 130mA.
NV_PLLVDD from 60mA to 35mA+35mA.
IFP_CDI OVDD from 150mA+150mA to 50mA+50mA.
IFPCD_PLLVDD from 35mA to 75mA.
IFP_ABIOVDD from 130mA+130mA to 45mA+45mA.
IFPAB_PLLVDD from 35mA to 75mA for power budget spec.

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P.25 P.26 Change FBA_PLLAVDD from 30mA to 15mA.
ABCP_LLAVDD from 30mA to 15mA.
Change NB8M-GT xx mA to NB8X 15mA
EMI_PLLVDD from 100mA to 75mA
PEI_PLL_VDD from 20mA to 10mA.
VDD33 from 110mA to 50mA.
NV_VDD from 16.25A to 13.37A.
change NB8M-GT : 1.1V(TBD) to NB8X : 1.2V for power budget spec.
Add H_PLLVDD power budget spec 15mA.

P.27,P.28 Add +1_8VRUN power budget spec 1.125A.
change +1_8VRUN from 1.2A to 1.125A for power budget spec.
P.1 Update the PCB P/N.

(2007/04/17)

P.17,P.19,P.20,P.21,P.22,P.23,P.24,P.25,P.26 Change U7A,U7D,U7E,U7F,U7H,U7G,U7C,U7I value from NB8M-GT-B-A2/H to NV_NB8M-GT-B-A2/H.
P.20 Change U82 to NV_ for low board needless it.

(2007/04/23)

P.56 PQ7 Change from SI4800BDY to FDS8880 because the +1_25VRUN load increase.

P.33 Add TP287 for test the RTCRST#.

P.49 Add C1559,TP288 for stable AV mode start.

(2007/04/24)

P.38 Change R715 to NV_ for low board needless it.

(2007/04/24)

P.44 Change U4 from MAX6509HAUK-T+ to G709T1UF for PUR request.

(2007/04/27)

P.44,45,46 Change U132 from 12-PC18402-0000 to 12-SPC1840-0000 for PUR suggest.

(2007/05/07)

P.11 Change D6,R4 from CA_ to stuff all the SKU for Intel suggest.

FOXCONN			HON HAI Precision Ind. Co., Ltd.	
History (1)			CCPBG - R&D Division	
Title				
Size	Document Number			Rev
A3	MS91-1-01			1.0
Date:	Thursday, June 21, 2007			Sheet 65 of 66

MS91 PVT
(2007/05/30)
P.43 Add Polyswitch (F7) and resistor (R2142)_NC co-layout on USB power input of M/B for TUV.
P.48 Add Polyswitch (F8) and change resistor R972 from stuff to NC co-layout on USB power input of M/B for TUV.

(2007/06/01)
P.6,32,60,63 Change RP11 value 33 to NC_33,
C1394 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C1389 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C735 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C730 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
CN64 value BTB_2*10 to NC_BTB_2*10,
Change BOSS5 value BOSS_4x2.8 to NC_BOSS_4x2.8 for lock robson.
for robson function Disable.

(2007/06/05)
P.52,53,54,55,58 Del PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for PVT stage.
P.52 Del net name +3VALW_PWM and +5VALW_PWM becuase del PJ2 and PJ1.
P.53 Del net name +1_5VRUN_PWM and +1_05VRUN_PWM becuase del PJ4 and PJ3.
P.54 Del net name +1_8VSUS_PWM becuase del PJ5.
P.58 Del net name NV_VDD_PWM and PEX_VDD+ becuase del PJ9 and PJ11.
P.43 Change C1398 Pin 1 net name from +5VALW to +5V_USB0_1.
P.48 Del co-layout resistor R971,R973 for level 6 suggest.
P.41 Del TP854 for level 6 suggest.

(2007/06/07)
P.43 Del Polyswitch (F7) and resistor (R2142)_NC on USB power input of M/B for MOR suggest.
P.48 Del Polyswitch (F8) and change resistor R972 from NC to stuff on USB power input of M/B for MOR suggest.

(2007/06/08)
P.1,18 Add three BOM on BOM configuration for Hynix VRAM.
P.38,49 Add option circuit for keyboard auto power on issue.
1> Del TP294
2> Add R2142(NC),R2143(NC),R2144(NC),R2145,R2146,R2147(NC).
P.37 CN32 change from 2N-0050004-FKG0 to 2N-0050006-FKG0 for level 6 suggest.

(2007/06/12)
P.24 Add R2148,R2149 for HDMI leakage issue.
P.30 R/G/B add C1762(NC),C1763(NC),C1764(NC) for EMI suggest.

(2007/06/20)
P.49 LAN controller U138 change from 88E8039 to 88E8036 for EMI fail issue.